University of Southampton

Faculty of Engineering and Physical Sciences

Optoelectronics Research Centre

Silicon-germanium by Rapid Melt Growth for the Silicon-On-Insulator Platform

by

Katarzyna Monika Grabska

Thesis for the degree of Doctor of Philosophy

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Abstract

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Silicon-germanium ($Si_{1-x}Ge_x$) and Ge are widely used in optoelectronics. It is fully miscible across the whole composition range, which allows for the whole spectrum of the band gap to be tuned between the values of pure Si and pure Ge. This versatility is extremely important for photonics applications such as electro-absorption modulators and photodetectors, where the operating wavelength is strongly dependent on the Si content. Traditional SiGe growth allows only a single SiGe composition to be grown across the wafer. On the contrary, Rapid Melt Growth (RMG) offers the opportunity of multiple compositions of SiGe by using just a single Ge deposition step and a single anneal step, as previously demonstrated on the silicon platform. This is made possible by engineering the structural parameters of the RMG structures to enable multiple uniform composition strips of SiGe across the wafer, each with a different, tuneable composition. Furthermore, RMG can be used for the growth of high-quality SiGe material with a smaller number of defects than other growth techniques, which can lead to the fabrication of higher performance active devices. Finally, the simplicity of the fabrication process provides a cost-effective growth method making this concept very attractive.

In this thesis, for the first time, RMG processing was successfully used to demonstrate constant composition SiGe and Ge structures (in range between 65 and 100% Ge) embedded within Silicon-on-Insulator (SOI) substrates. The structures embedded in the SOI platform enable integration to waveguides for the creation of both passive and active waveguide-based devices to form complex Photonic Integrated Circuits (PIC). This first demonstration promises to allow the development of new devices and associated applications with high performance and low cost. The findings of the research will lead to waveguide integration and work on active devices.

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Research Thesis: Declaration of Authorship

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Patents

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Conference Contributions

1. **Grabska K**, Ballabio A, Banakar M, Barzaghi A, Bucio TD, Isella G, Littlejohns C, Nedeljkovic M, Saito S., Gardes F, "Multi composition GeSi tuneable concentration silicon-germanium wire structures for CMOS photonics." IEEE 16th International Conference on Group IV Photonics (GFP), August 2019.
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Chapter 1 Introduction

The rapid technological development of electronic devices and communication networks witnessed in the last few decades has been driven by the increasing number of digital devices and the raising expectations for telecommunication and computing capabilities. We are currently living in the Information Age [1], where technology has grown following the predictions of Moore's law. This law describes an observation of increased (doubled) number of transistors per Integrated Circuit (IC) every two years as illustrated in Figure 1. Moreover, additional exponential formulations often considered derivatives of Moore's law have been used to describe the technological development witnessed over the past few decades in different areas [2]; like for optical fibres which have become a crucial part of telecommunication. Butters' Law expresses an exponential growth in their data transmission speed every nine months which makes the cost of transmitting data exponentially lower [2][3]. Another example of rapid development of computational technology are quantum annealers with doubled number of qubits throughout every year over ten years period as predicted with 'Rose's law'- an example of the 4-qubit is Calypso from 2005 and the 2048-qubit Washington machine in 2015 [3][4].

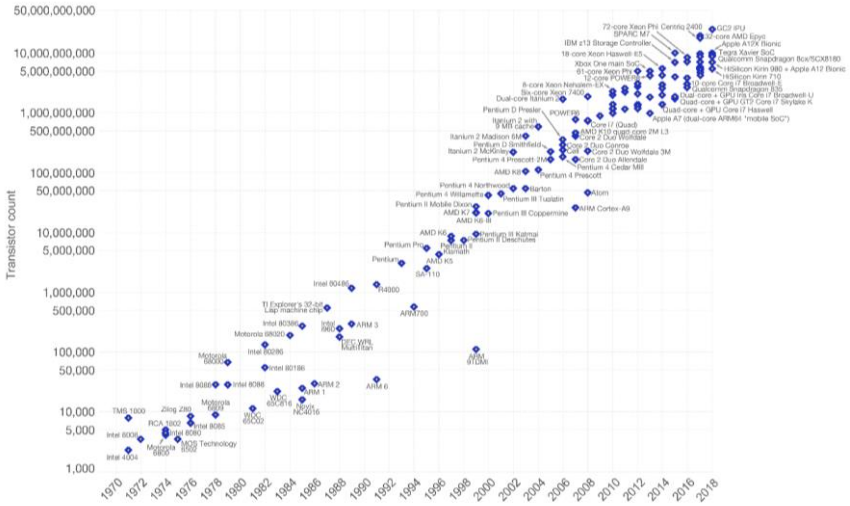


Figure 1 The visualisation of the Moore's Law being an observation about the number of transistors across the integrated circuit (IC) from [3].

The new technological developments have led to an ever-increasing need for data transfer, whilst transferring information at a low cost and retaining high processing speed and transmission rate. Electronic connections based on copper limit the performance of high-speed computers and interconnects, giving space for dramatic improvement through the use of optical connections. The replacement of traditional copper interconnects has proven to be crucial for the efficiency of high-speed data communication for both long and short distances, reducing heat dissipation and losses. A big part of the research on photonics has focused on developing higher data transmission rates, higher processing speed and higher bandwidth for telecommunication and computing systems respectively. A typical target application of silicon photonics has been the data links within data centres operating at 100Gbit/s or 400Gbit/s [5]. Turning point of this research was presented in 2004 as a metal–oxide–semiconductor (MOS) capacitor structure embedded in a silicon waveguide acting as a fast Si-based modulator exceeding 1 GHz [6].This research started a discussion about new possibilities for exceeding the speed of interconnects inside the computer [7].

The next chapter will introduce silicon photonics as a platform of choice for novel optoelectronics solutions highlighting silicon-germanium (SiGe) as a material suitable for high performance integrated devices. It discusses the focus of this project on the development and integration of crystalline SiGe and germanium (Ge) material on the silicon-on-insulator (SOI) platform. The integration is based on a technique called Rapid Melt Growth (RMG)/ Liquid Phase Epitaxy (LPE) [8][9] providing a means to integrate passive and active devices for silicon photonics applications, including high speed optical modulators and detectors, across a small area at a minimal cost.

1.1 Silicon Photonics

Silicon photonics is an evolving technology leading the way for low-cost, high performance applications bringing together the advantages of both photonics and electronics through integration onto the same substrate. Commonly used traditional silicon integrated circuits (IC) industry solutions can be easily adapted for the fabrication of optical interconnects at the chip level. Additionally, the compatibility with CMOS technology allows the integration of electronics and photonics on the same substrate.

Another factor leading to the success of silicon photonics is a high refractive index ratio of vital elements like e.g. silicon waveguide and silicon dioxide cladding (refractive index ratio for Si and SiO2 is 3.5/1.443) leading to smaller device footprint, more chips per wafer and to the realisation of sub-wavelength-sized cavities for photonic crystal structures, high-efficiency grating couplers [5] etc. Silicon technology also allows carrying more data with less power, avoiding the heating problems usually faced by traditional copper-based technology [5]. In addition, Silicon's

transparency at 1550 nm and compatibility with Ge optical modulators and photodetectors make this platform highly suitable for multiple optoelectronics applications and components [1], examples to be listed are optical transceivers [65], sensing applications [11] or LIDAR technology [12].

In 1988 the first company to commercialize silicon photonics was founded, Bookham Technology. The first product was introduced in 2000; it was an arrayed waveguide grating (AWG) multiplexer, integrated with variable optical attenuators (VOA) [13]. A great amount of research on silicon photonics has been conducted since than by international companies such as Melanox [14], HP [15], Luxtera [16] with Cisco [17], Intel [18][19], IBM [20][21], Huawei/ Caliopa [22][23] or Rockley Photonics [24]. The interest of these companies has led to the development of silicon photonics products that are commercially available, including products like transceivers and sensors [24].

1.2 Silicon germanium applications

Germanium (Ge) is an example of a well-established material in electronics, compatible with CMOS technology [11]. Ge and SiGe are highly important materials of silicon photonics especially for the receiving element of the photonic circuits, as they are materials that absorb in the entire telecommunication window from the O (1310nm) to the L (1595nm) wavelength bands. Photodetectors based on Ge materials have high responsivity up to 1550 nm [1][25][26]. Alloys of Si and Ge described as $Si_{1-x}Ge_x$, where the varied composition of Si is denoted by x, have been part of the mainstream CMOS production since 1989, when IBM introduced SiGe as a material of choice for their products to increase computer performance by enhancing speed, simultaneously reducing the power consumption [27].

However, although Ge and Si are compatible materials, the lattice constant difference produces a mismatch of 4.2% that causes problems for fabrication of defect free interfaces between the two materials. The lattice mismatch issues can be partially overcome by implementing buffer layers with a graded composition (from pure Si through multiple compositions of $Si_{1-x}Ge_x$ up to pure Ge) during the growth of the materials [28][29], but the technique is complex, expensive and challenging to implement. As a result, the development of a novel technology that can be used to integrate crystalline Ge/SiGe and silicon with an improved layer quality while minimising the cost and fabrication time is still desirable.

1.3 Rapid Melt Growth for silicon germanium and germanium on Silicon-on-insulator platform

Silicon-germanium ($Si_{1-x}Ge_x$) is fully miscible across the whole composition range, which allows for the whole spectrum of both the lattice constant and the band gap to be tuned between the values of pure Si and pure Ge [1][30]. The versatility of SiGe alloys is extremely important for photonics applications such as electro-absorption modulators and photodetectors, where the operating wavelength is strongly dependent on the Si content.

Moreover, $Si_{1-x}Ge_x$ is a material of interest for high-performance modulator devices working in the C band such as electro absorption modulators (EAM) based on the Franz-Keldysh effect [30][31]. The maintained constant composition and the quality of the $Si_{1-x}Ge_x$ alloys are crucial to determine the energy of the band gap and therefore the operating wavelength of said modulators. Previously reported results for SiGe EAM confirm lower power consumption (calculated modulator power 44 fJ/bit), and increased speed (data rate of 56 Gb/s at 1566 nm), making these devices attractive as building blocks for silicon photonics [31].

Traditional growth methods including various kinds of chemical vapour deposition (CVD) and epitaxy (e.g. Molecular Beam Epitaxy MBE) allow the growth of only a single SiGe composition across the wafer. Therefore, the devices that can be fabricated with these layers are strongly limited to a narrowband wavelength operation, while the simultaneous modulation of multiple wavelengths on a chip is desirable. Hence, the Rapid Melt Growth (RMG) technique has been proposed as a way to achieve the growth of multiple compositions at once with only one non-selective growth step and one anneal step. RMG is a technique, where the SiGe or Ge structures are grown as single crystalline material using the Si seed as a lattice template and a source of Si diffusing into Ge tailored structures embedded into an insulator. The composition of the $Si_{1-x}Ge_x$ alloys can be tuned by combining RMG with especially designed structures due to mentioned full miscibility of these two elements [8]. After the RMG process, trenches with the shape of strips have shown a graded composition with decreasing Si concentration as their length increases away from the seed. However, a constant composition can be obtained when branches are added along the strips. This modified RMG technique has allowed the creation of strips with multiple constant compositions across silicon substrates with a negligible number of defects [9]. The engineering challenges of this process are linked to the precise control of the composition along structures and removing defects within the area designated for the devices.

The silicon-on-insulator (SOI) platform has become the platform of choice for silicon photonics as the fabrication of structures embedded in the silicon overlayer of the wafers enable seamless

waveguide integration between both passive and active devices that can be fabricated simultaneously [26].

The novelty and aim of this work are to fabricate tailored SiGe structures on the SOI platform which, contrary to the silicon platform, are suitable for the integration of passive and active photonic devices. The engineering challenges are described in detailed in Chapter 5, process development.

1.4 Thesis outline

After a brief introduction to the work follows a discussion of background theory with special emphasis on silicon photonics and notable developments in the field. The thesis aims to demonstrate the importance of SiGe and Ge based photonics and the contribution this new work makes, which involves developing the integration of the RMG based Ge and $Si_{1-x}Ge_x$ growth technology on the SOI platform.

Chapter 2 provides a theoretical background about Si, Ge and $Si_{1-x}Ge_x$ properties along with applications of these materials. Additionally, a literature review of relevant techniques suitable for the material growth is presented. This leads to justification of the RMG technique development being the scope of this work.

Chapter 3 contains an overview of methods used for fabrication and characterisation of the RMG integration work and process development. Understanding of advantages and disadvantages of those is essential to explain choices made for the fabrication of RMG structures on SOI.

Chapter 4 explains motivation of the project with a special focus on waveguide integration. Further part provides masks and experiments design for RMG tailored structures on the SOI platform.

Chapter 5 contains description of work done on the process development for the experiments necessary for SOI integration. This chapter also contains the characterisation and discussion on results obtained for RMG structures embedded within the SOI platform.

Chapter 6 summarizes the PhD thesis with discussion and conclusions on the results of all work carried out. This chapter also contains the possible applications and future work based on findings explained in previous chapters.

Chapter 2 Theoretical background and literature review

This chapter contains theoretical background regarding a subset of semiconductors (Si, SiGe and Ge), which are crucial for this thesis, in Section 2.1. Understanding the theoretical background behind the growth process at a fundamental level will allow planning of processing for optimal photonic devices and therefore Section 2.2 is describing it. Section 2.3 introduces Rapid Melt Growth (RMG) background with an overview of materials deposition and growth methods traditionally used for fabrication of silicon photonics or electronic devices. Section 2.4 describes the hydrogen role in the grown film. Finally, Section 2.5 covers the surface tension topic.

2.1 Properties of Silicon, Germanium and $Si_{1-x}Ge_x$ alloys

Si and Ge are group IV elemental semiconductors with the electron structure as shown in Figure 2. Si is the chemical element with atomic number 14, whereas the Ge atomic number is 32, with electron configurations: $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^2$ and $1s^2\ 2s^2\ 2p^6\ 3s^2\ 3p^6\ 4s^2\ 3d^{10}\ 4p^2$, respectively. The higher number of electrons and filled d-orbital result in a larger atomic radius of the Ge atom and smaller band gap than Si. Additionally, Ge possesses both higher electron and hole mobility than Si [1][2].

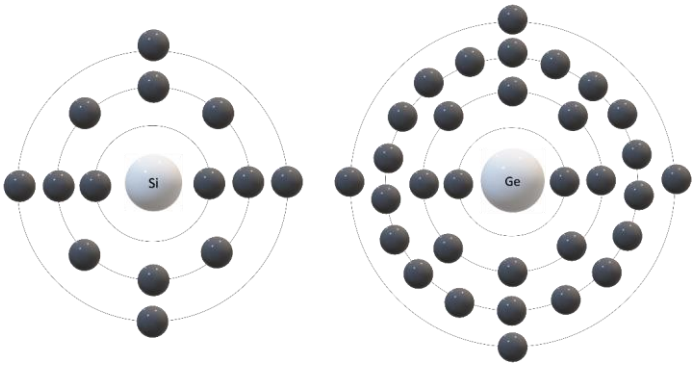


Figure 2 Si and Ge are group IV elements with atomic numbers of 14 and 32 respectively, with 4 valence electrons.

The most significant properties of Si and Ge for this thesis are gathered in Table 1 for a clear comparison between these two materials. The band gap and lattice constant can be tuneable by the RMG process which will be detailed in later parts of this thesis. The difference in melting point of these two materials allows RMG to occur, which will be expanded in later parts of this Chapter.

Finally, the hole mobility and electron mobility influence applications of semiconductors and have an impact on their success in electronics, e.g. by affecting operation speed or the circuit operating frequency [1].

Table 1 Important properties of Si and Ge reproduced from [3].

Property	Si	Ge
Band gap (eV)	1.12	0.66
Lattice constant (Å)	5.43	5.66
Melting point (°C)	1415	937
Hole mobility ($cm^2 (V\cdot s)^{-1}$)	450	1900
Electron mobility ($cm^2 (V\cdot s)^{-1}$)	1400	3900

For the fabrication of Si, Ge or SiGe based devices, the compatibility with the CMOS production line results in a major advantage over III-V group semiconductors, traditionally used in electronics but difficult to integrate with the Si platform [4]. Additionally, the higher carrier mobilities of Ge compared to Si could be given as a major advantage; however, the lack of a stable germanium oxide (GeO_2) is the main reason for the prevalence of Si as the prominent semiconducting material (Si forms a very stable native oxide, SiO_2). As mentioned in Chapter 1, the difference in refractive index of materials and their oxides is crucial for multiple applications including the waveguide fabrication, and Si has a strong refractive index contrast with its native oxide. Refractive index of SiGe alloys is highly dependent on the composition, although it will not be described in more detail as not being the main objective of research described within this thesis.

All of these properties are supporting the suitability of Si for photonics, however this material has much more to offer, including high thermal conductivity and high optical damage threshold, where both values are around 10 times higher than for GaAs, a commonly used III-V semiconductor [5].

2.1.1 Energy band gap

The energy band gap represents the minimum energy needed for an electron to move from the valance band to the conduction band. Semiconductor materials can be divided into direct and indirect band gap materials, as is shown in

Figure 3~~Figure 3~~. In direct band gap materials, the bottom of the conduction band and the top of the valance band correspond to the same value of electron momentum. However, in indirect band

gap materials, an additional change of momentum is required to achieve the transition from the valence band to the conduction band, thus resulting in a two-step phenomenon linked to a lower probability of occurrence compared to direct band gap materials.

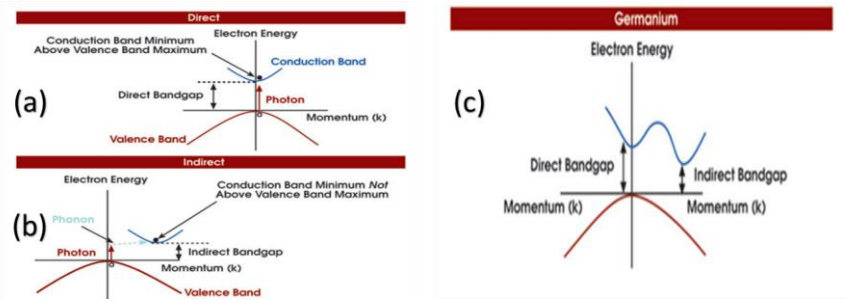


Figure 3 The band diagram for semiconductors: (a) direct band gap semiconductor diagram with the conduction minimum aligned in *k*-space with the valence band maximum, (b) indirect band gap semiconductor diagram with conduction band minimum shifted in *k*-space with respect to the valence band maximum, (c) Ge band diagram; reproduced from [6].

Si and Ge are indirect band gap materials, where the indirect band gap is equal to 1.11 eV for Si and 0.66 eV for Ge (at 300 K). Close to this indirect band gap, Ge possesses a direct band gap with slightly higher value of 0.8 eV. Examples of direct band gap materials like GaAs or InAs [7] are shown next to Si and Ge in Figure 4. In Figure 4, the absorption coefficient, α, of common semiconductors (including Si and Ge and those from the III-V group) is plotted as a function of Photon energy (corresponding to the wavelength).

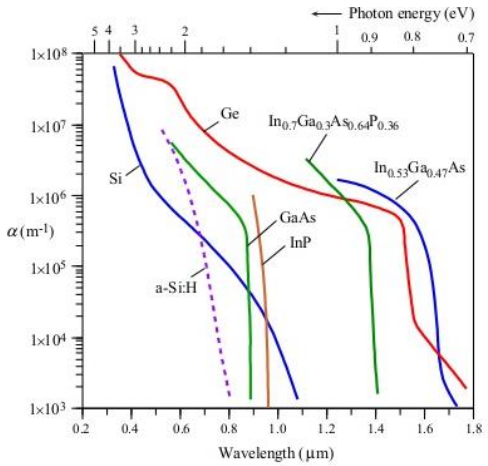


Figure 4 Absorption coefficient and band gap of different semiconductors for a range of wavelengths [8]. This plot is revealing the nature of their band-structure and band gap energy.

As shown in Figure 4, the value of the direct band gap of Ge corresponds to the telecommunication wavelength of 1550 nm, resulting in it being a suitable material for Electro-absorption Modulators (EAM) [5] and photodetectors. The band gap of Si (mentioned 1.1 eV) [8] corresponds to the optical absorption band edge at a wavelength of 1120 nm. Therefore, for $\lambda > 1120$ nm Si is transparent (applied e.g. for Si waveguides) in contrast to the range of $\lambda < 1120$ nm, where Si is highly absorbing (used e.g. in photodetectors). The window of low-loss wavelength (when Si is transparent) is expanded up to 7000 nm making Si a material of choice also for mid-infrared (MIR) applications [9]. The addition of Ge to Si and formation of the range of $Si_{1-x}Ge_x$ alloys, shifts the absorption edge from λ = 1120 nm to 1300 nm, or even to 1550 nm. The full miscibility of Si and Ge allows the tunability of the band gap between that of pure Si and that of pure Ge. The theoretical study of the band gap of these alloys was conducted as early as 1958 [10]. Afterwards, experimental results for low temperature band gap were fitted with analytical equations [11]. Equations 1 and 2 describe the value of band gap for varied compositions of $Si_{1-x}Ge_x$, where the critical content of Ge is x=0.85. For the Ge content x lower than 0.85 as described in Equation 1, the band gap is closer to the Si band gap value whereas with increasing value of x, the conduction-band is more like that of pure Ge and is even called "Ge-like" and described as in Equation 2 [12, 13].

$$E(x) = 1.155 - 0.43x + 0.206x^2 \text{ eV} \quad \text{(Equation 1)}$$

$$E(x) = 2.010 - 1.270x \text{ eV} \quad \text{(Equation 2)}$$

Based on equations 1 and 2, the graph for the SiGe alloy band gap can be drawn, as shown in Figure 5. The shape of a band gap curve for Ge content under *x*=0.85 is parabolic for unstrained SiGe, whereas for the Ge content above *x*=0.85 the energy band gap is linearly dependent on the composition. The band bad curve for strained SiGe with the Ge fraction x < 0.3, by contrast, is linearly dependent on the SiGe composition.

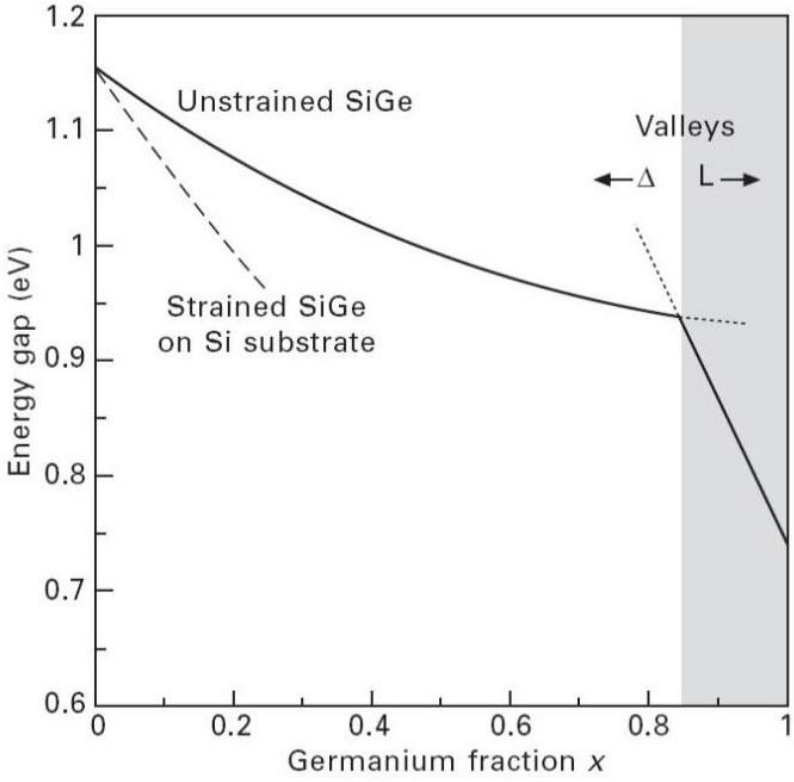


Figure 5 The band gap for the spectrum of $Si_{1-x}Ge_x$ alloys based on calculations expressed in equations 1 and 2 [12].

The valleys shown in Figure 5 correspond to the Brillouin zones for Si and Ge unit cells and will be further explained in 2.1.2.

2.1.2 Lattice constant

The lattice constant defines the distance between the units of a crystal lattice cell in three-dimensional space and depending on the shape of the cell, it can have either one, two or three different values. Similarly to many III-V group materials, structures of Si and Ge are defined as the face centred cubic (fcc) unit cell, also known as a diamond structure as shown in Figure 6. For the fcc structure, all dimensions of the lattice constant are equal and described as *a*.

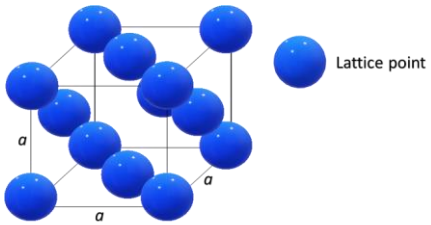
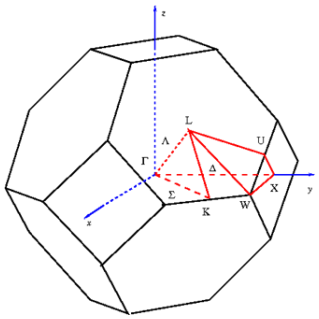


Figure 6 The diagram of fcc crystal structure, where the lattice points are located in the corners of a cube and in the centre of each face; a is a lattice constant.

The fcc structure can be represented in the k-wave vector coordinates which is called the Brillouin zone. As shown in Figure 7, the main symmetry points of the Brillouin zone are relevant for the shape of a band gap curve for $Si_{1-x}Ge_x$ alloys. This representation is shown in Figure 7 with the main symmetry points defined across the Brillouin zone. The conduction-band minimum (CBM) occurs at the L-point in the Brillouin zone in Ge and near the X-point in Si [14].



Symmetry points (u,v,w) $[k_x,k_y,k_z]$

Γ: (0,0,0) [0,0,0]

X: (0,1/2,1/2) $[0,2\pi/a,0]$

L: (1/2,1/2,1/2) $[\pi/a,\pi/a,\pi/a]$

W: (1/4,3/4,1/2) $[\pi/a,2\pi/a,0]$

U: (1/4,5/8,5/8) $[\pi/2a,2\pi/a,\pi/2a]$

K: (3/8,3/4,3/8) $[3\pi/2a,3\pi/2a,0]$

Figure 7 The Brillouin zone for the fcc unit cell with the characteristic symmetry points and their wave vectors [15].

The difference of lattice constant between Si and Ge, 0.5431 nm and 0.5658 nm respectively, causes a lattice mismatch with calculated value of 4.2% on the interface. For $Si_{1-x}Ge_x$ alloys, the lattice constant depends on the Ge composition with values obtained between those for pure Si and pure

Ge. The lattice constant of $Si_{1-x}Ge_x$ alloys can be calculated using Vegard's rule [16] described with Equation 3:

$$a_{Si1-xGex} = a_{Si} + x(a_{Ge} - a_{Si}) \quad \text{(Equation 3)}$$

where *a* is the lattice constant for Si, Ge or $Si_{1-x}Ge_x$ and *x* describes the Ge content.

The lattice constant parameters for varied Ge content, *x*, are included in Table 2, showing proportional trend across the whole range of the Ge content.

Table 2 The Ge content x in $Si_{1-x}Ge_x$ alloys and corresponding values of the lattice parameter [17,18]. A proportional relationship as predicted from Vegard's rule is observed for the whole range of x values.

Ge content, *x*	Lattice constant $Si_{1-x}Ge_x$, *a* (nm)
0	0.5431
0.25	0.54825
0.5	0.55373
0.75	0.5596
1	0.56575

The lattice mismatch strongly enhances the probability of crystal defects in Ge layers grown on Si [17], which typically inhibit the resulting device properties such as dark current and responsivity. Nevertheless, a great number of high-performance active devices based on Ge have been developed using epitaxial Ge grown directly on Si, which will be explained in detail in 2.2.

2.2 Ge and $Si_{1-x}Ge_x$ growth on Si

The lattice mismatch between Ge and Si is considered as a source of strain energy which causes deformation of the film and leads to the formation of several defects, especially on the interface between these materials [19]. As shown in Table 2, the lattice constant is varied for different SiGe composition which is also causing defects on the interface between SiGe and the Si substrate. For the simplicity of this Chapter, only growth will be described in detail on the example of pure Ge as the principle analogical to SiGe growth. Values of the SiGe lattice constant closer to the one of Si are used to minimised undesirable lattice mismatch e.g. as buffer layers which will be mention further on. Dislocations and twinning defects have an impact on the smoothness of the surface or the continuity of the layer, especially in the form of threading dislocations terminated at the

surface. Moreover, the further fabrication process e.g. wafer bonding [1] or selective etching can be interrupted if the number of defects is higher than the tolerance of the process; therefore, defects can impact the yield of the fabrication process [2]. The performance of photonics devices is also related to the number of defects including the lifetime of devices which has been shown to be extended with a decreased number of defects in the device material [1][3][20]. During the growth of Ge on Si, its lattice spacing will keep changing to conform to the Si lattice constant, however, a defect-free strained Ge on Si was demonstrated only for thickness in a range of 4-10 nm [19]. Above this value, the lattice mismatch causes increased stress within the grown layer and more defects. The defects are a mechanism for relieving the accumulated strain energy.

The fundamental modes of film growth can be distinguished as shown in Figure 8.

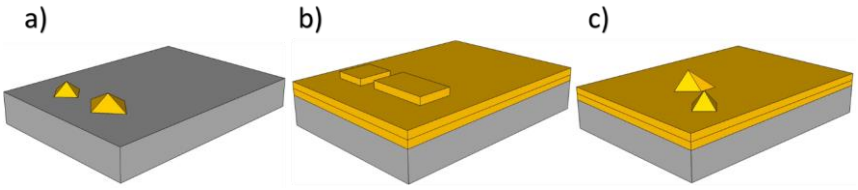


Figure 8 Basic modes of film growth: (a) Volmer–Weber mode; (b) Frank–van-der Merwe mode; (c) Stranski–Krastanov mode.

The Volmer-Weber mode corresponds to the situation where 3D islands of the material are formed directly on the substrate without any 2D layer underneath [20]. The Frank-van-der Merwe mode is a mode of the film growth layer by layer without island formation. This mode is typical for materials with perfectly matching lattices which is mostly relevant to homoepitaxy [21]. The Stranski-Krastanov mode corresponds to the two-step growth when 2D layers are formed up to certain critical thickness subsequently followed by formation 3D islands [22]. Firstly, to initiate the growth, a source of atoms or molecules in either liquid, solid or gaseous state is required. To build up a layer, a condition of lower chemical potential of the desired film in relation to the particles of the substrate must be conserved. The chemical potential describes how much energy is needed to join single particles to the material layer. In the situation with two materials of the same chemical potential, nothing would grow.

The strain energy can be determined by using Equation 4, where the strain energy increases proportionally to the thickness (t) of the Ge growth,

$$Estrain = \lambda A t \left(\frac{\Delta a}{a}\right)^2 \quad \text{(Equation 4)}$$

where λ is the biaxial elastic modulus, Δa is the forced change in lattice constant, a is the unstrained lattice constant, A is the area and t is the thickness of the film.

Over the critical thickness mentioned for Ge on Si growth, the probability of dislocations formed at the interface increases. This is leading to the formation of Ge islands and the reduction of the elastic energy of the surface as shown in Figure 9. The shown growth system is typical for Ge-on-Si thin heteroepitaxy, with the transition between 2D layer growth and 3D island growth [22, 23].

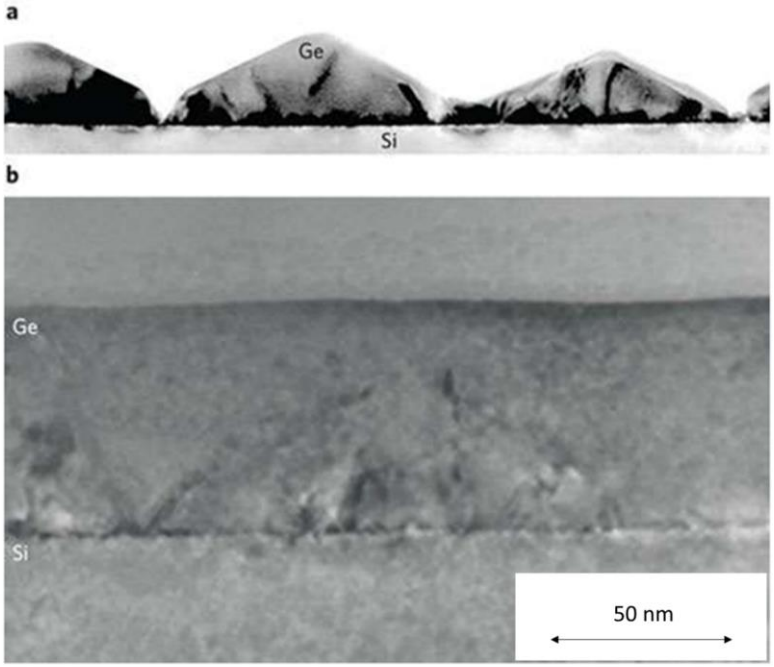


Figure 9 Transmission electron microscope cross-sections of Ge-on-Si layers for Ge epitaxial growth at different temperatures, Stransky–Krastanov growth of Ge-on-Si in an ultra-high vacuum CVD reactor at 550˚C and 350˚C (a, b respectively), reproduced from [24]. The thickness of the Ge layer shown here is 60 nm.

The mode of the crystal growth is dependent on the wetting mechanism and the surface strain energy [25]. The mechanism of growing Ge layers is shown in Figure 10.

The first monolayer of Ge on the top of Si (Figure 10a) and several further monolayers (Figure 10b) are characterised with the strain associated to the 4.2% lattice mismatch between Ge and Si. A wetting layer is firstly created on the surface of the substrate. As the film grows above the critical thickness, the strain energy becomes too large for the Ge to maintain its compressed form and therefore defects form to relieve the strain, supporting the growth of islands instead of smooth layers [26].

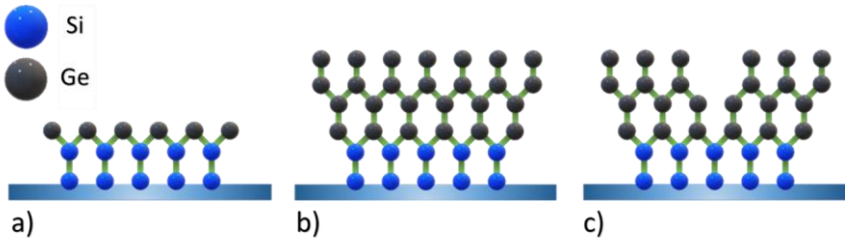


Figure 10 Cross-section atomic view of stages of the Ge-on-Si growth; a) the wetting layer, b) growth below the critical thickness, c) thickness over the critical thickness when dislocations and other defects occur.

The stress caused by the lattice mismatch between Si and Ge releases lattice dislocations which propagate throughout the Ge film in the form of threading dislocations. It is desirable to reduce the Threading Dislocation Density (TDD) in order to reduce the device dark current, the main source of noise in the resulting devices [27]. Furthermore, defects act as generation and recombination centres for carriers, and therefore acceptor-like dislocations in the Ge layer will form band barriers and reduce the responsivity of photodetectors [27]. The most widely used methods for measuring TDD are plan- view TEM and selective defect etching [12]. Reported typical values for Ge on Si are in the range from $2x10^{6}$ to 10^{10} cm^{-2} [19].

2.3 Ge and $Si_{1-x}Ge_x$ on Si growth techniques

A variety of crystalline Ge/SiGe-on-Silicon and Ge/SiGe-on-insulator (GOI/SGOI) fabrication techniques have been investigated for photonics devices in order to reduce material defects and improve the performance of the final device. The fabrication of high-quality and large-scale SGOI and GOI is also highly desirable for CMOS integrated circuits to alleviate some of the limitations of Si only based devices due to its wide band gap, especially important for wavelengths above 1.1 µm [28]. The addition of Ge to Si allows decreased size or lower power consumption of devices. Ge also creates a bridge between silicon photonics and III-V materials [29]. The quality of an interface between layers can vary with the method used for material growth, so in this section the main SiGe and Ge growth techniques are introduced with a focus on the well-established epitaxy and Chemical Vapour Deposition (CVD) methods.

2.3.1 Molecular beam epitaxy

Molecular beam epitaxy (MBE) is one of the well-established methods widely used for depositing layers or multilayers of semiconductors including complex structures like multilayer quantum wells [30]. The MBE technique grows material films by heating a solid crystalline source which will firstly sublimate and later condense on a substrate. This technique provides a high-quality film with the highest achievable purity over other methods, but the growth rate is slower due to an ultra-high vacuum (UHV) of the order of 10^{-8} Pa needed to obtain growth. Moreover, SiGe growth with a constant composition is more complicated because of a melting temperature difference between Si and Ge [31]. Well controlled MBE techniques can be used for reducing the threading dislocation density (TDD) in Ge layers, which was reported as early as 1984 with a graded SiGe buffer between Si and Ge [31]. A methodology using SiGe buffer layers was developed by the Fitzgerald's group over many years to demonstrate Ge films with threading dislocations of $< 2\times10^{6}$ cm^{-2} in 2006 [32]. This work contains a plethora of methods for defects, strain and roughness reduction like using a changeable temperature for specific SiGe composition growth, or Chemical Mechanical Polishing/ Planarization (CMP). MBE based Ge-on-Si growth with an additional annealing (700˚C, 30 minutes) was demonstrated as another possibility for lowering TDD (1×10^{7} cm^{-2} in 1989) [44]. In 2004, Liu et al. [33] developed the MBE process of Ge growth below 450˚C. This technique was used shortly after for fabrication of low temperature p-Ge/n-Si photodetectors for silicon-based photonics [34]. The very low defect concentration and a layer by layer growth mechanism are suitable for the fabrication of quantum wells [30], single crystal thin films or superlattices [3]. However, the cost of set-up is higher than other techniques and the growth rate is slower than comparable growth methods [4]. Finally, in order to achieve a good quality film growth, an extremely flat substrate surface is required. Nevertheless, in spite of higher cost, MBE is commonly used especially for fabrication of III-V materials and for all the applications where the higher cost of fabrication can be balanced by beneficial properties of the resulting material [4].

The ability to grow only one defined SiGe composition across the wafer and the relatively complicated and expensive fabrication (multilayers and multiple depositions) are the main disadvantages of MBE for SiGe layer growth.

2.3.2 Chemical Vapour Deposition

Another technique of SiGe/ Ge growth is the widely used Chemical Vapour Deposition (CVD) where the combination of gases, or even one gas, are reduced or decomposed which results in film deposition on the surface of the substrate [1]. Ge-on-Si growth using CVD started as early as 1981 with GeH_4 in H_2 atmosphere [47]. Firstly, a range of high temperature processes (600-900 ˚C) was used to form crystalline material. Lower temperature processes (500-600 ˚C) were also

demonstrated but only for films with a thickness in 1-2 µm range; below 1 µm thickness islands of material were created instead of smooth layers [47]. In order to decrease the number of dislocations, a graded SiGe buffer layer, post-process annealing, and CMP methods are used for CVD based materials. SiGe layers deposited with UHV/CVD were used as a buffer multilayer SiGe structure to achieve a lower dislocation density Ge structure on the top. To decrease the number of TDD within Ge layer from 10^7 to 10^6 per cm^2, an additional CMP step was implemented for buffer layers after reaching 50% Ge content within SiGe [48]. As SiGe buffer layer processing is well established, examples of its application for development of other materials, like GaAs deposited using Metal-organic CVD (MOCVD), were also demonstrated [49]. However, buffer layers are not desirable because of decreased uniformity along the thickness of the layer which either impacts properties of the miniaturised devices or is adding additional volume.

Nowadays, many kinds of CVD can be distinguished; based on a difference in pressure (from Atmospheric Pressure CVD (APCVD), Low Pressure CVD (LPCVD) [50] to Ultrahigh Vacuum CVD (UHVCVD)), character of vapour, heating method or plasma method like Plasma Enhanced CVD (PECVD). Reduced Pressure CVD (RPCVD) is commonly used for Ge growth [51]. The PECVD and LEPECVD [52,53] will be described in Chapter 3 as techniques used for the fabrication.

2.3.3 Rapid Melt Growth

Rapid Melt Growth (RMG), also known as Liquid Phase Epitaxy (LPE), is a further technique used for SiGe/Ge-on-Si or Ge-on-SOI growth. The origins of RMG in the semiconductor industry go back to 1960 for crystal growth of III-V semiconductor materials [35][36], which were commonly used for multiple applications like solar cells, laser diodes, detectors, and LEDs [37][38][39]. RMG has become a potential method for Ge and SiGe relatively recently, from 2004 [40]. Currently, various work based on RMG can be found across several research groups for GOI and SGOI growth [41][42][43].

The RMG process requires two different materials, e.g. Si and Ge, it is called heteroepitaxy and it is possible due to the difference between melting temperatures of Si substrate and Ge (melting points: Si - 1410 °C, Ge - 938 °C) [25]. The Si substrate with Ge structures propagating onto an insulator layer (and encapsulated in an insulator) is heated above the Ge melting point and Si diffuses from the seed area into the melted Ge structures. After the temperature peak is achieved, the system is subsequently cooled and SiGe is regrown from Si seeds. The higher melting point of the Si seed assures the solidification of the high Si content SiGe melt into a crystal with a lattice close to the Si seed. This solidification happens earlier than for pure Ge which enables the recrystallization to start in the seed area with the solid/liquid regrowth front propagating along the Ge features resulting in a single crystal growth. It should be mentioned that Si diffuses from the

seed until the solidification concentration is reached for an adequate temperature as shown in Figure 11. Following the phase diagram in Figure 11, Si is preferentially absorbed at the regrowth front into the solid depleting the liquid phase of Si leading to pure Ge at the end of the strip. This way of crystallisation minimizes the lattice mismatch due to the graded concentration of the SiGe along the strips.

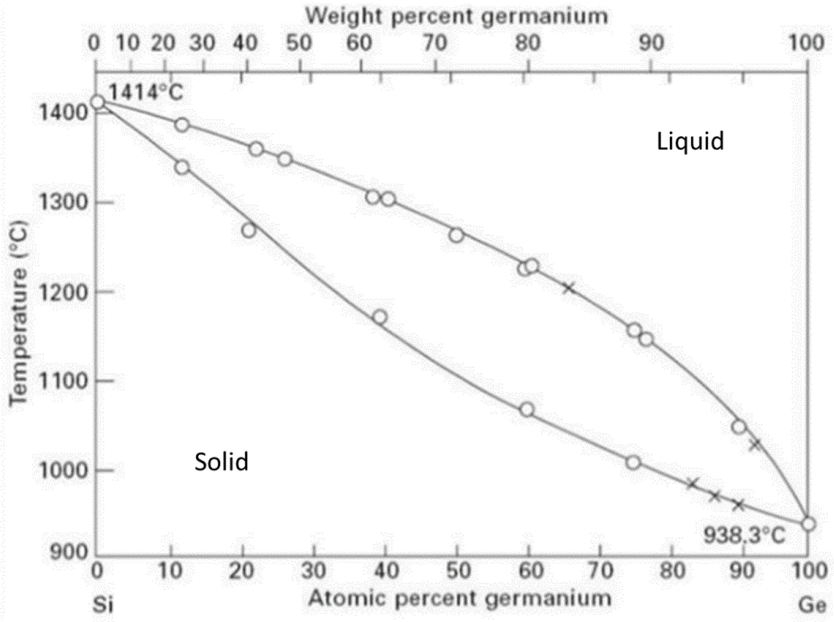


Figure 11 The phase diagram of the SiGe alloys, where L stands for liquid, crosses and circles correspond to different data sets used to construct the diagram. The top line of the curve is called liquidus and the bottom one is called solidus. The diagram was reproduced from [12].

The temperature range of the solidification process depend on the composition of $Si_{1-x}Ge_x$ alloys and can be described with solidus and liquidus lines of the phase diagram as shown in Figure 11. The alloys are heated to the temperature above the liquidus line, when the whole volume is liquid, and subsequently cooled to the fully solid state, with temperatures below the solidus line.

The defects across Ge/ SiGe strips are terminated on the interface with the insulating layers by the process known as the epitaxial necking [44,45]. This method provides a smaller defect probability along the structures because most of defects will be concentrated in the seed area. The principle of the mechanism is shown in Figure 12. The low-quality material found near the seed area is not used in later device fabrication.

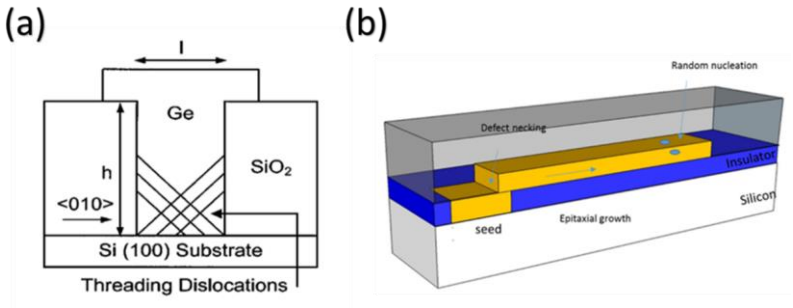


Figure 12 Epitaxial growth within the RMG structure; (a) diagram of the seed area showing the epitaxial necking mechanism [44], (b) cross-section of RMG growth mechanism showing the direction of the growth and the region of random nucleation.

An overview of the processes leading to the fabrication of RMG- based SiGe/ Ge structures is shown in Figure 13 for processing on a Si substrate.

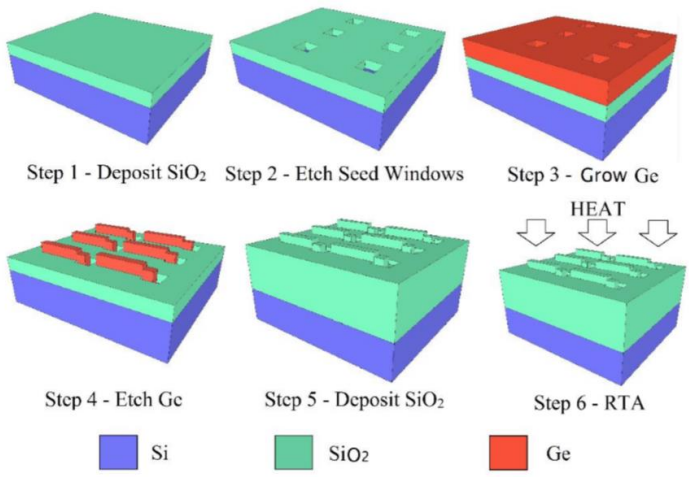


Figure 13 The RMG process for Ge structures on a Si substrate. Step 1- deposition of an insulator (e.g. SiO_2) on a Si substrate, Step 2- a patterned layer of insulator is etched to access the Si underneath, Step 3- Ge growth by any non-selective method, Step 4 -Ge structures are etched with preserved access to the Si seed, Step 5- deposition of an insulating capping layer, Step 6: Rapid Thermal Anneal (RTA). Reproduced from [17, 45].

The first application of RMG for no defect single crystalline Ge, performed in 2004, was based on UHV/CVD used for the non-selective Ge layer deposited on the top of an insulator with etched Si seed windows and Ge features [40]. This research was followed by work from another group to show a quality dependence on increasing width of Ge strips and to investigate the Ge composition along changeable distance from the Si seed [46]. The results from this work are shown in Figure 14 with visible limitation for the quality of Ge strips; only 3 µm wide strips and shorter than 70 µm were fabricated without major defects [46][47].

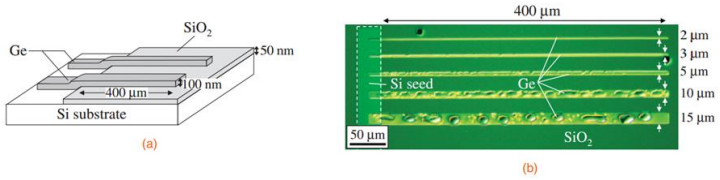


Figure 14 (a) Schematic structure and (b) optical micrograph of the sample [substrate: Si(100)] after RTA (1000° C, 1 s) reproduced from [47].

Research on the width limitation resulted in an increase to 5 µm width SiGe strips with Lanthanum (La) as an insulating layer [48]. However, La is not compatible with the CMOS production line creating issues with standard processing. Nevertheless, this research shows the dependence between the insulator layer and surface tension of SiGe RMG structures. Another group researched the influence of varied initial SiGe composition on the Ge final composition profile along melted structures for the SGOI growth. The outcome of their experiments confirmed the similarity between profiles along the length of strips for all initial compositions of SiGe in the melt (composition of first not selective growth/deposition) [49]. Results of this research are shown in Figure 15.

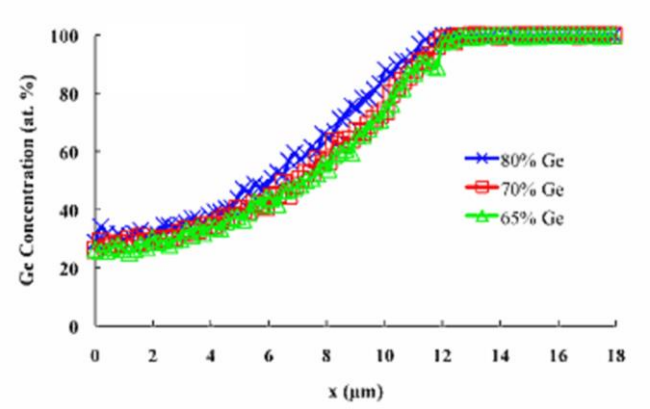


Figure 15 The dependence of the composition profile along the length of the strip, x, for a variety of initial compositions of SiGe [49].

Another stage of RMG-based SiGe processing was the introduction of the multilayer SiGe strips and presenting the dependence between the Ge composition and cooling rate (CR). The outcome of this experiment shows the impact of cooling rate and the strip length on the final composition of the strips [41][50]. Results of this research are shown in Figure 16 and Figure 17.

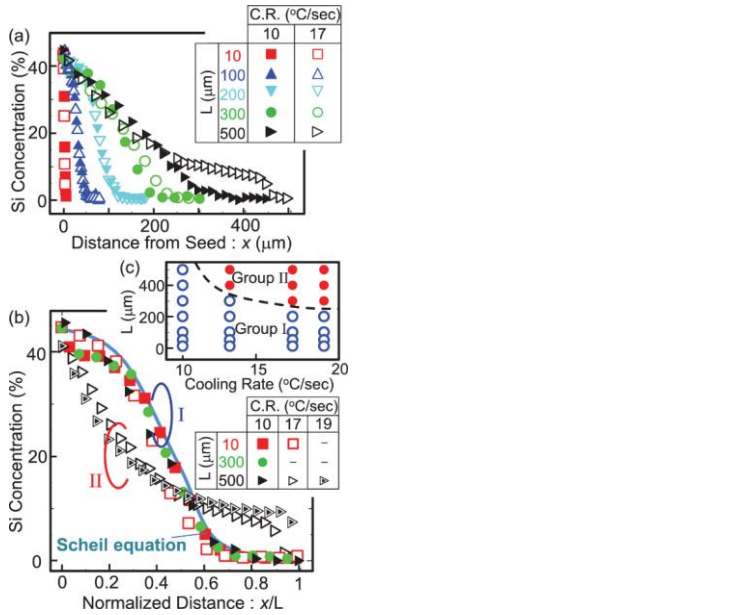


Figure 16 Dependence of the SiGe composition along strips for changeable cooling rate reproduced from [50].

Nevertheless, other experiments confirmed the profile independence of peak temperature anneal time [41].

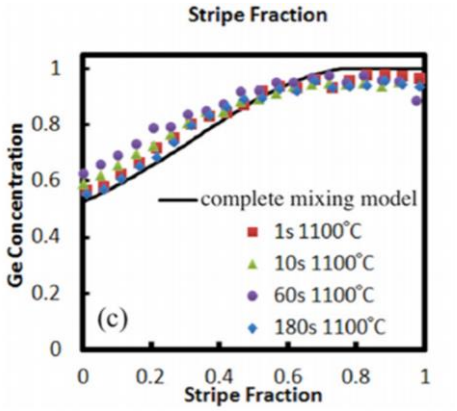


Figure 17 The comparison of SiGe composition profiles after RMG at a range of anneal times, reproduced from [41].

In 2014, waveguide integrated RMG based photodetectors were demonstrated on Ge stripes [72]. A constant composition within strips of SiGe is desirable to fabricate devices so the RMG process was developed further to maintain constant composition of SiGe within designated regions [17]. This result was obtained by forming crucibles shaped as tailored structure (called "tree-like structures") with cooling branches along the SiGe strips as shown in Figure 18 for Si platform.

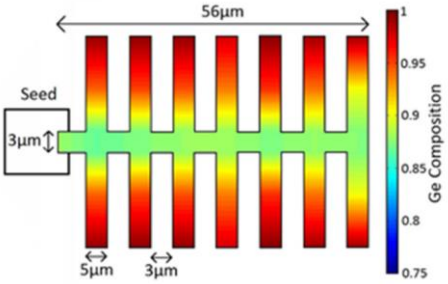


Figure 18 Tailored RMG structure on Si platform, reproduced from [1].

The RMG method was confirmed to be a method of choice for the growth of good quality SiGe material, with tuneable composition and, having low defect density. This is unique among the growth techniques mentioned. Crucially, controlled growth of the multiple composition of SiGe across a single structure grown on an SOI substrate is desirable and the first ever attempt is described in Chapters 4-6.

2.4. Hydrogen within Ge structures

Impurities have an impact on the continuity and quality of the layers of Ge or even SiO_2 obtained from each growth technique. A commonly occurring example of an extrinsic impurity within Ge or Si films is hydrogen, which is easily incorporated into the growing material during the growth or later processing [14]. The interstitial hydrogen is amphoteric in Si which means it can act as an acceptor (in n-type materials) or a donor (in p-type materials) of electrons. However, in the Ge lattice hydrogen is usually an acceptor [14]. Amphoteric character of hydrogen increases the chance of incorporation into layers of Ge film on insulator.

Hydrogen exists within the Ge lattice as hydrogen atoms or ions. The three forms of hydrogen can be distinguished as the following: H^+ which means proton only without electron, H^0 which is a neutral hydrogen atom and H^- describing a standard hydrogen atom with an additional electron. Possible configurations of fcc unit cells with incorporated hydrogen are shown in Figure 19.

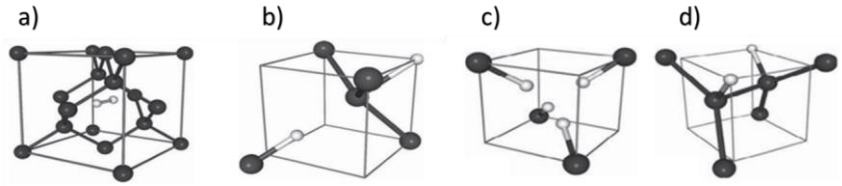


Figure 19 The positions of the hydrogen within the fcc unit cell, a) H_2 dimer rotating inside the diamond lattice, b) H∗2 defect with one hydrogen hidden within the structure, c) proposed structure for quadrihydrogen-vacancy (VH4) complex, d) proposed structure for hydrogen-saturated interstitial (IH2) complex, reproduced from [14].

Hydrogen is confirmed to be a reason for decreased performance of Ge based devices e.g. detectors, due to increased leakage current resulting in reduced sensitivity or increased risk of breakdown of the device [1].

The hydrogen presence can cause the voids within a layer because of hydrogen out-diffusion associated to higher temperature treatment [14]. An example of a high temperature process is annealing which is used for e.g. densification of layers or Rapid Thermal Anneal (RTA) for dopant activation or RMG. Due to the presented issues linked to hydrogen within the layer, in the literature, a possible method of dehydrogenation of Ge is listed as post deposition anneal at 300˚C for 30 min [14]. Hydrogen is also incorporated into SiO_2 films grown by PECVD [17], which can cause problems during subsequent thermal processes where the hydrogen can outgas into other layers. Hence it is often desirable to remove hydrogen from the SiO_2 layer, particularly for the RMG process described later. It has been shown that outgassing of hydrogen from SiO_2 can be performed at 700 ˚C for 30

minutes and the amount of hydrogen removed can be tested through the thickness measurement (e.g. ellipsometry) of the layer before and after annealing [17].

2.4 Surface tension

The surface tension is a cohesive force among liquid molecules tending to obtain a minimum surface area for a given volume e.g. shape of the sphere [58]. The liquid would often tend to obtain this shape after anneal/ melt. A way to avoid voids within the solidified layer is to introduce an optimized shape with lower surface tension.

As was reported in the literature, the surface tension and the contact angle (wetting angle) of the liquid Ge depends on the material below the Ge layer [41]. The possible shapes of the droplets and contact angles are shown in Figure 20. The contact angle is the angle between a surface and the drop.

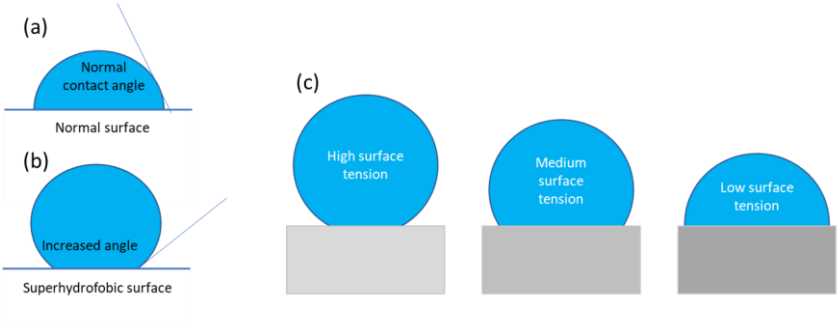


Figure 20 Contact angle for a water droplet on a) normal surface, b) superhydrophobic surface and c) shape of the drops for various levels of surface tension resulting in different contact angles.

The change of the material located underneath the Ge layer can be also important for RMG processing. The decrease of the observed surface tension within the SiGe structures (resulting in the possibility of wider dimensions of the device without visible voids or rounded shape in corners) was reported by using Lanthanum oxide La_2O_3 instead of the most commonly used insulator- SiO_2 [48]. The GOI strips of different widths after the anneal process are shown in Figure 21.

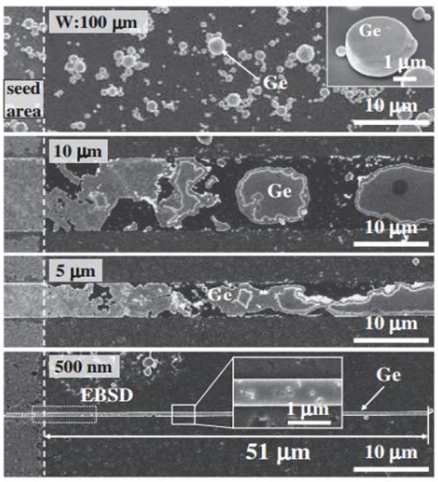


Figure 21 SEM images of Ge strips formed by RMG on SiO_2 with a cap thickness of 500 nm SiO_2 [40].

The rounded shape of the material (Ge), and breaks within the wire structures were explained by the deformation of the SiO_2 capping layer happening during the viscous flow of the RMG process. The high interface energy between liquid Ge and the solid SiO_2 causes the capping layer deformation and Ge aggregation, as the cap layer is softer at higher temperatures. The increase of SiGe/Ge wire deformation was observed with increased width of the wires. The main conclusion of this research work is the width constraints due to the interaction between the liquid Ge and the insulator layers interfaces [32].

The change of the shape of structures can be observed for both the melting process and cooling time [35], shown in Figure 22. The capping shape can be also affected according to the change of the liquid structures underneath.

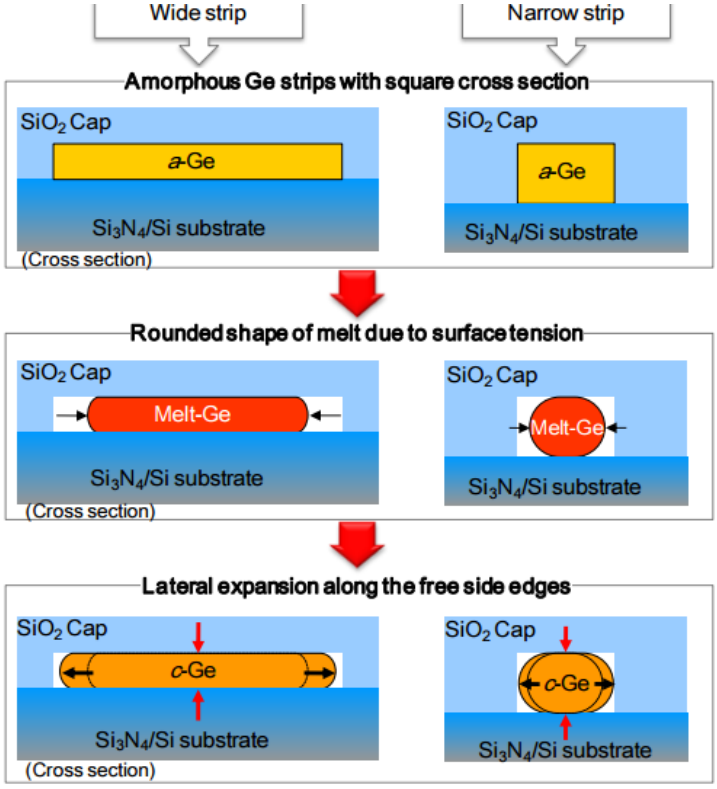


Figure 22 Comparison of Ge strips shapes before and after the RMG process reproduced from [59]. The effect of lateral expansion along free edges and surface tension were investigated for a variety of strip widths.

Reference [59] analyses and compares various aspects of the RMG for Ge on insulator with the thermal cap affecting structures underneath. According to the research, detailed analysis was performed for various dimensions of structures in order to determine how the surface tension affects the shape of the grown structures. However, this approach may not be fully practical for the design demonstrated later on in this thesis due to the silicon nitride layer underneath the Ge layer, which is replaced by an SiO2 layer in this work. The rounded shape of the strips is also linked to Ge volume contraction which was reported as 5.2% for the RTA melt [59]. Moreover, the curve of the free end of the strip is dependent on the ratio between the volume of the strip affected by the surface tension and the area of the free edge [42].

2.5 Summary

Si and Ge are vital elements of optoelectronics devices. The tunability of SiGe properties is highly attractive for a plethora of applications like detectors or modulators, hence the integration on SOI is required. Across the available methods of deposition, only RMG can deliver tuneable composition of SiGe alloys just after one not selective process. The SOI integration is challenging from the engineering point of view and challenges mentioned within Chapter 2 (e.g. Hydrogen content, geometry of structures and surface tension) must be considered.

Chapter 3 Methods

This chapter contains descriptions of the fundamental techniques required for the fabrication and characterisation of structures being a subject of this PhD thesis.

3.1 Fabrication

The microfabrication of multi-layered structures, including the ones described for the RMG process and referred as “tree like structures”, involves multiple subsequent processes like deposition, lithography, etching, planarization or annealing. This chapter contains a short overview of all techniques involved in the fabrication of SOI integrated RMG structures with a short explanation regarding the motivations for their selection. Process development and choice of the technique is crucial for the fabrication outcome, so the understanding of basics is of high importance.

3.1.1 Deposition techniques

The deposition techniques used during the fabrication can be listed as: Plasma Enhanced Chemical Vapour Deposition (PECVD) for SiO_2 (thermal cap for annealing and the first tests of insulating layer filling trenches) and Ge (first test runs only), Low Energy Plasma Enhanced Chemical Vapour Deposition (LEPECVD) for Ge or SiGe and thermal oxidation of Si in the final fabrication.

3.1.1.1 Chemical Vapour Deposition

Chemical Vapour Deposition (CVD) is a technique where the substrate, e.g. a Si wafer, is exposed to one or more volatile precursors, which can react with each other or decompose giving a desired thin film of a material on the surface of the substrate. The quality of the deposited layer depends on multiple process properties such as temperature, gas flow rate, precursors gases, pressure and the presence or not of plasma for enhanced deposition.

In particular, CVD techniques may be used for the deposition of Ge, SiO_2 and silicon nitride (SiN) through the reaction of precursor gases [1].

The reaction for Ge can be written as a decomposition of the precursor germane GeH_4 as follows:

$$GeH_{4(gas)} \rightarrow Ge_{(solid)} + 2H_{2(gas)}$$

This process is preferably conducted in lower range of temperature (around 400 °C) to avoid the oxygen incorporated into film.

The formation of SiO_2 films can be written as the following reaction between silane SiH_4 and nitrous oxide N_2O:

$$SiH_{4\,(gas)} + 2N_2O_{(gas)} \rightarrow SiO_{2(solid)} + 2H_{2(gas)} + 2N_{2(gas)}$$

The decomposition of SiH_4 requires higher substrate temperature (600-700 °C) than GeH_4. Hence, this mixture of gases is the most used for SiO_2 creation. N_2O is less reactive and more selective the oxygen O_2 giving more control over oxygen content throughout the film and slowing down reaction.

The formation of silicon nitride SiN_x is also an additional type of reaction based on SiH_4, however, ammonia (NH_3) is most often required. The reaction can be written as:

$$3SiH_{4(gas)} + 4NH_{3(gas)} \rightarrow Si_3N_{4(solid)} + 12H_{2(gas)}$$

The standard CVD technique can be modified in multiple ways, where the techniques PECVD and LEPECVD used within this thesis are based on using a plasma enhancement mechanism.

The main advantage of PECVD over CVD is lower deposition temperature obtained by using plasma which induces a chemical reaction and results in a faster deposition rate. Plasma is created with parallel electrodes; a grounded electrode and an RF-energized electrode placed around the chamber. The gases are transported into the chamber where Radio frequency (RF) power excites the reactants into plasma after dissociation and ionisation. The gases in this form are more reactive which increases the probability of film deposition on the substrate. After the deposition, the surface reactions are followed by the removal of by-products from the reaction chamber. It was found that coproduct gases, e.g. H_2, can be incorporated into the Si or Ge film which will impact the properties of the deposited material [2][3]. To avoid undesirable H_2 related effect in the film throughout further processing, a degassing thermal treatment leading to densification/relaxation is often used [4]. The temperature, pressure and gases flow parameters are the most important factors within the PECVD technique [5]. The substrate temperature is considered crucial for film properties such as optical (e.g. refractive index) or surface metrology like roughness or grain size [6][7] Moreover, high temperature can affect previously created features or doping profiles across the substrate, so it should be considered as a factor during process planning. In PECVD type deposition, the most common range of temperatures reported are between 200 and 400 °C, whereas standard CVD methods require temperatures from 600 up to 800 °C [4]. Also, pressure impacts rate of the film growth [8] and it has an impact on the uniformity across the wafer, where higher level of uniformity is reported for lower pressure techniques. Gas flow and gas ratio are related to the composition of the film and can be used to define deposition rate [5] along with previously mentioned parameters. The increased deposition rate is considered as a factor increasing a surface roughness of the film as demonstrated in [4][9].

A diagram of a PECVD tool is shown in Figure 23.

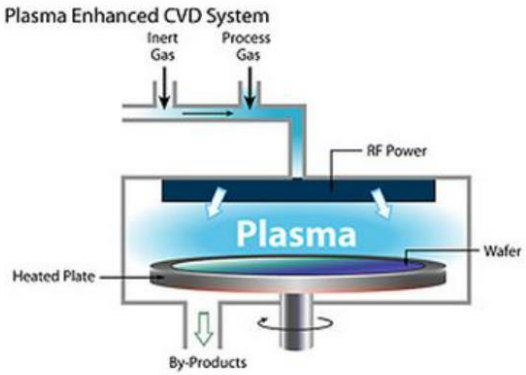


Figure 23 A diagram of a PECVD chamber with a view of the gas system, location of the RF power source and the location of the wafer. Reproduced from [9].

In the LEPECVD technique, a key modification is the lower energy of plasma ions compared to traditional plasma-based processing, which is applied to avoid possible damage to the crystalline structure of the deposited film by high energy ions existing for other techniques [8]. The source of electrons for LEPECVD can be e.g. a Tantalum (Ta) filament heated by high current which allows electrons to be thermally emitted. Argon is passed to the chamber where plasma is ignited by DC discharge from the heated filaments. The coils surrounding the chamber create a magnetic field which will help to focus the plasma onto the substrate. The technique is based on a low potential (+1V), high discharge current (~20 –70 A) to avoid ion damage and increase mass transfer to grow epitaxial films [10][11].

A low energy, high density DC Argon (Ar) plasma is used for efficient decomposition of precursors present within the chamber. Later lower energy ion bombardment is applied for removal of hydrogen from the substrate and further preventing of absorption of the H_2 present within the chamber, which is the major issue for other CVD techniques and affects the quality of the layer.

A diagram of an LEPECVD tool with all the main elements labelled is shown in Figure 24.

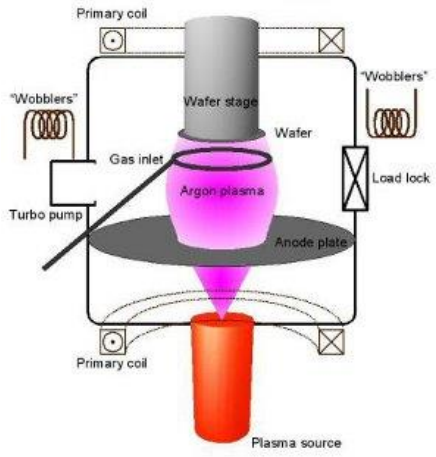


Figure 24 A diagram of an LEPECVD chamber with the argon plasma distribution controlled by the anode plate and the wafer's location. Reproduced from [10].

The effective dissociation of gases SiH_4 and GeH_4 used for Ge and $Si_{1-x}Ge_x$ growth is crucial to maintain high-quality growth at low temperature (around 500 °C for Ge films) [10][12]. The ratio of gases for the growth of $Si_{1-x}Ge_x$ is also crucial to maintain the defined composition of the growth layer. The difference in H_2 desorption rate in Si and Ge is no longer an issue using this technique, as opposed to PECVD techniques. The growth rate is independent of initial Ge composition or temperature of the substrate and is often faster than for CVD or PECVD methods with a reported value of 40 Å/sec [10] The deposition system allows to grow the wide range of thicknesses within the same reactor by modifying plasma density and gas fluxes (nanometer thick layers would be deposited with lower rate of 0.4 nm/s whereas thick layers can be deposited with the rate of 10 nm/s). The capabilities of LEPECVD has found multiple applications where precision and well-defined composition of SiGe are needed, e.g. for high mobility strained Ge channels, where precisely defined quantum wells and a thick buffer are realised during a single growth [13]. The possibility of growing high aspect ratio, self- assembled Si and Ge microcrystals was also developed by LEPECVD for deeply patterned Si substrates [14]. The results obtained from LEPECVD growth are very promising, making this method desirable to solve issues observed within heteroepitaxial growth e.g. the effect of the change in shape and therefore stress can be minimised due to the low temperature used and the lattice mismatch on the obtained film can be decreased due to the well-controlled SiGe composition (lattice constant) [14]. Nevertheless, LEPECVD is not widely

(commercially) available. Moreover, the tool requires extended maintenance and quality control to sustain high control of the process. For LEPECVD growth, the TDD value of $1.1\times10^{5}cm^{-2}$ and RMS rough-ness of 32 Å for pure Ge on Si via a graded buffer layer was reported by the LNESS group [10], which are both typically lower than the values reported using alternative growth techniques.

3.1.1.2 Thermal oxidation

As mentioned previously, SiO_2 can be obtained from various deposition methods, nonetheless thermal oxidation is preferred for some specialized cases. Furthermore, thermally grown SiO_2 has higher density, higher uniformity, higher breakdown voltage, lower roughness and slower etch rate in HF compared to CVD grown SiO_2 [15].

The thermal oxidation of Si can be described by the Deal-Grove oxidation model [15]. The initial stage of thermal oxidation requires access to bare Si substrate and then when all the Si substrate is covered with the first layer of thermal SiO_2, solid state diffusion occurs through this layer creating a thicker oxidized layer. The interface between SiO_2 and Si is stable and reproduceable. The thickness of the consumed Si to grown SiO_2 is in a 0.46 ratio, which means 2.17 µm of SiO_2 is grown per 1 µm of consumed Si. The thickness of the layer is well defined which allows well controlled processes even for thin layers, an example of a thermally grown SiO_2 layer on a Si substrate is shown in Figure 25 [1]. The oxidation of Si occurring without additional thermal processing is known as thermal growth of native oxide [15] and it must be considered when access to the underlaying layer is especially critical.

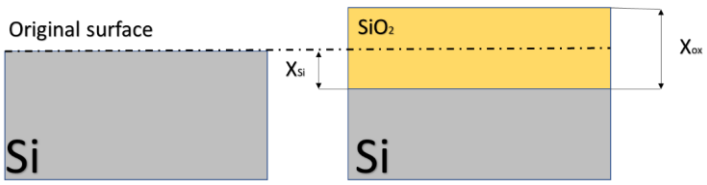


Figure 25 SiO_2 layer thermally grown on the Si substrate against the Si level.

Thermal oxidation is a high temperature process, which requires a tube furnace and a quartz carrier for samples/ wafers. This type of system is compatible with high temperature growth thanks to the high melting point of the quartz glass (1710°C) [16]. The temperature used for thermal oxidation of silicon is usually in the range of 1000-1200 °C or 800 °C for thin SiO_2. The quartz tube contains multiple inlets supplying gases uniformly across the tube and a wafer carrier with a slow and accurate control of the heating zones (e.g. +10 °C per minute) to control the growth and uniformity accurately [17]. Gaseous oxygen (O_2) or water/ steam reacts with the Si surface creating amorphous SiO_2. Dry oxidation is usually much slower but produces very uniform, dense layer. After the first

layer is formed, diffusion of O_2 towards the underlying Si occurs if the temperature of the furnace is high enough for the continued creation of SiO_2 [1].

The reaction for dry oxidation can be written as follows:

$$Si_{(solid)} + O_{2(gas)} \rightarrow SiO_{2(solid)}$$

For wet oxidation, O_2 is replaced by steam/water and the reaction with a Si substrate is written as:

$$Si_{(solid)} + 2H_2O_{(gas)} \rightarrow SiO_{2(solid)} + 2H_{2(gas)}$$

The system used for thermal oxidation is shown in Figure 26.

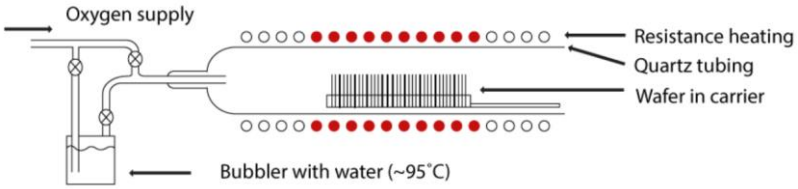


Figure 26 The diagram of the system used for the thermal oxidation [17].

Wet oxidation is chosen for higher thickness of the material, where growth rate control accuracy is not as crucial, whereas dry oxidation can be used for lower thickness for high control [17]. For the fabrication purposes, the dry oxidation was used as only thickness under 100 nm of SiO_2 was required.

3.1.2 Lithography techniques

Lithography is a vital process used in microfabrication to pattern substrates (either wafers or samples). Moreover, the accuracy of the design and all further processing heavily relies on the performance of the lithography making this process one of major areas of improvement or a possible bottleneck of the microfabrication [18]. Usually, multiple lithography steps are required in a fabrication process, with a particular emphasis on the fidelity of the pattern printed and the accuracy of the alignment between layers. After lithography, the substrate with the photosensitive material is etched (or other process such as ion implantation) and afterwards, the photoresist left on the surface can be removed allowing further processing.

For optical lithography techniques, the resolution limitation is a consequence of the Rayleigh formula written in Equation 5 [18].

$$\Delta x = \frac{k\lambda}{Na} \qquad \text{(Equation 5)}$$

where Δx- resolution of the system, k- process factor for specific optics, resist or process latitude, between 0.25 and 1 with typical value of 0.6, values can be confirmed experimentally for a set of known resolutions, Na- numerical aperture of the lens, defined as sine of angle of incidence, $\boldsymbol{\lambda}$-illumination wavelength.

The lithography methods used for this work are: photolithography – UV contact lithography (6'' wafers) or DUV projection lithography (8'' wafers), and electron beam lithography (6'' and 8'' wafers).

The visualisation of lithographic nodes and processor technology leading to 13 nm technology is shown in Figure 27 based on data from Zeiss [18].

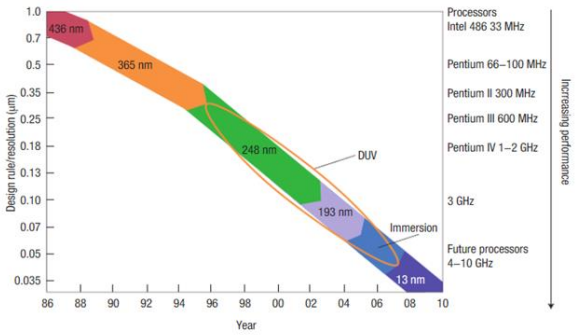


Figure 27 The correlation between resolution of the lithography and performance of the resulting microprocessors [18].

The 436 nm technology is used in contact photolithography, whereas the 248 nm technology is corresponding to the scanner used for fabrication within the Southampton Nanofabrication Centre.

The attention of researchers and industry throughout last decade was focused on crossing the barrier of 10 nm resolution and defining new limits of CMOS processing. The e-beam lithography is able to produce devices with resolution in range of a few nanometres, however, the optical lithography with lower cost is a tool of choice when the resolution is not critical.

The current capabilities of lithography allow fabrication with sub-10 nm resolution, mainly thanks to the application of immersion systems, double patterning technology, reticle enhancement techniques or, finally, applying extremely short wavelengths (13.5 nm) in techniques called Extreme ultraviolet lithography (EUVL) [19]. Also, next-generation lithography (NGL) based on even shorter

wavelengths for the X-ray lithography (XRL) (1 nm) [20] and deep X-ray lithography (DXRL) (0.1 nm) are under development.

3.1.2.1 Optical lithography

Ultraviolet (UV) lithography is a method where photosensitive polymer materials are spun onto a substrate and exposed to a wavelength of 436 nm (emitted by a Mercury Hg lamp) through a patterned chrome mask deposited on either fused silica (QZ) or soda-lime (SL) glass [21].

To perform successful lithography the following steps are most often necessary:

1) Substrate heating or surface preparation
2) Spin coating
3) Pre-exposure bake (softbake)
4) Mask alignment
5) Exposure
6) (Optional) Post-exposure bake
7) Development
8) Hard bake before next processes step

The preparation of the substrate involves baking or priming with chemicals. Thermal treatment in an oven or on a hot plate is mostly desirable to improve the adhesion to the substrate by dehydration and cracking the -OH bonds on the surface [22] Dehydration can be also performed with acetone and isopropanol, whereas improving adhesion requires chemicals like HMDS (Hexamethyl disilazane vapor) as an example of an adhesion promoter.

The prepared substrate can be covered with light sensitive polymers known as photoresists using a spin coating or spray technique; the thickness of the resist is a result of the resist viscosity and spin process settings.

Due to the possibility of having the solvent still present in the coated material, the substrate should be baked again either in an oven or on a hot plate with parameters (time of baking and temperature of baking) adjusted to the kind of resist and its thickness [22].

The UV exposure is a vital part of the optical lithography where light is initiating a plethora of chemical reactions across various photoresist types [15][23]. The structures are either exposed or covered by the chrome mask, depending on the type of resist or the field of the mask (dark or light field for varied coverage of the mask). To sum up, after UV exposure, positive photoresist becomes

soluble in the developer when exposed; while negative photoresist is soluble in the developer when unexposed.

Some resists need to be post-exposure baked to finish the photopolymerization processing initiated during the exposure [15]. This is the case for AZ2070 (as an example) where post exposure bake is a requirement, which is often the case for negative resists. Photoresist is then developed using a chemical which is different for each resist.

A schematic of a lithography process with subsequent etching for either positive (e.g. S1813) or negative (e.g. AZ2070) resist is shown in Figure 28 [15].

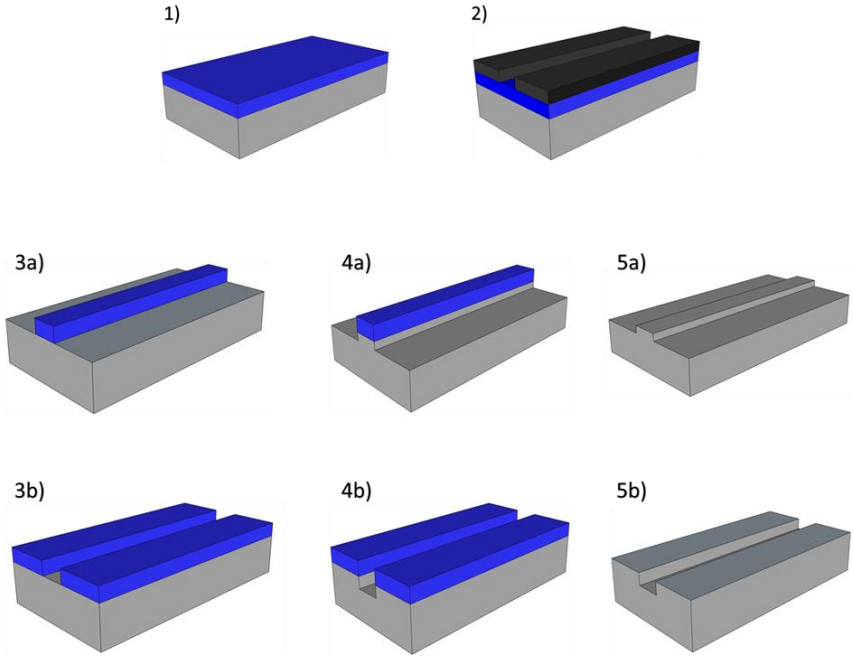


Figure 28 Lithography process for positive and negative type of photoresists. 1) The substrate (e.g. Si wafer) with photoresist on the top, 2) photomask placed above the substrate covered with photoresist and affected by the UV lamp, 3a) development of structures covered with negative resist, 4a) etching for structures covered with negative resist, 5a) negative resist removal, 3b) development of structures covered with positive resist, 4b) etching with positive resist 5b) positive resist removal.

One of the advantages of contact photolithography is the low cost of processing and accessibility, however, the pattern resolution and alignment between layers are limited to 0.5 or 1 µm [21][24] respectively. Given these limitations, predominantly the feature size limitation, contact lithography is not suitable to integrate photonic waveguides and either e-beam lithography or deep UV projection lithography must be used.

3.1.2.2 Deep ultraviolet lithography

Deep UV lithography (DUV lithography) is an optical projection type lithography technique where the pattern on a reticle/mask is projected to the wafer surface through an optical system. The DUV lithography technique is called an industry "workhorse" [25] and is used as a high-throughput technology suitable for large area and high accuracy volume production where traditional optical lithography does not meet expectations for minimum critical dimensions and alignment tolerances.

The wavelengths used for DUV lithography are 248 nm obtained using a Krypton Fluoride KrF laser or 193 nm obtained using an Argon Fluoride ArF laser. A diagram showing an example of a projection lithography system is shown in Figure 29.

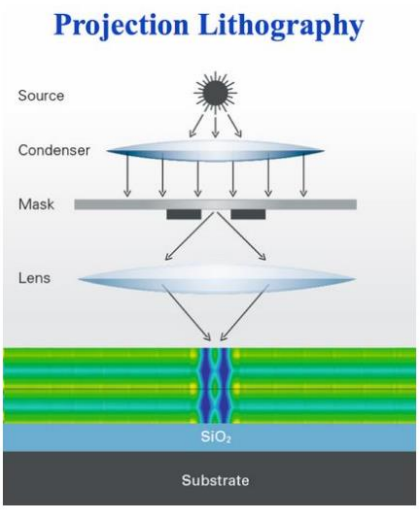


Figure 29 Principle of the projection lithography [26].

The DUV lithography available in the Southampton Nanofabrication Centre is based on the 248 nm KrF laser and allows to obtain features with resolution down to 150 nm [27].

3.1.2.3 Electron beam lithography

Electron beam lithography (EBL) is a powerful technique for creating nanostructures beyond the capabilities of conventional photolithography with possible resolutions of a few nanometres [28][29]. The Jeol JBX 9300 e-beam writing system in the Southampton Nanofabrication Centre (SNC) is capable to achieve linewidths of 8 nm with a minimum beam diameter of 2 nm [24].

The technique doesn't require physical optical masking, and patterns are exposed on the polymer by moving an electron beam over the sample following a digital template. The electron source is commonly created through hot Tungsten/ Zirconium (W/ZrO_2) filament used to obtain field electron emission, which are later focused either through electric or magnetic lenses. The preparation of the sample is similar to optical lithography and contains preparation of the surface to improve adhesion (e.g. additional chemicals before the resist) and to remove any unwanted residuals from the surface by heating. The prepared substrate is spin coated with either positive (ZEP or PMMA) or negative resist (AZ® nLOF 2000 Series), afterwards espacer acting as a conducting layer to remove the electrons and prevent charge build-up can be added. The resist is exposed to the electron beam interacting with the polymer (resist). The exposed areas of the resist are affected by the chain scission which is the degradation of the main chain of the polymer. As a result, the solubility of the resist changes within specific regions across the wafer enabling selective removal of unexposed regions using a developer [30]. The sample is scanned across the features with the electron beam patterning sample accordingly to the design delivered usually in the CAD file (.gds file) and processed by the Beamer software to deliver patterning. Due to easily changeable design which is replacing traditional lithographic mask, the cost and time between fabrication steps (mask order etc) can be decreased when the process can be conducted in a chip scale. The flexibility of the design is especially convenient for multiple variations of single processing operations on the design like during tests. After the exposure the substrate is developed with designated chemicals and ready for further steps like etching. The espacer is removed with water only before the development.

The e-beam technique provides very high resolution; however, limitations of this technique are also significant. The cost of the maintenance is high, and time of the exposure can be long for more detailed structures with time of exposure in several orders of magnitude longer on a large-area substrate compared to optical lithography [8]. Dimensions and accuracy of the pattern transfer from a file onto substrate compared to optical lithography [31]. Dimensions and accuracy of the pattern transfer from a file onto a substrate depends on either ebeam or resist/ development (thickness, time of development) parameters. Almost two decades ago, the optimized e-beam processing for standard PMMA resist was used to fabricate lines under 5 nm [32] [33]. Higher speed

(energy) electrons are needed to maintain higher resolution, whereas for lower speed (energies of electrons), energy in range 0-5 eV, the resolutions drop down to 100 nm [34]. The foundation for the energy and resolution dependence is the number of interactions causing scattering between electrons and the resist [35].

3.1.3 Etch techniques

Etching techniques are used for selective removal of Si, oxide/nitride/metal layers after they are exposed using one of the patterning lithography techniques. The "masking" material used to protect the features should not be significantly etched during the process to avoid affecting the shape of the pattern and to enable the required etch depth to be reached. Usually, the masking material is photoresist remaining after the lithography on the top of the wafer or a hard mask adjusted to the etched material and not sensitive to the etchant. After the etching, the mask is usually removed using either O_2 plasma ashing or another adequate etching technique (tailored resist stripper). Two major types of etching are dry etch (e.g. inductively coupled plasma ICP or Reactive Ion Etching RIE) and wet etch where a liquid phase etching solution is used. Depending on the design and technique used, it is possible to obtain different etch profiles as shown in Figure 30.

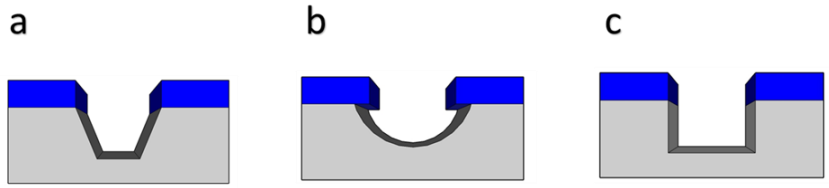


Figure 30 Etch diagrams: a) angled etch, b) isotropic dry etch, c) anisotropic etch. Grey colour corresponds to the substrate e.g. Si, whereas blue colour corresponds to resist or hard mask.

3.1.3.1 Dry etch

The Inductively coupled plasma etch (ICP) dry etch technique was mostly used in this project, however RIE etch was also investigated.

3.1.3.1.1 Inductively coupled plasma etch

The ICP technique can used for selective etch of Si, SiO_2 or Ge, usually with the assistance of either the resist layer on the top of the substrate or a hard mask supported by suitable recipes. ICP etch is a dry etching technique relying on RF currents (typical value 13.56 MHz) induced in electrodes (coil shaped) surrounding the chamber as shown in Figure 31. A strong RF current induces a

magnetic field, which subsequently induces an alternating electric current within the chamber, dissociating the gases into a plasma of ions and reactive neutral elements (highly reactive but not yet in a form of ions) [2].

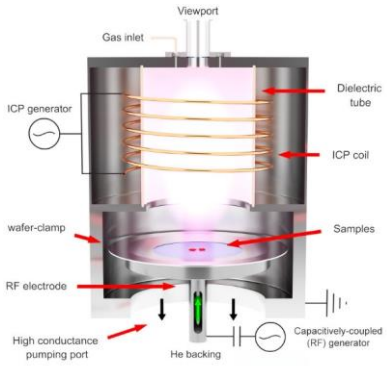


Figure 31 A schematic diagram of a standard ICP system used for dry etch [23].

Due to separated RF and ICP generators, the independent control of ion energy and ion density allows flexibility of the process. The ions obtained as a result of the plasma's creation take part in physical etching whereas the reactive neutral elements take part in chemical etching. A common chemical reaction for dry etch of SiO_2 by gaseous CF_4 can be written as following:

$$SiO_2(solid) + CF_4\ (gas) \rightarrow SiF_4(gas) + CO_2(gas)$$

3.1.3.2 Wet etch

Wet etching is used in microfabrication to remove layers or to etch structures within layers chemically, resulting in a very selective process (between materials), but an isotropic etch profile. Commonly, wet etching is conducted with diluted hydrofluoric acid HF for SiO_2 or tetramethylammonium hydroxide TMAH for Si.

The choice of the etching method is based on the material to be etched, available hard mask or resist, the depth and the desirable profile of the trench within the material. All these profiles can be desirable or avoided based on the purpose of the processing.

The example mechanism of wet etch can be described using reactions like the below reaction between SiO_2 and diluted HF as written:

$$SiO_2(solid) + 6HF(liquid) \rightarrow H_2SiF_6(liquid) + 2H_2O(liquid)$$

The etch rate for 20:1 HF is varied between 30 - 80 nm / min for thermal or PECVD SiO_2 respectively; (based on the etch rate measurement maintained in the cleanroom facilities, depending on the precise concentration of the etchant). The chemical doesn't attack the resist even after several hours and high concentration like 50% [24].

The issues during the wet etch may be linked to the lack of adhesion of the resist to the surface of the substrate which is shown in Figure 32 for poor adhesion and for sufficient adhesion between layers.

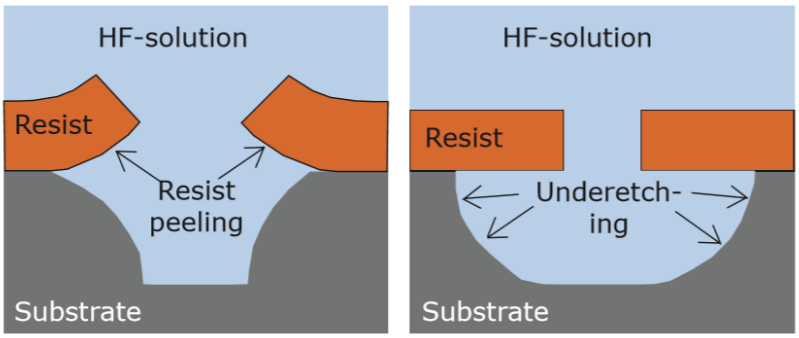


Figure 32 The adhesion of the resist is important for the profile of the etch and it has significant impact on further processing and performance of resulting devices [24].

When etching of the entire SiO_2 layer is required, which is the case for the removal of the capping layer or the hard mask, for example, the HF etch is used as a standard operation without any photoresist on the top of the wafer.

The Si etch is often conducted by dry etch, however, the angled etch or undercut is desirable for some applications e.g. suspended waveguides or membranes [25,26]. Strongly alkaline aqueous solvents like KOH, NaOH or TMAH are suitable for angled Si etching. In Figure 33, the structure of TMAH with OH- anion is illustrating the alkaline character of this component.

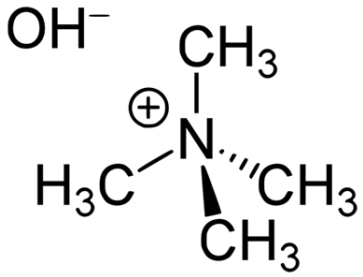


Figure 33 TMAH structure.

The mechanism of the TMAH etch for Si can be described using the general reaction for alkaline solvents as written in the following reaction:

$$Si(solid) + 2OH^{-}(liquid) + 2H_2O(liquid) \rightarrow Si(OH)_4(liquid) + H_2(gas)$$
$$\rightarrow SiO_2(OH)_2^{2-}(liquid) + 2H_2\,(gas)$$

The directionally TMAH etched structures within Si substrate are shown in Figure 34.

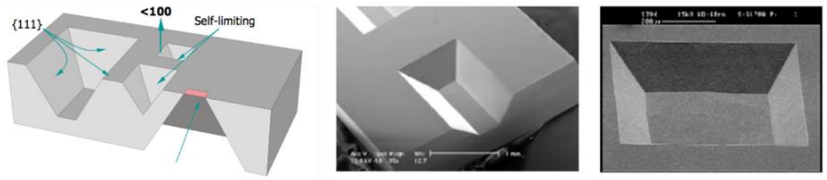


Figure 34 The diagram of directional etch and SEM images of etched structures [27].

As shown in Table 3, the TMAH is characterized with a good etch ratio for Si structures oriented (100/111) and (110/111) needed to obtain angled trench formation with atomically flat surfaces. Lower etch rates of SiO_2 and Si_3N_4 compared to Si allow the use of these materials as a reliable hard mask. However, due to this low etch rate, a short HF dip is always needed before the TMAH based processing as any native SiO_2 could form a masking layer preventing Si etching. Time of the HF dip should be adjusted to the expected thickness of the layer and confirmed etch rate of the HF solution, for the fabrication described in this thesis the time was set to 5 s in HF 20:1.

Table 3 TMAH properties for a wet etch reproduced from [24].

Etchant	Etch rate ratio for Si		Etch rate (absolute) [nm/min]		
TMAH (25%,80°C)	(100)/(111)	(110)/(111)	Si (100)	Si_3N_4	SiO_2
	37	68	0.3-1	<0.1	0.2

3.1.4 Chemical Mechanical Planarization (CMP)

Chemical Mechanical Planarization or Polishing (CMP) are processes which either smooth or planarize the surface of the substrate. In the age of constant demand for decreased size of features across the chip and demands for novel lithography techniques, global planarization is a necessity [40]. CMP is widely used for III-V compound semiconductors and silicon photonics (SiO_2, SiNx and SiGe/ Ge layers).

CMP combines simultaneous chemical etch and mechanical abrasion by abrasive particles to secure advantages and minimise undesirable effects of these processes separately. The surface of the polished substrate (chip or wafer) is affected simultaneously by high pressure and chemicals which allows effective planarization from a starting point of varied thicknesses of the material across the sample. The regions with thicker material on the substrate can be subjected to higher pressure of the polishing pad enabling higher planarization rate comparing to thinner layer or material within trenches on the same substrate [41]. This mechanism embraces the uniform planarization of the material on the top of the wafer.

The principles of the CMP process are shown in Figure 35.

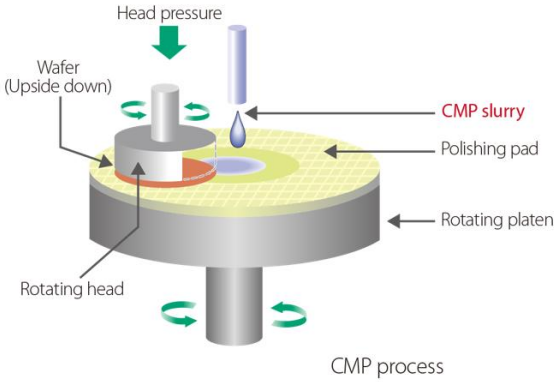


Figure 35 The process of CMP reproduced from [42].

The performance of CMP can be defined by the uniformity and the level of control of processing. Uniformity of the wafer can be considered on a multiple level including: WID (within die), WIW (within wafer) and WTW (wafer to wafer) planarity/ nonuniformity.

The uniformity and the rate of material removal depends on multiple conditions with special importance of the specification of the polishing system and the design.

Parameters of the processing like down force, platen and carrier speeds are confirmed to have an impact on CMP uniformity and removal rate [31]. The membrane installed between the rotation carrier and the wafer is responsible for applied down force on the back of the wafer [13]. Increased down force and faster platen or carrier speed increase the removal rate [14].

Parameters of the processing like down force, platen and carrier speeds are confirmed to have an impact on CMP uniformity and removal rate [31]. The membrane installed between the rotation carrier and the wafer is responsible for applied down force on the back of the wafer [43]. Increased down force and faster platen or carrier speed increase the removal rate [44].

Parameters of the substrate like design (pattern density) [45] and substrate dimensional characteristics, including substrate total thickness variation (TTV) and wafer shape (bow and warp) [34][46] should also be considered.

A plethora of applications of CMP rely on the selectivity of the slurry. Highly selective slurries are required to achieve tuneable selectivity for systems without a slurry sensitive stop layer.

On the contrary, the situation with required near-perfect planarity requires slurry with no selectivity to secure smoothness within the same level of various materials. The complexity of the polished system might also require multi-step processes with more than one type of slurry used for each step [44].

Besides selectivity, other properties of slurry are also of high importance. The concentration and additional components like H_2O_2 were researched for Ge designated slurry [32] [33]. The removal mechanism for CMP for Ge depends on the pH of the system due to the chemistry behind Ge creating chelate complexes with varied solubility. The polishing highly relies on this principle and can be described with various reactions for a whole range of pH [47].
The initial step is an oxidation of Ge on the top of the substrate and it can be described with following reaction:

$$Ge(solid) + 2H_2O_2(liquid) \rightarrow GeO_2\,(liquid) + 2H_2O(liquid)$$

The processing in acidic and neutral pH < 8 is resulting in creation of non-soluble in water Ge hydroxides like Germanic acid:

$$GeO_2(liquid) + 2H_2O(liquid) \leftrightarrow Ge(OH)_4(liquid)$$

For pH in range between 8 and 11 the dissociation of GeO_2 occurs more effectively as written in the following reaction:

$$GeO_2(liquid) + 2H_2O(liquid) \leftrightarrow Ge(OH)_3^-(liquid) + H^+(liquid)$$

The highest removal rate was reported for pH > 11 [48] when highly soluble Ge based anions are formed as written in the following reaction:

$$GeO_2(liquid) + 2H_2O(liquid) \leftrightarrow GeO_2(OH)_2^{2-}(liquid) + 2H^+(liquid)$$

The most commonly and commercially available slurries for Ge CMP are G1000 and W2000, used usually either for low or high pattern density respectively [49].

It is worth mentioning that a decreased TDD for Ge layers grown by UHVCVD was demonstrated for buffered SiGe systems after planarization [50]. The thicker buffers are linked to higher stress observed on the top of the layer; hence the planarization is used to remove the threads in pileups to relieve the strain introduced in the subsequent growth and minimize the nucleation of new threading dislocations [50].

3.1.5 Rapid Thermal Annealing

Rapid Thermal Annealing (RTA) is a heat treatment used for multiple processes including RMG, densification or/and dehydrogenation of layers, and dopant activation [4]. A Rapid Thermal annealer contains a chamber with heating tungsten W filament lamps mounted usually on the top of the chamber, above a stage with quartz holders to support the wafer. The maximum rate of heating up the wafer substrate is 100°C/s, which is controlled either by the thermocouple in direct contact with the backside of the wafer for lower temperatures or by measurement of the infra-red

emission by a pyrometer at higher temperatures. The temperature range and accuracy are specified for each type of thermocouple [51] and depend mostly on the metals used for the junction within the thermocouple. The heating zone is created above the wafer, whereas the walls of the chamber are kept at a constant temperature using process cooling water flowing around the chamber. The parameters of the process like temperature or lamp power are programable by a PID (Proportional, Integral and Derivative) loop control system based on collecting data from the measurement device, e.g. the temperature or power sensors, and constantly adjusting the response.

The RTA system is used for samples with tailored Ge or SiGe structures placed on the Si carrier wafer. It's worth mentioning that the relatively small volume and different absorption properties of the Ge surrounded by insulator might cause higher temperature within the Ge structures than measured either by pyrometer or by thermocouple attached to the back of for Si wafer. Moreover, especially for the measurements done by the thermocouple, an additional thickness of the carrier wafer is a reason for a considerably different temperature between that measured and that within the top Si layer on the SOI sample or Ge based structure. The difference in thermal conductivity between Si and SOI samples can also be considered as significant and enough for a temperature variance between platforms for a given lamp power. The range of anneal temperatures possible for both platforms is between 400 and 1200°C with varied time in the range 1 second and 30 minutes [4]. An ambient gas (e.g. hydrogen or nitrogen) can be pumped into the chamber to replace air. The gas is supporting the RMG process by adding an additional pressure to ensure encapsulation by the insulator cap on top of the melted structures to prevent these structures from balling up [4]. Gases used during RTA impact properties of the surface like e.g. roughness with advantage of H_2 over N_2 [4] [51]. Nevertheless, an N_2 flow was used for this project because H_2 is not supplied to the tool and the surface of the Ge is not exposed anyway.

RTA can also be used for an efficient removal of H incorporated within SiO_2 layers as confirmed in research on SiH_4 based SiO_2 films in a few temperature ranges as demonstrated in [52]. The efficiency of the hydrogen removal depends on the time and the temperature of annealing. Hydrogen concentration as a function of the depth from the free surface can be measured by secondary ion mass spectroscopy (SIMS) for a range of anneal temperature as shown in Figure 36.

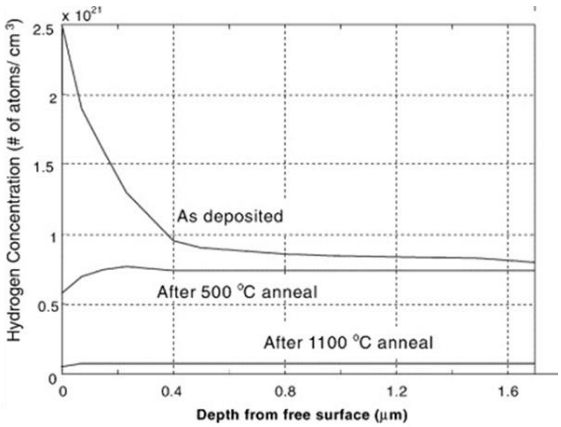


Figure 36 H content of SiH_4 based PECVD of SiO_2 as a function of depth from the free surface, reproduced from [52]. The measurement was performed with SIMS for various anneal temperatures.

Hydrogen removal matters for the RMG process when crystalline SiGe or Ge structures are formed in a temperature high enough to allow gas to leave the SiO_2 or Ge layers. If the dehydrogenation processing is not performed before annealing then the gas escaping these layers can create voids and decrease the consistency of the resulting structures. The bow of the wafer (caused by adding highly strained layers to one surface of the wafer) influences CMP or wafer bonding, so it is important to optimize the annealing process in order to remove a sufficient amount of hydrogen and at the same time avoid the negative effect of thermal processing on the wafer's bow. Annealing at 700 °C for 30 minutes was used for SiO_2 layer densification and H removal resulting in a thickness decrease of 5% for a 50 nm thick SiO_2 film [4].

3.2 Characterisation

Analysis techniques used for the material characterisation can be listed as follows: Scanning Electron Microscopy (SEM), Focused Ion Beam (FIB), Atomic Force Microscopy (AFM), Raman spectroscopy, reflectometry, profilometry and ellipsometry.

3.2.1 Material thickness and profile

The thickness control of layers is crucial for design and fabrication, especially for steps such as deposition and etching. The techniques used to measure layer thickness during this project were spectroscopic reflectometry and spectroscopic ellipsometry; both methods are non-destructive and contact-free, which is desirable for further processing.

One of methods used to determine not only thickness but also optical (e.g. complex refractive index) and dielectric properties is Spectroscopic Ellipsometry (SE), where the range of measured thicknesses is usually in the range of 1 nm to a few µm [53]. Ellipsometry can be used to measure most material types: dielectrics, semiconductors, metals, superconductors, organics, biological coatings, and composites of materials [54]. The technique is highly popular due to its sensitivity and a chance to obtain quick *in-situ* measurements.

The basis of spectroscopic ellipsometry measurement is the reflection and change in the polarisation of the reflected light after contact with the sample due to the changeable Fresnel reflection coefficient with the wavelength. A diagram describing the principle of the measurement is presented in Figure 37, where p-polarized light has an electric field direction parallel to the plane of incidence of a device, and s-polarized light has the electric field oriented perpendicular to that plane.

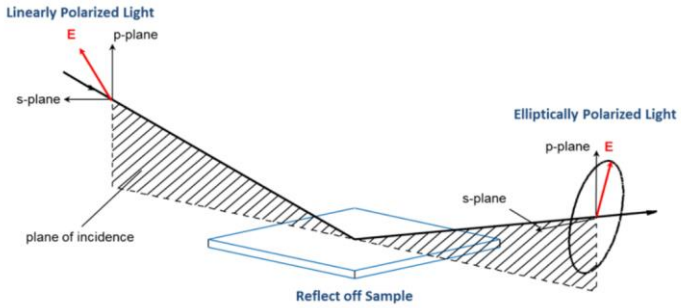


Figure 37 The ellipsometry measurement, reproduced from [53].

The polarization change ρ is represented as reflection parameters like an amplitude ratio, Ψ, and the phase difference, Δ, and can be express as equation 6.

$$\rho = tan(\Psi)e^{i\Delta} \qquad \text{(Equation 6)}$$

For fabricated structures, the obtained response was compared with the model library and the fitting set of layer parameters is calculated by the software of the tool M-2000 Ellipsometer from J. A. Woollam with targeted accuracy of the tool even as good as 0.01 % [53]. The accuracy of ellipsometry is enhanced by measuring the ratio of parameters instead of their absolute values.

Ellipsometry has limitations due to contamination or oxides present within layers of materials; the surface roughness should also be considered as a factor disrupting measurements.

Systems based on Ge with underlaying SiO_2 can be inspected on both Si and SOI substrates using Ellipsometry. However, the thickness of the Si substrate will not be defined after the measurement,

which is important when trying to measure etch depth into the Si substrate. This drawback implies the necessity of profilometry as a supplementing tool for measurements.

Reflectometry can be used for measurements of transparent or semi-transparent layers up to three layers which is also a limitation for measurements of non-transparent layers like Ge. The reflectometry is designated for smooth surfaces, however models considering roughness can be applied to improve an accuracy of the measurement.

3.2.2 Profilometry and Atomic Force Microscopy

As mentioned, profilometry is a technique complementing ellipsometry or used when other techniques are not enough to define the topography of the wafer, thicknesses of layers or differences within the thickness of the same layer (e.g. trenches etched within the Si wafer). Profilometry can be either light or stylus based. The stylus-based tools are usually slower and physically touch the surface. The probe touching the surface can damage the sample or introduce contamination. The result of measurements can be a single point, a line scan or even a full three-dimensional map.

Another technique used to define topography of a sample is Atomic Force Microscopy (AFM), especially useful to define surface roughness after processes like etching, deposition or CMP. The advantage of this technique is a much higher resolution in the z-direction. How-ever, only small areas can be mapped.

3.2.3 Raman Spectroscopy

Raman Spectroscopy is a non-destructive technique widely used for nanomaterial characterisation through a variety of disciplines from biology to optoelectronics [55]. The data obtained from this technique allow the determination of multiple properties of a material including: chemical composition, structure, phase, polymorphism, impurities or strain [56]. Based on the characteristic Raman spectrum, it is possible to identify the material with the help of extensive Raman spectra libraries.

This technique relies on a laser light source to irradiate a sample and generate Raman scattered light, which is detected as a Raman spectrum by a CCD camera. The resulting spectrum provides a characteristic pattern used to identify substances and confirm their properties.

An example of a Raman spectroscopy setup is presented in Figure 38; moreover, this specific tool was also used for measurements of $Si_{1-x}Ge_x$ composition carried within this project.

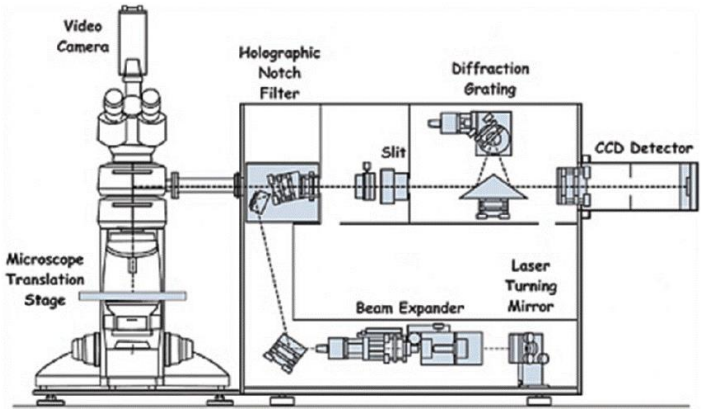


Figure 38 Schematic diagram of a Renishaw Raman microscope [57].

The working principle of Raman spectroscopy is the interaction between the laser photons and molecular vibrations, phonons or other excitations in the measured sample. The change of the energy between vibrational states is presented in Figure 39 for both elastic and inelastic scattering.

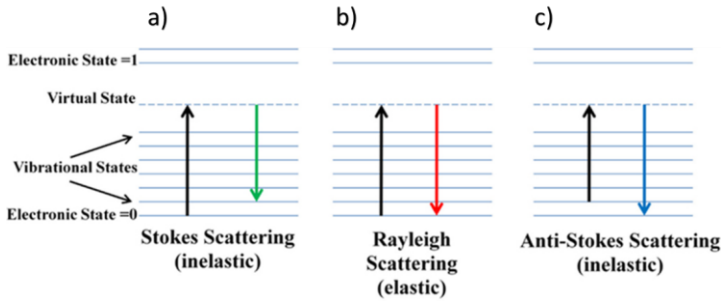


Figure 39 The energy diagram for processes occurring from the interaction of photon with a molecule; a) inelastic Stokes Scattering with the final energy level higher than the initial one, b) elastic Rayleigh scattering which implies the same energy level at the end and the initial level of the interaction, c) inelastic Anti-Stokes Scattering with the final energy level lower than the initial one [38,39].

The change in energy corresponds to the shift of the energy which can be presented by the change in wavelength as shown in Equation 7.

$$\Delta\omega = \frac{1}{\lambda 0} - \frac{1}{\lambda 1} \qquad \text{(Equation 7)}$$

where $\Delta\omega$ is the Raman shift, $\lambda 0$ is the incident wavelength and $\lambda 1$ is the scattered wavelength.

The penetration depth of the Raman measurement is highly dependent on the wavelength of the laser, wavelengths of 532 nm, 633 nm, and 785 nm can be used to probe varying depths of material, including Ge and Si, which is shown in Table 4.

Table 4 The penetration depth of light of various wavelengths into Si and Ge [4][59].

	Laser wavelength [nm]		
	532	**633**	**785**
Penetration depth in Si (nm]	980	2650	8930
Penetration depth in Ge [nm]	17	53	179

The numerical aperture of the lens used during the measurement and various lenses result in different spot size diameters as shown in Table 5. It should be mentioned that these values are valid for straightforward optical microscopy and are only an approximation for more complex Raman microscope.

Table 5 Spot size radius for a choice of lasers and magnifications [4].

Magnification	**Numerical aperture**	**Laser 532 nm**	**Laser 633 nm**	**Laser 785 nm**
		Spot size radius [µm]		
x5	0.12	2.71	3.22	4.00
x10	0.4	0.81	0.97	1.20
x20	0.75	0.43	0.51	0.64

Both these factors, penetration depth and the size of the spot, influence the Raman measurement and accuracy of the data especially when the measured structures are either on the top of the substrate or embedded into the substrate with a different material surrounding the structure. Sizes of the structures relevant for this thesis are varied in the range between 100 nm to 10 µm, and with the range of alloy composition varied between pure Si and pure Ge. Application of the Raman Spectroscopy technique for the composition measurement of Si, Ge and $Si_{1-x}Ge_x$ is based on the ratio between Ge-Ge and Si-Ge peaks and requires well defined, sharp peaks, which were achievable with the use of a high-density grating (3000 lines/mm) designated for the 532 nm laser

used for this project. The power of the laser was set to minimum value to avoid heating which can melt material and change the local composition.

The Ge and $Si_{1-x}Ge_x$ composition can be indirectly defined via Raman spectroscopy as peaks characteristic for Si-Si, Ge-Ge and Si-Ge can be observed on the Raman spectrum. An example spectrum is shown in Figure 40.

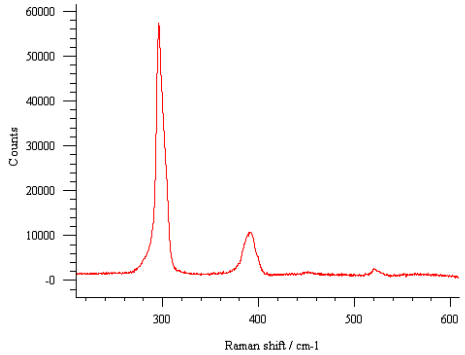


Figure 40 An example Raman spectrum for a SiGe structure obtained from the RMG processing. The asymmetry of the peaks can be minimised by decreasing the power of the laser and extending the time of measurement.

The Raman shift of single crystal Ge is measured to be 300.7 cm^{-1}, whereas for singe crystal Si it is 520.2 cm^{-1}; a full width at half maximum (FWHM) of 5.3 cm^{-1} is reported for Ge and 4.6 cm^{-1} for Si [59]. The Si-Ge peak can be observed between 390 cm^{-1} to 410 cm^{-1} [4]. The strain and the temperature can affect the position of peaks, but for the composition's calculations described in this thesis are based on equation 8 relating only to the intensity of Ge-Ge and Si-Ge peaks. This methodology of defining the $Si_{1-x}Ge_x$ composition is based on using the Mooney equation [60] (equation 8):

$$\frac{(I(siGe))}{(I(GeGe))} = \frac{(2(1-x))}{kx} \quad \text{(Equation 8)}$$

Where, *x* is Ge concentration to be calculated, *k* is a constant (1.2), I(SiGe) describes the integrated peak intensity for Si-Ge, and I(GeGe) describes the integrated peak intensity for Ge-Ge obtained from the spectrum, as shown in Figure 33. The constant *k* can be found from measurements of known composition samples and depends on the excitation wavelength.

The MATLAB software was used to fit Lorentzian curves to each peak visible on the Raman spectrum. The Raman peaks for alloys usually deviate from the Lorentzian fitting, hence areas of

the peaks were integrated for both cases, Lorentzian fitting and raw data, to determine errors. According to the Money equation, the error in the final composition can be given as a propagated error for the equation for the ratio of peaks. The error given for each peak was defined as a percentage difference between the area under the peak for raw data and the area under the peak fitted with Lorentzian curve. All the errors were estimated to be within 5% for the data (up to ±2.5 % for each data point), for the clarity of the graphs they are not included.

3.2.4 Scanning Electron Microscopy and Focused Ion Beam

The characterisation of materials in μm or nm scale require specialized tools to provide information needed for further processing. In nanofabrication, both top view and cross-section imaging are of high importance.

Commonly used Scanning Electron Microscope (SEM) is a type of microscope producing images by using a high energy electron beam to interact with atoms of the inspected material. The gathered data can be used to determine materials thicknesses (especially for cross-sectioned material or side view), topography of the surface and composition. The technique used to deliver cross-section is Focused Ion Beam (FIB) based on a liquid metal ion source (e.g. gallium (Ga) ion source) which is accelerated and focused by an electric field [61]. Many powerful systems rely on the collaboration between FIB and SEM, where the ion-beam system is used to mill the material and afterwards SEM is operated to image the facet of the cut. An example of such a combined SEM-FIB system is shown in Figure 41.

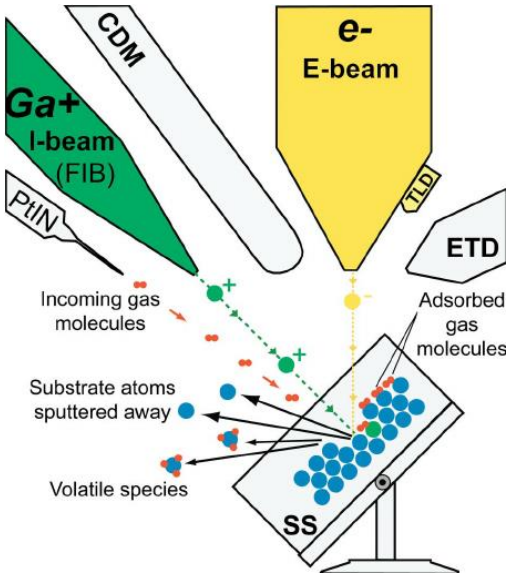


Figure 41 A combined SEM-FIB system with a Ga+ source where ETD, Everhart-Thornley detector; PtIN, platinum injection needle; SS, sample stage; CDM, continuous dynode electron multiplier detector; TLD, through-lens detector [62].

The topology of samples can be imaged by SEM using highly accelerated electrons, which interact in an inelastic way with electrons of the specimen's atoms. The response of the sample is collected and processed by suitable detector and presented as an image on the screen of a computer. Two main interactions of electrons in SEM technique are shown in Figure 42.

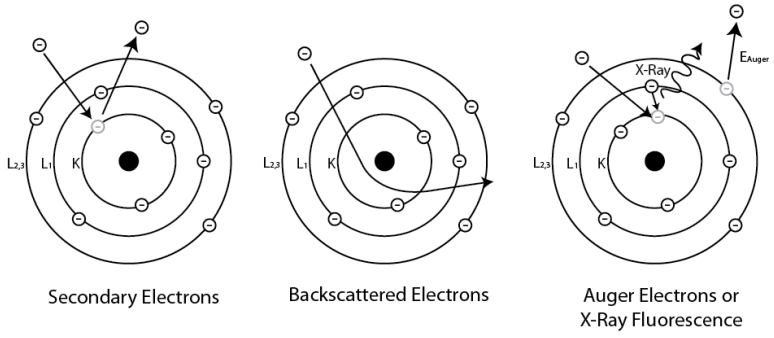


Figure 42 The diagram showing secondary electrons (SE) and Backscattered electrons (BSE) used for SEM imaging. K, L1, L2,3 correspond to electron shells around the atomic nucleus [63].

Secondary Electrons (SEs) will be emitted after inelastic interactions with the K shell of the atom whereas Backscattered Electrons (BSEs) will be elastically scattered with energy depending on the atomic number (Z) of the interacting atom. These kinds of interacting electrons play a key-role for SEM imaging; firstly, SE are especially beneficial for an inspection of the topography of the sample, secondly BSE can deliver information about composition of the specimen as the number of scattered electrons increase proportionally with Z number. The resolution depends on the excitation volume which results in high SE resolution reaching even the range of ~ 10 nm [62].

3.3 Summary

All described methods are used either for fabrication or characterisation of RMG samples. Some of methods (e.g. PECVD for first insulation layer) were used only on the stage of process development, however, leading to the solutions used for the final design. The fabrication was conducted in the wafer scale up to the RTA processing, annealing and characterisation (Raman spectroscopy and SEM) were conducted in the sample scale.

Chapter 4 Design of mask and experiments

This chapter provides a detailed description of the motivation behind the aimed SOI integration of Rapid Melt Growth (RMG) structures and an explanation of the design of the experiment and the process flow. The masks described here were used for process development and finally for obtaining the results described in Chapter 5.

4.1 Motivation for SOI integration

Rapid Melt Growth (RMG) on the SOI platform is a method of delivering multiple compositions of SiGe strips that can be used to fabricate devices e.g. modulators and detectors across the same chip or even within a single structure. The RMG process requires only a single Ge or SiGe deposition and a single anneal step. From an engineering point of view, said integration provides a way to minimize footprint while improving the performance of devices built in the RMG structures. The miniaturization is linked to the ability to create multiple types of devices within the same layer or even the same tailored structure. At the same time, the low number of defects results in a better device performance. The advantage of the RMG technique is also dramatically decreased cost of

fabrication when one anneal step can replace multiple deposition/epitaxy steps, which is the current solution for multiple SiGe composition across one wafer.

As explained in detail in Chapter 2, the properties of SiGe alloys are related to the Ge composition. The material engineering of SiGe structures is linked to the tunability of the band gap and the lattice constant where tailored RMG structures are engineered to tune the SiGe composition along a central structure. A typical application of SiGe material engineering is shown in Figure 43.

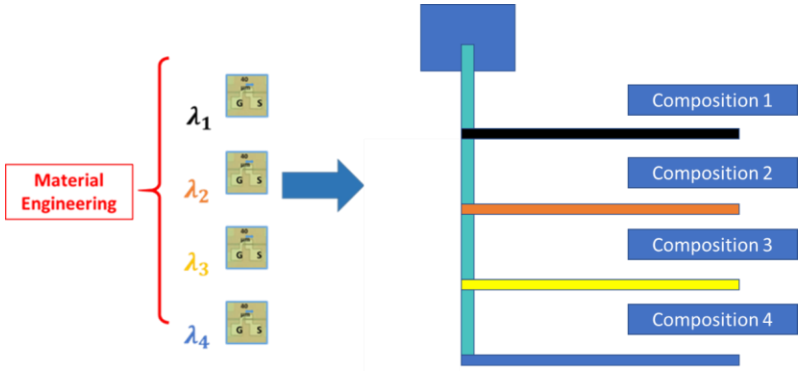


Figure 43 Material and band gap engineering of SiGe to vary the operational wavelengths of EAM modulators (images as an example design, based on work from the research group). The operational wavelength is dependent on the SiGe composition and devices would be incorporated into the structures as shown in the diagram. The composition 1 is designed for wavelength 1 based devices etc.

Devices like modulators or detectors built on RMG structures require waveguide integration. The main methods of coupling light into the photonics devices, e.g. detectors, are butt coupling or vertical (evanescent) coupling [1]. For evanescent coupling, the device is placed on the top of a waveguide, whereas for butt coupling, the device is in contact with a waveguide's facet. For many waveguide integrated applications, the waveguide material is Si and the material of photodetector or modulator is Ge or SiGe. Both, evanescent and butt coupling for Ge structures are shown in Figure 44.

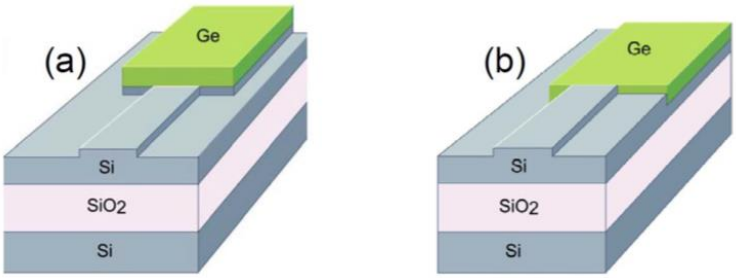


Figure 44 Methods of coupling light from a Si waveguide into a Ge photodetector, a) evanescent coupling, b) butt coupling, reproduced from [2].

A comparison of butt coupling and evanescent coupling for Ge structures is provided with finite difference time domain (FDTD) simulations, which results are presented in Figure 45.

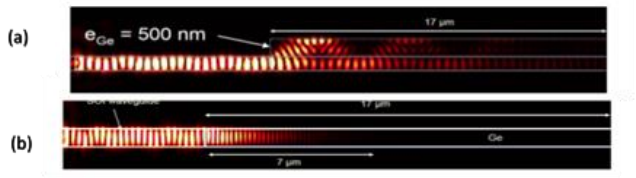


Figure 45 FDTD simulation of coupling light into Ge photodetector at 1.55 µm, (a) evanescent coupling, (b) butt coupling, reproduced from [2].

The FDTD simulations compare the light absorption within the Ge photodetector. The length required to absorb 95% of light in the evanescent coupled structure is 17 µm, whereas the same absorption was achieved within only 7 µm for the butt-coupled structure. Moreover, the thickness of the Ge structures used for evanescent coupling was 500 nm. In order to decrease the length of the device, a thicker layer would be required. A comparison of properties of butt or evanescent coupling were also provided by Silvaco and the results of the simulations are available in [3].

Although the evanescent coupling is easier to fabricate without an additional etch and careful alignment, which are required for butt coupling, the larger dimensions typically lead to a larger capacitance, and therefore, a slower device [1]. Surface planarity is also an advantage of butt-coupled structures, enabling more complex multi-layered systems.

4.2 Process flow

The fabrication of RMG structures on the SOI platform required modifications of the RMG process on the top of the Si platform which was described in detail in Chapter 2. The RMG structures suitable

for butt coupled integration within an SOI platform should be embedded within the Si overlayer and positioned onto the insulating layer to form a direct connection between the Si and the tailored structures areas. The final structures embedded into the SOI wafers were developed throughout multiple test runs. The final integration process of the RMG technique to form SiGe within an SOI cavity is shown in Figure 46.

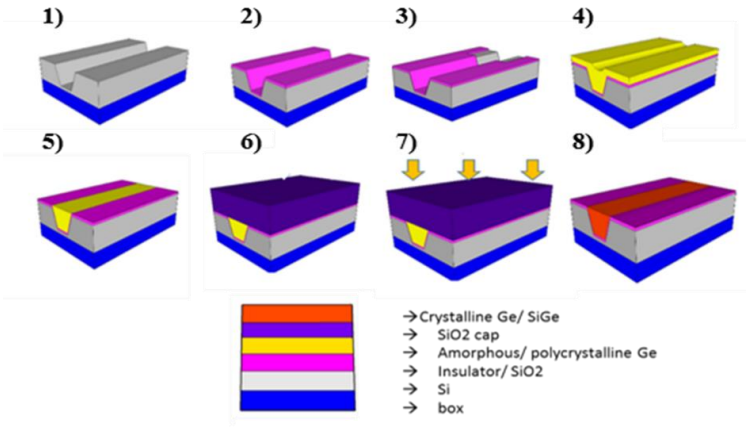


Figure 46 Process for Rapid Melt Growth (RMG): 1) trench creation, 2) insulator deposition, 3) seed etch, 4) blanket Ge deposition, 5) planarization of the Ge layer to wafer level, 6) deposition of the encapsulation layer, 7) RTA, 8) cap removal.

The design with Ge/SiGe filled trenches should be planarized to the Si level which can be achieved with the Chemical Mechanical Polishing (CMP) technique.

The full process flow is attached in Appendix 1, Table 1.

4.3 Mask design

The design of masks for the RMG processing was based on the research of tailored “tree-like structures” on the Si platform [1]. Tree like structures are designated to be integrated with waveguides and used as a base material for active device like e.g. recently reported Franz-Keldysh modulator [2][3] . The active area of the devices reported within this research was within 1-1.5 µm width and 40-55 µm length. Consequently, the stripes of the proposed SiGe tailored structures on SOI platform are designed to allow integration of waveguides and active devices in size as these reported (1-3 µm wide and 60 µm long strips alongside with other structures).

Masks included strips and two main types of tailored (“tree-like”) structures on SOI RMG as shown in Figure 47. The strips are needed to research gradually changeable SiGe composition on the SOI platform, whereas tailored structures with branches are required to achieve a uniform composition and for research on similarities to Si platform and further waveguide integration. The type 1 RMG and type 2 RMG structures can be distinguished based on the position of the strip of the tree-like structure (with added branches). For the type 1 RMG, an additional strip is added, leading from the seed towards tree-like structures. This design is dedicated for the waveguide integration through the strips led by the part with added branches (with desirably constant composition). The seed region was shifted outside the strip area to avoid complications of the waveguide’s design while the seed contains all the defects so it cannot be used as a part of devices. The main strip of type 1 RMG can be linked to changeable amount of tailored structures to accommodate multiple SiGe compositions and consequently be a base for multiple active devices place.

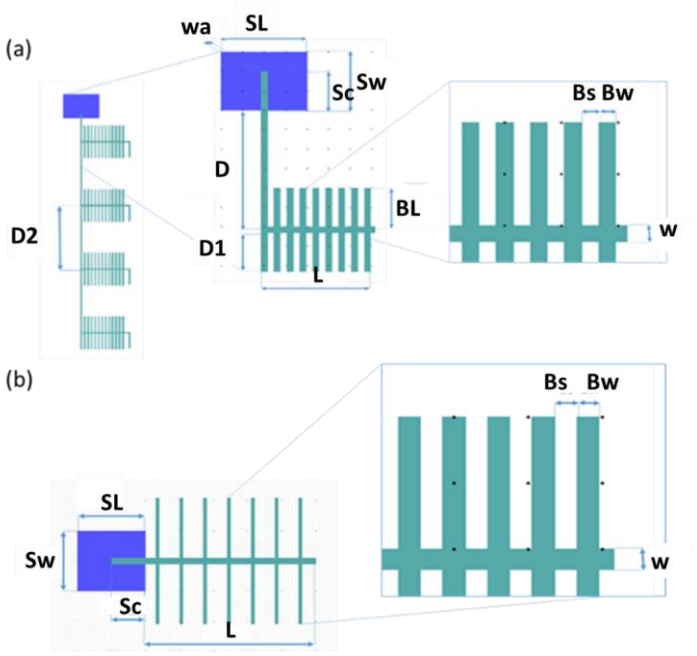


Figure 47 Main types of RMG structures. (a) type 1 RMG for either single or multi- tree structure with the waveguide space designed for main strips of each tree, (b) RMG type 2 for test structures. Description of symbols used to describe design: SL- Seed length, SW- seed width, SC- seed connection with the structure, L- length of the tree-like structure, w- width of the main trench of the tree structure (with branches), Bs- distance

between branches, Bw- width of the branches, BL- length of branches, D- distance between seed and the tree for type 1 RMG structures, D1- distance between the strip of the tree- like structure and the end of the main strip of structure, wa- width of the main strip for type 1 RMG, D2- distance between tree-like structures (branches) for multiple tree structures.

The design of the geometry of the structures included within this mask was based on the results obtained for the analogous structures on Si described in the literature [4, 5, 6] and former test development conducted within this project. The initial parameters were based on the Si results as a starting point. The added branches are responsible for cooling of the structures, which was described in detail in Chapter 2.

The masks presented in Figure 48 and Figure 49 were designed for the 6-inch platform for both Si and SOI wafers, where Si wafers are acting as test wafers for most of the processing. The general layout for 6-inch masks for e-beam and photolithography processing is shown in Figure 48. All masks are compatible with each other which allows integration of waveguides fabricated with e-beam lithography on layers previously patterned with photolithography.

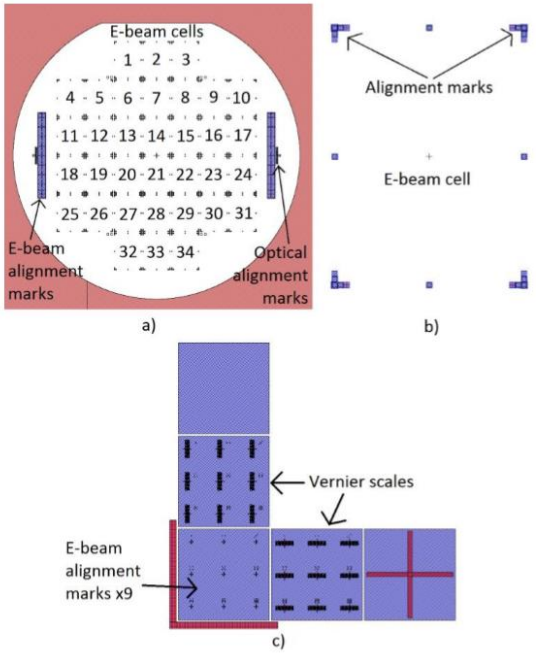


Figure 48 The 6 inch mask template a) the whole template suitable for processing combining optical lithography and e-beam lithography for 34 cells (typical size for e-beam cell), b)

6 typical positions of e-beam alignment marks for a single cell, c) detailed e-beam alignment marks with x and y Vernier scales to measure alignment errors for multi lithography processing. Reproduced from [4].

The first step of the process was performed with either photolithography or e-beam lithography to pattern the tailored RMG structures and alignment mark layers. This design decreases the number of steps due to excluding additional mask with alignment marks only. E-beam lithography was followed by three photolithography; for dummy squares within the same layer as the RMG structures, Si seeds and openings of dummy squares and further Ge etch with protective layer of squares covering previously formed openings. The process flow is presented in Appendix 1 for the sake of clarity. These layers could have been fabricated with photolithography due to less critical shape and dimensions. Dummy squares are included across all the layers to support uniformity of processes such as: Ge/SiGe growth and CMP. The last layer with waveguides was designed for e-beam lithography.

The template of a cell is shown in Figure 41. All cells from the mask were identical which was preferable when uniformity across the wafer is of high importance for processes. Deposition, etch or especially CMP depend either on the uniformity of the layer but also on the position of the cell. Additionally, the Rapid Thermal Anneal (RTA) used to melt RMG structures was carried at the chip level to allow multiple parameters (temperature, anneal peak time, etc.) to be researched.

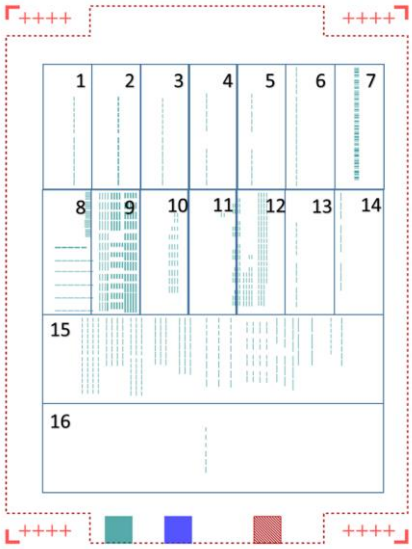


Figure 49 The template of the cell divided into section with various test structures for RMG processing. Sets 1-6, 13, 14, 16 are designed for waveguide integration, Set 7- variety of strips with access to Si seed, Set 8 – strips with branches, Sets 9-15 are designated for material tests for tailored parameters of trees.

Cells 1-6 were designed for waveguide integration by focused grating couplers which are used to ensure more efficient usage of the space across each cell. Nevertheless, the grating couplers are suitable only for a narrow wavelength range.

The parameters of cells 1-6 are presented in Table 6. Across all cells the type 1 RMG was used.

Table 6 Parameters of sets for waveguide integration.

Cell	nA	D, D1 [µm]	W [µm]	aw [µm]	Bw [µm]	Bs [µm]	Comments
1	1	30,30,30;30,90,150	3	3	3	3	Repeated from cell 10
2	1	30,30,30;30,90,150	1	2	1	2	
3	1	30,30,30;30,90,150	2	2	2	2	
4	1	30,30,30;30,90,150	2	2	2	2	L={20,40,50,60,70} µm
5	1	30,30,30;30,90,150	1	2	1	2	Repeated from cell 2 (for Raman)
6	2	30,40,50; D2=30	2	2	1	2	L={20,40,50,60,70} µm
7	4	50, D2=60	3	1	1	3	

13	1	30,30,30;30,90,150	3	3	3	3	Repeated from cell 1 (for Raman measurements)

Cell 7 was designed to research the composition and maximum width of strips embedded into SOI to compare with previous work done on Si platform, where the maximum width of strips not affected by surface tension was limited to 5µm [1][4].

The example of sets included within Cell 7 is shown in Figure 50.

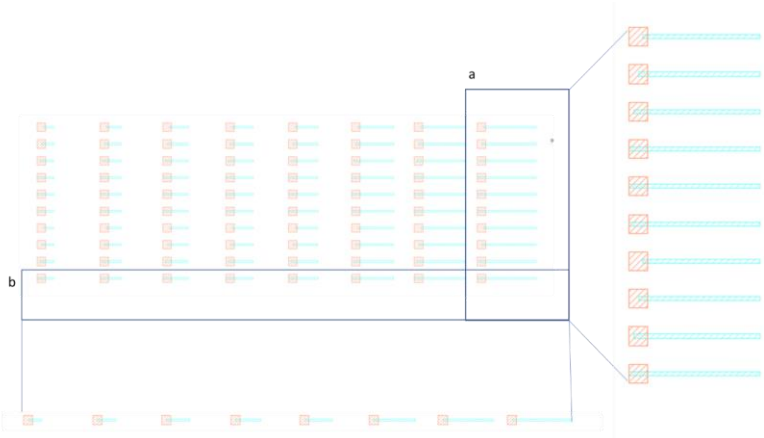


Figure 50 The example of data from the design of set 7; (a) Ge composition vs. seed connection, (b) Ge composition vs. strips length/ Ge composition vs. normalised length.

Set 8 is designed for the comparison of type 2 RMG structures as shown in Figure 51.

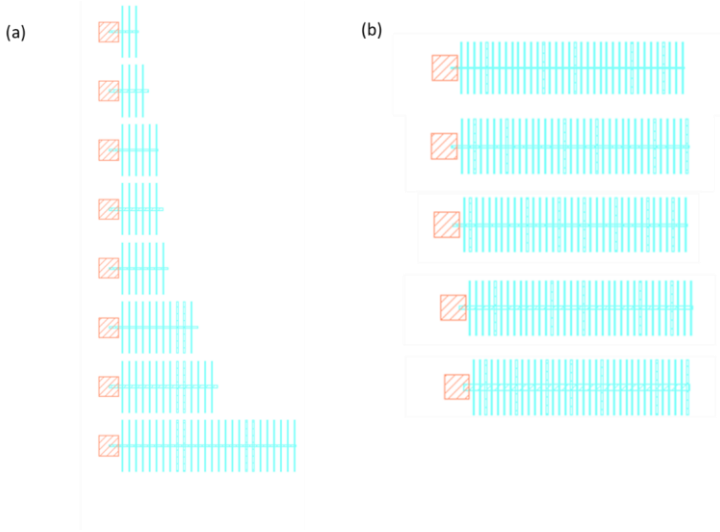


Figure 51 Example structures type RMG1 from set 8; (a) Ge composition vs. strips length/ Ge composition vs. normalised length, (b)varying width of the main strip.

The designed experiments for Ge composition vs. strips length/ Ge composition vs. normalised length and Ge composition vs. seed connection were also done parallel to structures from set 7, where the branches were added with identical parameters of width, length and seed connection as these ones for basic strips. This is meant to confirm the cooling effect of the branches added to the strips for RMG structures on the SOI platform. Besides this, more parameters were compared as shown in Figure 52. The example sets designed to gathered data are also shown in Figure 52 for structures with 2 trees on one main strip.

Figure 52 Example type 1 RMG structures (number of trees, n=2) from set 12. Structures were designed to confirm e.g. an impact of the seed connection on the SiGe composition of main strip, the impact of the width on the composition and to confirm the importance of length of the cooling branches of tree-like structures.

All the sets of the structures were designed to collect the data for specific parameters like branch dimensions, seed connection or distance from the seed for structures embedded into SOI platform. Results are presented in Chapter 5.

4.4 Summary

Masks and process flow described within Chapter 4 were used for the final fabrication after process development runs. The plethora of designs (variations of dimensions) was included to research the RMG process on the SOI platform. The possible difficulties of the fabrication were identified

(predicted) and resolved within the process development described in detail in Chapter 5; the final process flow was based on gathered solutions for undesirable effects.

Chapter 5 Fabrication of SiGe wires on SOI platform

This chapter describes process development leading to formation of constant composition SiGe wires on the SOI platform. One of the most crucial findings of this process development work has been linked to the importance of the shape of the trench filled with SiGe/ Ge on an insulating layer as well as the quality of the deposited Ge layer (from the growth and subsequent chemical mechanical polishing). Within the development of the RMG structures on SOI most issues were identified and solved without a substantial change of mask design.

5.1 Formation of angled Si cavities

The sidewalls of the cavities designed to be filled with Ge/SiGe on insulator were initially straight as shown in Figure 53. The process flow for structures embedded into the Si layer requires the planarization of the layer to the level of the insulator (the red line in Figure 53 indicates this level).

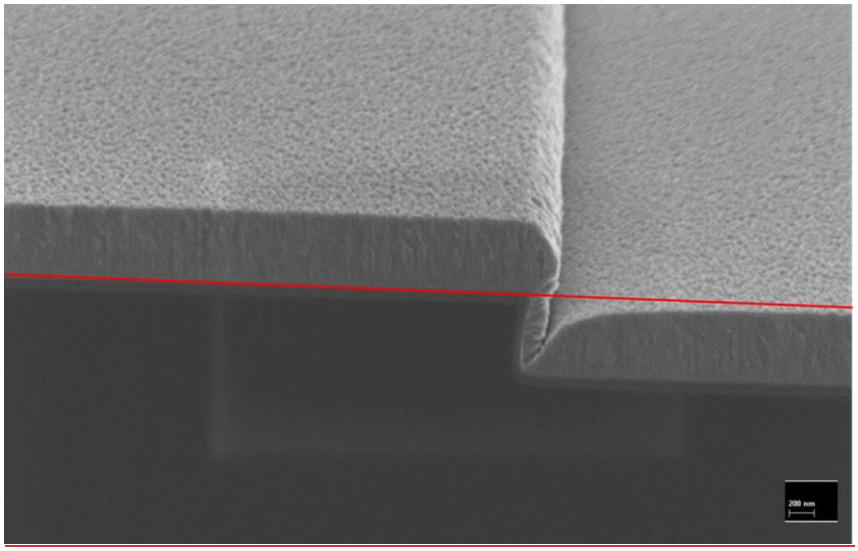


Figure 53 A cross-section of a Si trench filled with Ge showing a lack of material on the sidewall.

The lack of Ge in the bottom corners of the trench is clearly visible from the cross section of the trench. After planarization of these structures, the amount of Ge would not be enough to fill a whole trench after melting (this links to issues with the surface tension describe in Chapter 2 as the surface tension will cause the formation of rounded ends of Ge/SiGe structures or create rounded voids not filled with Ge/SiGe. Additionally, an insulating cap can collapse into voids not filled with material. Each of these issues might cause further complications and epitaxy breakdown resulting in a non-uniform composition across the strip.

One of the issues identified during the first process iteration was the lack of insulator between the Ge/SiGe and substrate layers on the bottom of cavities, especially in corners. This kind of discontinuity within the layer usually causes interaction between Ge and Si during the anneal step, which is undesirable outside of the seed area.

The solution was found by using a wet angled Si etch to shape trenches and subsequently prevent the lack of materials in corners. This modification resulted in more homogenous Ge layer and SiO_2 layer underneath enabling a continuous isolation/encapsulation of the SiGe strips or tailored structures. A comparison of dry etching (vertical sidewalls) and wet etching (angled sidewalls) is presented in detail below.

To compare dry and wet etch results and Ge layer quality after both etch techniques, 500 nm Ge was deposited with a PECVD tool. The structures etched were strips obtained using a standard photolithography mask containing a variety of strip widths, lengths etc.

5.1.1 Dry etch

The dry etch was performed in an ICP tool using the following etch recipe:

- Pressure: 15 mT
- Temperature: 15 °C
- RF Power: 50 W
- ICP Power: 800 W
- SF_6 Flow: 25 sccm, C_4F_8 Flow: 45 sccm

The sidewall angle of the structure after this etch is around 90˚ with slightly wider angle for Figure 54a than Figure 54b which has an impact on the Ge layer thickness which is different for horizontal and vertical parts of the trenches.

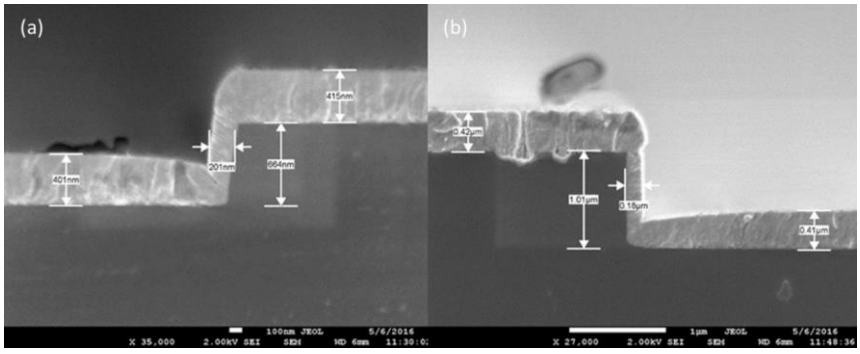


Figure 54 Dry etched Si sidewalls covered with Ge layer; (a) the slightly wider angle (approx. 5 ° from vertical) and shallower trench compared with (b), where the difference between filling of the corners and vertical/ horizontal part of the trench is more visible.

Though, it is possible to obtain the angled sidewalls by using a dry etch, the uniformity across the substrate and repeatability are not reliable enough for subsequent RMG processing.

5.1.2 Wet etch test

Uniformity across the wafer and repeatable results for etching were confirmed with TMAH angled Si etching. As previously for ICP etch, the wet etch process was carried out following deposition of

the SiO_2 and Ge layers. Due to the high selectivity of TMAH based solvents between Si and SiO_2, an HF 20:1 dip (5 seconds) for each sample was necessary before the TMAH etch. Wet etching was performed with 25% TMAH at room temperature (no additional heating) for 3 etch times: 30, 40 and 60 minutes. This concentration of TMAH at room temperature enables a relatively slow etch (theoretical etch rate around 8.8- 9 nm per minute for 54 °angle). Variation of the etch rate and sidewall angle are possible by varying the TMAH concentration.

For samples prepared for this test, the time needed to etch throughout the 400 nm Si overlayer (all samples were obtained from SOI wafer with 2 µm buried oxide (BOX) and 400 nm Si overlayer) was calculated to be 45 minutes. After analysis of results, the etch rate was confirmed to be 9 nm/minute at room temperature and 45 minutes is exactly the time needed to etch 400 nm Si. The sample exposed for 60 minutes in TMAH was etched fully without a further undesirable undercut effect; the 30 minutes etched sample confirmed the possibility of control of the process in case a specific thickness of Si overlayer is required for further processing. The sidewall angle and etch rate are both accurate and repeatable enough for the requirements of this experiment. Images of the etched trenches are shown in Figure 55.

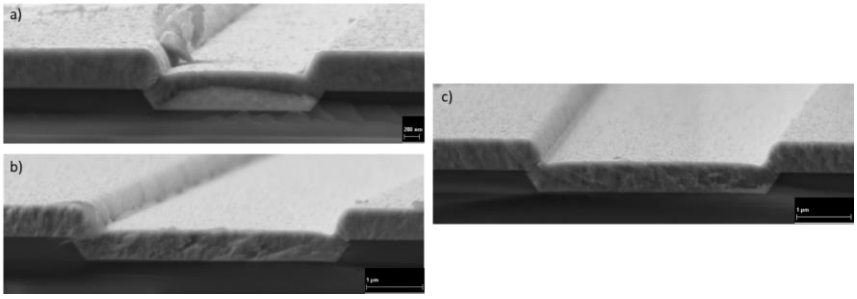


Figure 55 SEM images of the TMAH angled etched trenches filled with Ge; (a) 30 min TMAH etch, (b) 45 min TMAH etch, (c) 60 min TMAH etch.

5.1.3 Wet etch tests for tree-like structures

As mentioned previously, the lack of SiO_2 in the cavity corners can be indirectly identified during the Raman measurements of the RMG Ge layers or be visible by microscopy characterisation of the structures after RTA. The Si and Ge leakage from within the structures can be identified through FIB cross- section as intermixing between the Ge and Si in the corners as well as unexpected fluctuations of SiGe composition across the structures calculated after Raman analysis. Examples of non-continuous layers are shown in Figure 56.

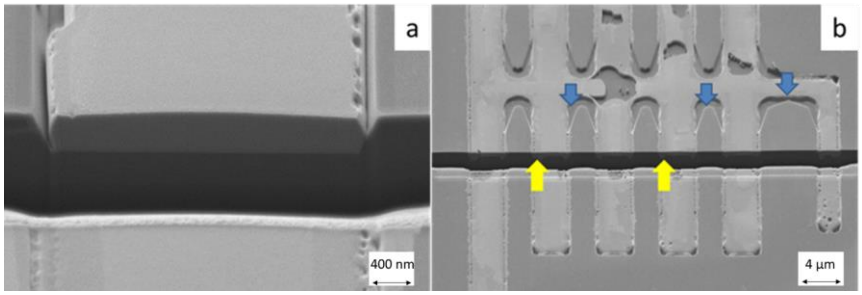


Figure 56 Tree-like structures obtained during process development for batch 1- after the RTA step, leading to identifications of possible issues linked to either photolithography or/ and, described here, trench etching; (a) the rounded shape of not entirely filled trench, (b) structural defects visible after SiGe melt- yellow arrows point the Ge and Si intermixing region due to non-continuous insulating layer between Si and Ge, whereas blue arrows indicate issues associated to photolithography and trench etching.

In Figure 56a, the border between Ge and Si seems continuous without the obvious leakage like the one visible in Figure 56b. It might be a proof of achieving the full continuity of the insulating layer or just a specific place without the intermixing issue as the insulating layer can be non-uniform across the structure and might not show signs of leakage along the entire length.

The TMAH etch was first tested on strips where the orientation was adjusted to directional (anisotropic) character of the etchant. The structures with corners (including tailored structures with branches) can also be affected by the directional etch.

The test structure obtained for test in Figure 56b was fabricated using photolithography, masking the SiO_2 layer for etching after photolithography, PECVD insulating layer to prevent intermixing between Si and Ge and TMAH angled etch for trenches. To resolve the addressed issues, the following development processes were necessary:

- Photolithography optimization to avoid rounded corners of the structures,
- The etch recipe tests to avoid the change of designed straight angles across tree-like structures. The TMAH etch is anisotropic which partially explains the shape of 'corners' visible in Figure 56b,
- Preventing issues on the interface between Si and Ge due to a non-continuous underlaying PECVD SiO_2 layer

Chapter 5

Based on the results obtained from the initial stage of process development, further work on the creation of angled sidewalls was performed and will be referred as Process development Batch 2. Firstly, it should be mentioned that the thickness of the insulating layer covering the trenches was increased to 50 nm which doubled the value of an analogous layer from wafers in Batch 1. This change ensured improved coverage of corners, even for partially filled structures, and also prevented over-etching during the Ge deposition (which required HF etching prior to deposition to remove native SiO_2 from the seed area). Modifications of the angled etch for trenches are detailed in Table 7.

Table 7 The parameters for wafers from the development Batch 2. Wafer SOI1 was broken during CMP.

PROCESS	WAFER	ICP etch depth	TMAH etch depth [nm]	PECVD SiO_2 thickness within the trench [nm]	PECVD SiO_2 thickness around structures [nm]
1	SOI1, SOI2,	-	300	50	50
2	SOI3, Si5	300	<100	50	50
3	SOI4	-	350	50	50+70=130

The idea of process for wafers from Batch 2 is also presented in Figure 57. The main difference was related to the creation of the trench and modifying the insulator layer. The hard mask caused issues during wet etch and additionally, it had an influence on directional etch. The trench creation was researched for the design based on either TMAH directional etch or combination of wet and dry etch.

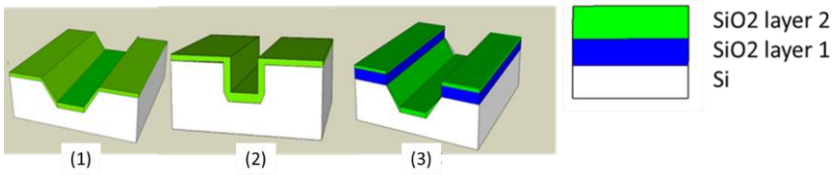


Figure 57 The shape of trenches for various wafers from Batch 2; (1) wafers SOI1, SOI2, (2) wafers SOI3, Si5, (3) SOI4.

The results for test development batch 2 obtained from the fabrication described in Table 7 and in Figure 57 are shown in Figure 58.

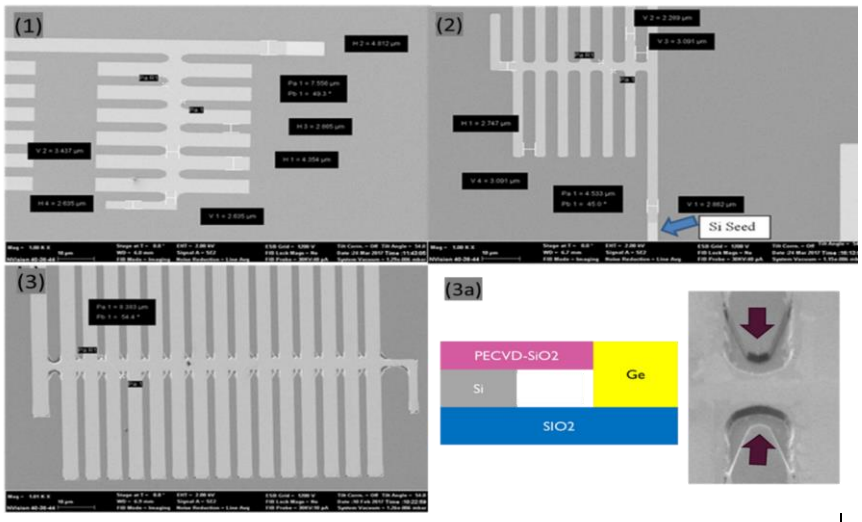


Figure 58 Comparison of main strip and associated branches for after the CMP step for process (1) SOI2, (2) SOI3 and (3) SOI4, (3a) explanation of the undercut effect occurring in the corner of structure (3).

The general summary of structures fabricated with either TMAH only or mixed TMAH/ICP ensured an impact of the etch on the shape of the corners and the number of voids in the Ge layer. The voids visible in Figure 58 for process (3) are caused by undercut occurring through the subsequent HF and TMAH etching as explained in Figure 58 in diagram (3a). The HF dip necessary before the TMAH etch should be conducted carefully (not longer than 1 s dip and in-depth water cleaning afterwards) to avoid the presented effect. The way to prevent any impact of residuals from

undercut SiO_2 layers is full removal of this layer after etch and deposition of the new SiO_2 layer across the whole wafer. In Figure 59, the importance of the undercut effect and rounded shape of structures corners is explained further.

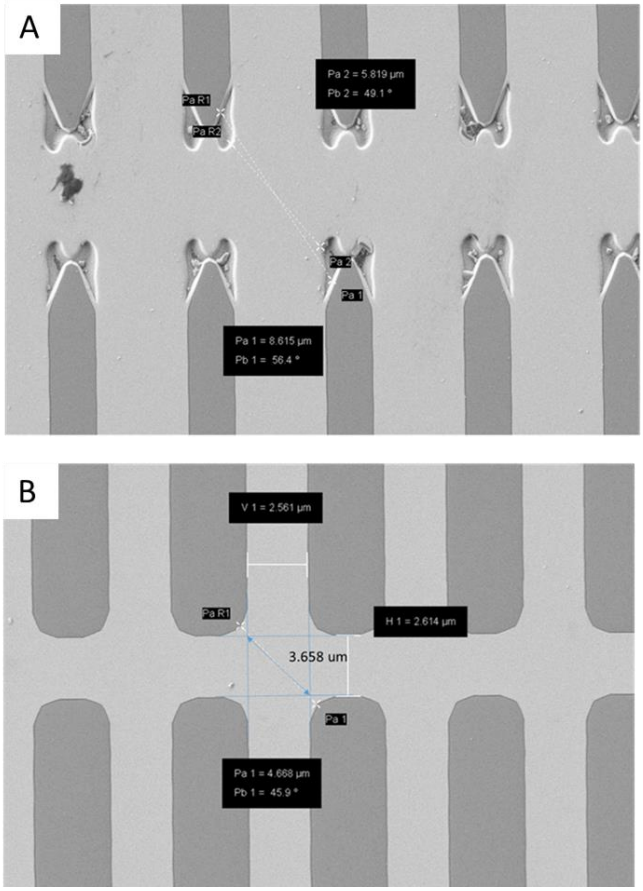


Figure 59 Measurements of the diagonal between opposite branches compared with minimum distance between these branches indicates significant difference and room for possible improvement of the final shape. Structure A is fabricated as mentioned described in process (3). Structure B is fabricated as mentioned described in process (2).

From Figure 59, one can observe that there is a significant size difference of more than 25% (1 µm) between achieved and theoretical minimal size of crossing for widths of measured branches for Wafer SOI 3. It is worth adding, that if the gap between fins is too big, it can be a reason for surface

tension appearing later on (during RMG) and affecting Ge structures, as was mentioned in the theoretical background chapter of this thesis. Further process development should be focused on bringing the achieved shape and size of the structures closer to the original design.

The coverage of the corners of the trench filled with Ge is visible in Figure 60. This result can be compared with the results initially presented Figure 53, where voids in corners were clearly visible.

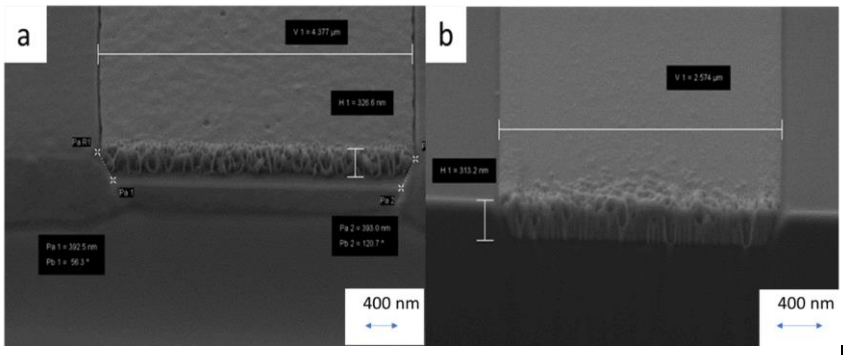


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Figure 60 A cross-section of the structures fabricated with ICP/TMAH etch; a) with the 5 µm main strip from the Wafer SOI3, done after RMG step, b) a cross-section of the 2.5 µm strip from Wafer Si5.

Based on the results from the development test performed for wafers from Batch 2, optimal processing for further creation of angled trenches and tree-like structures was chosen to be a combination of TMAH and ICP etch. The combined ICP/ TMAH etch for the Si layer led to the closest to the straight angle corner (from the top perspective). The ICP/TMAH etch depth ratio was 3:1 (300 nm to 100 nm Si) whilst the angle of Si etch was measured after FIB cross-section as 120˚. The optimized etch brings the shape of the obtained structures closer to the originally designed shape and minimizes the number of voids within corners. These conditions can be successfully used for the Si etch for further fabrication. However, the limitations of optical lithography will most likely be visible as rounded corners or changed size compared to the design (depending on the development, exposure and resist used). Section 5.3 below focuses on the process development of a lithography technique suitable for the tree-like structures embedded into an SOI platform.

5.2 CMP

The RMG process for SiGe tree-like structures embedded into SOI wafers requires planarization to the level of the top of the Si, filled with either Ge or SiGe. The initial CMP process and training on

CMP technique was conducted in collaboration with VTT in Espoo, Finland, to enable further continuation of processing at the University of Southampton facility. The processing for CMP on RMG structures consists of three stages: Batch 1 with only Si wafers was leading up as a test before the work with SOI wafers, Batch 2 with Si and SOI wafers (training on CMP) and Batch 3 processing in the cleanroom of University of Southampton.

To conduct CMP work on tree-like structures the following factors need to be considered:

- The presence and size of structures and spacing between branches (compare to Chapter 4 with mask description- Bs, Bw),
- RMG structures embedded within Si layer require precise control of the CMP stop point. The thicknesses of insulating layers and structures are within the range 100-600 nm which might be easily overpolished if removal rate (RR) of CMP will not be slowed down from standard reported values for pure slurry [1],
- the necessity of multilayer dummy structures design for uniform distribution of features across the wafer.

5.2.1 Batch 1 – process developments for 6-inch Si wafers

The process development batch was meant to gather data about CMP for tree-like structures and dummy structures surrounding them which will be used for the SOI batches. The general aim for this CMP test is shown in Figure 61.

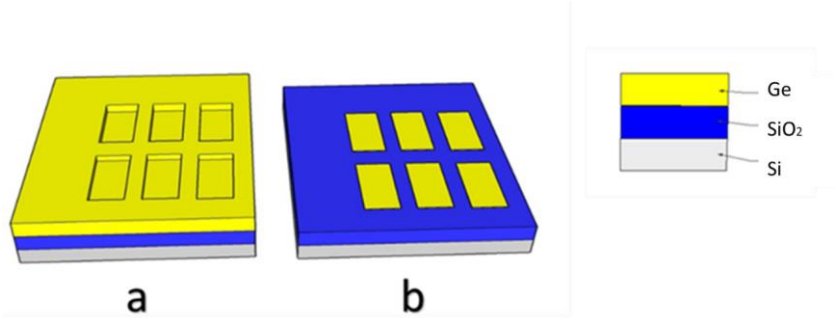

Figure 61 The CMP aim for batch 1; a) the substrate covered with Ge before CMP, a difference be-tween trenches and surrounding layer is clearly visible, b) the substrate planarized to the level of embedded structures.

The surface of each test wafer was covered with a uniform Ge layer with the thickness in range 400-600 nm. The stop layer for the Ge CMP was the PECVD SiO_2 layer (underneath the Ge layer,

surrounding tree-like structures), with a thickness aimed to be 100 nm. The aim of the CMP process was to remove the Ge from the areas not in the trenches and stop polishing/ planarization on the SiO_2 stop layer, leaving Ge only in the trenches. Due to the relatively large size of the features (in range from 1 µm for trees to 50 µm for dummy squares) and a clear contrast between Ge and SiO_2/ Si surrounding structures, the effect of CMP is visible via optical microscopy examination. The SiO_2 thickness around the Ge structures was investigated by Reflectometer FilmTek 2000M, although a reliable value was only achieved when the layer was smooth enough. The Ge-based structure profiles have been measured by "Dektak" Surface Profilometer after each CMP step to test for proper planarization. The thickness of Ge was determined based on indirect measurement from profilometer and height differences between the SiO_2 layer and Ge trench/feature (depending on the stage of CMP). The wafer bow was measured on an ADE 9500 UltraGage to test for stress in the Ge layer.

Polishing of Ge covered substrates (wafers or samples) can be performed using a variety of slurries, including Cabot W2000 or G1000. The slurry used for this thesis for Ge CMP was Cabot W2000, designed originally as a metal slurry for Tungsten (W), diluted 1 to 1 with DI water and with 0.5% H_2O_2 added. Afterwards, the wafers were cleaned carefully with DI water only. This slurry is recommended as a slurry for blanket wafers due to a high polishing rate (200-600 nm/min) but it can also be used for patterned wafers if diluted with deionised (DI) water [2]. Alternatively, the Cabot slurry G1000 is intended for low density patterned designs [3]. Therefore, mentioned low percentage addition (<5%) of H_2O_2 to the slurry/ DI water increases the rate of Ge CMP through enhanced GeO_2 creation [4][5].

Parameters of the CMP process are listed as the following:

- Downforce = 3 psi
- Carrier Speed = 79 increased to 149 RPM after the first wafer
- Table Speed = 83 increased to 151 RPM after the first wafer
- Slurry Flow = 120 ml/min
- Slurry Cabot W2000 diluted 1:1 with DI water and H_2O_2 added to the slurry

Severe erosion seemed to occur within Ge structures of the first wafer during CMP with lower carrier and table speeds, so value of both was increased for the following wafers to avoid this effect.

Cells across the wafer can be polished with different rates due to the wafer bow, with greater pressure and faster polishing on the edges than in the middle of the wafer [6]. To maintain control over the Ge removal rate, the structures from across the wafers (cells 7, 14 and 28 as shown in Figure 62) were measured with profilometry and reflectometry before and between the steps of

the CMP (1 to 3 steps per wafer). A map of the wafer with results for various locations are shown in Figure 62.

Results are in good agreement with the prediction as the polishing rate is slower in the middle of the wafer (cell 14) and this is proven by visible Ge left between structures and dummy squares, whereas for more distant cells (cell 7 and 28) Ge deposited between trenches was removed. The underlaying PECVD SiO_2 layer was also partly polished with a measured SiO_2 thickness of 10 nm less than at the beginning of the CMP process. The non-uniform polish rate across the wafer is an issue as the yield of fully polished cells is lower than expected.

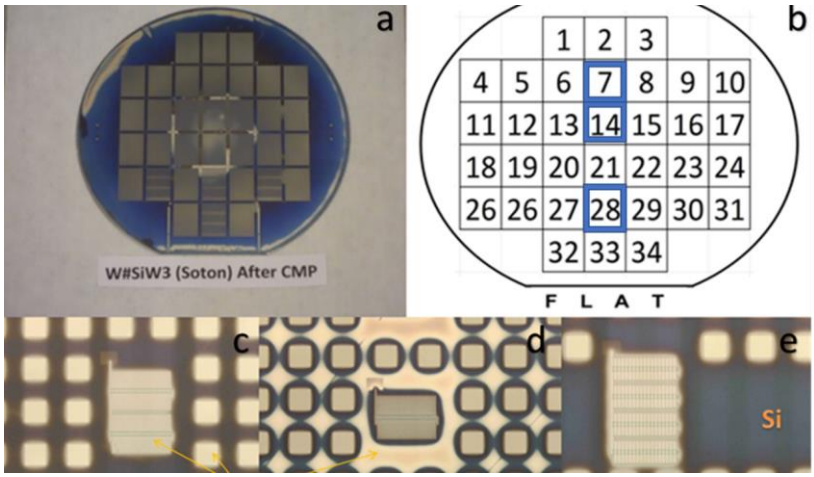

Figure 62 The Si W3 wafer after CMP; (a) the wafer after CMP, (b) a map of the wafer with the number assigned to all cells, (c) Chip 7, (d) Chip 14, (e) Chip 28.

The wafer bow was measured before and after CMP, showing a consistent trend of decreasing bow value for all wafers after CMP (bow in range 29-40 µm before CMP and 4-11 µm after CMP) due to the fact that the blanket Ge layer has been broken, therefore relieving the stress. The pressure applied during processing minimised the wafer bow whilst the polishing was taking place.

Between CMP steps, Ge seems to peel off (delaminate) in many places, especially in the dicing lanes which is likely to be connected to H_2O_2 added to the slurry which etches the Ge layer.

It was found that the polishing rate for dummy squares is lower than for tree-like structures (dummy squares and Ge covered spacing between them) due to a significantly bigger area than the tree-like structures. An improvement of this design was based on these results and other work on pattern density dependence reported in [7].

Based on the profilometer measurements, structures were polished within an average height difference of approximately 10 nm between the middle and the edge of the main strip of the structure (measured for structures from each cell) and more than 50 nm between average measurements for structures from cells 7 and 28. A non-uniform pattern density for the polished structures can lead to an effect called dishing which has been reported to be affected by pattern size and trench width [8].

To successfully perform the RMG, Ge or SiGe-filled trenches should be fully defined without this material left around the trench. At the same time, the structures should be still surrounded by the underlaying insulator to assure stopping CMP before over-polishing, which is defined by reaching Si. As the removal rate is faster on the edge of the wafer, the time of planarization should be optimized to stop it when there is no Ge left between the structures in the middle of the wafer and the SiO_2 layer underneath the structures is still present for cells located on the edge of the wafer.

Overall, based on the first CMP results, the SiO_2 thickness should be either increased to protect Ge within the trenches and the underlying layers during CMP, or the polishing rate should be decreased for a better control of the process.

Non-uniform polishing across the wafer can cause loss of test die across the wafer as they are not suitable for subsequent RTA because Ge left between structures can negatively affect further processing during anneal and waveguide integration for the following reasons. Firstly, Ge randomly left on the SiO_2 (without access to Si seeds) can create spherical voids during the anneal process due to surface tension between the Ge and SiO_2. Secondly, waveguides are designed between structures within the Si layer, so remaining Ge areas located on top of the Si must be removed before the waveguide etching step.

5.2.2 Batch 2 – process developments for 6-inch wafers

In light of findings from process development of Batch 1, a second batch was fabricated with a modified process as shown in Figure 63. The main modification was the introduction of an ICP etching step for the removal of the Ge surrounding the tree-like structures prior to the CMP step. In this way there is significantly less Ge to be removed in the CMP step, resulting in a more controllable and repeatable process without the risk of unwanted remaining Ge.

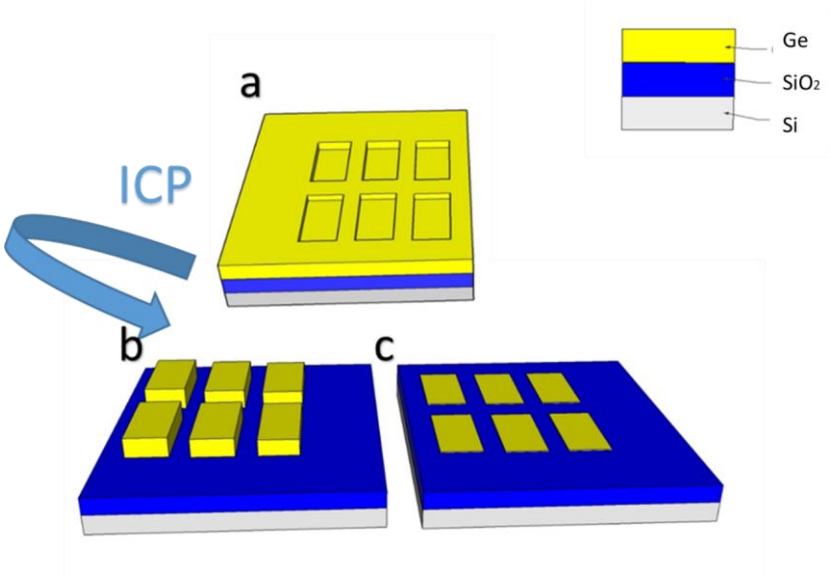

Figure 63 The CMP process for batch 2; a) a substrate covered with Ge before CMP with clearly visible difference between levels of trenches and surrounding layer, b) the substrate after an additional photolithography and subsequently coming ICP etch to remove Ge between the trenches, c) the substrate planarized to the level of the embedded structures.

The profiles of structures across the wafers were controlled before and between the CMP steps (the total number of steps varies between 2 and 5 for each wafer). The location of cells controlled for Batch 2 is shown in Figure 64. The location of cells was changed comparing to Batch 1 in order to increase the distance between cells and improve the uniformity measurement across the wafer. Analogously to Batch 1, the characterisation of wafers was based on measurements of SiO_2 thickness next to the Ge structures (by Reflectometer) and the structures' profiles ('Dektak' Profilometer).

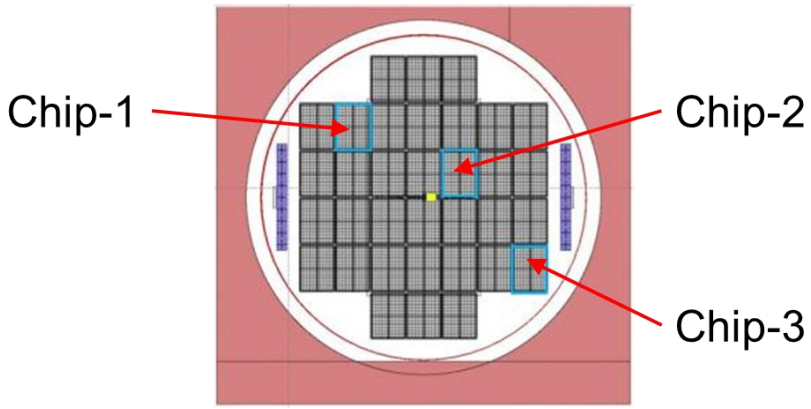

Figure 64 The mask template with the location of the cells used to control the CMP process.

During the CMP processing, SOI wafer number 1 was broken and was not processed further. However, the rest of wafers were planarized until the Ge structures were level with the SiO_2.

Parameters of the process are listed as follows:

- Downforce = 3 psi
- Carrier Speed = 47 RPM
- Table Speed = 53 RPM
- Slurry Flow = 120 ml/min
- Slurry Cabot W2000 diluted 1:1 with DI

Parameters were adjusted based on results for Batch 1. The slower speed (for carrier and table) was used to slow down the CMP process and allow to control the process even with an increased pattern density- after adding Ge etch mask, compared to Batch 1.

The slurry used for the Ge CMP was Cabot W2000 diluted 1+1 with DI water. H_2O_2 has been excluded due to delamination of Ge reported for CMP of Batch 1. Additionally, H_2O_2 also increases the polishing rate of Ge [9][10] and a high polishing rate is not needed for the thin layers in batch 2 with a low Ge coverage due to the new patterned design, which was meant to increase the polishing rate [7].

The initial and final thicknesses of SiO_2 across the example wafer are shown in Table 8. A significant amount of PECVD SiO_2 was polished away across the whole wafer, with even no SiO_2 left in some areas. Without the SiO_2 layer (stopping layer), the Si layer would be polished away along with the Ge structures, which would inhibit the performance of the waveguides which are to be etched as

the final processing step. The selectivity of the CMP between Ge and PECVD SiO_2 is around 2:1 (meaning that 200 nm of Ge was polished at the same time as 100 nm of PECVD SiO_2).

Table 8 Results for wafer Si3 (Si test substrate) with an insulating SiO_2 layer surrounding tree-like structures, before and after CMP. This data provides information about PECVD SiO_2 uniformity across the wafer and minimised wafer bow after processing.

WAFER	CMP TIME [s]	CHIP-1 SiO_2 [nm]	CHIP-2 SiO_2 [nm]	CHIP-3 SiO_2 [nm]	Wafer bow [µm]
Si3	0	94	96	105	15
Si3	420	43	14	0	8

The initial values of the wafer bow were much lower for Si wafers which had been processed with a Ge ICP etch compared to Si wafers covered with blanket Ge (Batch 1). The bow measured for Batch 2 was found to be around 15 µm compared with around 30 µm for Batch 1. The final values were comparable for both Batches.

The bow measured for SOI wafers was much higher than for Si wafers, even between 30 and 50 µm for each SOI wafer. The possible reasons for the high bow for SOI wafers have been presented in the literature [10], but it is apparent that the bow of a virgin SOI wafer is high according to the wafer specification from the wafer manufacturer.

Profilometer measurements were carried out to identify a profile variation within the tailored structures from wafers from Batch 1 and Batch 2. For Batch 1, dishing was commonly observed, while for Batch 2, the shape was convex. Structures (trenches) and surrounding them area from Batch 1 were evenly covered with the layer of SiGe or Ge, whereas for Batch 2, areas surrounding trenches were etched to the level of SiO_2. The accuracy of photolithography allows around 1 µm of margin around structures so overgrowth of the design was set to 1µm from any direction. The reason of the profile after CMP to change was a difference with access to the edges of structures for both batches. The area of spacing between structures, designated to be uncovered, is much bigger than area of branches or strips. This led to a difference in the polishing rate, higher for smaller regions like tailored structures (either stripes or branches). The slower planarization of area surrounding trenches with simultaneous faster planarization of branches is causing mentioned earlier dishing along structures and material left between structures. Waveguides are designed to be fabricated exactly between dummy squares, where material is not removed if additional mask for etch is not added. To sum up, process of Batch 2 was significantly more adjusted to the design's needs as Ge had been removed from all undesired areas, including spacing between the branches

of the tree-like structures. At the same time material within trenches were not over-polished. An example of Wafer from Batch 2 is shown in Figure 65.

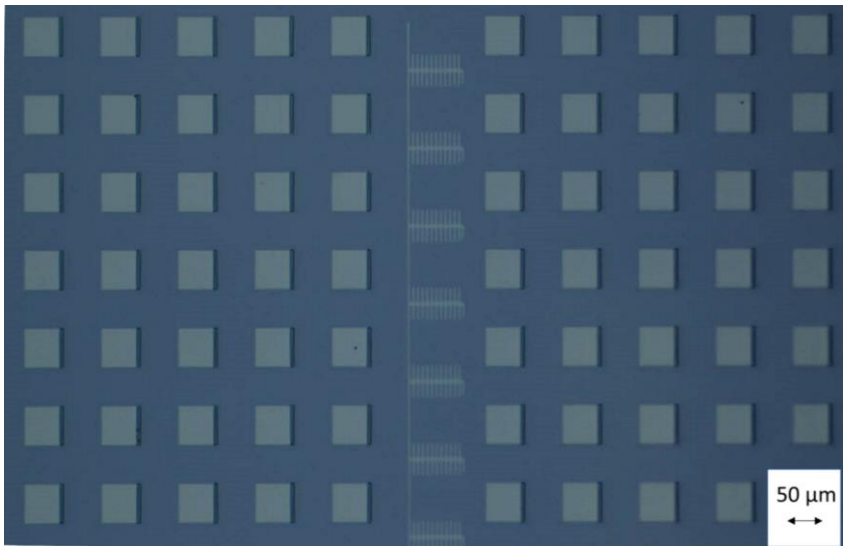

Figure 65 An optical microscope image of the surface of the wafer SOI 3 with tree like structures and dummy squares after CMP.

The result shown in Figure 65 can be compared with results for Batch 1 presented in Figure 62, where Ge between dummy squares and branches is still clearly visible due to not fully polished wafers.

A summary of the findings from the CMP process development performed on Batch 1 and Batch 2 are listed below:

- the uncovered PECVD SiO_2 can be problematic as it is too fragile to be a stop layer for Ge CMP. A denser thermal oxide layer could be used instead, although this consumes Si and would result in a thinning of the top Si overlayer, which will affect the waveguide and other devices performance,
- the size of dummy squares should be adjusted to match the size of the structures to be polished,
- parameters of the CMP tool (force applied on the back of the wafer, carrier speed) and slurry (concentration, other substances added to commercially available slurry) should be adjusted carefully when processing requires precision due to thin Ge and insulator layers,

- dummy squares and tailored structures should be fabricated in the same way; fabrication within 3 layers to allow uniform growth, planarization and RTA,
- the additional mask just before CMP to remove the Ge around structures is found to be beneficial for CMP performance.

5.3 Lithography

RMG processing requires minimum two layers to fabricate; structures on insulator and seeds. To adapt the process for the SOI platform, the trenches were etched first into the Si layer together with the dummy squares. After this step, an insulator layer was deposited, and it was followed by subsequent lithography for seed etching together with selectively removing the insulator from the dummy squares. After Ge deposition, the final lithography was designed to protect the Ge structures so that an etch step can remove the unwanted Ge before the CMP step.

Lithography was used for 3 steps of processing as shown in Figure 66 and Figure 67. The design was adjusted to account for the alignment accuracy of the photolithography with a tolerance of 1 µm for the second and third layers to cover the underlaying structures.

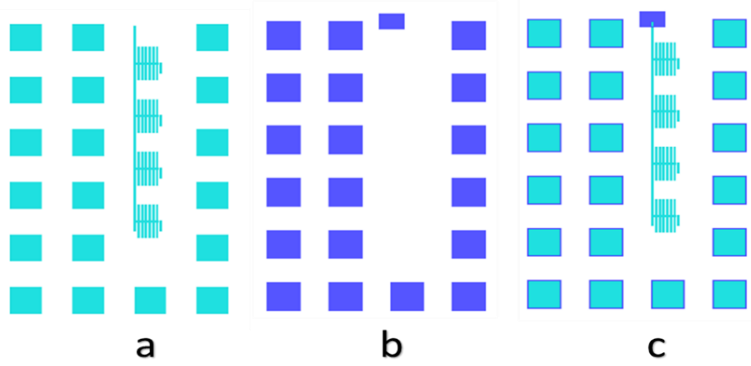

Figure 66 The layout for RMG structures; a) Mask 1 and tree-like structures and dummy squares, b) Mask 2 with seeds and another layer (to etch SiO_2) of dummy squares, c) the final structure after the photolithography 1 and the photolithography 2.

As mentioned in Section 5.1, process development of lithography can lead to general improvements of the shape of the structures patterned onto the substrate. Process development for photolithography is based on parameters like exposure time, using either contact or non-contact masks, or development time.

The findings from CMP processing led to another mask as shown in Figure 67. The mask was used before CMP process to remove material surrounding structures and dummy squares. From process development point of view, it is important to consider accuracy of the photolithography in range of 1µm and rounding shape of squares after typical for photolithography processes. The size and shape of structures after photolithography can be modified by just mentioned parameters considered for process development.

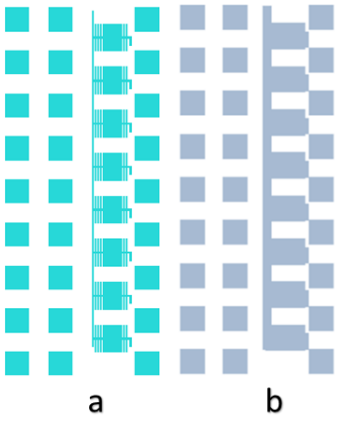

Figure 67 Lithography mask for process (a) is designed for tailored structures to be etched into the Si layer along with dummy squares during Photolithography 1. Lithography mask (b) is used after filling trenches with Ge/SiGe and etching seeds, the structures should be planarized as described in Section 5.2. The negative resist used for this design assures that all surrounding areas are etched, and that the trenches and dummies are protected from the etch.

Finally, the shape of the tailored structures was challenging to achieve using contact photolithography processing. The dimensions of the branches or strips, and the spacing between cooling branches, were within the range of 1-5 µm, challenging abilities of contact photolithography. As shown in Figure 68, the shape of the branches varied depending on the lithography technique used. Multiple photolithography processes with varied exposure time, development time or substrate contact with the mask (either contact or non-contact lithography) were examined with the final effect shown in Figure 68a.

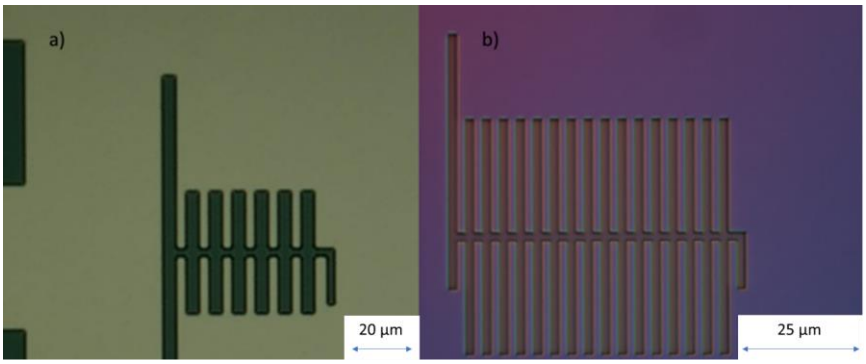

Figure 68 The photolithography ((a) for 1.8 sec exposure time, 40 sec development) results in rounded corners of the design with straight angles, whereas the structure obtained by e-beam (b) is in good agreement with designed structures.

The e-beam technique was ensuring the most accurate transfer from the design into the fabricated structures, based on the described process development for photolithography and e-beam lithography. The shape of the corners had an impact on the results from other processes like wet directional etching of either Si or SiO_2, which were especially visible after finishing the RMG processing.

Photolithography is significantly cheaper and faster than e-beam lithography, however, the technique compromised the shape of tailored structures in significant way. The SOI integration demanded RMG structures to be embedded into Si layer and patterns obtained after lithography had a direct impact on the result. Therefore, the e-beam lithography was required to meet design expectations.

5.4 Process development summary

As a summary of the process development, the following findings can be listed:

- all processes used for SOI integration of RMG structures impact the final effect in a significant way. The rounded shape obtained after photolithography was enhanced by directional wet etch causing increased difference from the designed shape. Even if rounded corners didn't have such a high impact on the tailored structures on Si, the results on SOI show less tolerance when the tailored structures were etched into the Si layer instead of being on the top of the Si layer.

- The CMP process required modification of the mask and the design to achieve the final effect of cleared areas around structures and not over polished structures. The dimensions and thicknesses were challenging for CMP where the slurry is usually designated for polishing more material in the short time.
- E-beam was the method of choice for defining the tailored structures. However, time and cost of processing were not ideal and left a room for improvements.

5.5 Constant composition SiGe/Ge wires on SOI platform

Based on the process development described in detail in the earlier sections of Chapter 5, a range of structures were fabricated to demonstrate RMG integration to the SOI platform. The modifications of the processing leading to constant composition SiGe/ Ge wires embedded in the silicon overlayer are presented in this chapter.

5.5.1 Fabrication

The fabrication was carried out on 6'' SOI wafers (400 nm Si, 2µm buried SiO_2) and Si test wafers. For the most effective photonics devices the RMG SiGe/Ge layers must be embedded within the Si layer to enable butt coupling to Si waveguides. To achieve this, the first step was the deposition of a 50 nm thick SiO_2 hard mask using plasma enhanced chemical vapour deposition (PECVD). The hard mask was then patterned using electron-beam lithography to deliver the desirable shapes for the cavities of the proposed structures. The cavities within the Si layer were etched using combined dry and wet etching techniques to obtain an etching depth varied between 100 and 300 nm with an angle of 54.3°, as a result of the TMAH etch. To avoid issues caused by under etching of the silicon, the hard mask was fully removed after this step. The insulating SiO_2 layer was than replaced across the whole wafer using dry oxidation of the Si layer. This step could be done by PECVD, however, this process would demand additional actions like thermal dehydrogenation and densification, as shown in the previous chapters. After the insulator formation on the whole wafer, the openings for the Si seeds were etched through the oxide. To achieve this, the substrates were patterned by contact photolithography and wet etched with HF etchant (diluted solution, 20:1). This step was used to expose the Si underneath and on the sidewalls of the trench-seed connection in the seed region as shown in Figure 69.

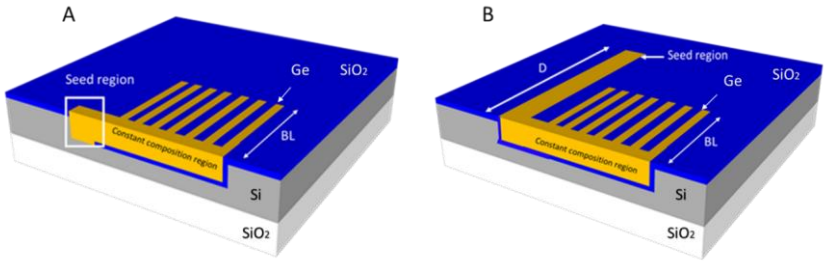

Figure 69 The diagram of (A) RMG1 type structure with selected seed region and branch length, BL, and (B) RMG2 with selected branch length and distance from the seed to the strip with constant composition, D.

A non-selective SiGe deposition was performed by using low-energy plasma-enhanced chemical vapour deposition (LEPECVD), in collaboration with LNESS group, to maintain high quality and low hydrogen content within the material. This step was preluded by an HF dip to ensure the removal of the native SiO_2 within the seed area, with the parallel formation of Si-H bonds which prevent surface oxidation in the time between the HF dip and the SiGe deposition. Wafers with a SiGe film covering the whole area of the substrate were then ready for planarization. To improve the performance of the CMP, the film was patterned with UV contact lithography and dry etched with an inductively coupled plasma (ICP) tool to remove the unwanted SiGe around the trenches. The level of the SiGe material was planarized to the level of the insulating layer by Chemical Mechanical Polishing (CMP) with dilute 1:1 W2000 slurry. As mentioned in Chapter 4, the fabricated design also contained dummy squares filled with SiGe, which are helpful to sustain pattern uniformity during the planarization process. The size of the dummy squares was 1x1 µm (for the trench etch layer) so that they were comparable to the size of the device trenches. The CMP processes was followed by PECVD of a 1 µm thick SiO_2 insulating cap. This material was deposited on top of the wafer to encapsulate the structures before the rapid thermal annealing (RTA) process. Afterwards, RTA was performed to finalize the creation of the RMG structures on the SOI platform. The temperature of the RTA was firstly stabilised at approximately 500°C before ramping up to the desired peak temperature in the range between the Si and Ge melting points (chosen to be 950 °C according to the thermocouple attached to the back of the wafer) at a rate of approximately 100°C/s. The time at the peak temperature was 1 s, before letting the wafer cool naturally (by switching off the RTA lamps). The resulting structures were characterised with Raman spectroscopy to confirm the composition across the structures. After Raman spectroscopy measurements, the top insulating layer was removed using a combination of dry etching (ICP) and 20:1 HF wet etching in order to facilitate the material characterization with scanning electron microscope (SEM).

5.5.2 Wires with graded composition on SOI

Conventional RMG is performed on simple straight strips emanating from a Si seed. Results for a variety of 3 µm wide strips with 10 µm overlap to the seed area (Sc) are shown in Figure 70.

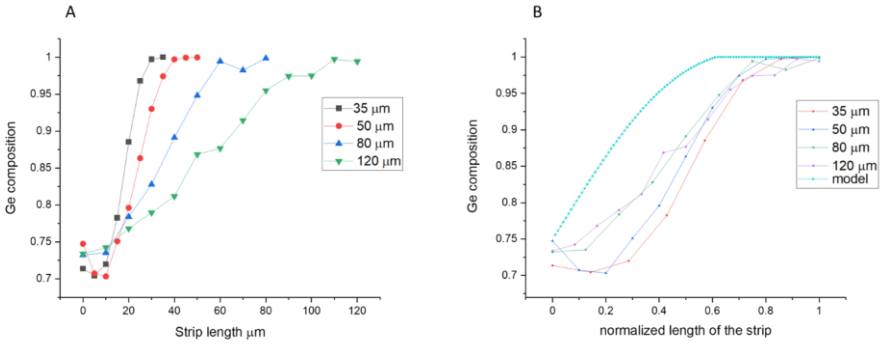

Figure 70 The Ge composition for strips embedded in the SOI platform, (A) a graph for 3 µm wide strips for a variety of lengths, (B) comparison of Ge composition for these strips with normalized length values next to the complete mixing model (referred as a model).

The anneal temperature within the structure (due to inaccurate measurement of thermocouple) might be determined locally based on the phase diagram for SiGe alloys and finding the temperature for the highest Si content in the structure (seed area). The 30 % Si content is related to around 1030 °C based on the phase diagram presented in Chapter 2.

As can be seen in Figure 70, the composition of RMG straight strips is graded along their length. This is a result of the separation between the solidus and liquidus on the SiGe phase diagram (details presented in Chapter 2) resulting in preferential Si rich solid formation. This situation occurs especially when cooling of structures is not immediate. The data from Figure 70A can be normalised against the strip length, as seen in Figure 70B. The graded composition of the SiGe stripes was also described by the complete mixing model [11], which is implemented into Figure 70B. This model assumes a relatively slow regrowth front propagation speed (slow in the sense that the regrowth front propagation speed is slower than the diffusion constant of Ge in SiGe/Si) enabling the Ge rich liquid at the regrowth front to fully diffuse into the melt [12]. The diagram of the complete mixing model is shown in Figure 71 to illustrate the principle of the mechanism.

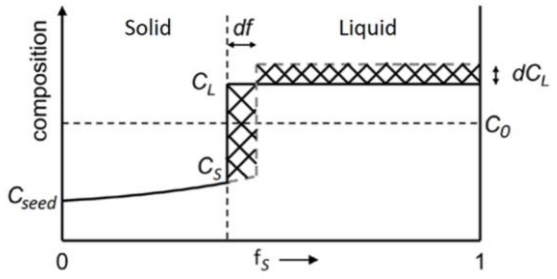

Figure 71 Complete mixing model adapted from [12].

The composition is changeable and according to the complete mixing model it should be dependent on the solidified fraction of the normalized length of the strip. Based on the difference of the area under the peak for raw data and Lorentzian fit, the errors for the composition were found to be within 2-4% of the data, which means the data on the graph is in a good agreement within this range.

The data from Figure 70B corresponds to a maximum of only 2% difference between each strip length after reaching 70% of the total length. This data can be compared with the research for strips on the Si platform in the literature [12] . Even if the trend is similar, the high composition (above 95% of Ge) is reached much earlier for the Si platform (around 0.5 of normalized length) than for the SOI platform presented in Figure 70 (around 0.7 normalized length). The anneal temperature presented here for the SOI platform was higher than the literature value for the Si substrate (1030 °C compared with 1008°C, when the anneal temperature is calculated in the same way for both substrates) and the amount of Si diffused further into the strip is higher due to the higher initial Si content. This finding shows that the trend for RMG strips embedded into the SOI platform is analogous as for the strips on the top of the Si substrate.

5.5.3 Branch parameters for RMG structures embedded into SOI

As mentioned in Chapter 4, the cooling branches of the RMG structures embedded into the SOI were expected to support faster cooling along the main strip, in turn leading to a faster regrowth front propagation speed, according to the steady-state solidification model [12]. The simulation done based on this model is shown in Figure 72 for varied regrowth front propagation speed.

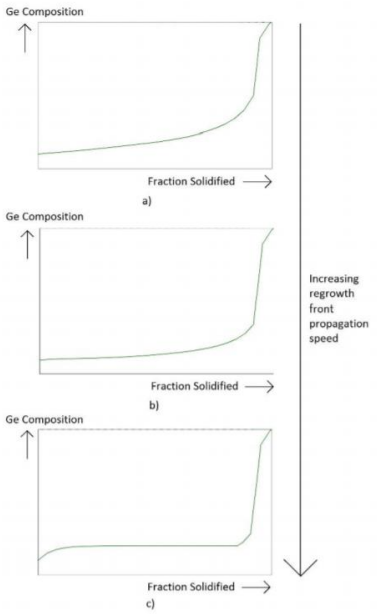

Figure 72 Simulations of SiGe growth using steady-state solidification model for the fast regrowth front propagation, adapted from [12]. Situations from a) to c) correspond to the increasing regrowth front propagation speed.

This model assumes that the regrowth front propagation speed is faster than the Ge diffusion into the Ge/SiGe melt, meaning that the Ge rich region at the regrowth front is not able diffuse into the melt. The faster propagation speed, the flatten the composition profile of the structures.

Within this project, the additional area of the added cooling branches was used for faster heat dissipation, subsequently leading to constant composition in the main strip of branches as shown in Figure 73. To confirm this hypothesis, parameters such as the branch length/ area, branch separation (BS) and the distance from the seed (D) were investigated when gathering results. Additionally, the potential applications for building active devices like Franz-Keldysh modulators were also considered to ensure appropriate structure geometry with a constant SiGe composition profile along a 50 µm long strip with a width greater than 1 µm. All the presented results were gathered from samples with deposited $Si_{0.015}Ge_{0.0985}$.

The correlation between the uniformity of the composition profile and the branch length was confirmed for both types of RMG structures presented in Chapter 4 (see Figure 69 for a clarification

of the two RMG types). Matching trends for both types of structures are highly important for further waveguide integration, where RMG2 type structures are preferable for easier integration of waveguides and active devices. This is related to the elimination of the seed from the area designated for device fabrication.

Based on the methodology described in Chapter 3, Raman spectroscopy was used to measure the spectra along the structures and subsequently to analyse it and to calculate the SiGe composition.

Results obtained from the RMG structures show the relationship between the branch length and the uniformity of the composition profile, as shown in Figure 73 and Figure 74.

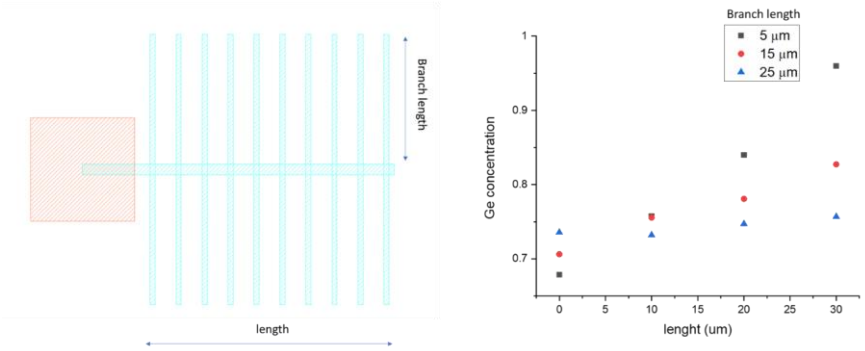

Figure 73 Dependence of the SiGe composition profile on the branch length for RMG1 type structures for 30 um long strips with a branch length of 5, 15 and 25 µm for structures A, B, C as shown in graph. The position of the measured strip is highlighted on each image.

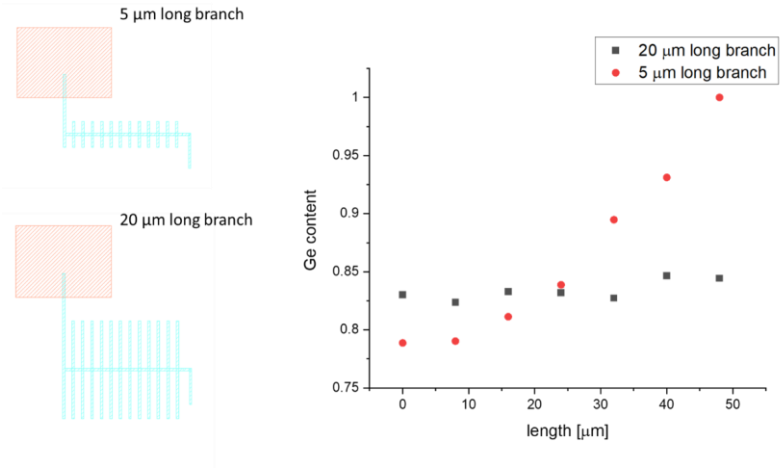

Figure 74 Dependence of the SiGe composition for single tree like structure (type RMG2) for different length of the cooling branches.

The length of the branches is confirmed to be crucial for the gradient of the composition profile, with a length of between 20 and 25 µm proving sufficient to achieve a uniform SiGe composition, which is shown in Figure 73 and Figure 74 for RMG1 and RMG2 respectively. The width of all branches (1µm) was the same for fair comparison of the composition profile. The width of the strip with constant composition was 2 µm for structures presented in Figure 73 and 1 µm for structures presented in Figure 74. All parameters can be found in Figure 75 for the sake of clarity.

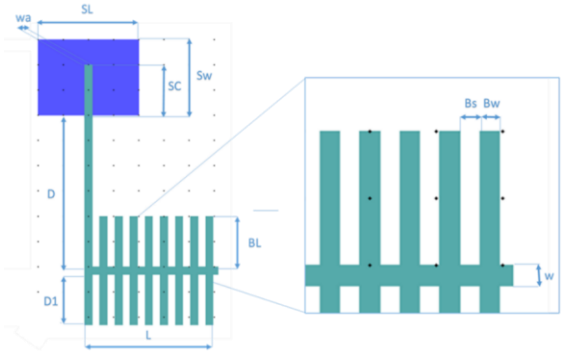

Figure 75 Parameters of the RMG2 type structure, where: Bs - Branch Separation, w - width of the strip with constant composition, Bw - Branch width, D - distance from seed to the start of the strip with constant composition, D1 - distance from the start of the strip with constant composition to the end of the main strip, SL - seed length, Sw – seed width, Sc- seed connection, L- length of the strip with constant composition.

A significant difference can be observed for a branch length in range 5-25 µm. The ratio of cooling branch area to the main strip area was found to be crucial for the composition profile. Structures RMG1 shown in Figure 74 had ratios as follows: 1.66 for 5µm long branches, 5 for 15 µm long branches and 8.33 for 25 µm long branches. For RMG2 structures, as presented in Figure 74, the ratio of cooling surface to the main strip were 2.4 for 5x1 µm cooling branches and 9.6 for 20x1 µm cooling branches. This implies that a ratio > 8 must be used in order to achieve a uniform composition in the main strip, which is of high importance for the heat dissipation from the main strip and in turn the cooling rate of the system. The area of cooling branches is of high importance for the heat dissipation because it leads to faster cooling by contact with the cooler surroundings. This is linked to a faster regrowth front propagation speed and a more uniform composition profile along the main strip. Minimising the length of the branches whilst achieving a constant composition profile is important to limit the footprint of the structure to enable densely packed devices and therefore a reduction in the cost per device.

Besides the length of the branches (BL), the separation between the branches (Bs) was also considered as a factor for the design of the tailored structures. For the sake of clarity, the parameters mentioned here are shown previously in Figure 75.

The results of varying the branch separation are shown in Figure 75. As above, structures had the branch length varied between 5 and 25 µm. The separation (Bs) was either 3 or 6 µm, for branches with the same width (Bw) and the same width of the main strip (w).

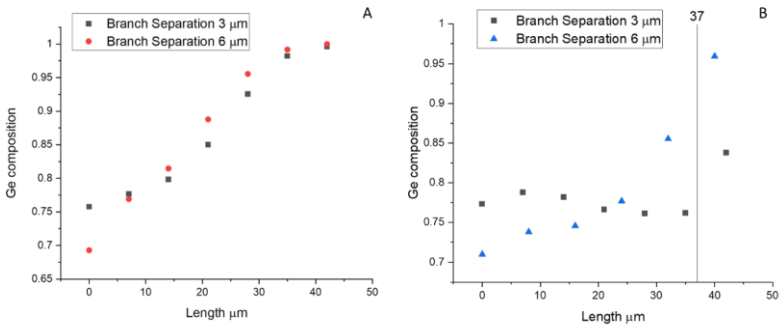

Figure 76 Composition profile for 2 different Branch Separations (Bs), other parameters are as follows: w= 2µm, Bw= 1 µm, BL= 5 µm for diagram A and BL=25 µm for diagram B.

These results are showing the dependence between the SiGe composition uniformity and the geometrical parameters of the tailored structures with a focus on the branch area and main strip ratio. To obtain enough cooling and subsequently constant SiGe composition along the main strip,

a greater surface area of cooling features is needed to maintain fast heat dissipation. In Figure 76, two separations were compared for two lengths of branches. The change in the composition profile was negligible for the shortest branches of 5 µm because the impact of this length of branch is insufficient to achieve fast cooling. On the contrary, the composition profile of the main strip with 25 µm long branches was much more affected by the change in separation. A changeable separation of the cooling branches corresponds to a change in ratio between the cooling branch area and the main strip. The calculated ratios are as follows: 0.75 and 1.25 for 5 µm long branches and 3.75 and 6.25 for 25 µm long branches, when the branch separation was 6 µm and 3 µm respectively. A uniform composition was achieved only for the ratio 6.25 for 25 µm long branches and 3 µm separation. Additionally, for the narrow branch separation, the minimum Ge content is higher than for a wider separation due to a bigger total area/ volume and limited diffusion from the Si seed. However, the composition profile is flatter for smaller branch separation, there is a limit (value to be confirmed) when the branches would stop help with heat dissipation and a whole structure would behave as a strip with graded composition. The length of the main strip with branches added was limited to 37 µm (after this length no branches were added) which explains the changeable composition after this length for the results shown in Figure 76b.

5.5.4 Seed connection for RMG structures embedded into SOI

The overlap between the SiGe strip and the seed (seed connection) was also tested as a parameter relevant for the tailored structures. The range of the contact length was varied when other parameters stayed constant. Results for the RMG2 structure with a uniform Ge composition profile are shown in Figure 77.

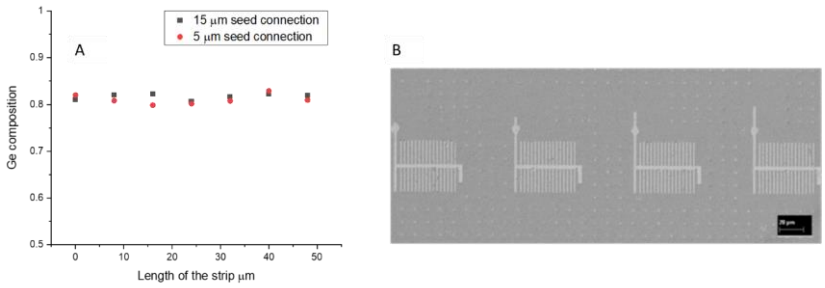

Figure 77 The seed connection (Sc) test, (A), test for RMG2 structures with parameters as following: BL=20µm, w=3µm, Bs=4µm, Bw=1µm, D=25µm, (B) SEM image showing an example test structure set with a variance of the seed connection.

Based on the seed connection test for SOI samples, there was no significant difference (above 2%) between the composition of the strip with constant Ge composition. This implies that Si diffusion from the seed is not limited by the overlap between the seed and the SiGe strip, which is expected due to the high diffusion coefficient of Si in liquid Ge [13]. Nevertheless, this test was conducted only for one anneal temperature and more research is required for a variety of anneal temperatures e.g. higher temperatures to obtain higher Si content within the strip.

5.5.5 Composition tuning for wavelength division multiplexing (WDM) on SOI platform

The RMG process on SOI can be utilised for a plethora of active devices e.g. modulators operating at a wide range of wavelengths aimed at exploiting wavelength division multiplexing (WDM) to dramatically increase the bandwidth of an optical link. To fabricate electro-absorption modulators suitable for exploiting WDM, the SiGe composition of each device should be tuned in a predictable manner, preferably as a function of the distance from the seed. In this way, the SiGe composition of each modulator can be tuned so that the operating wavelength of each modulator is matched to the wavelength of each channel in the WDM device. The experimental design to test this tuneability was based on single tailored structures (RMG2 type) with varied distance D of the "tree-like" structures from the seed, whilst maintaining consistent branch dimension parameters (set to be BL=20 μm long branches, Bw=1 μm, Bs=2 μm , w= 3 μm , and L=50 μm for the main strip to achieve constant SiGe composition). An example of the fabricated structures is shown in Figure 78 with all the parameters mentioned.

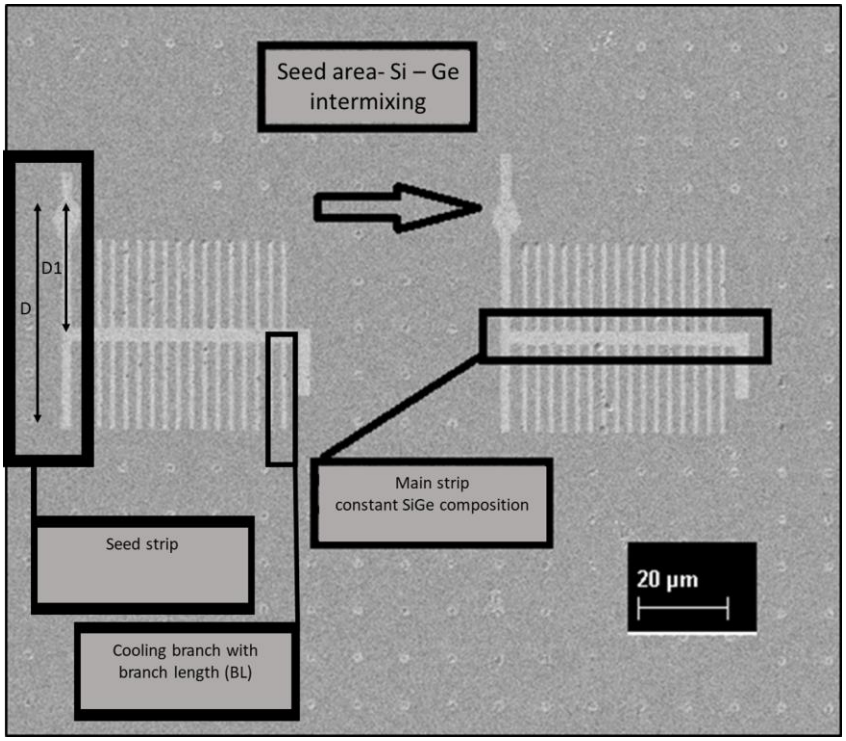

Figure 78 SEM image of structure used for obtaining tuned constant SiGe composition along the main strip. The varied parameter is distance, D1, from the seed to the strip with constant SiGe composition, distance, D, from the seed to the end of structure and Branch length (BL). Intermixing region between Si and Ge in the seed area is pointed on the image.

The structures shown in Figure 78 were used to research the relationship between the SiGe composition and the distance from the seed area. The results obtained for this experiment are presented in Figure 79.

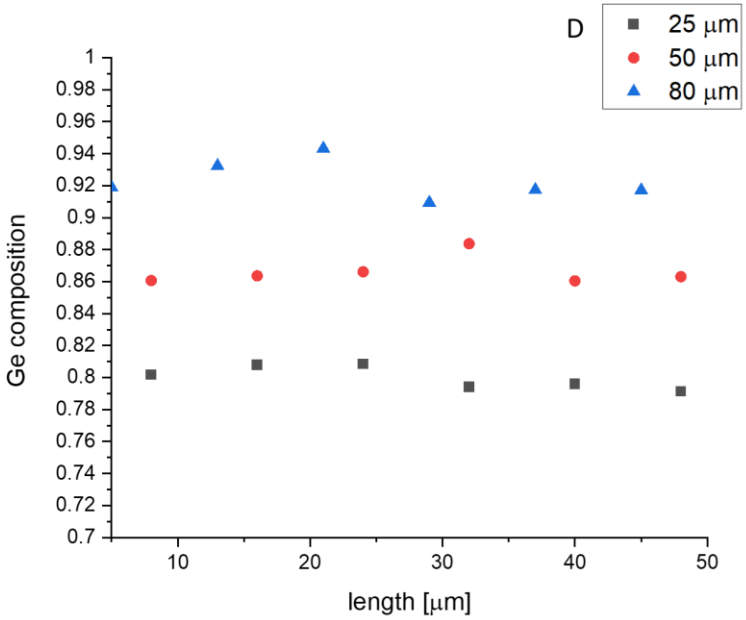

Figure 79 SiGe composition controlled by the distance, D, between the seed and the main strip with attached branches.

From Figure 79, the uniform profiles for various SiGe compositions can be seen. The Ge content increased with distance from the Si seed as expected, based also on results presented in Figure 71 for strips embedded into SOI platform. All added structures had the same dimensions to obtain the same ratio between the area of the cooling branches and the area of the main strip. The tuneability was based on a change of the ratio between distance D (distance between the seed and the main strip designed as a base for subsequent active device fabrication) and distance D1 (the remaining length of the strip emanating from the seed). Based on this, the ratio of D and D1 was found and described as proportional and it is shown in Figure 80. The length of the main strip, L, (50 μm) was designed as a suitable length for analogical active device fabrication as mentioned in Chapter 4.3.

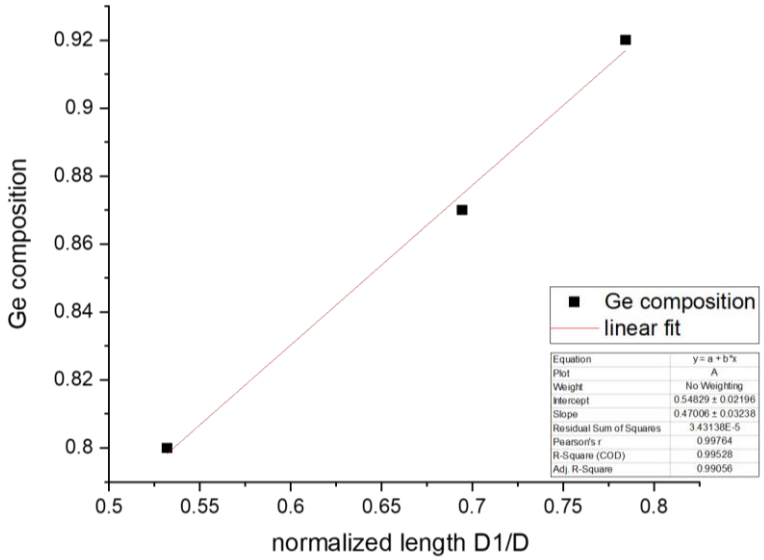

Figure 80 A diagram of the ratio of normalized length D1/D against Ge composition. The standard deviation for each set of measurements for each normalised length was respectively: 0.007, 0.008 and 0.01.

The first attempt to utilise the SOI platform for WDM applications is shown in Figure 81 for a tailored structure with 4 “tree-like” structures (Figure 81a).

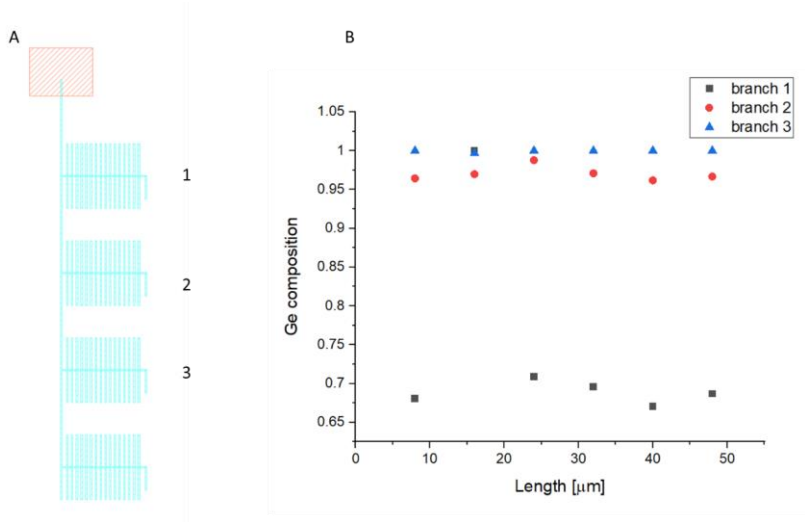

Figure 81 The tailored structure with 4 added "tree-like" structures as shown in (A) with the composition profile for branch 1, branch 2 and branch 3 as shown in (B). The distance, D, between seed and the first structure is 60 µm, distances between branches 1-2 and branches 2-3 are also set to 60 µm, Bs=2 µm, Bw=1 µm, w=1 µm. The total length of the strip of the structure is 264 µm.

Branches 2 and 3 are characterised with constant, high Ge content, which is promising for further development of this technique on the SOI platform for WDM applications in the C-band (where compositions in the range 98-100% are required) with devices of minimized area [14]. The fourth "tree-like" structure was not characterised due to a disconnection in the seed strip leading to incomplete RMG. Consequently, more process development on structures with multiple "tree-like" structures is required to obtain a uniform profile across all the structures.

In order to compare the effect of geometry on RMG structures embedded in Si, with those embedded in SOI, results from a Si test wafer are also presented in Figure 82. The Si substrate was processed in the same way as the SOI, with the "tree-like" structures embedded into the substrate. The structures had the same parameters for distances, D (25 and 80 µm) and D1 (20 µm), as structures from Figure 79 for the SOI platform.

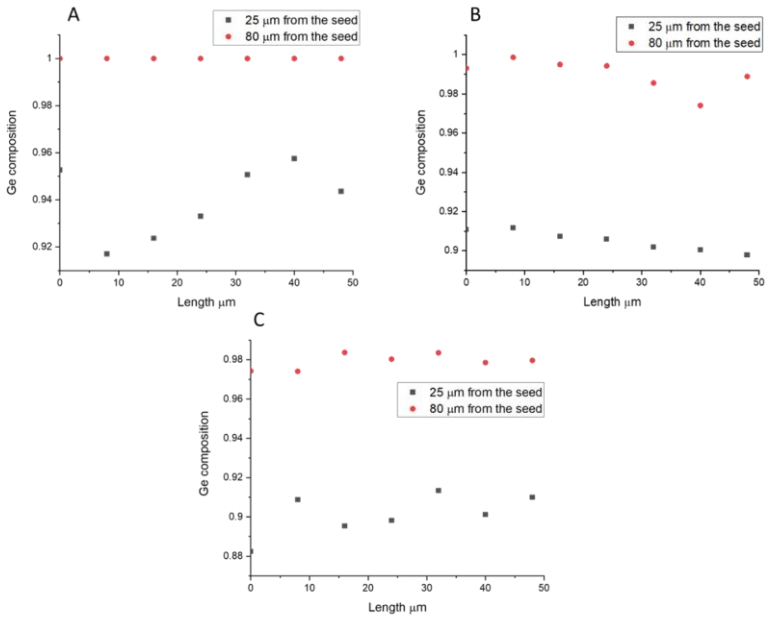

Figure 82 Results for a RMG2 type structures embedded onto the Si platform, Branch Separation, BS, was kept constant as 3 µm, other parameters are as follows: (A) Bw=1 µm, w=1 µm, (B) Bw=2 µm, w=2 µm, (C) Bw=3 µm, w=3 µm.

The ratio between the cooling branch area and the main strip area was as follows: 6.4, 8 and 9.6. for A, B and C respectively. Also, in this case a ratio of 8 is sufficient to result in uniform composition. Overall, the lowest deviation was shown for the set B with parameters: Bw=2 µm, w=2 µm.

A high Ge content is desirable for EAMs operating in the C-band and this data proves that it is possible to tune the Ge content within the desired range (98-100%), at least on the silicon platform. However, since the silicon based devices were processed in the same way as the SOI based devices, and all other trends have been comparable between Si and SOI, it points to the fact that it will be possible to achieve the same control on the SOI platform with further process optimisation and a lower annealing temperature.

5.6 Summary

The results presented in Figure 79 demonstrates the proof of principle for tuneability of RMG structures on the SOI platform. This result is crucial for the compatibility of the process developed in this thesis for the integration of active RMG devices with waveguides on the SOI platform, paving the way for a new era of low-cost devices like photodetectors or Franz-Keldysh modulators operating at a range of wavelengths, exploiting the significant benefits of WDM.

Within this work, the ability to not only achieve a uniform SiGe composition on the SOI platform using a RMG technique has been proven, but crucially the ability to tune the uniform composition across the wafer without modifying the processing steps has also been demonstrated. This proves the ability to tune the composition of the SiGe structures on the SOI platform using only a single deposition and single anneal step, a result that has never been reported for the SOI platform. Research on the effect of cooling branches has only been demonstrated previously for the Si platform [13][15]. This first demonstration on the SOI platform promises to allow the development of new devices with high performance and low cost. An example application can be EA modulators operating between 1500 nm and 1600 nm, which demand a Si content between 2% and 0.5%, respectively. Another potential application of the described RMG methodology is the growth of thin defect-free SiGe layers for applications like quantum wells for modulators or transistors at 1310 nm.

Chapter 6 Conclusions and Future Work

6.1 Conclusions

Both SiGe and Ge are highly important elements of photonics circuits, operating in a wide range of near-infrared and mid-infrared wavelengths. A variety of Ge and SiGe applications require systems with multiple Ge and SiGe based devices to be built across one chip; reported examples of high-speed active devices such as high-speed photodetectors, electro-absorption modulators or infrared waveguides are suitable for Ge-based design. The plethora of epitaxial growth methods for Ge and SiGe on Si are discussed in the literature review. However, there are a number of areas leaving room for improvement in the SiGe/Ge growth process including the fact that the presence of a lattice mismatch between Ge and Si results in high dislocation densities in the SiGe/Ge layer, and the ability to grow only a single composition on each wafer. Applications requiring multiple compositions of SiGe or pure Ge like wavelength division multiplexing (WDM) are not achievable with the commonly used growth methods. A single growth step allowing multiple compositions across a single wafer is a desirable solution for a high number of applications. This project is oriented with a special focus on finding opportunities for fabrication of devices operating within the C-band wavelength window (1530-1565 nm), and especially 1550 nm. This wavelength is suitable for active devices like Franz-Keldysh electro-absorption modulator (EAM). The composition of the structures to meet this aim is found to be around 98.5-99.5% along with a device length of approximately 50 μm.

This project focused on the development of SiGe and Ge structures obtained from the rapid melt growth (RMG) technique on the SOI platform, which is required for active device integration with waveguides. The RMG technique uses similar principles on SOI and Si platform. RMG allows the overgrowth of SiGe or Ge on an insulator layer from a Si seed. For the SOI platform, the formation of structures/ trenches is patterned into the Si overlayer, and then filled with Ge or SiGe, which is a critical step for the success of the subsequent processing. The trenches embedded into the Si and subsequently covered with an insulating layer should enable the Ge to fill the trench without voids and with connection to the Si only in the designated seed area. The design within the SOI platform demands that the surface is planarized with Chemical Mechanical Polishing/ Planarization (CMP). The substrate planarized to the level of the trenches filled with Ge is covered with additional insulating layer before Rapid Thermal Anneal (RTA) when the Ge will be melted. During the melt Si diffuses from the area into the Ge or SiGe structure, creating SiGe melt. The difference between melting temperatures for Ge and Si allows Si to stay in the solid state and to be used as a crystalline template for the epitaxial regrowth of SiGe.

The integration of the RMG structures into the SOI platform has required extensive process development work across many of the fabrication steps including trench etching, Ge or SiGe deposition and CMP.

RMG enables defect-free structures which is not achievable by any other technique of epitaxial growth. Defects associated to the lattice mismatch are trapped within the Si and Ge/ SiGe interface due to the epitaxial necking mechanism. This part of the structure is designed to not be used during waveguide integration or fabrication of active devices. The initial Ge/SiGe deposition is unselective with multiple available options e.g. PECVD or LEPECVD, however, the hydrogen content within the layer and other impurities play a role as a factor for further processing. The number of defects obtained from this initial growth step do not influence the final quality of the structure due to the Ge melt step at high temperature (above Ge melting point, 938 °C). The characterisation of the RMG structures is based on the Raman spectroscopy technique, which compares the intensity ratio of the Ge-Ge and Si-Ge peaks obtained from each measurement.

Tailored structures with varying area of cooling branches and varied distance from the seed were researched on the SOI platform to compare the composition across analogical structures on the Si platform. The impact of increasing the area of the cooling branches was confirmed for the SOI platform in fairy similar way as for the research on Si [1], with the most effective cooling, and therefore uniform composition profile, for 25 µm long branches. Also, the constant composition structures (in range 80-100% Ge) were presented on SOI platform. The controllability of the composition of the compound by design was demonstrated and further work on refining the process and structures would potentially demonstrate the suitability for EAM's for WDM applications.

RMG on SOI allows fabrication of multiple compositions of SiGe across the wafer after only a single deposition and a single anneal step, which is unique across all epitaxial growth methods. Moreover, the tuneability achieved by RMG can be controlled by the design of the structures and also uses standard, commonly accessible fabrication steps. This method creates a low-cost and accessible solution, removing the limitations of only being able to achieve one SiGe composition across the wafer, and the high SiGe/Ge layer defect densities resulting from the Si and Ge lattice mismatch.

6.2 Future work

The work on RMG growth of SiGe and Ge structures within the SOI platform delivers multiple area of interest for further research. Possible applications of an SGOI platform are listed below:

- Optimisation of RMG structures within the SOI layer for further miniaturisation of devices

- Expansion of the composition towards lower content of Ge (region below 85%): The properties of SiGe alloys depend on the composition. The SiGe alloys from Si-like composition region, under 85%, can be successfully applied as a component of modulators e.g. as a strain layer [2][3]. The Ge content as low as the range 15-40% could therefore be researched for photonics applications.
- Waveguide integrated structures on SOI platform: Waveguide integration within the SOI platform is required for tests of the optical properties of the material e.g. optical losses, band gap. This step is leading the way to a plethora of active devices like detectors or modulators placed within waveguides.
- SiGe devices like electro-absorption modulator (EAM) based on Franz-Keldysh effect: These are ideal devices in the age of increased demand for high-performance devices, where low power consumption and high speed are crucial. The high quality of the RMG material is a chance to improve speed or footprint of modulators [4] if built using the demonstrated RMG method with the added benefit to decrease the number of fabrication steps and cost.
- Fabricate a wavelength division multiplexed (WDM) optical link: The multi composition SiGe regions across one structure allows fabrication of an array of modulators working at slightly different wavelengths to be realised. Moreover, the high-quality pure Ge strips can also be realised as a material for photodetectors, allowing realisation of a full WDM optical link.
- Multilayer devices using Si seed: The ability to create RMG structures from Si seeds is a chance to fabricate multilayer devices using either Ge or SiGe. The ability to create photonics or electronics devices across multiple layers is a chance to maximize the number of devices per area of the chip.
- Improvement of Ge photodetectors on Si and SOI platform: Low cost photodetectors are important for silicon photonics. The material quality was proven to be highly important for the performance of the resulting device [5]. Further work on Ge photodetectors fabricated by RMG process is a chance to optimize the performance of devices.

Appendix A [Full process flow]

Step No.	Process Name	Process Description
1	SiO_2 Deposition #1	PECVD 50 nm / Standard Recipe
2	E-Beam Lithography #1	Trees trenches lithography
4	SiO_2 Etch #1	ICP etch 50 nm
5	Si Etch #1	ICP etch 100 nm
6	Plasma Clean #1	O_2 Plasma Standard Clean
7	Photolithography #1	Dummy squares/ S1813
8	SiO_2 Etch #2	ICP etch 50 nm
9	Si Etch #2	ICP etch 100 nm
10	Plasma Clean #2	O2 Plasma Standard Clean
11	HF Dip #1	HF Dip 5 seconds 20:1
12	Si Etch #3	TMAH Angled Si Etch 200 nm
13	HF etch	SiO_2 etch all layer
14	SiO_2 Deposition #2	PECVD 60 nm / Standard Recipe
15	Photolithography #2	Seed Windows / S1813
16	SiO_2 Etch #3	HF Etch 60 nm 20:1 (oxide removed only in the trench)
17	Plasma Clean #3	O_2 Plasma Standard Clean
18	HF Dip #2	HF Dip 5 seconds 20:1
19	SiGe Deposition #1	LEPECVD 300-400 nm SiGe/ it might be replaced by Ge LEPECVD
20	Photolithography #3	Ge etch / S1813
21	Ge Etch #1	ICP etch for Ge around structures
22	Plasma Clean #4	O_2 Plasma Standard Clean
23	CMP #1	CMP / Ge above the trench removal
24	Wafer Clean #1	
25	SiO_2 Deposition #3	PECVD / protective cap 1000 nm
26	Anneal #1	RTA / chip scale
27	SiO_2 Etch #4	ICP SiO_2 down to 70 nm of SiO_2
28	SiO_2 Etch #5	HF Etch All 20:1 SiO_2 left-- each sample separately
29	Characterisation #1	Raman / Optical Measurements

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Chapter 1 Introduction

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Chapter 6 Conclusions and Future Work

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