Designs of silicon nitride slot waveguide modulators with electro-optic polymer and the effect of induced charges in Si-substrate on their performance

Teerapat Rutirawut[1], Wanvisa Talataisong[1,2], Frederic Y. Gardes[1]

[1]Optoelectronics Research Centre, University of Southampton, Southampton, SO17 1BJ, UK
[2]School of Physics, Suranaree University of Technology, Nakhon Ratchasima, Thailand 30000

Abstract: Dimensional parameters are optimized comparing stoichiometric and Si-rich silicon nitride-based push-pull modulators using a slot waveguide structure, electro-optic polymer cladding, and in-plane ground-signal-ground electrode. An optical power confinement in slot spacing is examined for choosing the optimal device parameters for wavelength of 1550nm. The electrical simulations are set to calculate an asymmetric spatial distribution of poling efficiency and modulating refractive index change in polymer. The influence of carrier charge in Si-substrate is also considered. The voltage-length products as well as the poling efficiency of Si-rich SiN are calculated as 1.47 V·cm and 0.74 respectively for a polymer with a $\gamma_{33,bulk}$ of 100 pm·V^{-1}. For the selected polymer the calculated efficiency compares to standard silicon based plasma dispersion depletion modulators. The efficiency can be increased more than two times for demonstrated polymers with a $\gamma_{33,bulk}$ of ~230. Low metal absorption loss of ~ 1dB/cm can be achieved from the optimal designed device. Comparing to the conventional simulation method without Si-substrate effect, a more accurate simulation method is also presented in this work.

Index Terms: Electro-optical devices, SiN waveguide, EO-polymer modulator, Slot waveguide modulator, Si-substrate.

1. Introduction

There is a growing demand for low cost devices targeted at enabling high speed data traffic of optical interconnects. A high speed, compact, optical modulator based on a low-cost photonic platform is essential to support this increasing demand. Most optical modulators based on CMOS technology are commonly fabricated using silicon (Si) based photonic circuits due to the native modulation mechanisms available to silicon.

State-of-the-art Si based modulators are mostly depended on the concepts of carrier charge diffusion in Si such as pn-junction[1-4] and pin-junction[5]. Electric field modulators based on the Franz–Keldysh effect [4-6] have also been demonstrated in Germanium and rely on a pin junction. Apart from efficiency and fast speed, these modulators suffer from increase insertion losses due to carriers or bandgap absorption and require a complex fabrication process involving high temperature required for doping activation or germanium epitaxy. Alternative concepts of optical modulator which are simpler in terms of fabrication and are compatible with back end of the line (BEOL) multi-layer processing are based on the integrations or bonding of other non CMOS active material such as, lithium niobite ($LiNbO_3$)[6, 7], barium titanate (BTO)[8, 9], electro-optic PZT[10]. One of the simplest method in terms of fabrication to achieve modulation by coating optical waveguiding components is to use electro-optic polymers (EO-polymer)[11, 12].

A modulator based on the SiN platform feasibly provides several advantages beyond that on Si platform such as lower propagation loss[13, 14], fabrication flexibility[15-17], selectable refractive index[18], broader transparency range[19-21], tunable operating wavelength[22], and a high tolerance to temperature variation[23, 24]. Enabling a widening of the field of applications. However, SiN has a centrosymmetric behavior which does not allow intrinsic electrooptic properties and therefore it is not generally possible to obtain optical modulation through an electric field[25]. Moreover, optical modulation using charge diffusion cannot be applied to SiN due to its dielectric property. The integration of $LiNbO_3$ or BTO with SiN is a potential route but does require complex fabrication schemes such as planarization and bonding resulting in potential yield issues. Another route is the integration of EO-polymers with SiN waveguides to form optical modulators, this solution provides flexibility and simplicity for BEOL fabrication methods [14, 18]. Using EO-polymer, several modulators have achieved high-speed, energy-efficient modulation, whilst using few fabrication steps. The EO-polymer based modulators have been demonstrated at a very low voltage-length product of 0.345 V·mm [12] with a modulation frequency beyond 100 GHz[11].

Nevertheless, very few EO-polymer modulator based on SiN [26, 27] have been demonstrated. Owing to its lower index contrast compared to Silicon, the challenge on the SiN platform is to obtain the best modulation efficiency whilst retaining a low absorption loss. Few waveguide structures have been introduced to demonstrate modulation capabilities, however, their efficiency is still far from the Si modulator with efficiency such as 900 V·cm using a SiN ridge design[26], or 17.6 V·cm in a thin SiN waveguide design[27]. Slot waveguides coupled to a pn-junction have been adopted in high confinement materials

[28-31] such as Si to enable a high overlap between the optical mode, the E-field and the EO material, nevertheless this method does not provide any gain in terms of fabrication complexity or BEOL due to the necessity of forming doped areas within the silicon waveguide. Such method has not been demonstrated in SiN due to the insulator nature of the material.

Due to the random alignment of chromophores in the initial state of EO-polymers, its Pockels coefficient is zero as deposited and requires an activation process described as polling. The polling of EO-polymer is taking the form of a strong electric field applied through the polymer in the region surrounding the modulating waveguide whilst the temperature of the polymer is raised close to the glass transition temperature. To simplify the process, the poling is typically performed by using the device modulation electrodes[32, 33]. An in-plane electrode where the electrodes are located on the waveguide plane is an alternative structure to reduce the complexity of fabrication as it requires only one process step for metal lift-off[34]. The modulation performance of the modulator is proposed by only calculating an overlap integral factor of the optical power in the polymer or overlapping factor of the optical field and modulation electric fields within the polymer[35-37].

In this paper, a practical design of a slot waveguide modulator with an active EO-polymer cladding is proposed to provide waveguide based efficient modulation capabilities to a BEOL SiN photonic platform. The slot structure is optimized for the optimum overlapping of the optical field and the EO-polymer, whilst the in-plane GSG electrodes is utilized to offer an in-device poling ability. The performance of this modulator is estimated by using an improved in-device poling and AC-modulation simulations. A comparison of two different guiding materials based on [13, 38] (stoichiometric and Si-rich SiN) is also presented to compare performances.

2. Device Design

The main advantage of slot waveguides compared to strip waveguides is the guiding mechanism where the guided mode in the slot waveguide is partially confined in between two SiN ridges. Consequently, the guided mode will have a maximum interaction with the cladding material which in this case is an EO-polymer. Base on the virtue of the optical confinement behavior of the slot waveguide, the strength of the confinement is also implicitly influenced and see a reduction of the mode field distribution around the waveguide structure.

For the design of phase modulator based SiN slot waveguide, a stoichiometric SiN (n=2.0) [18] and Si-rich SiN (n=2.5) [39] have been defined as a waveguide material. The higher refractive index of Si-rich SiN aims to increase the index contrast and thereby improve the power confinement in the slot region while the lower index contrast in the stoichiometric SiN platform provides a higher tolerance for fluctuations from fabrication process and surface roughness. Thicknesses of SiN ridge in the slot waveguide have been optimized to prevent a proximity of effective indices between TE_0 and TM_0 mode, and to reduce a fabrication difficulty from high aspect ratio of waveguides. Thus, the thickness of 600nm and 550nm were achieved from the optimization for the stoichiometric SiN and Si-rich SiN, respectively. The cross-section designed device in this work is depicted in Fig. 1 where a stack of material layers (bottom-to-top) are included a silicon substrate, 3µm-thick buried oxide (BOX) and 2µm-thick EO-polymer. As presented in the schematic of the device cross-section, the SiN slot waveguide is placed on the top of BOX layer which is surrounded by EO-polymer.

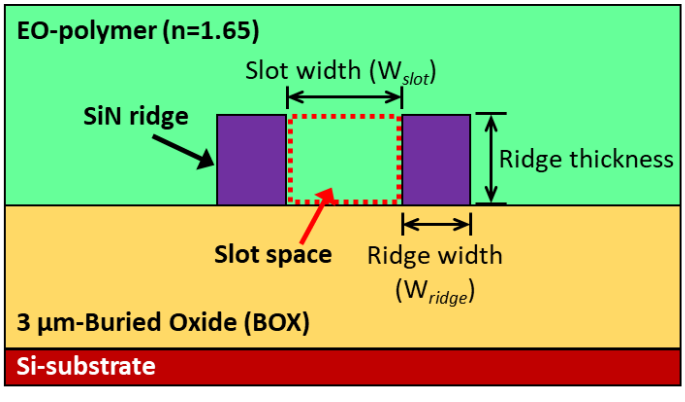

Fig. 1. Schematic cross section of SiN slot waveguide showing two SiN ridges with slot spacing in between them which are cladded by EO-polymer.

To ensure the maximum optical power confined in the slot of the slot waveguide, the waveguide design is accomplished by optimizing two important parameters of slot waveguide including slot width (W_{slot}) and SiN ridge width (W_{ridge}). The commercial software MODE Solutions (Lumerical) is employed to simulate the waveguide 2D-eigenmode and calculate the optical power in slot (P_{slot}). The refractive index of EO-polymer of 1.65 has been chosen for the simulation as it is the average index of most EO-polymers in other reports (1.6-1.7)[35]. The simulation is focused only on the optical wavelength of 1550nm (C-band in NIR) and the SiN and EO-polymer are assumed to have no material optical loss at this wavelength. To find the optimal dimension of the SiN, W_{slot} and W_{ridge} are swept in the ranges of 200-1200 nm and 200-600 nm for stoichiometric SiN and in the range of 100-500 nm and 150-400 nm for Si-rich SiN.

The contour plot in Fig. 2(a) reveals the percentage of optical power confined in slot space (P_{slot}) as a function of slot width (W_{slot}) and SiN ridge width (W_{ridge}) for the stoichiometric SiN. The maximum value of P_{slot} obtained from the graph is ~19% at W_{slot} = 750 nm and W_{ridge} = 360 nm. By considering the island-like shape of the power distribution in the contour plot, a wider uniformity region of high power confinement along the x-axis (W_{slot}) implies that the slot waveguide can have higher dimension variation for the W_{slot} rather than the W_{ridge}. The simulated optical field profiles of TE_0 mode in the slot waveguide with optimal dimensions is presented in Fig. 2(c). For Si-rich SiN waveguide, the contour plot of P_{slot} is depicted in Fig. 2(b), and the obtained maximum value of P_{slot} is ~29% when W_{slot}= 380 nm and W_{ridge} = 230 nm. Due to the higher refractive index in Si-rich SiN, the P_{slot} is ~10% higher than that of stoichiometric SiN waveguide. Therefore, the optical mode confined in the Si-rich SiN slot reveals a smaller radiation area as shown in Fig. 2(d). Fig. 2 (c-d) showing that the optical mode is not fully confined in the slot space as there is a distribution of modal concentrated around the waveguide structure which can be induced the higher loss if the waveguide is close to the electrode. Thus, the increase in confinement of the optical field in the slot space could develop the possibility to reduce electrode spacing compared to a simple strip waveguide.

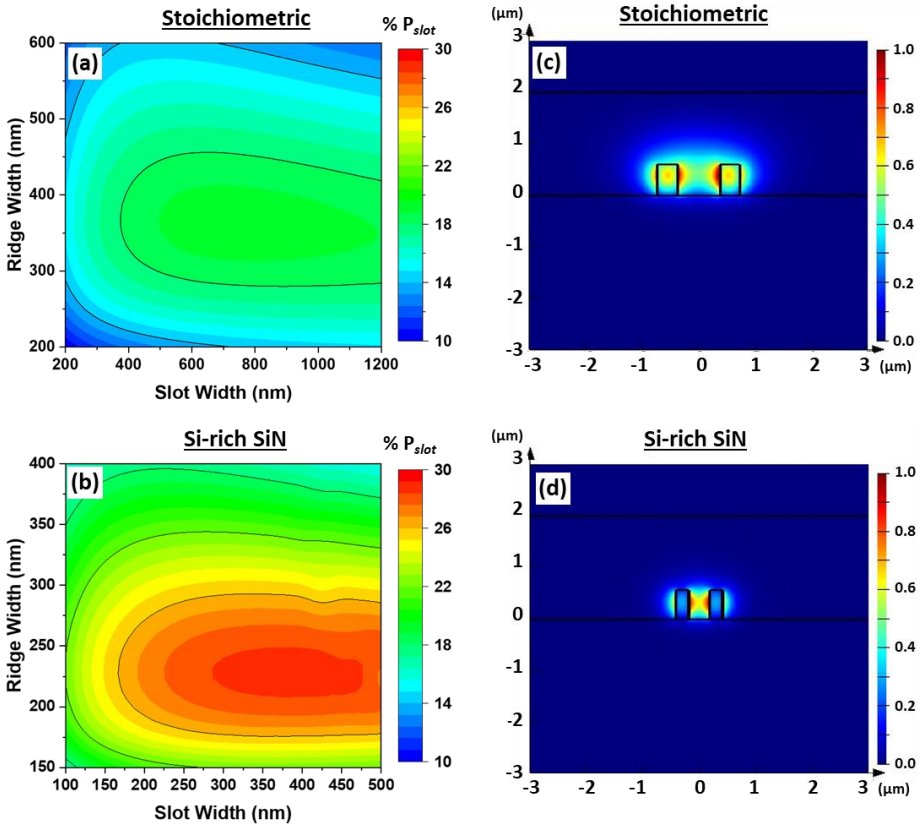

Fig. 2. (a)-(b) 2D-plot Percentage of optical power confinement (PC) within a slot space versus slot width and ridge width for the 600nm-thick stoichiometric and 550nm-thick Si-rich SiN slot waveguides, respectively. (c)-(d) Their electric intensity of TE_0 mode profile with the optimal waveguide dimensions.

Another key parameter in the design of optical phase modulator based on SiN slot waveguide is the electrode spacing (*d*) which is the distance between two metal electrodes. As the strength of electric field is inversely proportional with the electrode spacing, the closer of two electrodes leading to the higher and more uniform electric field. Therefore, the optimization of electrode spacing in the design is to position the metal electrodes as close as possible to the waveguide while keeping the absorption loss at acceptable levels (< 1dB/cm). Based on a cross-section of Mach-Zehnder modulator, the coplanar ground-signal-ground (GSG) transmission line is configured as a push-pull electrode. The GSG electrode structure is formed with a 300 nm-thick aluminium layer deposited on the BOX layer as shown in Fig. 3(a). This 300nm-thick layer of metal is chosen in order to ease a limitation of a lift-off process for electrode fabrication.

Propagation losses in the waveguide due to metal electrodes and power overlap of guided optical mode with the polymer will be examined to determine the dimension of electrode gap in the design. In the simulations, the electrode spacing (*d*) is swept while the propagation loss and optical power overlap in the active polymer for each electrode spacing were then calculated. The plotted between propagation loss and optical power overlap with different electrode spacing are presented in Fig. 3(b) for stoichiometric SiN and Fig. 3(c) for Si-rich SiN waveguides.

To define the optimal dimension of electrode gap in the design, propagation losses due to metal electrodes is limited to less than 1 dB/cm. Therefore, the optimal electrode spacing of stoichiometric SiN and Si-rich SiN waveguides are 8.6 µm and 4.0 µm (Fig. 3(b-c)) which is related to the percentages of integral optical powers overlapping in polymer of ~71% and ~68%

respectively.

In the modulator design, the width of central electrode was also optimized to minimize the reflection of the electrical signal at the end of the transmission line (GSG electrode). The optimal width of central electrode of stoichiometric SiN and Si-rich SiN waveguides are 30.53 µm and 18.73 µm were chosen to meet a CPW line impedance (Z_0) of 50 Ω. To be in line with a standard multilayer SOI based PIC fabrication process, the SiN waveguide deposited on a silicon-on-insulator wafer. The Si on insulator and SiN layers are shown (Fig. 3(a)) where the silicon has been etched under the SiN waveguiding areas leaving a width of 1 µm on each side of the simulation area. The silicon thickness is 300 nm and is positioned 2 µm above the Si-substrate.

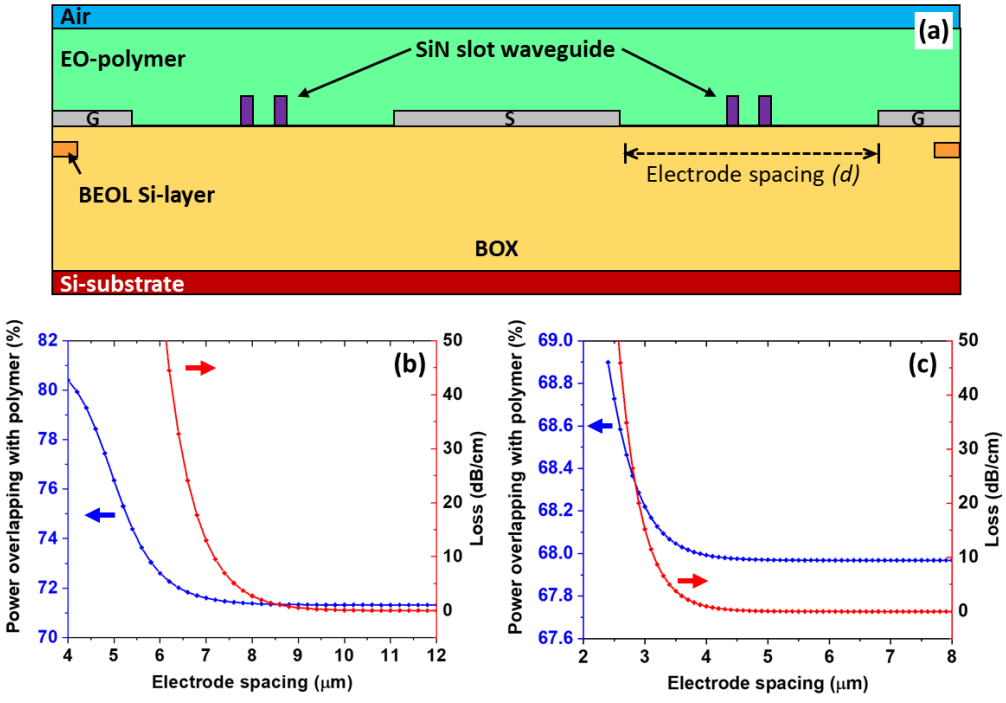

Fig. 3 (a) Cross-sectional view of Mach-Zehnder modulator with two identical slot waveguides and GSG electrodes. (b)-(c) Simulated optical power overlapping with polymer and propagation loss versus electrode spacing of phase-shifters with a stoichiometric and Si-rich SiN slot waveguide, respectively.

3. In-plane poling and modulating field

To monitor the performance of a Mach-Zehnder modulator (MZM) with two identical phase-shifters, the voltage-length product ($V_\pi L$) will be considered where a low $V_\pi L$ represents higher efficiency. The $V_\pi L$ of this type of modulator can be defined as the voltage (V_π) required to achieve a phase different of π between two arms of MZM for the length L [40-42]. Therefore, the $V_\pi L$ relationship of the proposed EO-polymer device can be expressed in Eq. (1) [43].

$$V_\pi L = \frac{\lambda \cdot d}{2 \cdot n_{EO}^3 \cdot \gamma_{33,in} \cdot (\Gamma_{EO})} \quad (1)$$

where λ is the optical wavelength in vacuum, d is the electrode spacing, n_{EO} is the refractive index of the EO-polymer, $\gamma_{33,in}$ is an in-device Pockels coefficient, and (Γ_{EO}) is an electrical-optical overlap integral factor in the EO-polymer region. By considering Eq. (1), it can be noticed that two parameters related to the design of the modulator structure are d and Γ_{EO}.

In term of a waveguide modulator with EO-polymer presenting in core or cladding region, the optical guiding mode is partially overlap to the polymer region. Thus, the effective index change of optical mode (Δn_{eff}) will be related to the EO-polymer index change; however, they are not directly changed with the same magnitude. The effective index change is associated to an overlap factor between the optical intensity ($\frac{c\varepsilon_0 n}{2}\left|\vec{E}_{opt}(x,y)\right|^2$) and the modulating electric field ($\vec{E}_{mod}(x,y)$) in the active polymer area. Note that only the TE component of E_{mod} in the EO-polymer will have an effect in modulation of the TE optical mode. So, the overlap of optical mode and the local chromophore orientation will be defined as the overlapping integral factor (Γ_{EO}) as expressed in Eq. (2).

$$\Gamma_{EO} = \frac{d}{V}\frac{\iint_{EO} E_{mod}(x,y)\cdot\left|E_{opt}(x,y)\right|^2 dxdy}{\iint_{-\infty}^{\infty}\left|E_{opt}(x,y)\right|^2 dxdy} \quad (2)$$

From Eq. (1) the voltage-length product ($V_\pi L$) can be decreased when an optimized waveguide leading to optimum electrode spacing has been designed to have the largest Γ_{EO} and smallest d whilst optical absorption losses due to the metal electrodes remains negligible.

A schematic of electrical poling connection which are used in this modulator simulations is demonstrated in Fig. 4. The GSG electrodes are designed for dually used for both in-plane poling and modulation purposes. For the modulation, a modulating signal is connected to the signal electrode (S) while the two sides electrodes (G) are grounded. For the EO-polymer poling, an applied poling voltage (V_{poling}) is applied only between two ground electrodes (right-to-left on Fig. 4), whilst the signal electrode (center on Fig. 4) is left as a floating contact. This poling connection works by the principle of method of image in the electrostatic theory [44]. Once the poling voltage is applied between the two ground electrodes, the E-field induces a movement of charges in the floating electrode following the field direction. Additional fields caused by the induced charges cancels all applied field inside the floating electrode, resulting in a net-zero field with a constant electrical potential. By ignoring all the perturbation from surrounding materials, a uniform gradient of potential as shown in Fig. 4(a) will be achieved while half of the applied voltage is automatically dropped across each electrical spacing. This uniform gradient implies a good uniformity of the generated electric field ($E = V_{poling}/2d$) leading to a high uniformity poling profile in the EO-polymer.

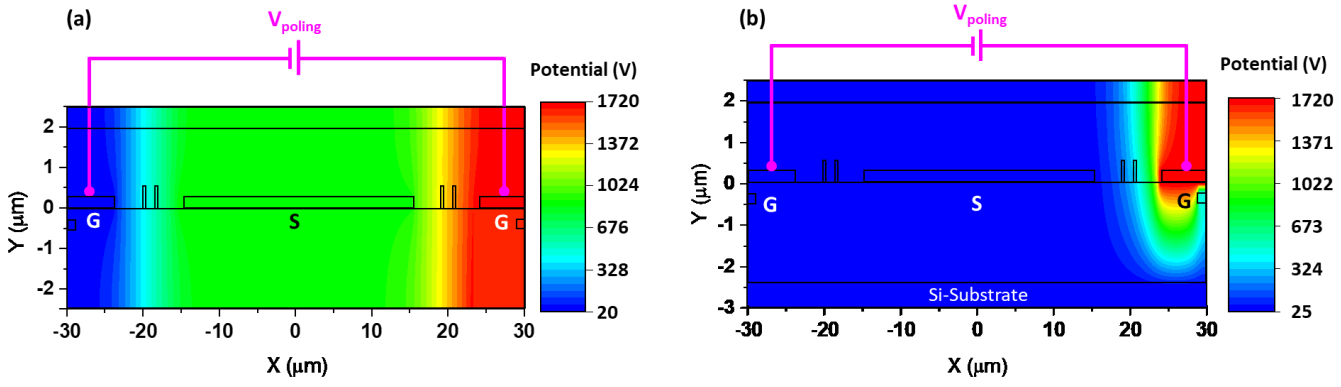

Fig. 4 Simulated electrical potential distribution of in-plane poling process with ground-signal-ground (GSG) electrodes (a) excluding an effect of a Si-substrate (b) including an effect of Si-substrate.

During the “in-device” poling process, the poling field can however be distorted by a difference in electrical properties of surrounding materials. The first disturbance considered is a contrast of dielectric constant between the EO-polymer, waveguide material and buried oxide. Particularly, within the slot waveguide structure, a moderate part of the optical mode power is confined in the slot, where the higher dielectric constant of the SiN ridges can distort the applied field during the poling process or during modulation. Another major distortion is due to an induced charge effect generated in the Si-substrate, as well as high substrate temperature which is necessary to the poling process will increase charge effect due to the excess of free carriers. Induced charge effect in Si-substrate resulting in the higher electron concentration on the right because the applied poling voltage (V_{poling}) is applied between the positive electrodes (right) and ground electrode (left). The peak of concentration is dependent on the strength of applied voltage. Therefore, nonuniformity of potential distributions during the poling is occurred when considering the induced charge effect in Si-substrate (Fig. 4(b)).

In order to accurately simulate the distribution of electric field, our simulation setup accounts for dielectric constants of all involving materials. The dielectric constants of SiN, EO-polymer and buried oxide are defined as 7.5, 3.0 and 3.9, respectively. The carrier charge distribution in the Si-substrate is also considered to include the effect of induced charges. The Si-substrate is specified as a p-doped (Boron, $1x10^{15}$ cm^{-3}) silicon wafer. The 2D distributions of electric field and charges are simulated by using the Atlas module in Silvaco™ TCAD software. For the poling configuration, the excess temperature induces an increase of the carrier concentration in the Si-substrate. Therefore, the expected poling temperature of 180°C at a Si-substrate boundary is set at by adding a thermal contact in the simulation. The applied poling voltage is designated by referring to the average electric field (100V/µm) required for poling EO-polymer as reported in several publications[35, 45, 46]. By assuming that the applied voltage is equal across two identical electrode spacings as formerly explained, the applied voltage can be calculated by taking the required electric field and the optimal electrode distance. Thus, the applied poling voltages will be designated as 1,720V for the case of the stoichiometric SiN waveguide and 800V for the case of the Si-rich SiN waveguide. For the simulation of optical

Following the description and definitions of the device parameters, the electrical simulation results of stoichiometric SiN and Si-rich SiN devices are presented in Fig. 5 and Fig. 6, respectively. The distributions of electron concentration reveal an influence of the applied voltage to the accumulation of carrier charges in the underlying Si-substrate when poling (Fig. 5(a)). These electrons are attracted and build up a layer as near as possible to the positive potential source at the BOX/Si interface.

As demonstrated in Fig. 5(a), electron concentration is higher on the right because the applied poling voltage (V_{poling}) is applied between the positive electrodes (right) and ground electrode (left). For the poling configuration, the potential distribution can be perturbated by the built-up charges and will be mostly confined to the positive electrode. As presented in Fig. 4(b), the voltage dropped across the central floating electrode and ground electrode on the left is less than one-sixth of the total applied voltage while most of the applied voltage is dropped across the space between the central floating electrode and positive electrode. For the simulated electric field during poling, an asymmetric poling field in Fig. 5(b) can be clearly observed. On the weaker field side(left), the strength of poling field inside a slot space is about 1.4 V/μm which is two order of magnitude lower than the expected average field. However, the field on the other side is elevated to ~134 V/μm which is more than 100 times stronger and ~30% higher than the expected field.

As the modulation efficiencies of EO-polymer based optical modulators can be significantly affected by the distribution of poling field. In order to enhance the field distribution, the application of an additional bias voltage onto the Si-substrate or the central electrode of the coplanar microwave electrode can play a role in improving the poling process. In this work, the voltage applied on the middle electrode for additional bias are 860V for stoichiometric SiN and 440V for Si-rich SiN while the voltage applied to the substrate are 860V and 400V for stoichiometric SiN and Si-rich SiN waveguides, respectively. As presented in Fig. 5(c) when the bias voltage is applied at the central electrode, the gradient of electron concentration of the induced charge in the Si-substrate is changed. The electron concentration will not only concentrate on the right of substrate but distributed more to the central part. When considering the electric field during poling, the strength of poling field between central electrode and substrate is increased as demonstrated in Fig. 5(d) resulting in the higher strength of poling field inside a slot space on the left which is about 64.7 V/μm. Thus, the field on the right side is decreased to ~106 V/μm.

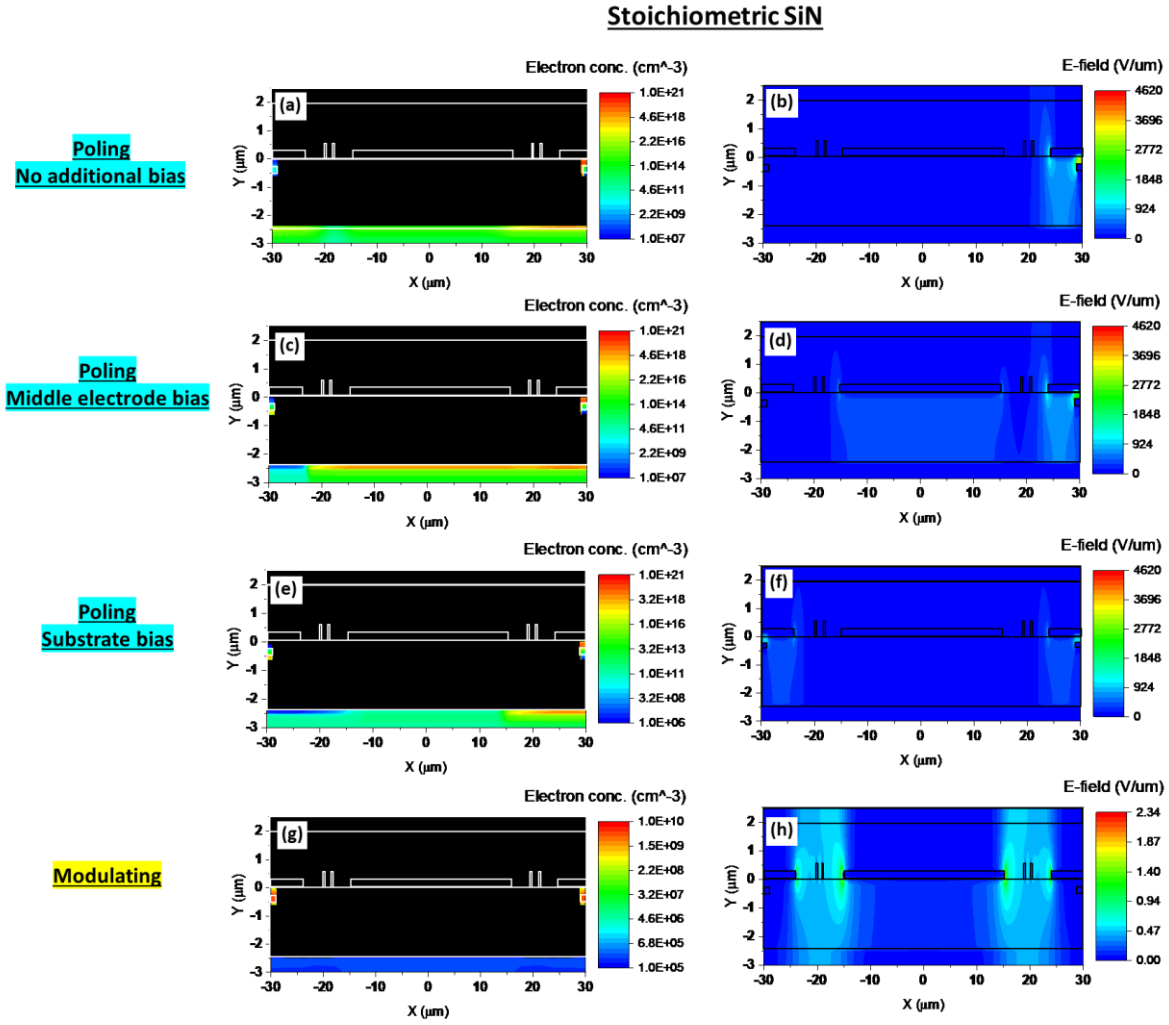

Fig. 5 Electrical simulation results of the poling process at 1720V and RF-modulation in the stoichiometric SiN design: the electron concentrations presented in Si-substrate (a) Poling with no additional bias, (c) Poling with middle electrode bias, (e) Poling with substrate bias, (g) RF-modulation. The electric field distributions when (b) Poling with no additional bias, (d) Poling with middle electrode bias, (f) Poling with substrate bias, (h) RF-modulation.

In case of an Si-substrate biasing, this will enable a reduction of the induced charge effect, where applying half of the poling voltage will enable the Ground-Ground poling E-field distribution to be equivalent to the ideal case in Fig. 4(a). The electron concentration in Fig. 5(e) showing a high concentration of charge in Si-substrate on both sides. This causes the more symmetry of the gradient of poling field inside the slot space as presented Fig. 5(f). The strength of E-field during poling when biasing the Si-substrate are ~66.4 and ~66 V/μm for the left and right slot space, respectively.

For the modulation process, the signal is connected to the central electrode which is signal electrode when the two sides electrodes are grounded. In the case of the DC-modulation, the built-up of carrier charges whilst operating the signal electrode

is mostly confine at the center. Thus, the modulating field will be more intense at the center (the signal electrode). However, at high frequency modulation (RF-modulation) without bias voltage, the carrier effect from substrate can be ignored due to the non-polarity of average E-field. Therefore, modulated E-field at the modulation frequency of 40 GHz will behave like the ideal case as presented in Fig. 5(g-h).

The effect of carrier charges in the underlying Si-substrate to the poling field for Si-rich SiN are also the same as stoichiometric SiN which is demonstrated in Fig. 6. The influence of the applied voltage to the distributions of electron concentration when poling with no additional bias, biasing middle electrode and biasing Si-substrate are presented in Fig. 6(a, c, e), respectively. These electrons are attracted and build up a layer as near as possible to the positive potential source at the BOX/Si interface resulting in the variation of poling electric field. The asymmetric poling field can be clearly observed in Fig. 6(b) for no additional bias, while more symmetric of poling field are revealed in Fig. 6(d) for biasing middle electrode, and Fig. 6(f) for biasing Si-substrate. The strength of poling field inside a slot space for no additional bias is about 7.2 V/μm when the field on the other side is elevated to ~160.3 V/μm. When considering the poling electric field when biasing middle electrode, the strength of poling field between central electrode and substrate is increased leading to the increasing of poling field inside a slot space on the left which is about 88.7 V/μm where the field on the right side is decreased to ~93.2 V/μm. For the poling field of Si-substrate biasing device, the strength of E-field is ~84.5 and ~85.5 V/μm for the left and right slot space, respectively. The modulating E-field in Si-rich SiN is also behaving like the ideal case when modulating with the high frequency of 40 GHz as presented in Fig. 6(g-h).

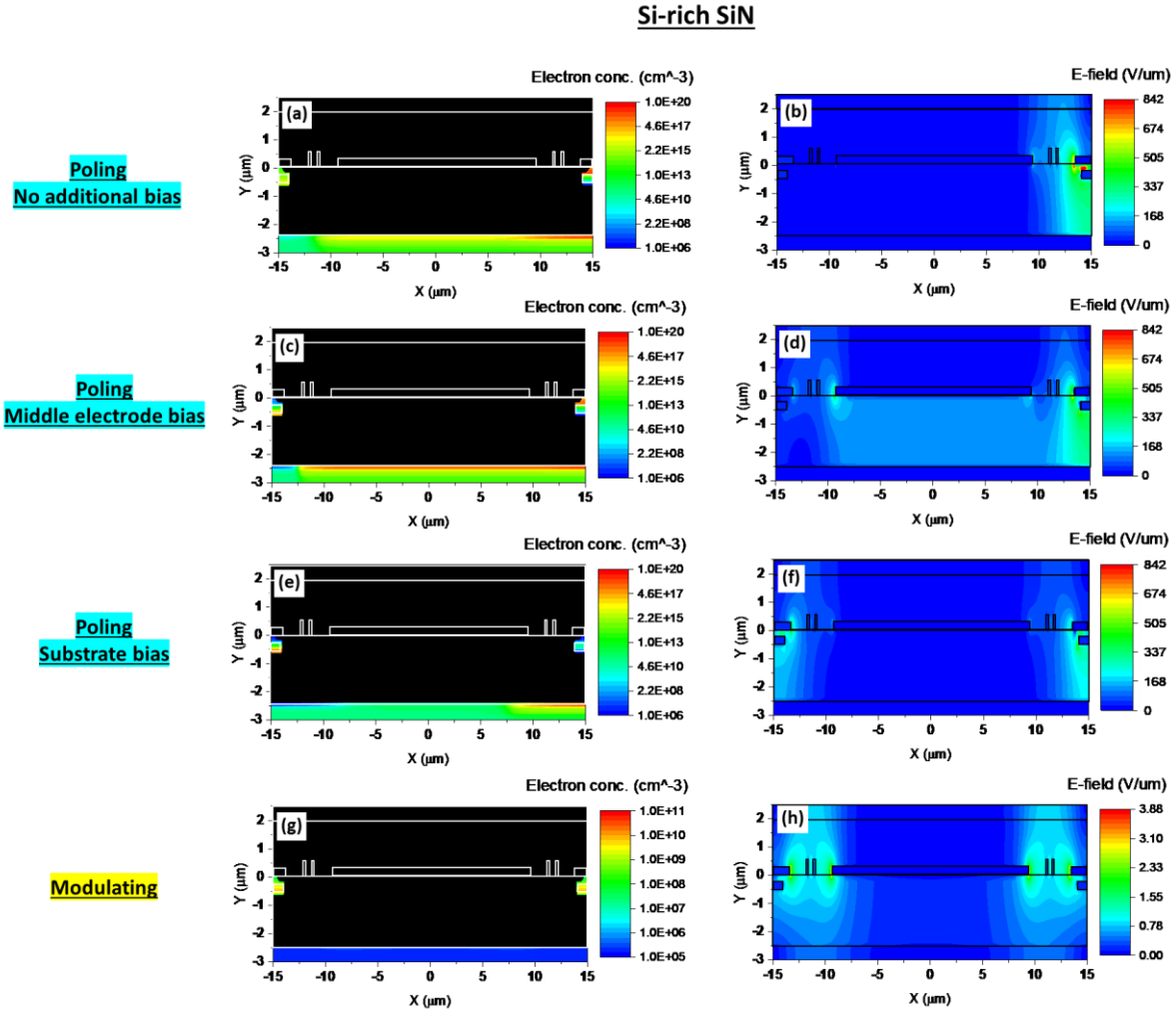

Fig. 6 Electrical simulation results of the poling process at 800V and RF-modulation in the Si-rich SiN design: the electron concentrations presented in Si-substrate (a) Poling with no additional bias, (c) Poling with middle electrode bias, (e) Poling with substrate bias, (g) RF-modulation. The electric field distributions when (b) Poling with no additional bias, (d) Poling with middle electrode bias, (f) Poling with substrate bias, (h) RF-modulation.

4. Reasonable simulation for predicting performance

In EO-polymers, chromophore molecules align preferentially to the applied electric field during the poling process. As shown in Fig. 5 and Fig. 6, the poling E-field is not entirely uniform across the electrode spacing, although a biasing has been applied to improve the distribution of poling electrical field. This nonuniformity leads to a difference of local poling efficiency in the EO-polymer. Therefore, to calculate the optical mode accurately, the value of poling field distribution must be transferred to a grid system in the optical simulation instead of assuming an ideally uniform poling profile across the EO-polymer.

As the poling efficiency is linearly related to the strength of poling field [35] and saturated at some certain level, the

calculation of Pockels coefficient (γ_{33}) is such that the spatial distribution of Pockels coefficients in poled EO-polymer can be defined by Eq. (3).

$$\gamma_{33}(x,y) = \begin{cases} \frac{\gamma_{33,bulk} \cdot E_{poling}(x,y)}{E_{sat}} & ; \left|E_{poling}\right| \le E_{sat} \\ \gamma_{33,bulk} & ; \left|E_{poling}\right| > E_{sat} \end{cases} \quad (3)$$

where $\gamma_{33}(x,y)$ is a local Pockels coefficient in each simulating grid after poling, $E_{poling}(x,y)$ is a local poling electric field and E_{sat} is a minimum electric field strength required for obtaining the saturated Pockels coefficient. In case of $\left|E_{poling}\right| > E_{sat}$, the term $E_{poling}(x,y)/E_{sat}$ is limited to be equal to 1.

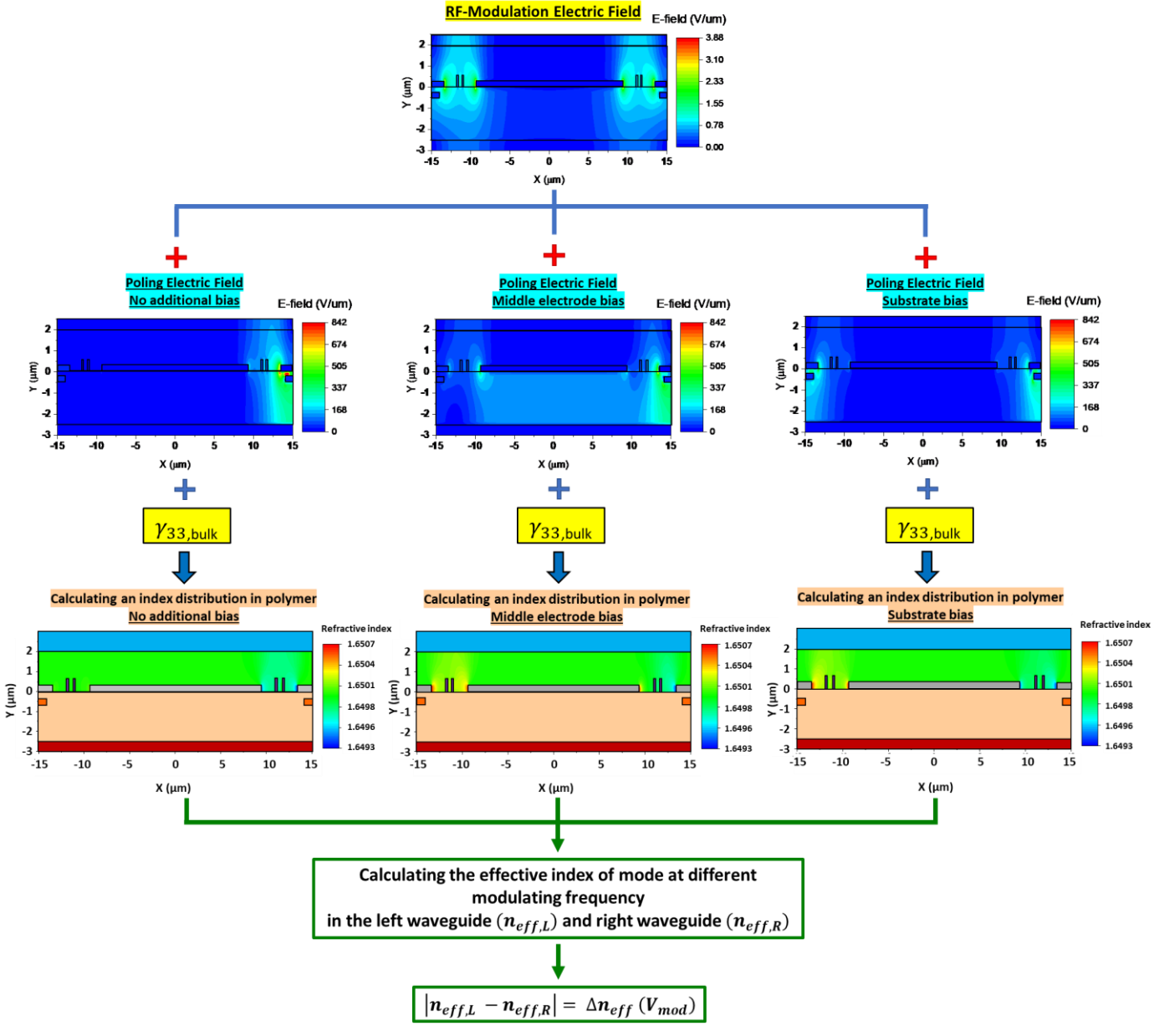

Fig. 7 Diagram of simulation process for accurately predicting the performance of the proposed SiN slot waveguide modulators.

To calculate the change of local refractive index in the EO-polymer when modulating, the result of simulated RF-modulation field is also required. The EO-polymer is considered as a diagonal anisotropic material, and the refractive index associated to a diagonal component in material permittivity is defined by n_i. The distribution of refractive index changes ($\Delta n_i(x,y)$) can be calculated by using the following Eq. (4).

$$\Delta n_i(x,y) = -\frac{1}{2}\, n^3 \gamma_{33}(x,y) \left[\hat{\imath} \cdot \frac{\vec{E}_{poling}(x,y)}{\left|\vec{E}_{poling}(x,y)\right|} \cdot \vec{E}_{mod,EO}\right] \quad (4)$$

where n is a refractive index of EO-polymer in the neutral state and $\vec{E}_{mod,EO}$ is a RF-modulating electric field while $\frac{\vec{E}_{poling}(x,y)}{|\vec{E}_{poling}(x,y)|}$ represents a unit vector pointing in the direction of the orientation of local chromophore which is defined by the direction of local poling electrical field. This equation is adopted from the general definition of refractive index change in Pockels effect $\left(\Delta n = -\frac{1}{2} n^3 \gamma_{33} E\right)$.

The performance of slot waveguide modulator ($V_\pi L$) in this work can be estimated by following the procedure presented in Fig. 7. Firstly, 2D distributions of applied electric field for the stoichiometric SiN and Si-rich SiN designs are simulated by assigning one setup for a poling configuration and another for RF-modulation as reported in Fig. 5 and Fig. 6. Then, the 2D distribution of poling electric field was combined with the Pockels coefficient of bulk polymer ($\gamma_{33,bulk}$) to find the local Pockels coefficient ($\gamma_{33}(x,y)$) at each mesh in EO-polymer region. After that, the simulated distributions of $\gamma_{33}(x,y)$ and RF-modulation electric field at each modulating voltage are used together to create a profile of refractive index change in EO-polymer region. Next, this profile will be imported to the optical simulator for calculating a modulated effective index of TE_0 mode between the waveguide on the left ($n_{eff,L}$) and on the right ($n_{eff,R}$) (phase-shifters) of modulator. In general, the length of a modulator is considerably longer than its cross-sectional dimensions, thus the electric field component along the length-side can be ignored. Then, the 2D-spatial refractive indices of modulated polymer are all calculated and transferred to the grid system of the optical simulation setup. Finally, the difference of effective index of TE_0 mode ($\Delta n_{eff}(v_{mod})$) between the phase-shifters is calculated as a function of the applied modulation voltages (V_{mod}). In this simulation, the Pockels coefficient of bulk polymer ($\gamma_{33,bulk}$) is ranged from 2 to 100 pm/V, and the saturated field (E_{sat}) is defined as 100V/μm which is averaged from a common poling field for determining an Pockels coefficient in polymer [32, 35, 36, 47]. Then, this are used to calculate a voltage-length product of this designed modulator by using the Eq. (5).

$$V_\pi L = \frac{\lambda}{2} \cdot \frac{V_{mod}}{\Delta n_{eff}(v_{mod})} \tag{5}$$

The inhomogeneity of the electric poling field that dictates the local orientation of the chromophore dipoles resulting in the non-uniformity of $\gamma_{33}(x,y)$. Due to this nonuniformity, we consider here the value of the Pockels coefficient in-device $\gamma_{33,in}$ which is depending on the poling coefficient (α) of this design device. A linear dependence of the Pockels coefficient of bulk polymer ($\gamma_{33,bulk}$) and Pockels coefficient in-device ($\gamma_{33,in}$) is furthermore assumed to be $\gamma_{33,in} = \alpha \cdot \gamma_{33,bulk}$. Therefore, the Eq. (1) can be rewritten as Eq. (6).

$$V_\pi L = \frac{\lambda \cdot d}{2 \cdot n_{EO}^3 \cdot \alpha \cdot \gamma_{33,bulk} \cdot (\Gamma_{EO})} \tag{6}$$

The plot between voltage-length products ($V_\pi L$) against different $\gamma_{33,bulk}$ for stoichiometric SiN and Si-rich SiN are presented in Fig. 8(a) and Fig. 8(b). The curve of plotted data is corresponded to the inverse relation of $V_\pi L \propto \frac{1}{\gamma_{33,bulk}}$ as shown in Eq. (6). The electrical-optical field interaction factor or overlap integral factor ($\Gamma_{EO,eff}$) of the designed device in this work can be calculated from the simulation. At this point, the poling coefficient (α) can be obtained by using a curve fitting technique, and this factor exhibits efficiency in poling of this design device.

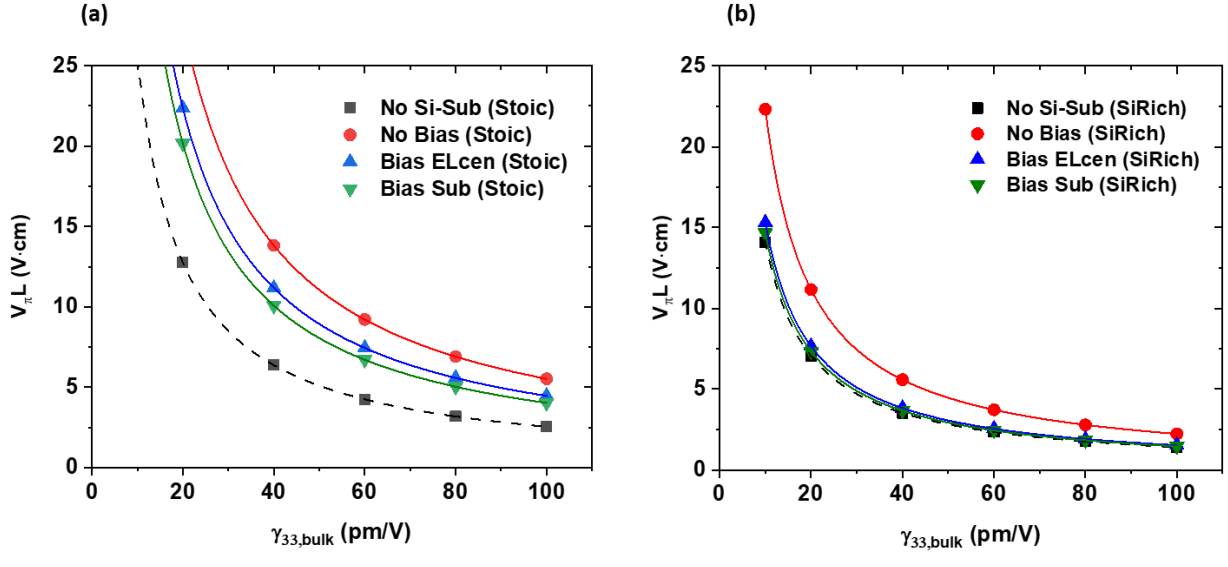

Fig. 8 The simulation results for calculating the Mach-Zehnder modulator performance. Voltage-length products ($V_\pi L$) versus Pockels coefficient of bulk polymer ($\gamma_{33,bulk}$) for (a) stoichiometric SiN and (b) Si-rich SiN design.

By implementing the method discussed above with designs based on slot waveguides modulator, the characteristic factors of the design device are obtained and presented in TABLE 1.

The results from the electro-optic simulations show that the poling efficiency (α) of slot waveguide modulators without the Si-substrate are highest for both stoichiometric SiN (α ~ 0.88) and Si-rich SiN (α ~ 0.75). For the slot waveguide modulators with Si-substrate, the insertion of carrier charge effect in Si-substrate significantly reduces the poling efficiency (α). The result of the device with Si-substrate with no applied bias voltage shows the lowest α of 0.43 and 0.49 for stoichiometric SiN and Si-rich SiN, respectively. This is a significant reduction due to induced carrier charges in the Si-substrate leading to nonuniformity of the poling electric field. These results are consistent with the electrical simulation results in Fig. 5 and Fig. 6(a-f). An introduction of bias voltage to the central electrode or the Si-substrate during the poling process dramatically increases the poling efficiency up to ~ 27% for stoichiometric SiN and ~ 34% for Si-rich SiN. The results also show that the poling efficiency for both devices is higher when biasing the Si-substrate rather than the central electrode. This is due to more uniformity of poling electric field when the bias voltage has been applied to the Si-substrate as revealed in Fig. 5(f) and Fig. 6(f). Finally, the poling efficiency of Si-rich SiN when biasing the central electrode and Si-substrate is the highest and the values are closer to the device without Si-substrate.

To exhibit the performance of the slot waveguide modulators, the voltage length product ($V_\pi L$) are presented in TABLE 1. The $V_\pi L$ of the stoichiometric SiN and Si-rich SiN show the lowest value with an efficiency of 2.55 V·cm and 1.41 V·cm, respectively, without Si-substrate. By including the effect of carrier charge in the Si-substrate, the $V_\pi L$ of the devices (with no additional biasing voltage) is increased for ~50%. A reduction of $V_\pi L$ can be observed when the biasing voltage has been applied to central electrode or Si-substrate. It is also shown that the $V_\pi L$ of slot waveguide modulator based on Si-rich SiN waveguide has the lowest $V_\pi L$ of ~ 1.47 V·cm which is only 4% higher than a device simulated without the Si-substrate.

It can be confirmed that carefully controlled biasing voltages applied to the device during the poling process can significantly improve the performance by almost 50%. However, through the study of devices proposed in this work, it is clear that more complex substrates such as single layer or multilayer SOI or with a high number of semiconductor or metallization levels could result in further distortion of the poling field distribution leading to a non negligeable impact on device efficiency. Finally, it should also be noted that the modulation efficiencies also strongly depends on the polymer and can be significantly improved by more than 2 times (compared to the efficiency reported in this work) if an EO-polymer with γ_{33} of 230 pm/V [48, 49] is applied to the modulators.

Although our simulation method which includes the Si-substrate without supplementary biasing process reveals the reduction in 50% performance compared to the device without Si-substrate, the modulator designs with Si-rich SiN can still show the voltage-length product in a comparable range (2.7 – 4.0V·cm for single phase-shifter) compared state-of-the-art silicon pn junction modulators [1, 50, 51].

TABLE 1
Parameters of Simulated SiN slot waveguide modulators in this work.

Parameters	**Stoichiometric SiN**				**Si-rich SiN**			
	Sim. w/o Si-substrate	Sim. w/ Si-substrate (No Bias)	Sim. w/ Si-substrate (Bias ELcen)	Sim. w/ Si-substrate (Bias Sub)	Sim. w/o Si-substrate	Sim. w/ Si-substrate (No Bias)	Sim. w/ Si-substrate (Bias ELcen)	Sim. w/ Si-substrate (Bias Sub)
Pockels coefficient bulk polymer, $\gamma_{33,bulk}$	100 pm·V^{-1}							
Optimal electrode spacing, *d* (µm)	8.6				4.0			
Overlap integral factor, Γ_{EO}	0.661	0.632	0.632	0.632	0.650	0.632	0.632	0.632
Poling coefficient (α)	0.880	0.425	0.525	0.582	0.754	0.489	0.713	0.744
Voltage-length product, $V_\pi L$ (V·cm)	2.55	5.55	4.49	4.05	1.41	2.24	1.54	1.47
Electrode absorption loss	< 1 dB/cm							

5. Conclusions

The proposed method for EO polymer simulation in this work demonstrates the large impact of electric field distortion by carrier charge in the Si-substrate. Without consideration of this effect, the calculation of modulator efficiency can be

overestimated by up to a factor of 2. For stoichiometric SiN slot waveguides, the optimal modulator presents a larger $V_\pi L$ of 5.55 V·cm but the performance can be improved to $V_\pi L$ ~ 4.05 V·cm when biasing the Si-substrate. Si-rich SiN waveguide modulator can lead to a practical $V_\pi L$ of 2.24 V·cm because of its higher mode confinement and smaller electrode spacing and the $V_\pi L$ can be further reduced to 1.47 V·cm when applying a bias voltage to the Si-substrate during poling process. While these efficiencies are calculated under the assumption of γ_{33} = 100 pm·V^{-1}, they can be improved further by using a higher Pockels coefficient polymer. Finally, both designs of modulators can be fabricated using only two lithography steps and a low-cost CMOS compatible BEOL process decreasing substantially fabrication time and design/test turnaround.

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