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A Low-Cost Laser Grooved Interdigitated Back Contact Solar Cell

by

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Thesis for the degree of Doctor of Philosophy

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Abstract

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES

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Work into the interdigitated back contact (IBC) cell to date has shown that the geometry can produce amongst the highest efficiency silicon solar cells. These current devices have yet to become the market leading technology due to the costly and tricky fabrication processes required to keep the doped regions of the p/n junction separate from each other whilst being on the same side of the wafer.

This project will demonstrate a novel approach using lasers to create deep surface grooves to allow localised doped regions on a single wafer surface. The purpose of this is to shorten the current path between the charge generation and charge collection regions, although potential benefits of this approach may be limited by increased recombination as a result of enlarging the metal-silicon contact area. Laser processing is however a very cheap and fast method that will allow a significant reduction in processing costs for IBC cells.

In this project, an initial crude proof of concept device with an efficiency approaching 1% was fabricated. This served to prove that the novel geometry proposed by this project could create a working device. Technology Computer Aided Design (TCAD) modelling was carried out, showing that with further processing steps and

optimisation of existing ones, devices with efficiencies exceeding 20.5% could potentially be created. Further experimental work was then performed to develop processes needed for the fabrication of the improved device design as modelled. In summary, the ability to utilise lower cost fabrication methods involving laser processing to produce highly efficient device geometries represents a promising approach to reducing the cost per watt of solar renewable energy.

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All data supporting this study are openly available from the University of Southampton repository at https://doi.org/10.5258/SOTON/D1361

Acronyms

AM	air mass
ARC	anti-reflective coating
aSI	amorphous silicon
BP	British Petroleum
BSE	backscattered electrons
BSF	back surface field
Btu	British thermal units
CAGR	compound annual growth rate
CdS	cadmium sulphide
CdTe	cadmium telluride
CIGS	copper indium gallium selenide
CNC	computer numerical control
CVD	chemical vapour deposition
CZ	Czochralski
DCS	dichlorosilane
DOE	design of experiments
DSSC	dye-sensitised solar cells
EDS/EDX	energy dispersive x-ray spectroscopy
EWT	emitter wrap through
FF	fill factor
FIB	focused ion beam
FIT	feed in tariff
FSF	front surface field
FZ	float zone
GDR	groove damage removal
GUI	graphical user interface
HWCVD	hot wire chemical vapour deposition
IBBC	interdigitated buried back contact
IBC	interdigitated back contact
IPA	Isopropyl alcohol
I_{sc}	Short circuit current
ITO	indium tin oxide
ITRPV	international technology roadmap for photovoltaics
J_{sc}	Short circuit current density
LGBC	laser grooved buried contact
LCOE	levelised cost of energy
LED	light emitting diode
LFC	laser fired contact
LPCVD	low pressure chemical vapour deposition
MPP	maximum power point
MWT	metal wrap through
Nd: YAG	neodymium-doped yttrium aluminium garnet
NREL	national renewable energy laboratory
OPV	organic photovoltaic
PCD	photoconductance decay
PECVD	plasma enhanced chemical vapour deposition
PERC	passivated emitter and rear cell
PERL	passivated emitter rear locally diffused
$POCl_3$	phosphoryl chloride
POLO	polycrystalline silicon on oxide
PV	photovoltaic
QD	quantum dot
QSSPC	quasi steady state photoconductance
R2R	roll to roll
RCA	Radio Corporation of America
RP	random pyramid
R_s	series resistance
R_{sh}	shunt resistance

SRH	Shockley-Reed-Hall
SCAPS	solar cell capacitance simulator
SCCM	standard cubic centimetres per minute
SDE	structural device editor
SDEVICE	Sentaurus device
SDR	saw damage removal
SE	secondary electrons
SEM	scanning electron microscope
SHJ	Silicon heterojunction
SLASH	structuring by laser ablation of silicon heterojunction
SRV	surface recombination velocity
STC	standard test conditions
SVISUAL	Sentaurus visual
TCAD	technology computer-aided design
TMM	transfer matrix method
UNSW	University of New South Wales
USD	United States dollar
V_{oc}	open circuit voltage
Wp	watt peak

Declaration of Authorship

I, Wassim J. Mughal, declare that this thesis entitled '***A Low-Cost Laser Grooved Interdigitated Back Contact Solar Cell'*** and the work presented in it are my own and have been generated by me as the result of my own original research.
I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University;

- Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;

- Where I have consulted the published work of others, this is always clearly attributed;

- Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;

- I have acknowledged all main sources of help;

- Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

- Parts of this work have been published / are to be published as:
    1. Mughal, W. J., H. A. Mughal, A. G. Laffoley, D. M. Bagnall, N. E. B. Cowern, S. Simdyankin, and S. A. Boden. "A high-efficiency, low-cost IBC cell using doped laser cut back-side contacts." Proceedings of the 10th Photovoltaic Science Application and Technology Conference (PVSAT-10), April 2014.

    2. Mughal, W. J., H. A. Mughal, A. G. Laffoley, A. Tarazona, S. Simdyankin, D. M. Bagnall, Stuart A. Boden, and N. E. B. Cowern. "HELICS cell: Laser-cut grooves to create a high-efficiency, low-cost IBC solar cell." In *2014 IEEE 40th Photovoltaic Specialist Conference (PVSC)*, pp. 2514-2518. IEEE, 2014.

    3. European Patent 'Deep Grooved Rear Contact Photovoltaic Solar Cells', Patent number: EP2356687B1, granted 12.10.2016 Bulletin 2016/41

Signed:

Date:

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A very special thank you must be given to Dr Stuart Boden my supervisor, who picked up my project and made me feel welcome and part of the group even though I was based elsewhere. His wisdom, guidance and insights particularly through the difficult times have been both greatly appreciated and valued. His friendship and advice have been essential in getting me to this stage.

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There is no possible way that a project of this magnitude can be taken on part time without some sacrifices being made. My wife Heather has had to endure large periods of me being absent both mentally and physically during this project and has not only put up with this but has supported it. Without her love and encouragement, I wouldn't have been able to do this. I love you.

Chapter 1 Introduction

1.1 The Global Energy Situation

Global energy consumption is increasing. More and more of the world's ever-growing population have greater energy requirements as the world continues to develop. Global primary energy consumption grew at a rate of 2.9% in 2018, the fastest growth in consumption since 2010, well above the 10-year average annual global energy growth being 1.5% [1]. Figure 1.1 shows the breakdown of the sources of electricity production that are currently used to meet the global energy requirements. From this diagram it is evident that only 23% of electricity is produced from renewable sources.

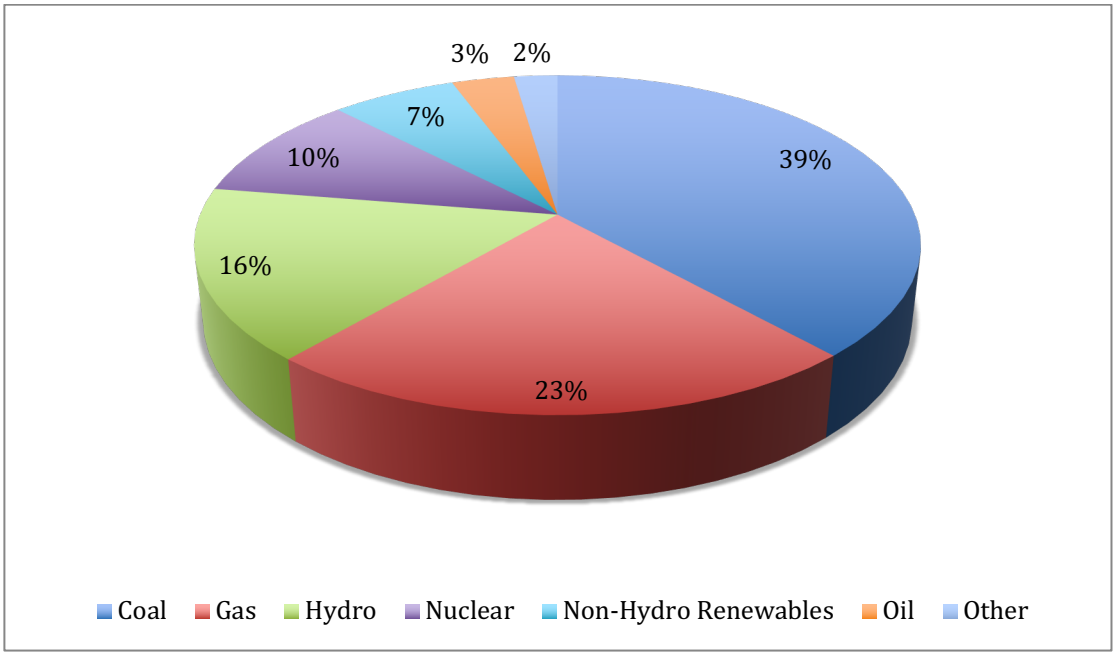


***Figure 1.1** - Global electricity production in 2017 by source.* [2]

The largest sources of global electricity production are currently coal and gas accounting for 63% of production in 2017. These fossil fuels are a finite resource that is running out, and the use of these sources for the production of electricity result in large emissions of CO_2 which has significant detrimental effects on the environment.

Figure 1.2 shows how the reserves-to-production ratios of both oil and gas have declined over time.

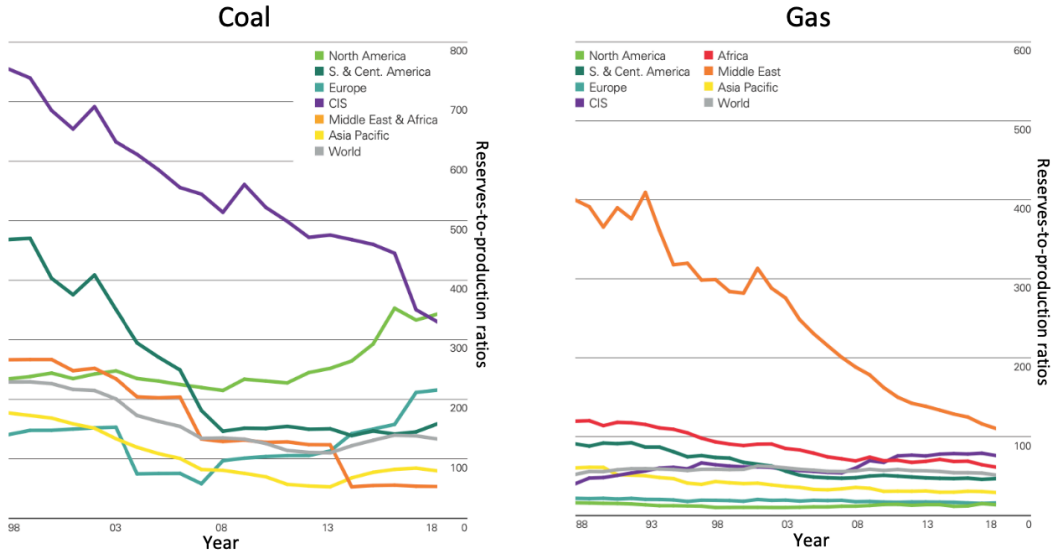


***Figure 1.2** – Reserves-to-production ratios of coal and gas over time* [1]

As the need for energy grows, so does the need to be able to depend upon a source of electricity production that results in a reduction of CO_2 emissions and is more abundant than coal or gas.

1.2 Using the Sun as an Energy Source

In 1839, the French physicist Alexandre-Edmond Becquerel demonstrated that there was a direct relationship between light and electricity [3]. However, it was not until after the development of the diode in 1938 and transistor in 1948 that it was possible to create solar cells. In 1954, Bell Labs patented the first silicon solar cell [4], which became the starting point for creating more efficient solar cells and thus the commercialization of the photovoltaic industry. These early solar cells had an efficiency of around 6% (which itself was a great improvement on earlier developments that had only yielded efficiencies of tenths of one percent). Between 1957 and 1960, Hoffman Electronics improved cell efficiency to 14% during which time the first solar powered satellite 'Vanguard I' was launched [5]. During the 1970s,

as a result of the energy crisis and oil embargos, the exploration of alternative energy sources increased considerably. It was during this time that Elliot Berman of the Exxon corporation identified that in order to create a demand for photovoltaics, the price per watt had to be reduced from the then current $100 down to $20 [6]; a feat that was achievable when Berman realized that silicon with minor imperfections, which was unsuitable for electronics applications, could be used for solar cells [6].

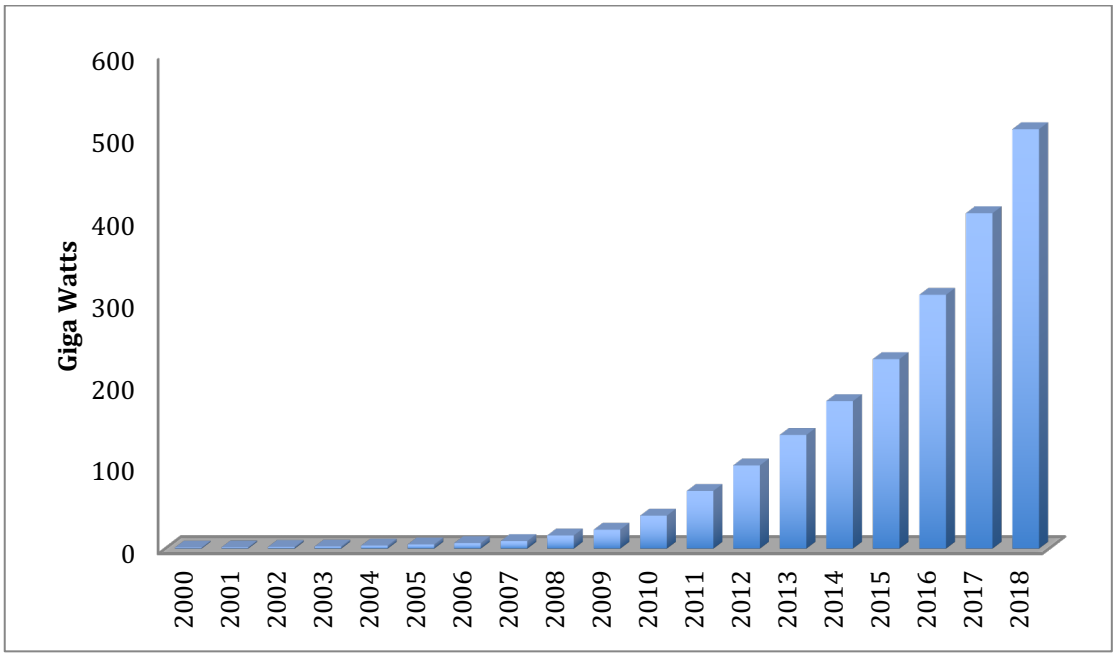


Figure 1.3 - *Global cumulative PV installations* [7]

During the 1980s, solar cells were becoming popular in consumable electronics, with devices such as pocket calculators and wristwatches incorporating tiny solar cells as their power source. By now, environmental concerns were beginning to become prevalent and incentives to build clean energy sources to reduce the amount of energy obtained from traditional sources such as coal and oil were introduced. During the 2000s, the falling costs of photovoltaic installations, coupled with the feed in tariff incentives that were available in some countries, contributed to an exponential growth in installed photovoltaics as shown in Figure 1.3.

1.3 Photovoltaic Costs

In 2010 the average cost of a home solar installation was $7.34 per watt. This cost has fallen year on year with NREL estimating that the average installation price was just $2.70 per watt in 2018 giving a 65% drop in price over 8 years (2018 USD per Watt DC used) [8]. Figure 1.4 shows how the decline in PV module cost over time fits with Swanson's Law, an observation named after Richard Swanson, the founder of SunPower Corporation. Swanson's Law states that the price of solar photovoltaic modules tends to drop 20% for every doubling of cumulative volume [9].

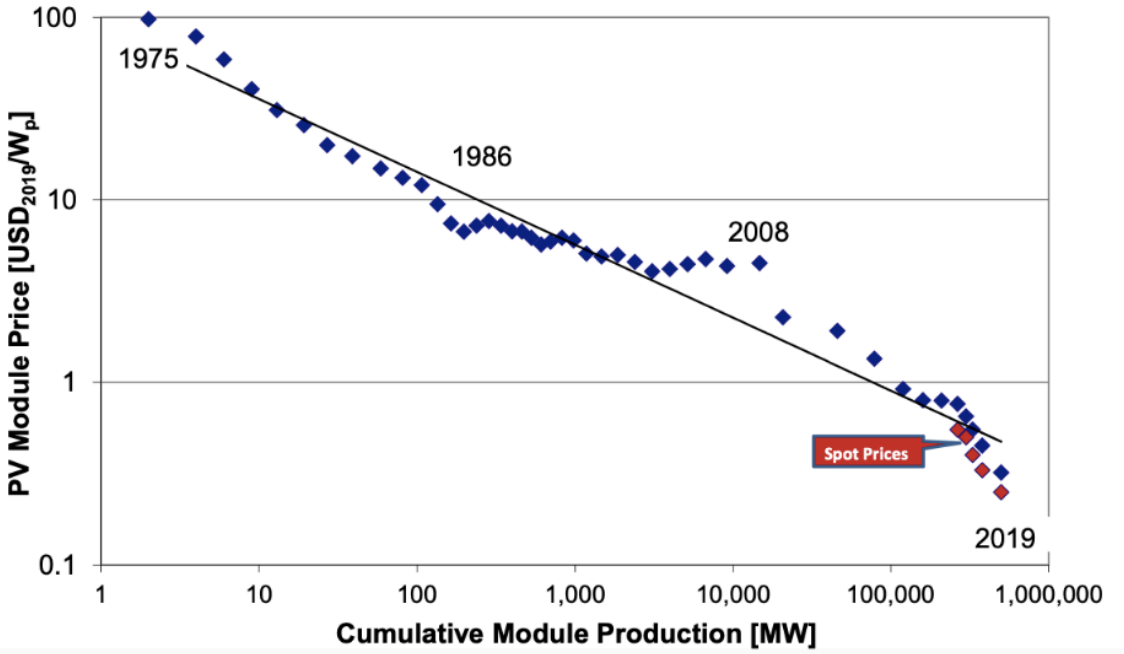


***Figure 1.4** –Decline in PV module prices as PV module production increases* [11]

As the importance of climate change has risen up the political agenda, many nations have pledged to dramatically cut their carbon emissions. As one approach to achieving this, several nations have tried to encourage the production of clean energy by introducing government backed feed in tariffs (FITs). These FITs paid consumers a fixed price for energy that they produced from green sources such as photovoltaic panels. This led to a huge increase in domestic installations of solar panels, as the payback period for the initial capital outlay was short enough to allow several years of

profits to be made by the consumer. These FITs helped with the increase in installed global PV capacity (as shown in Figure 1.3) which in turn allowed the pricing to follow Swanson's Law, resulting in the lowering of module costs (as shown in Figure 1.4).

1.4 Market Situation and Opportunity

In 2010 the global solar cell production volume was estimated at 23.5 GWp with the market capitalisation of the top 30 PV companies being €36.4 billion [10]. Just 8 years later in 2018, the global solar cell production volume had grown to an estimated 114 GW [11]. The market continues to grow strongly with a compound annual growth rate (CAGR) of over 40% since 2000 [11] with medium scenario growth rates of 18% predicted for 2022 [12]. In their 2019 PV status report, the European Commission states that the newly installed capacity of solar photovoltaic power increased by 7% in 2018 to approximately 107 GW. This figure represents more than half of all renewable capacity installed (excluding hydro) in 2018, and solar energy attracted 42.5% of all new renewable energy investments or $140 billion USD [11]. In October 2014, the European Council agreed on a new 2030 framework for climate and energy in which they specified a target of at least 27% of produced energy to come from renewable resources [13]. Within the PV market, there are several different types of technology used, however as shown in Figure 1.5 it is silicon technologies that are dominant.

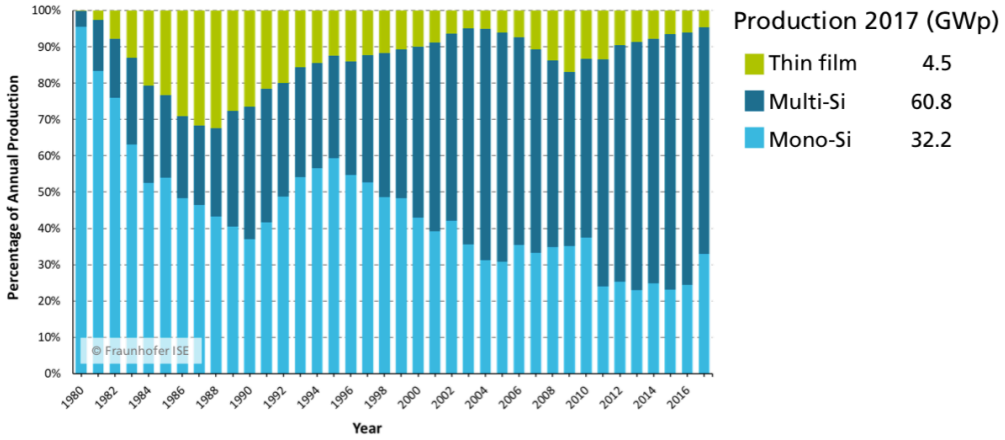


Figure 1.5 - *Annual global PV production by technology* [14]

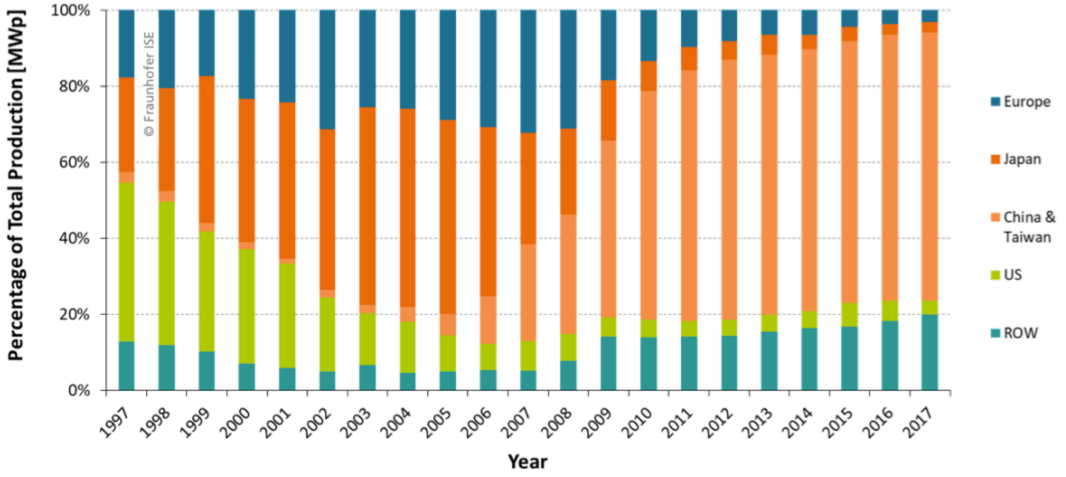


Figure 1.6 - *PV module production by region* [14]

Figure 1.6 shows that in 1997 90% of PV module production was in the US, Europe and Japan however this dropped to 10% by 2017 with Chinese and Taiwanese companies growing from a tiny market share in 1997 to dominate and become the largest PV module manufacturers in the world over the same 20 year period. This monumental shift came about because of the lack of production capacity to meet the demand for PV modules that was created by government incentive programs to promote domestic rooftop PV installations in counties such as Germany, Spain and Italy. Prior to this point, China had only a very small PV industry whose focus was on

using solar energy only as a source of electricity in rural areas remote from the power grid. As the global demand grew the Chinese government incentivised solar firms to manufacture in China with tax credits and cheap, skilled labour that allowed manufacturing costs resulting in the ability to produce cheaper modules than was possible in the US, Europe or Japan. Most manufacturers within the Chinese/Taiwanese region are all producing similar products, typically at the rate of 5 to 10 GWp each per annum and there is price competition to maintain or grow market share. This has helped to drive market prices down, from around 14,000 €/kWp to 1,070 €/kWp for a typical 10-100 kWp PV rooftop system, a net price regression of 92% over a 28 year period [14]. A large contributor to the recent fall in price has been the substantial growth in the supply of polysilicon, currently in the region of 580000 tons per annum [15] but future cost reductions must be found in other ways. One area of potential cost reduction where a lot of research is being done is to increase solar cell efficiencies. When considering a PV system, if a solar array can give the same output with fewer panels then the overall savings propagate due to the reduction in additional system costs (mountings, wiring etc.). This is known as the balance of system costs for installation.

The Levelised Cost of Electricity (LCOE) is becoming the standard way of comparing the lifetime costs of different types of power source. This is particularly useful for PV installations as the formula takes into consideration annual running costs, which for a PV system are minimal, as well as lifetime and initial costs. For the calculation of LCOE for new power plants, the following applies [16]:

(1.1)

$$LCOE = \frac{I_0 + \sum_{t=1}^{n} \frac{A_t}{(1+i)^t}}{\sum_{t=1}^{n} \frac{M_{t,el}}{(+i)^t}}$$

Where *LCOE* is the Levelised Cost of Electricity in USD/kWh, $\mathbf{I_0}$ is the investment expenditure in USD, $\mathbf{A_t}$ is the annual total cost in USD per year **t**, $\mathbf{M_{t,\,el}}$ is the produced amount of electricity in kWh per year, **i** is the real interest rate in %, **n** is the economic lifetime in years and **t** is the year of lifetime. Figure 1.7 shows the LCOE for a variety of different power generating technologies based on power plants in different locations in Germany in 2018. It is clear to see from this chart that PV systems compete well against all other energy conversion technologies when the LCOE is considered.

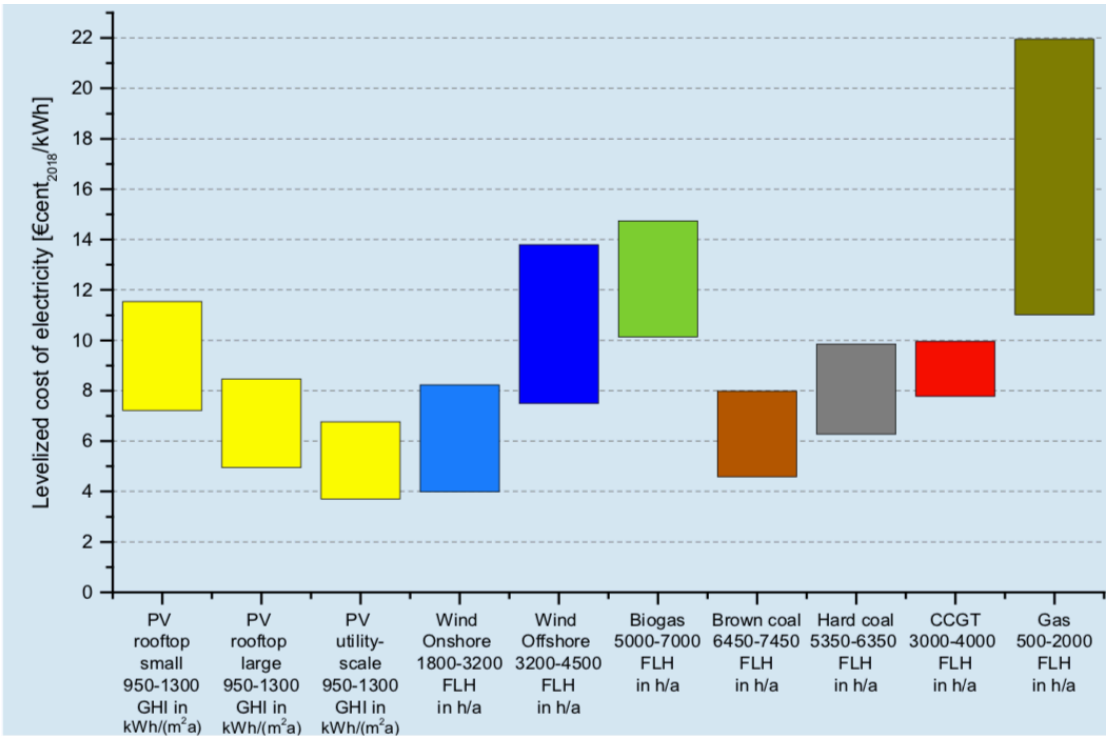


Figure 1.7 - *LCOE of different power generation technologies* [17]

Many manufacturers now routinely produce cells with power conversion efficiencies greater than 20%, however these come at a relatively high costs due to the capital required in order to convert or scrap existing cell production lines. An opportunity

exists for a cell that can be produced with a higher than 20% efficiency using conventional solar grade silicon without any additional costly processing steps.

1.5 Research Focus

This project will primarily focus on identifying, designing, modelling and fabricating a cost effective, efficient and manufacturable crystalline silicon photovoltaic cell. Various existing geometries will be reviewed; however, the key features are that the additional processing costs and steps must be minimised, the initial starting material costs must be minimised, and the device must have a high efficiency. The key premise of the thesis is to try and develop a high efficiency PV cell using low cost fabrication techniques so that the device can be fabricated on existing PV cell production lines with minimal capital expenditure. Various novel ideas will be considered and used to enable this to be achieved. A successful outcome will be achieved if the final solution can be modelled to show good potential efficiencies, and a working device can be fabricated using the proposed device geometry.

1.6 Thesis Structure

Chapter 2 of this thesis will look at the physics of photovoltaics and how they work and proceed to provide an overview of current photovoltaic technologies, discussing their merits and limitations. Chapter 3 will present the fabrication and characterisation methodology. It will look at the processing stages of the Saturn solar cell (a laser-processed cell developed by BP Solar) and how this can be adapted to make an interdigitated back contact device. Chapter 4 will present the initial device design and experimentation for this project which aims to prove that the chosen device geometry can produce a working solar cell. Chapter 5 will present modelling work that includes an optimization of the thin film antireflection coating and then a Technology

Computer Aided Design (TCAD) simulation of the full cell, for which various design parameter sweeps are performed. Chapter 6 will detail the fabrication processes investigated to try and build on the areas of improvement highlighted by the modelling chapter. Finally, Chapter 7 will present the conclusions of the work done and the further work prospects that have been identified to continue the project.

Chapter 2 Literature Review

2.1 Physics of a Photovoltaic Cell

Conventional solar cells that are seen in everyday applications are known as photovoltaic (PV) cells. These as the name implies (photo meaning 'light' and voltaic meaning 'electricity'), convert sunlight directly into electricity. As shown in Figure 1.5, most PV cells are made from the group IV element silicon which is a semiconductor. Figure 2.1 shows the arrangement of electrons within a single atom of silicon.

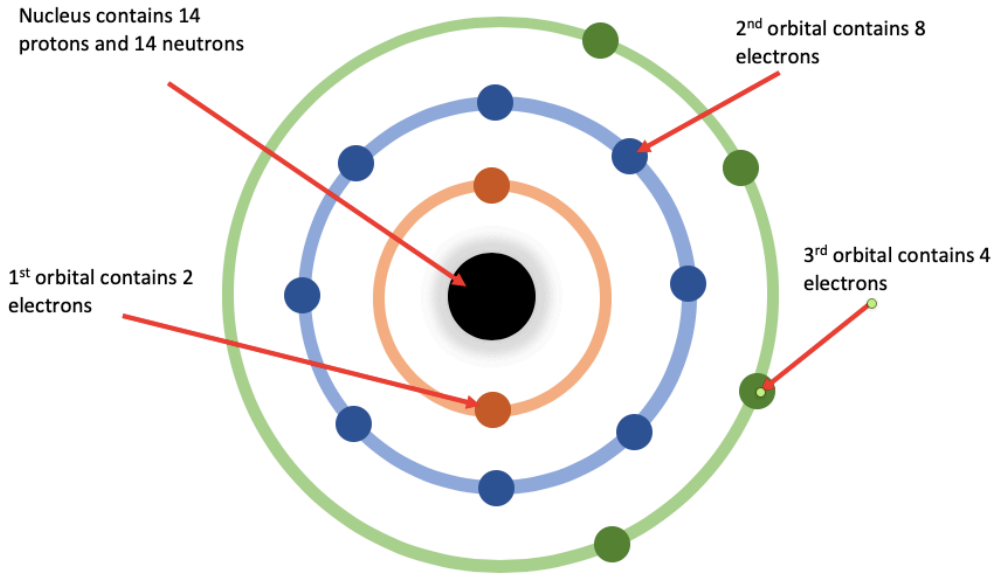


***Figure 2.1** - Atomic structure of silicon*

A single atom of silicon contains 14 electrons, which are arranged within three different atomic orbitals. The first orbital contains two electrons, and the second orbital contains eight electrons, thus both of these orbitals are completely full. The third orbital however is not full and contains only four electrons. The outermost orbital of an atom is known as the valence band, and the electrons that exist in it are

known as valence electrons. In silicon with no impurities (known as intrinsic silicon), these valence electrons are shared with four surrounding silicon atoms forming pairs of covalent bonds forming a crystal lattice as shown in Figure 2.2.

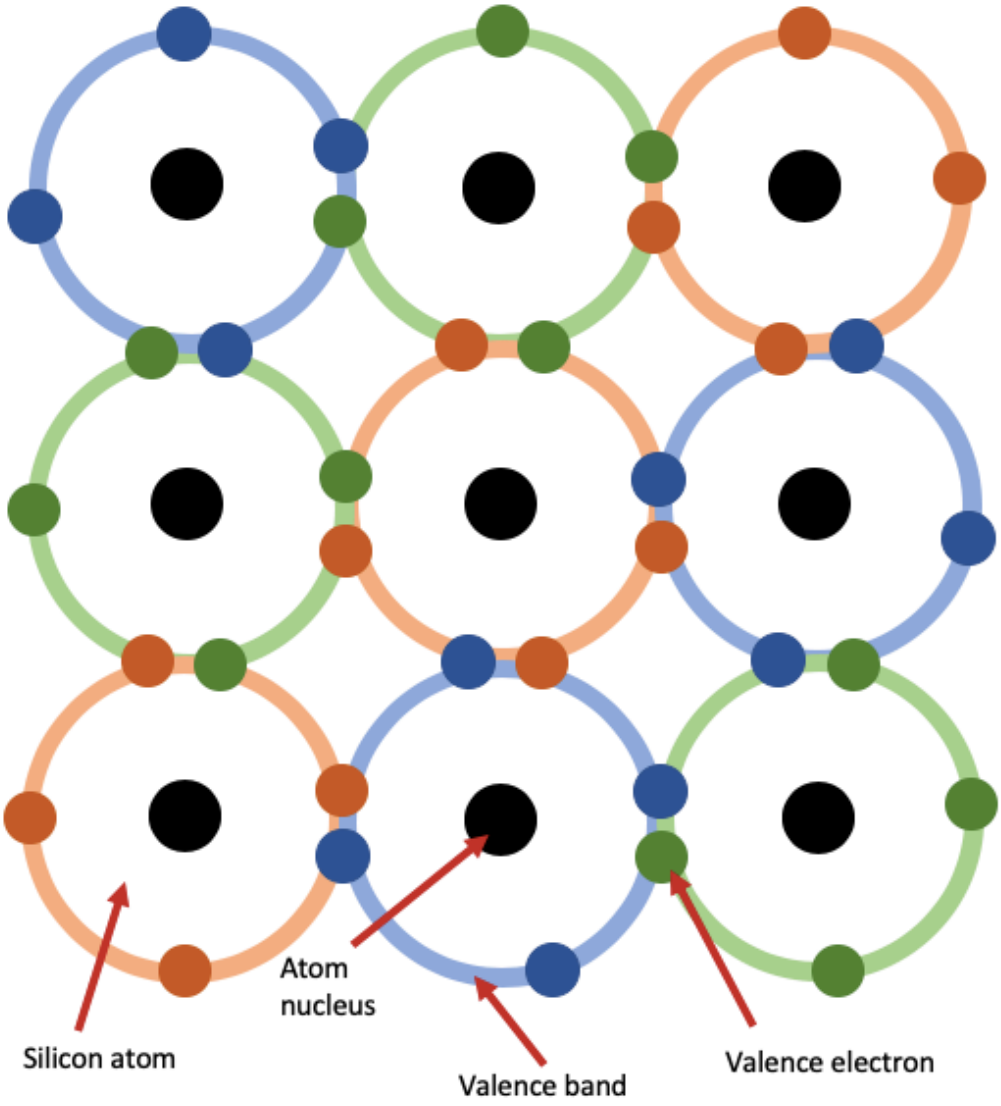


***Figure 2.2** – Intrinsic silicon molecule showing 9 silicon atoms forming part of a crystal lattice*

In order for conduction to occur, electrons need to be able to move about the crystal lattice, out of the valence band and into the 'conduction band'. For this to happen the electrons need energy. An electron is considered 'mobile' when it gains enough energy to participate in conduction and is known as being 'excited' or in a high

energy state. Conversely, an electron that does not have enough energy to participate in conduction remains in the valence band of its atom and is known as being 'bound' or in a low energy state. The minimum change in energy required for an electron to break from its bound state and become excited in order to participate in conduction is known as the 'energy band gap'. The lower the band gap is, the easier it is for electrons to become excited therefore the easier it is for conduction to occur. Silicon like all semiconductors can act as both an insulator and a conductor. At room temperature there are enough free electrons to allow it to conduct current, it is only at absolute zero that all of the electrons remain bound to the valence band resulting in the material being an insulator. The hypothetical energy level where the probability of an electron occupying it is 50% is known as the 'Fermi level'.

Figure 2.2 shows the valence electrons in intrinsic silicon atoms are all bonded with neighbouring silicon atoms. This leads to intrinsic silicon having a high energy band gap of 1.14eV at room temperature (302K). In order to improve the ease of conduction, impurities can be added to intrinsic silicon in a process known as 'doping'. Donor impurities donate electrons to the conduction band creating more electrons in the conduction band which can move around and carry charge. Acceptor impurities accept electrons from the valence band, creating holes in the valence band which can also move around and carry charge.

As an example, the group V element phosphorous has five electrons in its valence band, as shown in Figure 2.3. When phosphorous is introduced to intrinsic, the phosphorous atom will bond with four nearby silicon atoms, sharing four of its valence electrons to complete the valence band of the silicon atom. However, as there are 5 electrons in the valence band of the phosphorous atom one electron is free to participate in conduction as shown in Figure 2.4 (a). Because this free electron has no

covalent bond to another atom, much less energy is now required to excite it and allow it to break from its bound state.

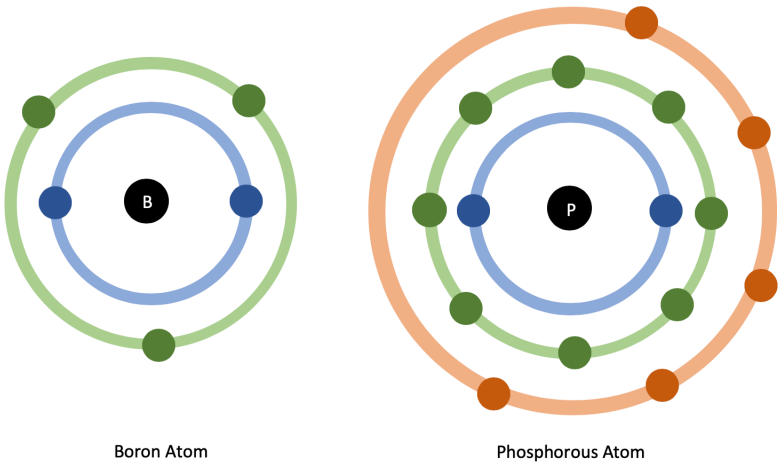


***Figure 2.3** - Atomic structure of boron and phosphorus*

The electron that has broken free of the atom now takes a random path through the crystalline lattice carrying with it an electrical charge.

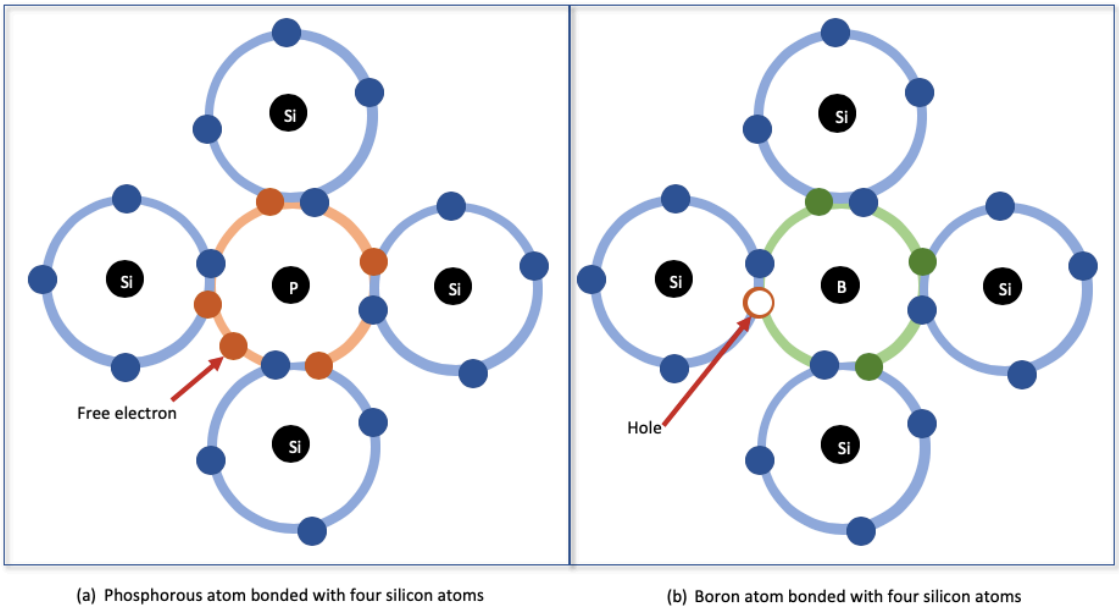


***Figure 2.4** - Atomic structure of phosphorus and boron atoms bonded with silicon atoms*

Silicon doped with elements that have more valence electrons than silicon is known as ‘n-type’ silicon with the name coming from the negative charge of the free electron. Similarly, silicon can be doped with a group III element such as boron (which has three electrons in its outer shell). In this scenario, there are not enough electrons in the valence band of the boron atom to allow it to share a valence electron with each of its four neighbouring silicon atoms. This leaves a hole, as shown in Figure 2.4 (b) that will accept electrons. Boron is an acceptor impurity; it accepts electrons from the valence band which creates holes in the valence band that can move around and carry charge. This type of doped silicon is known as ‘p-type silicon’ because of the positive charge associated with an electron hole.

Electrons and holes in the conduction band are known as charge carriers. In doped silicon where there is a majority of one type of dopant impurity, one carrier type is always greater than the other. The carrier type that has the highest concentration is known as the ‘majority carrier’ and the type of carrier that has the lower concentration is known as the ‘minority carrier’.

A p/n junction is formed at the interface where p-type and n-type doped regions are joined together. First consider a p/n junction with no light shining on it and no load attached to it. At equilibrium there is no net current flow, because the diffusion current flowing from the p-type region to the n-type region, is balanced by the drift current flowing from the n-type region to the p-type region. The p-type region has extra holes and the n-type region has extra electrons. Because of the higher concentration of holes in the p-type region, as a result of this concentration gradient some of them can diffuse into n-type region. This movement of holes creates the diffusion current. Similarly, the electrons can diffuse from the n-type region into the p-type region also causing a diffusion current. When the electrons and holes move

across the p/n junction, they leave behind exposed charges that are unable to move due to being fixed in the crystal lattice. As the diffusion continues, the electrons leaving the n-type region leave exposed positive ion cores and holes leaving the p-type region leave exposed negative ion cores behind. This causes an electric field that points from the n-type material to the p-type. This electric field causes a drift current due to minority carriers (holes in the n-type region and electrons in the p-type region) being pushed away by this electric field that has been created leaving behind a region depleted of charge carrier known as the 'depletion region' as shown in Figure 2.6. Therefore, with no light and no load there is a diffusion current flowing from the p-type region towards the n-type region caused by the concentration gradient, and a drift current flowing from the n-type region towards the p-type region. These currents balance and cancel each other out in this scenario.

A diode is a simple electronic device that restricts the direction of the movement of charge carriers. When a voltage is applied to the diode, it effects the diffusion current within it (as the voltage acts to increase or decrease the barrier to diffusion) but the drift current remains unaffected. If the applied voltage is positive, then it is considered to be forward biased and if the applied voltage is negative then it is considered to be reverse biased. When the diode is forward biased, the diffusion current increases and the drift and diffusion currents are no longer equal so do not cancel each other out. Similarly, when the diode is reverse biased the diffusion current decreases so again the state of equilibrium between drift and diffusion currents no longer exists.

Equation 2.1 shows the ideal diode equation and Figure 2.5 is a sketch of the IV characteristics of a typical diode.

$$I = I_0(e^{\frac{qV}{kT}} - 1)$$

(2.1)

Where:

I = the net current flowing through the diode

I_0 = "dark saturation current", the diode leakage current density in the absence of light

V = applied voltage across the terminals of the diode

q = absolute value of electron charge

k = Boltzmann's constant

T = absolute temperature

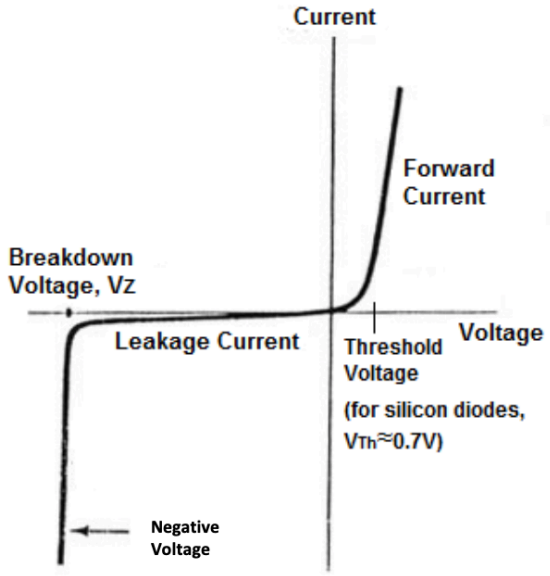


***Figure 2.5** - IV characteristics of a diode* [18]

Figure 2.6 shows the p/n junction, with the depletion region (called space charge region) and the drift and diffusion current directions. Figure 2.7 is an energy band diagram showing the drift and diffusion currents in equilibrium.

Now consider light is shining on the p/n junction under open circuit conditions. Photons can be absorbed as a result of electrons being excited from the valence band into the conduction band creating electron hole pairs, therefore increasing the number of mobile charge carriers in the region. If the hole of the electron hole pair created by

the light in the n-type region approaches the depletion region, the electric field will propel the hole into the p-type region. If the electron moves towards the depletion region from the n-type region it will be repelled by the electric field. Similarly, in the p-type region electrons will be propelled into the n-type region whereas the holes will be repelled by the electric field. The electric field has caused a drift current in the direction from the n-type region to the p-type region. This drift current builds up more holes in the p-type region making it more positively charged and more electrons in the n-type region making it more negatively charged. This creates an electric field which opposes the built-in field at the junction and so lowers the potential barrier, leading to an increase in the diffusion current. A new equilibrium is established whereby drift current and the diffusion current balance each other and a voltage is present across the terminal. This is known as the open circuit voltage (V_{oc}), the generation of which is known as the 'photovoltaic effect'.

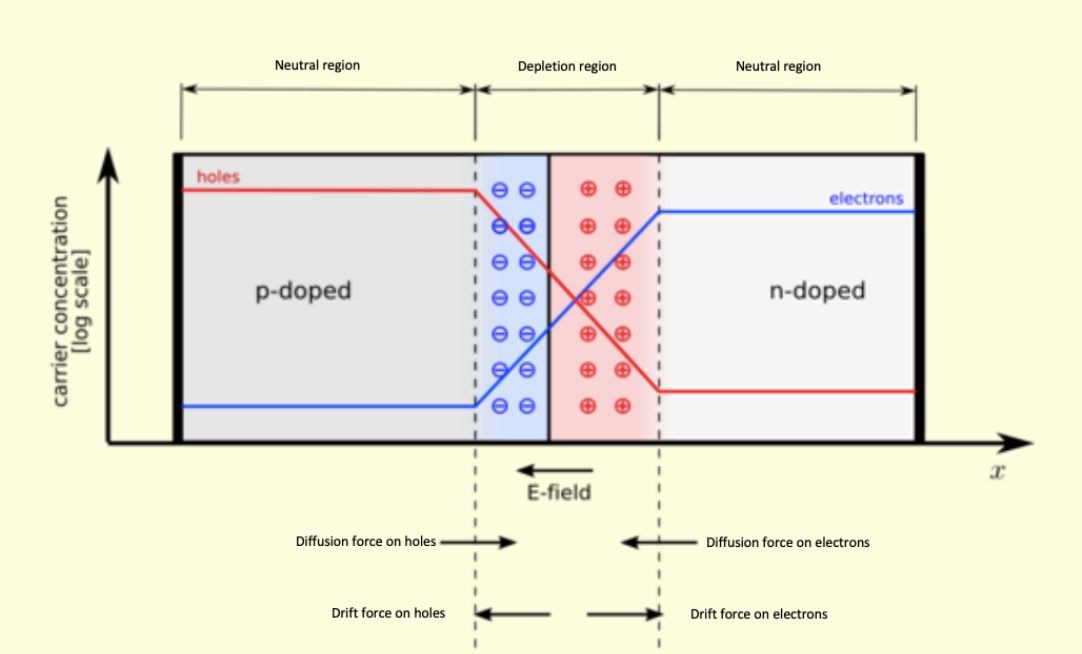


Figure 2.6 - *The p/n junction showing depletion region, and currents* [19]

If a resistance-free wire connects the terminals of the device, there is a current flow but no build-up of charge (and therefore voltage) within the device. This current is known as the short circuit current (I_{sc}).

If a load is added between the two contacts of the illuminated p/n junction whilst light is shone on it, both voltage and current are generated allowing power to be extracted from the device.

Figure 2.7 shows the energy bandgap diagram for a p/n junction at thermal equilibrium where the Fermi levels (E_f) of both the p-type and n-type materials are the same. E_c is the conduction band, E_v the valance band and the depletion region extends from $-X_p$ to X_n.

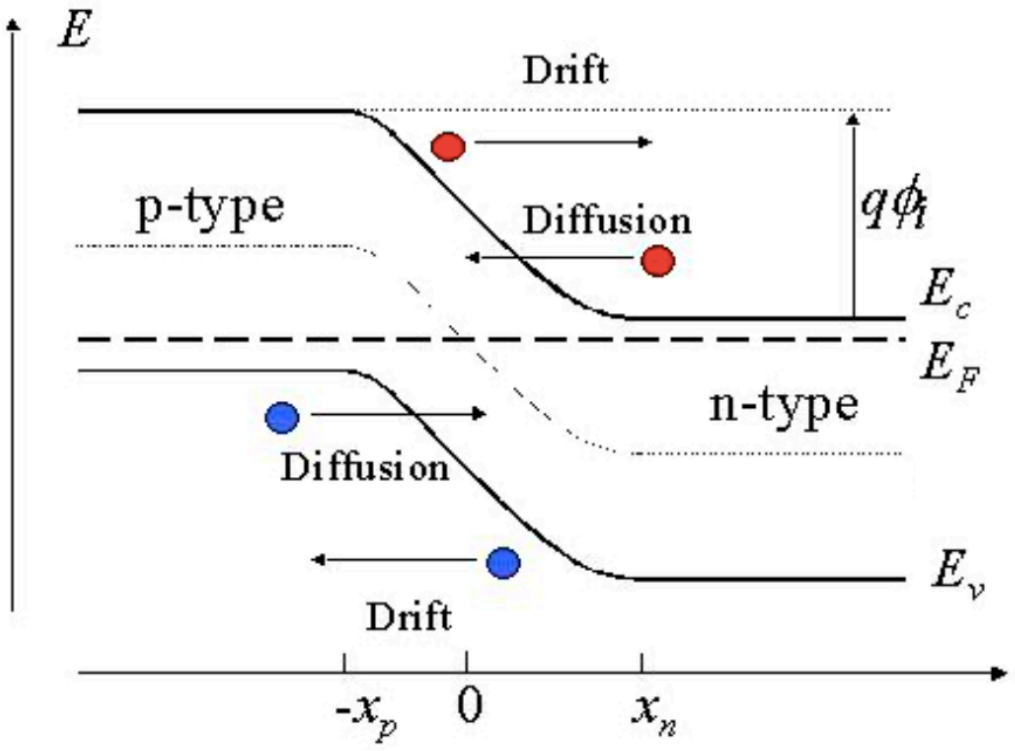


Figure 2.7 - *Energy band gap diagram of a p/n junction, showing electrons (red) and holes (blue)* [20]

2.2 Current-Voltage Characteristics

The efficiency of a solar cell η is defined as the maximum output power density divided by the incoming power density. As equation 2.2 shows, the maximum power density is made up of several components.

$$\eta = \frac{P_{out}}{P_{in}} = \frac{FF \cdot J_{SC} \cdot V_{OC}}{P_{sun}} \tag{2.2}$$

Where

η = Solar cell efficiency

J_{SC} = short circuit current density

P_{in} = Incoming sunlight power density

V_{OC} = open circuit voltage

P_{out} = Maximum output power density

P_{sun} = Power density from the sun

FF = fill factor

These components include the short circuit current density, the open circuit voltage and the fill factor (the ratio of the maximum power point (V_{mp}*I_{mp}) to the product of V_{oc}*I_{sc}). An improvement in any of these aspects will result in increased cell efficiency. Figure 2.8 shows a generic IV curve for a photovoltaic device highlighting the fill factor (FF), open circuit voltage (V_{oc}, the maximum voltage of a solar cell when the net current through the device is zero) and short circuit current (I_{sc}, the maximum current from a solar cell when the voltage across the device is zero). The power curve (blue) is also plotted which gives the maximum power point (P_{max}) which is where the solar cell should be operated in order to give the maximum power output. The maximum power point occurs at a voltage V_{mp} and a current of I_{mp} and is coincident with the point of maximum fill factor.

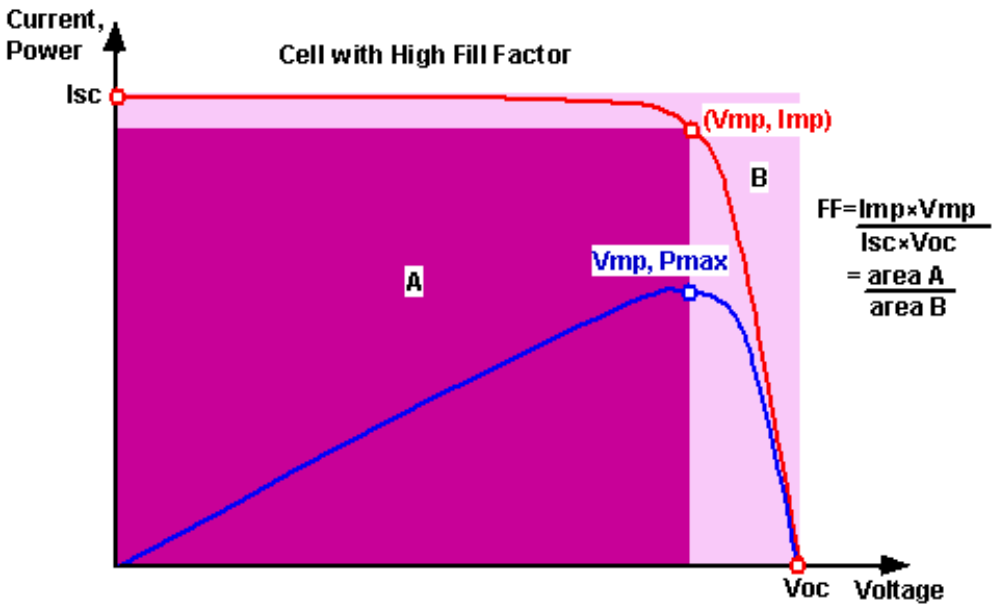


Figure 2.8 - *Generic IV curve of a solar cell* [21]

The parasitic resistances of a solar cell can also be approximated from the IV curve. The inverse of the series resistance (R_s) is approximately equal to the slope of the IV curve as it approaches $V_{OC,}$ and the inverse of the shunt resistance (R_{sh}) is approximately equal to the slope of the IV curve as it approaches I_{SC}. This is explained by considering the ideal diode equation in the presence of parasitic resistances as shown in equation 2.3 [22].

$$I = I_{SC} - I_0\left(e^{\frac{q(V+IR_s)}{kT}-1}\right) - \frac{V+IR_s}{R_{sh}} \tag{2.3}$$

Where R_s is the series resistance and R_{sh} is the shunt resistance. When both R_s and R_{sh} are high, the term involving R_{sh} can be neglected giving:

$$I = I_{SC} - I_0\left(e^{q(V+IR_s)/k_BT} - 1\right) \tag{2.4}$$

Which can be rearranged to make V the subject:

$$V = \frac{k_B T}{q} \ln\left(\frac{I_{SC} - I_0 - I}{I_0}\right) - IR_s \tag{2.5}$$

Differentiating gives:

$$\frac{dV}{dI} = \frac{k_B T}{q}\left(\frac{1}{I_{SC} - I_0 - I}\right) - R_s \tag{2.6}$$

At the open circuit point, I = 0 and V = V_{OC}

$$R_s = -\frac{dV}{dI}_{V=V_{OC}} - \frac{k_B T}{q}\left(\frac{1}{I_{SC} - I_0}\right) \tag{2.7}$$

As I = 0, the second term of equation 2.7 is small so this gives the following approximation:

$$R_s \approx -\frac{dV}{dI}_{V=V_{OC}} \tag{2.8}$$

Similarly, equation 2.3 can be manipulated in order to give an approximation for R_{sh} when both R_s and R_{sh} are low so R_s can be neglected:

$$I(V) = I_{SC} - I_0\left(e^{qV/k_B T} - 1\right) - \frac{V}{R_{sh}} \tag{2.9}$$

Differentiating this gives

$$\frac{dI}{dV} = -\frac{q}{k_B T} I_0 e^{qV/k_B T} - \frac{1}{R_{sh}} \tag{2.10}$$

So, at the short circuit point (V = 0, I = I_{sc})

$$\frac{1}{R_{sh}} = -\frac{dI}{dV} + \frac{qI_0}{k_B T}$$

(2.11)

The second term of equation 2.11 is again very small so the following approximation can be made:

$$\frac{1}{R_{sh}} \approx -\frac{dI}{dV}_{V=0}$$

(2.12)

The parasitic resistances can determine how well a solar cell will perform. Low shunt resistances (R_{sh}) cause power losses in solar cells as they indicate the presence of alternative current paths for the current that is generated by the light. This will reduce the amount of current flowing through the p/n junction of the solar cell, which in turn reduces the voltage produced by the cell. Because at low light levels there is less light generated current, this effect is then magnified when operating in these conditions. Typical values for R_{sh} are 1000-1000000 Ω.

Series resistance (R_s) comes about in one of three ways. Firstly, through the movement of current through the emitter and base of the solar cell, secondly the contact resistance between the metal and semiconductor and finally the resistance of the metal contacts. A high series resistance value can impact negatively upon the device by lowering the fill factor and possibly reducing the short circuit current (I_{sc}). Typical values for R_s are between 0.5-1.3 Ω.

2.3 Carrier Recombination

Recombination can be considered the opposite of generation. If generated electron-hole pairs recombine before they are separated (or "collected") by the p/n junction, they cannot contribute to the current produced by the cell. Therefore, minority carrier recombination should be minimized to maximize cell performance. There are three

types of recombination that can occur in the silicon bulk and its surfaces: Auger, Shockley-Read-Hall (SRH) and Radiative. When fabricating a cell, recombination can be reduced by passivation through either chemical, field effect or both.

2.3.1 Minority Carrier Lifetime

The fundamental principle of a solar cell is that when an external energy source (light from the sun) is presented to the device, the number of minority carriers is increased above that at equilibrium. Some of these minority carriers however recombine and cannot contribute to the useful energy generation of the device. The time that these minority carriers remain excited before recombining is known as the effective minority carrier lifetime [23]. As they are related, it can be said that the longer the minority carrier lifetime for a wafer, the lower the recombination rate. Therefore, the longer or higher the lifetime for a wafer, the more efficient the device that can be made from it will be.

2.3.2 Surface Recombination

A silicon wafer such as the kind used in the PV industry will have been sliced from a much larger silicon ingot prior to processing. When the wafer is sliced, the silicon crystal lattice can become disrupted leaving dangling bonds at the surface as shown in Figure 2.9.

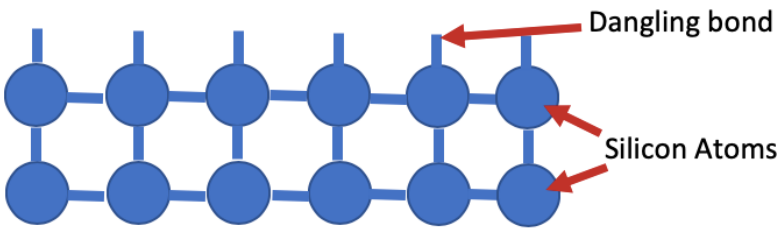


***Figure 2.9** - Atomic structure of silicon showing dangling bonds at the surface*

Dangling bonds can be considered defects in the silicon, and act as recombination centres leading to minority carrier recombinations. This high recombination rate depletes the region of excess minority carriers.

The industry standard way to reduce the number of dangling bonds at the surface is by surface passivation [24]. A dielectric layer such as silicon dioxide is grown on the surface, which combines with the damaged crystal lattice of the silicon, so as to remove the dangling bonds as shown in Figure 2.10.

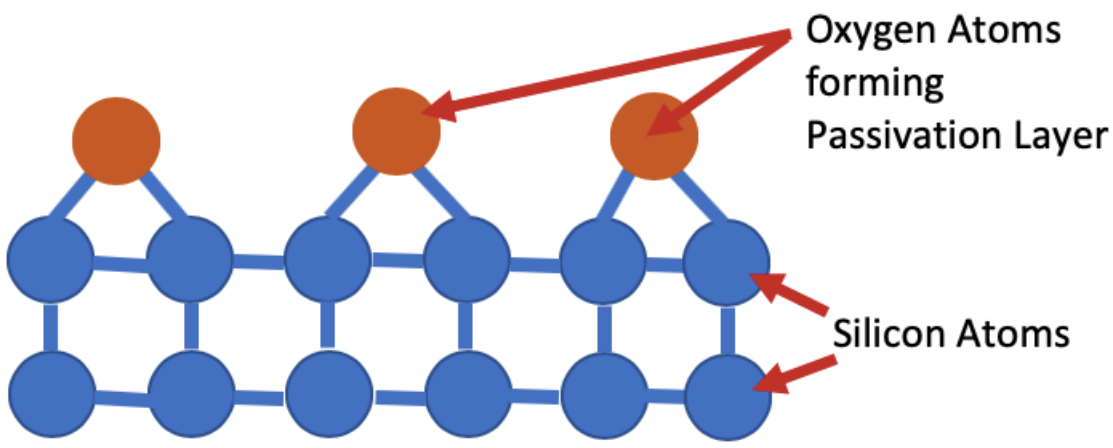


***Figure 2.10** - Atomic structure of silicon showing passivated dangling bonds*

The rate of surface recombination is dependent upon the quality of the passivating layer. The metric used to define recombination at the surface is the surface recombination velocity (SRV).

2.3.3 Other Types of Recombination

Recombination can occur in the silicon bulk as well as at the interfaces with other films and the device surface. There are different types of recombination, both radiative and non-radiative.

2.3.3.1 Radiative Recombination

Radiative recombination, also known as band-to-band recombination occurs when an electron in the conduction band recombines with a hole in the valence band [25]. The energy lost by the electron as a result of this recombination is released as a photon as shown in Figure 2.11 with the same or less energy as the one initially absorbed to generate the electron-hole pair. This type of recombination is more prevalent in materials such as GaAs; recombination in silicon cells is dominated by the SRH or Auger mechanisms.

2.3.3.2 Auger Recombination

The Auger effect was discovered in the 1920s by Lise Meitner [26] and Pierre Victor Auger [27] to whom the effect is credited [28]. Auger recombination is a non-radiative recombination mechanism that occurs when an electron and a hole recombine. Instead of the energy being released as a photon as it is done in a radiative recombination, the released energy is transferred to either an electron which is then raised higher into the conduction band or to a hole which is then pushed deeper into the valence band [29] as shown in Figure 2.11. The rate at which Auger recombination occurs is related to the carrier concentration with the Auger rate increasing in areas of high carrier concentrations such as regions that have been heavily doped.

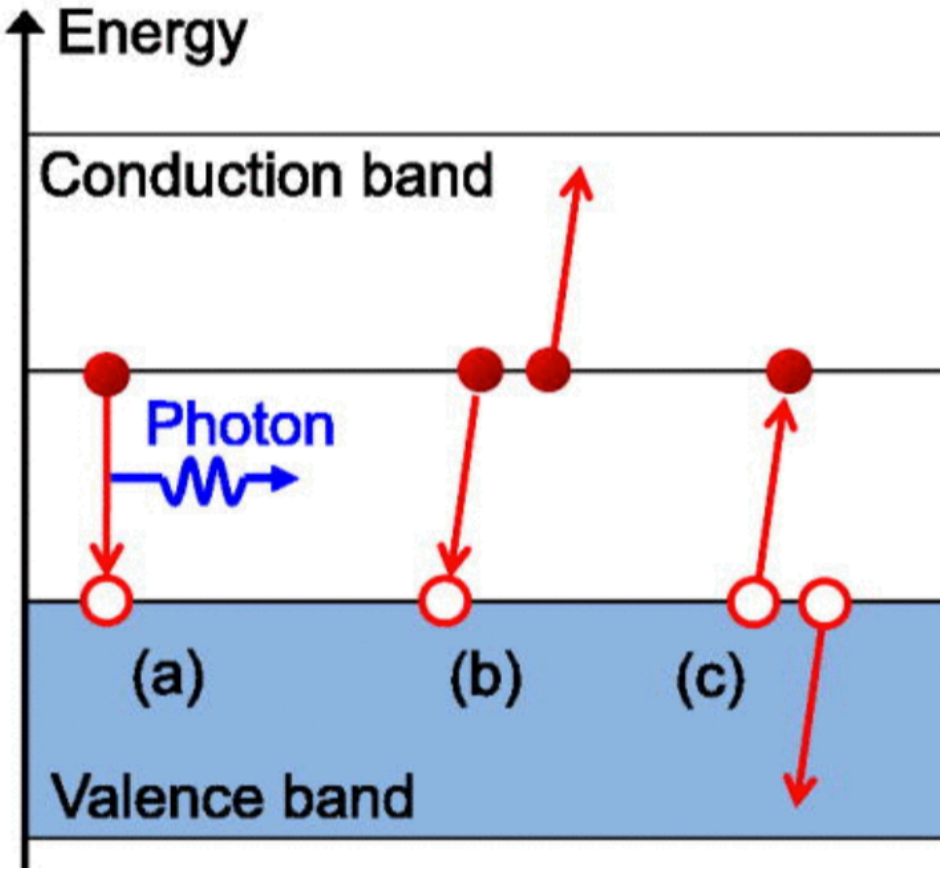


Figure 2.11 *– Radiative recombination (a) compared with Auger recombination (b and c)* [30]

Auger recombination can be minimized by ensuring that the doping levels are optimal.

2.3.3.3 Shockley-Read-Hall Recombination

Shockley-Read-Hall (SRH) recombination was first described in the 1950s [31,32]. It is also known as trap-assisted recombination. SRH recombination occurs when there are defects in the semiconductor crystal lattice. A defect energy level is created between the conduction and valence bands as shown in Figure 2.12.

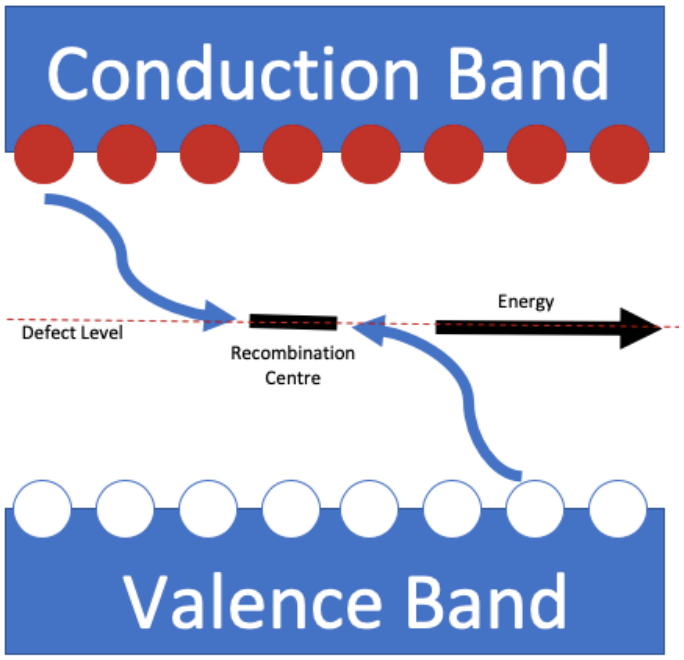


Figure 2.12 - *Diagram showing SRH recombination*

If the defect level occurs closer to the conduction band minimum level, then electrons are more easily captured, and holes are more difficult to capture. Conversely if the defect level occurs closer to the valence band minimum level then holes are more easily captured, and electron trapping is more difficult. The more defects that the silicon has, the more SRH recombination will occur. Defect levels can be removed and therefore SRH recombination minimised at the surface by passivation of the silicon with a dielectric material such as thermally grown silicon oxide [33].

2.4 Types of Crystalline Silicon Wafers used in Photovoltaics

2.4.1 Monocrystalline Silicon

The first solar cells were made from monocrystalline silicon wafers (mono-Si). Monocrystalline wafers can be made using a number of different production methods, the two main ones that are referred to in this body of work are the Czochralski process and float zone growth.

2.4.1.1 Czochralski (CZ) Wafers

The most common production method for producing monocrystalline silicon (as used in integrated circuits and PV cells) is the Czochralski method, named after the Polish scientist, Jan Czochralski who developed it. High-purity silicon (only a few parts per billion of impurities) is melted in a cylindrical quartz crucible at 1425°C to create the feed material. At this point boron or phosphorous can be added to the feed material to dope the crystal either p-type or n-type. A seed crystal with a diameter of a few millimeters is then dipped into the molten feed material forming a melt meniscus.

Figure 2.13 - *Silicon crystal grown using the Czochralski method* [34]

The seed is then slowly withdrawn (often under rotation) and the withdrawn feed material crystallizes at the interface forming a new crystal portion. The shape of the crystal can be controlled by varying the heat, the withdrawal rate and the rotation of the crystal [34]. Figure 2.13 shows a crystal of silicon made using the Czochralski method. The cylindrical crystal (ingot) is then sliced into thin wafers that are used to make PV cells.

The impurity with the highest concentration in CZ wafers is always oxygen which comes from the quartz crucible used to contain and melt the polysilicon. High concentrations of oxygen in silicon wafers can lead to crystal defects as the wafer undergoes high temperature processing during cell fabrication. These defects can then act as recombination centers which lower the overall performance of the solar cell by decreasing the I_{sc} and V_{oc}.

2.4.1.2 Float Zone (FZ) Wafers

Float zone (FZ) silicon is a high purity alternative method for growing monocrystalline silicon ingots. The main difference between CZ and FZ silicon is the number of impurities that exist within each type of silicon. The float zone process was developed by Henry Theuerer of Bell Laboratories. In order to reduce the number of 'light' impurities (such as oxygen and carbon) the float zone process occurs in a vacuum or inert gaseous atmosphere. A high-purity polycrystalline rod is then held face to face in a vertical position with a monocrystalline seed crystal. A radio frequency (RF) heater is then used to create a localised molten zone on the polycrystalline rod which, because of the seed crystal, begins the growth of a new crystal ingot. As the molten zone moves along the polysilicon rod, the molten silicon solidifies into a single crystal. FZ crystals can be doped by adding doping gases into the chamber (phosphine for n-type or diborane for p-type). Unlike with CZ silicon growth where the polysilicon is contained and melted in a quartz crucible, the silicon molten zone in FZ silicon is not in contact with anything other than the inert gas atmosphere and doping gas so there are far fewer impurities. However, because of the much greater cost in producing FZ silicon, no commercially available solar cells are made from it.

2.4.2 Multicrystalline Silicon

Multicrystalline silicon (mc-Si) is a cheaper form of silicon used in the production of PV modules. It is made by casting high purity silicon into large blocks so that a multicrystalline solid is formed with a grain size of around 1 cm. These blocks are then sliced into bricks and then the bricks are wire-sawn into thin wafers. Figure 2.14 is a photograph of a multicrystalline silicon solar cell showing the grain structure of the multicrystalline wafer from which it is made.

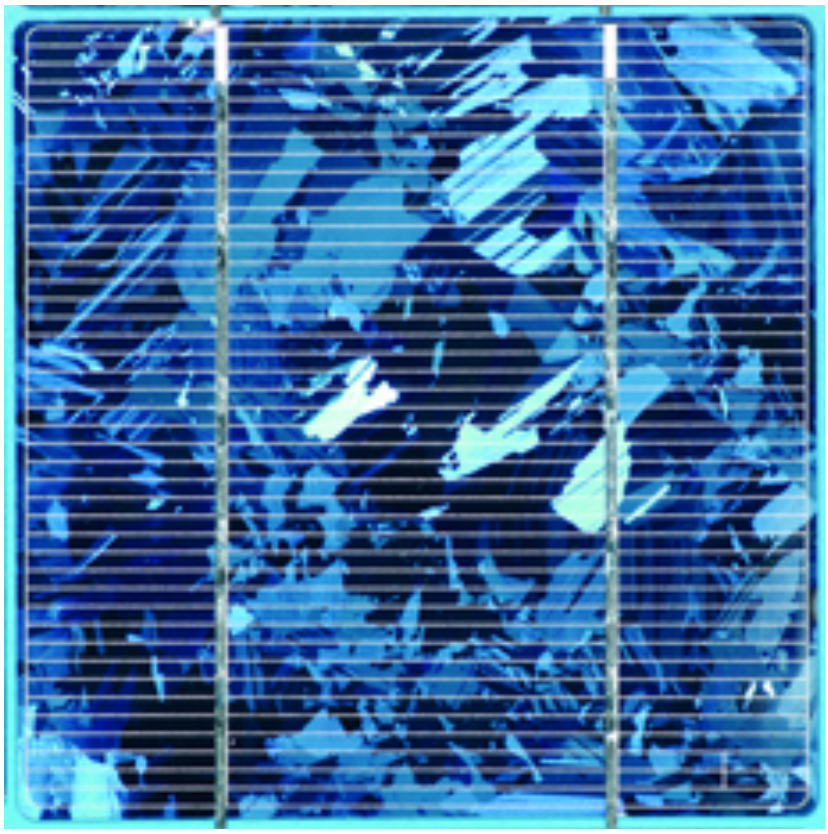


Figure 2.14 – *A multicrystalline solar cell*

The presence of grain boundaries in multicrystalline silicon results in solar cells with lower efficiencies than with mono-Si, however the advantage of multi-Si is that the cost of manufacturing it is lower than mono-Si, thus the unit cost of a multi-Si PV wafer is lower.

2.4.3 N-type vs. P-type Wafers

The very first solar cell produced by Bell Laboratories in 1954 was made using an n-type structure, but early demands for PV technology was driven by requirements in space. It was discovered that p-type silicon was more resistant to space radiation and degradation, so the p-type structure became the dominant technology upon which the PV industry progressed. The n-type wafers are made using phosphorous as the dopant whereas p-type wafers are doped with boron. When CZ silicon ingots are grown, they have high concentrations of dissolved oxygen in them. In the presence of boron doped silicon, this oxygen forms a recombination center known as a boron-oxygen defect. The n-type wafers are immune to boron-oxygen defects as they use phosphorous as the dopant. This leads to wafers that have higher minority carrier lifetimes and therefore wafers that can produce solar cells with higher conversion efficiencies. The lack of boron-oxygen defects also means that n-type cells are not affected by light induced depredation (LID). More and more solar manufacturers are now adopting n-type structures because of these additional benefits. There is little cost difference in producing n-type or p-type wafers, with only economies of scale driving the price of p-type wafers down. This however is starting to have less of an effect as n-type wafers become more commonplace.

2.5 Cell Technologies

Since the mid-1970s the research into producing more efficient solar cells has increased dramatically. Figure 2.15 reproduces the NREL efficiency chart [35] that shows the confirmed efficiencies of various research solar cells to date. As can be seen, no fewer that 29 different types of cell have been forged from a variety of materials. This chapter will now review these various technologies.

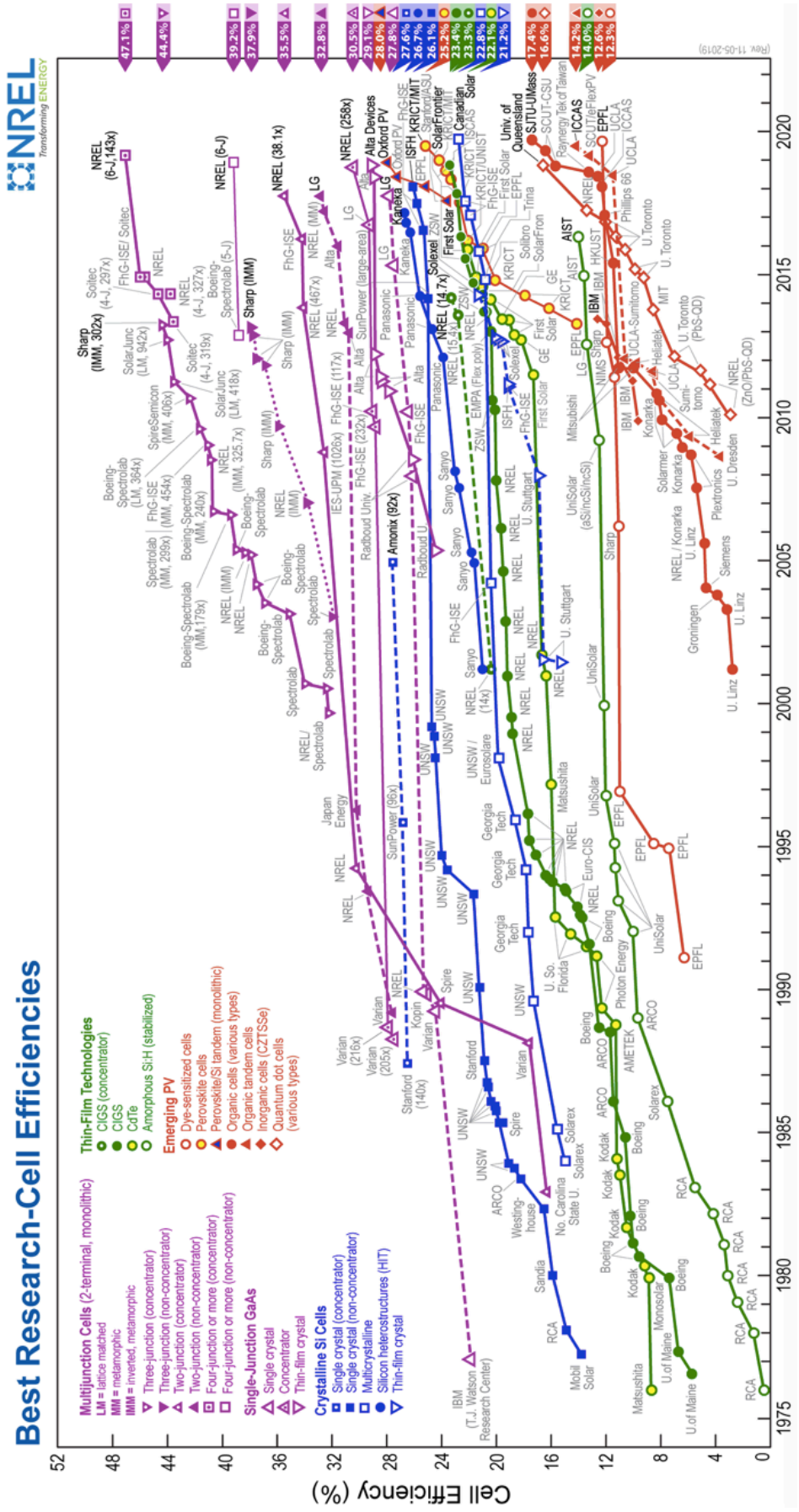


Figure 2.15 – *2019 NREL best research solar cell efficiency chart* [35]

2.5.1 Crystalline Silicon Solar Cells with Aluminium Back Surface Field

Conventional crystalline silicon solar cells with aluminium back surface field (Al-BSF) made from either single or multi crystalline silicon are currently and have for some time been the most common type of solar cell in global production. This cell technology's name is derived from the aluminium that is diffused into the silicon from the back contact which creates a field that repels electrons away from the back surface and so reduces surface recombination. It is comprised of a p/n junction that is parallel to and very close to the n-type surface of this type of cell. It also has metal contacts to the n-type region on the front surface of the cell. Figure 2.16 is a diagram showing these two features.

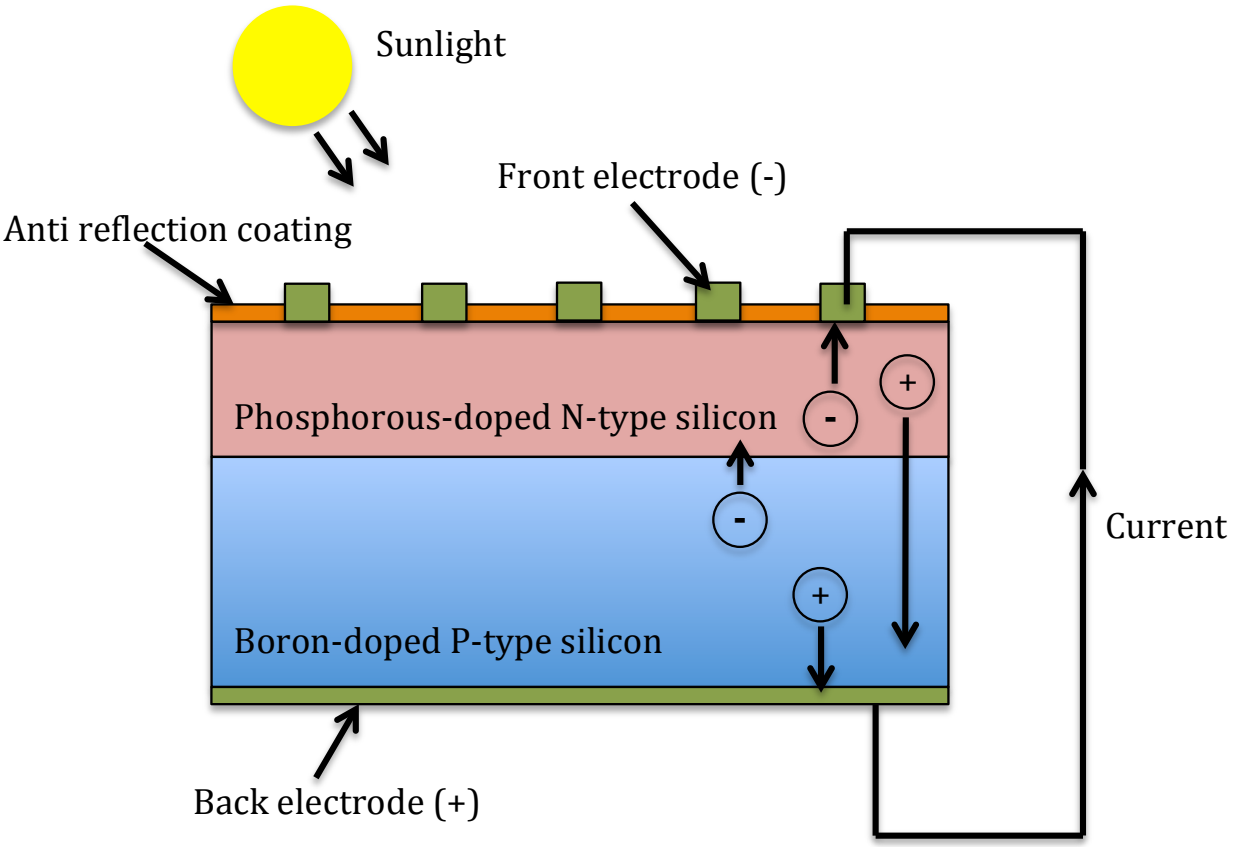


Figure 2.16 - *An AL-BSF solar cell showing the p/n junction and front side metal contacts*

The front surface of the cell is where the light enters the silicon to give the energy needed to generate the electron hole pairs as previously explained. However, the ability to do this is hindered by the metal front contacts on the front surface that cover areas of silicon preventing them from having access to the sunlight, thus creating shaded areas of the solar cell. Removing these contacts would increase the surface area of silicon exposed to sunlight, and therefore theoretically increase the amount of electrical energy that can be produced by a cell however, as is discussed later in this work, experimentally doing this has its own challenges which prevent it from being the dominant solar geometry. The standard Al-BSF types of monocrystalline or multicrystalline solar cell, however, are easy to manufacture and do not include many of the additional efficiency-improving techniques that are described later in this chapter. A typical Al-BSF device is created on a p-type wafer which is then given a strong alkali etch to remove saw damage from the surface of the silicon. For monocrystalline cells, to improve the amount of light that is trapped by the wafer, a selective alkali etch is done that preferentially etches (100) and (110) surfaces leaving (111) surfaces to give the front surface pyramidal texturing. For multicrystalline cells, an acid etch is used to form an 'isotextured' surface for the same reason. The wafer is then doped with phosphorous to create a p/n junction before the edges of the cells are etched so that the n-type regions on the front and rear surfaces of the wafer are no longer directly connected to each other. An antireflective coating is then deposited to improve light absorption before a thick layer of aluminium is deposited onto the rear of the wafer which is then heated to a temperature above 577°C the temperature at which the aluminium and silicon mixture melts (known as the 'eutectic temperature') [36]. As the liquid melts the silicon becomes doped with aluminium which overcompensates the previous n-type doping allowing a contact to be made with the

p-type region of the junction. Silver is then printed on the front surface through a mask to create a busbar and finger pattern (Figure 2.17), creating electrical contacts whilst allowing light into the cell. These metal front surface contacts are heated to a temperature greater than 650°C [37] (with the typical peak temperature being close to 800°C) at which point the silver diffuses through the antireflection coating and makes contact directly with the silicon so that a good front surface metal contact with the n-type region is made.

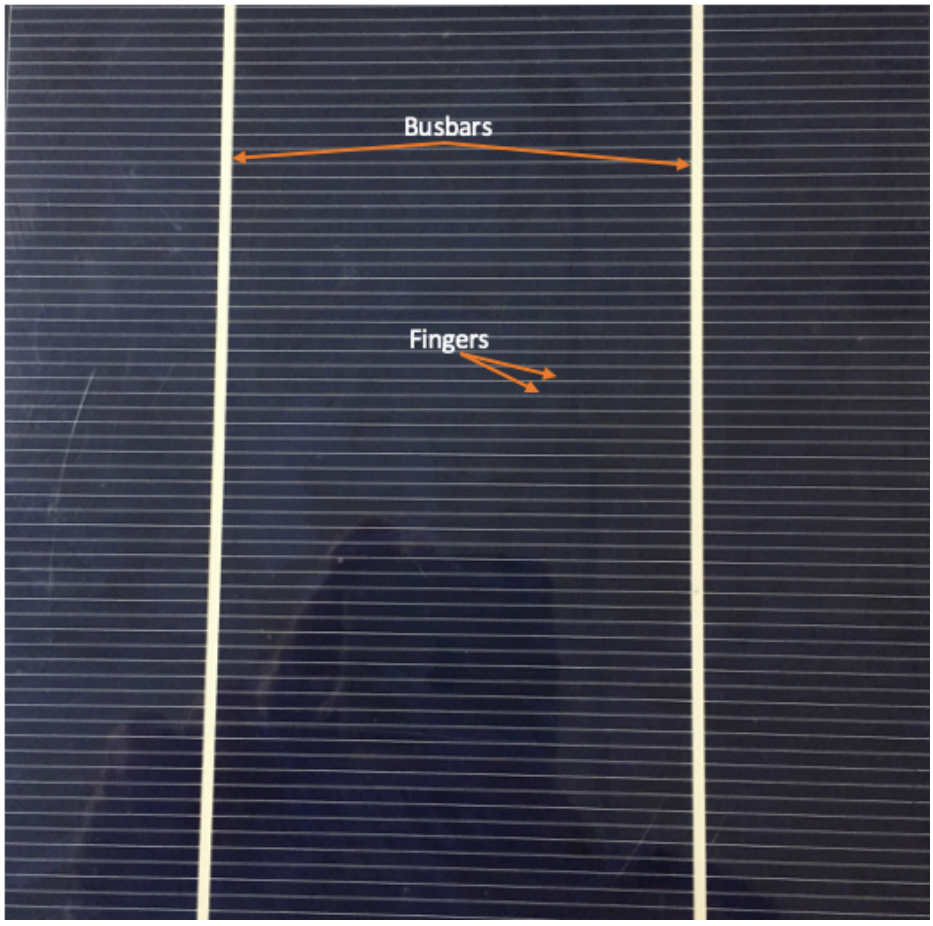


***Figure 2.17** - Photograph of a silicon solar cell showing metal front surface contacts*

2.5.2 High Efficiency Front & Rear Contact Solar Cells

With a proven working geometry, front & rear contact solar cells have been the most common kind of solar cell manufactured for many years. There have been great advances in the efficiencies of these devices over time. Early work into high

efficiency front & rear contact cells was done at the University of New South Wales (UNSW), Sydney Australia. Two of the early high efficiency cells were the PERC (Passivated Emitter and Rear Cell) cell and the PERL (Passivated Emitter, Rear Locally diffused) cell [38].

2.5.2.1 Passivated Emitter and Rear Cells (PERC)

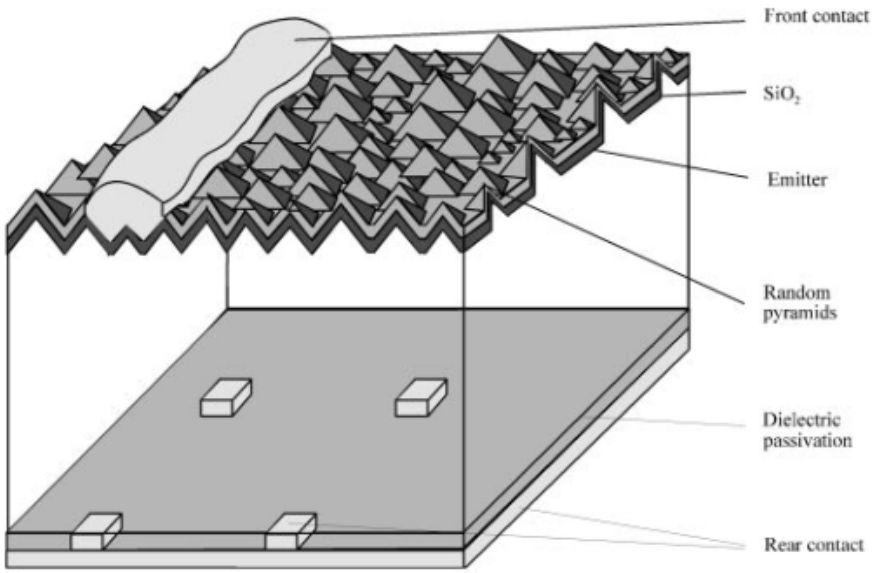


Figure 2.18 - *Random pyramid passivated emitter and rear cell (RP-PERC)* [40]

The PERC cell adds a dielectric passivation layer between the rear metal contact and the silicon as well on top of the emitter on the front surface as shown in Figure 2.18. This SiO_2 passivation layer reduces the number of carrier recombinations at the surface of the cell, acts as an antireflective coating and improves internal reflection of light from the back surface, thus producing a more efficient device. Early devices had a slight problem owing to the difficulty in making a good ohmic contact with lightly doped substrates which was resolved by making the cells on substrates with resistivities lower than 0.5 Ω-cm allowing PERC cells to be produced that demonstrated an efficiency of 22.3% [39]. At the Fraunhofer Institute for Solar Energy

Systems, Germany, a fast scanning laser was developed that enabled the aluminium rear contact to directly connect to the silicon. This was done by blasting through the rear surface passivation and melting the aluminium into the silicon. This method was called the Laser Fired Contact approach, or LFC [40]. These LFC cells have demonstrated 21.4% efficiency on 0.5 Ω-cm and 19.8% efficiency on 10 Ω-cm resistivity substrates and are amongst the highest for production ready silicon cell technologies [41].

2.5.2.2 Passivated Emitter and Rear Locally Diffused Cells (PERL)

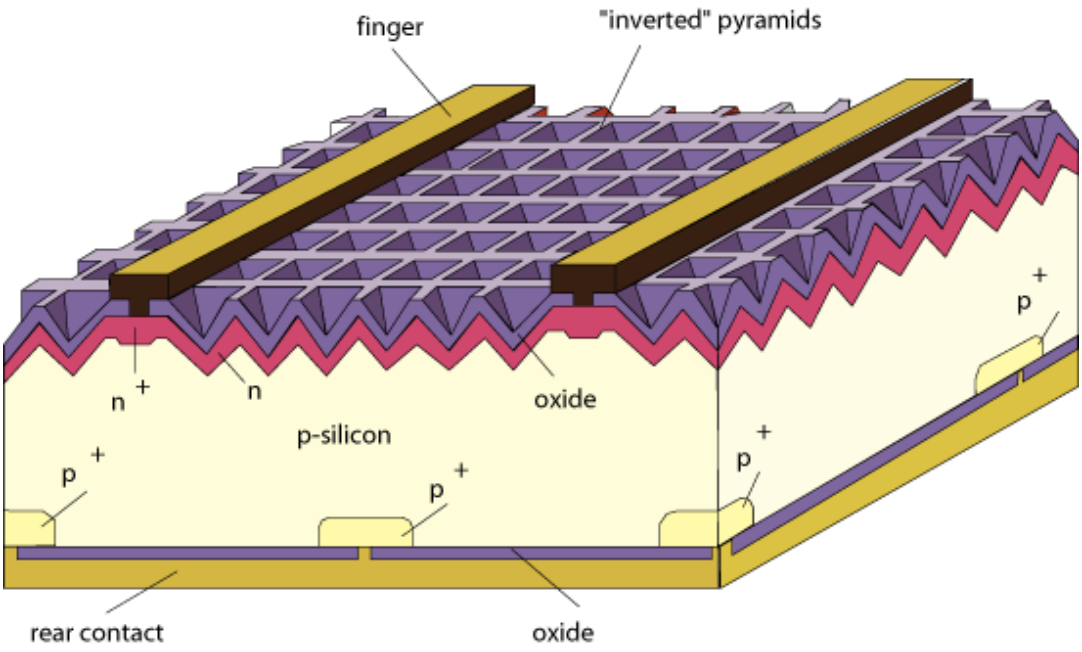


Figure 2.19 - *The PERL cell* [42]

The passivated emitter with rear locally diffused (PERL) cell is another device from the University of New South Wales. This device as shown in Figure 2.19 like the PERC cell from section 2.5.2.1 has a high-quality oxide on the front surface to act as a passivation layer reducing the number of surface recombinations. The PERL cell however has overcome the problems with the metal contacting that the PERC cell geometry had (requiring the PERC cell to have limitations on the substrates used in fabrication). This is achieved by diffusing locally only at the point of metal contact on

the rear surface. This minimises carrier recombination at the rear, but also allows for a good ohmic contact. PERL cells have been measured with cell efficiencies of 25% on monocrystalline silicon [43]. As the PERL cell further features such as double layer anti-reflection coatings (DLAR) [44] where incorporated into the cell design which lead to an enhancement in efficiency over the PERC cell but come at a higher cost.

2.5.2.3 Laser Grooved Buried Contact Solar Cells

Laser grooved buried contact (LGBC) solar cells are traditional front contact solar cells, but instead of having the front contacts screen printed onto the front surface of the solar cell, the contacts are formed by cutting grooves into the silicon with a laser, and then filling these grooves with metal. Screen-printing of front contacts has several problems associated with it, most noticeably that in order to get the volume of metal required down to minimise the series resistance (Rs), the fingers need to be rather wide. This then covers up more of the front surface meaning there is less useful surface area remaining. Buried contact cells do not have this problem. Because the fingers are cut into the silicon, as shown in Figure 2.20, the fingers can be thinner whilst still having the same volume of metal that a thicker screen-printed finger would have. This means that there can be more fingers, spaced closer together whilst retaining a high transparency. The fingers can also be flush or slightly recessed from the surface, therefore reducing any shading across the active surface area, leading to low reflection and therefore higher short circuit currents. As a result of cutting groves into the silicon to bury the contacts, these grooves can be heavily doped for optimal metal contact creating a ‘selective emitter’ whilst the front surface can have lighter doping for optimum current generation. This is not possible in traditional printed cells as there is no way to create a selective emitter for the metal contacts, so the whole front surface must be doped in a way that is not optimal for both metal contact and

current generation. In addition to these benefits, efficiencies are improved further in buried contact cells by the lower grid resistance. This is achieved because of the large volume of metal in the grooves, and by using copper which has a lower resistivity than the metal paste used in screen-printing. The BP Solar 'Saturn' cell is a buried contact solar cell that has been successful in being commercially mass-produced, achieving efficiencies of 18.3% [45].

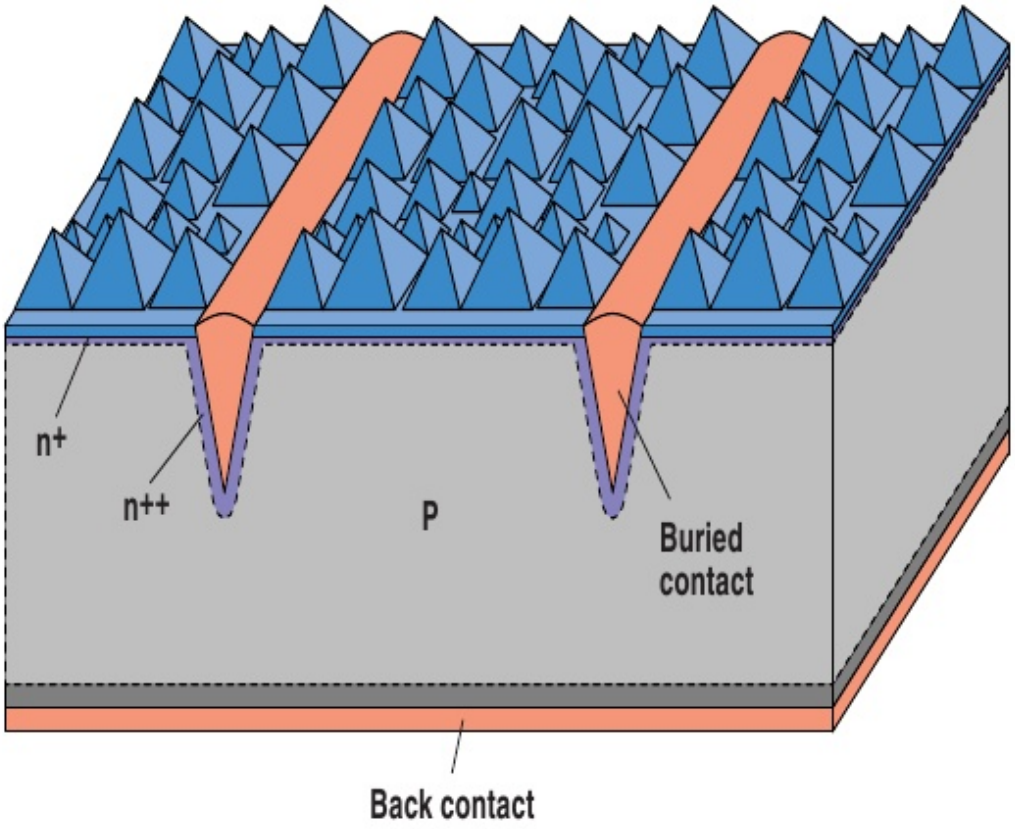


Figure 2.20 - *The laser grooved buried contact cell* [46]

2.5.2.4 Silicon Heterojunction Cells (SHJ)

Silicon Heterojunction (SHJ) solar cells came about in the early 1990s [47], pioneered by Sanyo (until the technology was later acquired by Panasonic) and are made by surrounding a thin crystalline silicon substrate with layers of amorphous silicon. Solar cells using this geometry have been in mass production since the late 1990s and have

reached efficiencies of 25.6% [48]. The SHJ cell differs from conventional crystalline solar cells as different semiconductor materials are used to create the p/n junction and back surface field. This, along with the introduction of an intrinsic layer, which as an excellent passivation layer and therefore helps prevent recombination of minority carriers, and a transparent conducting oxide, means that the SHJ cells show superior conversion efficiencies at high temperatures and higher open circuit voltages (V_{OC}). The temperature coefficient of a standard homojunction solar cell with passivated contacts is -0.35 %/°C [49] whereas SHJ cells exhibit excellent temperature coefficients of -0.23 %/°C [50]. For a 20% efficient cell at 70°C the difference in temperature coefficients between the homojunction and SHJ cells can lead to a temperature related efficiency loss of 5.4% relative [51].

In SHJ cells, the doped layers are normally formed using PECVD processes as opposed to thermal diffusion processes, which means that the thermal budget during fabrication for these cells is considerably reduced. Figure 2.21 shows the cross section of a traditional SHJ cell with front contacts.

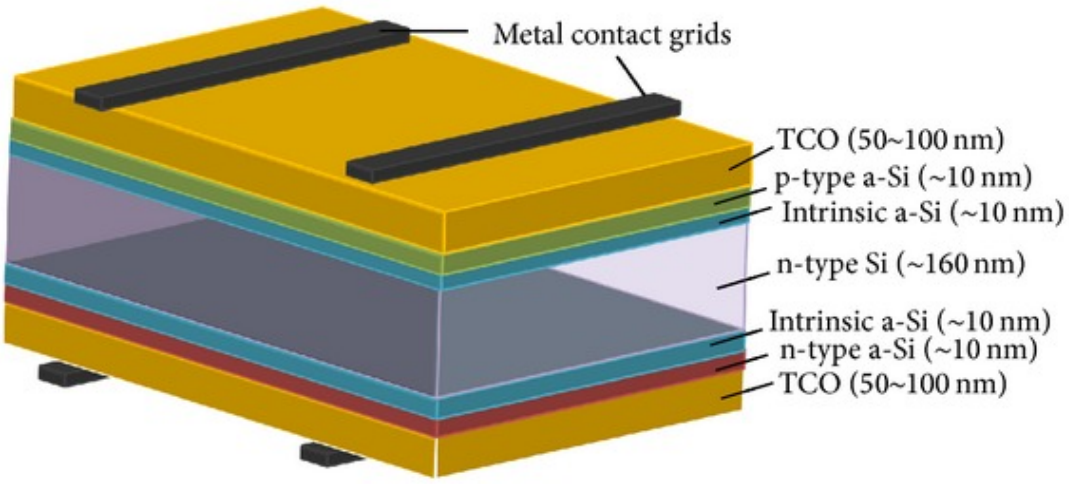


***Figure 2.21** - Diagram of traditional SHJ cell* [58]

Ensuring of the correct thickness of the amorphous silicon layer provides the greatest challenge in fabricating SHJ cells. As the total thickness of a SHJ solar cell decreases, the V_{oc} increases due to the ratio of the photocurrent density over the saturation current density enlarging. However, should the thickness decrease too much then the fill factor (FF) starts to fall due to an increase in SRH recombination leading to an overall less efficient device [52]. Thus, achieving the correct thickness is critical to creating a high performance SHJ solar cell.

2.5.3 Back Contact Silicon Solar Cells

Front and rear contact cells have one of the polarities collected from the front side of the cell, and the other from the rear side, as shown in Figure 2.16. Having metal fingers on the front side of the cell results in a significant area of the cell being shading by the metal fingers of the front contacts, thus preventing the sunlight from hitting the silicon directly. A device geometry that allows more of the front surface to be able to absorb sunlight will make more of the front surface 'useful' and therefore increase the efficiency of the device.

In section 2.5.2.3 with the buried contact cells showed an attempt to increase the available useful front surface area, however because there are still fingers on the front surface with this geometry, the total useful area is limited. Back contact cells completely remove the fingers from the front surface, placing both positive and negative metal contacts on the rear side of the cell. This maximizes the useful area on the front surface as the whole surface can be used to convert sunlight into electricity, completely removing shading from metal contact fingers. Current back contact solar cells that are already in production, whilst having high efficiencies (such as the 25.6% efficient heterojunction interdigitated back contact (IBC) cell developed by

Panasonic[53]), are still expensive so do not commercially compete with cheaper front contact solar cells unless available space is at a premium. These higher costs are predominantly due to the increased number of complex processing steps required. Another contributing factor is that as all of the current collection is done at the rear of the device, a high minority carrier lifetime bulk is necessary meaning that the substrate material used needs to be of a higher quality.

2.5.3.1 Metal Wrap Through (MWT) Cells

Metal wrap through (MWT) solar cells could be thought of as a hybrid between front contact and rear contact solar cells. Metal fingers remain on the front surface of the solar cell, as is the case with front and rear contact solar cells. However, the busbars that both connect to the current collecting grid and give a point of contact for the tabbing needed in module assembly are moved to the rear of the cell. In order to join the busbars to the fingers, metallised laser vias connect through the substrate to the front surface grid leading the current to the rear where it can be collected. The benefits of this cell geometry are an increase in useful area on the front surface as a result of placing the busbars at the rear, and also simplified module assembly with a better packing factor for cells when connected to form a module. This is because front and rear contact solar cells need the front grid to be connected to the back grid of the next cell, and the tabbing to do this requires space between the cells. Rear only tabbing is also much more uniform than front to back tabbing which would make automation of this process easier as well as reducing the space needed between cells. Figure 2.22 shows a schematic view of an MWT cell.

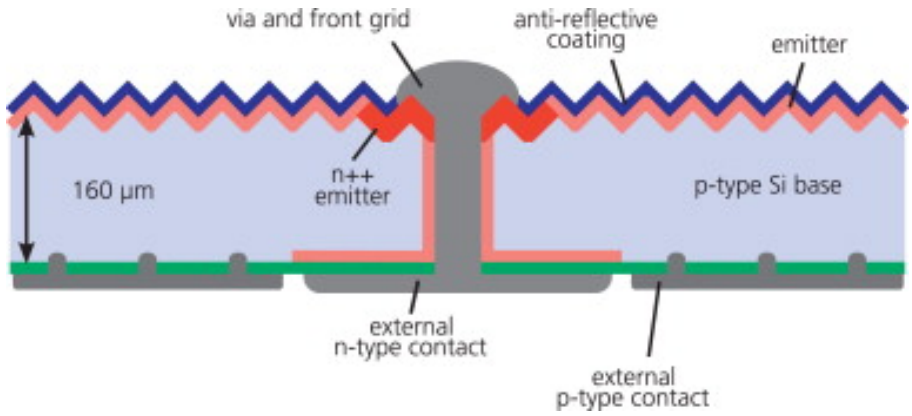


Figure 2.22 - *The metal wrap through (MWT) solar cell* [54]

Figure 2.23 shows a photograph of the front surface of an MWT solar cell. Here it is shown that the front metal collection grid is no longer limited to being in straight lines and can radiate out from the vias which are shown as silver dots in the photograph allowing the maximum spacing between the metal contact lines to be maintained and minimising the distance that carriers generated have to travel before reaching a metal contact.

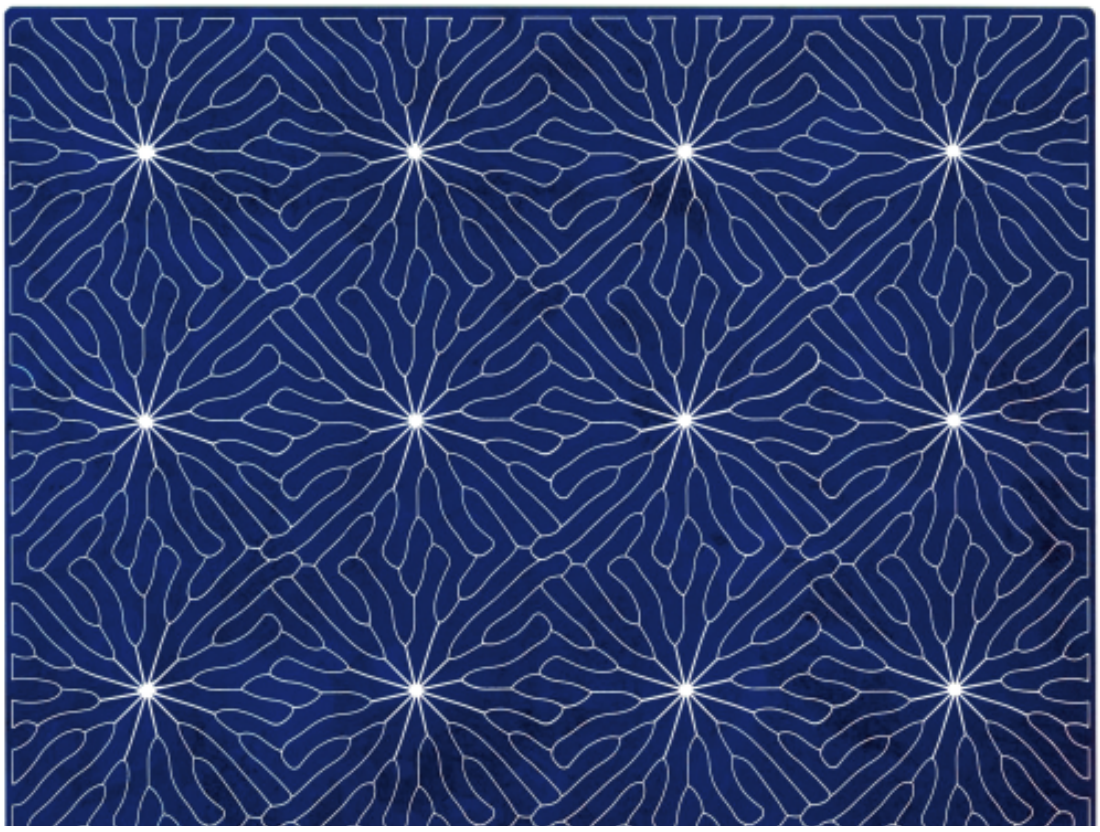


Figure 2.23 - *Photograph of the front surface of an MWT solar cell* [55]

2.5.3.2 Emitter Wrap Through (EWT) Cells

The emitter wrap through geometry is an approach to solar cell design, similar to the MWT cell but taking it a step further with both the n-type and p-type current collection grids being placed on the rear surface of the solar cell. This immediately has the benefit over front contact solar cells, as there are no metal fingers on the front surface, only dots from the vias, which increases useful front surface area and therefore potentially the cell efficiency. Figure 2.24 shows the schematic of the emitter wrapped through design as proposed by Gee et al [56]. The idea of the design is to have metalized laser drilled vias on the rear collection grid connected through the substrate to the front surface emitter.

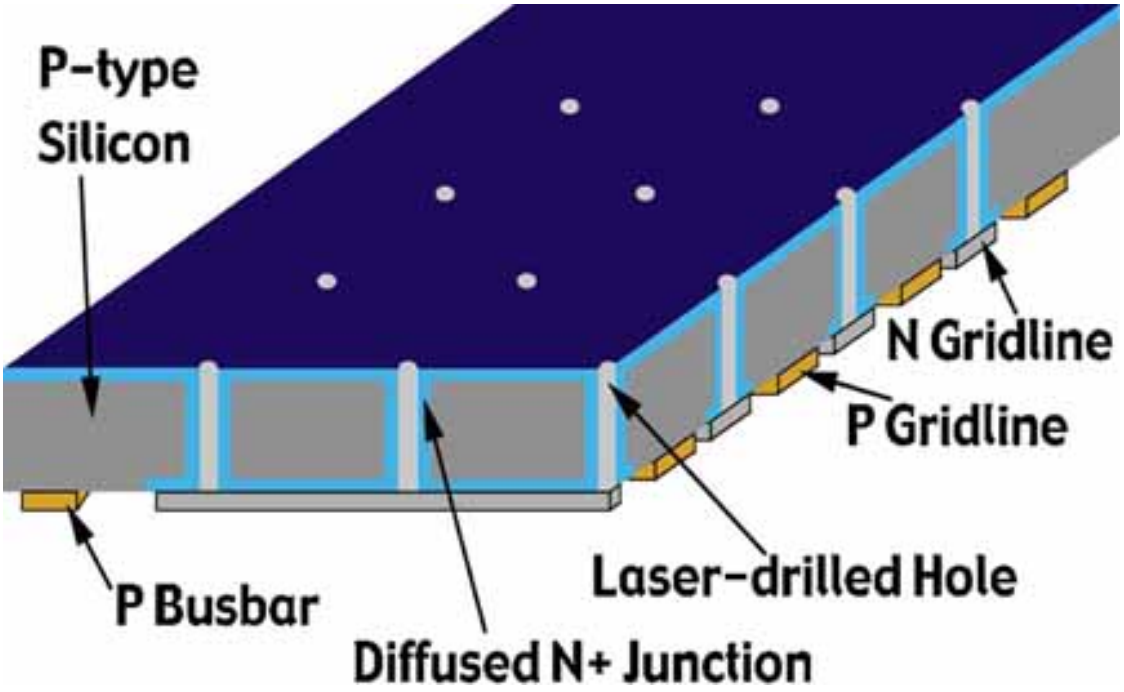


Figure 2.24 - *The emitter wrap through (EWT) solar cell* [73]

Taking the idea from the buried contact cell of cutting the contact grooves and using low resistivity metals to fill them, the EWT cell applies them to the rear of the cell. To improve efficiency and allow the use of cheaper, lower diffusion length materials, whilst creating the laser cut n-type grid on the rear surface, holes (vias) to the front of the cell are also drilled using the laser. These vias are also metallized at the same time as the rear collection grids and allow the current collection grid on the rear surface to connect, through the substrate, to the collection junction on the front surface. Results obtained from 2-dimensional modelling of this type of cell geometry have indicated efficiencies of 28% are possible with reported results of a J_{SC} of 40 mA/cm^2 and a V_{OC} of 543 mV using a 4 cm^2 test device [57].

2.5.3.3 Interdigitated Back Contact (IBC) Cells

Interdigitated back contact (IBC) cells are superficially similar in composition to EWT cells, in that all the contacts are on the back surface; however, unlike any device considered so far IBC cells have the emitter on the rear instead of the front of the device.

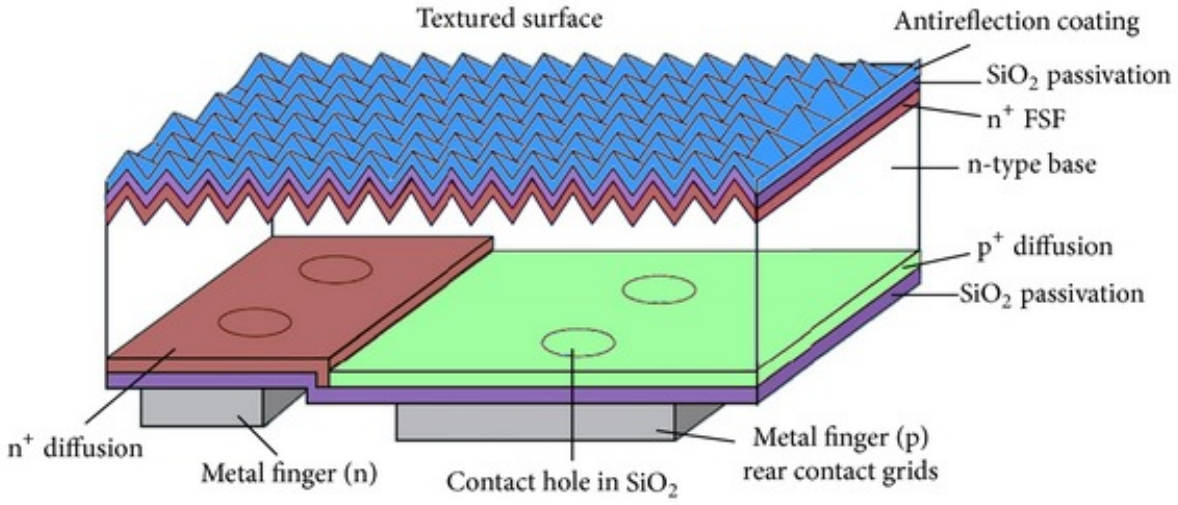


Figure 2.25 - *Schematic sketch of an IBC solar cell* [58]

As is shown in Figure 2.25, although the charge carriers are generated at the front surface, they are collected at the rear meaning that they have to travel through the entire thickness of the bulk material. There are also no vias to lead the carriers to the collector. This means that substrates with a higher minority carrier lifetime must be used. This higher quality silicon is more expensive than the lower grade silicon typically used in solar cell fabrication and increases the cost per watt of this type of device geometry. Figure 2.25 also shows that the contact areas are kept as small as possible. This reduces recombination at the metal/semiconductor interface, which allows IBC cells to produce higher short circuit current densities (J_{SC}). Michael Lammert and Richard Schwartz brought the first IBC cells to recognition in 1977 for concentrated solar applications[59]. With time, cell efficiencies have been going up, with commercially available IBC cells giving efficiencies of 24.2% [60]. The problem with this geometry is that having both the n-type and p-type grids on the same surface give the requirement to have both n and p type regions diffused into the same surface but kept separate from each other. This can be very challenging due to the nature of thermal processing, and currently requires the use of expensive processes such as lithography in fabrication, which results in a higher price per watt for the device.

2.5.3.4 Interdigitated Back Contact Silicon Heterojunction (IBC-SHJ) Cells

The IBC cell discussed in section 2.5.3.3 identifies that the IBC geometry gives devices that possess a high J_{sc}, and the SHJ cell discussed in section 2.5.2.4 identifies that SHJ geometry gives device that possess a high V_{OC}. These characteristics are very desirable and a device that can incorporate both of these would give a solar cell with a very high efficiency. The IBC-SHJ cell was spawned out of this idea, and a schematic image of this type of cell structure is shown in Figure 2.26.

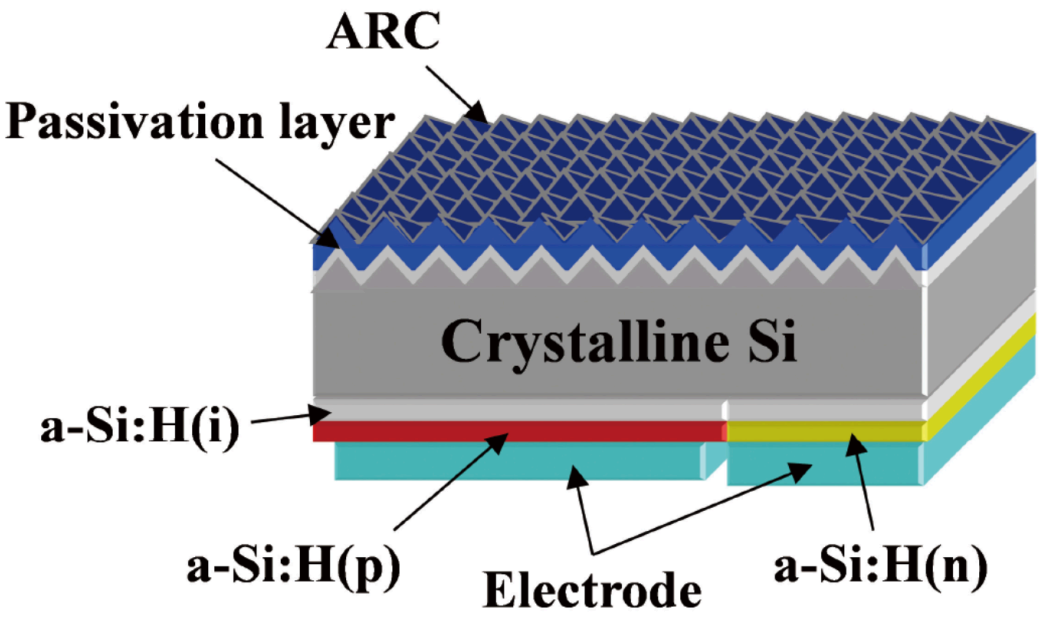


Figure 2.26 - *Schematic image of IBC-SHJ structure* [61]

Successful fabrication of this type of device has been carried out with excellent results. In 2016 Kaneka produced a device with a cell conversion efficiency of 26.33% [62], which at the time of fabrication was a world record for device efficiency.

2.5.4 Other Commercially Available Solar Cell Technologies

Most silicon solar cells need to have metal contacts that directly attach to the silicon in order for the current to be extracted from the device. Traditionally, the interface between the metal and the silicon is not passivated which leads to recombination. This recombination will eventually limit the maximum attainable efficiency of the device. Yan et al. have proposed a method whereby a self-passivating layer is placed between the metal and the silicon. This can be achieved with an ultra-thin layer of oxide (1.3-1.4 nm) and a doped layer of either polycrystalline silicon, amorphous silicon or a mixture of both [63]. Fabricating this significantly increases the amount of processing needed to create a working device, however implementation of such an approach to the rear side contacts of a n-type silicon solar cell has been achieved. The Fraunhofer Institute call this process 'TOPCon' and have managed to produce a champion device

with a 25.1% conversion efficiency [64]. In section 2.6.6 the POLO (Polycrystalline Silicon on Oxide) IBC cell is presented in the context of laser processed IBC silicon solar cells. This concept combines passivated contacts on a back-contact cell geometry.

Figure 2.27 is a graph produced by the International Technology Roadmap for Photovoltaics (ITRPV) predicting how world market share of cells will be distributed based on the cell technology. There is predicted to be quite a drop off of traditional BSF cells over the next 10 years with PERC, SHJ and back contact devices filling the gap created.

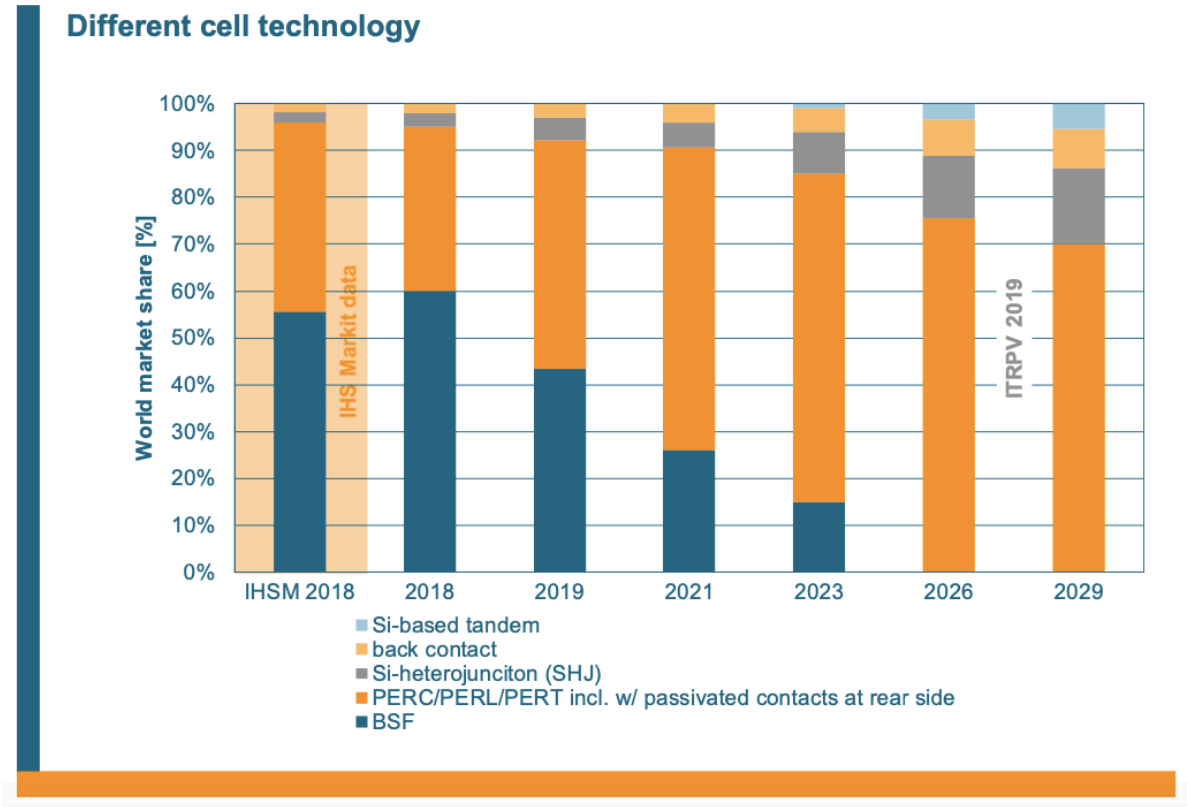


***Figure 2.27** - Predicted world market share based on cell technology [65]*

2.5.4.1 Bifacial cells

It is not only the front surface of a solar cell through which light can enter the cell; providing the rear surface has exposed areas of silicon in between the metal contacts,

then it too can allow light to be coupled in. This would allow the total energy generation of the device to increase. The first bifacial solar cell patent was issued in 1966 to Hiroshi Mori [66]. This work was then continued in the University of Madrid during the 1970s with further patents being granted [67] and the novel device geometry was proposed by Antonio Luque [68]. The concept was later revived with another patent being granted in the late 1990s to Yakov Safir [69] who proposed a concept using a semiconductor wafer as the substrate. Figure 2.28 shows the n-Pasha bifacial solar cell [70], a device that was developed in the Netherlands and has the potential to give efficiencies in excess of 20%. Although the bifacial cell design can give high performance, the main obstacle to them becoming the industry standard is that they depend upon several variables that have little effect on monofacial systems and are thus less well studied.

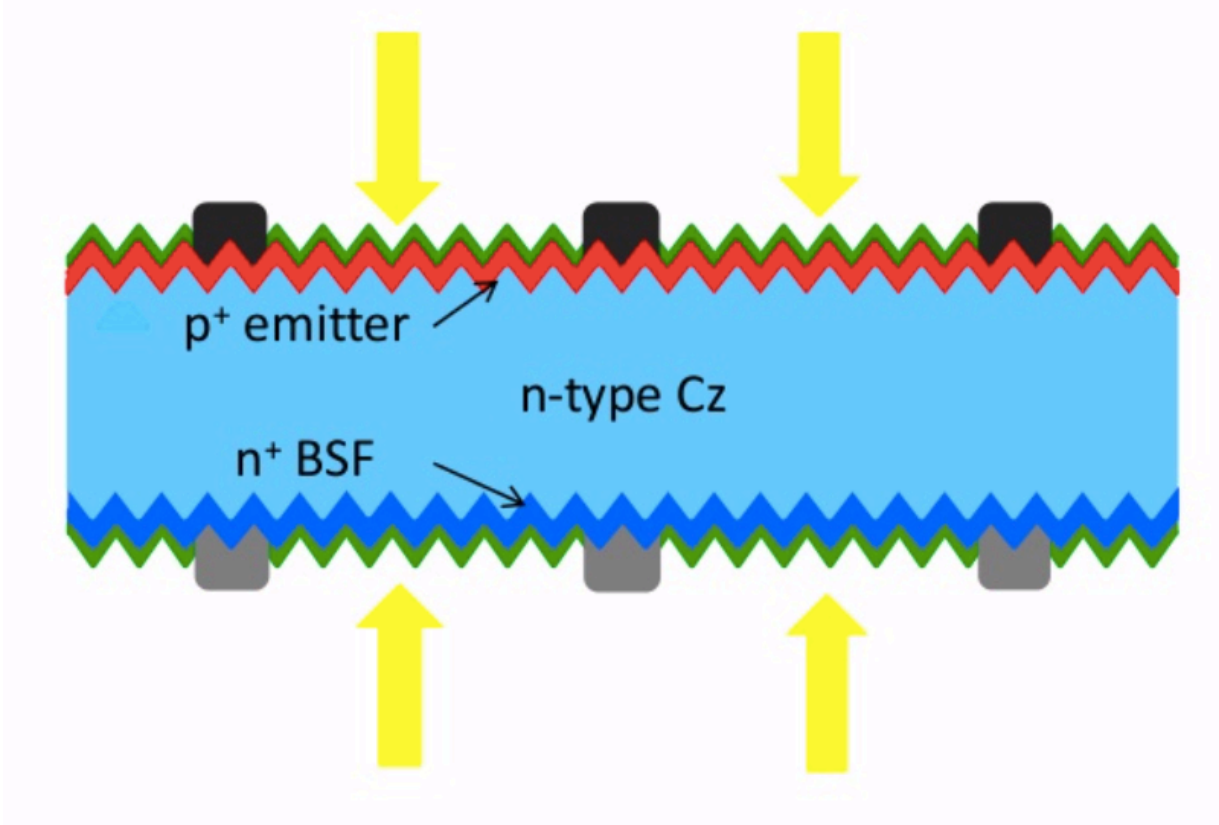


Figure 2.28 - *n-Pasha bifacial solar cell [70]*

Amongst these parameters that need to be considered for bifacial modules are the mounting height and tilt of the module so as to allow maximum light absorption by both front and rear sides of the module. The albedo (measure of ground reflectance) and any shading that may be caused by the mounting structure and junction boxes underneath the modules also affect the overall performance of the installation.

Figure 2.29 - *Photograph of a bifacial solar cell module*

In terms of module assembly, bifacial modules require the rear surface of the module to be transparent (as shown in Figure 2.29) in addition to the front surface. The tabbing of the solar cells needs to cover the minimum amount of the rear surface of the cell so as to allow as much light to strike the rear surface as possible. There are also slightly increased maintenance costs associated with bifacial module installations owing to both sides of the module requiring cleaning and the increased effect on energy production that a change in vegetation may have [71] [72]. As the benefits of bifaciality are growing, the amount of research into these previously unimportant variables and conditions has increased leading to the International Technology Roadmap for Photovoltaics (ITRPV) predicting that bifacial solar cell market share will increase from 13% in 2019 to 60% in 2029 [65] as shown in Figure 2.30.

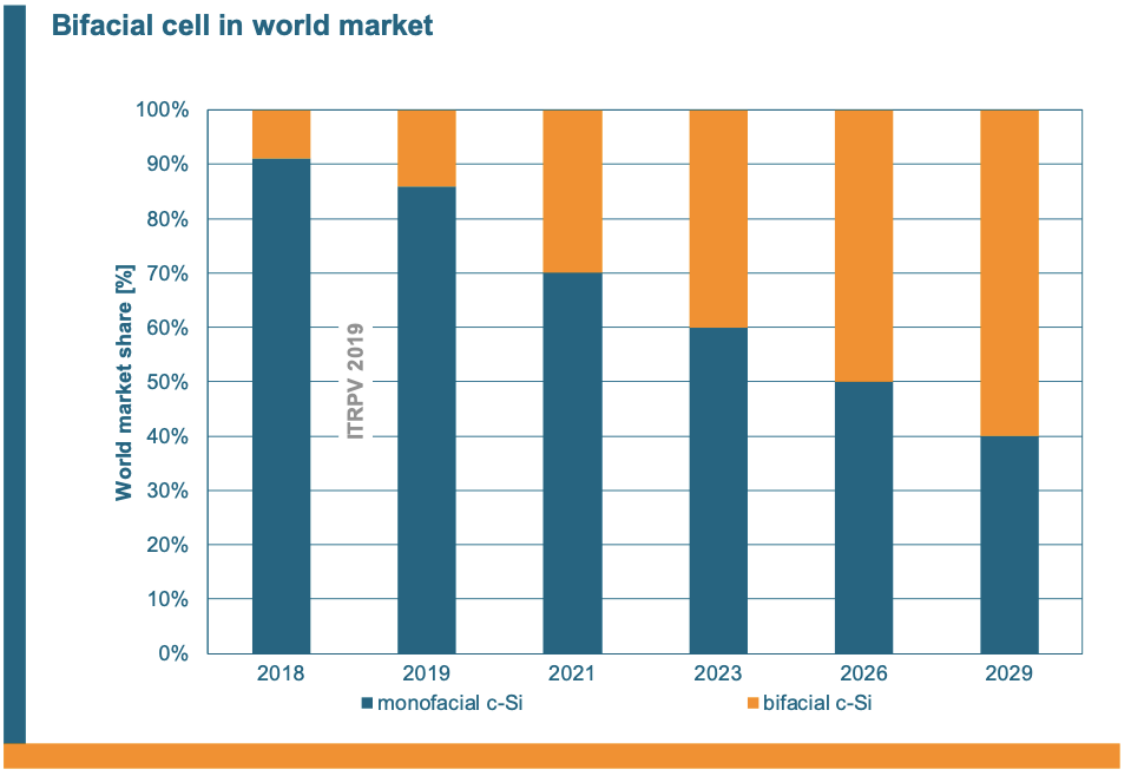


Figure 2.30 - *Predicted worldwide market share for bifacial cell technology* [65]

2.5.4.2 Thin Film Solar Cells

Thin film solar cells have been around since the 1980's and while they only have a market share of 5% today, between 1986-90 amorphous silicon thin films accounted for 30% of the PV market. Depositing one or more thin films of photovoltaic materials onto a substrate is how thin film cells are produced. The main advantage of thin film technologies is that they can be cheaper to fabricate than crystalline technologies due to the lower material cost of a 1µm thickness film as opposed to a 200µm thick high purity silicon wafer. Crystalline silicon technologies often use thermal diffusion for doping which is a considerably more expensive process. Up to now as shown in Figure 2.15, the conversion efficiencies have not been as good as for crystalline silicon wafer-based cells and they degrade at a faster rate than crystalline silicon technologies [73]. However, thin film cells are currently in production, and a few of the thin film technologies are described below.

2.5.4.2.1 Amorphous Silicon Cells

Amorphous silicon (aSi) is the non-crystalline form of silicon, the use of which in solar cells was first reported in 1976 by Carlson and Wronski [74]. The new technology sparked interest because of the promise of being able to produce an economically viable source of renewable energy. Photovoltaic cells are made by depositing thin layers of amorphous silicon onto a substrate such as glass or metal. These layers are doped p-type and n-type either side of an intrinsic layer so that a P-I-N junction is created. Figure 2.31 shows a cross section of an amorphous silicon solar cell.

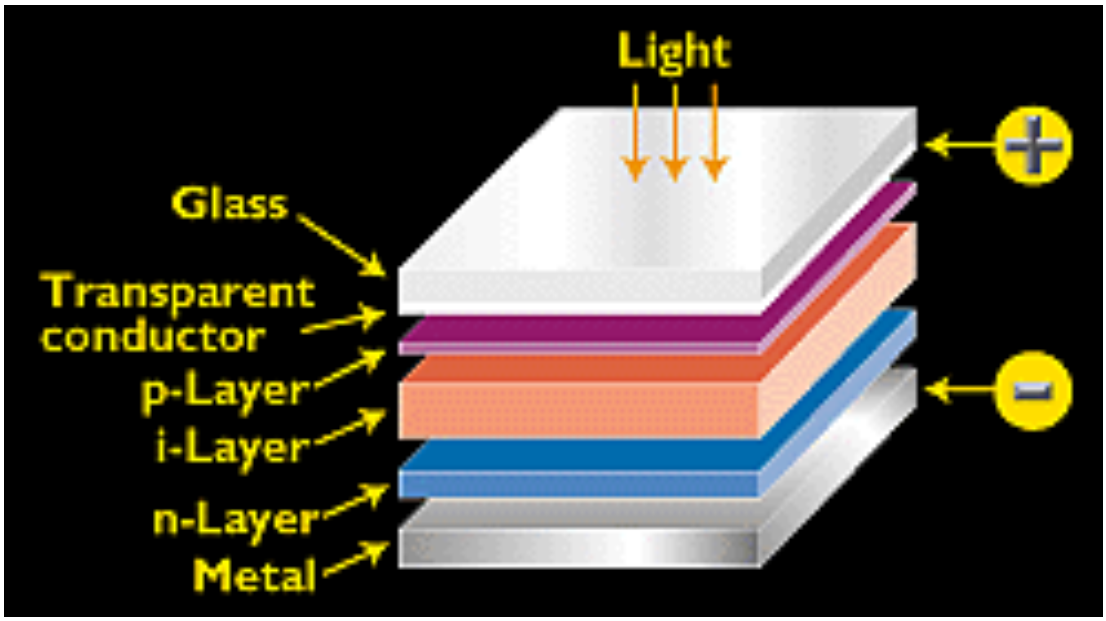


***Figure 2.31** - Diagram of an amorphous silicon cell* [75]

Amorphous silicon solar cells have the benefits of many thin film solar cells being lightweight, flexible (subject to the substrate used) and are relatively low cost to produce as well as being environmentally friendly due to the lack of toxic heavy metals being used in to produce them. As can be seen in Figure 2.15, the efficiency of stabilised amorphous silicon cell technologies is much lower than other technologies, with record efficiencies only reaching 13.6% [76]. However, because of they are lightweight and have low production cost, they are still used in low power portable

applications where cost is the prime factor mostly consumer electronic devices such as solar powered wrist watches and pocket calculators.

2.5.4.2.2 Cadmium Telluride (CdTe) Cells

CdTe technology is the most prominent of the thin film technologies currently in production. Global production of CdTe cells was 2.3 GWp in 2017, making up more than half of the thin film market [77]. CdTe devices are heterojunction thin film solar cells, the junction is made at the interface between two different crystalline semiconductors each with a different band gap. Research into CdTe as a semiconductor dates back to the 1950s [78] after its band gap (1.4 eV) was discovered to be the optimum band gap for the terrestrial solar spectrum. The current day leader in research and production of CdTe technologies is First Solar, based in Arizona, who have produced a CdTe cell with a record efficiency of 21.5% [79]. CdTe cells are made using thin layers of cadmium sulphide (CdS) and cadmium telluride (CdTe) which are deposited onto a glass substrate. The CdS layer forms the n-type region of the p/n junction, and the CdTe layer forms the p-type region. The structure of a CdTe solar cell can be seen in Figure 2.32.

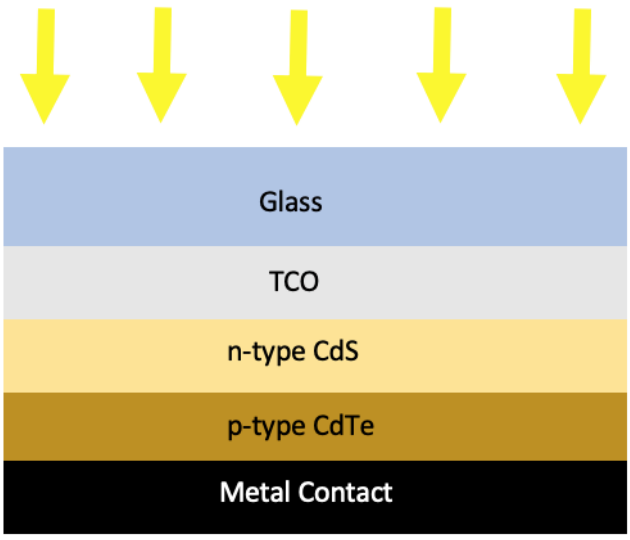


Figure 2.32 - *Schematic of a cadmium telluride solar cell (not to scale)*

Electrical contacts are made to the device through a metal contact at the back and the front contact is made with a transparent conducting oxide (TCO) such as tin oxide. Like amorphous silicon cells, these layers can be deposited using processes that are much cheaper than those required for crystalline devices. Current thin film deposition processes include sputtering, close spaced vapour transport (CSVT), spray pyrolysis and electrodeposition [80] The drawbacks of CdTe devices are that telluride is a rare element and cadmium is one of the most toxic materials known. This means that the disposal and long-term safety of CdTe panels detract from the benefits of the technology.

2.5.4.2.3 Copper Indium Gallium Selenide (CIGS) Cells

CIGS cells are made by co-evaporation of copper, indium, gallium and selenium onto a substrate (usually glass) to make a photovoltaic device. As with CdTe cells, CIGS cells are heterojunction devices cells with the p/n junction being made from p-type Cu (In, Ga) Se_2 layer and a thin n-type cadmium sulphide (CdS) layer. The layers in a CIGS device are thin enough for the whole device to be flexible allowing them to be deposited on flexible substrates as shown in Figure 2.33. Again, these devices can be made using low cost deposition processes, and devices with efficiencies of 21.7% [81] have been fabricated. CIGS cells share many of the benefits of CdTe cells, however the CIGS cell has a much lower level of cadmium in it, only in the form of the thin n-type cadmium sulphide layer. The cross-sectional structure of a typical CIGS cell is shown in Figure 2.34.

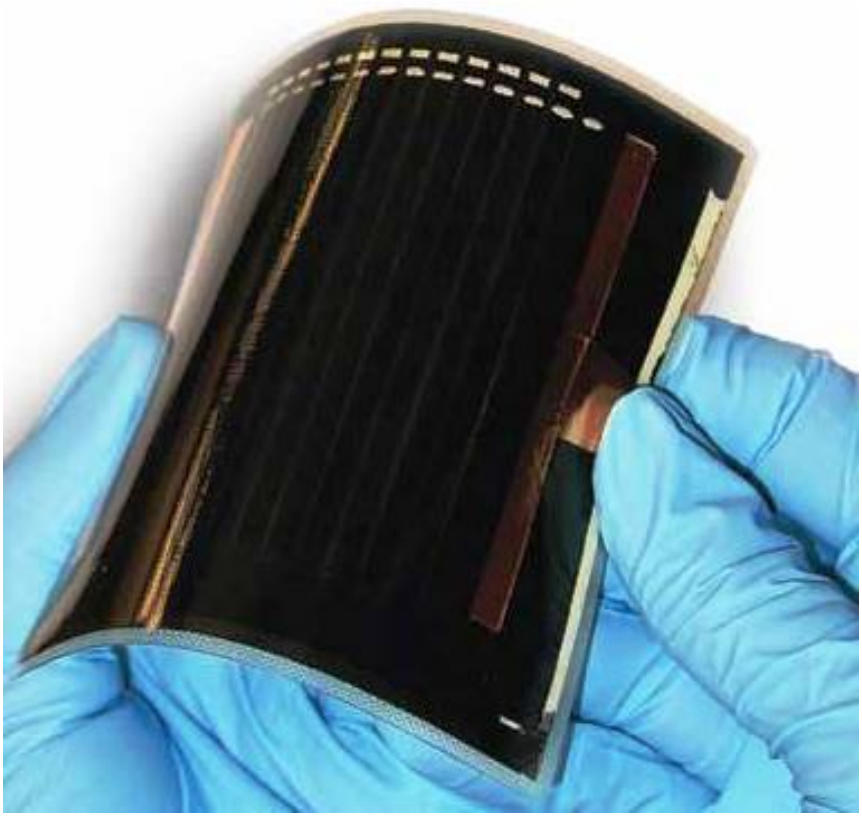


Figure 2.33 - *Photograph showing flexibility of a CIGS cell* [82]

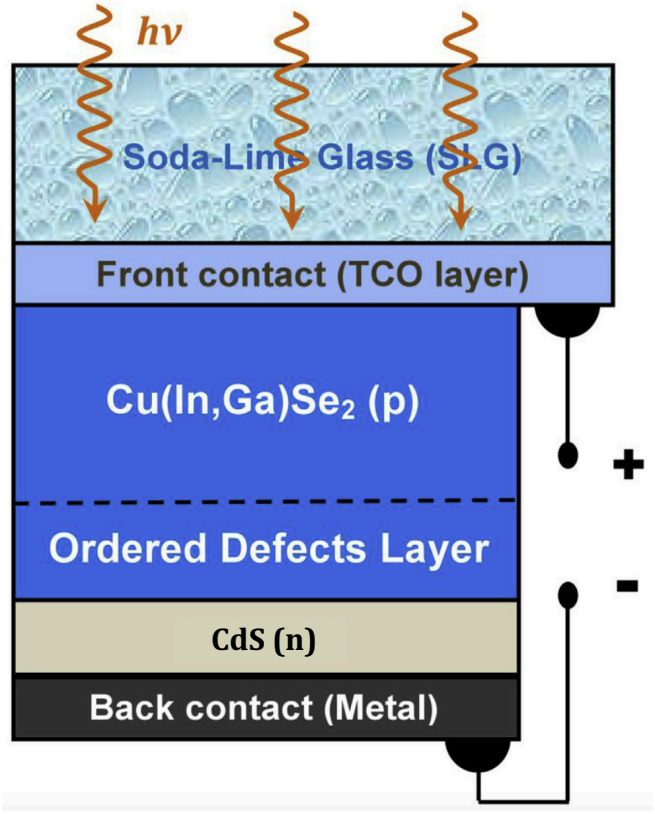


Figure 2.34 - *Structure of a typical CIGS cell* [83]

2.5.4.3 Multi Junction Cells

So far in this chapter, all the device technologies that have been looked at comprise of only a single p/n junction. Multi junction devices typically consist of 2-4 junctions made using different semiconductor materials. These different materials have different band gaps meaning that the device can respond to multiple wavelengths of light allowing more of the available solar spectrum to be captured and converted to electricity. Figure 2.35 shows how the different layers absorb different regions of the solar spectrum. The device shown in this diagram has three junctions stacked on top of each other with the same current flowing through each junction and their voltages adding together. The top junction is indium gallium phosphide, the middle junction is gallium arsenide and the bottom junction is germanium.

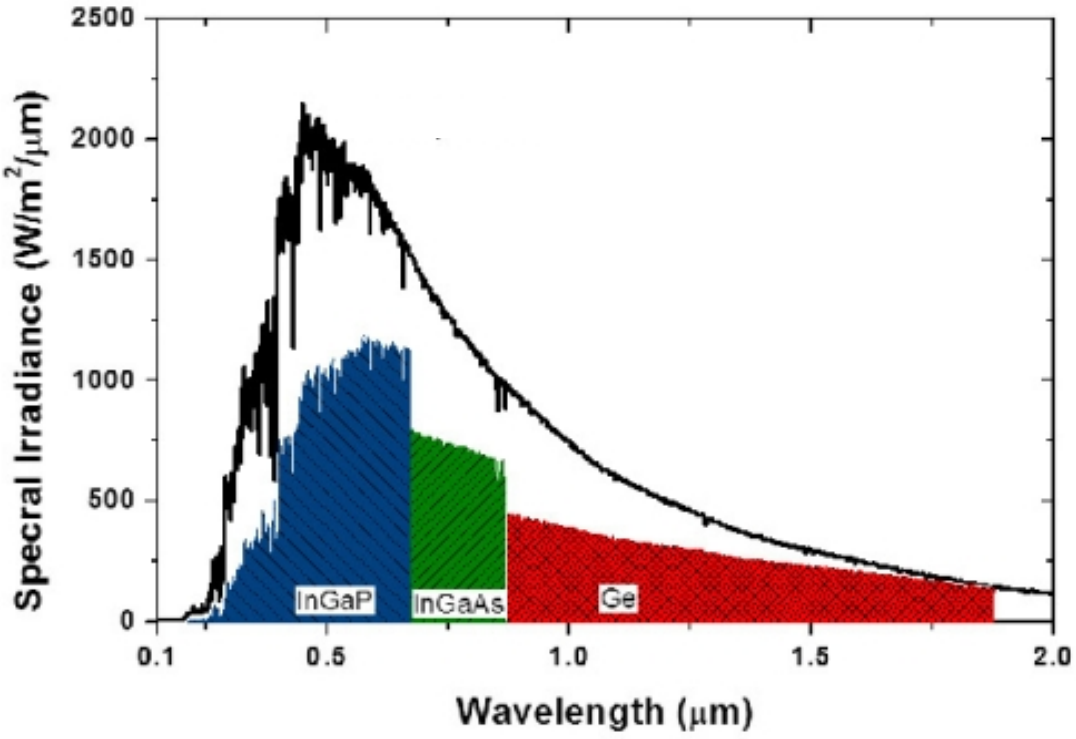


Figure 2.35 - *Graph of spectral irradiance vs. wavelength showing maximum conversion efficiency for each junction of a triple junction device* [84]

By having these additional junctions, and therefore the ability to convert more of the available energy in the solar spectrum to electricity, devices have been made with the highest efficiencies reported for solar cells at 38.8%[85] in normal light and 46%[86] in concentrated sunlight. Figure 2.36 shows the cross section of a triple junction cell.

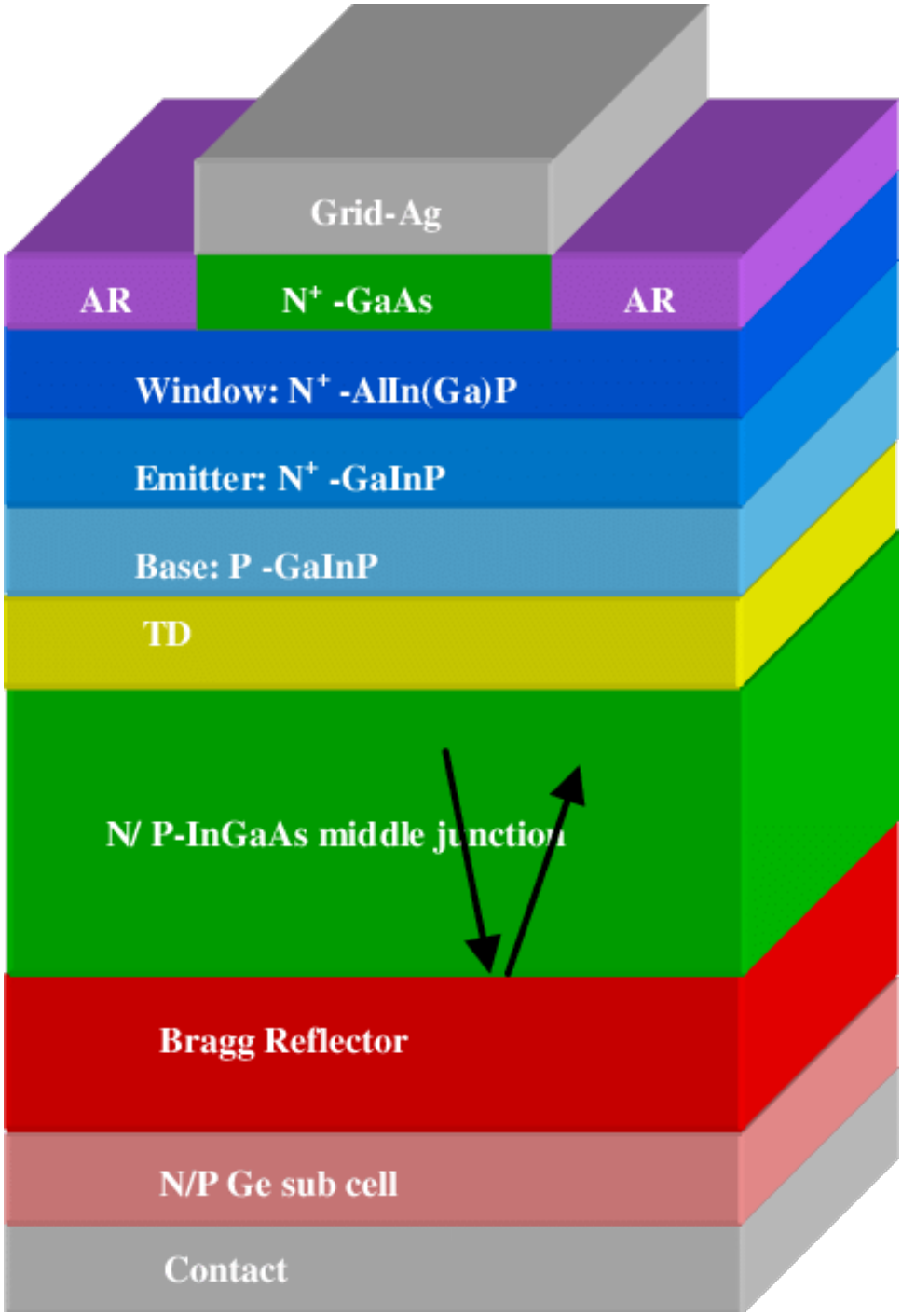


Figure 2.36 - *Diagram of a triple junction solar cell* [87]

Although these multi junction devices are capable of very high efficiencies, they are very expensive to manufacture, and economically unviable for most practical applications. The most common application for these high cost highly efficient devices is in space to power satellites and space stations where the power to weight ratio is valued more than the power to cost ratio. As a result, the energy yield from every kilogram of material needs to be as great as possible. On earth, multi junction cells can be used in conjunction with optical concentrators so that the cost of cell, which is the expensive part, is minimised by using smaller devices and optics to focus the light onto the active area. These setups however require dual axis tracking to follow the sun, which in turn is an additional capital cost and incurs additional ongoing maintenance costs. Figure 2.37 is a photograph showing the optics required to focus and concentrate sunlight onto a small area multi junction photovoltaic device.

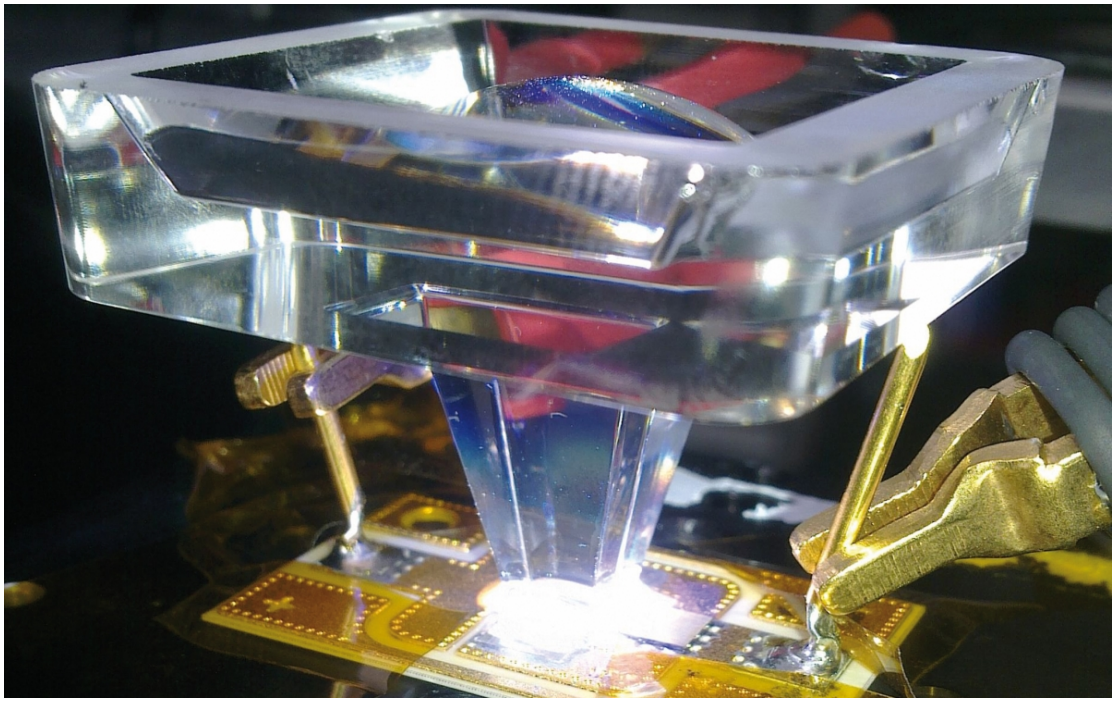


Figure 2.37 - *Solar concentrator for multi junction cells* [88]

2.5.5 Emerging Solar Cell Technologies

As the effort and investment to find more efficient renewable energy sources progresses, research is being done into novel approaches to solar cell design. A few of these are explored within this section of the literature review.

2.5.5.1 Dye-Sensitized Cells

Dye-sensitized solar cells (DSSC) were proposed in the late 1980s [89]. The principle of dye-sensitized cells is that a dye can be used to absorb light in order to create electricity. Sunlight passes through a transparent electrode into the dye layer where it can excite electrons, which flow through a layer of titanium dioxide (TiO_2). These devices can be very cheap to manufacture as they can be made using roll printing techniques although the conducting indium tin oxide (ITO) glass (as used in all the thin film devices) remains relatively expensive. Other disadvantages of the DSSC design include the use of a liquid electrolyte that has temperature stability problems. At low temperatures, this electrolyte can freeze ending power production and potentially leading to physical damage. The biggest problem with DSSC devices however is the lifetime of the cell. On average a DSSC cell has a lifetime of 5 years maximum [90]. Figure 2.38 shows an example of a DSSC device.

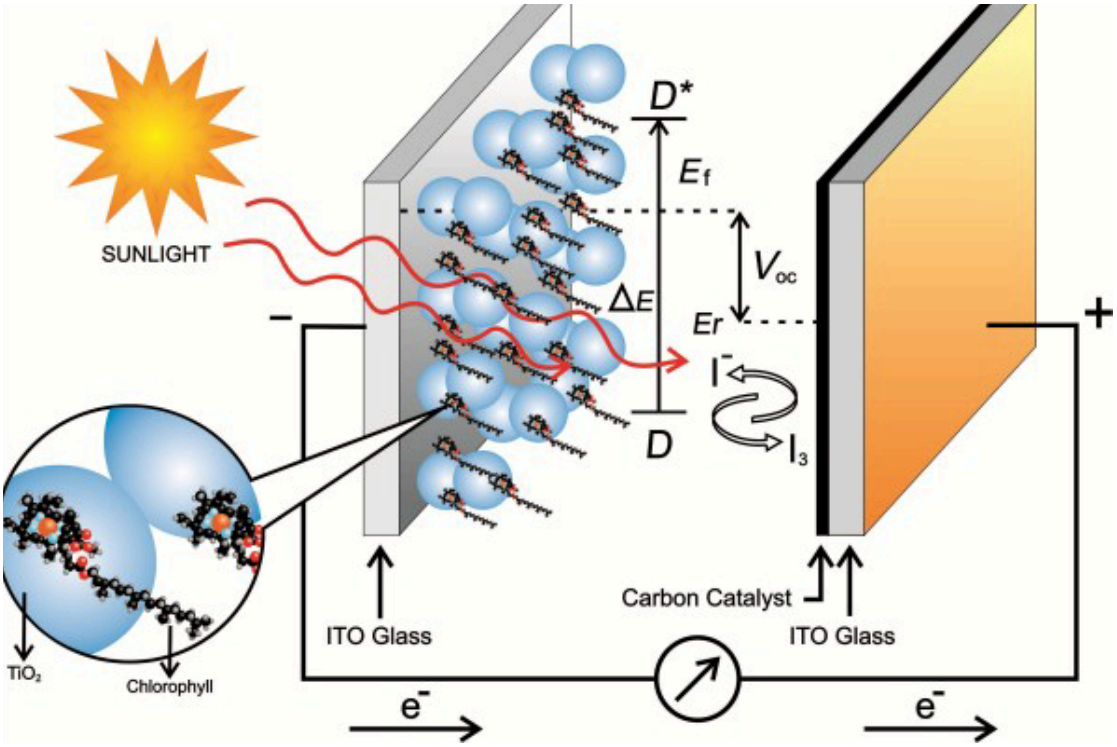


Figure 2.38 - *Example of a DSSC* [91]

2.5.5.2 Organic Photovoltaic Cells

Organic photovoltaic cells (OPV) are made using polymers and are often known as plastic solar cells. A typical OPV device consists of one or several photoactive materials sandwiched between two electrodes. Figure 2.39 shows the structure of a bilayer OPV device. In a bilayer OPV cell, sunlight is absorbed in the photoactive layers composed of donor and acceptor semiconducting organic materials to generate photocurrents. The donor material (D) donates electrons and mainly transports holes, while the acceptor material (A) withdraws electrons and mainly transports electrons. When the photoactive materials absorb light, a photon knocks out an electron in a polymer atom leaving a hole. The electron and hole form a bonded pair known as an 'exciton'. Due to the concentration gradient, the exciton diffuses to the donor/acceptor interface and splits allowing the electron to move independently to a hole formed by another absorbed photon. This continuous movement of electrons from hole to hole

produces an electric current. The primary advantage of OPV technology over inorganic counterparts is its ability to be utilized in large area and flexible solar modules, facilitating roll-to-roll (R2R) production. Additionally, manufacturing cost can be reduced for organic solar cells due to their lower cost compared to silicon-based materials and the ease of device manufacturing. However, in order to compete with the performance of silicon-based solar cells, both donor and acceptor materials in an OPV need to have good extinction coefficients (their ability to absorb light), high stabilities and good film morphologies.

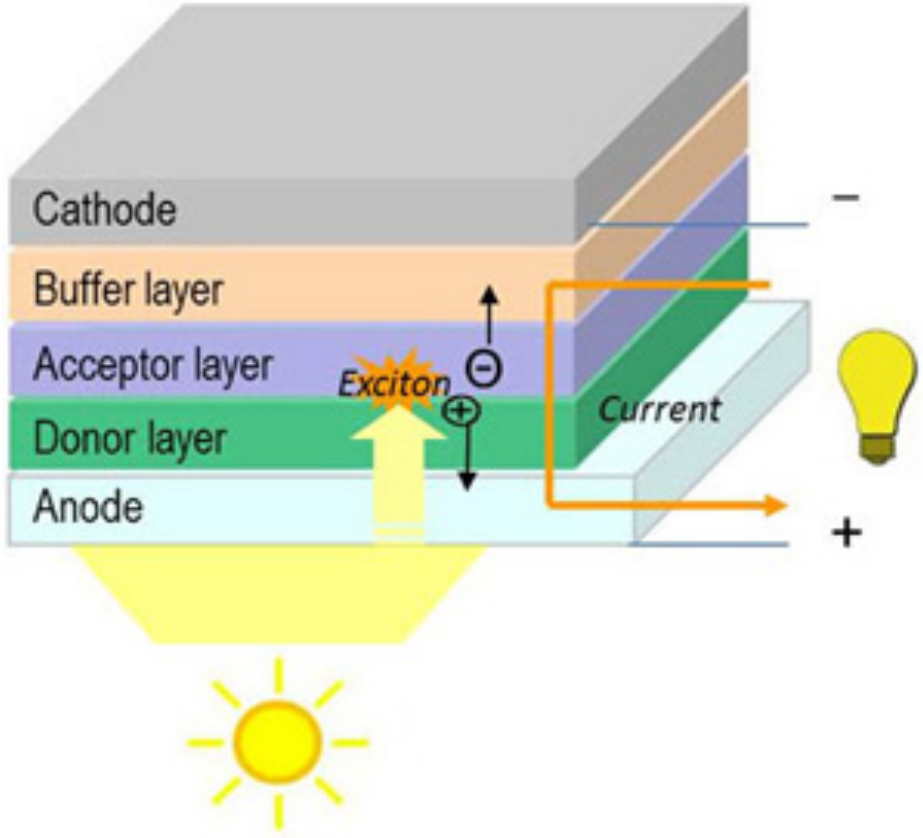


Figure 2.39 - *Structure of a bilayer organic PV device* [92]

2.5.5.3 Perovskite Solar Cells

The perovskite solar cell is a relatively modern concept in device technologies, but as seen in Figure 2.15, it is the fastest advancing solar technology in terms of efficiencies, improving from 3.8% in 2009 [93] to 20.1% in 2014 [94].

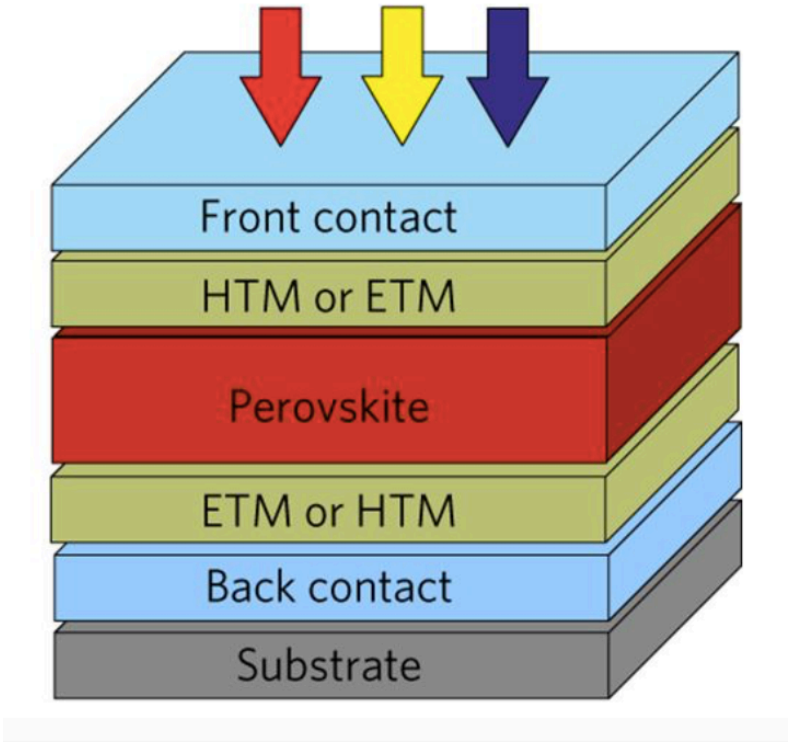


Figure 2.40 - *Structure of a perovskite solar cell* [95]

Perovskite crystals can both harvest light and transport electrical charge making them ideally suited for photovoltaics. Figure 2.40 shows the structure of a perovskite cell (where ETM is the electron transport material and HTM is the hole transport material). One of the key qualities of perovskites is that they exhibit higher conversion efficiencies with ultrathin films than conventional thin film solar cells discussed already in section 2.5.4.2 with conversion efficiencies in excess of 15% achieved using absorbing perovskite layers as thin as only 330nm [96]. However, perovskite materials degrade in the presence of moisture and ultraviolet light, so whilst devices with good efficiencies have been fabricated, long term stability issues have held back their commercial roll-out. Research is currently being done into using

the good light harvesting properties of the perovskite crystals as part of a hybrid cell combined with crystalline silicon cell technologies[97]. In December 2018 Oxford PV produced a new perovskite-silicon tandem solar cell, which achieved a perovskite solar cell world record conversion efficiency of 28%.[98]

2.5.5.4 Quantum Dot Cells

Quantum dot (QD) solar cells started to be fabricated in the early 2010's. The concept is to replace the bulk material such as silicon with tiny semiconductor particles, 'quantum dots', which have the advantage over traditional PV semiconductors as their band gaps can be varied or 'tuned' simply by changing the size of the dot.

Hypothetically, this would give the benefits of a multi-junction cell in that much more of the solar spectrum becomes accessible but, as it is actually a homojunction device, the high costs associated with multi-junction cell fabrication can be avoided.

In 2014, the University of Toronto produced a quantum dot cell with an efficiency of 10.6%, which at the time was a record [99]. This was subsequently improved in January 2019 when a quantum dot solar cell was produced at the University of Queensland with an efficiency of 16.6% [100].

Quantum dot devices can be coupled with other technologies such as dye-sensitized cells to form hybrid cells giving the benefits of both types of technology.

As shown in Figure 2.15 however, none of quantum dot, dye-sensitized or OPV technologies have come near to matching the conversion efficiencies achieved by perovskites despite the fact that these technologies have been around for a longer period of time than perovskites.

2.6 Laser Processing in IBC Photovoltaic Devices

So far, this literature review has given an overview of different PV device technologies that exist in various stages of development. However, silicon wafer technology is still the dominant player in commercial photovoltaics accounting for over 95% of the market [101]. The objective of this project is to create an efficient solar cell at a low fabrication cost. Laser processing is a low-cost fabrication process that can be easily incorporated into existing wafer production lines. There has already been some research into various ways that laser processing can be used in the fabrication of solar cells and this section of the literature review will examine the research and work done in this area in more detail.

2.6.1 Laser-Doped Back-Contact Cell

During laser processing, at the point that the laser beam interacts with the silicon, a large amount of heat is produced. This heat can be used in the doping process as it will cause the dopant to be driven into the substrate only at the localised area upon which the laser beam interacts. A study by Dahlinger et al. at the University of Stuttgart into laser-doped back-contact solar cells [102] looked further into this idea. Figure 2.41 shows their device, part (a) is the process flow, (b) the device design with a large contact pitch and (c) the device design with a small contact pitch. This process completely removes the need for costly photolithography processes to provide masking. The laser doping process enables a localised n^{++} BSF and p^{++} emitter to be formed with no masking. From their modelling on FZ wafers, an efficiency of 22.0% was realized [103], however due to their substantial costs no commercial solar cells are made from FZ silicon wafers.

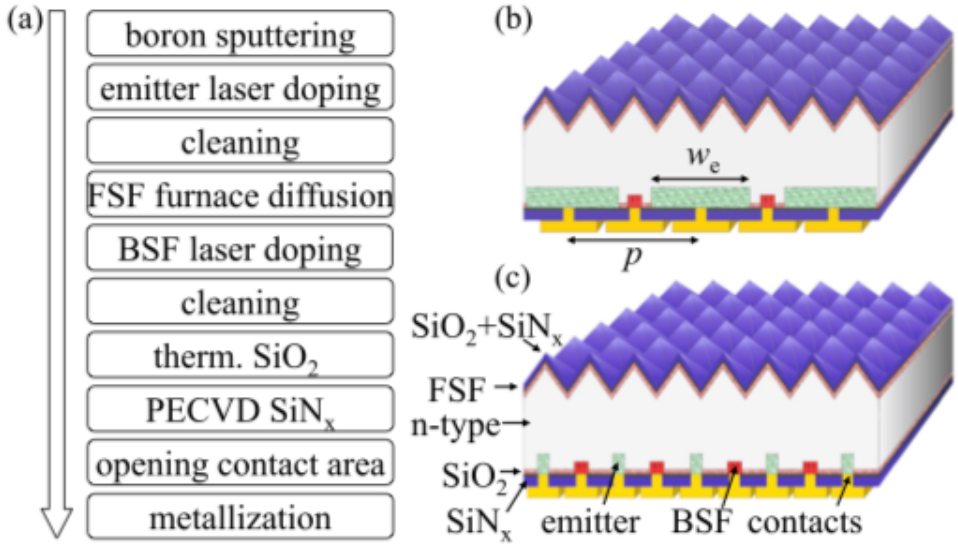


Figure 2.41 - *Laser-doped back contact cell* [102]

2.6.2 Laser Fired Contacts in Solar Cells

As has already been established, IBC cells can produce very high energy conversion efficiencies however they are hindered due to the complex processing required to have both the emitter and the BSF on the same side of the wafer. Sighu et al from Hareon Solar Technology investigated a method using a single step laser process to both dope and create point contacts at the same time [104]. Figure 2.42 shows a schematic of the geometry used in their research.

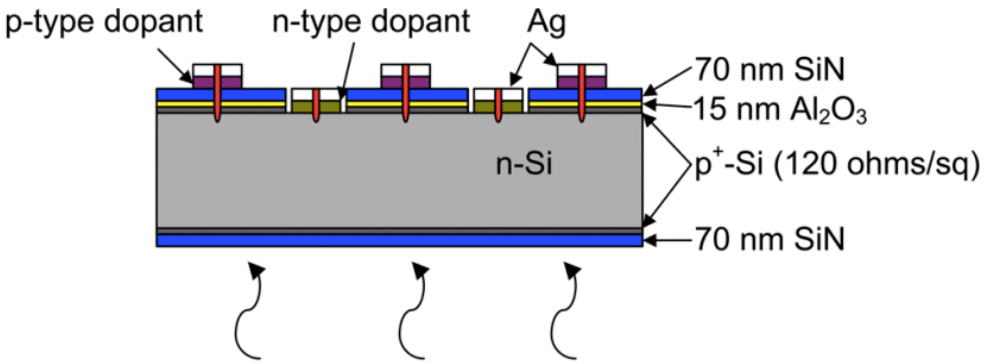


Figure 2.42 - *Schematic of laser fired contact IBC solar cell* [104]

In this process, both p-type and n-type dopant dots are screen printed on top of an Al_2O_3 passivation layer. An interdigitated silver grid is then screen printed on top of

that before a laser is used to form the contacts. The heat of the laser causes the screen-printed dopants and contacts to diffuse through the dielectric layers and into the silicon. Because there is no large area heating, the process has a very low thermal budget. In this study on n-type CZ wafers, IBC solar cells with energy conversion efficiencies above 18% were produced. The team concluded that with further optimisation of the device structure and laser processes, energy conversion efficiencies greater than 22% should be achievable [104].

2.6.3 Laser Ablation for Selective Patterning

The biggest challenge when fabricating an IBC cell is that, unlike conventional solar cells, both the emitter and the BSF contacts are on the same side of the device. This means that in order to successfully fabricate a device, these regions will need to be masked at various points in the fabrication process to allow selective patterning for dopants. The traditional method of achieving this is to use photolithography, a wet chemical-based process that is both costly and not suited to industrial scale photovoltaic manufacturing.

By comparison, laser processing is relatively cheap and can be automated, making it very easy to fit into established production lines. One idea to build on this is to use a dielectric film (such as a silicon nitride) which is deposited across the surface of the substrate. A dielectric film would act as a mask protecting the silicon beneath it from being doped. The deposition of these films is more economical and much more suited to industrial processing than other masking processes such as photolithography. Silicon nitride has the advantage over silicon oxide in that it is more resistant to any subsequent HF etching steps that might be required later in the fabrication process. A laser is then used to ablate (open) the dielectric at selected areas, thereby imitating a traditional photolithographic mask as shown in Figure 2.43.

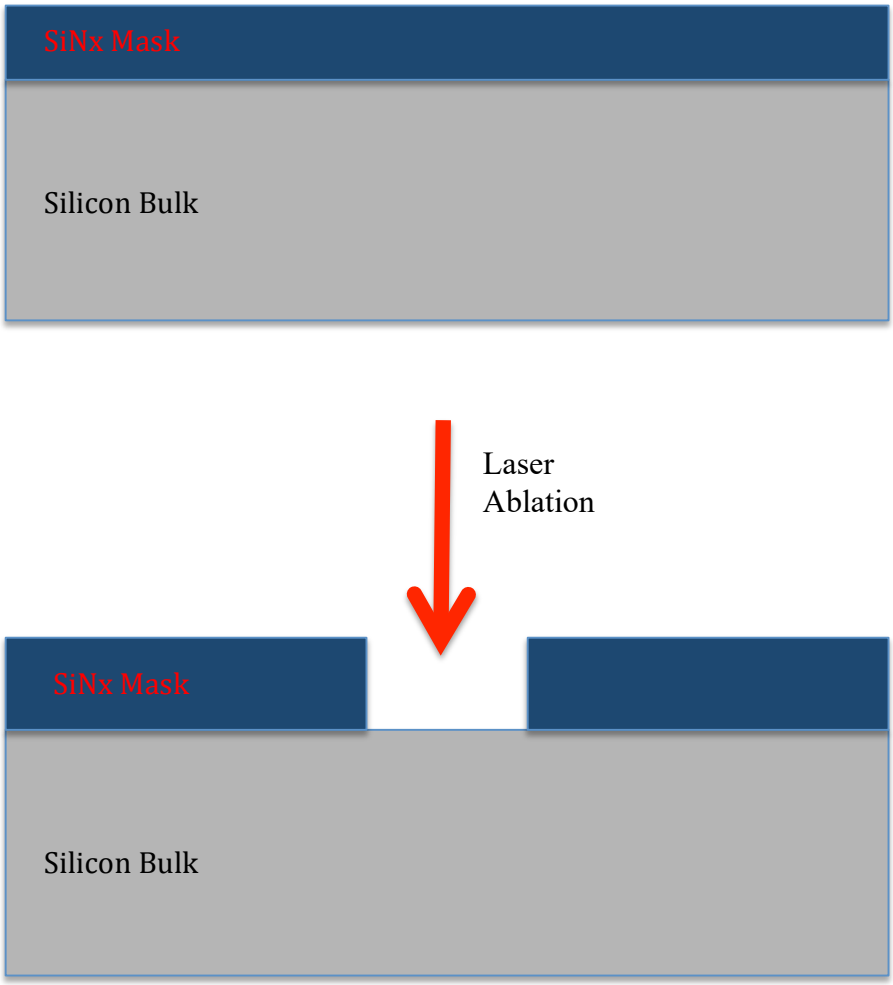


***Figure 2.43** - Processing diagram of laser masking*

In 2015, a team at the Australian National University published their research into laser ablation with an ultraviolet (248 nm) laser to remove the Si_3N_4/SiO_2 dielectric stack [105]. They compared identical devices; one fabricated using traditional photolithography and the other using a laser to cut openings in the dielectric. They found that using the laser did not significantly increase the recombination activity, and both of their devices gave open circuit voltages of 696 mV and verified small-area device efficiencies of 23.5%.

2.6.4 SLASH Concept IBC Solar Cell

Using laser ablation for emitter patterning allowed a heterojunction IBC cell to be developed that its inventors believed had a fabrication process compatible for mass production. This is called the SLASH (Structuring by Laser Ablation of Silicon Heterojunction) concept [106]. The benefit of this device was its simplified processing steps which were made possible by using lasers to pattern the emitter and back surface field. This provides a method of having both the emitter and BSF on the same side of the device without the need to lithography processing to keep them apart during processing. The experimental results for this cell geometry gave a conversion of efficiency of 19% based on a 5×5 cm^2 device, which was reportedly limited by poor current collection. Future work proposed for this geometry to improve passivation and rear side optimization is predicted to lead to power conversation efficiencies of 22%.

2.6.5 Laser Ablated IBC-SHJ Cell

SHJ cells were discussed earlier in section 2.5.2.4 of this literature review where it was seen that this approach to cell fabrication currently produces high conversion efficiencies of up to 24.7% [48]. Laser ablation for rear side patterning would bring down the fabrication costs of the SHJ cell geometry as laser processing is a fast and cheap technique. The challenge to overcome though is the adverse effect that laser irradiation has on amorphous silicon in that it causes significant degradation. Harrison et al. have been trying to circumvent this by using a sacrificial layer to protect the c-Si/a-Si:H interface layer as shown in Figure 2.44 [107]. In this diagram, the sacrificial layer is the thin SiO_2 layer that is designed to protect the amorphous silicon and the silicon interface from damage by the laser. This sacrificial layer will also allow the eventual removal of residues after laser opening. The p-type amorphous layer in

Figure 2.44 acts as both the absorption layer which is the layer that is removed by the laser (having been designed to absorb the maximum incidental laser power) as well as being the etch resistant layer which acts as a barrier for further chemical steps required to locally etch the amorphous silicon.

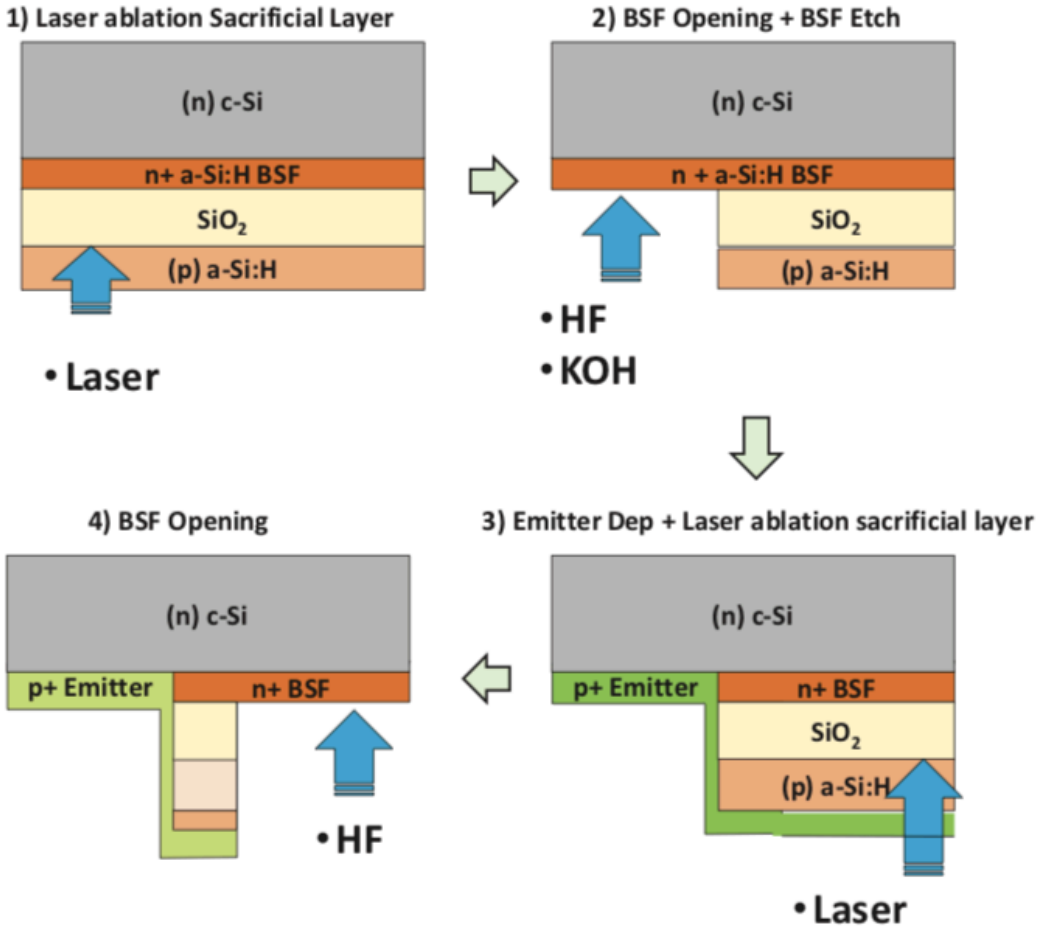


Figure 2.44 - *Laser ablated HIT-IBC cell process flow* [107]

The best cell conversion efficiency achieved so far by this team is 20.55% on an area of 18.11 cm^2. Their research leads them to conclude that laser patterning as a technique in solar cell fabrication is a process that is of high importance to explore. Furthermore, they state that worldwide to date the final process paths for laser patterning in solar cell fabrication have yet to be finalised and the process is still yet to mature.

2.6.6 POLO IBC Solar Cells

Another approach to using lasers in solar cell fabrication is in the Polycrystalline Silicon on Oxide (POLO) IBC cell developed by Haase et al in Germany [108]. Their approach is to use a laser to both open contact holes in an oxide layer to reach the polysilicon layer and then again later in the process to isolate the metal contacts following a blanket metallization of the device. Figure 2.45 details the process flow diagram that was followed for the fabrication of their device on a float-zone (FZ) p-type wafer. The successfully fabricated devices have a power conversion efficiency of 26.1%, which is a world record for p-type crystalline silicon solar cells.

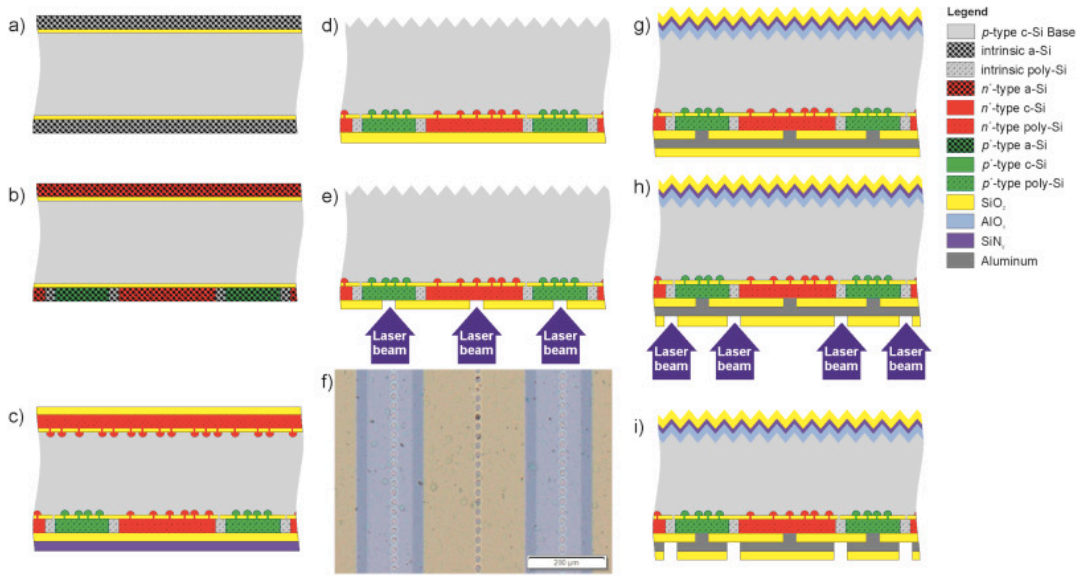


***Figure 2.45** - Process flow for POLO IBC cells [108]*

2.6.7 Interdigitated Buried Back Contact Cells

In the early 2000s, Gao et al. at the University of New South Wales Australia reported on taking the BP Saturn solar cell and using the principles of the laser grooved buried contact technology to create an interdigitated buried back contact (IBBC) solar cell [109]. Figure 2.46 shows a schematic of the suggested design geometry.

Gao's proposed method is to use an n-type doped float zone substrate, and then use a laser to cut grooves into the rear surface to create the p-type and n-type contacts. Both n and p type laser cut grooves can be considered shallow and are of uniform depth. The reported results show that devices with a V_{oc} of more than 680mV were measured, however when compared to the existing conventional buried contact groove technology, the extra cost of the silicon due to having higher bulk lifetime meant that the benefits were outweighed. The reported achieved conversion efficiency from this group with this geometry was 19.2% [110].

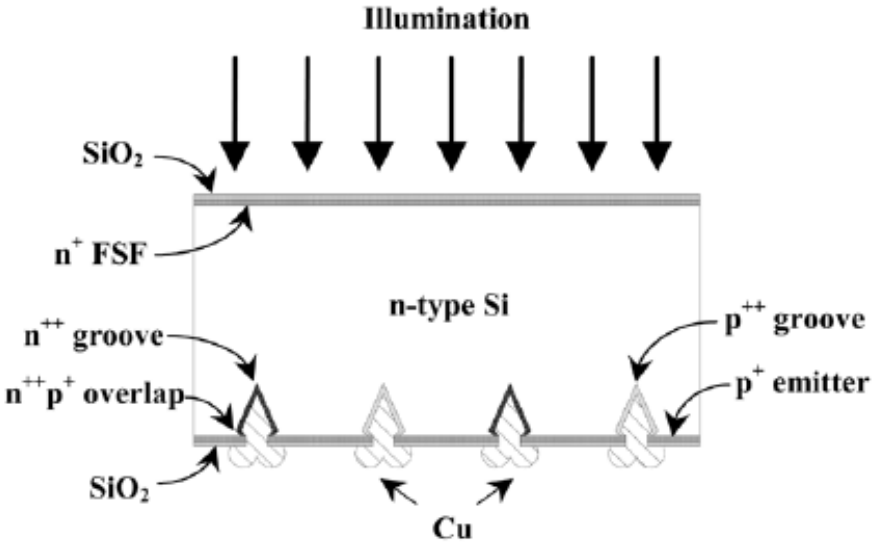


Figure 2.46 - *Schematic diagram of an IBBC solar cell* [103]

For the project that this thesis investigates, the device has been designed to overcome the limitations Gao et al. found of requiring high mobility lifetime silicon. This can be achieved by making the grooves on the rear much deeper than reported by Gao et al., therefore bringing the collection region (emitter) closer to the generation region. This will allow the use of conventional solar grade Czochralski (CZ) wafers as opposed to relying on the more expensive float zone (FZ) wafers. Gao et al. also used n-type wafers in their investigations, however the goal of this project is to be able to put the resultant technology into mass production with the minimum of modification to

existing wafer fabrication lines. Most wafer fabrication lines are set up to use p-type wafers so for this project, the substrate used will be p-type. There is also a large amount of metal deposited in typical laser cut buried contact designs. This project will investigate the effects of limiting the metal-silicon contact areas in the grooves which could potentially have the combined benefits of reducing cost and improving performance through the reduction in surface recombinations.

2.7 Summary

As has been shown, there are many different routes to improving efficiency in solar cells. Crystalline silicon dominates the solar cell marketplace and is the most commonly manufactured type of solar cell. For this project, the aim is to create a cell that is not only efficient, but low cost in terms of fabrication and capital expenditure, so the cell should be able to be fabricated on current cell production facilities with minimal additional equipment. From the reviewed front side contact cells, the PERC cell has suggested passivation of the rear surfaces to reduce surface recombinations, the PERL cell has given localised diffusion to improve ohmic contacts and the buried contact cell has shown that creating grooves filled with metal has its benefits. Current rear contact cells show benefits of increasing the amount of usable surface area by having no contacts on the front surface as shown in the IBC cell, or by having a front side emitter as shown in the EWT cell. The cell design for this project will incorporate many of these ideas mentioned whilst also attempting to overcome the problem of the distance between the front surface and rear surface for the collection of charge carriers without having any vias or fingers on the front surface that can reduce the useful area for sunlight conversion. Finally, to make it as cost effective as possible, expensive fabrication processes such as lithography should be avoided, with laser processing appearing to be a promising alternative patterning technique.

Chapter 3 Fabrication and Characterisation Methodology

3.1 Fabrication

The laser grooved IBC solar cell developed for this project employs many processing steps taken from BP Solar 'Saturn' cell. Chapter 3 will outline the methods adapted from the fabrication process flow of the Saturn cell and describe the additional fabrication and characterisation methods used in this project.

3.2 BP Saturn Cell Fabrication Processes

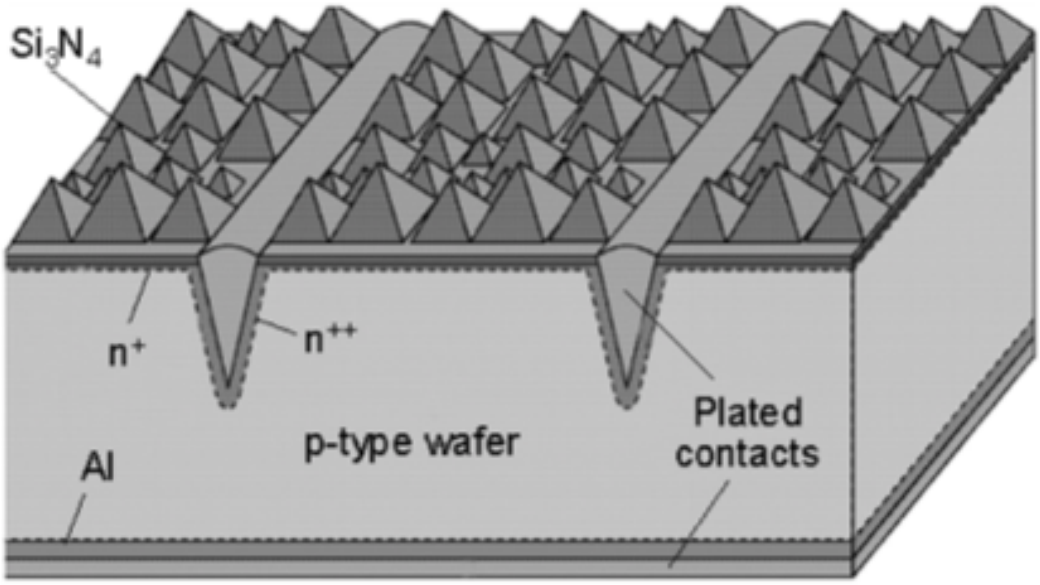


Figure 3.1 - *Cross-section of the BP Saturn solar cell* [112]

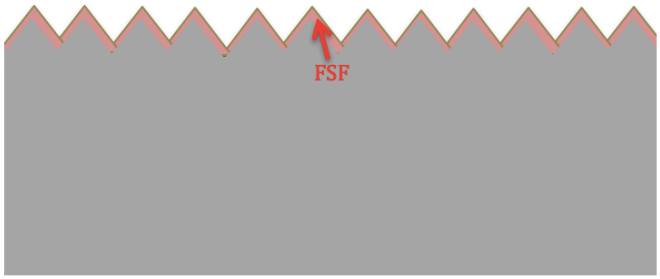
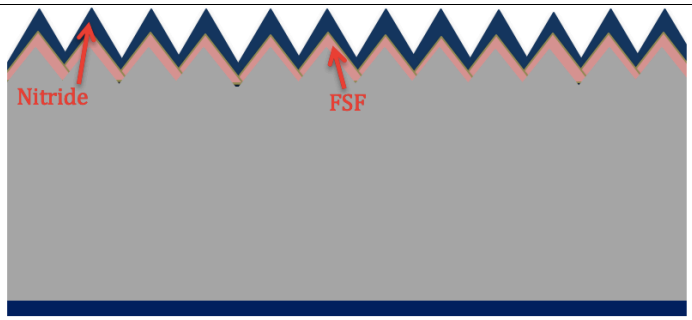
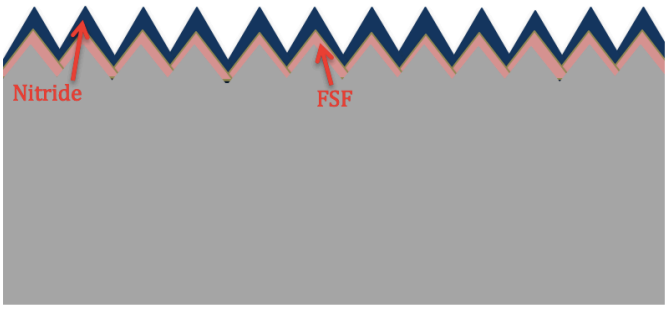
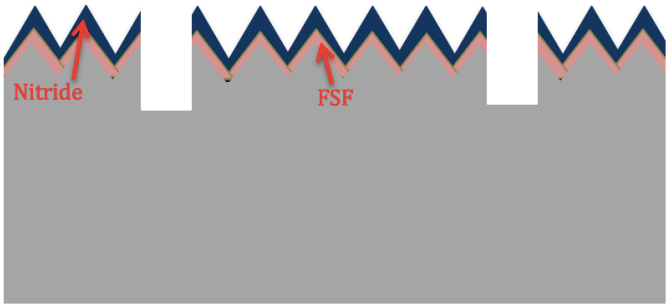
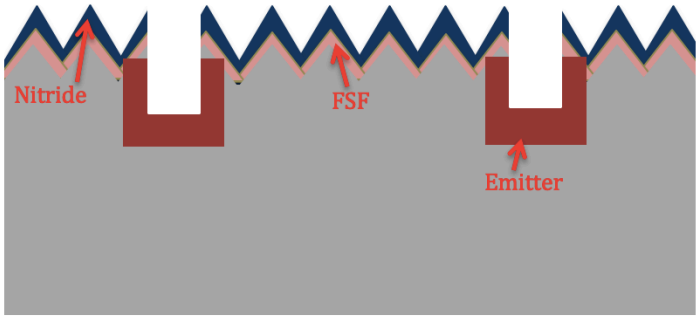
In section 2.5.2.3, the laser grooved buried contact solar cell was presented, with particular mention being made of the BP Solar Saturn cell as an example of this device geometry (Figure 3.1). The Saturn Solar cell was developed and manufactured in the early 1990s by British Petroleum (BP) [111] and became a widely used product with a 48% annual growth rate between 1994-2003 [112]. The cell was then enhanced in 2004 with an 11% performance improvement. As a result of the success of the Saturn

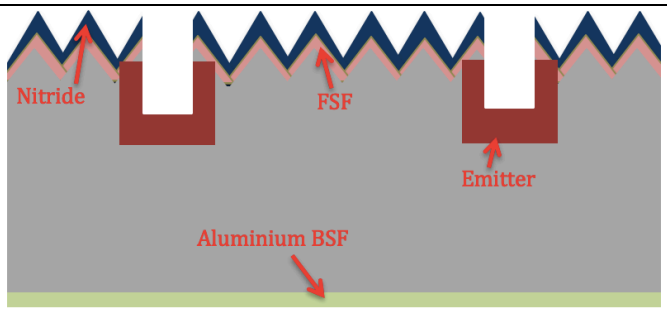
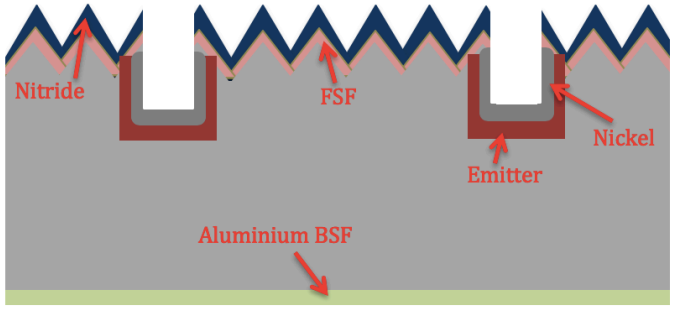
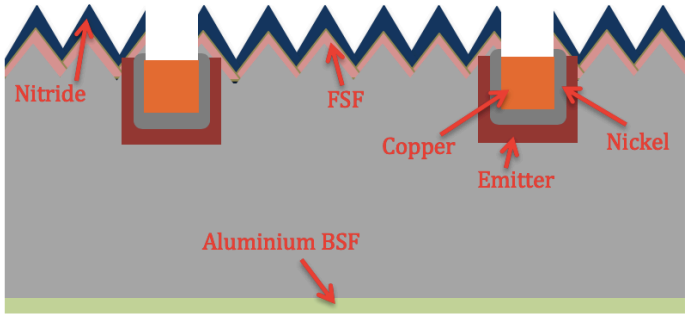
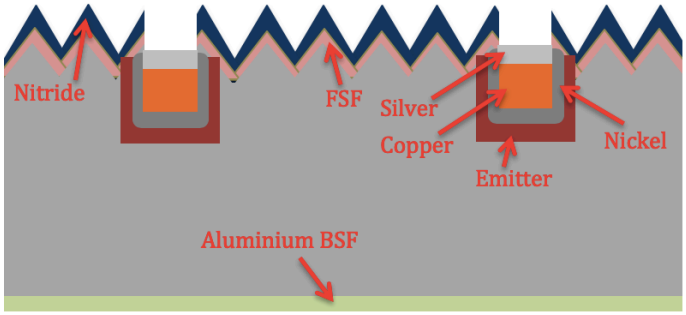
cell, many of the fabrication processes used in its production are quite well developed and commonly used in industry today. It therefore makes sense to try and utilise as many of these established processes as possible in the fabrication of devices for this project. Furthermore, following BP's withdrawal from the solar marketplace, several machines used in the manufacturing of the Saturn cell were available for use in this project. This section will detail the processing steps taken for the fabrication of the BP Saturn cell which are outlined in Table 3–1.

Table 3–1 – *BP Saturn cell process flow*

Colour	*Material*	*Colour*	*Material*
	Silicon		Aluminium
	Silicon Nitride		Nickel
	N++ phosphorous doped silicon		N+ phosphorous doped silicon
	Copper		Silver

#	**Cross Sectional Diagram of Wafer after Process Step**	**Details of Process Step**
1		Initial wafer cleaning and saw damage removal
2		Front surface wafer texturing

3		Front surface field (n+) doping with phosphorous
4		Silicon nitride anti-reflective coating
5		Rear surface plasma etch to remove oxide and nitride layers
6		Emitter groove cutting and groove damage removal
7		Emitter (n++) doping with phosphorous

8		Aluminium sputtering for BSF (P+) and rear contact
9		Electroless nickel plating
10		Electroless copper plating
11		Electroless silver plating

3.2.1 Wafer Selection

In the early 1990s when the Saturn cell was developed, multicrystalline silicon wafers were the cheapest and most widely used crystalline silicon wafers used in commercial PV production. However as discussed in section 2.4, monocrystalline silicon wafers

allow for higher efficiency devices to be fabricated than multicrystalline wafers particularly when subjected to high temperature thermal processes. The BP Saturn solar cell was designed to be a high efficiency device, and the Saturn fabrication process involves several thermal steps thus commercial grade monocrystalline CZ wafers were used [113]. Commercial monocrystalline CZ wafers suitable for PV cell fabrication are boron doped (p-type) with a resistivity of 0.5-3 Ω.cm, a crystal orientation of (100), typical minority carrier lifetimes of 5-10μs, dissolved oxygen impurities of $< 1 \times 10^{18}$ at/cm^3 and dissolved carbon impurities of $< 1 \times 10^{17}$ at/cm^3 [114].

3.2.2 Saw Damage Removal

The silicon wafers used are 200 μm thick; these wafers are sliced from a larger ingot. The process of slicing the silicon ingot leaves saw damage on the surfaces of the wafers. In order to remove this an industry standard recipe is used involving a 30% sodium hydroxide solution heated to 80°C and immersion of the wafers into the solution for 5 minutes. Equation 3.1 shows the chemical reaction that occurs between the silicon wafer and the sodium hydroxide.

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2 \quad (3.1)$$

3.2.3 Wafer Cleaning

Prior to processing, the wafers need to be cleaned of impurities and residues on the surfaces. This is to prevent the unwanted impurities being diffused into the wafer that could hinder the performance of the resultant devices, and to prevent the machines used in the processing from becoming contaminated. The cleaning procedure

developed by Werner Kern at RCA laboratories in the 1960s, known as the RCA cleaning process [115] is ideal for doing this as it does not attack the silicon surface, but selectively removes both organic and metallic contamination from the wafers. The cleaning process is a two-step process with an additional hydrofluoric acid dip to remove oxides that have formed from the surface of the silicon.

Step 1 – Organic clean – A solution of 5 parts DI water, 1-part aqueous ammonium hydroxide (NH_4OH), 1-part aqueous hydrogen peroxide (H_2O_2) creates the RCA 1 solution. This is heated to around 50°C and the wafers are immersed for 10 minutes followed by a 2 cycle DI water rinse. This step removes organic contamination from the surfaces of the wafers.

Step 2 – Ionic clean – A solution of 5 parts DI water, 1-part hydrochloric acid (HCL), 1-part aqueous hydrogen peroxide (H_2O_2) creates the RCA 2 solution. This is also heated to around 50°C with the wafers being immersed into it for a further 10 minutes followed by a 2 cycle DI water rinse. This step removes metallic (ionic) contamination, some of which was deposited in the RCA 1 cleaning stage. It also leaves a thin passivating layer on the silicon surface to prevent new contamination occurring.

During the RCA cleaning process, a thin silicon dioxide layer is formed on the surface of the wafers. To remove this oxide layer, a 30 second immersion in 1:20 (1-part hydrofluoric acid to 20 parts DI water) HF solution is performed.

Safety Notice

Hydrofluoric acid (HF) differs from other acids because it readily penetrates the skin and dissociates into fluoride ions, causing destruction of deep tissue layers, including bone. Pain associated with skin exposure to HF may not occur for 1-24 hours. Unless it is possible to rapidly neutralize the HF and bind the fluoride ions, tissue destruction

may continue for days and result in limb loss or death. Hydrofluoric acid vapours are also an inhalation hazard and can cause ocular irritation.

Ensure that non-expired calcium gluconate antidote is on hand before handling HF. Always handle HF in a properly functioning laboratory hood and in an area equipped with an eyewash and safety shower. Never work with HF alone. Full personal protective equipment should be worn when handling HF including face shield, acid resistant apron, double gloves and closed shoes. No areas of skin should be exposed.

3.2.4 Surface Texturing (KOH)

Texturing is a common method to improve the absorption of sunlight, by a solar cell. Random pyramidal texturing of crystalline silicon solar cells with alkali etchants was in PV production in the early 1980s. This is done by chemically etching pyramids onto the surface of the wafer. KOH etching is known as an anisotropic etch, which means that it etches certain crystallographic planes at a higher rate than others[116]. Thus, the (100) and (110) planes etch faster than the (111) plane. This is the fundamental principle used in pyramidal texturing. When a silicon wafer with a (100) surface is exposed to the etchant, the (100) and (110) planes etch rapidly, leaving the (111) planes exposed resulting in the random pyramid structures. The (111) oriented sidewalls have an angle to the surface wafer of 54.7° as given by equation 3.2.

$$\theta = \arctan\sqrt{2} \tag{3.2}$$

Figure 3.2 shows the difference between light hitting a wafer that has not been textured and light hitting a wafer that has had pyramids textured on the front surface. On the untextured wafer, the light has only one chance at being absorbed by the wafer, and all the subsequent reflected light is then wasted as it bounces off the

surface and cannot be used. When the surface has been textured with pyramids, because the surface is now angled, the reflected incident light can strike the wafer a second time, so more light is absorbed resulting in the amount of available light wasted by reflection from the top surface of the wafer being reduced. Furthermore, refraction of light enhances light trapping for longer wavelengths. To achieve pyramidal texturing during the Saturn cell fabrication, the front side of the wafers were etched with a heated alkali solution containing isopropyl alcohol (IPA) (which is used as a catalyst) and potassium hydroxide (KOH).

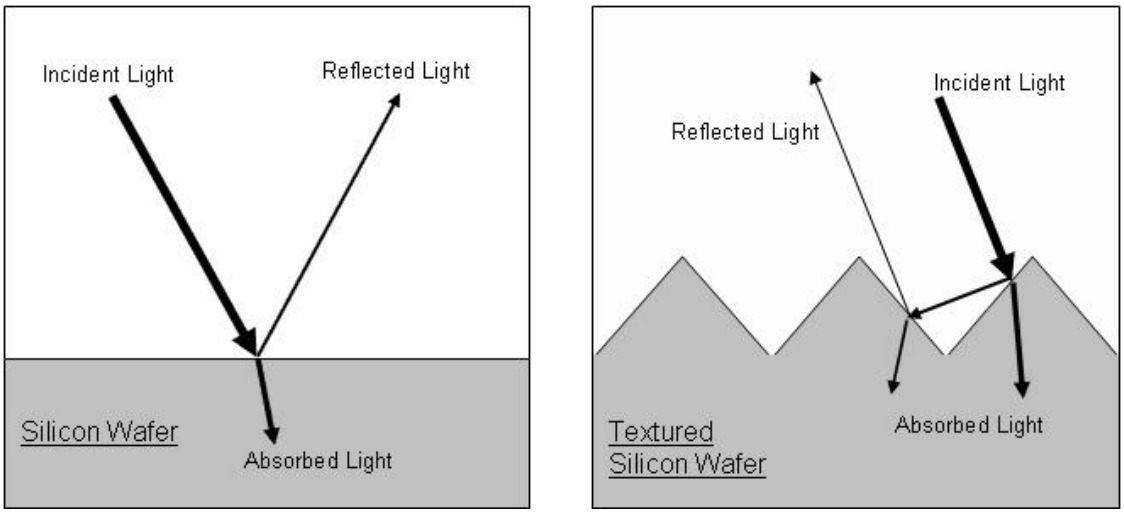


Figure 3.2 - *Sketch of light hitting untextured and textured silicon*

3.2.5 Floating Emitter

In section 2.5.2.1, the PERC cell was discussed and the advance in cell efficiency that was created by having a passivated floating emitter on the front surface of the device. The Saturn cell incorporated this design feature into its geometry. This process is similar to the one discussed later in section 3.2.10 for the n++ emitter diffusion using a $POCL_3$ diffusion furnace with the wafers inserted back to back to protect the rear side from being doped. The only difference is that whilst the n++ emitter is heavily diffused, the front side n+ floating emitter would have a much lighter diffusion.

Subsequent thermal processing steps would have had to be considered, as these would alter the resulting diffusion profile. Figure 3.3 shows the difference between the cross section of the front surface without an n+ floating emitter (a) and with an n+ floating emitter (b).

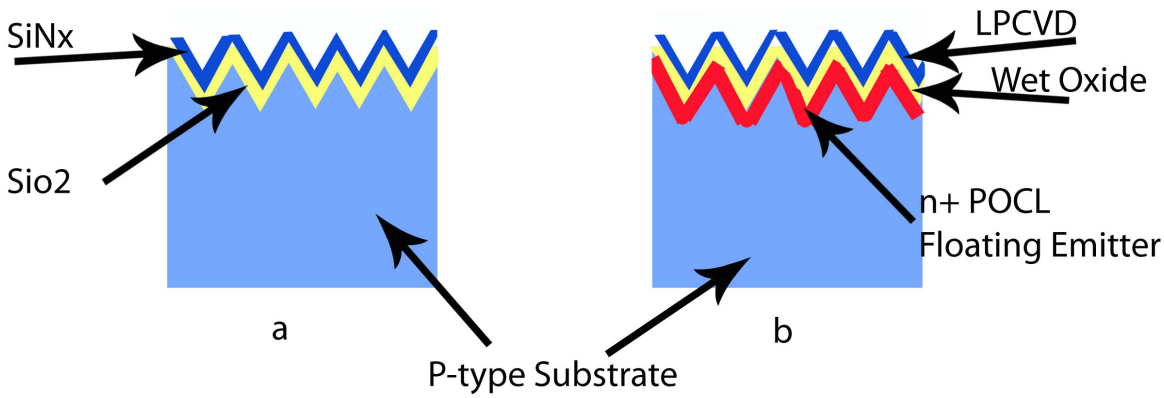


Figure 3.3 - *Diagram of front surface without (a) and with (b) floating emitter*

3.2.6 Antireflective Coating Deposition

Light reflection from the front surface of the device is undesirable. To minimise incident light reflection, it is common practice amongst PV manufacturers to deposit silicon nitride onto the front surface. Typically, silicon nitride is deposited in one of two ways either through plasma enhanced chemical vapour deposition (PECVD) or thermally through low-pressure chemical vapour deposition (LPCVD). For the Saturn cell, the thermal LPCVD silicon nitride process was used as although it has a higher thermal budget due to the higher temperature of the process, LPCVD silicon nitride gives a much better-quality deposition without the cracks and pinholes that are often found in PECVD silicon nitrides. Silicon nitride has a very slow etch rate in hydrofluoric acid when compared to other dielectric deposition layers such as silicon dioxide. This useful property means that by depositing the silicon nitride on top of the front and back surfaces of the silicon wafer the underlying passivation layer is

protected during the phosphorous glass removal stage. Furthermore, this property means that the silicon nitride layer can act as a mask during electroless plating processes. Because the silicon nitride is a dielectric, electroless plating will not occur on the surface but will only deposit on the conductive exposed silicon. This gives a much more economical way of selective metallisation than traditional photolithography would.

LPCVD silicon nitride deposition is a thermal process, with the resultant thickness of the nitride layer being determined by the length of time of the deposition phase in the furnace recipe. For LPCVD silicon nitrides, varying the deposition time, gas pressure and gas composition determines the deposition rate and thus the final thickness of the nitride layer. Silicon nitride is made when silicon is exposed to ammonia. The growth rate is typically slow however and needs to be performed at temperatures between 1000ºC and 1100 ºC. Faster growth rates can be achieved by depositing through reactions between dichlorosilane and ammonia (as described in equation 3.4) with the process being run at 700ºC to 800ºC.

$$3SiH_2Cl_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2 \quad (3.4)$$

The visible colour of silicon wafers changes depending on the thickness of the deposited dielectric layer(s). This gives a crude way for estimating the thickness of the dielectric layer(s). The final colour of the device will need to be taken into consideration as different colours allow for different ranges of wavelengths across the solar spectrum to be absorbed, and the flux of photons in the solar spectrum is not the same across all wavelengths. The objective of the ARC is to allow the device to absorb the broadest range of wavelengths tuned for the optimum effect to the peak in the solar spectrum. Figure 3.4 shows the spectral irradiance and photon flux of the

AM1.5G solar spectrum. Conventional, commercially available solar cells are typically dark blue to black in colour, although in recent times there has been a trend towards producing cells of different colours purely for aesthetic purposes although this change to the ARC can result in a cell that is not optimally tuned for sunlight conversion [117].

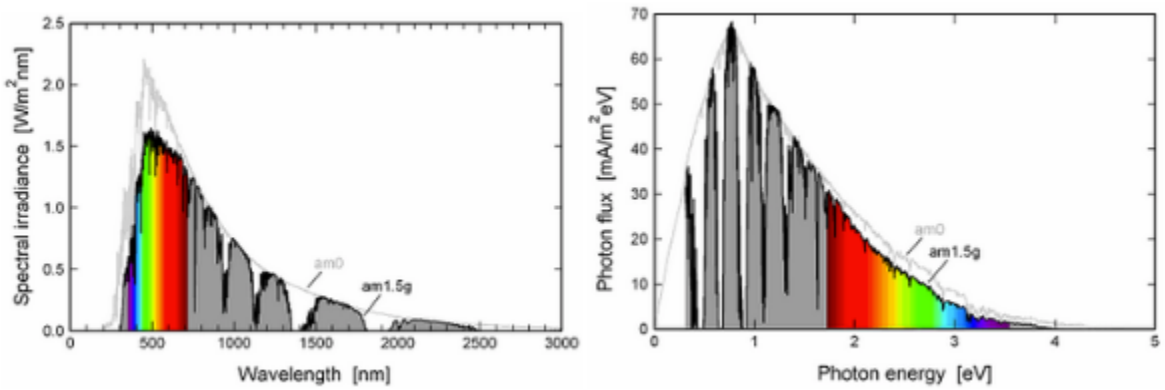


Figure 3.4 - *Spectral irradiance (left) and photon flux (right) of the AM1.5g spectrum* [118]

Figure 3.5 shows the expected colour of the wafers based on the total thicknesses of all dielectric layers deposited/grown on the wafer.

Oxide/Nitride Thickness [Å]	Colour/Code	Colour Name
375	D2B48C	Tan
562.5	A52A2A	Brown
750	B32F79	Dark Violet to red violet
937.5	2E73F3	Royal blue
1125	ADD8E6	Light blue to metallic blue
1312.5	D9ECB3	Metallic to very light yellow-green
1500	F9F9C8	Light gold or yellow slightly metallic
1687.5	DAA520	Gold with slight yellow-orange
1875	F6853D	Orange to Melon
2062.5	B32F79	Red-Violet
2250	5D3694	Blue to violet-blue
2325	0000FF	Blue
2437.5	0083AE	Blue to blue-green
2587.5	00FF00	Light green
2625	84D82E	Green to yellow-green
2737.5	84C82E	Yellow-green
2812.5	E2DE2B	Green-yellow
2925	FFFF00	Yellow.

Figure 3.5 - *Expected colour of wafers based on thickness of dielectric layers* [119]

3.2.7 Plasma Etch to Remove Silicon Nitride from Rear Surface

Unlike an IBC cell, the Saturn solar cell was designed to have front sided contacts as well as rear sided contacts. In order to have a back-surface field and rear contacts, the silicon on the rear surface must be exposed so a plasma etch would be performed to remove the deposited nitride dielectric layer. However in an IBC cell, both sets of contacts are on the rear surface so the masking properties of the silicon nitride as discussed in section 3.2.6 are desired and the silicon nitride layer needs to remain on the rear surface to achieve this. For the IBC cell that this project aims to produce, this step would not be necessary.

3.2.8 Laser Grooving of Emitter and Front Contact Areas

The great step forward that the Saturn cell made was to use a laser to cut into the silicon on the front surface. This serves two purposes, firstly it allows the N++ emitter to be selectively doped by cutting through the nitride ARC which acts as a mask. Secondly it allows narrower contacts than are achievable by surface screen printing, thus allowing for longer grid line lengths resulting in lower contact and series resistances.

The laser used to make these grooves in the Saturn cell has a neodymium-doped yttrium aluminium garnet (Nd: YAG) crystal and a wavelength of 1064 nm. These high speed, split beam pulsed lasers were manufactured by Lee Laser Inc. of America and are coupled with an Anorad 2000 CNC table to control the movement of the stage. Figure 3.6 is a photograph of one of the laser machines used in the development of the Saturn cell, and Figure 3.7 shows wafers on the CNC stage being processed in the laser machine.

Figure 3.6 - *Lee Laser Inc. 1064nm Nd: YAG laser used for Saturn cell fabrication*

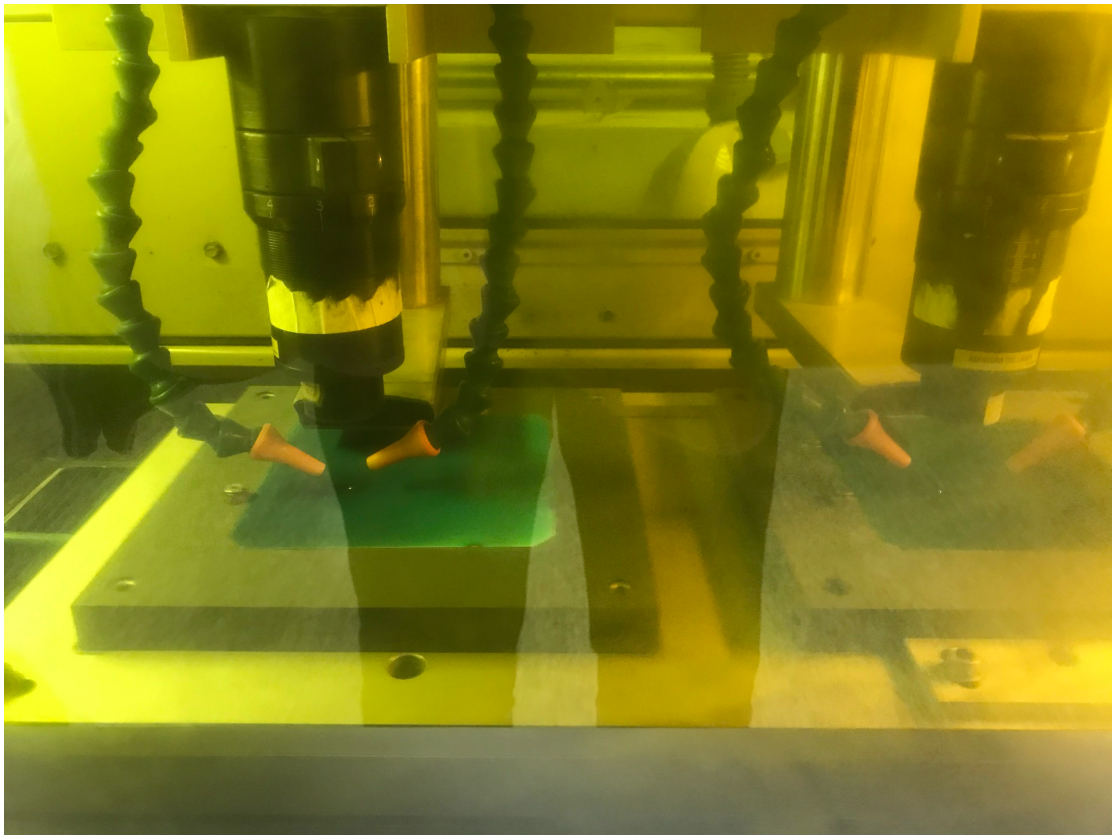


Figure 3.7 - *Wafers being processed in Lee Laser Inc. Nd: YAG laser*

The laser grooves cut for the Saturn cell are typically 40 µm deep and 20 µm wide and for the full-sized Saturn cell the groove pitch is 1.5 mm across the cell surface [120]. Figure 3.8 is a photograph of some 53 mm × 60 mm cell off cut fabricated using the same process steps as used in the Saturn cell. These cell offcuts are designed for use in concentrated solar application though, where the current carrying requirements are much greater than in conventional solar panels so there need to be more grooves with a smaller pitch between the grooves.

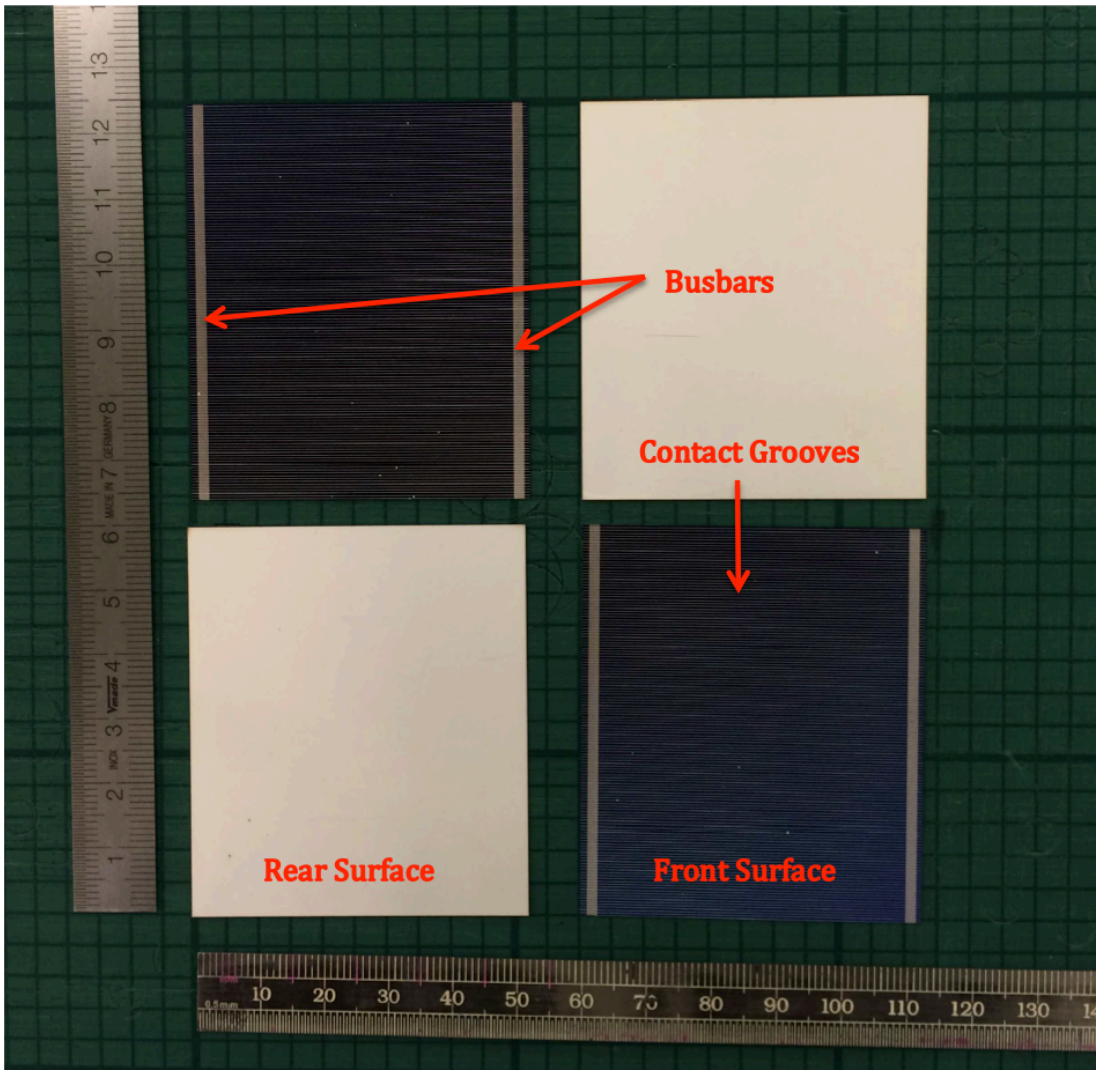


Figure 3.8 - *Photograph of cell offcuts fabricated with Saturn cell technology*

The depth of the grooves can be varied as desired by adjusting the power of the laser and the table speed during processing. Equally, modifying the CNC program code can also vary the groove lengths and the pitch between the grooves.

3.2.9 Groove Damage Removal Etch

The laser grooving process results in a lot of surface damage to the silicon wafers as well as a large amount of debris being left in the groove itself, resulting in a much greater surface area of exposed silicon. Figure 3.9 shows an SEM image of the damage that occurs to the surface of the wafer at the point where the laser interacts with the silicon to form the grooves.

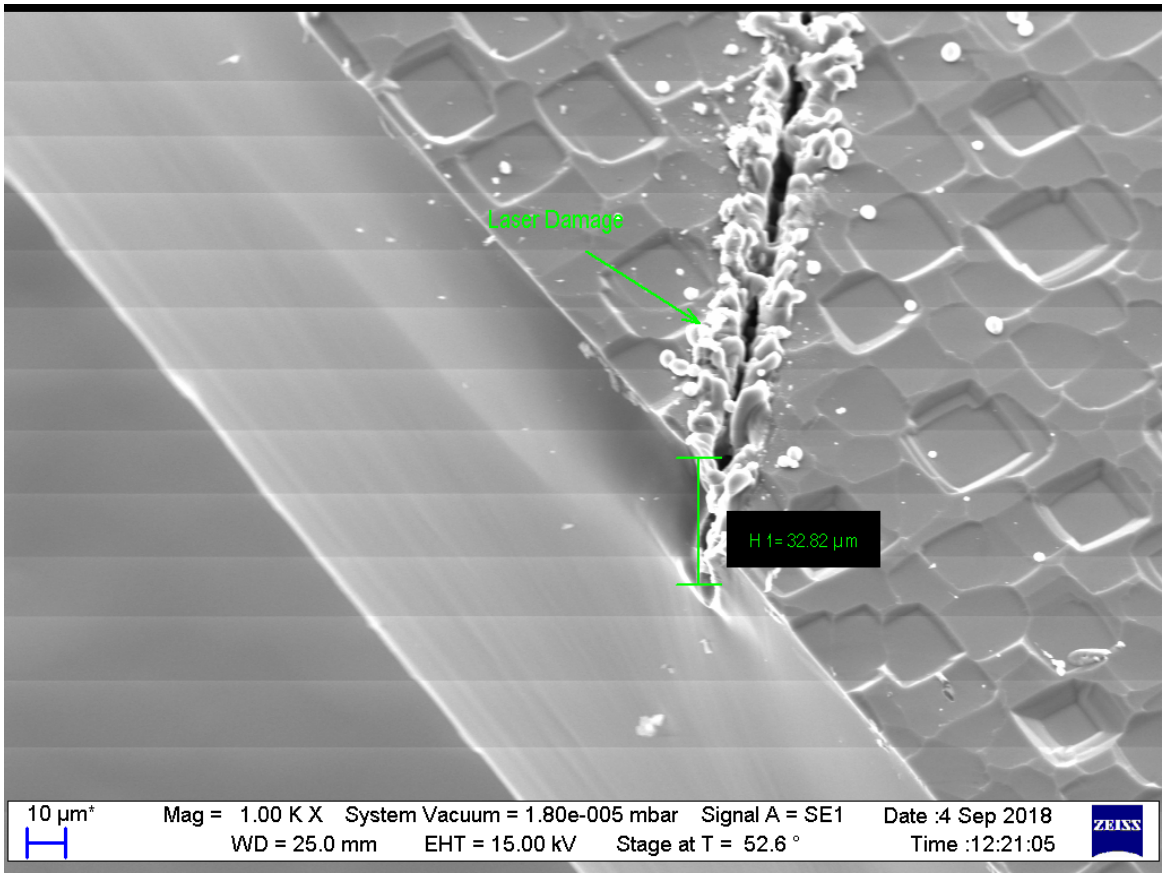


Figure 3.9 - *SEM of groove showing laser damage*

As discussed in section 3.2.6, during the Saturn cell fabrication process, the wafers already have a silicon nitride layer on the front surface. This acts as a mask so that the only areas of exposed silicon are those where the nitride has been removed during the

laser grooving process. This allows a localised alkali etch to be performed to remove the debris in the damaged areas at the surface of the wafer and the debris within the grooves themselves. This groove damage removal (GDR) etch involved immersing the wafer into a 10% sodium hydroxide (NaOH) solution at 60°C for 12 minutes.

3.2.10 N++ Diffusion to form Selective Emitter in Grooves

The Saturn cell was fabricated from a p-type bulk wafer, therefore in order to create the p/n junction required to make working devices, heavily doped N++ emitter regions need to be created. In the Saturn cell, this is achieved with a thermal phosphoryl chloride or phosphorus oxychloride ($POCl_3$) diffusion that diffuses phosphorous into the exposed silicon of the laser cut grooves. There are many techniques for phosphorus diffusion, however $POCl_3$ diffusion has been since the 1970s the de facto standard method for n-type emitter diffusion used in industry. The popularity of $POCl_3$ is due to the low costs, good stability, relative simplicity and high throughputs of the available production equipment [121]. The deposited silicon nitride layer discussed in section 3.2.6 acts as a mask to prevent diffusion into the silicon. This is important as it allows the emitter to be selectively placed. Varying the temperature that the process is run at, the time that the process runs for, the drive-in time and drive in temperature will alter the doping concentration and profile. For the Saturn cell, an N++ emitter sheet resistivity of less than 10 Ω/□ was created. During the deposition phase of the doping process, $POCl_3$ gas reacts with oxygen to form phosphorus-silicate glass (PSG) an alloy of silicon and P_2O_5, as shown in the simplified equation 3.5, on the surface of the silicon. The $POCl_3$ is a liquid at 20°C through which nitrogen is bubbled to give a $POCl_3$ gas flow into the furnace.

$$4POCl_3 + 3O_2 \rightarrow 2P_2O_5 + 6Cl_2 \qquad (3.5)$$

Some of the phosphorus in the PSG diffuses into the silicon surface to dope the silicon n-type as shown in the simplified equation 3.6.

$$2P_2O_5 + 5Si \rightarrow 5SiO_2 + 4P \quad (3.6)$$

After processing, in order to allow the metals to be deposited, the residual PSG must be removed. This is done by a 60 second immersion into a 20:1 hydrofluoric acid solution. Again, because of the previously deposited silicon nitride layer acting as a mask and the fact that nitride takes a long period of time to be etched away by hydrofluoric acid, only the phosphorous glass is removed by this process.

3.2.11 Al Sputtering for Rear Contact and Back Surface Field

As the Saturn cell has the emitter contacts on the front surface, unlike in an IBC cell, the rear surface only has to have the back-surface field (BSF) contacts formed on it. Hartley et al. at BP Solar presented a study into the effects of using thin layers of aluminium to create a p+ back surface field on the Saturn cell [122]. This 1 μm thin layer of aluminium is applied to the entire rear surface by vacuum deposition followed by a high temperature sinter at 995°C. The conclusions of this work demonstrated that a BSF improved the short circuit current (J_{SC}) of the device. For an IBC cell however, as the emitter is also on the back surface of the cell, this approach of creating a back-surface field across the entire back surface used in on the Saturn cell will not be suitable for this project.

3.2.12 Electroless Metal Plating

In the Saturn cell, metallization was achieved by a sequence of electroless metal plating processes involving nickel, copper and silver with intermediate metal sintering. An initial 0.1 μm thick layer of nickel is deposited then sintered to produce

a nickel silicide layer. This layer forms a diffusion barrier to prevent migration of the copper from the subsequently deposited 5 μm layer of copper into the silicon, as well as to produce a high adhesion contact. A very thin layer of silver is then deposited onto the copper to aid with soldering [120].

3.2.12.1 Electroless Plating of Nickel and Sintering

As the LPCVD nitride ARC has masked off the entire front surface of the device apart from the exposed doped grooves, there is no further masking requirement for electroless deposition of metal into the grooves. For nickel, the Enthone AL-100 process is suitable, which is made- up as per the manufacturer's guidelines shown in Table 3–2.

Table 3–2 - *Enthone AL-100 make up recipe*

	Make-up additions ml/litre
Enplate AL-100 A	150
Enplate AL-100 C	70
Deionised Water	780

The process is run at 60°C and a 60 second immersion allows a 0.1 μm layer of nickel to be plated into the grooves. Once the nickel has been deposited it needs to be sintered to produce nickel silicide which is created in an oven that has been purged with nitrogen to create a nitrogen atmosphere at ambient pressure. The process is run at 400°C for 10 minutes. Any native oxides that may form are then removed in a nickel activation process whereby the wafers are immersed in a solution of 10% hydrochloric acid for 2 minutes at room temperature. Nickel is used to act as a diffusion barrier between the silicon and subsequent metallisation steps.

3.2.12.2 Electroless Plating of Copper

Copper is a very good conductor of electrical charge and is a cheaper alternative to silver. For these reasons it was chosen as the metal to be deposited on top of the nickel. This is done as an electroless process by using the Enthone CU-240 process. The solution is made up as shown in Table 3–3.

Table 3–3 - *Enthone CU-240 make up recipe*

	Make-up additions ml/litre
HELIOFAB CU-240 A	60
HELIOFAB CU-240 B	60
HELIOFAB CU-240 C	22.5
Deionised Water	857.5

The process is run at 50°C for 2 hours. The process plates at a rate of 2.5 microns per hour, giving the desired thickness of 5 μm.

3.2.12.3 Electroless Plating of Silver

The final stage of the metallisation processing is to deposit a thin layer of silver on top of the copper so as to allow for easier soldering of tabs to the cell needed when creating modules. The electroless plating process that is used to do this is the Enthone AG-410. This is a two-step process that involves a pre-dip immersion and then a plating immersion. The solutions for both of these steps are made up as shown in Table 3–4.

Table 3–4 - *Enthone AG-410 make up recipe*

Pre-dip Make-up additions ml/litre		Plating Bath Make-up additions ml/litre
300	Heliofab AG-410 A	300
30	Heliofab AG-410 B	50
0	Heliofab AG-410 Silver	20
670	Deionised Water	630

The pre-dip is heated to 40°C and the wafers are immersed for 30 seconds. The plating bath is heated to 50°C for 2 minutes which will deposit 0.15-0.3 μm of dense non-porous silver.

3.2.13 Edge Isolation

As the edges of the wafer may also have been plated with metal during the metallisation process, at the end of the fabrication, the laser is run around the edge of the wafer so as to prevent any potential short-circuiting of the device.

3.3 Other Fabrication Methods Employed

In addition to the processing steps taken from the Saturn cell process flow, several other fabrication methods were used during this project.

3.3.1 Oxide Passivation

In section 2.5.2.1, the PERC cell is presented which showed the improvement in overall cell efficiency that a passivation layer can create by reducing the number of recombinations that occur. To achieve this, a thin layer of silicon oxide will be grown on the front and rear surfaces of the wafer. Two methods of oxidation that are available are wet oxidation and dry oxidation. Wet oxidation uses water vapour (steam) as the oxygen source to grow silicon dioxide on a silicon wafer as shown in

equation 3.7. Dry oxidation uses oxygen gas as the oxygen source to grow silicon dioxide as shown in equation 3.8.

$$Si + 2H_2O \rightarrow SiO_2 + 2H_2 \tag{3.7}$$

$$Si + O_2 \rightarrow SiO_2 \tag{3.8}$$

Wet oxide is much quicker to grow than dry oxide which is due to the oxidant solubility limit in silicon dioxide which is much higher for water than for dry oxygen and this is its biggest advantage. When it is required to minimise time at high temperature a wet oxide should be used. The trade-off for this speed of growth is that wet oxidation leaves more dangling bonds at the silicon interface, which allows for more surface recombinations to occur and results in a lower quality surface passivation layer. Wet oxidation produces a lower density oxide with lower dielectric strength.

Dry oxidation involves heating the wafers to the desired temperature before the atmosphere is filled with oxygen gas for the desired period of time to give the resultant desired thickness of the oxide layer. The oxidation rate is low (<100nm/hr),

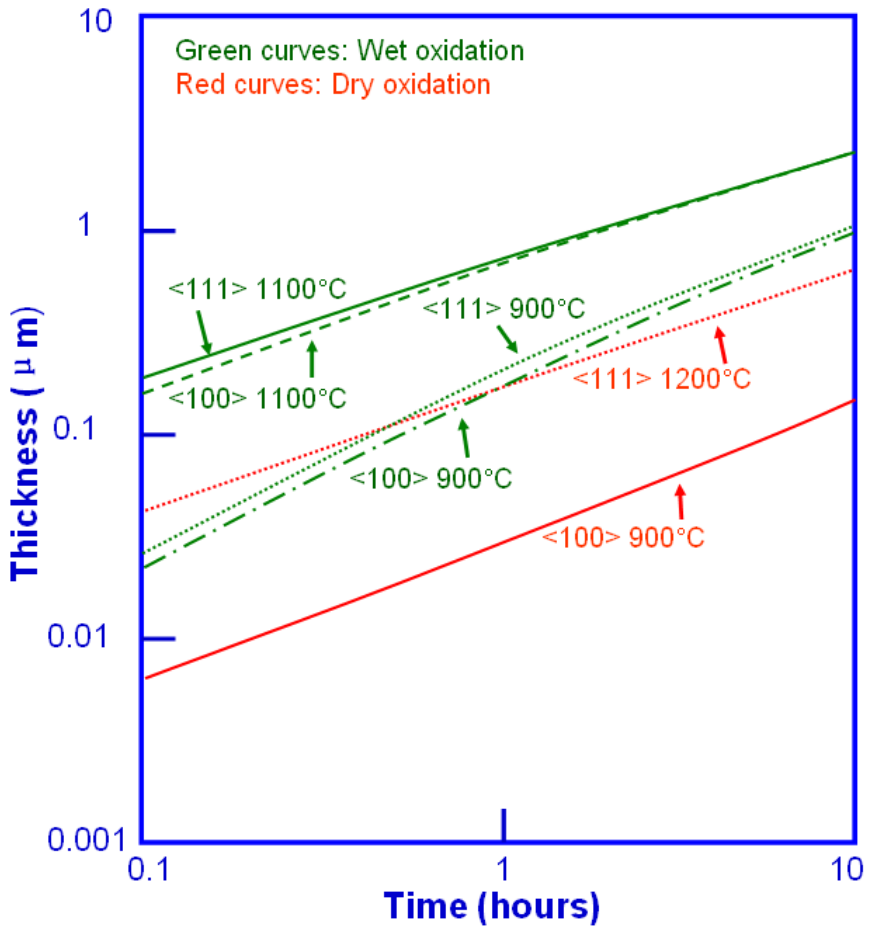


***Figure 3.10** - Wet and dry oxide growth rates for (100) and (111) crystalline silicon substrates at different process temperatures* [123]

Dry oxides are a higher density oxide with a higher dielectric strength that gives a better passivation layer by removing more of the dangling bonds at the silicon interface. However, dry oxides take much longer to grow meaning that the wafer has to spend more time at high temperature. Figure 3.10 shows the growth rates for wet and dry oxides on (100) and (111) crystalline silicon at different temperatures. From this graph, the recipes can be extrapolated for the 80nm wet oxide growth in section 4.2.2 and the 20nm dry oxide growth in section 6.2.

3.3.2 PECVD Silicon Nitride

Plasma Enhanced Chemical Vapour Deposition (PECVD) is widely used within the semiconductor industry as a method of depositing thin films. The process is run at low

pressure and low temperature, typically between 250°C and 350°C, making it ideal for applications where higher temperatures used in other CVD processes (such as LPCVD discussed in section 3.2.6) could damage the device being fabricated. In order to perform a deposition, the chamber must first be pumped to a base pressure (750 mTorr) and the electrodes heated to 350°C before the chamber is purged with nitrogen. Silane and nitrogen are then introduced as the reactant gases to form a plasma silicon nitride following the application of a pulsed high frequency (from a radio frequency (RF) power source up to 600W at 13.56MHz). Equation 3.9 shows the chemical reaction that occurs during this process which results in a Si_3N_4 film that incorporates some of the hydrogen and is often written in short form as SiN:H.

$$3SiH_4 + 2N_2 \rightarrow Si_3N_4 + 6H_2 \quad (3.9)$$

Deposition can also occur at pulsed low frequencies (around 100kHz) but in order for this to happen several hundred volts are required to sustain the plasma discharge. Because of the lower temperatures involved, PECVD deposition films tend to be less dense than higher temperature CVD process techniques.

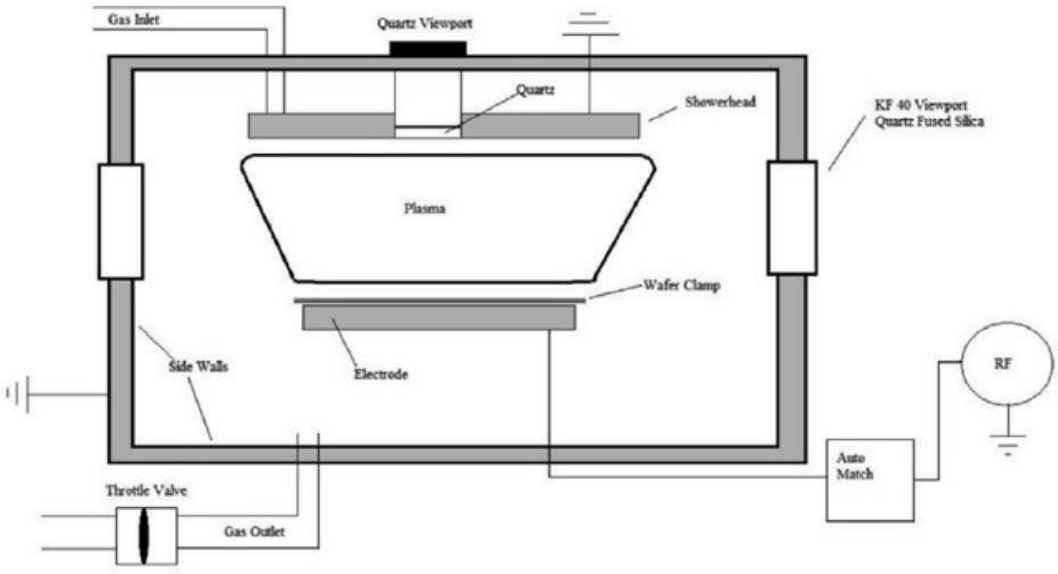


Figure 3.11 - *Schematic diagram of the Plasmalab System 100* [124]

A Plasmalab System 100 from Oxford Instruments was available for use in experimental work on this project. This tool features an automatic loading mechanism and is capable of depositing films of both silicon nitride and silicon dioxide. Figure 3.11 shows a schematic of the Plasmalab System 100.

3.4 Characterisation Methods

3.4.1 Optical Microscopy

Compound microscopes are amongst the most common used pieces of apparatus in scientific and engineering disciplines and are found in nearly every laboratory from secondary schools to high tech industries. They allow a magnified view of a sample to be observed with minimal time required to load the sample. A compound microscope is made of two lenses, one close to the sample called the objective lens that collects light and focuses on a real image of the sample. The second lens is in the eyepiece which magnifies the real image giving an enlarged but inverted image called the virtual image. A schematic of a compound microscope is shown in Figure 3.12.

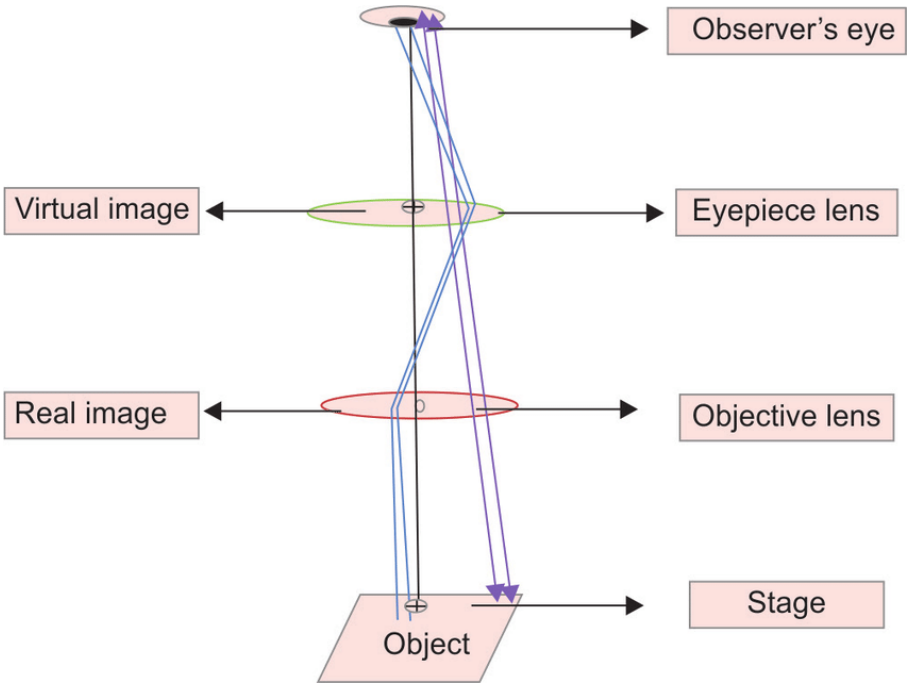
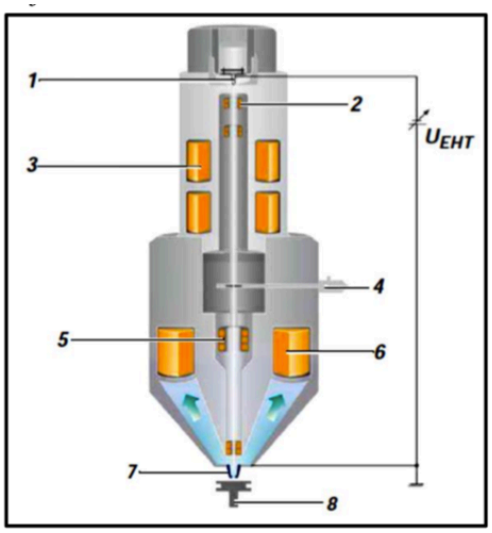


Figure 3.12 - *Schematic of compound microscope* [125]

When both lenses are taken into consideration the total magnification of a compound microscope is typically 40X, 100X and 400X.

3.4.2 Scanning Electron Microscopy

A scanning electron microscope (SEM) is a more advanced microscope that can be used to examine samples at higher magnifications than are possible with an optical microscope. This is done by bombarding the sample with a primary electron beam which causes interaction processes to occur. This generates secondary electrons (SE) and backscattered electrons (BSE) that can be picked up by different detectors within the SEM chamber. Figure 3.13 shows a schematic of a scanning electron microscope.



1 W or LaB6 cathode
2 Gun alignment and emission display coils
3 Double condenser system
4 Mechanical mid column aperture changer
5 Scanning and stigmator coils
6 Objective lens with through the lens pumping
7 CZ BSD
8 Specimen

***Figure 3.13** - Schematic of a Zeiss EVO SEM* [126]

These signals that have been detected can then be used to produce images and information about the sample. For this project, a Zeiss EVO LS25 was used which allows a maximum specimen height of 210 mm and a maximum specimen diameter of 300 mm, much greater than any samples sizes that will be examined. The EVO SEM also allows the sample to be tilted, which is useful for examining laser cut grooves, and has a resolution of 3 nm at 30kV.

3.4.3 Focused Ion Beam Scanning Electron Microscopy

The focused ion beam SEM (FIB-SEM) is a versatile tool that can be used to analyse the structure of a semiconductor device. It is operationally similar to a conventional SEM, however as shown in Figure 3.14, instead of just an electron column, a FIB-SEM features a second column that produces a focused beam of gallium ions. These ions possess high energy, and when they strike the sample, atoms from the surface of the sample can be displaced. This surface modification ability can be used to prepare localized cross-sections of features of interest that can then be imaged at high magnification with the integrated SEM.

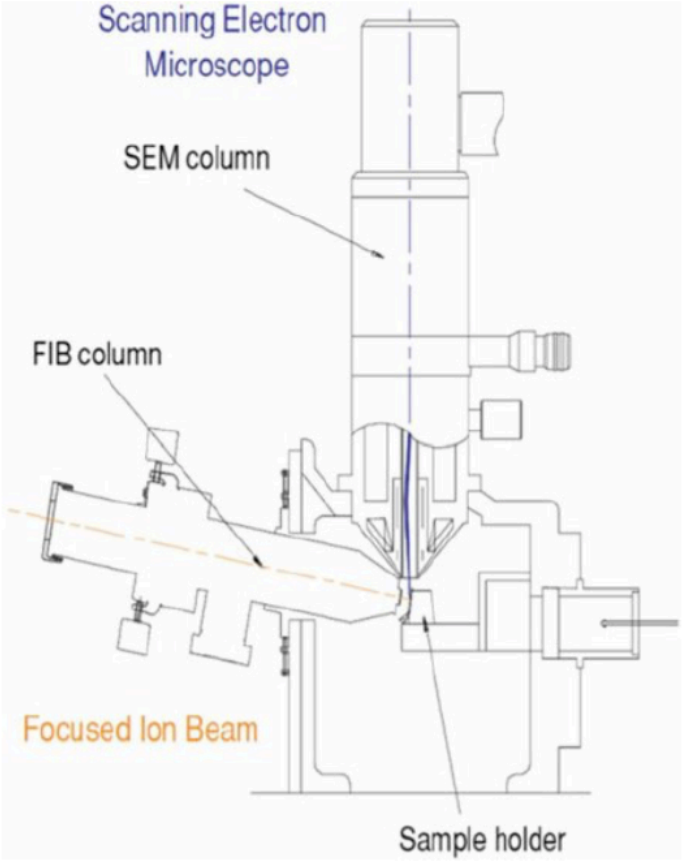


Figure 3.14 - *Schematic of FIB-SEM* [127]

For this project a Zeiss NVision40 FIB-SEM system was used. The integrated field emission gun SEM of the NVision40 is capable of higher resolution imaging compared to the EVO LS25 SEM and so for this project was used to image the thin

oxide and nitride passivation layers that are grown and deposited. The tool was also used to polish cross-sectional surfaces of metallised grooves for subsequent X-ray analysis.

3.4.4 Energy Dispersive X-ray Spectroscopy

Energy dispersive x-ray spectroscopy (EDX or EDS) is another analysis tool that can be used when running an SEM. The benefit that EDX analysis gives is that it can differentiate between different elements in a sample and allows a graphical element distribution map to be displayed. This is particularly useful in situations where layers of elements (such as metal) are applied to a sample as it allows the deposition of each layer to be identified and observed.

Every atom has a unique number of electrons that under normal conditions are present with specific energies. When the electron beam of the SEM hits a sample, part of its energy is transferred to the atoms of the sample. This transferred energy can excite an electron within the atom causing it to vacate the atom and leave a hole behind. The hole is then filled with an electron from a higher energy shell, and the energy difference of this transition can be released in the form of an X-ray. Figure 3.15 shows a schematic representation of this where the e-beam from the SEM energizes

electron A, which then vacates the atom. The resultant hole is then filled by electron B and X-rays are produced.

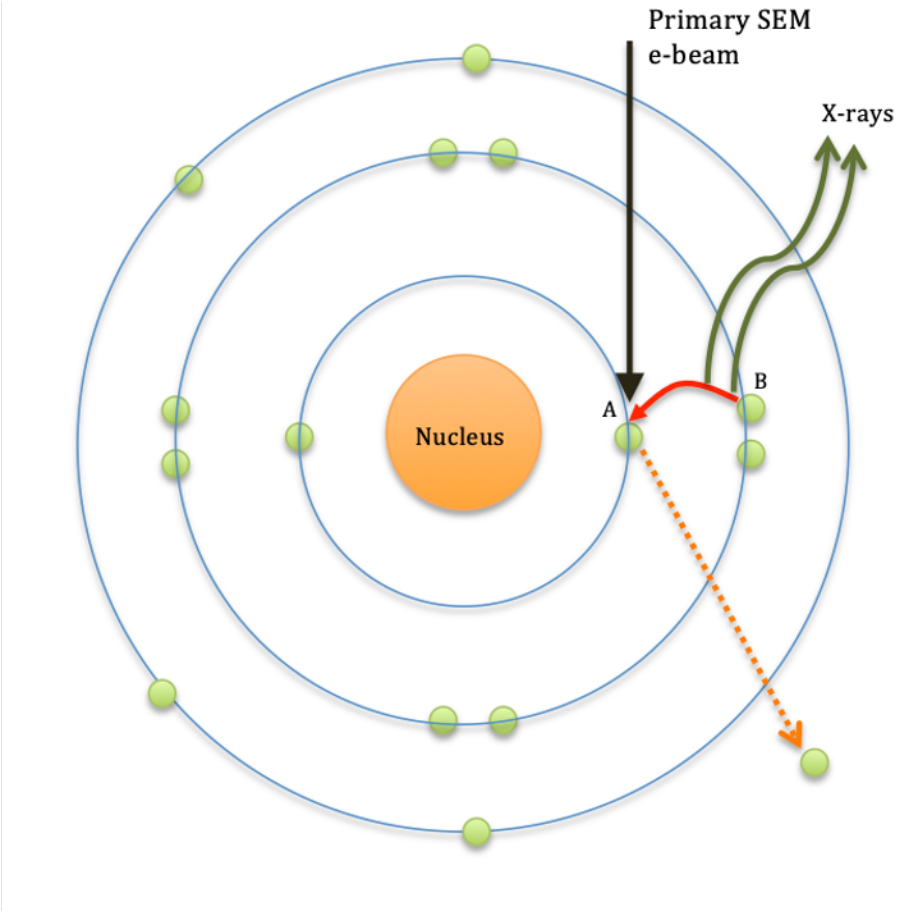


***Figure 3.15** - X-ray generation process in a SEM*

The X-ray that is produced has an energy which is characteristic of the energy difference between the two shells. From this the atomic number can be calculated for the atom that the X-ray has come from, allowing for elements to be identified. For this project, an X-act EDX detector made by Oxford Instruments and installed on the EVO LS25 SEM was used in conjunction with INCA EDX analysis software. The data is then presented as a series of peaks corresponding to the different elements that are detected in the sample. An example of the output of EDX analysis is shown in Figure 3.16. The system also allows for the mapping of elemental distribution through

the collection of multiple spectra from a grid of points on the sample.

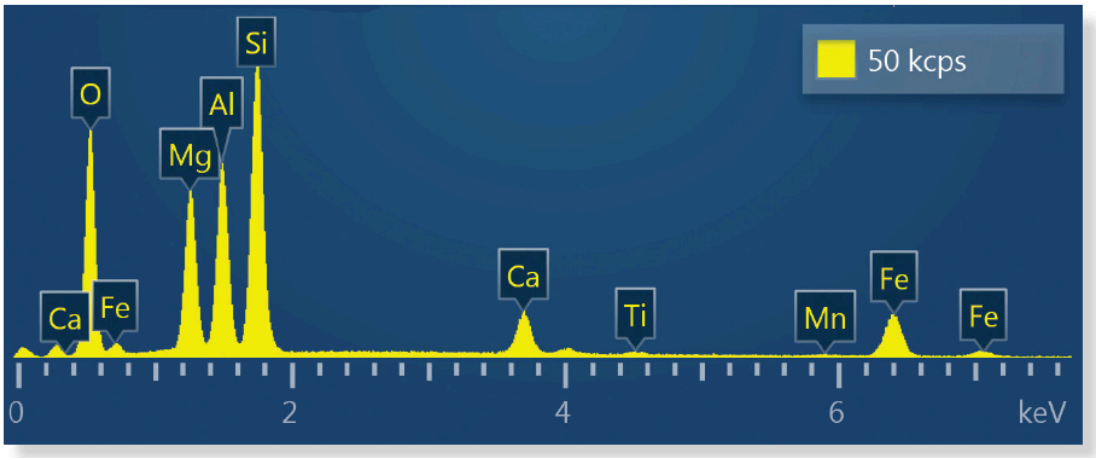


***Figure 3.16** - Example of peaks generated by EDX analysis* [128]

3.4.5 Minority Carrier Lifetime Measurements

In Chapter 2, the importance of good passivation layers leading to higher device efficiencies was discussed in relation to numerous cell designs. Poor passivation leads to high numbers of surface recombinations in the device, which inhibits its performance. The amount of surface recombination can be characterised by measuring the minority carrier lifetime. For this project, a WTC-120 photoconductance tool from Sinton Consulting was used in conjunction with a Xenon flash lamp to measure minority carrier lifetimes. The sample is placed on the WTC-120 where an inductor coil couples to the wafer and allows conductivity to be measured. When the lamp is flashed, a signal proportional to this conductivity is measured and the lifetime measurement is derived from the slope of photoconductance decay curve [129]. There are several different methods of using this tool to calculate the minority carrier lifetime. Where higher minority lifetimes are expected, the Transient method will give an accurate measurement where the rate of decay of the photoconductance is measured from a single, very short light pulse. However, in order to measure very low lifetimes, the quasi steady state

photoconductance method (QSSPC) must be used. This method requires a much longer flash allowing the minority carriers to obtain a steady state condition, which allows lifetimes in terms of nanoseconds to be measured.

3.4.5.1 Transient Photoconductance Decay (PCD) Method

In the transient photoconductance decay method, the carriers are generated by a very short pulse of light, and once the light is terminated the transient decay of the carrier density over time is measured. The effective minority carrier lifetime, τ_{eff} is determined using equation 3.10 which gives the decay rate (slope of the curve).

$$\tau_{eff} = \frac{\Delta n}{\frac{d(\Delta n)}{dt}} \tag{3.10}$$

Where Δn is the excess minority carrier concentration and t is time [130].

3.4.5.2 Quasi Steady State Photoconductance (QSSPC) Method

Quasi steady state lifetime measurements are performed with the light shining on the sample. The intensity of the light flash is assumed to remain constant, allowing the minority carriers in the sample to reach a steady state. This can occur so long as the minority carrier lifetime of the sample is less than the characteristic decay of the light source. The effective minority carrier lifetime is determined using equation 3.11 where G is the generation rate that is determined by measuring the amount of light that falls on the sample and correcting for the reflectivity and absorption coefficient of silicon[131].

$$\tau_{eff} = \frac{\Delta n}{G(t)} \tag{3.11}$$

Because the light source is constant, this method allows a more realistic measurement to be taken for a photovoltaic device in the conditions it is designed to operate under.

When measuring lifetimes of silicon above 150 μs, the transient method is the preferred technique as the transfer function in the QSSPC becomes less accurate. For lifetimes under 150 μs, the QSSPC method is preferred as the transfer function eliminates the surface recombination efficiently[132]. For this project, the QSSPC method will be used as the raw wafer samples have very low minority carrier lifetimes to begin with.

3.4.6 Current – Voltage Measurements

The electrical output performance of crystalline silicon and thin film PV modules are measured under standard test conditions (STC). This ensures that a relatively independent comparison and output evaluation of different solar PV modules is possible.

The industry-wide standard test conditions for PV cells specifies a cell temperature of 25°C, with an irradiance of 1000 W/m^2 when exposed to the AM1.5g light spectrum. Under these conditions a sample can be placed into a solar simulator. The solar simulator has a light source, which is used to illuminate the sample, and electrodes are attached to the sample contacts. Figure 3.17 is a schematic of the solar simulator setup used.

The lamp is briefly flashed (so that temperature control of the cell is not required) during which time the solar cell is swept from short circuit to open circuit whilst the source meter automatically applies a variable load with both the voltage and the current being recorded. This can then be used to plot an IV curve as well as derive other parameters such as fill factor and cell efficiency.

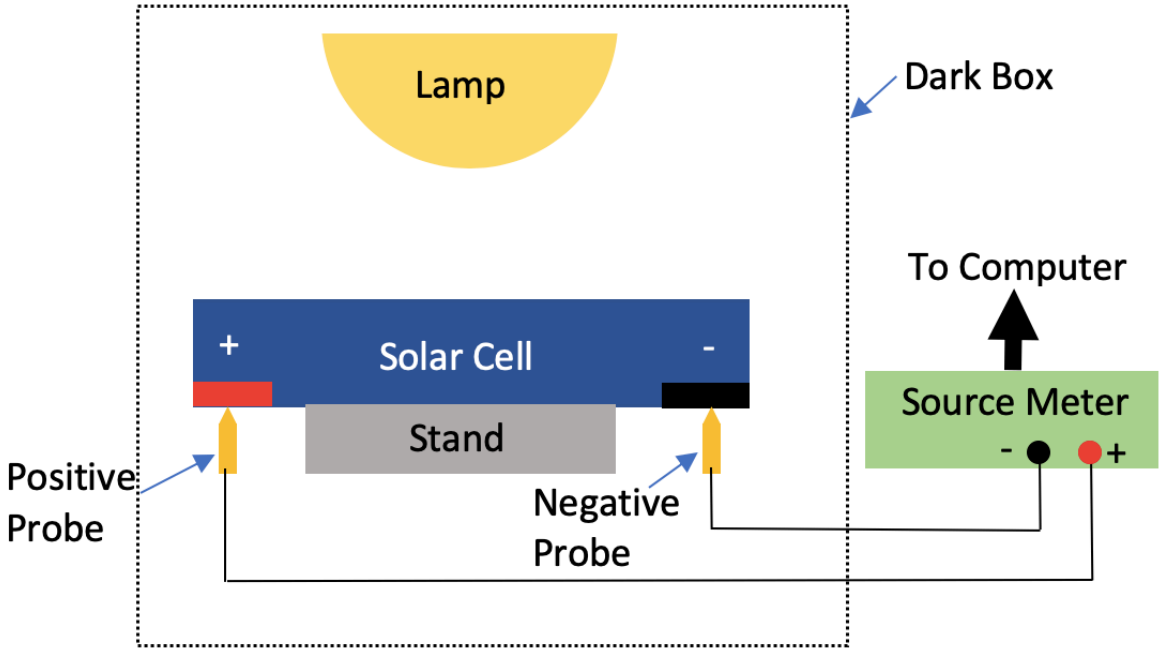


Figure 3.17 - *Schematic of solar simulator setup (not to scale)*

For this project a Keithley source meter along with a Sun3000 solar simulator from ABET technologies were used, which features a Xenon arc lamp, AM1.5g irradiation and a field size of 110 mm × 110 mm.

Chapter 4 Proof of Concept Device

4.1 Simplified Device Design

In order to ensure that the proposed geometry of the new cell will allow a working device to be produced, for this project a simplified cell design was fabricated. This chapter will explain the design elements of the simplified version of the device and present results from various characterisation experiments.

4.1.1 Substrate Selection

In order to make a p/n junction device, a substrate must be chosen that can be doped p-type and n-type. Crystalline silicon is suitable for use as a substrate because it can be doped with an element that will bond with the silicon atom giving either a free electron (n-type) or free hole (p-type) in the resultant crystalline structure. In section 2.1 doping with phosphorus to give n-type silicon or doping with boron to give p-type silicon was discussed. Since 2019, the price of n-type and p-type CZ wafers has been comparable (p-type being slightly cheaper largely due to market demand) [161]. At the beginning of this project the price difference was greater, and p-type wafers were more readily available. Furthermore, in order to create a p/n junction the substrate needs to be doped with phosphorus on a p-type wafer or boron on an n-type wafer. Phosphorus doping through the $POCl_3$ process (outlined in section 3.2.10) was available for use in this research whereas boron doping was not. Finally, should this research prove successful, one of the goals of this project is to be able to integrate into existing PV manufacturing setups as smoothly as possible and at the start of this project, 84% of silicon PV cells produced worldwide use a p-type substrate [133]. For experimental work within this project, boron doped p-type monocrystalline CZ wafers

with a bulk resistivity of 1.0-3.0 Ω.cm, a crystallographic surface orientation of (100) and a thickness of 200 μm were used. Wafers with a lower bulk resistivity (<1.0 Ω.cm) would have given a cell with a higher V_{oc} however for the experimental work in this project wafers with a bulk resistivity of 1.0-3.0 Ω.cm where used as these was the lowest bulk resistivity wafers made available (bulk resistivity (ρ) of a material can be used to calculate the sheet resistance (R_s) of a film by dividing it by the thickness of the film (t) as shown in equation 4.1).

$$R_s = {}^{\rho}/_{t} \tag{4.1}$$

4.1.2 Outline of Initial Fabrication Processes

The objective of this initial device is to prove that a solar cell can be fabricated with the proposed geometry, using process steps taken from the Saturn cell. For this proof of concept device, no optimisation was performed and the fabrication processes where minimised, so should a successful device be fabricated it would be not be expected to perform very well. Figure 4.1 shows schematics of the first 4 steps for this proposed device.

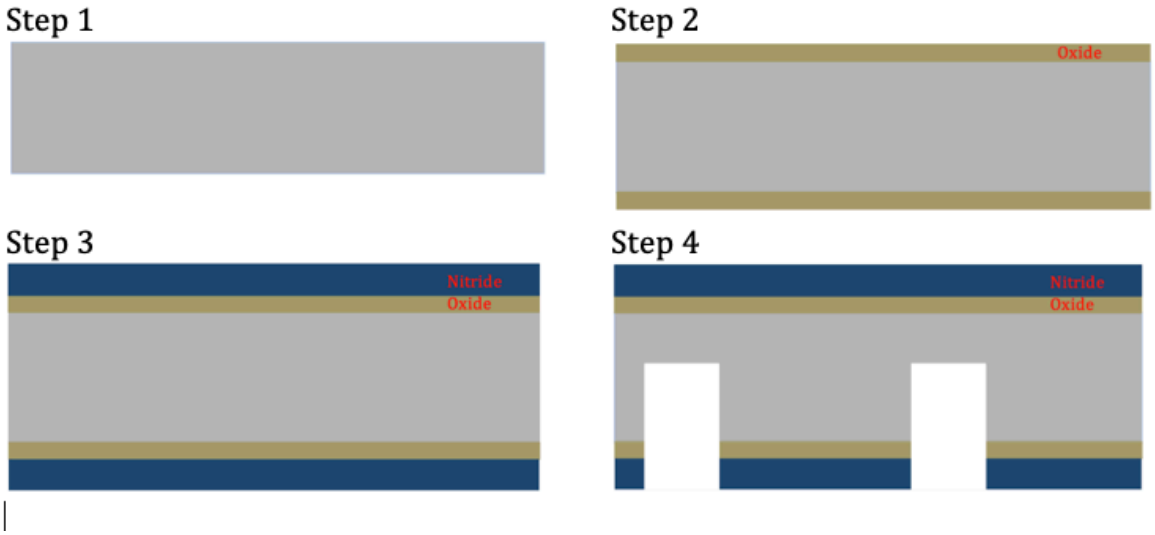


***Figure 4.1** – Steps 1-4 of initial fabrication processing*

Table 4–1 describes each of the process steps seen in Figure 4.1.

Table 4–1 *- Steps 1-4 of initial process fabrication*

Process Step Number	Process Details
Step 1	**Saw damage removal** – 30% NaOH at 80°C for 5 minutes. Followed by RCA cleaning
Step 2	**Wet oxidation** – 35 min wet oxidation at 900°C followed by 15 a minute anneal.
Step 3	**Silicon nitride deposition** – 100 nm PECVD nitride deposition at 350°C
Step 4	**N-type groove cutting**. Laser process run at 3.5 kW with table speed of 200mm/min. 10% NaOH dip at 60°C for 10 minutes groove damage removal.

The schematics for the remaining steps are shown in Figure 4.2.

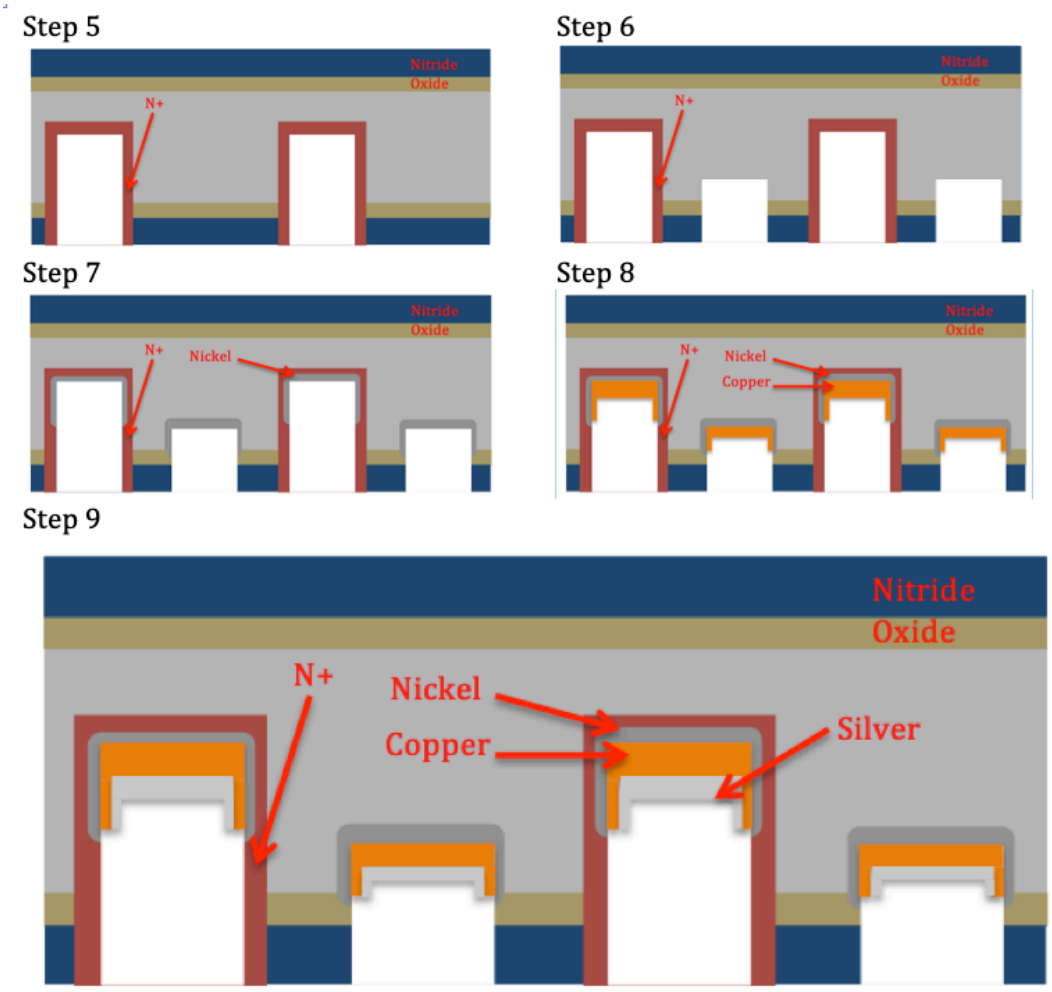


Figure 4.2 *- Steps 5-9 of initial fabrication processing*

Table 4.2 describes the process steps as shown in Figure 4.2.

Table 4–2 - *Steps 4-9 of initial process fabrication*

Process Step Number	Process Details
Step 5	**POCL Groove Diffusion** – 20-minute POCL diffusion at 930°C followed by a 10-minute drive in at 950°C to give sheet resistivity of 10 Ω/□
Step 6	**P-type groove cutting**. Laser process run at 2.5kW with table speed 200mm/min to give shallow grooves for p-type contact. 10% NaOH dip at 60°C for 10 minutes groove damage removal.
Step 7	**Nickel Deposition** – 60 second 7:1 hydrofluoric acid dip to remove phosphorus glass followed by Enthone AL100 process run at 60°C for 60 seconds followed by a 10-minute sinter at 400°C and activation by a 2-minute dip in 20:1 hydrochloric acid at room temperature
Step 8	**Copper Deposition** – Enthone CU240 process run at 50°C for 60 minutes with agitation.
Step 9	**Silver Deposition** – Enthone AG410 process, 30 second pre-dip at 40°C followed by a 2-minute plating dip at 50°C

4.1.3 Interdigitated Laser Groove Design

Originally on the BP Saturn cell, laser grooving was performed on the front surface only so as to provide the buried contacts. For this project, it will be applied to the rear surface for both positive and negative contacts. Laser processing is the key feature of this device geometry with the aim of allowing conventional solar grade silicon to be used whilst having all of the device contacts on the rear surface, therefore eliminating the front surface shading. As discussed in Chapter 2, the reason for using more expensive high lifetime silicon is that the charge carriers are generated at the front surface and collected at the rear. To overcome this in this design, the n-type grooves that make the emitters are cut deep into the silicon, thereby bringing them closer to the front surface where the charge carriers are produced. The effect of this is to shorten the current path between charge carrier generation and collection, however the enlarged silicon-metal contact area will lead to increased recombination which

will have a negative effect on the performance of the device. The collector fingers for both the p-type region and the n-type region interdigitate with each other and connect to either the p-type busbar or the n-type busbar at the edge of the device accordingly. The layout of the rear side laser grooving is shown as a 2D illustration in Figure 4.3.

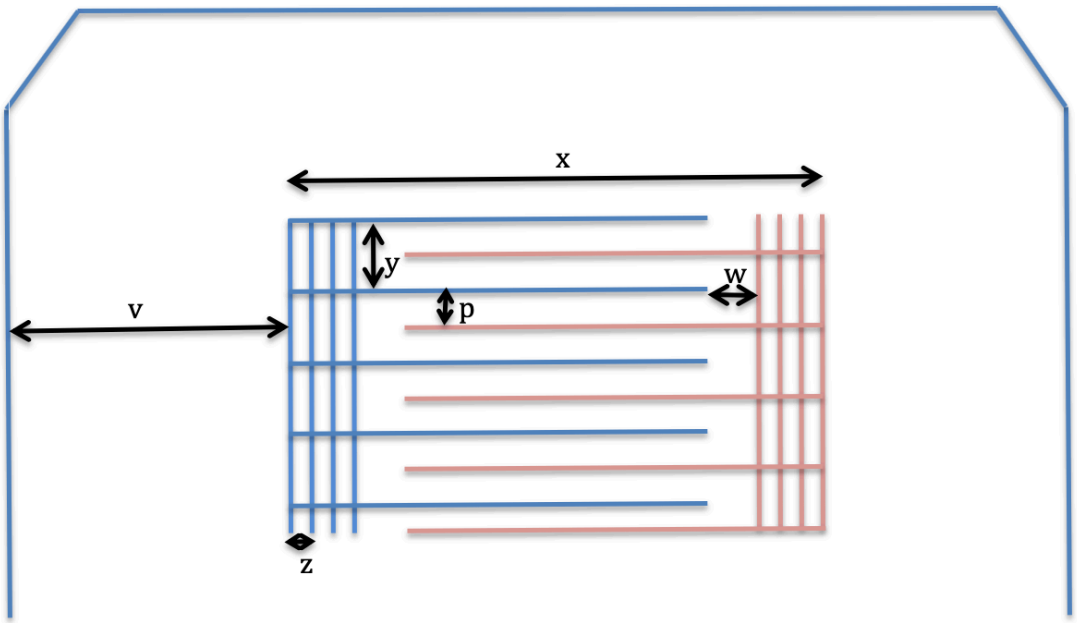


Figure 4.3- *Schematic of laser cut grooves*

The locations p, v, w, x, y and z marked in Figure 4.3 refer to dimensions detailed in Table 4–3. The wafers must be inserted into the laser machine for processing twice. This means accurate alignment of the wafer is vital so that the second laser-processing step does not cut into the grooves made in the first laser processing step. In order to increase the margin of error available on realignment (and thus decrease the wastage due to the potential misalignment on the laser stage) it is critical that the groove pitch (distance between the grooves marked 'p' in Figure 4.3) used for the initial fabrications is not too small. This is varied by changing the same type groove pitch, marked 'y' in Figure 4.3 in the laser grooving program code. The parameters shown in Table 4–3 have been chosen for initial fabrication to create a device size of 50 mm

× 50 mm which will allow for easy realignment as well as subsequent characterisation of the device to be performed.

Table 4–3 - Laser grooving parameters

Device side length (mm) (x)	50	Distance between Busbar lines (mm) (**z**)	0.1
Number of gridline fingers	165	Distance in from outside edge of wafer (mm) (**v**)	37.5
Same Type Groove Pitch (mm) (y)	0.3	Distance between busbar and non-connecting fingers (mm) (**w**)	0.2
Number of busbar lines	16		

4.2 Initial Process Development

4.2.1 Saw Damage Removal Etch

The saw damage removal etch described in section 3.2.2 was applied to the as-received raw wafers, followed by an RCA clean. After this process was performed, the wafers become visibly much more mirror-like as is demonstrated by comparing the photograph of the raw wafer in Figure 4.4, which has not had saw damage removal, with that of the wafer in Figure 4.5, which has been through the saw damage removal process. A visible reflection of the printed word is easily readable in Figure 4.5 whereas it is not in visible at all on the wafer in Figure 4.4. The saw damage removal process reduces the thickness of the wafer to approximately 180 μm.

Figure 4.4 - *Unprocessed wafer before saw damage removal*

Figure 4.5 - *Unprocessed wafer after saw damage removal*

4.2.2 Wet Oxidation

In Chapter 2, the need for a passivation layer was discussed in terms of improving the resultant efficiency of the final device. To achieve this for the proof of concept device, a layer of wet silicon oxide is grown on the front and rear surfaces of the wafer. Wet oxide is grown thermally, and for this initial experiment a relatively thick

layer of 80 nm is grown, which is not optimal but allows the proof of concept of the geometry to be achieved. From Figure 3.10, in order to achieve the desired thickness of wet oxide, a furnace recipe was run that incorporates a 35-minute wet oxidation at 900°C followed by a 15 minute anneal in nitrogen. Using ellipsometry, the resulting thickness of the grown layer of wet oxide was measured to be 80 nm (±2 nm). Figure 4.6 is a photograph of a wafer following this wet oxide growth.

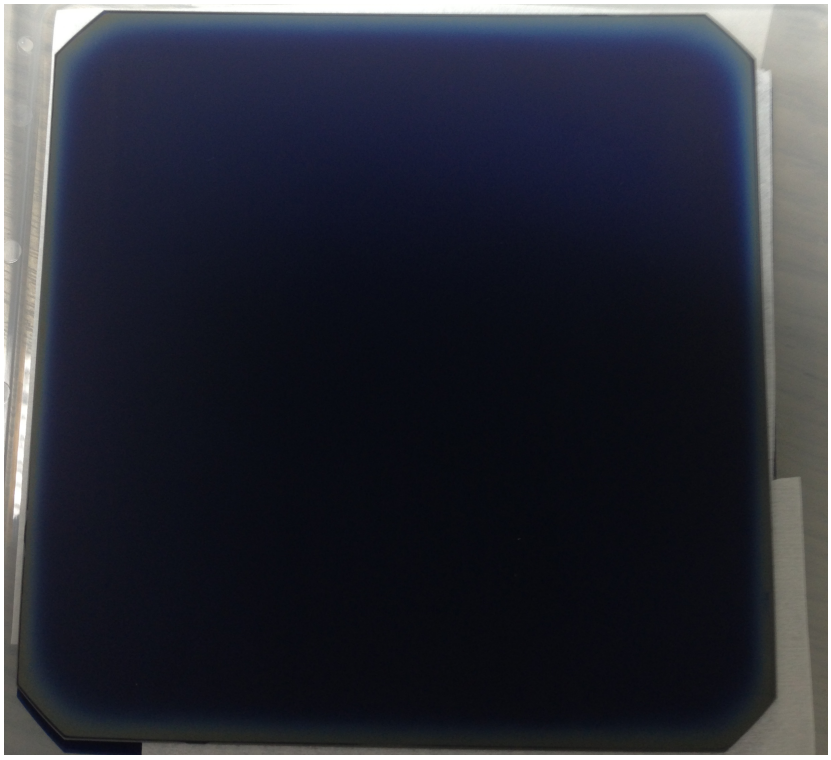


Figure 4.6 - *Photograph of wafer after a 35-minute wet oxide growth*

4.2.3 Silicon Nitride Deposition

As mentioned in section 3.2.6, there are several methods of silicon nitride deposition to consider for the anti-reflective coating. The two methods available for work in this project are plasma enhanced chemical vapour deposition (PECVD) and low-pressure chemical vapour deposition (LPCVD). PECVD silicon nitride can be deposited at lower temperatures, typically around 300°C, which is preferable to LPCVD, which must be done at higher temperatures, around 800°C therefore PECVD silicon nitride

impacts less upon the thermal budget of the resultant device. LPCVD however gives a denser, higher quality silicon nitride. Figure 4.7 shows two wafers, the left wafer has had an LPCVD silicon nitride deposited on it, and the right has had a PECVD silicon nitride deposited on it. During subsequent thermal steps, the PECVD silicon nitride has cracked, exposing the underlying silicon dioxide, which is then etched off during later hydrofluoric acid dips. This causes the underlying silicon to be exposed and subsequently plated during metallisation. This is a far from desirable situation resulting in a short circuit.

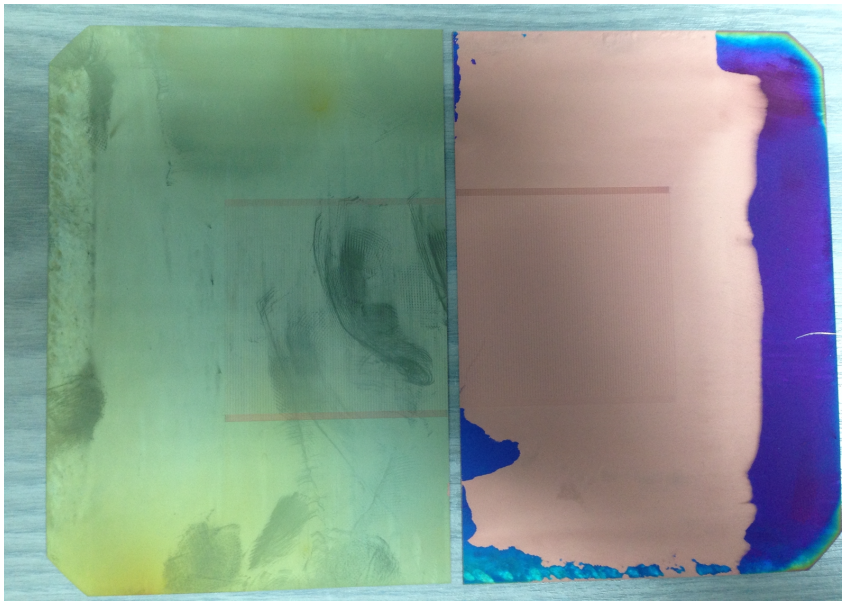


***Figure 4.7** - Wafers with LPCVD and PECVD ARC post metallisation*

The wafer with LPCVD silicon nitride however does not exhibit this problem and has acted as both an anti-reflective coating and a mask. Because the process has not been optimised, the colour of the wafer shown in Figure 4.7 appears gold which will not provide a good ARC. This gold nitride ARC layer was achieved by running a furnace recipe with a 25-minute nitride deposition at 800°C in a nitrogen atmosphere with the dichlorosilane (DCS) running at 60 standard cubic centimetres per minute (SCCM). This recipe gave a deposited silicon nitride thickness measured as 120 nm (±2 nm).

4.2.4 Laser Grooving and Groove Damage Removal

As explained in section 3.2.9, the laser grooving process results in a lot of surface damage to the silicon wafers as well as a large amount of silicon debris being left in the groove itself which increase the number of surface recombinations. When the laser interacts with the silicon, the silicon is vaporised and then re-solidifies leaving silicon debris. Figure 4.8 shows the silicon debris that occurs on the surface of the wafer where laser interacts with the silicon during the cutting of the grooves when viewed in an SEM.

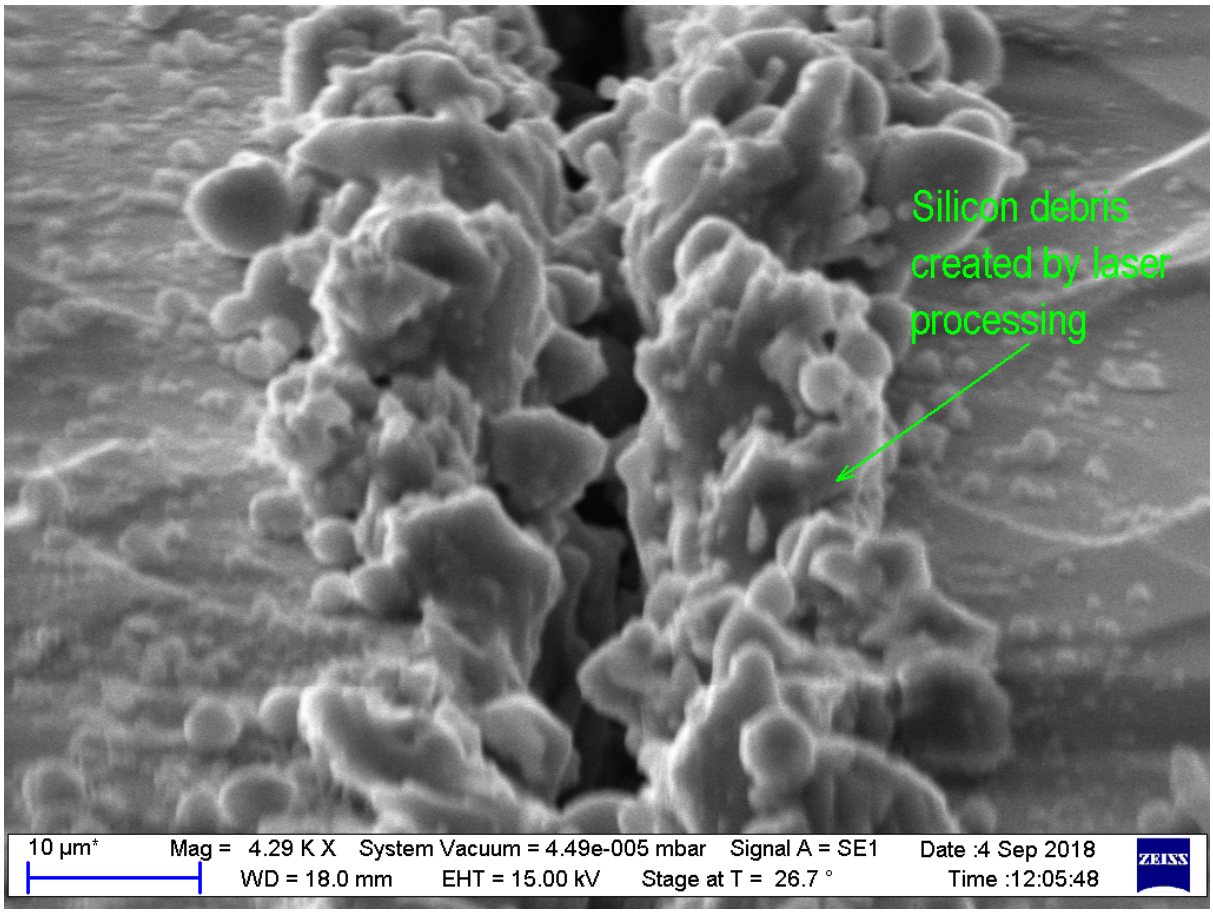


Figure 4.8 - *SEM images of silicon debris after laser processing*

It is not just the surface of the wafer that is damaged during the grooving; the laser process also leaves silicon debris in the grooves and leaves the groove walls uneven and rough as shown in Figure 4.9.

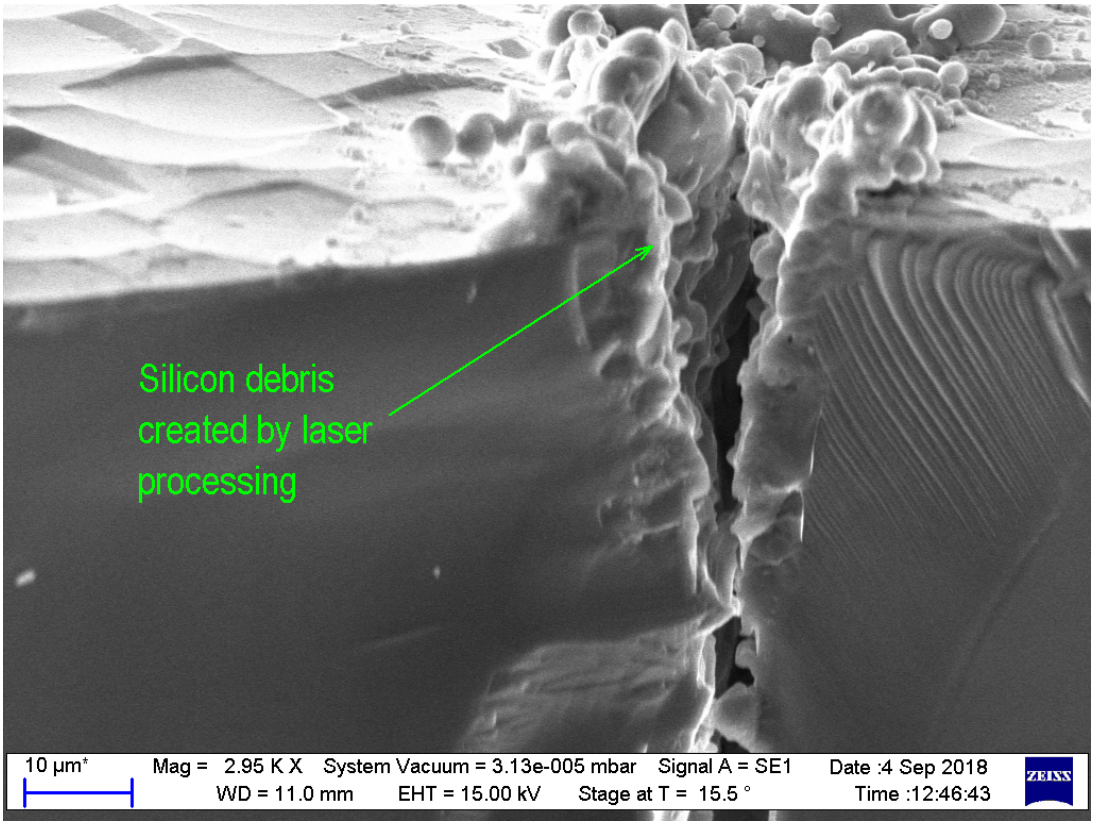


***Figure 4.9** - SEM image of laser damage within grooves*

Figure 4.10 shows wafers that have been given an alkali groove damage removal (GDR) etch following laser processing (see section 3.2.9). This etch involves immersing the wafers into a 10% sodium hydroxide (NaOH) solution at 60°C for 12 minutes. Contrasting these images with those seen in Figure 4.8 and Figure 4.9, the

surface now appears to be smooth up to the edges of the grooves, which in turn are clean and free from the debris caused by the laser processing steps.

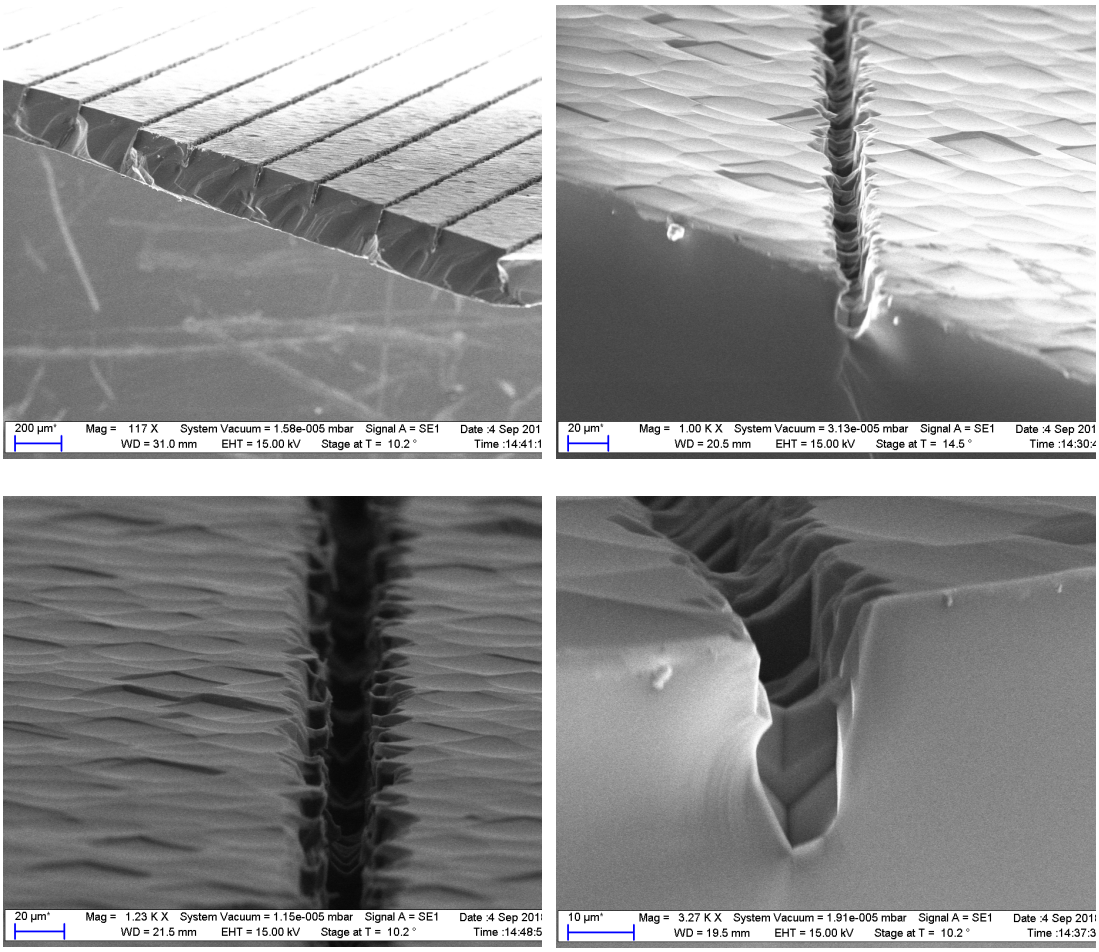


Figure 4.10 - *SEM images of grooves after an alkali groove damage removal etch*

4.2.5 Laser Groove Depth Analysis

Changing either the power that the laser operates at for cutting or the speed at which the table holding the wafers moves, allows the depths of the grooves to be varied. As has been discussed earlier, one of objectives of this project is to create an IBC solar cell using cheaper CZ wafers. The way that this is going to be achieved is by using a laser to cut into the silicon at the rear surface so as to bring the charge collecting emitter (the n+ doped grooves) closer to the front surface where the charge is generated. This narrowing of the distance the charge must travel should allow the use of the lower bulk lifetime CZ silicon material. By trying a range of different laser

powers and table speeds then measuring the resultant groove depth with an SEM it is possible to work out the recipe needed to cut grooves to a desired depth. Table 4–4 shows the depths of twelve grooves and the value of the variable parameters used to create them. For these experiments, the wafers already had silicon dioxide surface passivation and silicon nitride ARC layers and the laser was run in continuous wave mode (CW) with the laser passing over the groove twice (once in each direction). Lasers can also be run in pulsed mode where the laser pulses on an off (using a q-switch) allowing for more reproducible and uniform groove cutting however this facility was not available for this project.

Table 4–4 - *Groove depth results*

Groove	Table Speed (mm/min)	Laser Power (kW)	Groove Depth (µm) ± 2.0 µm
1	200	2.5	14.4
2	200	3.0	29.3
3	200	3.75	59.8
4	200	4.5	77.1
5	100	2.5	33.1
6	100	3.0	38.1
7	100	3.75	69.5
8	100	4.5	89.7
9	50	2.0	6.4
10	50	2.5	31.1
11	50	3.0	57.2
12	50	3.75	119.9

Each of the wafers was given an alkali groove damage etch comprising a 12-minute immersion in a 10% sodium hydroxide (NaOH) solution at 60°C following laser processing. Figure A-1, Figure A-2 and Figure A-3 in 7.3Appendix A show the SEM images of the grooves from which these measurements were taken. This data is then displayed graphically in the plot shown in Figure 4.11, showing the groove depth (µm) versus the laser power (kW) for different table speed on samples that have had the groove damage removal process performed.

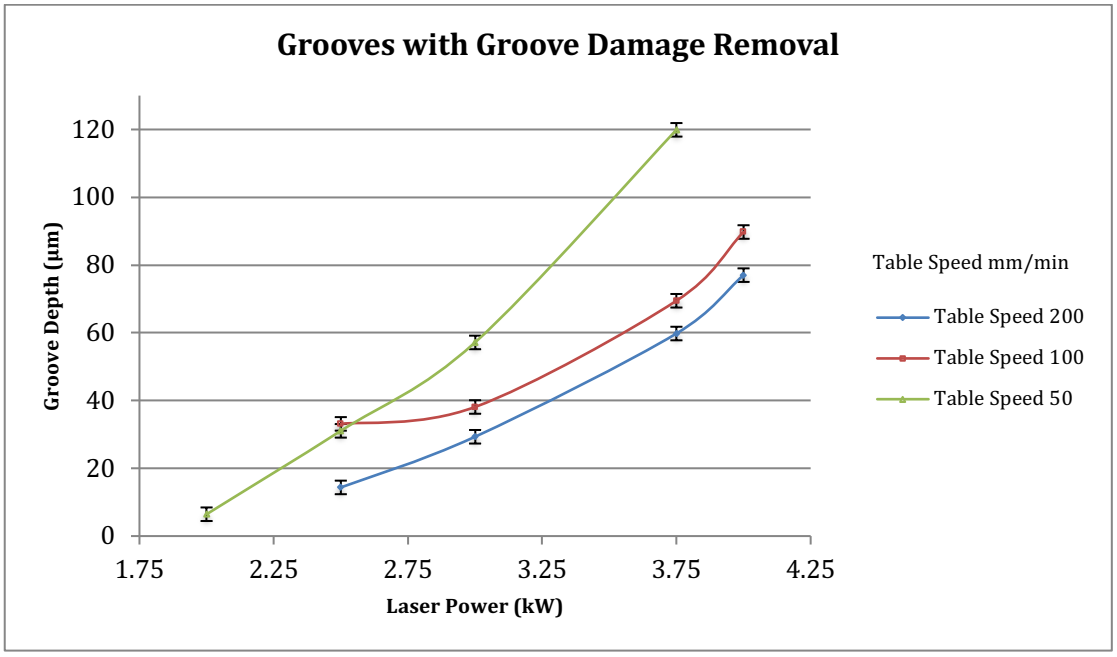


Figure 4.11 *- Plot of groove depth vs. laser power Error bars ± 2µm*

The effect of the laser grooving process on the minority carrier lifetime was then investigated by QSSPC as outlined in section 3.4.5. A raw wafer direct from the manufacturer that has only had the saw damage removal process described in section 3.2.2 as a base reference. The raw wafer selected for this experiment (using the Sinton tool described in section 3.4.5) had a minority carrier lifetime of 12.9 µs. Table 4–5 shows for a selection of groove depths how the average wafer minority carrier lifetime is affected. The wafers had all been subject to silicon dioxide surface passivation and a silicon nitride ARC before laser grooving. These dielectric layers allow only the exposed grooves and silicon debris to react in the groove damage removal process. These measurements are of 'effective lifetime', which could have contributions from both surface and bulk. The groove damage process is only changing the surface of the grooves so subsequent changes in effective lifetime will be due to a reduction in recombination there. This data is shown graphically in Figure 4.12.

Table 4–5 – *Average wafer lifetime measurements for wafers with grooves that have had groove damage removal performed*

Laser Power (kW)	Table Speed (mm/min)	Groove Depth (µm) ± 2.0 µm	Minority Carrier Lifetime (µs)
2.5	100	33.11	8.9
2.5	200	14.4	10.8
3.75	100	69.5	6.18
3.75	200	59.8	6.83

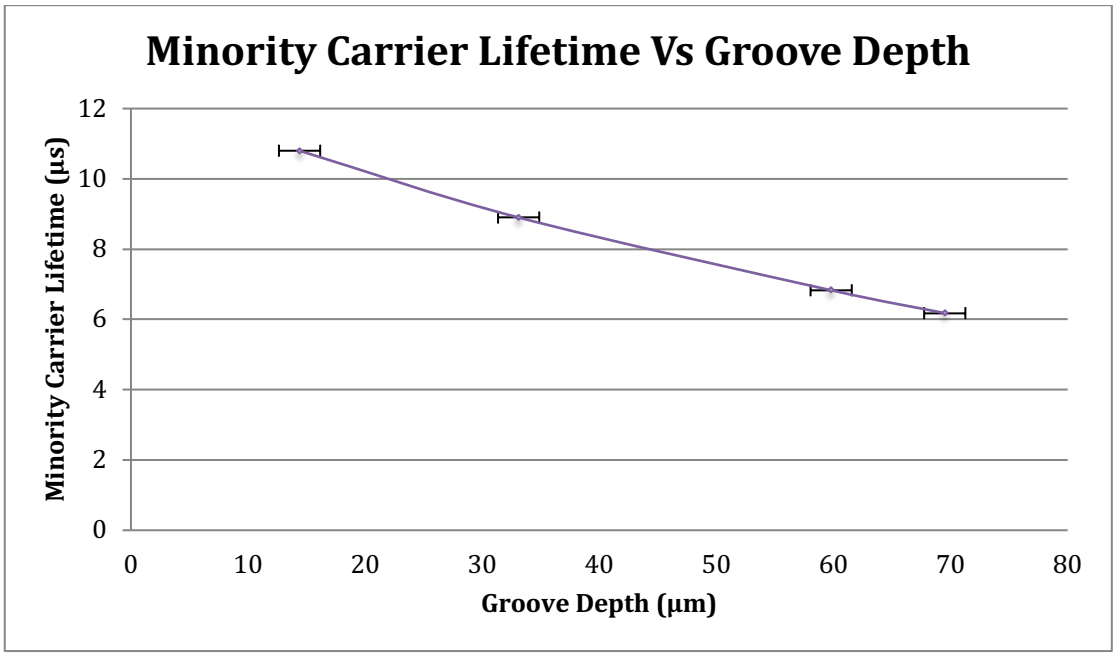


Figure 4.12 - *The effect of groove depth on average wafer minority carrier lifetime. Error ± 2µm*

From this information there is a compromise to be made between the depths of the grooves and the resultant minority carrier lifetime of the wafers. For the proof of concept cell, the deep n-type grooves, were cut to a depth of 77 µm ± 2 µm, just under half the width of the wafer and for the shallow p-type grooves a groove depth of 30 µm ± 2 µm was cut.

The widths of the grooves are fixed by the size of the focused laser spot and taper from the top to the bottom of the groove. Figure 4.13 is an SEM image of a groove

with a depth of 88µm ± 2 µm. The width of the groove is measures as being 30 µm ± 2 µm wide at the top tapering down to 19 µm ± 2 µm at the bottom.

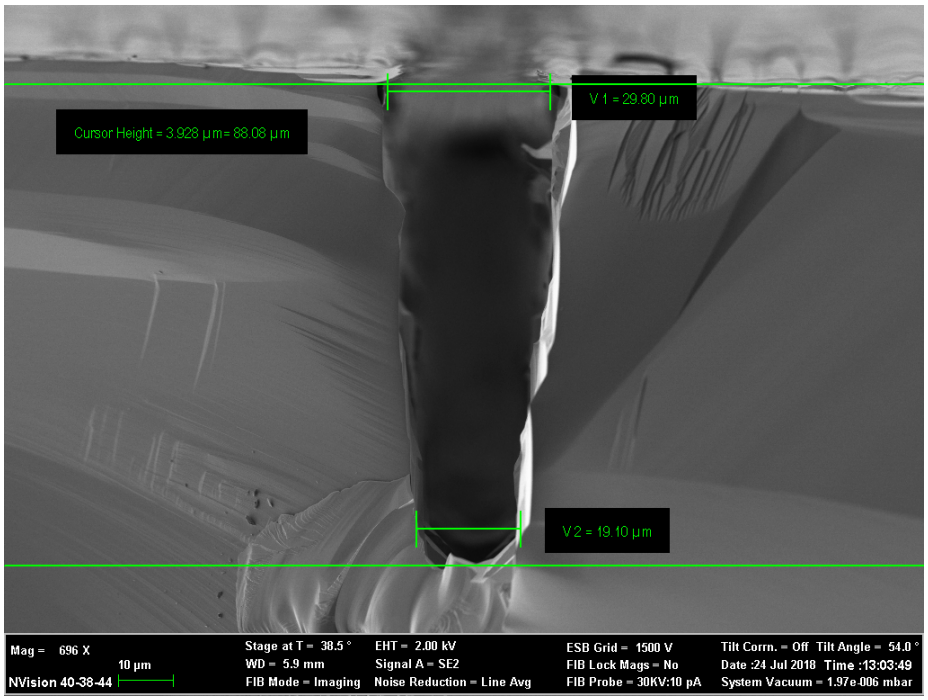


Figure 4.13 - *SEM of groove cross-section with width measurement annotated.*

Figure 4.14 shows the minority carrier lifetime measurements for wafers before and after the alkali groove damage removal etch was performed. There is a significant improvement to the minority carrier lifetime as a result of this process.

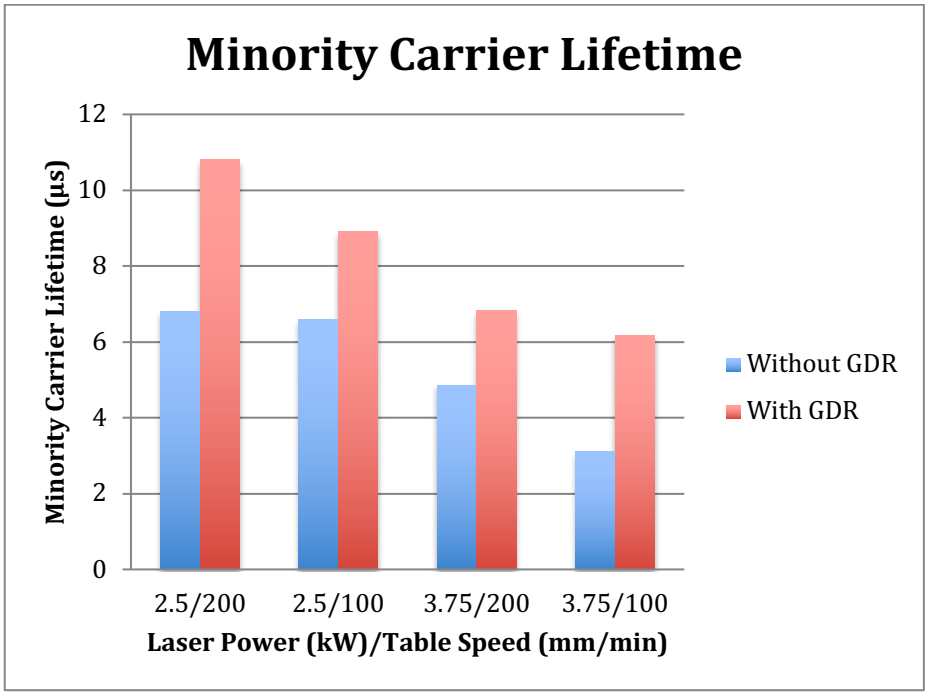


***Figure 4.14** - Chart showing minority carrier lifetime (µs) for wafers before and after an alkali groove damage removal etch*

4.2.6 Phosphorous Diffusion

Section 3.2.10 specified that a p/n junction must be created by selectively doping the deeper grooves n-type. To do this as explained in section 2.1, phosphorus atoms need to become the substitutional impurity (dopant) for a silicon atom. This requires another thermal process, diffusing phosphorus into the silicon exposed beneath the nitride ARC by the laser during the groove cutting process. To make a good ohmic contact that will be valuable in the later metallisation stages, the target sheet resistivity for the doping is less than 10 Ω/□. In order to achieve this, the furnace recipe executed undertakes a 15-minute $POCl_3$ diffusion at 930°C followed by a drive-in of 10 minutes at 950°C. When measured with a four-point probe, this process repeatedly produced a sheet resistivity of 8.89 Ω/□ (± 0.2 Ω/□).

4.2.7 Phosphorous Glass Removal

A residue of the $POCl_3$ processing is the formation of a layer of phosphorous glass above the diffused region. This glass is undesirable in the process design, as it has the effect of forming a mask on the exposed silicon within the grooves, therefore preventing the electroless plating from occurring. To remove this layer, the wafers were immersed in 7:1 hydrofluoric acid for 60 seconds and then rinsed in deionized water for 10 minutes.

4.2.8 Metallisation

The final process required for the proof of concept device is the electroless metal plating of the grooves and busbars so that an electrical connection can be made to the device. The three-stage process of nickel/copper/silver was performed following the recipes and immersion times as detailed in section 3.2.12.

Figure 4.15 is an optical micrograph of the nickel-plated grooves that have a yellowish tinge as a result of the nickel deposition. Figure 4.16 is an optical micrograph of the grooves and busbar once the copper has been deposited on top of the nickel and Figure 4.17 is an optical micrograph showing the deposited silver.

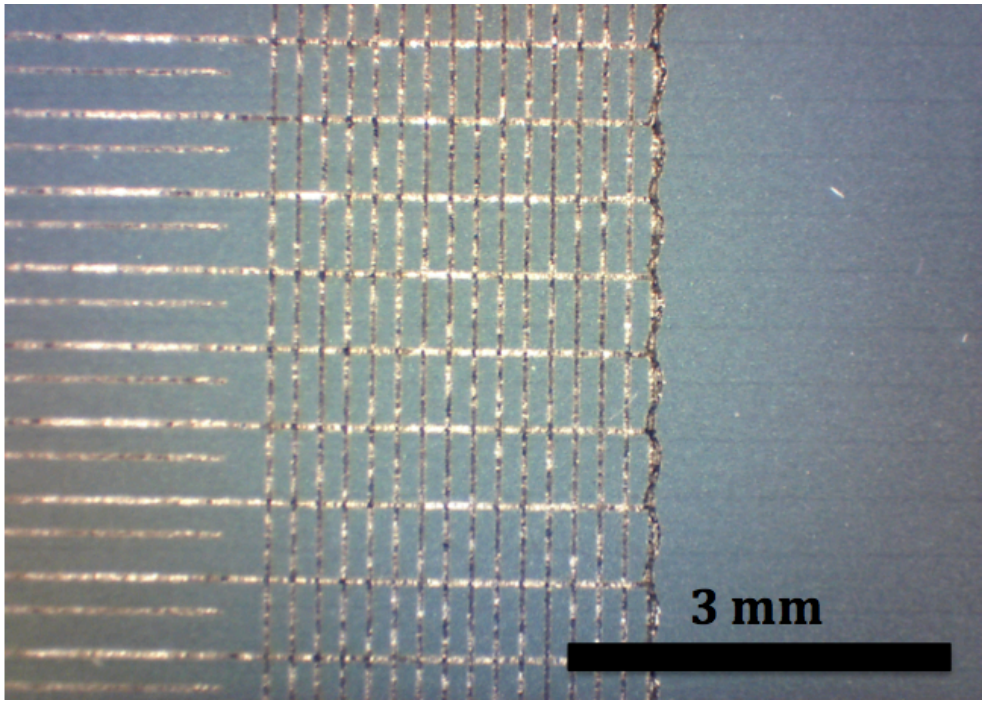


Figure 4.15 - *Optical micrograph showing yellowish nickel-plated grooves*

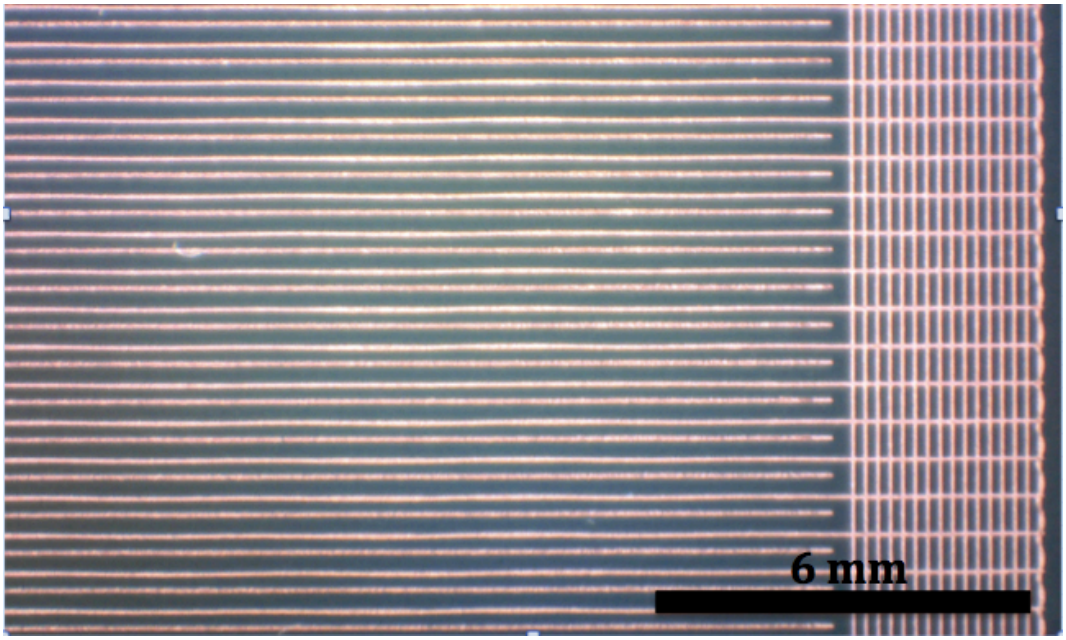


Figure 4.16 - *Optical micrograph of grooves after copper deposition*

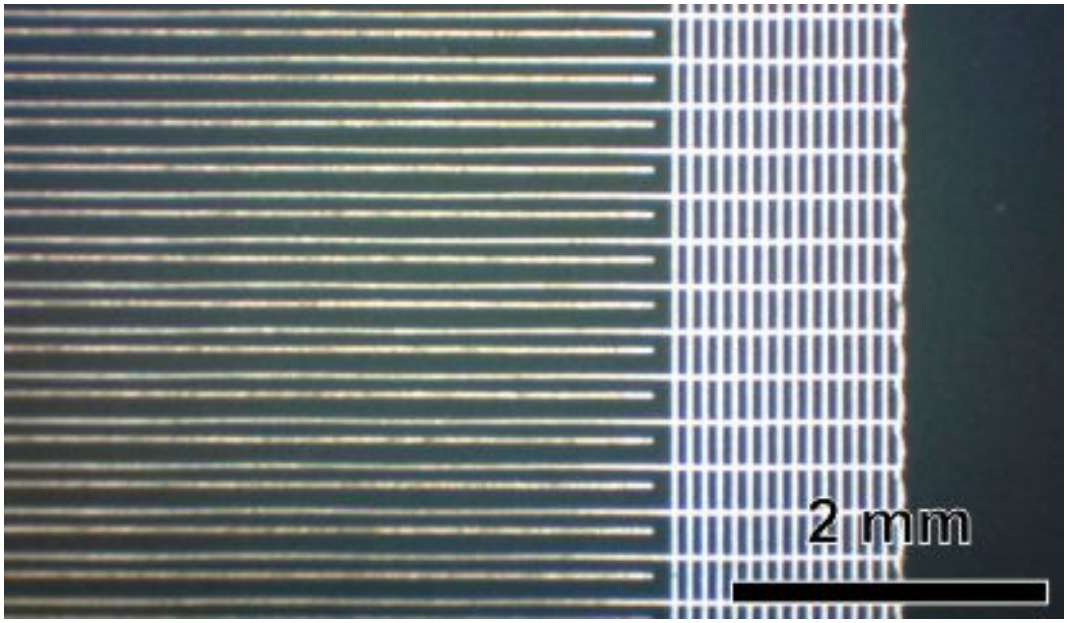
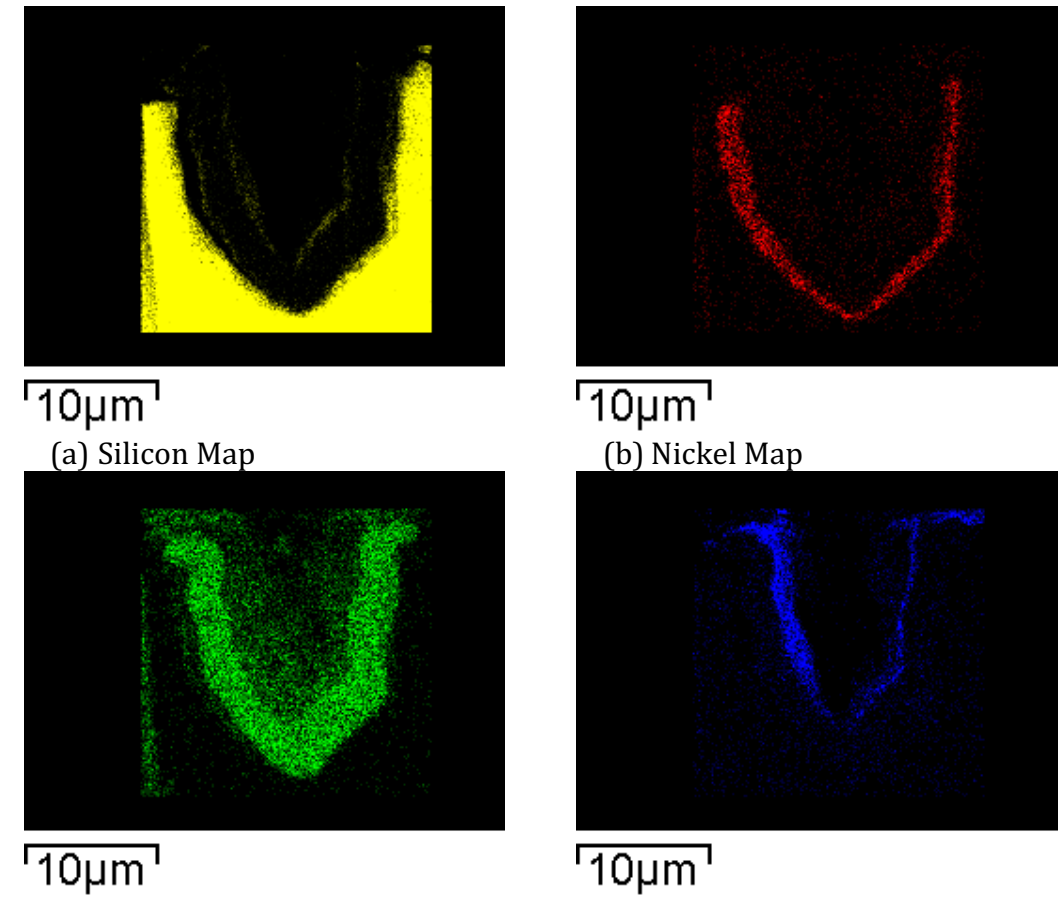


Figure 4.17 - *Optical micrograph of grooves after silver deposition*

4.2.8.1 SEM Characterisation of Shallow Groove Metallisation

Using the energy-dispersive detector (EDS) that is integrated into the SEM it is possible to identify the metal layers that have been deposited. Figure 4.18 is an EDS image of a metallised shallow groove identifying the individual elements. Note that the sample has been cleaved to reveal the cross-sectional surface and then polished flat using the FIB. The silicon substrate is identified, as are the locations of the deposited nickel (red), copper (green) and silver (blue). Figure 4.19 shows these individual images combined. EDS mapping of another groove prepared in the same way is presented in Figure 4.20, where the silicon is shown in red, nickel green and copper blue. From this it is possible to see that the metals are being laid down as anticipated, the nickel is connecting directly to the silicon and therefore creating the desired diffusion barrier. The copper is deposited on top of the nickel to act as a conducting layer and a layer of silver sits at the top of the metal stack to allow easier soldering of tabs to the busbars.



(a) Silicon Map (b) Nickel Map

(c) Copper Map (d) Silver Map

Figure 4.18 - *EDS showing the elements of a metallised shallow groove*

The images do reveal that there is some delamination of the copper meaning that the connection to the nickel is poor; with no intimate contact, the contact would fail. It is unclear whether this has occurred either during the processing itself or whilst preparing the sample for imaging. The result of this delamination would be a very high series resistance of the device.

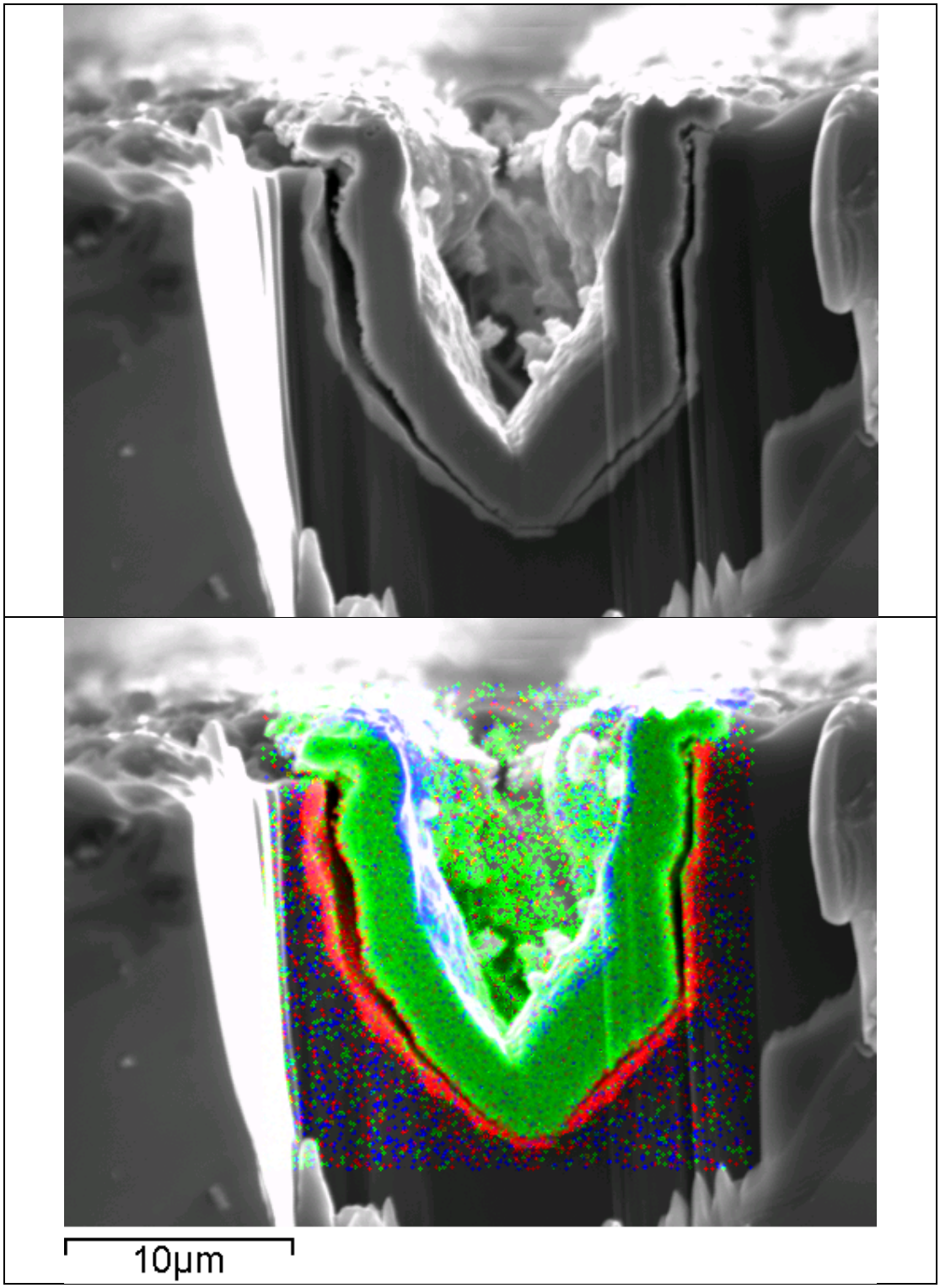


Figure 4.19 - *EDS of a metallised shallow groove with and without metals identified (nickel red, copper green, silver blue)*

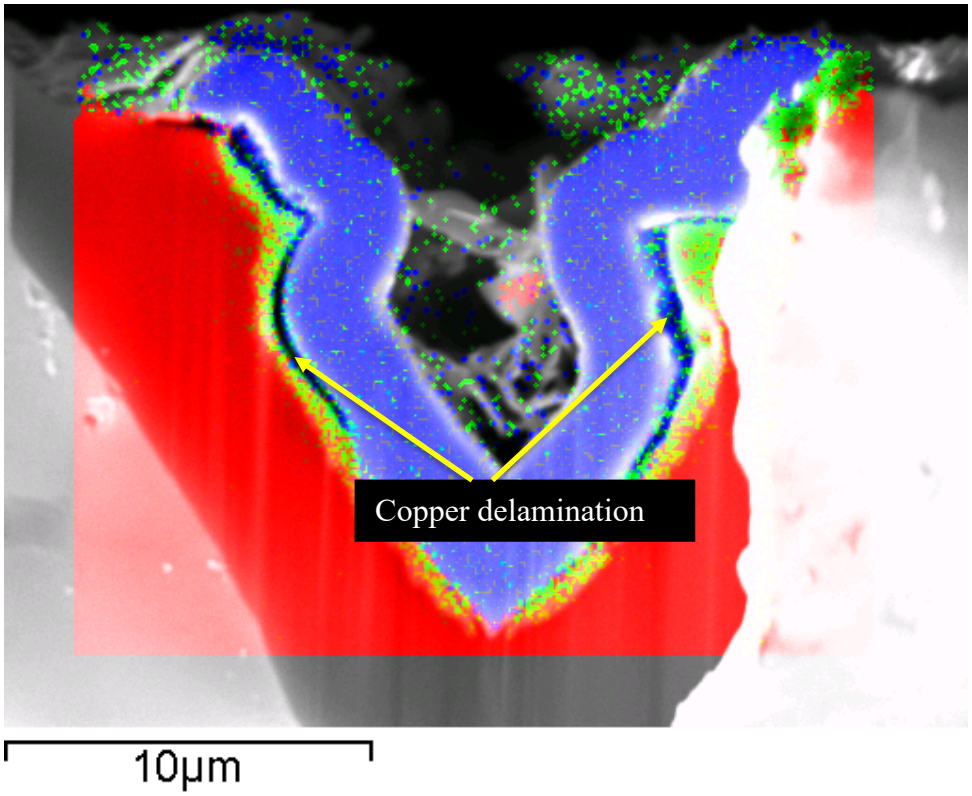


Figure 4.20 *- EDS image of shallow groove showing copper delamination (silicon red, nickel green, copper blue)*

4.2.8.2 Initial Metal Climb Out Problem

The initial fabrication attempts resulted in non-working devices due to a short circuit between the positive and negative busbars. On examination under a microscope, no obvious shorting could be seen between the fingers. However, under high power magnification it is clear to see that during the metallisation stages, in addition to plating the n-type doped grooves, metal had plated the exposed p-type silicon at the edges of these grooves. Figure 4.21 is an optical micrograph that shows the metal climbing out of the groove.

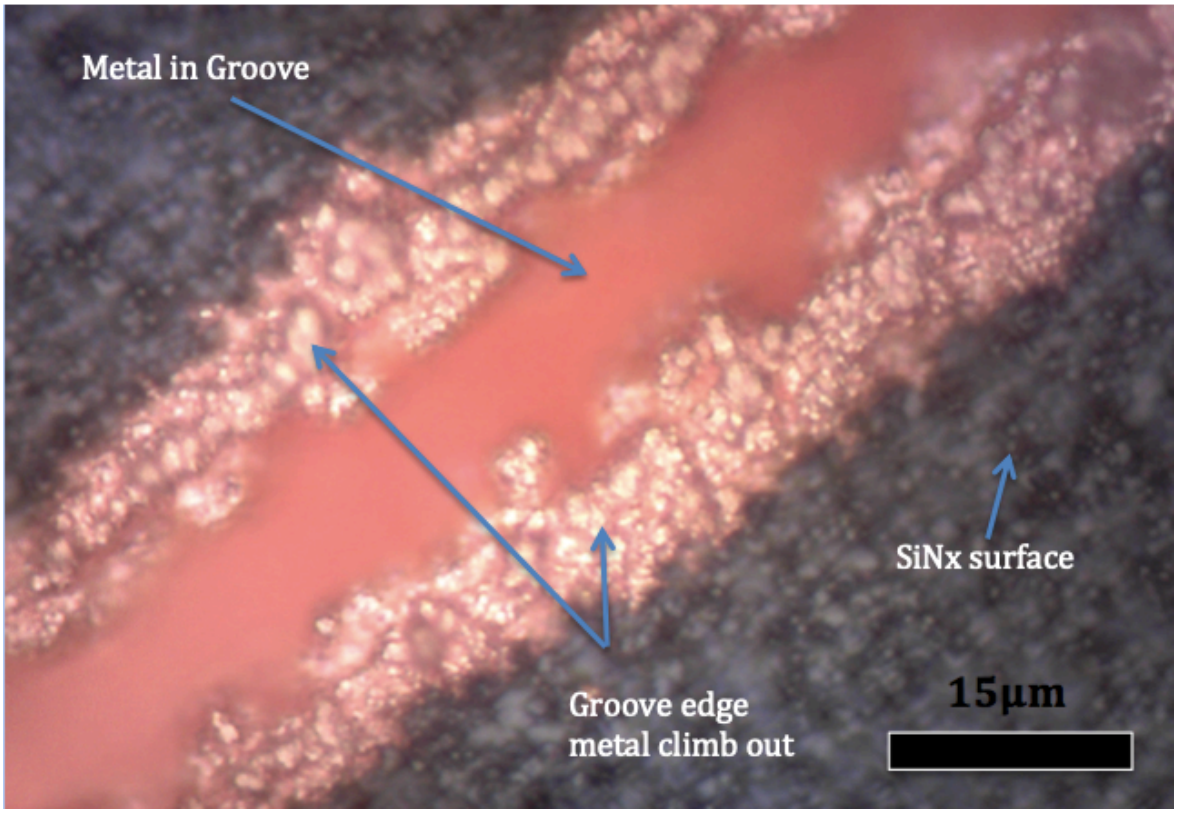


Figure 4.21 *- Optical micrograph showing metal climb out*

Whilst the groove itself is doped n-type, the surface of the silicon is still p-type, resulting in the short circuit found in the device. The reason for the unwanted plating is due to the silicon nitride protective layer being damaged during the laser processing stage. Prior to metallisation the hydrofluoric acid used in the phosphorous glass removal stage has removed the silicon oxide passivation layer at the groove edge thereby exposing the p-type silicon substrate to the metallisation process, thereby allowing both n and p type silicon to be plated and joined. A schematic of this is shown in Figure 4.22.

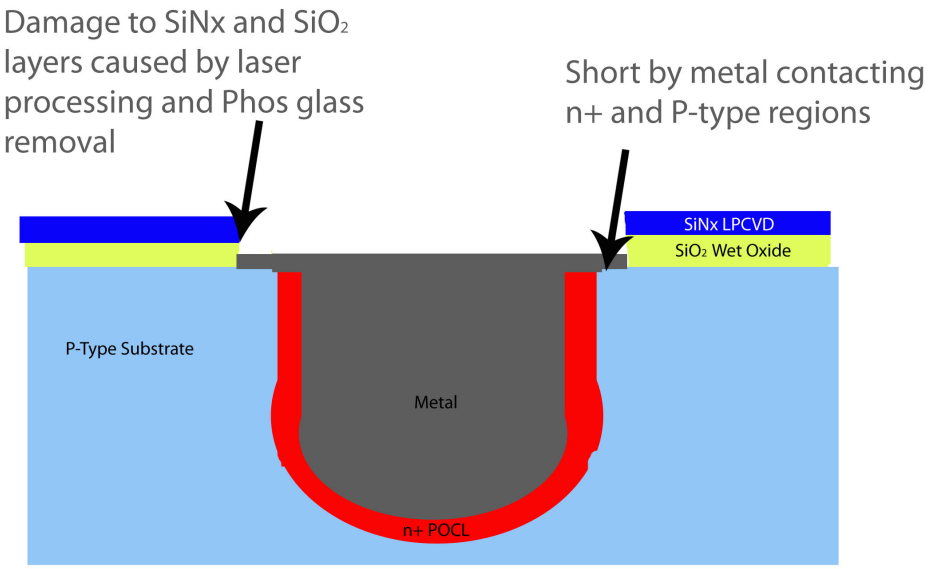


***Figure 4.22** - Diagram of how unwanted metal plating causes shorting problem*

4.2.8.3 Additional Hydrofluoric Acid Dip

An additional hydrofluoric acid dip was considered after the n-type grooves are cut and prior to the n-type diffusion process to resolve this. The additional HF dip would remove the silicon dioxide that has been exposed by the damaging of the silicon nitride layer during the laser processing. The result would leave the edges of the grooves exposed therefore also being doped n-type during the $POCl_3$ diffusion. Should the groove edges then become metallised there would be no short circuit between the p and n-type regions. Figure 4.23 is a step diagram of how an additional HF dip will resolve the shorting issue. In image B, the LPCVD SiN_x layer has been damaged in the laser grooving process exposing the underlying SiO_2 passivation layer. When the additional HF dip is performed, the exposed SiO_2 layer is cut back revealing the silicon substrate beneath it as shown in image C. This exposed silicon is then doped during the $POCl_3$ process as shown in image D so that all the areas that are in contact with the metal following metallisation are doped n-type as shown in image E.

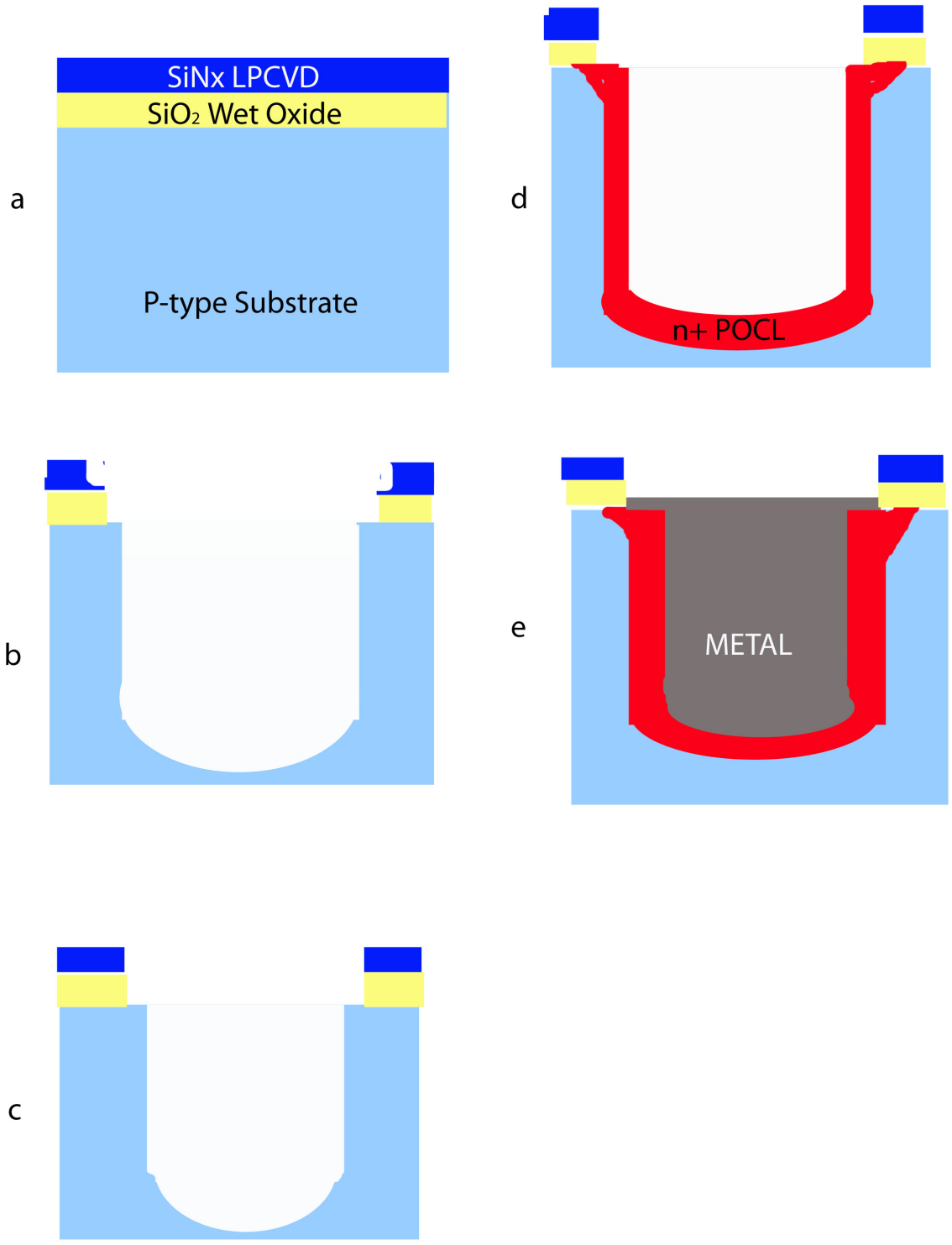


Figure 4.23 *- Step diagram of how additional HF dip overcomes shorting problem*

4.3 Revised Process Steps for Proof of Concept Device

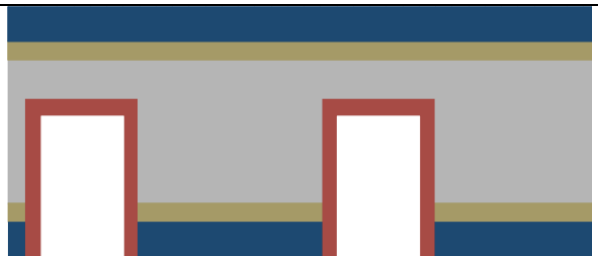
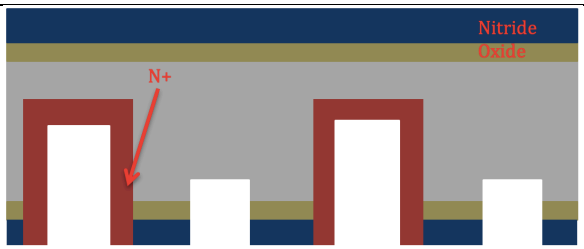
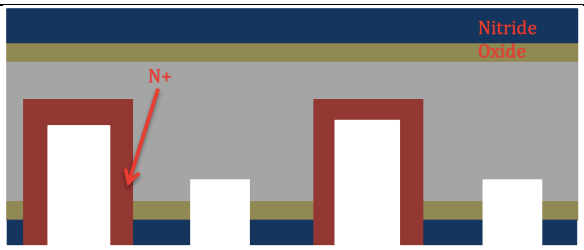
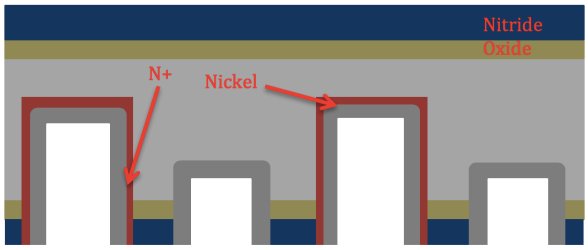
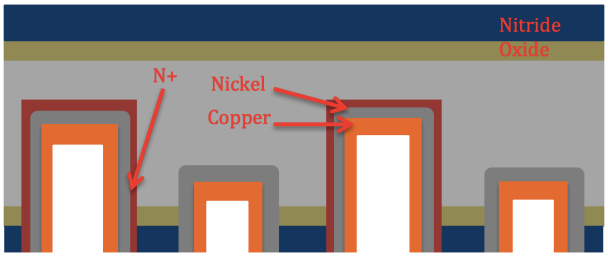
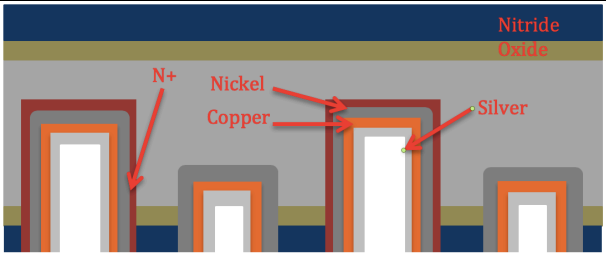
The additional steps to overcome the shorting problem can now be incorporated into the process flow for the proof of concept device, which is shown in Table 4–6.

Table 4–6 - *Updated process steps for proof of concept device*

Material Colour Legend

Colour	*Material*	*Colour*	*Material*
	Wet Silicon Oxide		Nickel
	LPCVD Silicon Nitride		Copper
	Phosphorus		Silver

#	Cross Sectional Diagram of Wafer after Process Step	Details of Process Step
1		**Saw damage removal** – 30% NaOH at 80°C for 5 mins. Followed by RCA cleaning
2		**Wet Oxidation** – 35-minute wet oxidation at 900°C followed by 15 min anneal. Target 180 nm of wet oxide
3		**LPCVD nitride deposition** – 25-minute deposition in furnace. Target 120 nm of nitride
4		**N-type groove cutting**. Deep groove program at 3.5 kW to give groove depth of 80 µm. 10% NaOH dip at 60°C for 10 minutes groove damage removal followed by additional 30 sec 7:1 HF dip

5		**$POCl_3$ Groove Diffusion** – 20-minute $POCl_3$ diffusion at 930°C followed by a 10-minute drive in at 950°C to give sheet resistivity of 10 Ω/□
6		**P-type groove cutting**. Shallow groove program at 2.5 kW to give groove depth of 30 µm. 10% NaOH dip at 60°C for 10 minutes groove damage removal
7		**Phosphorous Glass Removal** – 60 second dip in 10% hydrofluoric acid to remove phosphorous oxide (glass) deposited during $POCl_3$ diffusion
8		**Nickel Deposition** – Enthone AL100 process run at 60°C for 60 seconds followed by 10-minute sinter at 400°C and activation by 2-minute dip in 20:1 hydrochloric acid at room temperature
9		**Copper Deposition** – Enthone CU240 process run at 50°C for 60 minutes
10		**Silver Deposition** – Enthone AG410 process, 30 second predip at 40°C followed by 2-minute plating dip at 50°C

4.4 Proof of Concept Device Results

The working device that was fabricated for the proof of concept was then characterised using a solar simulator as outlined in section 3.4.6. For this the current is measured as the voltage is swept from -1 to 1 volt. These results are then plotted to show the initial device IV curve in Figure 4.24. The objective of this experiment was to prove that using the proposed novel device geometry of this project, a working device could be made.

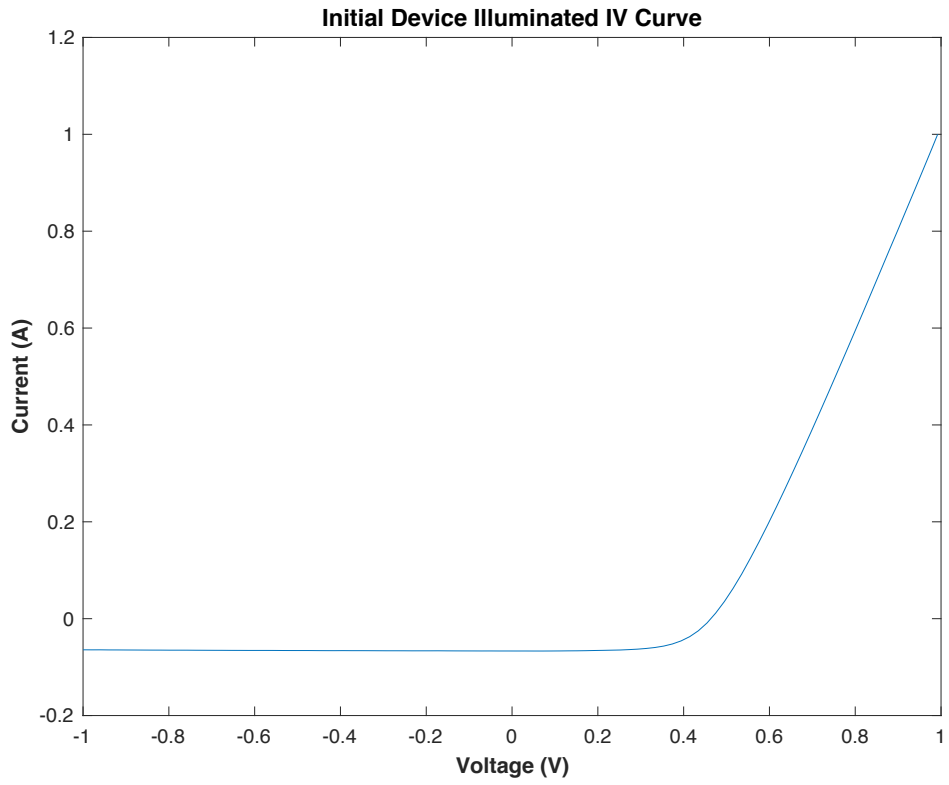


Figure 4.24 - *Initial device illuminated IV curve*

The IV curve plotted from measuring the initial device as shown in Figure 4.24 is that of a diode which is what would be expected in the case of a working device, so this initial experiment has proved that working devices can be fabricated using the proposed novel device geometry. From Figure 4.25, values can be extrapolated for open circuit voltage (V_{OC}), short circuit current (I_{SC}), maximum power point (MPP)

and fill factor (FF). From this the short circuit current density (J_{SC}) and device efficiency can be calculated using the formulae from section 2.1. These values are shown below in Table 4–7.

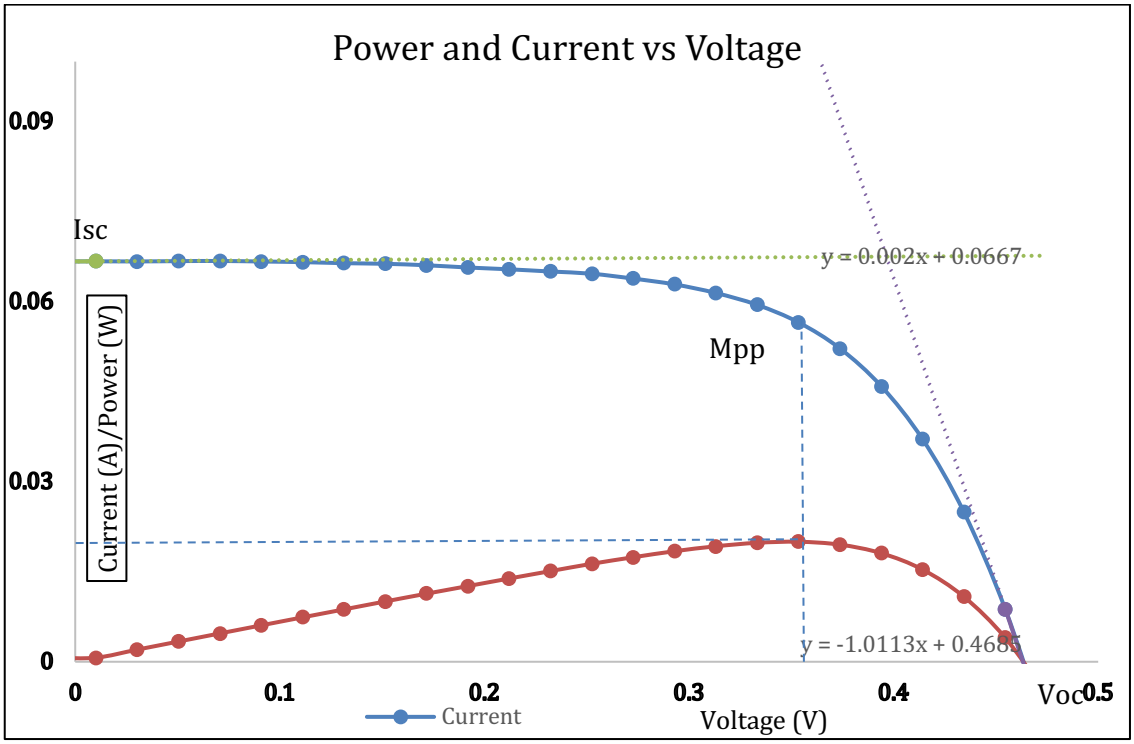


***Figure 4.25** - Initial device IV and PV curves*

Also from the equations in section 2.1 it is proven that approximations for the parasitic resistances can be derived from Figure 4.25 given the surface area of the device is 20 cm^2. The series resistance (R_s) is approximated as the inverse of the slope of the IV curve close to V_{OC}, which from Figure 4.25 is:

$$y = -1.0113x + 0.4685 \tag{4.2}$$

The gradient of the line is 1.0113 therefore $R_s \approx 0.99\Omega \times 20cm^2 \approx 19.8\Omega\ cm^2$

Similarly, the shunt resistance (R_{sh}) is approximated as the inverse of the slope of the IV curve close to I_{SC}, which from Figure 4.25 is:

$$y = 0.002x + 0.0667 \tag{4.3}$$

The gradient of the line is 0.002 therefore $R_{sh} \approx 500\ \Omega \times 20\ cm^2 \approx 10000\ \Omega\ cm^2$

Table 4–7 – *Initial device characteristics*

V_{OC} (V)	0.475	MPP (mW)	20.0
I_{SC} (mA)	**66.7**	**J_{SC} (mA/cm^2)**	**3.34**
FF	**0.631**	**Efficiency (%)**	**1.00**
R_s (Ω cm^2)	**19.8**	**R_{sh}** (Ω cm^2)	**10000**

4.5 Initial Device Fabrication Summary

The primary objective of this initial device was to prove that a working solar cell can be fabricated using the novel geometry proposed by this project. As such the actual fabricated device was put together in a crude form with no process optimisation and with several known enhancements discussed in Chapter 2 and Chapter 3 (such as surface texturing) omitted. When considered like this, the initial device has successfully proved its aim, in that with this device geometry, a working solar cell can be fabricated.

The main overall aim of the project however is to create a high efficiency solar cell. This is where this initial device falls short, the low V_{OC} of 0.475V and low I_{SC} of 66.7 mA gives a device efficiency of 1.00%, which does not meet the aims, nor objectives of the project. There are some encouraging elements though, the fill factor of 0.631 is reasonable, and the shunt resistance of 10000 Ω cm^2 is very good. The series resistance of 19.8 Ω cm^2 however is particularly high, typically for a device it should be 0.5-1.3 Ω cm^2. This may be explained by the delamination of the copper leading to a poor contact between the metal and silicon as shown in Figure 4.20.

In Chapter 5 the success of the initial device will be built upon, using computer modelling to look at ways to take the now proven working device and improve the efficiency of it so as to meet the original aims of the project.

Chapter 5 Optical and Electrical Modelling

5.1 Introduction

When building a semiconductor device such as a PV cell, there are many variables to consider when designing, building and then putting these devices into production. To try these processes experimentally in the laboratory is costly both in terms of resources and time.

In order to give an initial starting point for experimental parameters, device concepts are often modelled on a computer. A modelling suite can be used to replicate the device geometry and then simulate the optical, thermal and electrical behaviour for the device. This allows for the initial design to be fabricated using parameters that are expected to be in a range that will yield good results. These initial simulation sweeps to find these parameter regions can be done at a fraction of the time and cost that it would have taken to perform by experimental fabrication.

Another very useful element of modelling is that it gives a base line to reference against when measuring fabricated devices. If the device results are drastically different from the modelled results, further investigations into the fabrication process can be done.

Once a device is working in line with the expected model, the model can further used to optimise the device design. Modelling also has an important role to play in the move from lab concept to full scale manufacturing. The building, setup and commissioning of a semiconductor fabrication plant is a very costly process. Modelling means that the effect of the resultant output from different types of

machines can be predicted so only the correct machines will be selected in the setup of the production facility.

This chapter will first present the use of an online modelling tool to optimize the antireflective coating for the solar cell. It will then present a Technology Computer Aided Design (TCAD) model that has been built to represent the device that this project is proposing to fabricate.

5.2 Anti-Reflective Coating (ARC) Modelling Method

In order to get the most efficient device possible, the absorption of light (light trapping) into the bulk is an important feature. OPAL2, [134] which is free to use and available from www.pvlighthouse.com.au, is an online simulation tool with a user-friendly graphical user interface. This allows the simulation of the front surface reflectance and absorption to be done for a variety of different surface films over a range of light wavelengths [135]. OPAL2 also allows a variety of different surface textures to be modelled, including random pyramids and inverted pyramids which allow the results to be more useful. For this project, OPAL2 was used to simulate and optimize the thickness of the oxide/nitride stack used for the ARC. OPAL2 uses a combination of transfer matrix method (TMM) and ray tracing to allow the light transmission and reflectance to be calculated as it passes through the different films deposited on planar or textured silicon surfaces. There are numerous and varied methods available for calculating light reflectance and transmission in silicon and thin films associated with silicon. As a result, there are plenty of resources available where these different methods have been researched and explained [136] [137].

5.2.1 Transfer Matrix Method (TMM)

How light is reflected and transmitted at an interface between two different media (e.g. air and silicon) can be described by the Fresnel equations. In PV applications however, there are often multiple interfaces such as oxide/nitride ARC stacks on top of the silicon bulk. In these situations, each interface transmits and reflects light into adjacent media which can have both constructive and destructive effects.

In this situation, Maxwell's equations can be applied assuming that there are simple continuity conditions for the electric field across the interface of one medium to the next. This was proposed by following a model used for transmission lines and the analogy was formalised through the transmission line Telegraph Equations for analysis of thin film optical filters [138]. If the electric field is known as the light enters a medium, then the electric field as the light exits the medium can be resolved using the transfer matrix method (TMM) proposed by Abelès [139]. This allows the reflectance and transmittance of multilayer thin films to be calculated taking the effect of differing mediums upon each other into consideration.

5.2.2 Ray Tracing

Ray tracing uses a series of mathematical formulae that allow for the path of a single ray of light to be calculated as it passes through a series of different media with differing properties of transmission and reflectance. The basic principles of the most commonly used algorithm for this where published in 1962 by Spencer and Murty [140]. Ray tracing is used in a wide variety of applications such as camera lens design, but it can also be used to model the path of the light as it strikes a solar cell.

5.3 OPAL2 Modelling for Antireflective Coating (ARC) Optimisation

Built into the database of OPAL2 is a large library of refractive indexes (n) and extinction coefficients (k), although a user can upload their own values if they are using films that are drastically different from any of the provided ones. For the simulations required for this project, the LPCVD nitride deposited experimentally is similar to the LPCVD nitride used by McIntosh et al[141] which available in the OPAL2 libraries.

By inputting the thermal oxide/LPCVD nitride stack into the OPAL2 interface, the thickness of each layer can be altered, and the simulation will calculate the photon current absorbed into the substrate (J_G in mA/cm^2). This allows the optimal thicknesses to be determined.

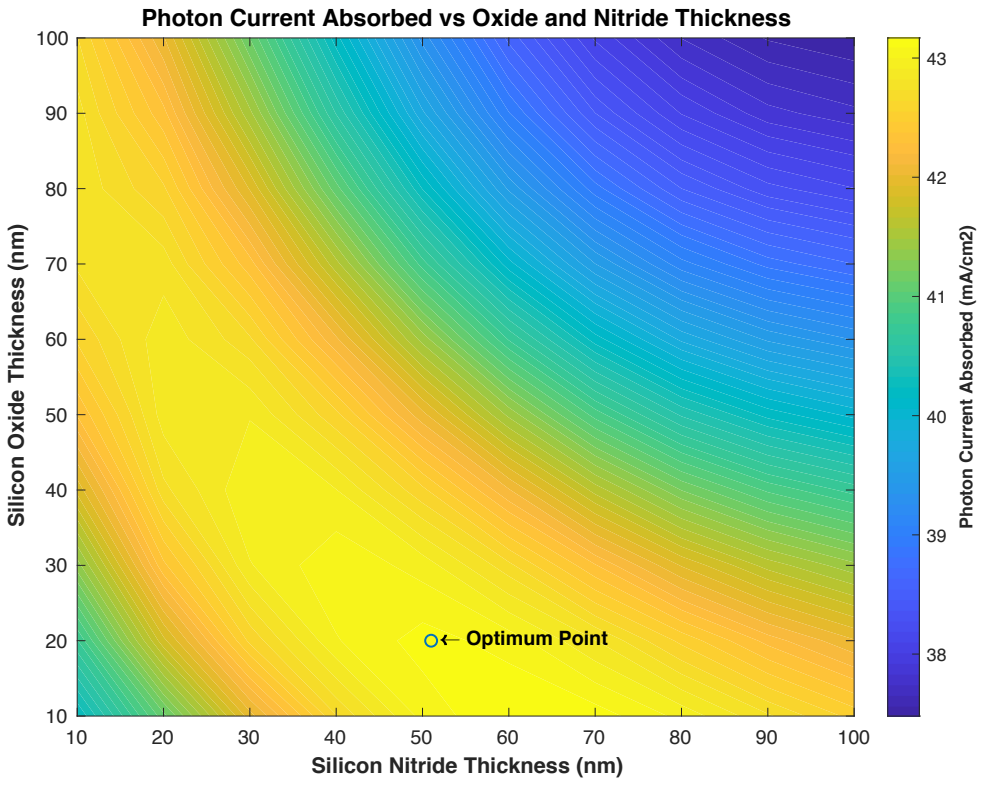


Figure 5.1 *- Contour plot showing absorbed photon current vs. film thicknesses*

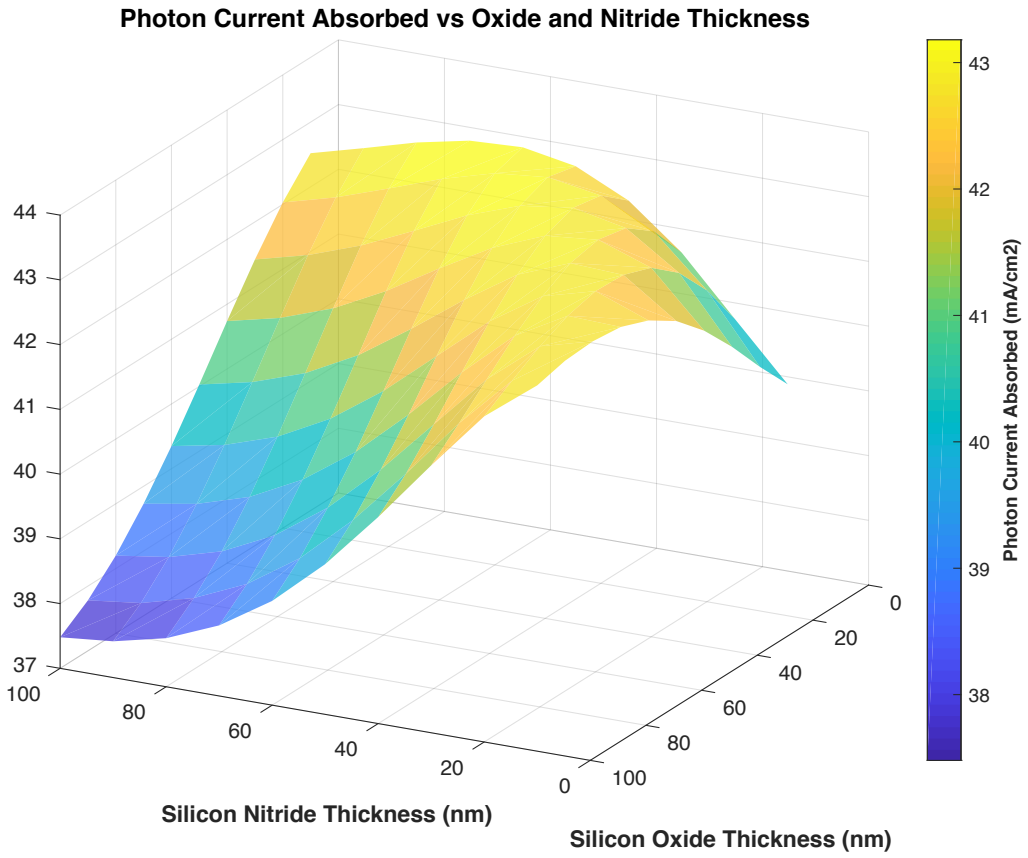


Figure 5.2 - *Surface plot showing absorbed photon current vs. film thicknesses*

Figure 5.1 and Figure 5.2 show graphically the results that the OPAL2 modelling produces when the thicknesses of the oxide and nitride layers are varied. If the films are too thin, then the photon current absorption is not optimal, and the same happens if the films are too thick. The silicon dioxide film serves as the passivation layer for the front surface as well as being part of the anti-reflective coating stack. Section 2.3 discusses the importance of good surface passivation leading to lower SRVs. In order to get as good a passivation layers as possible, the passivating film (in this case silicon dioxide) should be a reasonable thickness. From Figure 5.1 and Figure 5.2, it can be seen that thicknesses of oxide above ~20 nm result in a fall in the absorbed photo current, therefore 20 nm was chosen as the optimum thickness for the oxide layer.

By keeping the oxide thickness constant at 20nm, only the thickness of the nitride needs to be varied in the OPAL2 simulations. Figure 5.3 shows this simulation over a smaller area as identified from Figure 5.1.

***Table 5–1** - Optimised values for antireflective coating oxide and nitride thicknesses*

Oxide Thickness (nm)	20	**% Photon Current Reflected (mA/cm^2)**	2.0
Nitride Thickness (nm)	51	**% Photon Current Absorbed (mA/cm^2)**	98.0

With the range narrowed down, and the number of variables reduced, the built-in optimization tool in OPAL2 can be used to optimise the target values for the thickness of the front surface films. For all these simulations, the front surface morphology was modelled as being both planar and with random upright pyramids with a crystal plane angle (ω) of 54.74° (from section 3.2.4). These results are also shown in Figure 5.3, which, shows that by texturing the front surface of the wafers, far more light can be absorbed by the substrate. The optimised results are presented in Table 5–1.

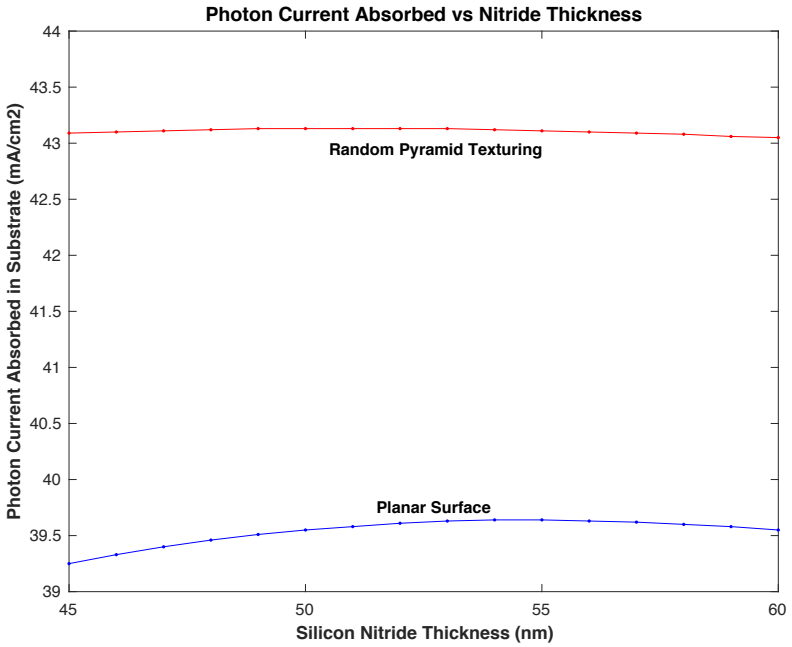


***Figure 5.3** – Graph of absorbed photon current vs nitride thickness.*

5.4 Device Modelling Package Selection

Modelling of semiconductor devices is a well-established and researched field. There are several different modelling packages that can be used to model PV devices each with their merits and drawbacks. This section will give an overview of a few of the modelling packages that were considered to see if they were suitable for use in this project. The modelling work presented in this chapter was carried out in collaboration with Dr Tasmiat Rahman of the University of Southampton.

5.4.1 Quokka

Quokka is a free and fast 3-dimensional simplified solar cell simulation program developed by Andreas Fell and available for use online at www.pvlighthouse.com.au. Quokka presents itself as a web-based GUI into which parameters are entered and a MATLAB code is subsequently generated which when run performs the desired simulation. Quokka uses the general set of semiconductor equations, namely a transport equation for minority and majority carriers and Poisson's equation for potential [142]. The modelling package builds on the ideas of Brendal who proposed a simplified method by treating the dopant-diffused layers as conductive boundaries [143]. This then negates the need to solve equations in the diffused regions and therefore the space-charge region. The package also applies the equality of excess carrier densities, also known as the quasi-neutrality condition, to the areas outside the space-charge region, building on the ideas of Kleinman [144]. The Quokka model accounts for non-ideal recombination currents at the boundaries and recombination losses in the emitter and is enhanced by contact resistance effects [142]. Quokka uses boundaries conditions as opposed to meshed regions to represent emitters, back

surface fields and metallised areas. This significantly reduces the amount of simulation time required, as there are fewer equations to solve due to the low number of points to solve for. This however is also the main limitation of Quokka. Because of the simplification of the way that conductive boundaries are treated, if the J_0 value of a doped region cannot be approximately accounted for then the Quokka modelling package cannot be used.

5.4.2 PC1D and PC2D

PC1D is another free-to-use modelling package that is widely used in the modelling of solar cells [145]. As the name suggests, PC1D can only model in 1-dimension which is not suitable for the application desired by this project due to the interdigitation of n and p contacts on the back surface. Similar to Quokka, by using Brendal's proposed method of treating dopant diffused layers as conductive boundaries [143] a 2-dimensional model can be numerically replicated for simulation, extending the PC1D package to become the PC2D modelling package [146]. PC2D is a simple to use circular-reference solar cell device simulator that works entirely within Microsoft Excel. The simulator uses a mesh approach to build the device structure with small mesh elements (20x20). The limitations of PC2D are its inflexible meshing, low computational speed and the fact that it is limited to 2-dimensional models only [142].

5.4.3 CoBoGUI

CoBoGUI is a script collection that allows for simplified 2-dimensional modelling of solar cells in a similar way to PC2D. CoBoGUI was developed at the Institute for Solar Energy Research in Hamelin (ISFH) and whilst the source code is freely available, it requires a COMSOL Multiphysics license to be able to run it and knowledge of the COMSOL Multiphysics finite element analysis platform [142].

5.4.4 SCAPS

SCAPS-1D (Solar Cell Capacitance Simulator) is a 1-dimensional solar cell simulation program that was developed at the University of Gent in the mid-1990s [147]. SCAPS was originally designed to be a numerical modelling program that can solve the solar cell parameters for thin film and multi-layer solar cells (e.g. CdTe and $CuInSe_2$). Subsequent developments have allowed SCAPS to be applicable to crystalline solar cells too.

The simulator works by solving the basic semiconductor equations, namely the Poisson equation relating the charge to the electrostatic potential, and the continuity equations for holes and electrons [148]. It can be used to model devices under a variety of different light spectra including AM1.5G.

SCAPS is an easy to use simulator that runs as a Windows based application program on a PC. SCAPS is freely available to the PV research community, however as already stated it can only be used for 1-dimensional device modelling.

5.4.5 Silvaco Atlas

Atlas by Silvaco is a 2-dimensional and 3-dimensional device simulator that performs AC, DC, and transient analysis for silicon devices [149]. Atlas enables the characterization and optimization of semiconductor devices. Unlike the modelling packages already looked at, Atlas is designed for modelling a wide range of semiconductor devices, not just photovoltaics. The Atlas framework is a powerful modelling tool that predicts the electrical characteristics of physical structures by simulating the transport of carriers through a 2-dimensional grid [150]. The structure is defined by mesh elements that are assigned to form regions, which can be used to replicate electrode locations, doped regions and passivation layers. An optical file is

also required for an accurate simulation that determines the transmission and reflection of light as it passes through the ARC and silicon.

Atlas is not a free simulation package and requires a licence to be able to use it. It also requires a working knowledge of the package in order to be able to extract accurate results out of it.

5.4.6 Sentaurus TCAD

Sentaurus TCAD is a very powerful simulation tool commonly used across the semiconductor industry and is used for both 2-dimensional and 3-dimensional device physics simulations without major simplifications [142]. Sentaurus was originally designed for simulating field-effect transistors (FETs) but was then discovered to be excellent for simulating PV devices. The structural device editor within the Sentaurus package is used to generate the device geometry for modelling. The elegance of the structural device editor is that the model is built using a polygon mesh, each element of which can be given different parameters. Due to their ability to tessellate, polygons are used as opposed to squares, which allows device geometries to be modelled with a greater accuracy. Differential equations are then applied to each of the mesh elements describing their electrical potential and carrier distributions. These are solved by the simulation package, which also uses a number solver to repeatedly iterate until a solution converges to a given accuracy. In a solar cell model, the major points of interest are the areas where the silicon mesh element interfaces with mesh elements with different parameters, (e.g. air, passivation films, doped regions and metals). To reflect this, the model can be designed with different sized mesh elements when it is built. At the different mesh element interfaces the mesh is fine, allowing for more accurate simulation data to be generated. As the distance from a differing mesh

interface increases, the size of the mesh exponentially grows. The starting size of the mesh, and rate of expansion of it are the definable parameters.

Sentaurus is a standalone application that needs a costly operating license to run. It also requires a large computing resource to operate in addition to detailed working knowledge on how to build device structures and run simulations using it.

5.4.7 Summary

Following the review of available device modelling tools, to finalise which one is most suitable to be used for this project, the following three factors were taken into consideration:

1. Is the package suitable for modelling the device?
2. Is that package available for use in this project?
3. Are the required skillsets and resources available to use the package?

A modelling package that is widely used within industry already is desired so that there is continuity should any of the research within this project be considered for industrial take-up. Of the considered packages only Atlas and Sentaurus meet this first consideration, although both packages require licenses and a substantial knowledge base. At the University of Southampton, there are already licenses for both Atlas and Sentaurus as well as a Linux computing cluster on which to run them. The most commonly used modelling package industrially of these two packages is Sentaurus TCAD. There are many publications where Sentaurus has been used for a wide range of semiconductor devices from MOSFETs [151] and bipolar transistors [152] to traditional solar cell process development [153] [154] and IBC solar cells[155]. Because of the history of Sentaurus TCAD being used to build comprehensive models that yield high accuracy results in literature over a long period of time, this is the modelling package that will be used for these simulations.

Dr Tasmiat Rahman, an expert user of Sentaurus TCAD, collaborated on modelling for this project, bringing his detailed knowledge of setting up and running TCAD models in Sentaurus.

5.5 Sentaurus TCAD Model

For this project, for the reasons outlined in section 5.4.7, the Sentaurus TCAD package was chosen to model the device. The Sentaurus package consists of several tools, and for the modelling of this device the following tools where used:

- *Workbench* – is a graphical user interface in the Sentaurus suite that allows the user to create, manage, execute and analyze TCAD simulations.
- *Structural Device Editor* – (SDE) is the tool in the Sentaurus suite in which the geometry of a device is defined. Both 2-dimensional and 3-dimensional structures can be defined using this tool.
- *Sentaurus Device* – (SDEVICE) is an advanced multidimensional device simulator that can simulate electrical, thermal and optical characteristics of silicon-based and compound-semiconductor devices.
- *Sentaurus Visual* – (SVISUAL) is an advanced visualisation tool for TCAD data. It includes the capability to plot X-Y data of both 2-dimensional and 3-dimensional TCAD structures and allows for interactive manipulation of the plots.

5.5.1 Meshing

In order to create a structure in SDE, a mesh must be set up. Sentaurus TCAD includes three different mesh generators which suit different device geometries and meshing strategies [156].

- *Mesh* – is the most basic of the mesh generators, it allows axis-aligned (rectangular) mesh elements which are simpler to create but offer fewer options for grid refinement which must all be done manually if required.
- *SNMesh* – is a more advanced axis-aligned mesh generator, which allows for user defined adaptive meshing (e.g. enables finer meshing at region boundaries and surfaces).
- *NOffset* – is most suited for devices where the main surfaces are not axis-aligned or curved. In this generator, offsetting material surfaces and boundaries produces meshes based on specified grid densities and offset distances. Any remaining areas are filled with either triangular or tetrahedral mesh elements.

For this project the surfaces can be considered as axis-aligned, and in order to speed up the simulation time and reduce the computing resources needed to perform simulations, an adaptive mesh with finer meshing at surfaces and region boundaries is preferable meaning SNMesh is the ideal mesh generator to use.

The model assumes that there is a gas region surrounding the device, which replicates the conditions that a fabricated cell would be tested under in a laboratory. At the interface between the silicon and gas, there are two factors that the model needs to take into consideration: the anti-reflective coating (ARC) and the surface recombination velocities (SRV). At the interface between the silicon and metal, only the SRV for these mesh elements is defined. For the doped silicon mesh elements, a Gaussian doping profile is used which can be defined within the model. The meshing strategy employed means that the model has a finer mesh at these points of interest.

In a 3D Sentaurus model, both ray tracing and the TMM are also used in simulation to model the path of light into the device. The simulation solves for each mesh interface as the ray strikes it.

5.6 Structural Device Editor 3-Dimensional Device Design

The structural device editor (SDE) tool in the Sentaurus package is used to define the geometric shape of the device. Figure 5.4 shows a sketch of the proposed device geometry that this model will replicate.

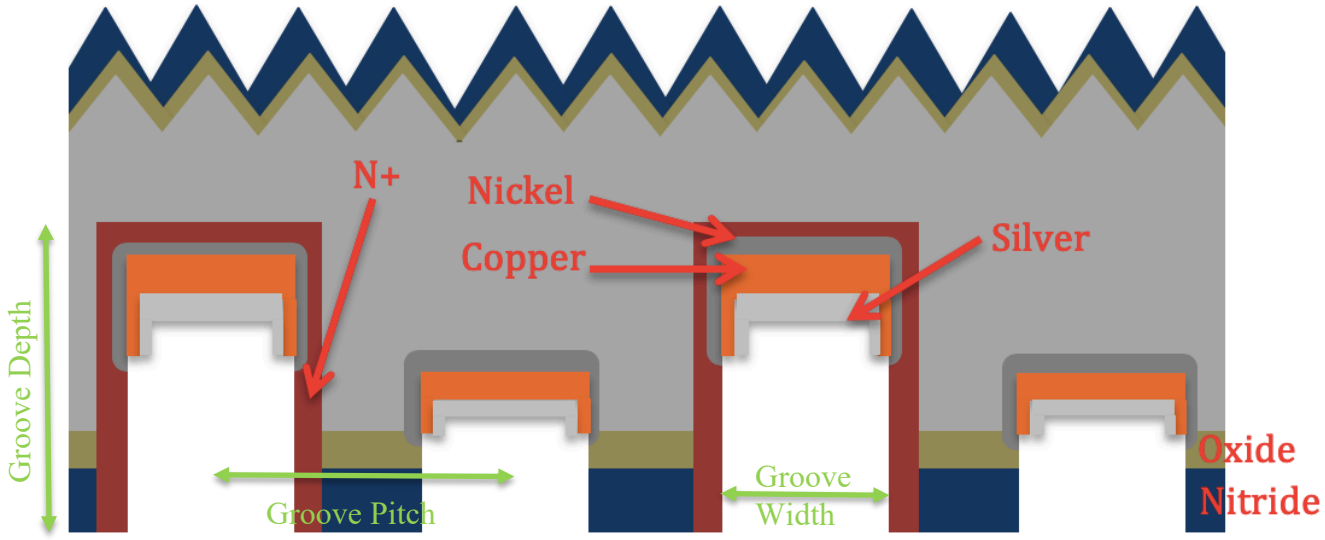


Figure 5.4 - *Diagram of proposed device geometry*

In order to reduce simulation times, the proposed device is simplified down to the smallest common building block whose repetition can be used to replicate the entire device. This is known as the unit cell, Figure 5.5 shows the starting unit cell used in this model before any optimisation or investigative sweeps were done to enhance it.

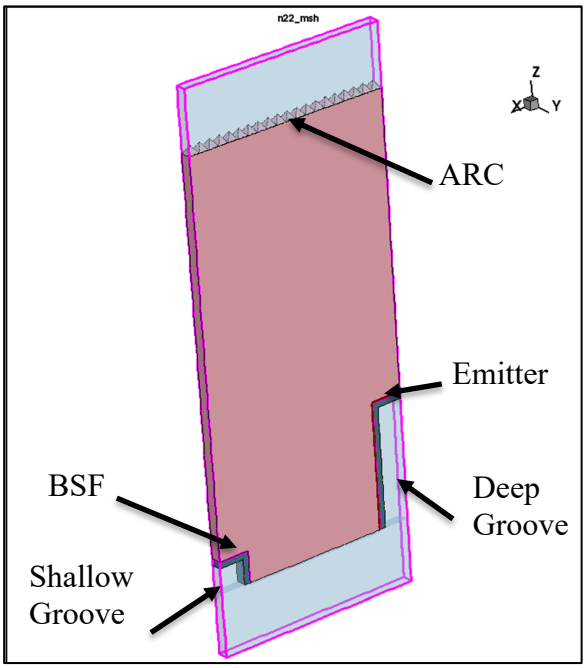


Figure 5.5 – *Basic geometry design of the 3D unit cell*

In this unit cell visualisation, the deep and shallow grooves can easily be seen, along with doped region within them, the bulk material and the surface texturing. Figure 5.6 shows the same unit cell, but with the meshing strategy superimposed.

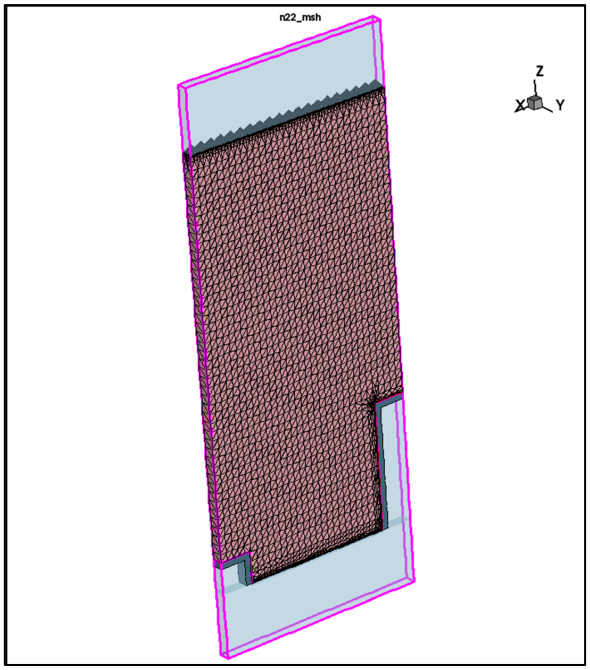


Figure 5.6 – *Unoptimised 3D unit cell showing meshing strategy*

The adaptive meshing discussed in section 5.5.1 is clearer in Figure 5.7 which is a magnified picture of the front surface of the unit cell.

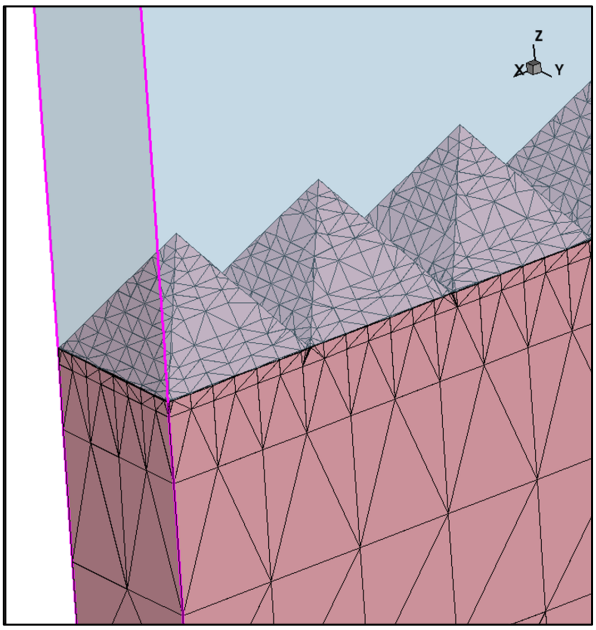


Figure 5.7 – *Front surface showing 3D pyramids and interface meshing strategy*

At the interface between the device and the air, the meshing is fine, leading to many more mesh points that must be solved. Moving away from this interface, the meshing becomes coarser which allows the simulation to run faster.

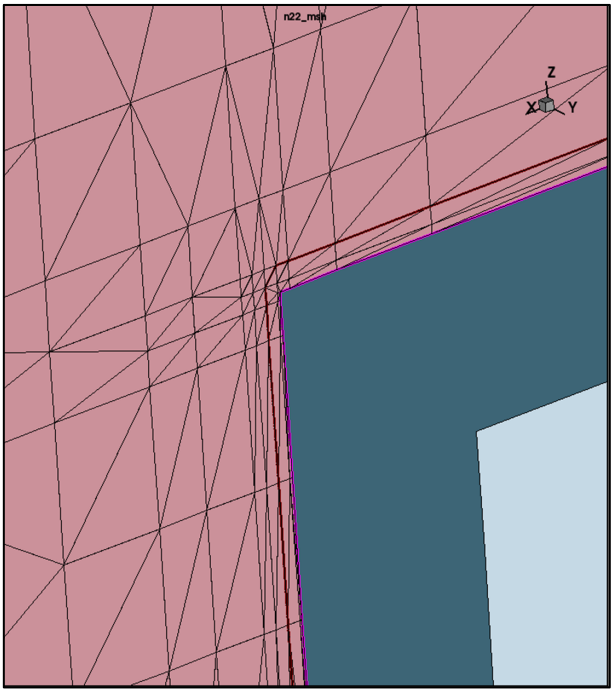


Figure 5.8 – *3D meshing strategy at the interface between silicon and metal*

This is also true at the interface between the silicon and the metal, as shown in Figure 5.8 which depicts the silicon interface in a deep groove.

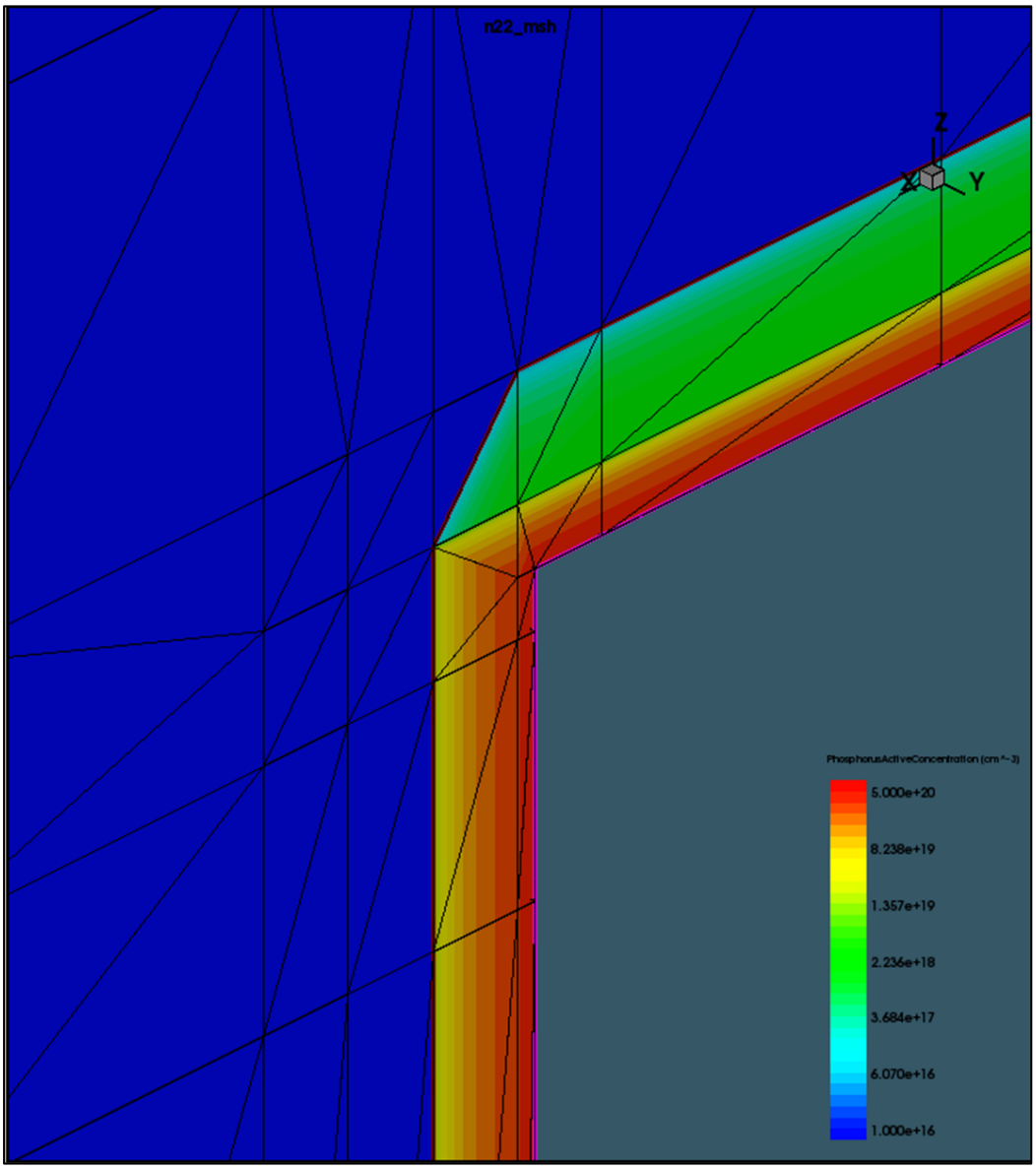


Figure 5.9 – *Phosphorous doping profile in 3D model*

The deep grooves are doped with phosphorous to create an emitter. This doping is also recreated in the TCAD model as a Gaussian doping profile, as shown graphically in Figure 5.9. The final parameter that must be defined in the model is the carrier generation profile. It is assumed in this model that there is no light entering the device from the back side, so the only surface that the light strikes is the top surface.

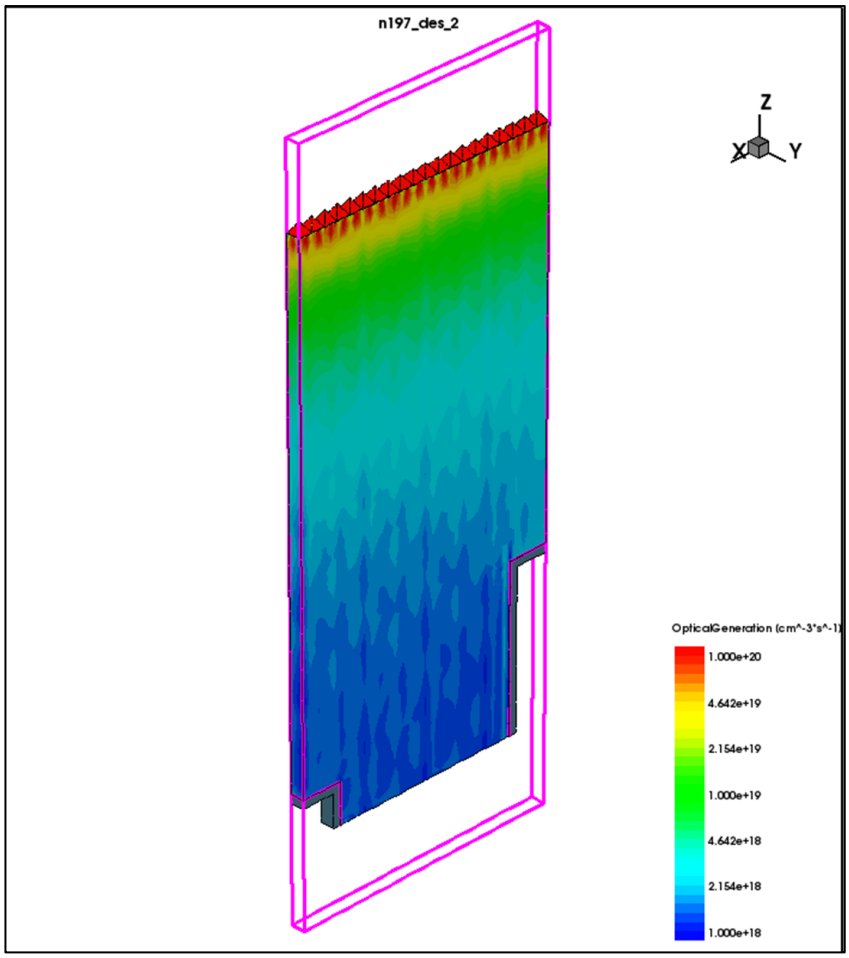


Figure 5.10 – *3D unit cell showing carrier generation profile*

Figure 5.10 is a graphical representation of the carrier generation profile. As described, the greatest concentration of generated carriers is at the front surface. Moving away from the surface, this reduces as the intensity of light remaining is reduced, although there is an assumption that there is some reflection off the deposited metal, which is also shown in the diagram.

5.6.1 3-Dimensional Model Convergence

A 3-dimensional model will give the most accurate results when it comes to simulating a 3-dimensional device. However, a 3D model will take a lot longer to run, to the extent where it may take longer to run the model than it would to experimentally create the device. In this scenario, the model would need to be adjusted and fine-tuned after every time it has been run in order to make the results as

accurate as possible. As a result, the time taken for the model to solve for a parameter set needs to be a matter of minutes. Using the model presented in section 5.6, it is possible to see how many mesh elements are required before the output J_{sc} value converges. This is done in 3D by representing the front texture as pyramids and varying the mesh density from low to high by changing the value of the minimum mesh size at the surface. As the mesh density increases, the J_{sc} converges but the simulation time increases. The initial input parameters for surface recombination velocities, as well as front and rear passivation fixed charges used to create this model were taken from a paper on input parameters for simulations of solar cells by Andreas Fell [157] and ray tracing is used to simulate light propagation and absorption in the device. The simulation times provided were for a single CPU use and the simulation sizes varied from 1Gb to 3Gb in size.

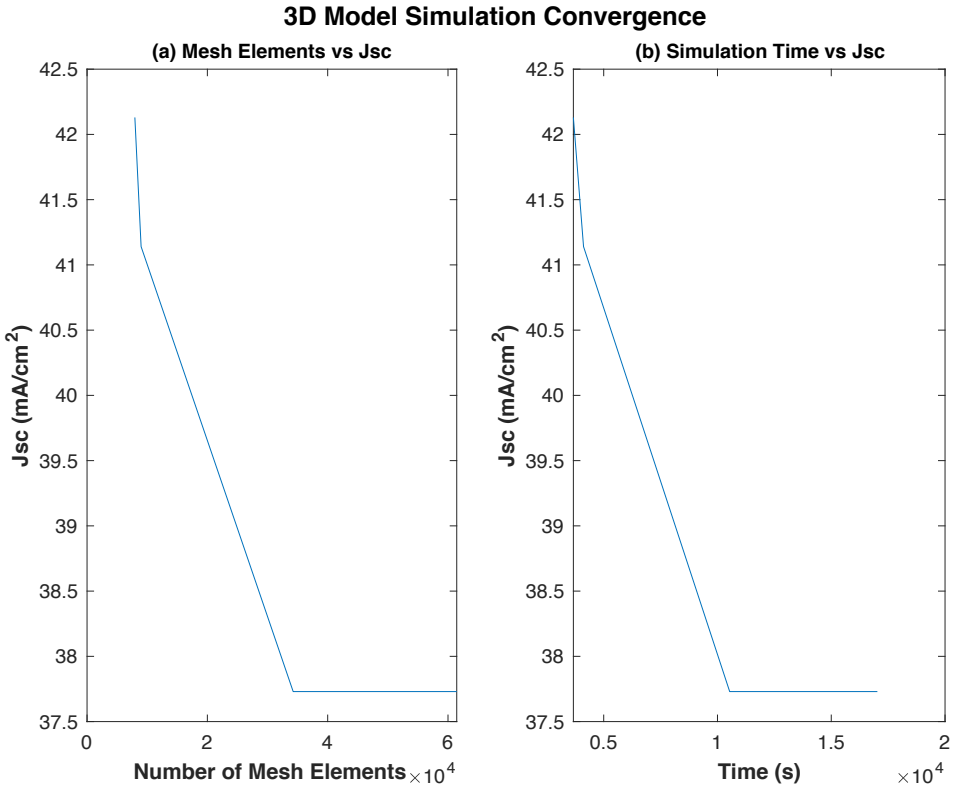


Figure 5.11 - *Number of mesh elements and time taken for 3D model to converge*

From the results shown in Figure 5.11, in order for the 3D model to converge, around 35000 mesh points are required. The time taken for the model to solve for over 35000 mesh elements is over 3 hours, which is not feasible when the objective is to perform sweeps of device parameters to find optimum values.

5.7 Structural Device Editor 2-Dimensional Device Design

In section 5.6.1, it is shown that with a 3-dimensional model the number of mesh elements required for the simulations to converge is prohibitive in terms of the time taken for the sweeps to run, based on the available computing resources. In order to reduce this, the device can be modelled as a 2-dimensional structure following the same principles as discussed in section 5.6. Figure 5.12 shows the initial unit cell used in the 2-dimensional model before any optimisation is done to the design to enhance it. It should be noted that to begin with both the emitter and BSF grooves were made to be the same depth.

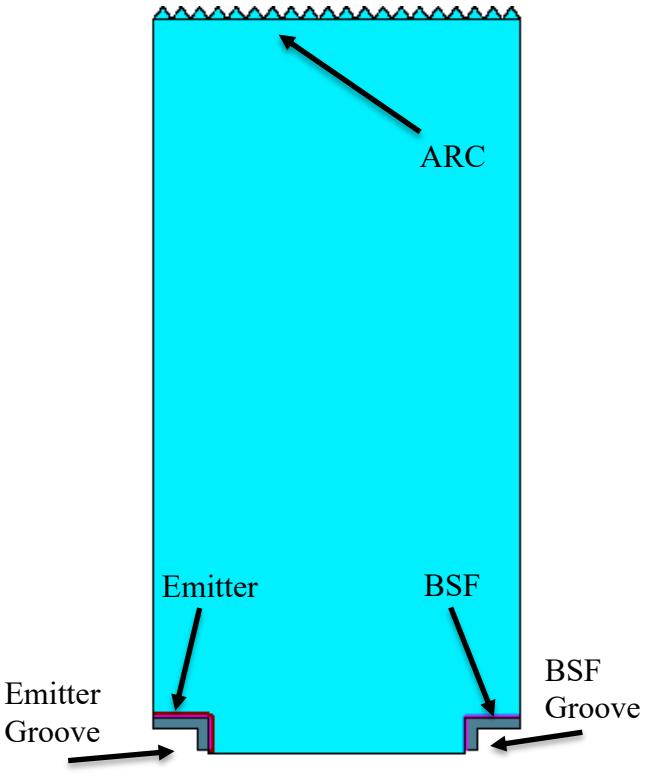


***Figure 5.12** – Initial geometry design of the 2D unit cell*

As with the 3-dimensional model already built, the 2-dimensional model uses the meshing strategy where a finer mesh is used around interface points which then becomes coarser retreating away from these interfaces. This is shown in Figure 5.13 where the entire meshing structure has been overlaid onto the unit cell. Figure 5.14 shows how the textured pyramids on the front surface of the device have been modelled with the meshing strategy overlaid and Figure 5.15 shows meshing strategy at the interface between the silicon and metal. The doping profile of phosphorous in the deep groove is shown in Figure 5.16 and the carrier generation profile is shown in Figure 5.17.

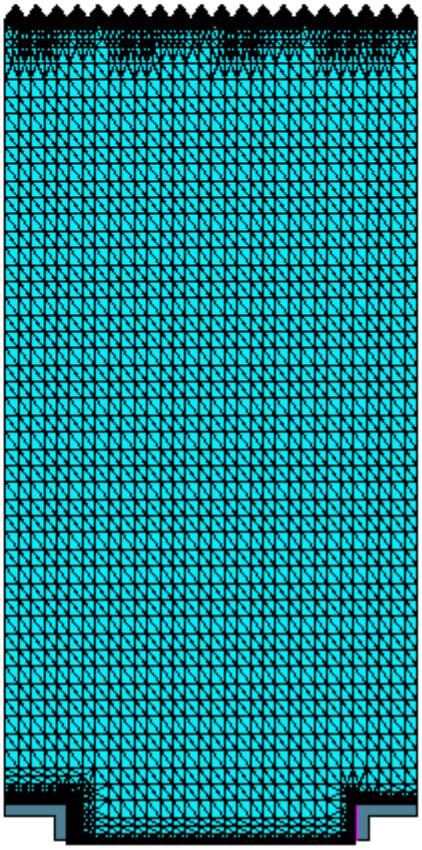


Figure 5.13 – *Non-optimised 2D unit cell showing meshing strategy*

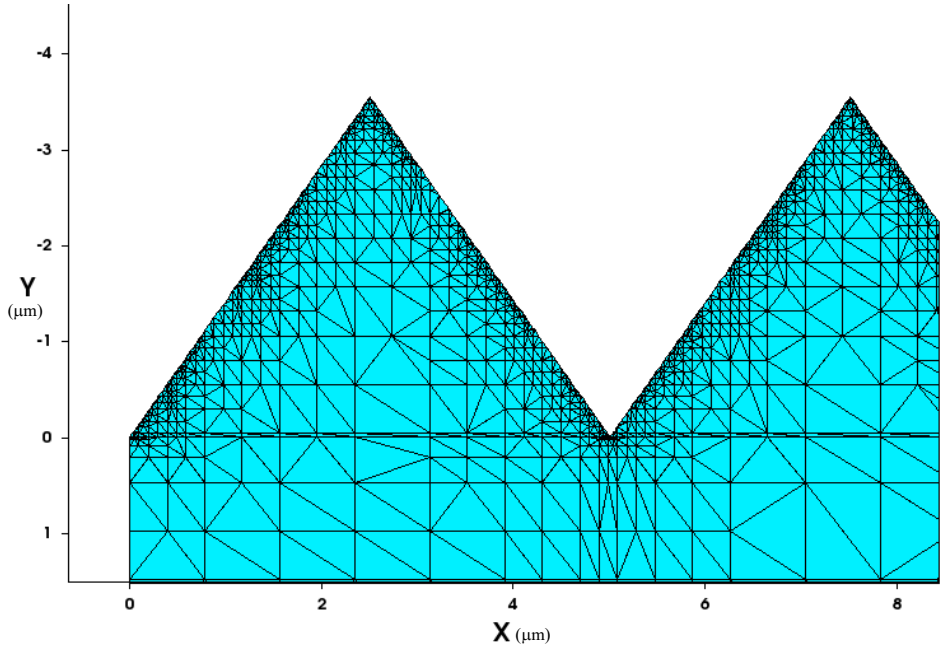


Figure 5.14 - *Front surface showing 2D pyramids and interface meshing strategy*

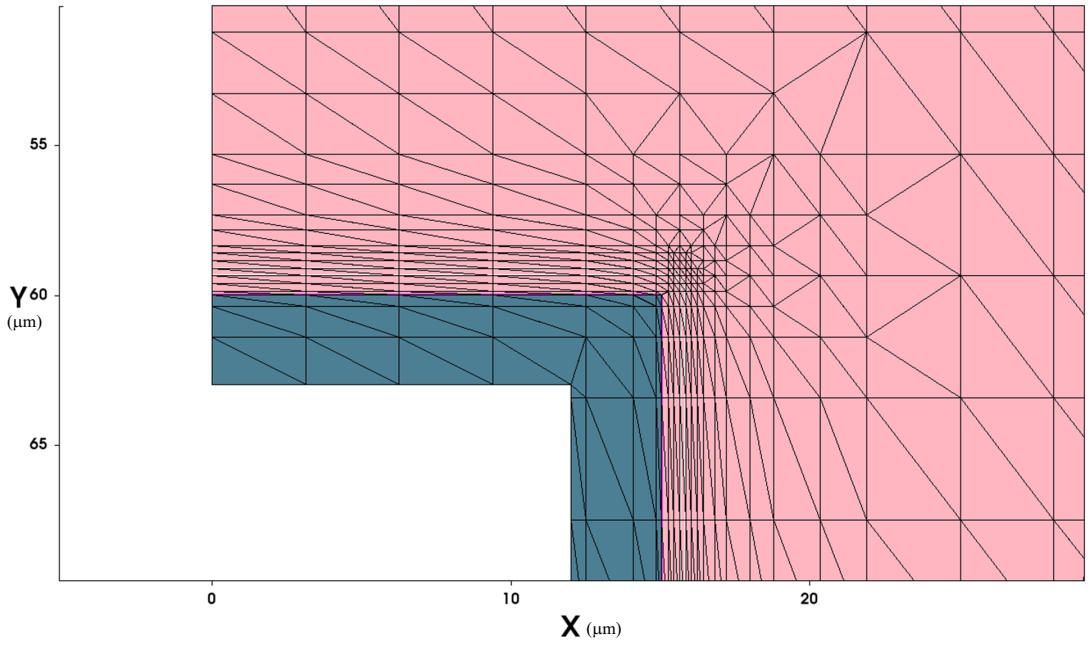


Figure 5.15 - *2D meshing strategy at the interface between silicon and metal*

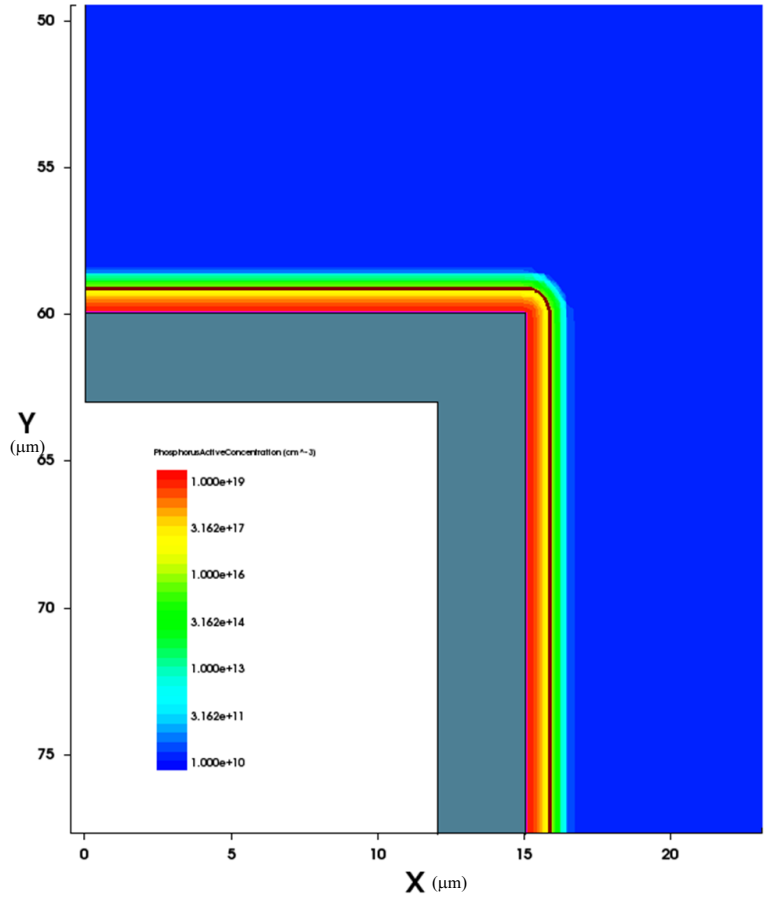


Figure 5.16 - *Phosphorous doping profile in 2D model*

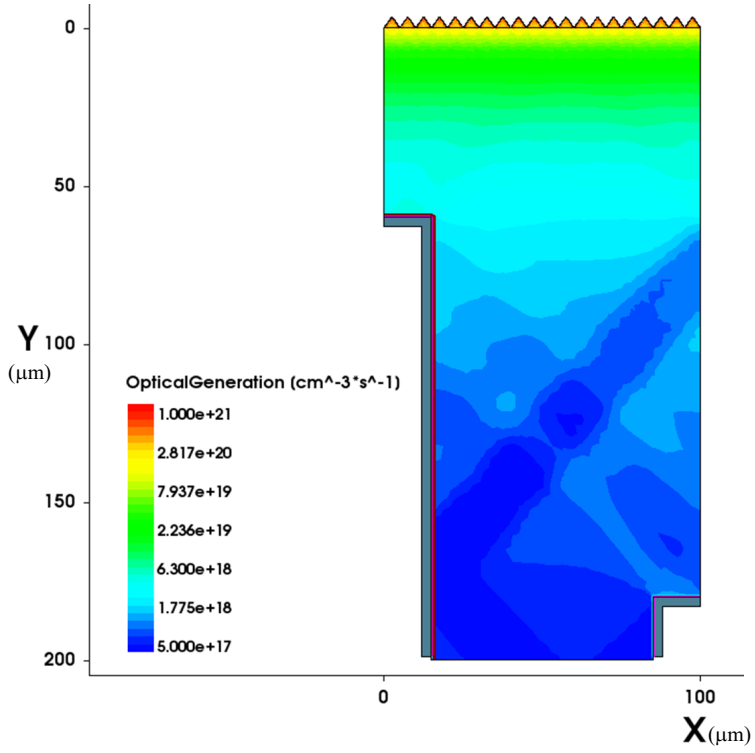


Figure 5.17 - *2D unit cell showing optical generation profile*

The 2-dimensional TCAD approximations of the pyramids appear to underestimate the antireflective properties of real 3-dimensional pyramids, therefore the simulation results will lead to rather conservative results. Figure 5.18 shows the TCAD unit cells for both the 2D and 3D models, clearly showing the change in representation of the pyramidal front surface texturing. An alternative approach to modelling the optics is investigated later in the chapter.

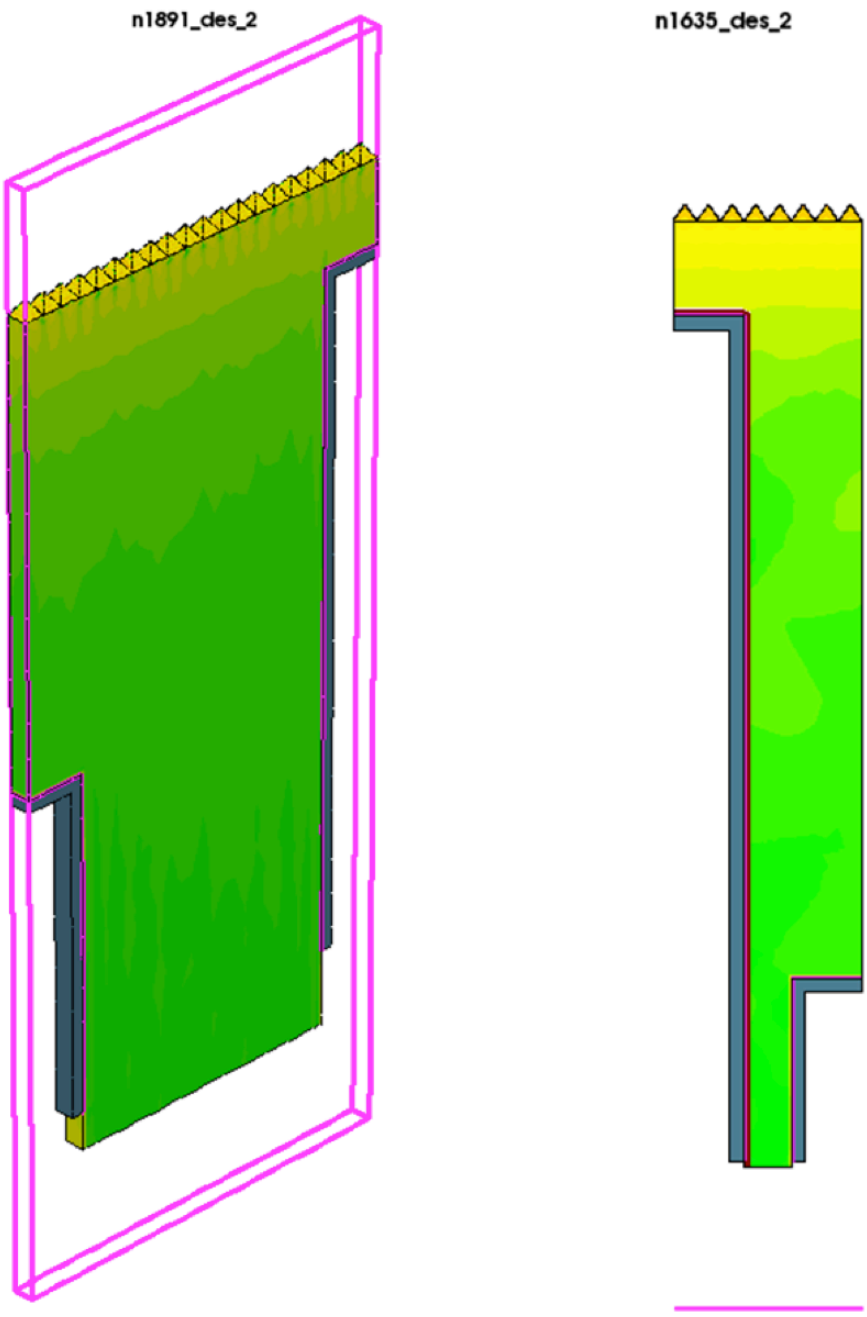


***Figure 5.18** - 3D and 2D TCAD model unit cells*

5.7.1 2-Dimensional Model Convergence

As with the 3D model, it is important to see whether the new 2D model that has been created can be run so that accurate results are given within a short period of time. This was done in the same way as the 3D convergence in section 5.6.1 but instead of representing the front surface as pyramids, in the 2D model the front surface is represented as triangles. The optics were again calculated via ray-tracing.

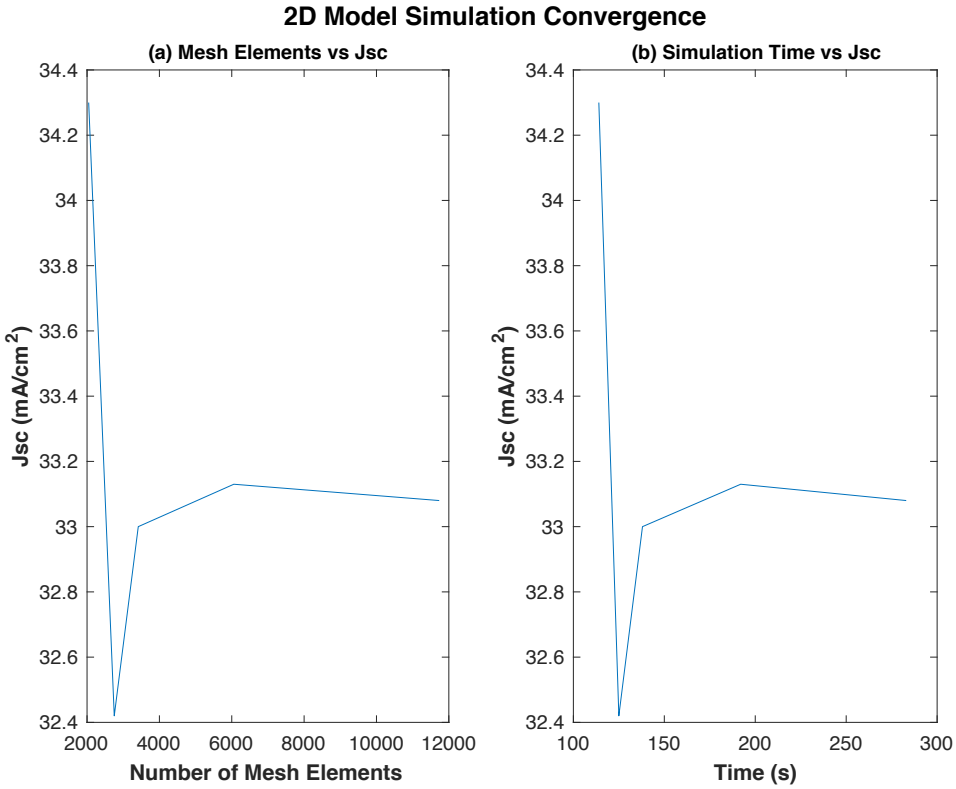


Figure 5.19 - *Number of mesh elements and time taken for 2D model to converge*

Whereas the 3D model was taking over 35000 mesh elements to converge, Figure 5.19 shows that the 2D model only requires around 6000 mesh elements to converge, and while the 3D model took over 3 hours to solve for this the 2D model can solve to convergence in around 3 minutes making it much more suitable for use with the resources available for this project.

5.8 SDEVICE Simulation Results and Discussion

Taking the 2-dimensional device outlined in section 5.7 from the SDE, parameters can be varied and using the SDEVICE simulation tool, the expected current-voltage characteristics of the device can be obtained. In this section, several different variables will be altered to see what effect they have on the characteristics of the device.

5.8.1 Emitter and BSF Groove Depth Investigation

In this study, the depth (as shown in Figure 5.4) of the emitter groove (n-type phosphorous doped) and back surface field groove (p-type boron doped) are varied between 20 μm and 180 μm. The results of this simulation sweep are shown graphically in Figure 5.20 with data for J_{sc}, V_{oc}, fill factor (FF) and device efficiency (η) displayed.

From this simulation, the graphs in Figure 5.20 are produced which show that depth of the emitter makes a significant difference to the performance of the device. As the emitter groove gets deeper, better results are obtained. Moving from 20 μm to 180 μm sees the J_{sc} and the V_{oc} improving, leading the overall device efficiency to go from around 2% to over 12%. This is as a result of the emitter (collection region) being closer to the generation region so the charge carriers have less distance to travel. The depth of the emitter however has very little effect on the device fill factor. In contrast to this, the depth of the BSF groove has very little effect on the J_{sc}, V_{oc} or device efficiency with better results found when the BSF depth is lower as more of the bulk material is retained. As with the emitter, there are only marginal increases in the device fill factor by less than 1% as the depth goes from 20 μm to 180 μm.

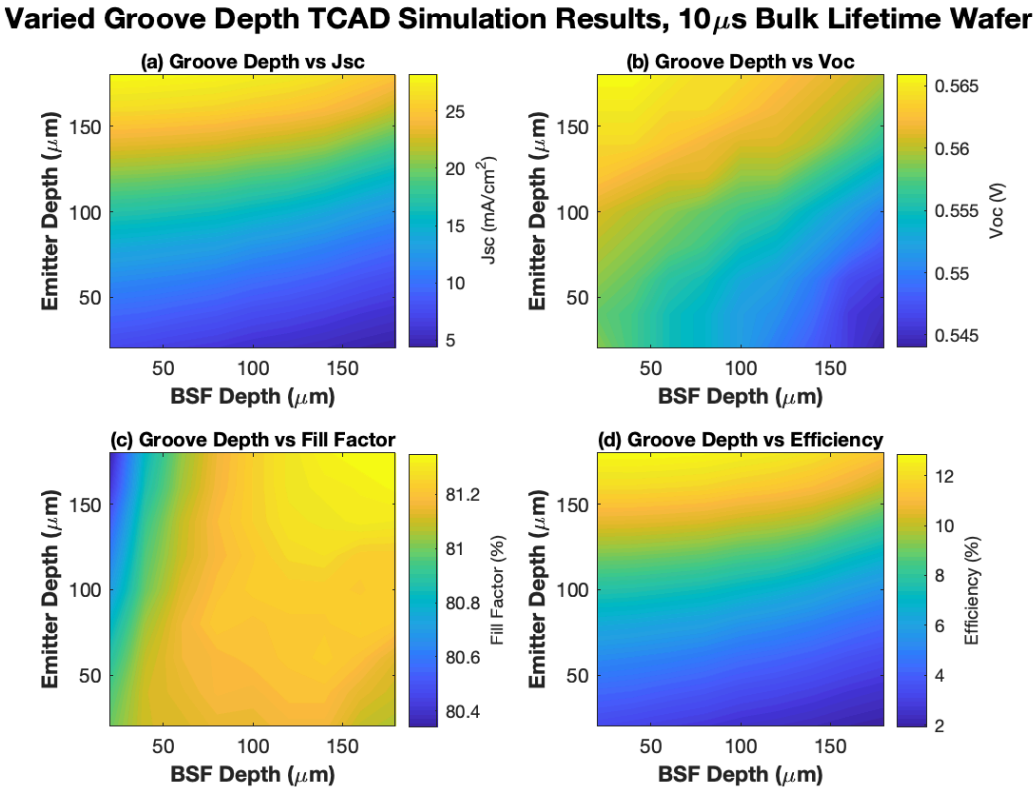


Figure 5.20 - *TCAD simulation results with depths of grooves varied on 10μs bulk lifetime silicon*

5.8.2 Groove Pitch Investigation

An unknown variable is how the pitch (as shown in Figure 5.4) of the grooves effects the performance of the device. Experimentally the pitch was kept constant for ease of handling with only a crude wafer alignment method available, however in the TCAD model the pitch can be easily be varied, so it is possible to investigate the effects that this has on device performance characteristics.

For this investigation, the pitch was varied between 40 and 180 μm. Figure 5.21 shows the results of the TCAD simulation for this investigation. As the pitch decreases, the J_{sc}, fill factor and efficiency all increase significantly. This occurs because when the pitch is lower there is a greater density of emitters, so the distance between the charge collection and generation regions again decreases. However, the

simulation shows that the V_{oc} increases with pitch. This can be explained by considering that when there are more emitters, there is a greater surface area of highly doped silicon which can lead to greater surface recombination and band gap narrowing, which in turn leads to a lower V_{oc}. The decreasing fill factor is due to an increase in the series resistance as the generated carrier will have to take a path of greater resistance to reach an emitter as the pitch gets larger.

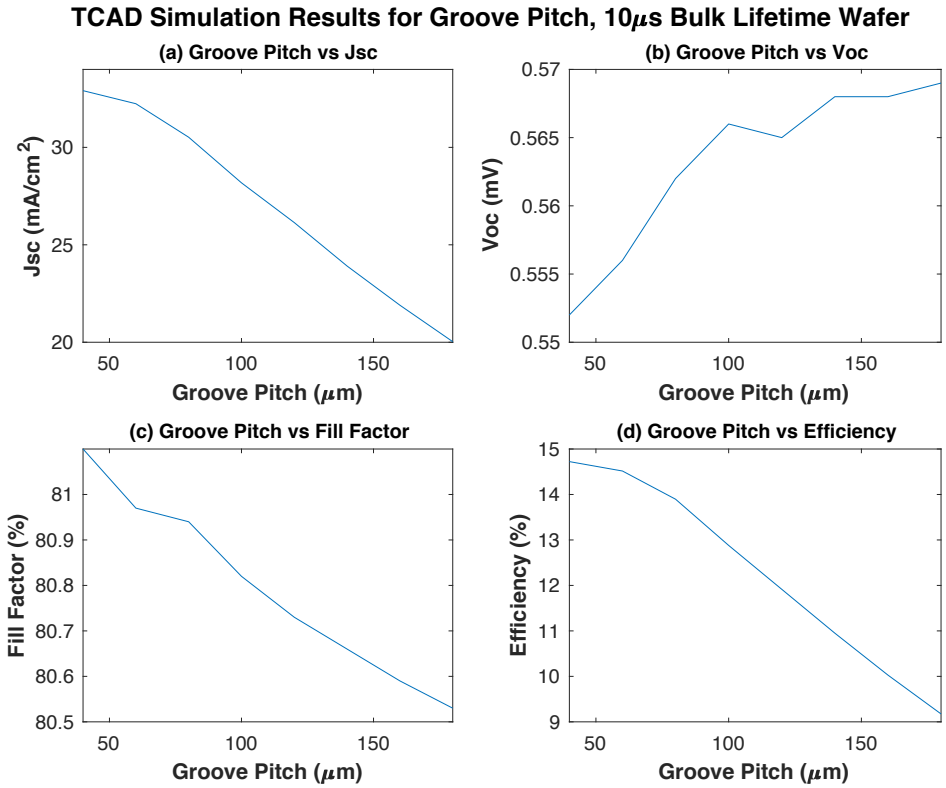


***Figure 5.21** – TCAD simulation results when groove pitch is varied on 10μs bulk lifetime silicon*

5.8.3 Doping Investigation

In this simulation, the doping of both the deep n-type groove (emitter) and the shallow p-type groove (BSF) are investigated. Experimentally altering the length of the dopant deposition time, and the dopant drive in time can change both the doping concentration and profile.

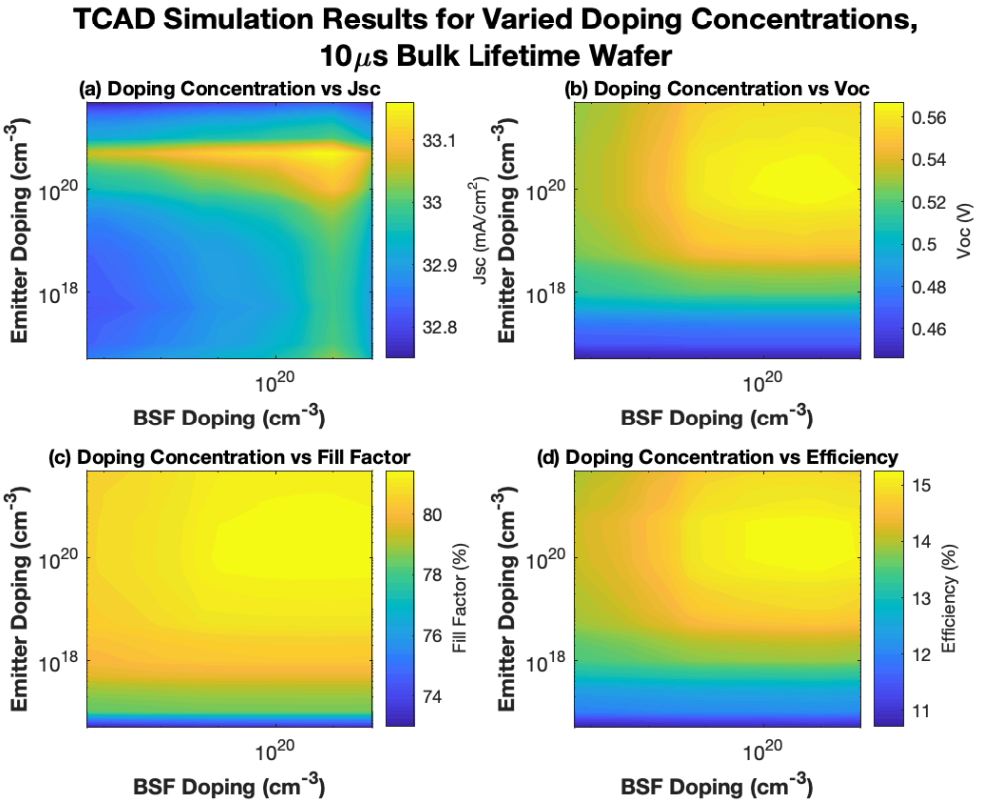


***Figure 5.22** - TCAD simulation results when emitter and BSF doping concentrations are varied on 10μs bulk lifetime silicon*

Figure 5.22 shows the results of the TCAD simulation when these elements of the diffusion recipes are varied to change the doping concentration. In all the simulations, the concentration of the emitter dopant has a much greater effect on the device performance than the doping concentration of the BSF. As the emitter doping concentration increases, increases are seen in J_{sc}, V_{oc}, fill factor and device efficiency until a peak doping concentration of 1E+20 cm^{-3} is reached, at which point the performance starts to decrease. This decrease is probably due to increase in Auger recombination which arises when areas are heavily doped. The peak BSF doping concentration is reached at 5E+20 cm^{-3}, although the maximum gain in device efficiency by increasing the BSF is only about 1%.

5.8.4 Metal Coverage Within Groove Investigation

The introduction of metal into the grooves, whilst essential in order to make an electrical connection to the device, also increases the metal-silicon contact recombination that can occur. This investigation looks into how the device would perform if part of the groove wall was passivated so as to limit the amount of metal that can be deposited into the groove, as shown in Figure 5.23.

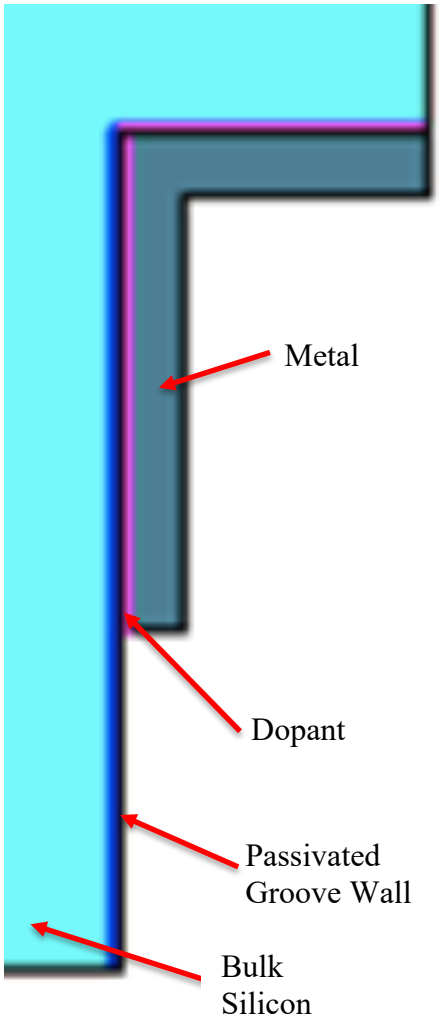


***Figure 5.23** – TCAD model of 40% passivated groove wall*

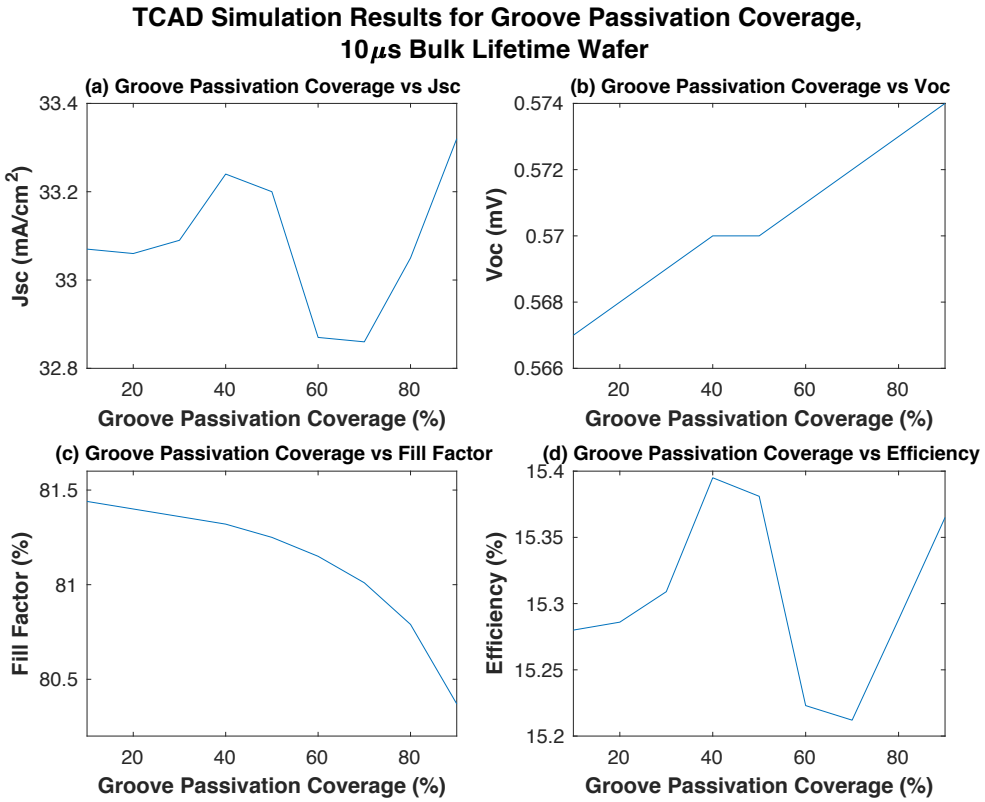


***Figure 5.24** - TCAD simulation results when a percentage of the groove is passivated on 10μs bulk lifetime silicon*

The TCAD simulation results for this investigation are shown in Figure 5.24 where the percentage of the groove wall covered with a passivation layer is varied between 10%-90%, with the percentage of the groove wall that is not passivated being metallised. From the results, the V_{oc} consistently improves as the percentage of the groove passivated increases. This is because metal-silicon contact recombination reduces as a result of less metal-silicon interfacial area present in the groove. The J_{sc} improves and then falls off before improving again as the amount of metal present decreases. There are several factors that would lead to this behaviour: the optical behaviour will change as the amount of metal varies and the series resistance will increase as the amount of metal decreases because the carriers will have to travel further to reach metal. This greater distance travelled may also increase the number of

carriers recombining in the bulk. From the modelling study, the optimum device parameters are achieved when 40% of the groove is passivated leaving the remaining 60% of the groove able to be metallised giving a cell efficiency of 15.39% on 10 µs lifetime wafers.

5.8.5 Bulk Lifetime Investigation

Modelling so far in this chapter has focused on low bulk lifetime (10 µs) wafers but it is interesting to explore through simulations how the deep laser cut groove geometry can work with higher bulk lifetime silicon.

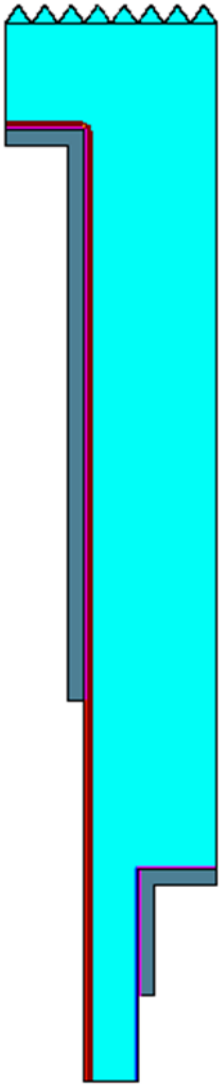


Figure 5.25 - *TCAD visualisation of optimised device for low bulk lifetime wafer*

For this simulation, the optimal values of all the previously investigated variables where inputted as shown in Figure 5.25, with only the bulk lifetime (tau) being varied.

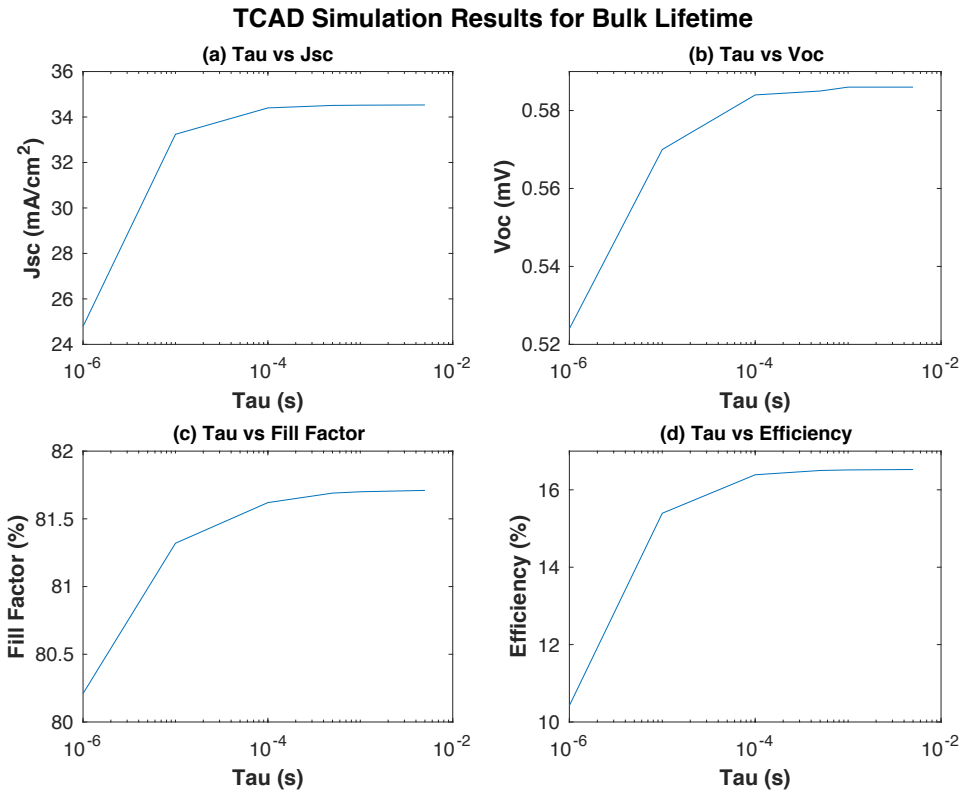


***Figure 5.26** - TCAD simulation results when bulk lifetime is varied*

Figure 5.26 shows the results of this TCAD simulation. As expected, the higher the bulk lifetime the better the device performs. This simulation shows that with high bulk lifetime silicon device based on this device geometry, theoretical efficiencies of 16.5% can be achieved, which is a 1% increase in efficiency compared to the cells made with 10 µs bulk lifetime wafers modelling to this point has been done on. The TCAD parameters used within this model in order to achieve these results are listed in Table 5–2 and a summary of the device characteristics obtained from the TCAD model are listed in Table 5–3.

Whilst the modelling suggests that optimal depth of the emitter is 180 μm, when the grooves are this deep the wafer becomes very fragile (the total wafer thickness is only 200 μm). In the experiments reported in section 4.2.5, the deepest grooves that were achieved were ~120 μm before the wafer became too fragile to handle whilst being transported between clean rooms for processing.

Table 5–2 - *TCAD values used for device parameters*

Device Parameter	TCAD Value	Device Parameter	TCAD Value
Background Doping (cm^{-3})	1.80E+16	Depth of Emitter (μm)	180
Emitter Peak Doping (cm^{-3})	1.00E+20	Depth of BSF (μm)	40
Emitter junc. Depth (μm)	1	Passivation Coverage of Groove (%)	40
BSF Peak Doping (cm^{-3})	5.00E+20	Bulk Lifetime (s)	Swept
BSF junc. Depth (μm)	1	SRV at Front Surface (cm/s)	100
Width of Emitter (μm)	30	SRV at Rear Surface (cm/s)	10
Width of BSF (μm)	30	Qf at Front (cm^{-3})	-5.00E+12
Pitch (μm)	40	Qf at Rear (cm^{-3})	-5.00E+12

Table 5–3 - *Device characteristics from TCAD model*

Bulk Lifetime	10 μs	500 μs
Jsc (mA cm^{-2})	33.24	34.51
Voc (mV)	570	585
FF (%)	81.62	81.69
η (%)	15.39	16.5

5.8.6 Localised Emitter Investigation

All the experimental and modelling work done in this project has involved doping the entire deep groove with phosphorous to create the emitter. It is known that large, heavily doped areas can increase the bulk and surface recombination, which negatively impacts upon the performance of the device. Because lasers can be used to apply heat to localised areas, the idea of using the laser to create a localised emitter becomes a possibility. This would reduce the size of the heavily doped areas of silicon, potentially lowering the bulk and surface recombination in the device. To investigate this, further simulations were done varying the percentage of the groove that was doped. The TCAD model was modified to replicate having a smaller emitter region, as shown in Figure 5.27.

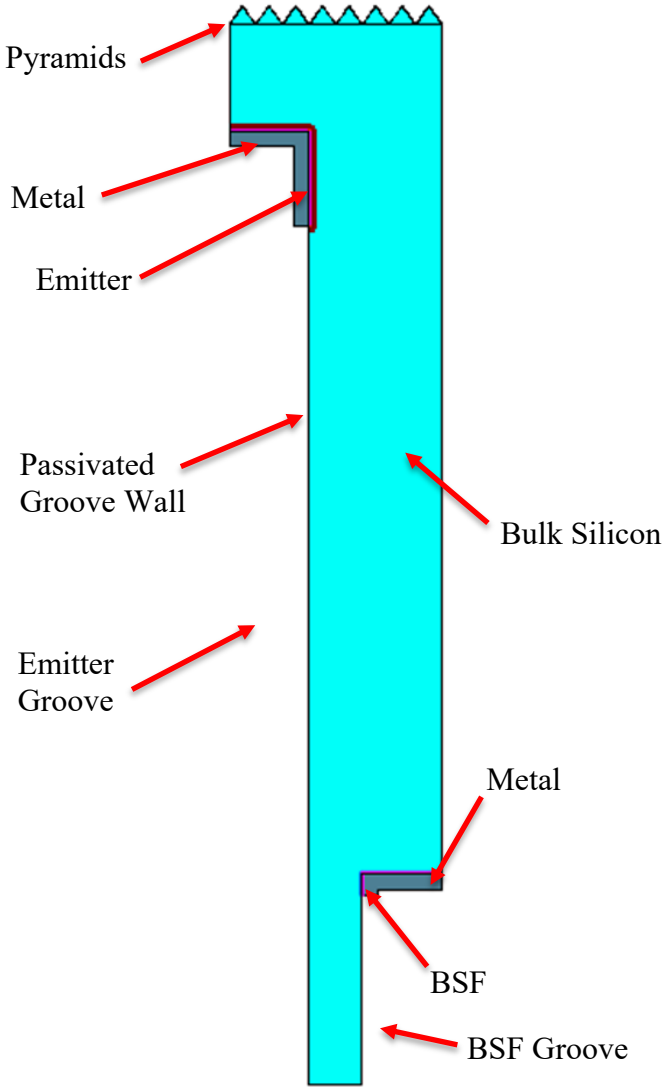


***Figure 5.27** - TCAD visualisation of optimised device for low bulk lifetime wafer with localised emitter*

5.8.6.1 Emitter Groove Coverage Investigation

For this simulation, the size of the emitter was varied as a percentage of the groove depth and the results are shown in Figure 5.28. As expected, as the size of the emitter decreases from 90% of the groove to 10% of the groove, the V_{oc} increases, confirming that the surface and bulk recombination increase as the size of the emitter decreases. As with the amount of metal investigation, the J_{sc} decreases as the size of the emitter decreases. The fill factor also decreases as the emitter size decreases due to the

carriers having to take a more resistive path to get to the emitter, therefore increasing the device series resistance. All of this results in the device efficiency increasing in excess of 15.5% on a 10 µs bulk lifetime wafer when the emitter size is about 20% of the groove. Once the emitter gets smaller than this, the efficiency starts to decrease, as this is the point that the requirement for an emitter exceeds the gains made by lowering the bulk and surface recombination.

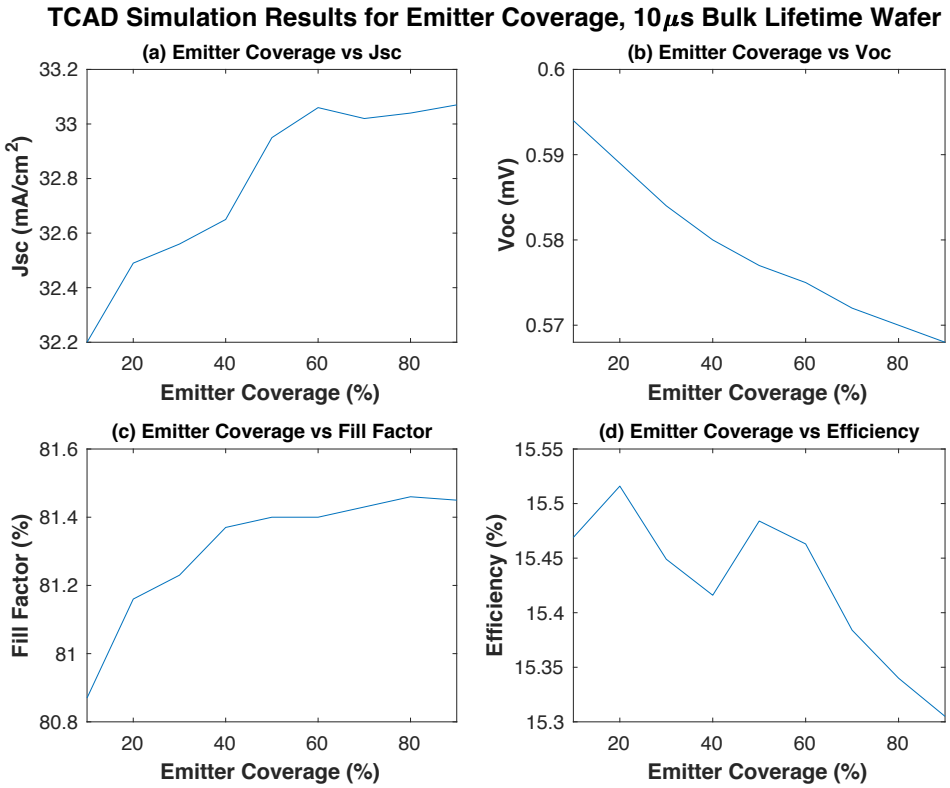


Figure 5.28 - *TCAD simulation results for differing sized emitter*

5.8.6.2 Bulk Lifetime with Localised Emitter Investigation

Having found the optimal size for the emitter, the bulk lifetime simulation can be run again to see how well the geometry would perform in accordance with the assumptions made in this model.

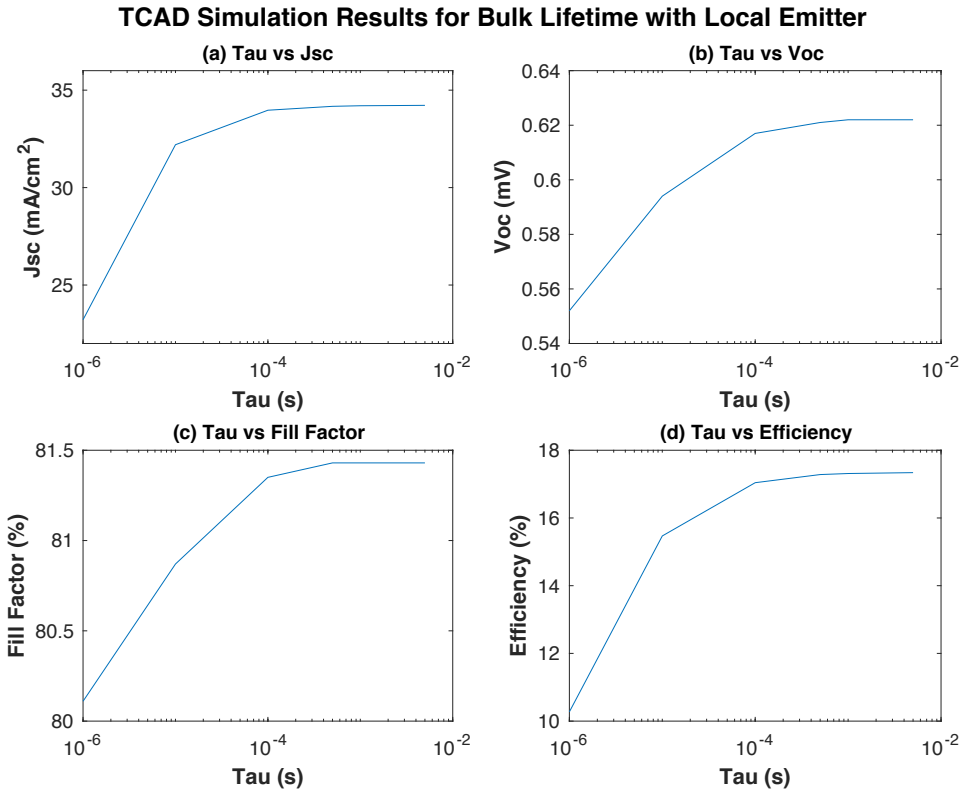


***Figure 5.29** - TCAD simulation results when bulk lifetime is varied and emitter localised*

The simulation results shown in Figure 5.29 reveal that the trends are almost identical to those found in the earlier lifetime simulation in section 5.8.5. Again, the device performance increases as the wafer bulk lifetime increases. A summary of the device characteristics is shown in Table 5–4. A visualisation of the optimised device is shown in Figure 5.27 with the input parameters used listed in Table 5–5.

***Table 5–4** - Device characteristics from TCAD model with localised emitter*

Bulk Lifetime	10 µs	500 µs
Jsc (mA cm^{-2})	32.2	34.17
Voc (mV)	0.594	0.621
FF (%)	80.87	81.43
η (%)	15.469	17.04

Table 5–5 - *TCAD values used for device parameters with localised emitter*

Device Parameter	TCAD Value	Device Parameter	TCAD Value
Background Doping (cm^{-3})	1.80E+16	Depth of Emitter (μm)	180
Emitter Peak Doping (cm^{-3})	1.00E+20	Depth of BSF (μm)	40
Emitter junc. Depth (μm)	1	Passivation Coverage of Groove (%)	90
BSF Peak Doping (cm^{-3})	5.00E+20	Bulk Lifetime (s)	Swept
BSF junc. Depth (μm)	1	SRV at Front Surface (cm/s)	100
Width of Emitter (μm)	30	SRV at Rear Surface (cm/s)	10
Width of BSF (μm)	30	Qf at Front (cm^{-3})	-5.00E+12
Pitch (μm)	40	Qf at Rear (cm^{-3})	-5.00E+12

5.9 Optimised TCAD Simulation Results for 500 μs Bulk Lifetime Wafers

As the price of silicon has fallen dramatically since the original premise of this project was envisaged, the notion of using high bulk lifetime wafers becomes a possibility. A brief investigation of this was done in section 5.8.5 where improved device performance was found to occur when higher bulk lifetime wafers were used. However, in the investigation in section 5.8.5, the device parameters used were optimised for low bulk lifetime wafers. In this section, the same sweeps that were performed in section 5.8 will be performed but with a bulk lifetime of 500 μs.

5.9.1 Groove Depth Investigation for 500 μs Bulk Lifetime Silicon

The results of the TCAD simulation for the sweep of groove depths on high bulk lifetime wafers are shown in Figure 5.30. In accordance with the investigation based around low bulk lifetime silicon, as the emitter depth is increased, the J_{sc} increases and the V_{oc} decreases As the BSF depth increases, both the J_{sc} and V_{oc} decrease. Unlike in section 5.8.1 where in low bulk lifetime silicon the carriers recombine

quicker, the optimum device efficiency point is no longer found when the emitter is at its deepest. This is due to the trade-off between increased surface area resulting in reduced V_{oc} and increasing photocurrent as the emitter is closer to photo-generated carriers at the surface. The TCAD simulation gives the optimum emitter depth at 140 µm whilst the optimal BSF depth remains at its shallowest.

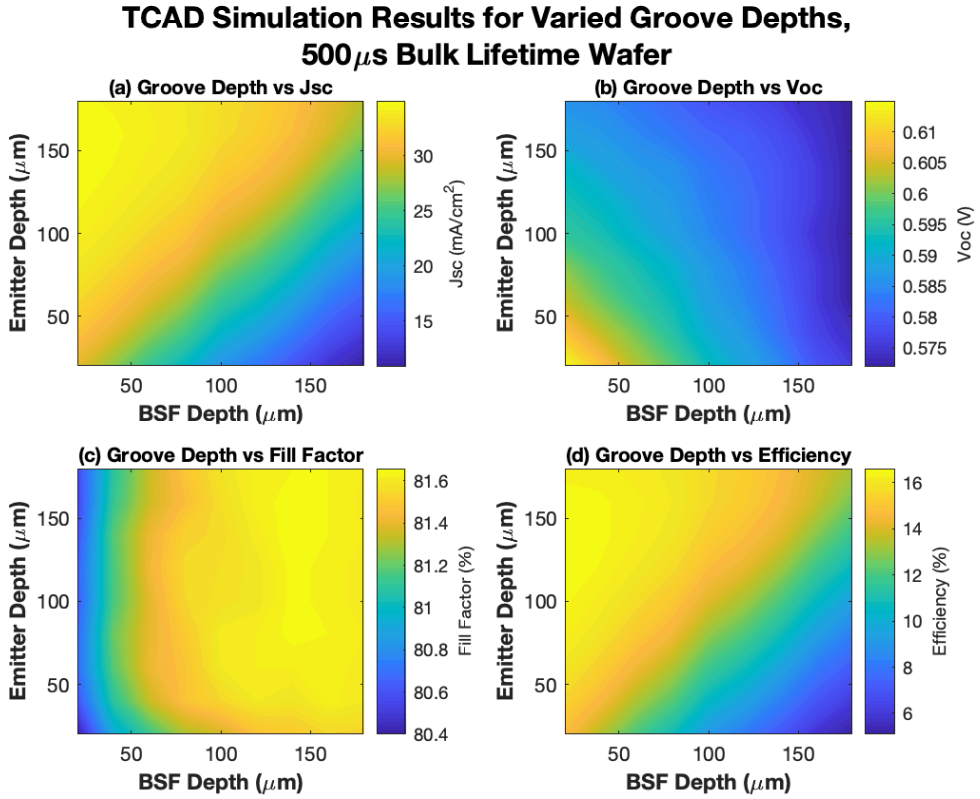


***Figure 5.30** - TCAD simulation results with depths of grooves varied on 500µs bulk lifetime silicon*

5.9.2 Groove Pitch Investigation

The results of the simulation sweep of groove pitch for a high bulk lifetime are shown in Figure 5.31. As was found when varying the pitch was simulated on lower lifetime silicon, J_{sc} and fill factor fall as the distance between grooves increases and V_{oc} rises. Unlike on low lifetime silicon though, on high lifetime silicon the device efficiency is not optimal when the grooves are closest together, initially as the groove pitch increases so does the device efficiency. However, the tip over point between reducing

surface and bulk recombination and increasing series resistance and optical losses is reached when the pitch is 80µm.

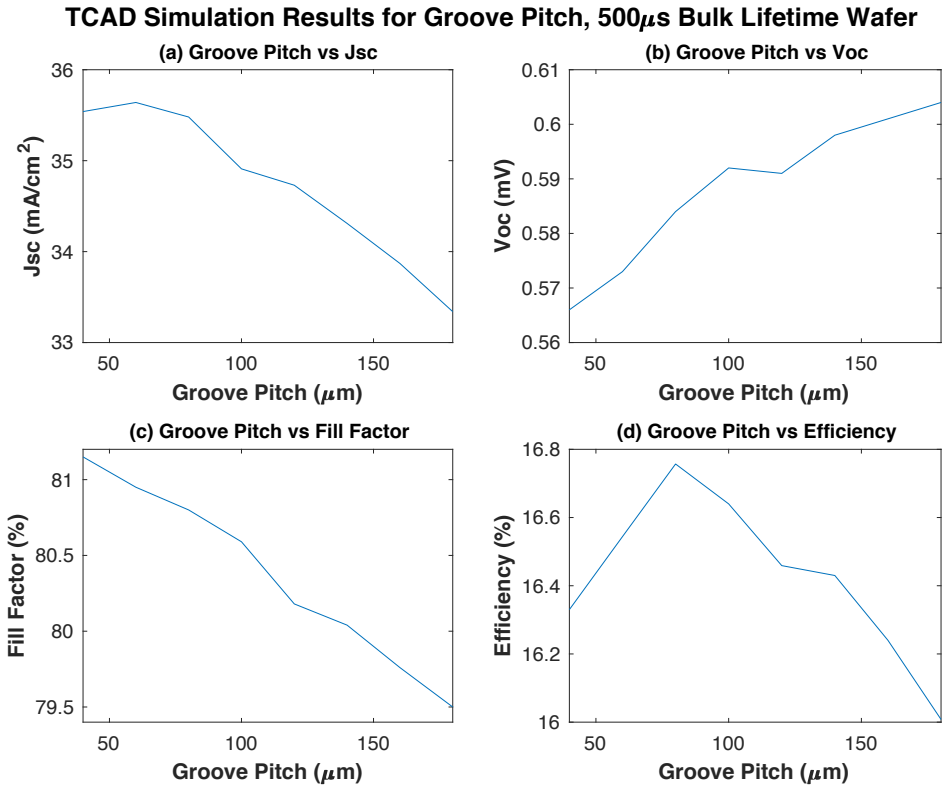


***Figure 5.31** - TCAD simulation results when groove pitch is varied on 500µs bulk lifetime silicon*

5.9.3 Doping Investigation on 500µs Bulk Lifetime Silicon

Varying the doping concentration of both the emitter and the BSF allows the optimum doping concentrations to be found. The results of this as shown in Figure 5.32 show that the doping concentration of the emitter has little effect on the J_{sc} but a great effect on the V_{oc}, causing it to increase as the doping concentration increases. Conversely the doping concentration of the BSF has a great effect on the J_{sc}, causing it to rise as the doping concentration increases but has little effect on the V_{oc}. Both the fill factor and the device efficiency are at their optimum when the doping concentrations of both the emitter and the BSF are at the greatest, although it is the doping concentration of the emitter that causes the greatest effect on these characteristics.

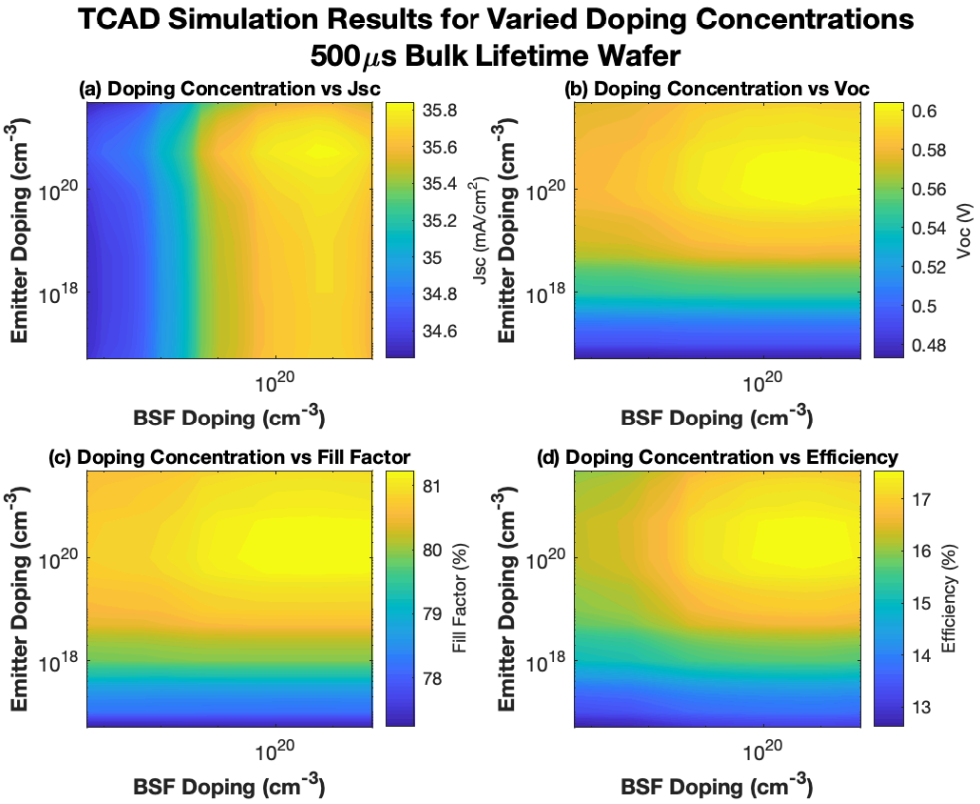


Figure 5.32 *- TCAD simulation results when emitter and BSF doping concentrations are varied on 500μs bulk lifetime silicon*

5.9.4 Groove Metal Coverage Investigation for High Bulk Lifetime Silicon

In section 5.8.4, an investigation into reducing the amount of metal deposited in the grooves was performed by assuming that if part of the groove was passivated then metal would not be able to be deposited into these areas. As was seen from the simulation results in 5.8.4, when the amount of metal deposited in the grooves decreases (and therefore the amount of the groove passivated increases), both the J_{sc} and V_{oc} increase due to the reduction in surface and bulk recombination. The results of this investigation for high lifetime silicon are shown in Figure 5.33 which also shows the fill factor decreasing as the metal content decreases due to the increase in series resistance. As the amount of metal decreases to around 20%, the device efficiency increases, approaching 18% but then falling off as the increased series resistance starts to hamper performance.

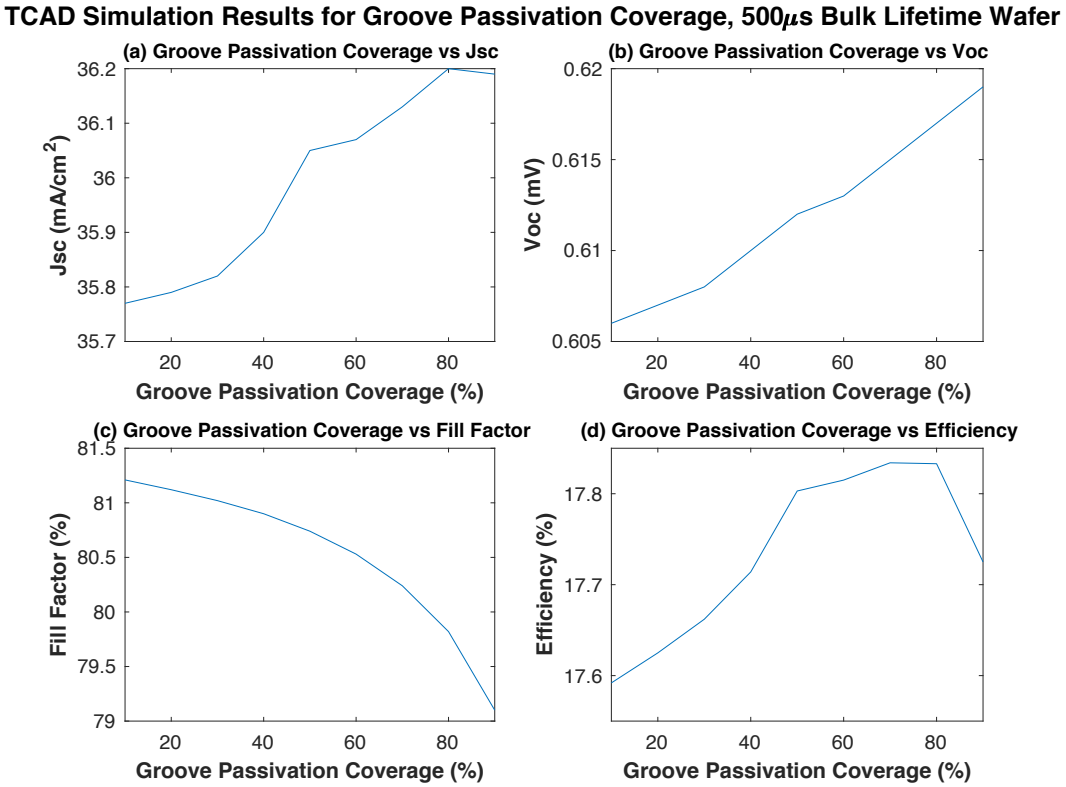


Figure 5.33 - *TCAD simulation results when a percentage of the groove is passivated on 500μs bulk lifetime silicon*

5.9.5 Emitter Groove Coverage Investigation for High Bulk Lifetime Silicon

The final simulation using high lifetime silicon run was to investigate the effect of reducing the size of the emitter. As expected, due to the decrease in amount of heavily doped silicon, the V_{oc} increases as the emitter gets smaller. As seen in Figure 5.34 this leads to device efficiencies in excess of 18% when the emitter size is at its optimum. The optimum parameters for the device when based on silicon with a bulk lifetime of 500 μs are given in Table 5–6 with the device characteristics listed in Table 5–7. Figure 5.35 is a TCAD visualisation of the optimised device unit cell.

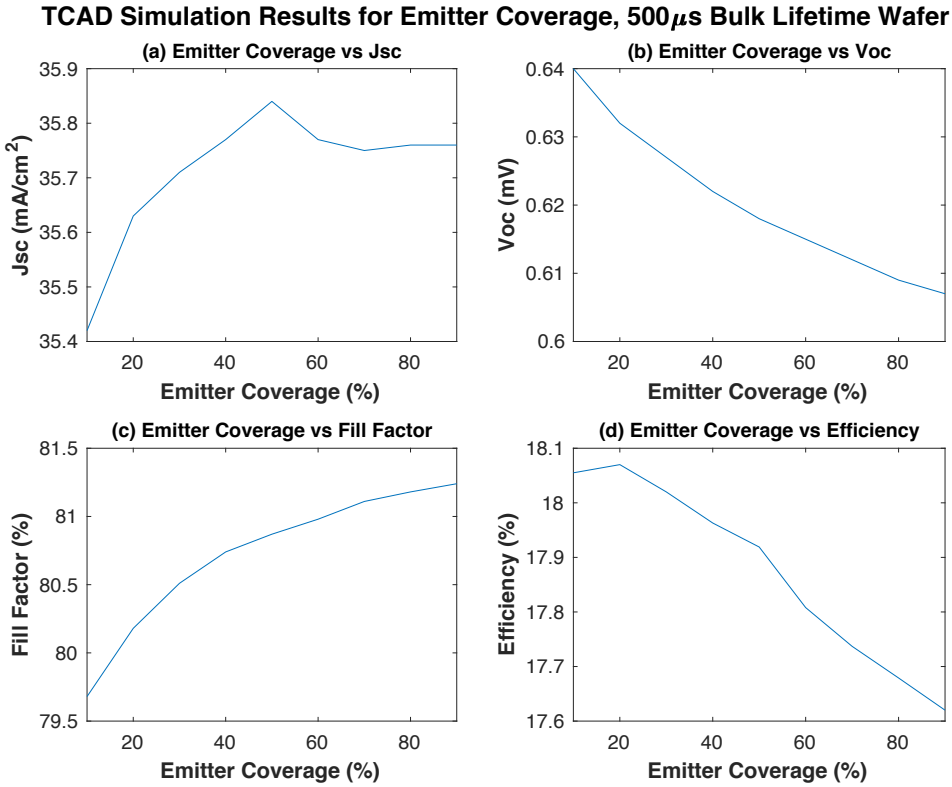


Figure 5.34 - *TCAD simulation results for differing sized emitter on 500μs bulk lifetime silicon*

Table 5–6 - *Optimised device parameters for 500μs bulk lifetime silicon used in TCAD model*

Device Parameter	TCAD Value	Device Parameter	TCAD Value
Background Doping (cm^{-3})	1.80E+16	Depth of Emitter (μm)	140
Emitter Peak Doping(cm^{-3})	1.00E+20	Depth of BSF (μm)	20
Emitter junc. Depth (μm)	1	Passivation Coverage of Groove (%)	0.9
BSF Peak Doping (cm^{-3})	5.00E+20	Bulk Lifetime (s)	500E-6
BSF junc. Depth (μm)	1	SRV at Front Surface (cm/s)	100
Width of Emitter (μm)	30	SRV at Rear Surface (cm/s)	10
Width of BSF (μm)	30	Qf at Front (cm^{-3})	-5.00E+12
Pitch (μm)	80	Qf at Rear (cm^{-3})	-5.00E+12

Table 5–7 - *Device characteristics for full and partial emitter on 10µs and 500µs bulk lifetime silicon*

	Full Emitter Groove		Local Emitter Groove	
Bulk Lifetime (µs)	10	500	10	500
Jsc (mA cm^{-2})	26.18	36.13	22.68	34.17
Voc (mV)	574	0.615	0.586	0.621
FF (%)	79.92	80.24	79.64	81.43
η (%)	12.016	17.834	10.595	18.055

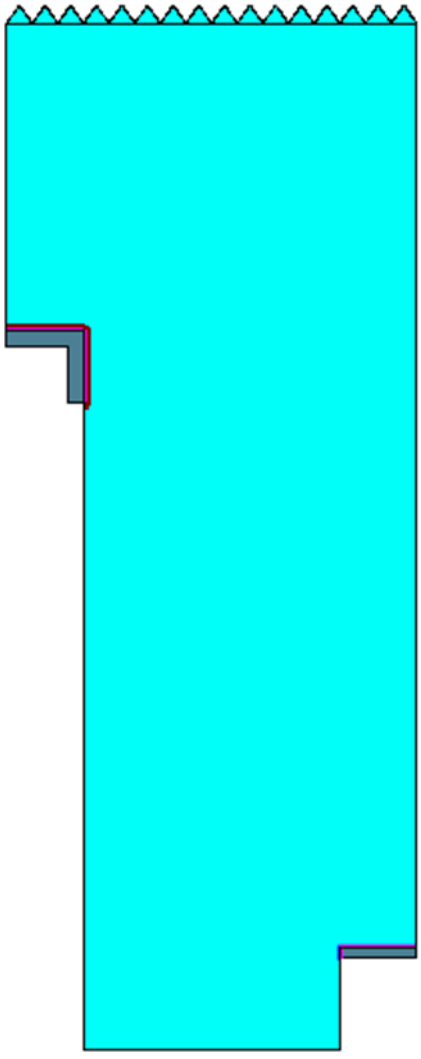


Figure 5.35 - *TCAD visualisation of optimised device for 500µs bulk lifetime wafer with localised emitter*

5.10 Optimised TCAD Simulations Using OPAL2 Optical Model

In section 5.7.1, the drawbacks of using a 2D model were touched on. Although the speed of simulation allows for many useful trends to be seen the overall results generated are very conservative. This is because the 2D TCAD approximation of the pyramids (which is built as grooves that leave triangles as opposed to actual pyramid) greatly underestimates the antireflective and light trapping properties of real pyramids.

Another way of modelling the optical properties is to use the OPAL2 simulator (previously used in section 5.3) instead of the ray tracing method used by TCAD.

***Table 5–8** - TCAD characteristics using both ray tracing and OPAL 2 optical generations*

Characteristic	Optimised 10 µs Cell		Optimised 500 µs cell	
	RT	OPAL2	RT	OPAL2
Jsc (mA cm^{-2})	32.2	35.38	35.42	40.38
Voc (mV)	0.594	0.597	0.64	0.643
FF (%)	80.87	80.75	79.68	79.24
η (%)	15.469	17.049	18.055	20.569

The results of this are shown in Table 5–8 which shows that using the OPAL2 optical generation as opposed to the ray tracing gives an improved value for the J_{sc}. This is due to the antireflective effects of the pyramids on the front surface being better. The results of this is that by using low bulk lifetime silicon, device efficiencies in excess of 17% can be expected and using high bulk lifetime silicon, device efficiencies in excess of 20.5% can be expected from this device geometry.

The disadvantage of using OPAL2 over ray tracing is that it does not include the effect of the changing propagation of light coming into the cell due to refraction at the

inclined facets of the pyramids, so even though the results have improved they are still on the conservative side.

5.11 3D Simulation Using Optimised 2D Parameters

The only way to include all of the effects in the TCAD model would be to use a full 3D simulation to perform the parameter sweeps. However as was shown in section 5.6.1 the mesh density needed to ensure accuracy is prohibitively large for the computational resources available during this project.

Once the 2D model has been used to perform the parameter sweeps, these parameters can be inputted into the 3D model. These parameters would not be optimal, this can only be achieved by performing the sweeps on the 3D model, however they can give a more accurate result of how a fabricated device may perform if built to these specifications. Table 5–9 shows the results when these optimised 2D parameters were used to run the 3D model.

Table 5–9 - *TCAD characteristics using optimised 2D parameters in 3D model*

Characteristic	Optimised 10 µs Cell	Optimised 500 µs cell
Jsc (mA cm^{-2})	35.36	39.17
Voc (mV)	0.598	0.643
FF (%)	80.72	79.62
η (%)	17.065	20.045

The visualisations of these 3D models with the optimised 2D parameter set are shown in Figure 5.36.

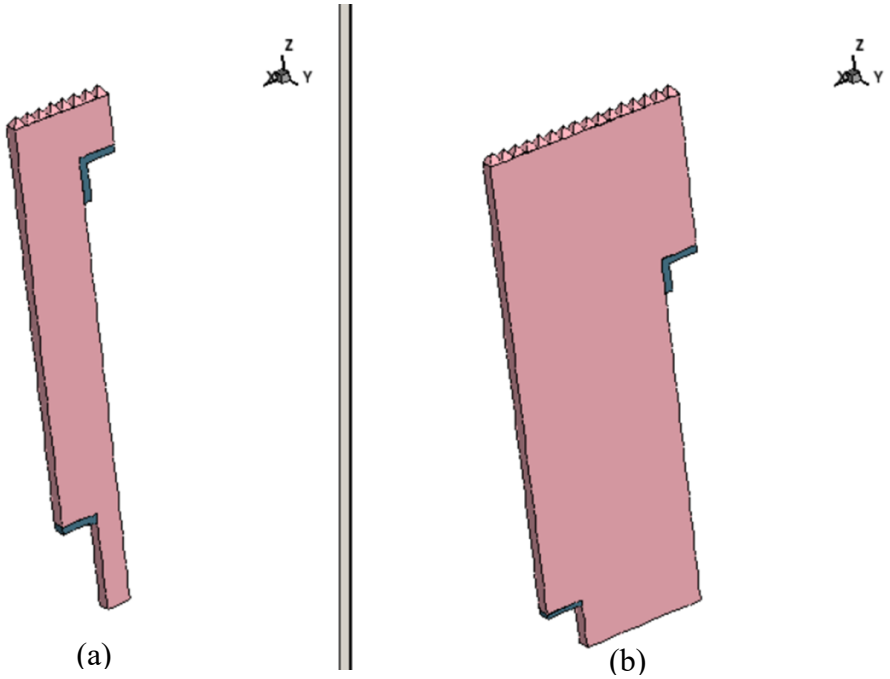


Figure 5.36 - *Visualisation of 3D model built with optimised 2D parameters*

Comparing the data from Table 5–8 and Table 5–9, it can be seen that the 3D model results and the 2D model results using the OPAL 2 optical model are very similar. The 3D model uses pyramids for the front surface texturing (as opposed to grooves in the 2D model) and uses ray tracing (discussed in section 5.2.2) for optical modelling. It confirms that the characteristic improvements seen in the 2D model using the OPAL 2 optical generation are accurate.

5.12 Modelling Summary

From the computer modelling described in this chapter, it is clear to see that considerable device performance improvements can be made to the proof of concept device fabricated in Chapter 4. The optical modelling in section 5.3 demonstrates that the thickness of the ARC layers affects the number of photons that can be absorbed by the substrate. This is a useful model, as it goes someway to explain the deficiencies experienced in the proof of concept device in section 4.4 where very thick ARC layers

were deposited. The optimal thicknesses of the ARC layers have wide thickness tolerance however which would make it easily achievable in mass production.

The TCAD modelling demonstrates that device performance gains are possible in back contact solar cells as a result of cutting deep grooves into the silicon to form the rear side emitter. In the low bulk lifetime model shown in section 5.8.1, because in low bulk lifetime silicon the carriers recombine too quickly, the deeper the groove (i.e. closer the emitter to the surface), the better the performing cell, and thus 180 µm (the upper limit in this simulation) is the optimal depth (as shown in Figure 5.20). The optimal emitter depth for high-lifetime as modelled in section 5.9.1, is 140 µm based on these TCAD simulations, due to a trade-off between increased surface area resulting in a reduced Voc, and that of increasing photocurrent as the emitter is closer to photo-generated carriers at the surface which is seen in Figure 5.30. A model for a front junction device was not created, so it is not possible to directly compare the improvements seen with a front junction device. From the literature relating to the BP Saturn cell, the modelled efficiency using a 200 µm thick wafer with a minority carrier lifetime of 25 µs of 19.1% [113]. However further details of this model were not available.

Further TCAD modelling within this chapter shows improvements that can be achieved by limiting the amount of metal deposited into the grooves as a result of a reduction in the metal/silicon contact recombination. The implementation of a doped p+ back surface field is also shown to improve device performance is it improves the ohmic contact to the BSF. The proof of concept device, in addition to the lack of front surface texturing and poor ARC shown in the optical modelling did not feature these additional improvements. These improvements, if able to be implemented, could

result in the fabrication of a back contact device that could have a place in the current solar cell marketplace.

To build on these findings, Chapter 6 will look at some practical work carried out to take the concepts identified by the modelling and realise them experimentally. The thickness of the ARC layers can be varied by modifying the furnace recipes used to create them and the texturing of the front surface of the wafer will be attempted. Finally approaches to limiting the amount of metal deposited and selective BSF doping will be investigated.

Chapter 6 Further Experimental Work to Improve Device

Chapter 4 demonstrated that with this proposed geometry, a working device can be fabricated, and Chapter 5 revealed through modelling that the initial device can be improved upon. This chapter will build upon the work already done experimenting with the fabrication processes needed in order to work towards achieving the expected results obtained from the modelling.

6.1 Front Surface Texturing

As was first discussed in section 3.2.4 and then modelled in 5.3, texturing the wafer surfaces with random 3D pyramids can enhance light trapping, therefore improving the overall efficiency of the device (see Figure 5.3). Alkali texturing of silicon wafers is a commonly used process in the PV industry. Initially an off-the-shelf sodium hydroxide (NaOH) etch was tried. This required the wafers to be immersed into a solution of 2% sodium hydroxide (NaOH) and 2% isopropyl alcohol (IPA) at 70°C for 20 minutes. The resultant textured surface is shown in Figure 6.1. It is observed at a higher magnification (Figure 6.2) that the surface is not fully covered by pyramids and there are large areas where the silicon has not been textured.

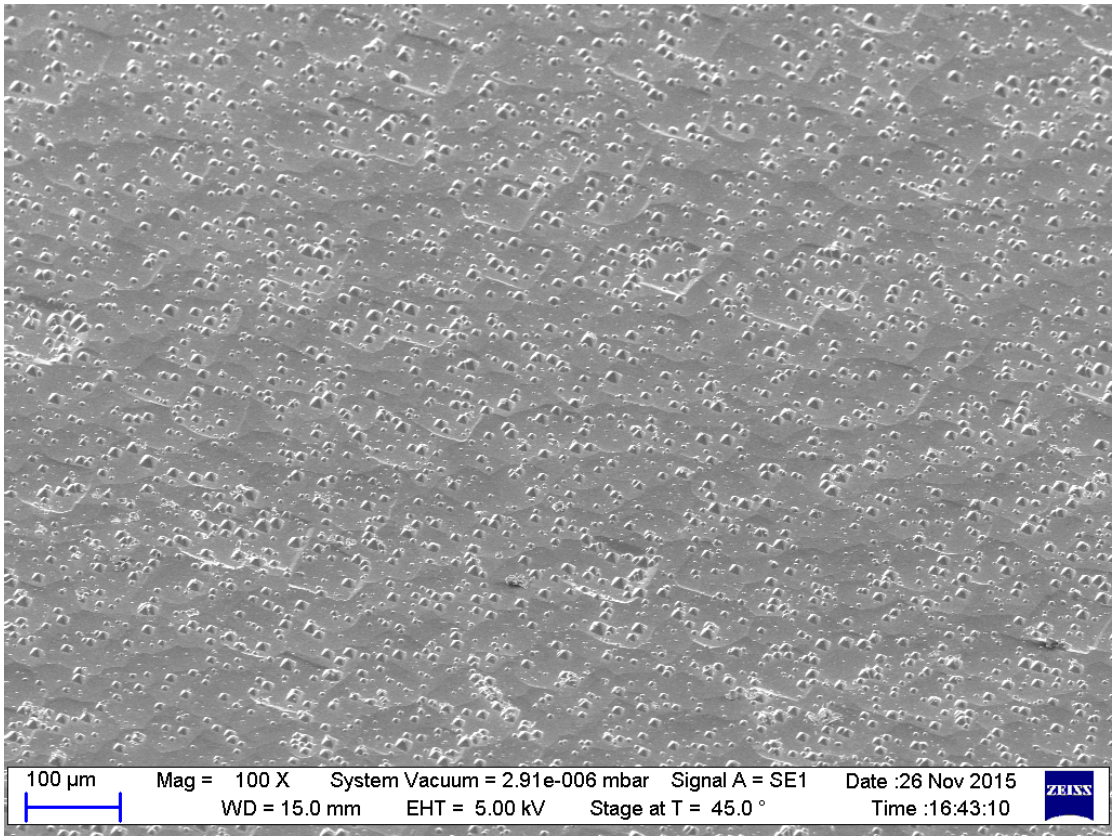


Figure 6.1 - *SEM micrograph of textured silicon surface using NaOH at 100x magnification*

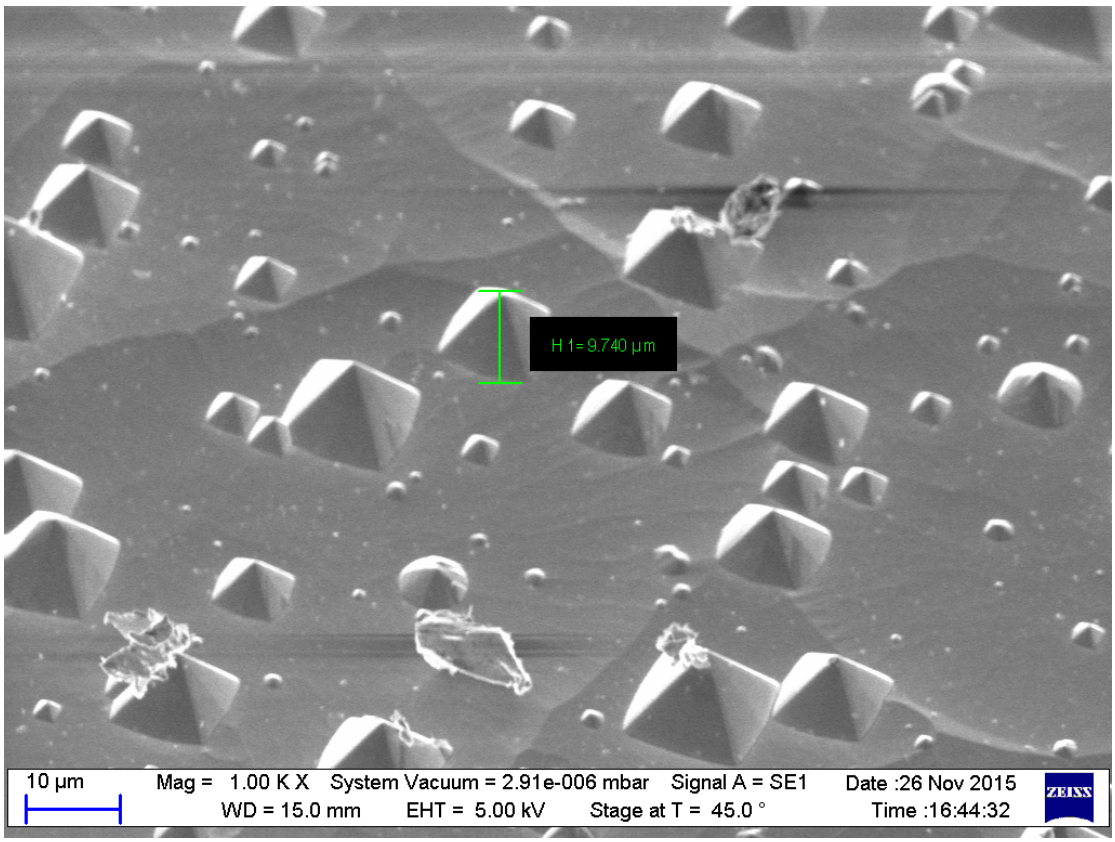


Figure 6.2 - *SEM micrograph of textured silicon surface using NaOH at 1000x magnification*

In order to achieve an optimum antireflective effect, the surface of the wafer needs to be completely covered with random upright pyramids. A literature search produced a recipe by King et al. to form random arrays of random upright pyramids[158]. This method uses a low concentration potassium hydroxide (KOH) solution as opposed to NaOH. The process requires the wafers to be immersed into a solution of 1.5% KOH, 3.8% IPA at 70°C for 45 minutes. Figure 6.3 shows the result of this texturing process at 100× magnification. Observed at greater magnification in Figure 6.4 there are no visible areas that do not have random pyramid structures, and it is a marked improvement on the result of the earlier process shown in Figure 6.2.

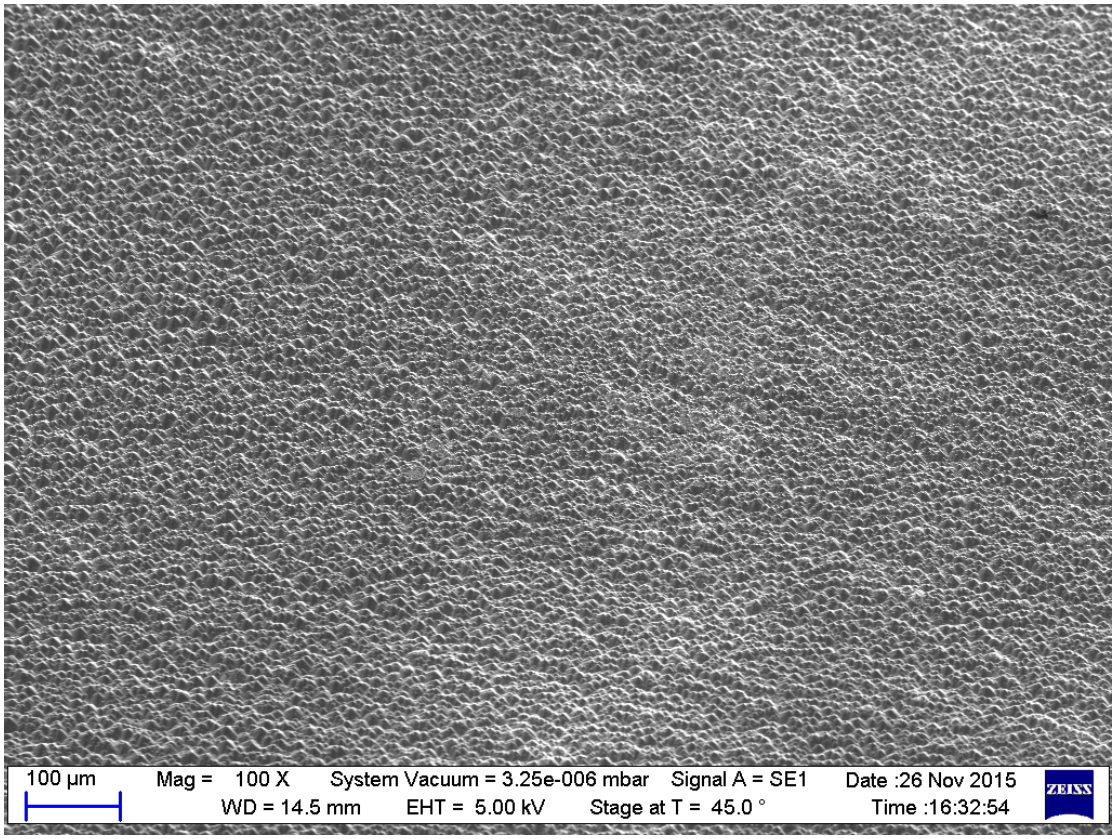


Figure 6.3 - *SEM micrograph of textured silicon surface using KOH at 100x magnification*

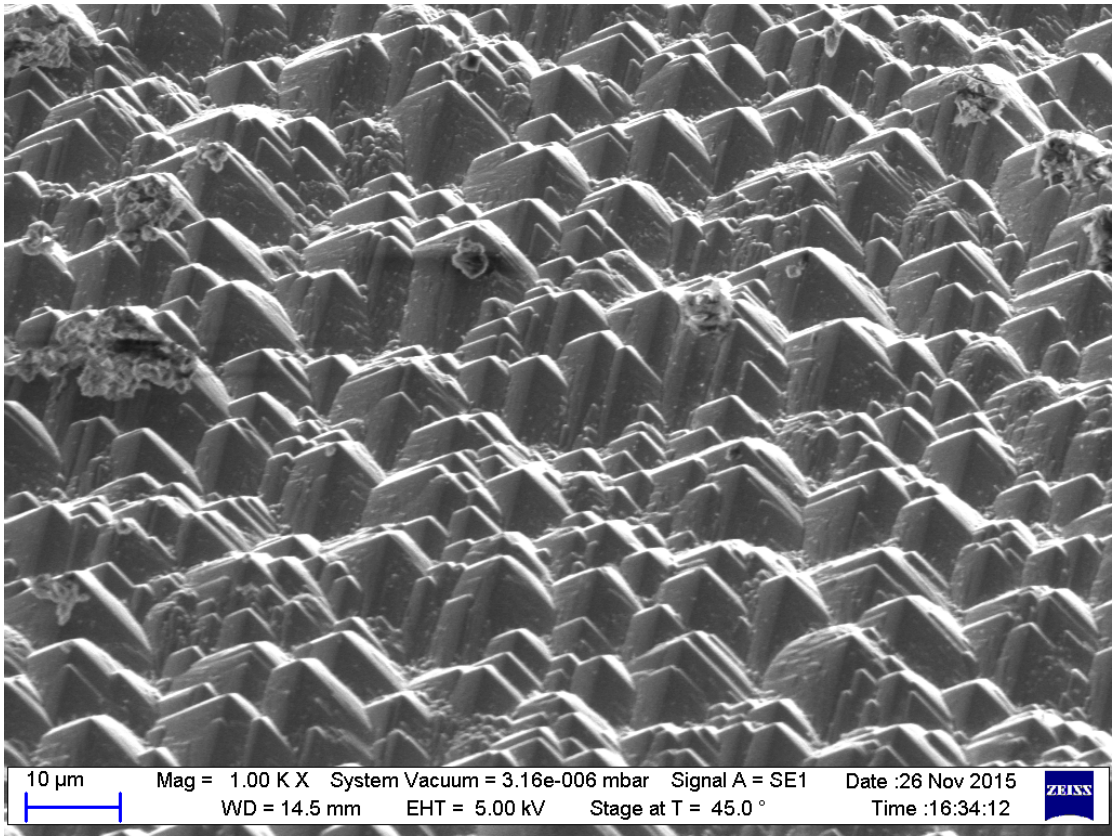


Figure 6.4 - *SEM micrograph of textured silicon surface using KOH at 1000x magnification*

For ease of processing both the front and rear sides of the wafer were initially textured by completely immersing the wafer in the KOH solution. In wafer production there are established processes already used to texture only one side of the wafer and leave a planar surface on the other side. Methods to do this include putting a sacrificial dielectric layer on one surface to act as a mask and protect it from the KOH etch, and polishing one side of a wafer after both sides have been textured [159].

The resulting devices from the experiments done however had electrical shorts between the p and n regions at the rear. Upon inspection of the shorted devices, deposited metal was observed on some of the pyramids on the front surface as shown in Figure 6.5.

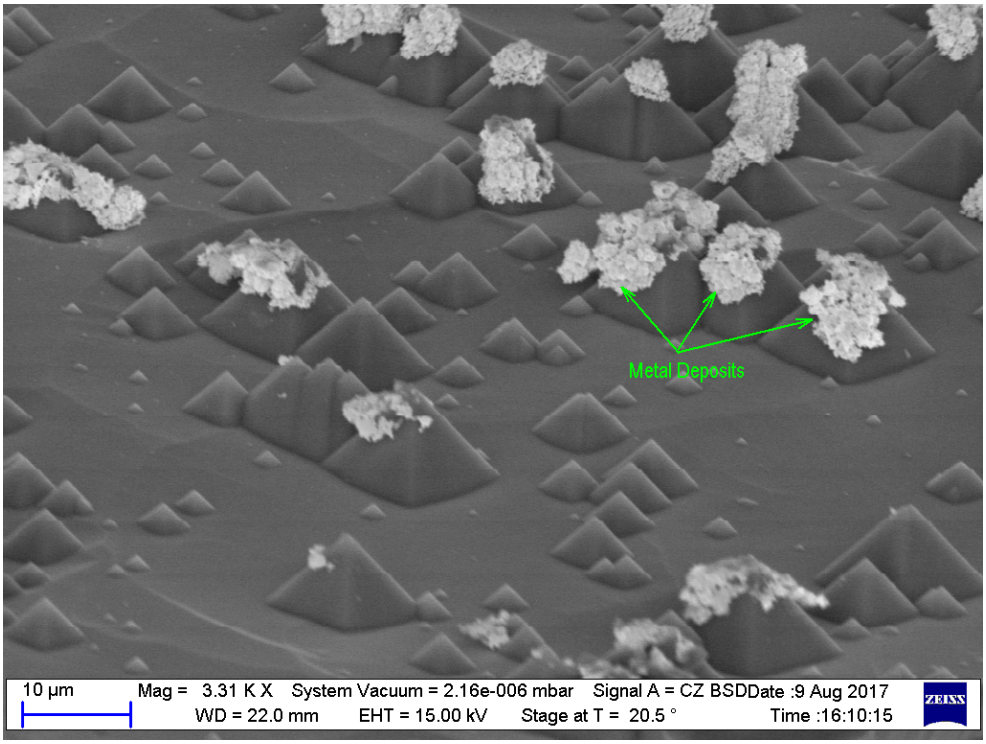


***Figure 6.5** - SEM micrograph of textured silicon surface showing metal deposits*

Whilst the metal deposition on the front surface would not cause a short circuit, any unwanted metal deposited outside the laser cut grooves on the rear surface may form a conductive connection between the N+ doped region and the p-type bulk resulting in a short circuit and a non-working device. The SEM shown in Figure 6.6 shows the cross section of one of the deep grooves. There are metal deposits all across the surface. Figure 6.7 shows a connection between the metal in the n-type groove and the deposited metal on the p-type surface at higher magnification. Figure 6.8 and Figure 6.9 are tilted views showing the excess metal.

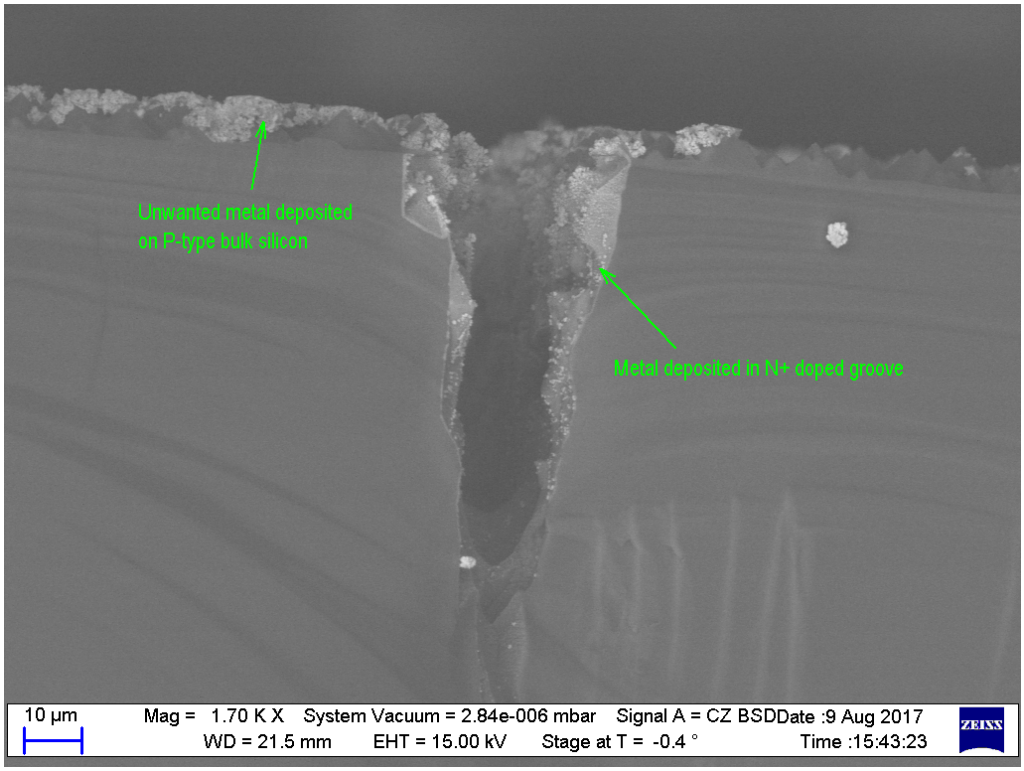


Figure 6.6 - *SEM of textured silicon surface showing surface metal deposits*

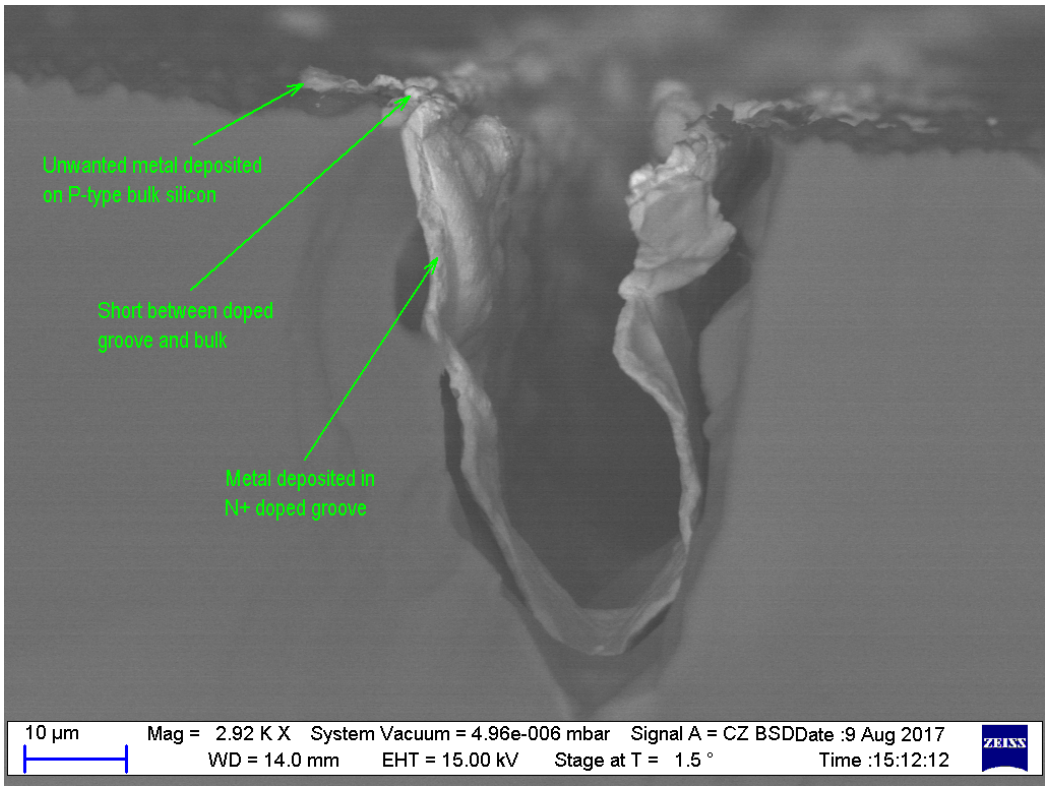


Figure 6.7 - *SEM of textured silicon surface showing metal deposits causing shorts*

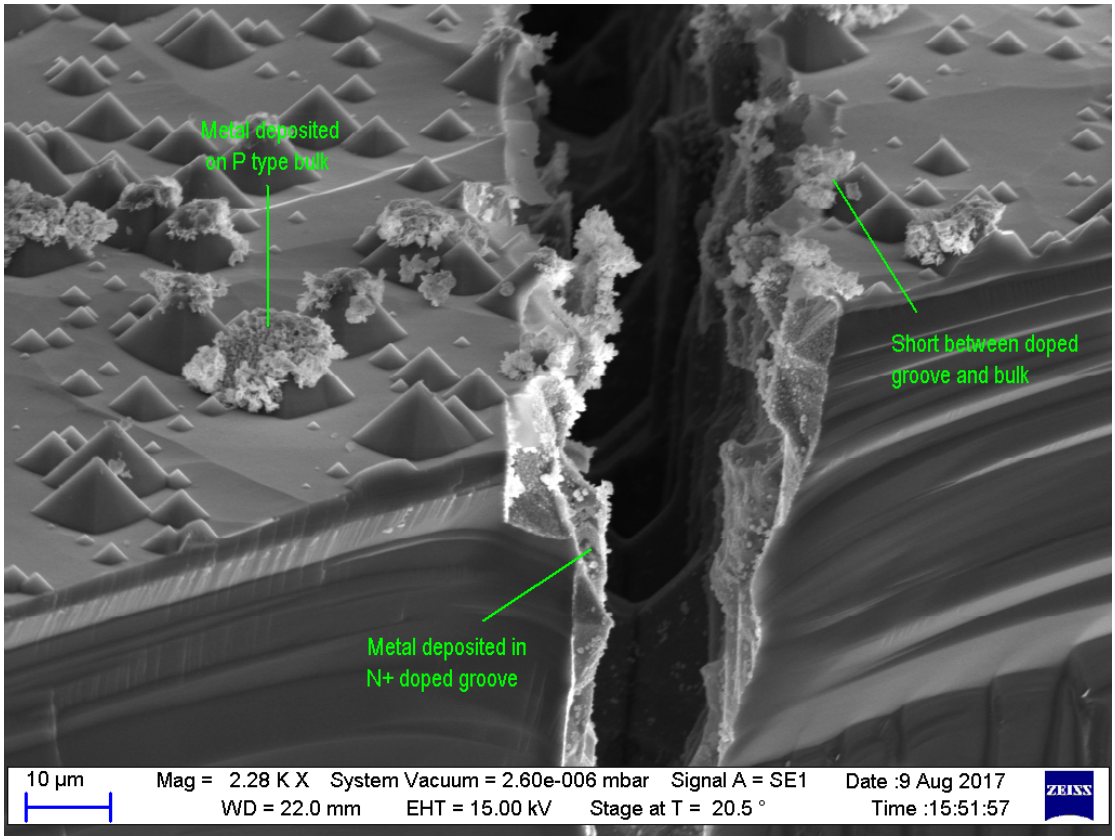


Figure 6.8 - *Tilted SEM of textured silicon surface showing excess metal deposits*

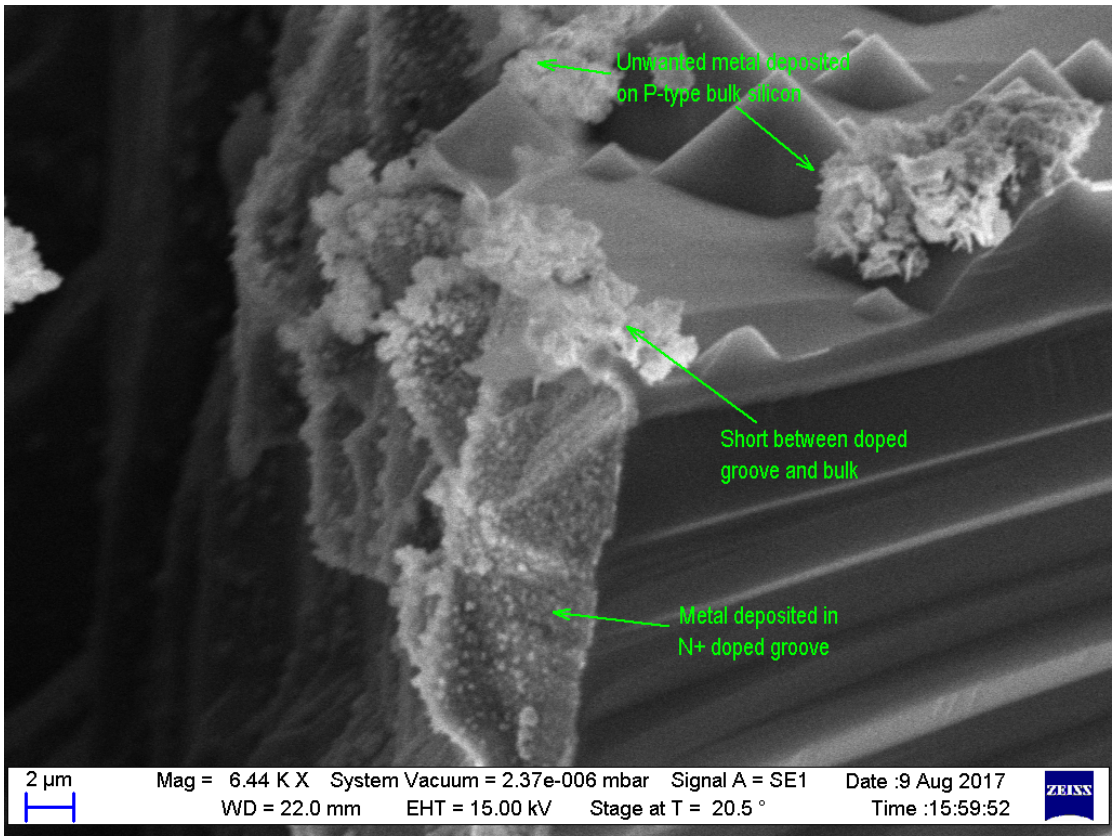


Figure 6.9 - *SEM showing metal contact between P and N+ regions*

The electroless metallisation plating process will only deposit metal on exposed conductive silicon. The rough surface of random pyramids causes microscopic holes in the LPCVD mask allowing some of the bulk silicon to be exposed. Depositing a thicker thermal layer of silicon nitride would be one way of overcoming this problem, however this would involve the wafer being in the furnace at high temperature for longer which is something that is not desirable. Another method would be to use a photoresist mask on the rear surface to prevent it from being textured, however this would vastly increase the processing costs. Because it is a sacrificial layer that will be removed after texturing the cheapest method to protect the rear surface prior to texturing is to deposit a 100 nm layer of PECVD silicon oxide. This is done in the plasma deposition tool, with SiO deposited for 1 minute 40 seconds with a table temperature of 350°C. Figure 6.10 shows grooves in wafers after metallisation. In Figure 6.10 (a) where there was no sacrificial oxide layer before texturing, pyramids can be seen with metal deposits on them. In Figure 6.10 (b) where a sacrificial oxide layer was used, texturing has not occurred leaving a planar surface with no unwanted metal deposits that can cause shorts.

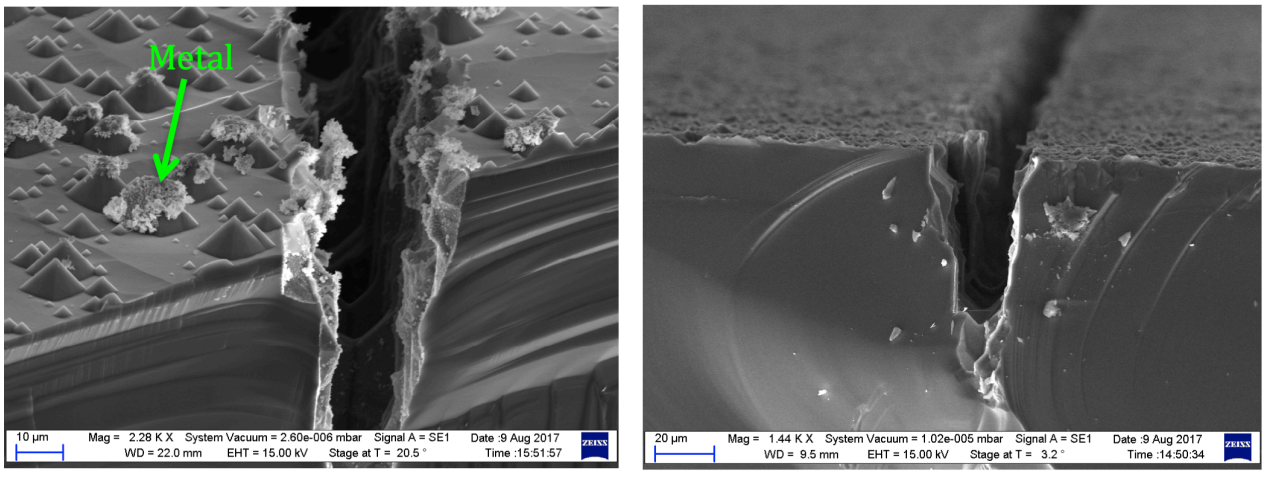


***Figure 6.10** - Metallisation without and with oxide protection before texturing*

6.2 Dry Oxidation

For the proof of concept device as discussed in 4.2.2, wet oxidation was used to grow the passivation layer. However as discussed in 3.3.1, dry oxidation provides a better passivating layer. The ARC thickness modelling performed in section 5.3 confirmed that only a thin layer of oxide is necessary and demonstrates the negative effects on device performance of having too thick an oxide layer. This means that it is possible to grow dry oxide without impacting negatively upon the thermal budget. Dry oxide, like wet oxide, is grown thermally, and from the ARC optimisation modelling a thin layer of 20 nm needs to be grown. Referring back to the graph in Figure 3.10, a furnace recipe that incorporates a 16-minute dry oxidation at 1000°C and a 15 minute anneal in nitrogen will produce a dry oxide growth of 20 nm. Using ellipsometry, the resulting grown layer of dry oxide was measured to be 22 nm (±2 nm) thick. Figure 6.11 is an SEM image of a wafer showing the oxide and nitride passivation layers.

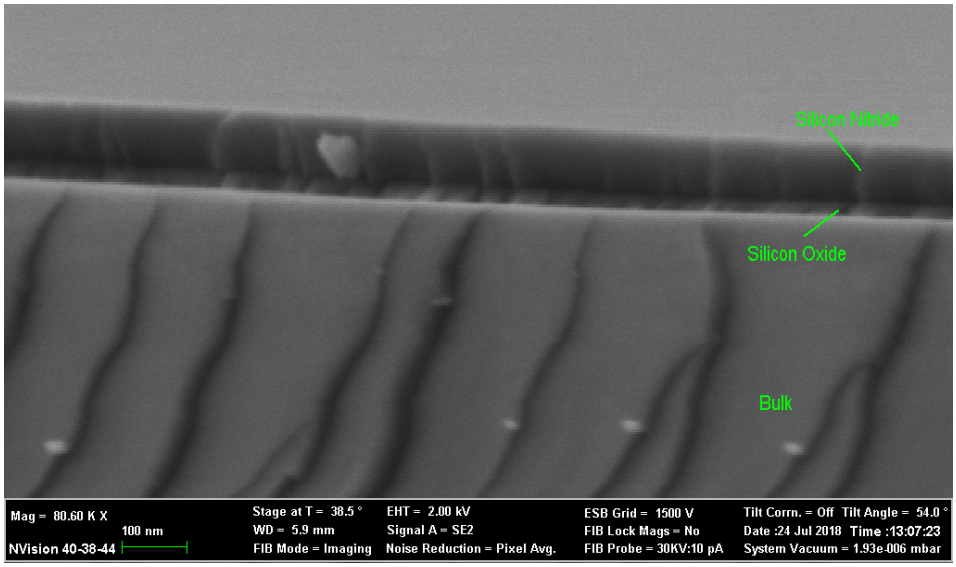


***Figure 6.11** - SEM image of wafer showing the oxide and nitride passivation layers*

These layers are measured at multiple points in Figure 6.12 with the average of these measurements for the oxide thickness being 23.0 nm (±1.1 nm).

6.3 LPCVD Silicon Nitride Thickness

The devices produced in Chapter 4 had no ARC optimisation and were gold coloured, which is a very reflective colour and therefore not ideal as an antireflective coating. By referring back to the ARC modelling in section 5.3, the total silicon oxide/silicon nitride stack making up the front side ARC should be approximately 71 nm thick. This would give a dark blue surface colour which is the traditional colour of typical solar cells available on the market. Following a silicon oxide growth with a thickness of approximately 20 nm from section 6.2, the silicon nitride thickness should be about 50 nm. Figure 6.12 shows multiple measurements of the silicon nitride thickness with the average of these being 89.6 nm (±2.1 nm). This was achieved by running a furnace recipe with a 13-minute nitride deposition at 800°C with dichlorosilane (DCS) and ammonia used as the reactant gases to form the silicon nitride (from equation 3.4). The process was run at a pressure of 200 mTorr.

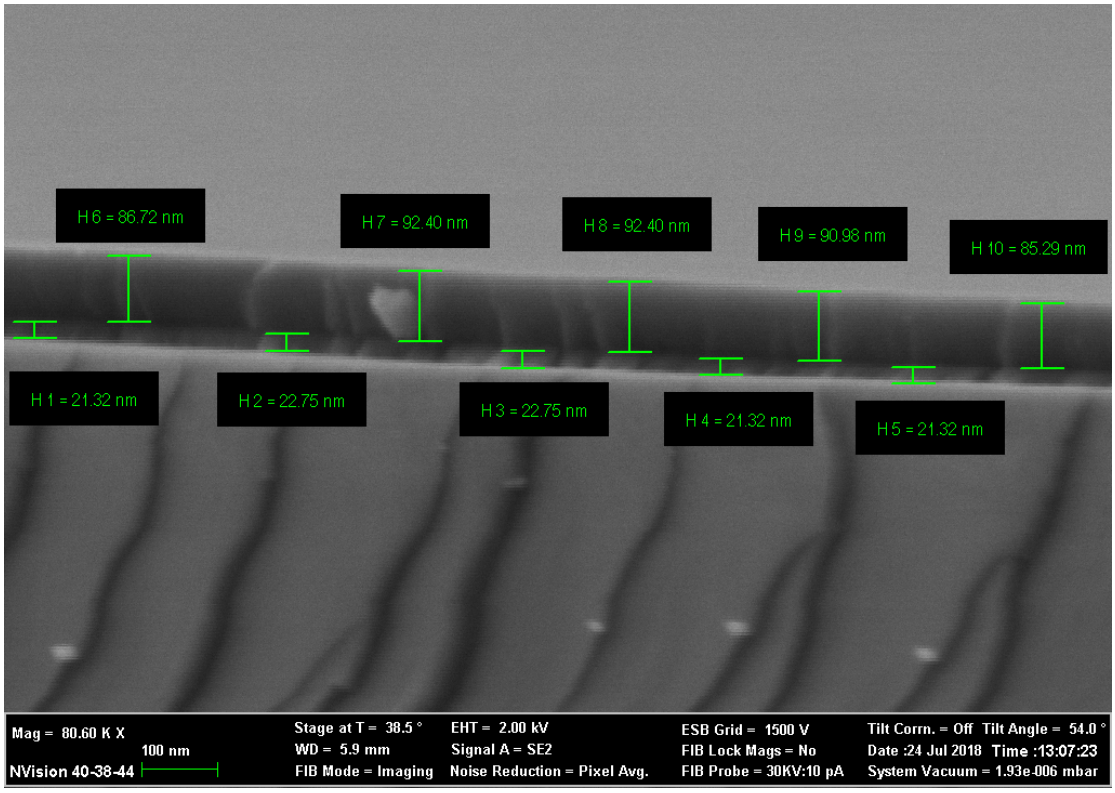


***Figure 6.12** - SEM of wafer showing measurements of the passivation layer*

The optimum thickness of the nitride film for anti-reflective coating purposes is 51 nm as was calculated in the OPAL 2 simulation described in section 5.3. In order to create this optimal nitride thickness, the deposition time can be adjusted further (in this case marginally reduced from 13 minutes).

6.4 PECVD Nitride Groove Wall Passivation

As shown in section 5.8.4, by reducing the amount of metal deposited in the device, the characteristics of the device improve. A proposed method of achieving this it to partially passivate the walls of the deep grooves so that the amount of metal deposited is limited and the grooves are only partially filled with metal. As the POCL diffusion process is the last thermal step proposed, PECVD nitride can now be used for passivation as it will not be subjected to the stresses that could create cracks resulting in excessive plating as shown in Figure 4.7. Figure 6.13 shows how the addition of a thin layer of PECVD silicon nitride can limit the amount of metal that is used to fill the grooves. Because the grooves themselves are deep, this nitride layer should only partially coat the sidewalls of the grooves, leaving only the silicon at the tip of the groove exposed so that the electroless plating process can be performed.

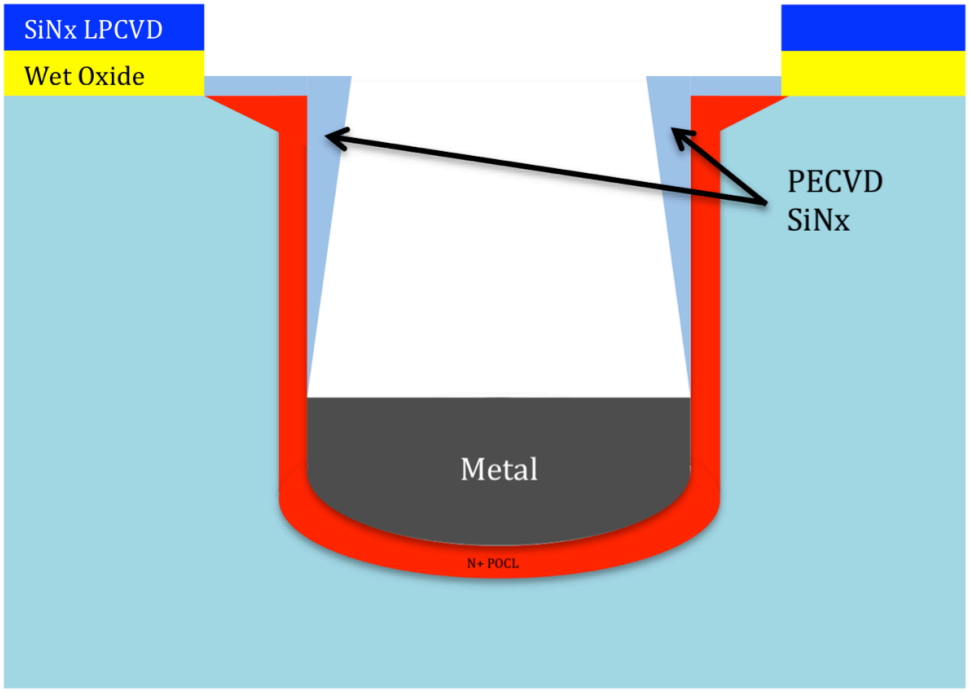


***Figure 6.13** - Diagram of device with PECVD passivated grooves*

6.4.1 SEM Characterisation of Groove Wall Passivation

Figure 6.14 is an SEM image showing a metallised deep groove after the additional HF dip (described in section 4.2.8.3) and PECVD nitride deposition. When a continuity meter was placed across the busbars, no short circuit was detected implying that the initial shorting problems identified in section 4.2.8.1 have not reappeared. However, in order to remove the phosphorous glass and any native oxides that had grown on the exposed silicon prior to electroless plating, further HF dips are required. During this experimental process the additionally deposited PECVD nitride was also removed meaning that unfortunately the entire groove wall was plated with metal as seen in Figure 6.14. If it was possible to remove the phosphorous glass and native oxides without using a process that etched the additional PECVD nitride then this would allow the groove walls to remain passivated. This could possibly be achieved with another laser run where the laser is at a much lower power and is run back over

the already cut groove so as to remove only the phosphorous glass layer or by using a buffered HF solution.

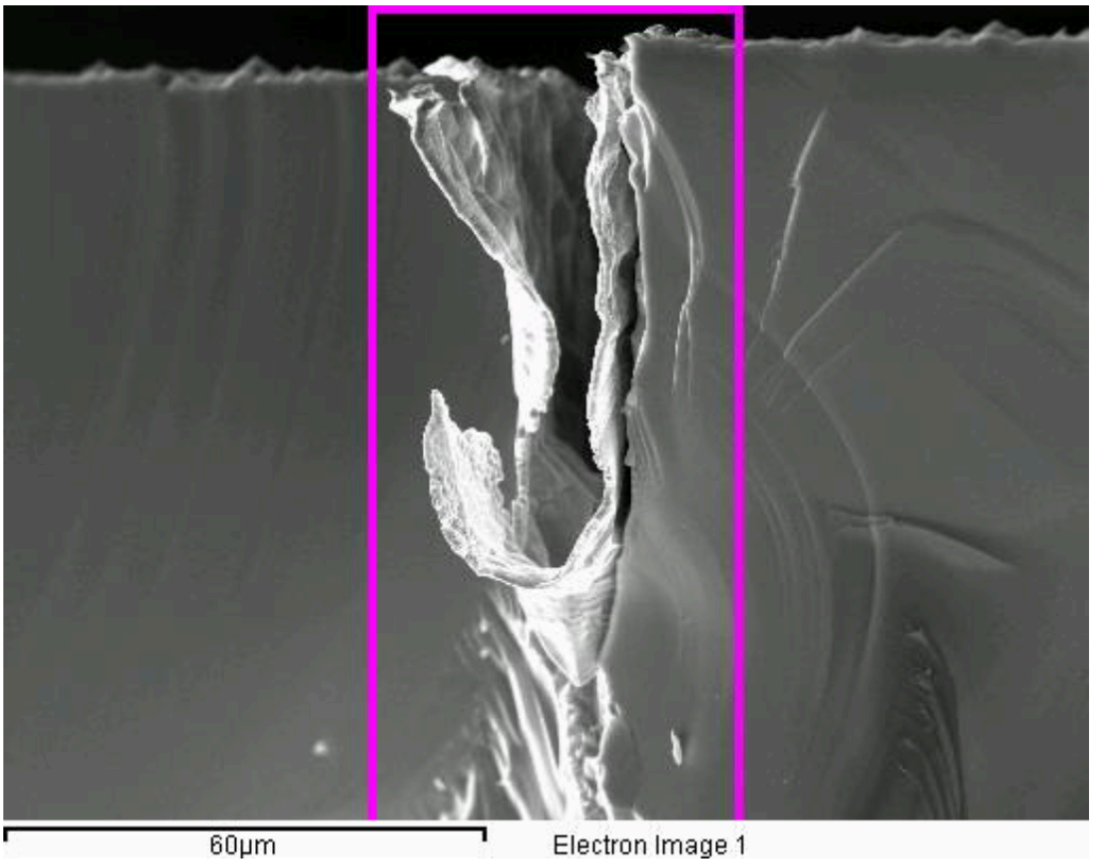


***Figure 6.14** - SEM of a metallised deep groove*

6.5 Back Surface Field

In section 5.8.3 it is shown that improvements to the device can be achieved by the addition of a back-surface field (BSF). This is achieved by doping the silicon in the p-type grooves with a p-type dopant such as boron in order to create a p+ region. Based on machines available for use at the time of this project an investigation was carried out into the feasibility of using hot wire chemical vapour deposition (HWCVD) to achieve the BSF formation. HWCVD allows growth of p-type polysilicon, when grown in a diborane (B_2H_6) environment. In this investigation, a Nitor 301 HWCVD machine developed by Echerkon Technologies Ltd. and shown in Figure 6.15 was used.

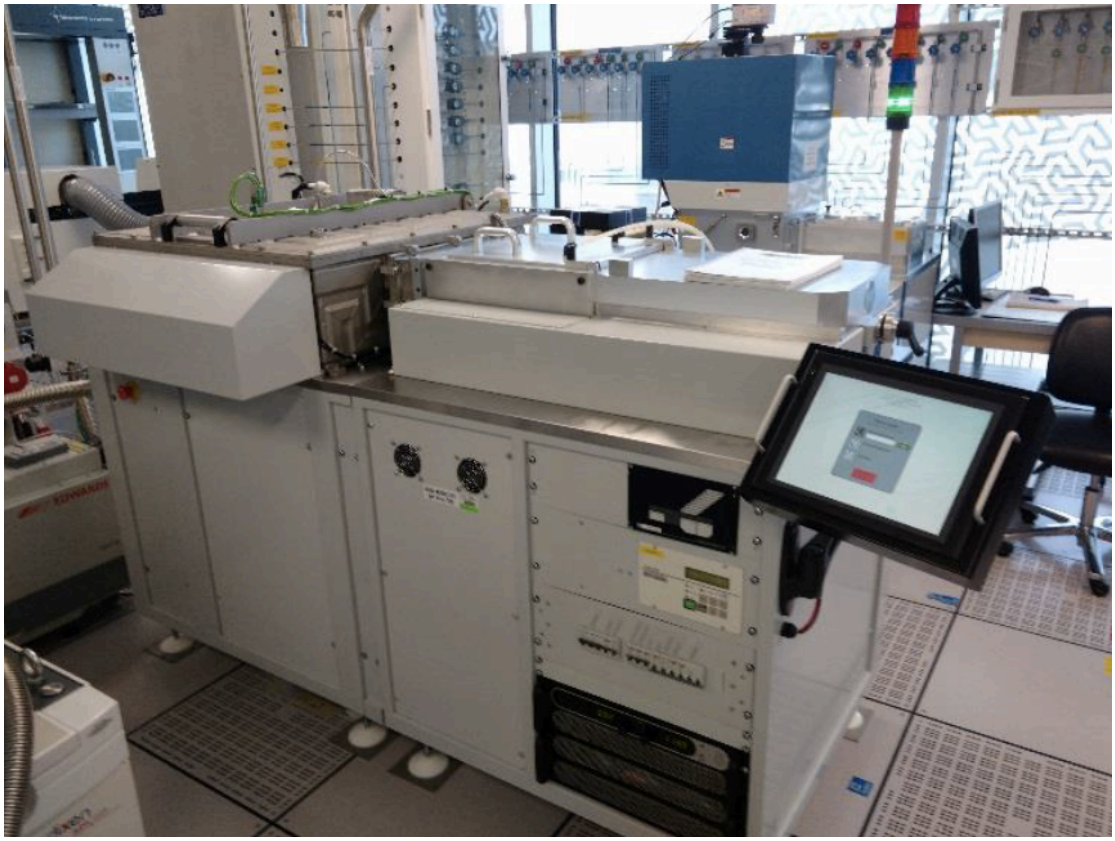


Figure 6.15 - *Nitor 301 HWCVD machine*

The sample wafers need to be stripped of any native oxides and then loaded into the machine within 3 minutes. Silane (SiH_4) enters the chamber before the sample is moved into the load chamber where a choice of process gases are available to be used depending on the desired outcome. For this process, diborane was used to create the p+ back-surface field. The doping levels can be altered by varying the process gases as shown in Figure 6.16, which gives the results of various HWCVD runs performed on blank silicon wafers.

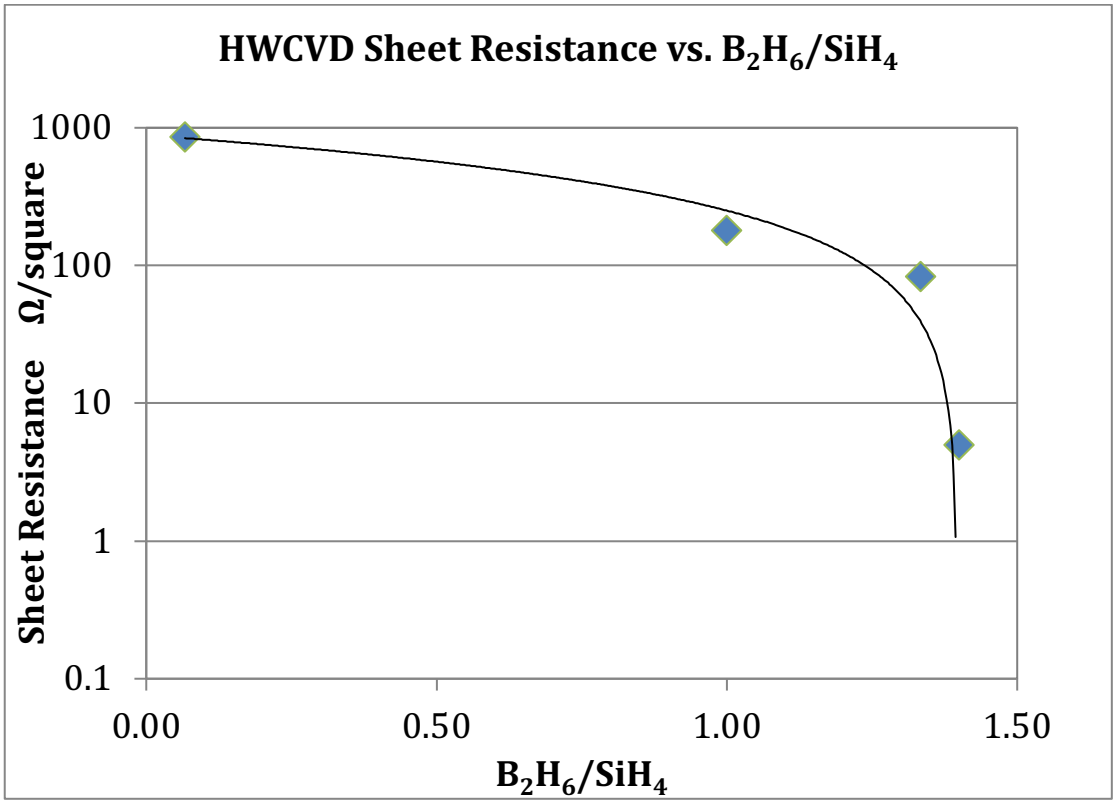


Figure 6.16 - *Graph to show sheet resistance vs. process gasses for HWCVD*

The HWCVD process does not allow for selective doping and a blanket growth occurs across the whole exposed side of the wafer. In order to achieve selective doping, a complex process was used whereby a protective layer of PECVD silicon oxide was deposited on the wafer before the shallow grooves where cut. Once the shallow grooves where cut and the groove damage removed the wafers could be cleaned using the RCA process. Any native oxides where removed with HF taking care not to remove the protective oxide layer and the wafers loaded into the HWCVD machine within 3 minutes so that no further oxides form. Following HWCVD an HF immersion would need to be performed to remove the protective oxide layer and, in this process, lift off the excess p+ growth, leaving P+ doping only in the p-type shallow grooves. These process steps are drawn in Figure 6.17.

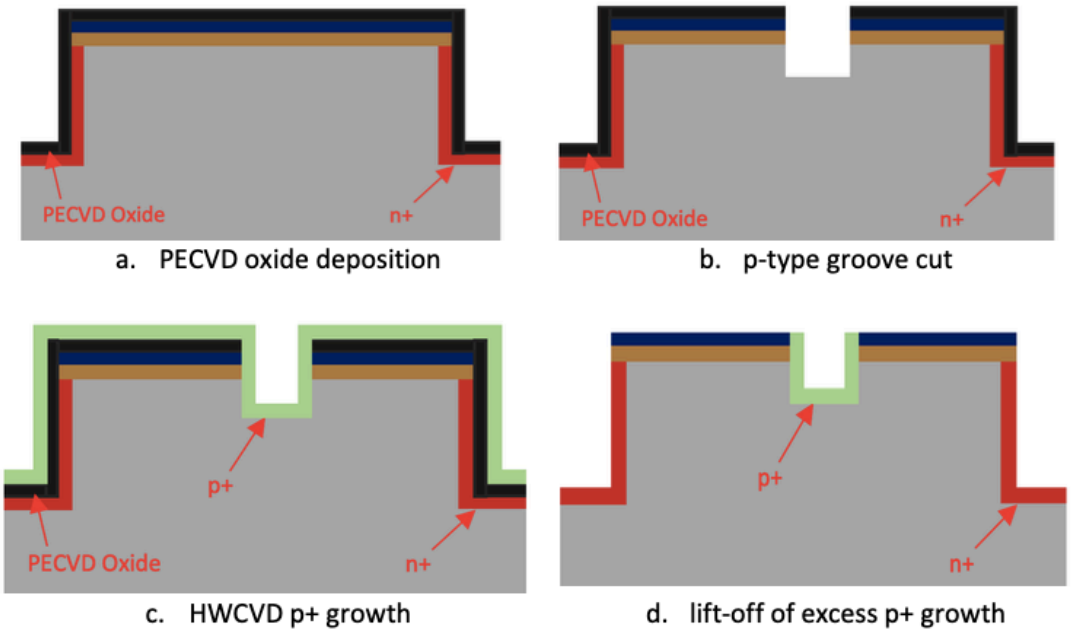


Figure 6.17 - *Proposed HWCVD process steps*

Experimentally, to carry out these proposed processes for the BSF turned out to be very challenging and with the facilities available for this project it was unachievable. The biggest problem was the execution of the lift-off stage, with the margin for error being very fine. It was found that either the HF dip was not long enough in which case the blanket p+ growth remained, or on the occasions that the excess polysilicon was removed, the passivating layer and nitride mask would also be removed meaning that selective metallisation of the grooves was then no longer possible.

6.6 Summary

In this chapter a range of experimental work was completed with varying degrees of success. Experiments were performed to create a front surface textured with random pyramids. A recipe was found that allowed this to be performed after initial failures to achieve a good coverage. The texturing of the rear surface however led to some problems with the device shorting after metallisation. This was overcome by

protecting the rear side of the wafer with a sacrificial dielectric oxide layer resulting in only the front surface being textured.

A better layer of passivation was also experimented with, taking the thickness required to give a good ARC from section 5.3. A switch was made to dry oxidation which is a denser oxide and therefore works as a better passivating layer as shown in Figure 6.18, where a study was done into how minority carrier lifetime was affected by differing oxide types for passivation [160].

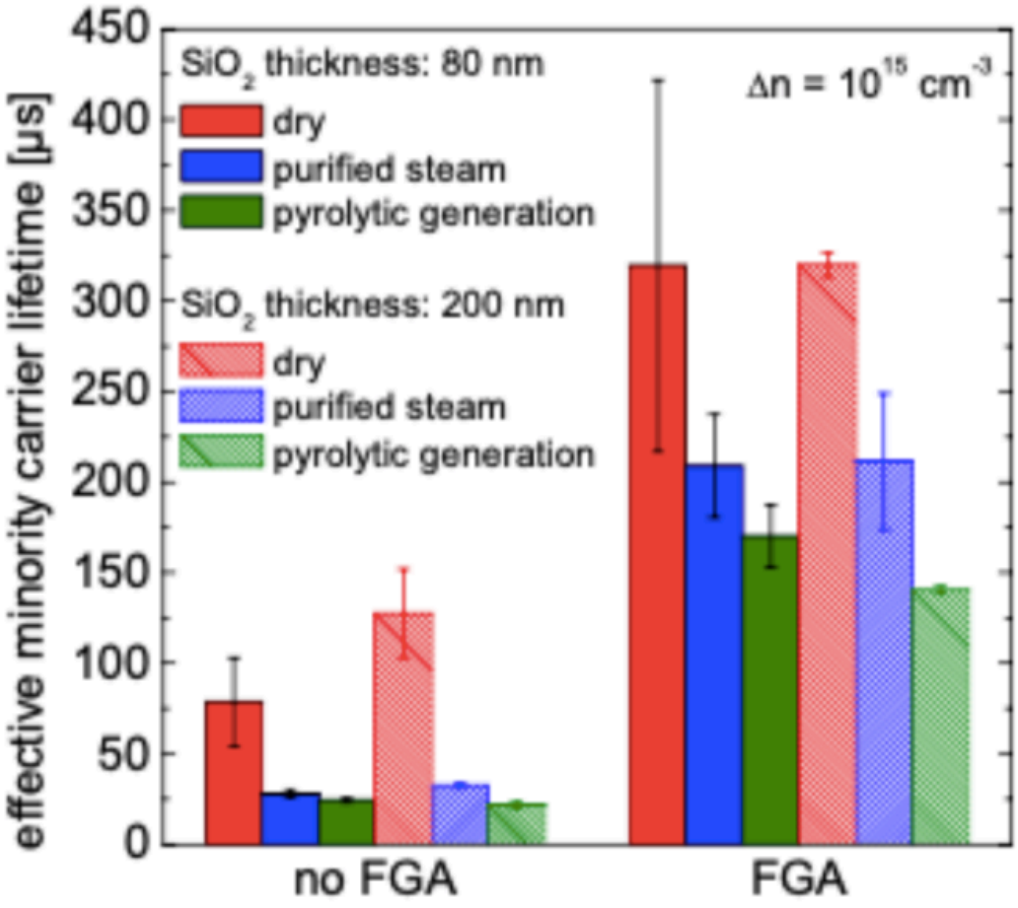


Figure 6.18 - *Passivation quality of wet and dry oxides [160]*

The ARC stack optimisation was completed with a thinner layer of LPCVD nitride that allowed the front surface stack to be close to the optimal levels, as discovered in section 5.3.

As found in the TCAD modelling performed in section 5.8, the incorporation of a BSF and the limiting of the amount of metal deposited in the grooves would yield a better performing device. For this, preliminary experimental work was performed with novel approaches taken. An attempt to limit the amount of metal deposited by passivating the walls of the grooves, whilst novel and theoretically simple to implement, turned out to be unsuccessful experimentally due to necessary processes performed in subsequent steps. Similarly, an approach to growing a p+ BSF using HWCVD proved to be unsuccessful due to the limitations of the facilities available for the experimental work.

Chapter 7 Conclusions and Further Work

7.1 Conclusions

Since the beginning of this project, the field of solar cell development has grown with new technologies emerging and existing technologies improving. The global political situation has also changed, with emphasis being placed on clean energy generation and lowering carbon emissions with many countries committing to rapidly increase their use of clean energy. Of all clean energy sources, solar has remained the preferred technology, particularly in light of the more recent decline in popularity of nuclear power. Within the field of solar cells, silicon based solar cells have remained the dominant technology throughout the period of this project, and according to all road maps will continue so for the foreseeable future. For PV to challenge the position of non-renewable energy production there is still a need for devices to become both more efficient and more cost effective. This continued need to improve clean energy production, along with the forecasted position of silicon based solar cells in doing this gives continued justification to the work done in this silicon technology-based PhD project.

In the literature it was seen that although there is research into the use of lasers in the fabrication of PV devices, the use of them was limited to surface-based treatments. The notion of using lasers to bury contacts within the silicon bulk has only been used for shallow front side grooves such as on the BP Saturn solar cell. The literature review reveals that the development of IBC solar cells has been rapid, and it is the leading approach to creating the most efficient devices, however there has been little

work done to investigate the application of low-cost fabrication methods in this field. The problem with IBC cells is ensuring the emitters and BSFs are locally sited, and the processes typically used to ensure this, such as lithography, continue to remain very costly.

The novel concept proposed in this PhD project of cutting deep grooves into the rear surface of the wafer to bring the charge collection region closer to the charge generation region continues to provide a neat and elegant solution to the problem of creating localised diffusion sites. During the course of the PhD project, patents have been awarded for this original concept.

The approach taken for this project was to start with experimental work. Owing to the proposed geometry being both novel and untried, initial experimental work was done to create a working proof of concept device. Following this, modelling was performed, firstly on top surface texturing and antireflective coatings using OPAL2, and then on the entire device using TCAD. This allowed different parameter settings to be tested quickly and economically to test the potential of this device. Finally, further experimentation was done to investigate methods of improving the original proof of concept device based on the findings of the device modelling.

In Chapter 4, a crude proof of concept device was fabricated. Initial samples produced did not work due to metal climbing out of the grooves and shorting between the p-type bulk silicon and the n+ doped region in the deep grooves. This was overcome by an additional HF dip as detailed in section 4.2.8.3, and a working device was fabricated. This succeeded in proving that the proposed device geometry could result

in a working device and gave justification for the continuation of the project. Although the measured values for the fill factor and shunt resistance of this device were very good, the series resistance, V_{oc}, J_{sc} and overall cell efficiency were all very poor. This was to be expected though, as many already documented process steps that would lead to better results (such as surface texturing) where not performed in this experiment. Furthermore, the steps that were performed (such as front surface passivation and ARC) were not optimised, with arbitrary values being used as the purpose of this experiment was only to see if a working device could be fabricated. The next stage of the process development was to use a computer-generated model to investigate what the effects of further processing steps would have on the device. Sentaurus TCAD was used as the modelling package and the device was built using it as described in section 5.6. The model allowed experimental data that would have taken many weeks to get to be obtained within a matter of hours. These modelling investigations proved that the unique concept of this project, the deep laser cut emitter grooves, do increase the overall device performance for rear contact solar cells. The deeper the grooves are, the better the device performs, the modelling showing generation efficiency increases from 5.5% to 16.5% as this parameter is optimised. This goes further to lend credence to the work done for this project. The modelling investigations also allowed optimisation of the front surface passivation, and emitter. It also revealed that the addition of a back-surface field would also improve the device further taking the generation efficiency from 16% to 17.5%. The current processing done so far for this project resulted in a large amount of metal being deposited in the grooves to allow the device to be connected to. A further modelling investigation went on to show that if this amount of metal could be minimised, the

device could potentially perform better still to in excess of 20.5% once all the other parameters had been optimised.

Following the successful proof of concept, further work was done to try to experimentally implement the findings of the modelling chapter. Experiments were performed to create surface texturing (which is a process widely used in PV device production for many years). The front surface stack of silicon dioxide passivation and silicon nitride ARC were successfully optimised both for passivation purposes and light trapping with further shorting problems being overcome. Experimental work was also done on a novel concept to try to reduce the amount of metal deposited in the grooves by partially passivating the groove walls which was not successful. The implementation of a BSF was also investigated with attempts to deposit doped silicon using HWCVD. This again did not prove successful.

The original aim of this project was to develop a cost-effective approach to an efficient solar cell. Whilst the working experimentally produced devices did not result in efficient devices, the modelling of the proposed device showed that a competitively efficient cell was theoretically possible. At no point in any of the fabrication were costly processes such as photolithography used, so the aim of producing a working device without increasing expense was achieved. When the project was started, the price of high bulk lifetime wafers was significantly greater than low bulk lifetime wafers which meant that only low bulk lifetime wafers were considered. Over time, the price gap between standard and high efficiency wafers has shrunk[161] (for 156 mm monocrystalline wafers, the price difference between standard and high lifetime wafers is about $0.04 USD per wafer[i]). This means that using high lifetime wafers would no longer defeat the cost saving objectives of the project.

[i] Pricing correct as of 3rd October 2019 [161]

Although the device efficiencies obtained from the modelling in Chapter 5 are not rivalling some of the other technologies that are available on the market, there are some applications that this device geometry could be suitable for which could be confirmed by further modelling as outlined in section 7.2. As a lot of the bulk has been removed from the device during laser processing, the device becomes potentially more flexible than a standard solar cell. The laser program can be adapted to enable further investigations into how the groove depth and pitch would affect flexibility. During experimentation, with a narrow groove pitch, the wafer did start to curl although as shown in section 5.9.2 the groove pitch does have an effect on the device performance. There are applications in which flexibility would be a useful property in a solar cell, so this geometry could have applications here. Furthermore, due to all of the contacts being on the rear of the device, the front surface becomes more aesthetically pleasing. The aesthetics of solar cells are often important in residential construction whereby architects try to incorporate renewable energy sources into building without them being overtly visible. Aesthetics of buildings are also an important consideration for planning departments, so an aesthetically pleasing solar cell could have applications here too. When compared to traditional solar modules, the aesthetics are also improved when the cells are put into a module as the tabbing that connects the cells together to create a string can be hidden as contacting is only done at the rear of the cell. This also means that there can be a much smaller gap between the cells when assembling the module.

Finally, as the metal is only in the grooves, the gaps between the grooves can still function and add to the output of the device, therefore possibly making this technology suitable for use as a bifacial cell. Bifaciality was not modelled in Chapter

5, so how this device compares to existing bifacial cells would need to be investigated.

Over the last decade, the available devices and benchmarks for highly efficient devices have moved on considerably. Record devices are now built using hybrid technologies, combining one technology with another such as the Kaneka IBC-SHJ [62] cell. Going forward, the proposed device geometry of this device could also be used in hybrid cell situations, as this would give the ability to produce IBC devices at low cost. Possibilities of this could be the application of the technology in silicon-perovskite tandem devices.

In summary, when this project was started in 2011 the limiting factor for cost-effective PV cell production was the quality of the wafers which in turn impacted upon the PV cell performance. The concept of an IBC cell with the emitter placed in a deep groove so as to make it as practicably close to the front surface was designed to extract the maximum performance from lower quality wafers by maximising the current collection. At the completion of the project, the cost of silicon wafers has become much more competitive with the availability of low-cost wafers with greatly improved (100 times) higher minority lifetimes negating the potential gains that were sought by putting emitters in deep rear side grooves. This project has shown through computer modelling that the concept of placing the emitter in a deep rear side groove could potentially have efficiencies of around 20% if metal-in-groove recombination is able to be avoided (17% if not). The processes and equipment available to undertake experimental work meant that whilst proof of concept devices were able to fabricated, the best efficiency achieved was only about 1%

7.2 Suggestions for Further Work

One of the limiting factors discovered in this project was the difficulty experienced achieving good realignment when reinserting wafers into the laser machine. As shown in Figure 7.1 the wafer is aligned against 4 bolts. This is a rather crude method and makes it very challenging for the wafer to be reinserted in the exact same position that it was previously.

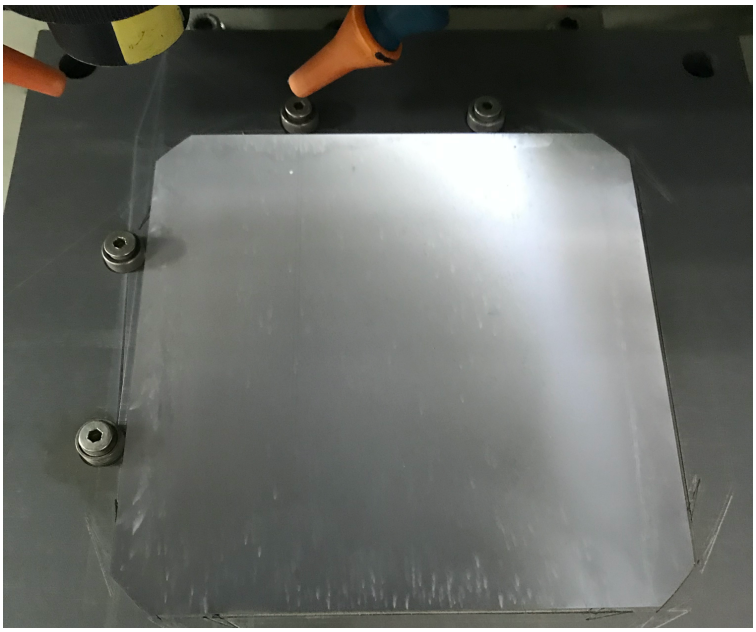


Figure 7.1 - *Wafer loaded on laser stage*

This problem was first discovered when trying to reinsert the wafers following the deep groove processing, meaning that often the shallow grooves would converge with the existing deep grooves during processing. As this wafer mounting system was the only one available during this project, the problem was overcome by widening the gap between the grooves so as to tolerate the realignment errors.

With a more accurate method of alignment, it would have been possible to cut a groove and then on reinserting the wafer into the laser, re-run the laser over the same groove. Further work based on a system like this would easily allow the grooves, once cut, to have a protective passivation layer deposited over them which could then be

selectively removed by the laser when needed. This would enable the BSF to be formed by protecting the already doped deep emitter grooved and allowing a localised boron diffusion to be done only in the shallow grooves. Furthermore, the laser could be used to selectively reopen the emitter, therefore minimizing the amount of metal deposited into the groove. The process list incorporating this suggested work to work already done is detailed in Table 7–1.

There are also interesting investigations that could be carried out into using the heat generated by the laser to allow localised diffusions of both emitters and BSFs where the dopant could be either spun or sprayed on once the groove has been opened and then the laser could pass over again to drive the dopant into the silicon. This would negate the need of furnace processing for dopants, thereby lowering the fabrication costs further as well as implementing device performance improvements caused by having a localised doped region that were modelled in section 5.8.6.

The modelling work done in this project could also be built upon in the future. A model for a front junction device could be built which would allow for a direct comparison to be made to investigate whether cutting deep grooves to form a rear side emitter would produce higher efficiency devices. Furthermore, as was mentioned in section 5.6.1, the time and computational resources available for this project were prohibitive for a full 3D simulation sweep to be performed. This has meant that the simulations were only done in 2D with a 3D simulation done only on the optimised parameters for a 2D model. This has led to compromises resulting in simulations that have given conservative predictions. With greater computing resources a full set of sweeps using the 3D simulation would allow for much more accurate predictions to be generated for solar cells using this device geometry. This could also further allow a design of experiments approach to be applied to the parameter optimisations which is

a better alternative to parameter sweeps. With this approach it would then be possible to find a global optimum set of design parameters for this device geometry. Additional modelling could include an investigation into how the device performs as a bifacial cell to see if there are any further applications for this device geometry.

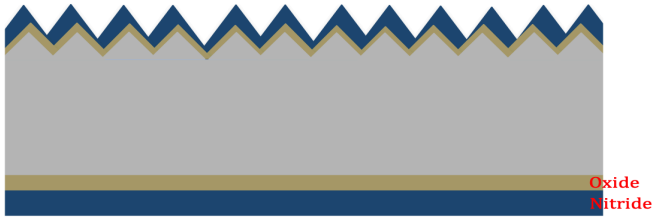
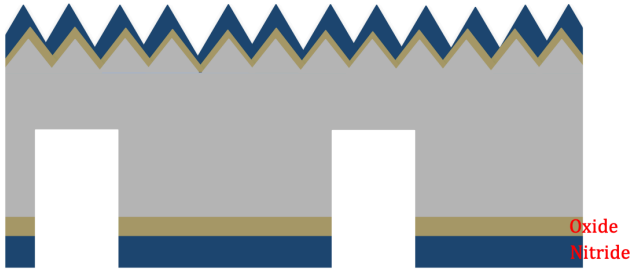
7.3 Proposed Improved Device Process Step Listing

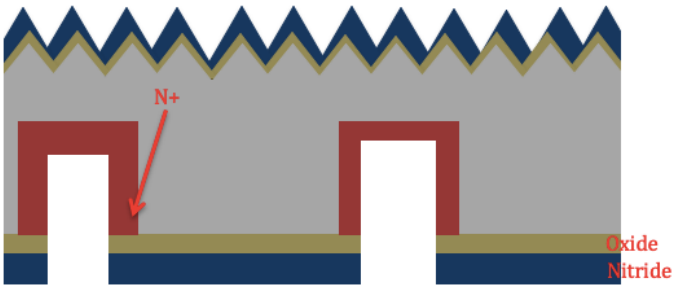
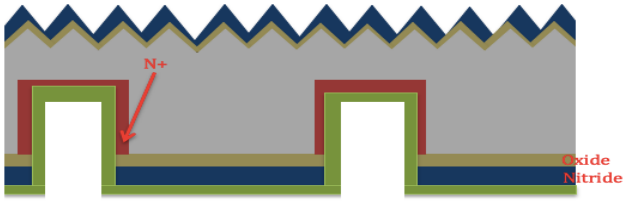
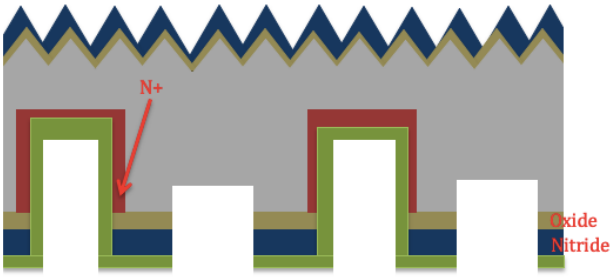
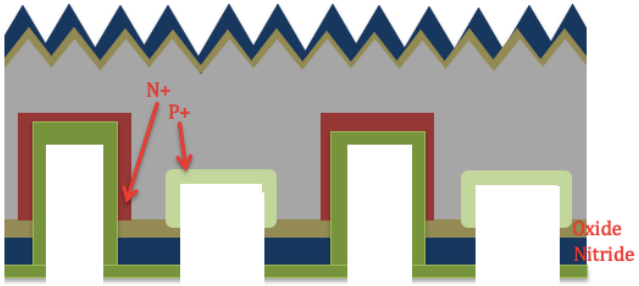
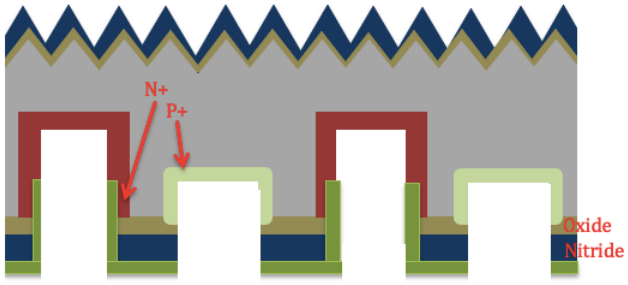
Adding the suggested future work to overcome the some of the experimental problems experienced in Chapter 6 to the already established methodology from Chapter 4 gives the proposed process step listing shown in Table 7–1. This process step listing requires the wafers to be realigned in the laser as described in section 7.2. With this ability and further processing optimisation, it should be possible for devices to be fabricated with efficiencies exceeding 20.5% as described by the TCAD modelling in Chapter 5. The proposed fabrication process involves 17 process steps, which may make it difficult to compete with other types of cells that are being made with fewer processing steps and achieving higher efficiencies.

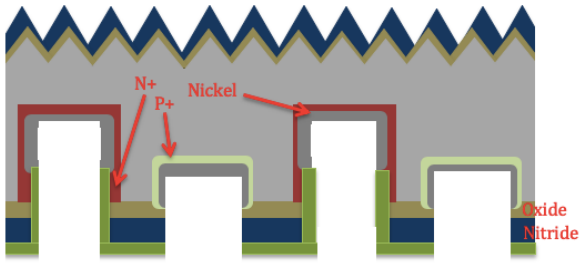
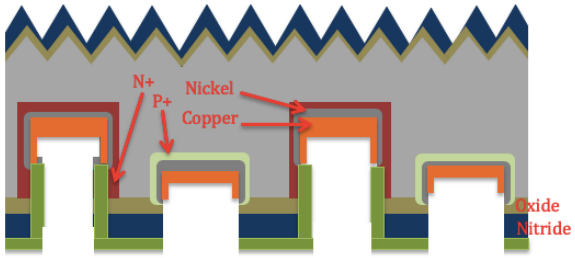
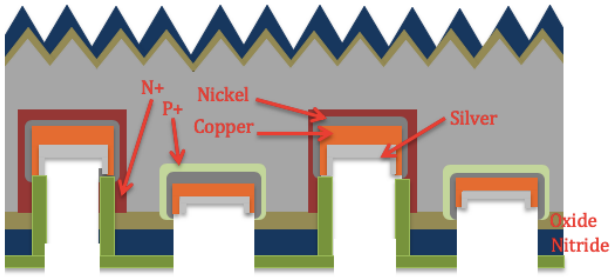
***Table 7–1** – Proposed improved device process flow*

Colour	*Material*	*Colour*	*Material*
	Silicon		PECVD Nitride
	Wet Oxide		Nickel
	LPCVD Nitride		Copper
	POCL		Silver
	PECVD Oxide		BSF

#	Cross Sectional Diagram of Wafer after Process Step	Details of Process Step
1		**Saw damage removal** – 30% NaOH at 80°C for 5 mins. Followed by RCA cleaning

2		**PECVD Oxide Growth** – 100 nm PECVD silicon dioxide growth on rear
3		**Texturing** – 1.5% KOH 3.8% IPA at 70°C for 45 minutes
4/5		**PECVD Oxide removal** with HF then **Dry Oxidation** – 16-min dry oxidation at 1000°C followed by a 15-min anneal. Target 20 nm of dry oxide
6		**LPCVD nitride deposition** – 12-minute deposition in furnace. Target 51 nm of nitride
7		**N-type groove cutting**. Deep groove cut at 3.5 kW to give groove depth of 140 µm. 10% NaOH dip at 60°C for 10 minutes groove damage removal followed by 30 sec 7:1 HF dip

8		**POCL Groove Diffusion** – 20-minute $POCl_3$ diffusion at 930°C followed by a 10-minute drive in at 950°C to give sheet resistivity of 10 Ω/□
9		**Emitter Protection** – 40 nm PECVD deposition of silicon nitride
10		**P-type groove cutting**. Shallow groove cut at 2.5 kW to give groove depth of 30 µm. 10% NaOH dip at 60°C for 10 minutes groove damage removal then 60s 10% HF phosphorous glass removal
11		**BSF** – doping of the shallow grooves using a P+ material such as boron.
12		**Laser Opening for Metal Deposition** – Rerun deep groove cut at ultra-low power to open emitter contacts

13/14/15		**Nickel Deposition** – Enthone AL100 process run at 60°C for 60 seconds followed by 10-minute sinter at 400°C and activation by a 2-minute dip in 20:1 hydrochloric acid at room temperature
16		**Copper Deposition** – Enthone CU240 process run at 50°C for 60 minutes
17		**Silver Deposition** – Enthone AG410 process, 30 second pre-dip at 40°C followed by 2-minute plating dip at 50°C

Appendix A Additional SEM Images

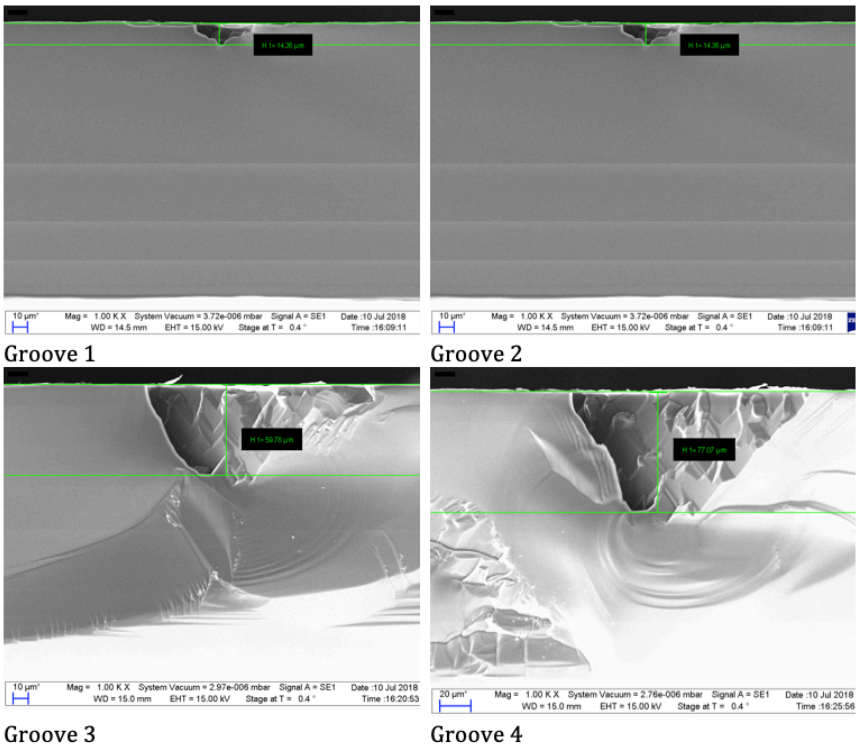


Figure A-1 *- Grooves cut at 200 mm/min table speed*

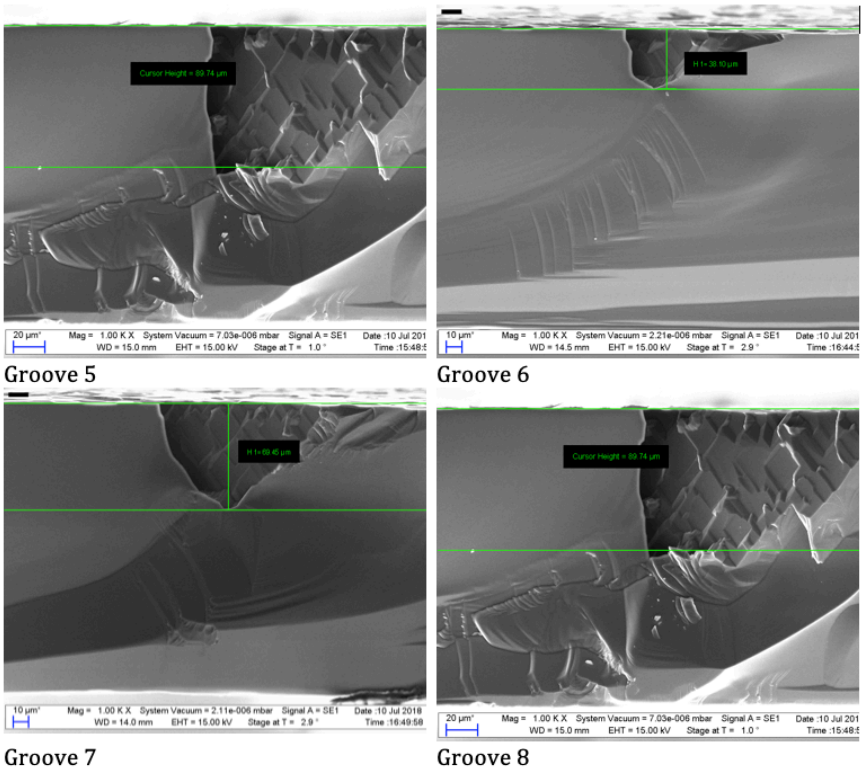


Figure A-2 *- Grooves cut at 100 mm/min table speed*

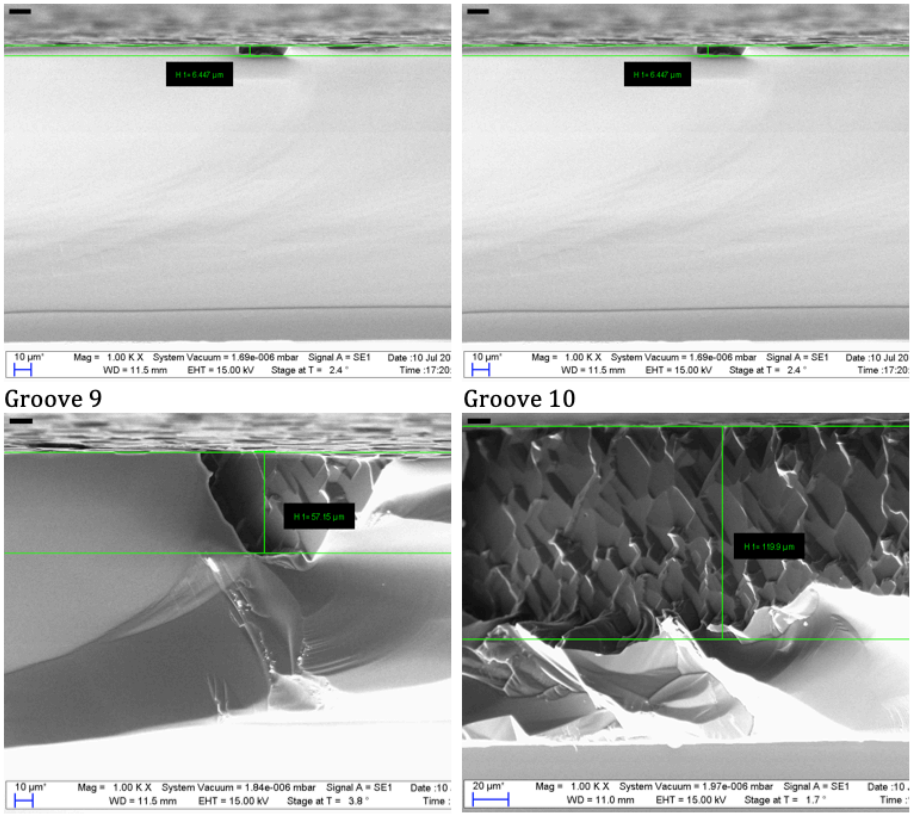


Figure A-3 - *Grooves cut at 50 mm/min table speed*

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