UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES

School of Electronics & Computer Science

Silicon-based Ultrathin Layers for Hole-Selective Contacts in Silicon Solar Cells

by

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ABSTRACT

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SILICON-BASED ULTRATHIN LAYERS FOR HOLE-SELECTIVE CONTACTS IN SILICON SOLAR CELLS

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This thesis presents a collection of work investigating the optoelectronic properties of atomic layer deposited silicon nitride nanolayers as a hole-selective tunnelling layer in passivating contacts for silicon solar cells. We also look at forming p-type polycrystalline silicon as charge modulation layers for such contacts via hot wire chemical vapour deposition. Carrier-selective passivating contacts are currently the state-of-the-art in terms of exceeding current power conversion efficiency barriers in high performance solar cell architectures. To date, less success has been achieved with hole-selective contacts than with electron-selective contacts. In this thesis, we first study the growth quality of polycrystalline silicon films using a hot wire process. We optimise the morphological characteristics towards creating more uniform films that require minimal post-deposition heat-treatment. Following this, we investigate using ultrathin silicon nitride as a tunnelling layer that can both reduce parasitic losses associated with charge carrier recombination and promote hole transport. For the first time in literature, we present an experimental report on the band alignments at the SiN-Si heterojunction interface, showing favourability towards hole transport. We then look at contact formation using various metal electrodes on our heterojunction, studying the specific contact resistivity. Finally, we show the prospects of a poly-Si/SiN/Si heterocontact via Sentaurus TCAD, with direct comparisons of carrier tunnelling probability and tunnelling current in a tunnelling oxide passivating contact counterpart. For SiN and SiO_2 films of equivalent thickness, hole current densities are predicted to be at least ten times higher in SiN. This work takes important steps towards forming high-performance carrier-selective contacts that can be utilized in multiples avenues of photovoltaics research.

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1. **Khorani, E**, McNab, S, Scheul, T.S., Rahman, T, Bonilla, R.S., Boden, S.A. and Wilshaw, P.R. (2020). Optoelectronic properties of ultrathin ALD silicon nitride and its potential as a hole-selective nanolayer for high efficiency solar cells, APL Materials, 8, 111106.
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5. Mercier, T.M, Krishnan, C, Rahman, T, **Khorani, E**, Shaw, P.J, Pollard, M.E, Boden, S.A, Lagoudakis, P.V, Charlton, M.D.B. (2020), High symmetry nano-photonic quasi-crystals providing novel light management in silicon solar cells, Nano Energy, under review.

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2. **Khorani, E**, Scheul, T, E, Tarazona, A, Rahman, T and Boden, S.A. Boron-doped silicon growth via Hotwire CVD towards emitter formation for interdigitated back-contact silicon solar cells, PV-SAT 15, Warwick, United Kingdom. 10 – 12 April 2019.
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Declaration of Authorship

I, Edris Khorani, declare that the thesis entitled silicon-based ultrathin layers for hole-selective contacts in silicon solar cells and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

• This work was done wholly or mainly while in candidature for a research degree at this University;

• Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;

• Where I have consulted the published work of others, this is always clearly at tributed;

• Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;

• I have acknowledged all main sources of help;

• Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;

Signed:.....

Date:.....

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Chapter 1

Introduction

1.1 Motivation for Photovoltaics

Our ever-increasing global energy demands have rapidly escalated the pressure put on our natural fossil fuel reserves, as well as amplifying the environmental detriment from using these non-renewable energy sources. The total share of global electricity production using fossil fuels has consistently remained above 60 % since 1990, with the current consumption reported at 65 % [1], [2]. This is the equivalent of almost 11 billion tonnes of oil in fossil fuels every year, equating to over 35 billion tonnes of annual CO_2 emissions [3]. At this rate of consumption, a maximum period of only a few hundred years' supply of fossil fuels is predicted. Furthermore, the increasing CO_2 emissions intensify the greenhouse effect, which in-turn traps the solar radiation within the earth's atmosphere and results in global warming. In fact, out of the 17 warmest years ever recorded to date, 16 have occurred since 2001 and a global temperature increase between 2 - 5 ^{o}C is forecasted by the year 2100 [4]. Further studies on this matter have shown that the severity of damaging human-induced change depends not only on the magnitude of the change but also the potential of irreversibility, where 1,000 years of irreversibility is predicted from our current activities [5]. Clearly, the world must find alternative energy sources to supply such high demands and to decelerate the current deterioration of non-renewable sources. Inevitably, renewable energy provides the most viable and sustainable solution to this problem, with the type of which typically dependent on geographical prospects and technological progress. Currently, a total share of only 10.4 % of electricity generation and 5.0 % of total energy generation is globally sustained through renewables [6].

Amongst all renewable energy sources, solar energy is considered key towards a completely 'green' future. Photovoltaic (PV) technologies offer great promise due to the high abundance of solar energy, the versatility and scalability of the technology, and the relative ease in development and installation in both domestic and commercial applications. In 2016, PV became the fastest growing source of net electricity generation capacity, with one-third of all

new electricity generation capacity installed globally in 2017 being in the form of PV [6], [7]. Furthermore, the continuous expansion of PV deployment is expected to result in this technology having the largest renewable electricity generation capacity by 2022, exceeding wind energy [8]. One of the main reasons for this transition is the continuous drop in the initial fixed cost of PV systems. To put this into perspective, the cost of typical PV panels has dropped from $76 to under $0.28 per peak watt from 1977 to 2019 [9]. In addition, the process of converting light energy to electrical energy using this technology has seen considerable improvements over the years. For example, single crystal silicon PV, which is currently the predominant commercial PV technology, has seen power conversion efficiency (PCE) improvements from 13 % to over 26 % from 1977 to date in research laboratories [10]. In turn, these improvements have allowed the levelized cost of energy of PV technologies to become increasingly competitive, promoting its global implementation. Despite these merits, further efforts must be made towards the expansion of PV deployment as currently only 2 % of global energy demands are being supplied by solar energy [6]. In other words, the levelized cost of this source of energy must be reduced further to extend the financial value of this technology to the consumer market and hence aid its further deployment.

Since the emergence of the first solar cell from Bell Labs in 1954 [11], PV technologies have been primarily fabricated using the semiconductor silicon (Si) as the light absorbing layer. This material is not only the second most abundant element in the earth's crust, but the technological evolution of PV using Si since its emergence has built a robust platform for its current widescale use in commercial and domestic applications. Currently, PV technologies using silicon comprise roughly 95 % of the commercial PV market and have consistently dominated with over 70 % of the market share since 1980 [12]. Inherently, silicon wafers are usually doped with either boron or phosphorus to create p-type or n-type doping respectively. This is to increase the amount of de-localised charge during photo-generation in this material for PV applications. Historically, p-type cells were preferred due to the greater resistance to irradiation damage that was crucial for space applications [13]. However, the industry is now focusing more on n-type cells due to the inherent boron-oxygen related defects that arise in p-type wafers which cause cell degradation [14]. This type of technology is conventionally grouped into categories, namely mono-crystalline and multi-crystalline silicon PV. The term crystallinity here refers to the degree of structural order to the atoms or molecules in a solid. Hence, in this case, a mono-crystalline silicon solar cell refers to an absorber layer with one periodic orientation or order of silicon atoms, and multi-crystalline meaning of many orientations or

orders. Typically, multi-crystalline silicon solar cells suffer from electrical losses due to the crystallographic dislocations and defects from the structural imperfections in the absorber layer. This results in a lower PCE being achieved when using multi-crystalline silicon instead of mono-crystalline. The popularity of multi-crystalline silicon over the years has mainly been due to the cheaper fabrication cost of this material and ease in processing. However, a sudden drop in the cost of mono-crystalline wafers in 2016 resulted in a large popularity shift towards mono-crystalline silicon PV. This is exemplified by the increase in the total market share of single crystal silicon PV from just under 25 % to over 65 % from 2016 to date [12].

As briefly mentioned, monocrystalline (or single crystal) silicon PV technologies have already reached a record PCE of 26.7 % [10], [15]. However, this is still at research level and the commercial market remains dominated by silicon technologies that have PCE's between 18 – 24 % [8], [16]. Further information regarding these specific types of silicon solar cells is provided in the next chapter. What is important for our discussion here is that the most predominant feature that currents limits the PCE of the majority of the silicon PV industry is the direct application of the metal electrode onto the silicon absorber layer [16], [17]. Traditionally, solar cells consisted of a p-type silicon wafer, with an n-type emitter layer (for charge separation), silver paste contacts and a silicon nitride anti-reflective coating. These types of cell architectures suffer from high electrical losses at the metal-Si interface, limiting these technologies to PCEs considerably lower (~20 %) than the single absorber solar cell theoretical limit of 29.4 % [16], [18]. This limitation occurs due to the high density of electronically active states that arise at the metal-Si interface. These active states are defective or trap regions that limit the flow of photo-generated charge carriers from the absorber to the external circuit, through a mechanism known as Shockley-Read-Hall (SRH) recombination [19]. In other words, the resistance to current flow is heightened by incorporating metal-Si interfaces in these devices. Attempts to mitigate this loss using highly doped regions under the contacts causes the excess energy of the photo-generated charge carriers to be lost, through a different mechanism called Auger recombination, which further limits the overall performance. Further attempts to reduce these losses involved reducing the contacted region area, but this does not eradicate the root of the problem and introduces further fabrication complexities.

Currently, industrial Si PV fabrication lines are based on the passivated emitter rear-contact (PERC) cell (more information on the functionality of this cell is provided in the next chapter) [8]. This architecture limits the recombination losses discussed to some extent by passivating the non-contacted regions of the cell. In simple terms, silicon passivation involves reducing the

surface states (“dangling bonds”) at these interfaces by introducing a dielectric medium [20]. Despite these benefits, the PERC cell is still limited to PCEs of up to 24 %, which is still considerably lower than the theoretical power conversion limit [18], [21]. Regardless of the cell architecture, the pathway to achieving higher performance silicon solar cells is to passivate the contacted regions of the device [16], [22], [23]. To passivate a contact, recombination must be prevented, but not at the expense of the contact conductance. As dielectrics are usually used for surface passivation, and these materials possess high resistance to current flow, the introduction of additional contact resistance with this method is unavoidable. Therefore, these dielectrics must not only be made thin enough to minimise resistance in these contacts, but a mechanism for promoting or demoting charge carrier transport through these contacts is also required, namely charge-carrier selectivity. In PV, the electron and electron-hole (or just hole) are considered as the negative and positive charges respectively, where a hole is the absence of an electron in the atomic structure. These types of contacts that can simultaneously provide charge carrier selectivity and suppress recombination are known as carrier-selective passivating contacts [16], [24].

Ideally, a good carrier-selective passivating contact suppresses the electrical losses at the interface whilst maintaining a low resistivity [16], [25]. Silicon PV devices require passivation of both electron and hole contacts in order to reach PCEs exceeding 25 % [16]. In emerging cell architectures, silicon dioxide (SiO_2) or phosphorous-doped hydrogenated amorphous silicon (a-Si:H) are used as electron-selective passivating contacts. The inherent silicon surface passivation ability and the favourable interfacial band alignments on crystalline silicon make these materials highly suitable. To further promote charge carrier-selectivity, the surface charge carrier concentration of these contacts is modulated using a material with a high fixed charge density, which is generally n-type polycrystalline silicon for electron contacts [24]. However, SiO_2 is not as effective for hole contacts as electron contacts [17], [26], [27]. In addition, the high temperature ex-situ (after-growth) doping process for the polycrystalline silicon conduction layer used for these types of contacts remains a fabrication barrier. Typically, using thermal diffusion to dope this layer in these contacts involves both forming relatively non-uniform doping profiles as well as fabrication methods that involve processing in temperatures exceeding 1000 ^{o}C for multiple hours [28], [29]. Work into alternative structures for hole contacts is currently an important area of research [30], [31]. To date, the most promising material candidates have been p-type amorphous silicon and silicon-rich silicon carbide, but compatibility with conventional high temperature Ag screen printing in industry still remains

an issue [15], [26]. Furthermore, a better method for growing polycrystalline silicon layers, with an in-situ p-type doping process, that can produce relatively uniform films at a lower thermal budget is also of importance. If successful, this growth method could also be implemented towards forming the emitter layer in conventional silicon solar cells, as the same issue with thermal diffusion of dopants (with ex-situ doping) still exists [29], [32], [33].

1.2 Thesis outline

The project discussed in this thesis is primarily focused on the formation of hole-selective passivating contacts for silicon solar cells. In summary, the three main objectives for the project outlined are:

1. Produce a novel chemical vapour deposition (CVD) process for growing polycrystalline silicon films with a highly uniform fixed positive charge density through in-situ doping.
2. Develop a highly controllable growth process for a dielectric material that can simultaneously enhance silicon surface passivation and promote hole tunnelling.
3. Form a hole-selective passivating contact for silicon solar cells. Analyse and compare electrical performance with counterparts.

This thesis is comprised of eight chapters in total, with three of these covering the experimental research carried out during this project. Each results chapter begins with a brief introduction, then several sections that essentially comprise the results and discussion, and ends with conclusive remarks and a note on contributions.

Chapter 2 discusses the fundamental properties of solar cells, which includes the general characteristics of semiconductors and PV devices and defines the key performance metrics of interest. In addition, the technological evolution in design, fabrication, and performance of silicon solar cells to date is discussed.

Chapter 3 follows on by reviewing the literature on relevant carrier-selective passivating contact architectures for PV applications. This is a built up towards our proposed hole contact architecture in this project, which involves using hot wire chemical vapour deposition (HWCVD) for conductive layer formation and atomic layer deposition (ALD) for dielectric nano-layer formation. This chapter is aimed at giving the reader a good understanding of both the topic of interest and how we propose to achieve a high-performance hole-selective passivating contact.

Chapter 4 encompasses the experimental and analytical techniques used in the subsequent results chapters. A brief description of the technique or apparatus, background principles and how these are intended to be used for our research is mentioned. This covers the fabrication procedures, characterisation methods and PV device modelling techniques that are a pivotal part of this project.

Chapter 5 is the first of the three results chapters in this thesis. This chapter is focused on the development of a HWCVD growth process for forming p^+ polycrystalline silicon films. At first, the growth capabilities of the HWCVD tool are analysed and the tungsten filaments are re-configured to increase the deposition temperature. We analyse the boron-doped films grown using this method, studying the morphological and electrical properties. In addition, the in-situ doped silicon growth process is optimized using a sharp post-deposition annealing process that improves film quality.

Chapter 6 studies the formation of a hole-selective silicon nitride nanolayer. This follows on from chapter 5 where we find the requirement for an interfacial layer to be essential for mitigating carrier recombination and to promote hole tunnelling. Hence, ALD-grown SiN is studied and a highly-controllable growth process is achieved. Using a photoemission-based method, the band alignments at the SiN/Si interface are studied to analyse the potential for hole-selectivity of this nanolayer. The work here provides important information relating to the band structure at this interface and the potential applications of this material.

Chapter 7, the final results chapter, looks at carrier-selective contact formation using the work from the two preceding results chapters. At first, the specific contact resistivity of ALD-grown SiN nanolayers are studied. We present findings on the effect of dielectric thickness and metal electrode work function on hole contact performance. Furthermore, we study the hole tunnelling probability and current in our contacts, and make direct comparisons with the SiO_2 counterpart provided.

Chapter 8 concludes the thesis, summarising the work and providing an outlook on the research carried out.

Chapter 2

Photovoltaic device characteristics & typical Si solar cells

2.1 Fundamentals of solar cell operation

2.1.1 Silicon Semiconductor Properties

A semiconductor is a material typically comprised from elements either in group IV of the periodic table, or from a combination of group III and V, or group II and VI. These materials possess an electrical conductivity range that lies between that of an insulator and a conductor, which is advantageous in optoelectronics. Simply put, this means that these materials can become conductive once sufficient optical or thermal energy is applied, where the amount of energy required is much lower than that would be required for an insulating material (typically less than 3.2 eV) [11]. This energy, namely the band gap energy, is equivalent to the energy gap between the highest filled electron energy level and the lowest unfilled energy level in the semiconducting material. The notion of energy levels here originates from the Bohr model, where each atom is defined as a small nucleus surrounded by orbiting electrons. Each of these orbiting electrons are at a unique energy level that is defined by the electrostatic force from the nucleus. When these atoms are bonded together in a material, so many electrons and hence energy levels co-exist that it becomes much simpler to define these as continuous bands. In semiconductors, the highest filled and lowest unfilled electron bands are known as the valence and conduction band, respectively. An illustration showing these bands and the difference in band gap between insulators, semiconductors and conductors is presented in Figure 1. As depicted, the valence and conduction bands in a conductor overlap, which is why materials like common metals are electrically conductive without requiring any external energy.

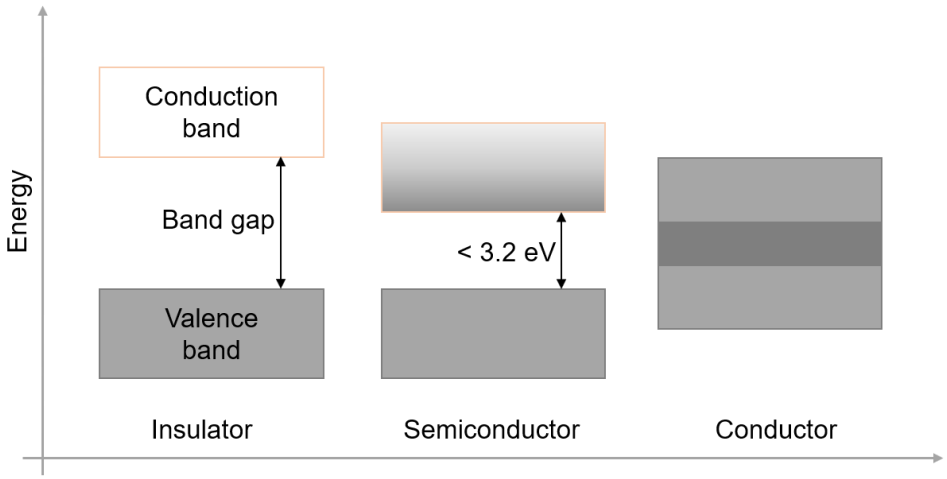

Figure 1: Illustration of valence and conduction bands in insulator, semiconductor and conductor materials.

The band gap energy is the minimum energy required to promote an electron from the valence band to the conduction band, which causes de-localisation of charge in a semiconductor material. When this occurs, free carriers have now been created in both energy bands – an electron in conduction and a hole (or electron absence) in the valence band. Hence, we consider two currents in semiconductor physics – electron and hole current. However, the simplified illustration of the energy bands in Figure 1 cannot depict the true transition of carriers between these bands. Typically, depending on the position of the minimum energy state in the conduction band and the maximum energy state in the valence band, semiconductor materials are classed as either direct or indirect band gap materials. These states are each defined by a certain momentum, k, in the Brillouin zone [34], where if the k-vectors are identical, the energy gap is considered to be a direct transition. On the other hand, if the k-vectors are different, an indirect band gap is considered. This phenomenon arises from the shape of the energy bands, where these are most often parabolic near the maximum and minimum points. An illustration of these energy bands showing the difference between a direct and indirect band gap material is shown in Figure 2. Silicon in crystalline form is considered to have an indirect band gap. This means that for the transfer of electrons between these bands, an intermediate state is required for momentum transfer, as depicted in Figure 2. Hence, when an electron recombines with a hole by relaxing to the valence band from the conduction band in such materials, a photon is rarely emitted, and this is considered as non-radiative recombination. For an indirect band gap material to undergo radiative recombination (as in Figure 2), the photon, phonon and electron-hole pair required in this process must occur at the same time and this is virtually impossible in the physical world. In most cases, the free carriers in indirect band gap materials

non-radiatively recombine via Shockley-Reed-Hall or Auger recombination (more information on these phenomena provided later in this chapter). Non-radiative recombination is disadvantageous for PV device performance as the recombination energy is dissipated through lattice vibrations, namely phonons, rather than optical energy that could be re-harnessed in the absorber layer.

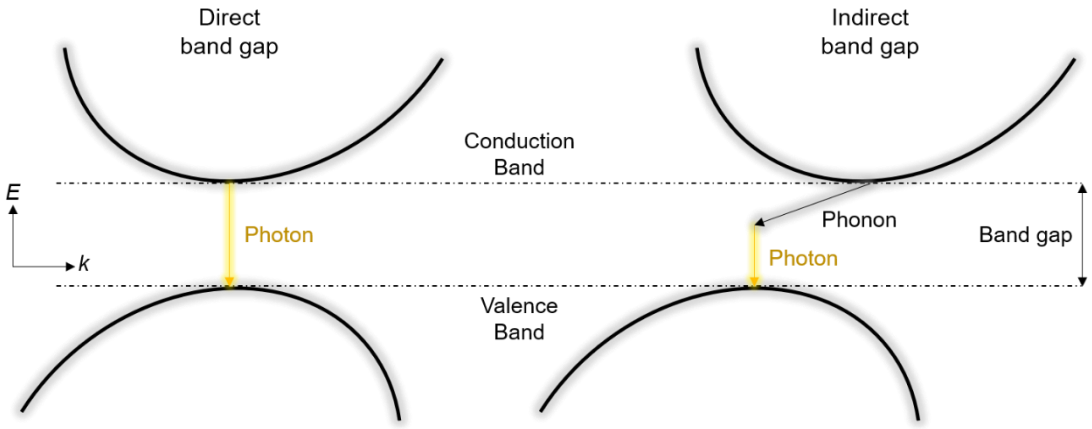

Figure 2: Energy band dispersion difference between direct and indirect band gap semiconductors.

Typically, a semiconductor material like silicon, which has not had impurities added to it to alter the concentration of carriers (or localised electrons/holes), is called an intrinsic semiconductor. In effect, the number of free electrons in the conduction band or holes in the valence band of such materials is called the intrinsic carrier concentration, n_i. This is typically defined as a function of temperature, T, by [35]:

$$n_i = 5.29 \text{ x } 10^{19}\left(\frac{T}{300}\right)^{2.54} e^{-6726/T} \quad (1)$$

For crystalline silicon, n_i is typically measured at 9.65×10^9 cm^{-3} at room temperature (300 K) [36]. To vary this concentration, silicon is usually doped with electron-rich (group VI) or electron-deficient (group IV) elements to increase the number of de-localised electrons or holes respectively. The notion of electron (n-type) and hole (p-type) doping in a silicon crystal lattice is depicted in the schematic diagram in Figure 3. When doped, namely extrinsic, the semiconductor now possesses a higher concentration of either electrons or holes, which are called the majority carrier in this medium. The other carrier type is named the minority carrier. Typically for photovoltaic applications, silicon substrates that are used as the absorber layer are doped at an extrinsic carrier concentration of between $10^{14} – 10^{15}$ cm^{-3}. At equilibrium, the product of the majority and minority carrier concentration is expressed by the Law of Mass Action and is defined as:

$$n_0 p_0 = n_i^2 \quad (2)$$

When n_0 and p_0 are the electron and hole equilibrium concentrations in the semiconductor.

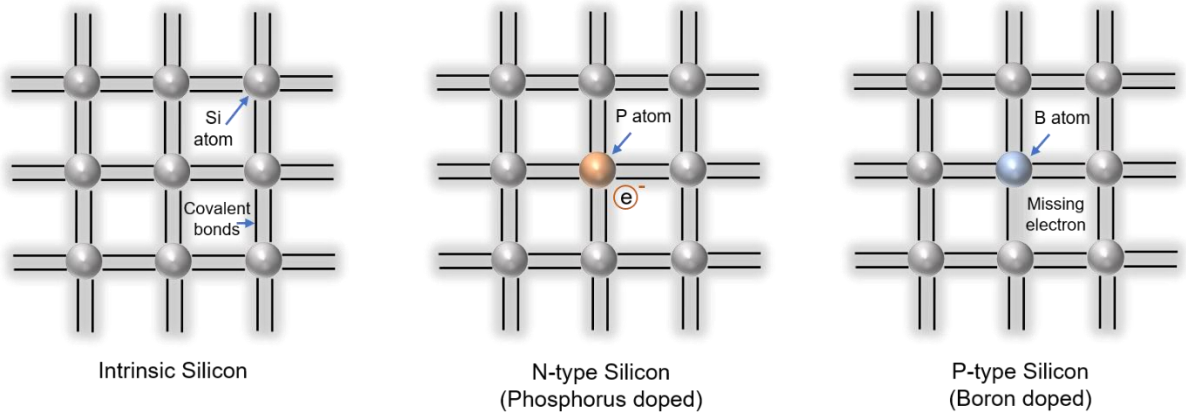

Figure 3: Schematic diagram of an intrinsic, n-type and p-type silicon crystal lattice.

2.1.2 P-N Junction Silicon Diodes and Charge Extraction

In semiconductors, the promotion of an electron from the valence band to the conduction band is generally not energetically stable as it is more favourable for electrons to relax to ground (or valence) state. Hence, the lifetime of these excited carriers in silicon are generally much less than 1 second as these excited electrons can easily recombine with a vacant hole within the crystal lattice. Therefore, the photo-generated charge carriers in a solar cell must be driven quickly to the external circuit before recombining. For this purpose, silicon solar cells have a P-N junction (a junction between p-type and n-type silicon).

A P-N junction allows the separation of the electron and hole carriers in a solar cell and creates a potential difference across the opposing electrodes. When p and n type silicon materials are taken from electrical isolation to being in-contact at thermal equilibrium, electrons from the n-type material diffuse to the p-type material and holes from the p-type material diffuse to the n-type material. This is due to the carrier concentration difference across this interface. As these charge carriers diffuse through the interface, they leave ions behind which collectively create an electric field that opposes the direction of carrier diffusion. This electric field causes the drift current of carriers in the opposite direction of the diffusion of carriers before reaching equilibrium. Hence, from this drift current, minority carriers (e.g. holes in n-type silicon) can effectively drift across this junction, allowing the separation of photo-generated charge carriers in solar cells. A silicon P-N junction showing the space-charge region, namely the depletion region, at the interface is illustrated in Figure 4(a).

To appreciate the transport of charge carriers through the depletion region further, it is useful to consider the energy band diagram of the P-N junction, as shown in Figure 4(b). In this diagram, three energy bands are drawn: the valence (E_V) and conduction (E_C) bands, and also the Fermi level (E_f). In all semiconductor materials, E_f is defined as the energy level that has a 50 % probability of being occupied by an electron in thermal equilibrium. This is merely a statistical entity as the occupation of E_f by an electron is energetically forbidden. Nonetheless, as the energy distribution of electrons obey Fermi-Dirac statistics, they can be defined by the Fermi-Dirac distribution at thermal equilibrium by:

$$f(E) = \frac{1}{e^{(E-E_f)/kT}+1} \tag{3}$$

Where k is the Boltzmann constant and T is the temperature. Hence, the distribution of charge carriers is a function of the temperature. The population of the energy states in the conduction band will be zero at T = 0 K and occupation of electrons in the conduction band occurs at T > 0 K.

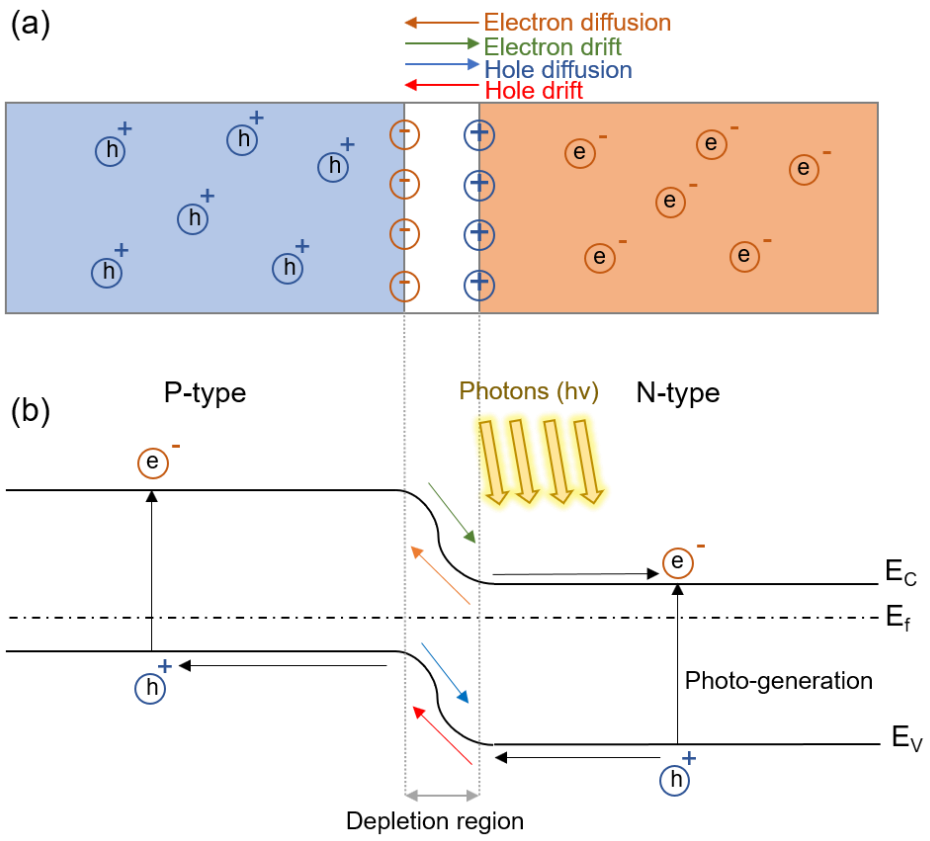

Figure 4: (a) P-N junction at thermal equilibrium and (b) schematic band diagram of P-N junction under illumination at steady-state.

The importance E_f in the band diagram is that when two semiconductor materials are brought together, the position of E_f at the interface aligns at thermal equilibrium. This means that if the position of E_f is not identical (relative to E_V or E_C) between the two materials, E_V and E_C bend equally at the interface relative to the energy shift. In a physical sense, this phenomenon occurs due to the difference in charge distribution of the two materials at the interface, which creates a potential difference that causes such energy bands to bend. This bending at the interface creates a potential difference between the energy levels and promotes charge carrier drift across the junction. In semiconductor physics, it is considered energetically more favourable for electrons to transition from higher potential to lower potential (or 'downhill') and for holes to move from a lower potential to higher potential (or 'uphill'). This is seen in Figure 4(b) from the difference in direction of drift current in the depletion region for electrons and holes respectively.

In the silicon semiconductor industry, a P-N junction is the classic model used for forming diodes. Despite the inherent use in PV, this is not necessarily required as the drift current of electrons and holes could be controlled using different mechanisms. Fundamentally, we can use the same principle from the dependence of the direction of charge carrier drift on the potential difference between the energy bands at a semiconductor interface to engineer electron and hole selective layers without using a P-N junction. A schematic diagram of the energy bands of this type of solar cell, namely a heterojunction, is shown in Figure 5. By fine-tuning the energy band difference at each interface, carriers can be separated at either side of the absorber layer. Furthermore, a potential barrier is created against minority carrier flow to the opposing contacts which reduces recombination losses and hence electrical resistance. In essence, this is a 'junction-less' cell as the extraction of charge carriers does not involve the use of a P-N junction. This introduces multiple advantages, which include no longer requiring an emitter layer and obtaining more control on carrier extraction in such devices [16].

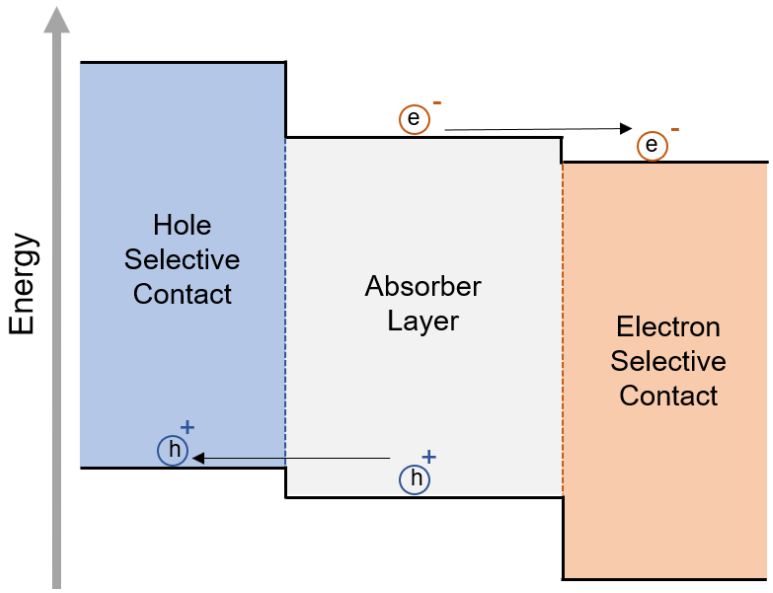

Figure 5: Simplified band diagram of solar cell with hole-selective and electron-selective contacts.

The band diagram shown in Figure 5 is analogous to carrier extraction in heterocontacts. More detail on the functionality and operation of such devices is provided in the next chapter.

2.1.3 The Photovoltaic Effect and Solar Cell Operation

The photovoltaic effect is the underlying fundamental principle of all PV technologies. It is the process that converts light energy directly to electrical energy. This phenomenon is understood from the quantum theory of light, where photons can be absorbed by electrons, transferring their energy and promoting the electron out of its valence shell. The photovoltaic effect differs from the photoelectric effect in that the electron is promoted to a conduction level (or band) within the material rather than to vacuum. As previously described, the photo-generated electron in its excited state must be extracted in a solar cell device before its energy is dissipated by relaxing back to ground state. Furthermore, the excitation of the electron leaves a hole in the valence shell, which acts as the positive charge carrier that is to be extracted from the opposing contact. In other words, these two charge carriers must be simultaneously extracted before recombining.

In essence, the general operation of solar cells can be simplified as:

1. The generation of light-generated carriers (electron-hole pair).
2. The collection of the light-generated carriers to generate a current.
3. The generation of a potential difference across the solar cell due to the build-up of

charge.

4. The dissipation of power in the load and in parasitic resistances.

As mentioned in section 2.1.2, a P-N junction is typically used to separate and collect the photo-generated carriers for current generation. When these devices are at thermal equilibrium, the net drift and diffusion currents of charge carriers is zero, meaning no current is transferred through the device. However, when light is incident on the device, due to the generation of carriers in the bulk absorber layer, the diffusion and drift current in the device become imbalanced. This is due to a generation of charge carriers with a rate, g_{op}, that occurs under illumination. Amongst the generated carriers, minority carriers (n_p and p_n) that are generated near the depletion zone in the bulk region are swept across due to the built-in electric field (i.e. drift current). The current as a result of the collection of the photo-generated minority carriers across the junction can be defined as:

$$I_L = qAg_{op}(L_p + L_n + W_t) \quad (4)$$

Where q is the charge of an electron, A is the junction area, L_p and L_n are the minority carrier diffusion lengths and W_t is the depletion region width. Due to this current, minority carriers can now be collected at the collectors (typically metal electrodes) that are conventionally placed on either side of such devices. The build-up of charge carriers at each polarity generates a potential difference, as depicted as V_{out} in Figure 6. This is the general process for all semiconductor diodes that are used for PV applications. This can be represented by the equivalent electrical circuit that is comprised of a diode, a current source (from light) and some parasitic resistances in the solar cell, namely series (R_s) and shunt (R_{sh}) resistance, as shown in Figure 6.

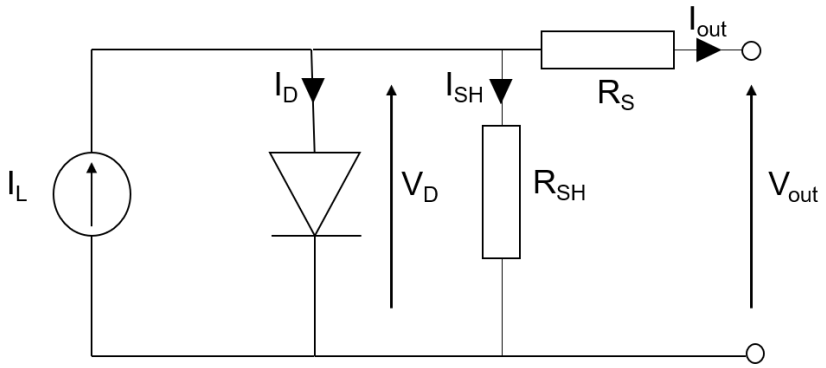

Figure 6: Equivalent electrical circuit for solar cells.

Using Kirchhoff's current law (KCL), the current generated through the output terminals, I_{out}, is equal to:

$$I_{out} = I_L - I_D - I_{SH} \quad (5)$$

Where I_L is the photogenerated current, I_D is the current through the diode representing the P-N junction, and I_{SH} is the current through the parasitic shunt resistor (R_{SH}). The voltage across the diode and R_{SH} are the same and are denoted as V_D, which is equal to:

$$V_D = I_{out}.R_S + V_{out} \quad (6)$$

Where R_S is the parasitic series resistance and V_{out} is the output terminal voltage. From the Shockley diode equation, the current through the diode, I_D, is equal to:

$$I_D = I_o(e^{\frac{V_D}{nV_t}} - 1) \quad (7)$$

Where I_0 is the dark saturation current, n is the ideality factor and V_t is the thermal voltage. In addition to this, the current through R_{SH}, I_{SH}, can be easily written as:

$$I_{SH} = \frac{V_D}{R_{SH}} \quad (8)$$

By substituting the equations for I_D and I_{SH} back into the equation for the output current, I_{out}, the overall electrical characteristics equation for a typical solar cell can be written as:

$$I_{out} = I_L - I_o\left(e^{\frac{I_{out}.R_S+V_{out}}{nV_t}} - 1\right) - \frac{I_{out}.R_S+V_{out}}{R_{sh}} \quad (9)$$

In order to maximise the output current from any solar cell, the importance of these parameters can be seen in equation 9. From this equation, the dark saturation current, I_0, and series resistance, R_S, can be clearly seen to be the most beneficial at a minimum, and others like the light generated current, I_L, and the shunt resistance, R_{SH}, ought to be kept at their maximum to generate the largest output current possible from a solar cell.

When the current – voltage characteristics of an operating solar cell are measured, a curve in the fourth quadrant is extracted which can then be manipulated for obtaining the key electrical performance metrics. This curve, namely the I-V curve, is generally inverted across the x-axis for easier appreciation and understanding of the performance metrics. A sketch of a typical I-V curve is illustrated in Figure 7. The x and y-intercept of the curve represent the open-circuit voltage (V_{oc}) and short-circuit current (I_{sc}) respectively. The open-circuit voltage is the maximum voltage available from a solar cell, which occurs when the current is zero (open-

circuit). The short circuit current is due to the generation and collection of light-generated carriers and occurs when the voltage is zero. In lab-scale research, short-circuit current density (J_{sc}) is generally used instead of short-circuit current to normalise for cell area. Trivially, the product of the current and voltage at any point on the curve represents the power at that point, with the power output curve indicated in Figure 7. Furthermore, at the maximum power point (P_{mpp}), some key performance metrics can be extracted. Note that the maximum power point is the product of the maximum power point current (I_{mpp}) and maximum power point voltage (V_{mpp}). One of these is the fill factor, FF, which is the ratio of the maximum power from the solar cell to the product of V_{oc} and J_{sc}. It can be calculated as follows:

$$FF = \frac{I_{mpp}V_{mpp}}{I_{sc}V_{oc}} \tag{10}$$

Another key performance metric that can be extracted from the I-V curve is the power conversion efficiency (PCE) of the solar cell. The PCE is defined as the ratio of the electrical power output from the solar cell to the input optical power on the front surface. This is the most representative parameter of any solar cell and is typically the first point of discussion in comparing solar cells. This can be calculated as follows:

$$PCE = \frac{I_{sc}V_{oc}FF}{P_{in}} = \frac{P_{out}}{P_{in}} \tag{11}$$

The parameters taken from the I-V curve are the most significant electrical performance metrics of PV devices and are typically used as a point of comparison.

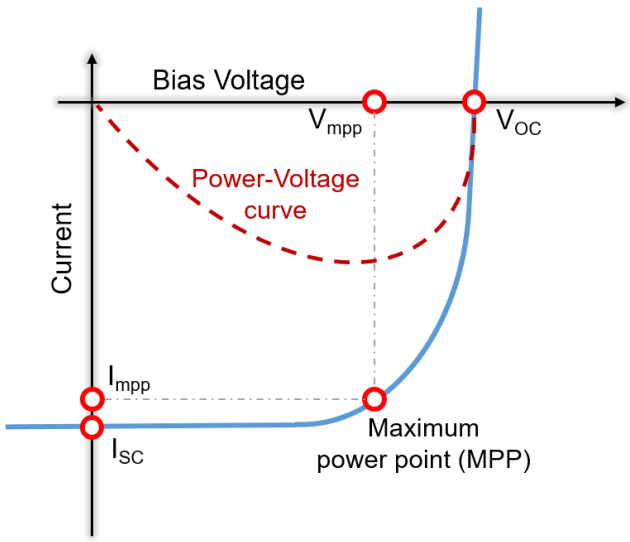

Figure 7: Typical I-V characteristics of illuminated solar cell. Key characteristics identified – V_{OC} is the open-circuit voltage, I_{SC} is the short-circuit current, and V_{mpp} and I_{mpp} are the voltage and current at the maximum power point.

2.1.4 The Theoretical Power Conversion Efficiency Limit

In 1961, Shockley and Queisser proposed a detailed technique for defining the maximum theoretical PCE limit of single junction (or absorber) PV devices [37]. This limitation, namely the Shockley-Queisser limit, examines the amount of electrical energy utilized per incident photon. The two primary power conversion loss channels identified are: (1) incident photons with energy, hν, less than the band gap energy, E_g, are not absorbed, and (2) the excess energy of electrons being lost through thermalization in the crystal lattice [37],[38]. These losses are considered as intrinsic, as they represent fundamental limitations of energy conversion within these operating devices which cannot be mitigated. These are presented in Figure 8, where the intrinsic losses with respect to semiconductor band gap are shown, based on the Shockley-Queisser limit [18]. If crystalline silicon, which has a band gap of 1.12 eV, is considered, a PCE loss of over 12 % is expected due to the transparency of the absorber layer to $h\nu < E_g$. A further PCE loss of over 30 % is further predicted due to the thermalisation of electrons, where the excess energy in excited carriers is lost. Besides these two primary losses, further intrinsic losses associated with semiconductors include the Boltzmann loss. This phenomenon is due to the mismatch in the angle of incident photons from the sun and isotropic re-emission of some photons from the absorber, also known as angular entropy, which further lowers PCE by approximately 10 %. Furthermore, analogous to a Carnot engine, the sun acts as a heat source and the earth's surface as a heat sink, representing a further 2 – 4 % energy loss. This is identified as Carnot in Figure 8. Additionally, the final loss considered in Figure 8 is emission losses, where ~1 % PCE loss is predicted due to ability of the solar cell to act as both an absorber and emitter (of photons) [18]. These fundamental intrinsic losses are inevitable barriers to the photovoltaic performance of single junction solar cells.

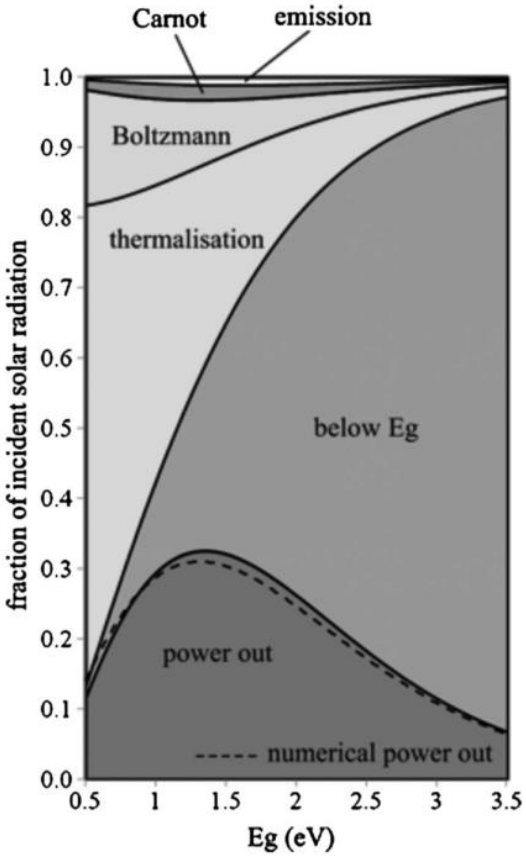

Figure 8: Intrinsic losses of single junction solar cells, based on the Shockley-Queisser limit, taken from [18].

As well as intrinsic losses, other types of losses also co-exist within PV devices that further limit device performance. These are conversion losses that stem from design or fabrication flaws, and in principle, can be mitigated [18], [37]. Primarily, these are recombination losses that are generated from impurities, trap regions (series resistance) and undesirable photo-absorption in certain regions of the device. Recombination of charge carriers in semiconductors are categorized into either radiative or non-radiative recombination. Radiative recombination is when an electron and hole recombine, and a photon is emitted from the process. This is a band-to-band electron transition where the Laws of Conservation of Energy are met through photon generation. On the other hand, non-radiative recombination provides no optical contribution in the semiconductor. Non-radiative recombination losses in semiconductor materials are generally associated to one of the two following mechanisms:

Shockley-Read-Hall (SRH) recombination is generally a trap-assisted form of recombination. In a semiconductor crystal lattice, localised energy state can arise within the band gap due to the existence of a defect or dopant. This creates an energy state closer to the

conduction band than the valence band, which provides an easy path for excited electrons to relax.

Auger recombination is associated with the optical energy loss from radiative recombination. In this loss mechanism, an electron and hole recombine in a band-to-band transition, but the resulting photon is absorbed by an excited electron in the conduction band. This energy is then dissipated through thermalization.

The transition of charge carriers across the valence and conduction bands in both radiative and non-radiative recombination are depicted in Figure 9.

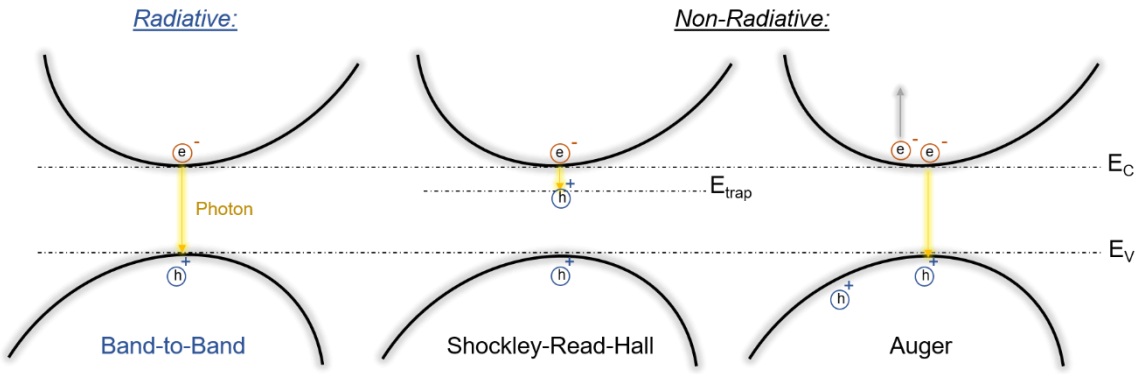

Figure 9: Carrier energy band transition in (a) band-to-band recombination, (b) Shockley-Read-Hall recombination and (c) Auger recombination.

Band-to-band recombination in semiconductors is an inevitable process. Essentially, a solar cell in reverse is a photo-diode, whereby the recombination of charge carriers causes photo-emission. This is a natural phenomenon that is the reverse of charge carrier generation. However, non-radiative recombination can certainly be avoided in PV devices by reducing the density of defects in the bulk of the absorber layer and at the material interfaces within the solar cell. Overall, the total decay rate of the photo-excited carrier population can be denoted as [20]:

$$\frac{1}{\tau_{total}} = \frac{1}{\tau_{rad}} + \frac{1}{\tau_{nonrad}} \tag{12}$$

Where $1/\tau_{total}$ is the total decay rate, and $1/\tau_{rad}$ and $1/\tau_{nonrad}$ are the radiative and non-radiative recombination rates.

2.1.5 Silicon Passivation

Passivation in PV refers to the processes used for removing electronically active defects within the device. This reduces the density of recombination sites (or active states) for charge carrier recombination, which reduces the overall device resistance to the passage of current. In general,

passivation is either chemical, where defects are removed or deactivated, or involves creating an electrical field within the device to limit the concentration of unwanted charge carriers. In general, there are three main regions of a solar cell which require passivation.

The **bulk absorber** layer in the solar cell must be well-passivated to avoid the recombination of photo-generated carriers before their collection. Inherently, silicon ingots with high purity (< 1 parts per million) are used for producing silicon wafers for PV applications in an extremely controlled manner [39]. Furthermore, the use of monocrystalline silicon has further reduced recombination in dislocations and grain boundaries that are typically found in multi-crystalline silicon. However, when silicon wafers are doped, the passivation of the bulk is affected as impurities are added to the material. Hence, a trade-off between the conductivity and passivation of wafers generally exists. Furthermore, the use of thermal diffusion or ion implantation to form various regions (e.g. emitter and BSF) in conventional silicon solar cells adds further stress to the bulk passivation.

Other ways of improving the bulk absorber layer performance include the removal of metal impurities via gettering [40], [41]. Adding hydrogen to the crystal silicon lattice is also a well-known method for improving the passivation of silicon. Hydrogen can passivate any dangling bonds or dislocations and can diffuse easily through silicon. Common hydrogenation methods include Forming Gas Anneal (FGA), hydrogen plasma treatment and UV-H_2 processes [42], [43]. Adding to these, a recent study by Grant et al. [44] showed that common silicon wafers undergo major bulk degradation when processed at temperatures between 450 – 700 ^{o}C. They studied several commercially available n- and p-type float-zone (FZ) silicon wafers from five leading suppliers and observed a major reduction in the bulk lifetime at these temperatures. FZ wafers are high-purity crystalline silicon grown via vertical zone melting and serve as a popular alternative to wafers grown via the Czochralski (Cz) process. Bulk degradation induced by thermal processing on FZ wafers can be observed in Figure 10, where the bulk carrier lifetime versus thermal processing temperature for five different ingots are shown. From this study, it was found that by heat-treating in an oxygen-rich atmosphere at temperatures exceeding 1000 ^{o}C, the active recombination sites are permanently annihilated, and the silicon wafers become stable during further thermal process steps in the fabrication process [44]. This is a crucial processing step that needs to be considered when using FZ Si wafers for PV.

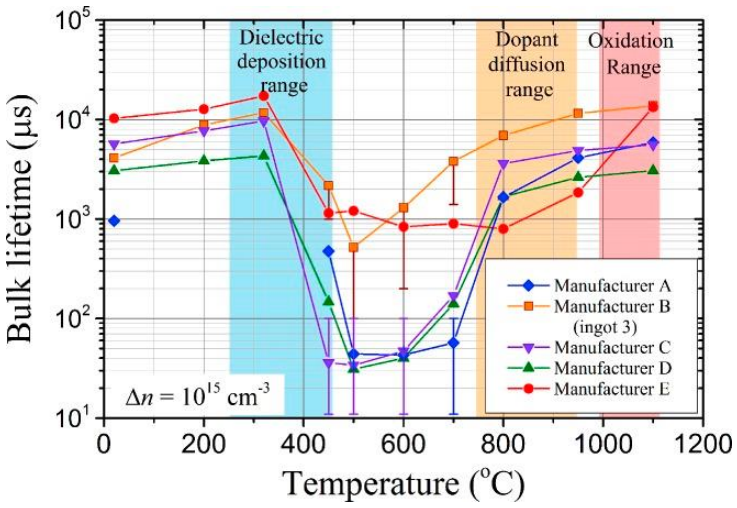

Figure 10: Bulk carrier lifetime versus annealing temperature for five different FZ silicon ingots [44].

The **surface** of the absorber layer must also be passivated. In PV, this is typically conducted using dielectrics such as silicon dioxide (SiO_2), aluminium oxide (Al_2O_3) and silicon nitride (Si_3N_4) [20]. Amongst these, Si_3N_4 is particularly suitable as it can simultaneously provide surface passivation and anti-reflection to a crystalline silicon surface. As well as these chemically passivating materials, it is also highly beneficial to provide field-effect passivation to the surfaces. This can either be provided by charge density modulation (e.g. doping) and/or using an intrinsic surface layer with suitable electronic band offsets to crystalline silicon [45]–[47]. The combination of these mechanisms will only strengthen this process as is desirable. More information regarding such possibilities is provided in the next chapter.

The **contact** structures of typical silicon solar cells that involve metal-silicon interfaces are another source of major recombination sites and lossy regions. Silicon-metal interfaces have an extremely high density of states which results in charge carrier recombination that is detrimental to device performance [16], [48]. As single-junction silicon devices are reaching closer to the Shockley-Queisser limit, improving the contact passivation is becoming increasingly important. More detail regarding such losses in contacts and their associated cell architectures is provided in the next chapter.

2.2 Silicon Photovoltaics – Past, Present & Future

In this section, we take a brief look at the history and evolution of silicon solar cell technology, leading towards more prominent architectures. This is aimed at extending the readers understanding of existing technologies and building towards the research outlined in this thesis.

2.2.1 Screen-printed and Al-BSF Solar Cells

Screen-printed solar cells are a well-established technology in the PV industry, dominating the terrestrial photovoltaic market. Since its early development in the 1970s, screen-printing has been favoured for fabricating silicon solar cells due to its cost-effectiveness and simplicity [49]. It does not include any complications involving photolithography and complex mask requirements. Instead, it offers a highly scalable and reproducible process for front-contact silicon solar cells.

Amongst the variety of manufacturing methods for fabricating screen-printed silicon solar cells, a simple process for producing such cells can be defined as [50], [51]:

1. Alkaline etching of virgin wafer for saw damage removal.
2. Homogenous phosphorous doping in furnace (typically approximately 1000 ^{o}C).
3. Edge isolation via plasma etching/laser cutting for removal of junctions at wafer edges.
4. A screen is lowered onto the rear of the wafer, with a metal paste dragged across the screen print mask.
5. Screen is removed, and the wet metal paste is baked to drive off undesired solvents.
6. Annealed in a furnace (>800 ^{o}C) to fire the metal paste to contact the silicon layer.
7. Steps (iv)-(vi) repeated for front surface, with the inclusion of a line pattern to minimize shading effects.
8. Cell is encapsulated and incorporated into a module.

Typically, a p-type wafer is used for such cells as the additional use of aluminium paste for the contacts forms a BSF for the cell [49]. This avoids any additional thermal diffusion (e.g. $POCl_3$ diffusion for n-type bulks) requirements in the manufacturing process. As well as the aluminium paste, typically an additional silver paste is applied to form a solderable contact. The bulk material used has historically mainly been multi-crystalline; however, many architectures have evolved to utilize a monocrystalline bulk. A top-down photograph taken

from a screen-printed multi-crystalline silicon solar cell is displayed in Figure 11(a), with the different grain orientations being visible from the multiple shades of blue being present. The two thick white lines represent the bus bars, with the branching finger contacts placed perpendicular to the bars with spacings between 2 - 4 mm for efficient carrier collection.

The extraction of charge carriers in this type of solar cell relies on a basic metal-silicon interface. This interface is rich with defects, resulting in an increase in the SRH recombination rate and hence degradation of device performance. Consequently, the region directly below the metal electrode is usually doped at a high concentration (typically between 10^{17} – 10^{19} cm^{-3}) to create a p^+ or n^+ silicon layer. The higher fixed charge density modulates the surface carrier concentration and introduces a form of carrier selectivity by promoting the passage of desirable (majority) carriers and blocking undesirable (minority) carriers. This is due to the electric-field generated by the difference in carrier concentration that causes a difference in energy bands and therefore generates a potential difference, analogous to the description of drift diffusion in P-N junctions in section 2.1.2. The positive (hole) contact from such architectures, as well as the respective band diagram, are shown in Figure 11(b) and 11(c) respectively. In Figure 11(c), ϕ_m and ϕ_s represent the metal and silicon work functions respectively, which is energy required to eject an electron to vacuum. Furthermore, χ_{Si} is the electron affinity of silicon, which is the energy required to promote an excited electron in the conduction band to vacuum.

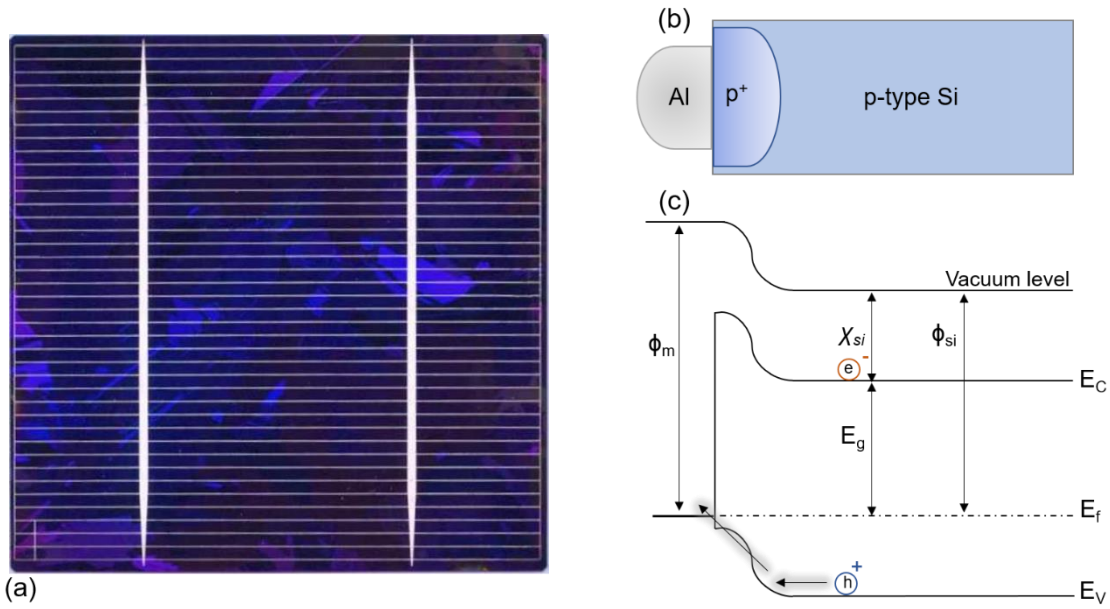

Figure 11: (a) top-down photograph of screen-printed solar cell, (b) schematic of heavily-doped p-type contact and (c) electronic band diagram of contact.

The primary underlying issue associated with the performance of such charge-extraction methods is the increase in Auger recombination in highly-doped regions. This occurs due to the higher concentration of de-localised charge carriers in the p^+ region which make the possibility of Auger recombination more possible. Typically, this type of architecture limits the solar cell PCE to under 20 %, which is considerably lower than the Shockley-Queisser limit of 29.4 % [16], [51]. In addition, the thermal diffusion processes used for forming such contacts generally possess a high thermal budget.

2.2.2 Passivated emitter rear-contact solar cell

Following from the inherent losses from carrier-extraction in the Al-BSF approach, the passivated emitter rear-contact (PERC) silicon solar cell was created. A comparison between the processing steps and cell architectures of the simple Al-BSF approach and PERC cell are shown in Figure 12. The PERC cell is manufactured similar to the process described in section 2.2.1, but with the inclusion of a rear-surface passivation layer and localized Al-BSF contacts [21]. Rear surface recombination is suppressed using the AlO_x passivating layer. Furthermore, by forming a selective emitter, metal-silicon coverage at the rear of the device is reduced, and the non-contacted regions are passivated. This allows the amount of SRH and Auger recombination to be reduced, which improves the device voltage. Overall, this allows PERC technology to be capable of PCEs of up to 24 % [16], [10], [21].

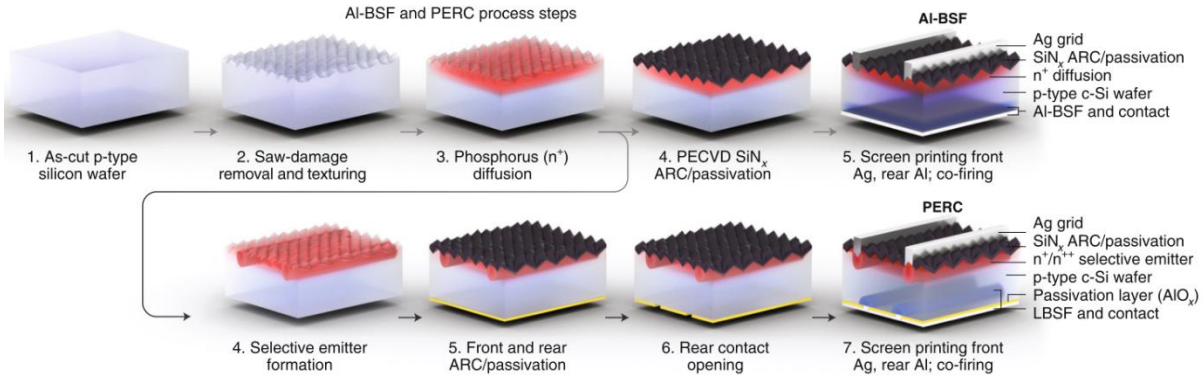

Figure 12: Fabrication of Al-BSF and PERC cells [16].

PERC devices suffer from higher fabrication complexities due to the selective emitter formation. The accurate formation of emitter and metal coverage based on optimized fractions can prove difficult when using photolithography. Furthermore, by only reducing the metal-silicon area, the problem has only been reduced and not completely solved. The use of highly-

doped regions still cause Auger recombination that is detrimental to PV devices, as well as adding further cost to the overall fabrication process.

2.2.3 Heterojunction and Buried contact solar cells

A heterojunction design refers to the variation in crystallinity across the junctions in the solar cell. This design is an improvement of the classic monocrystalline cell by using different materials other than just the crystalline wafer to create carrier transport layers. A heterojunction (HTJ) cell refers to a cell architecture that uses this approach for passivation and carrier extraction from the bulk absorber layer. A cross-section of a typical HTJ silicon solar cell is presented in Figure 13(a). The band diagram depicted in Figure 5 is analogous to the electronic structure of this device. This architecture addresses the reduction of losses at the junctions of the cell by utilizing amorphous silicon (a-Si) layers, resulting in higher power conversion efficiency [52]. It uses a doped mono-crystalline silicon bulk area with a-Si layers (intrinsic thin layer) on each side of the bulk, passivating the surface and acting as a buffer layer between the p-n junction. p^+ and n^+ doped regions above and below the a-Si layers This type of architecture is a great improvement on the conventional front contact solar cell, with record power conversion efficiencies for this architecture currently reaching 25 % [10].

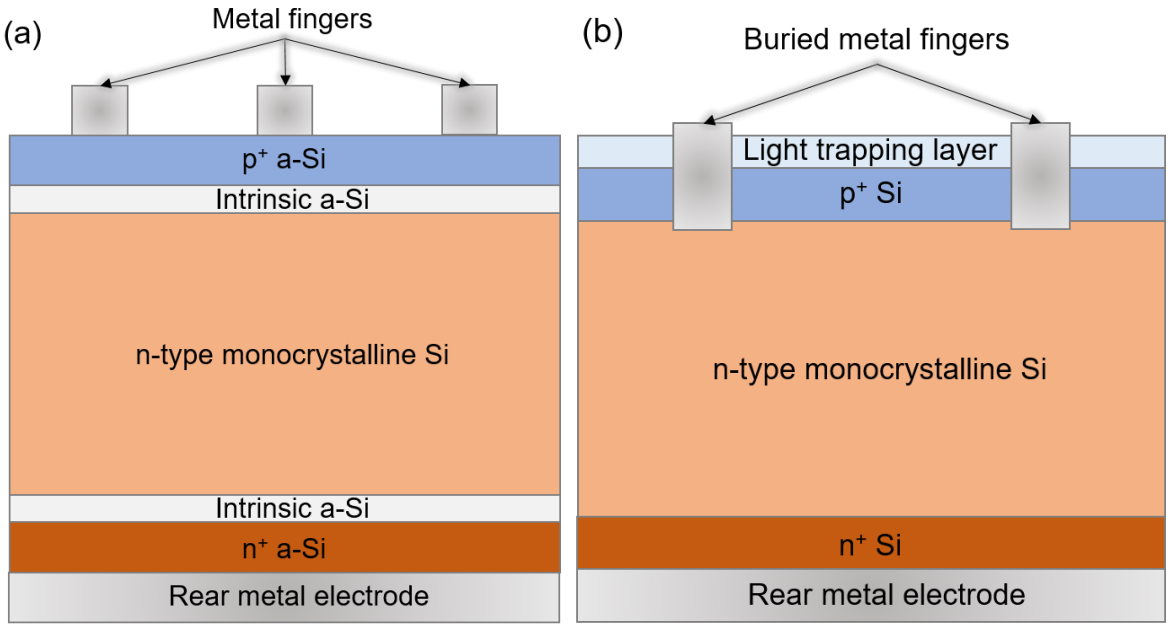

Figure 13: Cross-section schematic of conventional (a) heterojunction with intrinsic layer and (b) buried contact silicon solar cells.

Despite the considerable improvements with the HTJ cell, the electron and hole passivation and transport layers have poor thermal stability. Using a-Si limits the processing temperature

of these devices to less than 200 ^{o}C, as higher temperatures would cause the re-crystallisation of this material. Re-crystallisation would alter the optoelectronic properties of this material, which would drastically alter the device performance. Hence, this type of cell is not the most viable solution as it limits industrial applications to only low-temperature processes.

An alternative PV technology is the buried contact silicon solar cell, primarily differing by replacing conventional top contacts with laser-induced grooves on the top surface for the placement of metal contacts. A cross-section of this type of cell is illustrated in Figure 13(b). This design increases the solar cell efficiency by allowing a large metal height-to-width aspect ratio that allows a large volume of metal to be used in the contact finger without the burden of shading due to the width of the metal strips [53]. In addition, this design possesses a relatively high metal aspect ratio and fine finger spacing [53], [54], which permits a reduction in parasitic resistance losses. The emitter resistance is reduced in the buried contact solar cell as the narrow finger spacing reduces such losses and the metal grid resistance is also low in this case as the finger (contact) resistance is reduced due to the large volume of copper-alloyed metal in the grooves.

2.2.4 Interdigitated back-contact solar cell

Amongst the various silicon photovoltaics architectures, single junction back-contact silicon solar cells have grown progressively in the photovoltaic market [10]. The most revolutionary alteration to conventional single junction silicon solar cells is exhibiting both polarities of the metal electrodes on the back-side [55], [56]. This rear contact design is known as the interdigitated back-contact (IBC) silicon solar cell, with a typical cross-sectional schematic shown in Figure 14(a). These cells are generally fabricated with local diffusion of boron and phosphorus into the rear of the cell, generating an emitter layer (P-N junction) and the BSF [33]. The diffusion length of the carriers and the passivation quality of the n and p-type regions dictates the quality of carrier collection in such cells. As both the emitter and base electrodes are not present on the front region of the cell, this brings multiple advantages to both the optical and electrical properties of such devices. Firstly, the minimization of optical losses due to no shading from front contacts is exhibited by the IBC design. This generally leads to an increased current density of up to 5 – 8 % [33], [57]. In addition, the removal of front contacts and bars can provide modules that are more aesthetically pleasing, suiting wider applications. The focus of the front surface optimisation can be solely dedicated to optimum light trapping and surface passivation properties. This may include nano-texturing to utilize full light in-coupling with

perfect anti-reflective mechanisms, or the use of micro-texturing, where the scattering of light via different texturing features (i.e. random pyramidal texture) is used [58].

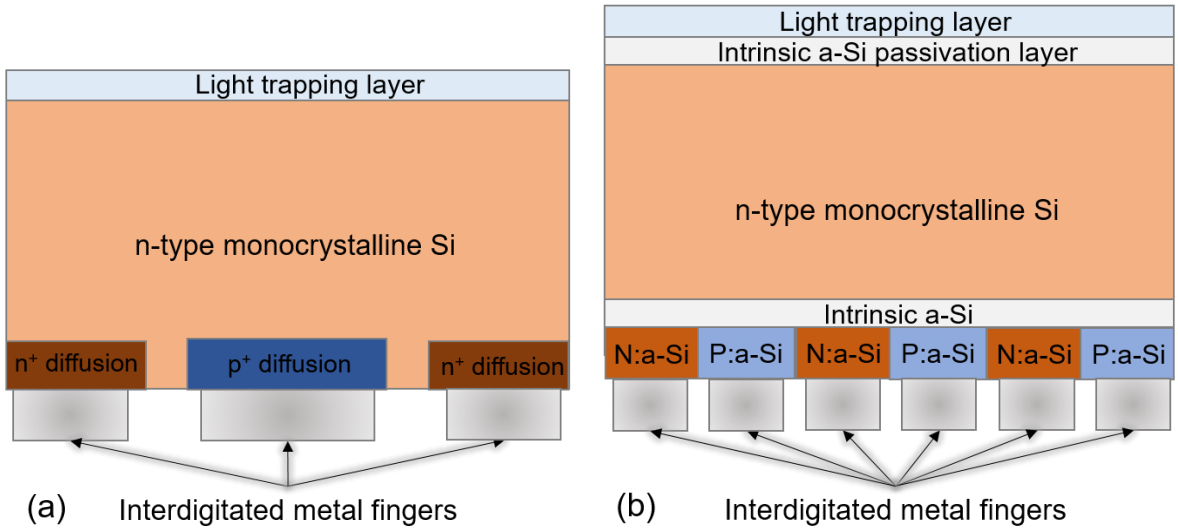

Figure 14: (a) Generic diffused junction IBC and (b) SHJ-IBC solar cell.

As the entire rear area of the cell is available for contacts, an optimised contact layout in IBCs can minimise the grid resistance due to the contacts [59]. All the back-surface area of an IBC is available for contacting, allowing the potential for novel and automated ways of interconnecting co-planar cells through conductive back sheets with the contacts [59], [60]. Metal grid designs can be optimised towards creating large-coverage contacts without the burden of potentially causing any optical loss. In addition, the rear placement of the emitter regions in the IBC means that the design caters for high lateral conductivity and high spectral response near the ultraviolet region of the spectrum [57].

Despite the numerous benefits from a back-contact solar cell model from Figure 13(a), there are some risks and challenges that such architectures face. The locality of the n+ and p+ emitter and electrodes risks shunting if the masking process is imperfect. Increasing the precision of such masks would increase the cost of fabrication. In addition, a high minority bulk carrier lifetime is required in order to ensure carriers can reach the appropriate collecting contacts at the rear surface [56]. Using high bulk carrier lifetime substrates, like n-type Czochralski (Cz) or FZ wafers, can potentially solve this issue as such wafers are less sensitive to common impurities and have some protection over light induced degradation [61]. A low recombination velocity at the top and bottom surface is also necessary and hence the surface passivation quality plays a large part in the performance of IBC cells. Beyond bulk and surface

recombination, contact recombination is a major impediment to effective carrier collection in IBC solar cells that possess diffused junctions with metal-silicon interfaces [16], [57].

To exceed the limitations from the diffused-junction IBC, Kaneka corporation produced a heterojunction IBC (HTJ-IBC) design which holds the current PCE world record of 26.7% in single-junction wafer solar cells [10], [15]. A cross-sectional schematic of the HTJ-IBC is shown in Figure 14(b). This cell benefits from the inherent advantages from using the back-contact model as well as reducing the contact recombination using p-type and n-type a-Si layers for carrier-extraction. Furthermore, an ultrathin (approximately 5 nm) intrinsic a-Si layer is used to passivate the top and rear surface of the crystalline absorber. Despite the considerable improvements from the HTJ-IBC model, the same issues that exist in the heterojunction cell (in section 2.2.3) still limit its performance. Ideally, a better method for carrier extraction, without using a-Si, could drastically enhance the capabilities of this type of silicon solar cell.

Other HTJ-IBC predecessors include Panasonic, who have recorded PCEs of 25.6 % [22], as well as Sharp who reported a PCE of 25.1 % [62] and SunPower with 25 % [63]. Furthermore, as IBC cells have developed over the years, increasing attention has been paid towards scaling these at an industrial level. In collaboration with the Australian National University (ANU), Trina Solar have also industrialised the IBC cell using 125 x 125 mm and 156 x 156 mm Cz substrates, achieving PCE's of 22.1 % and 23.2 % respectively [64]. Other companies, including Samsung and Bosch, have reported the development of large-area cells using the IBC model with relatively robust efficiencies between 22.1 - 22.4 %. The current large-scale applicability of IBC silicon wafer solar cells brings increasing attention towards developing high-efficiency industrial IBC cells with the incorporation of a thermally-stable, simplified and cost-effective fabrication process.

2.2.5 Progress & future of Si solar cells

The silicon solar cell architectures discussed up to now are the primary models used in silicon PV. The progress in PCE of such technologies, as well as all other PV technologies (beyond silicon PV), between the years 1976 and 2020 are shown in Figure 15 [10]. Amongst the crystalline Si cells (blue traces in Figure 15), Kaneka's HTJ-IBC holds the highest record at 26.7 %. Other record holding architectures include the p-type crystalline silicon cell with polysilicon on oxide (POLO) contacts for the Institute for Solar Energy Research Hamelin (ISFH) that possesses a PCE of 26.1 %. More information on the POLO contact structure is provided in the next chapter. Beyond silicon PV, the single-junction gallium arsenide (GaAs)

cell has seen noticeable improvements over the years, with the current record PCE at 27.8 %. Furthermore, other emerging technologies like perovskite cells have seen major improvements over recent years, with an astonishing upturn in PCE by over 12 % between the years 2014 and 2020. Despite the competitive PCEs that other single junction solar cells have presented in recent years, silicon PV remains at the forefront of the commercial PV market. From the other types of single junction cells mentioned, the GaAs cell suffers from the inherent high cost of the rare elements used for the absorber layer. In addition, perovskite cells currently still suffer from optical stability issues.

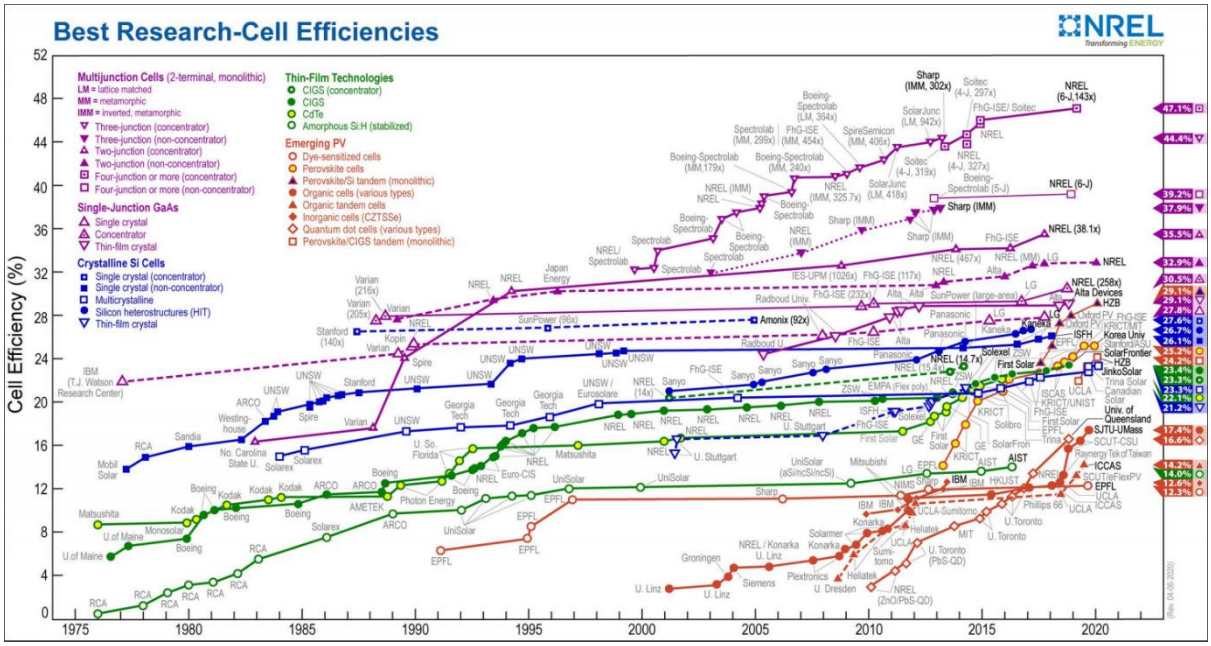

Figure 15: Research-scale progress in power conversion efficiency of PV devices between 1976 and 2020 [10].

Beyond single-junction solar cells, multi-junctions offer a much higher PCE potential as the Shockley-Queisser limit is exceeded by using multiple absorber layers. For example, a tandem solar cell can be created by stacking two cells vertically. Tandem solar cells provide an alternative photophysical solution to theoretical efficiency limitations by splitting the solar spectrum and minimizing the amount of thermalization using multiple absorptions [18], [65], [66]. The optimum band gap for the sub-cells within a tandem cell consists of a top cell at 1.7 – 1.8 eV and a bottom cell at 1.1 eV [67]. For such purposes, a crystalline silicon solar cell satisfies the bottom cell requirements. For the top cell, the perovskite cell has been shown to possess a tuneable band gap of 1.55 – 2.3 eV depending on the stoichiometry of the halide [68], [69]. The absence of the top electrode in IBCs allows monolithic stacking with other photovoltaic materials like perovskites. This exemplifies how adaptable the IBC model can be

and explains why this architecture holds high interest amongst the photovoltaics community. Currently, perovskite-IBC tandem architectures hold a record PCE of 29.1 %. This type of technology is far from its limits and is currently a well-researched topic in the field. In fact, to overcome the fast approaching PCE limit of 29.4 % for single-junction solar cells, there is a common belief in the PV community that tandem cells with carrier-selective passivating contact IBCs as the base cell will be the key driver in coming years [10], [16], [25]. As seen in Figure 15, other types of multi-junction cells, such as triple-junction and four-junction cells, have achieved astonishing record PCEs up to 47.1 %. However, these cell architectures suffer from extremely costly fabrication methods and processing requirements, due to the complex fabrication flow and rare earth elements (e.g. indium and gallium) used. These types of cells tend to be mainly focused towards space applications and are still far from reaching the consumer market.

Chapter 3

Carrier-selective contacts

3.1 Quantifying Carrier-selectivity

Carrier-selectivity in PV refers to the mechanism for maximising the flux of one type of carrier whilst minimising the flux of the other through a virtual medium or surface. The word virtual refers to the interface behaving almost as a semi-permeable membrane where only one type of carrier can travel through. The flux of these carriers is dependent on the gradient in electrochemical potential for charge carriers (η) and the conductivity (σ). Hence, a good level of control is required on these parameters for creating highly selective surfaces. Experimentally, it is difficult to extract η and σ and therefore the contact recombination current, J_0, and the contact resistivity, ρ_c, are generally used instead [16], [17]. In this method, J_0 represents the flux of non-collected charge carriers at the contact. In other words, this is a measure of the recombination at the contact and should be kept as low as possible. Furthermore, ρ_c measures the resistance to collected charge carriers and should also be minimised. The metrics for carrier-selectivity mentioned here are summarised in Figure 16. When considering carrier-selectivity, J_0 and ρ_c are two primary performance metrics that are used widely in literature for comparing various contact architectures. In essence, these two parameters are interrelated as they both depend on the conductivity of charge carriers through the surface. Hence, to simultaneously minimise both J_0 and ρ_c, the conductivity of majority carriers must be maximised and the conductivity of minority carriers needs to be minimised [24]. Historically, highly-doped regions in the silicon absorber were used as a way of modulating the concentration of such carriers at these surfaces. However, due to the reasons discussed in the previous chapter, our aim is achieving this asymmetry in conductivity without using this lossy process.

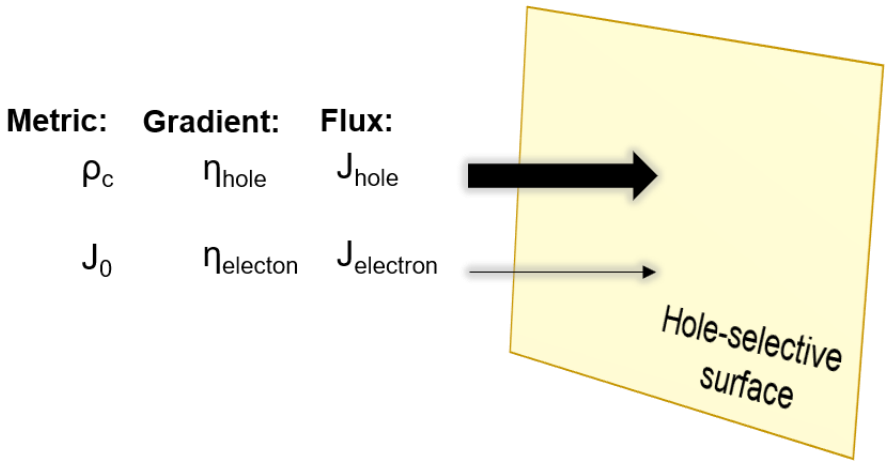

Figure 16: Schematic representation of a hole-selective virtual surface.

As mentioned in the previous chapter, the heterojunction cell possesses a form of carrier-selective contact where the band offsets between the absorber and carrier collection layers are engineered to control η for electrons and holes. This type of cell evades the typical high doping approach. Prior to examining the heterojunction method in more detail, we study the effects of J_0 and ρ_c on the performance of such solar cells further. We use Quokka, a commercial simulation software, to measure the electrical performance of a heterojunction silicon solar cell (similar to Figure 13(a)) with these two contact parameters swept at suitable ranges. The PCE as a function J_0 and ρ_c is shown in Figure 17. It is evident that a J_0 and ρ_c of less than 100 pA/cm^2 and 5 Ωcm^2 are required to reach a PCE of ~20 %. For high-performance heterojunction devices that can exceed 22 % in PCE, J_0 and ρ_c must be less than 100 fA/cm^2 and 1 Ωcm^2 respectively. In general, a relatively linear relationship between contact resistivity and PCE (due to changes in operating voltage) is realised from Figure 17. When the contact resistivity is sufficiently low, it becomes inconsequential towards the cell performance. In fact, it is found that if ρ_c can be kept less than ~0.14 Ωcm^2, its effect on a full-area contacted silicon solar cells performance becomes insignificant [70]. In contrast, an approximately logarithmic relationship is seen between J_0 and PCE. Ultimately, the contacted J_0 remains significant until another recombination mechanism in the device dominates (i.e. becomes more detrimental to the cell voltage).

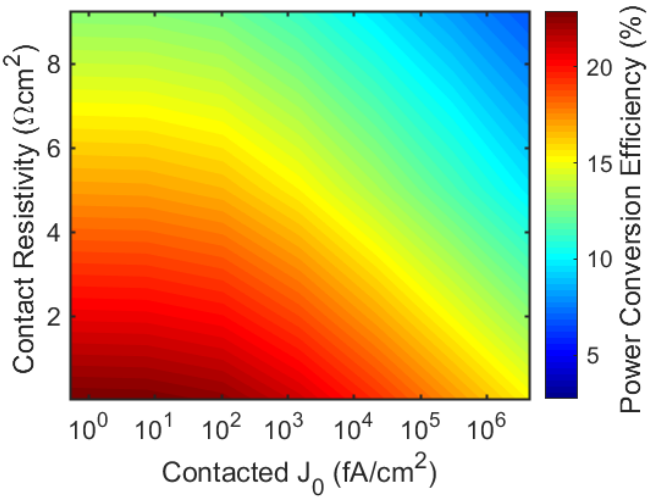

Figure 17: Quokka simulation showing the impact of J_0 and ρ_c on efficiency of an HTJ cell.

The measured J_0 and ρ_c from some of the leading contact architectures taken from recent literature [16], [24], [71] are shown in Table 1. From these structures, the Tunnelling Oxide Passivating Contact (TOPCon) possesses a highly competitive PCE of 25.7 %, due to relatively low J_0 and ρ_c. More information on this cell architecture is provided in section 3.3. Despite the classical HTJ having a ρ_c that is an order of magnitude higher than the TOPCon case, this architecture is also a leading design with a PCE of 25.1 %.

Table 1: The performance of various contact architectures in photovoltaics [16], [24], [71].

Contact architecture	**ρ_c (Ωcm^2)**	**J_0 (fA/cm^2)**	**PCE (%)**
Classical HTJ – Kaneka	0.02	10	25.1
TOPCon – ISE	0.005	4	25.7
TiO_x – ANU	0.25	30	22.1
p-PERC	0.04	140	20.7

3.2 Carrier-selectivity via Heterocontacts

In PV, carrier-selectivity is generally achieved by either creating a homojunction or heterojunction within the device. Typically, if the energy band gap between two materials or media of interest are identical, a homojunction is considered. For example, forming highly-doped regions in the silicon absorber layer is a form of homojunction where only the position of the Fermi level varies. On the other hand, a heterojunction is considered as the interface between two different materials that possess dissimilar band gaps. This includes materials that are constituted by the same chemical element but with different crystal structures (e.g.

amorphous and crystalline Si). We show examples of the energy band diagrams in a conventional p-type dopant diffused cell and n-type silicon heterojunction cell in Figures 18(a) and 18(b) respectively. Despite the noticeable difference in the energy band diagram between the two approaches, the fundamental mechanism for carrier-extraction in both homo and heterojunctions is the same – generate a high σ_{hole} and low $\sigma_{electron}$ at the hole-selective contact and vice versa. The dopant diffused approach achieves this by modulating the concentration of majority carriers at the silicon absorber surfaces which in-turn regulates η_{hole} and $\eta_{electron}$. The heterojunction approach achieves this regulation by interfacing the absorber with other materials that have valence and conduction band positions (relative to c-Si) that are favourable towards the extraction of one type of charge carrier and can block the other. In addition, the selection of these materials is dependent on their ability to chemically passivate the silicon surface. These types of heterojunctions that are used for carrier extraction are named heterocontacts.

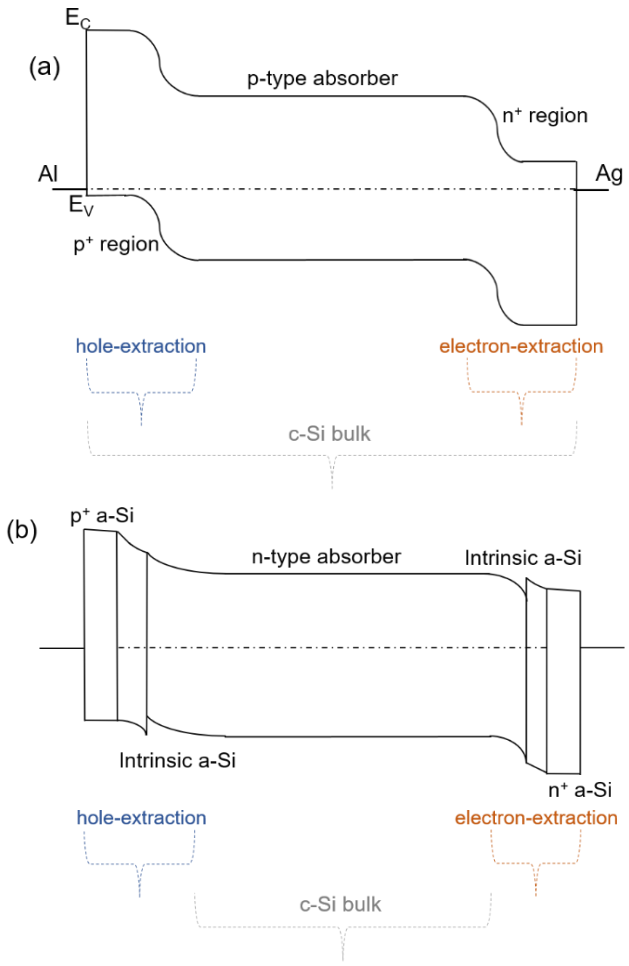

Figure 18: Energy band diagram of conventional (a) p-type dopant diffused and (b) silicon heterojunction solar cell at thermal equilibrium.

The use of heterocontacts for carrier collection in PV is typically known as a carrier-selective or passivating contact [16]. As mentioned, the function of these contacts is split into creating an asymmetrical conductivity for holes and electron at each respective contact and controlling the surface carrier concentration of the absorber layer. Achieving both of these is vital towards reaching high-performance devices, but both are not vital when considering carrier-selectivity. The combination of these two attributes enhances the efficient extraction of carriers at each contact and avoids the reduction in operating voltage. Typically, this can be a multi-layer architecture – e.g. a heterojunction cell uses an ultrathin (i)a-Si:H layer sandwiched between a p or n-type a-Si layer and the crystalline silicon absorber. The combination of these thin films on the absorber creates both excellent chemical passivation that reduces the flux of unwanted carriers and the appropriate modulation of η_{hole} and $\eta_{electron}$ due to the interfacial band structure created (shown in Figure 18(b)).

Ideally, our carrier-selective passivating contacts should be comprised of wide band gap heterocontacts that asymmetrically overlap the band structure of the absorber at each collection surface. This is to create no energy barrier to desirable carriers whilst generating a large barrier to the passage of unwanted carriers. Furthermore, the use of wide band gap materials mitigates parasitic photo-absorption in the carrier-extraction regions. The energy band overlaps at a crystalline silicon interface, namely the energy band offsets, of some typical thin films taken from literature [72]–[78] are shown in Figure 19. Based on the band offsets presented, it is evident that a-Si, SiO_2, Al_2O_3 and HfO_2 are more suitable to electron-extraction, whereas NiO and PEDOT:PSS are better for hole-extraction. This can be realised by determining the ratio between the conduction and valence band offsets ($\Delta E_C/\Delta E_V$), where a value larger than 1 is indicative of a hole extraction layer and vice versa. The absolute $\Delta E_C/\Delta E_V$ value can also determine how *carrier-selective* that layer is. For example, the $\Delta E_C/\Delta E_V$ for SiO_2-Si being 0.71 and for Al_2O_3-Si being 0.57 is indicative that the band offsets at the Al_2O_3-Si interface are more favourable towards electron transport.

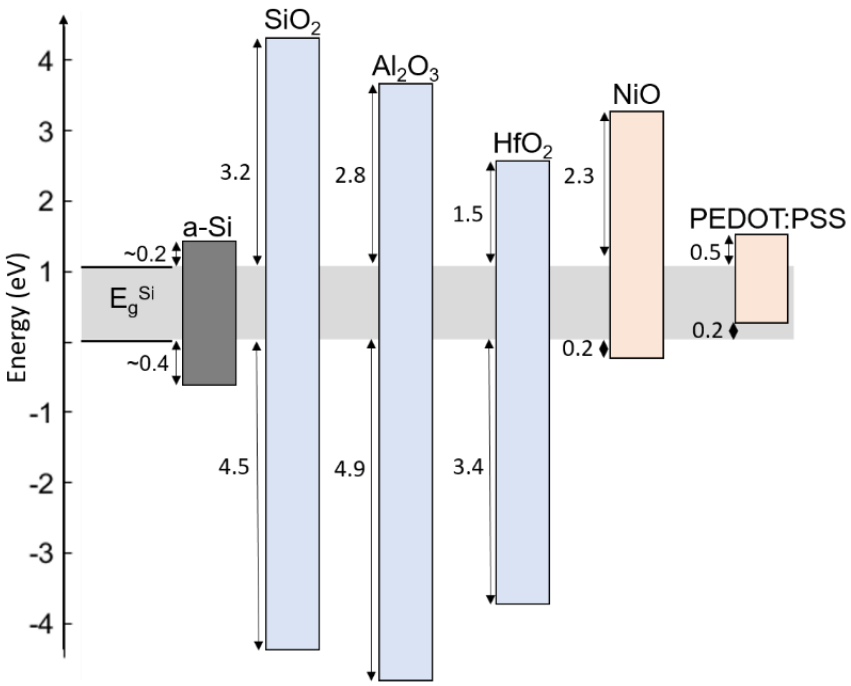

Figure 19: Valence and conduction band offsets of various thin film materials with respect to c-Si [72]–[78].

By introducing a passivating heterolayer, the option of either completely removing thermal diffusion or at least reducing the doping concentration of the thermal diffusion process is provided. Consequently, the opportunity for significantly reducing the level of doping and hence Auger recombination exists. In this approach, the limitations from requiring the formation of non-contacted and contacted regions (as in conventional approaches) can be eradicated, as well as enhancing lateral conductivity with larger area rear contacts [16], [70]. A good example of this approach is in the various polycrystalline silicon (poly-Si) type contacts in literature, e.g. TOPCon and POLO. The hybridisation of heterocontacts and doping in these contacts has enabled the formation of highly competitive contact architectures in PV research. We now study some of these architectures in further detail.

3.3 TOPCon and POLO

Tunnel Oxide Passivating Contact (TOPCon) technology is an emerging area of PV research that originated from Fraunhofer ISE [79]. In this approach, an ultrathin SiO_x layer is used at the rear of the absorber to both allow electron tunnelling and to chemically passivate the rear surface of the silicon absorber. This is due to the favourability towards electron transport (as discussed in section 3.2) and the relatively low density of defect states at the SiO_2-Si interface [20]. In addition, a phosphorus doped poly-Si layer is sandwiched between the metal electrode

and the SiO_x layer to both further promote electron conduction towards the electrode and to reduce the density of defects that form during heat-treatment at the metal-SiO_x interface [80], [81]. Despite these advantageous traits, achieving equally favourable properties at SiO_x thicknesses less than ~2 nm presents one of the main challenges with this structure. In order to maximise the efficiency of TOPCon cells, typically an annealing or hydrogenation step is required for crystallising the poly-Si layer (from a-Si) and saturating defects in the heterocontact with hydrogen atoms, which enhances the operating voltage of the solar cell [82]. A cross-sectional schematic diagram of a typical TOPCon silicon solar cell is shown in Figure 20(a).

The transport of electrons in TOPCon is understood to proceed by two different mechanisms [83], [84]. The first is from our understanding of changes in band offsets causing shifts in η_{hole} and $\eta_{electron}$ at the contact-absorber interface, namely quantum tunnelling. The other mechanism that is understood to contribute to carrier transport in TOPCon is the transport through pin holes, which are small opening within the oxide layer that causes electrical shorting between the following layers [17], [85]. The mechanism for carrier transport is generally dictated by the post-formation annealing steps conducted, where treatments above 900 ^oC are known to disrupt the SiO_x structure [85]. For annealing temperatures at or below 800 ^oC, there is still little tangible evidence for pinhole formation in TOPCon [85], [86]. Moreover, annealing at such temperatures is known to cause the diffusion of dopants from the poly-Si layer to the SiO_2 layer and even through to the absorber. Although this increases the conductivity of majority carriers, dopant diffusion introduces defects into the absorber that limit the electrical performance. Ideally, this would be an in-situ doping growth process that can form poly-Si films as-deposited, that would require minimal or even no post-formation annealing. Also, better control on the doping profile of such poly-Si layers would provide further benefit towards efficient carrier extraction from such contacts.

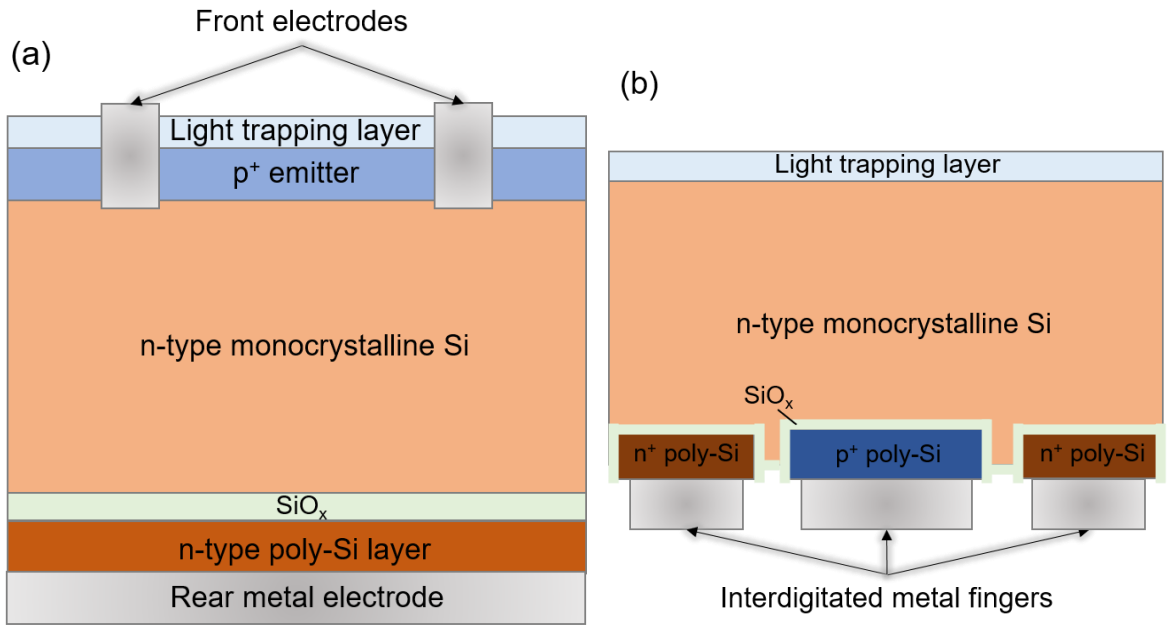

Figure 20: Cross-sectional schematic of (a) typical TOPCon and (b) POLO-IBC solar cell.

Due to the possibility of further enhancing carrier-selectivity, e.g. via the high fixed charge density in the poly-Si layer or the work function of the metal electrode, it has been found that TOPCon can be extended to form hole-selective contacts [16], [87]. Using a p^+ poly-Si layer and a high work function metal is known to promote hole selectivity in TOPCon. This is not as efficient as electron extraction as the band offsets of SiO_2-Si favour electron transport. Nonetheless, this technology has led to the Institute for Solar Energy Hamelin (ISFH) successfully fabricating a 26.1 % efficient Polycrystalline silicon on oxide (POLO) IBC (POLO-IBC) in 2019 [87]. A cross-sectional schematic diagram of a POLO-IBC is presented in Figure 20(b). This technology utilizes the advantageous traits from the IBC solar cell design (discussed in section 2.3.4) as well as the collection of electrons and holes using n-type and p-type TOPCon, respectively. Despite the highly competitive PCE achieved by the ISFH POLO-IBC, the hole-selective contacts are not optimised at this stage and this architecture still suffers from electrical losses in this region. In general, using SiO_x for hole contacts have not reached the same high efficiencies as have been achieved for electron contacts in literature [17], [27], [88]. Furthermore, the inherent issues with using an ultrathin SiO_x layer sandwiched between a poly-Si layer that requires post-formation heat-treatment still exist. Currently, work into alternative structures for hole contacts is an important area of research and presents a key sought-after development to be accomplished in this industry [16], [30], [31]. To date, the most promising material candidates have been p-type amorphous silicon and silicon-rich silicon

carbide, but compatibility with conventional high temperature Ag screen printing still remains a big issue with this architecture [15], [26].

3.4 Potential for SiN hole-selective contacts

Silicon nitride is renowned for its superior silicon surface passivation ability [20], [89]. The semi-continuum of forbidden energy states that arise at the surfaces in a solar cell are known to be well saturated by silicon nitride. To date, there have been no studies on using silicon nitride for carrier-selective contacts. Nonetheless, the use of this material as an anti-reflection, surface passivating layer has led to some studies on the interface between SiN_x-Si. The optoelectronic properties collated from literature [78], [90], [91] for this interface are shown in Table 2. In Table 2, ΔE_C and ΔE_V are the conduction and valence band offsets, and m_{0e} and m_{0h} are the electron and hole effective masses, respectively. Typically, the SiN_x has been deposited via plasma-enhanced chemical vapour deposition (PECVD). In addition, the band offsets presented from Robertson et al. [78] are merely theoretical calculations as no experimental report exists on the empirical values of band alignment at the SiN_x/Si interface. As discussed in section 3.2, these band alignments are important for dictating selectivity to carrier transport at such interfaces.

Table 2: Optoelectronic properties of PECVD Si_3N_4 [78], [90], [91].

Dielectric	**Band gap (eV)**	**ΔE_C (eV)**	**ΔE_V (eV)**	**m_{0e}**	**m_{0h}**
PECVD Si_3N_4	5.2 eV	2.3 eV	1.8 eV	0.5	0.5

Theoretical calculations for the band offsets at an Si_3N_4/Si interface show hole transport being favourable, with a 28% larger barrier to electron tunnelling than that for holes, measured in a $\Delta E_C/\Delta E_V$ factor of 1.28 [78]. The relatively large optical band gap is beneficial as this can avoid parasitic photo-absorption. Also, m_{0h} is lower for Si_3N_4 than what is recorded in literature for SiO_2 (m_{0h} = 0.77), whilst m_{0e} is identical between the two dielectrics (m_{0e} = 0.50) [72]. In POLO solar cells, the SiO_2 layer must be considerably thinner in the hole contact to cater for the higher effective mass [17], [27]. A reduction in dielectric thickness reduces the chemical passivation quality of the dielectric layer when dealing with such nanolayers (with thicknesses between 1.2 – 1.5 nm). Hence, this would result in a drop in the overall operating voltage when used as a device due to a higher carrier recombination rate. As an alternative, the limitation

with thickness could be eradicated if silicon nitride were to be used, as the effective mass does not change between electrons and holes in this dielectric.

A further option could be combining silicon nitride and oxide as an oxynitride layer as a passivating hole-tunnelling layer. Some of the best passivation results for Si_3N_4 include an oxide or oxynitride layer sandwiched between the Si and Si_3N_4 [20], [92]. In this approach, the field effect passivation from the fixed positive charges in the SiN layer is reduced but remains adequate to add passivation. For creating hole tunnelling, it is suggested by Feldmann et al. that silicon nitride is not a viable option due to fixed positive charges in a PECVD grown Si_3N_4 layer that would create an inversion layer in the contact [93], [94]. Nevertheless, whether these charges form during other processing techniques, or if they are sufficient to cause inversion in an ultrathin layer has not been determined.

In order to process silicon nitride for thin tunnelling layers, a good level of control on the growth rate and stoichiometry must be achieved. Inherently, PECVD is commonly used to grow thick SiN_x films for anti-reflection and/or passivation purposes. This method typically uses silane (SiH_4) and ammonia (NH_3) as precursors to grow Si_3N_4 layers. However, the relatively fast growth rate (between 0.4 – 1 nm/s) provides poor control and results in non-uniform films [92], [95]. Also, the continuous bombardment of plasma can cause morphological damage to the substrate surface. Another common method for depositing SiN_x is jet vapour deposition, where a supersonic jet of inert gas is used to transfer atomic Si and N in a microwave cavity towards the substrate. The growth rate of this technique can be controlled to as low as a monolayer per minute, however this method suffers from high surface damage due to the bombardment of precursor species onto the substrate [96]. As an alternative, atomic layer deposition (ALD) offers highly controllable growth rates with minimal surface damage. In fact, Knoops et al. have shown that using bis(tert-butylamino)silane and N_2 gas as precursors, highly stoichiometric silicon nitride films can be grown using plasma enhanced ALD [97]. The N_2 plasma in this process is generated inductively rather than capacitively, meaning that the plasma damage is significantly reduced in this method. Knoops et al. exhibited that growth rates as low as 0.2 Å per cycle can be achieved, forming silicon nitride films with good thickness uniformity [97].

3.5 CVD processes for conductive layer formation

As discussed in section 3.1, a layer with high fixed charge density is required in between the tunnelling dielectric and the metal electrode to form high-efficiency heterocontacts. This is to both improve the passivation between these two layers as well as modulating the surface carrier concentration of majority carriers to increase their conductivity. Unfortunately, the typical processes used for forming this layer require ex-situ doping and post-formation annealing which can cause dopant diffusion through the tunnelling layer and be detrimental to device performance. Therefore, we also investigate other potential fabrication methods for growing p-type crystalline silicon films with in-situ doping and no/minimal post-treatment required. If successful, this method could also be extended to create conduction layers in other regions of silicon PV devices (e.g. emitter).

CVD is a basic tool for manufacturing that is widely used across different sectors of industry. The process involves the controlled flow of precursor gases, which are vaporised via either thermal energy or pressure, into a chamber where the designated seed layer is located. The wafer surface does not react with the gases but serves as a substrate. There are several different types of CVD processes, the resulting depositions from which differ in density and coverage. Here we first briefly look at the industry-standard PECVD process to gain appreciation for why this is currently in play. We then focus on hot wire CVD (HWCVD) due to the highly beneficial traits that this thin film fabrication process possesses.

3.5.1 PECVD

PECVD is generally operated between 250°C and 350 °C depending on the specific film requirements, which is typically lower than general CVD. The lower deposition temperatures are critical in many applications where high temperatures could damage the devices being fabricated. Deposition via PECVD is achieved by releasing precursor gases between parallel electrodes where the capacitive coupling excites the gases into a plasma. This induces a chemical reaction onto the substrate, which is placed on the grounded electrode, where the reactant product is deposited.

PECVD technology is well-developed and is applied in many different fields, including small devices in the semiconductor industry, large-area flat panel displays and glass manufacturing. Gabriel et al. have used this method to successfully fabricate liquid-phase crystallised silicon solar cells onto large substrates (30 cm × 30 cm) [98]. In addition, Wehmeier et al. have used

PECVD for boron silicate glass layers, allowing them to fabricate solar cells with a single high-temperature co-diffusion process which minimised the total number of process steps, producing cells with up to 19.85% PCE [99]. The high versatility in this thin film fabrication processes has allowed many branches of the semiconductor industry to use PECVD for various applications.

3.5.2 HWCVD

HWCVD has developed to become a mature form of chemical vapour deposition (CVD) when compared to other CVD tools [100]. In the late 1980s, Matsumura and Tachibana used HWCVD to successfully produce hydrogenated amorphous silicon, which demonstrated a relatively high deposition rate at the time [101]. Mahan et al. in the early 1990s also produced hydrogenated amorphous silicon but at a device level [102]. These successes raised interest in the tool as a deposition technique and permitted the first thin film solar cells using HWCVD in 1993 by NREL and the University of Kaiserslautern [103]. Since then, multiple groups have managed to produce amorphous, microcrystalline and polycrystalline silicon thin films using this tool, with doping both p-type and n-type proving feasible [104], [105]. Selective area epitaxial film growth on silicon wafers has also shown viability [32], [106]. HWCVD is attracting attention for making higher quality interfaces by avoiding plasma damage of the substrate. This single-sided deposition method is capable of producing highly uniform films, for both thickness and doping concentration, in a controlled manner. In addition, this process is easily scalable to industrial processes.

Using HWCVD in various fabrication processes for IBC solar cells has proven beneficial, if not the same as other more energy consuming fabrication tools in literature. The work by Payo et al. on selective-area boron-doped silicon formation supports this with IBC cells in the high efficiency range of >22% [106]. Selective growth refers to a type of CVD growth that is a balance between silicon deposition and etching upon substrates where selected regions of the surface are masked with a dielectric and the remaining regions are free of any material. Payo et al. determined that this is only feasible on the condition that there are no pinholes on the dielectric, creating an imperfect mask, and that a surface roughness of <75 nm was sufficient for good epitaxy [106]. Branz et al. have also used HWCVD for growing silicon films, proving that an unlimited crystalline silicon thickness is possible on HF-dipped (100) silicon wafers [107]. For example, at 700 ^{o}C, growth continued to 40 µm in thickness before the experiment was terminated [107]. Furthermore, their work also shows the potential of growth on more

difficult silicon surfaces, where they have shown growth on (111) silicon wafers. Ingenito et al. also applied CVD for IBC cells by fabricating c-Si solar cells with epitaxial growth used for boron-doped emitter regions, while using phosphorus ion implantation to form the front and back surface field [57]. Their main aim was to design a fabrication process that could minimize the number of lithographic steps and the thermal budget. They successfully fabricated IBC c-Si solar cells with J_{sc} at a competitive value of 41 mA/cm^2 and overall cell efficiencies above 20 % [57]. These examples highlight some successful applications of HWCVD in current PV fabrication processes. We study this tool in more detail in the Chapter 4, as well as providing various findings using this process in Chapter 5.

Chapter 4

Experimental Methods

This chapter describes the experimental and analytical techniques used in later chapters. This is broken down into three sections that cover the fabrication procedures, characterisation methods and device modelling techniques used. Each sub-section briefly describes the apparatus or technique, provides some detail on the background principles, and discloses where they will be used later in this thesis.

4.1 Nanofabrication and processing methods

4.1.1 Hot wire chemical vapour deposition

Hot wire Chemical Vapour Deposition (HWCVD) is a vapour deposition technique where the catalytic dissociation of precursor gases at a heated filament allows film growth onto a designated seed layer [102], [104]. Using this low-pressure deposition technique, the precursors, which are generally SiH_4 and B_2H_6 for p-doped and SiH_4 and PH_3 for n-doped films, are injected onto a heated Tungsten filament where ionisation releases free radicals. These radicals, depending on the type, either adhere onto the seed layer forming the first monolayers of growth or onto the walls of the chamber where they are gradually pumped out. Figure 21 illustrates the growth process in the HWCVD chamber in a simplified format.

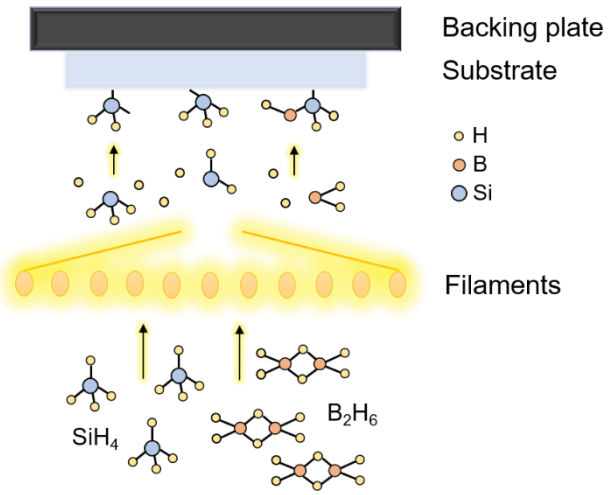

Figure 21: Schematic diagram of catalytic dissociation of precursor molecules in HWCVD chamber.

The Nitor 301 HWCVD instrument is used in chapter 5 to grow boron-doped silicon films. The tool is comprised of a process chamber, a load-lock and a wall mounted gas cabinet. The wall mounted gas cabinet houses seven Mass Flow Controllers (MFCs), isolation valves for the process gases, and the associated pneumatics control system. Available process gases are SiH_4, PH_3, B_2H_6, GeH_4, NH_3, and H_2. The cabinet also houses the nitrogen purge/vent lines for the process and load-lock chambers. Further details on the operation and configuration of the HWCVD chamber, as well as the growth recipes used, are provided in the next chapter.

4.1.2 Plasma-enhanced atomic layer deposition

Atomic layer deposition (ALD) is an advanced deposition technique capable of achieving ultrathin films with Angstrom (Å) level resolution in a reliable and controlled manner. This technique benefits from self-limiting surface reactions, reducing the likelihood of pin-hole formation, as well as allowing 3D structures to be covered with a conformal coating. Furthermore, ALD produces films with good adhesion with underlying substrates and these are generally deposited at relatively low chamber table temperatures. This technique is highly applicable for depositing materials including oxides, nitrides, fluorides, sulphides and metals. Ultimately, the high level of film and interface control is attractive towards thin film fabrication for photovoltaic applications.

Conventionally, ALD is a cyclic process, whereby multiple processing steps form an ALD cycle which are then repeated several times depending on the film thickness required. Each ALD cycle consists of four process steps:

1. **Dose** - Precursor is adsorbed and reacts to surface of substrate.
2. **Purge** - Any excess precursor is purged out of chamber.
3. **Plasma exposure** - Surface exposed with plasma composed of either oxygen or nitrogen free radicals that oxidise the surface, with reaction products depending on the precursor used.
4. **Purge** - Reaction products are purged out of chamber.

These steps describe a plasma enhanced ALD process, with the only difference with thermal ALD being in the use of H_2O instead of O_2/N_2 plasma. An Oxford Instruments FlexAL ALD tool is used in chapter 5 and 7 for AlO_x growth, and in chapter 6 for SiN_x growth. Figure 22 shows a schematic diagram of our ALD chamber. Further information regarding the growth recipes and processes are described in the respective chapters.

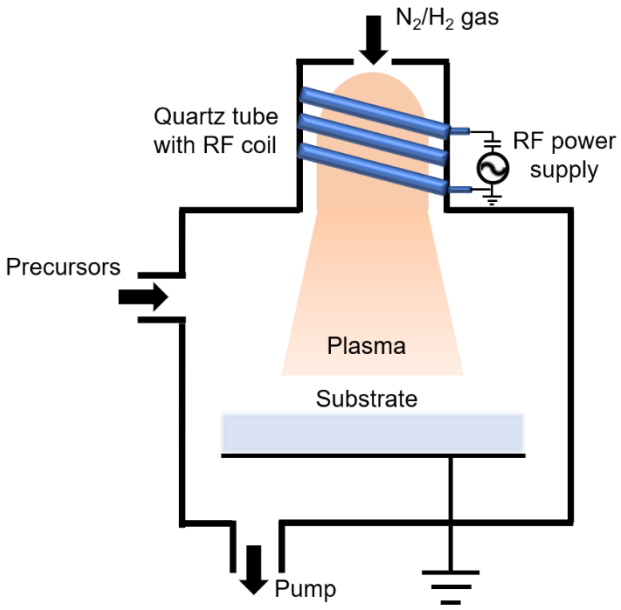

Figure 22: Schematic diagram of plasma-enhanced atomic layer deposition chamber.

4.1.3 Electron-beam evaporation

Electron-beam (E-beam) evaporation is a process where a beam of electrons is used to evaporate metal and consequently deposit on designated specimen. To generate the E-beam, electrical current is passed through a Tungsten filament, generating thermionic emission, and a high voltage is applied to accelerate the electrons. Using a strong magnetic field, the electrons are focused into a unified beam which is directed at the crucible containing metal. The energy of these electrons is then transferred to the metal, causing it to evaporate towards and deposit

onto the substrate. Figure 23 shows a simplified schematic diagram of the E-beam evaporation process described.

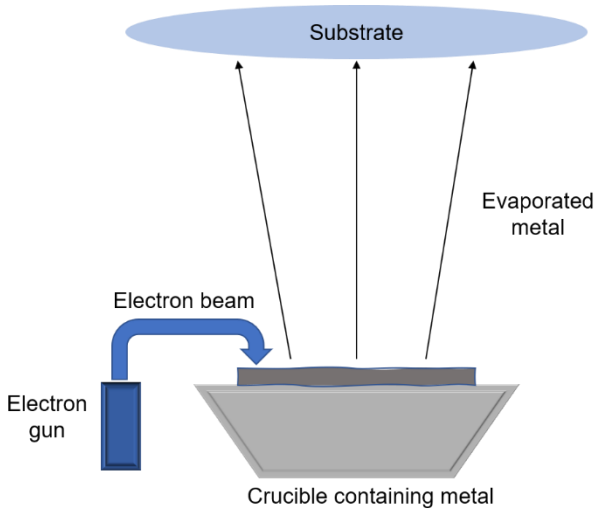

Figure 23: Simplified illustration of E-beam evaporation process.

An alternative metal deposition process that could have been used instead of E-beam evaporation is thermal evaporation. However, due to the inherent advantages of E-beam over thermal, we use E-beam evaporation in chapters 5 and 7 for Al and Au electrode depositions. These advantages include the ability to maintain the purity of the deposited metal by confining the electron beam to only the designated source material, as well as the E-beam being capable of heating materials to higher temperatures which permits higher deposition rates.

4.1.4 Rapid thermal annealing

Rapid thermal annealing (RTA) is a thermal treatment process which can be used instead of conventional tube furnace annealing or heat treatments. This method is advantageous due to the high heating and cooling ramp rates of up to 25 ^{o}C/s and simplicity in processing. Some typical high temperature applications of this tool are dopant activation in films with a high fixed charge density and re-crystallisation or crystal healing. In a typical RTA instrument, the furnace is built with a thermocouple and a pyrometer installed, which allow the temperature of a wafer to be measured. The thermocouple is used for sensing temperatures below 500 ^{o}C, whilst the pyrometer is used for temperatures above 500 ^{o}C. When in use, the thermocouple is in direct thermal contact with the rear of a substrate. The pyrometer measures temperature via the infra-red radiation emitted from the rear of a wafer. A thermocontroller operates the power supplied to the heating lamps to reach a set temperature, operating over 8 temperature zones. Each of these zones is defined by PID (Proportional Integral Differential) gains which define

properties of the heating such as time taken to reach set point, overshoot at set point, and time to settle once a set point has been reached.

In chapters 5-7, a JipElec RTA tool is used extensively. The uses of this in our work include the re-crystallisation of silicon films grown via HWCVD, activation of fixed charges in AlO_x passivating layers and improving the interfacial properties of Al electrodes. Further details on these processes are described in their respective chapters.

4.1.5 Wafer cleaning and wet chemical etching

To be able to fabricate high-performance photovoltaic devices, silicon wafers must be cleaned prior to any processing. Contaminants on silicon surfaces exist in the form of discrete particles, particulates and adsorbed gases or ions, and neglecting these prior to high temperature processing can be fatal to device performance. This can also cause interfaces between the silicon substrate and grown materials to be highly defective and therefore suffer from high carrier recombination and an overall lower minority carrier lifetime in fabricated devices. In our experimental studies, we clean our silicon wafers with fuming nitric acid (HNO_3). This is a powerful acid and oxidising agent that is conventionally used for this purpose in the photovoltaics industry. After this cleaning process, a thin SiO_x layer is formed at the surface of the Si wafer which must be etched prior to further processing.

In our work, we use 7:1 buffered hydrofluoric (HF) acid solution for etching of dielectrics (e.g. native SiO_x on wafers, SiO_x after cleaning/thermal oxidation and hard mask etching in our photolithography processes). The etch rate using this wet chemical process depends highly on the material structure, density and chemical compositional properties. For example, native oxide on Si has a typical etch rate of ~100 nm/min, whilst AlO_x grown via ALD is found to have an etch rate of ~ 20 nm/min using 7:1 buffered HF solution.

4.1.6 Photolithography

Photolithography refers to the process in which light is used to transfer a geometric pattern, usually in the micron scale, via a photomask onto a photo-sensitive photoresist that lies on the substrate or specimen. Through a series of etches and other chemical treatments, the exposed pattern acts as a photomask in which designated materials can be grown or deposited to create a new pattern. After this process, the photoresist is removed prior to any further processing. In general, two types of photoresist exist, namely negative and positive tone resist. Exposure of

negative resist to UV light causes the photoresist to polymerize, and the un-exposed regions of the photoresist are soluble in designated developer solutions. Conversely, positive resist becomes more soluble when exposed to UV light, meaning that the exposed regions are removed once developed. In general, higher resolutions can be achieved with positive resists, whereas negative resists benefit from a faster photo-development speed, better substrate adhesion and lower operating costs. In cases where high resolution is not required, negative tone resists are favoured.

In chapter 7, photolithography is used to fabricate devices for contact resistivity measurements using the Cox and Strack method. Further detail on the photolithography process and the procedure undertaken for these measurements is provided in this chapter.

4.2 Optoelectronic and morphological characterisation techniques

4.2.1 Raman spectroscopy

Raman spectroscopy has proven to be a robust analytical tool for investigating mechanical stress, molecular composition, phase and crystallinity of semiconductor materials in both bulk and film form over the last century [108], [109]. Raman scattering in semiconductors relates to the small proportion of photons from an incident light that undergo inelastic interactions with the crystal lattice [110]. Most photons are elastically scattered, namely Rayleigh scattering, which gives no contribution to Raman scattering. However, due to changes in vibrational or electronic energy of underlying molecules, approximately 1 in every 10^7 photons are scattered at optical frequencies lower than the frequency of the incident photons, giving rise to Raman scattering [108], [109]. In quantum mechanics, this phenomenon can be described by a laser-produced monochromatic light of frequency $\boldsymbol{\omega_i}$ incident on a crystal with direction $\mathbf{k_i}$, which produces an electron-hole pair. The excited electron interacts with a phonon with frequency $\boldsymbol{\omega_j}$ and wavevector $\mathbf{q_j}$, which causes the loss or gain of energy to the electron. Due to the recombination of the electron-hole pair, a photon $\mathbf{k_s}$, $\boldsymbol{\omega_s}$ is emitted, which gives rise to Stokes ($\boldsymbol{\omega_s = \omega_i - \omega_j}$) and anti-Stokes ($\boldsymbol{\omega_s = \omega_i + \omega_j}$) Raman scattering [111]. This phenomenon is depicted through the Feynman and energy level diagrams presented in Figure 24.

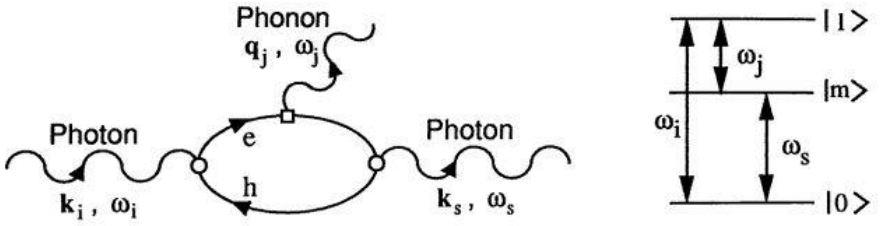

Figure 24: Feynman diagram and energy levels for a first-order Stokes scattering process [108].

For silicon Raman scattering, only the first-order silicon Stokes Raman peak at 520 cm^{-1} is of key interest. This peak tends to occur due to the absence of internal and external perturbations at that specific wavenumber [112]. The strong Si-Si bonds in crystalline silicon give rise to a sharp peak at 520 cm^{-1}. Significantly, this peak is only present at 520 cm^{-1} if the silicon lattice is perfectly crystalline. In other words, as the crystal size decreases, the silicon Stokes Raman peak shifts left (lower wavenumber). A decrease from 12 nm to 3 nm in crystal size gives rise to a peak shift from 520 cm^{-1} to 512 cm^{-1} [113]. At this wavenumber, the silicon crystal is classified as micro-crystalline (µc-si). Further left shift towards ~ 500 cm^{-1} represents nanocrystalline silicon, and a further peak arises towards 480 cm^{-1} from amorphous silicon [111]–[113]. This is generally seen as a broad peak consisting a superposition of multiple peaks due to the imbalance in crystal quality. This is generally known as polycrystalline silicon, whereby the silicon film is comprised on multiple types of crystallinities in various proportions.

A Renishaw inVia confocal Raman microscope with a 532 nm laser at 5 % laser power is used in chapter 5 for characterising the morphology of boron-doped silicon films grown via HWCVD. Further information on the characterisation of these films, as well as the Raman peak fitting method used, is provided in the proceeding chapter.

4.2.2 Scanning electron microscopy and X-ray diffraction

Scanning electron microscopy (SEM) is a type of electron microscope that scans the surface of exposed specimen with a focused beam of electrons. When these electrons interact with the surface atoms, various electronic signals are generated that are collected and interpreted into various information regarding the subjected surface. For SEM imaging, the secondary electrons that are ejected from the primary electron and surface interaction are used to generate an image of the exposed surface. These photo-ejected electrons are collected via a detector which translates the number of secondary electrons collected to an image. In chapter 5, a Zeiss

NVision40 FIBSEM is used with an accelerating voltage of 10 kV to take cross-sectional images of grown films of interest.

For morphological characterisation, X-ray diffraction (XRD) is a technique for determining the atomic and molecular structure of a material. In XRD, samples are irradiated with incident X-rays which causes X-ray emission from semiconductor materials. The intensity and scattering angles of photogenerated X-rays are collected and used for XRD analysis. In chapter 5, a Rigaku SmartLab diffractometer with a 9 kW (45 kV, 200 mA) Cu target rotating anode generator and a HyPix 3000 semiconductor detector is used.

4.2.3 Atomic force microscopy

The atomic force microscope (AFM) is a type of scanning probe microscope (SPM). SPMs are designed to measure surface properties, such as height, friction, magnetism, with a probe. To acquire an image, the SPM scans the probe over a small area of the sample, measuring the local property simultaneously. AFM operates by measuring the force between a probe and the sample. Normally, the probe has a sharp tip, which is 3-6 μm long and comes into contact with the material surface. Generally, AFM can be operated in either contact or non-contact (tapping) mode. In contact mode, the AFM tip is drawn across the material surface. On the other hand, in tapping mode the AFM tip oscillates across the material surface. In chapter 5, AFM in tapping mode is used to measure the top surface roughness of deposited films to aid the determination of their crystallinity.

4.2.4 Transmission electron microscopy and selective-area electron diffraction

Transmission electron microscopy (TEM) can provide real-space information on the atomic plane orientation and crystallographic structure of materials via high-resolution imaging. This is a type of electron microscope in which an E-beam is focused on the specimen and the transmitted electrons then create an extended version of the image over a fluorescent screen. The incident E-beam interacts with the material atoms through a series of elastic and inelastic dispersions which causes electron scattering. As TEM samples typically have thicknesses in the nanometer range (~100–200 nm), and the E-beam having an energy in excess of 100 keV, the scattered electrons are transmitted through the specimen quite easily. The transmitted electrons are then focused on the fluorescent screen using an objective lens. This microscope can be used as an instrument specifically for the analysis of dimensions in the micro space (10^{-}

^{6} m) and the nano space (10^{-9} m) [114]. In essence, the high level of detail revealed by this type of electron microscope is incomparable to any other microscopy technique.

Selective-area electron diffraction (SAED) is an advanced crystallographic analysis technique that is typically conducted inside TEM. This technique relies on the diffraction of electrons through the exposed specimen in TEM. As the incident E-beam in TEM possesses high energy, the electrons are treated like waves rather than particles when interacting with the material atoms, due to the wave-particle duality effect. Furthermore, as the spacing between the atoms is multiple orders of magnitude larger than the wavelength of the electrons, the atoms act as a diffraction grating for the incident electrons. Hence, depending on the crystal structure of the specimen, a fraction of the scattered electrons will propagate at particular angles, creating a diffraction pattern. This pattern is typically a series of spots, namely a selective-area electron diffraction pattern, and can provide useful information for studying the crystal structure of materials.

In chapter 5, a JEOL JEM-F200 electron microscope operated at an accelerating voltage of 200 keV that provides a point resolution of 0.19 nm is used. In addition, SAED is also used in this chapter, which was conducted at a 400 mm camera length using a GATAN OneView camera. All samples for this study were prepared using a FEI Quanta 3D focused ion-beam. All TEM and SAED measurements were conducted at the Henry Royce Institute for Advanced Materials at the University of Sheffield.

4.2.5 X-ray photoelectron spectroscopy

X-ray photoelectron spectroscopy (XPS) is widely used for detecting the presence of chemical elements and observing the formation of chemical compounds in various materials. This is a photoemission-based method that measures the shift in binding energy for located elements and changes in photoelectron line shape [115]. Additionally, XPS can also be used for measuring the potential at a semiconductor interface, enabling accurate determinations of heterojunction band discontinuities and Schottky-barrier heights [116].

Figure 25 illustrates the typical process conducted for XPS. Irradiating a sample with X-rays that possess sufficient energy causes electrons in specific bound states to be excited. In XPS, the x-ray energy is used to release photoelectrons from the nuclear attraction force of their element, i.e. their binding energy. Of these photoelectrons, some undergo direct emission with no energy loss, directly escaping the surface and being collected by the electron analyser. The

analyser then produces an energy spectrum showing the number of photo-ejected electrons against their binding energy, based on the kinetic energy of the electrons when collected. Essentially, the binding energy is calculated as the difference between the incident X-ray energy and the kinetic energy of the photo-ejected electrons.

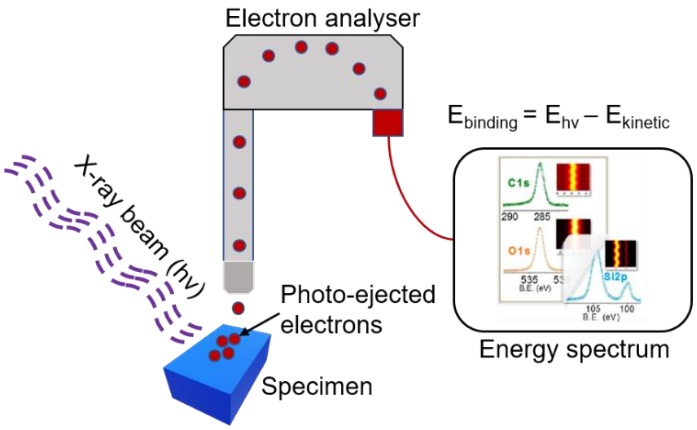

Figure 25: Simplified illustration of X-ray photoelectron spectroscopy process.

A Thermo Scientific Theta Probe XPS system with a monochromatic A1 Kα X-ray source is used in chapter 6 for analysing the chemical compositional ratio and stoichiometry of SiN_x films grown via ALD. Furthermore, this instrument is further employed for attaining the spectra used for calculating the band offsets at the SiN_x/Si interface. More details on the processes and calculations used are provided in chapter 6.

4.2.6 Secondary ion mass spectrometry

Secondary ion mass spectrometry (SIMS) is associated with analysing the chemical composition of solid films. Generally, this technique is used for determining the surface chemistry in different materials, as well as identifying trace elements or molecules at the surface. It can also be used to determine the distribution of elements or dopants through depth profiling and 3D imaging. In SIMS, a focused primary ion beam sputters atomic and molecular fragments from a surface, causing the ejection of secondary ions that are used for chemical characterisation. Typically, a mass analyser is used to detect and differentiate between various secondary ions. This is done by using the mass to charge ratio of each collected ion. For data analysis, a relative sensitivity factor is typically applied to the raw counts data to calculate the atomic concentration of respective elements.

In chapter 5, SIMS is used to measure the boron doping profile of the HWCVD polycrystalline silicon films. This is done using an IONTOF ToF-SIMS 5 instrument at University College London.

4.2.7 Spectroscopic ellipsometry

To characterise the optical properties of materials, spectroscopic ellipsometry is a robust tool that is widely used. The applications of this instrument are vast, but generally include studies involving thickness or surface roughness measurements, defining the refractive index or determining the complex dielectric constant of a material. The principle of ellipsometry involves the use of a linearly polarised light source, incident at an angle to the specimen. Due to electromagnetic interaction at the material surface, a phase shift is experienced, and the reflected wave becomes circularly polarised. Figure 26 illustrates this principle in spectroscopic ellipsometry. Note that the axes that are denoted p and s refer to the perpendicular and parallel polarisation planes respectively and indicate linear polarisation at the source in comparison to circular polarisation at the detector. In general, the difference between the phase shifts in the p and s planes are used in spectroscopic ellipsometry. In our work, a M-2000 J.A. Woollam ellipsometer is used extensively for taking spatial scans of various films for film thickness determination and optical characterisation. Further information on the spectroscopic ellipsometry techniques used are provided in the respective chapters.

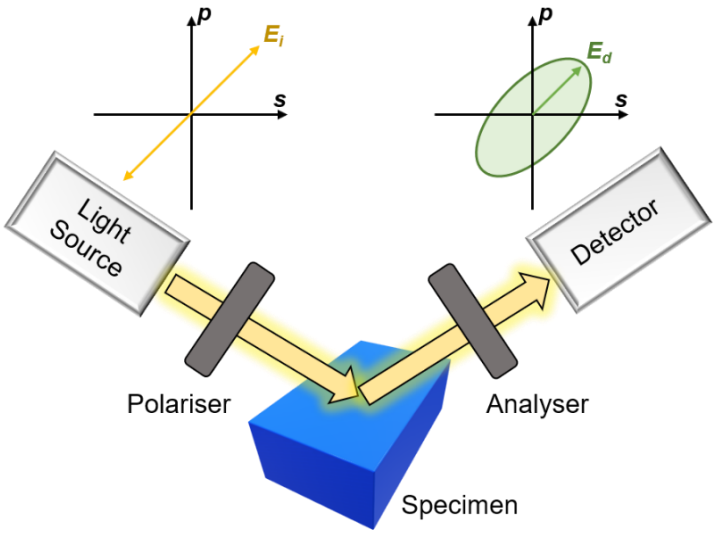

Figure 26: Simplified schematic diagram of the operation of spectroscopic ellipsometry, showing the linear and circular polarisation of light at the light source and the detector ends respectively.

4.2.8 Photoconductance lifetime

A quasi-steady-state photoconductance (QSSPC) lifetime tester is typically used for the characterisation of the passivation quality (i.e. saturation current) and dopant diffusion in PV materials or devices. Using this technique, the minority carrier lifetime can be measured under two modes, namely quasi-steady-state or transient mode. Quasi-steady state mode is used for samples with minority carrier lifetimes typically less than 200 µs. In this method, a relatively long pulse of light (1 s) is used in order to hold the excess carrier populations in steady-state, balancing the generation and recombination rates during the measurement. A conductance and light sensor are used to measure the sheet conductivity and flash intensity respectively, with which the excess carrier density (Δn) and generation rate (G) are extracted and used to calculate the minority carrier lifetime (τ_{eff}) using:

$$\tau_{eff} = \frac{\triangle n}{G} \tag{13}$$

On the other hand, the transient photoconductance decay method is generally used for samples with longer (> 200 µs) carrier lifetimes. For this, a rapid pulse of light (1/64 s) is directed onto the sample, and the conductance sensor measures the relatively slow decay of sheet conductivity and generates Δn. The derivative of Δn is used to calculate τ_{eff} as:

$$\tau_{eff} = \frac{-\triangle n}{d\triangle n/dt} \tag{14}$$

A Sinton QSSPC lifetime tester is used extensively in our work for measuring the minority carrier lifetime of various specimen. This is mainly used in chapter 5 in the passivation study conducted.

4.2.9 Current-voltage measurements

Amongst all photovoltaic device characterisation methods, one of the key electrical measurement techniques is the extraction of the current at various bias voltages, both under illumination and in the dark. Typically, these measurements are used to extract the four major metrics of PV devices. These are the short-circuit current density (J_{SC}), open-circuit voltage (V_{OC}), fill factor (FF) and power conversion efficiency (PCE). Further information on the significance of these metrics, as well as how they are extracted from current-voltage graphs, is provided in Chapter 2. A typical solar simulator set-up that is used for current-voltage extraction is illustrated in Figure 27. This consists of a source-measure unit that simultaneously provides a potential bias across the device and measures the electrical current. To measure the

electrical properties under illumination, a light source that mimics the AM1.5G solar spectrum is used for illuminating the device, as depicted in Figure 27. If measured in the dark, the diode response of the device is extracted, which is useful for extracting the dark saturation current density.

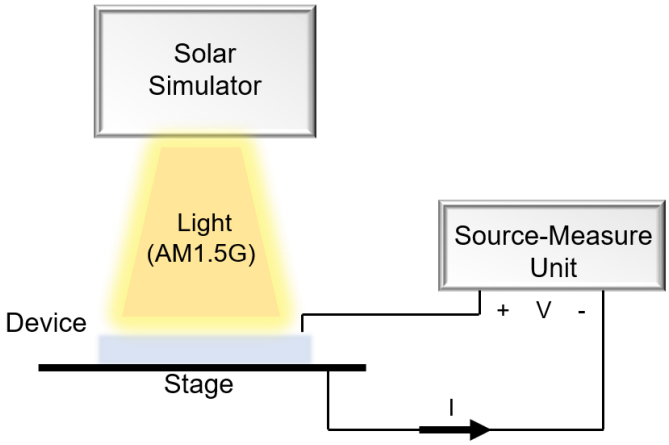

Figure 27: Illustration of solar simulator set-up used for current-voltage extraction from PV devices.

In chapters 5 and 7, an Abet Technologies Sun 3000 Solar Simulator with an irradiance power of 1000 W/m^2 and a Keithley 2400 source-measure unit is used to extract the current-voltage characteristics of our devices. In all current-voltage measurements conducted in this thesis, a forward scan is taken from -1 V to +1 V at a scan rate of 0.1 V/s.

4.3 Device simulation methods

4.3.1 Quokka 2

Simulations are a key route towards the efficient assessment and improvement of the design and performance of photovoltaic devices. To model solar cells in 1-3 dimensions, Quokka 2 is a MATLAB-based simulator that can be readily used to efficiently solve charge carrier transport in a quasi-neutral silicon device. Quokka 2 numerically solves these by defining surface dopant diffusions as conductive boundaries in the solar cell, without any major loss in generality [71]. This tool supports multiple types of cell designs, including front junction, PERC and IBC silicon solar cells. The software was written by Andreas Fell from the Australian National University (ANU) and is available online via PV Lighthouse [71], [117].

In this thesis, Quokka 2 is initially used in chapter 5 to model the IBC from [33], which is considered a robust silicon cell architecture in the field of PV. Once a working model is

completed, this is used as the platform for further simulations. Further details on the model and the simulations conducted are provided in the next chapter.

4.3.2 EDNA 2

EDNA 2 is a freely available online simulator that can determine the saturation current density, J_0, and the internal quantum efficiency (IQE) from an arbitrary doping profile [118]. The EDNA 2 algorithm operates by initially loading the background and emitter dopant profiles and calculating the sheet resistance in equilibrium. The intrinsic and equilibrium parameters of the semiconductor are then calculated as a function of depth. These include parameters like the donor (N_D) and acceptor (N_A) concentration, intrinsic carrier concentration and the electron and hole Fermi energy levels. EDNA 2 then computes the excess carrier density, Δn, as a function of distance using the shooting method, from which the carrier recombination rate is determined using EDNA's recombination calculator [118], [119]. Once the emitter's lower boundary is determined, EDNA 2 defines this as the junction and uses an iterative method to compute the current density and voltage. For further information on EDNA 2 and its capabilities, we refer the reader to [118]–[120]. In this thesis, EDNA 2 is used to compute J_0 and IQE in chapter 5 where a breakdown of these metrics, as computed by EDNA 2, is provided.

4.3.3 TCAD

TCAD Sentaurus is a visual simulator which uses physical models to represent wafer fabrication and device operation that can directly aid the optimisation of semiconductor devices [121]. TCAD can help reduce the development time and cost of semiconductor technologies, improve device design and yield and can help reduce time-consuming experimental works by providing a relatively high-speed device process and simulation flow. This tool has been successfully utilised in other research, including works by Jeong et al. using TCAD for simulations of nanocone textured IBCs [122], and Savin et al. simulating black silicon IBC solar cells [123], with both showing close agreement with fabricated devices. TCAD is used in chapter 7 for modelling the tunnelling current in various heterocontacts of interest. More detail regarding these simulations is provided in the respective chapter.

Chapter 5

P-type Polycrystalline Silicon formation via HWCVD

5.1 Introduction

Conventionally, thermal diffusion is used for doping of the conductive regions, i.e. emitter, back-surface field (BSF) and conductive layers in passivating contacts [15], [16], [57]. Despite some of these cells achieving high efficiencies beyond 20%, the production cost and complexity of interdigitated diffused junctions remain an issue [33], [57], [121]. We study silicon growth using hot wire chemical vapour deposition (HWCVD), with in-situ doping, as a low-cost alternative to forming these doped structures.

In this chapter, HWCVD is explored as a way of growing boron-doped silicon for photovoltaics devices. Some of the work presented in this chapter has been published as a material study on HWCVD films for silicon solar cells [124]. This silicon growth method is attracting increasing attention for fabricating higher quality silicon interfaces [32], [104]. The efficiency of gas use during growth is much higher than other CVD techniques, being up to ten times higher than that of plasma-enhanced CVD (PECVD) [125]. The relatively fast deposition rates, offering no plasma damage to the substrate surface, being a single-sided deposition method and the large-area deposition coverage of the tool makes scaling HWCVD towards commercial applications favourable [29], [125]. We focus on growing p-type silicon films towards emitter and passivating contacts applications. Currently, this is sought-after in the photovoltaics (PV) industry [16] for improving existing and up-and-coming cell architectures.

5.2 HWCVD deposition temperature configuration

In any chemical vapour deposition process, the deposition temperature plays an important role in dictating the crystallinity, structural density and uniformity of films grown. We monitor and attempt to control the temperature for the HWCVD process before growing boron-doped

silicon films. This will allow us to probe the capabilities of the tool, as well as defining different configurations for growing various silicon crystal structures of interest.

5.2.1 Tungsten filament configuration

A schematic diagram of our HWCVD chamber is shown in Figure 28(a). The spacing between the filaments and substrate is 5 cm, with top and bottom heaters included for further substrate temperature enhancement. The conventional filament arrangement is 31 0.2 mm diameter Tungsten filaments placed with 1.5 cm spacing in parallel, covering a deposition area of 0.16 m^2. To fabricate crystalline boron-doped silicon films, previous studies have shown that the normal configuration (NFC) requires a post deposition anneal for 1 hour at 1000 ^oC [29].

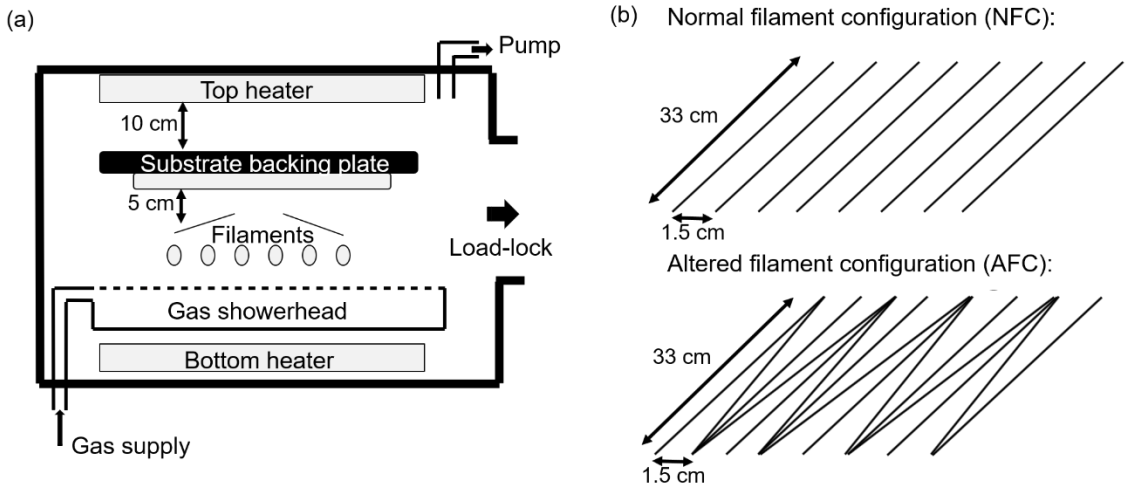

Figure 28: (a) Schematic diagram of HWCVD chamber and (b) NFC and AFC Tungsten filament configurations.

In this work, a higher density filament arrangement (AFC) is studied, as we are interested in further enhancing the deposition temperature from the conventional route. Increasing the deposition temperature can have an in-situ annealing effect, potentially producing more uniform crystalline films that require less or no annealing, further optimising our process. In addition, eradicating the annealing step can also avoid the diffusion of dopants through the underlying interface for applications such as passivating contacts where this is undesirable.

We remove 7 filaments from both ends of our filament array and include these as crossing filaments in between the parallel filaments for AFC. This increases the density of our filaments in the deposition area and still satisfies the tool current limit of 150 A. An illustration of NFC and AFC are shown in Figure 28(b).

5.2.2 Deposition temperature monitoring

Due to the position of the substrate in the chamber, monitoring the temperature using an optical pyrometer proves difficult due to the Infrared (IR) interference from the filaments or IR blocking from the backing plate. Hence, a custom-built temperature monitoring system was devised for measuring the deposition temperatures of interest, as depicted in Figure 29(a). A Type K thermocouple is used due to its temperature monitoring range (from -270 ^{o}C to 1260 ^{o}C), reliability and low cost. The AD8495 ARM chip is a thermocouple signal conditioner, acting as both a filter and amplifier to the relatively small signal generated from the thermocouple. Additionally, this allows the temperature of the reference junction to be known, satisfying the requirements for determining the temperature using the Seebeck effect. The output of the AD8495 signal conditioner is fed through a voltmeter where the measured voltage is converted to a temperature (with a precision of ± 1.1 ^{o}C). Ceramic beads are used to protect the exposed thermocouple from thermal stress, and the ceramic adhesive was used to create the hot junction (i.e. adhere the thermocouple tip to the dummy wafer).

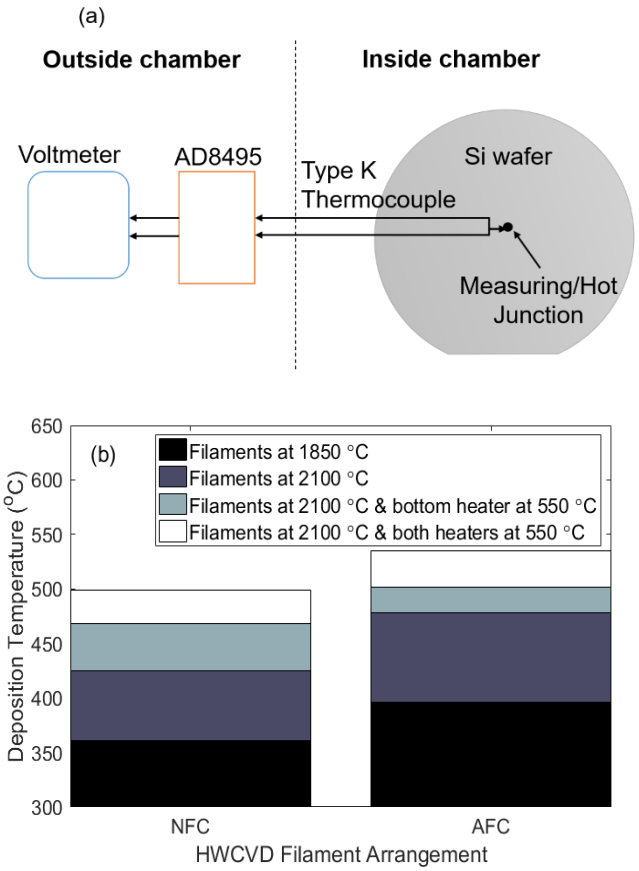

Figure 29: (a) Diagram of deposition temperature measurement set-up and (b) measured deposition temperatures under NFC and AFC.

The filament configurations of interest were tested with the filament temperature set to either 1850 ^{o}C or 2100 ^{o}C, with and without supplementary bottom and top heaters (both set at maximum temperatures of 550 ^{o}C). Generally, filaments are set at 1850 ^{o}C for amorphous silicon growth, and this is included for completeness. However, for crystalline silicon growth we are mainly interested in the upper limits of these temperatures and hence our primary focus is on the filament temperatures set at 2100 ^{o}C. Note that the maximum filament temperature is 2100 ^{o}C due to the current limit on the HWCVD tool. Table 3 summarises the measured HWCVD deposition parameters for NFC and AFC, with substrate deposition temperature measurements displayed in Figure 29(b).

Table 3: Measured HWCVD deposition parameters.

	Voltage (V)		**Current (A)**		**Bottom Heater**	**Top Heater**	**Pressure (x10^{-5} mBar)**		**Substrate temp. (^{O}C)**	
Filament temp. (^{O}C)	**NFC**	**AFC**	**NFC**	**AFC**			**NFC**	**AFC**	**NFC**	**AFC**
1850	25	30	90	98.5	OFF	OFF	0.9	6.3	361.3	396.2
2100	33	38	115	114.5	OFF	OFF	1.1	2.6	424.6	478.0
2100	33	38	115	114.5	ON	OFF	1.5	2.4	468.2	501.2
2100	33	38	115	114.7	ON	ON	1.1	2.6	498.5	534.8

As shown in Figure 29(b), an increase in deposition temperature is generated for all filament temperatures (and with heaters disabled/enabled) from NFC to AFC. This increase is between 7% and 13 %, depending on the filament temperature. An increase in the maximum deposition temperature to 535 ^{o}C from 498 ^{o}C is achieved using the altered filament configuration compared with the conventional configuration. The considerable increase in deposition temperature can aid the film quality by producing more uniform films with larger crystalline grains. However, we do not envisage the growth of monocrystalline silicon at such temperatures as we do not expect silicon epitaxy to be viable at temperatures below 600 ^{o}C based on findings in literature [57], [106].

5.3 Boron-doped silicon formation

5.3.1 HWCVD growth recipe

The growth of boron-doped silicon films using HWCVD is conducted as follows:

1. Clean float-zone (FZ) double-side polished, <100>, 280 μm thick 4" diameter n-type wafers in Fuming HNO_3, followed by immersion in 7:1 buffered HF solution for 30 s.
2. Load into HWCVD load-lock and pump down. Condition HWCVD chamber with H_2 at 300 sccm for 4 minutes.
3. Grow boron-doped silicon using SiH_4/B_2H_6 at a gas flow ratio of 10/10 sccm for 23 minutes.
4. Purge chamber with Ar at 200 sccm for 2 minutes. Unload wafer.

Immersion in buffered 7:1 HF solution is for native oxide etching and H_2 conditioning is aimed at cleaning the HWCVD chamber prior to deposition. A gas flow ratio of 10/10 sccm for SiH_4/B_2H_6 is used as when compared to 5/5 or 20/20, this produces the best film quality with no appearance of pinholes or blisters [29]. Microscope images taken from silicon film grown at 5/5 and 20/20 sccm gas flow ratios showing some of the bubble-like blistering are shown in Figure 30(a)-(c). A cross-sectional SEM image taken from a silicon film grown at a gas flow ratio of 20/20 sccm is also presented in Figure 30(d). We understand this to be due to the density of the film being poor under these gas flow ratios, and therefore causing the formation of blisters/pinholes when the film contracts during cool down after the deposition. Pinholes are detrimental for both emitter and passivating contact applications of this material as this would cause current shorting in these devices. Based on optical microscopy and SEM images, no pinholes or blisters were apparent under the 10/10 sccm gas flow ratio of SiH_4/B_2H_6.

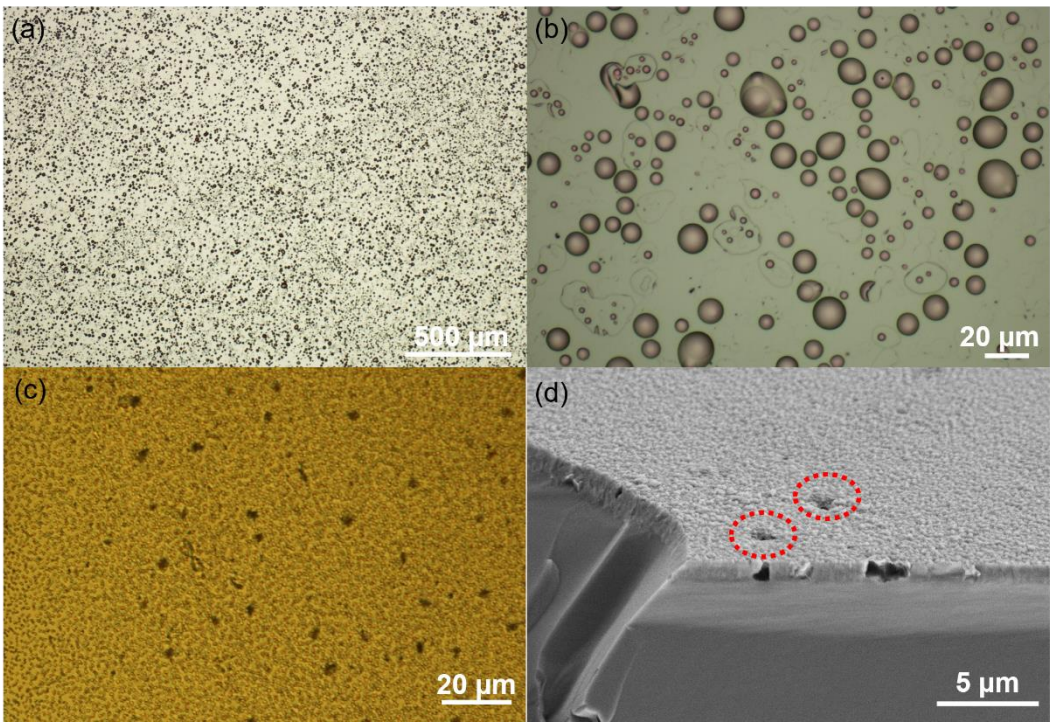

Figure 30: (a)-(c) Top-down microscope images taken from Si films grown using 5/5 and 20/20 sccm gas flow ratios and (d) cross-sectional SEM image of 20/20 sccm grown film.

5.3.2 Growth rate and thickness uniformity

A cross sectional SEM image of boron-doped silicon films using the 10/10 sccm recipe is shown in Figure 31(a). In addition, a spatial map of the thickness of silicon films after 23 minutes of growth, as measured via optical ellipsometry measurements, is presented in Figure 31(b). This was fitted to a model with 2 Tauc-Lorentz and 3 Gaussian oscillators. A mean square error (MSE) of 11.12 is achieved, indicating excellent agreement between the model and data.

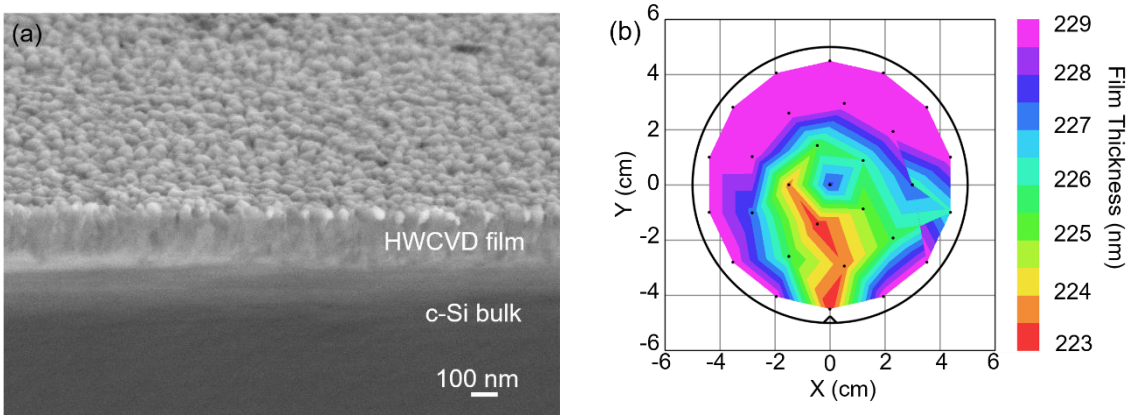

Figure 31: (a) Cross-sectional SEM image taken from boron-doped silicon film grown using 10/10 sccm gas flow ratio and (b) spatial thickness map taken from optical ellipsometry.

From the SEM image and ellipsometry thickness map in Figure 31(a) and 31(b), the average film thickness is determined to be 225.5 nm, equating to a deposition rate of 0.16 nm/s. Despite HWCVD being capable of deposition rates of up to 2-3 nm/s [126], a more controlled growth process was used here for achieving more uniform doping profiles and avoiding lattice dislocations or voids. A 2.7 % variation in film thickness can be determined from Figure 31(b), illustrating a good level of thickness uniformity across a 4" diameter wafer area. From Figure 31(a), the heterogeneity of the top surface suggests polycrystalline properties, but further morphological characterisation is required to confirm this.

5.3.3 Crystallinity of as-deposited films via Raman spectroscopy

Raman spectroscopy was used to determine the crystallinity of NFC and AFC deposited boron-doped silicon films. This was done using a 532 nm laser, targeting the deposited film and avoiding the bulk substrate. The Stokes Raman peaks (between 400 cm^{-1} and 600 cm^{-1}) for as-deposited boron-doped silicon films via NFC and AFC are shown in Figure 32(a) and 32(b) respectively.

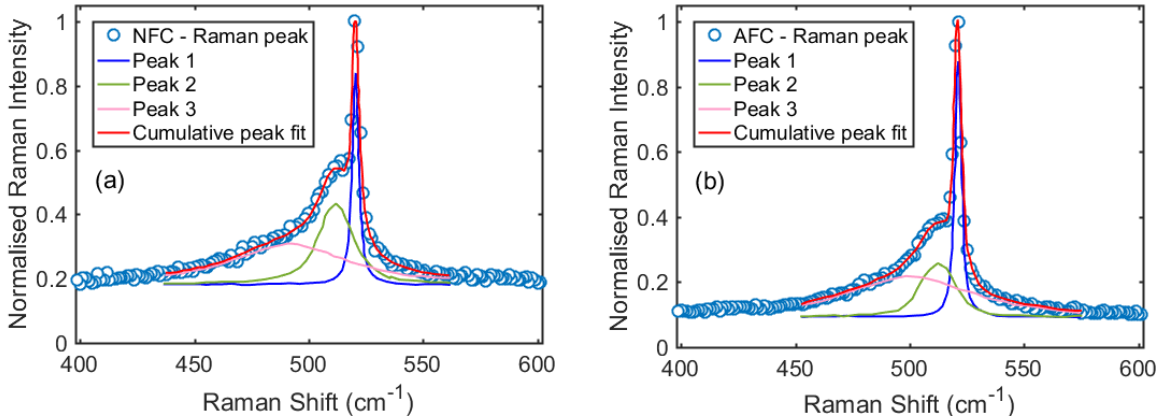

Figure 32: Stokes Raman spectra for as-deposited boron-doped Si films via (a) NFC and (b) AFC.

These are fitted using a Voigt function, which is the convolution of Lorentzian and Gaussian profile, defined as:

$$y = y0 + A\frac{2\ln(2)}{\pi^{3}/_{2}}\frac{WL}{WG^{2}}\int_{-\infty}^{\infty}\frac{e^{-T^{2}}}{(\sqrt{\ln(2)}\frac{WL}{WG})^{2}+(\sqrt{4\ln(2)}\frac{x-Xc}{WG}-t)^{2}}dt \quad (15)$$

Where y_0 is the offset, x is the Raman shift, X_C is the centroid position, A is the peak area and W_G and W_L are the Gaussian and Lorentzian full width at half maximum (FWHM) respectively. The convolution of the formula is:

$$y = y0 + (f1 * f2)(x) \quad (16)$$

where

$$f1(x) = \frac{2A}{\pi} \frac{WL}{4(x-Xc)^2 + WL^2} \quad (17)$$

And

$$f2(x) = \sqrt{\frac{4\ln(2)}{\pi}} \frac{e^{-\frac{4\ln(2)}{WG^2} * x^2}}{WG} \quad (18)$$

Hence, the function y = voigt(x, y_0, X_C, A, W_G, W_L) is defined to identify the individual peaks that have convolved as a broader peak in our Raman spectra results. The fitted peaks for the NFC and AFC Stokes Raman peaks are included in Figure 32(a) and 32(b) respectively, with the Voigt function parameters from these peaks shown in Table 4.

Table 4: Fitted Voigt function parameters for Raman spectra taken from HWCVD NFC and AFC grown films.

		Fitted Voigt function parameters				
		y_0	**X_C** (cm^{-1})	**A** (cm^{-1})	**W_G** (cm^{-1})	**W_L** (cm^{-1})
Peak 1	**NFC**	0.18 ± 0.02	520.63 ± 0.03	3.45 ± 0.34	0.99 ± 0.13	3.13 ± 0.54
	AFC	0.09 ± 0.01	520.78 ± 0.01	3.86 ± 0.21	1.65 ± 0.26	2.58 ± 0.27
Peak 2	**NFC**	0.18 ± 0.02	511.64 ± 0.43	6.54 ± 1.93	8.12 ± 1.78	13.78 ± 2.32
	AFC	0.09 ± 0.01	512.79 ± 0.52	3.71 ± 1.06	14.42 ± 2.05	6.85 ± 1.87
Peak 3	**NFC**	0.18 ± 0.02	491.59 ± 1.76	12.06 ± 2.22	1.76 ± 0.28	60.76 ± 7.55
	AFC	0.09 ± 0.01	498.79 ± 2.03	12.12 ± 3.05	1.85 ± 0.27	56.31 ± 6.28

Based on findings in literature, we expect to see a peak at 520 cm^{-1} for crystalline silicon (c-Si), 512 cm^{-1} for micro-crystalline (μc-Si) and 480 cm^{-1} for amorphous silicon (a-Si) [111], [112]. Both the NFC and AFC as-deposited films display a broad peak which extends across the 480 – 520 cm^{-1} Raman shift range. The shoulder-like peak present at ~512 cm^{-1} is evidence that both films possess micro-crystalline properties, with the sharp c-Si peak originating from the underlying substrate. Nonetheless, the right shift of peak 2 from 511.6 cm^{-1} to 512.8 cm^{-1} from NFC to AFC can be translated as the detection of larger crystals, as we transition from nanocrystalline to microcrystalline silicon [112].

The shoulder-like peak is seen to extend across the amorphous silicon range in both cases, meaning a-Si is detected for both NFC and AFC. However, when peak 3 (a-Si) for NFC and AFC are compared, the lower relative peak area (A) and right shift of this peak (X_C) indicate some level of improvement in crystal structure from the higher temperature configuration. Despite this, a post deposition anneal is evidently still required to re-crystallise the amorphous regions detected despite some improvement from the in-situ annealing of AFC. An optimisation of the post-deposition anneal is required as the 1 hour at 1000 ^{o}C from previous studies [29] for NFC ought not be required for AFC.

5.4 Optimisation of post-deposition anneal process

As the Raman spectra suggested that as-deposited AFC films were not completely crystalline, with evidence of the presence of some amorphous content, a post-deposition anneal for the re-crystallisation of boron-doped silicon films grown via HWCVD was developed.

5.4.1 Re-crystallisation

A rapid thermal anneal (RTA) process to treat the polycrystalline silicon films grown via HWCVD was developed. This study consists of using a temperature range of 800 – 950 ^{o}C and annealing times of 2, 15 and 30 minutes. Raman spectra of boron-doped films annealed for 2 minutes, 15 minutes and 30 minutes are shown in 33(a)-(c) respectively.

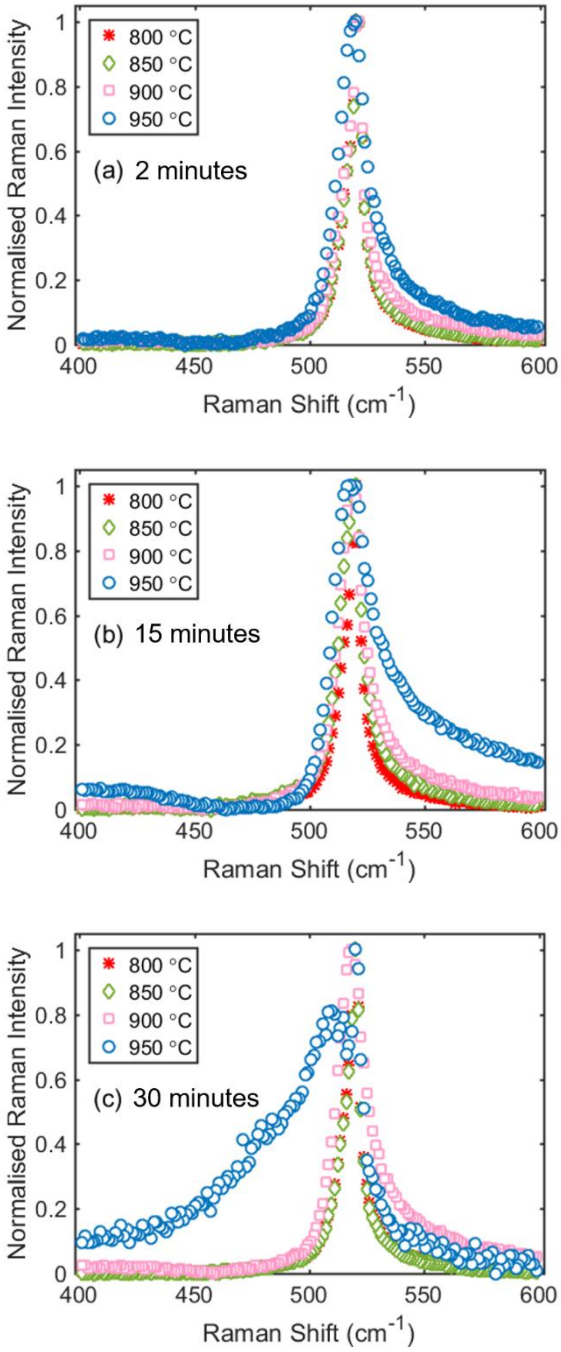

Figure 33: Raman spectra taken from boron-doped Si films after annealing at 800-950 ºC for (a) 2 minutes, (b) 15 minutes and (c) 30 minutes.

From Figure 33(a), it is clear that annealing for 2 minutes at all temperatures between 800 – 950 ºC eradicates the a:Si and µc-Si shoulder in the Raman spectra. A sharper peak at 520 cm^{-1} is seen, which suggests that the annealing for 2 minutes has crystallised all amorphous content. In fact, this is true for all the Raman peaks (apart from 950 ºC for 30 minutes in Figure 33(c)), as the shoulder peak ranging from 480 – 512 cm^{-1} is now non-apparent.

In Figures 33(a)-(c), the Raman peak located at 520 cm^{-1} for all cases widens with higher temperatures of annealing at each given duration, essentially becoming less sharp. This widening of the peaks indicates a poorer quality film, with grain sizes having some variation despite being large enough to be considered crystalline silicon. A very sharp peak at 520 cm^{-1} is highly desirable and tends to indicate a high-quality film in terms of uniformity. In addition, in Figures 33(a)-(c) an asymmetrical tailing effect can be seen with the Raman peaks, with a progressively increasing tailing-off on the right side of the peak being apparent as the anneal temperature is increased. This is due to a Fano-type resonance which occurs between the electron states and phonon states in cases of highly doped films ($>10^{17}$ cm^{-3}) [111]. This occurs as the dopants are driven through the interface and into the bulk layer due to the film being processed at such high temperatures and hence can be seen in Raman spectra as a tailing off on the right side due to the type of doping (p-type). This asymmetric tailing off would be seen on the left side if the film was n-type. Based on these results, it can be said that annealing at 800 ^{o}C for 2 minutes seems to suffice for the ex-situ crystallisation process. Not only does this give the lowest thermal budget, the film quality seems to also be the optimal amongst the annealing temperatures and durations tested.

5.4.2 Topographical characterisation

Atomic force microscopy (AFM) is used to scan the top surface of the as-deposited and annealed boron-doped silicon films. Figure 34(a) and (b) show a 3D-formatted scan across a 2 µm × 2 µm area of the as-deposited film and the film after a 2 minute anneal at 800 ^{o}C. The average surface roughness, R_q, was 3.9 nm and 3.7 nm for the as-deposited and annealed NFC film respectively, demonstrating a similarity between the morphology of these surfaces. The similarity in roughness and grain size between the as-deposited and annealed films would suggest there is little change in surface morphology despite the Raman study shown in Figure 33(a) showing significantly improved crystallinity. This would suggest that during the annealing process, crystallisation, which starts from the interface with the substrate, has not fully proceeded to the surface. This would explain the discrepancy between the Raman measurement, which considers the bulk of the film, and AFM which is focused only on the surface.

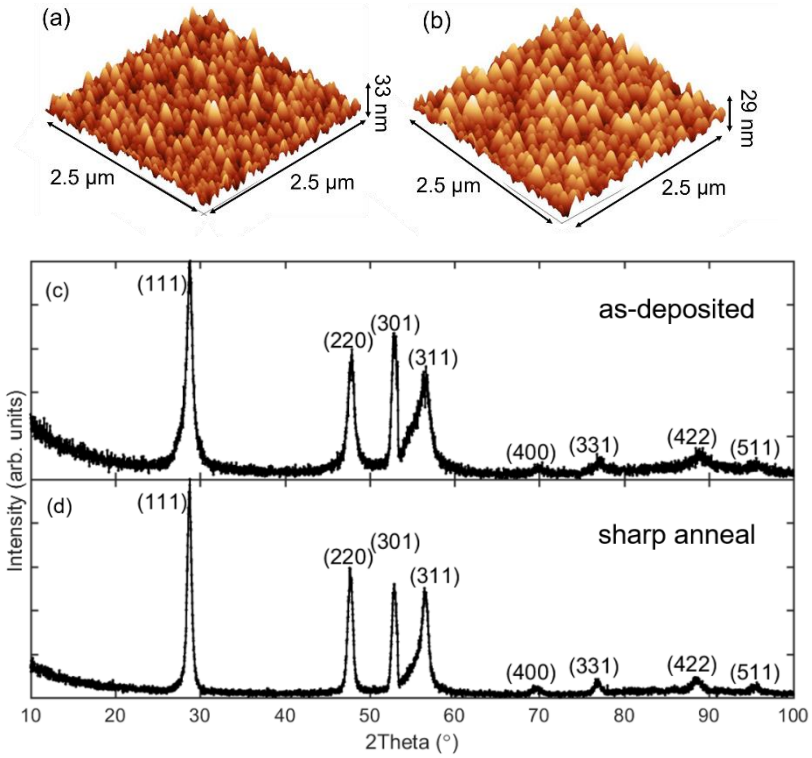

Figure 34: 3D-formatted AFM scan of (a) as-deposited and (b) heat-treated HWCVD films. (c) XRD spectra for as-deposited and heat-treated Si films.

Grazing incidence X-ray diffraction (XRD) scans at a low X-ray grazing angle of 1^{o} are employed to examine the as-deposited and 2 minutes anneal at 800 ^{o}C films. The XRD patterns for the as-deposited and heat-treated films are shown in Figure 34(c). The peaks associated with the different crystal orientations of silicon are identified. Both films display a similar peak pattern representing polycrystalline properties [127], [128]. A single peak at 69 ^{o} (<400>) would be expected if the film was monocrystalline (i.e. silicon epitaxy). The dominance of the <111> peak is evident for both films and is indicative of the presence of polycrystalline silicon.

5.4.3 Transmission electron microscopy imaging

Transmission electron microscopy (TEM) is used to characterise the morphological structure at the interface and the longitudinal variation in crystallinity pre and post annealing. Figures 35(a)-(b) and 35(c)-(d) show TEM images of the as-deposited and annealed boron-doped silicon films respectively. A platinum protective layer was deposited on our films prior to imaging, as seen in Figure 35(a). Thicknesses and growth rates agree with SEM and ellipsometry from Figure 31, with no considerable difference noticed in thickness post annealing for 2 minutes at 800 ^{o}C from these images.

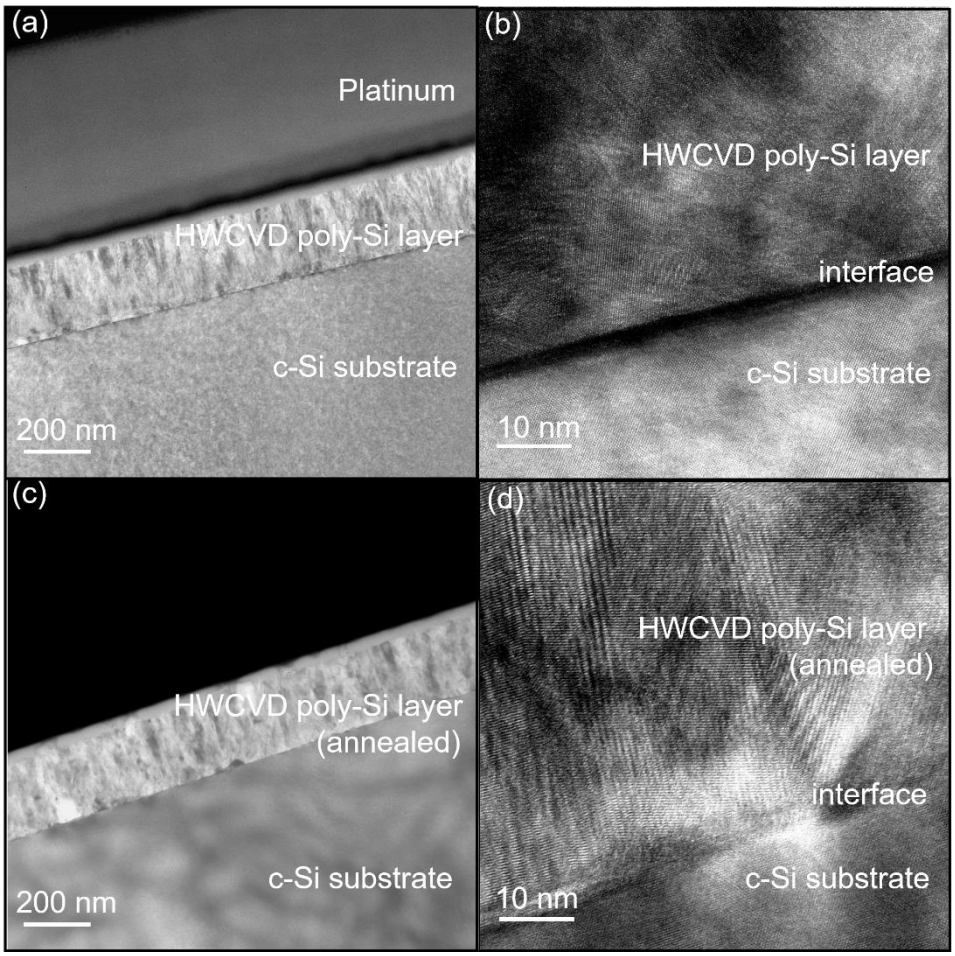

Figure 35:TEM images of (a)-(b) as-deposited and (c)-(d) heat-treated HWCVD boron-doped Si films.

From Figure 35(b) and 35(d), the grains present on both films show crystalline properties, with uniformity in atomic plane orientation in certain regions. The heterogeneity of the grains suggests polycrystalline properties. In fact, a distinct difference between the as-deposited and annealed films and the underlying monocrystalline substrate is evident in both Figure 35(a) and 35(c). Nonetheless, smaller grains can be deduced from Figure 35(b) in the deposited silicon film in comparison to the relatively larger grains visible in Figure 35(d) in the annealed case, illustrating that the annealing step has favourably crystallised the film further.

The interface between the deposited silicon and bulk substrate in the as-deposited case, as shown in Figure 35(b), illustrates void-like features with minimal evidence of lattice matching between the bulk and the deposited silicon. On the other hand, the interface of the annealed sample in Figure 35(d) appears significantly more uniform, with matching regions between the atomic plane orientation of the silicon atoms from the bulk (<100>) directly to the polycrystalline silicon layer. The heterogeneities in the interface could introduce defects that

would be detrimental to the transport of charge carriers through this p-n junction. The reduction in voids and enhancement in lattice matching suggests an enhancement in interfacial quality from the short post-deposition anneal. This would translate to an improvement in the overall carrier transport efficiency when used as an emitter or conductive layer in a solar cell [32], [57], [106].

5.4.4 Selective area electron diffraction

Selective-area electron diffraction (SAED) is used for examining the crystal structure in different regions of the structures from Figure 35. The diffraction patterns taken from the as-deposited and heat-treated samples are shown in Figures 36(a)-(c) and Figures 36(d)-(f) respectively.

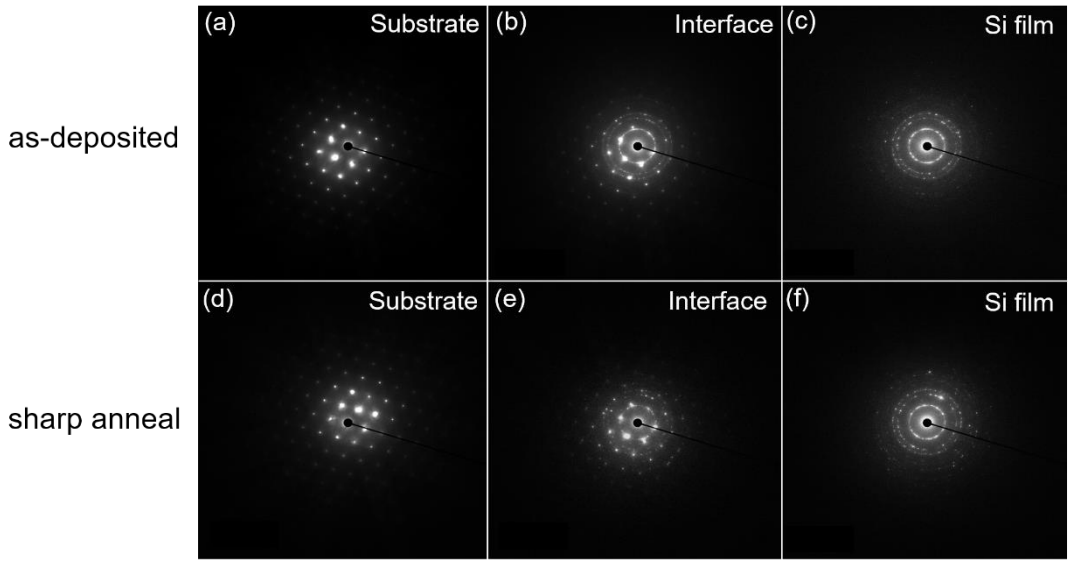

Figure 36: SAED diffraction pattern for as-deposited HWCVD samples taken at (a) c-Si substrate, (b) interface and (c) grown film. SAED pattern for heat-treated HWCVD samples taken at (d) c-Si substrate, (e) interface and (f) heat-treated film.

Using this technique, the resulting diffraction patterns are either spot patterns that correspond to single-crystal diffraction or ring patterns corresponding to diffraction from multiple crystals [129]. In cases where amorphous silicon is present, the ring patterns overlap to form an annulus. The bulk substrate of both samples in Figure 36(a) and Figure 36(d) appears as spot patterns, suggesting monocrystalline properties, as expected from the FZ wafers used in this work. The diffraction pattern of the interface region in both cases in Figure 36(b) and Figure 36(e) show concentric rings as well as spot patterns, indicating the transition from monocrystalline to polycrystalline from substrate into the film. Nonetheless, it is evident that the ring patterns are visibly less dominant in the interface of the annealed case in comparison to the as-deposited

interface region. This supports the enhancement in lattice alignment seen in the interface region of the annealed sample in the TEM image in Figure 35(d), as a stronger dominance from the <100> plane in this region translates as clearer spots rather than ring patterns. Figure 36(c) and Figure 36(f) show the diffraction pattern taken from the deposited silicon layer of the as-deposited and annealed structures, respectively. The clear ring patterns are supportive of this film being polycrystalline in both cases. The lack of a clear spot pattern suggests there is no dominant plane orientation present in this film.

5.5 P^+ doping evaluation

Identifying the doping concentration profile of the boron-doped HWCVD films that are grown on silicon substrates is important when evaluating their suitability for emitter or contacting applications. The effect of the doping levels on the electrical properties of an emitter, such as sheet resistance and saturation current, can play a critical role in the overall performance of such solar cells. A comparison between the as-deposited and heat-treated specimens is also of interest.

5.5.1 Dopant levels and diffusion

Secondary ion-mass spectrometry (SIMS) is used to measure the boron doping profile of the HWCVD polycrystalline silicon films. SIMS is conducted using an IONTOF ToF-SIMS 5 instrument with silicon and boron ions detected during milling. A relative sensitivity factor (RSF) was applied to the raw counts data to convert to boron concentration, with the RSF being measured and calibrated for boron in silicon. Figure 37 shows the doping profile of the as-deposited and heat-treated films as a function of depth.

Both films show a degree of uniformity in doping within their bulk, to the order of 10^{21} cm^{-3} boron concentration. A rapid decay of dopant concentration towards the interface region is observed for the annealed case. This is due to the dopants being driven through the interface and into the bulk, as observed from the presence of boron dopants up to 600 nm beyond the junction (as shown in inset in Figure 37) for the heat-treated sample. This is not the case with the as-deposited sample as the concentration of boron dopants remains high up to the interface in the SIMS profile and decays very abruptly. The high level of doping ($>10^{18}$ cm^{-3}) and the diffusion of dopants through the interface into the bulk region supports the Fano-type resonant interaction observed in the Raman results presented in Figure 33. The high doping concentration is useful for increasing conductance in this region that in turn can be utilized for

polysilicon passivating contacts in silicon solar cells, where high conductivity and a low minority carrier recombination velocity are of primary interest. A high fixed charge density is useful for modulating the carrier concentration at the silicon surface. There is, however, a trade off with the increased Auger recombination in these films from the higher concentration of dopants.

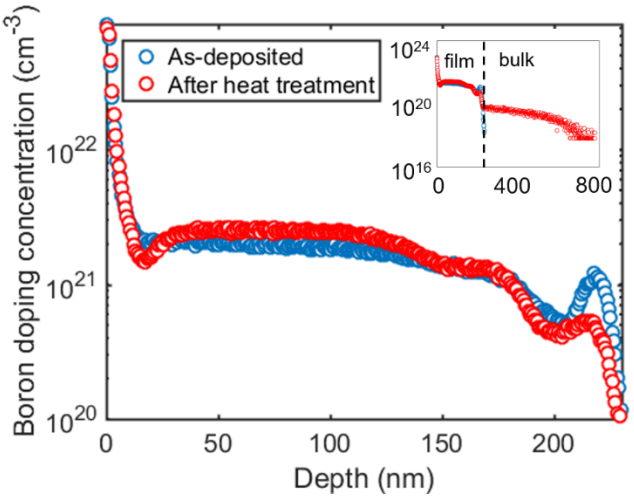

Figure 37: Boron doping as a function of depth for as-deposited and heat-treated films taken from secondary ion-mass spectrometry.

The kink observed in the 205-210 nm region for both films can be due to the adsorption of dopants to the walls of the HWCVD chamber during the initial growth period. Once the chamber is saturated, the doping concentration stabilises. One potential way of eliminating this effect could be to saturate the chamber with B_2H_6 prior to SiH_4 flow. In addition, a sharp increase in boron dopants (exceeding 10^{22} cm^{-3}) can be observed in the top 10 nm of the film. Likewise, a rapid decrease in the raw counts data for silicon is observed at the same top region of the film. This occurs at the latter stages of the deposition process when the SiH_4 and B_2H_6 flow has been terminated, but deposition continues for a short period of time as the walls start desorbing boron dopants. This region could be easily etched off before use in a contact.

5.5.2 Saturation current and collection efficiency

We use a freely available online emitter simulator called EDNA 2 (PV Lighthouse) [118], [120] to understand the implications of the measured doping profiles on the quality as an emitter or back-surface field region in a typical solar cell. EDNA 2 can calculate the recombination in heavily doped regions of silicon, which will also allow us to determine the emitter saturation current density for the HWCVD grown p-n junctions. For these simulations, the doping profiles

were used to create a basic model (based on the profile shape), which was then uploaded to EDNA 2. Table 5 shows the EDNA 2 simulation results using the as-deposited and heated treated HWCVD p^+ doping profiles. In Table 5, the sheet resistance (ρ_{sq}), dark saturation current density (J_{0E}) and internal quantum efficiency (IQE) for such emitters are presented.

Table 5: HWCVD silicon emitter electrical properties taken from EDNA 2 simulation results using p^+ doping profiles.

	EDNA 2 outputs		
	ρ_{sq} (Ω/sq)	**J_{0E} (fA/cm^2)**	**IQE_E (%)**
As-deposited emitter	16.4	310.5	42
Heat-treated emitter	7.5	1430	22

A ρ_{sq} of 7.5 Ω/sq from 16.4 Ω/sq after annealing our boron-doped silicon films for 2 minutes at 800 ^oC can be seen from Table 5. This is due to the diffusion of the dopants beyond the interface after annealing, with the gradual decrease in dopant concentration through the interface being favourable towards reducing the series resistance in this region. However, a considerably larger emitter dark saturation current density (J_{0E}**)** of 1430 fA/cm^2 from 310.5 fA/cm^2 after annealing is also determined. It is important to note that these values are the absolute minimum that they would be experimentally as other imperfections have been disregarded in the EDNA 2 simulations. J_{0E} signifies the generation-recombination current in equilibrium, which is why it is sometimes referred to as the thermal (or equilibrium) recombination current. This is unfavourable towards the electrical performance of such devices as this translates as a leakage current in the emitter. A breakdown of the recombination mechanisms contributing to J_{0E} for both the as-deposited and annealed emitters is shown in Figures 38(a) and (b) respectively. Both are highly dominated by Auger recombination, with over 75 % of J_{0E} being attributed to this recombination mechanism. This is caused by the high doping concentration (10^{21} cm^{-3} peak boron concentration from Figure 37) of our p^+ emitters. In this case, higher Auger recombination is the cost for gaining a higher conductivity after annealing and for improvements in the morphological structure of these emitters.

The emitter collection efficiency (IQE_E) from Table 5 is the percentage of generated carriers that are collected, based on the EDNA 2 simulations. A drop from 42 % to 22 % is seen after heat-treatment, showing an overall drop in device performance due to dopant diffusion beyond the interface. A diffused junction deeper in the bulk is seen to be less favourable for the collection efficiency of photogenerated carriers. A breakdown of the recombination

mechanisms that limit the IQE_E of the as-deposited and annealed emitters are shown in Figures 38(c) and (d) respectively. As with the dark simulations, the dominant loss in both cases is seen to be from Auger recombination. The higher radiative recombination in the as-deposited emitter is due to the higher peak concentration in the doping profile of this specimen. No considerable difference is seen in the Shockley-Read-Hall recombination from both doping profiles, with both being negligible from the EDNA 2 simulations.

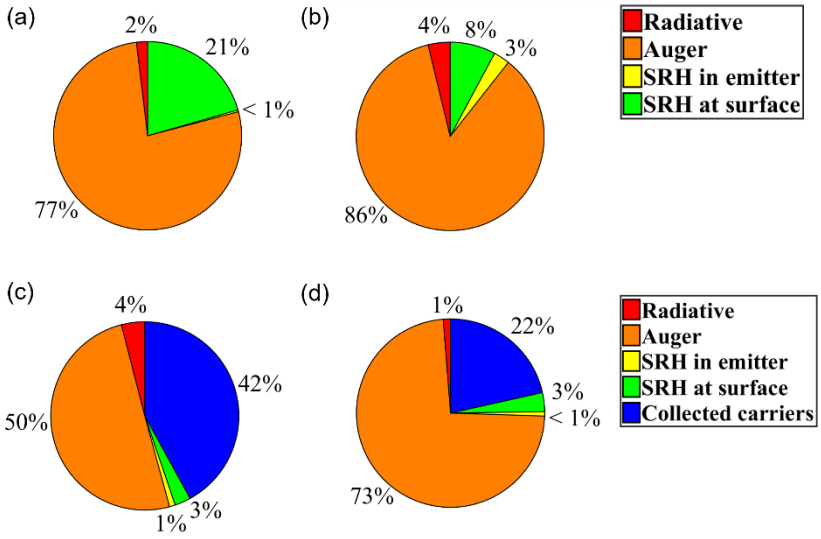

Figure 38: A breakdown of the contributing recombination mechanisms to J_{0E} for (a) as-deposited and (b) annealed HWCVD Si emitters. Similar breakdown for limitations to IQE_E for (c) as-deposited and (d) heat-treated emitters. Taken from EDNA 2 simulation results.

Understanding the significance of J_{0E} and ρ_{sq} to the overall silicon solar cell performance will aid our investigation as these parameters can play an important role when optimising such devices. We now use computational modelling to simulate the performance of an IBC silicon solar cell based on our parameters of choice, which in this case are emitter J_{0E} and ρ_{sq}.

5.5.3 Emitter implications on cell performance

Quokka is used to define an IBC silicon solar cell using the experimental parameters taken from the 24.4 % PCE IBC cell made in Australian National University [33]. These include the cell design, optics, passivation and electrical properties which can be found in Table 6.

Table 6: Input parameters for IBC model in Quokka, taken from IBC cell in [33].

Parameter	Value
Unit cell dimensions	(x) 250µm (y) 35µm (z) 230µm
Rear diffused geometrics	Large area p^+ diffusion, 165µm (Emitter) Local n^+ diffusion, 15µm (BSF)

Rear metal grid geometrics	Contact openings = 3.1µm x 3.1µm, 70µm pitch Number of contacts (unit cell) = 1.5 (emitter region) 0.5 (BSF region)
Front dielectrics	Inner film – 73nm PECVD SiN_x Outer film – 84nm PECVD SiO_2 Random pyramids (53^o characteristic angle) Carrier generation taken from OPAL 2 [117].
Bulk	n-type 1.5 Ωcm resistivity $\tau_p = \tau_n$ = 3ms
P^+ diffusion	166 Ω sheet resistance J_o = 33.2 fA/cm^2 (passivated) 1234 fA/cm^2 (contacted) Collection efficiency = 1
N^+ diffusion	35 Ω sheet resistance J_o = 176 fA/cm^2 (passivated) 202 fA/cm^2 (contacted) Collection efficiency = 0.87 (uniform generation)
Front passivation	J_o = 4.6 fA/cm^2
Rear passivation	J_o = 19.5 fA/cm^2
Series resistance	R_S = 0.051 Ωcm^2
Shunt resistance	R_S = 100 kΩcm^2

The unit cell described in Table 6 and extracted from the Quokka model is shown in Figure 39(a), where the green regions are n^+ diffused (BSF and front passivation) and the blue region is the p^+ emitter. Prior to making any changes or adjustments to the IBC model, it is important that the simulated model resembles the structure and model of the experimental cell to a satisfactory degree. Table 7 shows the J_{SC}, V_{OC}, FF and PCE from our IBC model in Quokka, as well as the simulated Quokka model by Fell et al. [71] and the experimental results from ANU [33]. Despite the 0.1 mV and 0.3 % difference in V_{OC} and FF between our Quokka model and Fell et al. model, the level of similarity between these can be said to be satisfactory. Hence, we will use this Quokka model as a core structure for modelling our IBC solar cell device characteristics.

Table 7: Simulated and measured IBC solar cell results using Quokka, comparing to Fell et al and ANU IBC [33], [71].

IBC Cell	**J_{SC} (mA/cm^2)**	**V_{OC} (mV)**	**FF (%)**	**PCE (%)**
Our Quokka simulated cell	42.2	704	82.8	24.7
Fell et al. simulated cell [71]	42.2	705	83.1	24.7
ANU – measured cell [33]	42.0	703	82.7	24.4

As our interest lies in emitter/bulk junction quality, the simulations focus on this region of the IBC device. The effect of the recombination parameter, J_{0E}, from the passivated p+ emitter region is studied using this model. J_{0E} is one possible conceptualisation to represent the recombination between electrons and holes, alternative to the material recombination parameter, minority carrier lifetime (τ) [130]. Based on our hypothesis and supporting literature, we assume that a poor junction results in a high J_{0E} value (> 200 fA/cm^2), due to the inhomogeneity of the junction and poor passivation qualities. A sweep of the emitter J_{0E} between 1 – 5000 fA/cm^2 was run using Quokka. Figure 39(b) shows the resulting fill factor and power conversion efficiency at these J_{0E} values.

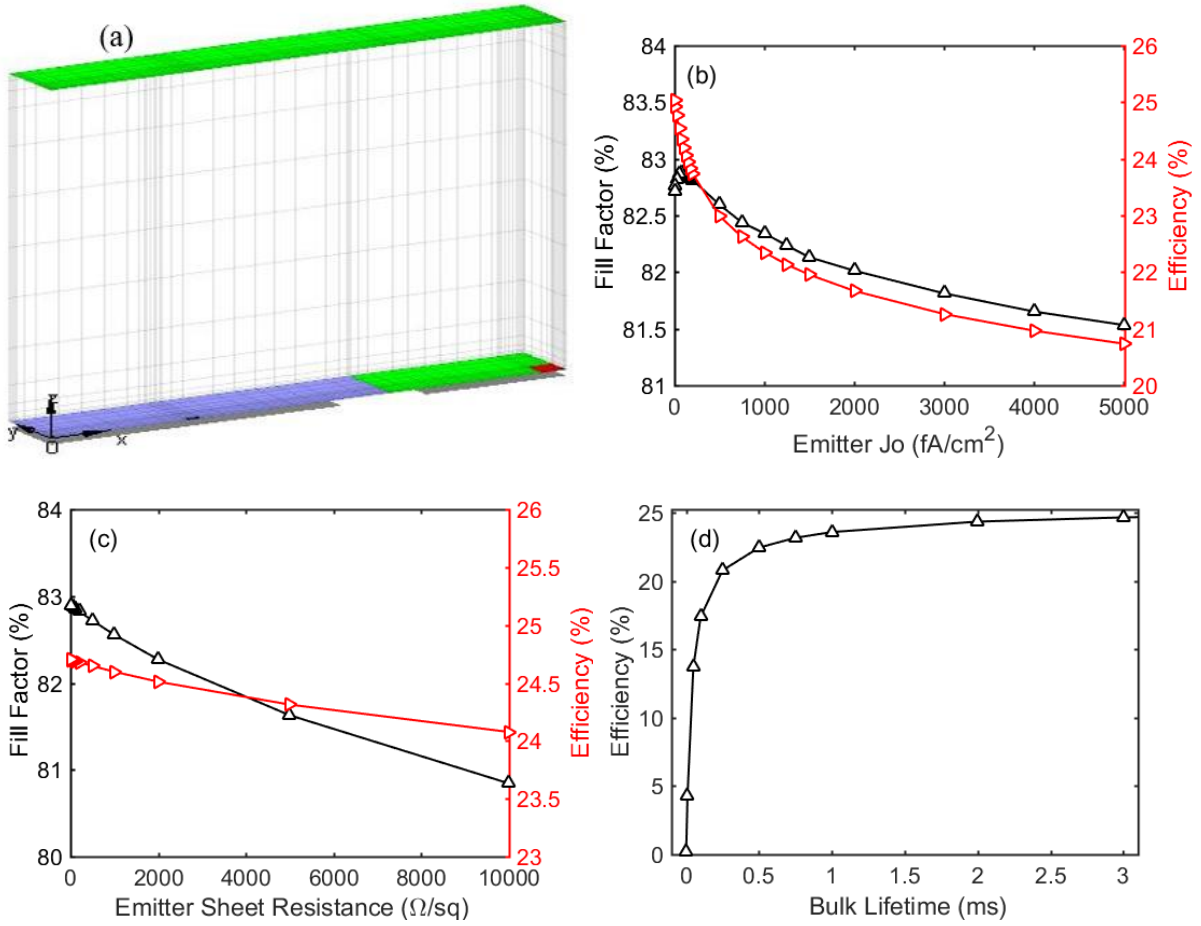

Figure 39: (a) IBC unit cell from Quokka model, with Quokka IBC simulation results used for quantitative analysis of (b) emitter J_0, (c) emitter sheet resistance and (d) bulk lifetime on IBC performance .

From Figure 39(b), a considerable difference of 4.3 % in power conversion efficiency is seen across the J_{0E} data range (1 – 5000 fA/cm^2). This is attributed to a 16 % decrease in the open circuit voltage, indicating the importance of J_{0E} on the cell performance. A drop in open circuit

voltage in return drops the overall collection efficiency. No considerable drop in fill factor is seen, with only 2 % drop across our J_{0E} data range. It is evident that a J_{0E} < 500 fA/cm^2 is required to reach a cell PCE > 23%, and J_0 < 200 fA/cm^2 to exceed 24 %. In fact, our simulation results show that if the J_{0E} value of the ANU cell (33.2 fA/cm^2) [33] can be reduced to 10 fA/cm^2, the overall power conversion efficiency of this IBC solar cell can be boosted by 0.7 %. These levels of improvement are considerably large when considering the Shockley-Queisser limit of single junction silicon solar cells being 29.4 % [18], hence re-emphasising the importance of J_{0E} on device performance.

The emitter sheet resistance was also swept using our Quokka model to measure the effect of our ρ_{sq} results on IBC cell performance. This was done between 1 Ω - 10 kΩ and the resulting fill factor and efficiency of the IBC cell are shown in Figure 39(c). This shows that neither of these parameters change by a considerable margin. A total drop of 2.05 % and 0.63 % in the fill factor and efficiency of the IBC cell is seen respectively across the 1 Ω to 10 kΩ range. Furthermore, we see from our simulations that the V_{OC} only drops by 300 µV and J_{SC} only changes by 20 µA/cm^2 across the data range. This is seen as relatively negligible considering the unrealistic value for ρ_{sq} of 10 kΩ taken into consideration. Hence, no considerable difference is seen in the overall IBC cell performance between our as-deposited and heated treated ρ_{sq} values from Table 5. This is mainly due to the relatively small thickness of this layer in the IBC cell with respect to the rest of the device.

As well as J_{0E} and ρ_{sq}, we pay some attention to the bulk lifetime (τ_{bulk}) of this cell architecture. This is because τ_{bulk} is crucial for the IBC solar cell architecture due to the rear junction properties in this design. As the generated carriers at the top region of the solar cell require a relatively long diffusion length to the rear collectors, τ_{bulk} dictates the quality of this type of solar cell. Furthermore, the next section on the effects of thermal processing on the bulk lifetime of FZ wafers from HWCVD will also signify the importance of this further. Hence, using the Quokka IBC model, the effect of a range of τ_{bulk} between 1 µs – 15 ms on the IBC performance is simulated. As the same trend was seen in all the performance metrics, Figure 39(d) only shows the power conversion efficiency of the IBC from the τ_{bulk} sweep. This is shown only up to 3 ms despite the sweep being up to 15 ms, as the region of significant change lies within this region and a plateau is seen beyond 3 ms.

An exponential decay of the overall cell efficiency is seen with a drop of τ_{bulk} from 3 ms. More significant losses are seen when the lifetime is reduced below 0.5 ms, with the occurrence of

more detrimental effects on the IBC performance. For example, a significant drop of 1.9 % in cell efficiency is seen from 0.5 ms to 0.25 ms, showing the importance of maintaining τ_{bulk} in the millisecond range. Furthermore, from these results we can see that $\tau_{bulk} > 1$ms is required to exceed cell efficiencies of 23 %. This will prove further significant when the effects of thermal processing on the bulk lifetime of FZ wafers will be discussed.

5.6Surface passivation

Silicon surface passivation is crucial for maintaining a high carrier collection efficiency. The semi-continuum of forbidden energy states that arise at such surfaces is detrimental to device performance and therefore must be saturated. Generally, dielectric materials are used for silicon surface passivation. Amongst these, aluminium oxide (AlO_x) offers great potential due its high negative fixed charges ($10^{12} – 10^{13}$ cm^{-2}) that are activated upon annealing and low density of interface states [131]. This material offers great surface passivation for both p-type and n-type silicon, with a typical thickness of 15 nm being sufficient [131], [132]. We study the use of AlO_x grown via plasma enhanced atomic layer deposition (PE-ALD) for passivating our p-type HWCVD silicon films and n-type substrates.

5.6.1 Passivation of p-type and n-type silicon using AlO_X

Prior to passivating the surface of our HWCVD grown films, it is useful to quantify the passivation quality of this material on n-type bare silicon substrates. We grow 15 nm aluminium oxide films using PE-ALD as follows:

1. Load wafer into ALD load-lock and pump down.
2. Heat chamber at 150 ^oC and load wafer into chamber.
3. O_2 treatment with 60 sccm O_2 and 300 W RF plasma for 30 s.
4. Cyclic AlO_x growth:
   - **(a)** Trimethylaluminum (TMA) dose with 60 sccm O_2 carrier for 20 ms.
   - **(b)** TMA purge with 60 sccm O_2 for 3 s.
   - **(c)** Plasma assisted O_2 dose with 60 sccm O_2 + 300 W RF plasma for 3 s.
   - **(d)** O_2 purge with 60 sccm O_2 for 1 s.

A post-deposition anneal is required to improve the chemical passivation, with some improvements in the charge density. Generally, annealing at temperatures between 400 – 425 ^oC is conducted for AlO_x [132]. We examine the effect of annealing duration at 400 ^oC using a

rapid thermal anneal process on the effective lifetime, τ_{eff}, of the substrates. τ_{eff} is measured using a Quasi steady-state photoconductance (QSSPC) decay method for this study. Figure 40(a) and 40(b) show τ_{eff} against the minority carrier density for annealing durations of 0 – 60 minutes for p-type and n-type silicon substrates, respectively. Improvements in τ_{eff} are seen with increasing the annealing duration up to 30 minutes for both cases. Furthermore, a substantial drop in τ_{eff} is also evident beyond 30 minutes annealing duration for both n-type and p-type silicon respectively. We compare τ_{eff} at a minority carrier density of 10^{15} cm^{-3}, as shown in Figure 40(c) and 40(d) for p-type and n-type silicon respectively. This is generally the absolute value used when comparing τ_{eff} in literature, as it signifies the typical injection level expected based on the doping concentration of our substrates.

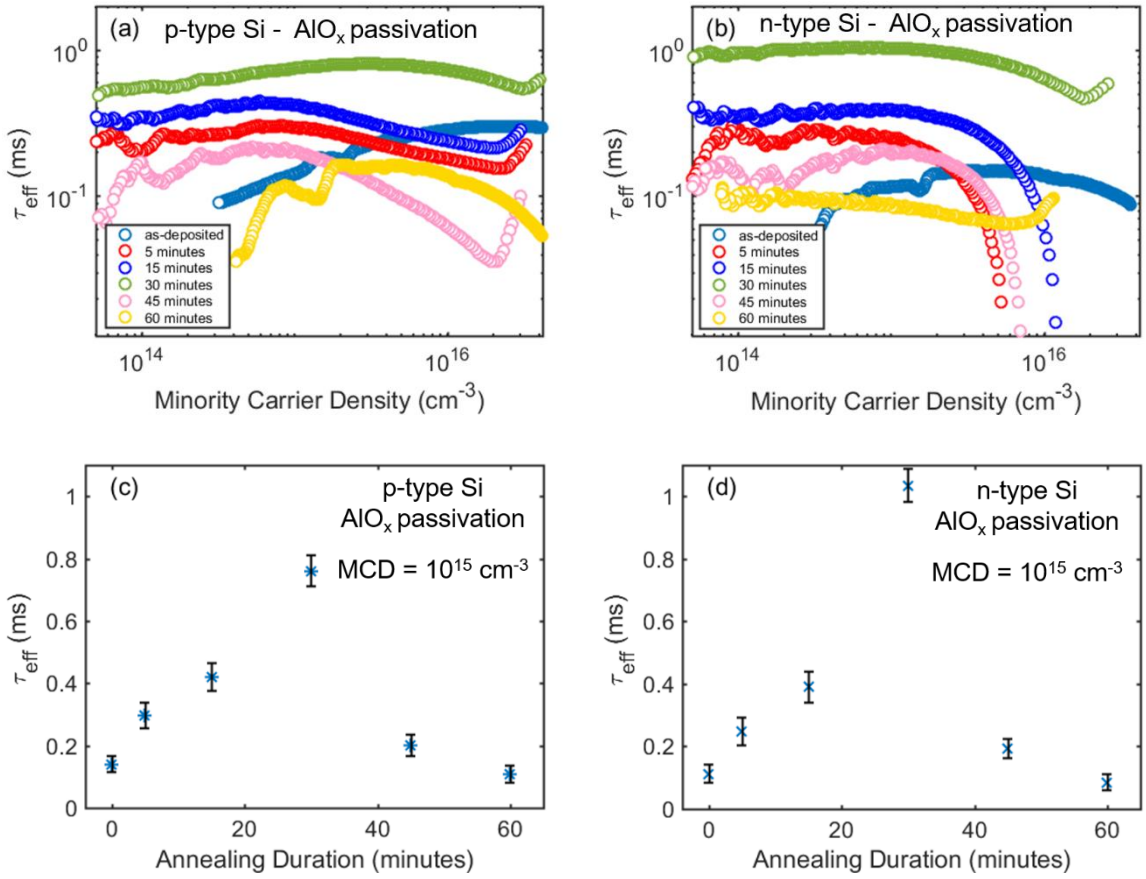

Figure 40: Effective minority carrier lifetime vs. carrier density measured for AlO_x passivated (a) p-type Si and (b) n-type Si, and effective minority carrier lifetime vs. annealing duration for (c) p-type Si and (d) n-type Si.

As visualised from Figure 40(c) and 40(d), the highest τ_{eff} is determined at an annealing duration of 30 minutes for both p-type and n-type silicon. A considerably higher absolute value for τ_{eff} of 1.03 ms is determined for n-type silicon than 0.76 ms for p-type silicon. This could be due to the field-effect passivation from the fixed negative charges being more effective for

n-type surfaces. Nonetheless, absolute τ_{eff} values at annealing durations below and beyond 30 minutes for p-type and n-type silicon are comparable. Up to 30 minutes, using a longer annealing duration effectively enhances the AlO_x/Si interface and boosts the density of fixed negative charges in the AlO_x layer. However, a rapid drop in τ_{eff} beyond 30 minutes is seen. Based on these results and our understanding from literature, a post-deposition anneal at 400 ^oC for 30 minutes of our AlO_x passivation layers will be conducted. This process will be used for both p-type HWCVD films and n-type substrates, based on the satisfactory τ_{eff} values determined from this study.

5.6.2 De-activation of intrinsic defects in FZ substrates

Before approaching the passivation of our structures, it is imperative to consider the effects of thermal processing on FZ silicon wafers on τ_{bulk}. As discussed in chapter 2, the activation of the passive intrinsic defects can occur when FZ substrates are processed in temperatures between 450 – 700 ^oC [44]. As our film deposition in the HWCVD chamber occurs within this temperature range, it is crucial for the overall device performance that this issue is addressed. To permanently recover the bulk lifetime in these wafers, i.e. permanently annihilate the intrinsic defects, Grant et al. [44] showed that an oxidation step at >1000 ^oC can be used. In order to validate this, a pre-oxidised (dry oxidation for 30 minutes at 1000 ^oC) wafer and non-oxidised wafer are passivated with AlO_x, followed by thermal treatment in a tube furnace for 10 minutes at 500 ^oC. The τ_{eff} is then measured using a QSSPC decay method in order to compare the effect of the pre-oxidation step. Figure 41 shows τ_{eff} versus the minority carrier density for the pre-oxidised and non-oxidised FZ substrates.

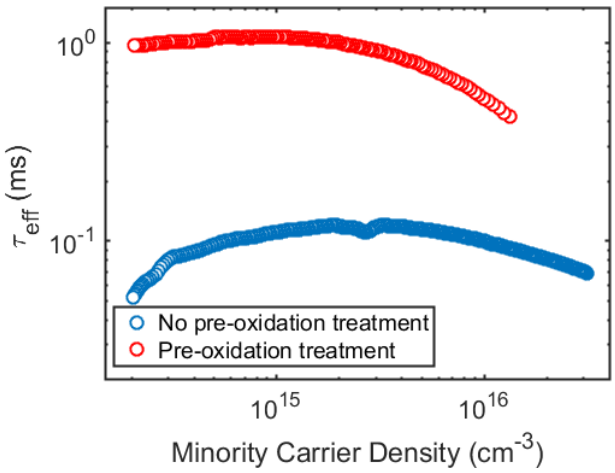

Figure 41: Minority carrier lifetime vs carrier density measured with and without pre-oxidation treatment of AlOx passivated n-type FZ Si wafer.

At a minority carrier density of 10^{15} cm^{-3}, τ_{eff} of the pre-oxidised wafer is 1.08 ms, which is an order of magnitude larger than the τ_{eff} of 0.10 ms of the non-oxidised FZ wafer. Based on our results from section 5.6.1, we can assume that we are not limited by $\tau_{surface}$ and therefore the significant difference in τ_{eff} here is due to alterations in τ_{bulk}. This illuminates the importance of this step in our fabrication process as maintaining τ_{bulk} in the millisecond range is imperative for our carrier collection efficiency. Hence, a pre-oxidation step for our wafers will now be included in our process before determining τ_{eff} from our HWCVD structures.

5.6.3 Passivation of HWCVD junction

Based on our findings thus far, the fabrication process for determining τ_{eff} of our HWCVD structures is refined as:

1. Clean float-zone (FZ) double-side polished, <100>, 280 µm thick 4" diameter n-type wafers in Fuming HNO_3.
2. Dry oxidation in a clean (non-metal) tube furnace at 1000 ^oC for 30 minutes.
3. Immersion in 7:1 buffered HF solution for 1 minute.
4. Grow boron-doped silicon films via HWCVD.
5. Deposit 15 nm AlO_x (method as described in Section 5.6.1) on both sides of structure.
6. Anneal in RTA chamber at 400 ^oC for 30 minutes.

We extend the immersion in 7:1 buffered HF solution as the silicon oxide layer oxidation is thicker than that of the native oxide (~40 nm from dry oxidation and ~2 nm from native oxide) and hence requires longer etching. With an etching rate of 50 nm/min, wafers are immersed in 7:1 buffered HF solution for 1 minute. We study the effect of post-deposition annealing on τ_{eff} of our HWCVD grown junctions. Based on our findings in sections 5.3 and 5.4, we anneal these films at 800 ^oC. Figure 42 (a) shows τ_{eff} versus the minority carrier lifetime for as-deposited and heat-treated HWCVD films. The absolute τ_{eff} values at a minority carrier density of 10^{15} cm^{-3} (extracted from Figure 42(a)) are shown in Figure 42(b).

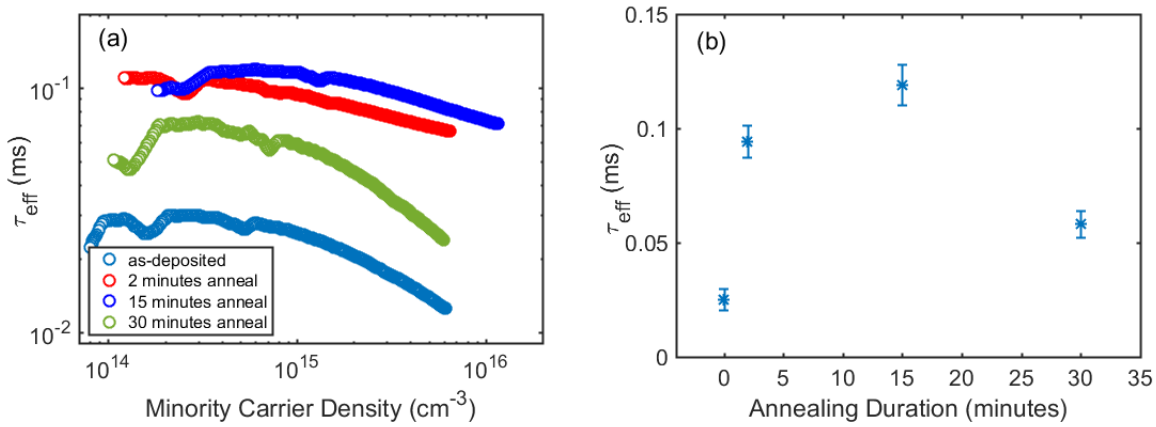

Figure 42: (a) Minority carrier lifetime vs carrier density and (b) minority carrier lifetime vs annealing duration for AlO_x passivated HWCVD emitters.

It is evident from Figure 42(a) and 42(b) that τ_{eff} improves after annealing our boron-doped HWCVD films. The highest τ_{eff} at a minority carrier density of 10^{15} cm^{-3} is seen after annealing for 15 minutes (τ_{eff} = 0.12 ms). A drop in τ_{eff} is determined after annealing for 30 minutes (τ_{eff} = 0.06 ms), although still being higher than the absolute τ_{eff} value from no annealing (τ_{eff} = 0.03 ms). This agrees with findings in section 5.4 where a significant improvement in the morphology of our HWCVD films was determined after annealing, with the optimum duration determined as 15 minutes. Therefore, it can be said that the morphological enhancements via post-deposition annealing translates as a reduction in trap states or voids in our films, based on the establishment of these improvements in minority carrier lifetime.

Despite the improvements from annealing and using AFC for HWCVD growth, the absolute τ_{eff} values from Figure 42(b) are all relatively poor as they are considerably lower than what we would expect for high efficiency devices. Based on findings in Sections 5.6.1 and 5.6.2, we can assume that τ_{eff} here is not limited by the bulk substrate or the exposed surfaces. Therefore, we can conclude that the defect density at the interface must be the limiting factor. Introducing an interfacial layer that can saturate these defects and hence improve τ_{eff} is where our attention lies as a solution. A post-deposition anneal at 800 ^{o}C for 15 minutes will still be required for enhancing the morphology of our boron-doped silicon films.

5.7 Dark current-voltage characteristics

Before approaching interfacial layers, we look at the dark current-voltage characteristics of our HWCVD junctions.

5.7.1 Al metallization for current-voltage extraction

For measuring the current-voltage characteristics, 1 µm of Al was deposited via e-beam evaporation to form contacts on both sides of the p-n junction. A cross-sectional SEM image taken from a metallized HWCVD junction is shown in Figure 43(a). Under dark conditions, the effect of the 15 minutes at 800 ^{o}C annealing step on the electrical characteristics of this film as an emitter was measured. Figure 43(b) shows the current density as a function of the voltage swept between -1 V and +1 V for the as-deposited and heat-treated HWCVD emitters.

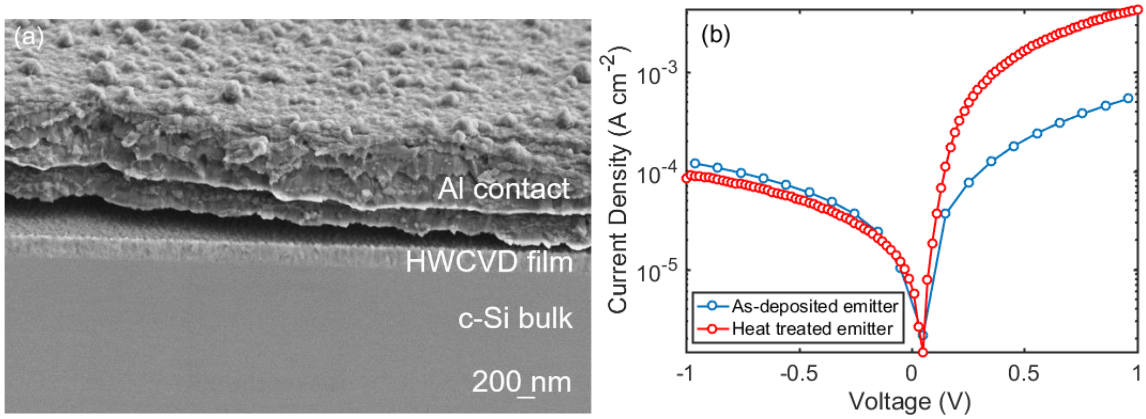

Figure 43: (a) Cross-sectional SEM image of metallized HWCVD junction and (b) current density vs. voltage for as-deposited and heat-treated HWCVD emitters.

The ratio of the current density taken at +1 V and -1 V is known as the rectification factor and can be used as a figure of merit to compare diode performance. A boost from 5 to 55 in the rectification factor is observed by the sharp annealing at 800 ^{o}C step. This agrees with the improvements after annealing in findings from the previous sections. This improvement could be explained by the improvement in morphological structure from Section 5.4, as this would translate as an enhancement in carrier mobility in this region and hence a higher passage of current. The crystallisation of remnant amorphous silicon in our films, the larger grains and higher uniformity from annealing could also be contributing to this improvement. Furthermore, dopant diffusion beyond the interface could also lead to higher carrier diffusion and hence current density (at 1 V) by improving the conductivity of this area.

5.7.2 2-diode model fitting

To analyse the diode characteristics further, the current-voltage results from Figure 43(b) are fitted to a two-diode model. The model used is derived in literature [133] following the equation:

$$J = J_{01}e^{\frac{q(V-JR_S)}{n_1kT}} + J_{02}e^{\frac{q(V-JR_S)}{n_2kT}} + \frac{V-JR_S}{R_{sh}} \quad (19)$$

Here, R_s and R_{sh} are the series and shunt resistances, J_{01} and J_{02} are the dark saturation currents and n_1 and n_2 are the ideality factors for the ideal and non-ideal diodes in the equivalent circuit of the two-diode model, respectively. The current-voltage data is fitted to this model using an open-source tool (2/3 Diode Fit) [134]. The results are shown in Table 8.

Table 8: 2-diode model fitting results from current density vs. voltage characteristics taken from HWCVD grown emitters.

HWCVD film	J_{O1} (nA/cm^2)	J_{O2} (nA/cm^2)	R_s (Ω/cm^2)	R_{sh} (Ω/cm^2)	n_1	n_2
As-deposited	5.2	405	1520	6730	2.2	1
Annealed	2.9	57	735	46040	2.0	1

A reduction in both saturation currents is seen post-annealing. Furthermore, a higher shunt resistance and lower series resistance is derived for the annealed diode. A small reduction in ideality factor for the ideal diode (n_1) is also observed. The reduction in saturation current can support the improvement in junction quality as this would suggest a reduction in carrier recombination losses at the interface, being further supported by the increase in shunt resistance. These changes support the improvement in diode characteristics after annealing, indicating a higher carrier collection efficiency and lower shunting losses in our diode. Despite these improvements, the absolute values for saturation currents are considerably high due to the lack of passivating material for non-contacted regions and no optimization of the ohmic contacts. Furthermore, this ties in well with findings from Section 5.6.3 where low carrier lifetimes were measured and it was suggested that an interfacial passivation layer is required to reduce the density of trap states and voids between the HWCVD layer and the substrate.

5.8 Conclusions

In this chapter, we discussed the growth of boron-doped silicon films via HWCVD for photovoltaic applications. We analysed the growth capabilities of our HWCVD tool and record a deposition temperature boost from 498 ^oC to 535 ^oC using a new filament configuration system that possesses a higher density tungsten filament array. The polycrystalline nature of the as-grown boron-doped films is evident from TEM images and further confirmed by Raman spectroscopy and XRD. With a sharp post-deposition anneal, an enhancement is seen resulting in larger crystals and a less-defective interface. Furthermore, remaining traces of amorphous

silicon are crystallised by the short anneal. Our results confirm p^+ properties with stable doping in the 10^{21} cm^{-3} region, as well as the presence of dopant diffusion beyond the grown interface up to 600 nm in the bulk after the optimised anneal step. However, simulation results predicted a high level of Auger recombination at this doping concentration and therefore some adjustments to the deposition recipe will be required. Improvements from heat-treatment was observed in the minority carrier lifetime recorded, with an order of magnitude increase in τ_{eff} from as-deposited to heat-treated cases. Dark current-voltage measurements show that a boost in current rectification factor is achieved, with improvements in diode characteristics suggested by fitting to a two-diode model. Based our findings in this chapter, it is suggested that an ultrathin layer than can promote hole-transport via tunnelling, as well as reducing the density of trap states at the silicon interface, is needed to further improve the performance. This will branch our work towards forming hole-selective passivating contacts, which are currently highly sought after in the PV industry.

5.9 Contributions

In this work, Antulio Tarazona supported the HWCVD filament arrangement study. John Nutter aided the TEM study, supported by the Henry Royce Institute. The content of this chapter has been published [124] and parts of the text have been included verbatim.

Chapter 6

SiN as Hole-Selective Nanolayers in Passivating Contacts

6.1 Introduction

An ideal passivating contact possesses an interfacial layer that suppresses the electrical losses whilst maintaining a low resistivity [16], [25]. Photovoltaic (PV) technologies require passivation of both electron and hole contacts in order to reach PCEs exceeding 25 % [16]. Furthermore, finding a suitable passivating material that can promote hole tunnelling in our HWCVD junctions (from the previous chapter) is of interest. Commonly, silicon dioxide (SiO_2) or phosphorous-doped hydrogenated amorphous silicon ((p)a-Si:H) are used as electron-selective passivating contacts. The inherent silicon surface passivation ability and the favourable interfacial band alignments on crystalline silicon make these materials highly suitable. However, using SiO_2 for hole contacts has not reached the same high efficiencies [17], [26], [27]. Work into alternative structures for hole contacts is an important area of research [30], [31]. Despite the advancements seen with electron-selective contacts, an efficient hole-selective passivating contact remains a key sought-after development to be accomplished in this field [16]. As discussed in chapter 3, silicon nitride offers great potential towards forming hole-selective contacts for PV devices. Here, we begin our studies on ALD-grown SiN nanolayers towards hole-selective passivating contacts.

6.2 ALD silicon nitride growth

The growth of SiN_x via ALD can be conducted using Bis(tertiary-butyl-amino)silane (BTBAS) as the precursor and a nitrogen plasma source. The precursor used (BTBAS) is known to be capable of growing SiN_x, as well as silicon oxynitride, with various concentration ratios depending on the growth conditions [135]. Following on from the work from Knoops et al.

[97], our aim is to grow uniform SiN_x nanolayers with highly controllable growth rates using plasma-enhanced ALD.

6.2.1 Cyclic SiN_x ALD recipe

The cyclic growth of SiN_x films in the PE-ALD chamber is conducted as follows:

1. BTBAS dose with 100 sccm N_2 carrier for 150 ms.
2. Precursor hold with 100 sccm N_2 for 2 s.
3. Precursor purge with 100 sccm N_2 and 200 sccm Ar for 2 s.
4. Plasma stabilization with 400 W RF plasma for 2 s.
5. Plasma strike with 100 sccm N_2, 200 sccm Ar and 400 W RF plasma for 10 s.
6. Post plasma purge with 100 sccm N_2 and 200 sccm Ar for 1 s.

The ALD process for each cycle of growth is comprised of two half-cycle reactions – (a) the precursor (BTBAS) half-cycle reaction (Step 1-3) and (b) nitrogen reactant half-cycle reaction (Step 4-6). Figure 44 illustrates the two primary steps in this ALD process. The first half-cycle consists of the chemisorption of precursor molecules onto the surface, followed by a purging step to remove excess molecules. The second half-cycle uses the nitrogen plasma to remove the unwanted surface ligands and form silicon-nitrogen bonds, followed by a purge to remove undesirable by-products. For this process, the chamber pressure was kept at 5 Pa, the plasma power at 400 W and the bottom plate temperature at 350 ^oC.

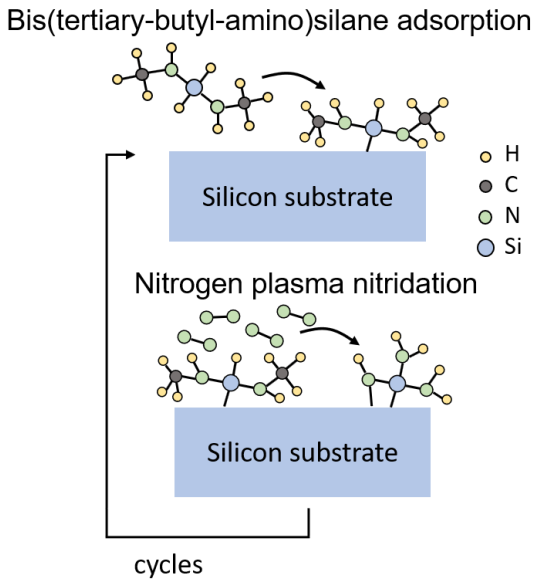

Figure 44: Schematic diagram illustrating the cyclic growth of SiN_x via atomic layer deposition.

6.2.2 BTBAS dosing time

It is important to measure the effect of precursor (BTBAS) dosing time on the growth rate of our SiN_x films. Based on the findings in [97], we expect the growth rate to saturate with respect to the dosing time. Using the ALD process described in Section 6.2.1, we grow SiN_x films using different BTBAS dosing times (25 ms – 225 ms) for a fixed number of 625 cycles. These depositions are conducted on 16 cm^2 silicon substates with pre-immersion in 7:1 buffered HF solution for native oxide removal. The thickness of films in this study are measured using spectroscopic ellipsometry. Figure 45(a)-(d) shows a range of the spatial maps obtained from films grown at 25 ms, 75 ms, 175 ms and 225 ms BTBAS dosing times respectively.

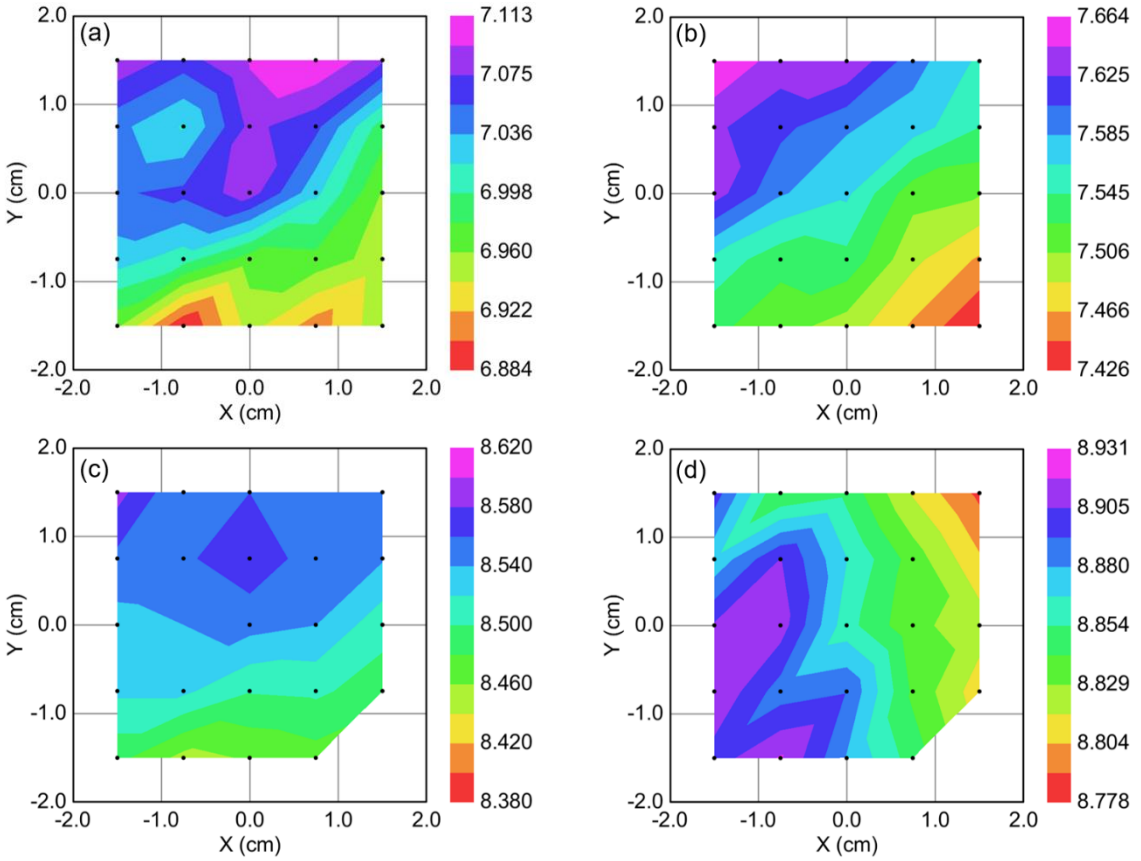

Figure 45: Spatial thickness maps from spectroscopic ellipsometry measurements taken from SiN_x films grown for 625 cycles at (a) 25 ms (b) 75 ms (c) 175 ms and (d) 225 ms BTBAS dosing times. The colour bar axis is measured in nm.

Across a 4 cm x 4 cm silicon substrate, all films show an average thickness non-uniformity of between 3.5% and 5 %. This can be considered highly uniform as such variations when using other deposition methods (e.g. PECVD) are generally higher. For this reason, film growth via ALD is advantageous as non-uniformities in our nanolayers of interest can be detrimental to device performance. In addition, film thickness is seen to increase with higher dosing times.

This is expected as higher volumes of the precursor in each cycle of growth increases the number of BTBAS molecules that can be adsorbed by the substrate surface, react with the N_2 plasma and hence result in a faster growth rate. The growth rate per ALD cycle of silicon nitride films as a function of BTBAS dosing time for dosages between 25 ms – 225 ms is shown in Figure 46. Error bars are not presented in Figure 46 as they would be smaller than the data point markers.

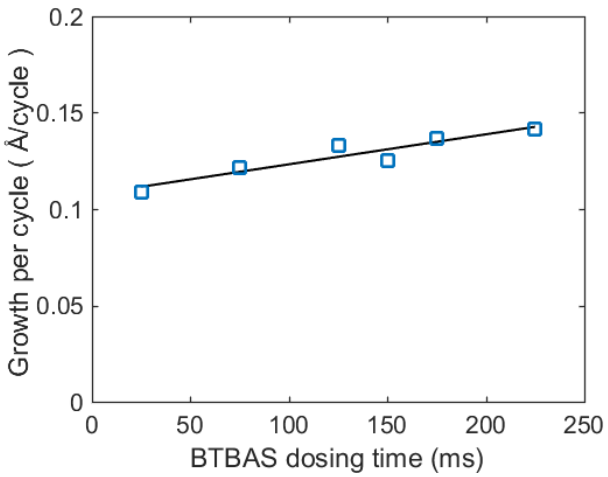

Figure 46: Growth of SiN_x per ALD cycle as a function of BTBAS dosing time.

The growth per cycle is seen to increase with BTBAS dosing time, but with some indication that this starts to saturate at higher (>125 ms) dosing times. Despite some differences in our ALD growth recipe, this relationship can be said to match well with the findings in [97]. A fixed dosing time of 150 ms will be used for the rest of the work, based on the saturation of the growth rate found at this dosing region in Figure 46 and the close agreement with Knoops et al [97].

6.2.3 Growth rate of ALD SiN_x

To determine the growth rate using a 150 ms BTBAS dosing time, we grow SiN_x films with different thicknesses by varying the number of ALD cycles. We vary the cycle number between 160 – 2000 cycles and measure the thickness of the respective films using spectroscopic ellipsometry. Figure 47 shows the film thickness as a function of number of cycles grown at a BTBAS dosing time of 150 ms.

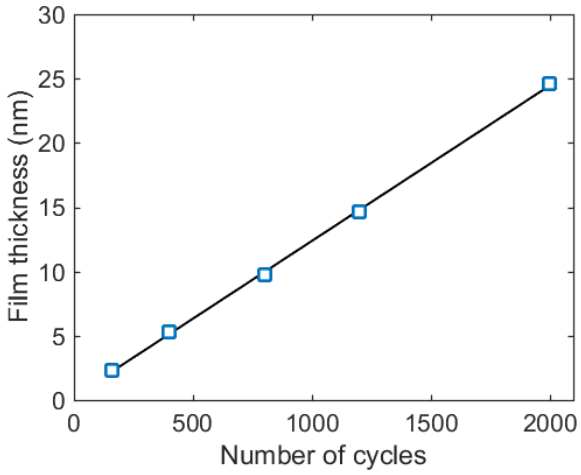

Figure 47: SiN_X film thickness as a function of number of ALD cycles grown at a fixed BTBAS dosing time of 150 ms.

A linear relationship is seen between the film thickness and the number of ALD cycles. This is important as a linear growth rate is needed to accurately grow nanolayers of specified target thicknesses. The growth rate can be determined using the gradient of the fitted line in Figure 47, indicating a rate of 0.122 Å/cycle. This relatively slow growth rate is useful for accurately growing ultra-thin films for use as passivating interlayers, where differences in film thickness at an Å scale can cause significant variations in device performance. The relatively low growth rate is suggested to be due to the incomplete reaction of N_2 plasma with the tert-butyl groups of BTBAS. Furthermore, the non-uniform nucleation on the surface of the underlying substrate in the early cycles further reduces this growth rate.

6.2.4 Thickness uniformity

As mentioned in Section 6.2.2, nanolayer film thickness uniformity is important for the performance of devices when used as an interlayer for emitters and/or passivating contacts. Despite having some appreciation of this from Figure 45, measuring the non-uniformity in thickness at a wafer scale is important for industrial applications. Using the recipe from Section 6.2.1 and a fixed dosing time of 150 ms, silicon nitride was grown using 2000 ALD cycles on a 4” Si (Cz, 1-10 Ω-cm, <100>, 300 μm) substrate and the thickness was measured using spectroscopic ellipsometry. Figure 48 shows the spatial thickness map of the SiN_x film from this study.

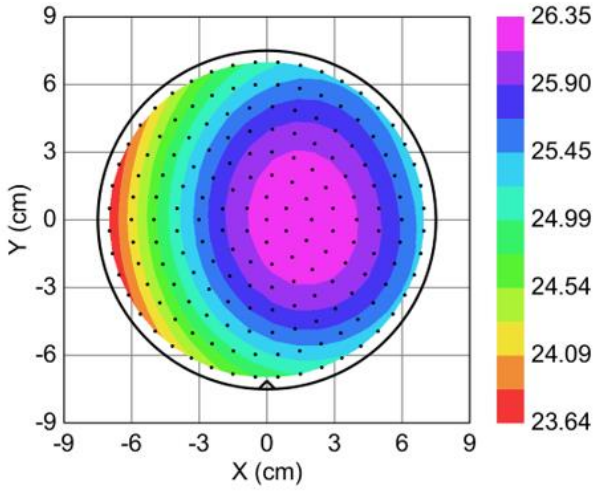

Figure 48: Spatial thickness map taken from spectroscopic ellipsometry measurements taken from SiN_X films grown from 2000 ALD cycles at a fixed BTBAS dosing time of 150 ms. The colour bar axis is measured in nm.

A maximum thickness variation of 10.8 % is determined from the spatial map in Figure 48. This is considerably higher than the variation seen in the 16 cm^2 specimens from Figure 45 (showing variations between 3.5-5 %). As we intend to grow nanolayers (with thicknesses less than 4 nm), this variation ought not to cause large differences across each designated specimen. However, we must still mitigate this in order to avoid unfavourable variations in device performance. One way this could addressed, especially at an industrial scale, is to use a considerably larger ALD chamber and ensuring the isotropic dispersion of precursor and plasma molecules across the entire substrate surface. As most of our studies using this ALD process will be conducted at a much smaller scale, generally between 1 cm^2 and 16 cm^2 in substrate area, this will prove not to be a major issue. Hence, based on the findings in Section 6.2, we can move towards analysing the optoelectronic properties of this material and our structures of interest by using this ALD recipe for growing SiN_x nanolayers.

6.3 Ultrathin ALD nitride properties

6.3.1 Refractive index

Using variable angle spectroscopic ellipsometry measurements, the refractive index of SiN_x films grown at a fixed dosing time of 150 ms is extracted. Figure 49 shows the average refractive index across all ellipsometry angles as a function of wavelength.

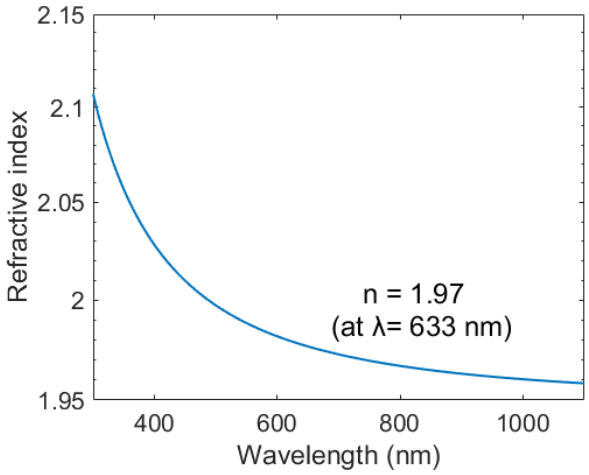

Figure 49: Refractive index of ALD SiN_X taken from variable angle spectroscopic ellipsometry. K data is negligible beyond 235 nm.

The real part of the refractive index (n) is dependent on the wavelength of incident light, as depicted in Figure 49. The n values are seen to decrease with increasing wavelength, with some indication of saturation at n = 1.95. The imaginary part (k data) is negligible beyond 235 nm in photon wavelength and hence is omitted from the plot in Figure 49. The refractive index at a wavelength of 633 nm is extracted as 1.97. When considering the refractive index of air (n = 1) and silicon (n = 3.4), a refractive index of 1.85 is known to be ideal for an interlaying medium to allow constructive interference of light. Hence, the refractive index of our ALD SiN_x can be said to fit closely with this requirement and well-suited to anti-reflection on silicon surfaces. This can become useful when considering the application of this material for surface passivation in the front region of solar cells, where mitigation of optical losses is of high interest.

6.3.2 Atomic concentration ratio

To determine the chemical compositional ratio of our ALD SiN_x films, X-ray photoelectron spectroscopy (XPS) was used. This is done using a monochromatic A1 Kα X-ray (1.487 keV) source with the same geometry used for emission in all measurements. Since the incident X-ray energy is lower than 1.5 keV, the photoelectron kinetic energy is lower than 1.5 keV, which results in a shallow escape depth (between 3-5 nm) for photoelectrons [136]. Full XPS spectra taken from our p-Si (Cz, 1-10 Ω-cm, <100>) substrate and a 25 nm thick SiN_x film are shown in Figure 50(a) and 50(b), respectively. The spectra for p-type c-Si is also presented for appreciation and comparison with the spectra from the ALD SiN_x films.

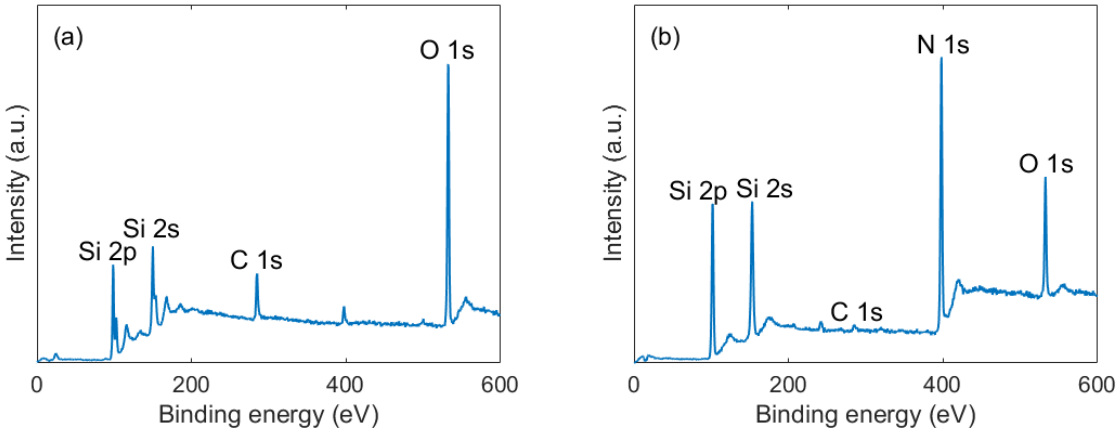

Figure 50: X-ray photoelectron spectroscopy spectra taken from (a) p-Si substrate and (b) 25 nm SiN_X film grown on p-Si substrate.

The electronic core levels (CLs) present at the surface of p-Si and ALD SiN_x can be seen in Figure 50(a) and 50(b) respectively. The presence of oxygen (O 1s) and carbon (C 1s) at the surface of both p-Si and SiN_x is likely due to organic contaminants and hydroxyl groups respectively. Nonetheless, the much larger O 1s peak found in Figure 50(a) for p-Si is mainly due to the native oxide on the p-Si surface.

To measure the relative atomic concentrations of the elements present in our 25 nm thick SiN_x film, high resolution (0.01 eV) scans of the CLs of interest (Si 2p, N 1s, O 1s and C 1s) are taken via XPS at various milling depths. Depth profiles are conducted by milling away material using an Ar ion gun with a current density of 1 $\mu A.mm^{-2}$ and a raster area of 4 mm^2. Based on the ion current density, sputter yield and film density, the etch rate of this film using Ar ions is estimated to be ~0.20 nm/s. To obtain the relative concentration ratio between the chemical elements at these various film depths, all CLs obtained in this study are fitted and corrected using their corresponding XPS sensitivity factors. This method takes the mean free path of the photoelectrons and photoionization cross sections of the CLs into account [137], [138]. Survey identification and chemical state analysis techniques are used to investigate the chemical composition of this film. The relative atomic concentration of Si, N, O and C as a function of etching time in an as-deposited 25 nm thick SiN_x film is shown in Figure 51.

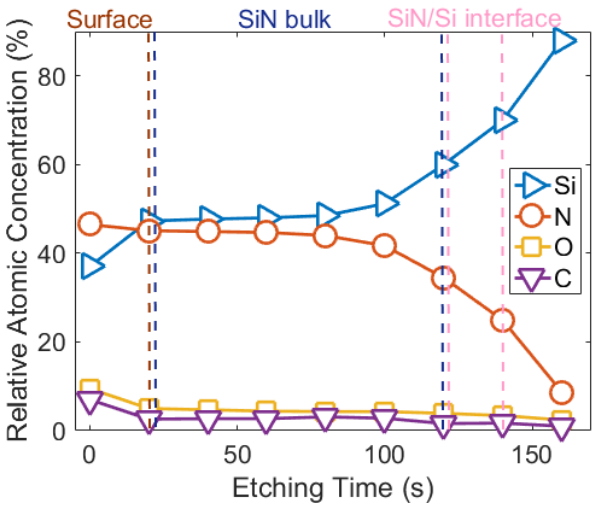

Figure 51: Relative atomic concentration of Si, N, O and C as a function of etching time in as-deposited 25 nm SiN_X film.

The relatively high concentration of oxygen and carbon present at the surface is seen to drop after milling for 20 s (~4 nm depth). Oxygen and carbon concentrations are less than 5 % and 2 % beyond the surface respectively and can be considered negligible in our as-deposited films. In Figure 51, if only silicon and nitrogen are considered, a 1:1 ratio between these elements can be seen beyond the surface which suggests that the chemical composition of our ALD films is SiN. In addition, a sudden drop of nitrogen concentration beyond ~120 s of etching is due to the milling of this material reaching the interface. Hence, we can interpret the 120 s etch region from Figure 51 to be the interface between our 25 nm thick SiN film and p-Si substrate. This supports the results from the spectroscopic ellipsometry thickness measurements as the etching rate of SiN using Ar ions (~ 0.20 nm/s) should result in the interface being reached after ~125 s of etching.

6.3.3 Optical transmission & band gap

We measure the optical transmission through ALD grown SiN via ultraviolet-visible (UV-Vis) spectroscopy. SiN films are grown on Quartz glass substrates that are ultrasonically cleaned in acetone and then rinsed in deionized water. Baseline removal is conducted by taking the transmission spectra of the glass substrates into account during measurements. The transmission spectra for 10 nm and 25 nm thick SiN films are presented in Figure 52(a). At wavelengths larger than approximately 320 nm, a flatter response (i.e. higher transmission) is seen with the 10 nm thick SiN film. This is expected as we would assume the longer optical pathlength of photons through a thicker dielectric would result in higher optical losses. An abrupt absorption edge at approximately 320 nm is seen for both SiN film thicknesses in Figure

52(a). This can give some appreciation of the optical band gap of this material, as this inflection point translates as the region at which the film starts absorbing (i.e. $h\nu \geq E_g$). To analyse this further, the Tauc method [139], [140] is used to determine the optical band gap from the spectra. This method uses the relation between the absorption coefficient, α, and the band gap energy, E_g, as:

$$\alpha h\nu = A(h\nu - Eg)^{1/2} \tag{20}$$

where A is a constant and hν is the photon energy. The absorption coefficient is determined from the absorbance, A_b, as:

$$\alpha = 2.303\frac{Ab}{t} \tag{21}$$

where t is the thickness of the film. The optical band gap of the ALD SiN films deposited on quartz substrates is calculated from the intercept on the energy axis obtained by extrapolating the linear region of the Tauc plot (i.e. $(\alpha h\nu)^2$ vs photon energy plot). Figure 52(b) shows the Tauc plot for the 10 nm and 25 nm thick SiN films.

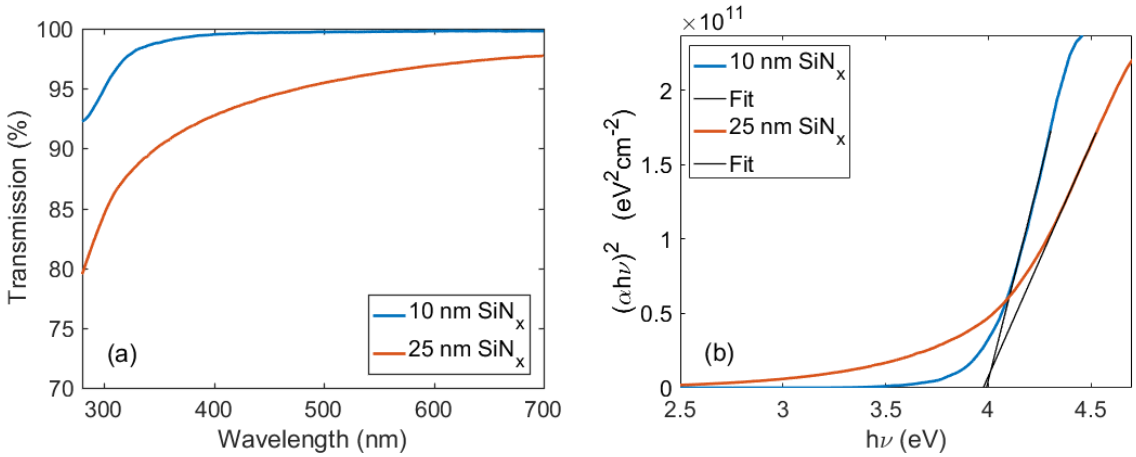

Figure 52: (a) Transmission spectra and (b) Tauc ($(\alpha h\nu)^2$ vs hν) plot for 10 nm and 25 nm SiN_x film.

To determine the optical band gap, Figure 52(b) shows the extrapolation from the linear region of the absorption edge to the baseline for both the 10 nm and 25 nm thick SiN films. An optical band gap of 3.98 ± 0.04 eV is established using this approach for our ALD SiN. The band gap determined for both thicknesses are in close agreement. This is anticipated as we would expect the band gap to be independent of the film thickness. The band gap determined for ALD SiN is considerably lower than the band gap generally quoted in literature for PECVD Si_3N_4 (typically around 5 eV) [89], [141], [142]. Based on the atomic concentration ratio of ALD SiN (from Section 6.3.2), a less nitrogen rich film is seen in ALD films grown here than with

PECVD (where Si_3N_4 is generally deposited). A more silicon-rich silicon nitride film is expected to possess a smaller optical band gap [143] and hence we would expect this material to have a band gap lower than 5 eV. The band gap of 3.98 ± 0.04 eV determined here is used for calculating the electronic conduction band offset at the SiN/Si interface in Section 6.4.

6.4 SiN_x/Si band offset determination

6.4.1 Krauts method for band offset determination

When a semiconductors lattice structure is disrupted by the presence of an insulator, metal, other semiconductor or even vacuum interface, a large deviation of charge distribution occurs at the junction, relative to the bulk of the semiconductor. Poisson's equation predicts a spatially varying electrostatic potential that bends all of the energy levels present equally as a function of distance from the interface [144]. Based on this electrostatic potential, we can define the band bending from this potential, V_B^x, in the energy bands, as shown in the generalised energy band diagram of an abrupt semiconductor interface in Figure 53. From this phenomena, the X-ray photoemission based method proposed by Kraut [116], [145] and widely reported in literature [146]–[148] utilises XPS spectra to determine the valence band offset (ΔE_V) and conduction band offset (ΔE_C) energy at a semiconductor interface. In this approach, the binding-energy difference between the electronic core level energy (E_{CL}) and valence band maxima (VBM) are determined experimentally and used in Kraut's formulae to calculate ΔE_V and ΔE_C.

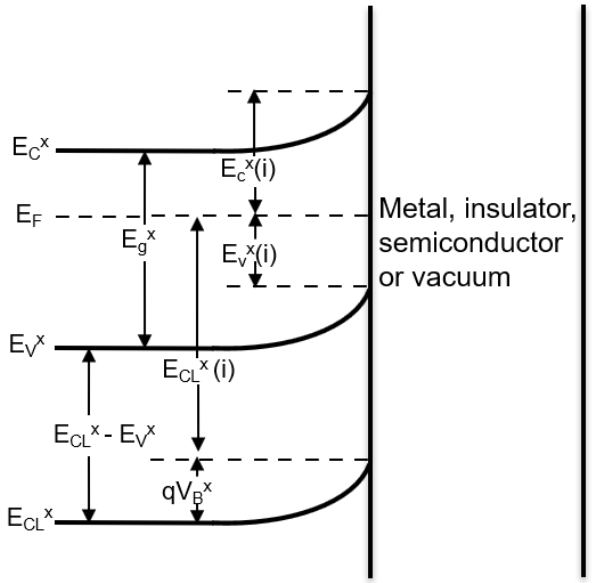

Figure 53: Generalised energy band diagram at an abrupt interface between a semiconductor and metal, insulator, different semiconductor, or vacuum. Inspired from [145].

All energy levels are calculated with respect to the Fermi level (E_F = 0 eV). Using the schematic band diagram in Figure 53, we can define our valence band maximum at the interface, $E_V^x(i)$, as:

$$E_V^x(i) = E_{CL}^x(i) - (E_{CL}^x - E_V^x) \quad (22)$$

And the conduction band minimum at the interface, $E_C^x(i)$, as:

$$E_C^x(i) = (E_{CL}^x - E_V^x) + E_g^x - E_{CL}^x(i) \quad (23)$$

If we have a heterojunction interface, i.e. another semiconductor at the interface, we can define $E_V^y(i)$ and $E_C^y(i)$ in the same way as for semiconductor x in Equations 22 and 23, respectively. Hence, we can calculate the change in valence band energy, ΔE_V, at the interface as:

$$\Delta E_V = E_V^x(i) - E_V^y(i) \quad (24)$$

By fitting Equation 22 for material x and y into Equation 24, we can determine ΔE_V as:

$$\Delta E_V = [E_{CL}^x(i) - (E_{CL}^x - E_V^x)] - [E_{CL}^y(i) - (E_{CL}^y - E_V^y)] \quad (25)$$

For clarity towards XPS analysis, this equation is generally written as:

$$\Delta E_V = (E_{CL}^x(i) - E_{CL}^y(i)) - (E_{CL}^x - E_V^x) + (E_{CL}^y - E_V^y) \quad (26)$$

Here, $(E_{CL}^x(i) - E_{CL}^y(i))$ is the energy difference between the electronic core levels of the two materials at the interface, also known as ΔE_{CL}. Additionally, $(E_{CL}^x - E_V^x)$ and $(E_{CL}^y - E_V^y)$ are the energy difference between the electronic core level centroids and valence band edges of semiconductor x and y respectively. We can also calculate ΔE_C by using Equation 23 for both materials to find the change in conduction band energy, similar to Equation 24 for ΔE_V, which is shown in its simplified format in Equation 27:

$$\Delta E_C = \Delta E_V - (\Delta E_g)_{x\text{-}y} \quad (27)$$

Where $(\Delta E_g)_{x\text{-}y}$ is the energy difference between the band-gap of the two semiconductors.

As we are interested in the interface between ALD SiN and p-Si, we can replace x and y in Equations 7 and 8 with these materials. A schematic band diagram at the SiN/p-Si interface that illustrates ΔE_C and ΔE_V from these calculations is shown in Figure 54.

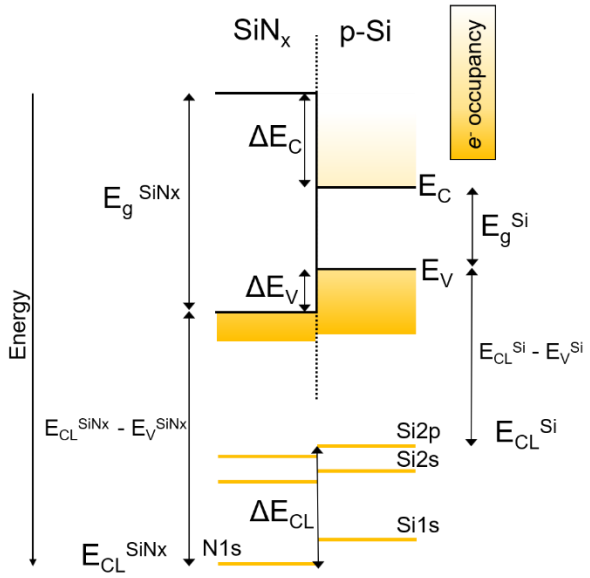

Figure 54: Schematic diagram of band offsets at the SiN/Si interface.

The electronic core levels and valence band maxima for the calculations using Equation 26 and 27 are determined experimentally via XPS. To probe the interface and determine ΔE_{CL}, a 3 nm SiN film on a Si substrate is studied, based on the XPS photoelectron escape depth being under 5 nm. The energy difference between the core level centroids and valence band edges for Si $(E_{CL}^{Si} - E_V^{Si})_{Si}$ and SiN $(E_{CL}^{SiN} - E_V^{SiN})_{SiN}$ are obtained from XPS of the respective thick films. SiN films with thicknesses of 25 nm and 10 nm are examined as independent bulk films in this study. The N 1s and Si 2p orbital peaks are used as E_{CL}^{SiN} and E_{CL}^{Si} respectively. Linear extrapolation of the leading edge to the baseline of the valence band spectra from the respective thick films is used to obtain E_V^{Si} and E_V^{SiN} [146]. This method is widely reported as an accurate way of determining VBM of semiconductors, assuming the use of high-precision (>0.1 eV) XPS.

6.4.2 Electron core level energy and valence band maxima determination

XPS spectra showing core level energy centroids and valence band edges for bulk Si, 25 nm SiN and 10 nm SiN, as well as the CLs at the (3 nm) SiN-Si interface are shown in Figure 55. The CL positions did not change with X-ray irradiation time, and all XPS spectra are calibrated to the C 1s peak at 284.8 eV. A Savitsky-Golay filter is used to fit all valence band edge spectra to a polynomial using the least squares method [149], and all core level peaks are fitted using Shirley backgrounds and Voigt functions [148].

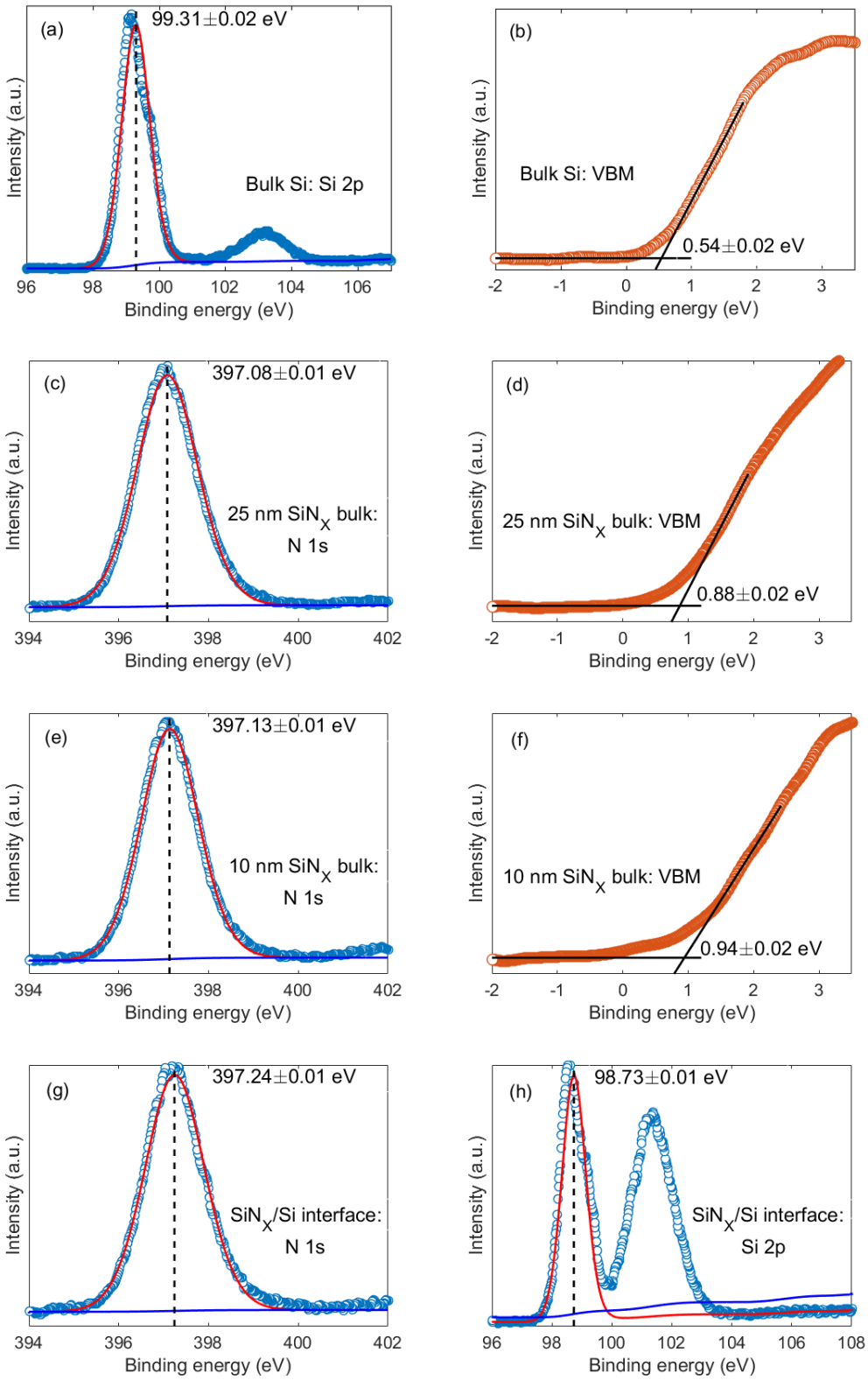

Figure 55: XPS spectra showing (a) Si 2p CL and (b) valence band edge from bulk p-type Si, (c) N 1s CL and (d) valence band edge from 25 nm (bulk) SiN_x, (e) N 1s CL and (f) valence band edge from 10 nm (bulk) SiN_x and (g) N 1s CL and (h) Si 2p CL from 3 nm (interface) SiN_x on p-type Si. Solid red lines show Voigt fits, solid blue lines show the Shirley background, dashed black lines show the CL centroid positions (in a, c, e, g and h) and the solid black lines show the extrapolations to determine the VB edge (in b, d and f).

From Figure 55(a) and (b), the Si 2p core level energy and the leading edge of the valence band spectra for bare p-type Si are determined as 99.31 ± 0.01 eV and 0.54 ± 0.02 eV respectively. This suggests an energy difference of 98.77 ± 0.03 eV for $(E_{Si2p} - E_V)_{Si}$, which is in agreement with findings in literature [146], [150]. Figure 55(c)-(d) show the N 1s core level energy and leading edge of the valence band spectra for the 25 nm thick films. The N 1s core level energy is detected at 397.08 ± 0.01 eV and the valence band edge at 0.88 ± 0.02 eV. Figure 55(e)-(f) show the N 1s core level energy and leading edge of the valence band spectra for the 10 nm thick films. The N 1s core level energy is detected at 397.13 ± 0.01 eV and the valence band edge at 0.94 ± 0.02 eV. Hence, an energy difference of 396.20 ± 0.03 eV and 396.19 ± 0.03 eV for $(E_{N1s} - E_V)_{SiN}$ using the 25 nm and 10 nm specimen as bulk SiN is determined. The core level energy peaks for SiN (N 1s) and Si (Si 2p) at the interface from the 3 nm thick SiN specimen are shown in Figure 55(g) and (h). In Figure 55(h), two peaks are seen for Si 2p core level at the interface. This is because the Si 2p core level at the interface has contributions from both the substrate and the ultra-thin SiN layer. Based on the ALSCOF XPS peak fitting library, the Si 2p peaks found closest to 101.30 eV and 99.4 eV are known to be due to nitrides and elemental silicon respectively. Therefore, the core level energy at the interface of Si $(E_{Si2p}^{Si})_{SiNx/Si}$ and SiN $(E_{N1s}^{SiN})_{SiN/Si}$ are determined as 98.73 ± 0.01 eV and 397.24 ± 0.01 eV respectively, with the energy difference between these core levels at -298.51 ± 0.03 eV.

6.4.3 SiN-Si band offsets

For calculating the band offsets at the SiN/p-Si interface, Table 9 displays a summary of the measured XPS data. By using Equation 26 from Section 6.4.1, the valence band offset is determined as -1.08 ± 0.08 eV and -1.09 ± 0.08 eV using the 25 nm and 10 nm thick SiN films as bulk SiN respectively. A negative band offset value suggests that the valence band energy of SiN is at a greater energy relative to the vacuum than the valence band energy of Si. From these ΔE_V values and using the optical band gap of the two bulk materials, the conduction band offset is determined as 1.78 ± 0.13 eV and 1.77 ± 0.13 eV.

Table 9: XPS data required for determining the band offsets at the SiN/Si interface using the Krauts method, taken from the measured data in Figure 55.

	Si bulk	SiN bulk		Interface
	Bare p-Si	(25 nm)SiN/Si	(10 nm)SiN/Si	(3 nm)SiN/Si
E_{CL} (eV)	99.31 ± 0.02 (Si2p)	397.08 ± 0.01 (N1s)	397.13 ± 0.01 (N1s)	397.24 ± 0.01 (N1s) 98.73 ± 0.01 (Si2p)
E_V (eV)	0.54 ± 0.02	0.88 ± 0.02	0.94 ± 0.02	-

From these calculations, $\Delta E_C/\Delta E_V$ ratios of 1.64 ± 0.24 and 1.62 ± 0.24 are established, suggesting favourability towards hole transport at this interface. The values calculated for both bulk SiN_x films (10 and 25 nm thicknesses) are understandably in close agreement (and within the experimental uncertainty). Based on the $\Delta E_C/\Delta E_V$ ratios, a lower tunnelling potential barrier is defined for holes than for electrons. Despite showing favourability towards hole transport when as-deposited, it is important to examine if these band offsets change over time or are altered by external influences.

6.5 Understanding nanolayer degradation

6.5.1 Thickness alteration

To understand the impact of ageing on these films when stored under different conditions, 3 nm SiN films grown on Si were stored in our cleanroom within a desiccator, both with and without photoresist, over a two-week period. During this time, film thickness was repeatedly measured by spectroscopic ellipsometry, the results from which are plotted in Figure 56.

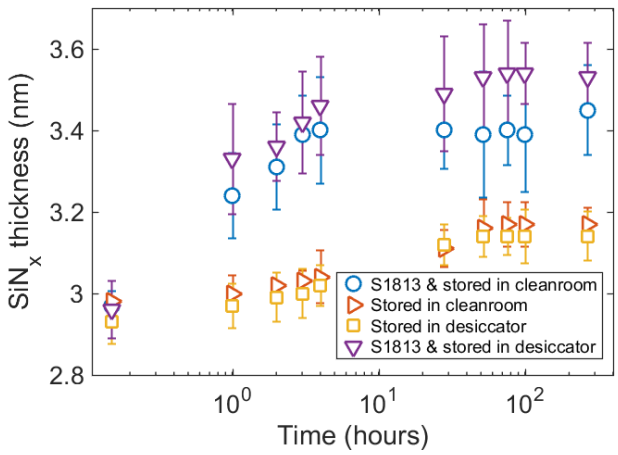

Figure 56: SiN thickness measured over two weeks when stored in a cleanroom and desiccator, with and without S1813 photoresist protection layer.

The thickness of all SiN films studied is shown to increase over time, with no significant difference observed between storing in a desiccator or cleanroom. Thickness alterations cease within the first 48 hours. Films without photoresist protection are shown to increase in thickness by ~0.2 nm, whereas the photoresist protected samples are shown to increase by ~0.5 nm. This can be attributed to either remnants of photoresist after rinsing with acetone and isopropanol prior to each thickness measurement, or due to alterations caused during the baking step after photoresist spinning. Quantifying the impact of ageing on the hole-selectivity of this film is crucial. Furthermore, thickness changes due to degradation must also be considered as these variations can have detrimental effects on device performance.

6.5.2 Degraded SiN/Si band offsets

Identical XPS measurements as Section 6.4.2 are conducted on these films after they were stored in the cleanroom for one week. Figure 57 shows the core levels and valence band edges for 25 nm and 10 nm thick SiN and the core levels detected at the SiN/Si interface after ageing. The N1s core level energy and leading edge of the valence band spectra for the 25 nm thick films are shown in Figure 57(a)-(b). The N 1s core level energy is detected at 397.47 ± 0.01 eV and the valence band edge at 1.34 ± 0.02 eV. Figure 57(c)-(d) show the N 1s core level energy and valence band spectra for the 10 nm thick film. The N 1s core level energy is detected at 397.51 ± 0.01 eV and the valence band edge at 1.37 ± 0.02 eV. Therefore, this suggests an energy difference $(E_{N1s} - E_V)_{SiN}$ of 396.13 ± 0.03 eV and 396.14 ± 0.03 eV after degradation, using the 25 nm and 10 nm specimen as bulk SiN. The core level energy peaks (E_{N1s}^{SiN} and E_{Si2p}^{Si}) at the interface, as shown in Figure 57(e) and (f), are determined as 397.45 ± 0.01 eV and 98.79 ± 0.01 eV respectively, resulting in ΔE_{CL} as -298.66 ± 0.03 eV. Therefore, the valence band offset at the SiN/Si interface is determined as -1.30 ± 0.08 eV and -1.29 ± 0.08 eV after degradation.

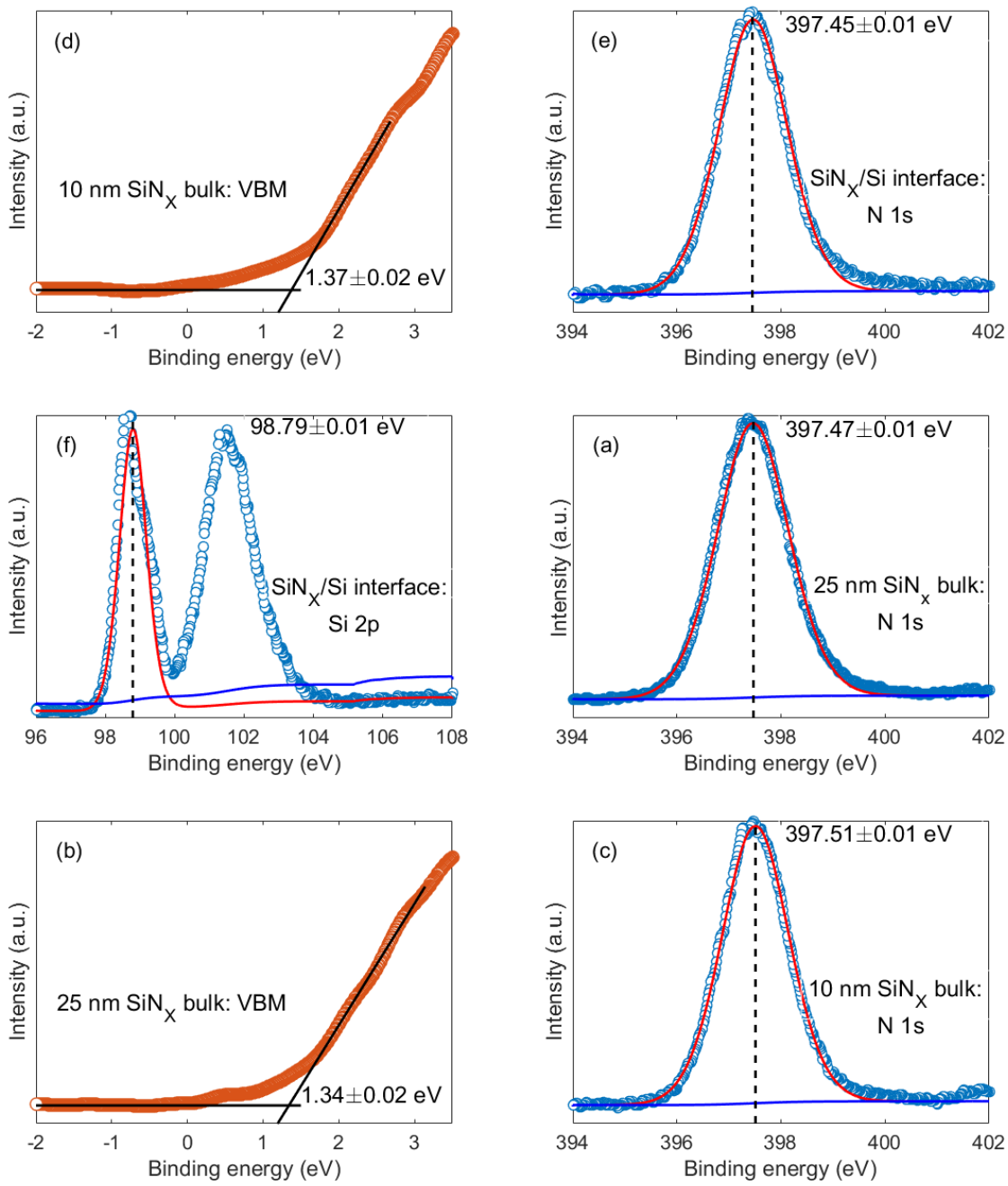

Figure 57: XPS spectra of aged films, showing (a) N 1s CL and (b) valence band edge from 25nm SiN_x, (c) N 1s CL and (d) valence band edge from 10nm SiN_x and (e) N 1s CL and (f) Si 2p CL from 3nm SiN_x on p-Si. Solid red lines show Voigt fits, solid blue lines show the Shirley background, dashed black lines show the CL centroid positions (in a, c, e and f) and the solid black lines show the extrapolations to determine the VB edge (in b and d).

The optical band-gap determined immediately after film growth did not show a considerable difference with the aged band-gap. The conduction band offset at the interface after degradation can therefore be determined as 1.56 ± 0.13 eV and 1.57 ± 0.13 eV, suggesting $\Delta E_C/\Delta E_V$ as 1.20 ± 0.17 and 1.22 ± 0.18. This implies that the hole-selectivity degrades.

6.5.3 Chemical compositional ratio

Changes in the chemical composition of these films after ageing are investigated. The relative atomic concentrations of the elements in the aged 25 nm thick SiN film were determined from CL peaks (Si 2p, N 1s, O 1s and C 1s) taken from survey scans at multiple milling depths, similar to the as-deposited SiN XPS measurements in section 6.3.2. These are shown in Figure 58.

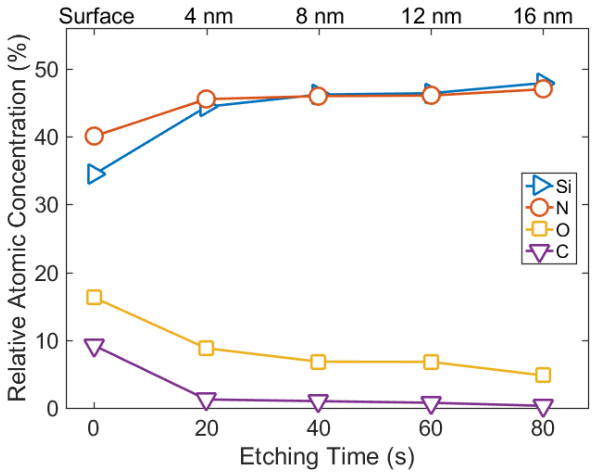

Figure 58: Relative atomic concentration ratio of Si, N, O and C as a function of etching time (corresponding to depth into the film) in aged SiN bulk (25 nm thick film).

The relatively high concentration of oxygen and carbon at the surface is likely due to organic contaminants and hydroxyl groups respectively. The carbon concentration is negligible beneath the surface, whilst the presence of oxygen beneath the surface, shown to be between 9 % and 5 % from a 4 nm to 16 nm depth, remains. The concentration of oxygen is seen to be higher at all milling depths when compared to the as-deposited SiN case in section 6.3.2. This suggests a transition to a more oxygen rich film with ageing. Furthermore, chemical state analysis using the ALSCOF library gives some indication of the film transitioning from silicon nitride to silicon oxy-nitride, based on the concentration levels detected. This could be the cause of the thickness and band offset shifts observed with ageing.

Increases in film thickness will reduce the conductivity of a passivating contact but this could be mitigated by growing a thinner initial film. Decreases in band offset ratio (and so hole selectivity) would be detrimental to the performance of a passivating contact but it is encouraging that $\Delta E_C/\Delta E_V$ remains greater than 1, even after ageing. For industry applications, encapsulating this material with novel protective layers could avoid the degradation of the tunnelling dielectric.

6.6 Conclusions

In this chapter, the formation of a hole-selective silicon nitride nanolayer was studied. Highly controllable, Å-scale growth of SiN films using atomic layer deposition was conducted and their hole selectivity using a photoemission-based method to determine the band alignments at the SiN/Si interface was explored. The film thicknesses determined immediately after growth are seen to rise by 2-5 Å over a period of 48 hours, after which the thickness stabilises. A band offset ratio ($\Delta E_C/\Delta E_V$) of 1.62 ± 0.24 is determined for freshly-grown SiN nanolayers. However, the hole selectivity reduces due to degradation, with a final $\Delta E_C/\Delta E_V$ value of 1.22 ± 0.18. Despite the reduction in band offset ratio, a larger barrier to electrons than to holes remains and therefore these films show promise for application in hole selective contacts for silicon solar cells. Furthermore, this nanolayer could be combined as an interfacial layer for the HWCVD-formed junctions described in chapter 5 towards emitter applications (i.e. forming a SHJ solar cell).

6.7 Contributions

The content of this chapter has been published [151] and parts of the text have been included verbatim.

Chapter 7

Contact formation using SiN nanolayers

7.1 Introduction

The band alignments at the SiN/Si interface determined in the previous chapter showed great promise towards hole-selective carrier transport. However, to form a fully-functioning carrier-selective passivating contact that can competitively enter the PV industry, further characteristics like contact resistivity and surface passivation need to be explored. The contact resistivity, ρ_c, is the interface resistance presented to collected charge carriers (holes). The surface passivation capability of such contacts is generally measured through the dark recombination current, J_0, which is the flux of non-collected charge carriers (electrons) in the contact. Ideally, a 'good' passivating contact possesses a relatively low ρ_c and J_0, but generally a trade-off exists between these when forming passivating contacts [16], [17], [152]. Here, we explore the properties of this material further towards carrier-selective passivating contact formation.

7.2 Contact resistivity

Maintaining a low ρ_c is a crucial factor for pursuing high performance devices. In essence, ρ_c is a quantitative metric that characterises the passage of electrical current through a carrier-selective contact. To measure ρ_c of an Ohmic contact, the Cox and Strack method (CSM) and transfer length method (TLM) are generally used [153]–[155]. These methods rely on using the current-voltage characteristics to extract the resistivity of the contact. The TLM technique measures the resistance via current flow only in the inversion layer of the contact, whereas current flows vertically in the CSM technique (as shown in Figure 59(a)) under an applied voltage. The CSM technique is advantageous as the current distributes homogeneously below the contact rather than distributing exponentially directly below the contact as in the TLM technique. Nonetheless, in cases where hole transport materials and substrates are Schottky heterojunction rather than Ohmic, the traditional approaches fail to accurately extract ρ_c due to

rectification effects [156]. To tackle this, an expanded CSM technique that can effectively separate the contact resistivity from Schottky contacts has been reported and successfully used [156]. This combines the traditional CSM approach with Cheung's method to extract an effective ρ_c [156]–[158] and will be used in our work.

7.2.1 Expanded Cox and Stack method

In the traditional CSM model, an array of circular electrodes with incremental diameters are deposited on the front of the substrate and a blanket deposited electrode on the rear side. Under a varied applied voltage, the current flows longitudinally in the device, which is depicted in Figure 59(a). As seen from Figure 59(a), the total resistance, R_T, is comprised of:

$$R_T = R_C + R_S + R_O \tag{28}$$

Where R_C is the contact resistance, R_S is the spreading resistance in the substrate and R_O is the residual resistance. The spreading resistance is defined as:

$$R_S = \frac{\rho}{d\pi}\arctan\frac{4t}{d} \tag{29}$$

Where d is the diameter of the circular electrode and ρ and t are the resistivity and thickness of the substrate respectively. The contact resistance is defined as:

$$R_C = \frac{\rho_c}{\pi d^2/4} \tag{30}$$

To eradicate the rectification effects from the current-voltage characteristics of potential non-Ohmic contacts, we can extract R_T by combining the traditional CSM approach with [156]:

$$\frac{d(V)}{d(\ln(I))} = R_T I + \frac{nq}{kT} \tag{31}$$

Where I is the current, V is the voltage, n is the ideality factor of the substrate, q is the electrical charge, k is the Boltzmann constant and T is the temperature.

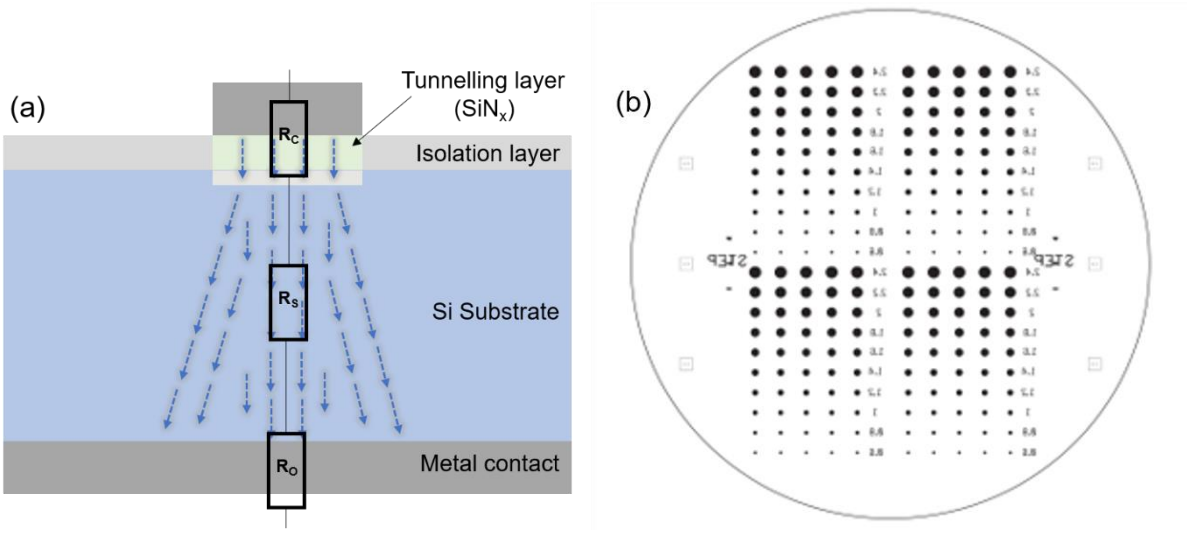

Figure 59: (a) Cross-sectional current flow in carrier-selective contact device structures using the Cox and Strack method and (b) an example from the lithography masks made for conducting the Cox and Strack technique for extracting ρ_c.

For this method, we design and fabricate lithography masks using acetate sheets with periodic circular disk patterns with varying diameters in order to accurately fabricate the front contacting regions of devices. This is shown in Figure 59(b). The refined photolithography process for achieving these circular electrode structures consists of:

1. Deposit 50 nm Al_2O_3 as isolation layer on Si wafer.
2. Spin S1813 photoresist on isolation layer at 5000 rpm for 30 s, followed by baking at 115 ^oC for 1 minute.
3. Expose photoresist for 2.5 s in soft contact mode with 250 µm mask-wafer separation using dark-field mask. Following exposure, develop in MF319 for 45 s, followed by a rinse in de-ionized water.
4. Etch Al_2O_3 in openings with buffered 7:1 HF solution for 2 minutes, followed by a rinse in de-ionized water.
5. Rinse resist off with acetone, followed by IPA. Immediately load in ALD tool for SiN deposition. Deposit SiN layer.
6. Spin AZ2070 photoresist at 6000 rpm for 1 minute, followed by baking at 110 ^oC for 1 minute.
7. Expose photoresist for 12 s in soft contact mode with 250 µm mask-wafer separation using light-field mask. Following exposure, bake at 110 ^oC and develop in 726MIF for 90 s, followed by a rinse in de-ionized water.

8. Deposit 100 nm of metal (Al/Au) via E-beam evaporation on front and rear side of wafer.
9. Lift-off in N-Methyl-2-pyrrolidone overnight, kept at room temperature. Rinse with acetone and IPA.

From the current-voltage characteristics that are extracted from our fabricated structures of interest, R_T is determined by using Equation 31 ($\frac{d(V)}{d(ln(I))}$ vs I). Following this, R_S is calculated using Equation 29 and R_C is calculated using Equation 28. Consequently, we can determine the specific contact resistivity, ρ_c, by plotting R_C (or $R_T - R_S$) against 1/S (where S is the contact area) and extracting the gradient.

7.2.2 Al/p-Si contact resistivity

Aluminium (Al) is widely used for electrode formation in the PV industry, as well as in integrated circuit technology. Prior to examining the contact resistivity using Al electrodes on our SiN tunnelling layer, we study the resistivity of just Al-Si contacts. This is to ensure that our later resistivity measurements, which include the tunnelling layer, are not limited by the Al-Si contact at the back electrode. To form an Ohmic contact on p-type or n-type silicon using Al, a heavily doped layer (either Al/p^+/p or Al/n^+/n) must lie at the interface to improve carrier transport in this region [159]. One way to achieve this is by conducting a sharp anneal. When Al on Si is annealed, a p^+ region near the Al-Si interface is generated, which reduces the depletion width and the conduction is led by tunnelling. In addition, the uniformity of the contact area morphology is significantly improved through annealing, which in turn drastically reduces the contact resistivity [160].

We fabricate Al/Si/Al structures that possess circular Al electrodes with varying diameters between 1 mm and 2 mm at the front, as well as full-area rear electrodes, as illustrated in Figure 59(a). A set of samples are heat treated for 1 minute at 350 ^oC, 400 ^oC and 450 ^oC using rapid thermal annealing. The current-voltage characteristics are extracted by applying a varying voltage and measuring the current using a Keithley source meter set-up. The current-voltage characteristics for the as-deposited structures are displayed in Figure 60(a) and for the annealed structures in Figure 60(b)-(d).

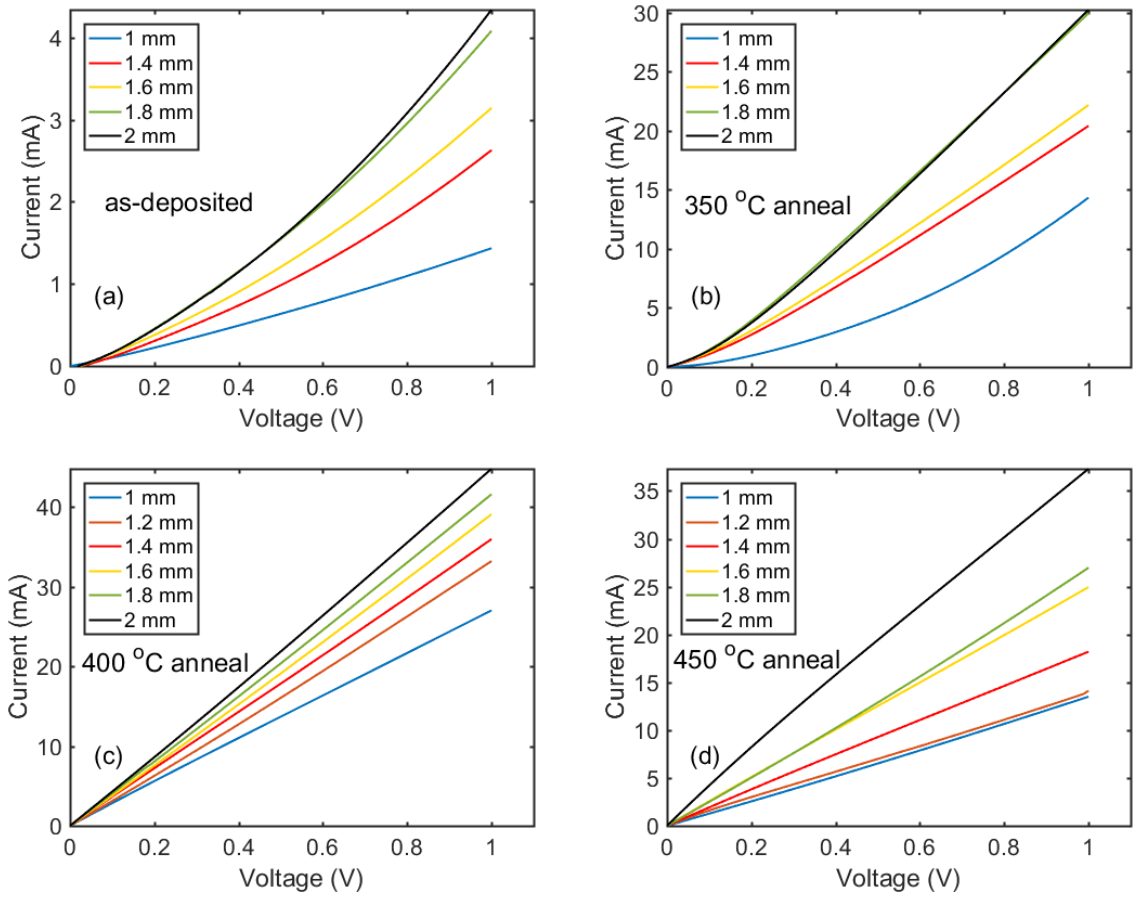

Figure 60: Current-voltage characteristics taken from Al/Si/Al structures (a) as-deposited, annealed at (b) 350 °C, (c) 400 °C and (d) 450 °C.

The regular dispersion of the current-voltage curves in Figure 60 are indicative of the variation of the series resistance due to the varying contact area. This translates as a variation in the contact resistance. From Figure 60(a), the as-deposited Al-Si contacts can be said to be non-Ohmic (or Schottky) as we would expect a linear current-voltage relationship for Ohmic contacts. Once annealed at 350 °C for 1 minute (Figure 60(b)), the current at all voltages can be seen to have significantly increased, with some cases showing Ohmic behaviour. This is further improved by annealing at 400 °C, as a higher overall current can be seen in Figure 60(c), as well as all contacts illustrating Ohmic behaviour. As shown in Figure 60(d), the Ohmic behaviour is maintained at an annealing temperature of 450 °C, despite a slight reduction in overall current flow when compared to Figure 60(c).

As mentioned earlier, the expanded CSM model is used to fit the current-voltage curves to Equation 31 and extract R_T from the linear region. The contact resistance, R_C (or $R_T - R_S$), for each electrode diameter is then plotted against 1/S, and the gradient of the linear fit is extracted

for determining ρ_c. The $R_T - R_S$ versus 1/S plots for the as-deposited structures are displayed in Figure 61(a) and the annealed structures in Figure 61(b)-(d).

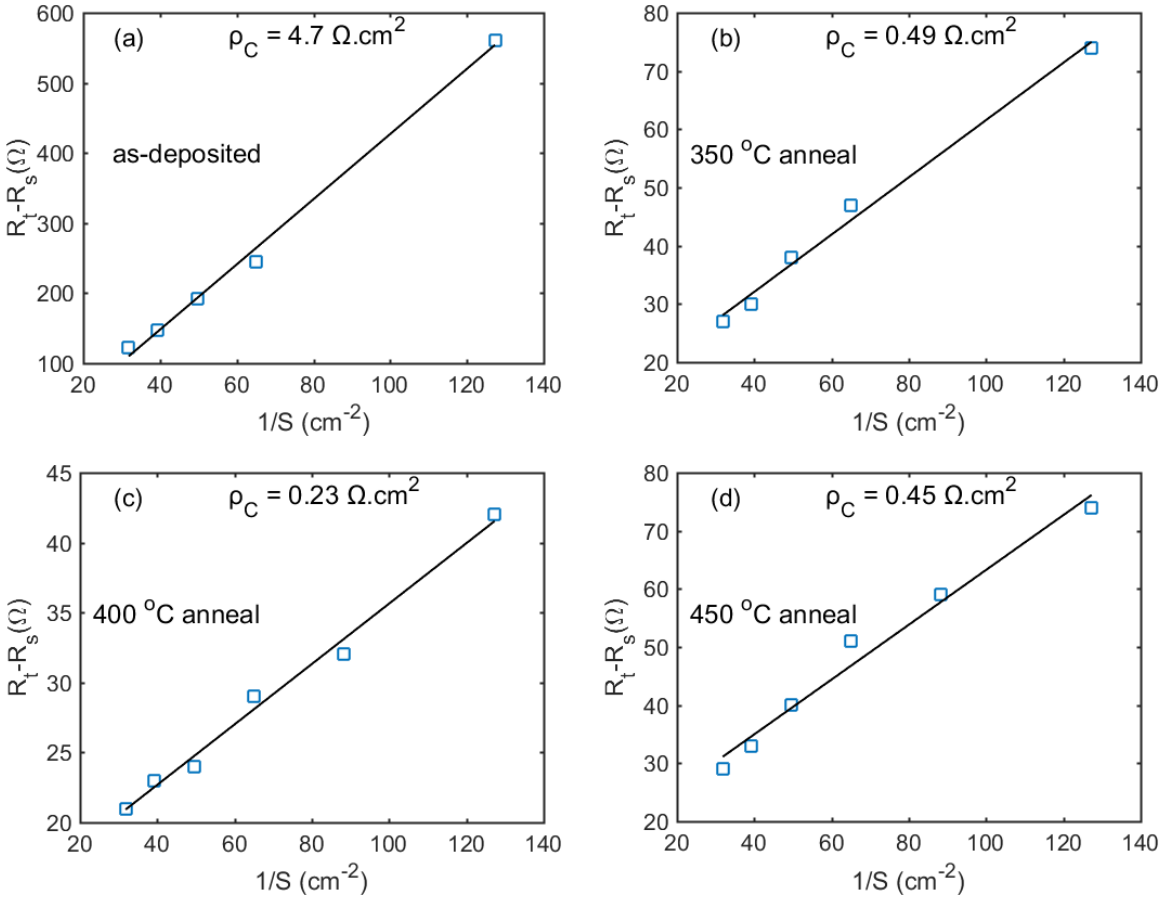

Figure 61: R_T - R_S versus 1/S plots and the corresponding linear fits for extracting ρ_c from Al/Si/Al structures. (a) as-deposited, annealed at (b) 350 °C, (c) 400 °C and (d) 450 °C.

The dependence of ρ_c of the Al-Si contacts on the post-deposition annealing temperature is summarised in Figure 62. It is evident that a post deposition anneal reduces the contact resistivity by at least an order of magnitude. The optimal post deposition annealing temperature of the Al-Si contacts, based on the ρ_c values from Figure 61, is determined to be 400 °C. This shows a resistivity of 0.23 Ω.cm^2, which is significantly lower than 4.7 Ω.cm^2 from the as-deposited Al-Si contact. Furthermore, the Ohmic behaviour seen from Figure 2(c) is highly desirable for electrical connections in our semiconductor devices. It is expected that the formation of a highly doped silicon layer underneath the metal electrode coating during the annealing step allows the Schottky barrier at the metal/semiconductor interface to be overcome. Improvements in the contact morphology from annealing further enhance our contact resistance.

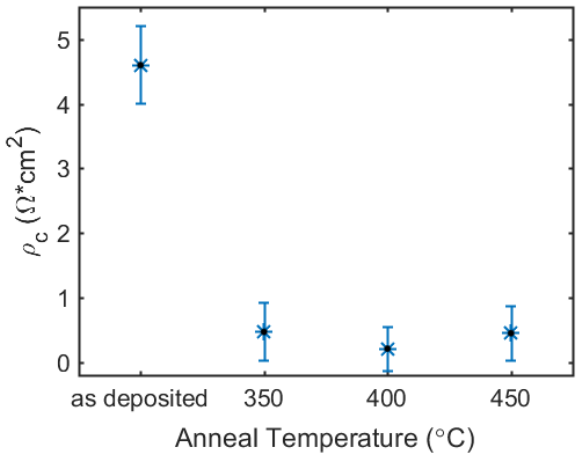

Figure 62: Dependance of ρ_c of the Al-Si contacts on the post-deposition annealing temperature.

7.2.3 Al/SiN/p-Si contact resistivity

Following on from Section 7.2.2, Al/SiN/Si/Al structures that possess circular Al electrodes with varying diameters between 1 mm and 2 mm are fabricated at the front, with full area electrodes at the rear. A range of SiN layer thicknesses between 1 nm and 4 nm are studied to examine the effect of the thickness of the tunnelling layer on the contact resistivity. In addition, the effect of a post-deposition anneal at 400 ^{o}C for 1 minute is studied. This is mainly aimed at improving the contact quality at the rear side of the devices. The current-voltage characteristics of the devices with SiN thicknesses of 1 nm – 4 nm are displayed in Figure 63(a), 63(c), 63(e) and 63(g), with the annealed cases shown in Figure 63(b), 63(d), 63(f) and 63(h).

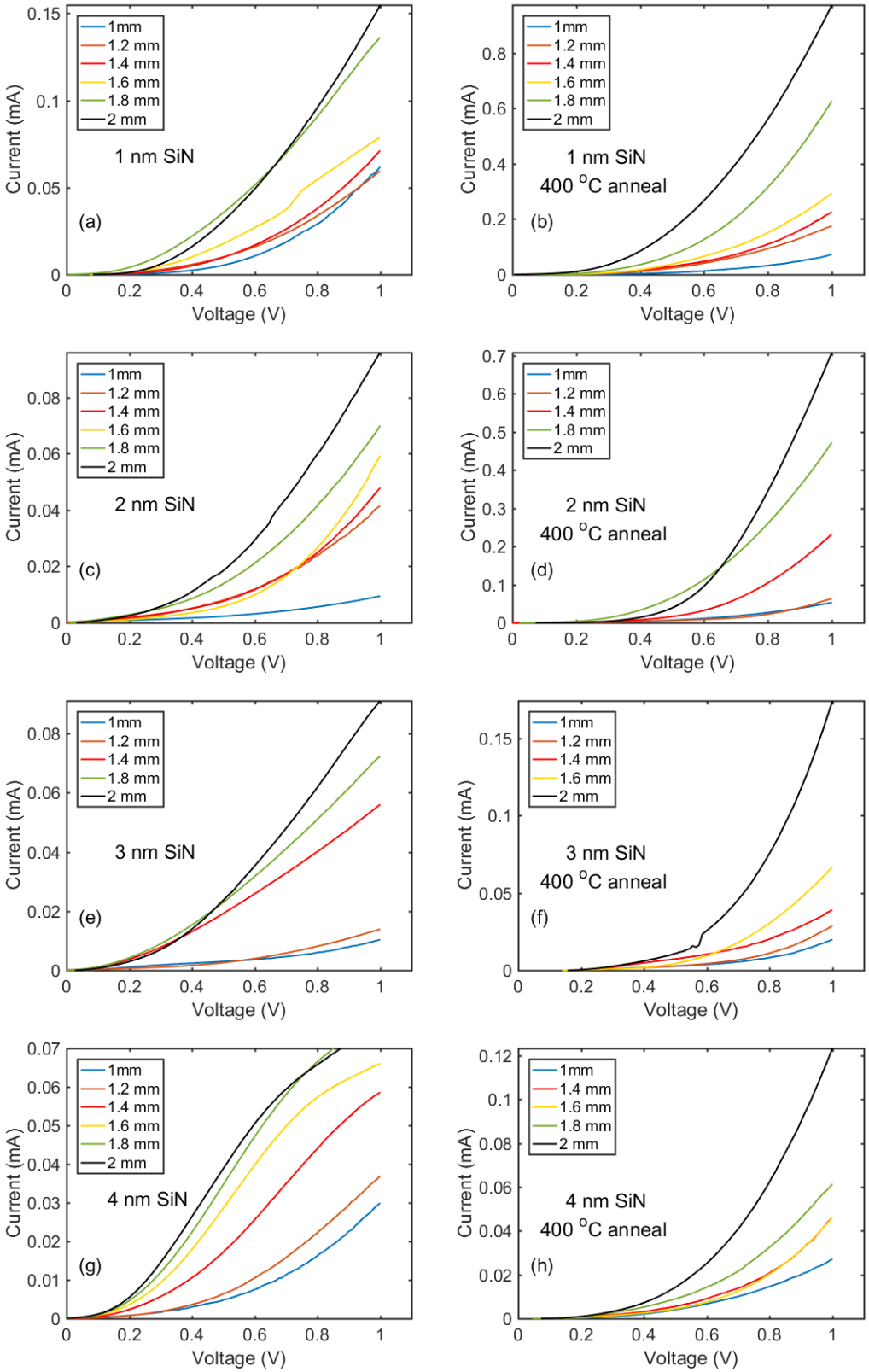

Figure 63: Current-voltage characteristics taken from Al/SiN/Si/Al structures. As deposited: (a) 1 nm SiN, (c) 2 nm SiN, (e) 3 nm SiN and (g) 4 nm SiN. Annealed at 400 °C for 1 minute: (b) 1 nm SiN, (d) 2 nm SiN, (f) 3 nm SiN and (h) 4 nm SiN.

All current-voltage plots shown in Figure 63 are seen to be non-Ohmic. The addition of a dielectric layer under the front electrode can be said to underpin the Schottky barrier formation shown in our current-voltage curves. In general, a higher overall current flow is extracted as the thickness of the SiN layer is reduced from 4 nm to 1 nm. A post-deposition anneal is seen to improve the performance of these contacts, as a higher current at all voltages is extracted for the annealed cases at all thicknesses. Nonetheless, the non-Ohmic behaviour of these contacts remains. To evaluate the quality our Al/SiN/Si contacts further, we use the CSM model to extract the contact resistivity from the current-voltage curves in Figure 63. The $R_T - R_S$ versus 1/S plots for the as-deposited structures with SiN thicknesses of 1 nm – 4 nm are displayed in Figure 64(a), 64(c), 64(e) and 64(g), and the annealed cases shown in Figure 64(b), 64(d), 64(f) and 64(h).

The contact resistivity is seen to increase with increasing SiN thickness. In addition, a post-deposition anneal is seen to reduce ρ_c for all SiN thicknesses. The dependence of ρ_c on the thickness of the SiN tunnelling layer, as well as enhancements from the annealing step, is displayed in Figure 65. Despite the considerable drop in ρ_c after the anneal step, the absolute values of ρ_c for all cases in this study can be considered too high for silicon contacting applications. Furthermore, the effects of the annealing step on the Al-SiN interface is undetermined and may be detrimental to the contact quality. In general, a different metal or alloy that possesses Ohmic behaviour as deposited on silicon needs to be investigated for the purposes of precisely determining the resistivity of the tunnelling layer, without being limited by the metal electrode performance.

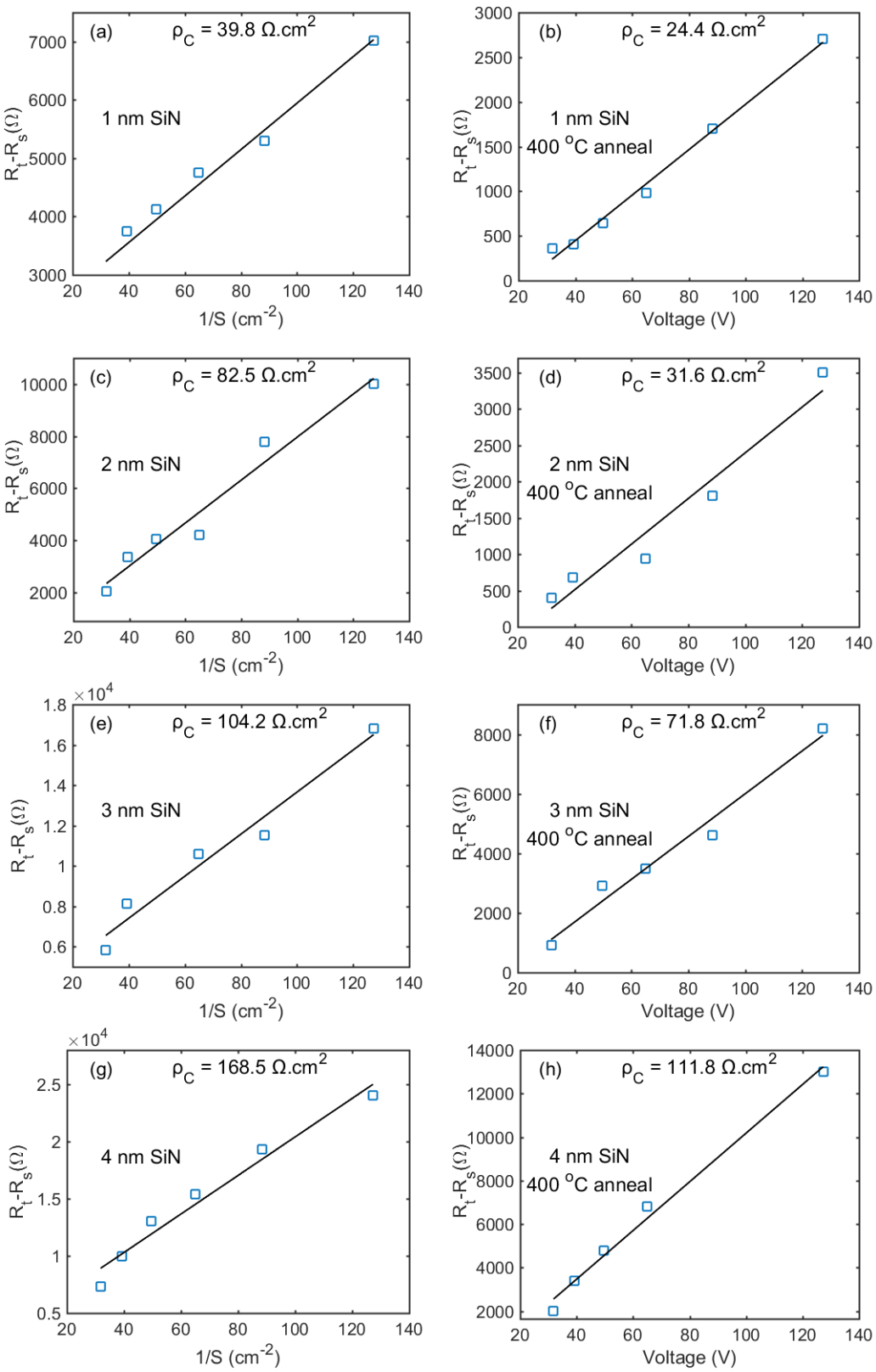

Figure 64: R_T - R_S versus 1/S plots and the corresponding linear fits for extracting ρ_c from Al/SiN/Si/Al structures. As deposited: (a) 1 nm SiN, (c) 2 nm SiN, (e) 3 nm SiN and (g) 4 nm SiN. Annealed at 400 ºC for 1 minute: (b) 1 nm SiN, (d) 2 nm SiN, (f) 3 nm SiN and (h) 4 nm SiN.

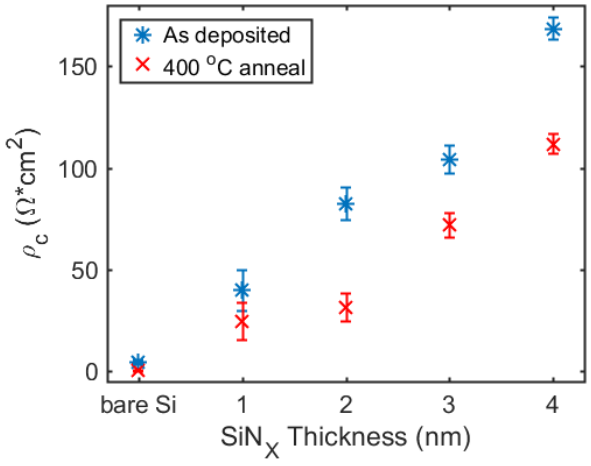

Figure 65: Dependence of ρ_c of the Al-SiN-Si contacts on the thickness of the SiN tunnelling layer for thicknesses between 1 nm – 4 nm.

7.2.4 Limitations of Al for hole contacts

When considering the formation of Ohmic or Schottky contacts, it is useful to consider the energy band diagrams at the metal-silicon interface. If a metal and semiconductor are taken from electrical isolation to being in contact at thermal equilibrium, the metal work function, ϕ_m, aligns with the semiconductor Fermi level, which in other words is the semiconductor work function (ϕ_s). Due to this shift in energy levels, the bands bend at the interface in favour of this transition. When ϕ_m is greater than ϕ_s, the energy bands at the interface bend upwards and vice versa. This is depicted is Figure 66(a) and 66(b), which show the energy bands for a metal and p-type silicon substrate under electrical isolation and thermal equilibrium (when $\phi_m > \phi_s$), respectively.

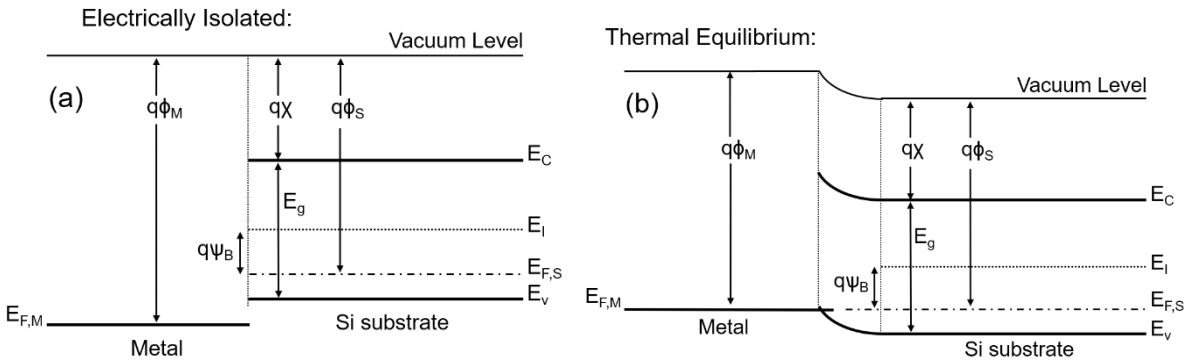

Figure 66: Energy band diagrams for metal-Si interface under (a) electrical isolation and (b) thermal equilibrium.

For a p-type semiconductor, where holes are the majority carriers, the energy bands at interface bending upwards is favourable no Schottky barrier is formed against hole transport. This leads to the accumulation of holes at the interface. Furthermore, an abrupt barrier against electron transport from semiconductor to metal forms under this regime. Consequently, for a hole-selective contact structure, we require ϕ_m to be greater than ϕ_s. To cater for this, ϕ_s must be determined. We refer to Figure 66 for further appreciation for this calculation. The vacuum energy level is our reference point (i.e. E_{vacuum} = 0 eV). The semiconductor Fermi energy level, $E_{F,S}$ (in other words $q\phi_s$), can be determined as:

$$E_{F,S} = q\chi + \frac{E_g}{2} + q\psi_B \tag{32}$$

where χ and E_g are the electron affinity and band-gap of the silicon semiconductor and ψ_B is the potential difference between $E_{F,S}$ and the intrinsic Fermi level, E_I, of silicon. For a p-type semiconductor, ψ_B is determined as:

$$\psi_B = \frac{kT}{q}\ln\left(\frac{p}{n_i}\right) \tag{33}$$

where p is the majority (hole) carrier concentration and n_i is the intrinsic carrier concentration. Using a Boron (acceptor) doping concentration of 10^{15} cm^{-3} and n_i for silicon as 9.65 x 10^9 cm^{-3}, $q\psi_B$ is calculated as 0.297 eV. With a known band-gap of 1.12 eV and electron affinity of 4.05 eV for silicon, we can calculate $E_{F,S}$ as 4.91 eV for a p-type semiconductor with an acceptor concentration of 10^{15} cm^{-3}. Therefore, ϕ_m needs to be greater than 4.91 eV for Ohmic contact formation on this p-type silicon substrate. The case where a thin dielectric is interfaced between the metal and silicon substrate must also be considered. Figure 67 illustrates the energy bands at the metal-dielectric-Si interface. This is represented at flatband condition, which is referred from gate applications in transistors. The alignment of ϕ_m with $E_{F,S}$ still occurs under thermal equilibrium and hence the band bending phenomena discussed for the metal-silicon interface will still exist in this case. Hence, it is still favourable to achieve $\phi_m > \phi_s$.

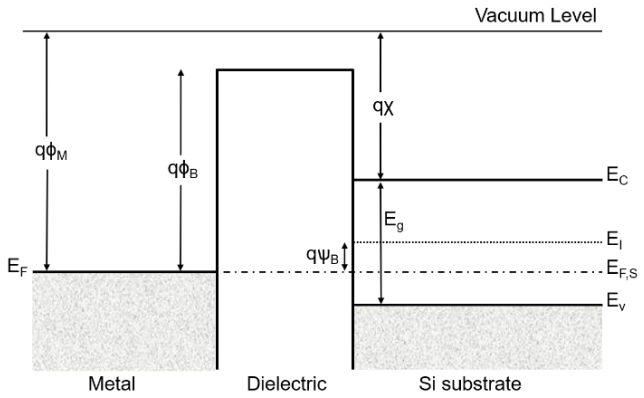

Figure 67: Energy band diagram for metal-dielectric-silicon interface at flatband condition.

The work function of Al is known to be between 4.06 - 4.26 eV [161]. This explains why the as-deposited Al-Si structures were not Ohmic. In general, contacting Si using Al inherently introduces some issues to semiconductor devices. The potential barrier heights at the Al-Si interface are highly sensitive to the interfacial properties, i.e. the Si surface pre-deposition and the metal evaporation conditions. In addition, this can be significantly altered by heat treatment below the Al-Si eutectic temperature due to the dissolution of Si to Al and recrystallisation that occurs at this interface. An alternative metal which is highly conductive, possesses a larger work function (that exceeds ϕ_s) between 5.10 eV and 5.47 eV and that can be easily evaporated on silicon is gold (Au) [161]. Using Au instead of Al can help to mitigate the limiting resistance from the Schottky rear contact when analysing the conductance and specific contact resistivity using our ultrathin dielectrics. In addition, achieving Ohmic contacts by just evaporating metal on silicon is favourable as we can avoid any heat treatment that can interfere with the dielectric resistivity.

7.3 Contact resistivity using Au

7.3.1 Au/p-Si contact resistivity

We fabricate Au/Si/Au structures that possess circular Au electrodes with varying diameters between 1 mm and 2 mm at the front, as well as full-area rear electrodes. The fabrication process from Section 7.2.1 is followed. The current-voltage characteristics are displayed in Figure 68(a). By using the CSM model, we extract the contact resistivity of the as-deposited Au-Si contacts from the $R_T - R_S$ versus 1/S plot, as presented in Figure 68(b).

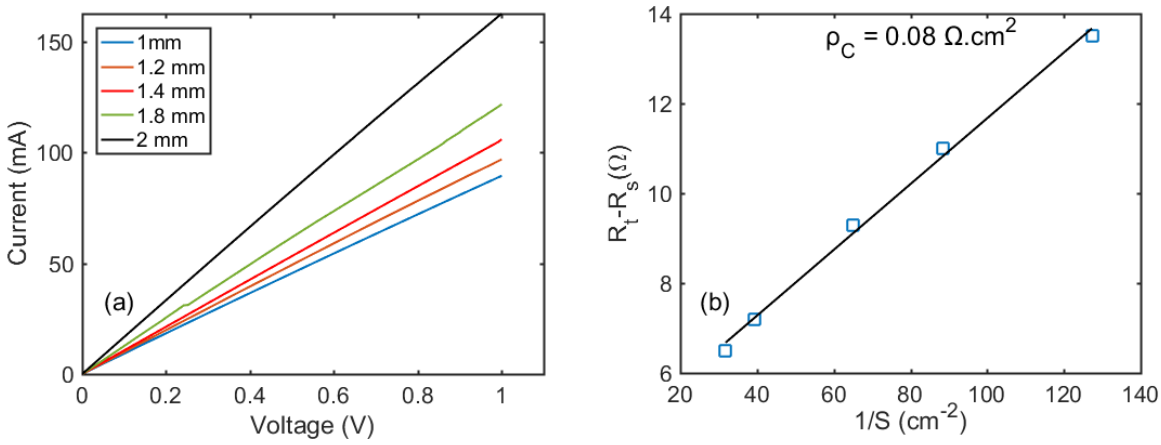

Figure 68: (a) Current-voltage characteristics taken from Au/Si/Au structures, and (b) R_T - R_S versus 1/S and the corresponding linear fit for extracting ρ_c.

The current-voltage characteristics using Au electrodes show Ohmic behaviour in Figure 68(a). This is achieved without any post deposition heat treatment, which is considered highly beneficial both in terms of performance and thermal budget. The contact resistivity being as low as 0.08 Ω.cm^2 demonstrates the high passage of current from Si bulk to Au electrode in these contacts. Despite the considerably low contact resistivity, other factors such as the density of trap states at this interface, which significantly impacts the carrier lifetime in this region of the device, should also be considered. Adding a dielectric layer can aid the reduction of the defect density at the metal-Si interface, as well as support carrier tunnelling, as discussed in previous sections. We now investigate the effects of adding an ultrathin SiN tunnelling layer to these contacts.

7.3.2 Au/SiN/p-Si contact resistivity

To study the resistivity of Au-SiN-Si contacts, we fabricate Au/SiN/Si/Au structures with the CSM electrode pattern, similar to the preceding section. The current-voltage characteristics are measured from our fabricated contacts using a Keithley source meter set-up. Figure 69(a) illustrates the fabricated CSM structures for this study. The impact of the SiN layer thickness on these contacts is measured by varying thickness between 1 nm and 4 nm. Examples of the current-voltage characteristics and $R_T - R_S$ versus 1/s plots from this study, showing the 2 nm SiN structure characteristics, are displayed in Figure 69(b) and 69(c) respectively. The dependency of the specific contact resistivity of these contacts on the SiN thickness found in this study is presented in Figure 69(d).

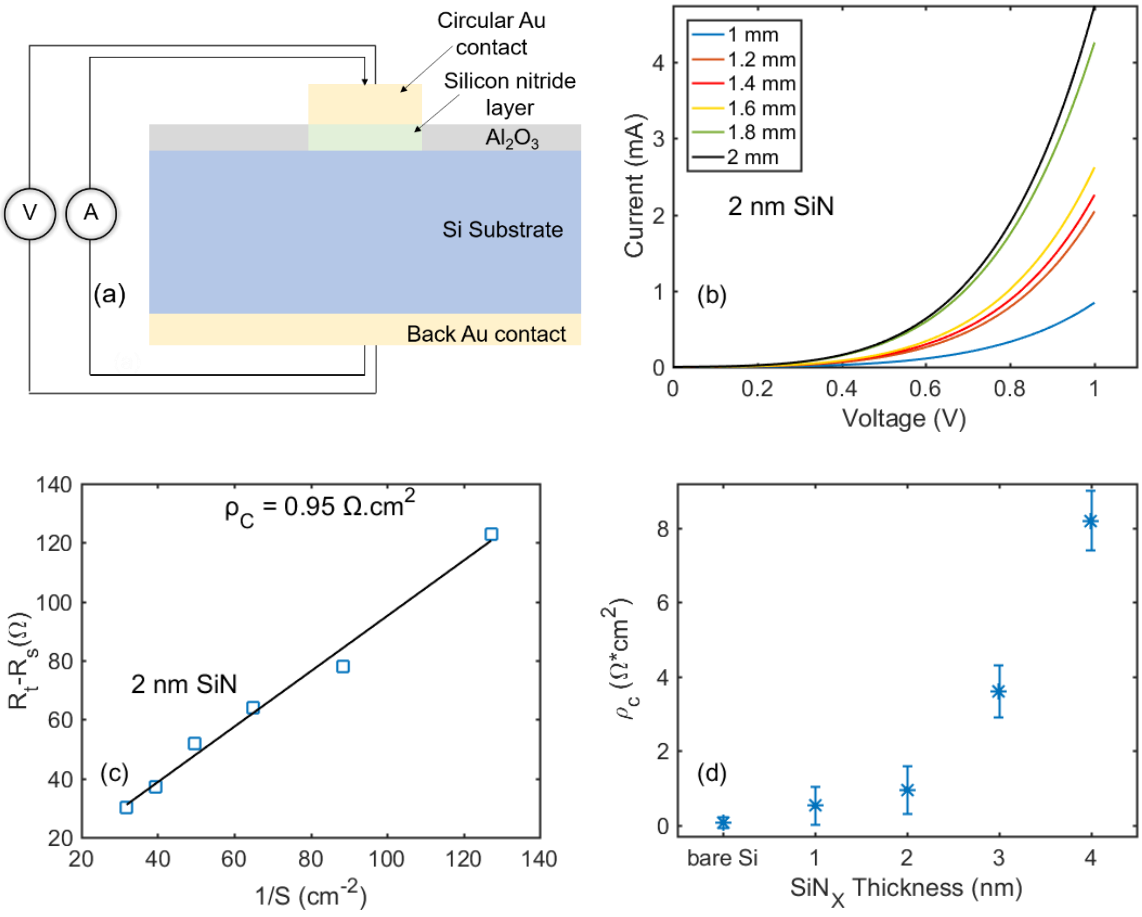

Figure 69:(a) Cross-sectional diagram of fabricated Au/SiN/Si/Au for CSM measurements, (b) current-voltage characteristics from 2 nm SiN thickness structure, (c) R_T – R_S vs 1/s from 2 nm SiN thickness CSM structure and (d) dependency of ρ_C on SiN thickness.

Overall, a considerably lower contact resistivity is achieved by using Au electrodes, without requiring any post-deposition heat treatment. Using a SiN thickness of 1 nm, ρ_c as low as 0.52 Ω.cm^2 is achieved. This was found to increase up to 0.95 Ω.cm^2, 3.6 Ω.cm^2 and 8.2 Ω.cm^2 when using a SiN layer thickness of 2 nm, 3 nm and 4 nm respectively. The general trend between increasing dielectric layer thickness resulting in a higher ρ_c in this type of contact is re-emphasized. Despite the significant improvement in ρ_c, the current-voltage characteristics of the Au-SiN-Si contacts are found to be non-Ohmic. Our work on Au-Si contacts in the preceding section eliminates the possibility of Schottky at the rear (Si-Au side in Figure 69(a)). Hence, we can conclude that the Schottky barrier has formed at the front junction.

To promote carrier-selectivity and avoid Schottky barrier formation, multiple mechanisms can be introduced in carrier-selective contacts. Firstly, using a dielectric tunnelling layer, that when interfaced with silicon, can achieve favourable band alignments which can promote majority

carrier transport from the substrate to the external circuit. This was studied in the preceding chapter on hole-selectivity of ultrathin ALD SiN. Another way is to use a large work function metal that exceeds the work function of the silicon substrate, promoting upwards band bending (as discussed in Section 7.2.4). Despite the existence of these two traits in our structures, the surface carrier concentration needs to be modulated further to promote hole transport. This can be achieved using a material with a charge modulation layer in between the metal electrode and SiN tunnelling layer, as typically done for TOPCon that use an SiO_2 tunnelling layer. The work done on p^+ polycrystalline silicon growth using HWCVD showed highly promising characteristics that could suit this application. Other methods, including what is typically used for polycrystalline silicon grown in TOPCon, are Plasma-enhanced CVD and Low-pressure CVD. In addition to the p^+ silicon layer, the hole tunnelling probability needs to be determined so that the optimum thickness of the ultrathin layer for these contacts can be identified.

7.4 Silicon nitride nanolayers as hole selective contacts

7.4.1 SiN electron hole tunnelling probability

Thin film passivating layers for carrier selective contacts are dependent on current transport through what would classically be considered insulators. Whilst there is debate on the exact nature of current transport through dielectric structures, it is generally accepted that, at least for oxide layers <2 nm, carrier tunnelling plays a significant role [162]–[164]. Using the Wentzel-Kramers-Brillouin (WKB) approximation, the tunnelling probability of carriers is shown to be strongly dependent on the barrier height ($\Delta\phi_b$ given in eV), effective mass, m^*, and the dielectric thickness, t. This dependency is described by Equation 34 [165] for the carrier tunnelling probability, P_t:

$$P_t = \exp\left(-\frac{2}{\hbar} t\sqrt{2\, m^*_e q\, \Delta\phi_b}\right) \quad (34)$$

The intrinsic carrier selectivity of the dielectric, S_h, can be calculated as the ratio of the tunnelling probability of electrons to the tunnelling probability of holes [166]:

$$S_h = {P_{t,h}}\Big/{P_{t,e}} \quad (35)$$

The tunnelling probability of ALD SiN films are compared with SiO_2 from typical TOPCon passivating contact structures in literature. To calculate the tunnelling probabilities in SiO_2, the conduction band barrier ΔE_C is set to 3.2 eV, while the valence band barrier ΔE_V is 4.5 eV [72]. The effective masses for electrons and holes are set to 0.5 and 0.77 respectively [72]. The band

alignment found in the preceding chapter is used for the SiN, with ΔE_C =1.77 eV, and ΔE_V =1.09 eV. For SiN, the electron and hole effective masses are both set to 0.5 [167]. The band offset values are visualised in Figure 70(a), highlighting the smaller bandgap of ALD SiN compared to SiO_2, and the band alignment of the dielectric in relation to a silicon base. Figure 70(b) compares the tunnelling probability and selectivity of SiO_2 and (as deposited) SiN.

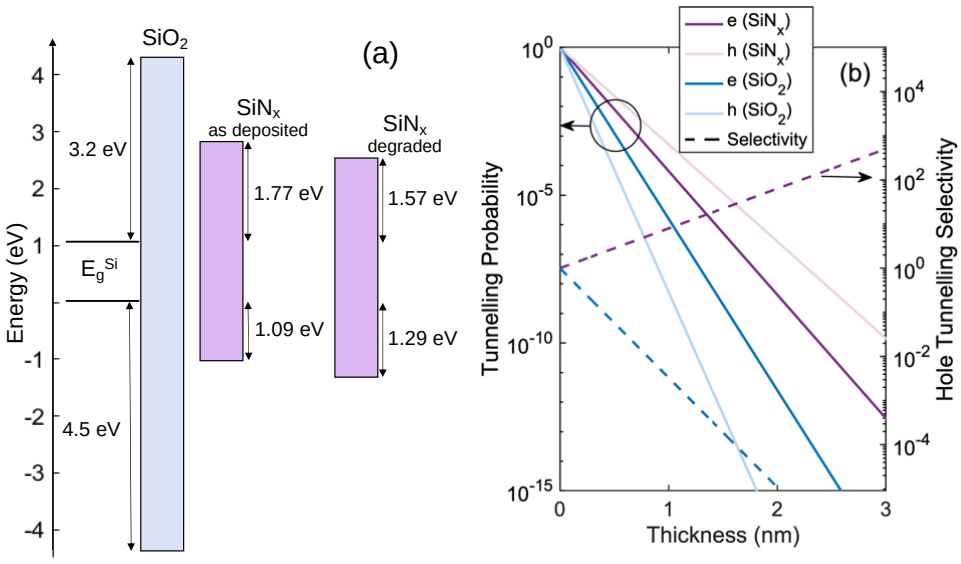

Figure 70: (a) Measured ΔE_C and ΔE_V of ALD SiN compared to that for SiO_2, and (b) tunnelling probability and tunnelling selectivity of ALD SiN and SiO_2.

The SiN has larger tunnelling probabilities at all thicknesses due to the smaller offsets, and it clearly favours hole tunnelling as opposed to the electron selective SiO_2. For a hole tunnelling probability of 10^{-5}, a SiN layer of ~1.5 nm is required, equating to 22 times more hole tunnelling than electron tunnelling. A similar hole tunnelling probability would require a 0.7 nm SiO_2 layer, which exhibits ~15 times as much electron to hole tunnelling. This highlights the benefits of SiN_x for hole selective contacts. We now look at elucidating the effect that tunnelling probability has in the current transfer dynamics across our dielectric tunnelling layers.

7.4.2 Tunnelling current via Sentaurus TCAD

Sentaurus TCAD is used to simulate the current flow across our ALD SiN nanolayers in an operating device. In this study, comparisons of the SiN selective contacts with with the SiO_2 nanolayer based contacts in TOPCon solar cells are continued. A cross-sectional schematic of the structure used in these simulations is presented in Figure 71. A p-type polycrystalline Si layer is included to modulate the surface carrier concentration, similar to how TOPCon is typically fabricated. The wafer resistivity is set to 1 Ω.cm, the poly-Si doping density to 6 ×

10^{19} cm^{-3}, and a diffusion of Boron acceptors is set at the surface of the wafer with a 0.15 µm depth factor using a Gaussian profile. Tunnelling across the dielectrics was simulated using Sentaurus' Nonlocal tunnelling model that implements Schenk and Heiser's approach [168], with the extensions in [169], [170]. Mobility was modelled using Klaassen's mobility model [171], while Schenk's low injection model was used for band gap narrowing [172].

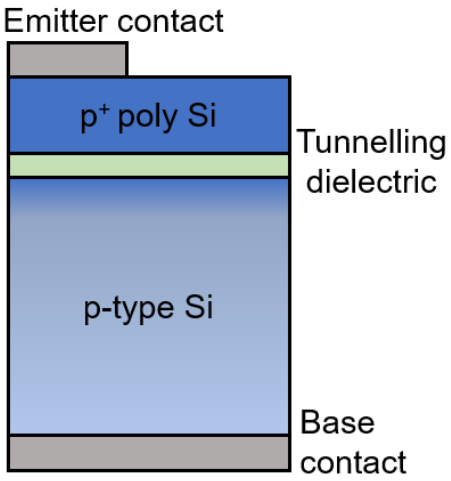

Figure 71: Schematic of structure used for tunnelling current simulations via Sentaurus TCAD.

Figures 72(a) and 72(b) compare the tunnelling current for selected thicknesses of SiN and SiO_2 respectively. The curves show that the SiN current remains limited by resistivity in the rest of the structure until larger thicknesses, compared to the p-type SiO_2. Devices using SiO_2 in a hole selective layer typically use a thickness of ~1.4 nm [17], [26]. In comparison, a SiN layer can be ~3.5 nm thick and achieve the same tunnelling current. This highlights a key advantage of SiN as the film thickness does not require as rigorous control as for SiO_2. For SiN and SiO_2 films of equivalent thickness, hole current densities are at least ten times higher in SiN. Furthermore, having the ability to possess a thicker dielectric when using SiN can aid the performance of these contacts by improving the passivation quality at the contact interface further.

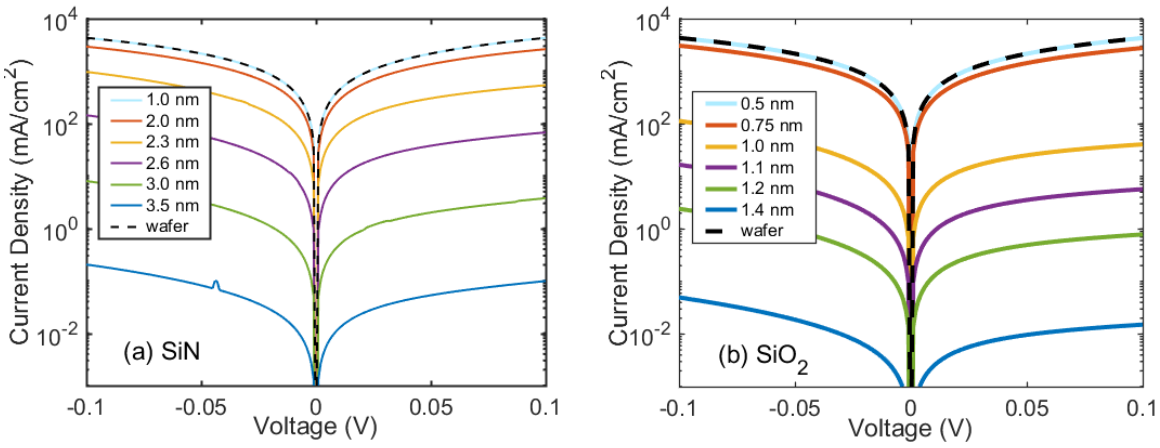

Figure 72: Tunnelling current of (a) ALD SiN and (b) SiO_2.

From Figures 70(b) and 72(a), it is evident that the favourable band alignment of SiN translates into high hole tunnelling current and high selectivity in the contact structures. Using ALD to deposit SiN gives extremely accurate control of thicknesses, allowing the structures to be tailored to maximise the selectivity, whilst maintaining sufficient current. The addition of a p^+ polycrystalline silicon layer is found to further promote the passage of current. This is understood to be due to the modulation of the carrier concentration at the surface further supporting selectivity towards hole transport.

7.5 Conclusion

In this chapter, the specific contact resistivity of ALD SiN nanolayers was studied. Improvements in contact quality are seen when using Au rather than Al for p-type contacts due to the larger work function of Au, with contact resistivity as low as 0.08 $\Omega.cm^2$ for Au-Si contacts. However, the high cost and adhesion issues of Au on Si make this option not viable and other metals/alloys ought to be investigated. The formation of Au-SiN-Si contacts were found to have a resistivity between 0.52 $\Omega.cm^2$ and 8.2 $\Omega.cm^2$ for SiN layer thicknesses between 1 nm and 4 nm. For a hole tunnelling probability of 10^{-5}, a SiN layer of ~1.5 nm is found to be required, equating to 22 times more hole tunnelling than electron tunnelling. Furthermore, based on TCAD simulations, a SiN layer with a thickness of 3.5 nm is found to achieve the same tunnelling current as an SiO_2 layer with a thickness of 1.4 nm in TOPCon. Hole current densities are at least ten times higher in SiN for SiN and SiO_2 films of equivalent thicknesses.

7.6 Contributions

In this work, Shona McNab and Sebastian Ruy Bonilla aided the tunnelling probability and Sentaurus TCAD study. Some of the results in this chapter have been published [151] and parts of the text have been included verbatim.

Chapter 8

Conclusion and Outlook

8.1 Key findings

In this thesis, work is presented on forming hole-selective passivating contacts using ultrathin silicon nitride as a hole-tunnelling layer. To begin with, a HWCVD process for growing boron-doped silicon films as an alternative method for conductive layer and emitter formation in silicon solar cells was studied. Adding a thin tunnelling dielectric was then investigated to promote hole transport and reduce the density of defect states at the bulk silicon boundary. The optoelectronic properties of atomic layer deposition (ALD) grown SiN nanolayers were studied to determine the band offsets at the SiN/Si interface. Finally, contact formation was explored using ALD grown SiN nanolayers with direct comparisons in performance with the industry standard tunnelling oxide passivating contact (TOPCon). The key findings of the project can be summarised as follows:

In **chapter 5**, a new tungsten filament array was implemented in a HWCVD chamber and used to optimise the growth of ex-situ doped p-type silicon films. The altered filament configuration (AFC) achieves a deposition temperature increase from 498 ^{o}C to 535 ^{o}C when compared to the conventional configuration. This translated to an improved polycrystalline nature of the boron-doped silicon films grown, which exhibited larger crystals and a less-defective interface after a sharp post-deposition anneal. Using the HWCVD growth recipe, p^{+} properties with a uniform doping profile in the 10^{21} cm^{-3} region were obtained and an enhanced current rectification factor of an order of magnitude was achieved by performing a short post-deposition anneal at 800 ^{o}C. The results suggest that the addition of an ultrathin layer between the deposited silicon and the substrate to passivate the interface whilst promoting the passage of holes could be beneficial in moving towards the goal of producing an effective hole-selective contact.

In **chapter 6**, an ALD process for growing SiN nanolayers to act as the tunnelling layer in hole-selective passivating contacts was developed. Angstrom-scale growth of SiN films was achieved, with a chemical compositional ratio of 1:1 between Si and N and an optical band-gap of 3.98 ± 0.04 eV. This represents the first experimental report of the energy band alignments at the SiN/Si interface using a photoemission-based method, showing a band offset ratio ($\Delta E_C/\Delta E_V$) of 1.62 ± 0.24 that suggests favourability towards hole transport. Undesirably, it was found that these nanolayers degrade during the first 48 hours after growth, with a higher oxygen content, increase in thickness (between 0.2 nm and 0.5 nm) and a lower $\Delta E_C/\Delta E_V$ value of 1.22 ± 0.18. Hole-selectivity is still considered to be favourable after degradation from the altered band offsets and work then moved towards contact formation using these nanolayers.

In **chapter 7**, the contact resistivity of SiN/Si with Al and Au electrodes was studied. Due to the larger work function of Au, improved results were seen when using this metal rather than with Al. Ohmic contacts to p-type silicon, with resistivity as low as 0.08 $\Omega.cm^2$ were formed using Au. Adding a SiN tunnelling layer increased the specific contact resistivity to between 0.52 $\Omega.cm^2$ and 8.2 $\Omega.cm^2$ for SiN thicknesses between 1 nm and 4 nm. Using Sentaurus TCAD, the hole current densities were determined to be at least ten times higher in SiN for SiN and SiO_2 films of equivalent thicknesses. The tunnelling current achieved when using an SiO_2 layer with a thickness of 1.4 nm (which is conventional used for TOPCon) is equally achieved using a SiN layer as thick as 3.5 nm, showing that the film thickness does not require as rigorous control as for SiO_2. It was also found that adding a p^+ polycrystalline silicon layer between the metal and SiN layer aids carrier transport by modulating the concentration of carriers at this boundary. The next step towards forming hole-selective passivating contacts with ALD grown SiN nanolayers is to enhance the surface passivation ability of this nanolayer on silicon to reduce the flux of non-collected negatively charge carriers in the contact.

These findings contribute to the field of PV due to the recent shift in the industry towards passivating contacts technology. An on-going need for an efficient hole-selective passivating contact currently exists in this field and the use of industry-compatible silicon nitride is highly attractive to serve this purpose. The suitable optoelectronic properties of this material naturally provide great flexibility in cell architectures. This includes potential incorporation in tandem cell configurations (where control over the top surface optics of the silicon solar cell is of high interest), and in bifacial designs that couple in light from both sides of the absorber. At this stage, there is a common belief in the PV industry that placing both (electron- and hole-selective) passivating contacts at the rear-side of the device in an interdigitated back-contact

(IBC) configuration is the ultimate design for high performance silicon solar cells. The findings in this work support the notion that the combination of a ALD grown SiN hole tunnelling layer and a HWCVD grown p^+ polycrystalline silicon layer could serve as the hole-selective passivating contact in a high-performance IBC cell configuration.

8.2 Research Outlook

To further the impact of this work, the next step should be to study and enhance the silicon surface passivation of ALD grown SiN nanolayers. A brief description of potential routes towards this, with some preliminary results, are discussed in this section.

8.2.1 Silicon surface passivation using SiN nanolayers

Achieving superior silicon surface passivation using ALD grown SiN nanolayers is crucial towards forming high performance passivating contacts. A high dark saturation current at the SiN/Si interface translates as large minority carrier flow in this region of the device, which promotes Shockley-Read-Hall recombination at this boundary. For this reason, it is imperative to mitigate this phenomenon in PV devices. Commonly, silicon nitride grown via PECVD is reported to have a density of interface states as low as 10^{11} cm^{-2} and a recombination velocity lower than 1 cm s^{-1} [141], [173]. Silicon surface passivation using this material also relies on the field-effect passivation due to the fixed positive charges within this dielectric. However, no report exists on whether these charges form during processing or on their potential to cause inversion in ultrathin layers [93], [174]. Furthermore, the low density of defect states may not be achievable at ultra-low thicknesses. Nonetheless, one way to overcome the Shockley-Read-Hall recombination is to neutralize each defective bond with the addition of a hydrogen atom, namely performing a hydrogenation step [175].

Hydrogenation treatments for PV technology are typically performed either by forming gas annealing (FGA) in a mixture of H_2 and inert gas [176], [177], rapid hydrogen plasma processing (RPHP) [93] or by depositing hydrogen-rich capping layers and annealing them in N_2 or FGA [43], [178]. Hydrogenation of ultrathin layers is challenging without the addition of capping layers, with results in literature showing little improvements in performance from using only FGA or RPHP [175]. Conversely, when capping layers and post-deposition heat-treatments are applied, passivating contacts performance are reported to improve significantly [175], [179], [180]. Using a Quasi-steady state photoconductance (QSSPC) decay method, we take preliminary effective minority carrier lifetime (τ_{eff}) measurements from a p-type silicon

substrate coated with 3.5 nm SiN grown via ALD on both sides. Figure 73 shows the τ_{eff} from as-deposited and FGA and RPHP treated specimen.

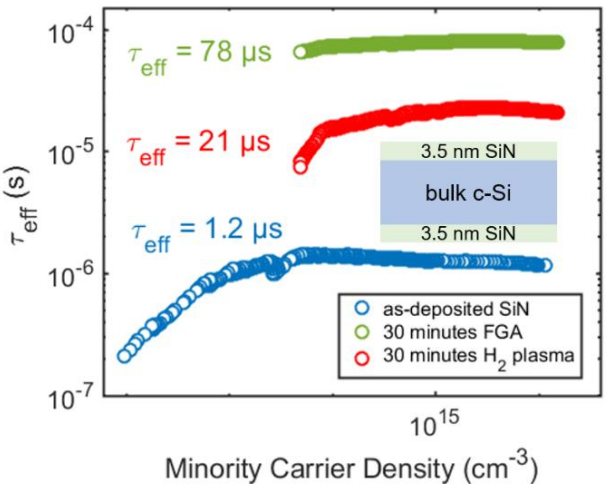

Figure 73: Minority carrier density as a function of effective carrier lifetime from SiN/Si/SiN structures, measured as deposited, after rapid plasma hydrogen passivation and forming gas annealing.

The highest τ_{eff} of 78 µs is measured from the RPHP sample, with some improvements also seen after FGA that show a τ_{eff} of 21 µs. Nonetheless, these τ_{eff} values are too low to achieve any worthy performance in a contact. As stated earlier, a hydrogen-rich capping layer is required to increase the concentration of H atoms that can diffuse to the SiN layer. Furthermore, the effusion of hydrogen out of this structure must also be mitigated. A study that can potentially pave the way towards reducing the density of defect states and ultimately improve τ_{eff} further is described in Figure 74. The poly-Si layer grown on the ultrathin SiN layer must be hydrogen-rich. In other words, a higher hydrogen concentration must be used during the poly-Si growth. This could easily be achieved using HWCVD. An additional Al_2O_3 layer, which can be deposited via ALD, should also be studied as a hydrogen effusion barrier. From each structure shown in Figure 74, QSSPC, micro-photoluminescence (µ-PL) and Transmission electron microscopy (TEM) can be used to effectively measure the performance via metrics that include τ_{eff}, implied open-circuit voltage (i-V_{OC}) and the morphology before and after heat-treatment. Furthermore, the effect of FGA and RPHP treatments should also be studied after forming each structure and compared with the as-deposited cases.

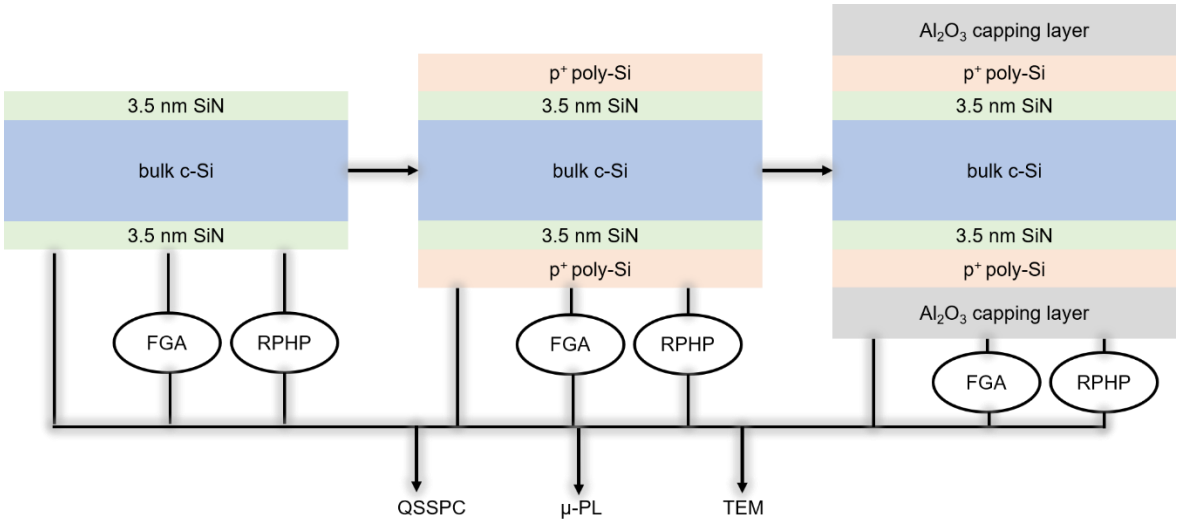

Figure 74: Schematic diagram showing various passivation stacks to promote hydrogenation in SiN nanolayer and possible measurements identified to determine performance in a passivating contact configuration.

From a recent study by Truong et al. [175] on the hydrogenation of poly-Si/SiO_x passivating contacts, significant improvements were seen from using hydrogen-rich aluminium oxide (AlO_x:H) and silicon nitride (SiN_x:H) on the τ_{eff} and i-V_{OC} of their devices. This is presented in Figure 75, which shows the τ_{eff} and i-V_{OC} from their samples before and after various hydrogenation methods. The as-deposited and only FGA treated samples were found to have low τ_{eff} values in the microsecond range. However, after adding AlO_x:H and SiN_x:H capping layers and conducting FGA, significant improvements were seen of at least an order of magnitude in τ_{eff}. The best performance was found after adding a SiN_x:H capping layer and FGA, with a remarkable τ_{eff} of 12 ms and i-V_{OC} of 0.73 V. This signifies the importance of this passivation study for our hole-selective contacts as careful consideration in hydrogenation treatments can evidently provide major improvements in device performance.

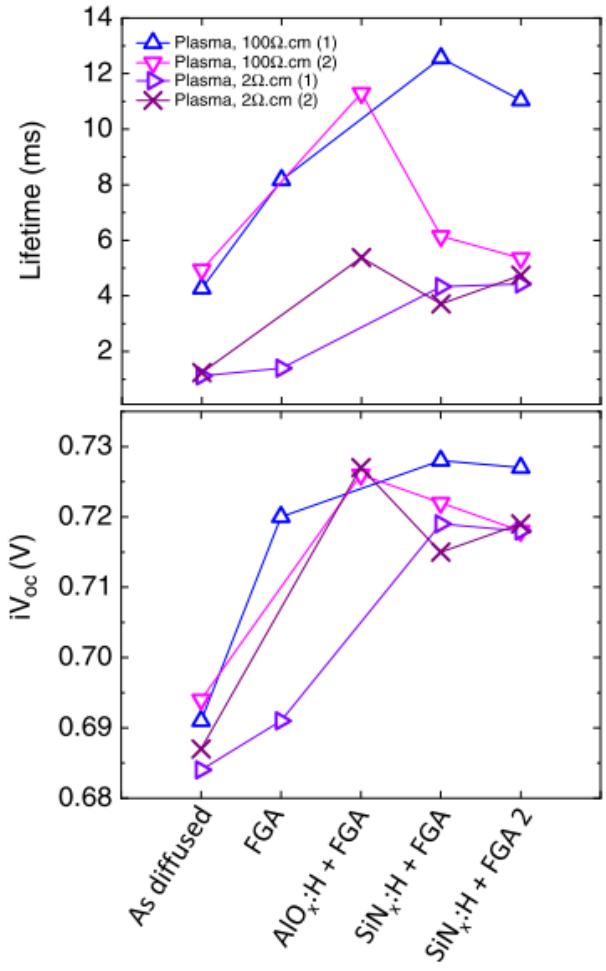

Figure 75: Implied open-circuit voltage and minority carrier lifetime from samples before and after FGA and capping layer formation taken from plasma-assisted ALD deposition from [175].

8.2.2 IBC silicon solar cell with SiN hole-selective contacts

In the PV industry, the interdigitated back-contact design is currently the leading single-junction solar cell architecture, with the record power conversion efficiency (PCE) at 26.7 % [15], [16]. The current record-holding cell uses hydrogenated intrinsic amorphous silicon (a-Si:H) as a thin passivating layer, and p-type and n-type a-Si:H layers are used as conductive transport layers in an interdigitated format at the rear of the cell. Despite the remarkable performance from this architecture, some inherent issues with these a-Si:H contacts exists and must be addressed. Firstly, the thermal stability of amorphous silicon is too low for industrial applications. During high-temperature processing (after contact formation), these a-Si:H layers will crystallize and their optoelectronic properties will change significantly. Examples of high-temperature processes that could follow the a-Si:H growth in this cell architecture include the

electrode formation step and encapsulation of the solar cell. In addition, there are parasitic absorption losses associated with a-Si:H, as the optical band-gap of a-Si:H is generally reported between 1.7 – 1.9 eV [139].

We propose an IBC silicon solar cell that uses SiN and SiO_2 tunnelling layers for hole and electron selective contacts, respectively. Figure 76 shows a cross-sectional diagram of the proposed cell design. This includes interdigitated SiN and SiO_2 layers with thicknesses of 3.5 nm and 1.4 nm respectively, grown on a n-type FZ Si substrate. The dielectric thicknesses are taken from our tunnelling current study, but further optimisation would be required based on the findings from the passivation study. Both SiN and SiO_2 can be deposited via ALD for this process. A p-type and n-type poly-Si layer, grown via HWCVD, is deposited on the SiN and SiO_2 layers respectively. Note that separate HWCVD chambers would be required for this process, as cross-contamination of boron and phosphorous dopants in the poly-Si layers can be detrimental effects to cell performance. The metal electrode is then deposited on the poly-Si layers, completing the rear side of the cell. At the front of the solar cell, a thin SiN layer is applied, serving as a passivating and anti-reflection coating (ARC).

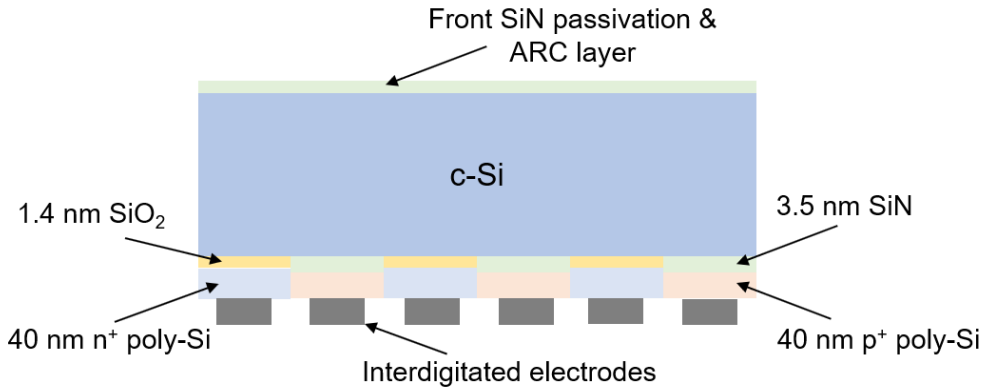

Figure 76: Cross-sectional schematic diagram of IBC solar cell with SiN hole tunnelling contacts.

The absence of any contacts on the front side of this cell provides flexibility towards implementation in tandem configurations that can exceed the single junction solar cell power conversion efficiency limit [18]. The use of high-performance carrier-selective contacts could break current PCE barriers by forming a heterojunction cell. Ultimately, this cell architecture opens multiple new avenues of research that can be followed for increasing the impact from this work.

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Appendix

9.1 Quokka (MATLAB) solar cell models

The Quokka (MATLAB) models for IBC and HTJ silicon solar cells are based on solar cells from literature [33], [71]. The MATLAB scripts for these cells are provided in this appendix.

9.1.1 IBC silicon solar cell

```
version.design='IBC';

% bulk properties
bulk.type='n-type';
bulk.taubfixed=1e20;
bulk.rho=1.5;
bulk.SRH.midgap.taup0=3000;
bulk.SRH.midgap.taun0=3000;

% bulk conditions
bulk.nk='Green08_300K';
bulk.Auger='Richter2012';
bulk.mobility='Klaassen';
bulk.nieff='fixed';
bulk.T=298.15;
bulk.nieffvalue=8.27e9;
bulk.Brad=4.73e-15;

% unit cell geometry
geom.dimensions=3;
geom.Wz=230;
geom.Wx=250;
geom.Wy=35;
geom.leftcont.shape='rectangle';
geom.leftcont.wx=3;
geom.leftcont.wy=3;
geom.leftcont.pitchx=70;
geom.leftcont.numberx=1.5;
geom.leftcont.w_metal=140;
geom.rightcont.shape='rectangle';
geom.rightcont.wx=3;
geom.rightcont.wy=3;
geom.rightcont.pitchx=70;
geom.rightcont.numberx=0.5;
geom.rightcont.w_metal=65;
geom.leftcont.y_position='aligned';
geom.meshquality=1;
```

```
% Boundary properties

% passivated and undiffused rear recombination
bound.nonconduct{1}.location='rear';
bound.nonconduct{1}.noncont.rec='J0';
bound.nonconduct{1}.noncont.J0=19.5e-15;

% passivated and undiffused front recombination
bound.nonconduct{2}.location='front';
bound.nonconduct{2}.noncont.rec='J0';
bound.nonconduct{2}.noncont.J0=4.6e-15;


% right localized conductive boundary - n+ diffusion
bound.conduct{2}.location='right';
bound.conduct{2}.Rsheet=35;
bound.conduct{2}.cont.rec='J0';
bound.conduct{2}.cont.J0=202e-15;
bound.conduct{2}.cont.rc=1.2e-5;
bound.conduct{2}.noncont.rec='J0';
bound.conduct{2}.noncont.J0=176e-15;
bound.conduct{2}.wx=11.9;
bound.conduct{2}.wy=11.9;
bound.conduct{2}.shape='rectangle';
bound.conduct{2}.jctdepth=1.5;
bound.conduct{2}.colleff=0.87;

% large area left conductive boundary - p+ diffusion
bound.conduct{1}.location='left';
bound.conduct{1}.Rsheet=166;
bound.conduct{1}.cont.rec='J0';
bound.conduct{1}.cont.J0=1234e-15;
bound.conduct{1}.cont.rc=2e-5;
bound.conduct{1}.noncont.rec='J0';
bound.conduct{1}.noncont.J0=33.2e-15;
bound.conduct{1}.shape='line';
bound.conduct{1}.wx=165;
bound.conduct{1}.jctdepth=0.5;
bound.conduct{1}.colleff=1;

% generation settings
generation.type='1D_model';
generation.suns=1;
generation.illum_side='front';

% model
generation.transmission='ext_file';
generation.transmission_filename='IBC_ANU_Tfront.csv';
generation.Z='ext_file';
generation.Z_filename='IBC_ANU_Z.csv';
generation.spectrum='AM1.5g';
generation.facet_angle=53;

% external circuit
```

```
circuit.Rseries=0.051;
circuit.Rshunt=1e5;
circuit.QE.wavelength_values=[300:20:1200];
circuit.terminal='IV_curve';
```

9.1.2 HTJ silicon solar cell

```
version.design='FRC';

% bulk properties
bulk.type='n-type';
bulk.rho=5;
bulk.taubfixed=1e20;
bulk.SRH.midgap.taup0=15000;
bulk.SRH.midgap.taun0=1000;

% bulk conditions
bulk.Auger='Richter2012';
bulk.nk='Green08_300K';
bulk.mobility='Klaassen';
bulk.nieff='fixed';
bulk.nieffvalue=8.27e9;
bulk.Brad=4.73e-15;
bulk.T=298.15;

% unit cell geometry
geom.dimensions=2;
geom.Wz=150;
geom.Wxfront=840;
geom.Wxrear=840;
geom.frontcont.shape='line';
geom.frontcont.wx=50;
geom.rearcont.shape='full';
geom.meshquality=2;

% Boundary properties

% Injection dependent front recombination and TCO sheet resistance
bound.conduct{1}.location='front';
bound.conduct{1}.Rsheet=150;
bound.conduct{1}.noncont.rec='expr';
bound.conduct{1}.noncont.expr='8.27^2/8.52^2*dn*(const.N+dn)/const.nieff^2*1e-
15*10^(1.367+0.7028*cos(log10(dn))+0.2459*sin(log10(dn))-0.04068*cos(2*log10(dn))-
0.2271*sin(2*log10(dn)))';

bound.conduct{1}.cont.rec='expr';
bound.conduct{1}.cont.expr='8.27^2/8.52^2*dn*(const.N+dn)/const.nieff^2*1e-
15*10^(1.367+0.7028*cos(log10(dn))+0.2459*sin(log10(dn))-0.04068*cos(2*log10(dn))-
0.2271*sin(2*log10(dn)))';

bound.conduct{1}.cont.rc=1e-4; % TCO - metal contact
bound.conduct{1}.shape='full';

% Injection dependent rear recombination
```

```
bound.conduct{2}.location='rear';
bound.conduct{2}.Rsheet=100;
bound.conduct{2}.noncont.rec='expr';
bound.conduct{2}.noncont.expr='8.27^2/8.52^2*dn*(const.N+dn)/const.nieff^2*1e-
15*10^(1.029+0.293*cos(log10(dn)*1.304)-
0.5323*sin(log10(dn)*1.304)+0.01279*cos(2*log10(dn)*1.304)+0.1621*sin(2*log10(dn)*1.30
4))';

bound.conduct{2}.cont.rec='expr';
bound.conduct{2}.cont.expr='8.27^2/8.52^2*dn*(const.N+dn)/const.nieff^2*1e-
15*10^(1.029+0.293*cos(log10(dn)*1.304)-
0.5323*sin(log10(dn)*1.304)+0.01279*cos(2*log10(dn)*1.304)+0.1621*sin(2*log10(dn)*1.30
4))';

bound.conduct{2}.cont.rc=1e-5; % TCO - metal contact
bound.conduct{2}.shape='full';

% generation
generation.type='1D_model';
generation.suns=1;
generation.illum_side='front';
generation.shading_width=55*0.7;
generation.transmission='ext_file';
generation.transmission_filename='HJT_projected_Tfront_bb_scaled.csv';
generation.Z='ext_file';
generation.Z_filename='HJT_projected_Z.csv';
generation.spectrum='AM1.5g';
generation.facet_angle=54.7;


% external circuit
circuit.Rseries=0.239+0.161;
circuit.Rshunt=1e5;
circuit.terminal='light_IV_auto';
circuit.QE.wavelength_values=[300:20:1200];'
circuit.Voc_guess=0.7;
```