Transformation of digital to analog switching in TaOx-based s

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An oxidizable metal diffusion barrier inserted between the active metal electrode and the switching layer decreases the electroforming voltage and enhances the switching stability and synaptic performances in TaOx-based conducting bridge memristor devices. The TiW barrier layer avoids an excessive metal ion diffusion into the switching layer whilst the TiWOx interfacial layer formed between the barrier and switching layer. It modulates the oxygen vacancy distribution at top interface and contributes to the formation and rupture of metal ions-oxygen vacancies hybrid conducting bridge. We observe that the device that relies upon non-hybrid (metal ions only) conducting bridge suffers from the poor analogous performance. Meanwhile, the device made with the barrier layer is capable of 2-bit memory and robust 50 stable epochs. The TaOx also acts as resistance suppressing and thermal enhancement layer, which helps to minimize overshooting current. The enhanced analog device with high linear weight update shows multilevel cell characteristics and stable 50 epochs. To validate the neuromorphic characteristic of the devices, a simulated neural network of 100 synapses is used to recognize 10x10 pixel images.

Keywords: analog devices, CBRAM, memristor, neuromorphic devices.

In recent years, significant efforts have been put into emerging non-volatile memory technologies for future data storage applications, such as phase change, ferroelectric, magnetic, and memristor memories.[1,2] Among these technologies, memristor has shown great potential to replace conventional memory due to its scalability, durability, and compatibility with the conventional complementary metal-oxide-semiconductor framework.[3] Memristor has two major classes, conducting bridge random access memory (CBRAM)[4] and oxygen vacancy random access memory (OxRAM).[5] In CBRAM, metal ions originated from the top electrode diffuses into the switching layer and form a metallic bridge which serves as a conduction path of electrons.[6,7,8] On the other hand, the conduction path in OxRAM is attributed to the formation of oxygen vacancy conducting filament.[9] Nevertheless, the formation of a hybrid conducting bridge consisting of metal atoms and oxygen vacancies was also reported.[10,11] However, most of these reports only focus on the conduction mechanism while the feasibility of this hybrid system to the switching and synaptic performance is still less-understood.

In order to realize memristor-based neuromorphic system, the device should exhibit gradual change in conductance states; the gradual behavior is also termed as analog switching, meanwhile, abrupt change in conductance states is called as digital switching.[12,13] Henceforth, careful engineering in the formation and rupture of conductive filament/bridge to achieve gradual switching is required.[14] Several techniques are recently reported that digital switching can be transformed into analog switching in memristor devices either by using annealing processes, different doping concentrations, or different top electrodes.[15–17] In this work, we demonstrate that such transformation could also be achieved by the employment of a barrier layer(BL) in TaOx-based CBRAM devices. A metal barrier layer is usually used to control the diffusion of active metal ions during the formation and rupture of the conducting bridge in CBRAM devices.[18–20]

Nevertheless, the interfacial engineering to induce analog switching by utilizing a barrier layer (BL) technique is still less explored. The formation of interfacial layer at the bottom interface may help to induce analog behavior in memristor devices.[21] However, in this work, we found that such technique may not sufficient to achieve both analog set and reset. TaOx was employed as a switching layer of the CBRAM device due to its compatibility in CMOS processes.[22–25] However, TaOx-based CBRAM faced several challenges such as non-uniform switching and the requirement of a high forming voltage.[26] This letter reports a suitable TaOx-based CBRAM design to answer these challenges.

A 20-nm-thick TiN bottom electrode (BE) was deposited onto a Pt/Ti/SiO_2/Si substrate by plasma-enhanced atomic layer deposition. The use of a thin layer of Pt benefits to reduce the sheet resistance of TiN electrode. A 10 nm TaOx layer was deposited using RF sputtering technique. The sputtering power, gas flow ratio (Ar/O_2), and working pressure were 100 W, 2/1, and 10 mTorr, respectively. A 100 nm thick Cu top electrode(TE) with 150-μm diameter was patterned using a shadow mask. For making a Cu/TiW/TaOx/TiN stack, a 20 nm thick TiW layer was deposited by DC sputtering. All layers were deposited at room temperature. The device fabricated without the insertion of TiW as a barrier layer is used as reference or control sample and is denoted as Device A while the device made with BL is denoted as Device B. Switching and synaptic characteristics were measured using an Agilent B1500A probe station. A voltage bias was applied at the Cu top electrode and the TiN bottom electrode was kept ground. A compliance current (I_{cc}) during positive bias was used to prevent device breakdown. The film structure of the devices was investigated using a transmission electron microscope (TEM, JEOL 2100FX). The element profile of the film and the oxygen defect distributions of the oxide layers were investigated by X-ray photoelectron spectroscopy (XPS, PHI Quantera SXM).

Figures 1(a) and 1(b) show the I-V curves of Device A and B, respectively. The devices were formed with I_{cc} of 500 uA. It is found that Device A requires 2.1 V to switch the device from pristine state to low resistance state (LRS, ON), meanwhile, Device B only requires 1.1 V. Hereafter, both devices can be switched from the LRS to the high resistance state (HRS, OFF) with a negative bias voltage of -1.2 V (V_{reset}), termed as reset process. The devices can be switched back to the ON state by applying positive bias voltage (V_{set}) of approximately 0.7 V and 0.6 V for Device A and B, respectively, while employing an I_{cc} of 1mA. Device B performs better endurance than Device A by showing stable switching for more than 1000 cycles with an On/Off ratio of 10 times, as depicted in Figs. 1(c) and (d). Retention test was conducted to assess the memory non-volatility of the devices, and the results are indicated in Figs. 1(e) and (f). Device A shows poor retention by exhibiting HRS decay characteristic after 500 sec. at room temperature; conversely, Device B exhibits stable LRS and HRS retention even at 120 ^{o}C for more than 10000s without any degradation. Note that the Device B structure also shows good device-to-device uniformity. This indicates that the Cu/TiW/TaOx/TiN stack is a promising design for the next generation memristor data storage application.

We observe that Device A shows abrupt switching behavior during the set process while gradual switching during the reset process (Fig. 1(a)). On the other hand, Device B exhibits gradual switching for both set and reset processes (Fig. 1(b)). Henceforth, Device B is found to be more appealing as an analog device for neuromorphic applications.[27,28] In order to evaluate its analogous behavior, we performed multilevel cell (MLC) characteristic test, and the result is shown in Fig. 2. Device B is capable of showing 2-bit per cell (00, 01, 10, and 11 states)[13] by controlling the HRS level with various V_{reset} (Fig. 2(a)) or controlling the LRS level with various I_{cc} (Fig. 2(b)). This

result confirms that Device B exhibits excellent analog capability in both set and reset process, which is a promising indication to achieve a highly linear synaptic response.

We further examine synaptic characteristics with electrical pulses to perform potentiation and depression; the pulse scheme used for Potentiation of Device A is of 10 µs pulse width and read amplitude of 0.2 V with a width of 1 ms, as shown in Figure 2(c). For Depression of Device A -1V pulse width is used. Similarly, scheme for potentiation of Device B is of 10 µs pulse width and read amplitude of 0.2 V with a width of 1 ms, as shown in Figure 2(d). For Depression of Device B -1V pulse width is used. For each potentiation and depression cycle, we use 100 and 150 pulses for Device A and Device B, respectively. The potentiation in Device A can only be triggered by a pulse height of as low as 1.4 V, as shown in Fig. 2(c), Device A exhibits abrupt conductance change and it reaches saturation just after few pulses. However, the device can exhibit a gradual decrease of conductance with a pulse height of -1 V. On the other hand, Device B demonstrates stable gradual potentiation and depression employing pulse heights of 1.2 and -1 V, respectively, as depicted in Fig. 2(d). The device performs excellent synaptic endurance for more than 50 epochs, as shown in Fig. 2(e). This result indicates that the device made with a barrier layer (Device B) shows promising potential for neuromorphic applications.

The TEM cross-sectional images of Device A and Device B are shown in Figs. 3(a) and (b), respectively. It is observed that both devices have an interfacial layer (TiTaON) that is formed at the bottom interface between TiN and TaOx; Device B, however, has an additional metal-oxide interfacial layer (TiWO) at the top interface between the TiW and the TaOx. This interfacial layer is confirmed by AES depth profile analysis, as depicted in Figs. 3(c) and (d). The AES profile for pristine devices also shows that the Cu diffusion in the oxide layer is limited by the insertion of the TiW barrier layer (Fig. 3(d)). Figure 3(e) and 3(f) shows XPS spectra of O 1s in TaOx layers

in Device A and Device B, respectively. The O_{II} peak which is depicting oxygen defects or vacencies is higher in Device B as compared to Device A as shown in Fig. 3(e)-(f). This result suggests that Device B has higher oxygen vaccancies in oxide layer and this leads to formation of interfacial layer TiWO.[29] Note that Cu2p core level of XPS-depth spectra of Devices A and B are centered at 932.6 eV and no significant peak shift neither any additional peak was observed which indicates Cu-Cu bond and metallic nature of Cu (data not shown).[30]

In order to validate the nature of the conductive filament, we calculate the temperature resistance coefficient employing the method suggested in the literature.[11] The On state current was measured at room temperature and 120 ^{o}C, and the calculated temperature coefficient (α) is presented in Table 1. It is found that α of Device A is 0.0016 indicating a pure Cu metallic nature of the filament,[31] however, the value of α 0.0023 for Device B does not indicate the same metallic nature. Henceforth, we can assume that the conductance filament in Device B can consist of metallic ion and oxygen vacancy defect species.

Based on above investigation, we propose the conduction mechanisms for Device A and Device B in Figs. 4(a) and (b), respectively. Device A has a large amount of diffused copper(Fig. 3(c)) at the pristine state, Fig. 4(a)(i). Nevertheless, we can infer that despite the high amount of Cu atoms in the pristine Device A, these Cu atoms are mainly dispersed in the top region of the TaOx and the bottom region of the TaOx film still has high resistivity. Hence, the device has high barrier height at the TaOx/TiN junction. Consequently, it requires high voltage for the electron to pass this barrier during the initial formation of the filament (forming process, Fig. 1a). Conversely, in the Device B, the TiW/TiWO junction has low barrier height and the oxygen vacancies-rich TaOx layer of Device B decrease the resistivity of the TaOx film; these factors contribute to the

low pristine resistance in Device B and thus, Device B requires lower forming voltage than that of A (Fig. 1b).

It is reported that Cu ions drift in the TaOx layer is low under electric field;[32] hence the device requires high $V_{forming}$ (Fig. 1(a)). The abundant amount of Cu species on the top interface region of the stack in the pristine device leading to an inverted thick conical shaped filament formation, Fig. 4(a)(ii). The excessive number of Cu atoms in the oxide layer also leads to the formation of multiple filaments. During reset process, a negative voltage is applied at top electrode, and it will cause repulsion of Cu ions towards top electrode and rupture the Cu filaments, Fig. 4(a)(iii). Then, when the positive set process happens, the Cu ions are pushed towards bottom electrode, Fig. 4(a)(iv). However, the reset and set processes occur with the formation and rupture competition between the multiple filaments resulting in the unstable switching behavior (Fig. 1(c)). The introduction of a barrier layer alters the oxygen concentration across the TaOx layer (Fig. 4(b)(i)). The TiW absorbs oxygen from the TaOx to form a TiWO interfacial layer and an oxygen-poor region at the top region of the TaOx (Figs. 3(b) and (d)). The positive bias ionizes the Cu atoms from the TE, then those ions move towards BE forming a conical shape filament (Fig. 4(b)(ii)); the apex, however, consists of oxygen vacancies defects that acculumated to complete filament and result in a hybrid filament (Table 1). This is because metallic ions drift faster than oxygen vacancy species. The Cu ions are more easily to drift in an oxygen vacancy-rich environment;[33,34] consequently, Device B requires lower $V_{forming}$ than that of Device A (Fig. 1b). The reset process occurs when the negative bias induces the recombination of oxygen vacancies with the nearby oxygens and repulse some of the Cu atoms back to the top electrode; thus, this process ruptures the filament at the top interfacial region (Fig. 4(b)(iii)). The single formation of filament during forming helps the occurrence of switching uniformity, where the rupture and

rejuvenation of the filament happen at the same position (Fig. 4(b)(iv)). We also suggest that the formation of hybrid filament plays role in the exhibition of long retention shown in Device B (Fig. 1(f)). It is well known that the filament consisting of pure Cu often suffers from an HRS decay due to the existence of residual filaments and the remnant of Cu atoms that disperse in the oxide after the reset process; thus, they could promote self-diffusion around the filament and result in the HRS decay.[35] On the other hand, the switching mechanism of hybrid filament involves oxygen vacancy defects (Fig. 4(b)(ii)) and reduce the number of Cu atoms take part in the switching process and eventually reduce the possibility of the occurence of the residual filament and dispersed Cu atoms in the oxide layer (Fig. 4(b)(iv)).

Potentiation and depression have similar mechanisms to set and reset, respectively. In the case of Device A, the potentiation exhibits abrupt conductance change and require a higher amplitude than that of Device B; this is because of the low mobility of Cu ions in the TaOx material and, thus, a higher electric field is required to ionize the ions.[32,36] However, once the device is potentiated (complete filament formation), the depression shows a gradual conductance change. This is because it is easier to re-ionize and pulse the Cu atoms back to the top region since the tip of the filament is connected directly or close to the electrode. Meanwhile, the contribution of the oxygen-poor region in the TaOx in Device B induces the gradual motion of the species resulting in excellent potentiation and depression.

Synaptic linearity is essential to ensure efficient computation in neuromorphic applications. The excellent analogous behavior of Device B (Fig. 1) contributes to the superior linearity, as observed in Figs. 5(a) and (b). We then evaluated the neuromorphic capability of these devices by employing Hopefield neural network scheme[13] to recognize 10 x 10 pixels images; each pixel represent a single artificial synapse (memristor). The weights for the initial image were fed

randomly based on the conductance states provided in Figs. 5(a) and (b). 15 images of decimal digits with 10 x 10 pixels were used as the data set for training (data not shown). It is found that Device B performs faster recognition achieving 95% accuracy with only six interations, as shown in Figure 5(c). Figure 5(d) and (e) show visual representations of the iterations where Device A and B recognize digit "8", respectively. It is shown that the computation employing Device B results in a more precise image after six iterations than that of Device A.

In conclusion, the insertion of the TiW barrier layer limits the Cu diffusion in the oxide layer during the fabrication process. This diffusion limiting of Cu ions in the oxide layer leads to the suppression of multiple filaments and improve switching stability. Device B performs excellent data retention at room temperature and at high temperature. Due to the formation of an interfacial layer between the oxide layer and barrier layer, the conduction mechanism is changed from purely Cu filament to hybrid filament. This hybrid filament conduction leads towards analog switching and multilevel cell characteristic, which is the key attribute for neuromorphic computing. The enhanced device has a highly linear and stable 50 epochs and effectively recognizes a 10x10 pixels image employing the Hopfield neural network scheme simulation. This study proposes an effective interfacial engineering method to achieve reliable analog CBRAM devices employing a hybrid filament for neuromorphic applications.

Acknowledgments

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Data Availability

The data that support the findings of this study are available from corresponding author upon reasonable request.

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Figure Captions

FIG. 1. I-V curves of Device A and Device B in (a) and (b), respectively (with forming curves). (c) and (d) shows endurance of both devices. Retention of device A at room temperature in (e) and retention of device B at RT and at high temperature in (f).

FIG. 2. Multilevel cell characteristic endurance with different reset voltage (shown in inset) "-0.8V, -1.0V and -1.2V" (a) and different compliance current (shown in inset) "1mA, 3mA and 10mA" (b). Synaptic measurement of Potentiation/Depression for (c) Device A and (d) Device B(pulsing scheme in insets). (e) Stable 50 epoch trainings. Read pulse used is +0.2V.

FIG. 3. Typical cross-sectional TEM images of (a) Device A and (b) Device B. XPS element profile for (c) Device A and (d) Device B. XPS spectra of O 1s in TaOx layer for (e) Device A and (f) Device B.

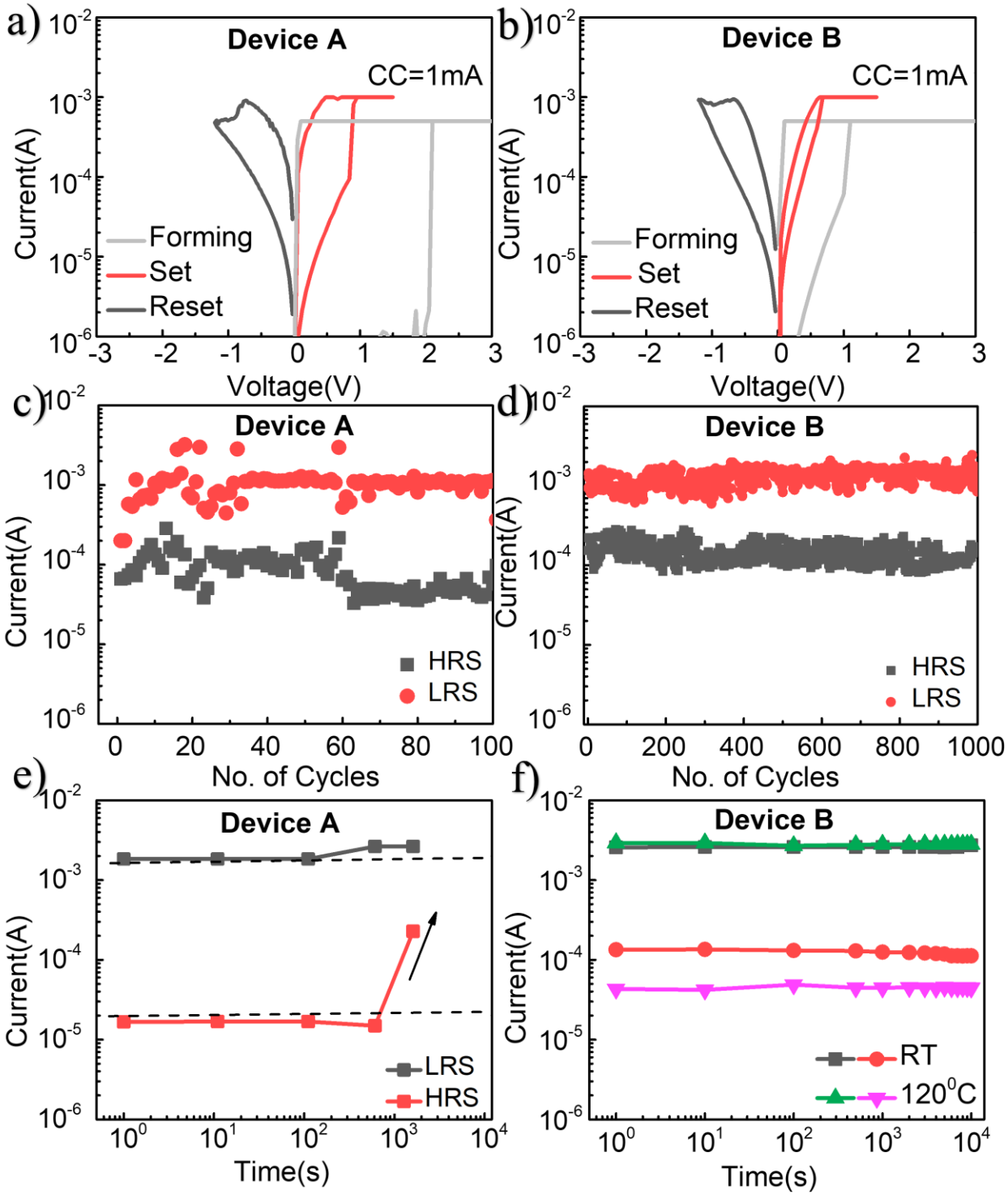
FIG. 4. Schematic figure for conducting mechanism of (a) Device A and (b) Device B.

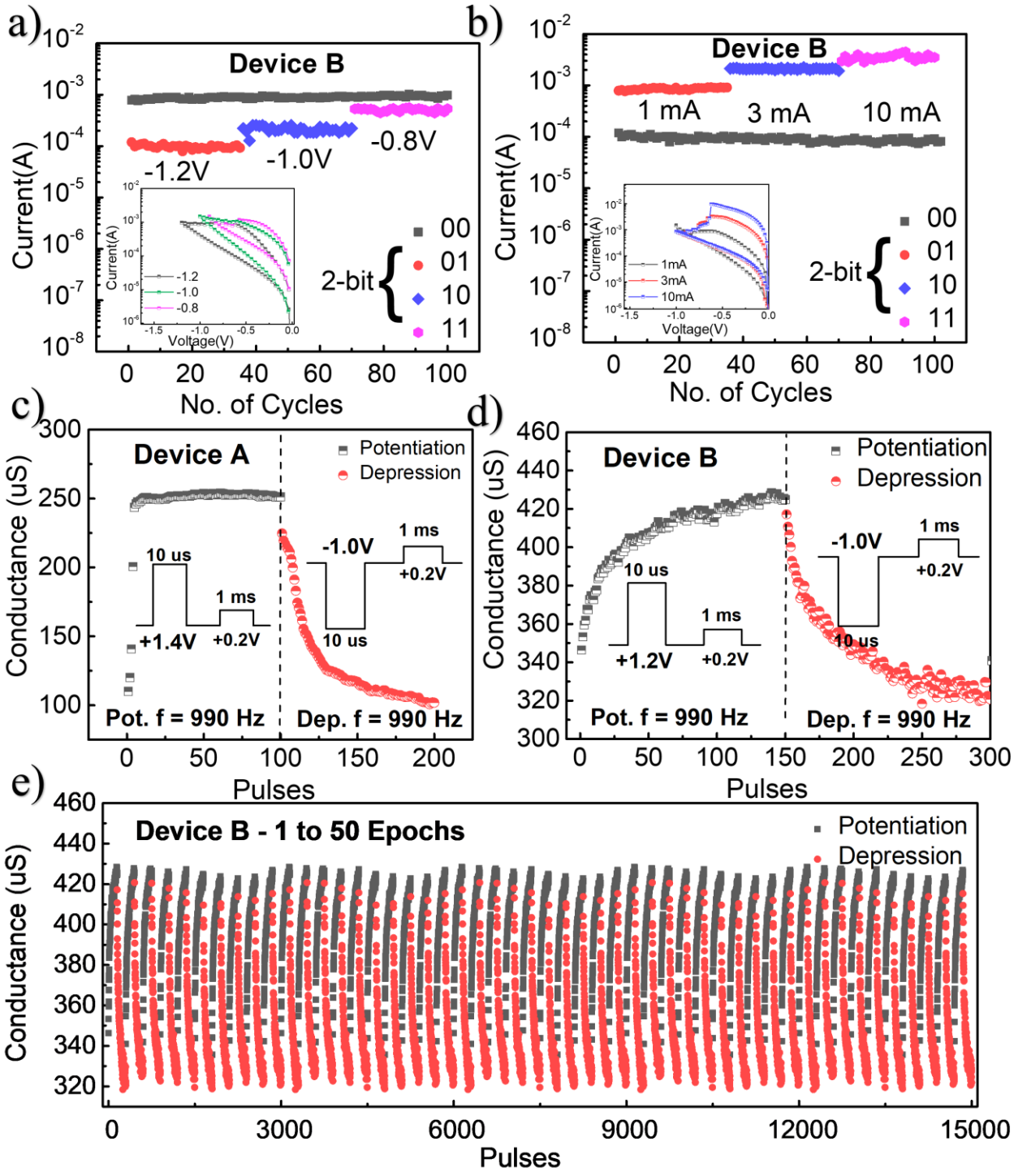
FIG. 5. Non-linearity curve with normalized conductance for (a) Device A and (b) Device B. (c) Neural network training accuracy for Device A and Device B. Various stages of 0, 2, 4 and 8 iterations for (d) Device A and (e) Device B.

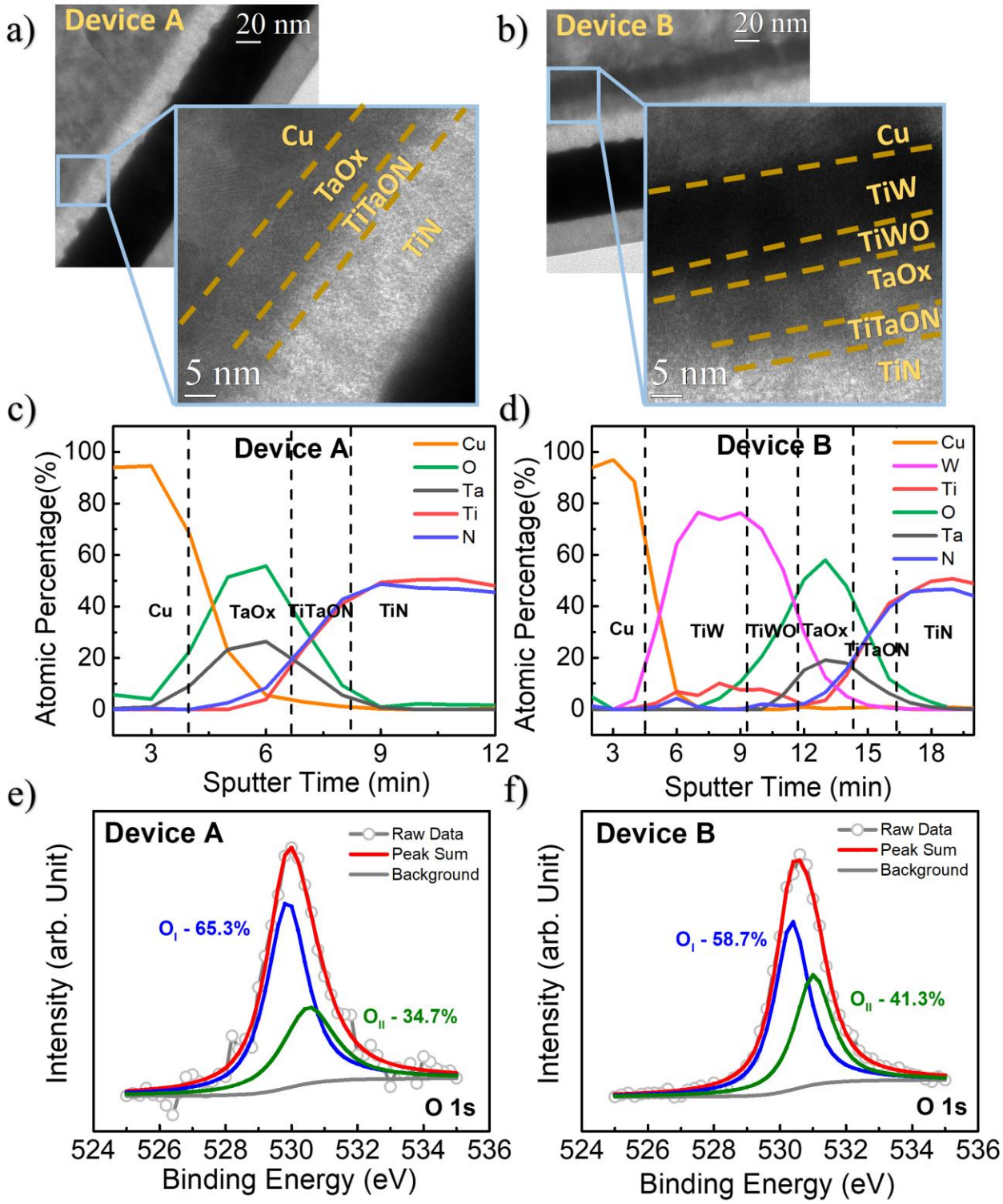
Table 1

Temperature coefficients for Device A and Device B

Devices	I_{RT}	I_T @ 120 °C	A
Device A	0.00184	0.00162	0.0016
Device B	0.00293	0.00240	0.0023


a)
Device A
CC=1mA
Forming
Set
Reset
Current(A)
Voltage(V)
b)
Device B
CC=1mA
Forming
Set
Reset
Current(A)
Voltage(V)
c)
Device A
HRS
LRS
Current(A)
No. of Cycles
d)
Device B
HRS
LRS
Current(A)
No. of Cycles
e)
Device A
LRS
HRS
Current(A)
Time(s)
f)
Device B
RT
120°C
Current(A)
Time(s)


a)
Device B
-1.2V
-1.0V
-0.8V
Current(A)
No. of Cycles
Voltage(V)
-1.2
-1.0
-0.8
2-bit
00
01
10
11
b)
Device B
1 mA
3 mA
10 mA
1mA
3mA
10mA
c)
Device A
Potentiation
Depression
10 us
1 ms
+1.4V
+0.2V
-1.0V
Pot. f = 990 Hz
Dep. f = 990 Hz
Conductance (uS)
Pulses
d)
Device B
+1.2V
e)
Device B - 1 to 50 Epochs


a)
Device A
20 nm
Cu
TaOx
TiTaON
TiN
5 nm
b)
Device B
20 nm
Cu
TiW
TiWO
TaOx
TiTaON
TiN
5 nm
c)
Device A
Cu
O
Ta
Ti
N
Atomic Percentage(%)
Sputter Time (min)
d)
Device B
Cu
W
Ti
O
Ta
N
Atomic Percentage(%)
Sputter Time (min)
e)
Device A
Raw Data
Peak Sum
Background
O_I - 65.3%
O_II - 34.7%
O 1s
Intensity (arb. Unit)
Binding Energy (eV)
f)
Device B
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Background
O_I - 58.7%
O_II - 41.3%
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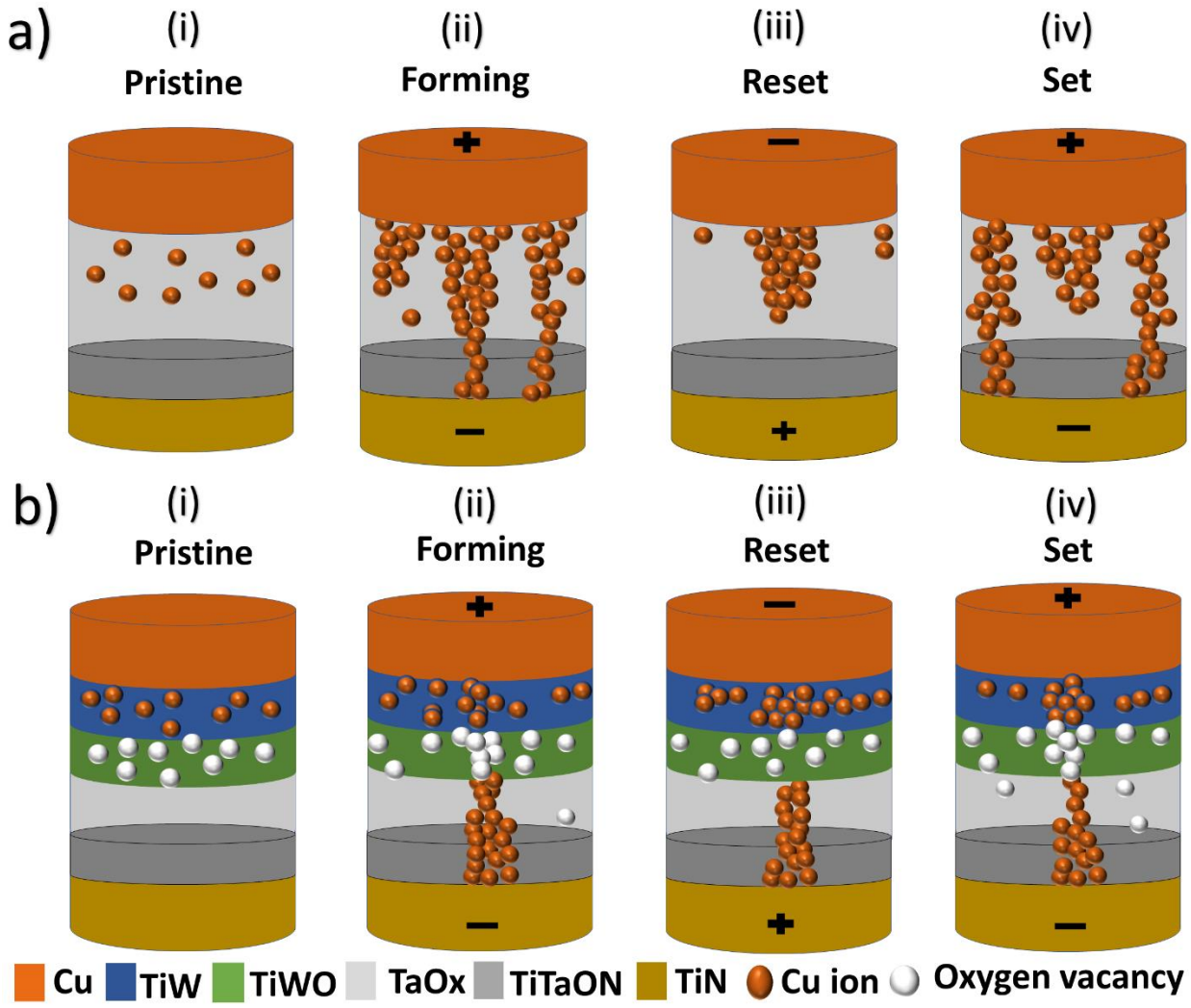
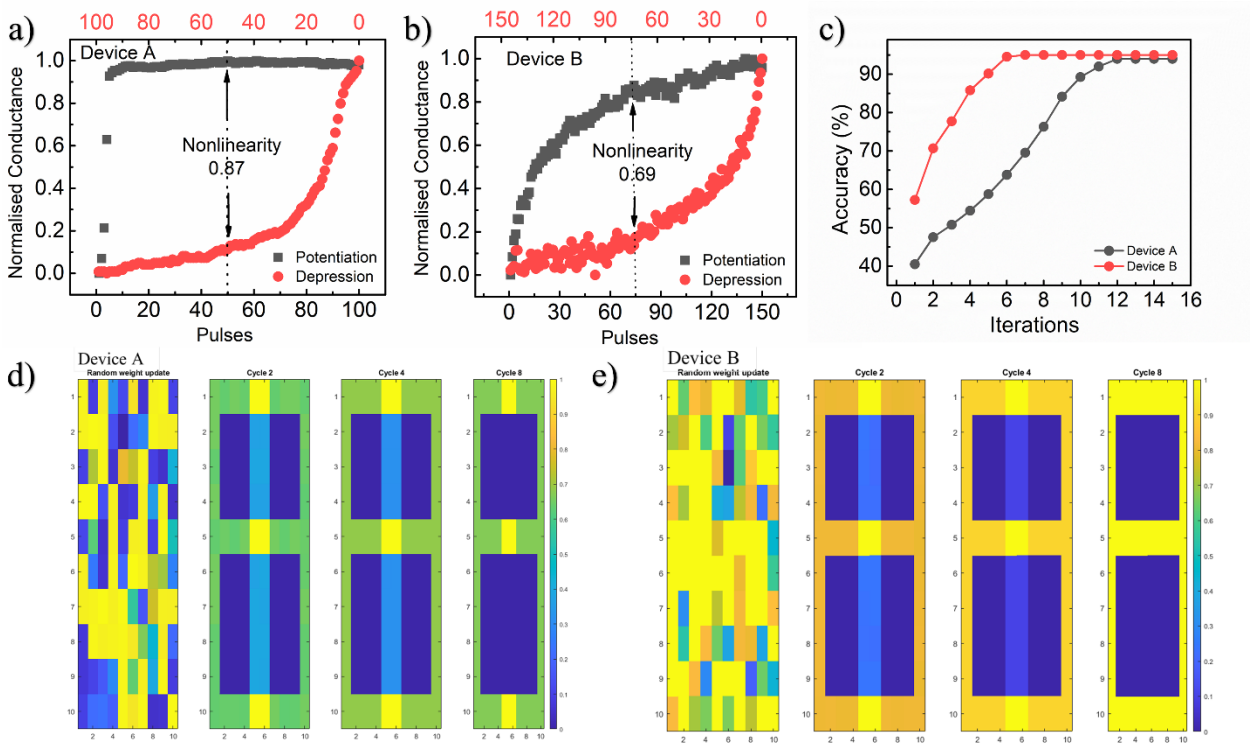
Binding Energy (eV)


a)
(i)
Pristine
(ii)
Forming
(iii)
Reset
(iv)
Set
b)
(i)
Pristine
(ii)
Forming
(iii)
Reset
(iv)
Set
Cu
TiW
TiWO
TaOx
TiTaON
TiN
Cu ion
Oxygen vacancy


a)
Device A
Normalised Conductance
Nonlinearity
0.87
Potentiation
Depression
Pulses
b)
Device B
Normalised Conductance
Nonlinearity
0.69
Potentiation
Depression
Pulses
c)
Accuracy (%)
Device A
Device B
Iterations
d)
Device A
Random weight update
Cycle 2
Cycle 4
Cycle 8
e)
Device B
Random weight update
Cycle 2
Cycle 4
Cycle 8