Power Losses Calculation for Medium Voltage DC/DC Current-Fed Solid State Transformer for Battery Grid-Connected

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Keywords

« Solid State Transformer », « Power Losses », « Battery », « Grid Connected ».

Abstract

Current fed solid-state transformers (CF-SSTs) offer substantial weight and size reduction advantages over 50/60Hz traditional transformers. CF-SSTs have low source current ripple which makes it suitable for the connection of large batteries in the medium voltage grid. However, power losses are high compare to the traditional one due to the high operating frequency range. Therefore, power losses calculations are the main key to select the main design parameters. Unlike most of the published work dealing one aspect of power losses or a specific element and only consider voltage fed Solid State Transformers topology (VF-SSTs), this paper presents a power losses calculation method for CF-SSTs considering all the power losses, the shape of the voltage waveforms, cores dimensions and manufacturer datasheets are main paper pros. ANSYS and Matlab Simulink are employed to validate the analytical equations. Due to simplicity, this method can be used for optimization.

Introduction

Battery Energy Storage System (BESS) is becoming a crucial element in the smart grid. BESS can smooth Renewable Energy Source (RES) output power and provide grid support such as frequency response and voltage control. Traditionally, BESS is connected to the medium voltage (MV) grid (1-35kV) via a bidirectional power electronic DC/DC converter, DC/AC converter and line frequency step-up transformer. These converters are responsible for ensuring grid operation codes and standards are met, and power from/to the battery is controlled. Due to limited voltage and current capabilities of the power electronic devices (up to 6.5kV/25A [1]), many power electronics topologies are proposed to meet the required voltage and current specifications.

To achieve the advantages of galvanic isolation, weight reduction and low battery voltage, Solid State Transformer (SST) can be employed [2]. SST offers many advantages over the traditional transformer such as power flow control, voltage sag compensation, fault current limitation, reduced size and weight, improved power quality, and high power density [1]. SST has mainly emerged from Dual Active Bridge

converter (DAB) technology. There are two main topologies for DAB, voltage-fed DAB (VF-DAB) and current-fed DAB (CF-DAB). The voltage phase shift technique is employed to transfer the power to the load in VF-DAB. There are different control techniques to achieve the phase shift in the voltages. Single-phase shift (SPS), dual-phase shift (DPS) and triple-phase shift (TPS) [3, 4]. DPS is the most suitable control technique [5]. In the CF-DAB, a choke coil is employed to transfer the power [6]. The turn-off voltage spike is the main problem in CF-DAB due to the storge energy on the leakage inductance. RCD snubber circuits, active clamp, zero current switching and secondary modulation can be employed to overcome this problem [7-10]. VF-DAB suffers from several limitations of high input pulsating current, high circulating current through devices and magnetics [4]. Therefore CF-DAB is more suitable for grid-connected battery applications. Current fed solid-state transformer (CF-SST) topology is considered in this paper. There are three main losses in CF-SST; core losses, copper losses and power electronics losses.

Numerous publications proposed techniques to calculate power losses based on the power electronics parameters and core losses equations [11-16]. They can be divided into three categories. The first one, authors gave much detail about core losses calculation and no much details about the power electronics losses. The second one, the authors considered only power electronics losses and employed ordinary core losses equations based on sinusoidal waveforms. The last one, the authors employed a practical measuring of the core losses or power electronics losses. In this paper, a power losses calculation method is proposed based on the manufacturer datasheets. The proposed method considers all the power losses of the CF-SST, voltage waveform shape, core flux and operating frequency. Furthermore, the main dimensions of the transformer core and choke coil core are calculated to find the volume of the cores. This method can be a useful tool to find the optimum design to achieve high efficiency or smaller size due to its simplicity.

CF-SST System Configuration

A CF-SST consisting of a medium frequency transformer, choke coil and H-bridge is shown in Fig. 1. Converter modules are connected in series and/or parallel to reduce the voltage or current stress on the power electronic devices. Fig. 2 shows a simple model for CF-SST [10]. There are two modes of operation, charging mode (buck converter) and discharging mode (boost converter). In the discharging mode, the choke coil and H-Bridge 1 operate as a boost converter. In the charging mode, H-Bridge 2 operates as a buck converter and H-Bridge 1 operate as a rectifier. The choke coil is assumed high enough to smooth the battery current, i.e, ripple currents very small. The load current is also assumed as constant and ripple-free.

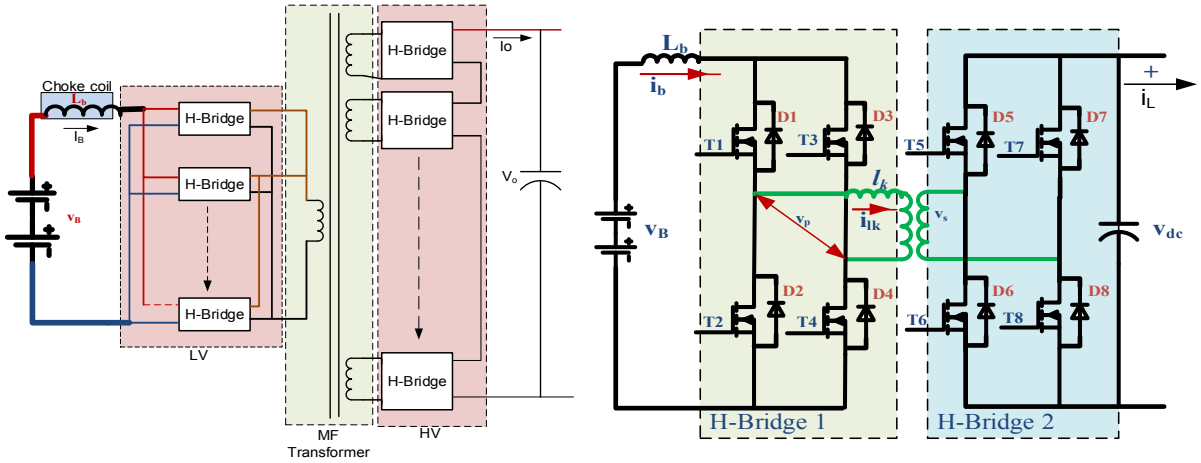

Fig. 1: SST System configuration

Fig. 2: Simplified CF-SST model

CF-SST Power Losses Calculation

The CF-SST system power losses can be divided into transformer core and copper losses, power electronics losses, choke coil core and copper losses. Details about these losses and how to be calculated are shown in the next sections.

Transformer Core and Copper Losses

Hysteresis and eddy current losses are the main iron losses in the transformer core. The hysteresis loss is related to the re-orientation of the magnetic domains while the eddy-current loss is due to the induced voltage within the magnetic core. To calculate the iron losses, the Original Steinmetz Equation (empirical equation) is normally employed [17]. This equation, however, is only applicable to a sinusoidal excitation so it is not valid for SST case where the magnetic material is excited with nonsinusoidal waveforms. Core losses under nonsinusoidal waveforms can be estimated by the Generalized Steinmetz Equation (tuned) based on the rate of change of the flux density can be estimated according to equation (1). [18, 19].

$$P_v = \frac{1}{T} k_i (\Delta B)^{\beta-\alpha} |2\Delta B|^{\alpha} (DT)^{1-\alpha}, \tag{1}$$

$$k_i = \frac{K}{(2)^{\beta-1}(\pi)^{\alpha-1}\left(1.1044 + \frac{6.8244}{\alpha + 1.354}\right)}, \tag{2}$$

The core losses in (1) are calculated per unit volume. To get the total core losses of the transformer core, the design of the transformer core is considered to calculate the core volume as in (2) [20-22]:

$$Vol_c = 2A_i \left(\sqrt{\frac{A_w}{r_w}} (r_w + 1) + \frac{d_c}{\sqrt{K_c}} \right), \tag{3}$$

where, A_i is the area product of the transformer core, A_w is the window area, r_w is the ratio of winding window height to width and d_c is the diameter of the core circumscribing. All these parameters depend on the operating frequency and core flux density. The transformer core losses can be calculated based on (1) and (2). For the copper losses, the ac resistance of the primary (R_p) and secondary voltage winding (R_s) can be calculated as in (3) [23] considering the skin effect. where ρ_c is the resistivity of the winding material, l_{pp} and l_{ps} are the total length of the primary and secondary winding respectively. δ is the skin depth. A_{cup} and A_{cus} are the cross-section of the winding conductor for the primary and secondary winding respectively. r_{op} and r_{os} are the radius of the winding conductor for the primary and secondary winding respectively.

$$R_p = \rho_c \frac{l_{pp}}{A_{cup}} \left[1 + \left(\frac{(r_{op}/\delta)^4}{48 + 0.8(r_{op}/\delta)^4} \right) \right] \tag{4}$$

$$R_s = \rho_c \frac{l_{ps}}{A_{cus}} \left[1 + \left(\frac{(r_{os}/\delta)^4}{48 + 0.8(r_{os}/\delta)^4} \right) \right] \tag{5}$$

Choke Coil Core and Copper Losses

The value of the choke coil depending on the duty cycle of the converter (D_1), the switching frequency (f), the supply voltage (V_{dc}) and the maximum allowance ripple in the DC current (ΔI_{dc}) as shown in (4) for boost operation of the SST system (battery discharging) [18]. The choke coil resistance is based on the mean length of the turn (MTL), number of turns (N_c) and cross section of the winding (A_{cuc}) as in (5).

$$L_B = \frac{(D_1 - 0.5)V_B}{f\Delta I_B} \tag{4}$$

$$R = \rho \frac{N_c \times MTL}{A_{cuc}}, \quad \text{where } MTL \cong \pi \left[\sqrt{{H_c}^2 + {W_c}^2} + W_w \right], \tag{5}$$

where H_c is the height of the core cross-section, W_c is the width of the core cross-section and W_w is the width of the core window. The winding window area (A_{wc}) equals to$W_w H_w$. The core cross-section area (A_c) equals to$W_c H_c$. The area product of the core ($A_{pc}\ and\ equlas\ to\ A_{wc}A_c$) is the main parameters to find a suitable core for the choke coil. A_{pc} can be calculated as in (6) [24].

$$A_{pc} = \frac{2En \times 10^{-4}}{B_{mc} J K_u}, \tag{6}$$

where En the energy in watt-seconds, J is the current density, B_{mc} is the choke coil flux density and K_u is the choke coil window utilization factor for the core. The number of choke coil turns can be calculated as in (7) [25]. where K_{uc} is the effective window factor for the choke coil core, K_f is the filling factor, I_{B-rms} is the RMS value of the battery current and $K_{cc}$is the ratio of the winding are to the core cross-section area.

$$N_c = \frac{K_{uc} K_f I_{B-rms}}{J\sqrt{A_{pc} K_{cc}}} \tag{7}$$

Here, the fluctuation of the flux density of the choke is very small due to the low ripple on the choke coil current. Therefore, the core losses of the choke coil can be calculated by simple core losses equation. Based on the volume of the core, the choke coil core losses can be calculated.

Power Electronics Losses

Power electronics losses have two main losses, conduction losses and switching losses. Assuming several H-bridges are connecting in parallel at the low voltage side to reduce the current stress in the switch and several parallel H-bridges on the high voltage side to reduce the voltage across the switch as shown in Fig. 1. Based on the circuit diagram in **Error! Reference source not found.** and mapping the on-state characteristic as shown in Fig. 3, the RMS and average of the switch current of the H-Bridge 1 (for switch T1) under discharge mode are [10]

$$I_{T1} = \overline{I_B} \sqrt{\frac{2 - D_1}{3}} \tag{6}$$

$$\overline{I_{T1}} = \overline{I_B} \frac{3 + D_1}{4} \tag{7}$$

The RMS and average of the switch, I_{T5}, and diode currents, I_{D5}, of the H-Bridge 2 (for switch T5) are

$$I_{T5} = \bar{I}_L \sqrt{\frac{D_2}{3}} \tag{8}$$

$$\overline{I_{T5}} = \bar{I}_L \frac{D_2}{2} \tag{9}$$

$$I_{D5} = \bar{I}_L \sqrt{\frac{5 - 4D_1 - 2D_2}{6}} \tag{10}$$

$$\overline{I_{D5}} = \bar{I}_L \frac{3 - 2D_1 - 2D_2}{6} \tag{11}$$

where D_2 is the duty cycle of the switch in H-bridge 2, and $\bar{I}_L$ is the average load current.

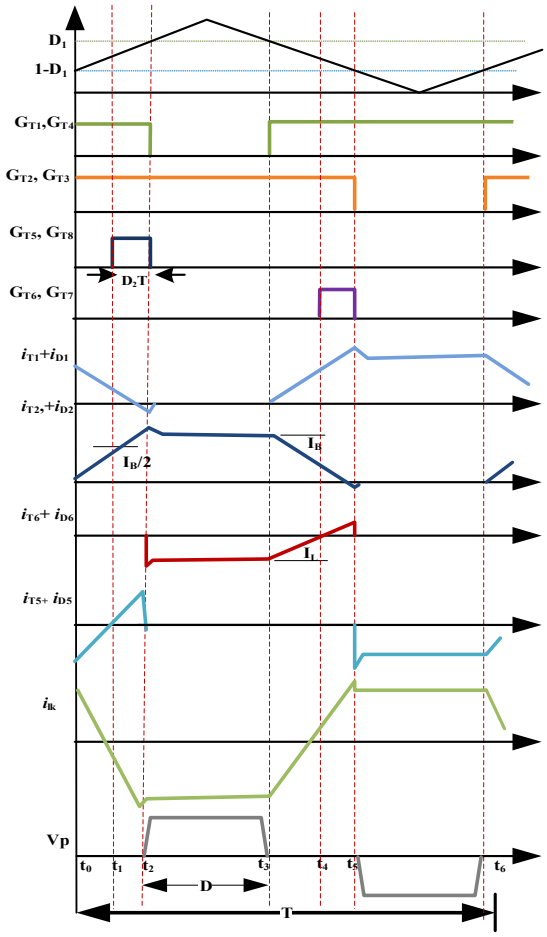

Fig. 3: Details of CF-SST operation over one cycle [10]

Based on mapping the on-state characteristic and employing equations and consider the effect of the junction temperature, the conduction losses and turn OFF power dissipation of the switches and diode can be calculated for the CF-SST configuration in Fig. 1 as [26, 27].

$$P_{cond\_T} = N_{LV}(K_1 I_{T1}^2 + K_2 \overline{I_{T1}}) + N_{HV}\left(I_{T5}^2 K_1 + K_2 \overline{I_{T5}}\right) \tag{12}$$

$$P_{sw\_T} = K_3 f E_{on+off}\left(N_{LV}\left[\frac{I_{T1}}{I_{ref}}\right]^{K_{is}}\left[\frac{V_B}{2V_{ref}}\right]^{K_{vs}} + N_{HV}\left[\frac{I_{T5}}{I_{ref}}\right]^{K_{is}}\left[\frac{V_o}{2N_{HV}V_{ref}}\right]^{K_{vs}}\right), \tag{13}$$

$$P_{cond\_D} = N_{HV}[I_{D5}^2 K_5 + \overline{I_{D5}} K_4]\,, \tag{14}$$

$$P_{sw\_D} = K_6 N_{HV} f E_{rr}\left[\frac{I_{D5}^2 K_5}{I_{ref}}\right]^{K_{id}}\left[\frac{V_o}{2N_{HV}V_{ref}}\right]^{K_{vd}}, \tag{15}$$

where

$$K_1 = V_{CE(25^0C)} + TCs_V(\Delta T_j)\,, \tag{16}$$

$$K_2 = r_{CE(25^0C)} + TCs_r(\Delta T_j)\,, \tag{17}$$

$$K_3 = 1 + TCs_{Esw}(\Delta T_j)\,, \tag{18}$$

$$K_4 = V_{f(25^0C)} + TCd_V(\Delta T_j)\,, \tag{19}$$

$$K_5 = r_{f(25^0C)} + TCd_r(\Delta T_j)\,, \tag{20}$$

$$K_6 = 1 + TCd_{Err}(\Delta T_j)\,, \tag{21}$$

where N_{LV} is the total number of switches at the low voltage side and N_{HV} is the total number of diodes at the high voltage side. D_2 is the duty cycle of switches of H-Bridge 2, $\overline{I_L}$ is the average load current. TCs_V and TCs_r are temperature coefficients of the on-state characteristic for the switch and TCd_V & TCd_r are the temperature coefficients of the on-state characteristic for the diode. ΔT_j is the increase in the junction temperature from the ambient temperature. The other parameters and their values are shown in TABLE I [26, 27].

TABLE I : POWER ELECTRONICS LOSSES PARAMETERS

Term	Meaning	Value
K_{is}	Exponent for the current dependency of switching losses (switch)	≈1
K_{vs}	Exponent for the voltage dependency of switching losses (switch)	≈1.3 to 1.4
K_{id}	Exponent for the current dependency of switching losses (diode)	≈0.6
K_{vd}	Exponent for the voltage dependency of switching losses (diode)	≈0.6
TCs_{Esw}	Temperature coefficient of the switching losses	≈0.003
TCd_{Err}	Temperature coefficients of the diode switching losses	≈0.006

Simulation Results

1MW DC/DC CF-SST is considered as a study model. The battery voltage is 600V and the dc-link voltage for MV is 18kV. Due to the high battery current (1.7kA), four parallel H-bridges are employed to reduce the current on the switch to 417A. For the high voltage side, 6 series H-Bridge are considered to reduce the reverse voltage. The analytical calculations are compared with the simulation based on the MATLAB Simulink. Matlab Simulink calculates the power electronics losses with the help of a 3-D lookup table from the manufactures datasheets [28]. A Simulink model for the CF-SST is built on the Matlab Simulink platform. The IGBT module 5SNG 0450X330300 [29] is considered as the power electronics switches for the CF-SST. The IGBT junction temperature is fixed at 125°C. The on-state resistance for the IGBT (r_{CE})and the diode (r_f) are not included in datasheets. To estimate these values,

the typical on-state characteristic relationship between V_{CE} and I_C can be employed. Based on the V_{CE} and I_C curves, $r_{CE} = 3.2m\Omega$ and $r_f = 2m\Omega$ at 125° C junction temperature.

Fig. 4 shows the power electronics losses of the CF-SST by analytical equations and Matlab simulation at the different switching frequency and the full load. It seems that there is a small mismatch between the analytical and simulation results. For the core losses, finite element analysis (FEA) is employed to verify the analytical equations by ANSYS Workbench. SURA No18 is employed as a core material [30]. The 1200 V input voltage waveform is injected to the transformer primary. Under different duty cycles of low voltage H-Bridges, the core losses of the transformer calculated by the analytical equations and by ANSYS are shown in Fig. 5. There is an error between the ANSYS and analytical equations not more than 20%. The core losses increase with the decreases in the duty cycle. This is due to the increase in the duty cycle decrease the width of the injected voltage to the transformer.

Fig. 6shows transformer copper and core losses, choke coil copper and core losses and power electronics losses at different operating frequencies and a fixed flux density of 1T. At the low frequency, the copper losses are the dominant losses while power electronics losses are the main losses for frequency more than 200Hz. All these curves depend on the core materials selection and the power switching technology. The core losses of the choke coil are small due to the change of the flux density of the choke coil core is very small. The total CF-SST losses under different operating frequency and core flux density are shown in Fig. 7. The operating frequency about 600Hz seems to be the optimum value for minimum power losses.

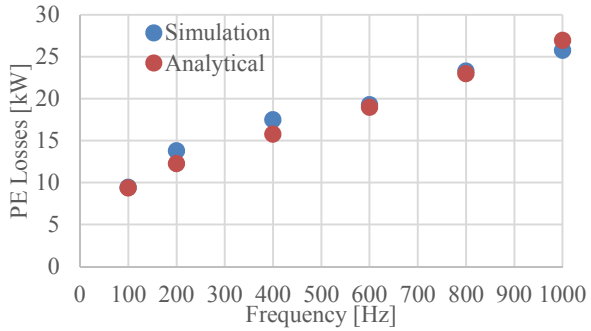

Fig. 4: Power electronics losses for the CF-SST by simulation and analytical method

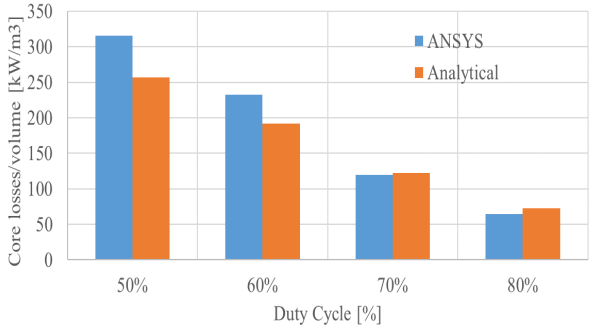

Fig. 5: Transformer core losses by ANSYS and analytical method at a different duty cycle

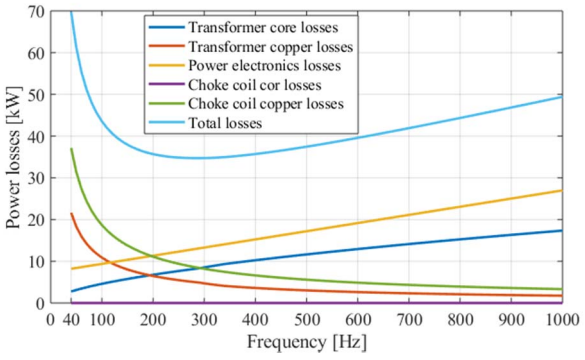

Fig. 6: CF-SST copper, core and power electronics losses

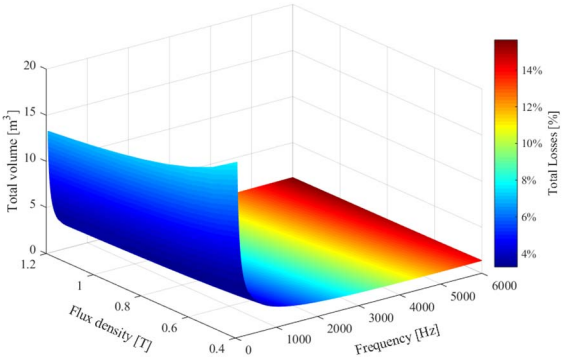

Fig. 7: Total CF-SST losses at different operating frequencies and flux density

Conclusion

This paper presents an analytical method to calculate the power losses for current fed solid-state transformer based on the manufacturer datasheets, operating frequency and core flux density. It considers the nonsinusoidal voltage waveforms to calculate the core losses and power electronic losses. ANSYS and Matlab Simulink are employed to validate the analytical results. At low frequency, the copper losses are the main losses. As the frequency increases the copper losses decreases and the power electronics and core losses increase. There are an optimum operating frequency and flux density where the total losses are minimum. This is topology can be employed to find the optimum flux density and operating frequency to gain maximum efficiency.

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