Direct observation of surface charge redistribution in active nanoscale conducting channels by Kelvin Probe Force Microscopy

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Surface-exposed uniformly doped Silicon-on-Insulator (SOI) channels are fabricated to evaluate the accuracy of Kelvin Probe Force Microscopy (KPFM) measured surface potential and reveals the role of surface charge on the exposed channel operated in the ambient environment. First, the quality of the potential profile probed in the vacuum environment is assessed by the consistency of converted resistivity from KPFM result to the resistivity extracted by the other three methods. Second, in contrast to the simulated and vacuum surface potential profile and image, the ambient surface potential is bent excessively at the terminals of the channel. The excessive bending can be explained by the movement of surface charge under the drive of geometry induced strong local electric field from the channel and results in non-uniform distribution. The dynamic movement of surface charges is proved by the observation of time-dependent potential drift in the ambient measurement. The result suggests the surface charge effect should be taken into account of the measurement of the surface potential in the ambient environment and the design of charge sensitive devices whose surfaces are exposed to air or in ambient conditions in their operation.

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1. Introduction

High-resolution topography and local potential image together are a very powerful tool to understand the local environment of nanoelectronic devices, for example, the dopants fluctuation in nanowires [1–3], defects in nanowires [4] and 2D materials [5], junction formation in various nanostructures [6–11], band bending in crystal grains boundaries [12,13], the surface potential change on sensors [14–20]. Furthermore, the operational status of devices can be studied by in-situ local potential extraction e.g. surface plasmon field [21], potential fluctuation in crystal grains [12,22], junction of sollar cell under illumination [23], potential change in p-n junction under biasing [7,24–26], non-linear local potential drop due to Schottky contacts [27], the variation of doping or surface charge [28]. The local electrical potential is not only associated with the properties of materials or device themselves but also with the measurement environment [29–31], applied bias induced local charge trapping or injection [30,32–34], and ion transportation [35]. This dynamic surface potential change is not well studied but important, associated with various kinds of nanoscale charge sensitive devices, especially for sensing applications.

KPFM [36] has been developed to extract the high-resolution potential image from micro- and nanostructures. It is based on the technique of Atomic Force Microscope (AFM) that can detect nano-newton-level force change between the cantilever and sample with the distance of less than 5 nm. The KPFM system is capable to sense, in addition to atomic force, the electrical or capacitance force [37,38] which is generally considered to be the response to the workfunction of materials [36,39], applied bias [4,27,40], trapped charges on the surface [41–43]. Therefore, KPFM has the high sensitivity [36] to the local potential (~ 0.1 mV) and inherit the lateral resolution of sub-nanometer scale. On the other hand, the recent studies reveal that the scanned potential values need to be deconvoluted [44,45] due to the mulitple capacitance coupling [46], tip-sample distance [46], the

response of feedback mode and the screening effect of surface charges on various materials [29,47,48].

Considering the quest of detailed investigation on the surface charge behaviour on nanoscale sensor devices, we have designed simple and surface-exposed conducting SOI channels as a test structure and developed the capability to scan the device with current flow in the vacuum environment. In this paper, we report the KPFM surface potential images and profiles of the conductive SOI channels that have been measured under various bias and environmental conditions systematically for the first time. We present not only accurate extraction of the actual local potential drop in the channel linking with the local resistivity evaluation of the devices, but also the observation of novel dynamic surface charge redistribution under the ambient condition that has been identified after the intensive analysis of the surface potential data taken under various conditions.

2. Experimental

2.1 Sample preparation

A fabrication process of the heavily-doped silicon channels is schematically shown in Fig. 1. We have employed the top-down fabrication process to use the high-quality single-crystalline SOI for the channel so that potential crystal defects introduced by bottom-up growth of silicon nanowires [4] can be avoided. A p-type 6-inch SOI wafer (SOITEC) was used as a starting wafer. The SOI layer thinned to 50 nm by thermal oxidation was coated by spin-on-dopant (SOD, Filmtronics P507), and then loaded in a furnace at 950 ˚C for 30 minutes to diffuse phosphorous uniformly into the 50 nm SOI. The conventional thermal diffusion for the ultra-thin (50 nm) SOI is beneficial to minimise the doping concentration fluctuation in the active channel layer. The SOD layer and a SiO_2 layer formed in the diffusion process were etched by using 2.3 % Hydrogen Fluoride (HF) solution. The thickness

of the n-type uniformly-doped SOI layer after the etching was measured 30 nm by ellipsometry, and the resistivity was evaluated as $\rho_{4p} = 4 \times 10^{-4}$ Ω·cm on average by a JANDEL four-probe measurement instrument corresponding to a doping concentration of 2.1×10^{20} cm^{-3}. The Hall resistivity $\rho_{Hall} = 2.5 \times 10^{-4}$ Ω·cm has also been obtained by a Nanometrics HL5550 cryostat Hall effect measurement system for a wafer with van der Pauw electrode, corresponding to 1.5×10^{21} cm^{-3} [49]. The device pattern was drawn on a negative resist, RHEM UVN30 by using electron beam lithography system JEOL JEX-9300 and then transferred onto the top silicon layer by reactive-ion-etching (RIE) by using Plasma 100 (Oxford Instruments). An SEM top view image of the device is shown at the right-bottom of Fig. 1. The dimensions of the main channel is 1 μm in length and 500 nm in width. Both the ends of the narrowest part are connected to the lead regions with a width of 5 μm and the length of 20 μm. The chip surface is finally cleaned by 10-min oxygen plasma ashing and followed by 0.15 % HF etching for 5 min to remove the native oxide. Soon after the cleaning process, the sample is wire-bonded quickly and then put in a Nanonics CV 2000 vacuum chamber for KPFM measurements.

2.2 KPFM measurement configuration

The overall configuration of the Nanonics CV2000 KPFM measurement system is summarised in Fig. 2. The schematic diagram in Fig. 2 (a) presents the electrical connection of the KPFM measurement system showing how the source-drain bias V_d is applied to the device under test. The sample is loaded on the scanner port in the vacuum chamber (Fig. 2 (b)) which is connected by the turbo and ion pumps to maintain the vacuum level down to 1×10^{-7} Torr and the measurement lab is controlled at 20~22 ˚C with humity ~50% RH (ambient condition). For applying the voltage to and measuring the current of the device terminals, a custom-made chip holder shown in Fig. 2 (c) on which the device terminals are wire-bonded, is embedded in the vacuum chamber. The terminals are

electrically connected to the source meter Keithley 2400 through a hermetic connector. An optical image of a wire-bonded device with a laser spot on a cantilever in KPFM measurements is shown in Fig. 2 (d). The cantilever is located perpendicular to the device to avoid unnecessary parasitic capacitance coupling. The KPFM tips we used for this measurement is PtIr coated Nanosensor ATEC-EFM-10 with the resonant frequency f_0 = 65 kHz. The KPFM signal is taken under the AC frequency f_{ac} = 58 kHz with Amplitude Modulation (AM). The samples are scanned under the tapping mode, and the KPFM signal has been recorded during each AFM scan simultaeneously. The noise level is estimated 10 mV from KPFM signal fluctuation when a tip is engaged with a sample but without lateral scan. The laterial spatial resolution of 20 nm is estimated from the average tip radius of ~ 10 nm. These values are enough to observe the device structure and charging effects around the nanoscale channels.

3. Results

3.1 Sample and KPFM tool test

To test both KPFM system and the sample fabricated for the surface charge effect observation, the sample with L = 2 μm was placed in the KPFM system chamber under high vacuum (1×10^{-7} Torr) for 72 hours to avoid the interference of the surface charge [29–31,47,48]. The potential profiles are taken in vacuum from the centre of the channel by fixing drain bias V_d for each scan and the range of V_d is from -5 V to 5 V with the step of 2.5 V, and the drain side is always grounded during all measurements. The potential profiles from the left-hand-side drain lead terminal to the source lead terminal via a narrow conductive channel within the scanning range of 8 μm are presented in Fig. 3 (a). The slope of the potential along the channel has changed and each potential curve has shifted according to the change of the external bias. This shift is due to parasitic potential changes

throughout the circuit including effects of the resistance of wider lead regions and contact resistance between the wires and SOI in applying V_d. Note that the offset of V_{CPD} = -0.24 V observed for the profile with V_d = 0 in Fig. 3 (a) suggests the inherent work function difference between the tip and SOI channel. Here we use the local potential drop along the channel observed in Fig. 3 (a) to estimate the average resistivity of the channel. Figure 3 (b) is a blow-up of the V_{CPD} change of the fitting region indicated in Fig. 3 (a). For the convenience to compare the data with different drain voltages explicitly, the offsets of the V_{CPD} at the right-hand-side terminal is normalised in this plot without changing the slope of the profile. The extraction of the slope has been done by fitting the data points taken on the main channel area. The slope of the V_{CPD} along the channel corresponds to the average of electric field E_x along the channel. In Fig 4 (c), the E_x is plotted as a function of the current density along the channel direction $J_d = I_d/wt$, where the I_d is the current measured simultaneously with each KPFM scan. According to Ohm's law, $E_x = \rho_{KPFM} J_d$, the slope of the fitting curve in Fig. 3 (c) corresponds to the resistivity ρ_{KPFM} extracted from this measurement. The fitted slope value of ρ_{KPFM} is in Fig. 3 (c) is 7.1 ± 0.47 $\times 10^{-4}$ Ω·cm, which is very close to the value 7± 0.08 $\times 10^{-4}$ Ω·cm that has been obtained from the conventional *I-V* characterisation. For further details of the *I-V* characterisation, see Figure S3 in the supplementary information.

3.2 Ambient and vacuum potential map

To explore the effect of surface charge under the influence of operational bias, the potential map from a 1-μm-long channel device is scanned in ambient, and another device with 2-μm-long channel is scanned in vacuum for comparison. Although the channel lengths of the devices are different, fairness of this comparison will be addressed later in terms of the electric field applied to the channel. Figure 4 summarises two-dimenational (2D) maps obtained by AFM or KPFM measurements of the conductive channels together with corresponding AFM or KPFM profiles along the centre of the

channel of the devices. Figure 4 (a), (b) and (c) are for the device with 1 μm in length and 500 nm in width and the images were taken in the ambient environment. Figure 4 (d), (e) and (f) are for the device with the channel with 2 μm in length and 500 nm in width, taken in vacuum with the pressure of $\sim 1 \times 10^{-7}$ Torr. Both the AFM images in Fig. 4 (a) and (d) show the surface roughness level of less than 1.8 nm. The KPFM image at V_d = 0 V taken in ambient in Fig. 4 (b) shows relatively uniform surface potential over the left-hand-side drain lead and the channel, and edges of the SOI device structure are clear. The surface potential is slightly drifted on the source side from top to bottom. In contrast, the image taken in vacuum in Fig. 4 (e) does not show the potential drift on either of the leads except for randomly-distributed high V_{CPD} regions, especially on the drain lead. Note that the line scans in Fig. 4 (e) shift downwards about 0.5 V to the line in Fig. 4 (e). Figure 4 (c) shows KPFM surface potential map of the conducting channel taken in ambient at V_d = 5 V. It is noticeable that a characteristic circle-like pattern with the relatively lower V_{CPD} emerges at the junction between the channel and drain lead, and the potential change at the corners of the lead regions is blurred. On the other hand, the image taken in vacuum in Fig. 4 (f) does not show the pattern and the edges of the electrode structures are clearly identified. In the line scans along the channel under biasing, while monotonous decreases of V_{CPD} from the source to drain with smooth crossovers at both the channel edges are found for the vacuum-exposed channel in Fig. 4 (f), the data taken for the air-exposed channel plotted in Fig. 4 (c) show non-monotonous changes that are particularly characterised by a dip at the junction between the channel and drain. This anomalous profile corresponds to the formation of the circle pattern observed in Fig. 4 (c). Similar results have been confirmed with the other air-exposed SOI channel with a length of 1.5 μm as shown in Figure S1 in the supplementary information. We have also confirmed the potential drift does not relate to the topography change in the AFM image as shown in Fig. S4 in the supplementary information.

To compare with theoretical aspects, numerical simulation has been performed for a model of the conductive silicon channels by using the self-consistent 3D device simulator ATLAS (Silvaco) which includes the Fermi-Dirac and Boltzmann statistics, effective density of states, intrinsic carrier concentration, Passler's model for temperature dependent bandgap, bandgap narrowing, and the universal energy bandgap model to estimate charge carrier density inside of the semiconductor. The mobility model is included to calculate the electron mobility change dpending on the temperature, high or low field, impact ionization, and strain. We have confirmed the typical parameters calculated in the simulation are consistent with the values expected for heavily-doped conucting channels. Figure 5 (a) shows a calculated potential map for a silicon device with the channel length of 1 μm and a uniform doping concentration of 1.2×10^{20} cm^{-3} [49] which results in the same resistivity value 7 $\times 10^{-4}$ Ω·cm measured by *I-V* and KPFM methods above. To simulate the potential in Fig. 4 (f), a current of 1.207 mA is applied to the device while the right-hand-side edge of the source is grounded. The potential profile curve along the line through the centre of the channel is also plotted. A monotonous behaviour with gradual slope changes at the points of two junctions is quite similar to the experimental surface potential profile of the vacuum- exposed channel in Fig. 4 (f). This consistency suggests that under appropriate treatment of the surface, the CPD of the KPFM traces the potential drop along the conductive channel. The comparison also indicates that additional effects should be taken into account to explain the surface potential behaviour of the air-exposed channel shown in Fig. 5 (c). By taking the space derivative of the local potential, the local electric field, E_x, has been calculated and the magnitude of the x component of the electric field, E_x is mapped as shown in Fig. 5 (b). A profile of E_x along the centre of the channel is also plotted below the 2D map. It is noticeable that further drastic change of the electric field at the edges of the channel connected to the lead regions and the spatial distribution of the lead regions are somewhat similar to the experimental V_{CPD} image shown in Fig. 4 (c).

3.3 Voltage and time dependent surface charge redistribution

To investigate the influence of the operational bias on the surface potential in ambient environment in further detail, the surface potential of the 1 μm device is mapped in Fig. 6 (a), (b), (c), and (d) for V_d equal to 5 V, 2.5 V, 1 V and 0.5 V, respectively. A circular-like pattern in the centre of the images which is the channel region, can be clearly observed in Fig. 6 (a), (b), and (c) but obscurely in Fig. 6 (d). Refering to the potential profile under the potential map image, the circular-like pattern represents the downwards shift of potential value for 0.12 V, 0.28 V, 0.14 V and 0.05 V in Fig. 6 (a), (b), (c), and (d), respectively. It is notable that the height of potential shift increases from 0.19 V to 0.28 V for the V_d reduction from 5 V to 2.5 V and then decreases from 0.28 V to 0.14 V by changing V_d from 2.5 V to 1 V. The potential profile turns to be almost straight when V_d is reduced to 0.5 V. Besides, the symmetric funnel-like potential contour on the leads is connected to the circular-like pattern on the channel from both left-, and right-hand-side which can be clearly observed in both Fig. 6 (a) and (b). On the other hand, the funnel-like potential contour on the leads has almost disappeared in both images of Fig. 6 (c) and (d).

It is also noteworthy that the level of the electric field induced in the channel in Fig. 6 (a) (V_d = 2.5 V for the 1-μm-long channel) is smaller than that in Fig. 4 (f) (V_d = 5 V for the 2-μm-long channel) according to the relationshi between the electric field and current [49], $E_x = I/q\mu nA$, where the E_x is the electric field along with the channel, I is the current, q is the electron charge, μ is the electron mobility, n is the effective charge carrier density, and A is the cross sectional area of the channel which is 500×30 nm^2. As the factors $q\mu nA$ in both devices are identical, the magnitude of E_x difference is only decided by current value, I, which are 0.635 mA and 1.044 mA in Fig. 6 (a) and Fig. 4 (f) respectively. The characteristic anomaly in ambient condition appears clearly at the channel edges particullarly a dip on the drain side in Fig. 6 (b) instead of smooth and monotonious transitions observed at the channel edges in vacuum in Fig. 4 (f). This additional comparison can support our

argument that the characteristic anomaly cannot attribute to the magniture of the electric field but of an effect of environmental difference, and can assure our comparison between in vacuum and in ambient in Fig. 4 is sensible.

To observe the time-dependent potential change clearly, the V_d was set to -5 V to induce the maximum accumulation of surface charge on one side of the electrode. Then V_d was fixed at 1 V until two potential map scans are taken. In Fig. 7 (a), V_d 's initial status set from -5 V to 1 V, the potential dip on the channel is presented as in Fig. 6 (c). Another image was taken directly after the first scan, which takes about 40 minutes, to observe surface potential status change. The second scan in Fig. 7 (b) indicates the surface potential is clearly changed with time and more uniform, but the potential value is still not aligned to the value in Fig. 6 (c). Figure 7 (c) shows the potential on the right-hand-side source electrode region shifts downwards about 300 mV, while the potential on the channel shift upwards about 100 mV after leaving the device for 40 minutes under V_d = 1 V. Compared to the potential on the source and channel, the potential change on the drain side is relatively small except for the part near the channel where the potential shifted downwards about 50 mV. See Figure S2 in Supplementary Information where how the KPFM surface potential image is changed with respect to the time is represented for further information about the dynamic behaviour.

4. Discussion

First, we discuss the KPFM and sample test result. The group of potential profiles in Fig. 3 (a), which were taken in the vacuum environment demonstrates the response of surface potential change along with the channel to the operating bias. The potential slope from the channel in Fig. 3 (b) and the fitted relationship between E_x and J_d in Fig. 3 (c) indicates our KPFM system is able to measure the operating bias induced local potential drop from the thin-film devices. The accuracy of the potential value is examined by converting the extracted electric field E_x, which is along with the Source-Drain

direction, and current density information to the value of resistivity ρ_{KPFM} and by comparing the resistivity with that evaluated by the *I-V* characterisation. The ρ_{KPFM} of $7.1 \pm 0.47 \times 10^{-4}\ \Omega \cdot \mathrm{cm}$ is well consistent with ρ_{IV} of $7.0 \pm 0.08 \times 10^{-4}\ \Omega \cdot \mathrm{cm}$ suggesting that our KPFM measurement system set-up with the capability of *in-situ* biasing and current monitoring can be used to determine the resistivity of a single device with a level of accuracy. Note that the accuracy is assured from the data taken in vacuum or equivalent environment where effects of the surface charges can be negligible. As is shown in the difference between Fig. 4 (c) and (f), the surface potential profile at the terminals of the channel is bent in the ambient condition where effects of surface charges should be taken into account. The extracted slope from Fig. 4 (c) in ambient is 7.46 kV/cm, while the slope from Fig. 5 (f) is 5.16 kV/cm, resulting in a considerable difference of of $1.86 \times 10^{-4}\ \Omega \cdot \mathrm{cm}$ in resistivity extraction. This quantitative difference also supports existence of additional effects due to surface charges to be discussed below.

Here, we discuss the difference of surface potential maps and profiles between in ambient and in vacuum. At V_d = 0 V, while overall surface potential maps are relatively flat, but potential profile in Fig 4 (e) shifts downwards about 0.5 V in the vacuum environment to the potential profile in Fig 4 (b) in ambient. In addition, a level of drift of the surface potential has been observed in Fig 4 (c), which is about V_{CPD} ~ 0.2 V, when V_d is increased to 5 V in ambient, but not observed in the vacuum scan in Fig. 4 (f). The measured contact potential difference V_{CPD} is primarily associated with the work function which is directly related to the carrier concentration *n* in the material. However, the 0.5 V drift of V_{CPD} on the channel in Fig. 4 (c) and (e) cannot be explained because (1) both the channel and lead regions are formed on the uniformly heavily-doped SOI and (2) the drift is only observed in the map taken in ambient. Therefore, excess charges at the surface of the surface-exposed devices in ambient would be a possible source of this additional potential change. In addition to the potential shift on the channel, the dissimilar shape of potential contour on the leads is clearly present

in Fig. 4 (c) and (f). Where the vacuum potential map contour in Fig 4 (f) is similar to the simulation in Fig. 5 (a), the vacuum result in Fig. 4 (c) is similar to the simulated magnitude of the electric field in Fig. 5 (b). The potential maps in Fig. 6 indicate the shape of the potential contour depends on the magnitude of the device operating bias. In the weak potential field area on the leads, the reshaping of potential contour can be only seen in the large biased images in Fig. 6 (a) and (b). Therefore the excess charge on the surface is shaped by the electric field from the device's surface, and the amount of charges is related to the magnitude of the electric field. As a result, the electric field is not strong enough to drive the movement of excess charges and forms the funnel shape contour on the leads in Fig. 6 (c) and (d). Note that at $V_d = 0$, the appearance of this excess charge distribution is not limited to the drain region but spread randomly without any systematic behaviour identified. Refer to the value of vacuum $V_{cpd} \approx$ -0.25 V in Fig. 4 (e) the ambient $V_{cpd} \approx 0.25$ V, the surface is negatively charged in ambient.

Next, we briefly discuss the transient behaviour presented in Fig. 7. Notably, the characteristic of excessive potential bending we have pointed out in Fig. 4 (c) have been more prominent at the scan just after applying V_d, and then the potential contour and lineshape after 40 minutes becomes much closer to in Fig. 4 (c). In the context of surface charge redistribution discussed above, this observation indicates that (1) a larger amount of surface charges at the channel-lead interfaces have been induced first in application of the voltage across the channel, and (2) there is relatively slow surface charge relaxation mechanism with the time constant from tens minutes to hours. Further systematical studies are under consideration to address these kinds of complex transient behaviours in ambient condition.

Finally, we illustrate the mechanism and result of excess surface charge accumulation in the ambient measurement using a simplified model in Fig. 8. The image in Fig. 8 is made by overlapping the simulated electric field map on top of the potential map. The charges are accumulated in the strong

electric field area as shown in the ambient measurements in Fig. 4 (a) – (c) and Fig. 6. The measurement results indicate that the surface charges are movable but there might be a threshold electric field. The moving charges could stop at the threshold region's boundary. Note that, the V_{cpd} is recorded as energy potential for electron, i.e. the V_{cpd} on the annode is negetive. As a result, the excess positive charges accumulate on the left-hand-side channel-lead boundary where the positive bias is applied, and the excess negative charges on the right-hand-side channel-lead boundary. The result is consistent with Ref. [35], where the cations (anions) are accumulated on the anode (cathode). This assumption is supported by plotting the inherent (simulated) and measured potential profile together in Fig. 8. It is clear that the KPFM potential profile on the drain lead (D) is lower than the simulated value; meanwhile, the KPFM potential on the source lead (S) is higher than the simulated value. The mechanism of charge accumulation is (1) at the source side, the local dipoles (water) are reformed with the direction from the channel to lead so that effective negative charges are accumulated on the lead region just outside the channel, and (2) at the drain side, the local dipoles (water) with the direction from the lead to the channel are induced so that positive charges are effectively accumulated on the lead connected to the channel. The result suggests that abrupt change of the geometrical parameters of nanoscale channel devices can induce additional factors to the potential distribution around the change by interacting with surface charges that are unavoidable when the devices are exposed to the ambient condition. Therefore, the effect should be taken into account in designing down-scaled conducting semiconductor channel sensor devices, in particular as the effect is more prominent in the devices with shorter channel lengths and under a higher electric field. The number density of charge n_q is expressed as $n_q = CV_c/qA$, where V_c is the voltage change due to the charges, q is the unit charge and A is the area for the capacitance. Assuming a simple parallel capacitance model, C is estimated as 1.11 aF for the KPFM tip radius tip of 20 nm and the average distance of 10 nm between the tip and the sample surface. In this geometrical configuration, the 0.2 V of the potential drift observed in Fig. 5 (b) corresponds to an additional negative charge

areal density of 1.1×10^{11} cm^{-2}, which is a reasonable value of excess charge density at the surface of Si [29,30].

5. Conclusion

We have accommodated KPFM to measure SOI-based conducting nanoscale devices under current flow and analysed surface potential maps and profiles taken under various biasing and environmental conditions. The channel resistivity has been estimated from the slope of the KPFM surface potential along the channel and the simultaneous current measurement data of the single device and proved consistent with the wafer-level resistivity evaluation and the conventional analysis of *I-V* measurements of multiple devices. The difference observed in the surface potential maps and profiles taken in ambient condition from those taken in vacuum indicates how the surface charges respond to the internal biasing applied to the conducting channels. By taking account of the simulation results of surface potential and electric field distribution, the characteristic of excessive potential bending found at the interface between channel and leads are caused by the polarisations induced by surface charge redistribution in response to the geometrically concentrated electric field gradient. This effect should be taken into account in measuring the surface potential in ambient and designing nanoscale sensing devices where the surface of semiconductor channels have to be exposed to air or ambient environment for further accurate measurements. To the best of our knowledge, this is the first detailed analysis of the surface potential maps and profiles of the conductive silicon channel under biasing, focusing on the interface with the geometrical change and surface charges.

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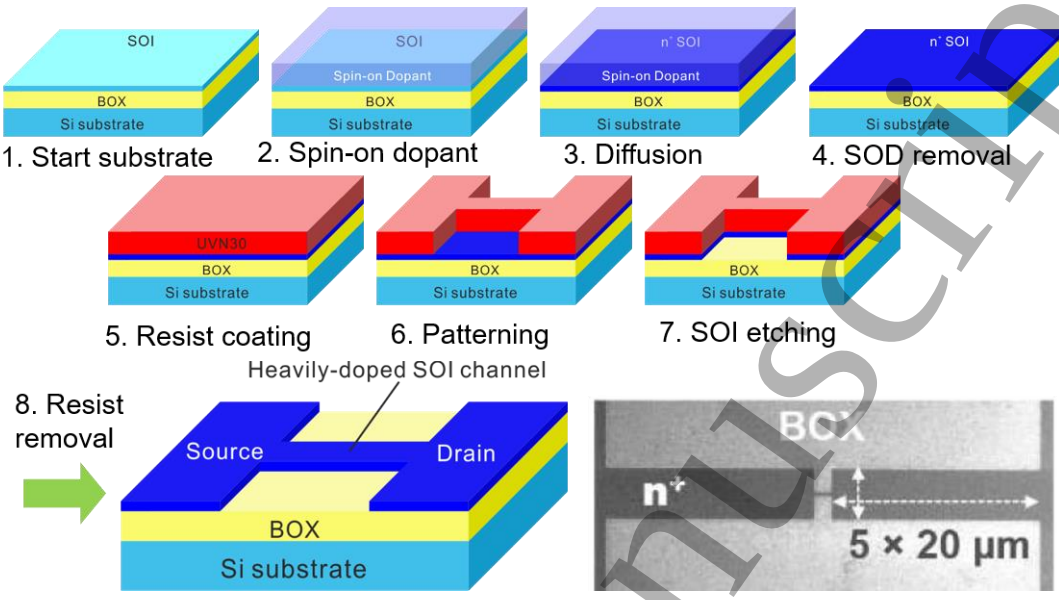

Figure 1. Schematics of fabrication process of heavily-doped conductive SOI channels together with an SEM image of a fabricated device with channel length L = 2 μm and channel width w = 500 nm.

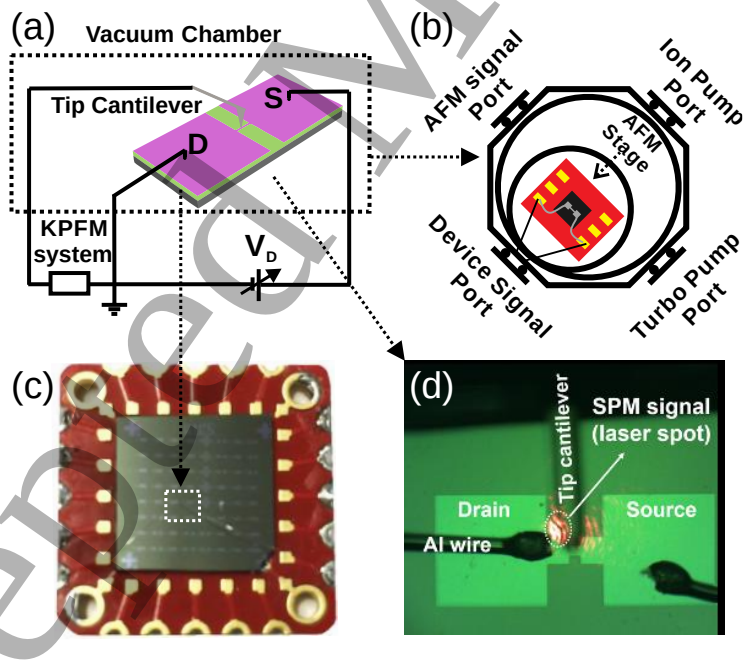

Figure 2. Kelvin Probe Force Microscopy *(*KPFM) measurement system and sample configuration. (a) A schematic diagram of electrical connection of the KPFM measurement system (b) A schematic of the vacuum chamber integrated with the KPFM sample stage. (c) Optical image of a chip holder for electrical connection to the KPFM system. (d) The optical image of a 2 μm device with the KPFM cantilever before scan (during the actual scan the light is off).

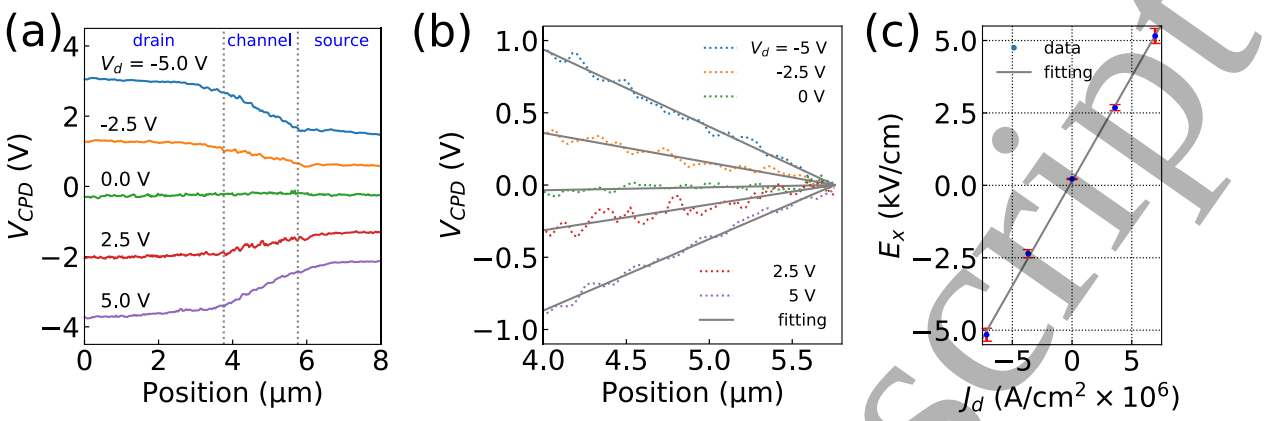

Figure 3. KPFM potential profiles and fitting procedure to extract the resistivity for the device with L = 2 μm: (a) Potential profiles along the channel under different drain bias. (b) The normalised surface potential profiles and linear fitting results of the slope of the potential drop at the channels. The position range shown corresponds to "fitting region" indicated in (a). (c) The potential slope corresponding to the magnitude of the electric field along the channel is plotted as a function of the current density obtained from the simultaneous current measurements. The resistivity, the fitting slope of this plot is estimated 7.2 x 10^{-4} Ω-cm.

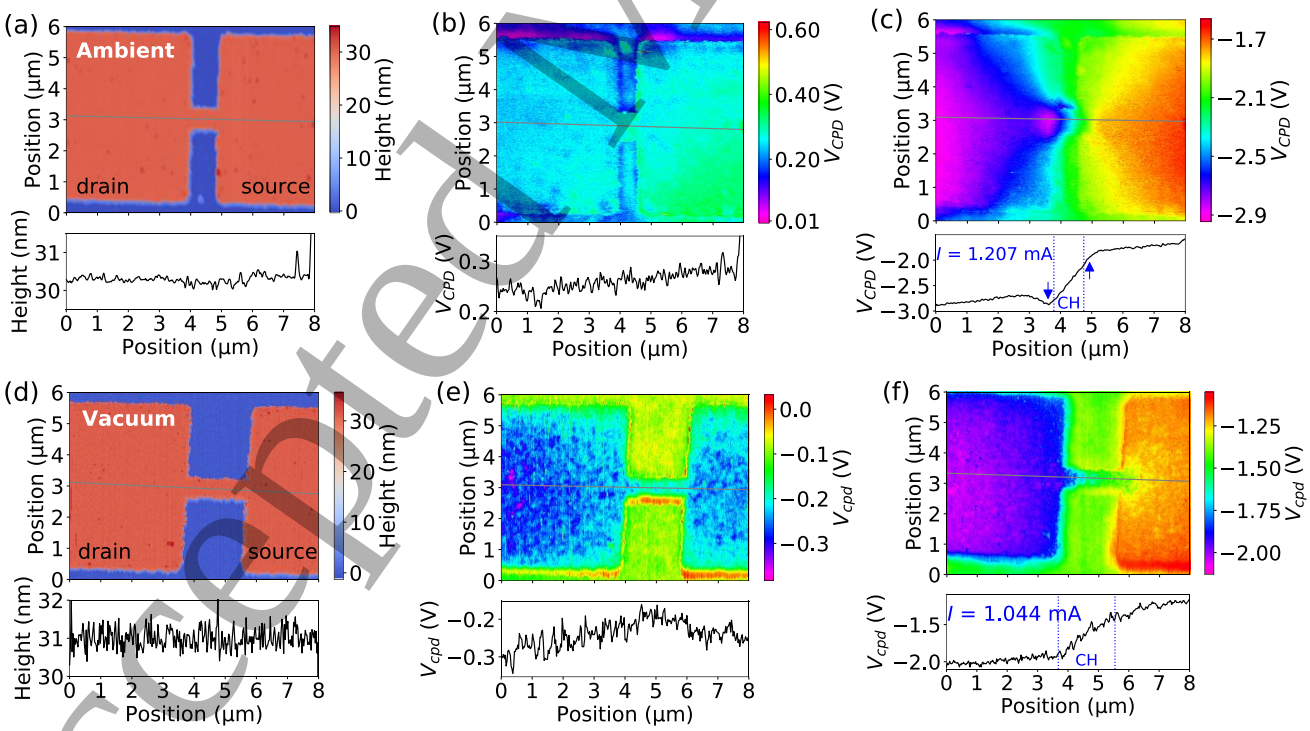

Figure 4. Two dimensional (2D) images together with line scan profiles along the conductive channel (traces are indicated in the 2D maps) for the SOI conducting channels taken under vacuum and ambient environmental conditions. Top row: (a) AFM topography measured at V_d = 0 V, (b) KPFM surface potential at V_d = 0 V and (c) KPFM surface potential at V_d = 5 V taken in ambient condition for the device with the channel length of 1 μm. Arrows in the profile graph in (c) indicate the excessive potential bending in the text. Bottom row: (d) AFM topography measured at V_d = 0 V,

(e) KPFM surface potential at V_d = 0 V and (f) KPFM surface potential at V_d = 5 V taken in vacuum condition for the device with the channel length of 2 μm.

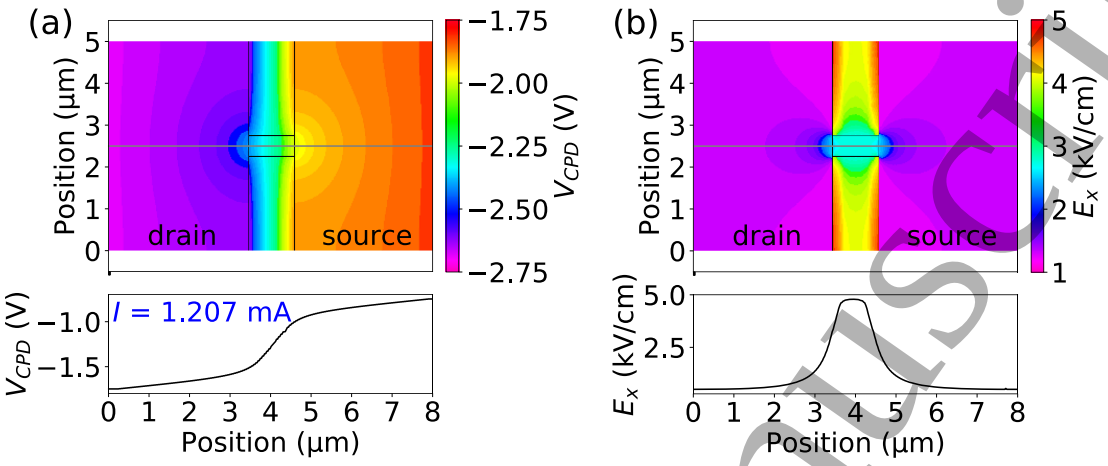

Figure 5. (a) A simulated 2D potential map and corresponding potential profile along the channel indicated in the 2D map are shown for the heavily-doped silicon conductive channel of similar design to the fabricated devices. The dimensions of the Si channel are 0.5 μm in width, 1 μm in length and the doping concentration is set 2.1×10^{20} cm^{-3}. Simulated potential map under V_d = 5 V while the source is grounded. (b) Simulated 2D electrical field map and profile along the channel for the same structure.

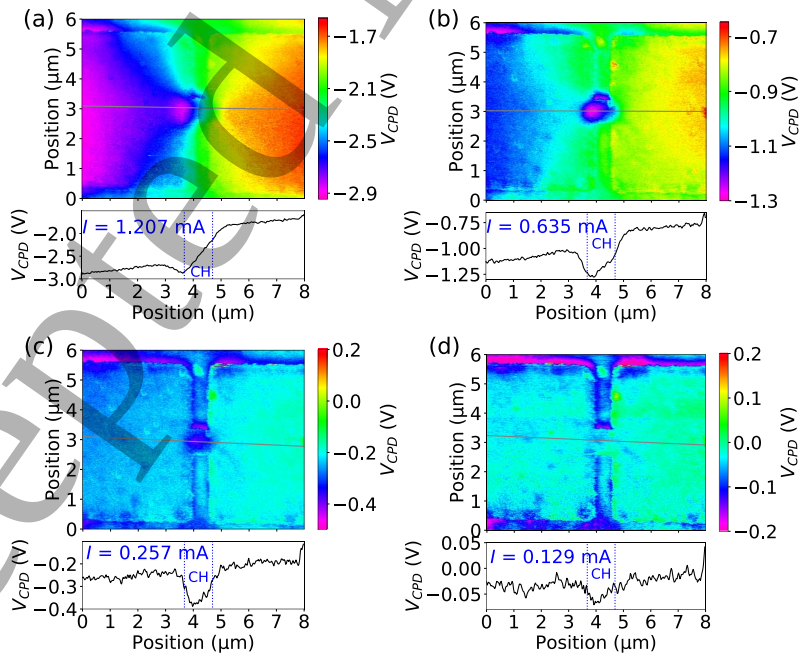

Figure 6. The drain voltage (V_d) dependent potential map for a 1-μm-long channel device with (a) V_d = 5 V (b) V_d = 2.5 V (c) V_d = 1 V, and (d) V_d = 0.5 V, respectively. All the images and profiles are based on the data taken in ambient condition.

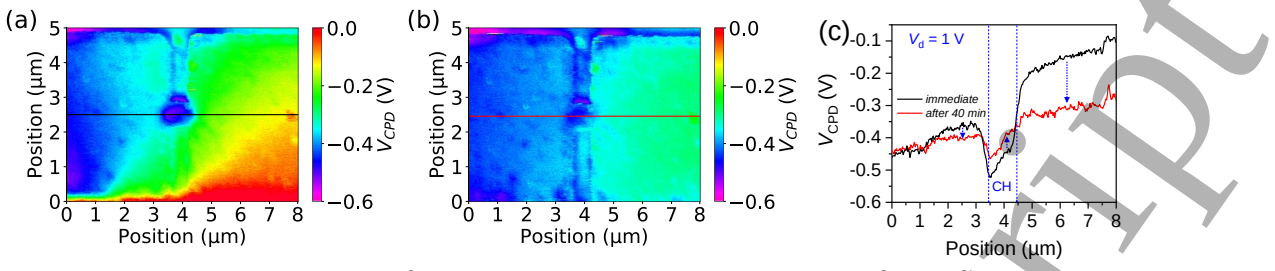

Figure 7. Dynamic behaviour of potential map on 1-μm-long device for V_d fixed at 1 V. (a) potential map taken immediately after reversing V_d from - 5 V to 1V, and (b) subsequent potential map taken 40 minutes after reversing V_d. (c) the potential profile taken from the indicated line in (a) and (b). All the images and profiles are based on the data taken in ambient condition.

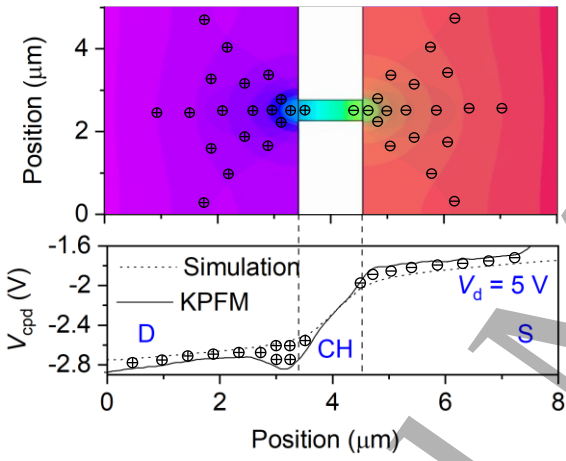

Figure 8. A schematic model of surface charge redistribution. The top image includes the excess positive (+) and negative (-) charge distribution in the area. The bottom graph compares measured and simulated (relative value) potential profiles. The differences can be explained by assuming surface charge distribution associated with to the geometry and electric field distribution.