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Parallel PV Configuration with Magnetic-Free Switched Capacitor Module-Level Converters for Partial Shading Conditions

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Abstract: In this paper, a module-level photovoltaic (PV) architecture in parallel configuration is introduced for maximum power extraction, under partial shading (PS) conditions. For the first time, a non-regulated switched capacitor (SC) nX converter is a used at the PV-side conversion stage, whose purpose is just to multiply the PV voltage by a fixed ratio and accordingly reduce the input current. All the control functions, including the maximum power point tracking, are transferred to the grid-side inverter. The voltage-multiplied PV modules (VMPVs) are connected in parallel to a common DC-bus, which offers expandability to the system and eliminates the PS issues of a typical string architecture. The advantage of the proposed approach is that the PV-side converter is relieved of bulky capacitors, filters, controllers and voltage/current sensors, allowing for a more compact and efficient conversion stage, compared to conventional per-module systems, such as microinverters. The proposed configuration was initially simulated in a 5 kW residential PV system and compared against conventional PV arrangements. For the experimental validation, a 10X Gallium Nitride (GaN) converter prototype was developed with a flat conversion efficiency of 96.3% throughout the power range. This is particularly advantageous, given the power production variability of PV generators. Subsequently, the VMPV architecture was tested on a two-module 500 W_P prototype, exhibiting an excellent power extraction efficiency of over 99.7% under PS conditions and minimal DC-bus voltage variation of 3%, leading to a higher total system efficiency compared to most state-of-the-art configurations.

Keywords: gallium nitride; magnetic-free converters; module-level converters; parallel architecture; partial shading; photovoltaic systems; switched capacitor converters

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1. Introduction

Low-power residential rooftop and façade photovoltaic (PV) systems (in the range of a few kW) are expected to dominate in future distributed energy resources (DERs) and smart grid applications [1]. However, partial shading (PS) in such low-power PV systems, caused by moving clouds, neighboring buildings, trees and other objects, hinders their maximum energy production, especially in urban areas with low installation height [2,3]. In these conditions, the highly shaded panels are bypassed by the integrated antiparallel diodes that protect the panels against hotspot formation and degradation, as described in [4]. According to [5–7], PS is responsible for a reduction of the annual energy yield by 10–20% (depending on the installation type) in building-integrated PVs (BIPVs).

To increase the PV energy production under PS conditions, various software and hardware solutions have been proposed over recent decades. More specifically, building-integrated PV enhanced maximum power point tracking (MPPT) algorithms have been developed, such as particle swarm optimization [8] and artificial bee colony [9], which are

able to distinguish global from local optima of the P-V characteristic. Alternative software techniques presented in [10–12] propose power peak estimation through analytical PV models and parameter extraction via electrical measurements. Although economical and easily applicable, software solutions can only have a limited impact since the shaded modules will still be bypassed or will operate at sub-optimum power point.

On the contrary, hardware solutions can offer a significant improvement in PV generation during PS. Various PV array interconnection schemes have been proposed, namely total-cross-tied (TCT), bridge-link (BL) and honey-comb (HC), that reduce the PS losses in comparison to the conventional series-parallel (SP) architecture [11]. Other studies investigated the physical relocation of individual panels, for applications where the shading pattern is easily predictable [13], or real-time array rearrangement for addressing dynamic changes of the shading conditions [14,15]. These solutions exhibit better performance than the aforementioned static interconnection schemes but require a large number of switching devices and a complex network of voltage/current or irradiance sensors, while local optima will still exist in non-uniform insolation conditions.

The most effective hardware solution for PS loss mitigation relies on module-level power electronics (MLPEs), which aim to maximize the power yield of each individual panel through dedicated MPPT. In this field, micro-inverter topologies have proven commercially successful, since they offer the flexibility to connect any number of PV modules directly to the AC grid [16]. However, they exhibit low power density, due to the large component count and filter requirements imposed by the strict grid-interface regulation [17], and limited capability to provide ancillary services, which is a prerequisite for future DERs [18]. Another popular MLPE alternative uses PV power optimizers (PVPOs), which are buck-boost DC-DC converters, integrated with the solar panels of a typical string arrangement [19]. According to the study performed in [5], PVPOs have lower long-term efficiency compared to micro-inverters and reduced expandability, due to the minimum required string length [20]. The same limitations hold true for the distributed power processors [21] and voltage equalizers [22], that are connected between two panels in a string configuration.

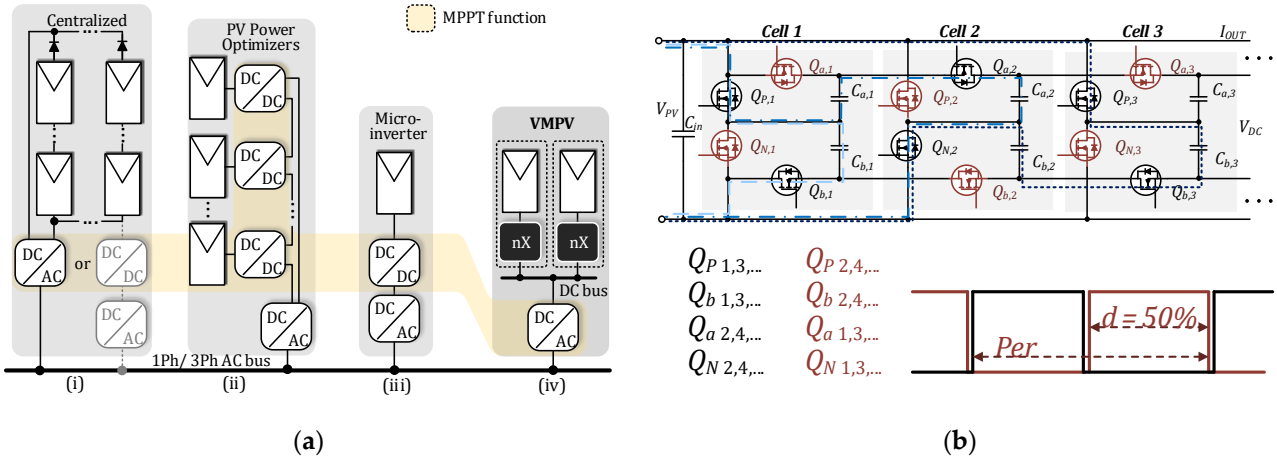
To overcome the aforementioned limitations of the conventional MLPE approaches, an alternative promotes micro-converters that allow parallel connection of the PV modules in a single DC-bus, through high step-up DC-DC converters [23]. This solution aims to exploit the clear advantages of parallel configuration for addressing PS effects [24]. Converter topologies with a large voltage boost ratio have been proposed for the interface between the low-voltage PV module and the high-voltage DC-bus, including cascade boost [23], coupled inductors [25], switching capacitors [26] and combinations of the above [27–29]. However, these topologies are known to require complicated control algorithms [15] and, most importantly, employ electrolytic capacitors and magnetic components that limit the power density and the lifetime of the system, as found in [16,17]. They also exhibit a significant efficiency drop in low loading conditions, which is a drawback, given that a PV generator operates within 30–80% of its nominal power for 80% of the time [30].

Therefore, there is a clear need for a new MLPE system that addresses PS effects in rooftop PV systems and façade BIPVs, with a high boost ratio, high efficiency throughout the power range and simple structure and controllability. In this paper, we aim to satisfy these requirements by introducing a new PV architecture, based on the parallel connection of fixed-step, per-panel micro-converters. To the best of the authors' knowledge, it is the first time that a magnetic-free switched capacitor (SC) "*voltage amplifier*" has been used as a front-end conversion stage of a parallel PV configuration. It is a hybrid solution that combines the expandability of micro-inverters and the control simplicity of a single-stage grid-side inverter. The new approach exhibits (a) a high conversion efficiency of 96.3% even at low loading, (b) an excellent extraction efficiency of 99.7% under severe partial shading, (c) a high power density due to the omission of magnetic components and electrolytic capacitors and (d) limited DC-bus voltage variation with the operating conditions.

The operating principles of the novel PV architecture are explained in Section 2, followed by simulation results on a 5 kW grid-connected residential PV system in Section 3. The design, development and experimental validation of a 500 W prototype are presented in Section 4. The main conclusions of this work are summarized in Section 5.

2. Proposed Module-Level PV Architecture

The foundation of the new approach relies on the combinations of a non-regulated high step-up micro-converter with each PV panel, to form a high-voltage/low-current building block. All the voltage-multiplied PV (VMPV) modules are connected in parallel at the input of the grid-side inverter, which simultaneously regulates the operating point of all PV panels with a central MPPT. A simplified block diagram of the proposed VMPV architecture against the centralized and conventional MLPE configurations, such as microinverters and PVPOs, is presented in Figure 1a. For every architecture, the converter responsible for the MPPT is highlighted with a yellow background. This reveals a unique feature of the proposed system: that the MPPT is not performed by the DC-side converter, but is shifted to the grid-side inverter, as will be explained in Section 2.2. The schematic of the SC converter, which will be described in detail in the following subsection, is shown in Figure 1b.



(**a**) (**b**)

Figure 1. (**a**) PV architectures, including (**i**) central inverter, (**ii**) PVPOs (**iii**) micro-inverters and (**iv**) the proposed VMPV architecture. (**b**) Schematic diagram of the magnetic-free SC voltage amplifier.

The effect of the PV module voltage amplification can be viewed as "*stretching*" the output I-V characteristic to higher voltages and lower currents, while keeping the produced power constant, as shown in Figure 2. The multiplication factor, n, should be higher than the V_{DC}/V_{MP} ratio, where V_{DC} is the required DC-link voltage for grid integration (e.g., 400 V) and V_{MP} is the nominal PV panel voltage at MPP (e.g., 40 V). Each module contributes additively to the total system output by injecting the power that corresponds to the common DC-voltage, i.e., $P_{PV\text{-}j}(V_{PV\text{-}j} = V_{DC}/n)$, where $P_{PV\text{-}j}$ and $V_{PV\text{-}j}$ are the output power and voltage, respectively, of the j panel.

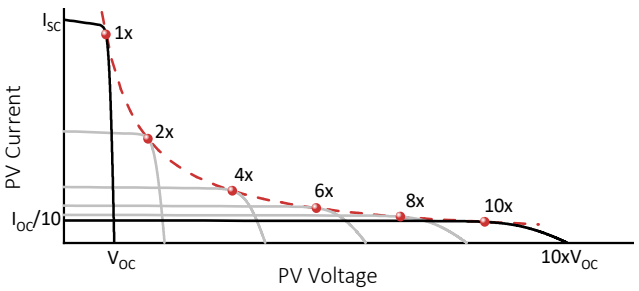


Figure 2. Modified I-V characteristic at the output of the voltage-multiplied PV module.

The operating principles of the two stages are presented in the following subsections, along with a short discussion on the advantageous features of the new layout.

2.1. PV-Side Voltage Multiplier

The voltage amplification function can theoretically be performed by any topology from the high step-up converter family mentioned in the Introduction. However, these solutions would add unnecessary complexity to the system and increase its size and weight, given that no voltage regulation is required. As an alternative, we propose the use of the nX converter, first introduced in [31], which combines high power density with high conversion efficiency and a fixed voltage ratio. This feature come with the omission of all magnetic components and the modular structure. The fixed boost ratio is not a limitation for this application, given the inherently small voltage variation of the MPP with the environmental conditions, as will be shown in the simulation and experimental results.

An example of a six-times boost nX converter ($n = 6$) is depicted in Figure 1b. The power devices constituting the nX converter can be grouped in two sets: the Q_P and Q_N that are always connected to the input and form a bridge leg configuration, and the ones at the top and bottom rail, Q_a and Q_b, that form a series connection between the different cells. The transistors are driven by a complementary switching pattern with a fixed 50% duty cycle, as indicated in Figure 1b, corresponding to the two operating modes: transistors in black conduct in the first operating mode, while the ones depicted in red conduct in the second operating mode. The same pattern holds for any number of cells.

The different current paths during the first operating mode are indicated with blue lines in Figure 1b. More specifically, when transistors $Q_{P\ 1,3}$, $Q_{b\ 1,3}$, $Q_{N\ 2}$ and $Q_{a\ 2}$ are conducting, three current paths are formed simultaneously:

1. the input voltage source is directly connected across C_{b1} (dashed blue line),
2. the source is connected in series with C_{a1} to charge capacitor C_{a2} (dash–dot blue line), and
3. the source is connected in series with C_{b2} to charge capacitor C_{b3} (dotted blue line).

In general, the output capacitors of each cell, $C_{a(i)}$ and $C_{b(i)}$, are charged by connecting the capacitor of the previous cell $(i - 1)$ in series with the input voltage, V_{PV}, as described in (1).

$$V_C(i) = V_C(i - 1) + V_{PV}, \qquad 1 < i \leq n/2 \tag{1}$$

Applying (1) to successive cells, the voltage stress across the top and bottom rail power devices can be deduced and is equal to $2{\cdot}V_{PV}$. The only exception to this rule holds for the first cell, in which $V_{DS\text{-}a,b}(1) = V_{PV}$. On the other hand, transistors Q_P and Q_N are always connected to the input power source, hence $V_{DS\text{-}P,N}(\mathrm{i}) = V_{PV}$. Provided that the current flowing through each path is equal to the output current, I_{OUT}, it can be easily observed that the current stress of the top and bottom rail transistors is $I_{D\text{-}a,b}(i) = I_{OUT} = I_{PV}/n$ and for transistors Q_P and Q_N it is $I_{D\text{-}P,N}(i) = 2{\cdot}I_{OUT} = 2{\cdot}I_{PV}/n$. An exception to this rule is the last cell, where $I_{D\text{-}P,N}(n/2) = I_{OUT}$. These equations give an indication of the devices' stress and help select the components for the experimental validation in Section 4.1.

An advantage of the nX converter topology is that there is no need for a feedback control loop and, thus, no requirements for voltage/current sensors, micro-controllers and communication links. Additionally, the simplicity of the pulse width modulation (PWM) strategy allows for a cost-effective PWM integrated circuit (IC) generator, as opposed to a costly microprocessor. Further, the converter inherently operates under soft switching conditions, resulting in low switching losses, as explained in [32,33].

In its current form, the presented nX converter has a high transistor count ($2{\cdot}n$). However, state-of-the-art Gallium Nitride (GaN) technology offers a unique potential for the monolithic integration of multiple devices on a single power chip [34]. In addition to that, the high switching frequency capability of the high electron mobility transistors (HEMTs) allows for the replacement of electrolytic capacitors, which is the most common point of failure [16,17], with robust and efficient ceramic capacitors. This technology migration improves the lifetime of the micro-converter to match that of the solar panels (more than

25 years), an important requirement for rooftop and BIPV systems. The small footprint and low driving requirements of GaN devices further contribute to the miniaturization of the micro-converter, as presented in [35].

By adopting the GaN transistor technology in a magnetic-free converter topology, an ideal platform for future VMPV modules can be developed.

2.2. Grid-Side Inverter

Regulation of the operating point of a PV module, string or system is traditionally performed by the front-end converter, as indicated by the highlighted area in Figure 1a. In this study, the fixed voltage ratio at the PV-side requires that the MPPT function is performed by the grid-side inverter, much like a single-stage system. Therefore, although the proposed topology is fundamentally a two-stage system, it operates like a single-stage centralized system in terms of MPPT function, but with higher MPP tracking efficiency. Specifically, the merits of this new architecture are:

1. The entire PV system always has a single MPP, even under mismatched irradiance and temperature conditions, due to the parallel connection of the VMPVs. As a result, no PV module is bypassed and the MPP is always successfully tracked, as opposed to the multi-peak P-V curves in centralized architectures, leading to almost 100% power extraction efficiency under any partial shading conditions.
2. The DC-link voltage variation is limited due to the inherently small deviation of V_{MP} with the environmental conditions. This makes it easy for the inverter to extract the maximum power while meeting the input voltage requirements, in contrast to single-stage systems under PS.
3. Having a single grid-side inverter permits the implementation of sophisticated control functions, such as ancillary services to the grid (e.g., fault ride through, reactive power injection, frequency regulation), as opposed to the micro-inverters that cannot afford such complexity.

3. Modeling and Simulation

In this section, the power extraction efficiency of the proposed architecture under PS conditions is assessed against conventional PV configurations, through simulations in Matlab/Simulink. First, it is important to define the total system efficiency, η_{sys}, as the product of conversion efficiency, η_c, and extraction efficiency, η_{ext} (also found in the literature as tracking or MPPT efficiency):

$$\eta_{sys} = \eta_c \cdot \eta_{ext}. \tag{2}$$

$$\eta_{ext} = P_{PV}/P_{TOT} = P_{PV}/\left(\Sigma_1^N P_{MPj}\right) \tag{3}$$

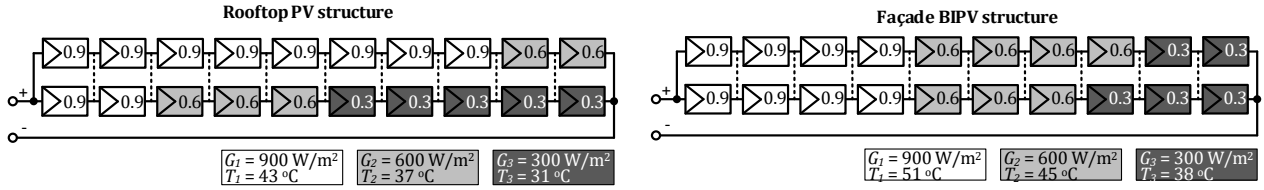
η_c represents the hardware's efficiency to convert the power from the PV-side to the grid-side and will be discussed in Section 4. η_{ext} is given as the ratio of the average output power of the PV system, P_{PV}, to the total available power from all individual modules, P_{TOT}, as shown in (3), for N panels. This efficiency factor represents the ability of the architecture to extract as much of the available power as possible, regardless of the converters/electronics used. The reduction of η_{ext} is usually attributed to three factors: (a) shaded modules operating at a sub-optimal operating point or completely bypassed, (b) MPPT locked on a local maximum and (c) MPPT oscillating around the normal operating point. For a fair comparison of the VMPV with other conventional architectures, only component (a) of η_{ext} should be considered. Thus, for the rest of the paper, it is assumed that the MPPT algorithm can always find the global maximum, even in the case of multiple power peaks at PS, with negligible oscillation around the MPP.

To extract η_{ext} for any PV configuration in real time, the PV model described in [10] is used, that expresses the module voltage and current in explicit form.

3.1. PV Generator Configuration Comparison

The focus of this sub-section is to study the extraction efficiency of the parallel-connected VMPV architecture under PS conditions against the conventional SP and TCT interconnection schemes, the TCT configuration with dynamic rearrangement capability [14] and the ideal MLPE architecture. A 5 kW_P residential (rooftop or façade) PV system of 20 panels is considered. Each PV module consists of 72 cells and has V_{OC}(STC) = 53 V and V_{MP}(STC) = 44.3 V, to match the characteristics of the commercial VBHN245SJ25 panel. A 10X step-up conversion ratio for the VMPV architecture is adequate for integration to the single-phase grid.

Two realistic shading patterns are examined, inspired by [14] and depicted in Figure 3. Solid lines show the SP configuration and dashed lines represent the TCT interconnection scheme.



(**a**) (**b**)

Figure 3. Indicative PS scenarios. (**a**) Long–narrow shading pattern A and (**b**) short–wide shading pattern B.

3.1.1. Shading Pattern A: Long–Narrow

In this case, the shadow covers the majority of one string of a rooftop PV structure, giving rise to three irradiance intensity levels, G_1 = 900 W/m^2, G_2 = 600 W/m^2 and G_3 = 300 W/m^2, as shown in Figure 3a. An ambient temperature of 20 °C and wind speed of 1 m/s are considered, according to the international standard IEC-61215. The nominal operation cell temperature (NOCT) has been extracted from [36], considering both the photoelectrical and photothermal conversion effect, and is included in Figure 3. Solid lines show the SP configuration and dashed lines represent the TCT interconnection scheme.

The simulation results for this case study are presented in Figure 4. The gray dashed line in Figure 4b corresponds to the total PV system available power, P_{TOT}, calculated by adding the maximum available power of all modules, P_{MPj}, j = 1, . . . , 20, as in (4) and (5) for the shading patterns A and B, respectively. P_{TOT} is used as a benchmark in the architecture comparison.

$$P_{TOT-A} = \Sigma_1^{20} P_{MPj} = 10 \cdot P_{MP(0.9)} + 5 \cdot P_{MP(0.6)} + 5 \cdot P_{MP(0.3)} = 3.17 \text{ kW} \quad (4)$$

$$P_{TOT-B} = \Sigma_1^{20} P_{MPj} = 8 \cdot P_{MP(0.9)} + 7 \cdot P_{MP(0.6)} + 5 \cdot P_{MP(0.3)} = 3.04 \text{ kW} \quad (5)$$

It is evident that both SP and TCT configurations exhibit poor extraction efficiencies of 73.59% and 74.94%, respectively, due to the bypassing of the shaded modules. On the other hand, the dynamic rearrangement of the panels significantly improves the efficiency to 93.12% and reduces the number of local maxima to two. However, it is the proposed VMPV architecture that achieves the best extraction efficiency of 99.86% with just a single global MPP.

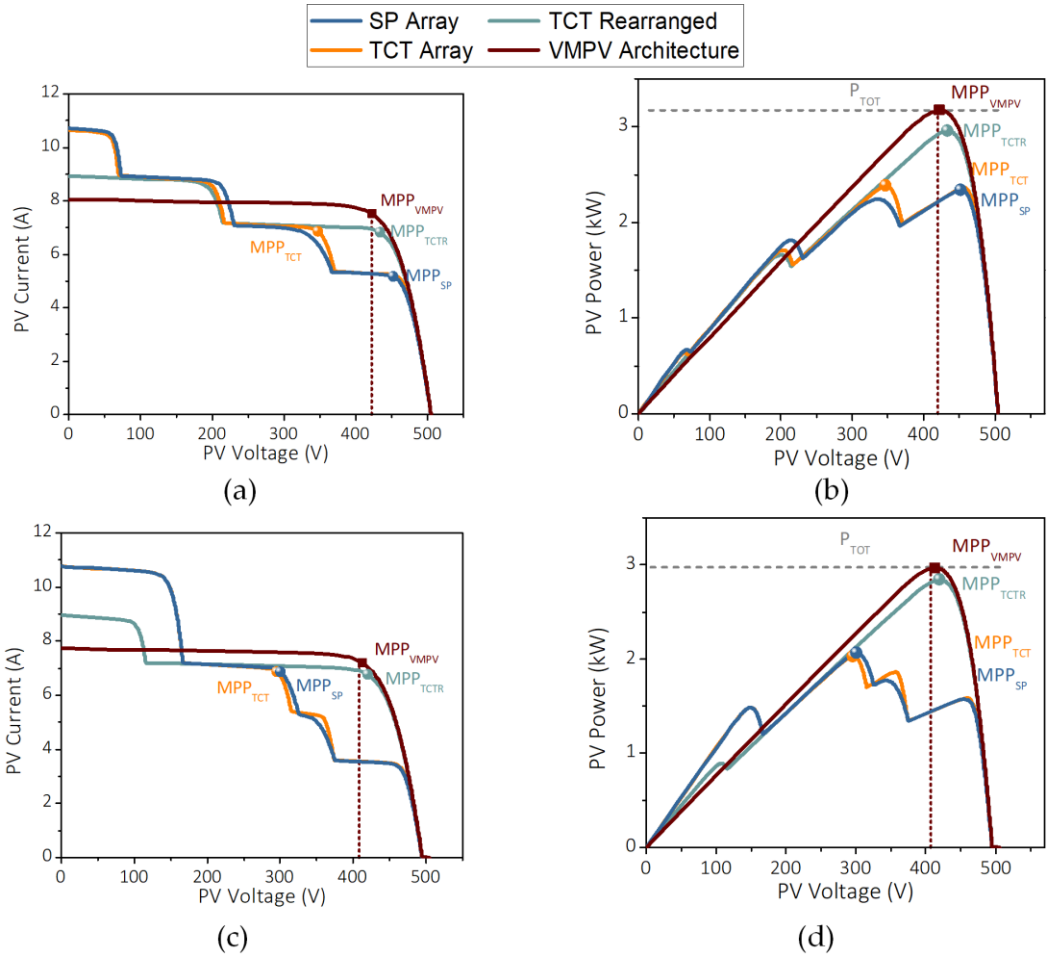


Figure 4. I-V and P-V curves of the examined PV architectures under (**a**,**b**) the shading pattern A and (**c**,**d**) the shading pattern B.

3.1.2. Shading Pattern B: Short–Wide

This scenario concerns a façade PV system, partially shaded by the pattern illustrated in Figure 3b. In contrast to an open rack rooftop structure, the BIPVs are characterized by a higher temperature (included in Figure 3b), since only one side of the panel is in contact with the air. The output I-V and P-V characteristics for the shading pattern B are presented in Figure 4c,d. Even under these highly non-uniform irradiance and temperature conditions, the VMPV architecture still exhibits a near-perfect efficiency of 99.8%. As a comparison, the SP and TCT interconnection schemes have η_{ext}(SP) = 69.4% and η_{ext}(TCT) = 68.3%, respectively, while the electrically rearranged TCT array has η_{ext}(TCTR) = 95.5%.

3.2. Grid-Connected VMPV System

To evaluate the time response of the whole system under variation of the atmospheric conditions, the proposed PV architecture is connected to a single-phase grid-side inverter. Two scenarios are simulated, where the PV structure is initially uniformly insolated (G_1 = 900 W/m^2) and gradually shaded to match shading pattern A or shading pattern B. A linear drop of the irradiance is considered (see Figure 5), at a rate of 25 W/m^2 per second, which is a representative value for rapidly changing environmental conditions [18]. The temperature variation of the individual PV groups is shown in Figure 5b, for both investigated shading patterns A (continuous lines) and B (dashed lines).

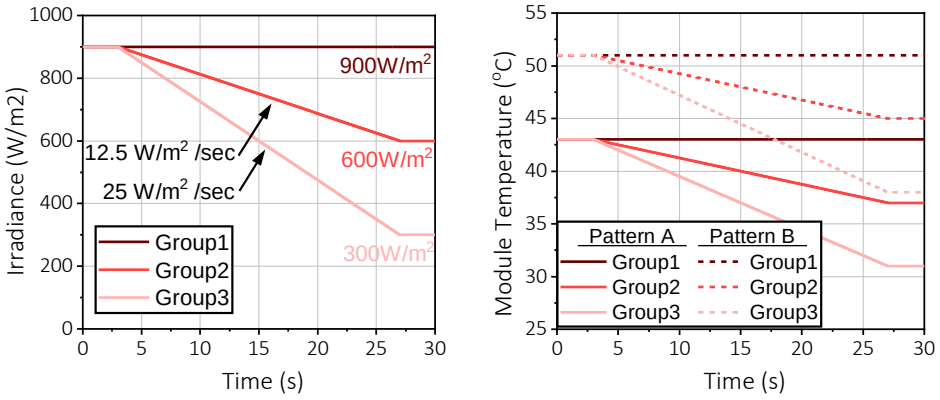


Figure 5. (**a**) Irradiance and (**b**) temperature variation with time for the three PV groups of the VMPV architecture.

The inverter control is structured in three nested control loops, as outlined in Figure 6, [37]. The outer control loop is a perturb and observe (P&O) MPPT that is applied at the common high-voltage DC-bus and produces the reference DC-voltage, V_{DC}*. In the middle control loop, a PI controller regulates the active and reactive power reference to be injected to the grid, P* and Q*, respectively. A proportional resonant (PR) current controller is implemented in the inner control loop and the grid frequency is extracted by a second-order generalized integrator phase locked loop (SOGI-PLL).

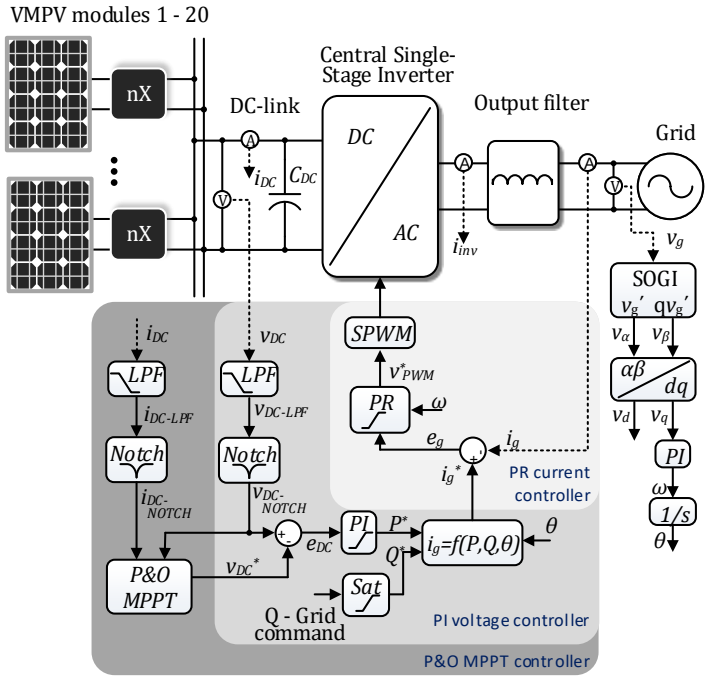
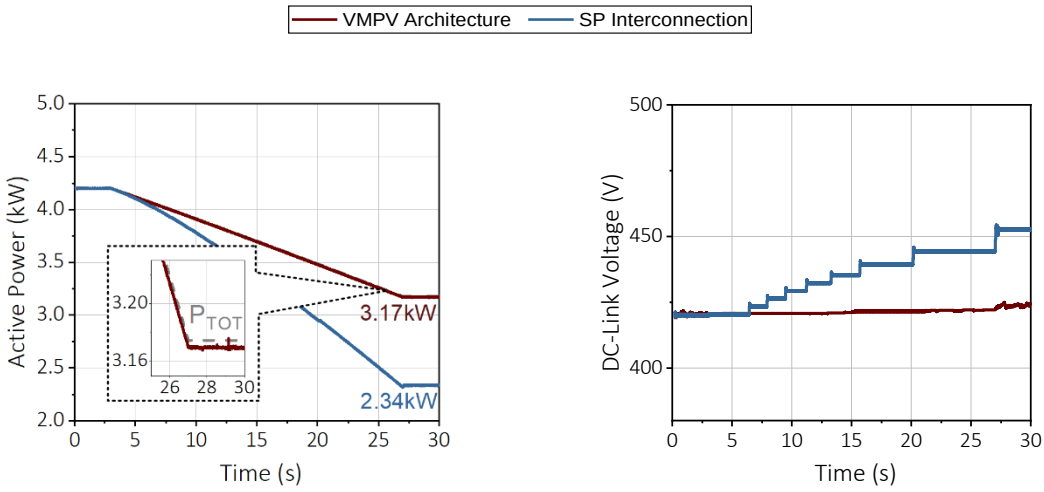


Figure 6. Complete control scheme of the proposed grid-connected PV system, consisting of three nested control loops.

Figure 7a shows the active power fed to the grid, P_{OUT}, with respect to the total available PV power, P_{TOT}. The new VMPV architecture follows closely the benchmark curve, even when all the shaded panels have reached their steady state conditions (Time > 27 s). For comparison purposes, the output power of the conventional SP interconnection is also included in the same figure. Notably, the DC-link voltage variation is limited to a range of just 4 V (from 420 V to 424 V) in the VMPV case, as can be seen in Figure 7b, despite the

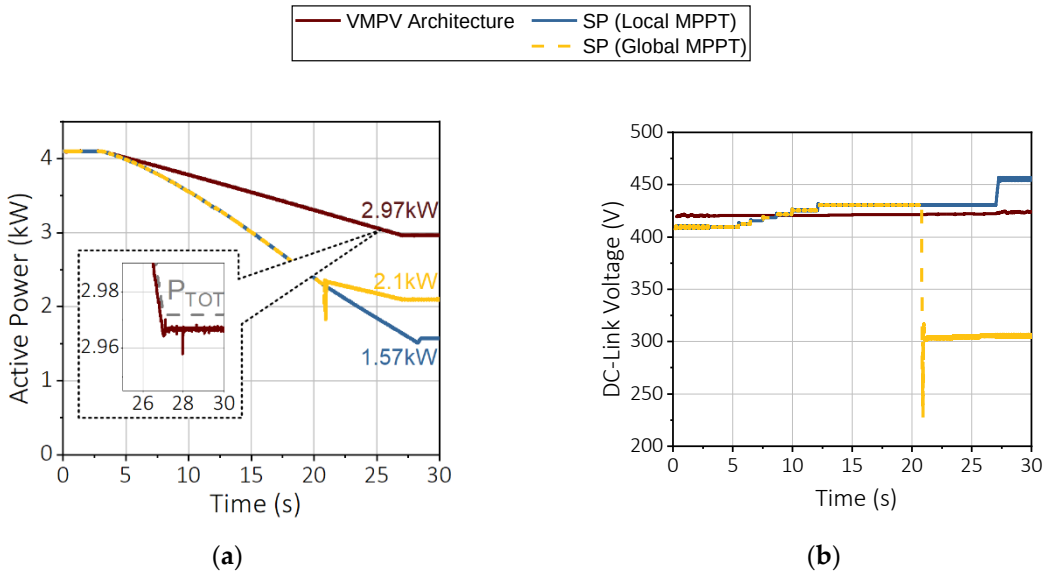
significant variation of the produced power. In contrast, the voltage variation of the SP configuration is 33 V for the same shading pattern.



(**a**) (**b**)

Figure 7. (**a**) Active power fed to the grid and (**b**) DC-bus voltage variation with time for the proposed VMPV under shading pattern A.

Similarly, Figure 8 shows the power and voltage variation of the proposed VMPV and standard SP architectures when the shading evolves towards shading pattern B. This scenario better highlights the merits of a single MPP in the proposed parallel connection against the multiple peak formation in conventional SP configurations and the challenges in identifying the global one. Even if a sophisticated MPPT algorithm is employed that always converges to the global MPP (yellow dashed curves), the respective DC-link voltage (300 V in Figure 8b) may be outside the inverter limits, thus not allowing operation at the MPP, leading to even lower extraction efficiency.



(**a**) (**b**)

Figure 8. (**a**) Active power fed to the grid and (**b**) DC-bus voltage variation with time for the proposed VMPV under shading pattern B.

The simulation results show that the proposed VMPV architecture combines the best of MLPE and centralized topologies: it yields near-optimal power extraction (like MLPE,

in contrast to centralized) while allowing for sophisticated control functions in the inverter (like centralized, as opposed to micro-inverters).

4. Experimental Validation

In this section, the favorable operation of the VMPV architecture under uniform and PS conditions is experimentally validated and compared to a conventional string configuration.

4.1. Experimental Setup

Two 245 W_P PV modules of the same type, VBHN245SJ25, are used as inputs to two nX converters that are connected in parallel at the high-voltage side, as depicted in Figure 9. Throughout the experiment, both PV panels are placed close to each other on a structure of fixed inclination with respect to the horizon. Semi-transparent fabric is used to cover one PV module completely and uniformly to emulate PS conditions.

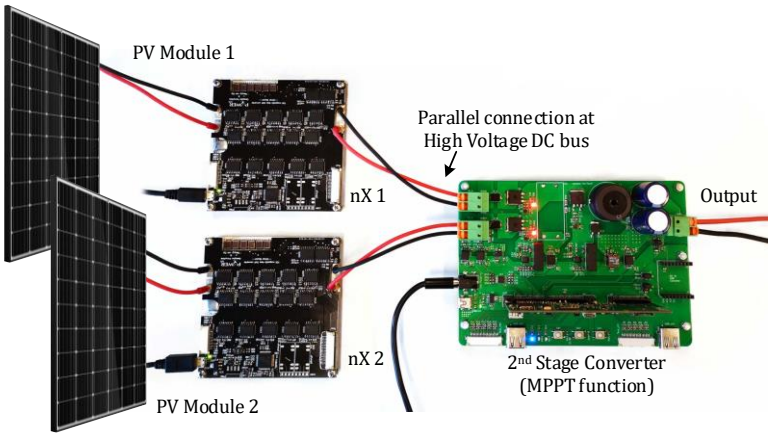


Figure 9. Experimental setup consisting of two VMPV modules.

The objective of these experiments is to study the first stage of the system independently from the topology of the second stage. To this end, a DC-DC converter that performs all control functions, including scanning of the PV curves and MPPT, feeding a resistive load, was used as a simple substitute of the grid-tied inverter. This setup allows for safe and repetitive testing of the new architecture, while the results are also valid for the grid-connected system. The switching frequency of the buck converter was set to 20 kHz and the MPPT period to 250 ms. All voltage and current measurements were continuously monitored with a sampling rate of 4 k samples/s and then filtered via a digital low-pass filter (LPF) with a cutoff frequency of 100 Hz to reject the switching noise. The key components and parameters of the experimental setup are summarized in Table 1.

4.2. PV-Side nX Converter

The backbone of the new architecture is the GaN-based magnetic-free nX converter, depicted in Figure 10. It has a 10-times step-up ratio to match the simulation conditions in Section 3. The developed prototype consists of two separate printed circuit boards (PCBs): the drive board, shown in Figure 10a, and the power board, in Figure 10b. One side of the power PCB is reserved only for the GaN HEMTs, a design aspect that provides flexibility to mount the board on any flat surface, such as a heat sink or the backside of the PV panel. Four parallel-connected multilayer ceramic capacitors (MLCCs) of 2.2 μF each, with low internal series resistance (ESR), constitute the output capacitance of each cell.

Table 1. List of components of the experimental setup.

Component	Parameter	Value
PV modules	Part Type	VBHN245SJ25
	V_{MP}	44.3 V
	I_{MP}	5.53 A
	V_{OC}	53 V
	I_{SC}	5.86 A
Module-level nX converter	Transistors in $Q_{P/N}$ position	GS61008T
	Transistors in $Q_{a/b}$ position	GS66508T
	Switching capacitors	4 × 2.2 µF, X6S
	Gate driver	LM5114
	Digital/Power isolator	ISOW7842F
2nd-stage DC-DC converter	Series diodes	S10KC
	$L_{DC\text{-}DC}$	1.5 mH
	$C_{DC\text{-}DC}$	50 µF
	Transistor	IPB65R190CFD
	Switching diode	C3D08065E
	Micro-controller	TMS320F28379D
	Switching frequency ($F_{SW\text{-}B}$)	20 kHz
	MPPT period (T_{MPPT})	250 ms
	Voltage/Current sampling rate	4 k samples/s
	LPF cutoff frequency (F_0)	100 Hz
Output Resistor	R_{out}	0–240 Ω

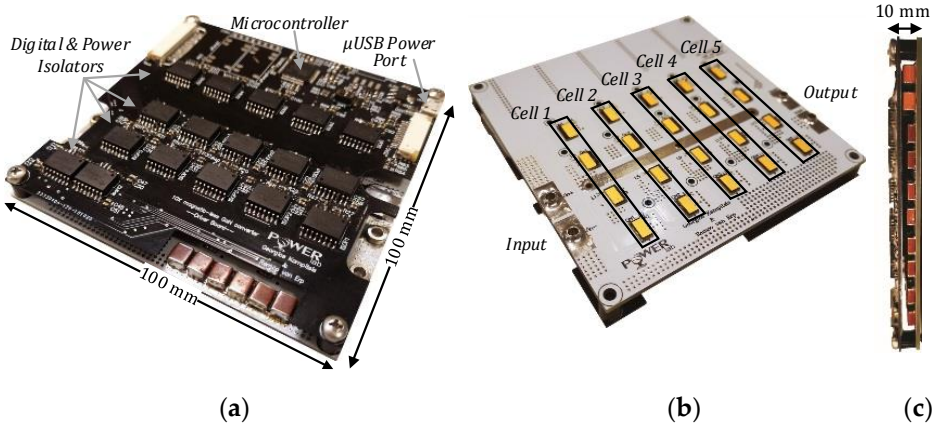
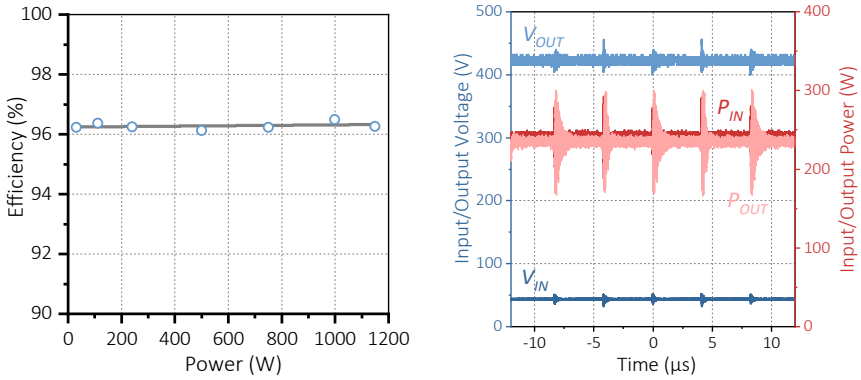


Figure 10. (**a**) Front side—drive board, (**b**) back side—power board and (**c**) side view of the magnetic-free nX converter prototype.

The switching frequency is tuned to match the circuit resonant frequency, $F_{SW\text{-}nX}$ = 200 kHz, to achieve zero current switching (ZCS) operation and, thus, minimize the switching losses. The entire converter occupies just 100 mL of volume (100 mm × 100 mm × 10 mm) and has a fixed conversion efficiency of 96.3%, throughout the power range, as shown in Figure 11a. This is a strong point of this converter that ensures a high energy yield, even under low irradiance conditions. In contrast, other high step-up micro-converters exhibit efficiencies that peak from 94–98% [25,27,29], but drop significantly (below 90%) in low loading conditions, due to higher switching losses from entering discontinuous conduction mode or exiting the soft switching window. On the other hand, the magnetic-free nX converter is always operating at a fixed 50% duty cycle, and is inherently operating under soft switching, as explained in [32]. Please note that the calculated conversion efficiency does not account for any losses from the grid-side inverter or the output filter, which is expected to introduce a non-linearity to the total system efficiency curve at light loads. It should be mentioned

that the conversion efficiency can be further improved by choosing GaN HEMTs with even lower on-resistance and faster switching transients.



(**a**) (**b**)

Figure 11. Experimental results of the developed 10X converter. (**a**) Efficiency curve over operating power and (**b**) voltage and power waveforms during operation at 250 W.

Voltage and power waveforms of the system operating at 250 W are illustrated in Figure 11b. Under these conditions, the temperature increase in the transistors was maintained below 15 °C, avoiding the use of bulky heat sinks. More design details and considerations regarding the component selection and test conditions can be found in [35]. The high power density (greater than 11 kW/l) and the low cooling requirements are both key factors that enable the integration of the nX converter with the solar panel.

4.3. Output Characteristics of the VMPV System

The I-V and P-V characteristics of the proposed PV system were recorded in two shading patterns: (A) uniform irradiance and temperature conditions and (B) partial shading, where one panel is uniformly shaded while the other one remains unshaded. The curves are captured by slowly changing the operating point within 5 s (scanning), which guarantees that the measurements are not affected by transient phenomena attributed to the second-stage inductance and output capacitance.

Figure 12a,b show the characteristic curves of the two individual PV modules (dashed and dash–dot lines) and the combined curve of the proposed VMPV architecture (solid red line), under uniform irradiance and temperature conditions. It should be noted that, although the parallel connection takes place at the high-voltage side of the nX converters, the I-V and P-V characteristics are translated to the PV-side for consistency with the string topology (blue line).

As shown in Table 2, the two modules are not identical and their MPPs differ by 3.4 W and are spaced by 1.17 V. However, the power loss of the VMPV approach is just 0.4 W, resulting in an excellent extraction efficiency of 99.9%. In fact, both modules operate at 99.9% of their respective MPPs. In this scenario, the string arrangement also has near-perfect extraction efficiency but no conversion losses. It should be noted that the total available PV power $P_{TOT} = P_{MP1} + P_{MP2}$ and the actual extracted power P_{PV} are measured in successive experiments within a short time duration to ensure equal irradiance and temperature conditions; it is impossible to measure the maximum available power of the individual modules when they form a PV string that operates at a different operating point.

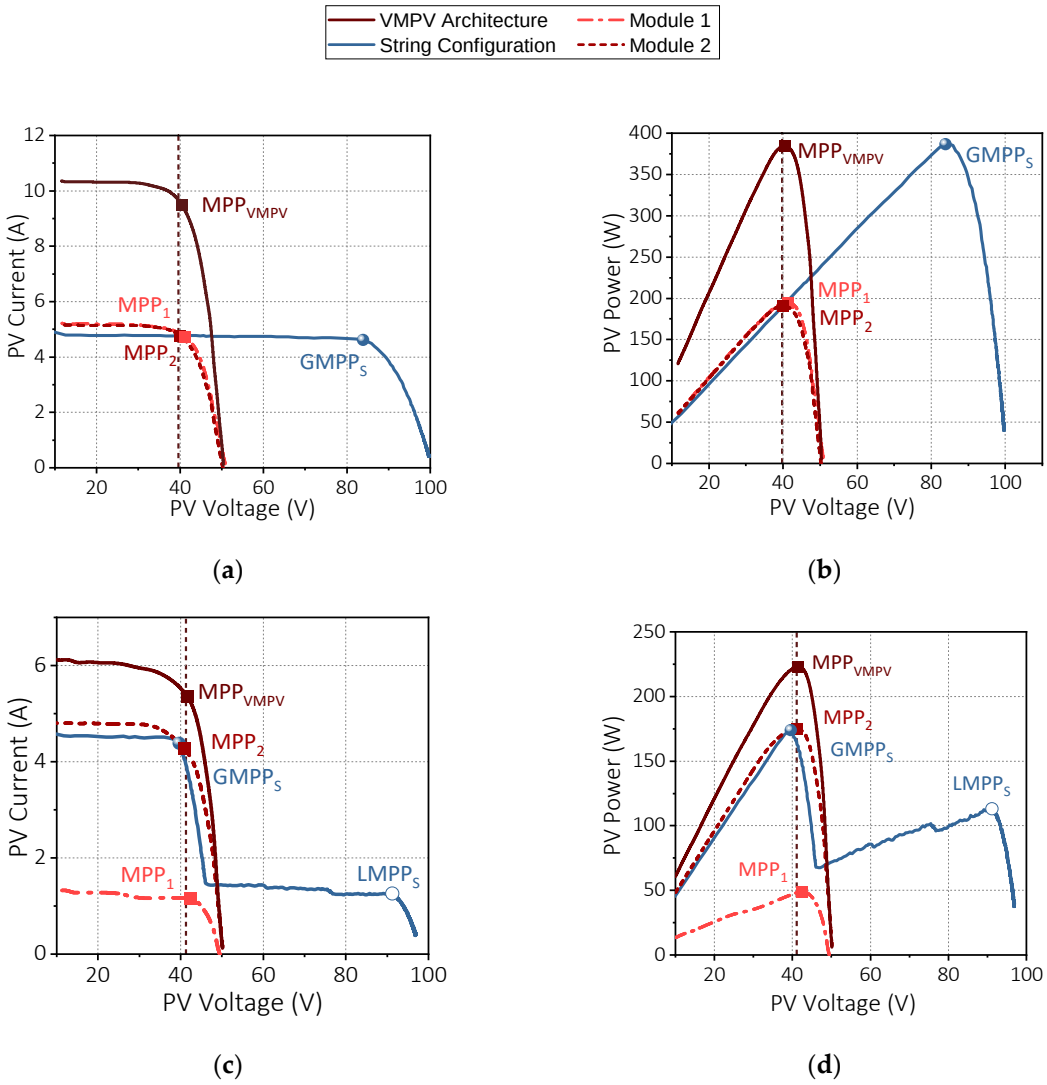


Figure 12. Experimentally extracted I-V and P-V characteristics of the PV modules under (**a**,**b**) the shading pattern A: uniform irradiance and (**c**,**d**) the shading pattern B: PS conditions.

Table 2. MPP data from the experimentally extracted characteristics.

Test Conditions	PV Module/PV System	V_{PV} (V)	I_{PV} (A)	P_{PV} (W)	Extraction eff. (%)
Pattern A: Uniform Conditions	Module 1 (MPP_1)	41.25	4.705	194.1	-
	Module 2 (MPP_2)	40.08	4.757	190.7	-
	VMPV Architecture (MPP_{VMPV})	40.52	9.475	384.4	99.9
	Module 1 (@MPP_{VMPV})	40.52	4.785	193.9	99.9
	Module 2 (@MPP_{VMPV})	40.52	4.702	190.5	99.9
Pattern B: PS Conditions	Module 1 (MPP_1)	42.5	1.145	48.7	-
	Module 2 (MPP_2)	41.05	4.26	174.9	-
	VMPV Architecture (MPP_{VMPV})	41.6	5.36	223	99.74
	Module 1 (@MPP_{VMPV})	41.6	1.161	48.3	99.18
	Module 2 (@MPP_{VMPV})	41.6	4.20	174.7	99.89
	Series Connection ($GMPP_S$)	39.65	4.38	174	77.8
	Series Connection ($LMPP_S$)	91.3	1.255	113	50.5

Figure 12c,d show the experimentally extracted I-V and P-V traces under the shading pattern B: Module 1 is entirely shaded, while Module 2 remains unshaded. Although

$P_{PV}(\mathrm{MPP}_1)$ = 48.7 W is more than 3.5 times smaller than $P_{PV}(\mathrm{MPP}_2)$ = 174.9 W, their respective voltage difference is just 1.45 V, leading to an almost perfect η_{ext} = 99.74% for the VMPV system. Taking the effect of η_c into account, the total system efficiency is η_{sys} = 96.05%. On the other hand, the global MPP of the series connection is $P_{PV}(\mathrm{GMPP_S})$ = 174 W, equal to MPP_2 minus the power dissipated at the bypass diode of Module 1, resulting in an extraction efficiency of just 77.8%. Still, it is highly possible that a simple MPPT algorithm would converge at a local MPP (LMPP), in which case half of the PV power would be lost ($\eta_{ext}(\mathrm{LMPP_S})$ = 50.5%).

4.4. Real-Time MPPT of the VMPV Architecture

For this experiment, a P&O algorithm was executed by the second-stage converter, with a period of 250 ms and an MPPT duty cycle step of 1%. The two PV modules were subjected to the two shading patterns of the previous subsection (uniform and PS conditions).

Figure 13 shows the output power and DC-bus voltage variation under real-time tracking of the MPP. The MPPT algorithm always converges to the single MPP, guaranteeing near-perfect extraction efficiency in any conditions and effectively addressing the tracking challenges of SP configurations. In addition, the DC-link voltage is insignificantly affected by PS (only a 3% deviation), which allows for a narrow predetermined input voltage range for the grid-side inverter, in contrast to the single-stage PV systems.

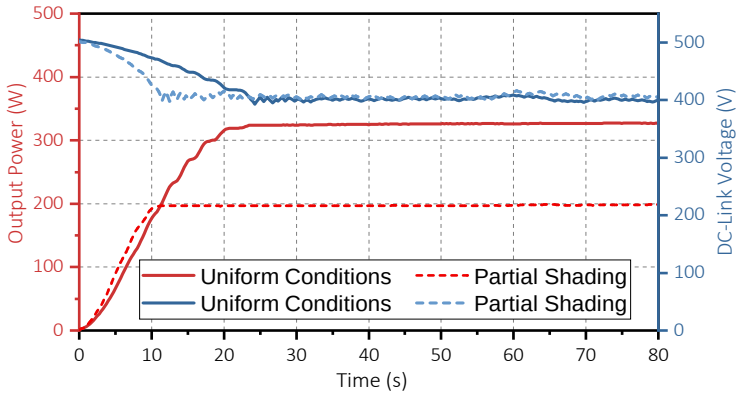


Figure 13. Response of the new VMPV architecture during real-time MPPT, under uniform and PS conditions. Output power (in red) and DC-bus voltage (in blue) variation with time.

The experimental results show that the proposed VMPV architecture combines the near-perfect extraction efficiency of MLPE with a flat conversion efficiency in any conditions; this leads to a higher total system efficiency than most state-of-the-art configurations, including other MLPE architectures.

5. Conclusions

In this paper, a new highly efficient architecture for residential grid-connected PV systems has been demonstrated and experimentally verified. The PV modules are connected in parallel through fixed-step high step-up nX converters (voltage multipliers), thus eliminating the partial shading challenges of typical series connections and delivering almost 100% extraction efficiency. At the same time, the nX converter features a high flat conversion efficiency of more than 96.3% irrespective of the power level, leading to better total system efficiency at partial shading than most centralized and distributed PV architectures.

The developed magnetic-free nX converters use GaN HEMTs that are switching at high frequency which, in turn, allow for longer lifetime ceramic capacitors in place of the conventional bulky electrolytic capacitors. This, along with the omissions of all magnetic components and the low cooling requirements, lead to a very compact solution that can be integrated with the backside of the PV panel, forming a new voltage-multiplied PV module.

All control functions, including MPPT, are transferred to the inverter, simplifying the DC-DC micro-converter requirements for micro-controllers and voltage/current sensors. The high-voltage parallel connection results in a small variation of the DC-link voltage with the environmental conditions which, in turn, simplifies the requirements for the grid-side inverter, as in two-stage string inverters.

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Abbreviations

BIPV	Building-integrated photovoltaic
BL	Bridge-link interconnection scheme
DER	Distributed energy resources
ESR	Capacitor's internal series resistance
GMPP	Global maximum power point
HC	Honey-comb interconnection scheme
HEMT	High electron mobility transistor
IC	Integrated circuit
LMPP	Local maximum power point
LPF	Low-pass filter
MLCC	Multi-layer ceramic capacitors
MLPE	Module-level power electronics
MPPT	Maximum power point
NOCT	Nominal operation cell temperature
P&O	Perturb and observe algorithm
PCB	Printed circuit board
PLL	Phase locked loop
PR	Proportional resonant controller
PS	Partial shading
PV	Photovoltaic
PVPO	Photovoltaic power optimizer
PWM	Pulse width modulation
SC	Switched capacitor
SOGI	Second order generalized integrator
SP	Series-parallel interconnection scheme
STC	Standard test conditions
TCT	Total-cross-tied interconnection scheme
TCTR	Electrically rearranged TCT array
VMPV	Voltage-multiplied photovoltaic system
ZCS	Zero current switching

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