A 77-dB DR 16-Ch 2nd-order Δ-ΔΣ Neural Recording Chip with 0.0077mm²/Ch

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Abstract

This paper presents a scalable 16-channel neural recording chip enabling simultaneous acquisition of action-potentials (APs), local-field potentials (LFPs), electrode DC offsets (EDOs) and stimulation artifacts (SAs) without saturation. By combining a DC-coupled Δ-ΔΣ architecture with new bootstrapping and chopping schemes, the proposed readout IC achieves an area of 0.0077mm² per channel, an input-referred noise of 5.53±0.36μV_{rms} in the AP band and 2.88±0.18μV_{rms} in the LFP band, a dynamic range (DR) of 77dB, an EDO tolerance of ±70mV and an input impedance of 283MΩ. The chip has been validated in an *in vitro* setting, demonstrating the capability to record extracellular signals even when using small, high-impedance electrodes. Because of the small area achieved, this architecture can be used to implement ultra-high-density neural probes for large-scale electrophysiology.

Introduction

Area reduction is one of the most critical challenges in the design of neural recording ICs and CMOS neural probes. This is driven by the demand for ever higher channel counts to enable the readout of as many neurons as possible via implanted electrodes. CMOS high-density neural probes that achieve 0.12mm² [1] and 0.035mm² per channel [2] have been recently reported and are now widely used. However, it is difficult to scale up these probes to thousands of channels due to the chip-size constraints, especially for electrophysiological applications in small animals. Recent years have seen significant improvements in channel input range [3], [4] and power consumption [5], but the area of those designs is still large. In contrast, dramatic area reduction has been achieved by using direct ΔΣ conversion at the expense of noise [6]. Although small area has also been achieved in several low-frequency (ECoG) readouts [7], [8], those architectures cannot be easily extrapolated to the larger bandwidth and higher electrode impedance required for AP readout. In this paper we propose a readout architecture that achieves a good compromise among area, noise, bandwidth, EDO tolerance and input range.

Proposed Neural Recording Chip Architecture

Each channel is based on a Δ-ΔΣ modulator [9], [10] that uses a hybrid discrete-time (DT) and continuous-time (CT) cascade of integrators with feedback (CIFB) structure (Fig. 1). A DC-coupled architecture is chosen instead of the conventional AC-coupled readout to facilitate chopping, thus suppressing the flicker noise and reducing the area of transconductor G_{m1}. Delta modulation around a 2nd-order ΔΣ core is used to achieve large DR and ensure that APs (<1mV_{pp}), LFPs (<10mV_{pp}), EDOs and SAs can all be captured without saturation in a signal bandwidth 20x larger than that in [9], [10]. Delta modulation is implemented using a feedback 5-bit current DAC ($IDAC_1$) and a feedback accumulator (*FB-ACC*). The DAC current is subtracted from the input signal via G_{m1} before integration onto C_{INT1}. Second-order noise shaping is obtained by the CT integrator comprised of G_{m2} and C_{INT2}. The loop-filter output is quantized by a dynamic comparator, and its Δ-modulated bitstream is integrated by *FB-ACC*. Data weighted averaging (DWA) is used to achieve 1st-order mismatch shaping of the elements in $IDAC_1$. The DACs, comparator, accumulators and DWA operate at 10.24MHz, resulting in an oversampling ratio of 512 for a signal band of 10kHz. A separate accumulator (*OUT-ACC*) is used to integrate the comparator's output before decimation. *OUT-ACC* can be reset to mid-range independently from *FB-ACC*, thus enabling offset removal without requiring any additional power- or area-hungry digital subtractor. A 3-stage cascaded-integrator-comb (CIC) decimation filter follows *OUT-ACC* to produce a 14-bit 20kS/s output.

New bootstrapping and chopping schemes are proposed in this work to achieve high input impedance. As shown in Fig. 2, the choppers are placed outside of the modulator's feedback loop to avoid the aliasing of high-frequency-shaped noise through $IDAC_1$. The AC feedback currents always flow through *MP3~MP6* due to the low output resistance resulting from the flipped-voltage-follower (FVF) stage. The equivalent input impedance when using chopping is determined by the chopping frequency and the parasitic capacitance at the gate of the input transistor, and it is constant in the whole signal bandwidth. In our circuit, bootstrapping is achieved by transistors *MP1,2* and *MN1,2*. The drain current of *MN1,2* is fixed to keep a constant voltage difference between the source and the drain of the input transistors. Since the input transistors are in source-follower configuration and their bulk is connected to the source, the signal at the gate will be followed by its source, drain and bulk. Hence, all the parasitic capacitances at the gate are neutralized.

Measurements

The prototype chip was fabricated in 55nm CMOS and fully characterized. The achieved SNDR for an input signal of 20mV_{pp} and a DC offset of 40mV is 59.5dB (Fig. 3a). The SNDR and SNR were also measured with different input amplitudes, resulting in an effective DR of 77dB (Fig. 3b). Although the SNDR degrades for amplitudes beyond 10mV_{pp}, the THD is still <1% (acceptable limit in this application) for amplitudes up to 80mV_{pp}. More importantly, the SNR does not degrade with amplitudes up to 148mV_{pp}. The measured EDO tolerance is shown in Fig. 3c. Here, the THD remains below 0.44% for a DC offset ranging from -70mV to +70mV. Good noise uniformity across channels and the effectiveness of the proposed chopping method are demonstrated in Fig. 3d. The achieved input-referred noise in the AP band (300Hz-10kHz) is 5.53±0.36μV_{rms}. The channel input impedance is measured as 283MΩ at 10Hz, which is sufficient to interface with the small (144μm²) recording electrodes used in neural probes (100MΩ @1Hz) [1]. As shown in Fig. 4, about half of the channel area is occupied by the digital part, which can scale down with technology. To test our chip in an *in vitro* setting, iCell Cardiomyocytes[2] were grown on top of TiN electrodes of various sizes (20-121 μm²). Fig. 5 demonstrates that, even when using very-small high-impedance electrodes, this chip can record extracellular signals and tolerate EDOs without saturation. Note that the noise levels in this experiment are dominated by the electrode impedance.

As shown in Table I, we report a scalable neural readout architecture that achieves the best compromise among area, noise, bandwidth, EDO tolerance, input range and input impedance. The main limitation of our implementation is the large power consumption, which primarily (72%) comes from the digital circuit. From this digital power, >80% is consumed by the decimation filter, which was not optimized in this prototype. Despite this, the total power is comparable to well established CMOS neural probes [2]. By occupying an area <0.01mm^2/channel, the proposed readout opens opportunities for the development of ultra-high-density neural probes.

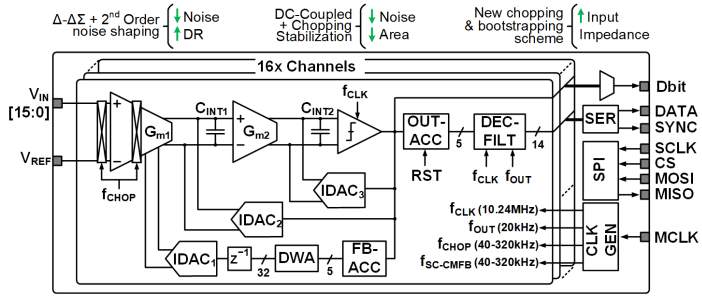

Fig. 1. Proposed 16-channel DC-coupled Δ-ΔΣ front-end architecture.

References

[1] C. M. Lopez *et. al.*, *TBCAS*, 2017. [2] S. Wang *et. al.*, *TBCAS*, 2019. [3] H. Chandrakumar *et. al.*, *JSSC*, 2018. [4] C. Lee *et. al.*, *JSSC*, 2020. [5] S. Park *et. al.*, *JSSC*, 2018. [6] D. De Dorigo *et. al.*, *JSSC*, 2018. [7] J. P. Uehlin *et. al.*, *TBCAS*, 2020. [8] M. R. Pazhouhandeh *et. al.*, *JSSC*, 2020. [9] H. Kassiri *et. al.*, *JSSC*, 2017. [10] C. Kim *et. al.*, *JSSC*, 2018.

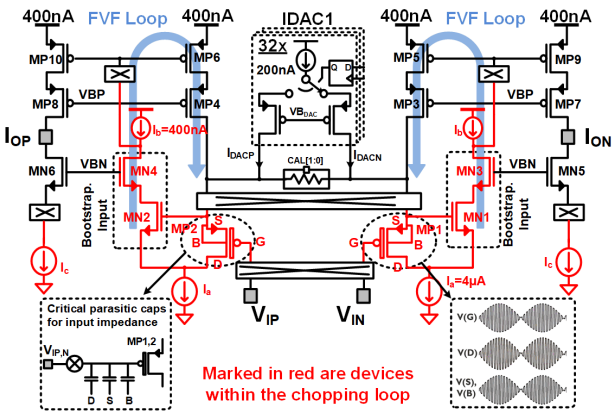

Fig.2. The schematic of the G_{m1}-stage showing the chopping and the input impedance bootstrapping principles.

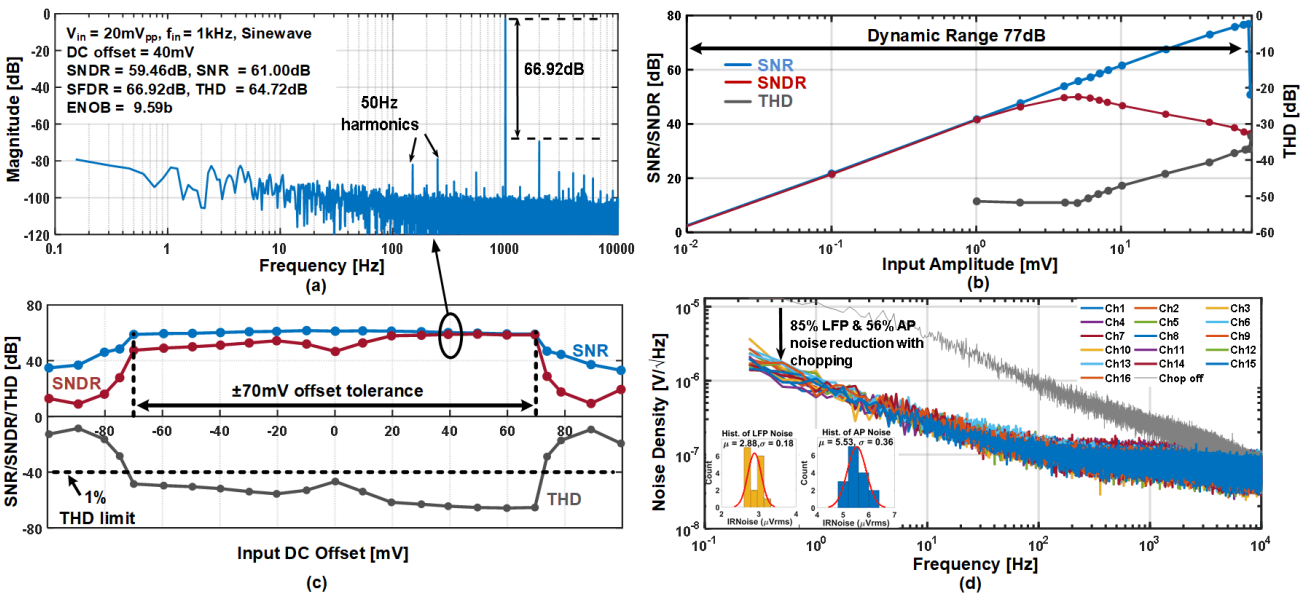

Fig. 3. (a) Measured PSD with 20mV$_{pp}$, 1kHz sine input and 40mV DC offset. (b) Measured DR over different input amplitudes and 0mV DC offset. (c) Measured SNDR/SNR/THD with different DC offsets and 20mV$_{pp}$ sine wave. (d) Measured noise density over the 16 channels.

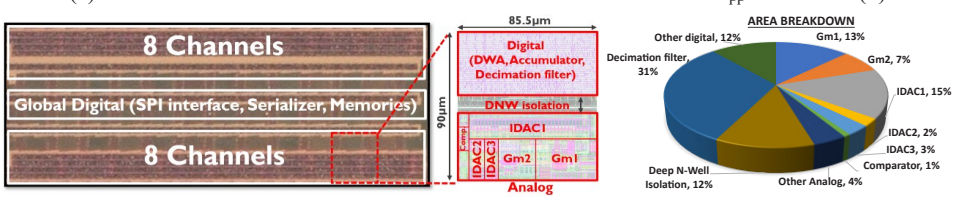

Fig. 4. Die photo of the 16-channel fabricated IC, and channel area breakdown.

Table I. Comparison with State-Of-The-Art Neural Recording (AP, LFP) ICs

	This Work	[2]	[6]	[3]	[4]	[5]
Technology / Supply (V)	55nm / 1.2	130nm / 1.2	180nm / 1.8	40nm / 1.2	110nm / 1.0	180nm / 0.5/1.0
# of channels	16	384	144	1	1	128
Channel topology	2nd-order Δ-ΔΣ	IA+SAR	1st-order IΔΣ	IA+3rd-order ΔΣ	2nd-order ΔΣ	IA+1st-order Δ-ΔΣ
Input structure	DC-coupled with chopping	AC-coupled	DC-coupled	DC-coupled with chopping	DC-coupled	AC-coupled
Input Impedance (Ω)	283M@10Hz	179.9M@1kHz	∞@DC*	1.52G@DC; 19.6M@5kHz	∞@DC*; 13.3M@10kHz	*
AC input range (mV$_{pp}$)	148	12.5	40	200	300	*
EDO tolerance	±70mV	Rail-to-rail*	±45mV*	±100mV	±50mV	Rail-to-rail*
THD @1kHz input	0.05~0.44%@20mVpp***	0.17%@10mVpp	0.75%@40mVpp	0.009%@200mVpp	0.0095%@285mVpp	0.019%@3mVpp
Bandwidth (kHz)	10	10	10	5	10	10.9
AP noise 0.3~10kHz (μV$_{rms}$)	5.53 ± 0.36	7.44	20.19	6.35 (1Hz ~5 kHz)	9.5 (1Hz ~10 kHz)	3.32 (0.5Hz ~12.7 kHz)
LFP noise 0.5Hz~1kHz (μV$_{rms}$)	2.88 ± 0.18	7.65	8.43			
NEF (AP+LFP)	17.1 / 9.8**	26.1	42.6	8.5**	9.3**	3.02
Power/channel (μW)	61.2	48.7	46.29	7.3**	6.5**	3.05
Area/channel (mm^2)	0.0077	0.035	0.0049	0.113**	0.078**	0.058

*Not measured **Decimation filter not included ***With -70mV ~ +70mV DC offset

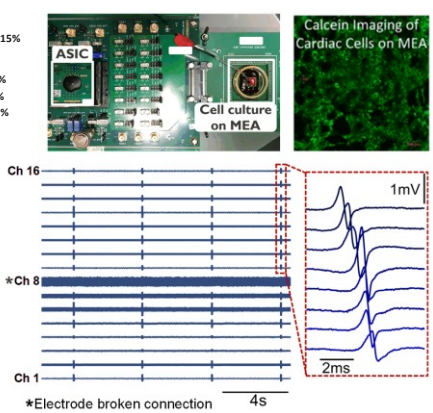

Fig. 5. *In vitro* test setup and measured extracellular cardiac cell signals from 16 channels.