A Compact, Low-Power Analog Front-End with Event-Driven Input Biasing for High-Density Neural Recording in 22-nm FDSOI

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***Abstract*—An ultra-small-area, low-power analog front-end (AFE) for high-density neural recording is presented in this paper. It features an 11-bit incremental delta-sigma analog-to-digital converter (ΔΣ ADC) enhanced with an offset-rejecting event-driven input biasing network. This network avoids saturation of the ADC input caused by leakage of the input-coupling capacitor implemented in an advanced technology node. Combining AC-coupling with direct data conversion, the proposed AFE can tolerate a rail-to-rail electrode offset and achieves a good trade-off between power, noise, bandwidth, input impedance, and area. Fabricated in a 22-nm fully-depleted silicon on insulator (FDSOI) process, the design occupies an active area of <0.001 mm², the smallest obtained to this date for a neural AFE, and consumes <3 μW from a 0.8-V supply. It achieves an input-referred noise of 11.3 μV_{rms} in the action potential band (300 Hz – 10 kHz) and 10 μV_{rms} in the local field potential band (1 Hz – 300 Hz).**

***Index Terms*— Small area, low power, AFE, multi-channel neural recording, reset alignment, event driven, incremental, ΔΣ ADC, AC-coupling, direct data conversion, reconstruction.**

I. Introduction

Multi-channel, high-density extracellular neural recordings of low-frequency local field potentials (LFPs) and high-frequency action potentials (APs) [1] have contributed substantially to neuroscience research. Knowledge gained from those studies greatly enables the understanding of neurological disorders and their underlying mechanisms. However, as the maximum number of simultaneously recorded neurons to this date is many orders of magnitude smaller than the total number of neurons in the brain, there is a strong need for a much higher number of parallel readout channels in electrophysiology tools. This could be achieved by significantly reducing the area of the readout channel, while still maintaining low-power operation and high signal fidelity, in combination with high-density arrays of small electrodes (a few tens of μm diameter or less).

As shown in Fig. 1, the past two decades have witnessed the emergence of several novel neural readout architectures that try

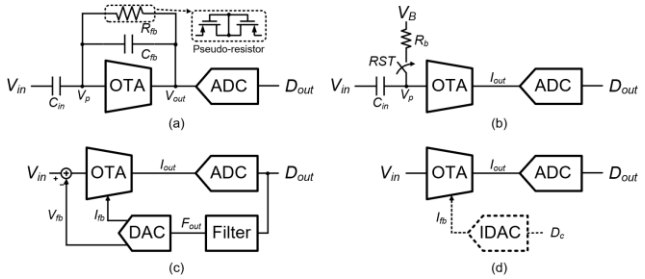

Fig. 1. State-of-the-art neural AFEs: (a) AC-coupling with pseudo-resistor, (b) AC-coupling with duty-cycled resistor, (c) DC-coupling with mixed-signal feedback, and (d) DC-coupling with direct data conversion.

to achieve the requirements mentioned above. Since its first introduction in [2], AC-coupled amplification with pseudo-resistor biasing (Fig. 1(a)) has been used widely [3]-[5]. However, pseudo-resistors are highly sensitive to process variations and light, nonlinear, and very prone to large offsets caused by leakage currents. Duty-cycled resistors (Fig. 1(b)) with single- and multi-rate control [6], [7] have been proposed to address some of those issues. Nonetheless, the maximum achievable resistance (~tens of GΩ) is limited by the parasitic capacitors, and large passives are still needed to achieve a sub-Hz high-pass corner frequency. DC-coupled solutions have been explored as well. A mixed-signal feedback (Fig. 1(c)) was implemented in [8]-[10] to reject electrode DC offsets and low-frequency disturbances. In this case, the corner frequency is tuned in the digital domain. The main drawback of such approach is the limited offset rejection, which requires large power or area for the low noise and wide dynamic range (DR) feedback digital-to-analog converters (DACs). By removing the feedback path or adding a coarse DAC for offset rejection (Fig. 1(d)), a significant area reduction is achieved in [11], [12]. With the help of a global reference control, those designs work well using a floating measurement setup. While for grounded *in vivo* applications, they may bring the OTA out of its input common-mode range. A wide DR for offset and artifact

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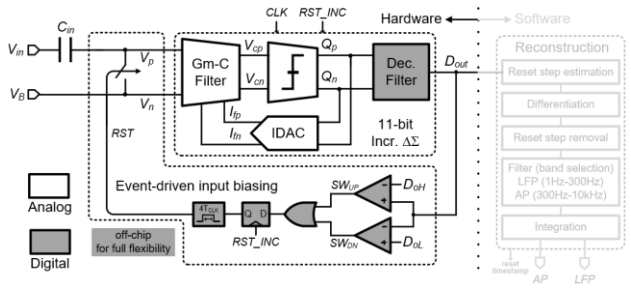


Fig. 2. Proposed hybrid AFE based on the hardware and software co-design.

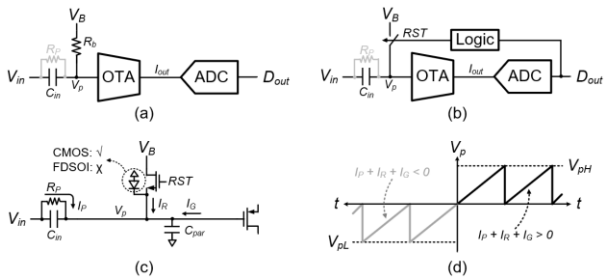


Fig. 3. Direct data conversion with (a) AC-coupling with pseudo-resistor, (b) event-driven input biasing; (c) Circuit schematic showing the main leakage paths and (d) illustration of time-domain waveform at node V_p with event-driven input biasing.

tolerance has also been implemented in [13]-[16]. However, since the large unwanted electrode offset is also digitized together with the small neural signals, this approach achieves poor power efficiency. It is worth mentioning that direct time division multiplexing at the electrode is another promising method to achieve area reduction [17], [18]. However, it works well only for the large mm-scale electrodes used for ECoG [18], while the low input impedance and noise folding induced by the multiplexing operation pose big concerns for small μm-scale electrodes [17].

This paper presents an ultra-small-area low-power analog front-end (AFE) that tackles these offset-rejection problems by introducing a direct data conversion architecture with an event-driven input-biasing solution. The incremental operation, combined with reset timing control and signal reconstruction, prevents data-sample corruption in the occurrence of an input biasing reset event.

II. Neural AFE with Event-Driven Input Biasing

Fig. 2 shows the simplified block diagram of the proposed hybrid AFE architecture. It consists of an input capacitor C_{in}, an 11-bit incremental ΔΣ ADC, an event-driven input-biasing network and a reconstruction block for signal post-processing. The decimation filter and the event-driven logic are implemented off-chip for full flexibility in the fabricated test chip. The signal reconstruction, which is outside the critical closed-loop control of the AFE, is done in software and could easily be merged with other external signal processing units, e.g., spike detection and sorting algorithms. The different components of this architecture are explained in the following subsections.

A. Event-driven Input Biasing

The area efficiency of direct data conversion using oversampled ADCs without pre-amplification has already been demonstrated in [11], [12], [19]. However, the asynchronous control in [19] makes the serialization of the multi-channel outputs difficult to implement in a power-efficient manner, and the area and power consumption of the digital logic in [11], [12] are significant due to the relatively old process used (180 nm). Hence, an architecture that combines AC-coupling with direct data conversion implemented in a scaled technology node would address all the above-mentioned limitations and enable the implementation of high-channel-count neural interfaces. Such a scheme is shown in Fig. 3(a) and it consists of a passive high-pass filter for electrode-offset rejection and a ΔΣ modulator with Gm-C technique to achieve sufficiently low quantization noise and distortion. In our design, we use a 22-nm fully-depleted silicon-on-insulator (FDSOI) technology to benefit from the power and area scaling in the digital circuits. However, the high-density metal-oxide-metal (MOM) capacitors in this scaled technology node suffer from significant leakage. As illustrated in Fig. 3(a), the parasitic resistor R_P that models the leakage of the AC-coupling capacitor C_{in} forms a voltage divider with the pseudo-resistor R_b. Therefore, only finite attenuation is achieved at DC, which causes a residual offset voltage at node V_p. This residual offset can saturate the AFE when large input DC offsets are present at the electrode interface. This problem can be tackled by removing the pseudo-resistor R_b and pre-charging the node V_p to a biasing voltage V_B before recording. However, the leakage currents will cause this node to drift up or down until it saturates the AFE. To avoid this, the node V_p can be pulled back to V_B when it comes close to the limit input range of the modulator. This concept is shown in Fig. 3(b), where V_p is dynamically biased via an event-driven reset switch. Fig. 3(c) illustrates the main leakage current paths at node V_p. In order to limit the occurrence of the reset event to only once every few seconds, the leakage at node V_p has been minimized and maintained within the fA range. In this way, the reset will have a negligible impact on the overall signal quality. The gate leakage I_G generated by the input differential pair of the Gm-C filter can be minimized by using thick-oxide transistors. The leakage from the reset transistor I_R is made negligible by sizing it to achieve large OFF resistance. Moreover, the source-to-bulk leakage path is not present in the used FDSOI technology.

A high-density (4.5 fF/μm^2) alternate-polarity MOM (APMOM) capacitor is chosen for the input capacitance and stacked above the active circuits to minimize area. Simulations show that the capacitor leakage I_P dominates when a large electrode offset (V_{in}) and a bias voltage (V_B) of 0 V are applied. The time-domain waveform at node V_p when event-driven biasing is applied is illustrated in Fig. 3(d). The reset switch is turned ON whenever the node V_p crosses the low-limit (V_{pL}) or high-limit (V_{pH}) thresholds of the linear input range. A sampling kT/C noise of 40.5 μV_{rms} is introduced at the instant of a reset event. However, this noise gets averaged and becomes negligible due to the very infrequent reset operation. While large motion or stimulation artifacts could potentially trigger the input reset more frequenly and temporarily increase the kT/C noise, such artifacts do not occur often and are limited to short periods.

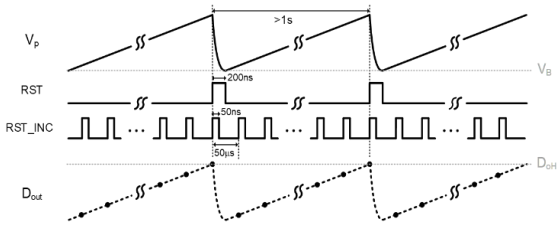
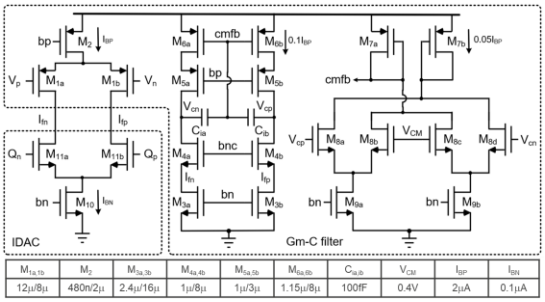


Fig. 4. Timing diagram of input reset (*RST*) and incremental ΔΣ reset (*RST_INC*).



$M_{1a,1b}$	M_2	$M_{3a,3b}$	$M_{4a,4b}$	$M_{5a,5b}$	$M_{6a,6b}$	$C_{a,b}$	V_{CM}	I_{BP}	I_{BN}
12µ/8µ	480n/2µ	2.4µ/16µ	1µ/8µ	1µ/3µ	1.15µ/8µ	100fF	0.4V	2µA	0.1µA

Fig. 5. Circuit schematics of Gm-C filter and IDAC.

Note that the proposed input-biasing scheme is similar to the signal folding technique reported in [20], where a reset is applied to extend the limited AFE input range (~0.2 mV_{pp}) and enable the recording of large LFP signals. Due to the small input range, large signals would trigger the reset very frequently, significantly degrading the noise. In contrast, the input range of our AFE is designed large enough (>10 mV_{pp}) to accommodate both LFP and AP signals and make sure that the sporadic resets would have only negligible impact on the overall noise.

B. Incremental Operation with Reset Alignment

The approach of event-driven input biasing achieves a large offset rejection with negligible area and power overhead. However, at every reset event, the node V_p is quickly pulled back to the initial DC biasing point, which is essentially a large step of half the linear input range. Due to the finite-bandwidth response of the decimation filter following a classical ΔΣ modulator, this large step would result in signal distortion (glitches with long recovery time). This can be avoided by operating the modulator in incremental mode. Since the steps are caused by input resets, we know very accurately when they occur. This knowledge is leveraged to properly align the input reset *RST* and the incremental reset *RST_INC*, as shown in Fig. 4. This technique guarantees that only one data sample in the digital output D_{out} gets "corrupted" at every reset event. Since only 4 clock cycles (200 ns) are sufficient to reset the input and the incremental integration period (50 µs) consists of 1000 clock cycles, the Nyquist-rate sample following the reset event can be converted with ≤ 0.4% error.

C. Signal Reconstruction

The slow drift caused by leakage current and the large reset steps are removed by post-processing the output signals in the digital domain. The reconstruction algorithm estimates the reset step and filters the data within the signal band of interest. The residual error at the time of a reset may affect the shape of an AP signal occurring concurrently. Therefore, the reset events are time-stamped to enable further data processing by other external software algorithms. Due to the very slow drift caused by the fA-level leakage current, an AP event could trigger the biasing reset when the baseline is near the thresholds. To prevent this, the reset activation is delayed with respect to the threshold crossing by a few samples. This delay allows the acquisition of the AP waveform without any residual error, reducing further the chance of distorted spikes that could be mis-classified by a spike sorter.

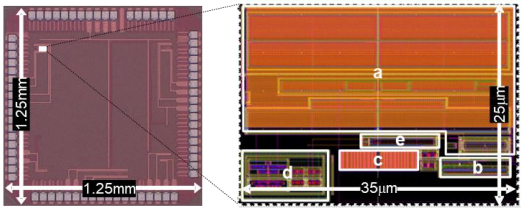


Fig. 6. Chip micrograph and AFE layout, (a) OTA and C_{in}, (b) common-mode feedback, (c) integration capacitors, (d) comparator, (e) feedback IDAC.

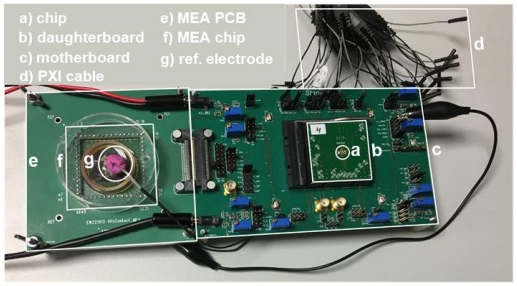


Fig. 7. Setup for electrical characterization and *in vitro* measurements.

III. Circuit Implementation

As shown in Fig. 2, the input capacitor C_{in} decouples the OTA input common-mode voltage from the electrode offset. It is a 2.5 pF APMOM capacitor from metal 5 to metal 8, and has an area of 35 µm x 16 µm. This capacitor value leads to a signal attenuation of <10% and a negligible modulator distortion due to the non-linear parasitic capacitance C_{par} at node V_p. A ground-shielding layer is placed below the input capacitor to avoid any coupling from the active circuit. Fig. 5 shows the circuit schematics of the Gm-C integrator and the feedback current DAC (IDAC). A fully-differential folded-cascode architecture is employed for the Gm stage to obtain a large output impedance. The common-mode feedback amplifier sets the DC common-mode output level. The auxiliary high-frequency capacitive-feedback path (from the common node of the integration capacitors to node *cmfb*) enhances the phase margin of the common-mode feedback loop. For minimal area, the IDAC is implemented using current sinks only. Simulations show that the asymmetrical current feedback has a negligible impact on the overall distortion performance. This is because the ripple at the oversampling frequency is attenuated by the output common-mode rejection of the Gm-C filter.

A StrongARM dynamic comparator quantizes the filter output to a bitstream running at the system clock *CLK*. The 11-bit digital output signal can be obtained by a 10-bit ripple counter, which is extended with 1 bit by extracting the sign information of the comparator input at the end of each conversion [11]. The calculated quantization noise is 1.6 μV_{rms} for a full-scale input range of 11.5 mV_{pp}. Due to the frequency-

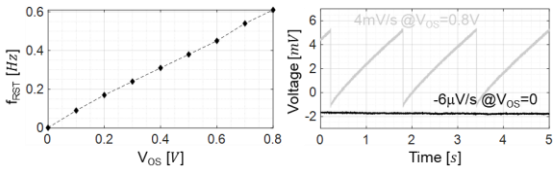


Fig. 8. Measured reset frequency f_{RST} as a function of electrode offset V_{OS} (left) and leakage of node V_p with an offset of 0 V and 0.8 V (right).

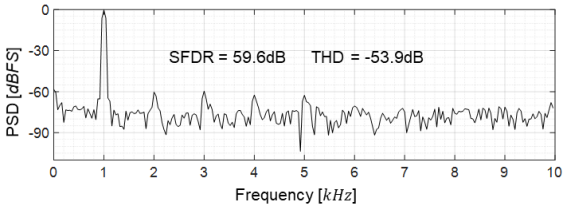


Fig. 9. Linearity measurement with a 1 kHz full-scale input.

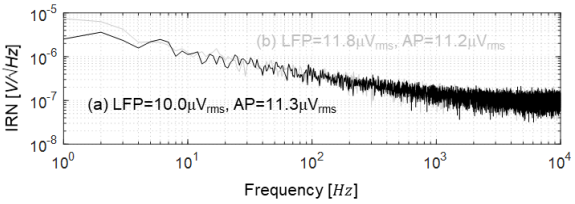


Fig. 10. Input-referred noise (IRN) measurements with (a) a zero offset and (b) periodic reset at 1 Hz.

resolution limitation of the instrument used for testing, a 20-MHz system clock was used for simplicity, resulting in an over-sampling ratio of 1000 (instead of 1024). The slightly degraded quantization noise has a negligible impact on the overall output signal fidelity. This is because the quantization noise is a bit over-designed compared to the circuit intrinsic noise (thermal and flicker), with little power overhead. An input biasing-reset pulse is generated when the decimated output D_{out} reaches the upper limit D_{oH} or the lower limit D_{oL} of the linear output range, which is then time-aligned to *RST_INC* to perform the reset. The pulse width is tuned to be 4 clock cycles to achieve the proper input resetting, as discussed above.

IV. Measurement Results

A single-channel prototype of the proposed AFE architecture has been implemented in a 22-nm FDSOI process to prove the concept. Fig. 6 shows the chip micrograph and zoomed-in channel layout with an active area of only 875 μm^2 (35 × 25 μm^2). The power consumption is 2.5 μW from a 0.8-V supply. In this prototype, the digital part (decimation filter and event-driven logic) is implemented off-chip for full flexibility. Its power and area are estimated to be around 0.3 μW and 100 μm^2 for an on-chip implementation, resulting in only ~10% overheads. The signal reconstruction is done in software, and can easily be merged with other signal-processing algorithms such as spike-sorting analysis.

Fig. 7 shows the setup used for the electrical characterization and *in vitro* measurements described below. The measured input-biasing reset frequency and leakage at node V_p are presented in Fig. 8. The drift is only -6 μV/s with an offset of 0 V and 4 mV/s with a worst-case offset of 0.8 V. This results in a maximum reset frequency of only 0.6 Hz. The worst-case offset is limited by the standard IO ESD protection, but it is

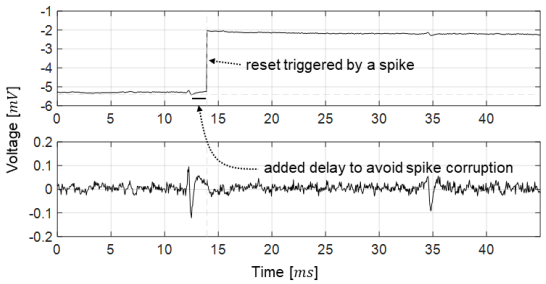


Fig. 11. *In vitro* measurement of neuronal action potentials, before (top) and after reconstruction (bottom).

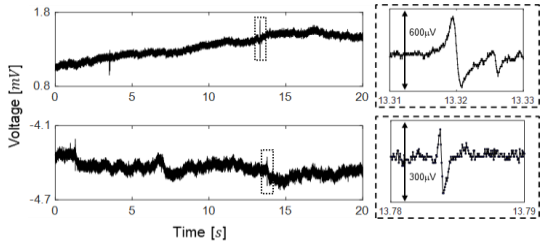


Fig. 12. *In vitro* measurements (raw data without filtering) of cardiac cells (top) and neuronal cells (bottom).

sufficient to accomodate the electrode offsets and artifacts normally observed in our setups. The thresholds at which a biasing reset is triggered are made programmable and set to ±5.4 mV. This means that, before reaching the saturation limits of ±5.75 mV, the system still has a headroom of 0.35 mV for any ongoing AP signal. Shown in Fig. 9, the measured spurious-free dynamic range (SFDR) and total harmonic distortion (THD) are 59.6 dB and -53.9 dB when applying a 1-kHz full-scale sine wave directly at node V_p. In this measurement, the input capacitor C_{in} is bypassed to avoid any offset-induced drift at node V_p and ensure full control of the input signal amplitude. Fig. 10 shows the noise measurements for two different conditions: (a) V_{in} shorted to ground and node V_p controlled by the automatic reset mechanism (i.e. no offset and minimum reset frequency), and (b) node V_p periodically forced to reset at 1 Hz (approximately representing the worst-case offset scenario). The noise is analyzed after reconstruction, and the spectrum indicates the effect of the residual reconstruction error on the noise in the LFP and AP bands. These measurements confirm that, even with worst-case resetting, the input-bias reset results in only ~10% noise increase in the LFP band, which is well within the acceptable range for the application.

In order to test the functionality of the proposed AFE and validate the effectiveness of the reconstruction algorithm in a real application, we have done *in vitro* recordings with neuronal and cardiac cells grown on top of multi-electrode array (MEA) chips. The MEA consisted of TiN electrodes of different sizes (20-121 μm^2), while the reference electrode was an external Pt wire. All the experiments involving primary cell cultures were executed according to the guidelines approved by the KU Leuven animal ethics committee and compliant with the European Communities Council Directive of November 24, 1986 (86/609/EEC). Fig. 11 shows *in vitro* measurements of neuronal AP signals before and after reconstruction. In this recording, a reset event was triggered by a spike. A delay of around 20 Nyquist samples (1 ms) is added to avoid spike

TABLE I. PERFORMANCE SUMMARY AND COMPARISON

	Huang[10] SSCL'18	Leene[19] JSSC'18	De Dorigo[11] JSSC'18	Uehlin[18] TBCAS'20	Wendler[12] ISSCC'21	**This Work**
Technology	65nm	65nm	180nm	65nm	180nm	**22nm**
Supply [V]	0.6	0.5	1.8	0.5/2.5	1.8	**0.8**
Power [μW]	3.2	1.275	39.14/43.32/46.29[a]	2.98	8.59	**2.5[h]**
Bandwidth [Hz]	0.1-500	10-11k	0-10k	1-1k[b]	0-10k	**10k[c]**
IRN [μV_{rms}]	2.2 (1-500Hz)	3.8 (10-10kHz)	10.46/13.04/20.19[d] 6.02/5.85/5.64[e]	1.66 (1-1kHz)	4.37[d] 2.72[f]	**11.3[d]** **10[e]**
THD	--	0.21% @2mV_{pp}	0.22% @10mV_{pp}	1%[g] @0.6mV_{pp}	0.078% @10mV_{pp}	**0.2%[i]** **@11.5mV_{pp}**
Input impedance	>500MΩ (in band)	--	--	92MΩ @2kHz	--	**398MΩ[i]** **@1kHz**
Offset tolerance	100mV_{pp}	rail-to-rail	sum: 22.5/45/90mV_{pp}	sum: 110mV_{pp}	120mV_{pp}	**rail-to-rail**
Input range	≥2mV_{pp}	4mV_{pp}			14mV_{pp}	**11.5mV_{pp}**
Area [mm^2]	0.01	0.006	0.0049	0.0023	0.00462	**0.000875[h]**

[a] Power for data transfer on the probe shank included [b] 10Hz high-pass corner during CMS
[c] High-pass corner determined by the input capacitor and leakage resistor (measured around 3mHz)
[d] For AP band of 300Hz-10kHz [e] For LFP band of 1Hz-300Hz [f] For LFP band of 0.5Hz-1kHz
[g] Frequency dependent for Δ modulator, estimated from measurement for frequencies above 200Hz
[h] Decimation filter and event-driven logic not included, estimated power 0.3μW and area 0.0001mm^2
[i] Input capacitor bypassed [j] From post-layout simulation [NA] Not allowed – Not reported

distortion due to the reset operation. Additional *in vitro* measurements of cardiac cells and neuronal cells are shown in Fig. 12. Here, spikes with larger amplitudes and longer durations are recorded from cardiac cells. Low-frequency components, mostly coming from the electrode noise and voltage drift, are also observed in this recording. No reset was required over more than one minute of acquisition due to the low leakage (only 20 seconds are shown).

The performance summary of the designed prototype and a comparison with state-of-the-art readout circuits (i.e. those achieving very small silicon area) are shown in Table I. With an active area occupation of <0.001 mm^2, our design is over 4x smaller than the non-multiplexed AFE in [12] and over 2x smaller than the highly multiplexed design in [18]. With respect to [12], a rail-to-rail electrode offset can be tolerated in this work without having to bias the OTA input or cell culture to an arbitrary voltage. A much smaller recording bandwidth of 1 kHz is covered in [18], which makes that design unsuitable for AP-signal recording. The input-referred noise in our design could be improved by using chopping, but at the cost of a degraded input impedance. Finally, a preliminary design analysis suggests that the event-driven logic and decimation filter could be implemented on-chip with ~10% area and power overhead in this technology node. This means that the proposed AFE could be easily scaled to a multi-channel implementation.

V. CONCLUSION

An ultra-compact, low-power AFE for multi-channel high-density neural recording applications is presented. It features an offset-rejecting event-driven input biasing scheme with direct data conversion. Co-design across the hardware and software dimensions greatly improved the area- and power-efficiency of the readout circuit. Compared to the state-of-the-art, the smallest channel-area to this date has been achieved while comparable electrical performance is still maintained.

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