RRAM-Based STDP Network for Edge Computing in Wearable/Implantable Devices

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Abstract— **With the technology advancement of wearable and implantable devices, the demand is increasing for low power computing circuits that allow processing of the acquired data on the edge to shorten the response time and save data bandwidth. Resistive-memory-based computing circuits have attracted broad interests due to their potential to implement low-power computing-in-memory macros and neuromorphic processors. This paper explores the hardware implementation of an artificial spiking neural network with the capability of online STDP learning by using a low-power analog CMOS circuit and a resistive random-access memory (RRAM) device. We examined the low power characteristics of the proposed circuit and its potential use for *in situ* signal processing, which holds promise for neural recording applications using implantable devices such as neural probes.**

I.   INTRODUCTION

Edge computing in wearable and implantable devices is becoming imperative as the amount of data generated is increasing rapidly. Neuromorphic computing could pave the way to a new generation of smart wearable and implantable devices that can process signals locally through Spiking Neural Networks (SNN) with online-learning capability based on the Spike-Timing-Dependent Plasticity (STDP) rule. As reported in [1]-[2], low power implementation of STDP networks is becoming plausible thanks to the advances in Resistive Random-Access Memory (RRAM) technologies, which are potential candidates to efficiently build synapses with STDP characteristics. In particular, the researchers in [3] investigated the possibility of an on-chip spike sorting scheme based on RRAM-based STDP networks, which can process the recorded neural signals *in situ*.

In this paper, we explored the hardware implementation of a binary artificial SNN which holds the potential for on-chip STDP learning. A hafnium-oxide RRAM device is utilized to build the connections between neurons, known as artificial synapses. The analog neuron cell within the SNN is based on the Integrated-and-Fire (IF) model and designed in a 65-nm CMOS process.

II.   NETWORK DESCRIPTION

A. RRAM-based Synapse Implementation

The schematic diagram of our mixed-signal SNN is shown in Fig. 1, which is composed of an IF neuron cell, an RRAM-synapse array and a control logic block for STDP rule mapping.

The RRAM device is connected in series to an NMOS transistor (M_0), forming a '1T1R' configuration. M_0 serves as a selection device and limits the maximum current that can flow through the RRAM device, thus preventing unexpected breakdown of the device. The pre-synaptic spike signal is connected to the gate of M_0. The synaptic weights are represented by the RRAM resistance states that can be tuned by voltage pulses with different polarities (see the inserted I-V curves of the 1T1R synapse in Fig. 1).

B. IF Neuron Implementation

The 1T1R synapse converts the input voltage spike to a synaptic current and feeds it to the subsequent neuron cell. The IF neuron model reproduces the neuron summation process and membrane potential evolution with an integration operation. An operational amplifier (OpAmp) based integrator provides a relatively fixed voltage value at the summing node of the neuron cell, i.e. the source line (SL) of the synapse array, which eliminates the risk of losing information due to the floating SL node.

The integrated membrane voltage V_{mem} is compared to a reference value V_{ref} via the comparator, and a post-synaptic spike will be generated once V_{mem} hits V_{ref}. A current scaling block is used to lower the injected synaptic current, which allows to reduce proportionally the membrane capacitor (C_{mem}) size. This contributes to significant area reduction of the neuron cell. A level shifter is utilized to increase the voltage level of the output spike, thus enabling a better driving capability for interfacing the following synapses.

C. STDP Rule Mapping

The network operation model can be divided into communication and STDP learning modes. In communication mode, V_{out} is logic low, indicating that there is no output spike generated. The neuron cell continuously integrates the injected synaptic current in this mode. Once an output spike is fired, the network will enter the STDP learning mode. Fig. 2 shows the waveforms for an example network with three inputs V_{G0}-V_{G2} and single output V_{out} in different operation modes. The STDP rule can be described as follows: if a pre-spike occurs before a post-spike (see V_{G0} and V_{out}), then the synaptic connection should be strengthened (see the positive set voltage pulse with PW width); if the pre-spike comes after the post-spike (see V_{G1} and V_{out}), the synaptic weight should be weakened (see the negative reset voltage pulse with PW width); if there is no overlap between the pre- and post-spikes within the considered

time window (see V_{G2} and V_{out}), the synaptic weight remains unchanged. The synaptic weight updates can be mapped to the network by switching the bit line (BL) node of the synapse array to different voltage levels via a custom designed control logic.

III. RESULTS

The functionality of our analog network was examined by using Cadence Spectre simulator. The excitatory and inhibitory 1T1R synapses realized in this work present resistance values of 8 kΩ (LRS) and 55 kΩ (HRS), respectively. The power consumed by the 1T1R synapse during the communication mode is rather low (50mV*50mV/8kΩ=0.3μW).

Fig. 3 shows the network simulation results for a 6-channel pattern recognition. Light pixels (2, 4 and 6) correspond to active pre-neurons that fire spikes more frequently, while dark pixels (1, 3 and 5) are mostly inactive pre-neurons. All RRAM cells are initialized to HRS. After feeding the pattern to the network, the synapses that are connected to light pixels are potentiated, i.e. the RRAM cells are switched to LRS. The post-neuron fires spikes with varied rates during the learning phase, indicating the change of synaptic weights. The inserted green line denotes the neuron membrane voltage V_{mem} integrating and resetting over time.

In Table I, we compare our neuron cell with other state-of-art neuron implementations. As yet, there is only limited literature discussing silicon neuron designs that are compatible with RRAM-based synapses. In contrast to other RRAM compatible neuron cells, our current scaling technique allowed for a much smaller membrane capacitor, which substantially reduced the area occupation of our proposed analog neuron cell.

IV. CONCLUSION

In this work, we explored the hardware implementation of an artificial SNN with the capability of online STDP learning by using a low-power analog CMOS-based neuron cell and an RRAM-based synapse. We demonstrated the learning functionality of our network with a relatively low power consumption and its feasibility for local signal processing.
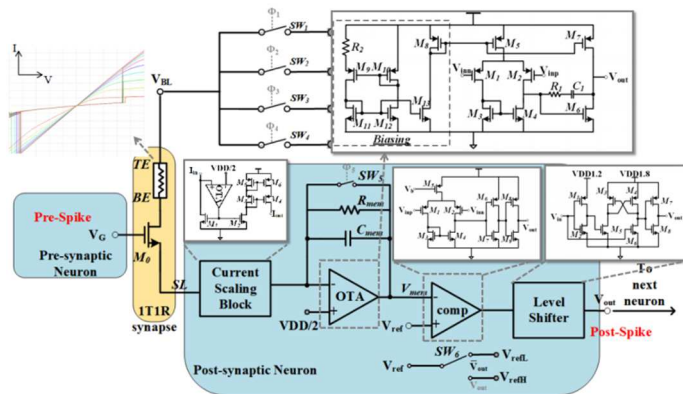
Figure 1. Illustration of our proposed SNN including a post-synaptic IF neuron connected to a pre-synaptic neuron via a 1T1R synapse.
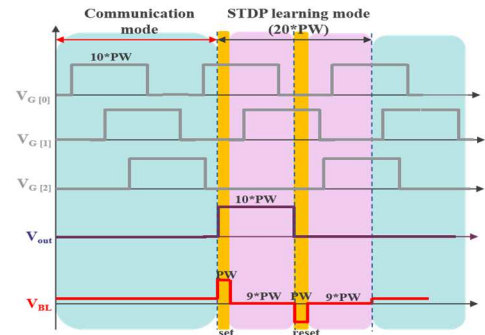

Figure 2. Waveforms for a network with 3 inputs and a single output in communication and STDP learning modes.
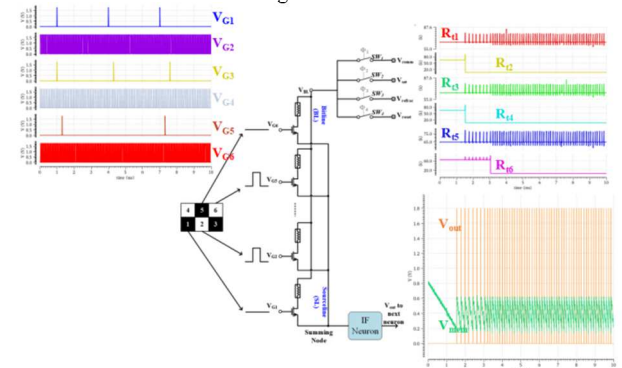

Figure 3. Network simulation results with different input spike frequencies and initial RRAM resistance states.

TABLE I
COMPARISON WITH OTHER NEURON IMPLEMENTATIONS

	This work[1]	[4]	[5]	[6]	[7]
Technology (nm)	65	180	65	14	28
Supp.Volt.(V)	1.2/1.8	1.8	2.5/1.2	0.5-1.25	0.7-1.05
Neuron model	IF	IF	AdEx IF	IF	Aug. IF
Implemen-tation	Analog			Digital	
Mem.cap.(F)	1p	20p	2.36p	NA	NA
Area(μm²)	~2155	12100	3372	14	14.3
Power(μW)	34	22	NA	NA	NA
RRAM compatible	√	√	×	×	×

1. The values are based on simulation results

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