

# A Compact Chopper Stabilized $\Delta$ - $\Delta\Sigma$ Neural Readout IC with Input Impedance Boosting

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**Abstract** This paper presents a scalable neural recording analog front-end architecture enabling simultaneous acquisition of action potentials, local field potentials, electrode DC offsets and stimulation artifacts without saturation. By combining a DC-coupled  $\Delta$ - $\Delta\Sigma$  architecture with new bootstrapping and chopping schemes, the proposed readout IC achieves an area of  $0.0077 \text{ mm}^2$  per channel, an input-referred noise of  $5.53 \pm 0.36 \mu\text{V}_{\text{rms}}$  in the action potential band and  $2.88 \pm 0.18 \mu\text{V}_{\text{rms}}$  in the local field potential band, a dynamic range of 77 dB, an electrode-DC-offset tolerance of  $\pm 70 \text{ mV}$  and an input impedance of  $663 \text{ M}\Omega$ . To validate this neural readout architecture, we fabricated a 16-channel proof-of-concept IC and validated it in an *in vitro* setting, demonstrating the capability to record extracellular signals even when using small, high-impedance electrodes. Because of the small area achieved, this architecture can be used to implement ultra-high-density neural probes for large-scale electrophysiology.

**Index Terms**— Neural recording, neural amplifiers, electrophysiology, DC-coupled readout,  $\Delta$ - $\Delta\Sigma$  modulator, chopping, bootstrapping.

## I. INTRODUCTION

ONE of the major challenges of neuroscience research is stable monitoring of neural activity at large scale and over long periods of time [1]–[3]. In the last years, CMOS high-density neural probes [4], [5] are becoming the new golden standard in electrophysiology since they allow unprecedented recordings of large numbers of neurons at single-cell resolution and across different brain regions [6]–[8]. These tools are now used not only in small rodents, but also in non-human primates [9] and humans [10].

The implementation and further scaling of these CMOS probes require readout circuits that are area- and power-efficient, achieve sufficiently low noise performance to detect action potentials (APs) as small as few tens of  $\mu\text{V}$ , and can reject or tolerate electrode DC offsets (EDOs) as large as tens of mV [11]–[13]. One of the most common readout architectures employed to accomplish these requirements uses AC-coupled amplification followed by an analog-to-digital converter (ADC). Such architecture has resulted in areas of  $0.12 \text{ mm}^2$  [4] and  $0.035 \text{ mm}^2$  per channel [5] in our previous works, but it has been scaled to  $<0.007 \text{ mm}^2/\text{channel}$  [14], [15] very recently. This area is typically dominated by the input transistors of the neural amplifier, which need to be sufficiently large to achieve low flicker noise in both the local field potential (LFP,  $0.5 \text{ Hz} - 1 \text{ kHz}$ ) and AP ( $300 \text{ Hz} - 10 \text{ kHz}$ ) bands. Effective circuit

techniques to mitigate flicker noise, such as chopping and autozeroing, cannot be easily combined with AC coupling due to the ultra-high impedance at the gate of the input transistors. When applied to capacitive-feedback amplifiers, choppers can introduce noise or reduce the input impedance depending on their location [16], [17]. Thus, to avoid the area overhead required to mitigate these issues, chopping has been often applied to other devices such as the active load in [5] or the current-controlled oscillator in [18]. Another limitation of AC-coupled neural amplifiers lies in the limited

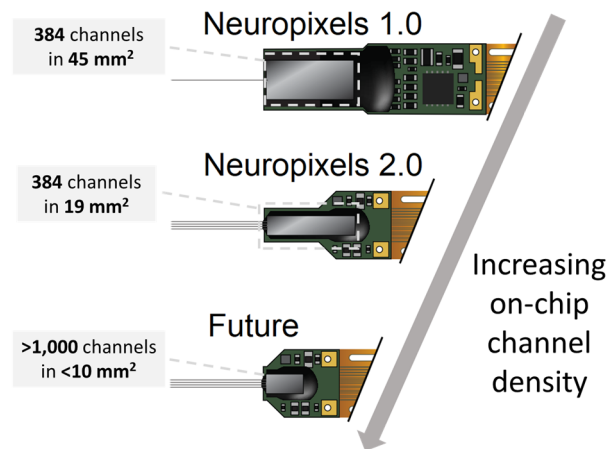


Fig. 1. The objective of this work is to meet the demand for increasing on-chip channel density in *in vivo* neural probes.

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dynamic range (typically  $<20 \text{ mV}_{pp}$ ), which prevents recording neural signals in the presence of large stimulation artifacts, as it is required in closed-loop neuromodulation applications [19]–[22].

To address the limitations related to AC coupling, DC-coupled analog front-ends have been explored. However, this approach requires extending the input range significantly in order to deal with the large EDOs and stimulation artifacts [23]. Several mixed-signal techniques have been proposed to address these challenges, and the field has recently seen significant improvements in channel input range [23]–[26] and power consumption [27], however, usually at the expense of area. In contrast, impressive area reductions have been achieved by applying direct  $\Delta\Sigma$  conversion to the electrode interface [12], [28], but at the expense of either increased noise ( $10.46/20.19 \mu\text{V}_{rms}$ ) or reduced input range ( $14 \text{ mV}_{pp}$ ). Although small area has also been achieved in several low-frequency readouts [21], [22], [29]–[31], those architectures cannot be easily extrapolated to the larger bandwidth and higher electrode impedance required for AP recording.

In this paper we present a DC-coupled  $\Delta\text{-}\Delta\Sigma$  neural readout architecture with new bootstrapping and chopping schemes, which provide large dynamic range while maintaining a high input impedance. In this way, we achieve a good compromise between area, noise, bandwidth, EDO tolerance, input impedance and input range. As shown in Fig. 1, the main goal of our channel architecture is to enable further area and density scaling in future implantable CMOS neural probes as the ones reported in [4], [5]. Therefore, a multi-channel chip prototype has been fabricated to demonstrate the performance and applicability to this application. This paper is an extension of our previous conference paper [32] and it is organized as follows. Section II describes the system architecture and the working principle of the proposed  $\Delta\text{-}\Delta\Sigma$  modulator. Section III gives details of the different circuit techniques used in each building block. The measurement results, including an *in vitro* validation, are described in Section IV, while the conclusions are drawn in Section V.

## II. CHANNEL ARCHITECTURE

The recording channel is based on a  $\Delta\text{-}\Delta\Sigma$  modulator [30], [31] that uses a hybrid discrete-time (DT) and continuous-time (CT) cascade of integrators with feedback (CIFB) topology (see Fig. 2). The  $\Delta\Sigma$  core of the modulator is implemented with a 2<sup>nd</sup> order CT loop-filter employing  $G_m\text{-}C$  integrators ( $G_{m1}$ ,  $C_1$ ,  $G_{m2}$ ,  $C_2$ ), non-return-to-zero (NRZ) current digital-to-analog converters (DACs,  $IDAC_2$  and  $IDAC_3$ ) and a single-bit quantizer. The  $\Delta$ -modulation, implemented using a feedback 5-bit current DAC ( $IDAC_1$ ) and an accumulator ( $FB\text{-}ACC$ ), is used to further extend the dynamic range of the single-bit  $\Delta\Sigma$  modulator core as illustrated in the following derivation. The signal transfer function of the DT equivalent model of the  $\Delta\text{-}\Delta\Sigma$  modulator (see Fig. 3), is given by:

$$STF_{\Delta}(z) = \frac{V_{\Delta}}{U} = \frac{k_q b_3 (z-1)^2 + k_q b_2 c_2 (z-1)}{(z-1)^3 + k_q a_3 (z-1)^2 + k_q a_2 c_2 (z-1) + k_q a_1 c_2}. \quad (1)$$

Therefore, using the low-frequency approximation ( $f \ll f_s$ ,  $z = e^{j2\pi f/f_s} \approx 1 + \frac{j2\pi f}{f_s}$ ), the full-scale of the modulator can be determined to be

$$V_{FS} = \frac{\Delta}{|STF_{\Delta}(f)|} \approx \Delta \frac{a_1 f_s}{b_2 2\pi f}, \quad (2)$$

where  $f_s$  is the sampling rate and  $\Delta = 2$  is the quantizer's output step. The maximum signal power,  $P_{S,MAX}$ , and the input-referred quantization error,  $P_{ni,Q}$ , are respectively given by:

$$P_{S,MAX} = \frac{\alpha^2}{8} V_{FS}^2 = \Delta^2 \frac{\alpha^2 a_1^2}{8 b_2^2} \left( \frac{f_s}{2\pi f} \right)^2, \quad (3)$$

$$P_{ni,Q} = \frac{1}{k_q^2 b_2^2 c_2^2} \frac{\Delta^2}{12} \frac{\pi^{2L}}{(2L+1)OSR^{2L+1}}, \quad (4)$$

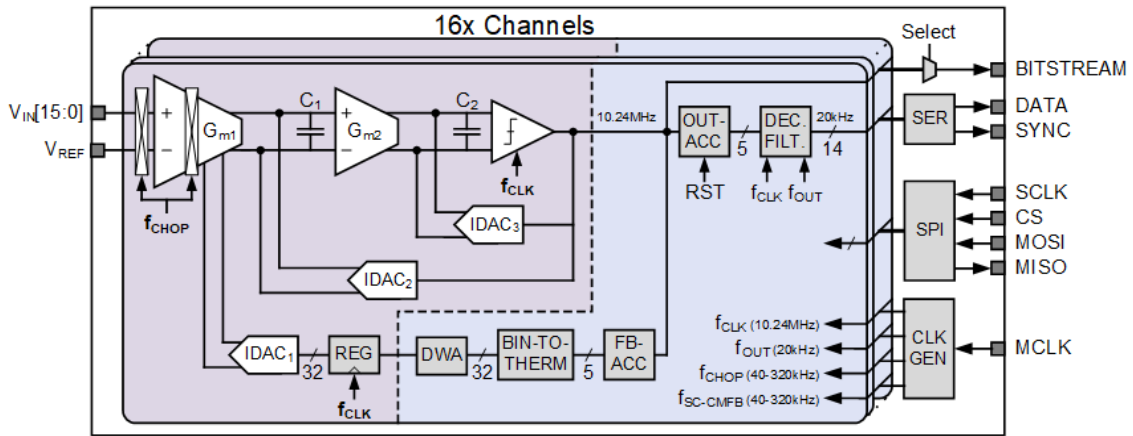


Fig. 2. High-level architecture of the proposed 16-channel DC-coupled  $\Delta\text{-}\Delta\Sigma$  neural readout prototype.

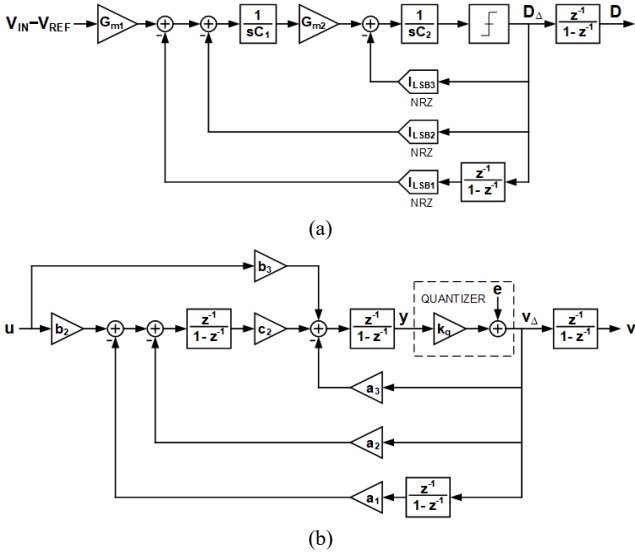


Fig. 3. Topology of the 2<sup>nd</sup>-order hybrid CT-DT  $\Delta$ - $\Delta\Sigma$  modulator. (a) Implementation. (b) DT equivalent model.

where  $\alpha < 1$  is the ratio of the maximum stable amplitude to the full-scale,  $L = 2$  is the order of the noise shaping, and OSR is the oversampling ratio. Therefore, the signal-to-quantization-noise ratio (SQNR) is:

$$SQNR_{\Delta\Delta\Sigma} = \frac{3\alpha^2 a_1^2 c_2^2 k_q^2 (2L + 1) OSR^{2L+1}}{2\pi^{2L}} \left( \frac{f_s}{2\pi f} \right)^2. \quad (5)$$

Equation (5) shows that the SQNR is inversely proportional to the frequency, as also determined in [27] through numerical simulations. Compared to a  $\Delta\Sigma$  modulator of the same noise-shaping order, the SQNR is increased by

$$SQNR_{\Delta\Delta\Sigma} = \left( \frac{f_s}{2\pi f} \right)^2 SQNR_{\Delta\Sigma}. \quad (6)$$

In practice, the input range is limited by the full-scale of the feedback DAC:

$$V_{FS,DAC1} = 2^{N_{DAC}} LSB_{in}, \quad (7)$$

where  $N_{DAC}$  is the number of bits of the feedback DAC of the outer loop ( $IDAC_1$ ) and  $LSB_{in} = \frac{a_1}{b_2}$  is the input-referred least significant bit (LSB). In [31], the recording channel is also based on a  $\Delta$ - $\Delta\Sigma$  modulator with digital integrators for the  $\Delta$ -modulation path. In that design, to achieve low input-referred quantization error with 1<sup>st</sup>-order noise shaping and low OSR, a large gain is adopted for the forward path, corresponding to a large  $b_2$  coefficient and resulting in an input-referred LSB  $< 100 \mu\text{V}$ . That choice enables low power consumption but requires a 12-bit DAC in order to digitize an input range of 260 mV<sub>pp</sub>, resulting in significant area overhead. In our case, to reduce the number of bits and area of the feedback DAC, a relatively large input-referred LSB of  $\sim 6 \text{ mV}$  was chosen, requiring only 5 bits for a target input range

TABLE I  
MAPPING BETWEEN COEFFICIENTS OF DT EQUIVALENT MODEL AND CT-DT IMPLEMENTATION PARAMETERS

DT Equivalent	CT-DT Implementation
$a_1$	$\frac{l_{LSB1}}{C_1 f_s}$
$a_2$	$\frac{l_{LSB2}}{C_1 f_s} + \frac{l_{LSB1}}{2C_1 f_s}$
$a_3$	$\frac{l_{LSB3}}{C_2 f_s} + \frac{l_{LSB2} G_{m2}}{2C_1 C_2 f_s^2}$
$b_1$	0
$b_2$	$\frac{G_{m1}}{C_1 f_s}$
$b_3$	$\frac{G_{m1} G_{m2}}{2C_1 C_2 f_s^2}$
$b_4$	0
$c_1$	1
$c_2$	$\frac{G_{m2}}{C_2 f_s}$

sufficient to allow the concurrent acquisition of LFPs ( $< 10 \text{ mV}_{pp}$ ), EDOs and stimulation artifacts without saturation [23]. A 2<sup>nd</sup>-order noise shaping and an OSR of 512 were used in our design to achieve low quantization error while also extending the signal bandwidth to 10 kHz, i.e. 20 times larger than that in [30], [31], for the acquisition of APs. Increasing both the LSB and the sampling-rate also allows to track artifacts with faster dynamics. In fact, the full-scale of the  $\Delta$ - $\Delta\Sigma$  modulator can also be determined in terms of the slope of the input signal:

$$\max \left( \frac{dV_{IN}}{dt} \right) = LSB_{in} \cdot f_s. \quad (8)$$

Obviously, condition (8) reduces to (2) for a sinusoidal input signal. In our case, the maximum input slope that can be tolerated without saturating the modulator is  $\sim 60 \text{ mV}/\mu\text{s}$ .

Dynamic Weighted Averaging (DWA) was chosen to mitigate the effects of the mismatch of the elements in  $IDAC_1$ , resulting in 1<sup>st</sup>-order mismatch shaping. The critical path for the excessive loop delay (ELD) is represented by the outer feedback loop, comprising the feedback accumulator  $FB-ACC$ , the binary to thermal converter, the DWA logic and  $IDAC_1$ . To relax its timing requirements, a CIFB topology was chosen for the modulator, since it uses a delaying integrator in the outer loop. This allows a full-clock cycle for the digital part of the critical path. A separate accumulator ( $OUT-ACC$ ) is used to integrate the comparator's output before decimation.  $OUT-ACC$  can be reset to mid-range independently from  $FB-ACC$ , thus enabling offset removal without requiring any additional power- or area-hungry digital subtractor. A 3-stage cascaded-integrator-comb (CIC) filter follows  $OUT-ACC$  to filter and decimate the bitstream, producing a 14-bit output at 20 kS/s.

The DT equivalent model was mapped to the DT-CT implementation parameters using the impulse invariant transformation, according to the relations in Table I. The DT  $b_3$  coefficient, as well as the dependency of  $a_2$  and  $a_3$  on  $LSB_1$

and  $LSB_2$ , respectively, arise from the double continuous-time integration in the cascade of  $G_{m1}-C_1$  and  $G_{m2}-C_2$ , as described for example in [33]. The choice of the design parameters results in small integrating capacitors  $C_1$  and  $C_2$  of only 230 fF and 100 fF, respectively.

### III. BLOCK LEVEL DESIGN

#### A. Input Transconductor ( $G_{m1}$ )

The first stage transconductance amplifier ( $G_{m1}$ ) serves as the input stage of the entire channel, and therefore it is critical for the noise performance and input impedance. It is also through  $G_{m1}$  that the input neural potentials are converted into current signals, which get integrated on  $C_1$  after subtraction of the  $IDAC_1$  feedback current, forming the first CT loop filter.

As shown in Fig. 4(a),  $G_{m1}$  is implemented using a current balancing structure [34]–[36]. This topology offers good input linear range because the transconductance is determined by the resistor  $R_{Gm1}$  instead of by the input differential pair. As illustrated in the half-circuit equivalent in Fig. 4(b), the input pair ( $MP_{1,2}$ ) together with  $MN_{1,4}$  and  $MP_{3,6}$  forms a flipped voltage follower (FVF) structure.  $MN_{1,4}$  contribute to an additional loop gain given by:

$$Av \approx g_{m,MN1} r_{ds,MN1} g_{m,MN3} r_{ds,MN3}, \quad (9)$$

where  $g_{m,*}$  is the transconductance and  $r_{ds,*}$  the on-resistance of the transistors. Thus, the equivalent impedance ( $Z_{eq}$ ) at nodes  $FB_P$  and  $FB_N$  gets further attenuated by this gain, and is given by:

$$Z_{eq} \approx \frac{1}{Av * g_{m,MP5} g_{m,MP1} r_{ds,MP1}}. \quad (10)$$

This low impedance facilitates driving  $R_{Gm1}$ ; therefore, the voltages at nodes  $FB_P$  and  $FB_N$  follow closely the input signal. The resulting current of  $V_I/R_{Gm1} - I_{IDAC1}$  is copied to the output through the 1:1 current mirror comprising  $MP_{3,10}$ . The equivalent transconductance of  $G_{m1}$  is 29  $\mu$ S, which is the inverse of the resistance of  $R_{Gm1}$ . This resistance is implemented with a polysilicon resistor for good area efficiency, and a 2-bit resistance trimming is used to achieve good accuracy over power, voltage and temperature variations. The resistance value is chosen considering the trade-off between power consumption, thermal noise and the desired input range. Note that the bandwidth of the signal path from nodes  $FB_P$  and  $FB_N$  to the outputs needs to be sufficiently wide [37] to accommodate the feedback signals from  $IDAC_1$ , which is clocked at 10.24 MHz.

Since the DC-coupled structure allows chopping at the input of  $G_{m1}$  to remove the flicker noise, the area of  $G_{m1}$  can be significantly reduced. As shown in Fig. 4, the choppers are deployed such that the current mirrors  $MP_{3,10}$ , where the feedback current of  $IDAC_1$  flows, remain at baseband. This consequently avoids any aliasing of high-frequency-shaped quantization noise in the  $IDAC_1$  feedback. There are several

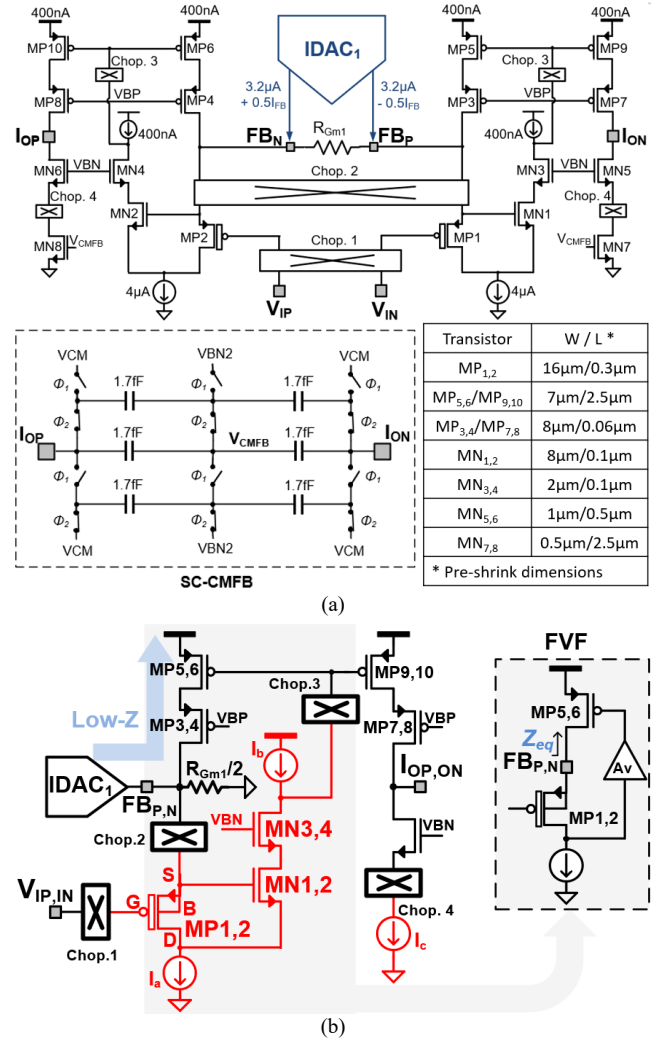
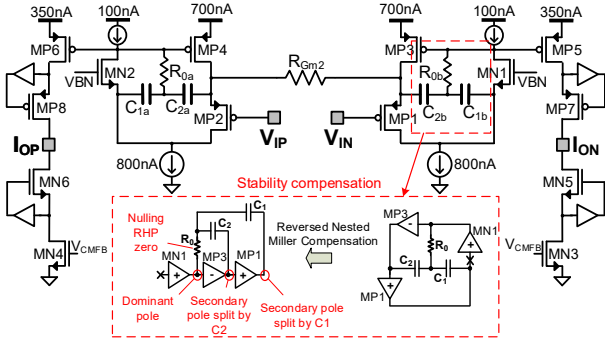


Fig. 4. (a) Schematic circuit of  $G_{m1}$  including the SC-CMFB. The listed transistor dimensions are pre-shrink values, since the 55-nm technology is a linear shrink process from the 65-nm technology. The actual fabricated transistor dimensions are 0.9 times the listed values. (b) Half-circuit equivalent. The flicker noise from the devices marked in red are mitigated by the proposed chopping scheme.

alternative methods to mitigate quantization-noise aliasing issues in  $\Sigma\Delta$  modulators such as chopping at the modulator sampling frequency, using a finite-impulse-response (FIR) DAC or using a return-to-zero DAC, but these are subject to high power consumption [38], increased area occupation [39] or high-precision clocks requirement [40].

Another challenge of chopping directly at the input of  $G_{m1}$  is the input impedance reduction. The parasitic capacitances at the input transistors  $MP_{1,2}$ , which are  $C_{gs}$ ,  $C_{gb}$ , and  $C_{gd}$ , form a switched-cap resistor when chopping is applied, which effectively reduces the input impedance. These capacitances are simulated as 8.4 fF, 2.6 fF and 6.4 fF, respectively. To mitigate this, several measures are taken in our design. Firstly, in the current balance and the FVF structures,  $MP_{1,2}$  have a fixed current flowing through them and hence act as source followers. This means that the gate and source have the same AC voltage, effectively bootstrapping out  $C_{gs}$ . Secondly,  $MP_{1,2}$  have their bulks connected to the sources, similarly mitigating the effects of

Fig. 5. Circuit schematic of the  $G_{m2}$  stage.

$C_{gb}$ . Finally, the transistors  $MN_{1,2}$  force the drains of  $MP_{1,2}$  to follow their sources. Thus, their gates, and consequently  $C_{gd}$ , are bootstrapped as well. Quantitatively, the relationship between the terminal voltages of  $MP_{1,2}$  is governed by the following the equations:

$$\begin{cases} (V_S - V_D)g_{m,MN1} \approx V_D/r_{ds,MN1} \\ (V_G - V_S)g_{m,MP1} \approx (V_S - V_D)/r_{ds,MP1} \\ V_S = V_B \end{cases} \quad (11)$$

where  $V_S$ ,  $V_D$  and  $V_B$  are the source, drain and bulk voltages of transistors  $MP_{1,2}$ . It can thus be derived that:

$$\begin{cases} V_S = V_B \approx \frac{(1+A_{v,MN1})A_{v,MP1}}{1+(1+A_{v,MN1})A_{v,MP1}} * V_G \approx V_G \\ V_D \approx \frac{(1+A_{v,MN1})A_{v,MP1}}{1+(1+A_{v,MN1})A_{v,MP1}} * \frac{A_{v,MN1}}{1+A_{v,MN1}} * V_G \approx V_G \end{cases} \quad (11)$$

where  $A_{v,MN1} = g_{m,MN1}r_{ds,MN1}$ ,  $A_{v,MP1} = g_{m,MP1}r_{ds,MP1}$ . Therefore, the effects of all the parasitic capacitances of  $MP_{1,2}$  are mitigated. The remaining parasitic capacitance that determines the input impedance after chopping is the one caused by metal routing between the first chopper (*Chop. 1*) and the input transistors. This has been minimized in the layout by keeping the routing distance short. Additionally,  $MP_{1,2}$  are thick-oxide transistors, which further avoids input impedance degradation due to potential gate leakages. Based on our pre-layout simulations, the proposed bootstrapping technique can increase the input impedance by a factor 3x.

The input-referred offsets caused by device mismatches will be upmodulated by the choppers, resulting in chopping ripple. This ultimately limits how small the devices can be, and trade-offs were made in the design to ensure that the induced chopping ripples do not exceed the LSB range of  $IDAC_1$  nor the dynamic range of the current mirrors  $MP_{3-10}$ . In this way, the chopping ripples will not interrupt the modulator operation or saturate  $G_{m1}$ , thus they can be effectively removed by the digital decimation filter.

Switched-capacitor-based common-mode feedback (SC-CMFB) is used to stabilize the output common-mode voltage to  $V_{CM}$ , which is half the supply voltage. SC-CMFB is used for good power-efficiency and stability. As shown in Fig. 4(a), complementary capacitor banks are used, which operate with opposite clock phases ( $\Phi_1$  and  $\Phi_2$ ) to ensure that

the output nodes have the same loading from the SC-CMFB in each phase [41]. The inputs to the SC-CMFB are nodes  $I_{OP}$  and  $I_{ON}$  where the signals are already at baseband. *Chop. 4* only chops the mismatch and flicker noise of  $MN_{7,8}$ . Therefore, no additional chopper is needed for the SC-CMFB. The reference  $V_{BN2}$  is generated from replica biasing based on the dimension and drain current of  $MN_{7,8}$ . Minimum-size metal-oxide-metal (MOM) capacitors are used to reduce area occupation, and the switching frequency is a compromise between the  $G_{m1}$  output impedance and the CMFB bandwidth.

Finally, the input stage of  $G_{m1}$  can tolerate common-mode input voltages between -100 mV and 500 mV. This is sufficient to accommodate common-mode EDO's or artifacts.

### B. Second Transconductor ( $G_{m2}$ )

The transconductance amplifier for the second integrator ( $G_{m2}$ ) interfaces with the output of the 1<sup>st</sup> integrator. Its output is connected to  $C_2$ ,  $IDAC_3$  and the comparator. Thus,  $G_{m2}$  needs to accommodate large voltage swing (600 mV<sub>pp</sub>) at both input and output. A high output impedance is also required to maintain the modulator noise transfer function. Similar to  $G_{m1}$ , a current-balanced structure with FVFs is used to obtain sufficiently high linearity for the required input range. As shown in Fig. 5, the required equivalent transconductance of 1  $\mu$ S is obtained by using an  $R_{Gm2}$  with 500-k $\Omega$  resistance and current mirrors  $MP_{3-6}$  with 2:1 ratio to the output branch. Reversed nested miller compensation comprising  $R_{0a-b}$ ,  $C_{1a-b}$ , and  $C_{2a-b}$  is used to stabilize the FVF loop [42]. To boost the output impedance, regulated cascodes are applied to all the output branches. A SC-CMFB is also used here for the same reasons as in  $G_{m1}$ . The switching clock edges are set far away from the rising edge of the sampling clock of the comparator at which the quantization is done, and thus the impact of switching transitions on the quantization accuracy is mitigated.

### C. Current DACs

$IDAC_1$  implements the first feedback current steering DAC of the readout channel. As seen in Fig. 6(a), it is a 2-level, 5-bit thermometer-coded DAC consisting of 32 unit elements. It receives the thermometer codes generated by the DWA logic inside the digital block and sends its outputs to the feedback nodes of  $G_{m1}$ . The DWA logic [43] includes a barrel shifter controlled by a 5-bit pointer register  $P[4:0]$ . Each of the  $IDAC_1$  unit elements is a current steering structure, where the unit current is set by the PMOS current source and a pair of complementary switches. Cascode transistors are used to increase the output impedance, and the switches are inserted in between the tail current source and the cascode to mitigate the impact of the switching glitches on the output. The flicker noise of  $IDAC_1$  is not mitigated by the chopping used in  $G_{m1}$  and thus not negligible. Based on our simulations, it contributes to ~38% of the total noise at low frequency (0.5Hz-1kHz).

The remaining two DACs,  $IDAC_2$  and  $IDAC_3$ , are respectively the 2<sup>nd</sup>- and the 3<sup>rd</sup>-stage feedback DACs in the

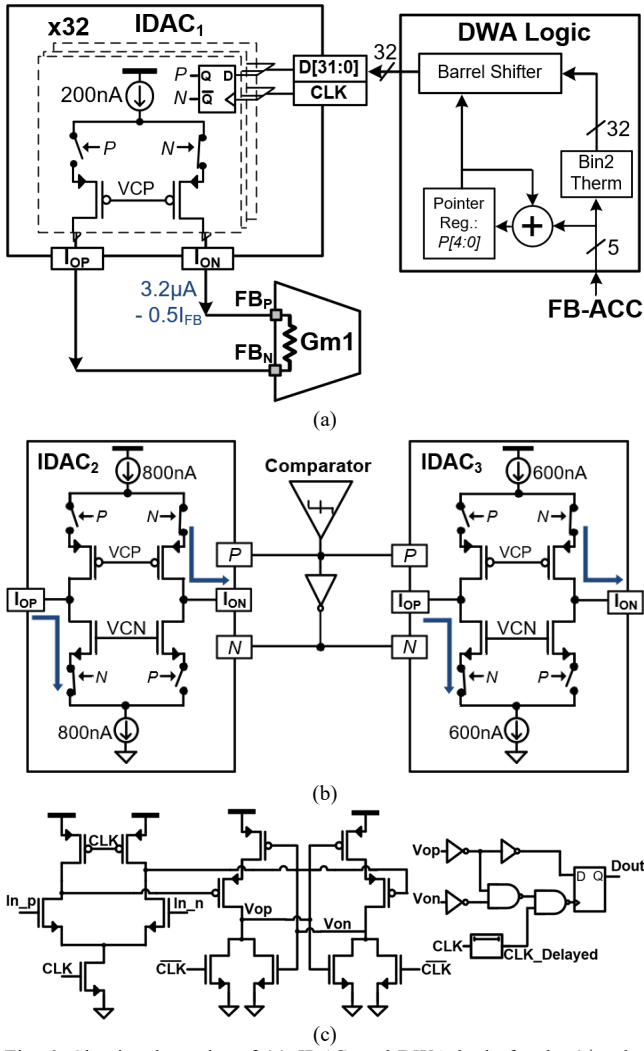


Fig. 6. Circuit schematics of (a)  $IDAC_1$  and DWA logic for the 1<sup>st</sup>-order mismatch noise shaping, (b)  $IDAC_2$  and  $IDAC_3$  and (c) comparator.

modulator (Fig. 6(b)). The designs of the two blocks are highly correlated as they use the same unit elements, and they share the same biasing.  $IDAC_2$  scales the unit element by 4, whereas  $IDAC_3$  scales them by 3. The input of the two blocks is from the quantization (comparator) output bitstream. Control signals for these two blocks are generated from the quantization bitstream with a shared logic block. The outputs of the two blocks interface respectively with the outputs of  $G_{m1}$  and  $G_{m2}$  where large voltage swings are present.

#### D. Comparator

As shown in Fig. 6(c), the comparator, based on the topology of [44], performs single-bit quantization. Its offset and noise requirements are significantly relaxed thanks to the noise shaping nature of delta sigma modulator. The remaining critical design target is to achieve minimum kickback; therefore, the ‘double tail’ topology is used here.

### IV. EXPERIMENTAL RESULTS

A 16-channel proof-of-concept IC was fabricated in 55-nm CMOS technology. The chip micrographs and the area breakdown for the individual blocks in each channel are

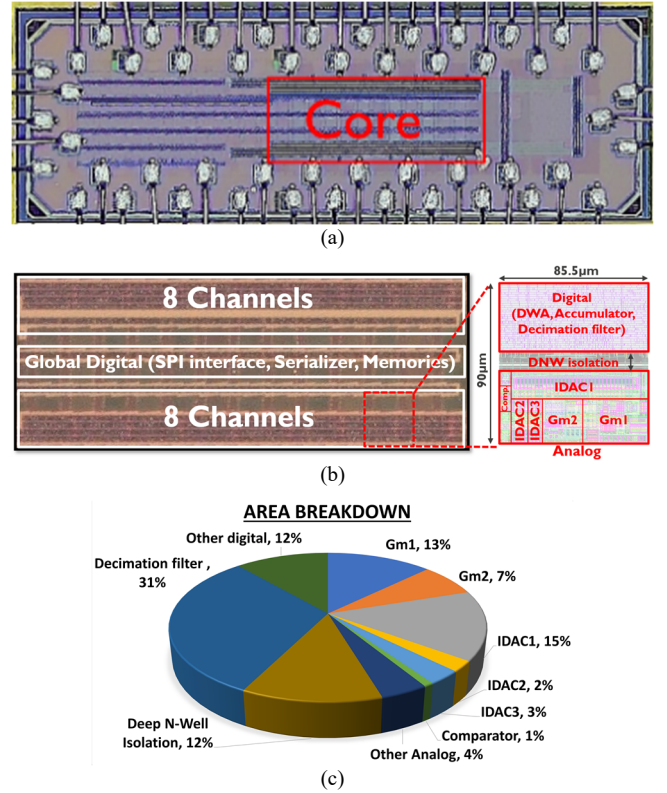


Fig. 7. (a) Chip micrograph, (b) micrograph of the chip core area highlighting the different building blocks, and (c) channel area breakdown.

shown in Fig. 7. The achieved channel area is only  $90 \mu\text{m} \times 85.5 \mu\text{m}$ , which includes all the analog and digital circuit blocks of the proposed  $\Delta$ - $\Sigma$  mixed-signal architecture. A deep-Nwell isolation was included in each channel to shield the sensitive analog blocks from the digital switching noise. The total power consumption in each channel is  $61.2 \mu\text{W}$ , of which  $17 \mu\text{W}$  (28%) are consumed by the analog circuits and  $44.2 \mu\text{W}$  (72%) by the digital portion of the channel. Over 80% of the digital power consumption is due to the decimation filter, which was not optimized in this prototype. Additionally, the digital circuits were synthesized using regular-Vt standard-cells libraries working at a nominal voltage of 1.2 V, and followed a standard place-and-route methodology. By optimizing the decimation filter architecture and the register-transfer-level (RTL) design, the power of the decimation filter could be potentially significantly reduced.

To demonstrate the effectiveness of the  $\Delta$ - $\Sigma$  modulator, we measured the noise spectra before the decimation filter with grounded inputs. As shown in Fig. 8, the 2<sup>nd</sup> order noise shaping, equivalent to 40 dB/decade, is clearly visible in the output spectrum. The 40-kHz CMFB clock and 80-kHz chopping clock and their harmonics all fall outside the signal band and will be filtered out by the decimation filter. This was confirmed by measuring the noise after the decimation filter (see Fig. 9(a)). The achieved full-channel input-referred noise in the AP (300 Hz – 10 kHz) and LFP (0.5 Hz – 1 kHz) bands are  $5.53 \pm 0.36 \mu\text{V}_{\text{rms}}$  and  $2.88 \pm 0.18 \mu\text{V}_{\text{rms}}$ , respectively, with excellent uniformity across the 16

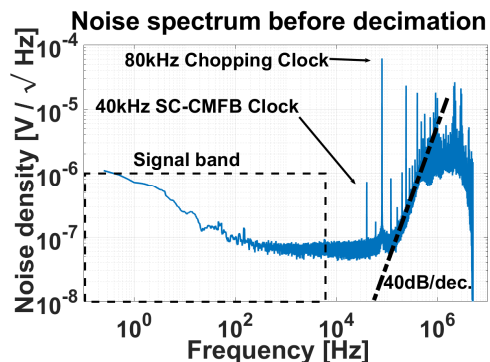


Fig. 8. Measured input-referred noise spectrum before the decimation filter.

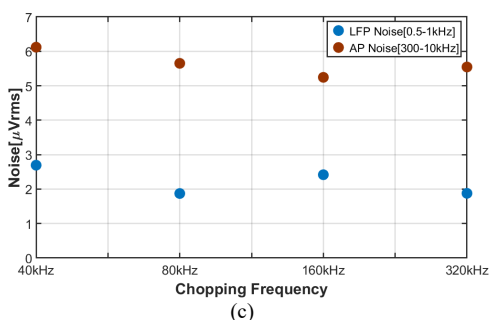
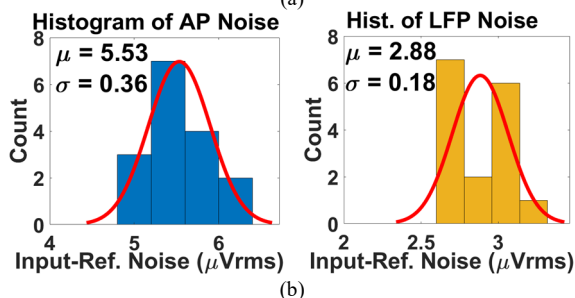
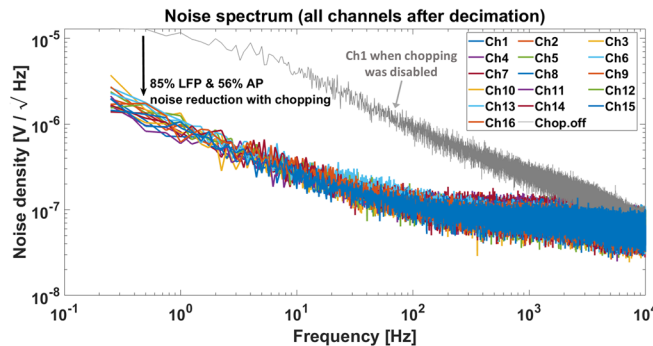


Fig. 9. (a) Measured noise spectrums from all channels after decimation. (b) Histograms of the input-referred noise in the AP (left) and LFP (right) bands. (c) Measured input-referred for noise for different chopping frequencies.

channels (see Fig. 9(b)). These measurements also confirm the effectiveness of the chopping technique implemented in  $G_{m1}$ . The measured noise for different chopping frequencies in one channel is shown in Fig. 9(c). The LFP noise gets slightly improved at higher frequencies as expected. As explained in Section III-A, the remaining flicker noise in these measurements is caused by the PMOS current mirrors  $MP_{5,6}$  and  $MP_{9,10}$  in Fig. 4, which were not chopped intentionally. Fig. 10 shows the measured output transient waveforms of all the 16 channels when a 10-mV<sub>pp</sub>, 1-kHz

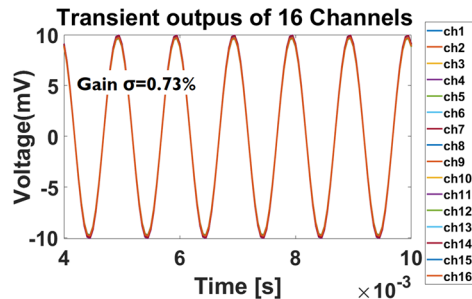


Fig. 10. Measured outputs from the 16 channel when a sinusoidal input is applied.

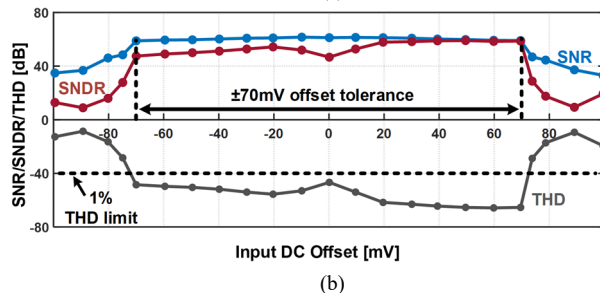
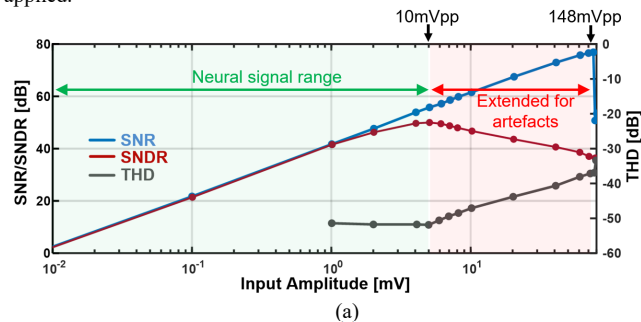


Fig. 11. Measured SNR, SNDR and THD against (a) input amplitude, and (b) input DC offset.

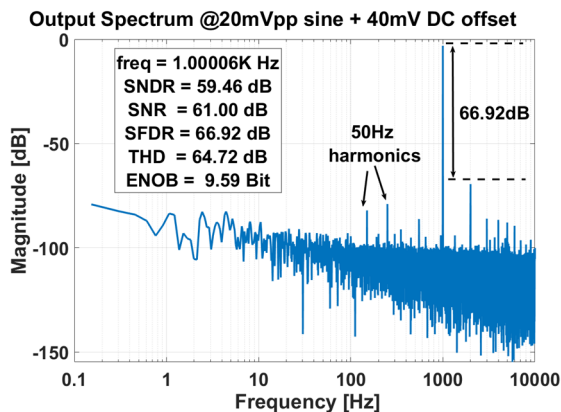


Fig. 12. Output spectrum with peak SNDR for a 20-mV<sub>pp</sub> input sine wave with 40 mV DC offset.

sinusoidal input signal was applied. The gain across channels is also very uniform, with a standard deviation of only 0.73%.

Fig. 11(a) shows the measured signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SNDR) and total harmonic distortion (THD) versus the input amplitude for a 1-kHz input signal with no input DC offset. The THD remains below -50 dB (0.3%) for AC input amplitudes of up to 10 mV<sub>pp</sub>, which is considered the maximum amplitude of extracellular neural signals. While distortion starts to appear

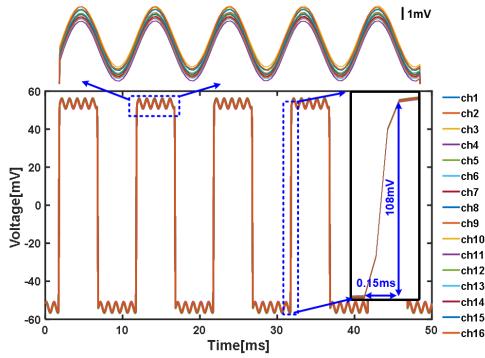


Fig. 13. Measured output signal when a large transient step (emulating a stimulation artifact) is superimposed to a small sinuswave input signal.

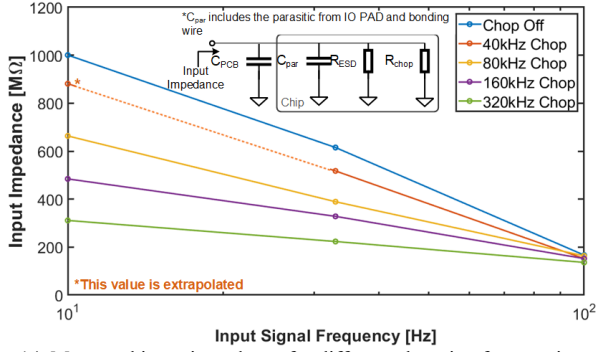


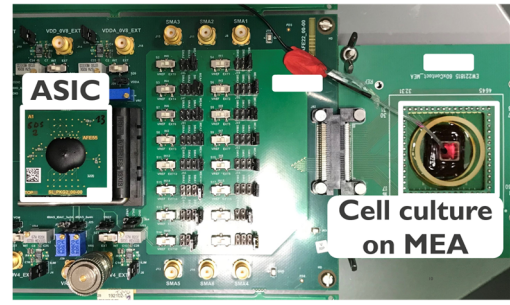
Fig. 14. Measured input impedance for different chopping frequencies.

for larger signals, primarily due to the non-linearity of  $IDAC_1$ , the THD remains below 1% for AC input amplitudes up to  $\sim 80$  mV<sub>pp</sub>, which is generally considered acceptable in a neural recording application. Furthermore, our readout architecture achieves a maximum SNR of 77 dB for an input amplitude of 148 mV<sub>pp</sub>, at only slightly reduced THD ( $\sim 1.5\%$ ) performance.

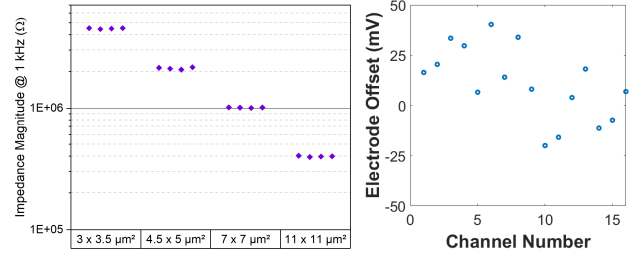
To validate the performance in the presence of EDOs, we applied a sinusoidal signal with a worst-case amplitude of 20 mV<sub>pp</sub> and swept the DC offset. The results shown in Fig. 11(b) indicate that the chip can tolerate up to  $\pm 70$  mV input DC offsets with minimal performance degradation, which is in line with our design targets. The output spectrum for a 20-mV<sub>pp</sub> input sine wave with 40 mV DC offset is shown in Fig. 12. In this specific case, the peak SNDR was measured as 59.5 dB.

To characterize the input tracking capability, we measured the response of the readout channel to a synthesized waveform that combines a sinusoidal signal (10 mV<sub>pp</sub> @ 1 kHz) with large transient pulses (110 mV<sub>pp</sub>) mimicking stimulation artifacts. Fig. 13 shows the measured output signal for the 16 channels, demonstrating that fast tracking was observed at every transient event without saturation.

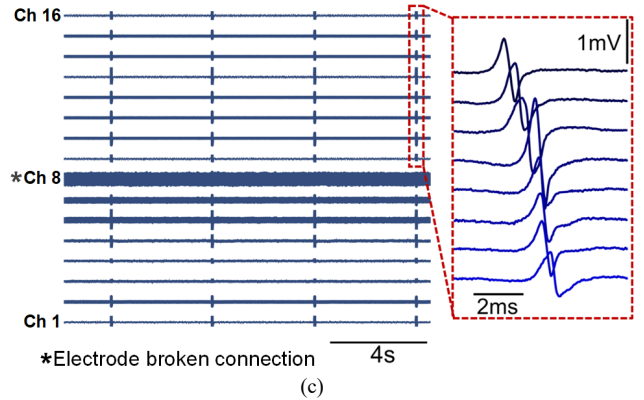
The input impedance of the readout channel (see Fig. 14) was measured for different chopping frequencies over a low-frequency range from 10 Hz to 100 Hz. As expected, the input impedance gets degraded for higher chopping frequencies. As shown in the figure, the measured input impedance includes the leakage currents of the IO pads ( $R_{ESD}$ ), and the parasitic capacitances of the IO ( $C_{par}$ ) and PCB ( $C_{PCB}$ ). Since the input impedance is not constant over



(a)



(b)



(c)

Fig. 15. Validation of the chip *in vitro* with cardiac cells cultured on an external MEA. (a) *In vitro* setup. (b) Measured electrode impedance for 4 electrode sizes and input offsets extracted from our *in vitro* measurements. (c) Measured cardiac action potentials.

this low-frequency range as expected in a chopper-stabilized amplifier, we deduced that this input impedance is dominantly degraded by the parasitic capacitance at the channel input ( $C_{par} + C_{PCB}$ ). The input impedance at 10 Hz for an 80-kHz chopping frequency is 663 MΩ. This is sufficiently high to enable the recording of neural signals without degradation from the small ( $144 \mu\text{m}^2$ ) TiN electrodes used in our neural probes [4].

Finally, to demonstrate the functionality of the proposed readout architecture in a real biological application, we have performed *in vitro* experiments. For this, the proof-of-concept IC was connected to a passive microelectrode array (MEA), which consists of an array of TiN electrodes of various sizes ( $20\text{-}121 \mu\text{m}^2$ ) and was packaged on a custom PCB (see Fig. 15(a)). A glass ring was glued on top of the PCB to contain the cells and the cell medium, and an external Ag-AgCl wire was used to ground the cell medium. We cultured iCell Cardiomyocytes<sup>2</sup> cells on the MEA. Extracellular action potentials from cardiac cells have the same frequency distribution as neural signals with slightly higher amplitudes, and they were used in our experiments



TABLE II.  
PERFORMANCE COMPARISON WITH STATE-OF-THE-ART NEURAL RECORDING CHIPS (FOR PENETRATING-ELECTRODE APPLICATIONS ONLY)

	This Work	Wang, TBCAS19	Wendler, ISSCC21	De Dorigo, JSSC18	Chandrakumar, JSSC18	Lee, JSSC20	Park, JSSC18
Technology / Supply (V)	55nm / 1.2	130nm / 1.2	180nm / 1.8	180nm / 1.8	40nm / 1.2	110nm / 1.0	180nm / 0.5/1.0
# of channels	16	384	8, 12 & 24	144	1	1	128
Channel topology	2nd-order $\Delta$ - $\Delta\Sigma$	IA+SAR	Two-step $\Delta\Sigma$	1st-order $\Delta\Sigma$	IA+3rd-order $\Delta\Sigma$	2nd-order $\Delta\Sigma$	IA+1st-order $\Delta$ - $\Delta\Sigma$
Input structure	DC-coupled with chopping	AC-coupled	DC-coupled	DC-coupled	DC-coupled with chopping	DC-coupled	AC-coupled
Input Impedance ( $\Omega$ )	663M@10Hz	179.9M@1kHz	$\infty$ @DC*	$\infty$ @DC*	1.52G@DC; 19.6M@5kHz	$\infty$ @DC*; 13.3M@10kHz	*
AC input range (mV <sub>pp</sub> )	148	12.5	14	40	200	300	*
EDO tolerance	$\pm 70$ mV	Rail-to-rail*	$\pm 7$ mV*	$\pm 45$ mV*	$\pm 100$ mV	$\pm 50$ mV	Rail-to-rail*
THD @1kHz input	0.05-0.44%@20mVpp***	0.17%@10mVpp	0.074%@10mVpp	0.75%@40mVpp	0.009%@200mVpp	0.0095%@285mVpp	0.019%@3mVpp
Bandwidth (kHz)	10	10	10	10	5	10	10.9
AP noise 0.3-10kHz ( $\mu$ V <sub>rms</sub> )	$5.53 \pm 0.36$	7.44	3.93	20.19	6.35	9.5	3.32
LFP noise 0.5Hz-1kHz	$2.88 \pm 0.18$	7.65	2.31	8.43	(1Hz ~5 kHz)	(1Hz ~10 kHz)	(0.5Hz ~12.7 kHz)
NEF (AP+LFP)	17.1 / 9.8**	26.1	6.8	42.6	8.5**	9.3**	3.02
Power/channel ( $\mu$ W)	61.2	48.7	13.94	46.29	7.3**	6.5**	3.05
Area/channel (mm <sup>2</sup> )	0.0077	0.035	0.00378	0.0049	0.113**	0.078**	0.058

\*Not measured

\*\*Decimation filter not included

\*\*\*With -70mV ~ +70mV DC offset

because of the ease of the cell culturing, the spontaneous beating, and the straightforward interpretation of the data. The TiN electrodes on this MEA were fabricated using the same process as those in [4], but are smaller and thus have higher impedance (see Fig. 15(b) left) and noise. Despite this, our chip was able to record extracellular signals from all electrode sizes and tolerate EDOs without saturation as shown in Fig. 15(c). Note that the noise levels in this experiment are dominated by the electrode impedance. We have extracted the input-referred offset from this *in vitro* measurement and the values are shown in Fig. 15(b) right. Please notice that this offset is not the open-circuit potential (OCP) of the electrode, but the total offset that appears at the input of our readout circuit. This offset has contributions from the OCP, the voltage divider formed by the electrode impedance and the readout input impedance at DC, the input-referred offset of our readout and any leakage flowing through the electrode.

The chip performance is compared with the state of the art in Table II. Please notice that only neural recording chips for penetrating-electrode applications were considered. The best compromise among area, noise, bandwidth, EDO tolerance, input range and input impedance has been achieved in this design. Compared to our previous neural probe design which is now widely used in neuroscience community [5], this design reduces the area per channel by roughly a factor 5, while achieving even better noise performance and the capability to tolerate large artifacts.

## V. CONCLUSION

In this paper we proposed a DC-coupled 2<sup>nd</sup>-order  $\Delta$ - $\Delta\Sigma$  readout architecture for scalable neural recording. This architecture uses new bootstrapping and chopping schemes, which provide large dynamic range while maintaining a high input impedance. A 16-channel proof-of-concept IC was fabricated and fully characterized. Our results confirm that we achieved a good compromise among area, noise,

bandwidth, EDO tolerance, input impedance and input range. Although the power consumption in this prototype is high, the digital power can be significantly reduced by optimizing the decimation filter design and lowering the supply voltage. The analog power consumption is mainly needed in our architecture to achieve high input impedance and low input-referred quantization noise. Thus, a different trade-off could be made to reduce this power. Finally, our chip was verified in an *in vitro* experiment, demonstrating the functionality of our architecture in a cell-interfacing application. With the validated architecture and circuit techniques, this work opens new opportunities for the development of future neural probes to achieve ultra-high-density electrophysiology.

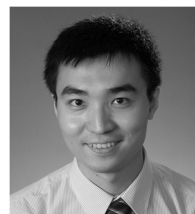
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