

Conduction Channel Configuration Controlled Digital and Analog Response in TiO₂-based Inorganic Memristive Artificial Synapses

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1 Operating current regime is found to play a key role in determining the synaptic characteristic
2 of memristor devices. Conduction channel that is formed using high current compliance prior to
3 the synaptic operation results in digital behavior; the high current stimulus forms a complete
4 conductive filament connecting the cathode and anode, and the high electric field promotes
5 abrupt redox reactions during potentiation and depression pulsing schemes. Conversely, the
6 conduction can be reconfigured producing filamentary-homogeneous hybrid channel by utilizing
7 low current stimulus, and this configuration enables the occurrence of analog behavior. The
8 capabilities of memristors showing programmable digital-to-analog or analog-to-digital
9 transformation open a wide range of applications in electronics. We propose a conduction
10 mechanism to explain this phenomenon.

Index Terms – memristor, artificial synapse, resistive memory, analog, digital

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Analog memristor technologies offer promising potential for in-memory computing applications.¹ In-memory computing is a state-of-the-art computer architecture that envisages data processing in the memory unit and, thus, overcomes data latency between memory and central processing units.¹ Memristor device has a facile top-electrode/metal oxide (switching layer)/bottom-electrode sandwich architectonic rendering ultra-high-density circuits;² the recent effort has successfully fabricated cross-bar arrays having sub-15 nm cells.³ Moreover, such a small dimension and its low power operation could realize memristor-neuron coupling to enable silicon-brain interface.^{4,5}

Several physical and chemical mechanisms have been proposed to explain the electron conduction in the memory cell, such as based on metallic diffusion (electrochemical metallization), valence change, thermo-chemical, and interfacial coupling mechanisms.⁶⁻⁸ Valence change memristor is controlled by an electric field that induces the formation and rupture of oxygen vacancies filaments to switch the device On (state 1) and Off (state 0), respectively, also called memristive behavior.⁹ The formation of the filament is initiated by the creation of oxygen vacancies by ionizing the oxygens from the lattice of the oxide switching layer, and these vacancies grow from cathode to anode while the oxygen ions drift to and are oxidized at the anode/switching layer interface; the electrons, then, can easily flow through this filament enabling the device in low resistance state (LRS, state 1).¹⁰ Conversely, the filament can be ruptured by re-ionizing the oxygens at the anode/switching layer interface to recombine with the vacancies creating a conduction gap between the electrode and remnant of the filament and, hence, switch the device to a high resistance state (HRS, state 0).¹⁰

Furthermore, the formation and rupture of the filaments can be exploited by an electric stimulus having short pulses and small amplitude to exhibit multiple states (beyond 1 and 0

states); consequently, the device can perform an analogous gradual rise and fall of the conductance.¹¹ The gradual rise and fall of the conductances are called potentiation and depression, respectively, mimicking the mammalian brain's analogous synaptic weight response.¹² However, the fabrication of analog memristors requires careful design and optimization, which makes the manufacturing process is still a great challenge; this is because the memristor devices often show digital behavior instead of analog, where the conductance change occurs abruptly.¹³

Various designs have been proposed to achieve a reliable synaptic response, but mostly focus on programming the pulse scheme¹¹ and engineering the switching materials such as bilayering,¹⁴ doping,¹⁵ embedding with nanocrystals,¹⁶ and surface modification.¹⁷ These methods indeed could improve the synaptic response; however, the fundamental question of the relationship between the electron conduction and the structure of the filaments determining such analog and digital in memristor devices is still less examined. In this work, we investigate the conduction channel configuration at the interface responsible for dictating the analog and digital response of the memristors. We explain the occurrence of digital-to-analog transformation in the device, and the conduction mechanism is also proposed by studying the phenomenon observed in the devices having different thicknesses.

The device architecture and measurement setup are depicted in Figure 1(a) and (b), respectively. A 15 nm TiN bottom electrode (BE) was deposited onto Pt/Ti-coated Si-wafer substrate employing atomic layer deposition technique. TiO₂ switching layer films with thicknesses of 16 and 25 nm were deposited onto the bottom electrode. Hereafter, TiN/Ti bilayer top electrodes (TE) having a diameter of 250 μm were patterned onto the TiO₂ films using a metal shadow mask. The sheet resistance of the TiN electrodes is found to be less than 19 ohm/sq. The

thicknesses of TiN and Ti are 50 and 15 nm, respectively. The TiO₂, TiN, and Ti films were deposited using a DC sputtering system from a Ti target in a mixture of Ar/O₂, Ar/N₂, and Ar ambient, respectively. The devices made with 16 and 25 nm thick TiO₂ films were denoted as D16 and D25, respectively. The electrical characteristics were investigated using an Agilent B1500A semiconductor analyzer. A voltage bias was applied to the top electrode while the bottom electrode was ground; a current compliance (CC) was used during the positive bias voltage sweep to avoid permanent breakdown. For DC sweep, a negative bias of -1.4V was used for all devices to switch the device Off. In the case of synaptic measurement, AC pulse schemes were used to induce the response by applying pulse amplitudes of -1.2 and 1V for depression and potentiation, respectively, with a pulse width of 20 μ s. Meanwhile, the pulse read was conducted using an amplitude of 0.1V with a width of 1 ms. An epoch consists of 500 pulses of depression (D) and 500 pulses of potentiation (P). Note that the synaptic response test was conducted after several switching cycles. The element profile and defect were measured using x-ray photoelectron spectroscopy (XPS, PHI Quantera SXM).

D16 device requires an electroforming process with a CC of 10 mA to activate the memristive behavior by switching the pristine resistance state to a low resistance state (LRS, On) with a positive bias of 2.7 V, as depicted in Figure 1(c). Hereafter, the device can be switched to a high resistance state (HRS, Off) and low resistance state (LRS, On) by sweeping a negative bias voltage (called as RESET) and a positive bias of approximately 0.9V (called as SET). The synaptic behavior of the devices was initiated with a depression scheme after the devices were switched to the On state. It is found that the conductance of D16 is abruptly decreased during the first pulse, from approximately 8 to 1 mS, and the conductance value saturates at approximately 1 mS regardless of the continuous pulses (inset of Fig. 1(c)); similarly, the conductance is

abruptly increased to approximately 9 mS during the first pulse of potentiation scheme, and conductance saturates at this level. Note that the pulse amplitudes of -1.2 V for depression and 1 V for potentiation are the minimum voltages to exhibit such conductance changes in D16. The abrupt conductance change indicates that the D16 device shows digital behavior and is unable to perform an analog synaptic response (denoted as D16CC10). However, the synaptic response can be observed after we carry out the switching process at a lower operating current (employing CC of 2 mA for the SET process prior to the synaptic response test, denoted as D16CC2), as shown in Figure 1(d). Figure 1(e) shows that D16CC2 is able to show analogous gradual conductance changes performing 9 stable epochs (a total of 9000 pulses) with a dynamic range of approximately 3.6 times.

The above results brought us to question why a device that was initially operated using a high CC can be programmed to perform a digital-to-analog transformation by utilizing a low CC. To confirm the relationship between the operating current and switching transformation, whether such phenomenon can occur in the reverse direction (analog-to-digital) by increasing the CC, we conducted the same experiment on the device having a thicker switching layer (D25). A thicker switching layer film provides enough pristine cell resistance that allows us to activate the memristive behavior at a lower CC.¹⁸ D25 requires an electroforming at CC of 2 mA with a positive bias of 3.6V, and thereafter, the RESET and SET processes can be performed at this current level, as depicted in Figure 2(a). The forming voltage of the D25 is higher than that of D16 due to the higher energy is needed to construct the filament across the larger gap between the BE and TE.¹⁸ The D25 device is able to perform an analogous synaptic response by exhibiting gradual fall (depression) and rise (potentiation) of conductance upon the repeated pulses, as depicted in the inset of Fig. 2(a) (denoted as D25CC2). Hereafter, for comparison, we

raised the CC of the SET process to 10 mA, and the device switches at this current level, as shown in Fig. 2(b) (denoted as D25CC10). Similar to the D16CC10 case (Fig. 1(c)), the high CC leads to an abrupt conductance change (inset of Fig. 2(b)). The employment of the SET process with a high CC prior to the synaptic test degenerates the synaptic response in the D25 device; the conductance falls (during the depression) and rises (during potentiation) abruptly during the first few pulses, and their conductance level saturates thereafter (inset of Fig. 2(b)). This abrupt characteristic can be classified as digital behavior. The epoch endurance of the D25CC10 exhibits highly nonlinear potentiation and depression with a larger dynamic range as compared to the D25CC2 device, as demonstrated in Figures 2(c) and (d), indicating analog-to-digital transformation phenomenon.

Note that we notice the rise and fall of conductance in D25CC2 are rather steep; this is because the pulse amplitudes were too high for this device. The synaptic linearity can be adjusted by simply varying the pulse amplitude,¹¹ as demonstrated in Fig. 3. The nonlinearity can be decreased to 42% employing pulse amplitude of -0.9 and 0.86 V for depression and potentiation, respectively. The linearity-dynamic range trade-off dilemma is commonly observed in analog synaptic memristor devices;¹⁹ when the pulse amplitudes decrease, the linearity increases while the dynamic range of the synaptic response decreases. Nonetheless, all of the pulse schemes perform robust epoch endurance for more than 9000 pulses.

Several reports suggest that the thickness of the oxide material controls the switching characteristics of the device.^{20–23} However, in our case, we observed that the switching characteristic (digital or analog) is dependent on the applied current level (CC) to construct the filament (forming/SET), not the thickness. The CC level dictates the number of electrons that can flow through the cell²⁴ and, thus, could determine the structure of filament (size and shape) in the

cell. We conduct curve-fitting on the LRS curves to elucidate the electron conduction mechanism in the devices, and the result is shown in Figure 4; the LRS curves were taken from the SET process. The electron conduction in the devices that endure a SET process using CC of 10 mA is dominated by Ohmic conduction ($I \propto V$).²⁵ Meanwhile, the ones using CC of 2 mA have two mechanisms; the low and high voltage regions are dominated by Ohmic and Frenkel-Poole ($\log(I/V) \propto \sqrt{V}$)²⁵ emissions, respectively. The schematic of the band diagram is shown in Figure 4(c-e).^{26–28} In Ohmic conduction, a number of electrons are generated due to thermal excitation and move in the conduction band, whereas in Frenkel-Poole conduction, the electrons can hop from the traps to the conduction band owing to the high electric field.²⁵ The transition from single to double conduction mechanisms when the maximum operating current level of the device is changed from high (10 mA) to low (2 mA), or vice versa, indicates that the conduction channels (filament structure) of the two cases may be different.

The defect concentration in the switching layer, especially at the interface region where the switching mainly occurs, plays a role in determining the formation of the conduction channels;²⁹ henceforth, we carried out XPS analysis to elucidate the oxygen vacancies (Vo) defect distribution in the device. Figure 5(a) shows the depth-XPS spectra of the TiN/Ti/TiO₂/TiN (D25) stack. It is observed that the Ti layer scavenged some oxygens from the TiO₂ layer. We analyzed the O1s spectra of the TiO₂ at the top interface (near TE), middle, bottom interface (near BE) regions, and the result is shown in Figure 5(b). The spectra can be deconvoluted into two distinct peaks centered at 529.8 and 531.9 eV owing to the oxygen concentration in the lattice (fully oxidized) and non-lattice (oxygen-deficient) regions, respectively.³⁰ The defect concentration was calculated by taking the ratio between non-lattice and lattice oxygens,³⁰ and it is found that the Vo concentration near TE is high and it gradually decreases when closer to BE;

the Vo concentration at the top interface, middle, and bottom interface is 28.8, 21.3, and 14.9 %, respectively.

Based on the above results, we propose a conduction mechanism to explain the electrical phenomenon in the device, as depicted in Figure 6. The pristine state of the TiO₂ layer has a high amount of Vo (Fig. 5(b)), and most of these pre-existing Vo drift to the BE during positive bias sweep and form a filament that grows from BE to TE; however, the employment of low CC (2 mA) is not sufficient to form a complete filament Fig. 6(a)(i). Nevertheless, the electron can still flow through the abundant Vo defects that scatter in the O-poor region at the Ti/TiO₂ interface (Fig. 5(b)). Henceforth, we suggest that the conduction channel in a low CC scenario ((D16CC2 and D25CC2) consists of an incomplete filament and a conducting bulk (homogeneous) configuration. At low voltage supply, a low number of electrons are injected into the cell, and the electrons can easily flow from cathode to anode following Ohmic conduction mechanism; however, at high voltage supply, the conducting bulk (homogeneous region) needs to accommodate the flow of a large number of electrons where most of the electrons hopping through the traps (Vo) following Frenkel-Poole emission mechanism (Fig. 4). This filamentary-homogeneous configuration helps the occurrence of analog characteristics. During depression (Fig. 6(a)(ii)), the negative amplitude pulses gradually ionize the pre-existing oxygens in the Ti layer ($\frac{1}{2}O_2 + 2e^- \rightarrow O_i^{2-}$), that were scavenged from the TiO₂ (during the fabrication process), and then recombine with Vo defects in the O-poor region ($Ti_{Ti}^x + 2V_o^{2+} + 2O_i^{2-} \rightarrow TiO_2$). Conversely, the potentiation process is followed by a continuous re-ionization of oxygen from the homogeneous region, and these oxygens drift back to the Ti scavenger layer. Note that only a small number of electrons can be injected into the cell at each pulse since the operating current level in the device is low; hence, this condition further assists the moderate oxygen ionization

and recombination processes. On the other hand, the employment of high CC (10 mA) to SET the device providing sufficient energy to repulse the Vo (including from the O-poor region at the top interface) towards the bottom electrode and forming a complete filament (Fig. 6(b)(i)); moreover, since the operating current level in the device is high, a high electric field is generated in the cell, and it encourages the creation of new Vo defects ($O_o^x \rightarrow V_o^{2+} + O_i^{2-}$) to accelerate the filament formation further, and thus, resulting some additional oxygens drift to the Ti scavenger layer. Henceforth, a single or few negative pulses (during depression scheme, Fig. 6(b)(ii)) are enough to ionize most of the pre-existing and additional oxygens in the Ti layer to rupture the filament resulting large gap between the top interface and the apex of the remnant filament. The reverse process occurs in potentiation (Fig. 6(b)(iii)), a high injection of electrons with a single or few positive pulses can spontaneously rejuvenate the filament by re-ionizing the oxygens and repulsing them back to the Ti scavenger layer. The rupture and rejuvenation of the filament happen instantaneously (inset of Figs. 1(c) and 2(b)), and these processes result in large dynamic ranges (inset of Fig. 1(c) and Fig. 2(d)), which demonstrates digital characteristics.

The potentiation and depression curves of D25CC2 device (inset of Fig. 2(a)) are steeper than that of the D16CC2 device (inset of Fig 1(d)), we assume this is due to the pristine resistance of the two devices is different (owing to the thickness effect) and, hence, the electroforming results in different filament dimension. As observed in the electron conduction analysis (Fig. 4(a) and (b)) of the slope of D25CC2 device in low voltage region is closer to the ideal ohmic relationship than that of D16CC2, this could be due to a wider filament was exist at the TiO₂/TiN bottom interface of D25CC2. Thus, the electron injection into D25CC2 is slightly easier and makes the synaptic weight change is more responsive (nonlinear) to the electrical pulse stimulus.

Consequently, the employment of a pulse amplitude with a lower voltage (Fig. 3) for the synaptic operation helps to enhance the linearity of the potentiation and depression curves.

Analog and digital memristors have different circuit functionalities due to their distinct electrical characteristics (operational speed, current level, voltage range, etc.). For example, digital memristors could be exploited for making content addressable memory, reconfigurable logic circuits and operations, digital gates, etc.; on the other hand, analog memristors could enable neuromorphic network, chaos circuit, variable gain amplifier, difference comparator, oscillator, etc.³¹ Henceforth, the realization of convertible digital-analog memristor could open broad opportunities in electronics, such as enabling simultaneously tunable and bypass-able filters,³² the design and implementation of mixed-signal circuits utilizing the same device technology. This technology could also allow for the implementation of a customizable balance between high-speed operation in the digital low resistive state and low power operation in the digital high resistive state.³³

In conclusion, the maximum operating current level determines the synaptic response of memristor devices. The devices that operate at high operating current exhibit digital behavior; conversely, the device exhibits analog when it operates at low operating current. The employment of high current compliance encourages the formation of a complete filament conduction channel that connects cathode and anode, and thus, the high electric field induces the movement of a high number of defects promoting instantaneous redox reaction during synaptic operations. On the other hand, a low operating current level results in the formation of filamentary-homogeneous configuration and induces analog behavior where each pulse stimulus can only ionize a small number of oxygens during depression and potentiation, which occur in the homogenous region. This study not only provides an insight to produce an analogous

synaptic response of memristor devices but also offer a technique to realize convertible digital-analog memristors that could open broad capabilities in electronic circuit and system.

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DATA AVAILABILITY

The data that support the findings of this study are available from corresponding author upon reasonable request.

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FIGURE CAPTIONS

Figure 1. (a) Cross-sectional TEM images of TiN/Ti/TiO₂/TiN device stack. (b) Schematic of the TiN/Ti/TiO₂/TiN device structure and electrical measurement setup. The typical I-V curves of D16 device employing current compliance (CC) of (c) 10 and (d) 2 mA. Insets in (c) and (d) show the synaptic response of the device. (e) Epoch endurance of the device after a SET process employing CC of 2 mA.

Figure 2. (a) Typical I-V curves of D25 device employing CC of (a) 2 and (b) 10 mA. Insets in (a) and (b) show the synaptic response of the device. Epoch endurance of the device after a SET process employing CC of (c) 2 and (d) 10 mA.

Figure 3. Examples of optimization of synaptic linearity by varying the pulse amplitudes. P and D values represent the amplitude used for potentiation and depression.

Figure 4. Log-log scale of LRS curves of (a) D16 and (b) D25 devices. Schematic of the band diagram of TiN/Ti/TiO₂/TiN in (c) equilibrium state (d) Ohmic, and (e) Frenkel-Poole conduction; the work function of TiN and Ti, and the electron affinity of TiO₂ were taken from the literature.^{26–28}

Figure 5. (a) Depth-XPS profile of TiN/Ti/TiO₂(25 nm)/TiN stack and (b) O1s core level spectra of TiO₂ at various depths. Note that the concentration of oxygen in the TiN layers as shown in

295 (a) may higher than the actual due to the surface oxidation of the sample and depth-profiling
296 knock-on effect.

297 **Figure 6.** Schematic of conduction mechanism in the device that was programmed with (a) low
298 and (b) high current compliance.

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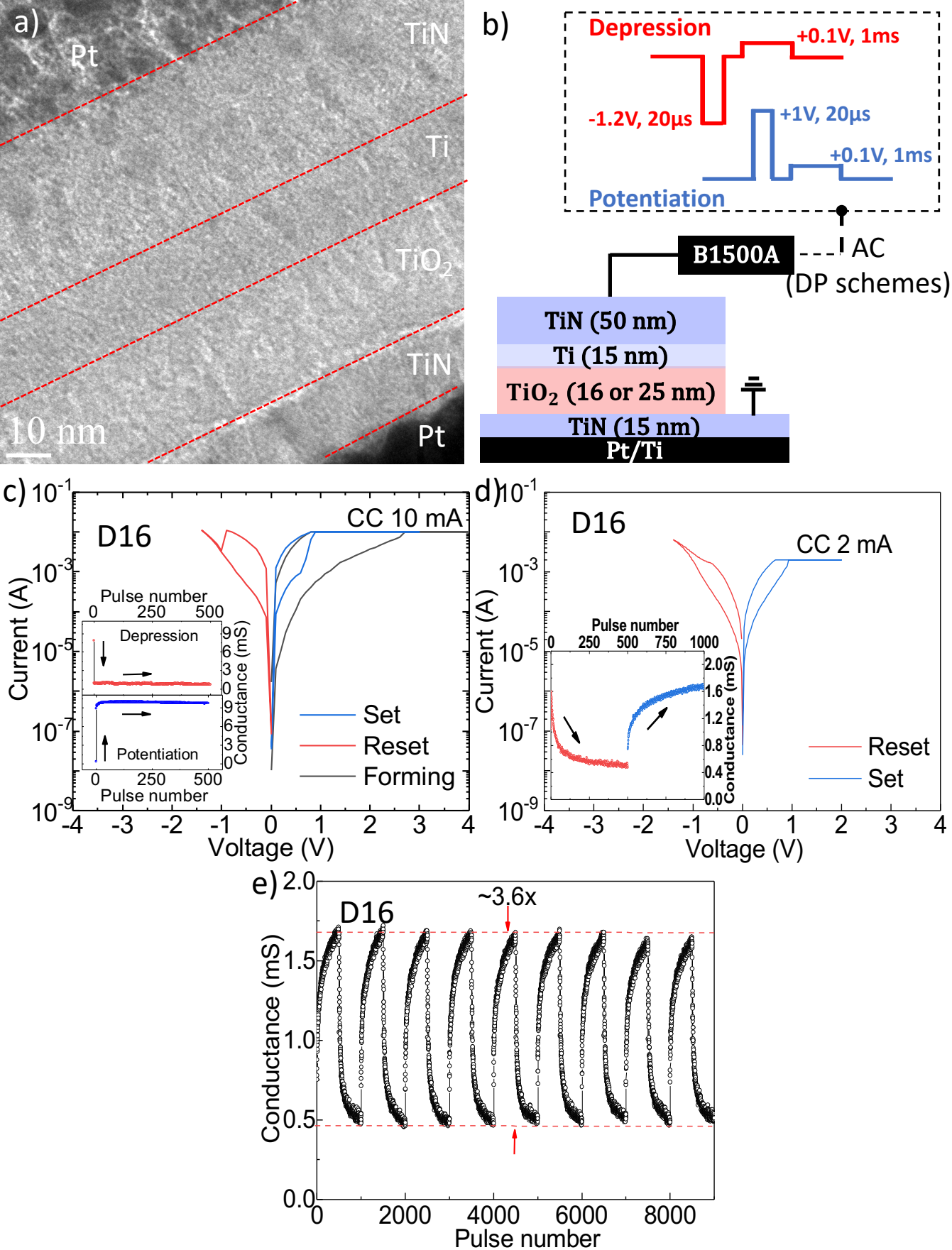


Fig. 1 Simanjuntak et al.

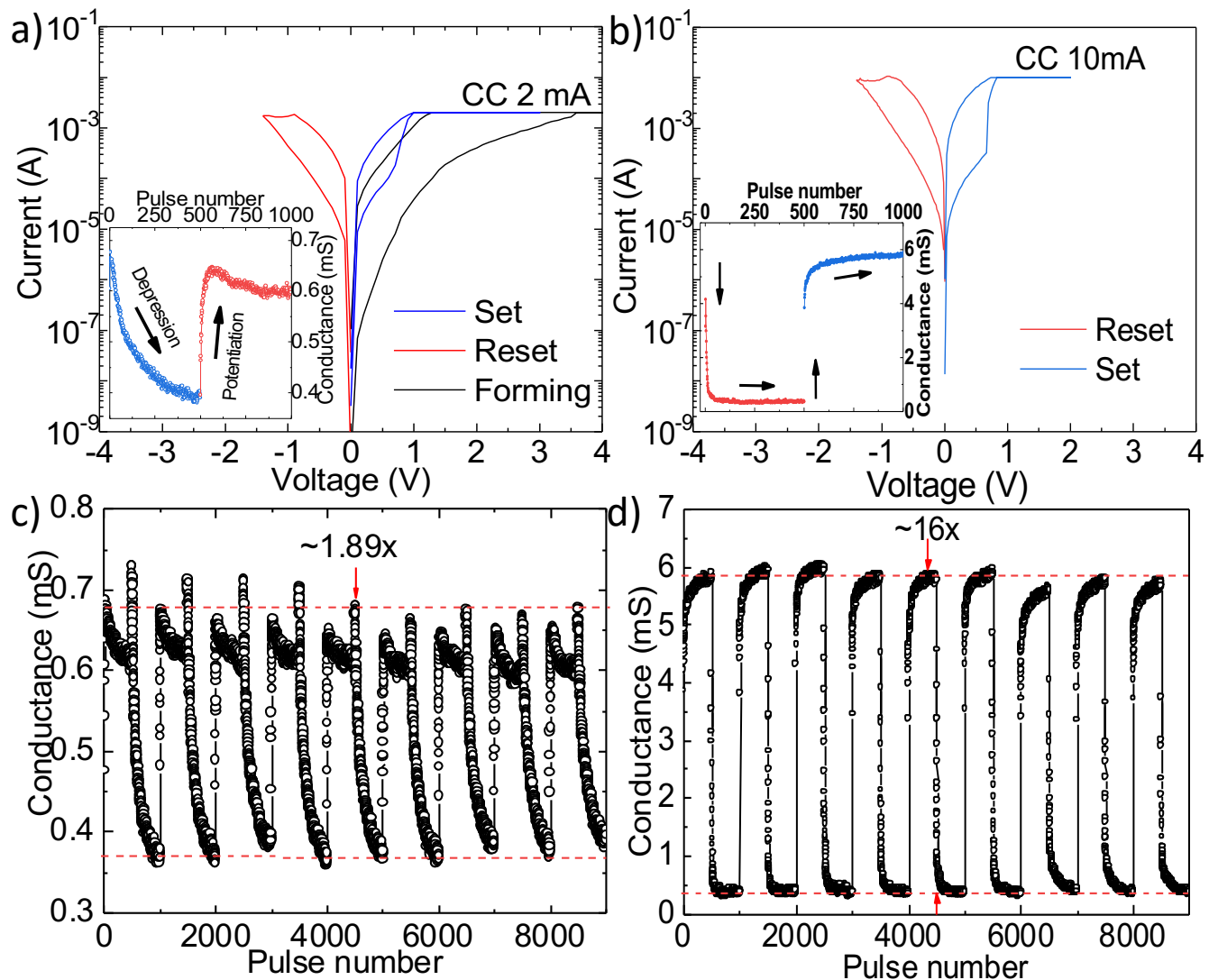


Fig. 2 Simanjuntak et al.

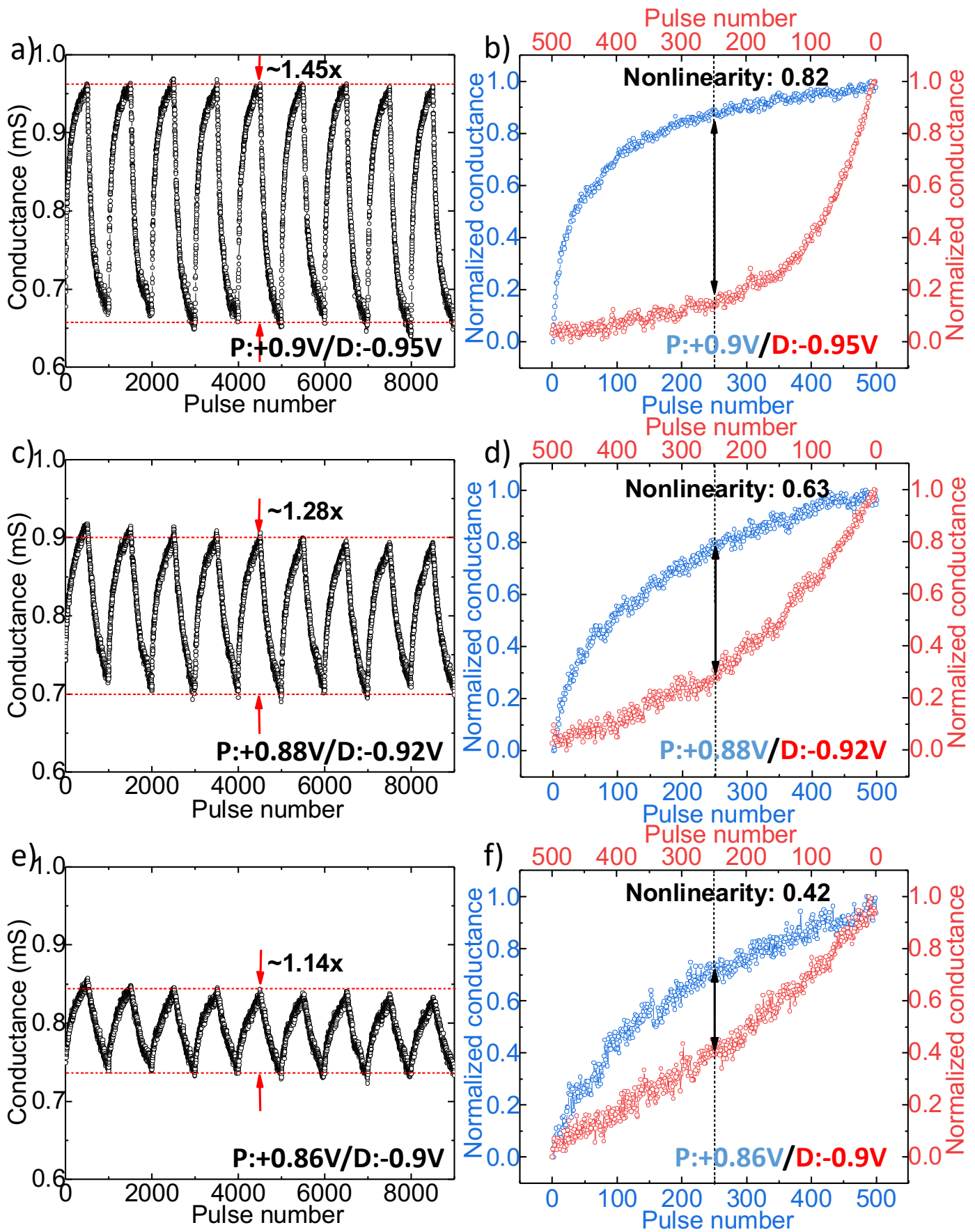
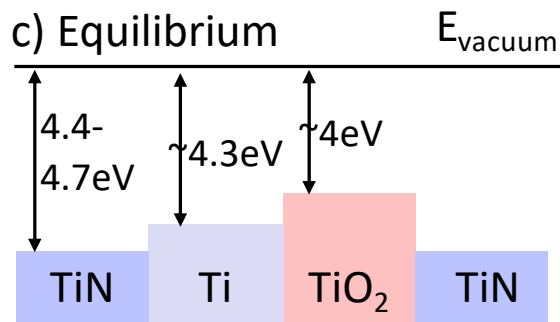
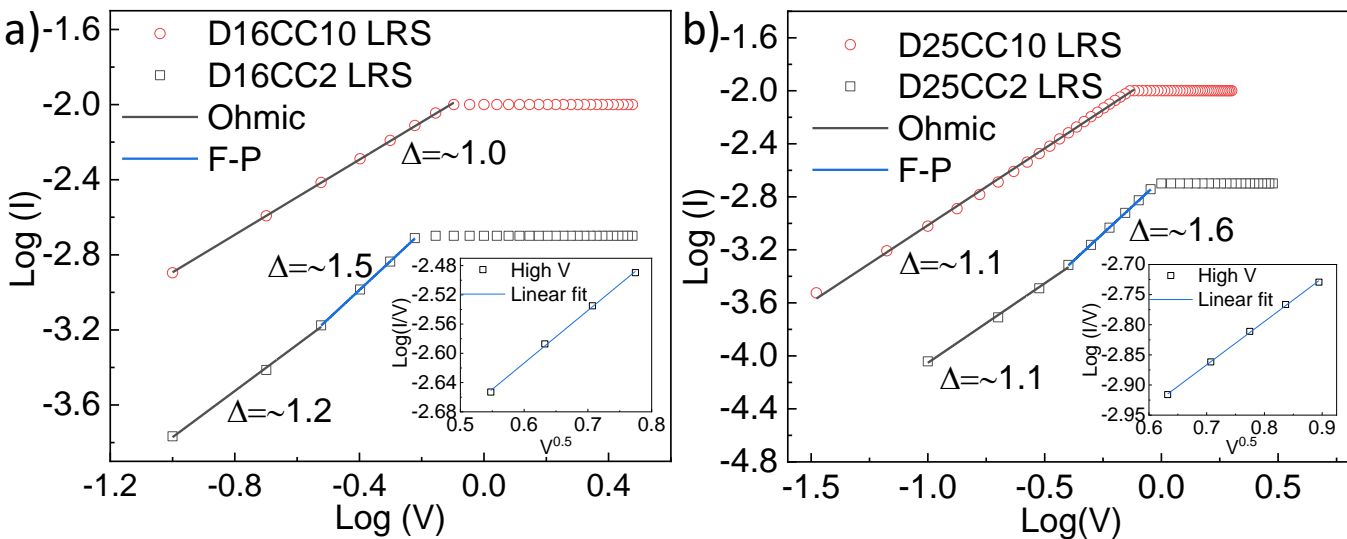
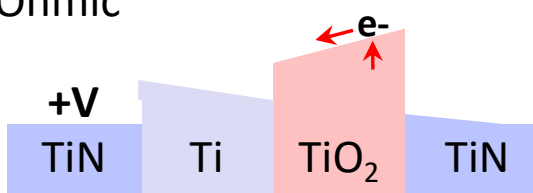


Fig. 3 Simanjuntak et al.



d) Ohmic



e) Frenkel-Poole

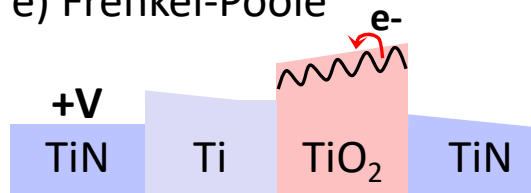


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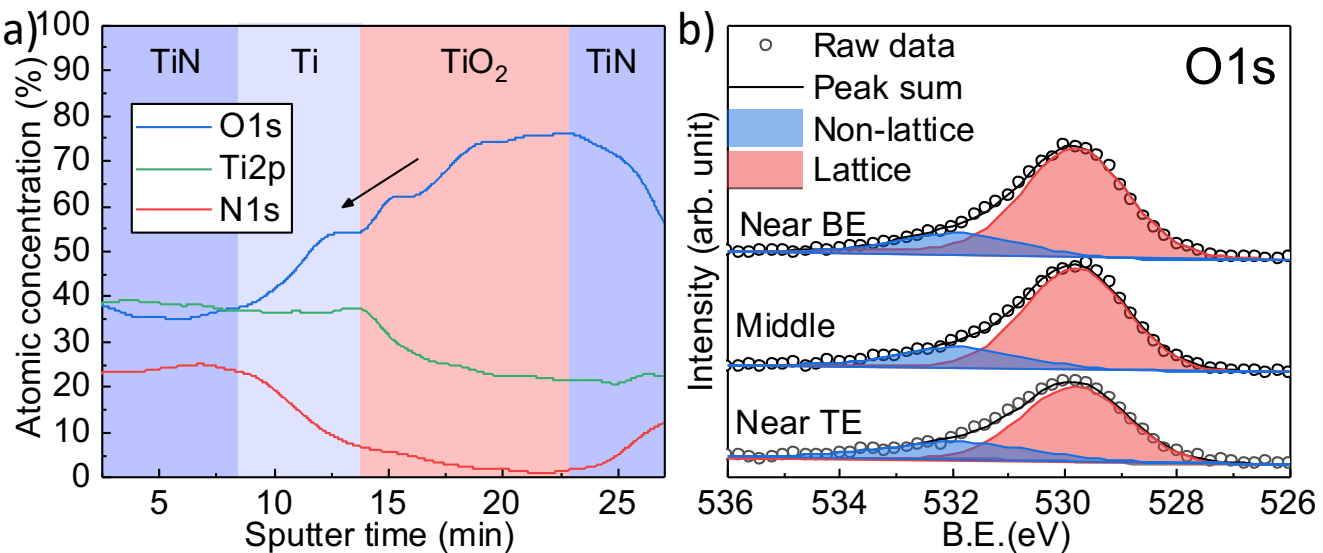


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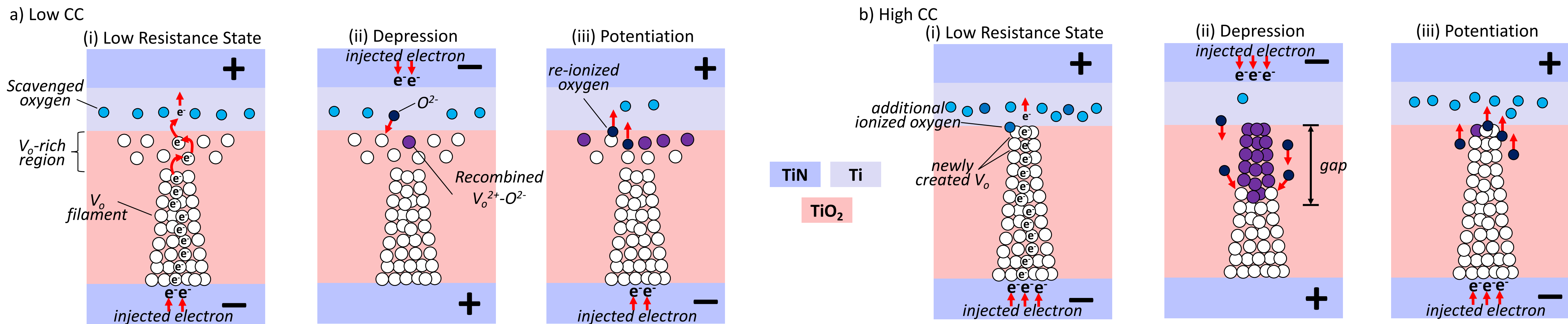


Fig. 6 Simanjuntak et al.