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Abstract. In this work, we experimentally investigate the impact of electrical stress on the tunability of single hole transport properties within a p-type silicon MOSFET at a temperature of T = 2 K. This is achieved by monitoring Coulomb-blockade from three disorder based quantum dots at the channel-oxide interface, which are known to lack tunability as a result of their stochastic origin. Our findings indicate that when applying gate biases between -4 V to -4.6 V, nearby charge trapping enhances Coulomb-blockade leading to a stronger quantum dot confinement that can be reversed to the initial device condition after performing a thermal cycle reset. Re-applying stress then gives rise to a predictable response from reproducible changes in the quantum dot charging characteristics with consistent charging energy increases of up to $\approx 50\%$ being observed. We reach a threshold above gate biases of -4.6 V, where the performance and stability become reduced due to device degradation occurring as a product of large-scale trap generation. The results not only suggest stress as an effective technique to enhance and reset charging properties but also offer insight on how standard industrial silicon devices can be harnessed for single charge transport applications.

1. Introduction

The ability to form quantum dots (QDs) through the fabrication of dedicated multi-gate devices as well as single impurity based structures has led numerous breakthroughs in quantum transport and quantum information processing schemes through manipulating individual charges [1, 2, 3, 4, 5, 6]. Various single electron and hole device architectures were designed and developed over the years, from single hole transistors (SHTs) and single carrier pumps, to charge sensors and quantum bits [7, 8, 9, 10, 11, 12, 13]. Ultimately, technological impact as a result of such endeavours can only become a reality if the physical components can be manufactured on a large-scale, which are reproducible and have guaranteed stability.

To promote better integration with classical control hardware, attempts are being made to develop functioning single charge devices using industry standard fabrication processes, which have the clear advantage of utilizing well established silicon (Si) fabrication technology and promote very large-scale integration (VLSI) [14, 15]. Recently, MOSFETs have gained attention within the field of quantum information technology owing to the need for closer system integration of cryogenic circuits and large-scale quantum computers [16, 17]. This approach has many advantages including reducing wiring complexity by simplifying interconnects, improving signal-noise ratio and low power consumption with sufficiently high power output [18]. Building on this, a common mechanism used throughout quantum information processing known as Coulomb-blockade (CB) also occurs within industry grade Si MOSFETs at low temperatures as a consequence of disorder based QDs [19, 20]. CB is an electrostatic phenomenon whereby single carrier tunnelling is prohibited, which is advantageous for not only controlling discrete charges but also enables information on the dimensions and charging parameters of a QD system to be determined [21]. As such, MOSFETs provide an excellent test platform to explore single charge interactions. However, QDs originating from defects present in MOSFETs suffer from the inability to control aspects such as carrier number, size and coupling which are largely fixed by the poly-Si grains and interface defects that produce them [22, 23, 24, 25]. Despite this, successful attempts at mitigating the random nature by tuning disorder QDs for quantum information processing and memory purposes have been carried out, as well as taking advantage of the inherent randomness by demonstrating that the unique charging properties can be of use as a physically unclonable function (PUF) [26, 27, 28].

On the other hand, if the origin and behaviour of defect based QDs were better understood, this would show a path towards controlling single charging characteristics through manipulating the disorder, with the possibility of tuning MOSFET QDs. This would satisfy the need for an efficient and scalable device capable of SHT operation using a VLSI platform. The most significant challenge in this regard is that of device variability owing to random and uncontrollable charges in the vicinity of the QD, which are the leading causes of unpredictable behaviour. This has meant exploring methods to improve the consistency and tunability of features that are essential to SHT function, such as charging energy (E_c), capacitive couplings and activation energy (E_a) [29]. One method is through the application of electrical stress in the form of a large gate bias. Applying this technique draws parallels from the significant effort put forward historically into oxide reliability when down-scaling transistors in search of better performance, together with the development of resistive memory, where state switching is initiated as a consequence of voltage driven structural change within the

oxide [30, 31].

In this study, we intentionally induce stress within a Si MOSFET by systematically applying high gate biases and investigate the beneficial changes to quantum transport via E_c and E_a through monitoring CB. In addition, we quantitatively analyse the resulting threshold voltage (V_{th}) shift and gate leakage to assess the effect on conventional MOSFET operation as well as to identify a threshold of stability upon which further stress compromises performance. Our work is comprised of three sections, with section 2 outlining the device specification and stress procedure, followed by the results in section 3 which details the stress-induced changes to the E_c and E_a. We end with a discussion in section 4, comparing and summarizing our findings together with an explanation of how our proposed method is beneficial for future quantum technologies when utilizing disorder based QDs.

2. Device and stress methodology

The necessary high-resolution current-voltage (I-V) characterisations were acquired by utilising a B1500 semiconductor analyser through biasing the gate (V_g) and source (V_{SD}) terminals whilst measuring the gate leakage (I_g) and drain current (I_d). The experimental procedure for measurement and application of stress was conducted at a temperature of 2 K, via wire bonding and mounting the sample into a Cryogenic cryogen-free cryostat. The device under investigation is a p-type Si MOSFET fabricated by standard 65 nm-node technology with a gate length of 60 nm and width of 10 μm. The gate and oxide materials are composed of highly doped poly-Si and Si-oxynitride respectively, with an equivalent oxide thickness of 2.4 nm. A channel length of 60 nm was chosen, as it is reported that distances of less than 80 nm are required for single carrier tunnelling [32]. A schematic of the device is given in Figure 1(a) with the associated terminals for voltage/current measurements. These terminals control the transport of individual charges via QDs in the channel acting as a capacitor that is coupled to each of the three terminals, depending on the gate and source/drain voltage conditions V_g and V_{SD}. The circuit model describing this situation can be seen in Figure 1(b).

Electrical stress is performed by applying a double gate sweep, from 0 V to a maximum gate voltage for given sweep ($V_{g,max}$), and then back to 0 V while recording I_g. The stressing procedure commenced at an initial value of $V_{g,max}$ = -4 V up to a maximum $V_{g,max}$ = -5.6 V through -200 mV increments. The effect of such large V_g biases on quantum transport was monitored via Coulomb-diamonds (CDs) by generating a charge stability diagram (CSD) before and after applying stress. CDs are a key measurement tool to visualize the charging and transport properties of QDs, which appear in I-V characteristics as a result of CB in the sub-threshold region. During this regime, tunnelling is blocked due to the electrostatic charging energy of the occupying holes.

For the MOSFET device under investigation, this transport scheme is realised as the channel becomes inverted and a 2-dimensional hole-gas (2DHG) begins to form. Structural randomness then leads to additional confinement via valance-band bending along the lateral directions of the channel 2DHG, generating island-like structures (QDs) as a product of quantum confinement due to their size [33]. Single carrier transport is then observed as a result of discrete charging from levels within the altered potential profile. Consequently, applying sufficient gate voltage leads to non-uniformity across the channel because of the modified threshold for inversion at these

small regions, since holes are able tunnel through the defect originated levels, whereas tunnelling barriers exist on either side. In our device, the structural randomness is suspected to originate from disorder-based defects such as Si dangling bonds or poly-Si grains, as depicted in Figure 1(c). Single hole transport as a product of these defects is confirmed in Figure 1(d) for low V_{SD} by the presence of Coulomb oscillations (current peaks) and CB.

The first gate sweep stress measurement, $V_{\mathrm{g,max}} = $ -4 V, is displayed in Figure 2(a) with the total gate leakage I_{g} (black), and the carriers separated into electrons (blue) and holes (red). Separating the leakage current into the corresponding carriers is important to document trapping and oxide breakdown mechanisms which can be carrier specific. As observed in Figure 2(a) I_{g} is predominantly composed of hole tunnelling at the onset of stress from the n-Si well to the p+ poly-Si gate (I_{g} - I_{sub}). However when $|V_{\mathrm{g}}| > 1.5$ V electrons (I_{sub}) begin to tunnel directly from the p+ poly Si valence band to the n- well conduction band. The magnitude of V_{g} bias applied is sufficient to induce electron and hole traps in combination with interface states, which can lead to non-trivial effects to QD charging characteristics and therefore heavily influences changes to the interface disorder. Because of these processes, stress has been widely reported to trap both holes and electrons within the oxide together with the generation of interface states as illustrated in Figure 2(b) [34, 35]. The origin of stress-induced leakage current and charge trapping can be attributed to carrier specific tunnelling across the oxide through mechanisms such as anode hole injection (AHI) [36, 37, 38]. During AHI, biases above $|V_{\mathrm{g}}| \approx 3.5$ V are able to generate sufficiently high fields for electrons to be injected into the n-Si well [39]. Here, the energy is transferred to an electron deep in the valence band, creating a hot hole [40, 37, 41]. These hot holes then tunnel back through the oxide and induce trap generation at the interface and create weak points in the oxide layer, as shown in Figure 2(b).

3. Results

Figure 3(a)-(c) displays CSDs with identical V_{SD} and V_{g} parameters where each subplot in a given row only differs in the amount of stress applied prior to measurement. An initial CSD was taken before stress, and then immediately after $V_{\mathrm{g,max}} = $ -4 V, -4.2 V, -4.4 V and -4.6 V in Figure 3(i)-(v) for each column respectively. A $V_{\mathrm{g,max}}$ value of -4 V was chosen in particular to identify any differences which emerge from the onset of trapping at the interface due to AHI. The resulting CB patterns are a product of three distinct QDs, whereby the CD dimensions along V_{SD} are proportional to the charging energy. In Figure 3(a)(i)-(v) QD_1, QD_2 and QD_3 are highlighted by the white, pink and black regions to track the progressive change from $V_{\mathrm{g,max}} = $ -4 V to -4.6 V. Between Figure 3(a)(v)- (b)(i), as well as (b)(v)-(c)(i), the device underwent a thermal cycle, from 2 K to 295 K and then back to 2 K, as a way to determine the permanency of the stress related changes and to gain further evidence on the mechanism. Repeat stress measurements in Figure 3(b) and (c) also allow the stability and reproducibility of the CD structure to be assessed, serving as a comparison to Figure 3 (a). After applying $V_{\mathrm{g,max}}$ of -4 V, the same significant increase in charging energy of QD_1 is observed with a moderate increase for QD_2, however a less consistent change in the charging properties of QD_3 as $V_{\mathrm{g,max}}$ increased can be noted. The most striking feature is the similarity of the regions outlined in Figure 3(a)(i)-(v) when compared to (b)(i)-(v) and (c)(i)-(v) evidencing that the variation caused by stress is temporary, and there exists not only a reversible trend

but also a consistent response due to stress. The initial states in Figure 3(b) and (c) clearly show an almost identical CDs pattern when compared to (a). This provides further support on the relationship between stress and QD changes when analysing the CDs after the 1st and 2nd thermal cycles where the CB pattern reverted to the initial device condition. QD_1 most notably matches the enhanced features after stress, with QD_2 appearing moderately more confined but less consistent, and as before an unpredictable relationship between stress-induced changes and the charging properties of QD_3.

Further CSDs were generated at elevated $V_{g,max}$ values of -4.8 V to -5.2 V (Figure 4(a)(i)-(iii)). The effect of applying biases greater than $V_{g,max}$ = -4.6 V clearly demonstrates device degradation. This is evident from the manifestation of CD features gradually appearing smaller, fewer in number, and unstable when moving from (i)-(iii) in Figure 4(a). To highlight the impact of stress-induced traps on QD stability, I_d - V_g sweeps were taken after $V_{g,max}$ = 5.2 V and plotted (Figure 4(b)) where significant random telegraph signal (RTS) appeared in I_d [42]. Large discrete switching events between high and low states are plainly visible throughout the sweep, but appear most detrimental around V_g = -720 mV for low V_{SD}, owing to their magnitude relative to the Coulomb oscillation peak. Here, the high/low signals refer to an occupied or unoccupied trap due to a single charge, where each state results in a V_{th} shift from a modified electric field in the channel and therefore leads to a sudden change in I_d [43, 44, 45, 46]. This suggests that breakdown mechanisms within the oxide and at the channel-oxide interface are beginning to greatly hinder device stability.

Greater insight on stress-induced changes can be unveiled through calculating V_{th} shift, an important parameter for characterising global transport changes across the MOSFET channel as an outcome of trapped oxide charge. Since V_{th} shift is a clear indicator that charge is becoming trapped within the oxide, or at the interface, it represents capacitive changes experienced across the whole channel in response to oxide breakdown. Here, we defined the V_{th} as the gate bias at which I_d becomes greater than 1 nA . Therefore a negative V_{th} shift corresponds to an increase in negative gate bias in order to invert the channel and compensate for trapped positive charge [47]. Based on this, V_{th} shift was calculated after every $V_{g,max}$ sweep. In Figure 4(c) a -160 mV V_{th} shift is attained when comparing the initial I_d and after applying $V_{g,max}$ = -5.6 V. This is consistent with the injection of holes into the oxide layer leading to a negative shift in V_{th}. A very similar trend is observed in Figure 4(d) for the charge fluence (Q_f) through the oxide, which is calculated via equation (1) [48]:

$$Q_f = A \int_0^t I_g(t) dt \tag{1}$$

where A is the channel surface area, I_g is the leakage current of each respective carrier and t the total measurement time for a given sweep. Focusing on the increase in carrier tunnelling across the oxide in Figure 4(d), it is worth noting that between $V_{g,max}$ = -4 V to -4.6 V, Q_f rises from 25 to 81 cm^{-2} for holes and 50 to 179 cm^{-2} for electrons. This is in contrast to an increase by more than an order of magnitude between $V_{g,max}$ = -4.6 V to -5.6 V, whereby the values rise to 927 C cm^{-2} and 1916 C cm^{-2} for holes and electrons respectively within the unstable region.

Another key attribute of QDs is the barrier height, otherwise known as E_a, which can be utilized to study any stress-induced changes to the system. E_a can be calculated by measuring the temperature dependence of I_d during the Coulomb oscillation peaks

between CDs. The I_d temperature dependence is displayed in Figure. 5(a)(i) and (a)(ii), where I_d-V_g plots over a temperature range of 10-40 K are displayed for the initial state and after $V_{g,max}$ = -4 V respectively. Evidently, increases in temperature are met with elevated I_d, in addition to the Coulomb oscillation peaks for each QD (labelled) becoming less defined and shifting to lower V_g values. This is consistent with the thermal emission of holes within the QDs. Comparing Figure 5(a)(i) and (a)(ii), the most significant change after stress, mirroring the CSDs in Figure 3, is the drop in I_d due to the CD expansion for QD_1. Using the peak I_d oscillation for each QD level at a given temperature, E_a can be approximated according to the well known Arrhenius model via the equation [49]:

$$I_d = I_{d0} e^{\frac{-E_a}{kT}} \tag{2}$$

where I_{d0}, k, and T are the initial drain current as the temperature approaches 0 K, the Boltzmann constant and temperature respectively. Arrhenius plots based on this model are shown in Figure 5(b)(i) -(vi) where E_a is estimated via the gradient during the thermal emission regime as indicated. Figure 5(b)(i)-(iii) display plots for extracting E_a of the initial state for QD_1, QD_2 and QD_3. Figure 5(b)(iv)-(vi) depict the same plots after $V_{g,max}$ = -4 V which yield increases of 0.5 meV for QD_1 and 0.4 meV for QD_2, while a modest increase of 0.1 meV is observed for QD_3.

To summarize the key differences as a result of stress, E_a, E_c and lever arm (α) of the three QDs after each stress voltage were determined. This is achieved using Figure 3(a)(i)-(v) with equations $E_c = \frac{e}{C_\Sigma}$ and $\alpha = \frac{V_{SD}}{V_g}$ together with Figure 5(a)(i)-(ii) and equation (2). These parameters for each QD during the initial state and after $V_{g,max}$ = -4 to -4.6 V are displayed in Table 1 above. In addition, we also approximated the initial QD diameter (d_{QD}) given the QD surface area (S_{QD}) and effective oxide thickness (t_{eff}) by $d_{QD} = \sqrt{4S_{QD}/\pi}$, using $S_{QD} = C_g/C_{eff}$ and $C_{eff} = \epsilon_{ox}/t_{eff}$, where ϵ_{ox} is the permittivity of the oxide. This yields a d_{QD} of 28 nm, 46 nm and 31 nm for QD_1, QD_2 and QD_3 respectively.

4. Discussion

In Table 1 the α values obtained serve as a strong indicator that each of the CDs tracked after applying stress are indeed from the same three distinct QDs. Considering that α reflects the ratio of QD couplings (from CD dimensions), a higher value such as 0.8 for QD_1 suggests a strong coupling and in close proximity to the gate, whereas a lower value of 0.3 implies QD_3 is located further away from the interface. Based on this, we propose the origin of QD_1 to be a Si dangling bond at the oxide-interface, given the high α value as well as an E_c close to 13 meV above the valence band, which is agreeable for this type of trap site [50]. QD_2 and QD_3 on the other hand are presumed to be generated by disorder of a different nature, for example, poly-Si grains, where small non-uniformities in the gate are small enough to create confined levels for single carrier transport. QD_1 initially had a larger E_c of 12.5 meV in Figure 3(a)(i), which then gradually increased to 19.3 meV in (a)(v), a rise of more than 50%. This overall pattern is matched for QD_2, although its E_c decreased after applying $V_{g,max}$ = -4.2 V, from 2.5 meV in Figure 3(a)(i) to 2.0 meV in (a)(iii), before finally reaching an enhanced 4 meV in (a)(v). For QD_3 however this tendency of an increasing E_c for larger a $V_{g,max}$ is not observed. The first -4 V stress sweep resulted in a 30% enlargement in E_c, but despite this, after the application of stress for all other values

Table 1. Summary of single hole transport properties of QD_{1-3} when subjected to electrical stress.

No.	$V_{g,max}(V)$	E_a (meV)	E_c(meV)	α
QD_1	Initial	4.2	12.5	0.7
	-4	4.7	13.8	0.7
	-4.2	4.7	16.8	0.8
	-4.4	4.9	15.0	0.7
	-4.6	4.4	19.3	0.8
QD_2	Initial	3.8	2.5	0.4
	-4	4.2	3.8	0.4
	-4.2	4.4	2.0	0.4
	-4.4	4.5	4.0	0.5
	-4.6	3.9	4.0	0.5
QD_3	Initial	2.8	5.5	0.3
	-4	2.9	7.3	0.4
	-4.2	3.1	5.5	0.4
	-4.4	3.3	3.5	0.3
	-4.6	2.4	5.5	0.4

from -4.2 V to -4.6 V the outcome was either a reduction to the initial E_c or less. Our findings suggest that QD_1 yielded the greatest stress response from the largest increases in E_c by magnitude, although QD_2 demonstrated a similar response relative to it's CD dimensions.

The enhanced charging properties can be explained by changes to the oxide integrity in combination with the likely QD origin. If single hole transport is a product of dangling bonds or poly-Si grains at the oxide interface, charge traps are more likely to form close to these sites as a consequence of weaker oxide performance. As a natural outcome, stress-induced trapping would then lead to a build up of charge at the interface close to regions harbouring the defects, resulting in the narrowing of the potential profile and hence stronger confinement. Aside from anomalous trapping which can produce matching responses, a model to explain the similarity between QD_1 and QD_2 may be related to the larger size of QD_2 (46 nm), when compared to QD_1 (28 nm). The reasoning is that a smaller α value of QD_2, and therefore weaker interaction with the interface charge, may be compensated for by the greater QD surface area exposed to oxide trapping. QD_3 on the other hand not only exhibited less predictable changes but also possessed the weakest interface coupling in combination with a smaller size of 31 nm.

Comparisons between the impact of stress and E_a from Table 1 yield the same tendencies for all QDs. A systematic trend is ascertained from an enlargement in E_a after $V_{g,max}$ = -4 V, which differed in magnitude and then revealed the same tendency of a sudden decrease at $V_{g,max}$ = -4.6 V, close to or below the initial value. In fact, when $|V_{g,max}| > 4.6$ V, a transformation in the behaviour is expected to take place in order to reflect the precipice of significant oxide degradation. At higher $V_{g,max}$ values the sheer magnitude of charge trapping within the oxide cannot be efficiently removed and therefore leads to the instabilities as displayed in Figure 4 (a) and (b). A rising V_{th} shift in Figure 4(c), accompanied by an escalating Q_f through the oxide in Figure 4(d) is to be expected due to AHI, as described in section 2. This may also explain the possible reason behind the drop in E_a at $V_{g,max}$ = -4.6 V, since the

potential barrier height between the QD and source/drain may well become reduced from many trapped oxide charges. Furthermore, the AHI model offers a solution to the polarity of carrier trapping, where positive charge associated with trapped holes and interface states collectively dominate the negative charge and therefore result in a negative threshold shift (Figure 4(c)) [51]. This can be explained by electron trapping at defect sites being far less efficient even though the electron fluence is significantly higher than the hole fluence [52, 53]. Interface states however have been found to remain for considerable periods of time, with their effect being the most dominant on QD charging properties within the $V_{\mathrm{g,max}}$ = -4 V to -4.6 V region due to the absence of V_{th} shift. Subsequently, the variation experienced by single hole transport is considerably more dependant on local anomalies in contrast to changes in E_{a}, that are associated with differences in barrier height on either side of a QD. As such, any correlation reflects both large-scale changes to the valance band across the channel and at the QD site. For example, the introduction of a single trap state in the near vicinity of a QD would alter the interface disorder and therefore modify the capacitive coupling, which then leads to differing CD charging properties. A scenario such as this is largely independent of any global stress-induced trends across the channel as a product of large-scale trapping within the oxide.

The repeatability of the CD pattern when subjected to stress in Figures 3(a)-(c) also reinforces that the induced changes are predictable and controllable to an extent. The significance of observing similar responses for all three QDs after stress and reset cycles is not a trivial matter, considering that the physical nature behind the changes is a consequence of stochastic phenomena and hence should lead to a plethora of varied charging characteristics. For example, the CSDs obtained in Figure 3 are a result of three QDs which vary in location and size. Accordingly, the response due to stress will likely always display some variation, depending upon the sensitivity and proximity of the defect level to both the differences at the interface and within the oxide. Therefore we can only claim that the stress-induced trapping is consistent (at the same sites) for a given device in order to produce the matching CD response. The reasoning as to why this happened is suggested to be a product of charges becoming trapped at the same preferential sites due to unique structural non-uniformities at the oxide-interface. These include poly-Si grain edges within the oxide, or close to the oxide-interface near Si dangling bonds, which would lead to a repeatable effect for a given device. This almost fully resettable nature back to the initial state in Figures 3(a)(i), (b)(i) and (c)(i) therefore highlights a complete annihilation of the stress-induced interface states by relaxation at elevated temperatures, which we also confirmed in another, similar, device.

Our stress technique offers a path towards tuning charging characteristics in a controllable and reversible way that enables Si MOSFETs to perform as optimized QD devices. For example, because stress introduces temporary interface traps it can aid in offsetting the parasitic background charges of SHTs that produce unwanted device variability. Furthermore, increasing E_{c} is advantageous for optimizing SHT performance to aid in reducing the gate leakage together with higher temperatures of stable operation. The large-scale changes due to stress also demonstrate that the CD pattern for a given device can be altered to such a degree that the pattern becomes unrecognisable when compared to the original state, which is then fully resettable to the initial condition. Our stressing method is therefore capable of introducing an appreciable difference to CB and E_{c}, which provides support for single charge memory applications from the formation of two distinct device states that can be

written, erased and re-written. In addition, when using the CD structure as a PUF for transistors, the variation induced by stress to CB should be considered when developing applications for device identification and security purposes.

5. Conclusion

We implemented electrical stress as a new method to selectively modify single hole transport characteristics in p-type MOSFETs. When applying stress up to $V_{g,max}$ = -4.6 V the charging energy tends to become enhanced, with reproducible changes following thermal cycles owing to stable device operation. These beneficial transitions in device characteristics are worth considering given the VLSI platform. A threshold is reached at further greater biases however, and a crossover occurs where the benefits are diminished from instability and poorer performance on account of large-scale oxide tunnelling and trap generation. We demonstrated consistent operation and propose the attributes outlined to be advantageous towards quantum transport applications such as SHTs and single charge memory devices.

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Data Availability Statement

The data that support the findings of this study are openly available in Southampton ePrint research repository at: https://doi.org/10.5258/SOTON/D1910.

References

[1] Unruh W 1995 *Phys. Rev. A* **51** 992
[2] Loss D and DiVincenzo D 1998 *Phys. Rev. A* **57** 120
[3] Likharev K K 1999 Single-electron devices and their applications *Proc. IEEE* vol 87 p 606
[4] Lu W, Ji Z, Pfeiffer L, West K and Rimberg A 2003 *Nature* **423** 422–425
[5] Takahashi Y, Ono Y, Fujiwara A and Inokawa H 2002 *J. Phys. Condens. Matter* **14**
[6] Laucht A, Hohls F, Ubbelohde N, Gonzalez-Zalba M F, Reilly D J, Stobbe S, Schröder T, Scarlino P, Koski J V, Dzurak A, Yang C H, Yoneda J, Kuemmeth F, Bluhm H, Pla J, Hill C, Salfi J, Oiwa A, Muhonen J T, Verhagen E, LaHaye M D, Kim H H, Tsen A W, Culcer D, Geresdi A, Mol J A, Mohan V, Jain P K and Baugh J 2021 *Nanotechnology* **32** 162003
[7] Kastner M A 1992 *Rev. Mod. Phys.* **64** 849
[8] Ishikuro H and Hiramoto T 1997 *Phys. Rev. Lett.* **71** 3691–3693
[9] Fujiwara A, Nishiguchi K and Ono Y 2008 *Appl. Phys. Lett* **92**
[10] Giblin S P, Wright S J, Fletcher J D, Kataoka M, Pepper M, Janssen T J B M, Ritchie D A, Nicoll C A, Anderson D and Jones G A C 2010 *New Journal of Physics* **12** 073013
[11] Morello A, Pla J J, Zwanenburg F A, Chan K W, Tan K Y, Huebl H, Möttönen M, Nugroho C D, CYang, Van-Donkelaar J A, Alves A D C, Jamieson D N, Escott C C, Hollenberg L C L, Clark R G and Dzurak A S 2010 *Nature* **467** 687
[12] Ladd T D, Jelezko F, Laflamme R, Nakamura Y, Monroe C and O'Brien J L 2010 *Nature.* **464** 45
[13] Morello A 2015 *Nanotechnology* **26** 502501
[14] Maurand R, Jehl X, Kotekar-Patil D, Corna A, Bohuslavskyi H, Laviéville R, Hutin L, Barraud S, Vinet M, Sanquer M and Franceschi S D 2016 *Nat. Comm.* **7** 13575
[15] Fogarty M A, Chan K W, Hansen B, Huang W, Tanttu T, Yang C H, Laucht A, Veldhorst M, Hudson F E, Itoh K M, Culcer D, Ladd T D and Dzurak A S 2018 *Nat. Comm.* **9**

[16] Patra B, Incandela R M, van Dijk J P G, Homulle H A R, Song L, Shahmohammadi M, Staszewski R B, Vladimirescu A, Babaie M, Sebastiano F and Charbon E 2018 *IEEE Journal of Solid-State Circuits* **53** 309–321

[17] Pauka S J, Das K, Kalra R, Moini A, Yang Y, Trainer M, Bousquet A, C Cantaloube N D, Gardner G C, Manfra M J and Reilly D J 2021 *Nat Electron* **4** 64–70

[18] Xue X, Patra B, van Dijk Jeroen P G, Samkharadze N, Subramanian S, Corna A, Paquelet Wuetz B, Jeon C, Sheikh F, Juarez-Hernandez E, Esparza Brando Perezand Rampurawala H, Carlton B, Ravikumar S, Nieva C, Kim S, Lee H J, Sammak A, Scappucci G, Veldhorst M, Sebastiano Fabio Babaie M, Pellerano S, Charbon E and Vandersypen L M K 2021 *Nature* **593** 205–210

[19] Branz H M and Silver M 1990 *Phys. Rev. B.* **42**

[20] Ono K, Giavaras G, Tanamoto T, Ohguro T, Hu X and Nori F 2017 *Phys. Rev. Lett.* **119** 156802

[21] Grabert H D M 1992 *Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures* (New York: NY: Springer US)

[22] Li J and Ma T P 1987 *J. App. Phys.* **62** 4212

[23] Saito S, Torii K, Shimamoto Y, Tsujikawa S, Hamamura H, Tonomura O, Mine T, Hisamoto D, Onai T, Yugami J, Hiratani M and Kimura S 2004 *Appl. Phys. Lett.* **84** 1395

[24] Li Z, Husain M K, Yoshimoto H, Tani K, Sasago Y, Hisamoto D, Fletcher J D, Kataoka M, Tsuchiya Y and Saito S 2017 *Semicond. Sci. Technol.* **32** 075001

[25] Li Z, Sotto M, Liu F, Husain M, Yoshimoto H, Sasago Y, Hisamoto D, Tomita I, Tsuchiya Y and Saito S 2018 *Sci. Rep.* **8** 250

[26] Hillier J, Ono K, Ibukuro K, Liu F, Li Z, Husain M K, Rutt H N, Tomita I, Tsuchiya Y, Ishibashi K and Saito S 2021 *Nanotechnology* **32** 260001

[27] Ibukuro K, Husain M K, Li Z, Hillier J, Liu F, Tomita I, Tsuchiya Y, Rutt H and Saito S 2019 *Front. Phys.* **7** 152

[28] Tanamoto T, Nishi Y and Ono K 2019 *Appl. Phys. Lett.* **115** 033504

[29] Lee S, Lee Y, Song E B and Hiramoto T 2013 *Appl. Phys. Lett.* **103**

[30] Yao J, Sun Z, Zhong L, Natelson D and Tour J M 2010 *Nano Letters* **10** 4105–4110 pMID: 20806916

[31] Buckwell M, Montesi L, Mehonic A, Reza O, Garnett L, Munde M, Hudziak S and Kenyon A J 2015 *physica status solidi c* **12** 211–217

[32] Ono K, Mori T and Moriyama S 2019 *Sci. Rep.* **9**

[33] Ono K, Tanamoto T and Ohguro T 2013 *App. Phys. Lett* **103** 183107

[34] Nissan-Cohen Y, Shappir J and Frohman-Bentchkowsky D 1986 *J. Appl. Phys.* **60**

[35] Liu W J, Liu Z Y, Huang D, Liao C C, L F Zhang and Z H Gan W W, Shen C and Li M F 2007 *IEDM Tech. Dig.* 813–816

[36] DiMaria D J and Stathis H J 2001 *J. App. Phys.* **89** 5015

[37] Chen I C, Holland S, Young K K, Chang C and Hu C 1986 *Appl. Phys. Lett.* **49** 669–671

[38] DiMaria D J, Cartier E and Buchanan D A 1996 *Appl. Phys. Lett.* **68** 304

[39] Nicollian P E, Krishnan A T, Chancellor C A, Khamankar R B, Chakravarthi S, Bowen C and Reddy V K 2007 *IEEE Rel. Phys.* pp 197–208

[40] Crook D L 1979 *Tech. Dig.*

[41] Schuegraf K F and Hu C 1994 *IEEE Trans. Elec. Dev*

[42] Martinez F, Leyris C, Neau G, Valenza M, Hoffmann A, Vincent J V E, Boeuf F, TSkotnicki, MBidaud, DBarge and BTavelc 2005 *Micro. Elec. Eng.* **80** 54–57

[43] Hung K K, Ko P, Hu C and Cheng Y C 1990 *IEEE Elec. Dev. Lett.* **11** 90–92

[44] Simoen E and Claeys C 2016 *Random Telegraph Signals in Semiconductor Devices* (Bristol: IOP Publishing)

[45] Liu F, Ibukuro K, Husain M K, Li Z, Hillier J, Tomita I, Tsuchiya Y, Rutt H and Saito S 2018 *Nanotechnology* **29** 475201

[46] Ibukuro K, Hillier J W, Liu F, Husain M K, Li Z, Tomita I, Tsuchiya Y, Rutt H N and Saito S 2020 *AIP Advances* **10** 055025

[47] Ortiz-Condea A, Sáncheza F G, Lioub J, Cerdeirac A, Estradac M and Yued Y 2002 *Microelectronics Reliability* **42** 583

[48] Verweij J and Klootwijk J 1996 *Microelectronics Journal* **27**

[49] Leroux M, Grandjean N, Beaumont B, Nataf G, Semond F, Massies J and P Gibart J 1999 *J. App. Phys.* **86**

[50] Spruijtenburg P C, Amitonov S V, Mueller F, van der Wiel W G and Zwanenburg F A 2016 *Sci. Rep.* **6** 38127

[51] T Hori a H I and Tsuji K 1988 *IEEE Trans. Elect. Dev.* **35**

[52] Lusky E, Shacham-Diamand Y, Bloom I and Eitan B 2002 *IEEE Elect. Dev. Lett.* **23**

[53] S Takagi N, Yasuda and Toriumi A 1996 326–326

[54] DiMaria D J and Pantelides S T (eds) 1978 *The Physics of SiO_2 and its Interfaces* 160-178 (Peragamon, New York)
[55] DiMaria D J and Cartier E 1995 *J. App. Phys.* **78**
[56] Bude J D, Weir B E and Silverman P J 1998 *Tech. Dig.* pp 179–182
[57] Degraeve R, Groseneken G, Bellens R, Ogier J L, Depas M, Roussel P J and Maes H E 1998 *IEEE. Trans. Elec. Dev* **45**
[58] Nicollian P E, Hunter W R and Hu J C 2000 *Proc. Rel. Phys.* pp 7–15

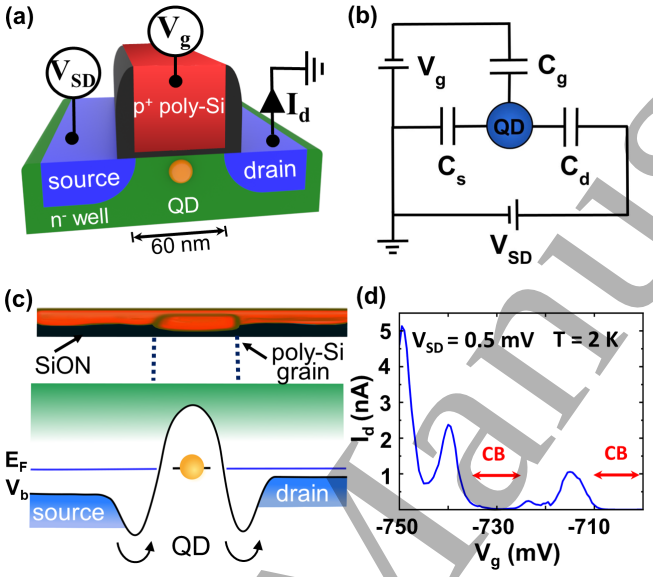

Figure 1. (a) A schematic of the p-type MOSFET with an illustration of a quantum dot in the channel. (b) A circuit diagram showing how a quantum dot in the channel is capacitively coupled to the gate (C_g), source (C_s) and drain (C_d). (c) A quantum dot can be created by silicon dangling bonds or poly-silicon grains (depicted) at the gate-oxide interface which results in valance band bending and quantized energy levels for single hole transport. (d) An I_d-V_g plot displaying Coulomb oscillations and Coulomb-blockade (CB) as a result of quantum dot formation in the channel at a temperature of T = 2 K.

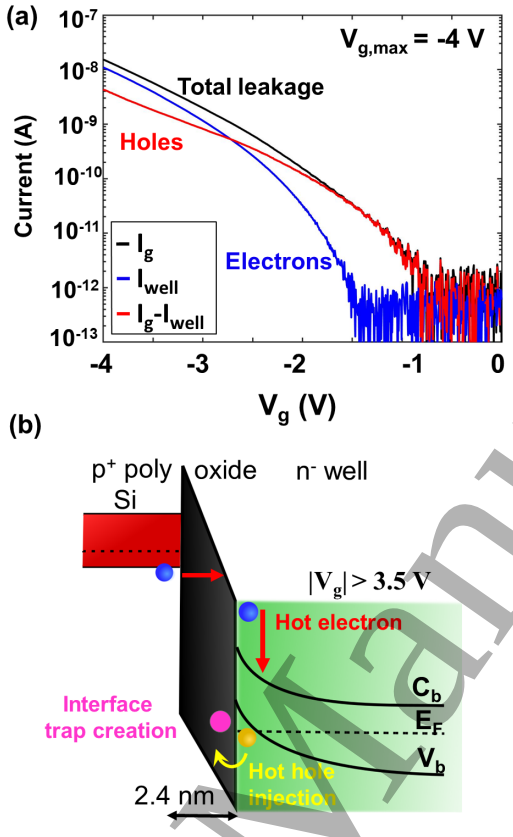

Figure 2. (a) I_g-V_g stress sweep for $V_{g,max}$ = -4 V. The total I_g (black) is separated into the respective carriers, with electrons tunnelling from the gate (blue) and holes from the channel (red). (b) A band diagram illustration displaying the leakage mechanisms as a result of anode hole injection (AHI) for $|V_g| > 3.5$ V, where hot electrons tunnelling across the oxide lead to the generation of hot holes, which are injected back into the oxide and create interface traps.

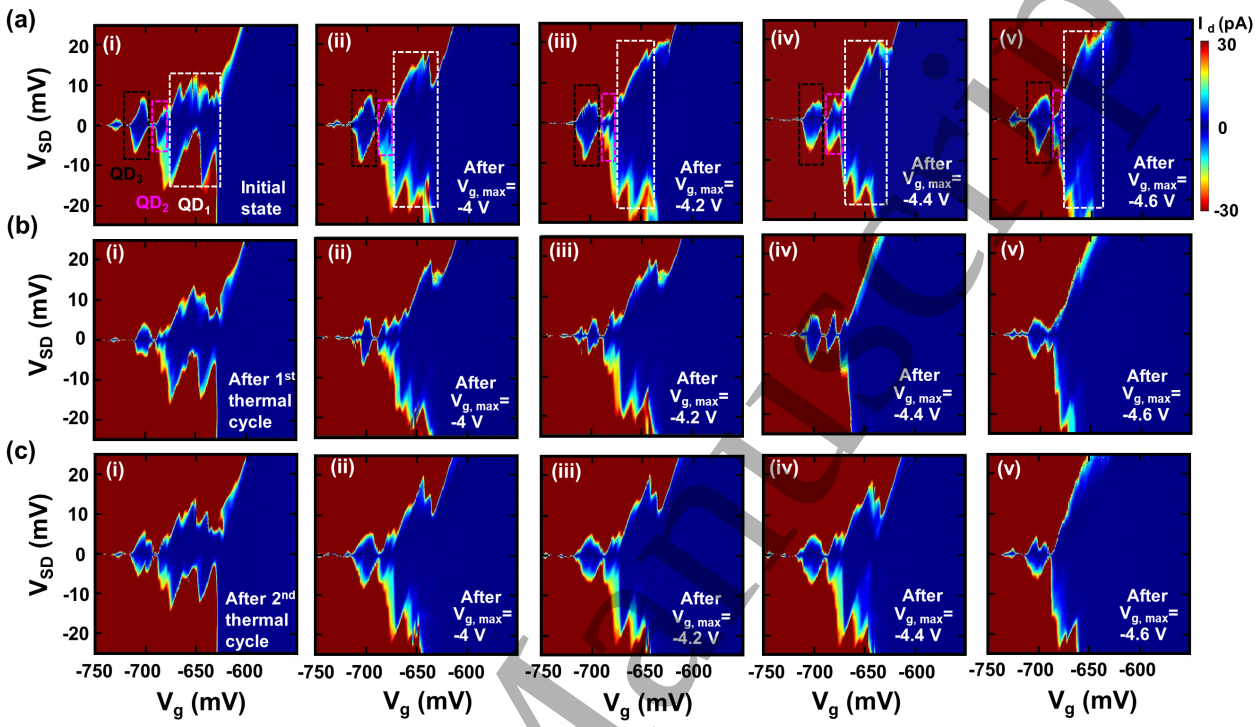

Figure 3. Charge stability diagrams (CSDs) generated from experimental data by biasing the source (V_{SD}) and gate (V_g), whilst measuring drain current (I_d) in the sub-threshold region. (a) CSDs taken of the initial state and immediately after $V_{g,max}$ = -4 V, -4.2 V, -4.4 V and -4.6 V stress sweeps in (i)-(v) respectively. The white, pink and black dashed rectangles highlight the changes to the Coulomb diamond pattern from QD_1, QD_2 and QD_3 respectively, as a result of stress-induced changes at the interface. (b) After performing one thermal cycle to 295 K and back to 2 K, the CSDs were remeasured with identical parameters in (i)-(v). (c) A second thermal cycle was performed and the CSDs were retaken again in (i)-(v) to verify a consistent response.

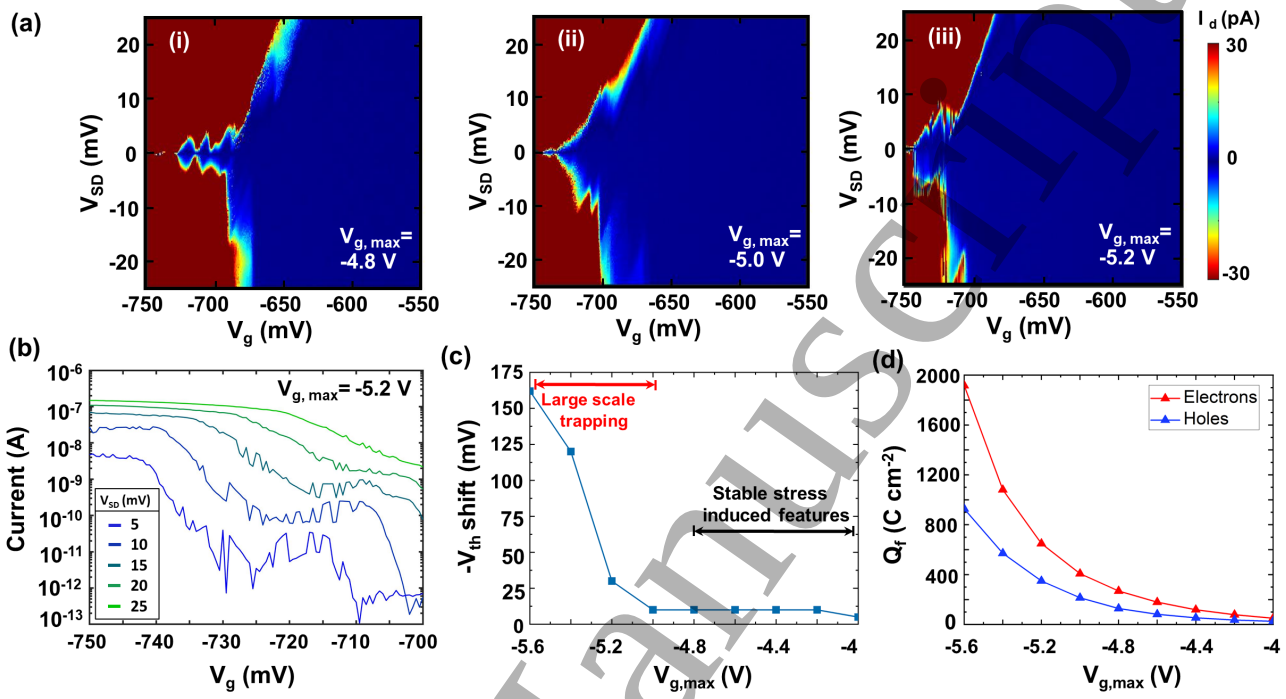

Figure 4. For $V_{g,max}$ = -4.8 V and beyond, the experimental data suggests that the device stability is compromised from large-scale trapping. (a)(i)-(iii) CSDs at elevated $V_{g,max}$ values of -4.8 V, -5 V and -5.2 V respectively. The Coulomb diamonds appear unstable in (i) with RTS becoming more prominent in (ii) and (iii). (b) I_d-V_g sweeps after $V_{g,max}$ = -5.2 V for V_{SD} = 5-25 mV, the RTS becomes very prominent and greatly affects device performance. (c) The respective change in threshold voltage (V_{th}) shift as the maximum applied stress voltage, $V_{g,max}$, increased from -4 V to -5.6 V. A significant shift can noted above $V_{g,max}$ = 5 V. (d) Charge fluence (Q_f) for both electrons and holes through the oxide at each $V_{g,max}$.

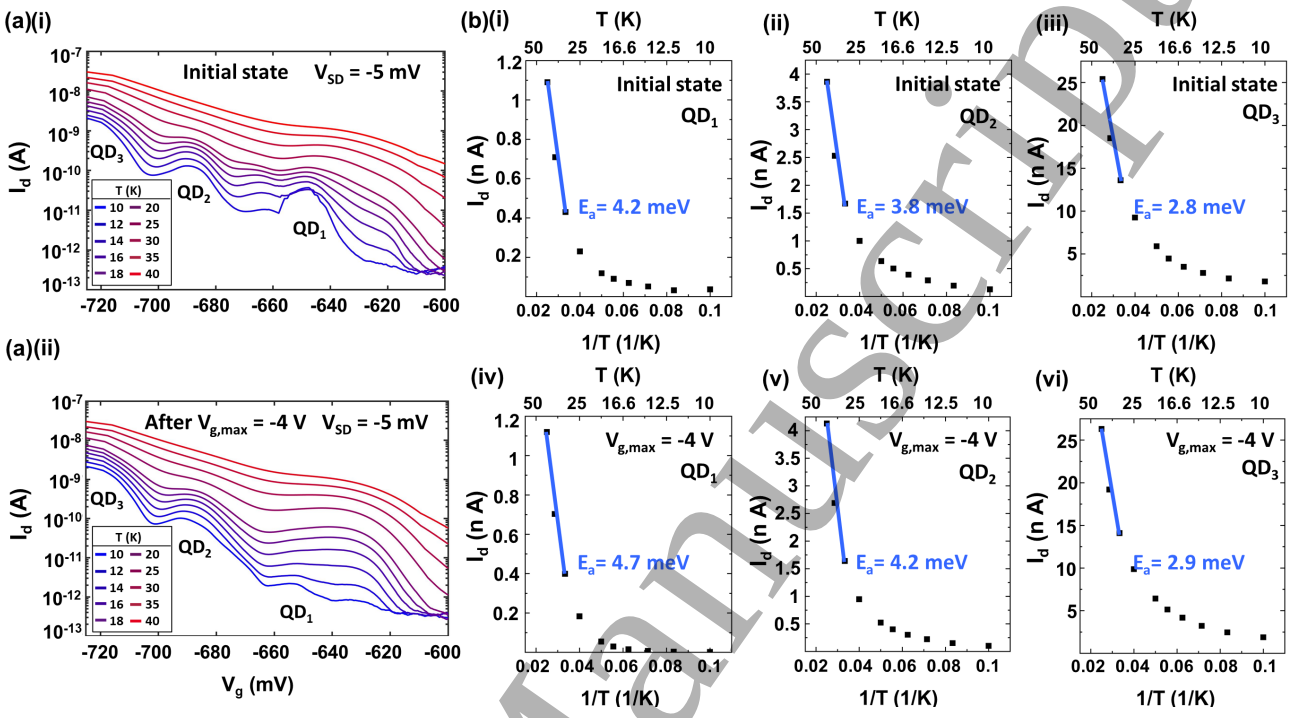

Figure 5. Estimating changes to the activation energy (E_a) after stress by using the QD temperature dependence. (a)(i) Coulomb oscillation peaks at 10-40 K for QD_1, QD_2 and QD_3 in the initial pre-stressed state and after applying $V_{g,max}$ = -4 V in (a)(ii). (b)(i)-(iii) Arrhenius plots over a 10-40 K temperature range to extract E_a from the Coulomb oscillation peaks of each QD during the initial state and after applying $V_{g,max}$ = -4 V in (b)(iv)-(vi).