Electrodeposition of GeSbTe Based Resistive Switching Memory in Crossbar Arrays

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ABSTRACT: In this work, we report on the fabrication of resistive random-access memory (ReRAM) cells based on electrodeposited GeSbTe material between TiN top and bottom electrodes in a crossbar architecture. The cells exhibit asymmetric bipolar resistive switching characteristics under the same SET and RESET compliance current (CC), showing highly uniform and reproducible switching properties. Multi-state switching behavior can be also achieved by varying the sweeping voltage and CC. Unlike phase change switching, the switching between high resistance state (HRS) and low resistance state (LRS) in these cells can be attributed to the formation and rupture of conductive Te bridge(s) within the Te rich-GeSbTe matrix upon application of a high electric field. The results point towards the usage of electrodeposition method to fabricate advanced functional device structures for application in non-volatile memory.

1. INTRODUCTION

Semiconductor memory has played a vital role in the development of modern electronic industry.[1] Driven by the desire of ultrafast data processing and massive data storage, several novel non-volatile memory technologies have been proposed and achieved significant progress in recent years.[2] Among them, resistive random-access memory (ReRAM) devices are considered as one of the most promising candidates for next generation non-volatile memory applications due to their unique characteristics. These include large resistance OFF/ON ratio (more than 10^6 orders of magnitude),[3] high switching speeds (sub 5 ns),[4] long data retention time (more than 10^6 s),[5] excellent endurance capabilities (up to 10^{12} cycles),[6] simple two-terminal Metal-Insulator-Metal (MIM) structure,[7] and low power operation.[8] In addition, by implementing these two-terminal structures into a crossbar array architecture where they are sandwiched between a set of parallel bottom electrode lines (word lines) running perpendicular to top electrode counterparts (bit lines), ReRAM can also achieve high density and scalability which will be extremely beneficial to overcome the scaling limit of current Flash memory technologies.[9]

The switching between two non-volatile resistance states (i.e. high-resistance state HRS and low-resistance state LRS) is realized in ReRAM by applying voltage pulses with different polarities and/or amplitudes. This resistive switching phenomenon is most likely associated with the repeated formation and rupture of local conductive filaments (CFs), although interfacial/bulk-based switching has been also reported.[10] Resistive switching has been observed in a wide range of materials, such as binary metal oxides,[11–15] perovskites,[16–18] 2D materials,[8,19–21] organics,[22–25] and organic-inorganic composite materials.[4,5,34–36,26–33]

Semiconductor chalcogenides represent an exciting class of materials that are demonstrating increasing potential in a variety of different memory applications.[37,38] They offer excellent

scalability and compatibility with CMOS circuits.[39] The most widely used chalcogenide is the ternary GeSbTe which has seen extensive usage in phase change memory (PCM).[40–42] The data storage in PCM relies on the rapid and reversible switch between amorphous (high resistance) and crystalline (low resistance) phase of the material. This involves a melt-quenching reset process that requires a high programming current, which has become the major obstacle for the integration of PCMs.[43–49] Resistive switching does not involve major structural phase changes and the switching can be achieved at lower voltages, resulting in longer device life.[50] This promising prospect has stimulated a significant amount of effort to investigate the resistive switching behavior of chalcogenide materials.[51] Several chalcogenide alloys including GeSbTe,[50,52–60] AgGeSe,[61] AgGeTe,[62] and AgInSbTe[63] have been reported to demonstrate resistive switching behavior. In most cases, the resistive switching effects observed in chalcogenide materials are induced by connecting and breaking the CFs from the migration of metal cations (e.g. Cu, Ag) provided by active (oxidizable) electrodes, [39,53–57,59,62,63] which is also known as the electrochemical metallization (ECM) process. This process, which requires adoption of Ag or Cu as the active metallic element could pose a problem with contamination control in mass-production lines for semiconductor device fabrication.[58] To address this concern, several chalcogenide materials-based resistive switching devices have been deposited between two inert top and bottom electrodes and exhibit reliable switching properties. In these devices, the switching between two states depends on either the formation and rupture of Sb and Te conductive filaments inside the chalcogenide materials,[50,58,64–66] or the uniform migration induced by Joule heating, which causes a high local enhancement of ionic diffusivity of Ge, Sb and Te upon application of large electric field.[52,67]

Most of the reported chalcogenide materials were deposited by techniques such as physical vapor deposition (PVD), chemical vapor deposition (CVD) and atomic layer deposition (ALD).[68] Although capable of producing device quality thin films, these "top-down" approaches normally require ultra-high vacuum (UHV) equipment and/or high temperatures, which lead to high deposition costs and slow deposition rate. Electrodeposition is a well-established deposition method in the electronics industry that offers a low-cost and fast alternative solution for chalcogenide deposition.[69,70] As a 'bottom-up' growth method, it is a site selective technique, which can be extremely beneficial for deposition into nanopatterned substrates and 3-dimensional nanostructures.[71,72] Our group has previously reported the electrodeposition of amorphous ternary GeSbTe thin films from a single, highly tunable, non-aqueous electrolyte.[46,48] The process offers good control over the composition across the GeSbTe ternary phase diagram.[73] These device-quality thin-films have demonstrated both phase change switching,[46,74] and ECM-based resistive switching when integrating with active Ag electrodes.[57]

This work will present, for the first time, the resistive switching of the electrodeposited chalcogenide GeSbTe material in a crossbar architecture. Sandwiched between two inert TiN electrodes, the cell demonstrates enhanced bipolar switching behavior with low switching voltage, narrow switching voltage distribution and good cycling endurance. The resistance states can be also controlled by varying the switching voltage and CC. The current conduction model as well as the possible switching mechanism will be also discussed.

2. EXPERIMENTAL SECTION

2.1 Non-aqueous Electrodeposition Process

Solution: Electrolytes were prepared in anhydrous CH_2Cl_2 (Sigma-Aldrich, 95 %), dried and degassed by refluxing with CaH_2, followed by distillation and then stored in the glovebox. A 0.1

M $[N^nBu_4]Cl$ (Sigma-Aldrich, ≥ 99.0%, dried) was used as the supporting electrolyte. The electrolyte contains 2.5 mM $[N^nBu_4][GeCl_5]$, 1 mM $[N^nBu_4][SbCl_4]$ and 2 mM $[N^nBu_4]_2[TeCl_6]$, which were synthesized as described previously.[73]

Electrodes: Silicon substrates with pre-patterned TiN bottom electrode lines (word lines) were prepared through a series of lithography processes to produce memory cells with a diameter of 1 μm. These word lines will also serve as the electrode for electrodeposition. A Cr (10 nm)/Au (200 nm) global contact at the top quarter of the substrate was also patterned to connect each individual word line with the potentiostat. The detailed fabrication process can be found in our previous work.[74,75] A Pt/Ir (90%:10%) disk was employed as the counter electrode and an Ag/AgCl wire (0.1 M $[NnBu_4]Cl$ in anhydrous CH_2Cl_2) was used as the reference electrode.

Electrochemistry: All cyclic voltammetry (CV) and electrodeposition experiments were carried out in a recirculating glovebox (Belle) to exclude moisture and air. Oxygen levels were kept below 10 ppm. A microAutolab 3 potentiostat and a Nova 1 software package were used for all electrochemical measurements. Prior to GeSbTe electrodeposition, voltammetry was recorded on a TiN bottom line structure in CH_2Cl_2 solution containing 2.5 mM $[N^nBu_4][GeCl_5]$, 1 mM $[N^nBu_4][SbCl_4]$ and 2 mM $[N^nBu_4]_2[TeCl_6]$ at a scan rate of 50 mV s^{-1}, Figure 1a. On the first scan reduction starts at around -1 V and there is evidence of a nucleation loop, consistent with deposition on the electrode surface, on the return scan. Similar behavior is seen on the second and third scans although now the reduction current increases less steeply, possibly due to the presence of a semiconducting deposit of GeSbTe at the electrode surface. On the return scan a stripping peak is evident at +0.5 V. This voltammetry is broadly consistent with our earlier work.[75] Electrodeposition of GeSbTe was carried out at -1.75 V vs Ag/AgCl with a cut off charge of 5 μC to allow a complete filling of the memory cells, as shown in Figure 1b. The electrode was held at

open circuit potential for the initial 5 s, followed by applying -1.75 V vs Ag/AgCl at the working electrode. The measurement stops automatically when the charge passed at the working electrode reaches 5 μC. The substrate was then rinsed in CH_2Cl_2 and stored in the glovebox.

2.2 Cell Fabrication and Characterisation

After electrodeposition of GeSbTe, TiN top electrode lines (bit lines) were patterned to form the crossbar structures with 1×10 arrays (shown in Figure 1c and 1d). The connection paths between the global electrode to each word line were subsequently broken to isolate each array.

Destructive focused ion beam (FIB) sectioning with transmission electron microscopy (TEM) and STEM-EDX measurements have been used to characterize the composition and morphology of individual electrodeposited cells. The sample was imaged and analyzed by means of STEM-EDS in doubly corrected JEOL ARM200F TEM equipped with a 1000TLE windowless Oxford Instruments spectrometer. The electrical characteristics were measured at room temperature and ambient pressure using a probe connected to a Keysight (B1500) system. For all measurements, the voltage was applied to the top electrode (bit line) while the bottom electrode (word line) was grounded.

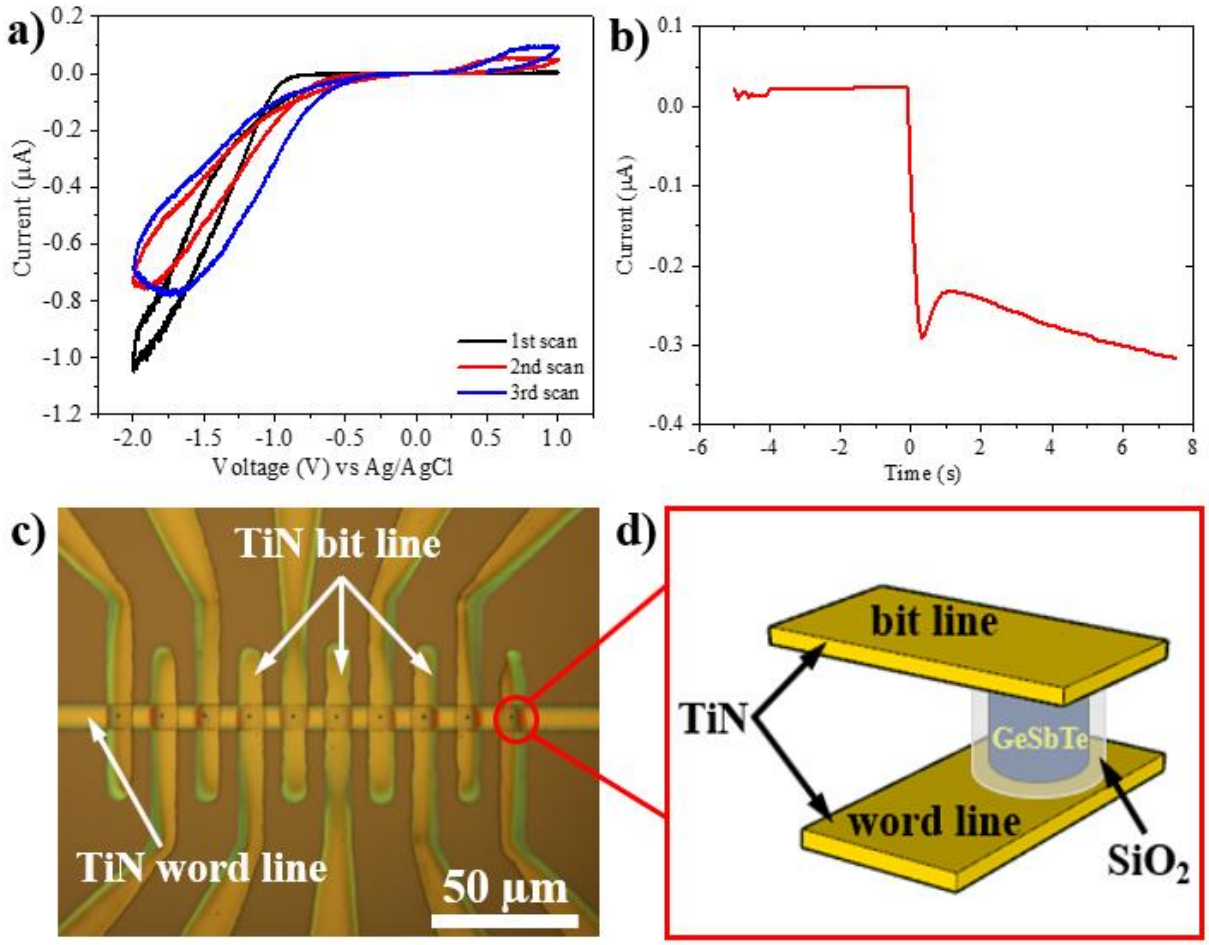

Figure 1. (a) CV of the TiN crossbar substrate (containing 1 μm TiN microelectrodes) in 0.1 M $[N^nBu_4]Cl$ electrolyte containing 2.5 mM $[N^nBu_4]GeCl_6$, 1 mM $[N^nBu_4]SbCl_4$, 2 mM $[N^nBu_4]_2TeCl_6$. Scan rate: 50 mV s^{-1}. (b) Current time transient for GeSbTe electrodeposition at deposition potential of -1.75 V vs Ag/AgCl. The cut-off charge is -5 μC. (c) Optical microscopy image of a fabricated 1 x 10 crossbar array. (d) Schematic of an individual ReRAM cell.

3. RESULTS AND DISCUSSION

3.1 Morphology and Composition

The morphology and composition of the crossbar GeSbTe resistive switching cells were investigated. Figure 2a shows a TEM cross-section image of the as-fabricated cell where the

GeSbTe layer is sandwiched between top and bottom TiN electrodes. Both bright and dark regions can be observed within the GeSbTe layer, implying the density of the electrodeposited GeSbTe varies within each memory cell and the layer is likely to be porous. We have reported similar density variations in our electrodeposited GeSbTe thin films, in which the porosity improves the ECM-based resistive switching performance by providing the pathways for Cu ion migration in the film.[57] TEM-EDX maps were taken to characterize the composition of the material and are presented in Figure 2b-f. Although all three elements can be observed in the GeSbTe layer, the as-deposited GeSbTe are clearly Te-rich. The Ge:Sb:Te composition ratio in this Te-rich GeSbTe was found to be 7:10:83. The full EDX spectrum of the layer is presented in Figure S1.

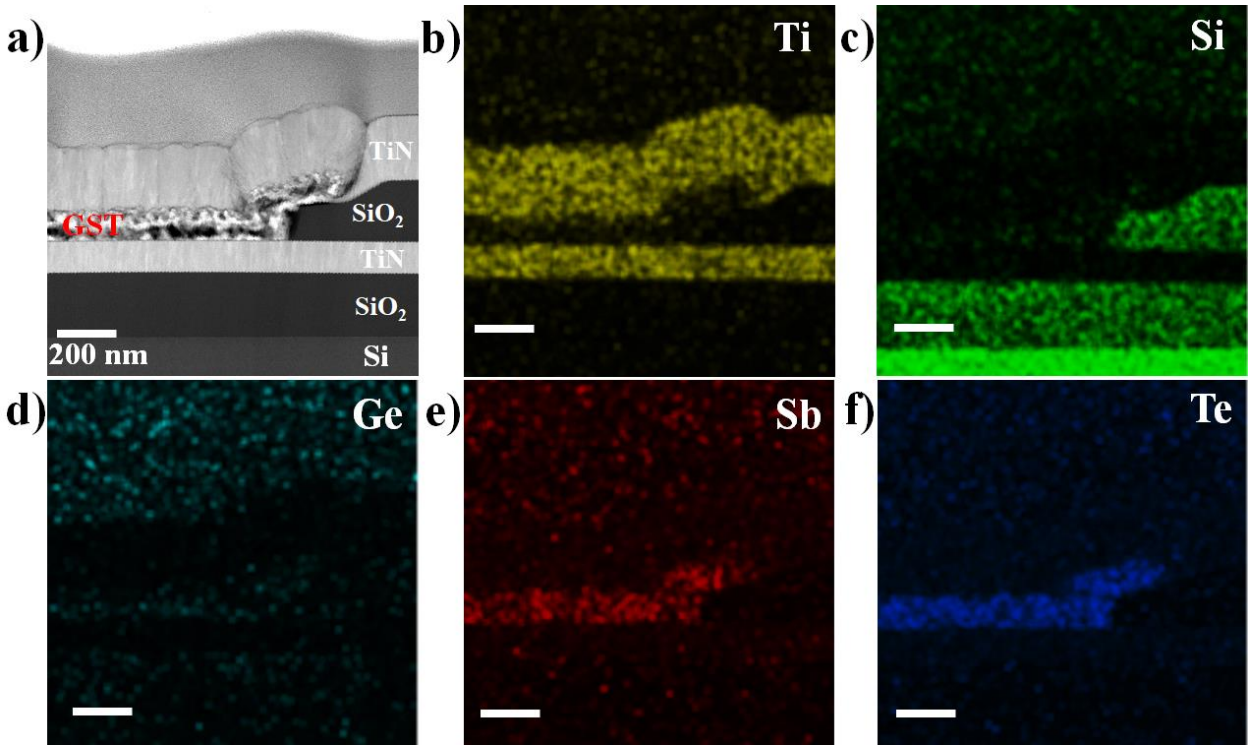

Figure 2. (a) A cross section TEM image for as-deposited GeSbTe layer in between top and bottom TiN electrodes. (b-f) Cross-sectional TEM-EDX of the as deposited GeSbTe crossbar cell. The scale bar is 200 nm.

3.2 Electrical Characteristics

DC sweeps were applied to the TiN/GeSbTe/TiN memory cells to characterize their resistive switching properties. The pristine cells were measured to be in the high-resistance state. This further confirms the amorphous phase of the as-deposited Te-rich crystals GeSbTe layer. A large positive forming voltage (~8 V) was required to induce the soft dielectric breakdown and initialize the switching through a local crystallization of the GeSbTe due to Joule heating effect as shown in the inset of Figure 3a. After forming, the cell can be switched between HRS and LRS *via* applying DC sweeps with a voltage of ± 5 V. Figure 3a shows the successive I-V characteristics of the cell after RESET process. The direction of current sweep is indicated by arrows. The cell is initially in a high resistance state (HRS). By applying a positive sweep voltage (from 0 V to +5 V), the cell switched from the HRS to LRS at a SET voltage of approximately 2 V. The cell remained in its LRS during the backward sweep voltage (from +5 V to 0 V) and even for the subsequent negative sweep voltage (from 0 V to -5 V). However, the cell switched from the LRS to HRS at a RESET voltage of approximately -2 V by reversing the negative sweep voltage (from -5 V to 0 V). Further DC sweeps for another cell showing a reproducible switching performance are reported in Figure S2a This switching behavior is clearly distinguished Such bipolar switching behavior from GeSbTe films has been reported previously where Sb and Te It is therefore reasonable to speculate that a filamentary based switching is also likely to take place in this cell. This is further supported by the abrupt transition from the HRS to It is worth noting that a CC of 1 mA was implemented in both RESET and SET processes to limit the operating current and protect the cell from breakdown. In the absence of the CC during the RESET process, the cell switches to a higher operating current value, in which the cell cannot be switched back to the HRS by application of a negative sweep voltage as shown in the Supporting Information Figure

S3. In addition, Figure S4 shows the TEM image of a cell after breakdown in the absence of CC during the RESET process. The large Joule heat generated in absence of the CC caused permanent damage to both the GeSbTe layer and the TiN electrodes.

Figure 3b shows a reproducible cycling endurance in the DC sweep mode for 70 cycles. The resistance ratio between the HRS and LRS is about 1 order of magnitude at 0.5 V, which is sufficient for memory application. Both HRS and LRS showed excellent uniformity without significant degradation. To elucidate further the switching stability of the cell, cumulative probability distributions for HRS and LRS are plotted in Figure 3c. The figure clearly shows that the HRS and LRS are uniformly distributed with the coefficients of the variation (σ/μ, σ is the standard deviation and μ is the mean value) calculated to be 1.34% and 1.68% for HRS and LRS, respectively. Furthermore, high uniformities were also observed for both V_{SET} and V_{RESET} as shown in Figure 3d, where the coefficients of the variation were 8.42% and 4.67%, respectively. The high uniformities of both programming voltages are essential for the large-scale ReRAM applications. Retention data test for a TiN/GeSbTe/TiN memory cell in both the HRS and LRS was also performed as shown in the Supporting Information Figure S2b.

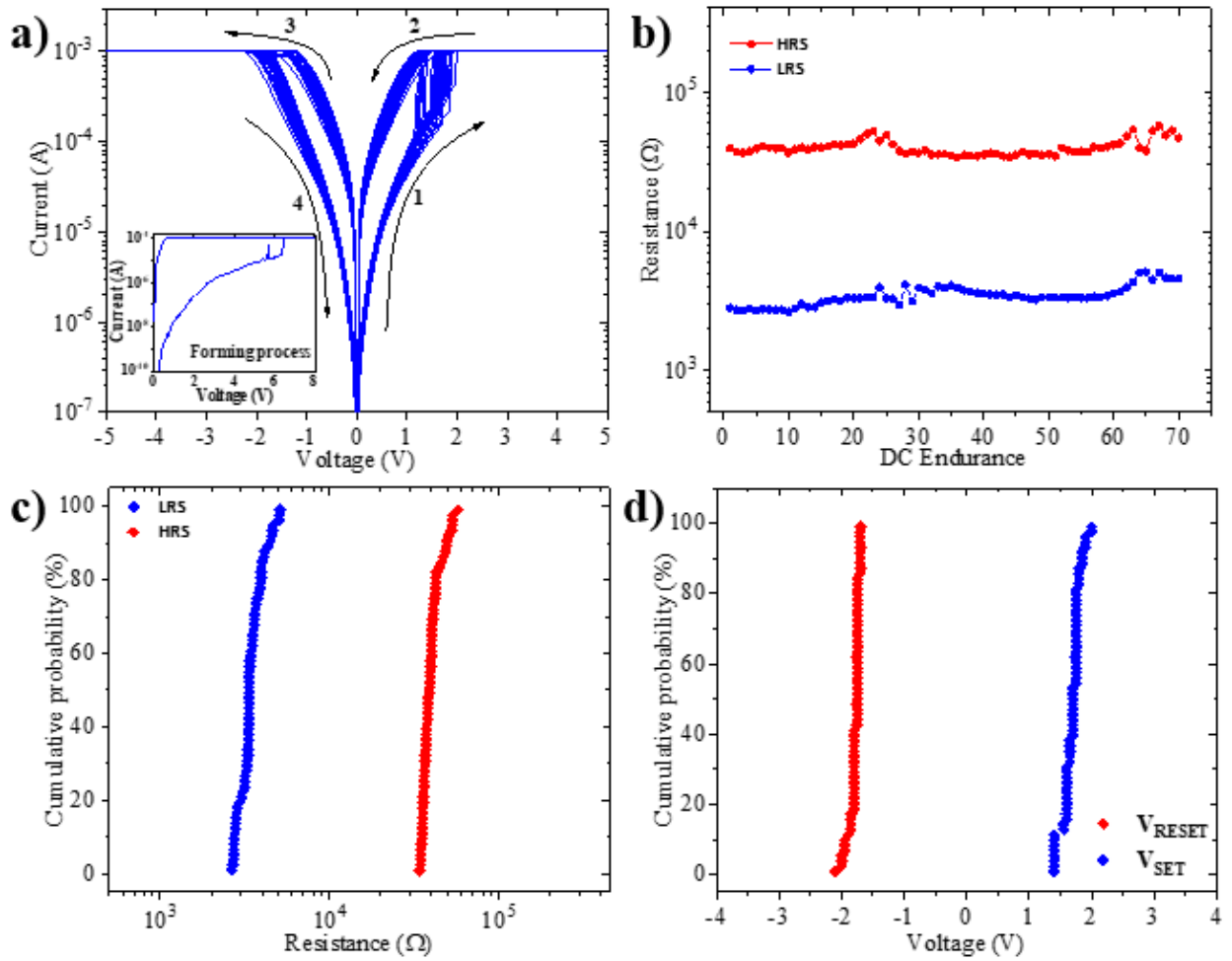

Figure 3. Resistive switching properties of the electrodeposited crossbar TiN/GeSbTe/TiN memory cell. (a) Consecutive I-V characteristics , inset shows the forming process with CC of 100 µA; (b) Endurance characteristics; (c) Cumulative probability of HRS and LRS, and (d) V_{SET} and V_{RESET}.

The resistive switching in our memory cell can be also controlled by varying the voltage and CC to demonstrate multi-state switching behavior. Figure 4a shows the I-V characteristics of a TiN/GeSbTe/TiN cell measured at different DC sweep voltages (±5 V and ±7 V) with a fixed CC at 500 µA. After the forming process, the cell can be switched between the HRS and LRS upon the application of a negative and positive DC sweep, respectively. During the first RESET DC sweep from -5 V to 0 V (blue), the RESET was observed at *ca.* -2 V and the HRS was measured

to be *ca.* 110 kΩ (@ 0.5 V). After SET the cell back to LRS, the subsequent RESET was conducted with a DC sweep from -7 V to 0 V (green). The RESET during this sweep took place at *ca.* -2.9 V and resulted in an HRS of *ca.* 450 kΩ (@ 0.5 V) which is over 4 times higher than the previous HRS, clearly indicating its potential for multi-state storage applications. This behavior is rather unexpected considering the actual voltages on the cell are less than the programmed voltages due to the implementation of CC. However, a larger voltage effectively implies a longer electrical stress being applied on the cell (i.e. 0.35 s in this case). The higher OFF resistance state obtained here is therefore likely to be induced by a combination of elongated electrical stress and potential larger electrical field. Apart from the RESET DC sweep, the resistance states can be also controlled *via* different CC levels. As demonstrated in Figure 4b, the CC level was increased from 500 μA to 700 μA after the first DC sweep cycle (blue). This resulted in a higher OFF resistance state after the RESET sweep from -5 V to 0 V (red), which could be ascribed to the higher RESET voltage allowed on the cell with higher CC. After RESET, the cell can be further SET to a lower ON state at CC of 700 μA, achieving an increment of the OFF/ON resistance ratio from *ca.* 6 to 35 (@ 0.5 V). Such CC-dependence control has been widely reported to be an effective way to achieve multi-state switching for resistive memory and can be associated with the formation of filaments with different dimensions across the cell.[3,79,80] Supporting Information Figure S5 shows a reproducible multi-state switching behavior for a TiN/GeSbTe/TiN memory cell.

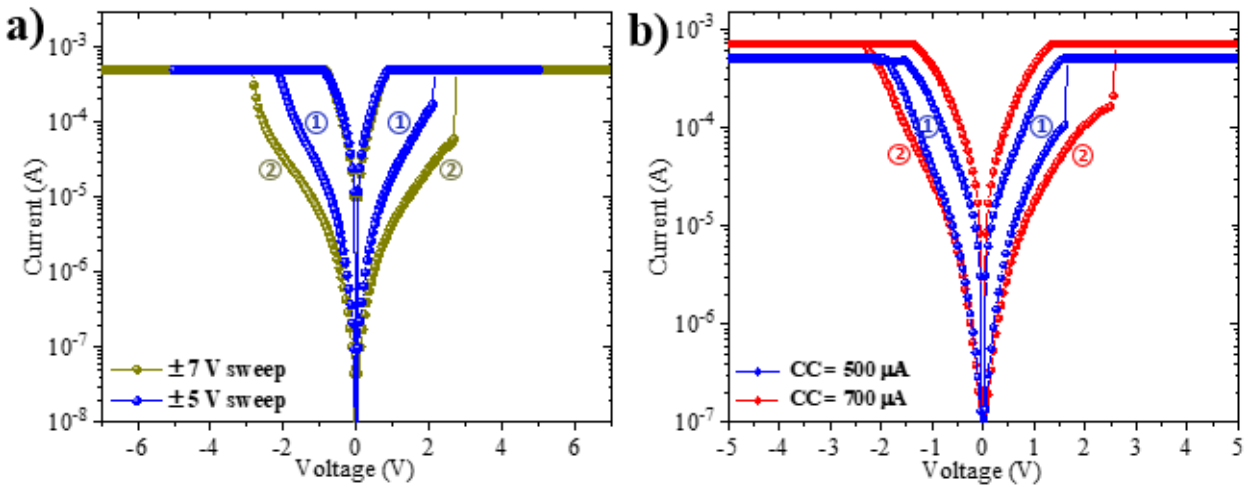

Figure 4. (a) I-V characteristics of a TiN/GeSbTe/TiN crossbar ReRAM cell for different maximum voltage sweeps. (b) I-V characteristics of a TiN/GeSbTe/TiN crossbar ReRAM cell for different current compliance.

The conduction mechanism of the electrodeposited GeSbTe crossbar ReRAM cell is examined by plotting the positive part of the I-V curve for the memory cell swept between ±5 V on a log – log scale as shown in Figure 5a. The fit suggests that the conduction mechanism in our ReRAM cell is governed by the Space-Charge-Limited-Current (SCLC) model. Initially from 0 V to 0.25 V at HRS, the cell shows a linear dependence of current with applied voltage ($I \propto V$), with a slope of about 1. This is attributed to Ohmic conduction mechanism, which arises from thermally generated charge carriers.[31] At higher applied voltage, 0.3 ≤ V ≤ 1.3 V, the slope changes to about 2, and the current shows the voltage square dependence ($I \propto V^2$). In this regime, charge injection from the electrode begins to dominate and trap-controlled space charge limited current (TC-SCLC) takes place, as described by the Mott-Gurney law:[81]

$$J = \frac{9\varepsilon\mu V^2}{8d^3} \quad (1)$$

where J is the current density, ε is the dielectric constant, μ is the free carrier mobility, V is the applied voltage, and d is the insulator thickness. In the region of $1.35 \leq V \leq 2.1$ V, a much steeper rate of current increase occurs ($I \propto V^{\alpha}$, $\alpha \approx 3$). This indicates that all traps are filled, and the conduction mechanism in this region can be ascribed to trap-filled space charge limited conduction (TF-SCLC). At the threshold of 2.15 V, a sharp transition in the current occurs, switching the cell from the HRS to the LRS. In the case of the LRS, the conduction mechanism is dominated by two regions: Ohmic conduction at low applied voltage, featuring by the linear dependence of current with applied voltage, ($I \propto V$), and SCLC at higher voltage, where the current shows the voltage square dependence, ($I \propto V^2$) . The similar conduction mechanism is observed for the memory cell swept between ±7 V, as shown in Figure 5b.

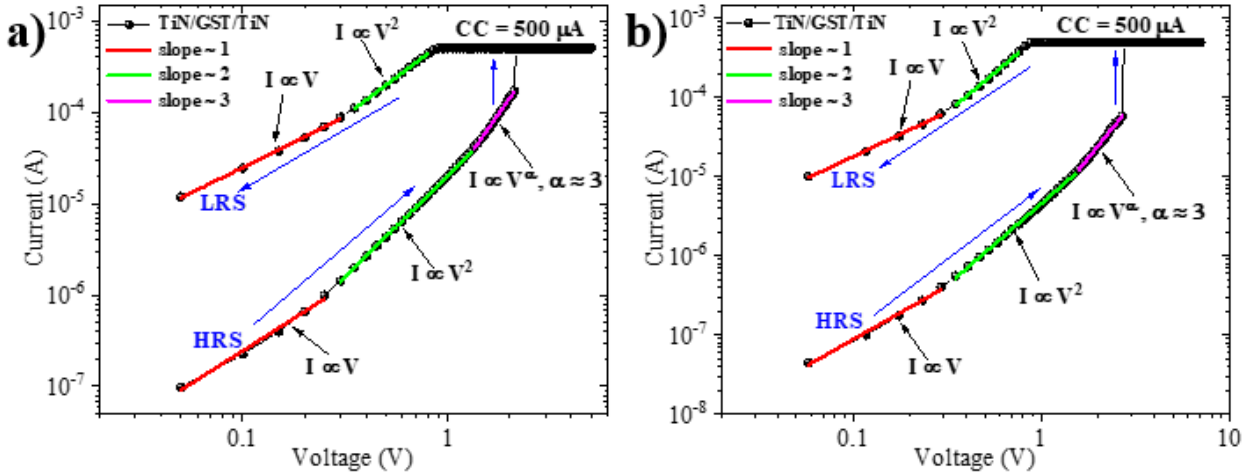

Figure 5. I-V sweeps for a TiN/GeSbTe/TiN ReRAM cell demonstrating fits to the SCLC mechanism for the HRS to LRS transition for different maximum voltage sweeps; ±5 V (a) and ±7 V (b).

The resistance switching effect induced by changing the polarity of an applied electric field can be related to the solid-state electrolyte behavior of the GeSbTe chalcogenide. Applying the electric field in one polarity induces electrochemical reactions at the interfaces leading to ionic conduction.

Once the applied electric field is sufficient, conductive filaments across the GeSbTe thin film can form and connect the two electrodes, switching the cell to the LRS. Changing the polarity of applied electric field ruptures the conductive filaments owing to ion movement in the opposite direction, switching the cell to the HRS. It has reported that the switching mechanism between the two resistance states in chalcogenides such as Ag-Ge-Se[61] and Ag-Ge-Te,[62] is based on formation and rupture of Ag conductive filaments. However, in the absence of any active electrode or metallic dopants (e.g. Ag or Cu), the resistive switching observed in our cell is likely related to the filaments formed by the elements (e.g. Ge, Sb or Te) in the electrodeposited GeSbTe layer. In fact, such mechanism has been reported in GeSbTe chalcogenide[50,64] based resistive switching cells in which the resistive switching effect attributed to the formation and rupture of conductive Sb filaments instead of Ag. A similar switching mechanism in our Te-rich GeSbTe based cells is more likely occurred when the GeSbTe is subjected to different electric field polarity. The switching between LRS and HRS states can be ascribed by the formation and rupture of conductive Te filament(s) between the GeSbTe and the top and bottom electrodes. The selected area electron diffraction (SEAD) pattern of the electrodeposited Te rich- GeSbTe chalcogenide material is presented in Figure 6. The graph indicates the existence of the Te nanocrystals (~5-10 nm) in the as electrodeposited GeSbTe material. These Te nanocrystals facilitate the formation process of CFs through a resistive phase of GeSbTe matrix. It has to be mentioned that the chalcogenide materials fabricated by electrodeposition technique show a nonporous structure, which can also facilitate the formation process of Te CFs.[57] The GeSbTe material can act as an electrolyte in which a resistive switching behavior induced by electrochemical reactions can occur upon changing the polarity of an external applied electric field.

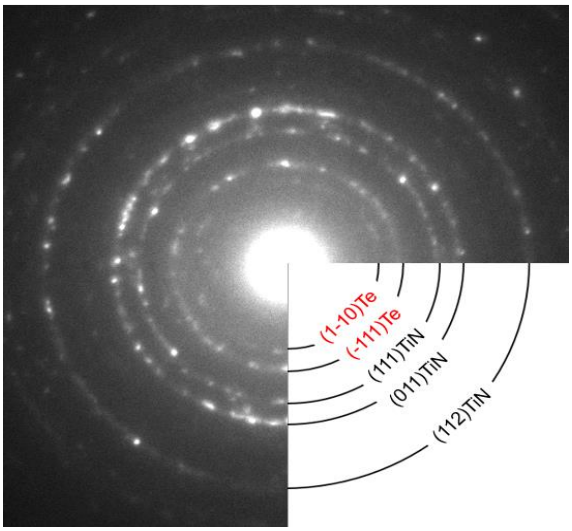

Figure 6. The selected area electron diffraction (SEAD) pattern of the electrodeposited Te rich-GeSbTe chalcogenide material.

The schematic of the proposed switching mechanism is presented in Figure 7. Figure 7a shows the initial state of the cell where a large amount of Te atoms are available in the GeSbTe matrix. Applying a positive/negative potential to the top/bottom TiN electrode ionizes the Te atoms (Te^{2-}) at the bottom electrode through the injected electrons.[82] Under high electric field, the Te^{2-} ions can move to the top electrode, where the neutral Te atoms are accumulated and start to form a filament (Figure 7b). Once the grown filament reaches the bottom electrode, the cell switches to the LRS (SET process) as illustrated in Figure 7c. In contrast, upon reversing the polarity of applied potential, the Te^{2-} ions formed at the top electrode move to the bottom electrode and rupture the existing filament, resulting in switch the cell back into the HRS (RESET process) as shown in Figure 7d. A similar mechanism has also been proposed for sputtered amorphous GeSbTe ReRAM cells with excess Te in the film.[58]

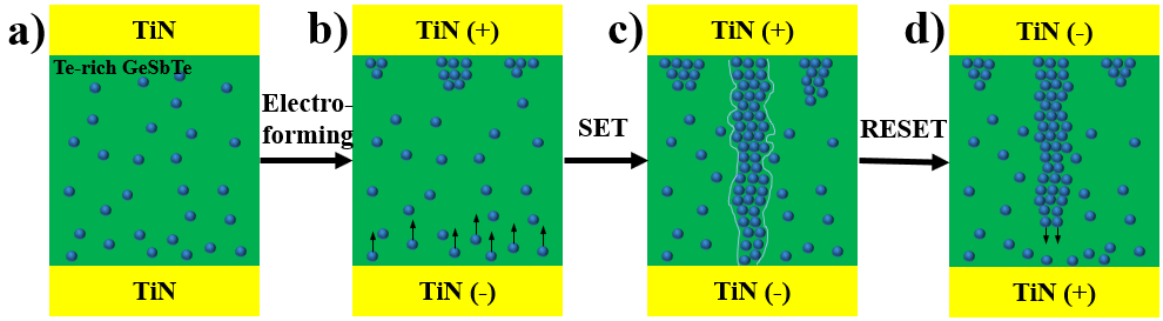

Figure 7. Schematic showing the resistive switching mechanism in Te rich- GeSbTe based ReRAM cells. (a) Initial state; (b) electro-forming process; (c) SET process, and (d) RESET process.

4. CONCLUSIONS

In summary, we demonstrate a typical resistive switching behavior in electrodeposited Te rich-GeSbTe chalcogenide material in a crossbar architecture. The cells show a polarity-dependent switching behavior with low switching voltage, narrow switching voltage distribution and good cycling endurance. The resistance states can be controlled *via* the sweep voltage and current compliance, demonstrating multi-state switching behavior. The fitting of the I-V curve showed that the conduction mechanism for the transition from the HRS to the LRS is dominated by space charge limited conduction. The formation and rupture of conductive tellurium filament(s) upon application of different polarity of a high electric field is proposed to explain such bipolar switching behaviors in the absence of any active electrodes and dopants. The successful demonstration of the high-quality switching performance on a crossbar structure through our low-cost electrodeposition approach provides a promising future for this method to be used for large scale non-volatile memory manufacturing.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at

Extra details of the EDX spectroscopy, TEM, and electrical characterization are available in the Supporting Information document ()

Notes

There are no conflicts to declare.

Data supporting this study are openly available from the University of Southampton repository at DOI: https://doi.org/10.5258/SOTON/D2026. Additional data from this study are available from the corresponding author upon reasonable request.

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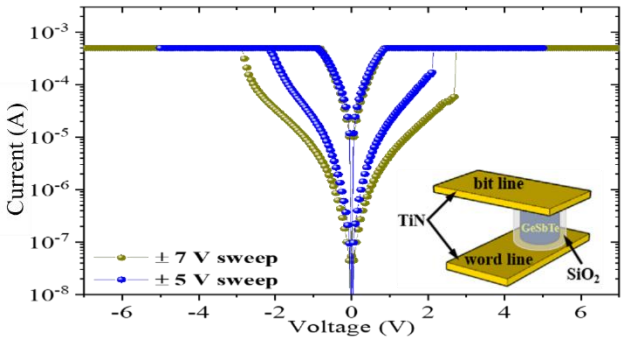
TOC Graphic (8.25 cm*4.45 cm)



Supporting Information

Electrodeposition of GeSbTe Based Resistive Switching Memory in Crossbar Arrays

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Supplementary Figures

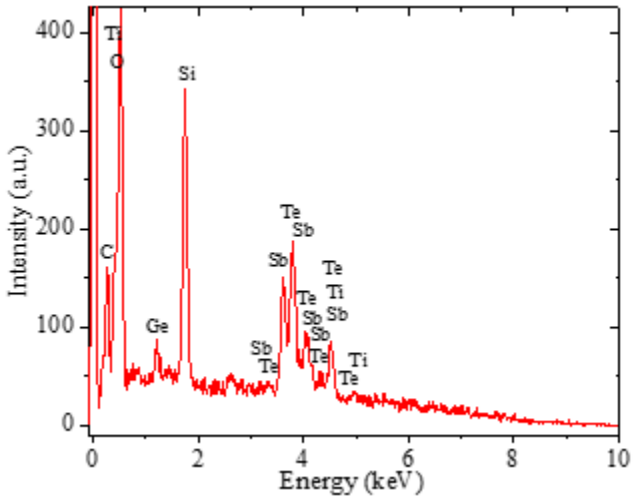

Figure S1. EDX spectrum of the electrodeposited GeSbTe showing the existence of Ge in the GeSbTe crossbar array. The EDX spectrum shows the presence of Cl inside the cell, which is originated from the electrolyte.

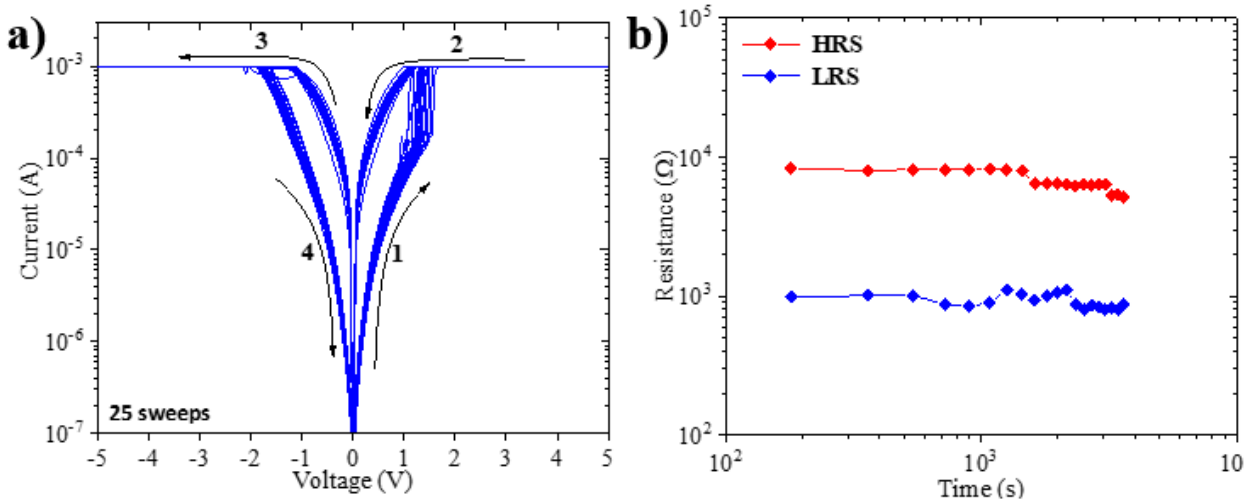

Figure S2. (a) Consecutive I-V characteristics of an electrodeposited crossbar TiN/GeSbTe/TiN memory cell swept between -5 V and 5 V with CC of 1 mA. The graph clearly shows a uniform and reproducible resistive switching properties of the memory cell. (b) Retention data test for a TiN/GeSbTe/TiN memory cell in both the HRS and LRS measured at 0.2 V for 1 hour without considerable resistance degradation.

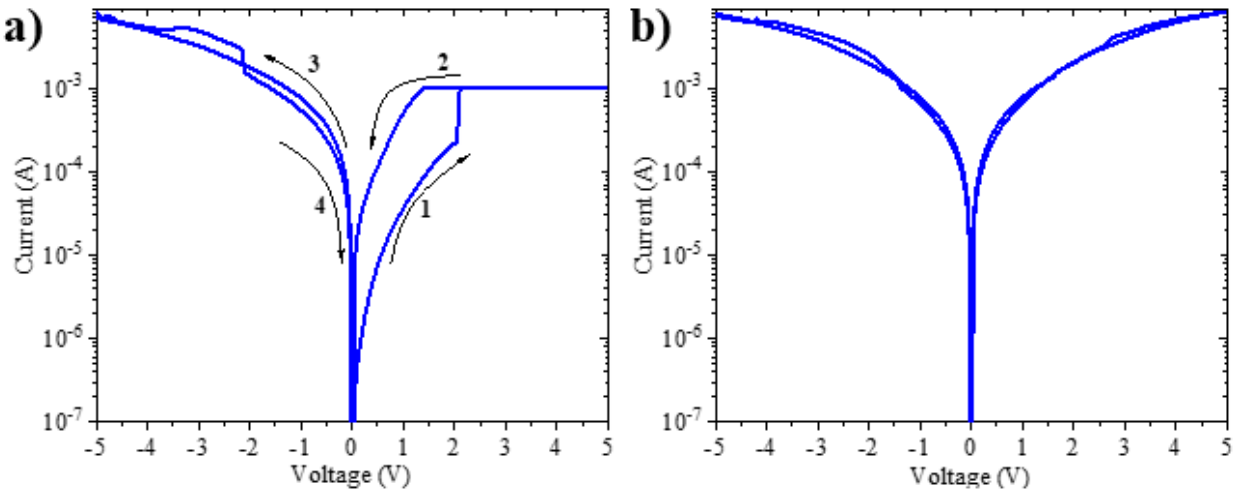

Figure S3. I-V characteristics of an electrodeposited crossbar TiN/GeSbTe/TiN memory, showing the impact of absence of the CC during the RESET process on the resistive switching properties. (a) I-V curve shows that the cell switches to a higher operating current value, in which the cell cannot be switched back to the HRS by application of a negative sweep voltage. (b) The subsequent I-V curve shows the diminishing of the resistive switching properties of the cell.

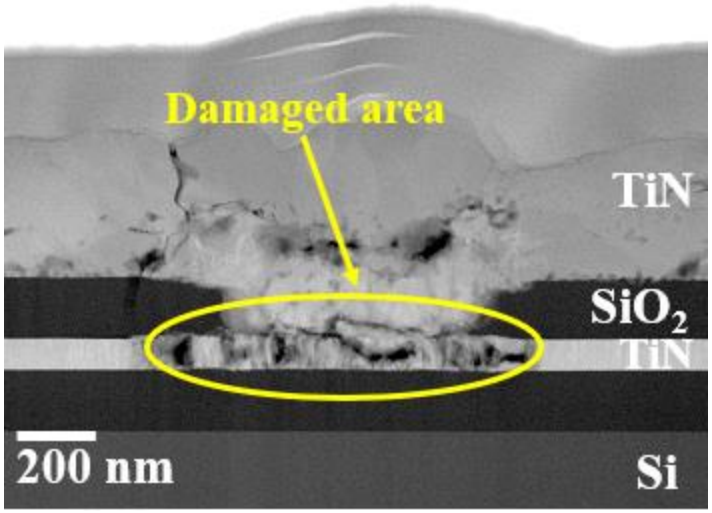

Figure S4. TEM image of a damaged device after breakdown. The large Joule heat generated in the absence of the CC during the RESET process caused permanent damage to both the GeSbTe layer and the TiN electrodes.

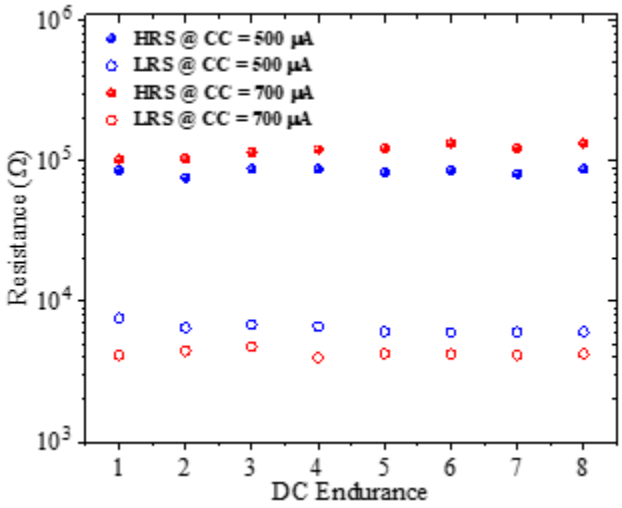

Figure S5. Multi-state resistance behavior of a TiN/GeSbTe/TiN memory cell by varying the CC from 500 μA (blue data) to 700 μA (red data). It can be observed that changing the CC resulted in the variation of LRS and HRS.[1,2] The resistance values of both LRS and HRS were measured at 0.5 V.

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