

**High-bandwidth InGaAs photodetectors heterogeneously integrated on silicon waveguides using optofluidic assembly**

*Youngho Jung, Sunghyun Bae, Kyungmok Kwon, Colin J. Mitchell, Ali Z. Khokhar, Graham T. Reed, James S. Wilkinson, Yun C. Chung, and Kyoungsik Yu\**

Dr. Y. Jung, Dr. S. Bae, Dr. K. Kwon, Prof. Dr. Y. C. Chung, Prof. Dr. K. Yu  
School of Electrical Engineering, Korea Advanced Institute of Science and Technology,  
Daejeon 34141, Korea  
E-mail: ksyu@kaist.edu

Dr. C. J. Mitchell, Dr. A. Z. Khokhar, Prof. Dr. G. T. Reed, Prof. Dr. J. S. Wilkinson  
Optoelectronics Research Centre, University of Southampton, SO17 1BJ Southampton, UK

Dr. Y. Jung  
Present address. Max Planck Institute of Microstructure Physics, Weinberg 2, Halle 06120,  
Germany

Dr. K. Kwon  
Present address. Department of Electrical Engineering and Computer Sciences, University of  
California, Berkeley, CA 94720, USA

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Light-induced manipulation techniques have been utilized to transport, trap, or levitate microscopic objects for a wide range of applications in biology, electronics, and photonics. Without making direct physical contact, they can provide simple yet powerful means for high-precision assembly of micro-scale functional blocks and components within the integrated circuit platforms, thereby offering a viable alternative to the conventional heterogeneous integration techniques, such as wafer/die bonding and transfer printing. Using a microbubble-based optofluidic pick-and-place assembly process, we experimentally demonstrate heterogeneous integration of compact III-V semiconductor photodetectors on a silicon-based photonic integrated circuit chip, enabling direct high-speed vertical electrical contacts for significantly improved photo-generated carrier transit distance/time. The microdisk-shaped InGaAs p-i-n photodetector integrated on the silicon waveguide has a 3-dB bandwidth exceeding 50 GHz under the applied bias voltage of  $-1$  V for near-infrared wavelengths around  $1.55$   $\mu\text{m}$ . The light-induced optofluidic assembly will provide a promising route for

seamless heterogeneous integration of various optoelectronic components with high-speed and low-noise electrical interconnection on the fully processed silicon photonic/electronic integrated circuit platforms.

## 1. Introduction

Photodetectors (PDs), which translate optical intensity signals into the electrical domain, are one of the essential building blocks in photonic integrated circuits (PICs). Even though the optical transparency of Si materials at near infrared wavelengths enables highly-confined light guiding with small absorption losses in silicon (Si)-based PICs, such transparency also makes optical-to-electrical conversion very inefficient in Si. Although Si-based sub-bandgap near infrared PDs have been implemented by taking advantages of non-intrinsic light absorption effects, resulting from deep-level defect formation in the Si lattice by implanting various ions or dopants,<sup>[1, 2]</sup> surface states absorption or photon-assisted tunneling effects,<sup>[3-5]</sup> these effects still require relatively large bias voltages ( $>5$  V) and/or long absorption lengths ( $>100$   $\mu\text{m}$ ). Therefore, heterogeneous integration of other semiconductor materials for high-performance photodetection with reasonable footprints and operation conditions has been actively sought to overcome the intrinsic limitations of Si-based PICs. For example, germanium (Ge)<sup>[6, 7]</sup> and direct-bandgap III-V compound semiconductors<sup>[8-13]</sup> have been successfully integrated with Si-based PICs. Among various materials, this study focuses on indium gallium arsenide (InGaAs)-based PD devices because of small leakage currents and high sensitivity in the optical telecommunication bands.

The overall performance of the heterogeneously integrated III-V compound semiconductor-based PDs, especially in terms of their responsivities and bandwidths, are critically dependent on the integration technique as well as the device structure design. High-speed III-V compound semiconductor-based PDs directly integrated on the Si-based PICs have been mainly achieved by wafer/chip-level bonding<sup>[8-11]</sup> and hetero-epitaxial growth.<sup>[12-16]</sup> However, to create electrical contacts to the vertically grown III-V compound semiconductors, the so-called mesa structures

(lateral electric contact configuration) need to be defined by post-fabrication steps after the bonding or material growth process. Unfortunately, the metal contact for the bottom semiconductor layer is usually located at least several micrometers laterally away from the top metal contact areas, which significantly increases the overall carrier transit distance/time. Furthermore, the remaining thin bottom semiconductor layer for efficient light coupling will require sophisticated fabrication steps, although the series resistance has been much improved down to few Ohms recently.<sup>[17, 18]</sup> This non-ideal electrical interconnect configuration may result in substantial degradation of operation bandwidths and power consumptions, and it is therefore hard to realize large 3-dB bandwidths (*e.g.*, >35 GHz) using the III-V p-i-n PDs heterogeneously integrated on the Si-based PICs, to the best of our knowledge.

In this study, as an alternative to the conventional mesa-type device structure, we demonstrate a vertical electrical interconnection technique for Si waveguide-coupled InGaAs p-i-n PDs, which can considerably improve the device operation bandwidth by reducing photo-generated carrier transit distance/time. To achieve such a vertical electrical contact configuration for heterogeneous optoelectronic integration, we take advantage of a localized light-induced pick-and-place micro-manipulation and assembly technique that is capable of optofluidic tweezing, levitation, and transport of micro/macrosopic objects with a wide range of applications.<sup>[19-22]</sup> We previously introduced the laser-induced microbubble manipulation method for sophisticated integration of micro-scale III-V compound semiconductor blocks in liquid as shown in Supporting Movie 1.<sup>[23]</sup> Compared to other manipulation techniques, it requires no additional fabrication steps for in-situ bubble generation, such as deposition and patterning of light-absorbing layers, because the micro-scale compound semiconductor block itself has a good photothermal conversion efficiency in the near-infrared wavelengths. In addition, the assembly position of the integrated device can be accurately controlled with less than one-micrometer precision and the proposed optofluidic assembly process does not introduce physical/optical damages to the micro-scale semiconductor blocks.<sup>[23]</sup> These unique

features allow precise pick-and-place assembly of fully processed micro-scale III-V compound semiconductor blocks ( $<100\ \mu\text{m}$ ) onto the PICs, and, therefore, additional etching of III-V semiconductor materials is not required after micro-assembly. In contrast, the direct wafer/die bonding or epitaxial growth techniques still require additional fabrication processes for the metallization of a bottom layer of III-V semiconductor.

## 2. Results

### 2.1. Device Fabrication

**Figure 1** illustrates the overall microbubble-based optofluidic assembly process for heterogeneous integration of an InGaAs-based p-i-n PD on a Si waveguide with high-speed vertical electrical contacts. The III-V epitaxial layer structure consists of an intrinsic  $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$  layer with a thickness of 400 nm for a light absorption layer, sandwiched between 50-nm thick p- and n-type InGaAs layers for Ohmic contacts to the bottom and top metal electrodes, respectively. **Figure 2a** shows the scanning electron micrograph (SEM) of the fabricated PDs with a thin metal contact layer on the p-type layer just before the final releasing process from the indium phosphide substrate. We selected a circular microdisk-shaped PD structure because it is rotationally symmetric, allowing an easy alignment and assembly process regardless of the device orientation. Next, we carried out the microbubble-based assembly for heterogeneous integration on the silicon-on-insulator (SOI) rib waveguide comprising of a Si device layer thickness of  $\sim 400\ \text{nm}$ , an etch depth of  $\sim 250\ \text{nm}$ , and a waveguide width of  $\sim 450\ \text{nm}$  for single-mode optical waveguiding at a wavelength of  $1.55\ \mu\text{m}$  (see “Experimental Section/Methods” and Figure S1 for the details of our fabrication processes). After the III-V semiconductor PD blocks were transferred onto the Si photonic chip in a fluidic environment (in our case, deionized water; Figure 1a) using a syringe, a continuous-wave 975-nm-wavelength laser beam was focused on the surface of the PD object to locally raise its temperature and generate a microbubble adhered on the PD surface (Figure 1b). The PD object can be trapped by thermocapillary convective flows around the microbubble and dragged in

any lateral directions by moving the laser heating spot. When the microdisk-shaped PD block was precisely moved and dropped onto the assembling pedestal position (red circular spots shown in Figures 1a and 1b), the thin metal layer of the PD was adhered to the bottom metal layer of the assembling area; that is, a metal-to-metal contact using thermo-optic effects and Van der Waals forces (Figure 1c). The details of the microbubble manipulation process are described in our previous work.<sup>[23]</sup> Finally, top metallization was realized following low-temperature SiO<sub>2</sub> passivation layer deposition (Figure 1d). Figures 2b and 2c show a cross-section and a top view of the fully processed heterogeneous integration, highlighting the details of the directly vertical electrical contact as well as the optical coupling region between the InGaAs PD and the Si rib waveguide. The short transmission line and electrical pads are designed for a standard ground-signal-ground (GSG) type radio frequency (RF) probe for high-speed response measurements.

Realizing this type of vertical electrical contact configuration using direct wafer/die bonding or epitaxial growth techniques is nontrivial, due to the surface flatness requirements for the wafer bonding and lattice constant and thermal expansion coefficient mismatch for the direct epitaxial growth. Other pick-and-place techniques, such as flip-chip bonding<sup>[24]</sup> and stamp-assisted transfer printing<sup>[25-27]</sup> can be a good alternative, but it is not always straightforward to apply such techniques with high assembly precision required for miniaturization of active semiconductor optoelectronic devices compatible to the PIC feature sizes.

## 2.2. Static Response Characterization

The final integrated III-V semiconductor PD structure has a diameter of 20  $\mu\text{m}$ , and the light coupling length between the integrated PD and the underlying Si waveguide is about 12  $\mu\text{m}$  (inset of **Figure 3a**). A typical static current-voltage (I-V) characteristic without light input after assembly is shown in Figure 3a. The dark currents under a bias voltage of  $-0.5\text{ V}$  and  $-1\text{ V}$  are around 0.5 nA (corresponding to the current density of  $\sim 1.6 \times 10^{-4}\text{ A/cm}^2$ ) and 2 nA ( $\sim 6.4 \times 10^{-4}\text{ A/cm}^2$ ), respectively, which is similar to or better than the previously reported results for bulk-

type III-V p-i-n PDs heterogeneously integrated on the Si-based PIC platforms.<sup>[11-13]</sup> To obtain lower dark currents, researchers have explored novel integration techniques using quantum wells/dashes/dots for absorption layers to take advantages of two- or three-dimensional carrier confinement.<sup>[28-31]</sup> Although such approaches may lead to the ultralow dark currents down to the tens of pA level ( $10^{-6}\sim 10^{-8}$  A/cm<sup>2</sup>), the demonstrated device bandwidths have been mostly limited to only a few GHz (See Supporting Information for more details).

From the measured I-V curve, the device exhibits a total series resistance as low as 8.7  $\Omega$ , including the resistance caused by the probe tips and metal routing lines ( $\sim 3.5$   $\Omega$ ). For five different samples, the average resistance was measured to be  $\sim 6.8$   $\Omega$ , implying that the Van der Waals force of the metal interface between the PD and the assembling position is enough to form electrical contacts without additional heat or pressure treatment after microbubble-based optofluidic assembly.

For responsivity measurements, a reverse bias voltage of  $-0.3$  V was applied and laser light with a wavelength of 1.55  $\mu\text{m}$  was injected from an optical fiber into the Si rib waveguide through a grating coupler. The integrated PD is optically coupled to the Si waveguide through vertical evanescent-wave coupling. Excluding the average fiber-to-grating coupling loss of  $\sim 5$  dB from a laser input power of  $\sim 10$  mW, the waveguide-to-detector responsivity was measured to be  $\sim 0.22$  A/W ( $=676$   $\mu\text{A}/3.05$  mW), corresponding to an external quantum efficiency of 18 %. The relatively low responsivity and the quantum efficiency resulted from the short coupling length and a relatively large vertical gap between the PD and waveguide (refer the absorption simulations in Figure S2). Degradation of absorption efficiency from both top and bottom metal electrodes was negligible according to the three-dimensional finite-difference time-domain (FDTD) simulation. If the vertical gap dimensions were optimized by adjusting the thickness of the metal layer on the PD and the SOI assembling position, it would have been possible to achieve more efficient evanescent coupling and higher light absorption within the PD absorption layer, resulting in better responsivity and external quantum efficiency without

compromising the overall bandwidth characteristics (although the detailed coupling structure design and the optimization process to maximize the optical power transfer are beyond the scope of our current work). The linearity at different incident optical power levels in the range of 200 nW to 3 mW was also analyzed. As shown in Figure 3b, we achieved a good linearity for a power dynamic range over 40 dB. The low dark current allows reliable photodetection down to sub-microwatt levels.

### 2.3. Dynamic Response Characterization

The dynamic response of the heterogeneously integrated PD was first characterized by an impulse response measurement using a femtosecond fiber laser with a pulse width of 600 fs and a repetition rate of 100 MHz. A bias voltage ( $-1$  V) was applied through a 50-GHz RF probe connected to a bias-tee. The output signal was collected by a digital sampling oscilloscope with a 63-GHz electrical bandwidth (up to 5.6-ps rise time). At a bias voltage of  $-1$  V, the measured full width at half-maximum (FWHM) of the pulse response was 12.5 ps and the 10%~90% rise time was 8.9 ps (as shown in the inset of **Figure 4a**). The fast Fourier transform of the temporal response, after padding the signal with zeros up to 20 ns to extend the frequency range, is shown in Figure 4a. After de-embedding the frequency responses of the external RF cables, bias-tee and RF probe, the 3-dB bandwidth was estimated to be  $\sim 52$  GHz.

The total 3-dB bandwidth was also theoretically estimated as a function of the PD's intrinsic layer thickness, as shown in Figure 4b (see "Experimental Section/Methods" for more details). There are two main factors which limit the total 3-dB bandwidth ( $f_{3dB}$ ) of the p-i-n PD: (1) the drifting time for the carriers to transit across the intrinsic absorption layer, and (2) the RC time constant from an inherent resistance and capacitance of the p-i-n structure. When the intrinsic layer is thin (i.e.,  $< 310$  nm), the RC time constant (blue dotted curve in Figure 4b) is the dominant factor determining the total  $f_{3dB}$  (black solid curve). Otherwise,  $f_{3dB}$  is transit time-limited (red dotted curve). Consequently, according to the 400-nm thick InGaAs intrinsic layer, the total  $f_{3dB}$  of the fabricated PD is estimated at  $\sim 58$  GHz. The slight deviation of  $f_{3dB}$ , compared

to the measured value ( $\sim 52$  GHz), is attributed to the asymmetrically longer fall time caused by the diffusion current. Since the vertical electrical contact structure produces strong electric fields in the intrinsic layer, photo-generated carriers can drift faster than those in the conventional heterogeneously integrated devices with mesa-type electrical contacts. Thus, the shorter transit distance and smaller series resistance contribute to a higher opto-electrical bandwidth.

We also evaluated the performances of the integrated PD device by using a 50-Gb/s on-off keying (OOK) signal. The detailed measurement configuration and reference transmitter eye diagram can be found in the Supporting Information (Figure S3). Figure 4c shows the measured eye diagram by using the integrated PD device. In this measurement, the extinction ratio of the input OOK signal was set to be  $\sim 8$  dB. The clear eye opening demonstrates high-quality digital data reception performance at 50 Gb/s. We repeated the same experiment by using a lower-rate 40-Gb/s OOK signal having a smaller extinction ratio of only  $\sim 2.7$  dB (Figure 4d). Its eye opening was less clear because an external electrical amplifier with a noise figure of 6 dB and the impedance mismatching between the PD device and the amplifier should reduce signal-to-ratio. This device could be used with the on-chip Si-based intensity modulators (which have relatively small signal swings).

### 3. Conclusion

The heterogeneous integration of high-bandwidth InGaAs-based p-i-n PDs on Si-based PICs has been experimentally demonstrated using a microbubble-based optofluidic assembly process. Our accurate and simple pick-and-place method enables vertical electrical contact configuration with low-temperature post-fabrication processes ( $<120$  °C). An important advantage of the proposed technique is that it does not require stringent fabrication requirements (e.g., surface flatness and lattice matching), compared to the conventional wafer/die bonding hetero-epitaxial direct growth techniques. Moreover, the microscale III-V semiconductor objects themselves have a high photothermal conversion efficiency, and additional heating structures and electric



sources are not necessary for real-time optofluidic manipulation. The integrated PD shows a dark current of  $\sim 2$  nA ( $\sim 6.4 \times 10^{-4}$  A/cm<sup>2</sup>) at a reverse bias of 1 V and a high linearity over a wide dynamic range down to sub-microwatt incident power levels. This electrical configuration is also found to be superior in terms of the series resistance and carrier transit distance/time, compared to the typical mesa structure commonly employed for conventional heterogeneous integration techniques. An opto-electrical 3-dB bandwidth of  $>50$  GHz and 50-Gb/s OOK signal reception have been realized at the bias voltage of  $-1$  V. The proposed optofluidic manipulation approach has a relatively low yield, but it is suitable for the in-situ heterogeneous integration of various materials and devices (e.g., light sources, modulators, and detectors) on diverse chip-scale PIC platforms. We have used single light beam-based operation in this study, but, by employing independent actuation of many entities in parallel or by cooperative manipulation<sup>[21]</sup> for high-throughput assembly, we believe that our simple yet effective optofluidic manipulation method can help the development of the high-performance heterogeneously integrated photonic/electronic platforms.

## 4. Experimental Section/Methods

### 4.1 Device fabrication

The device fabrication started with epitaxial growth of Indium gallium arsenide (InGaAs) on an indium phosphide (InP) substrate by molecular beam epitaxy, which has direct bandgap properties and relatively large absorption coefficients over a broad near-infrared wavelength range. The III-V epitaxial layer structure consists of an intrinsic In<sub>0.53</sub>Ga<sub>0.47</sub>As bulk crystal layer with a thickness of 400 nm for an absorption layer, sandwiched between 50 nm thick highly Si- and Be-doped ( $\sim 3 \times 10^{19}$ /cm<sup>3</sup>) InGaAs. Before defining the microdisk-shaped PD structure, circular Ti ( $\sim 10$  nm)/Au ( $\sim 90$  nm) metal electrode layers were patterned on the p-type InGaAs layer (Figure S1a). The circular microdisk pattern was defined by typical photolithography and bromic acid (HBr)-based wet chemical etching (Figure S1b). The etched devices were finally

released by selectively etching the InP substrate with diluted hydrochloric acid (Figure S1c), and subsequently immersed in deionized water.

SOI rib waveguides and assembling pedestal positions (referred to below as supporters) for the III-V PD device, which have a Si device layer thickness of ~400 nm, an etch depth of ~250 nm, and a waveguide width of ~450 nm are defined through standard electron beam lithography and inductively coupled plasma reactive ion etching (ICP-RIE) as shown in Figure S1d. Surface grating couplers at the end of the waveguides were fabricated for fiber-to-waveguide light input/output measurements. After a ~2 μm-thick SiO<sub>2</sub> layer deposition on top of the whole chip for passivation, the SiO<sub>2</sub> overcladding in the areas of waveguides and supporters were selectively removed by a combination of RIE dry-etching and buffered oxide etch (BOE)-based wet-etching steps (Figure S1e). Ti (20 nm)/Au (180 nm) metal layers for bottom electrodes were deposited on the supporter areas using thermal evaporation in combination with a lift-off process (Figure S1f), and this thickness of the metal layers controls the vertical gap between the integrated III-V PD and the Si waveguide for efficient light coupling. After the microbubble-based assembly process (Figure S1g), a SiO<sub>2</sub> dielectric layer was deposited on top of the assembled components at a relatively low temperature (~100°C) to minimize interfacial metal diffusion. Vias were subsequently opened by BOE-based wet-etching. Finally, thick Ti (~20 nm)/Au (~1.2 μm) metal layers were deposited for the metal plugs and the probe pads as shown in Figure S1h.

#### 4.2 Theoretical estimation of 3-dB bandwidth

The total 3-dB bandwidth ( $f_{3dB}$ ) can be theoretically calculated by<sup>[32]</sup>

$$\frac{1}{f_{3dB}} = \sqrt{\left(\frac{1}{f_{tr}}\right)^2 + \left(\frac{1}{f_{RC}}\right)^2} = \sqrt{\left(\frac{t}{0.45v}\right)^2 + \left(\frac{2\pi\epsilon_0\epsilon_r AR}{t}\right)^2}$$

where  $f_{tr}$  and  $f_{RC}$  indicate the transit-time-limited and capacitance-limited bandwidths, respectively.  $A$ ,  $t$ ,  $v$ ,  $R$ ,  $\epsilon_r$ , and  $\epsilon_0$  stand for the metal electrode area (~25π μm<sup>2</sup>), InGaAs absorption layer thickness (400 nm), carrier drift velocity (~6×10<sup>6</sup> cm/s), series resistance (58.7

$\Omega$ ), relative dielectric constant (13.9), and vacuum dielectric constant ( $8.854 \times 10^{-12}$  F/m), respectively.

### Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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### Conflict of Interest

The authors declare no conflict of interest.

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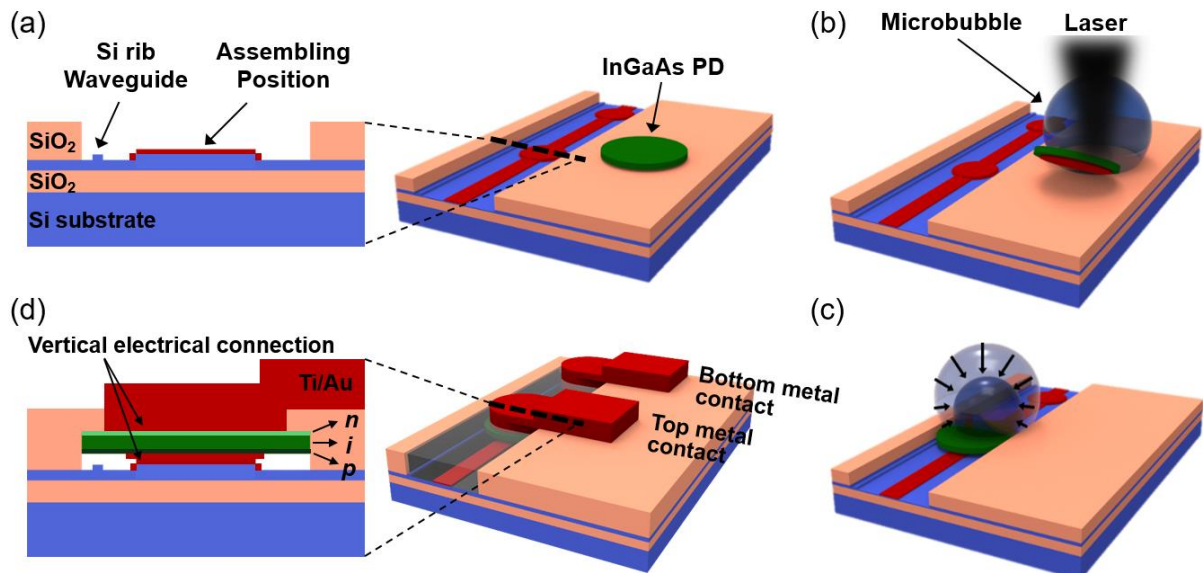
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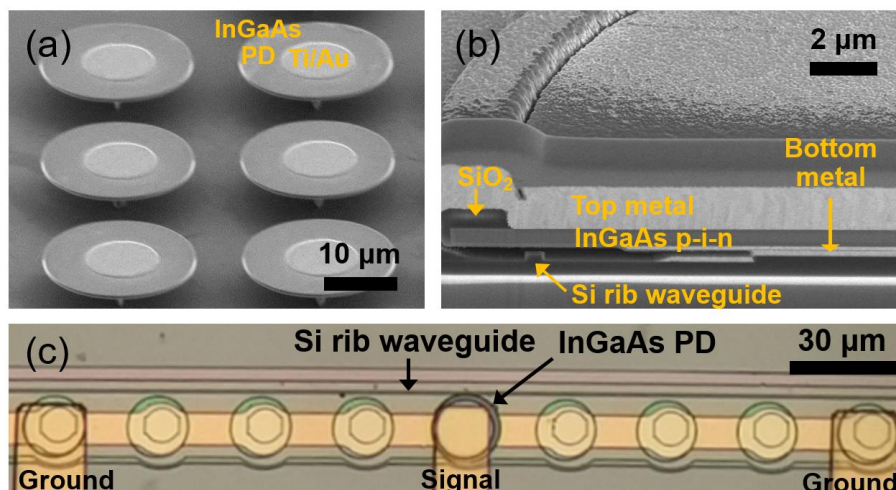
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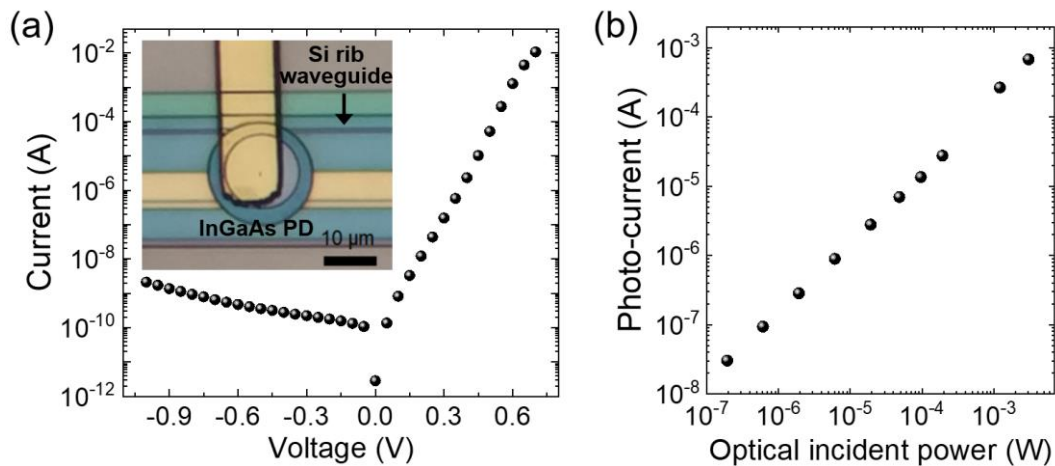
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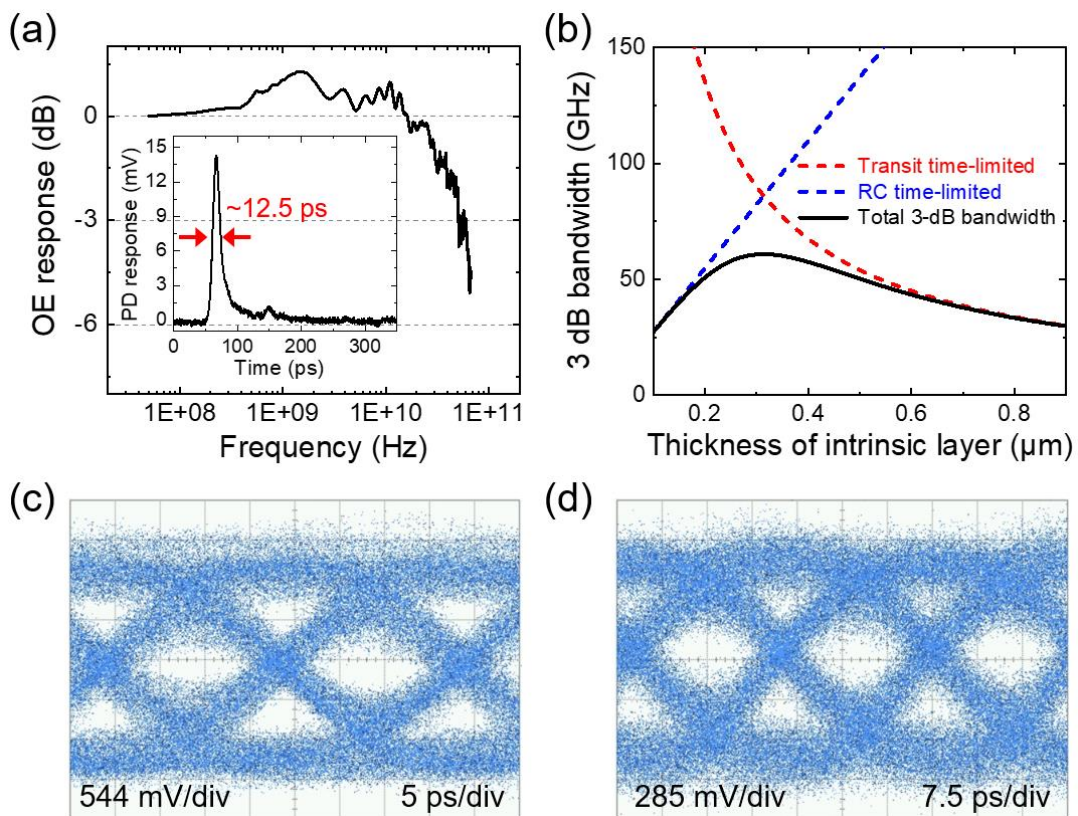
**Figure 1.** a) Cross-sectional and perspective view illustration of a Si rib waveguide (blue color), SiO<sub>2</sub> cladding layers (apricot color), and assembling positions with a thin bottom metal contact layer (red color). b) and c) Pick-and-place assembly process of an InGaAs PD (green color) on the pedestal position using the microbubble-based optofluidic manipulation technique. (The aqueous solution is not illustrated.) d) Final structure after the top passivation and metallization process, showing the cross-sectional vertical electrical contact configuration. (Part of the top passivation layer is shown as transparent for illustrational purposes.)



**Figure 2.** a) SEM image of the unreleased InGaAs PD array with the metal contact layer on the partially etched InP pedestal. b) Cross-sectional SEM image of an InGaAs PD integrated on the Si rib waveguide with the vertical electrical connection. c) Optical microscope image of an InGaAs PD integrated onto a Si waveguide.



**Figure 3.** a) Log-scale I-V curve without light input. The inset shows the magnified top view of a fabricated device. b) Photo-response under different optical incident power levels at an applied bias voltage of  $-0.3$  V.



**Figure 4.** a) PD opto-electronic (OE) response. The inset shows the measured impulse response of the integrated PD device by using a femtosecond laser. b) Theoretically estimated RC- and

transit-limited 3-dB bandwidths as a function of the thickness of the InGaAs PD's intrinsic layer. c) Measured eye diagram (inner eye width: ~10 ps, height: ~640 mV) from the integrated PD for a 50 Gb/s digital signal with an extinction ratio of ~8 dB at an input wavelength of 1.55  $\mu\text{m}$ . d) Measured eye diagram (inner eye width: ~12 ps, height: ~365 mV) for a 40 Gb/s digital signal with an extinction ratio of ~2.7 dB. In these measurements, the bias voltage of the PD device was set to be  $-1$  V.