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Adaptive Tuning of Resonant Inductive Power and Communication Links

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Research Thesis: Declaration of Authorship

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Abstract

Resonant inductor-capacitor (LC) circuits with high quality factors are required to efficiently generate large magnetic fields for transmitters in wirelessly-powered communication applications. The narrow bandwidth from such high quality factor circuits necessitates accurate tuning of the resonator, requiring multiple tuning capacitors and additional circuitry, incurring greater manufacturing costs due to the need for greater board and die area, as well as a greater number of high-voltage switches needed to withstand the high capacitor voltage caused by the high quality factor. Furthermore, the narrow bandwidth of the resonant circuit impedes fast data transmission to the receiver, resulting in a trade-off between power transfer efficiency and data bandwidth.

This work explores a new topology and timings for tuning large-signal LC circuits, whereby only a single additional capacitor is needed to achieve accurate and wideband tuning. This method of zero-voltage switched fractional capacitance is low-loss and synchronous with the resonator oscillation. The need for only a single tuning capacitor significantly reduces system costs by reducing the amount of high-voltage circuitry required. The new tuning method also permits easy detection of the resonant condition, allowing for low system complexity for a self-tuning architecture. The tuning method also facilitates synchronous adjustment of the resonant and operating frequency, presenting the opportunity for frequency and phase modulation at data rates exceeding the classical limitations due to the antenna quality factor.

This report consists of five primary sections: literature review; analysis, simulation and implementation of the new tuning method using LTSpice and discrete components; implementation of the tuning method in an integrated circuit; using the tuning method to achieve synchronous frequency/phase modulation without energy loss from the antenna; and implementation of the modulation method in an integrated circuit.

The initial simulations and breadboarding provide insight into the system-level challenges, however the main benefits of the tuning method are best realised in integrated form, with all system functions on a single silicon die. Translating the basic tuning and modulation concepts into self-contained integrated systems involves considerable amounts of design effort, as well as additional challenges to overcome and trade-offs to make. The first integrated circuit explores the basic tuning method and resonance-detection, and how to combine high-speed timing generation and tuning error detection with on-chip antenna drivers and tuning switches. The second integrated circuit includes new system-level architecture to achieve frequency/phase shift modulation, with new architecture developed to achieve precise modulation.

1 Introduction

1.1 Motivation

Wirelessly-powered communication (WPC) is becoming an increasingly attractive way to power devices and machinery without mechanical contact. This may either be done for safety reasons where high voltages are involved, or convenience reasons such as contactless payment systems and Radio Frequency Identification (RFID). With the latter and increasingly the former, there is also a need to transfer information between the source and sink of power, either for power control information or for other data requirements. As devices become more complex, more data transfer is required and hence more bandwidth. However, a higher bandwidth can conflict with the conditions of high-efficiency wireless power transfer, i.e. high Q and low bandwidth.

High Q circuits are also more susceptible to the effects of detuning, which may move the resonant frequency of the LC circuit far enough so that the amplitude of oscillation is significantly reduced, hence the inductor current (and hence magnetic field strength) is reduced. Detuning may be caused by both component tolerances and variation with temperature, as well as by parasitic capacitances and inductances introduced during operation. It is therefore essential that a WPC system can be tuned to counteract these effects to ensure maximum power transfer.

The requirements of high bandwidth and high Q factor are typically subject to a trade-off so that the same carrier may be used for both data and power transfer purposes. Alternatively, different frequencies may be used for wireless power and data transfer respectively, incurring an additional spectrum usage cost as well as system complexity. A third alternative is to retune the resonant circuit used for wireless power to allow wider data bandwidth whilst ensuring that the circuit is still delivering the optimum power level. This third option requires a form of rapid, dynamic tuning, a method for which is presented in this report. Patents on the system-level architecture for tuning and frequency modulation have been granted [1][2].

1.2 Research goals and contributions

The primary aim of this research is to implement the new tuning method of inductor-capacitor (LC) circuits into an integrated circuit (IC), firstly to tune the high-Q LC circuit to resonance and secondly to modulate the oscillation for frequency shift keying (FSK) and phase shift keying (PSK). The tuning method must be first analysed and simulated, followed by the construction of a discrete circuit board to understand the system-level operation and limitations. Additional challenges of IC implementation are faced, with key research contributions made to overcome them:

- Creation of a mixed-signal architecture to provide on-chip antenna drivers and tuning switches alongside fast and accurate timing references, using a commercially-available IC process [3].
- Re-arrangement of the ideal switched fractional capacitance circuit topology to avoid the need for an ideal high-voltage bi-directional switch [3].
- Development of a method to safely sense the resonant condition on the high-voltage switch excursions required for tuning [3].
- Creation of a method of timing reference phase trimming to compensate for systematic time delays which cause non-symmetrical switching of the tuning capacitors [4].
- Modifying the existing mixed-signal timing generation circuitry to permit accurate control of frequency modulation to minimise losses in the antenna circuit, overcoming the classical trade-off between high-Q factor and high data bandwidth [5].
- The creation of an adaptive frequency calibration method to achieve precise phase modulation by means of a controlled temporary frequency shift.

1.3 List of publications

1.3.1 Principal project publications

1) H.R.B. Kennedy et al., "Continuous Tuning of Inductive Link Antennae with Zero Voltage Switched Fractional Capacitance", IEEE 59th International Midwest Symposium on Circuits and Systems (MWSCAS), October 2016

2) W. Redman-White et al., "Adaptive Tuning of Large-Signal Resonant Circuits Using Phase-Switched Fractional Capacitance", IEEE Transactions on Circuits and Systems II: Express Briefs (T-CAS II), Volume 64, Issue 9, pp. 1072-1076, November 2016

3) Henry Kennedy et al., "A self-tuning resonant inductive link transmit driver using quadrature-symmetric phase-switched fractional capacitance", IEEE International Solid-State Circuits Conference (ISSCC), pp. 370-371, February 2017

4) Henry Kennedy et al., "A Self-Tuning Resonant-Inductive-Link Transmit Driver Using Quadrature Symmetric Delay Trimmable Phase-Switched Fractional Capacitance", IEEE Journal of Solid-State Circuits (JSSC), Volume 53, Issue 6, pp. 1694-1706, March 2018

5) Henry Kennedy et al., "A High-Q Resonant Inductive Link Transmit Modulator/Driver for Enhanced Power and FSK/PSK Data Transfer Using Adaptive-Predictive Phase-Continuous Switching Fractional-Capacitance Tuning", IEEE International Solid-State Circuits Conference (ISSCC), February 2019

1.3.2 Related project publications

1) T. Lee et al., “A CMOS MF energy harvesting and data demodulator receiver for wide area low duty cycle applications with 230 mV start-up voltage”, IEEE Nordic Circuits and Systems Conference (NORCAS), November 2016

2) T. Lee et al., “An MF Energy Harvesting Receiver with Slow QPSK Control Data Demodulator for Wide Area Low Duty Cycle Applications”, IEEE 44th European Solid State Circuits Conference (ESSCIRC), September 2018

2 Literature Review

This chapter details the background theory behind WPC and why highly-resonant circuits are needed. The requirement for accurate tuning of these circuits is then introduced, followed by the current state-of-the-art in tuning techniques.

2.1 Wirelessly Powered Communication (WPC) Overview

WPC is the transfer of power and information between devices entirely by wireless means, typically using magnetic fields or electromagnetic radiation [6]. Devices being powered may range from small sensors and actuators to heavy industrial machinery [7]. This project will focus on near-field inductive coupling.

2.1.1 Principle of inductive coupling

At its simplest, inductive coupling relies on Faraday's law of induction:

$$\nabla \times E = -\frac{\partial B}{\partial t} \tag{2.1}$$

Faraday's law of induction [8]

which states that an electromotive force (EMF) E will be generated in a conductor by a rate of change in magnetic flux B with respect to time [9]. From equation 2.1, the magnetic flux must continually change in order to provide a continuous electromotive force. The classical method of achieving this is a sinusoidal waveform, since the derivative and integral of a sine wave is another sine wave with a 90^{O} phase offset. I.e. a sinusoidal voltage of constant amplitude will be induced by a sinusoidal magnetic field.

In order to transfer power using inductive coupling, two coils may be used, the "primary" at the transmitter and "secondary" at the receiver. In the context of WPC the secondary may also be referred to as the "pickup". To increase the amount of EMF induced into the secondary coil, both must be aligned as closely as possible so that the maximum flux from the primary is captured by the secondary. The efficiency of transfer of flux is described in terms of a coupling coefficient k, taking a value between 0 and 1. Whilst tightly-wound transformers may have $k > 0.8$, WPC applications can experience $k < 0.1$ due to the typically poor alignment between the primary and secondary coils [10].

A lower value of k results in a lower voltage being induced into the pickup coil. For a given amount of power transfer, a higher magnetic field is required at the transmitter, hence a larger current is required, increasing the power dissipated due to ohmic losses. In high power applications such as vehicle charging, the total power dissipation may become uneconomic. In some applications such as medical implants, heating due to ohmic losses must be controlled for patient safety reasons [11]. Hence it is preferable to reduce the inductor resistance for lower power losses.

2.1.2 Principle of LC resonance

A common method of implementing inductive WPC transmitters is by means of a resonant inductor-capacitor (LC) circuit. Figure 2-1 shows the typical model of an LC circuit, including a component to model resistive losses.

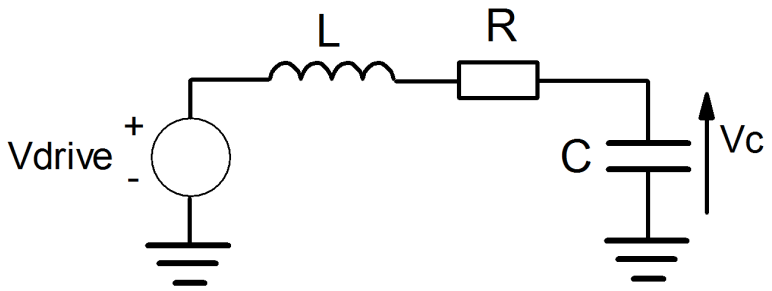

Figure 2-1: Example LC circuit model with losses modelled as a series resistance R.

The LC circuit will resonate because of energy being transferred back and forth between the magnetic field in the inductor and the electric field in the capacitor. This may be demonstrated by the time domain solution of the circuit. Considering an un-driven LC tank, the relation between the voltages and currents in the components are:

$$i_c(t) = C\frac{dv_c}{dt} \tag{2.2}$$

$$i_r(t) = \frac{v_r(t)}{R} \tag{2.3}$$

and

$$v_l(t) = L\frac{di_l}{dt} \tag{2.4}$$

hence

$$\frac{dv_l}{dt} = L\frac{d^2i_l}{dt^2} \tag{2.5}$$

Due to Kirchhoff's voltage law, the voltage across the three components adds up to zero, so

$$L\frac{d^2i_l}{dt^2} + R\frac{di_r}{dt} + \frac{1}{C}\,i_c(t) = \frac{d^2i_l}{dt^2} + \frac{R}{L}\frac{di_r}{dt} + \frac{1}{LC}\,i_c(t) = 0 \tag{2.6}$$

The general solution for equation 2.6 is given by equation 2.7, where $\alpha = \frac{R}{2L}$ and $\omega = \frac{1}{\sqrt{LC}}$

$$i(t) = e^{-\alpha t}[A\cos(\omega t) + B\sin(\omega t)] \tag{2.7}$$

If the initial condition is assumed such that $i(0) = I_0$ and $\frac{di}{dt}\Big|_{t=0} = 0$ (i.e. there is some energy already stored in the tank) then

$$\frac{di}{dt} = -A\omega\sin(\omega t) + B\omega\cos(\omega t) = 0 \tag{2.8}$$

hence $B = 0$, hence $A = I_0$. If there are no resistive losses, then the expression for the time domain response of the circuit is

$$i(t) = I_0\cos(\omega t) \tag{2.9}$$

E.g. an LC circuit will oscillate with a sinusoidal response, with a frequency of $\omega = \frac{1}{\sqrt{LC}}$. A lossless LC so-called "tank" would oscillate forever, but in practice there are resistive losses in the inductor, meaning that a continuous drive is needed to maintain oscillation. Losses may also be incurred by the

capacitor, for example in the resistance of the connecting leads, but these effects are usually small compared with those of the inductor.

The ratio of energy stored to the energy dissipated per cycle is defined as the quality or "Q" factor. The Q factor can also be related to the ratio between the resonant frequency and the 3dB bandwidth, as per equation 2.10.

$$Q = \frac{2\pi f \varepsilon_{stored}}{P_{dissipated}} = \frac{2\pi f L}{R} = \frac{1}{R}\sqrt{\frac{L}{C}} = \frac{f_c}{\Delta f} \tag{2.10}$$

where f_c is the centre frequency of the LC circuit and Δf is the 3dB bandwidth [12]. The higher the Q factor, the more energy stored in the LC tank. For a given amount of energy delivered per cycle, the amplitude of oscillation will therefore take longer to reach a maximum value and will take longer to decrease once the drive is removed.

The Q factor is an important consideration in the context of WPC, because the voltage and current in the LC tank, and hence magnetic field, are a function of the input drive level and the Q factor. Considering the driven RLC circuit in figure 2-1, the magnitude of the capacitor voltage may be defined:

$$\left|\frac{V_c}{V_{drive}}\right| = \left|\frac{Z_c}{R + Z_L + Z_c}\right| = \left|\frac{\frac{1}{j\omega C}}{R + j\omega L + \frac{1}{j\omega C}}\right| = \left|\frac{1}{j\omega RC - \omega^2 LC + 1}\right| \tag{2.11}$$

At resonance, $\omega = \frac{1}{\sqrt{LC}}$, so

$$\left|\frac{V_c}{V_{drive}}\right| = \left|\frac{1}{\frac{jRC}{\sqrt{LC}}}\right| = \frac{1}{R}\sqrt{\frac{L}{C}} = Q \tag{2.12}$$

Note that at resonance there is only a negative imaginary component left. This means that the phase angle between the drive voltage and capacitor voltage is a lead of 90 degrees. Note that V_c and V_{drive} represent root mean square (RMS) values, as it assumed that sinusoidal signals are being used.

It then follows that the series current, and hence the inductor current, must also be related to the Q factor. The voltage across the resistor Vr may be expressed in terms of V_{in}, so at resonance (i.e. $\omega = \frac{1}{\sqrt{LC}}$) :

$$\left|\frac{V_r}{V_{drive}}\right| = \left|\frac{R}{R + Z_L + Z_c}\right| = \left|\frac{j\omega RC}{j\omega RC - \omega^2 LC + 1}\right| = 1 \tag{2.13}$$

and hence the circulating current in the tank may be defined in terms of the resistance and the input drive level:

$$I_{tank} = \frac{V_{drive}}{R} \tag{2.14}$$

Since the intention is to maximise magnetic field strength, the RMS inductor current must be maximised, hence tank resistance must be minimised. Therefore, a high Q factor is preferable in order to maximise power transfer.

High-Q LC circuits also allow for simpler drive circuitry for multiple reasons. Firstly, the linear relation between the RMS drive voltage and inductor current means that a larger Q factor provides a larger magnetic field for a given drive voltage. A lower drive voltage allows for smaller and faster transistors

in the driver than would otherwise be needed to stand-off a higher drive voltage, hence system cost is reduced.

Secondly, equation 2.10 implies that a high Q circuit will have a narrow bandwidth. This means that any driving signal with a frequency which deviates significantly from the resonant frequency shall be attenuated. This permits the use of a square wave drive to the LC tank, allowing the use of simpler and more efficient drive circuitry compared with that needed for a sinusoidal drive. If the Q is high enough, the harmonics will be filtered and the current drawn by the LC tank will be essentially sinusoidal.

As has been shown, it is preferable to have a high Q factor tank for effective wireless power transfer. By equation 2.10, the Q factor can be increased by using an inductor design which achieves the required inductance with a lower loss resistance. The design considerations of high-Q factor inductors are covered in appendix A.

2.1.3 Principle of Magnetic Resonant Coupling

As mentioned in section 2.2.1, some applications of WPC involve low coupling factors, leading to low power transfer and potentially lower system efficiency. In a system where both the transmitter and receiver utilise LC tank circuits with equal resonant frequencies, high Q factors may be used to counteract the performance degradation due to low k [13].

The high Q factor of the primary LC tank means that it may have a very strong magnetic field around it. Since the secondary tank also has a high Q factor, a larger EMF is induced from the smaller available magnetic field, compensating for the reduction in coupling factor. Given both tank circuits are at the same resonant frequency, no energy will be dissipated due to attenuation of non-resonant frequency oscillations. This means that WPC by magnetic resonant coupling can operate over a much larger distance than non-resonant coupling [14][15][16]. In [15], a magnetic resonant system was used to transfer 60W wirelessly over a 2m air gap.

An ideal magnetically-resonant coupled system is shown in figure 2-2. The coupling factor k defines a mutual inductance M, such that $M = k\sqrt{L_T L_R}$. The resonant frequencies of the transmit and receive loops are the same, although the particular inductance and capacitance may be different for each. When driven resonantly, the reactive components cancel, so the solution to the current mesh at the transmitter is given by equation 2.15.

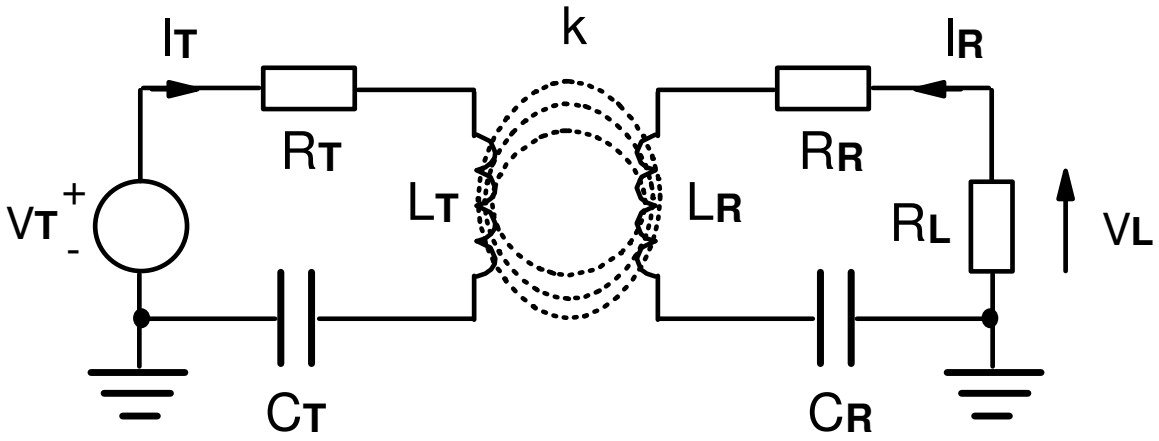

Figure 2-2: Magnetically-coupled circuit example

$$V_T = I_T\left[R_T + j\omega L_T + \frac{1}{j\omega C_T}\right] + I_R[j\omega M] = I_T R_T + I_R[j\omega M] \qquad (2.15)$$

And the current mesh at the receiver is given by:

$$0 = I_R\left[R_R + R_L + j\omega L_R + \frac{1}{j\omega C_R}\right] + I_T[j\omega M] = I_R(R_R + R_L) + I_T[j\omega M] \tag{2.16}$$

Hence:

$$I_T = \frac{-I_R(R_R + R_L)}{[j\omega M]} \tag{2.17}$$

The power transfer efficiency is denoted as η and is given by the magnitude of the ratio of output power $P_L = I_R^2 R_L$ over the input power $P_T = V_T I_T$, i.e. :

$$P_T = I_T^2 R_T + I_R I_T[j\omega M] = R_T\left(\frac{I_R(R_R + R_L)}{j\omega M}\right)^2 - I_R^2(R_R + R_L) \tag{2.18}$$

Substituting in the expression for the mutual inductance, the efficiency η may be expressed as:

$$\eta = \left|\frac{P_L}{P_T}\right| = \frac{I_R^2 R_L}{R_T I_R^2\left(\frac{R_R + R_L}{j\omega M}\right)^2 - I_R^2(R_R + R_L)} = \frac{R_L}{\frac{R_T(R_R + R_L)^2}{\omega^2 k^2 L_T L_R} + (R_R + R_L)} \tag{2.19}$$

The inductances, resistances and operating frequency can be replaced with the respective Q factor expressions for each loop, hence:

$$\eta = = \frac{R_L}{(R_R + R_L)\left[\frac{1}{k^2 Q_T Q_R} + 1\right]} = \frac{R_L}{(R_R + R_L)}\frac{k^2 Q_T Q_R}{1 + k^2 Q_T Q_R} \tag{2.20}$$

Hence the power transfer efficiency may be increased by increasing the Q factor, compensating for a small coupling factor. Note that if the inductive antenna at the receiver is sufficiently high quality, then $R_R \ll R_L$, hence:

$$\eta = \frac{k^2 Q_T Q_R}{1 + k^2 Q_T Q_R} \tag{2.21}$$

Figure 2-3 shows graphically how the efficiency approaches 100% as the Q factors are increased, for various values of k.

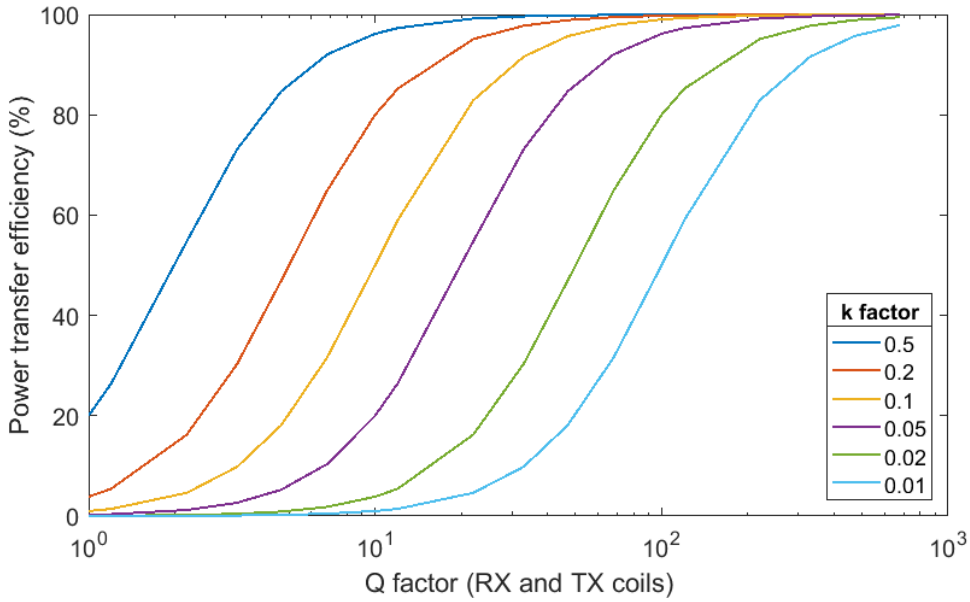

Figure 2-3: Efficiency of magnetic resonance coupling with varying Q factor, for different k factors

An interesting phenomenon known as frequency splitting must also be considered where highly-resonant systems are used. Consider a system with a primary and secondary LC circuit with identical resonant frequencies. As the coupling factor is increased (i.e. the inductors are brought closer into magnetic alignment), the increased mutual inductance between the two systems results in two independent resonant frequencies being created [17].

Figure 2-4 shows how the effect of frequency splitting on the frequency response of $|V_c|$ as the coupling factor k is varied. For loosely coupled systems, this phenomenon has a negligible effect. For the purposes of this work, the frequency splitting effect due to high coupling with a resonant load circuit will be considered as a detuning effect, i.e. the transmitter circuits must be adjusted so that the circuit can continue to resonate when driven at the intended operating frequency.

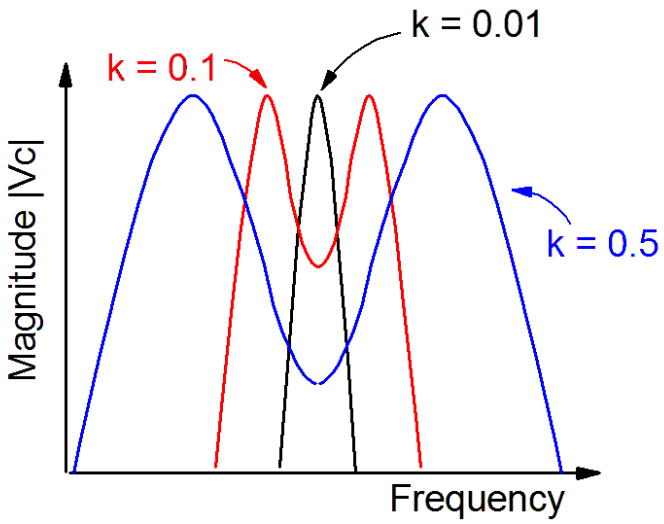

Figure 2-4: Frequency splitting phenomenon for highly-resonant LC circuits: the two resonant frequencies increase in distance as k increases (reproduced from [17])

2.1.4 Q Factor vs Bandwidth

It is desirable to be able to transfer data as well as power wirelessly. Applications range from RFID and smartcards where the receiver has no auxiliary power, to high-power transfer systems such as vehicle charging, where it may be desirable to have power control information sent wirelessly. Data may be transferred by modulating the amplitude, phase or frequency of the oscillating magnetic field used for power transfer.

Regardless of the modulation used, the desired data bandwidth must exist within the 3dB bandwidth of the resonant LC circuit used for power transfer, otherwise the data will be corrupted. It has been previously discussed that high-Q LC circuits are preferable for efficient wireless power transfer, however the resulting narrower bandwidth reduces the maximum rate of data transfer. Hence, a trade-off exists between the desired Q factor and the desired data transfer rate.

The most common example of data modulation is Amplitude Shift Keying (ASK) where the modulation index is unity, i.e. the data is represented by switching the carrier oscillation on and off. This mode is also known as On-Off Keying (OOK) and is used in ID products such as MIFARE [18]. Figure 2-5 shows the effect of OOK on the inductor current in a low-Q and high-Q resonant LC circuit. The high-Q circuit is capable of storing more energy since it has by definition fewer losses. This results in a greater amount of time taken for changes in amplitude to become manifest, resulting in a lesser distinction between the '0' and '1' amplitudes and hence a greater probability of incorrect detection. In frequency terms, the sidebands of the amplitude modulation must be closer to the carrier for error-free data transfer.

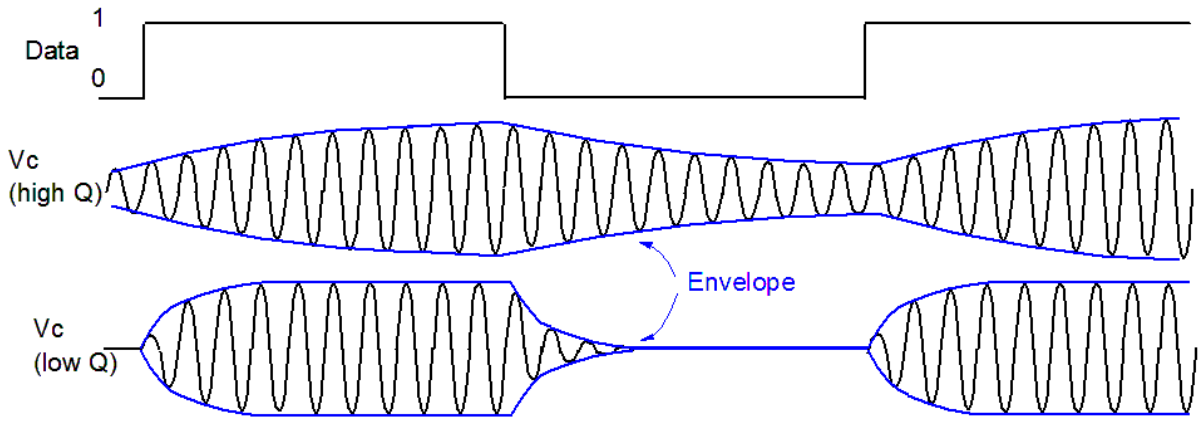

Figure 2-5: The effect of OOK on inductor current for a low-Q and high-Q LC circuit

A similar effect is observed for Phase Shift Keying (PSK) modulation. Although the carrier frequency remains the same, PSK modulation results in an instantaneous phase change of the driver to the LC tank. Such an instantaneous phase change requires very high bandwidth, which is not available due to the high-Q LC circuit. The resulting behaviour is a gradual change in phase of the inductor current, limited by the Q factor.

For reliable detection at the receiver, the driver phase at the transmitter cannot be permitted to change again until the oscillating inductor current is correctly aligned with the driver, hence the data transfer rate in PSK is limited by the Q factor. The most extreme case is where the phase is changed by 180 degrees, also known as Binary Phase Shift Keying (BPSK). Smaller changes in phase may be used in order to reduce the time needed for inductor current phase alignment, however these require more complex detectors at the receiver, increasing power consumption.

Data modulated by Frequency Shift Keying (FSK) is also limited by the Q factor. The data bandwidth must exist within the acceptable bandwidth of the LC circuit, otherwise it will not correctly propagate to the receiver and hence data will be lost. The mark and space frequencies must also exist within the 3dB bandwidth so that a large inductor current is maintained, by keeping the drive frequency close to the resonance frequency of the LC antenna.

One solution to this problem is to use completely separate bands for power and communications. One such example is the typical implementation of remote keyless entry systems for cars, where the uplink from the car to the key operates in the UHF band [19]. This allows for any desired communications standard to be used as data bandwidth in the uplink direction is no longer restricted by the requirements of power transfer. However, the usage of entirely separate systems for power transfer and communication increases the complexity and therefore cost of the system. Furthermore, the increasing amount of wireless communication taking place in general necessitates the most efficient use of the frequency spectrum wherever possible.

2.1.5 Effect of Tuning Mismatch

All discussion so far regarding LC circuits has assumed that such circuits are already correctly tuned to the desired frequency of operation. If this is not the case, then the coupling efficiency of the WPC system will be reduced, since a tuning offset will result in LC circuits being driven at non-resonant frequencies. The effect of tuning mismatch is shown in the diagram in figure 2-6. Ideally, the resonant bandwidth is centred around the intended antenna drive frequency for maximum current. Detuning effects cause the antenna resonant bandwidth to move so that this is no longer the case. The intersection between the detuned curves in red and the ideal drive frequency is at a point considerably below -3dB, hence the inductor current is significantly reduced and the ability to transfer power efficiently is hindered.

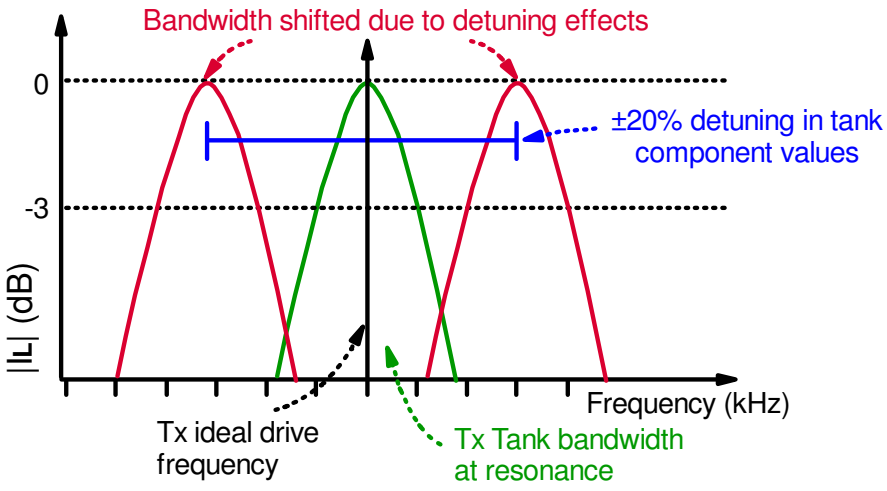

Figure 2-6: Effect of LC antenna circuit drive and resonant frequency mismatch due to detuning effects

Furthermore, the higher the Q factor, the better the matching needs to be between the drive and resonant frequencies, since the bandwidth is lower and therefore a fixed amount of frequency offset has a far greater penalty on transmitted power.

A numerical example demonstrates the need for accurate tuning. Ceramic capacitors which may be used in commercial discrete resonator circuits may have ±20% tolerance. For example, an LC circuit with a resonant frequency of 125kHz and Q factor of 50 will have a 3dB bandwidth of 2.5kHz (i.e. from 122.5-127.5kHz). Allowing for ±20% tolerance in the capacitors alone, the practical resonant frequency of the LC tank may be anywhere between 114.5kHz and 139.75kHz. Therefore, there is a high chance that two systems from the same manufacturing batch are likely to have resonant frequencies that are incompatible.

Post-manufacture detuning may increase detuning further. The inductor may be detuned by metallic structures nearby, especially ferromagnetic objects such as steel or iron pipes in buildings and machinery [20]. Temperature variations may also slightly modify the values of the passive components, resulting in further detuning [21]. The effect of resonant load detuning mentioned earlier will also contribute to the offset due to frequency splitting. For these reasons, practical WPC systems require a method of online self-tuning to compensate for detuning effects. Otherwise, optimal power transfer may not be achieved.

2.2 Tuning of resonant LC circuits

2.2.1 Static Tuning Methods

2.2.1.1 Variable Capacitance Techniques

The capacitance of a capacitor is determined by its physical dimensions and the relative permittivity of its dielectric. In most WPC applications it is not practical to adjust these parameters. For example, mechanically-adjusted plate capacitors are physically large and incur a cost due to moving parts. Some applications may however necessitate the use of mechanical tuning, for example when a high breakdown voltage is needed.

Tuning by electrical means may instead be achieved with a varactor. This is a variable capacitor whose value is controlled by an applied DC bias. Varactors may be made from PN junctions [22] or CMOS devices [23]. The varactor must remain reverse biased and the DC bias tuning voltage must be large compared to the amplitude of oscillation. This makes varactors useful for tuning low power oscillators in RF circuits (where the signal amplitude is small) but impractical for WPC resonant antennas where very large voltages are present on the capacitor.

Figure 2-7 shows the symbolic representation of a PN junction varactor and how it may be used in an LC circuit. A resistor is used to provide isolation from the tune voltage so that the DC bias across the varactor is set without significant loss of RF current. The varactor capacitance decreases as the tune voltage increases, due to the charge in the depletion region of the PN junction being pushed further apart, reducing the capacitance of the diode.

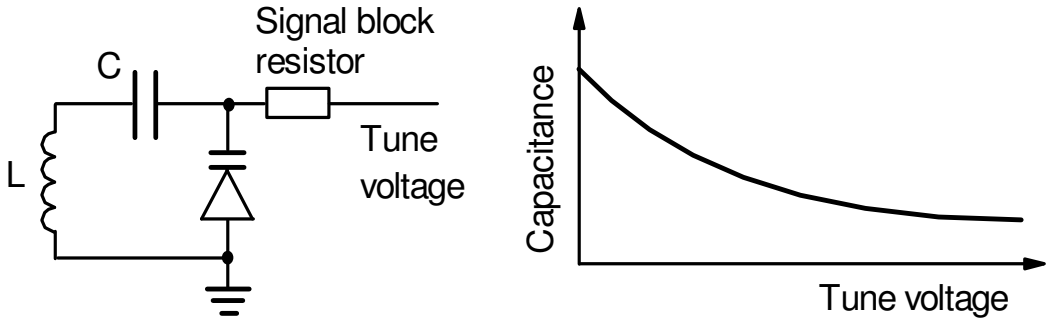

Figure 2-7: Varactor tuned circuit, using an analogue DC voltage. Adapted from [22]

Tuning may instead be achieved by choosing from a selection of available fixed capacitors, typically configured in a binary-weighted fashion as per figure 2-8. The tune setting is determined by a digital code, corresponding to the capacitor switches which may either add or remove them from the tuned circuit. Examples of such systems are given in [24], [25].

The desired tuning resolution determines how many capacitors are required. For the example system operating at 125kHz with a Q factor of 50, the 3dB bandwidth is 2.5kHz. In order to guarantee tuning to within this bandwidth, at least 5 binary-weighted capacitors are required. In practice, random mismatch between each capacitor may result in non-monotonicity and non-linearity in the tune range, hence it may be necessary to increase the number of capacitors to ensure that the resolution requirement can be met, depending upon the requirements and components available.

Furthermore, the switches for each capacitor must be able to withstand high voltages, since a high-Q LC circuit will have a large multiplicative effect on the capacitor voltage. Hence, switches that are open must be rated to withstand the peak voltage on the fixed capacitor. The switches also must be rated to carry the maximum inductor current when closed and have low resistive losses to prevent degradation in the Q factor. The capacitor switches may be implemented with discrete MOSFETs, or as on-chip devices. In both cases, adding more switches increases the size and cost of the system, as discrete FETs require more PCB space, whilst on-chip devices of useful capacitance require vastly more die area.

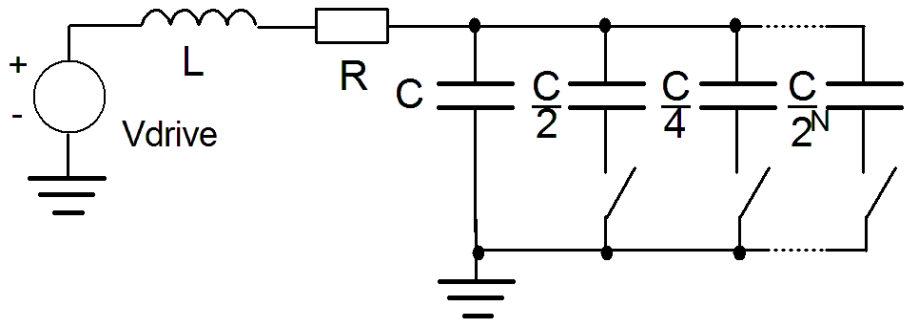

Figure 2-8: Binary capacitor bank tuning example.

Combinations of varactor and capacitor-bank tuning may also be used. In [26] a VCO is presented which uses such a combination, primarily to mitigate the problem of phase noise caused by the varactor. This particular scheme is aimed more at VCO applications, and may not be suitable without the

provision of a varactor which can withstand high voltages which may exist in a resonating LC tank in a WPC application.

2.2.1.2 Variable Inductance Techniques

In the context of WPC, it is preferable that the inductor remain at maximum value at all times in order to maintain a high Q factor for high power transfer. If however inductor tuning is desired it can be implemented in several ways. The first is using a bank of weighted inductors, in a similar manner to that used for binary weighted capacitors. The relative physical sizes of inductors may make such an option impractical.

Alternatively, a single inductor may be "tapped" at intervals. Tapping further along gives an increased overall inductance. The ability to perform this method of tuning may be limited by the desired shape of inductor, as factors such as the number of turns may limit the number of taps that can be practically used. Figure 2-9 shows symbolically how digital inductor tuning may be implemented.

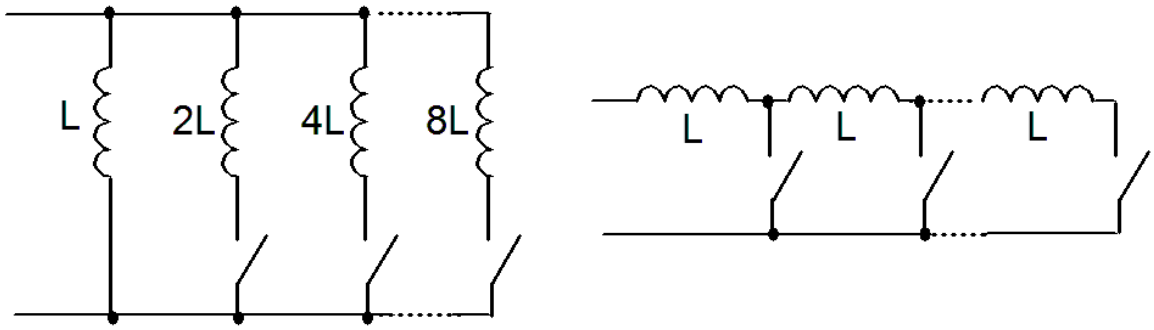

Figure 2-9: Digitally-tuneable inductor configurations. Left: Binary-weighted parallel inductances. Right: Summable series inductances

Another method to vary inductance is by partial cancellation of the magnetic field using a second inductor with some flux running in the opposite direction. The differential pair in figure 2-10 feeds back some of the output signal of the oscillator formed by L_2 and C_2, the amount of feedback is set by the input DC bias on $V_{control}$. This method of tuning is presented in [27] for VCO applications, however the method of cancelling the magnetic field is itself not desirable where the intention is to maximise this field, as is the case for wireless power systems. It is however a more interesting method of tuning an LC circuit and may allow for a much higher tuning resolution than the use of discrete inductor taps. The circuit is noted for having high control voltage – frequency linearity.

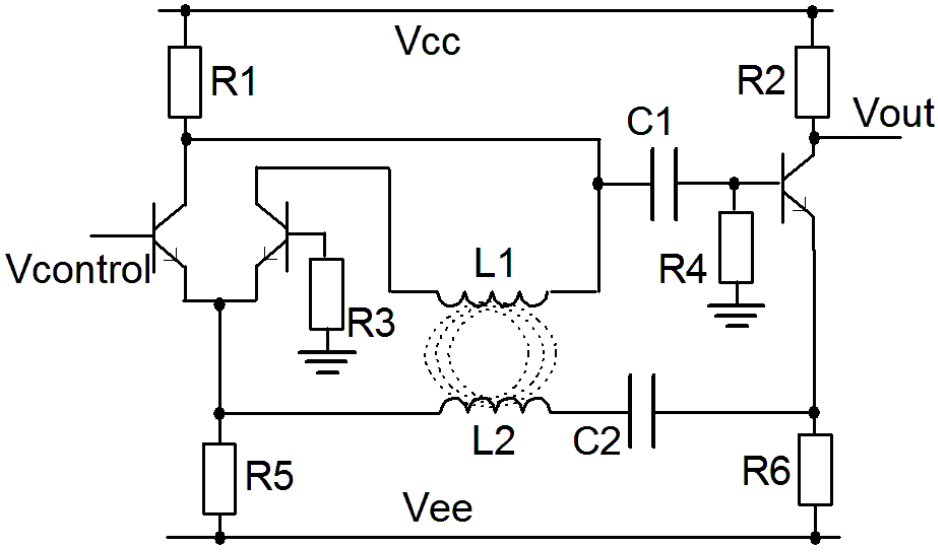

Figure 2-10: Johnson oscillator, utilising flux cancellation tuning. Reproduced from [27]

2.2.2 Dynamic Tuning Methods

The previously discussed tuning techniques have been considered as "static" as the control of tuning is independent of the cyclic nature of the oscillation. That is to say that a tuning setting may be established at any point and left in position for an arbitrary amount of time. Alternatively, LC circuits may be tuned dynamically on a per-cycle basis, i.e. adding and removing a tuning component from the circuit in a cyclic fashion, so as to produce an apparent variable inductance or capacitance.

2.2.2.1 Boys et al: Switched Inductor Pickup

A variable inductor WPC receiver is presented in [28]. An inductor is introduced in parallel with a pickup circuit on a cyclic basis in order to modify the resonant frequency. Components L and C in figure 2-11 represent the pickup circuit. Inductor L_2 is switched in and out of the circuit in order to modify the resonant frequency.

The modified resonant frequency is a function of the time period per cycle for which current is permitted to flow through the tuning inductor L_2. The maximum frequency is achieved when L_2 is left continually connected to the pickup, since the effective inductance of the LC circuit is determined by the parallel combination of L and L_2, resulting in minimal inductance and hence maximum frequency. The lowest frequency may be achieved by excluding the inductor for the entire cycle. Frequencies within this range may be achieved by switching in L_2 for part of the cycle, according to the timings in figure 2-12.

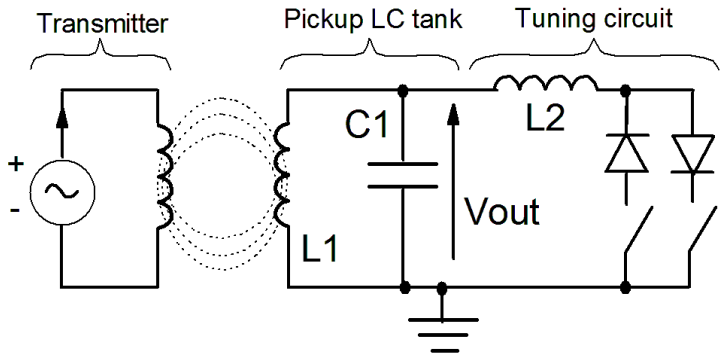

Figure 2-11: Boys et al. switched inductor tuning method. Adapted from [28]

Each switch is implemented with a thyristor, meaning each switch only conducts on one half of the cycle. This is advantageous because it results in the switch opening automatically when the current through it reduces to zero, since the thyristor will reset under this condition. This ensures that the switched inductor current excursions start and end at zero amps.

The period of time for which L_2 is conducting is set by using a saw tooth waveform and "slicing" it with DC references. Moving the reference levels therefore controls the tuning setting. In figure 2-12a, the waveform shows the tank voltage V and the switched inductor current I. Figure 2-12b is used as the input to a phase-locked loop (PLL) which generates the sawtooth wave in figure 2-12c. A comparator then uses this sawtooth wave to produce the switch control signals in figure 2-12d.

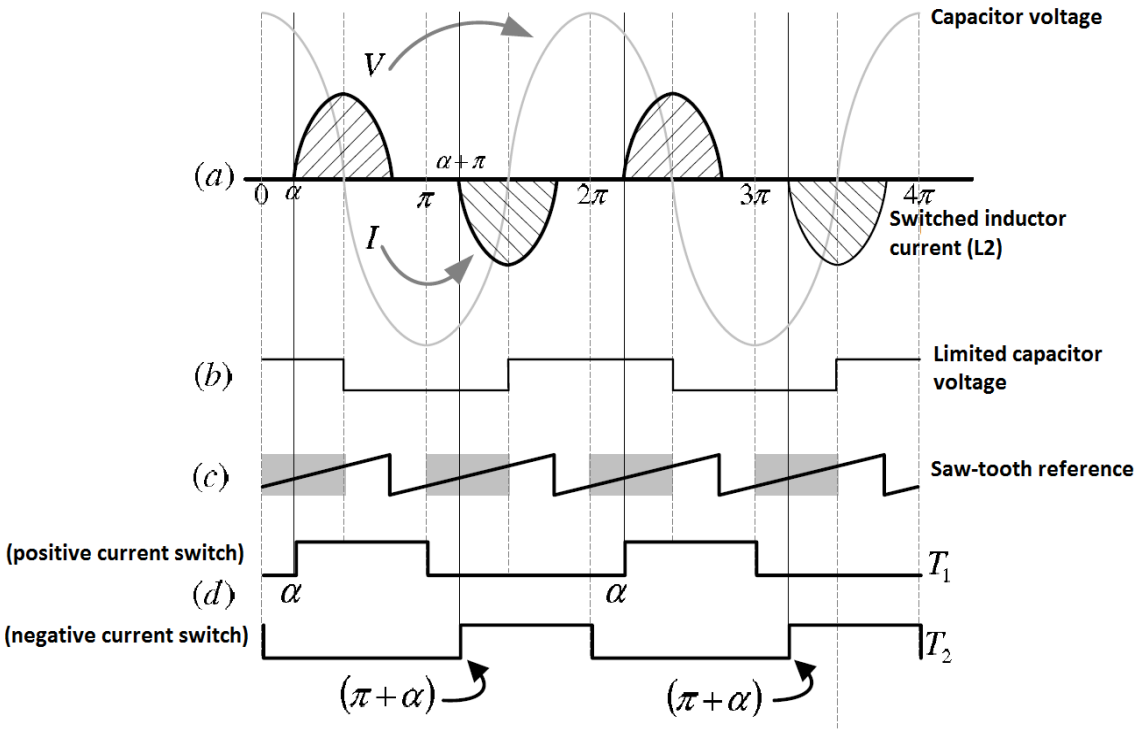

Figure 2-12: Waveforms for switched inductor tuning. Extracted from [28]

An advantage of this tuning method over static tuning methods previously discussed is the ability to retune the circuit on a per-cycle basis, making it easier to compensate for transient detuning effects. The tuning resolution possible is now determined by how accurately the saw-tooth wave may be sliced, rather than the tolerances in a binary weighted tuning bank of inductors or capacitors. This tuning method is primarily aimed at improving a pickup coil, but no mention is given to its usage in a transmitter.

2.2.2.2 Hill: Switched Capacitor Transmitter

For tuning of a transmitter LC tank, a method of switched capacitance is presented in [29], using a second capacitor for tuning the LC tank by creating an average capacitance to ensure that the tank resonates with maximum amplitude. Figure 2-13 shows the circuit used for this method.

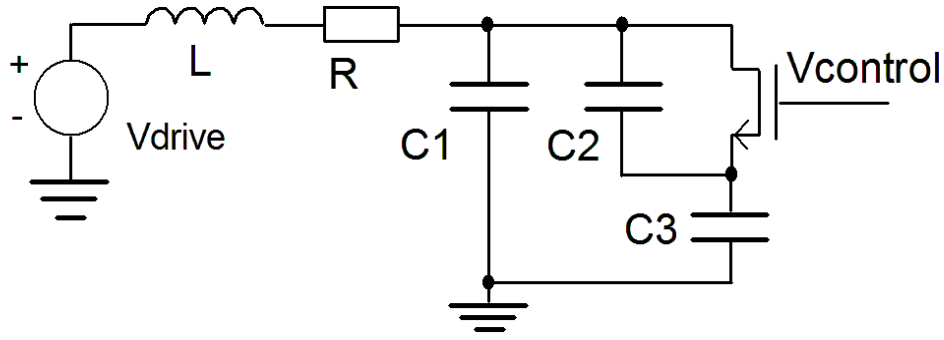

Figure 2-13: Hill switched capacitor tuning method. Adapted from [29]

The tune setting is determined both by the amplitude of oscillation in the LC tank and the gate voltage applied to the MOSFET. The FET conducts when the $V_{gs} > V_t$, bypassing C_2, hence the total capacitance is given by the sum of C_1 and C_3. When the tank voltage swings around such that $V_{gs} < V_t$, the FET stops conducting and the total capacitance is given by the sum of C_1 and the series combination of C_2

and C_3, resulting in a lower overall capacitance and hence a higher resonant frequency. The waveform in figure 2-14 is the result of this switching behaviour.

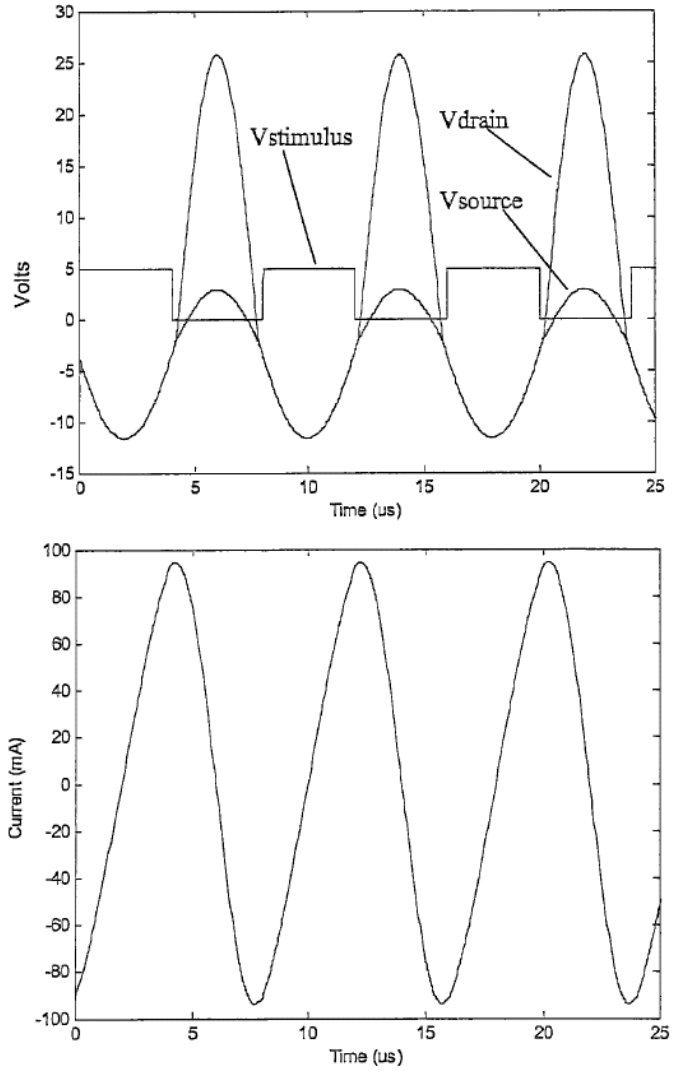

Figure 2-14: Hill switched capacitor timing diagram. Extracted from [29]

The maximum usable frequency occurs when the FET does not conduct at all, so the effective capacitance is the sum of C_1 and the series combination of C_2 and C_3. When the FET is conducting 100% of the cycle, the resonant frequency is set by the sum of C_1 and C_3. This assumes that the on resistance of the FET is negligible and so the potential at both ends of C_2 is the same, hence it makes no contribution to the resonance.

The circuit guarantees that the waveform is continuous, since the switching action is directly controlled by the tank oscillation rather than an external drive as per the Boys et al. tuning method [28]. This method does however cause some additional dissipation of power in the MOSFET, since the value of V_{gs} transitions slowly through the linear region of the FET. Both the amplitude of oscillation and the gate voltage must be carefully monitored to ensure that the duty cycle is controlled for optimal tuning.

Although the inductor current is maximised when the LC circuit is correctly tuned, the current waveform is not exactly sinusoidal as the stimulus is not symmetrical. This suggests that additional harmonics will be created and the used bandwidth is needlessly increased.

2.2.2.3 *Pan et al.: Self-Tuning Variable Frequency Driver*

An interesting variable operating frequency technique is presented in [30]. The k and Q factors of the system in figure 2-15 are sufficiently high that a change in k or the load current at the receiver can significantly modify the resonant frequency seen at the transmitter. However, the system inherently tracks the optimum resonant frequency because the oscillator and tank driver are combined, hence the transmitter runs freely at resonance, changing frequency as the load conditions change. If the load is constant and the k factor is adjusted, the circuit also inherently tracks the frequency splitting due to the magnetic resonance as it occurs.

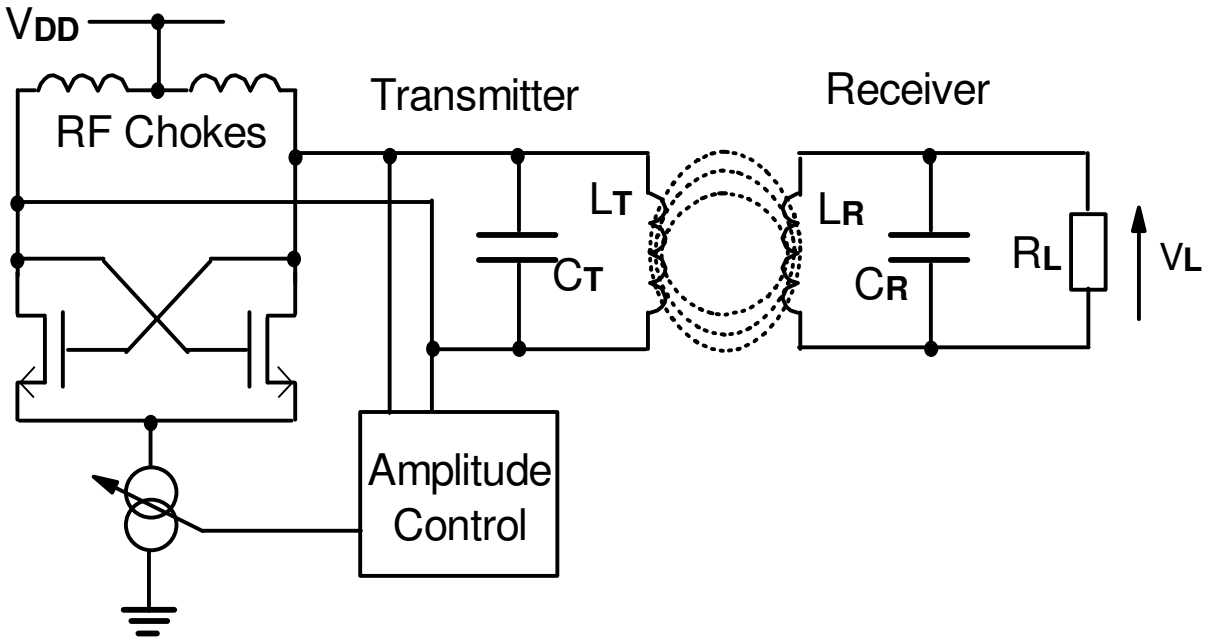

Figure 2-15: Pan et al. variable frequency transmitter. Adapted from [30]**.**

The system also includes a means of controlling the receiver load voltage from the transmitter, by adjusting the drive amplitude as the coupling factor changes. This behaviour is desirable in medical implant applications, where voltages must be well controlled for patient safety.

The operating frequency of the proposed system is very large, from 10.4-13.56MHz, which is an unusually high bandwidth. Most applications require a very narrow operating range to avoid interference with neighbouring spectrum users. Therefore, this tuning method is limited to scenarios where low power is transmitted over short distances, such biomedical implants, to minimise radiated interfering signals which can occupy a large bandwidth. The particular implementation in [30] is limited to 18mW of power transferred over 4.2cm.

2.2.3 Resonant condition detection and adjustment

For all of the tuning methods previously described, there must also be a method to determine if the system is resonating correctly. The simplest method to achieve this is to measure the amplitude using a full or half wave rectifier and using a comparator to determine if the oscillation is at a maximum magnitude [31]. Peak detection may also be used [32]. The largest amplitude indicates that the best possible tune state has been achieved. Figure 2-16 shows an example relation between tune setting and amplitude which may be observed.

Knowledge of the amplitude alone is not enough however for adjustment of the tune state, since it does not indicate in which direction the tune setting needs to be adjusted, i.e. for a higher or lower resonant frequency. A search algorithm is needed to assess the nearby tuning settings and determine if the tuning setting should be moved up or down.

For the switched inductor method presented by Boys et al., peak detection is proposed as the method of tuning control. It is mentioned however that a phase measurement between the current and voltage in the LC pickup would be preferable, since this method of detection would indicate resonance as earlier derived without requiring knowledge of the Q factor or particular amplitude of oscillation at resonance.

The method of phase measurement may also be applied to a driven LC tank in a transmitter. As shown in equation 2.12, when at resonance there is a 90 degree lead of the capacitor voltage over the drive voltage. If the drive frequency is too low, the phase lead will be less than 90 degrees. If the drive frequency is too high, there will be a phase lead of more than 90 degrees. Taking a measurement of this offset indicates not only whether or not optimal tuning has been achieved, but it also indicates in which direction the tune setting needs to be adjusted. This additional information reduces the complexity of the tuning algorithm and therefore system cost. Figure 2-16 shows the plot of a hypothetical system which considers the magnitude and phase of V_c relative to V_{drive} in order to determine the optimal tuning setting.

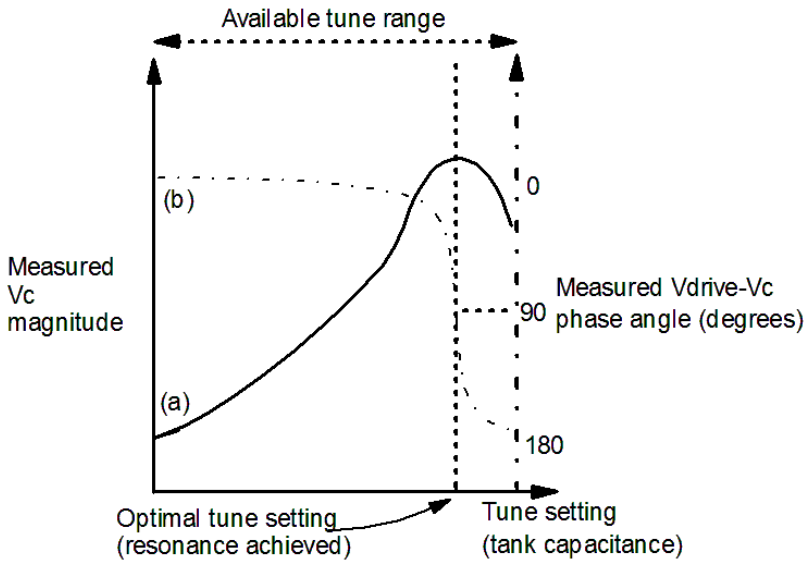

Figure 2-16: Tuning metric comparison for varying antenna capacitance: measured Vc magnitude (a) and measured Vdrive-Vc phase angle (b) vs tune setting

2.3 Summary of prior art

In an inductive coupling WPC system, the transmitter must induce a sufficiently large EMF at the receiver to activate its circuits, in order to transfer both power and data. Hence a large magnetic field must be created, i.e. the transmitter's antenna must permit a large current to flow. To efficiently achieve the required current, the transmit antenna is preferably high Q, in order to reduce unnecessary power dissipation and to permit the use of simpler drive circuitry. However, a high Q factor constrains the data bandwidth that can be modulated onto the carrier, hence there is a trade-off between power transfer efficiency and data rate. Furthermore, real-world antenna circuits are detuned by manufacturing tolerances and environmental effects, necessitating precise tuning so that the antenna's resonant frequency closely matches the system drive frequency. The prior art of static and dynamic methods of tuning the antenna have been discussed, as well as methods of detecting that the resonant condition has been achieved.

To reduce system costs, it is desirable to reduce the number of tuning components required to achieve a sufficiently high tuning resolution (i.e. tuning to within the 3dB bandwidth of the antenna). It is also desirable to continuously track the resonant condition in the foreground, rather than periodic background calibration which may otherwise disrupt normal operation. The next chapter introduces a new tuning method to help overcome these challenges.

3 Zero-Voltage Switched Fractional Capacitance

This chapter introduces the zero-voltage switched fractional capacitance method of tuning LC circuits, in order to reduce the number of components required for tuning. It is shown how the method also provides a new means of sensing the resonant condition, leading to an elegant self-tuning architecture. Simulation results demonstrate that the method is viable for implementation with discrete components.

3.1.1 Continuous fractional capacitance tuning concept

The previously discussed tuning methods present several challenges. Firstly, there is a trade-off with data bandwidth and Q factor where in fact it would be preferable to maximise both. Component tolerances and detuning during operation also mean that the tuning methods must be accompanied by some form of resonance detection, usually involving amplitude measurement. What is most preferable is a form of tuning which permits high Q factor, as well as an easy method to determine the resonance condition. The proposed tuning method in [1] provides a solution to these criteria.

At its simplest, the proposed method for continuous tuning of an LC circuit involves a single additional capacitor in parallel with the main capacitor of the LC antenna. This additional capacitor has a switch which can disconnect it from the ground reference, as per figure 3-1. This topology is first presented in [33], however no consideration is given to the timing of the switching action of the second capacitor, hence energy may be dissipated from the LC circuit if the switch is closed when there is significant voltage across it.

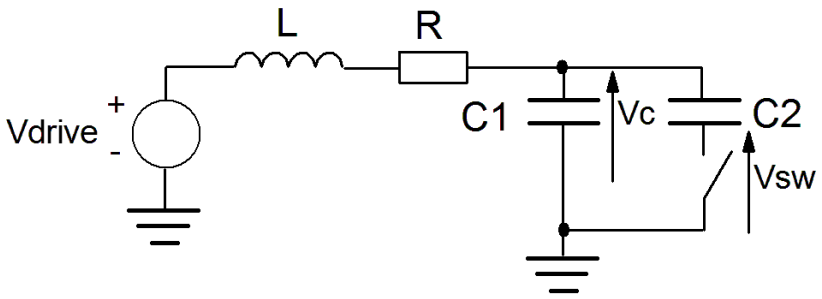

Figure 3-1: Fractional capacitor tuning concept circuit. Adapted from [33]

Figure 3-2 shows how the resonant frequency may be modified in a synchronous fashion. The circuit is being driven at the desired modified resonant frequency, and all timings are assumed to be exactly correct for the purpose of demonstration. At the beginning of a quadrant of oscillation, the capacitor switch is closed. The shape of $v_c(t)$ is determined by the minimum frequency, set by the sum of C_1 and C_2.

The capacitor voltage $v_c(t)$ increases until $t = t_c$, where the capacitor switch is opened. The operating frequency is now determined by C_1 only, since C_2 has been removed from the resonant circuit. The voltage across C_2 remains constant and is equal to $v_c(t_c)$. The switch voltage $v_{sw}(t)$ begins to deviate from the ground potential, tracking the shape of $v_c(t)$.

At $t = t_p$, the capacitor voltage reaches a peak and the first quadrant of oscillation is complete. The second quadrant mirrors the action of the first, such that the capacitor switch is closed when $v_{sw}(t) = 0$. This synchronous and symmetrical switching action ensures that there is no voltage across the switch when it is closed. No energy is therefore dissipated by the switching action, providing a lossless modification of the resonant frequency. The second quadrant ends where $v_c(t) = 0$, with the third and fourth quadrants occurring in a similar manner to the first and second, as per figure 3-2.

Whilst $v_c(t)$ is visibly no longer sinusoidal, the inductor current $i_{tank}(t)$ will be essentially sinusoidal provided the Q factor of the LC circuit is high. Any high-frequency components introduced by the

switching action will be filtered out, resulting in an inductor current (and therefore magnetic field) which has low harmonic content.

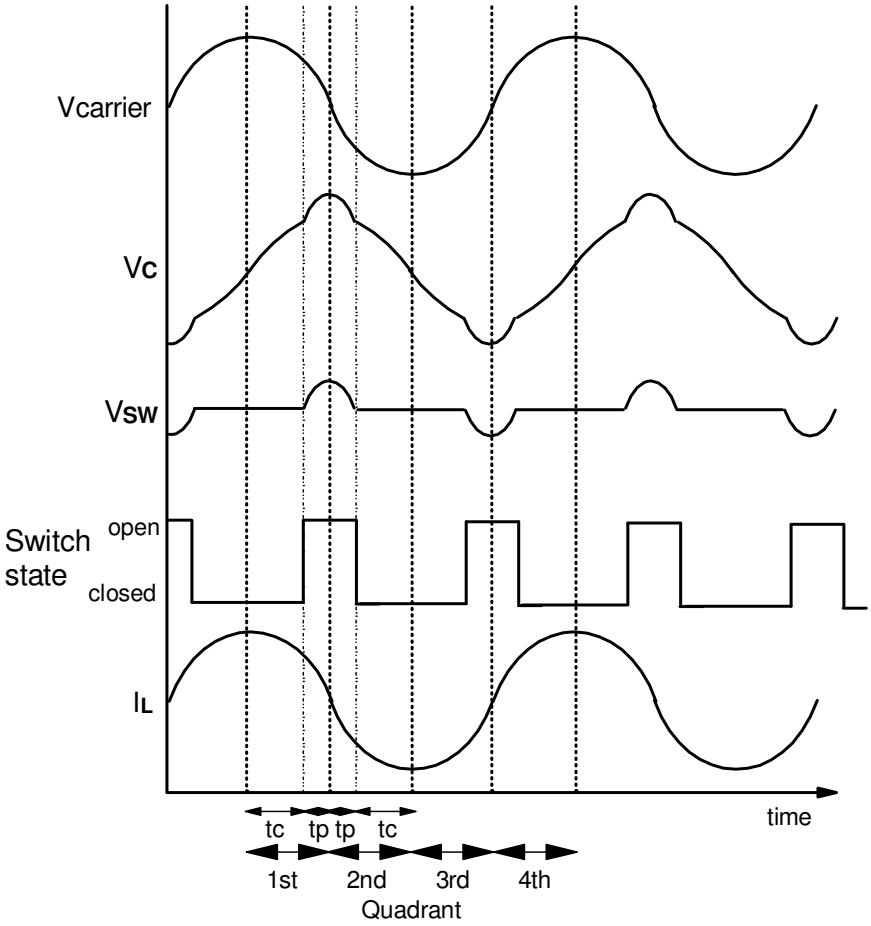

Figure 3-2: example waveforms for fractional capacitance tuning at resonance

3.1.2 Available Tune Range using Zero-Voltage Switching of Fractional Capacitance

When the additional capacitor C_2 is switched out of the tank, i.e. the switch is open for the entire cycle, the resonant frequency is at maximum and given as $\omega_{max} = \frac{1}{\sqrt{LC_1}}$. When the C_2 is switched in for the whole cycle, the resonant frequency is $\omega_{min} = \frac{1}{\sqrt{L(C_1+C_2)}}$. Any resonant frequency in between may be achieved by including C_2 for part of the cycle. Provided that the switching action is symmetrical according to figure 3-2, no energy will be dissipated by the switching action.

The relationship between the modified resonant frequency and the phase angle of switching action may be derived by analysing the circuit in the time domain. The general time domain solution for the current in an LC tank is given as per equation 3.1, as derived in section 3.2.2. For the sake of demonstration, the tank is assumed to be lossless. The initial condition is assumed such that $v_c(0) = 0$ and $i(0) = 1$. The resonant frequency is ω_{min} since both capacitors are switched into the circuit.

$$i(t) = \cos(\omega_{min} t) \tag{3.1}$$

The tank voltage is defined across the capacitors, so this may be expressed in terms of the integral in equation 3.2, where t_c is a period of time between 0 and the duration of one quadrant of oscillation, i.e. $0 \leq t_c \leq \frac{\pi}{2\omega_{min}}$. The rate of change of the current may be expressed by equation 3.3.

$$v_c(t) = \frac{1}{C_1 + C_2}\int_0^{t_c} \cos \omega_{min} t \, dt \tag{3.2}$$

$$\left.\frac{di}{dt}\right|_{t \leq t_c} = -\omega_{min} \sin \omega_{min} t \tag{3.3}$$

At the instant where t = t_c, the switch is opened. Since C_2 is now disconnected from the circuit, the voltage across it will remain constant, whilst the voltage across C_1 will continue to change. The reduction in overall capacitance has caused a change in circuit response and the higher resonant frequency now applies. The initial condition of this new system may be given in equation 3.4, which is the expression for the final value of the previous system, i.e. the value of the current at the moment the switch was opened.

$$i(t_c) = \cos(\omega_{min} t_c) \tag{3.4}$$

The new system has the general solution in equation 3.5. Since a new system is being considered, equation 3.4 also represents the value of A. The value of B must be determined by differentiating to yield equation 3.6.

$$i(t) = A \cos(\omega_{max} t) + B \sin(\omega_{max} t) \tag{3.5}$$

$$\frac{di}{dt} = -\omega_{max} \cos(\omega_{min} t) \sin(\omega_{max} t) + B\omega_{max} \cos(\omega_{max} t) \tag{3.6}$$

At the instant of t = t_c, the gradient of $v_c(t)$ before and after the switch was closed must be the same, otherwise the waveform would be discontinuous. The same is true for the current. Hence, B may be derived as per equations 3.7, 3.8 and 3.9.

$$\left.\frac{di}{dt}\right|_{t=t_c} = -\omega_{max} cos(\omega_{min} t) sin(\omega_{max} t) + B\omega_{max} cos(\omega_{max} t) = -\omega_{min} sin(\omega_{min} t_c) \tag{3.7}$$

$$0 + B\,\omega_{max} = -\omega_{min} \sin(\omega_{min} t_c) \tag{3.8}$$

$$\mathrm{B} = -\frac{\omega_{min}}{\omega_{max}} \sin(\omega_{min} t_c) \tag{3.9}$$

The new time domain system response can therefore be given as

$$i(t) = \cos(\omega_{min} t_c) \cos(\omega_{max} t) - \frac{\omega_{min}}{\omega_{max}} \sin(\omega_{min} t_c) \sin(\omega_{max} t) \tag{3.10}$$

To determine the total length of a cycle, and hence the modified resonant frequency, we must consider both halves of the switch state. The duration of the first interval (where the switch is closed) is already defined as t_c, whilst the second interval (where the switch is open) can be derived from the new response.

The system was assumed to have started at a condition where $v_c(0) = 0$. The end of the first quadrant of oscillation will therefore occur where $v_c(t)$ is maximum, i.e. i(t) = 0. Equation 3.10 can hence be reformulated to yield

$$\cos(\omega_{min} t_c) \cos(\omega_{max} t_p) = \frac{\omega_{min}}{\omega_{max}} \sin(\omega_{min} t_c) \sin(\omega_{max} t_p) \tag{3.11}$$

where t_p is the time duration between the end of the first quadrant of oscillation and the time t_c. Equations 3.12, 3.13 and 3.14 show how the value of t_p may now be expressed in terms of parameter t_c.

$$\frac{sin(\omega_{max}t_p)}{cos(\omega_{max}t_p)}\frac{\omega_{min}}{\omega_{max}} = \frac{cos(\omega_{min}t_c)}{sin(\omega_{min}t_c)} \tag{3.12}$$

$$tan(\omega_{max}t_p) = \frac{\omega_{max}}{\omega_{min}}\, cot(\omega_{min}t_c) \tag{3.13}$$

$$t_p = \frac{1}{\omega_{max}} tan^{-1}\left[\frac{\omega_{max}}{\omega_{min}}\, cot(\omega_{min}t_c)\right] \tag{3.14}$$

The time duration of one quadrant is equal to the sum of t_c and t_p, as per equation 3.15.

$$T_q = t_c + \frac{1}{\omega_{max}} tan^{-1}\left[\frac{\omega_{max}}{\omega_{min}}\, cot(\omega_{min}t_c)\right] \tag{3.15}$$

Since there are four quadrants per cycle, the total period of oscillation is given by $4T_q$, hence equation 3.16 is the expression for the modified resonant frequency of the LC tank, ω_{res}.

$$\omega_{res} = \frac{2\pi}{4\,T_q} = \frac{\pi}{2\left(t_c + \frac{1}{\omega_{max}} tan^{-1}\left[\frac{\omega_{max}}{\omega_{min}}\, cot(\omega_{min}t_c)\right]\right)} \tag{3.16}$$

In order to normalise equation 3.16, the phase angle of switching action may be used, defined as $\theta_c = \omega_{min}t_c$, resulting in equation 3.17.

$$\omega_{res} = \frac{\pi}{2\left(\frac{\theta_c}{\omega_{min}} + \frac{1}{\omega_{max}} tan^{-1}\left[\frac{\omega_{max}}{\omega_{min}}\, cot(\theta_c)\right]\right)} \tag{3.17}$$

The time at which the switch is opened and closed therefore determines the new resonant frequency. The derivation assumes that each quadrant is symmetrical, such that figure 3-2 represents the time domain behaviour of the waveforms in the circuit. Figure 3-3 shows how ω_{res} varies with θ_c, for a system where $\omega_{min} = 1$ and $\omega_{max} = \sqrt{2}$, i.e. $C_1 = C_2$.

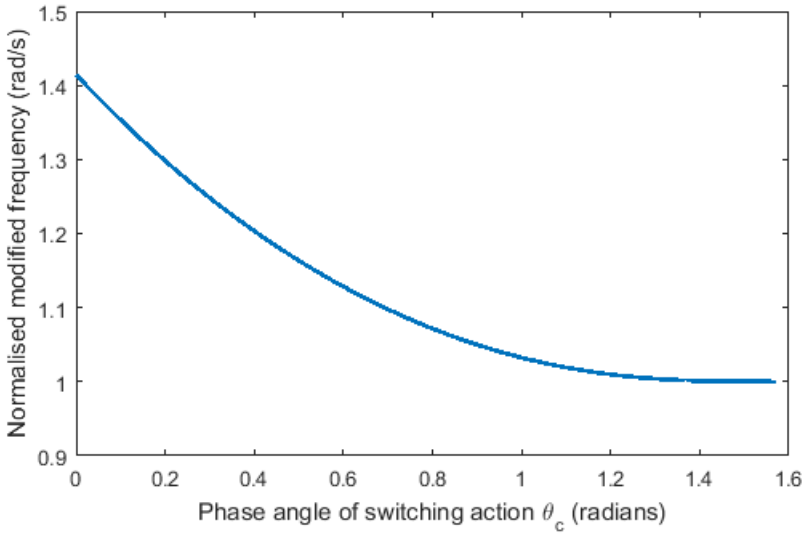

Figure 3-3: Modified resonant frequency vs phase angle of switching action θ_c

3.2 System Architecture for Fixed Frequency Tuning

In order to achieve resonance using fractional capacitor tuning, the tank drive and switch control must be synchronous, as opening and closing the switch at the incorrect moment will result in a non-resonant condition.

3.2.1 Timing Generation

Two methods to achieve synchronous signals are described in [1]. The first derives the switch control timings from the carrier wave used to drive the tank, as per figure 3-4.

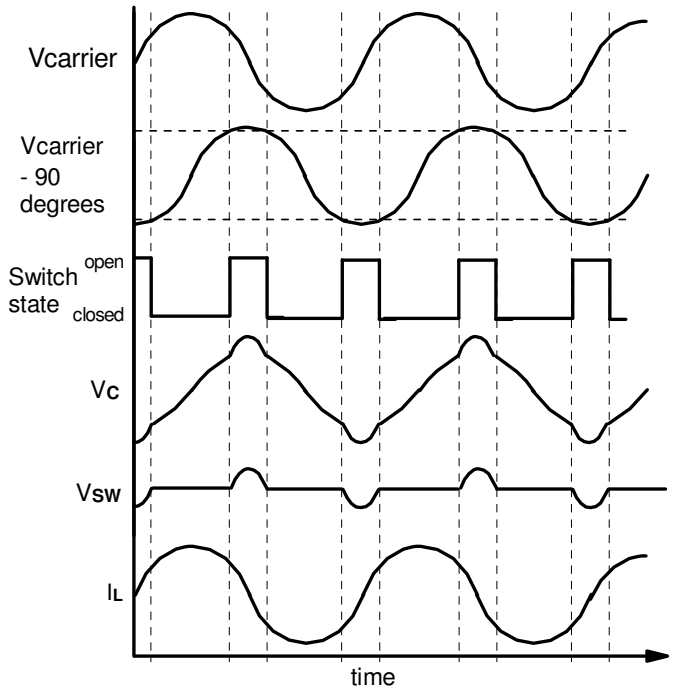

Figure 3-4: Fractional capacitor timing generation using "sine slicing" method

When at resonance, the tank voltage oscillation V_c is exactly 90 degrees out of phase with the carrier. Therefore, to create a switch control which is correctly phase-aligned, the timings can be derived from a 90-degree shifted version of the carrier which is created and “sliced” with a pair of comparators. When the 90-degree reference is between the slicing voltages, the switch is closed. When it exceeds the slice voltages, the switch is open. Adjusting the slice voltage therefore adjusts the modified resonant frequency.

The sine-slicing method is convenient where a sinusoidal carrier wave is readily available. Both a buffered drive signal and a 90-degree reference may be obtained from the same signal, keeping the tuning correctly phase aligned. However, the relationship between the slicing voltage and t_c is non-linear. When the slice level is near the peak and trough, the pulse width becomes more sensitive to minor variations in the amplitude of the sine wave, which may create jitter in value of t_c, causing detuning.

For a linear relationship between the slice voltage and t_c, the second proposed timing generation method may be used, as per figure 3-5. The triangular waveform is kept 90 degrees out of phase of the drive. In this case, the drive signal may be derived from the triangle wave using a differentiator. A square wave drive to the LC tank is acceptable, provided that the unwanted harmonics can be attenuated by the narrow bandwidth due to high Q factor as earlier discussed. The switch control timings are derived as per the sine-slicing method by comparing the triangle with voltage references.

It is assumed that the triangle has the same gradient on both the rising and falling edges. If these gradients are not the same then a phase offset will be caused between the drive and switch control signals. Figure 3-6 (left) shows an extreme case of detuning caused by triangle slant. The switch voltage offsets become asymmetric, such that on one excursion of V_c the pulse width appears to be too narrow and on the other excursion it appears to be too wide.

It is also assumed that the slicing levels are symmetrical with respect to the midpoint of the triangle wave. Resonance may still be achievable if both slice voltages are offset by the same amount, since the total time the switched capacitor is included may be the same per cycle as shown by figure 3-6 (right). It is not ideal however for such a situation to arise. The tuneable frequency range is reduced, as one of the slicing voltages will reach the end of the tune range before the other. For maximum tuning range the slicing voltages should therefore be symmetrically spaced with relation to the centre of the triangle.

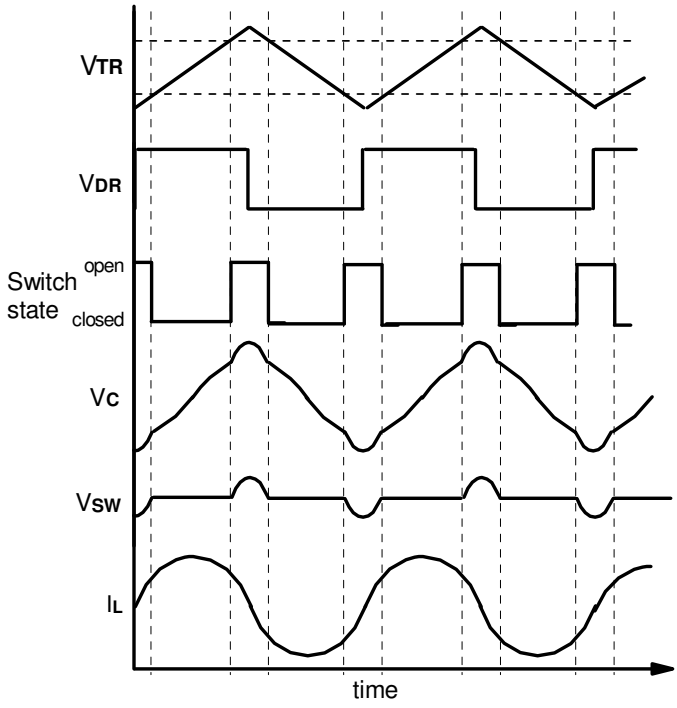

Figure 3-5: Fractional capacitor timing generation using "triangle slicing" method

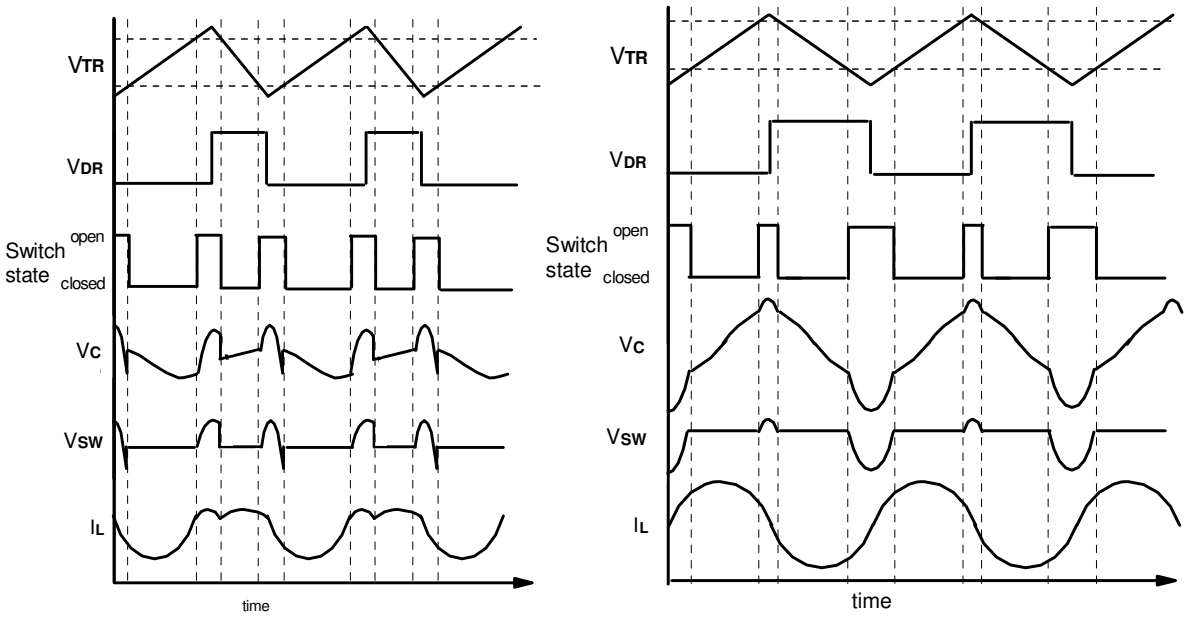

Figure 3-6: Extreme example of detuning caused by triangle slant (left), asymmetric slicing levels for fractional capacitor tuning (right)

Whilst triangle-slicing provides a linear relationship between t_c and the slice voltage, it requires a triangular waveform with equal positive and negative slew rates, as previously discussed. Using the voltage-current relation of a capacitor, it is possible to turn a square wave of current into a triangle wave of voltage. Assuming that the peak and trough of the triangle are fixed, the frequency of the triangle may be determined by the integration capacitance C and the integration current I. The frequency of oscillation may therefore be determined using the parameters indicated in figure 3-7, giving rise to the solution in equation 3.20.

$$I = C\,\frac{dv}{dt} \tag{3.18}$$

$$f = \frac{1}{T} = \frac{1}{2dt} \quad \therefore \quad dt = \frac{1}{2\,f} \tag{3.19}$$

$$f = \frac{I}{2\,C\,dv} \tag{3.20}$$

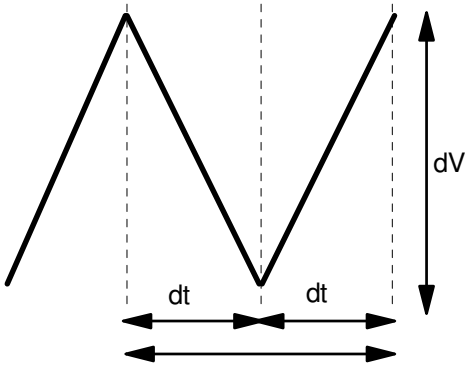

Figure 3-7: Definition of triangle parameters used for current-frequency relationship

In order to change direction of the triangle gradient, the current direction should be reversed, however its magnitude should remain constant to avoid slanting the triangle wave and creating a phase offset. To detect the peak and trough of the triangle, a pair of comparators may be used, whose outputs are latched in order to determine the current direction. The outputs of the latch in figure 3-8 indicate whether the integrator should be ramping upwards or downwards.

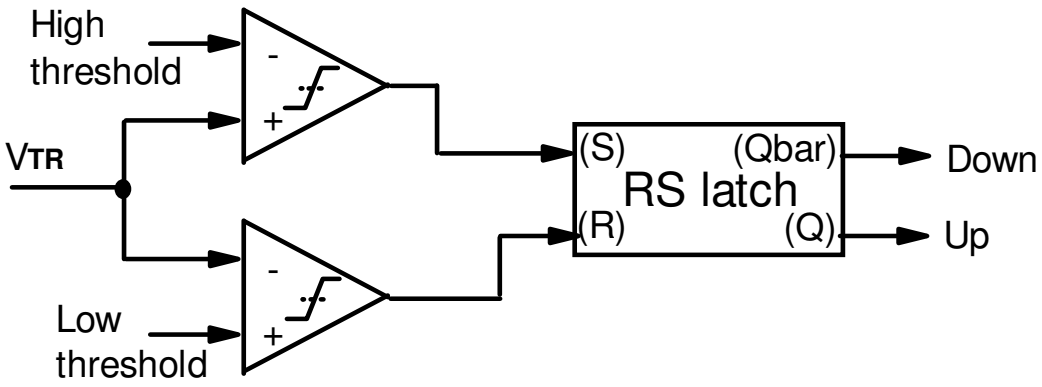

Figure 3-8: Triangle peak and trough detection using comparators and RS latch

The resulting triangle wave generation architecture is as per figure 3-9. Note that the integrator is buffered using an operational amplifier (op-amp) to provide a fixed common mode voltage into which the up/down current can flow. This op-amp should be have a sufficiently high slew rate such that it can

provide the required triangle wave gradient. Note also that the "up" waveform may also be used for the tank drive signal, removing the need for a differentiator circuit.

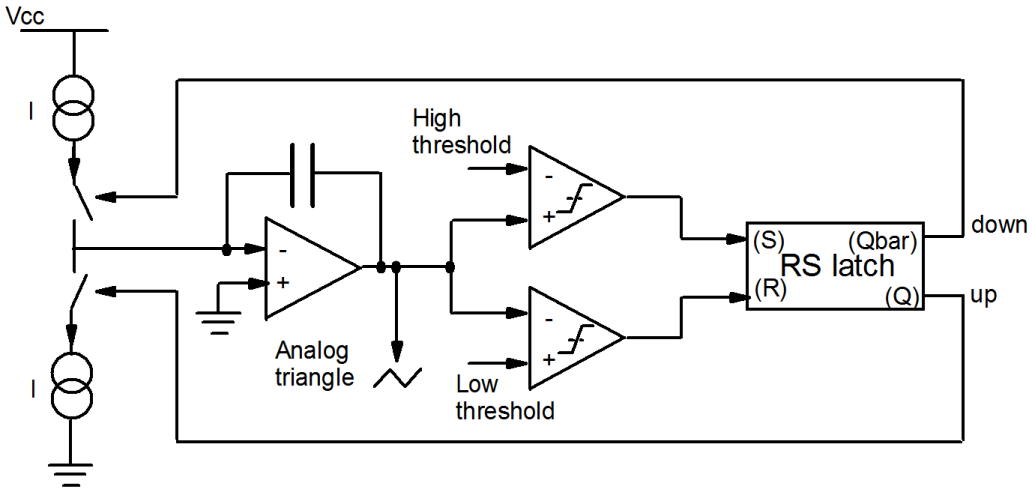

Figure 3-9: Current source-based triangle generator concept.

The current integrator-oscillator was simulated in LTSpice. The approximate frequency range of 8-12kHz was chosen, as it was considered to be a sufficiently low frequency to permit easy breadboard implementation later, allowing reliable operation with discrete components and manual wiring for construction, whilst being high enough to demonstrate moderate Q factor.

The integration current was set to be in the 1-5mA range, requiring a capacitance of approximately 30nF for operation at 8-12kHz. A full schematic of the circuit is included in appendix B. Figure 3-10 shows the square wave of current and resulting triangle wave.

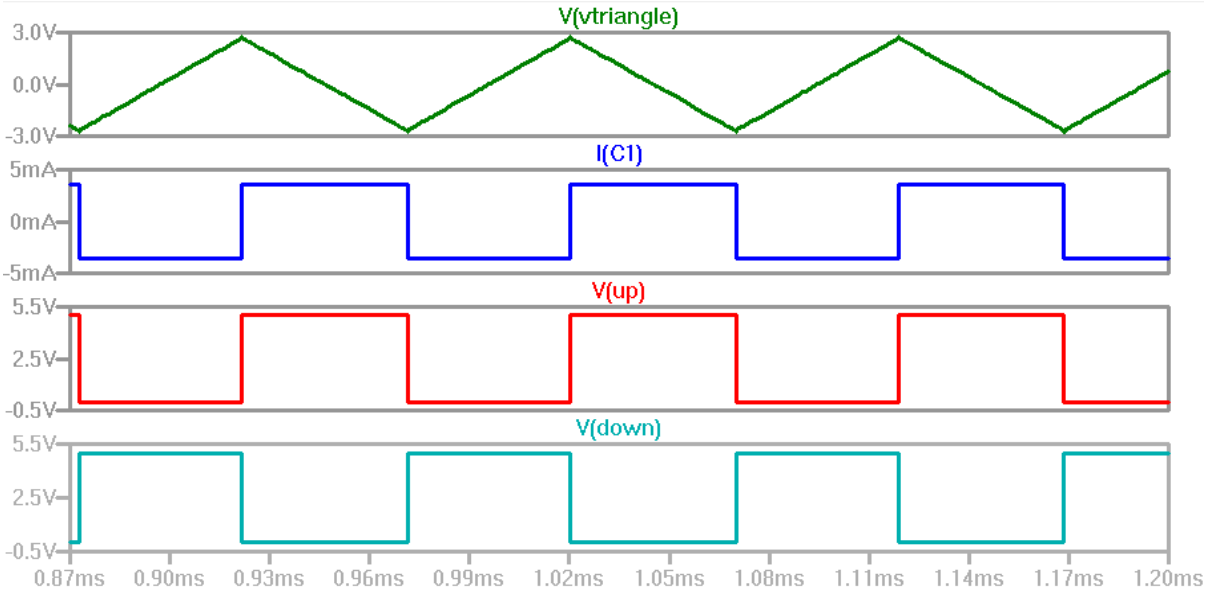

Figure 3-10: Triangular voltage waveform generated from square wave current

3.2.2 Basic Tuning

As previously described, comparators may be used for generation of the switch control signal from the triangle wave. The switch should be closed when the triangle is between the higher and lower slicing voltages, and open when it exceeds either. To achieve this, the comparators may be configured to produce a logic 0 output when the absolute magnitude exceeds the threshold, and logic 1 otherwise.

This produces two signals, θ_L and θ_H which when combined in an AND gate produce the switch control signal.

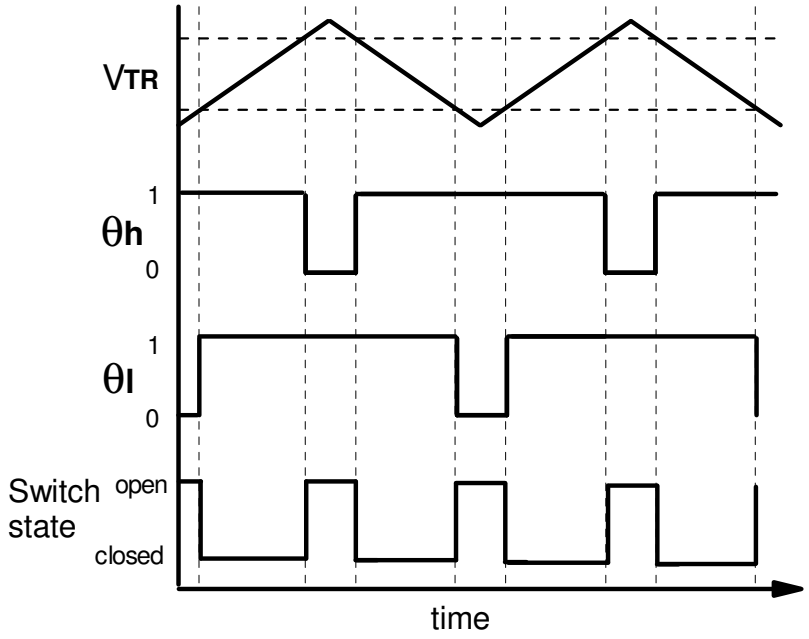

Figure 3-11: Triangle slicing waveforms used to generate the switch state.

In order to ensure that both the slicing waveforms are symmetrical around the triangle's midpoint, an inverting amplifier with unity gain may be used, so that one input voltage may result in a pair of symmetrical slicing voltages as per figure 3-12.

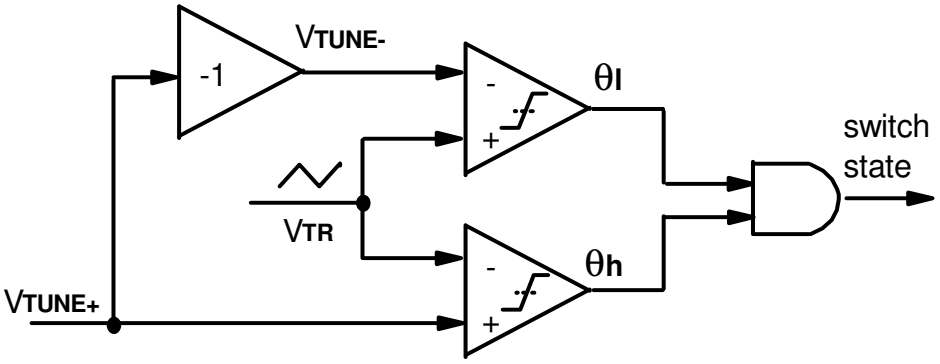

Figure 3-12: Triangle symmetrical slicing comparators and switch control

The previous LTSpice simulation was extended to test tuning of a resonant circuit, according to the block diagram in figure 3-13. A resonant LC circuit with a Q factor of 50 at 10kHz, with an ideal behavioural driver and tuning switch. The full schematic is provided in appendix B. Figure 3-14 shows a linear sweep of the tuning voltages to determine the optimal resonant condition, indicated by a peak in the amplitude of the antenna voltage and current, occurring at approximately 84.5ms, i.e. V_{TUNE+} is approximately 2.099V

Figure 3-15 shows a closer inspection of the antenna voltages and currents at resonance. The switch is opening and closing symmetrically around the peaks and troughs of V_C, and the V_{SW} excursions are correctly starting and terminating at zero voltage. Away from the resonant condition, the V_{SW} excursions do not reach the zero voltage before switch closure in figure 3-16 (i.e. the system is below resonance), or the excursions cross through zero volts in figure 3-17 (i.e. the system is above resonance).

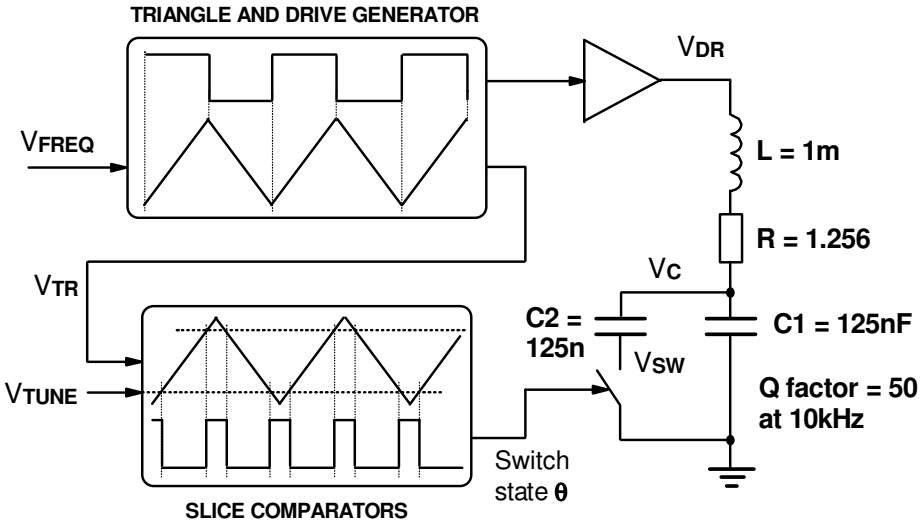

Figure 3-13: Block diagram of basic tuning simulation

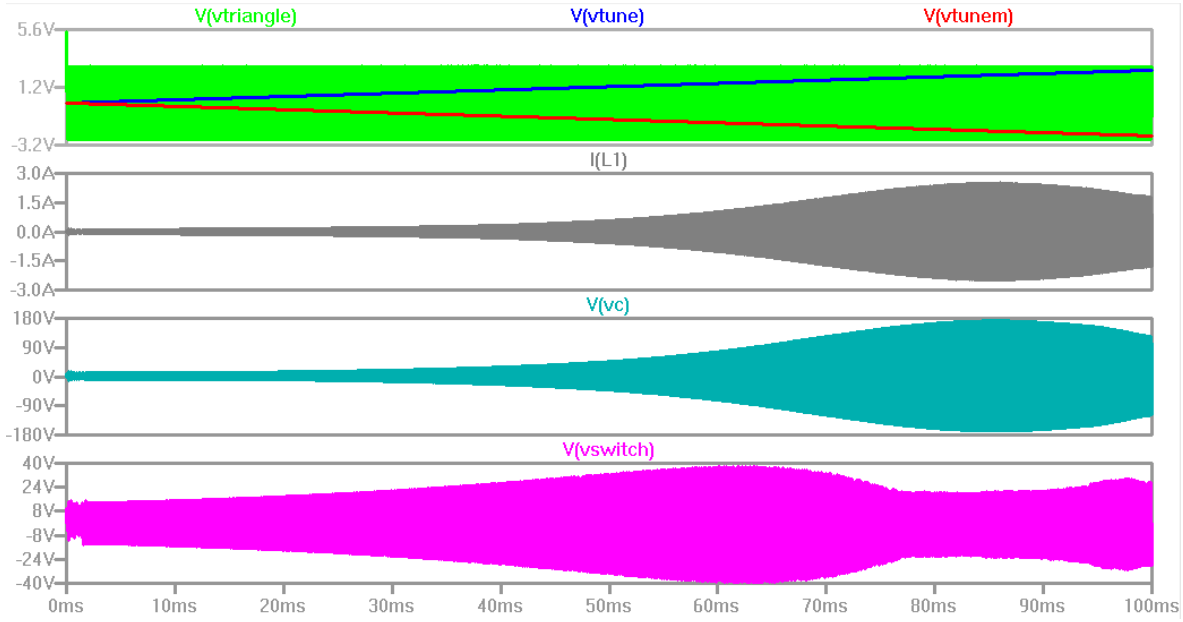

Figure 3-14: Sweeping the slicing voltage V_{TUNE} from 0V to 2.5V at a drive frequency of 10kHz

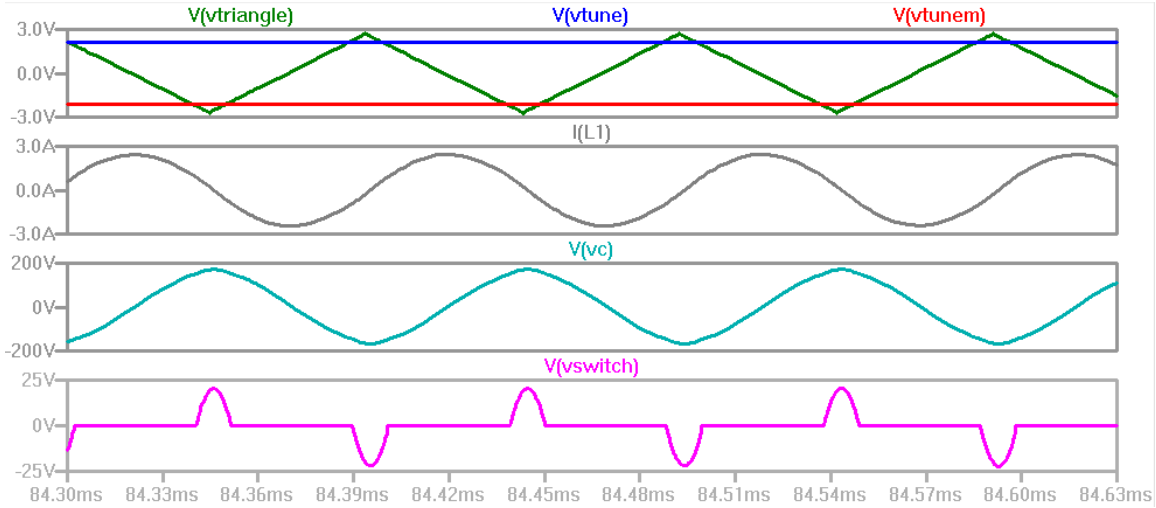

Figure 3-15: Switched fractional capacitance tuning at 10kHz, showing correct waveform timing (V_{TUNE+} = 2.099V)

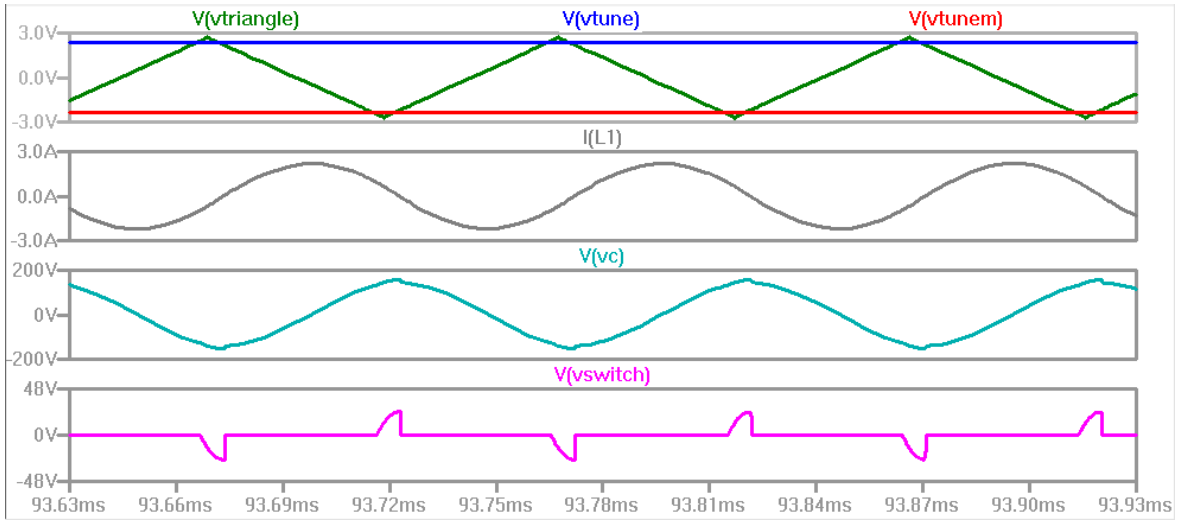

Figure 3-16: Fractional capacitance mistiming: modified resonant frequency is too low (V_{TUNE+} = 2.343V)

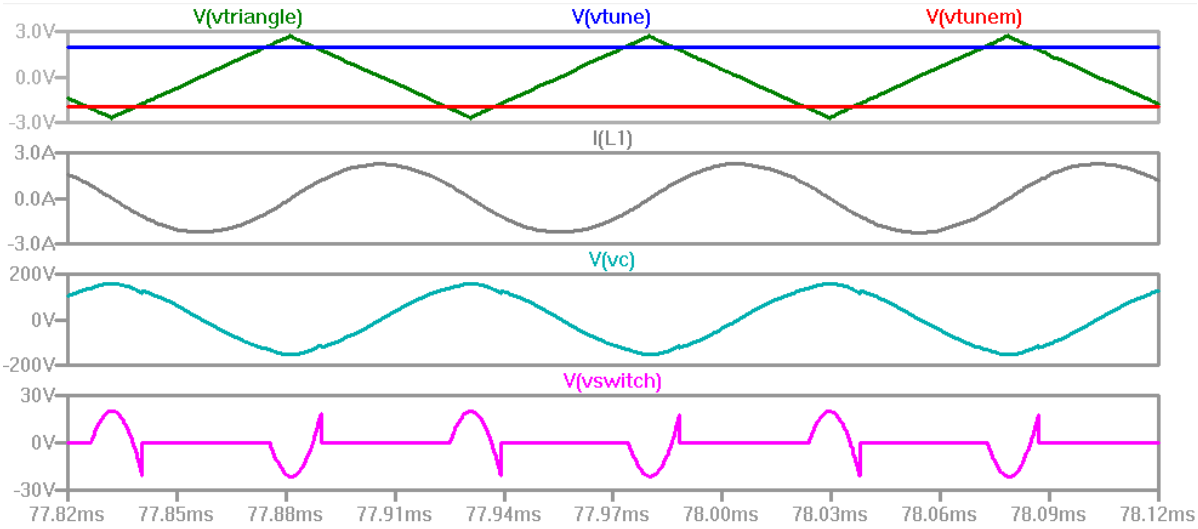

Figure 3-17: Fractional capacitance mistiming: modified resonant frequency is too high (V_{TUNE+} = 1.948V)

3.2.3 Equivalent Tuning Range and Resolution: Fractional Tuning vs Selectable Capacitors

A system of tuning by switched fractional capacitance that uses an ideal and completely analogue timing generator theoretically has a continuous tuning resolution, i.e. any resonant frequency in the physical tuning range (as set by the fixed and switched capacitors) can be achieved. In practice, the accuracy of a physical system will be limited by propagation delays or DC offsets causing error between the ideal tuning setting and actual operation of the fractional capacitor switch. Such a limit on the tuning accuracy can be considered as a limit on the tuning resolution, as there is a finite precision available for tuning. Furthermore, a completely continuous tuning resolution is not normally necessary for most practical applications, since tuning need only be good enough to meet a specification (for example, tuning to within the 3dB bandwidth of the LC tank circuit).

In order to fairly assess the tuning accuracy of a fractional capacitor system, it can be compared with the equivalent number of capacitors needed to achieve the same accuracy for the same operating Q factor. Figure 3-18 shows a binary-weighted tuning circuit, with a ΔC tuning capacitor and binary-weighted elements derived thereof. The tuning resolution for this circuit can be expressed in terms of the fixed capacitor ΔC and smallest selectable element $\delta C = \Delta C/2^N$, as per equation 3.21, where $\omega = 1/\sqrt{LC}$ and $\omega = 1/\sqrt{L(C+\delta C)}$. Where tuning to within the 3dB bandwidth is desired, the Q factor can be inserted in place of the ω terms.

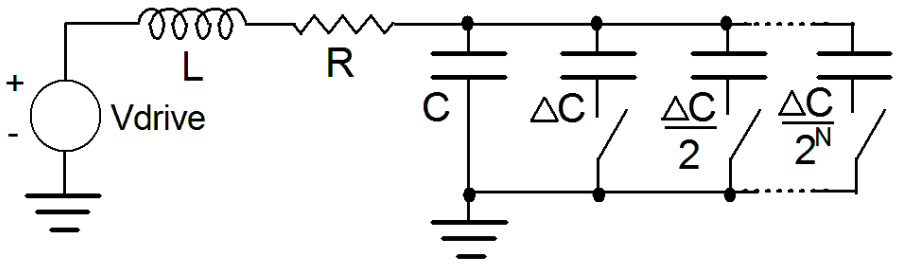

Figure 3-18: Binary weighted tuning, with fixed size C and ΔC weighted elements

$$\frac{\delta C}{C} = \left(\frac{\omega + \Delta\omega}{\omega}\right)^2 - 1 = \left(\frac{Q + 1}{Q}\right)^2 - 1 \qquad (3.21)$$

The tuning resolution may be translated into a number of capacitors by taking the log_2 of the inverse of the relationship in equation 3.22 and rounding up the result.

$$N_{cap} = \log_2 \frac{C}{\delta C} = \log_2 \left[\frac{1}{\left(\frac{\omega + \Delta\omega}{\omega}\right)^2 - 1}\right] = \log_2 \left[\frac{1}{\left(\frac{Q + 1}{Q}\right)^2 - 1}\right] \qquad (3.22)$$
$$= \log_2 \left[\frac{Q^2}{2Q + 1}\right]$$

Note that the tuning range must also be checked, to ensure that a sufficiently large range is covered. In equation 3.23, C_S is the sum of the selectable capacitors. Hence the sum of the selectable capacitors should be given as per equation 3.24.

$$\frac{\omega_{max}}{\omega_{min}} = \frac{1/\sqrt{LC}}{1/\sqrt{L(C + \sum_1^{N_{cap}} \frac{\delta C}{2^{N-1}})}} = \sqrt{\frac{C + C_S}{C}} \qquad (3.23)$$

$$C_S = \sum_{N=1}^{N_{cap}} \frac{\delta C}{2^{N-1}} = \left(\left(\frac{\omega_{max}}{\omega_{min}}\right)^2 - 1\right) C \qquad (3.24)$$

A numerical example can be computed, where compensation for 20% combined tolerances and tuning to within 3dB at operating Q of 50 are required. Equation 3.22 shows that 5 selectable capacitors are required. Equation 3.21 indicates that $\delta C \approx 0.0404\, C$. To meet the tolerance requirements, a tuning range of $\omega_{max}/\omega_{min} \approx 1.22$ is needed, hence $C_S \approx 0.488\, C$. To meet this second requirement, 4 selectable capacitors are needed, hence in this case the earlier requirement sets the number required.

3.2.4 Switch Voltage Ratings

When the capacitor switch is open, the voltage $v_{sw}(t)$ tracks the shape of $v_c(t)$. When the switch is open for the entire cycle, the amplitude of $v_c(t)$ and $v_{sw}(t)$ will be the same, hence the capacitor switch must be rated to withstand the maximum amplitude of $v_c(t)$, given by the product of the drive voltage and Q factor, which may be in the order of hundreds of volts. A high voltage device may therefore be required, incurring an increased cost.

If the switch is only opened for part of the cycle, the maximum amplitude of $v_{sw}(t)$ will be less than $v_c(t)$. This implies that the tune range may be traded-off with the maximum switch voltage rating. Figure 3-19 shows this graphically for a hypothetical system with a root-2 tune range, i.e. $C_1 = C_2$. The plot is normalised to act as a multiplier, such that when the $\theta_c = 0$ the maximum voltage observed by the switch will be equal to $V_{drive} \times Q$. Note that this assumes that losses in the LC circuit are dominated by the inductor and antenna driver, i.e. the contribution of the tuning switch resistance to the LC circuit

losses is negligible. A practical switch would have some finite on resistance, reducing the Q factor in the conduction cycle.

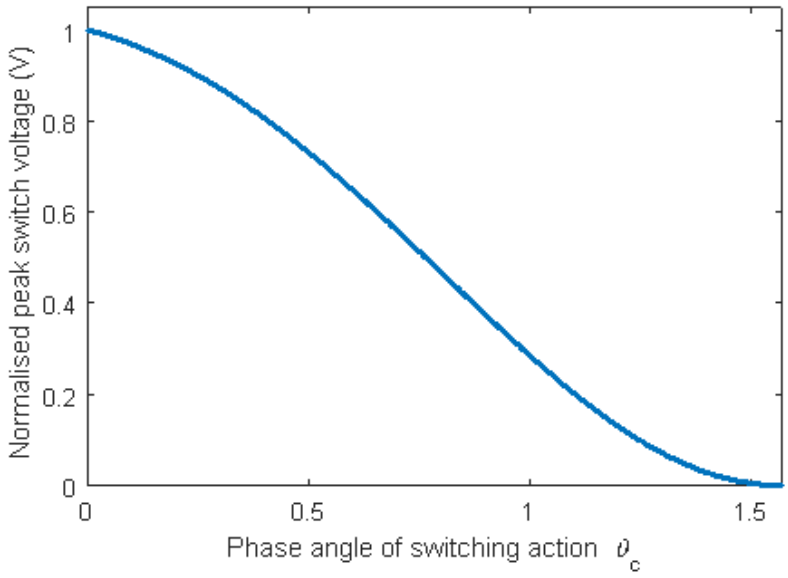

Figure 3-19: Normalised maximum switch voltage vs phase angle of switching action

Imposing a minimum value on the phase angle of switching action therefore results in a reduced peak voltage observed by the switch, at the expense of the available tune range. Alternatively, the amplitude of $v_{sw}(t)$ may be reduced with the architecture in figure 3-20. This divides the voltage across the capacitance, such that the observed voltage across the switch is a fraction of $v_c(t)$.

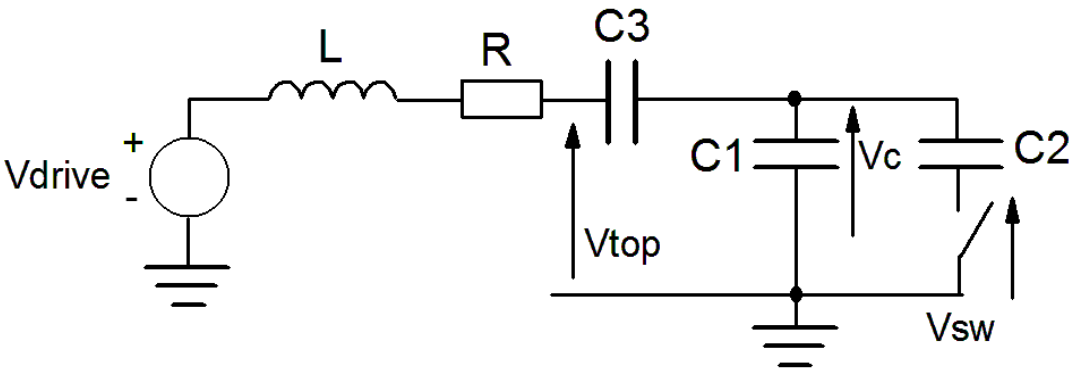

Figure 3-20: Switch voltage reduction by means of capacitive division

The maximum amplitude of V_C, and hence maximum possible amplitude of V_{SW}, is now determined by the capacitive divider ratio formed by C_3 and C_1. The value of C_2 need not be considered for working out the maximum switch voltage, since it is excluded from the divider when the switch is open. The division ratio n is given by equation 3.25, such that the peak capacitor voltage is given by $V_{DR} \times Q \times n$. As C_3 is decreased, the division ratio decreases, i.e. the maximum switch voltage decreases for a given value of V_{TOP}.

$$\left|\frac{V_c}{V_{TOP}}\right| = \left|\frac{Z_{C_1}}{Z_{C_1} + Z_{C_3}}\right| = \left|\frac{\frac{1}{j\omega C_1}}{\frac{1}{j\omega C_1} + \frac{1}{j\omega C_3}}\right| = \frac{C_3}{C_1 + C_3} = n \qquad (3.25)$$

Using this method, the effective capacitance in the LC tank is now determined by the series combination of C_3 with C_1 and C_2, the maximum and minimum frequencies given as per equations 3.26 and 3.27 respectively.

$$\omega_{max} = \frac{1}{\sqrt{L(C_3||C_2)}} = \frac{1}{\sqrt{L(\frac{C_2C_3}{C_2 + C_3})}} \quad (3.26)$$

$$\omega_{min} = \frac{1}{\sqrt{L(C_3||(C_1 + C_2))}} = \frac{1}{\sqrt{L(\frac{(C_1 + C_2)C_3}{C_1 + C_2 + C_3})}} \quad (3.27)$$

If $C_1 = C_2$, then the tuning range becomes

$$\frac{\omega_{max}}{\omega_{min}} = \frac{\frac{1}{\sqrt{L(\frac{C_1C_3}{C_1 + C_3})}}}{\frac{1}{\sqrt{L(\frac{2C_1C_3}{2C_1 + C_3})}}} = \frac{\sqrt{2}\sqrt{C_1 + C_3}}{\sqrt{2C_1 + C_3}} \quad (3.28)$$

Hence as C_3 is decreased in order to reduce the maximum amplitude of V_{SW}, the available tune range tends towards 1. Figure 3-21 compares the normalised peak switch voltage against the available tune range for both methods of switch voltage reduction, for the case where $C_1 = C_2$. As is expected, the switch voltage is reduced where the tune range is restricted for both methods, although the method of capacitive division yields a slightly greater reduction for a given tune range. Capacitive division has the added advantage that it is inherently safe, by providing a physical limit on V_{SW} with respect to V_C regardless of the tuning setting.

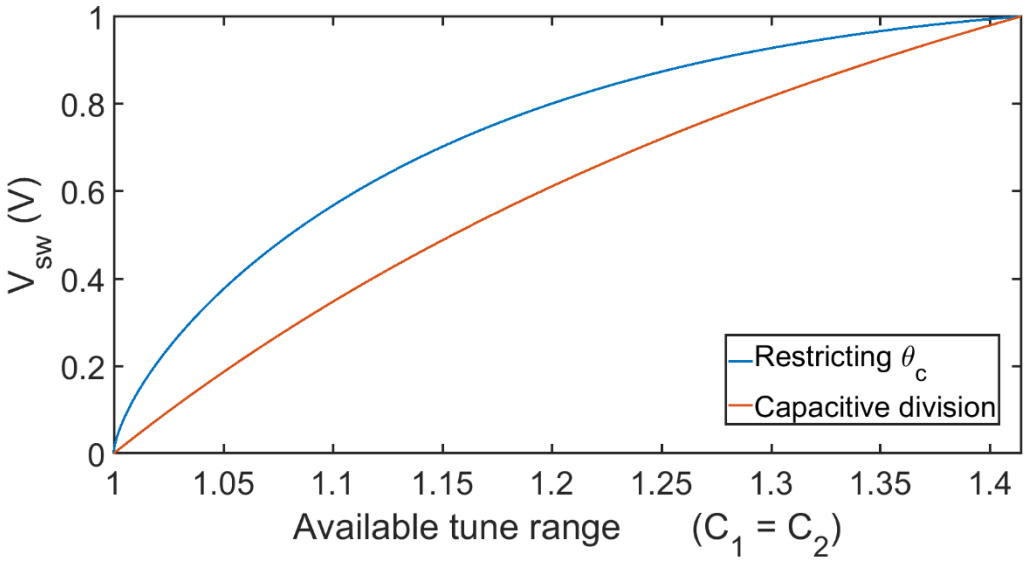

Figure 3-21: Normalised peak switch voltage vs available tune range, comparing methods of switch voltage reduction: θ_c restriction and capacitive division ($C_1 = C_2$ for both cases)

3.2.5 Continuous Self-Tuning Concept

It has been shown so far that the new tuning method allows for wide-range and fast retuning of an LC circuit with a single additional capacitor and without the need for long settling time after the frequency change. The new tuning method also inherently provides a metric to determine the current resonance condition.

The tuning state may be determined by the voltage across the capacitor switch $v_{sw}(t)$. From t = 0 to t_c, the switch is closed and therefore $v_{sw}(t)$ is equal to the ground potential. When the switch is opened, there is no longer any current flow through C_2 and $v_{sw}(t)$ tracks the AC component of the tank voltage $v_c(t)$. Since it is necessary for zero-voltage switching that the fractional tuning timings are symmetrical at resonance, the switch opens and closes symmetrically around the peaks and troughs of $v_c(t)$. This also implies that, when in tune, excursions $v_{sw}(t)$ will start and end at exactly 0V.

If the LC tank is not correctly tuned, this implies that the chosen value of t_c is either too great or too small, such that the zero-voltage condition of $v_{sw}(t)$ is no longer met. If t_c is too large, the switch will be closed before $v_{sw}(t)$ has returned to 0V. If t_c is too small, the switch will close after $v_{sw}(t)$ has crossed 0V. In both scenarios, the closure of the switch when $v_{sw}(t) \neq 0V$ creates a discontinuous change in the $v_c(t)$ waveform, caused by the difference in $v_c(t)$ and the stored voltage on C2.

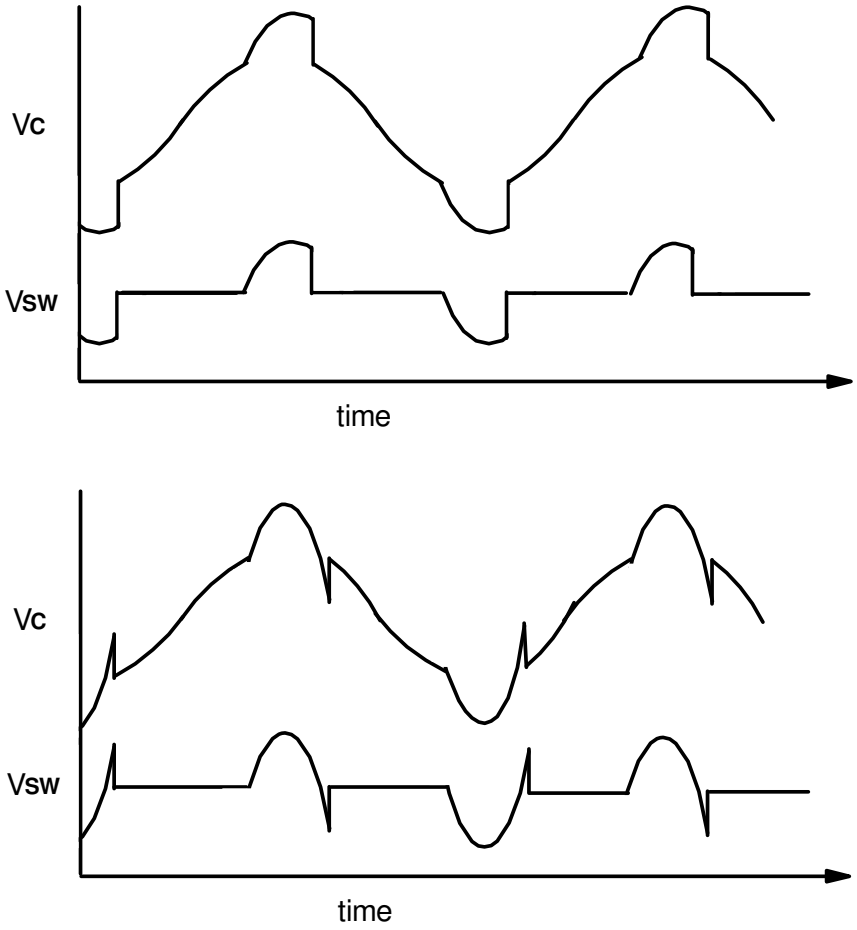

Figure 3-22: Incorrect tune setting examples. Top: switch not open for long enough, modified frequency is too low. Bottom: switch open for too long, modified frequency too high

The ability to determine the tuning condition from detecting the sign of $v_{sw}(t)$ makes the new tuning method very convenient for a self-tuning controller. Consider the final value of the $v_{sw}(t)$ excursion, i.e. just before the switch is closed. The sign of $v_{sw}(t)$ at this moment indicates whether t_c is too large or too small. Hence, the tuning method provides a metric for convenient self-tuning, since it is inherently known in which direction the tune setting needs to be adjusted in order to achieve resonance.

Furthermore, the opportunity to obtain tuning information is presented twice per cycle, meaning that transient detuning may be detected in less than one period of oscillation. This allows for continual monitoring of the resonant condition and the opportunity for very fast correction of such transient detuning.

3.2.6 Automatic Tuning

As previously discussed, the fractional capacitor tuning method provides a metric to determine the tuning state of the circuit. This information is available from the sign of $v_{sw}(t)$ just before the switch is closed. In order to capture this information, a comparator with the reference voltage tied to the switch ground potential may be connected to $v_{sw}(t)$.

Since θ_h and θ_l control the switch action, they may also be used to indicate the moment at which sampling of the sign should occur. According to the timing diagram in figure 3-11, a rising edge on either of the theta signals means that the switch is about to close. Figure 3-23 shows two architectures where the rising edges of θ_h and θ_l are used by D-type flip-flops in order to capture the sign information.

The sign information itself must be captured just before the switch is closed. Therefore, there must be some time delay between the capture of this information and the closing action of the switch. Figure 3-23 shows that this may be implemented by adding a pure time delay either to the switch action itself, or to the output of the comparator. The second option is preferable, as the first creates a small amount of phase offset between the tank drive and the switch control, which may lead to additional detuning.

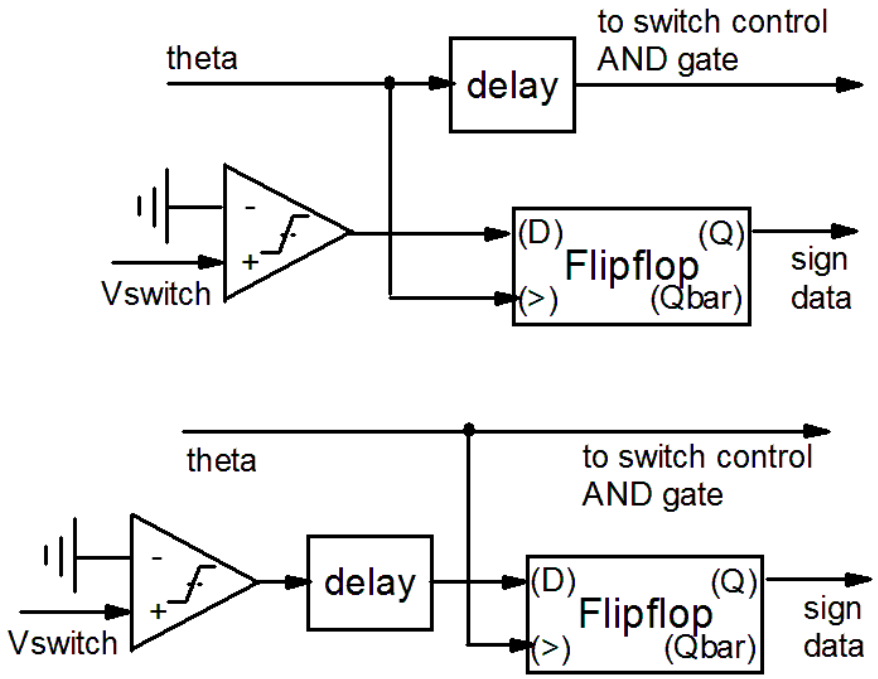

Figure 3-23: Switch voltage sign detection options. Top: delaying the switch control. Bottom: delaying the sign data.

Figure 3-24 shows how a small delay in the output of the integrator can ensure that valid sign information is sampled by the flip-flop. On the left, the switch is open for too short an interval, resulting in the final voltage of the positive excursion being above the ground rail. The delayed sign signal is high at the moment the switch closes, ensuring that the sampled sign is correct.

On the right, the switch voltage excursion has crossed the rail. The delayed sign signal is only delayed by a short amount, such that correct sign data is sampled. If the delay is too long, the sign will be incorrectly detected. Hence a balance must be struck in the value of the delay, which must be long enough for the hold time of the flip-flop but also short enough to ensure that it is still representative of the final value of the switch voltage excursion.

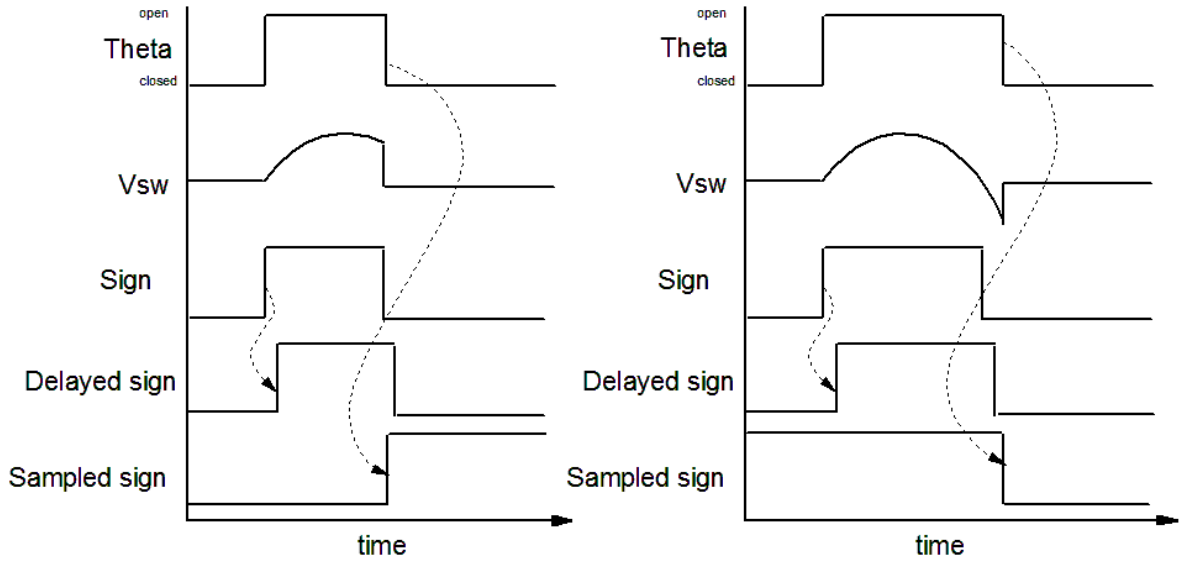

Figure 3-24: Switch voltage sign sampling timings. Left: positive sign detected, Right: negative sign detected

The captured sign of the switch voltage only determines in which direction the tuning control voltage must go, hence the sign information may be integrated over multiple cycles in order to reach the correct tuning voltage. An integrator with a large time constant will take longer to self-tune, however transient detuning will not cause the tuning control voltage to vary dramatically and hence a stable tuning condition may be reached.

Figure 3-25 shows the integration waveform of self-tune system. Note that whilst the optimal tune condition is reached, the integration function causes the tune setting to oscillate around the optimal point. If a small time constant is used, the control loop will reach the optimal tune point faster, however it will also overshoot it by a greater amount. This may result in overall poorer tuning of the system due to the slice voltages deviating greatly from the optimal tune point.

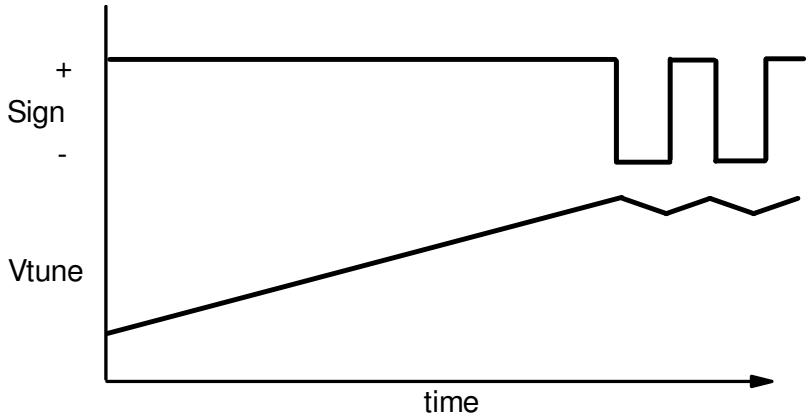

Figure 3-25: Integration using sign data from a single excursion of the switch voltage

More information may be gathered if the sign from both excursions is captured as per figure 3-26. If the captured sign from the positive and negative excursions give conflicting information (i.e. one indicates that t_c is too large whilst the other indicates that t_c is too small) then the self-tuning integrator can remain locked until new information is available. Such a situation is most likely to occur when the tune setting is close to optimal. Temporary transient minor detuning will not necessarily cause the tune voltage to change, improving the stability of the system. Only when the system becomes significantly detuned will the integrator change value.

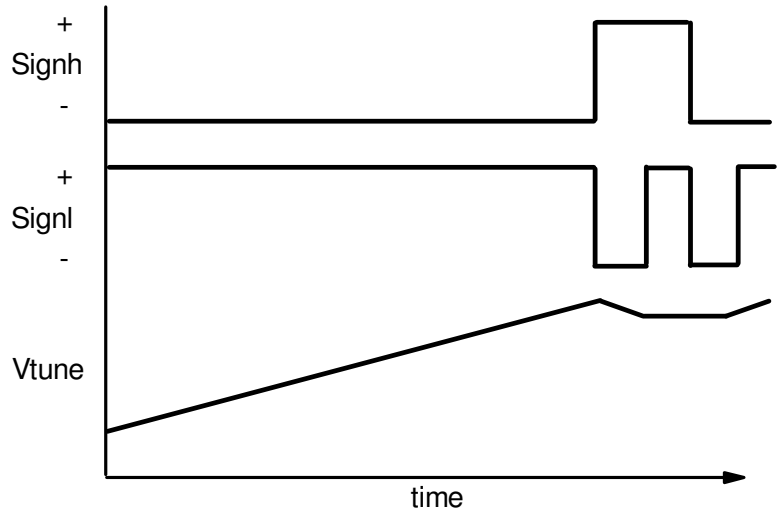

Figure 3-26: Integration using sign data from both excursions of the switch voltage, providing more stability in the integrator output

A more advanced control loop may be realised by sampling the switch voltage more often. The switch voltage excursion may be interpolated as per figure 3-27, such that its final value can be predicted before it occurs. A proportional response can be applied to the estimated time error to allow for a very rapid response to detuning without the large overshoot caused by a simple integrator loop.

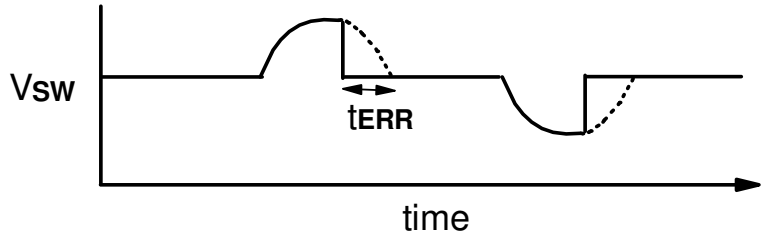

Figure 3-27: Estimation of tune timing offset t_{err} by interpolation

The resonance detection method using the sign of V_{SW} was simulated in LTSpice, building upon the previous 8-12kHz simulation with the block diagram in figure 3-28. A full schematic is provided in appendix B.

An active integrator similar to the triangle generator was used to create the V_{TUNE} voltages from the captured sign data, providing a fixed common-mode voltage at the input of the integrator so that a simple resistor connected directly to the output of the flipflops could be used to achieve a DC integration current. A lower time constant was required to provide a steady tuning setting at resonance, so a lower current of 50µA and integration capacitance of 500nF was used, so that at 10kHz the V_{TUNE} voltages would only change by approximately 10mV per cycle, i.e. approximately 0.4% of the tuning range.

Note that it was not necessary to insert an additional delay to enforce that sign detection took place just before the closure of the tuning switch, since the comparator model included a propagation delay to achieve the same effect.

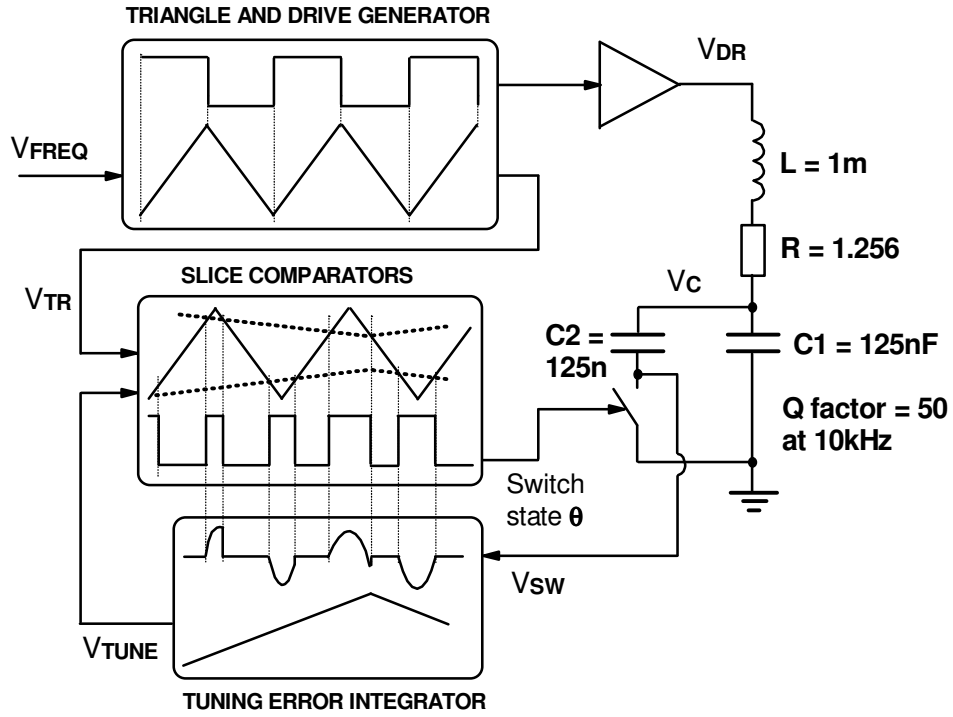

Figure 3-28: Block diagram of self-tuning simulation

Figure 3-29 shows the system self-tuning at 10kHz. The slice voltage V_{TUNE+} begins at the midpoint of the triangle, and is increased by the integrator until it reaches a steady state at the correct optimum V_{TUNE} voltages. Some ripple can be seen in the steady-state value of the V_{TUNE} voltages, indicating the tuning loop is still running and tracking the resonant condition.

Figure 3-30 shows the effect of reducing the tuning loop time constant by a factor of approximately 15x, by reducing the capacitance to 33nF. The system reaches the steady state quicker, however there is a greater ripple in the steady-state values. The adjustment of V_{TUNE} between each cycle is such that there is visible detuning on V_{SW}. The steady-state RMS amplitude of V_C is reduced from approximately 114V to 108V due to the resultant detuning. Hence there is a trade-off between a fast response time and settled tuning accuracy.

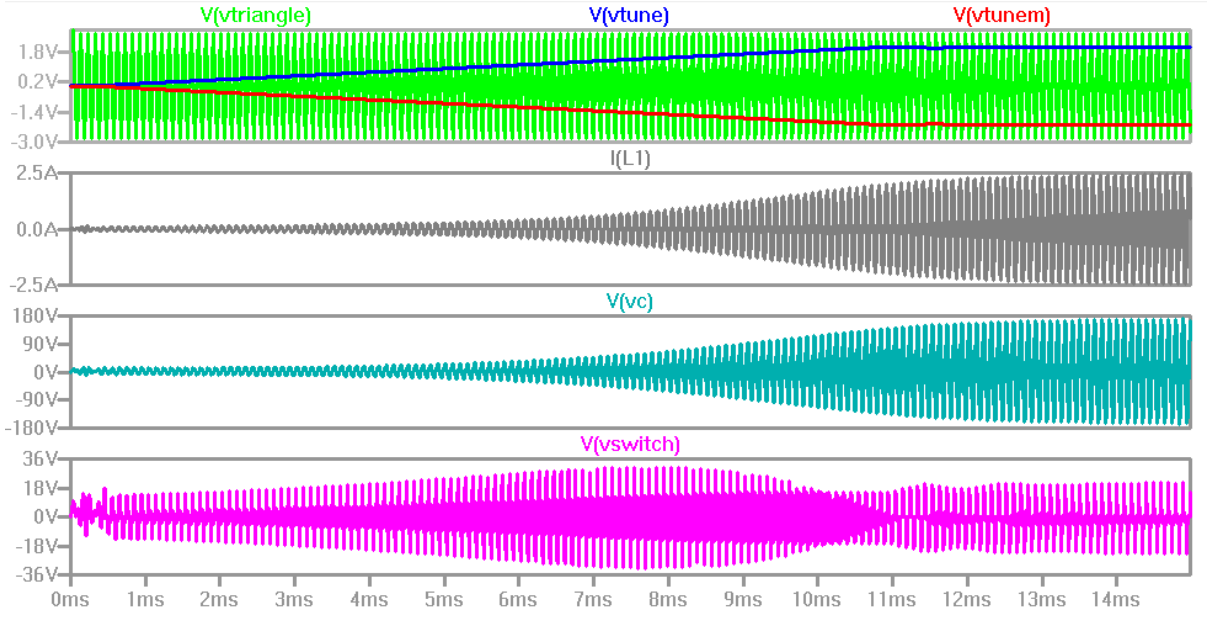

Figure 3-29: Fractional capacitance self-tuning at 10kHz

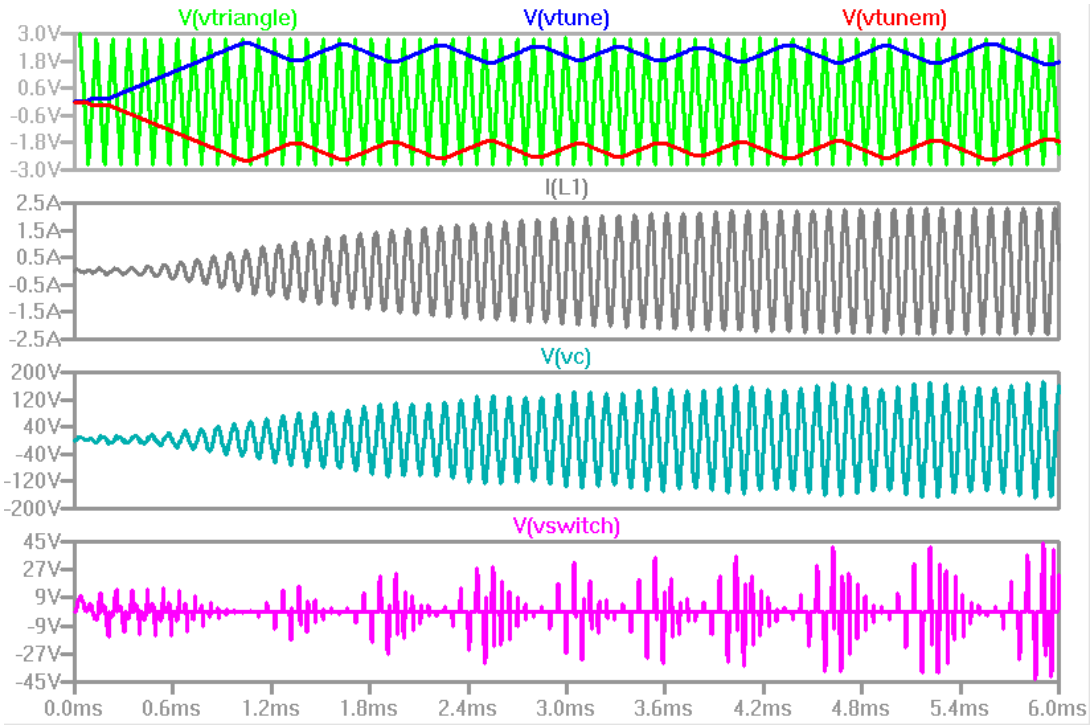

Figure 3-30: Self-tuning with 15x integration time constant

The transient effect of detuning the resonant LC circuit is shown in figure 3-31. The system is permitted to achieve resonance from an untuned state, then an additional fixed capacitance of 25nF is connected between V_C and ground at 18ms. The tuning loop quickly identifies that the system is no longer resonating and adjusts the V_{TUNE} voltages to compensate. The switch is opened for a higher duty cycle to reduce the average antenna capacitance back to the optimal value, indicated by the larger excursions on V_{SW}. The system has returned to resonance within 5ms in this case.

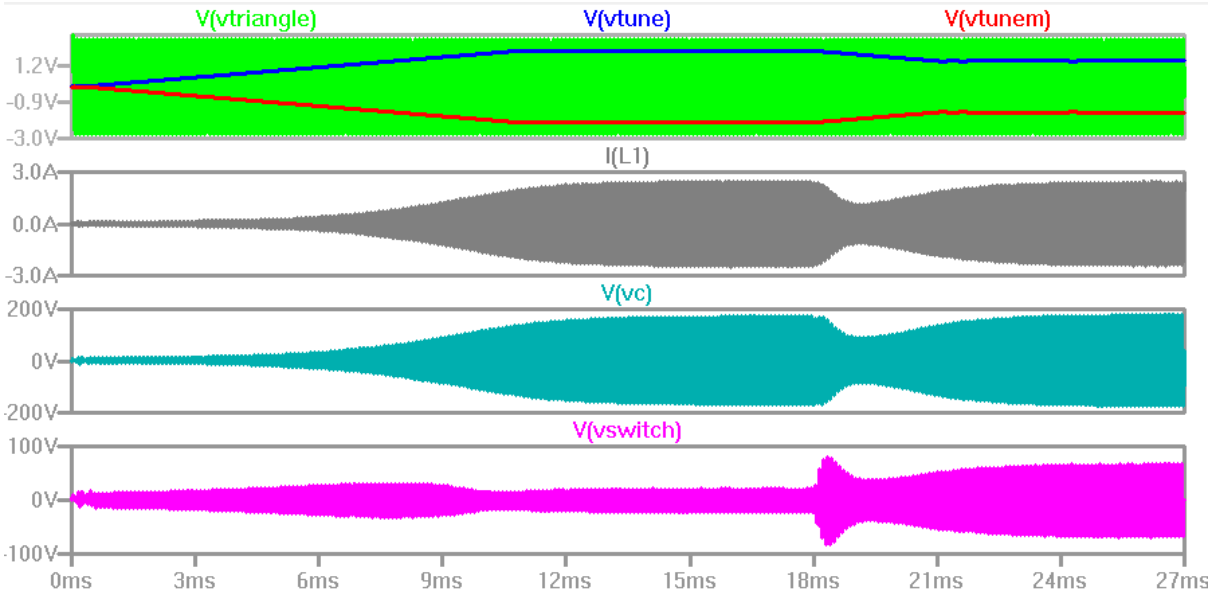

Figure 3-31: Self-tuning response to a step increase of 25nF in LC antenna at 10kHz operating frequency

3.3 Summary of zero-voltage switched fractional capacitance

It has been shown how continuous tuning can be achieved using the zero-voltage switched fractional capacitance method. The resonant antenna is tuned by switching a single tuning capacitor in and out of the circuit for part of each cycle to create a time-averaged resonant frequency. A zero-voltage switching criterion is enforced on the tuning switch to minimise losses and ensure that the circulating current in the inductive antenna remains essentially sinusoidal. The exact resonant frequency is set by the duty cycle of switching on the tuning capacitor, hence with completely analogue timing generation the available tuning range is essentially continuous. This allows precise tuning for high Q without the need for large banks of static tuning capacitors, reducing hardware costs. The tuning range available is set by the size of the fixed and switched capacitors, hence a wide tuning range can be set to compensate for the expected detuning effects which may occur.

Observation of the voltage excursion on the tuning switch determines if the switching duty cycle is correct. The sign of the voltage excursion just before tuning switch closure determines if the resonant setting is too high or too low. This information can be used to adjust the switching duty cycle accordingly, automatically adjusting the system to resonance. The tuning switch is operated twice per cycle, permitting continuous foreground detection of the resonant condition, hence background calibration is not necessary.

The tuning method has been simulated using LTspice. The next chapter describes the implementation of the method using discrete components on a circuit board. This helps identify any practical issues which would otherwise not be revealed by simulation. The problems of tuning switch voltage rating and the need for an accurate sampling instant have already been foreseen and solutions proposed.

4 Implementation of zero-voltage fractional capacitance tuning with discrete components

This chapter details the implementation and measurement of the zero-voltage fractional capacitance tuning method with discrete components, in order to investigate system-level issues which may affect an IC implementation which are not apparent in idealised LTSpice simulation. A fully self-tuning system is created for operation in the 10kHz region. A fixed-tuning version created for operation in the 125kHz region to explore the effects of hardware propagation delays on the tuning timing accuracy. Full schematics for the breadboard is included in appendix C.

4.1 8-12kHz implementation

Unlike previous LTSpice simulation, a physical implementation of the antenna drive and tuning system has physical limitations which require consideration. Figure 4-1 shows the 10kHz block diagram, with critical issues highlighted for each part.

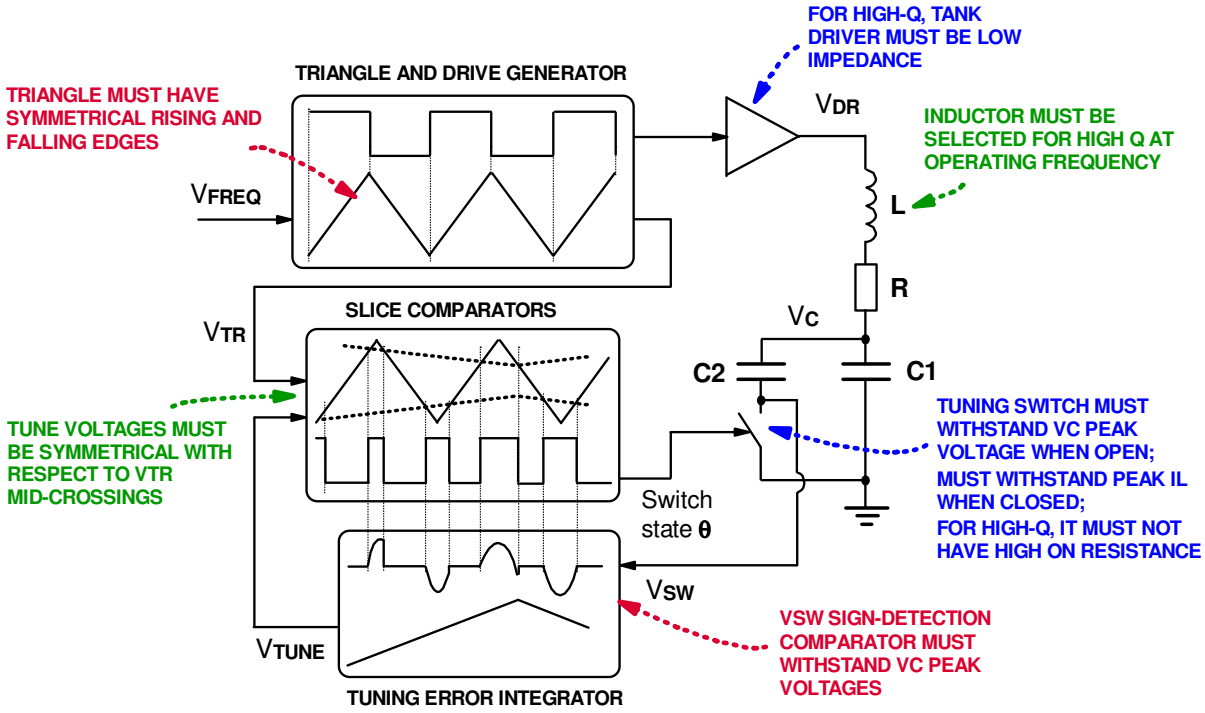

Figure 4-1: 10kHz region breadboard block diagram, indicating key implementation issues

Symmetrical switching of the tuning switch on the positive and negative excursions required a symmetrical triangle wave V_{TR}. Any differences in the positive and negative ramp current would skew the triangle and violate this condition. It was also preferable to set both the positive and negative current from a single reference for convenient frequency adjustment. A voltage-to-current circuit was used with PNP and NPN transistors to mirror the current and provide the up/down ramp references. The current integrator oscillator and RS latch were constructed with a readily-available TL081 opamp and 7400 series logic respectively. Figure 4-2 shows the V_{TR} and V_{DR} signals operating correctly at 12.29kHz. Glitches are visible near the trough of V_{TR}, caused by high transient current drawn by the comparators used. For this breadboard, the glitch is sufficiently high in frequency that undesirable glitching on the antenna tuning switch does not occur, however an integrated circuit will require a more ideal timing reference to avoid this behaviour.

The tuning technique for the LC circuit assumes that an ideal high-voltage bi-directional switch is used. In practice, a real switch will have a finite resistance when closed, which must be small in order to prevent the LC antenna Q factor from being degraded. The switch must also be able to open/close

sufficiently fast to avoid creating a timing offset in the switching action. The switch must be able to withstand the positive and negative peak voltages on V_C (which occurs at maximum frequency, when the switch is fully open for the entire cycle). It must also be rated to withstand the circulating current in the inductor when closed.

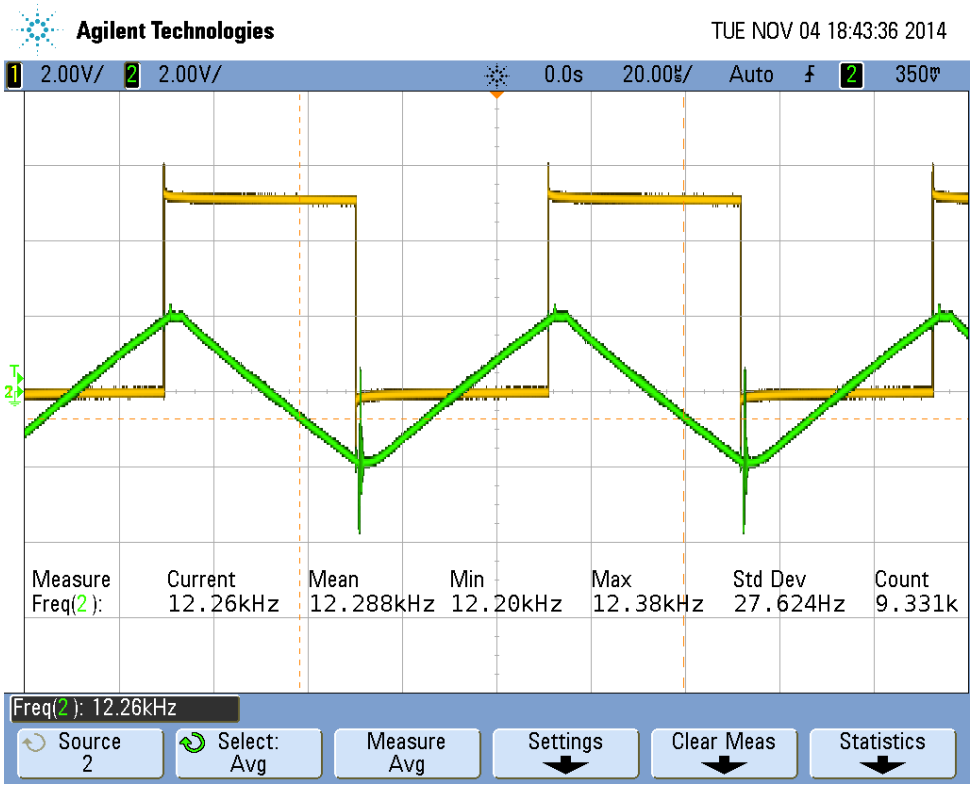

Figure 4-2: Breadboard triangle wave and tank drive signals at 12.29kHz. Yellow: tank drive, Green: triangle wave

An ADG452 quad transmission gate IC was used for the tuning switch. On a dual-rail 5V supply the typical output resistance of a single switch is approximately 7Ω [34], so all four switches were placed in parallel so that the overall resistance would be under 2Ω. The propagation delay is approximately 70ns, avoiding significant timing skew in the frequency range used. The switch-closed current rating is 100mA continuous and with a 5V dual supply the excursion on V_{SW} must be limited to 5V maximum.

Whilst the amplitude of V_{SW} must be controlled, the Q factor must be sufficiently high to demonstrate the effectiveness of the tuning method on a realistic antenna circuit. Hence the amplitude of V_C should be reduced not by reducing the Q factor but by reducing the drive voltage amplitude V_{DR}. An off-the-shelf 3.3mH inductor with 8Ω loss resistance at 10kHz was chosen, permitting a Q factor of approximately 25 at this frequency. Fixed and fractional capacitances of 47nF and 68nF respectively were chosen, providing a 1.56:1 maximum:minimum antenna tuning range to operate across the triangle generator operating range.

Figure 4-3 shows two approaches considered for controlling the amplitude of V_{DR} to protect the HV switch from damage. On the left, a level-shifted driver from a variable supply provides the correct gate voltages to PMOS and NMOS devices to provide a low-voltage drive amplitude directly to the LC circuit. This requires additional circuitry which must operate symmetrically (i.e. the NMOS and PMOS switches must align correctly with the ideal 50% duty cycle of V_{DR}.

On the right, a nominal supply voltage drive reference is attenuated. This removes the need for level-shifted gate drivers and also relaxes the output impedance constraints on the driver, since the LC antenna circuit Q factor is dominated affected by the parallel impedance of the attenuator and not the driver. Given the ready availability of 74HCT125 driver ICs, the second option was chosen to reduce the

breadboard complexity. With the combined impedances of the inductor, HV switch and attenuator, it was expected that the Q factor be reduced from 25 to approximately 12.

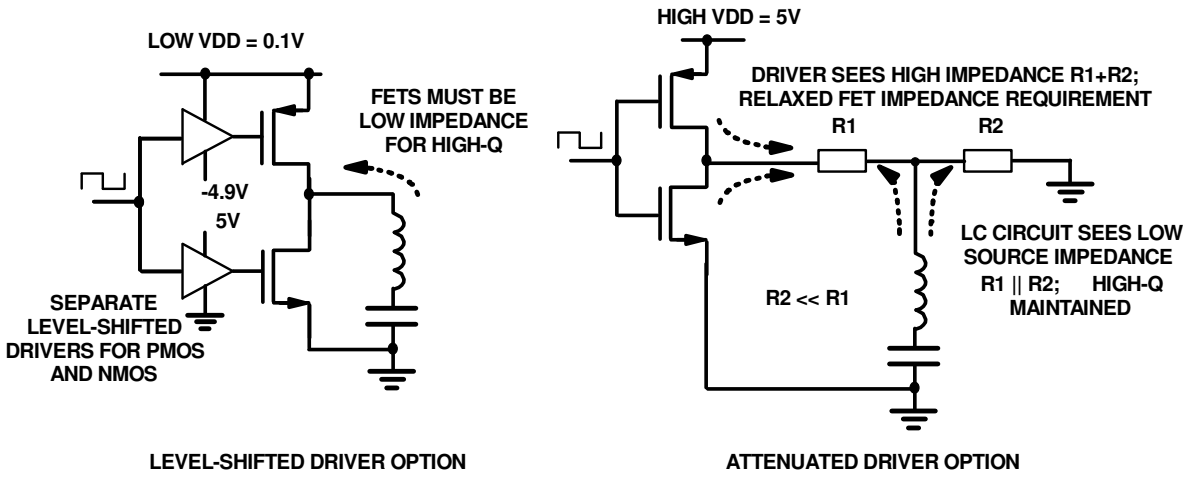

Figure 4-3: Circuit configuration options for reducing V_C whilst maintaining high Q

Figures 4-4 and 4-5 show the system resonating at opposite ends of the antenna tuning range, showing V_C and the HV switch enable signal. Note that the antenna is a of an insufficient Q factor to fully attenuate the switching noise of the comparators, and glitching can be seen on the V_C waveforms. At 12.42kHz, the switch is open for most of the cycle, with brief closure instants near the zero-crossings of V_C. At 8.43kHz, the switch is closed for most of the cycle, with short opening durations around the peaks and troughs of V_C. The amplitude of V_C is approximately 1V pk-pk, well within the safe range for the ADG452 switch.

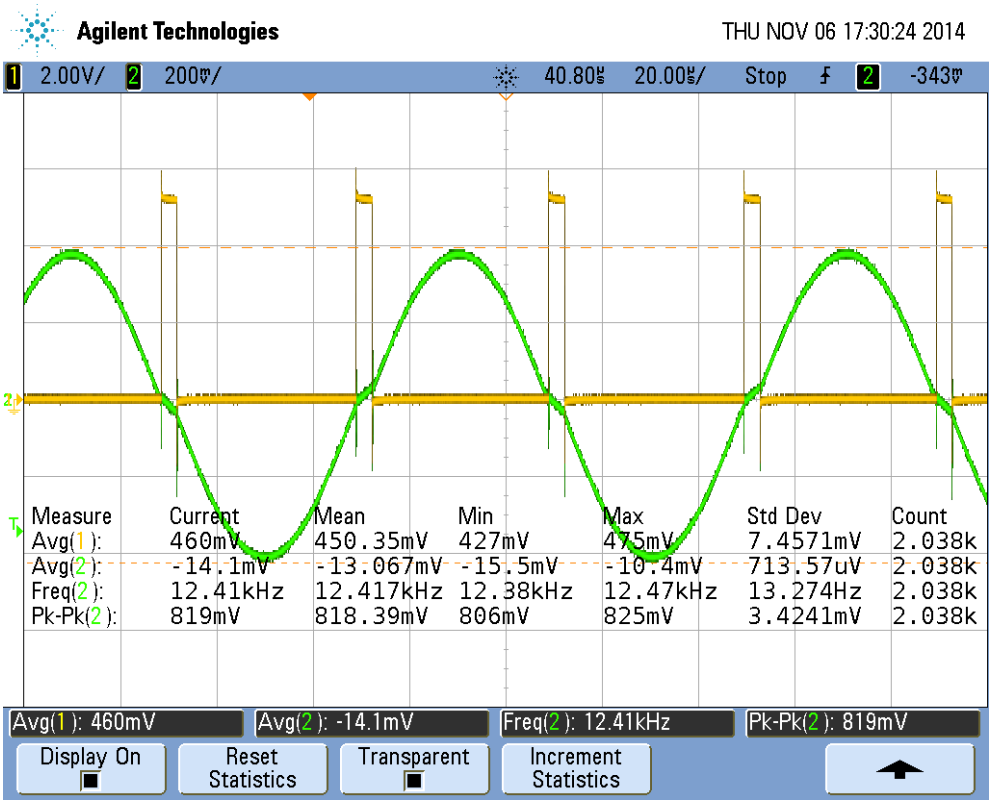

Figure 4-4: Breadboard operation of tuning at 12.42kHz. Yellow: switch enable, Green: V_C

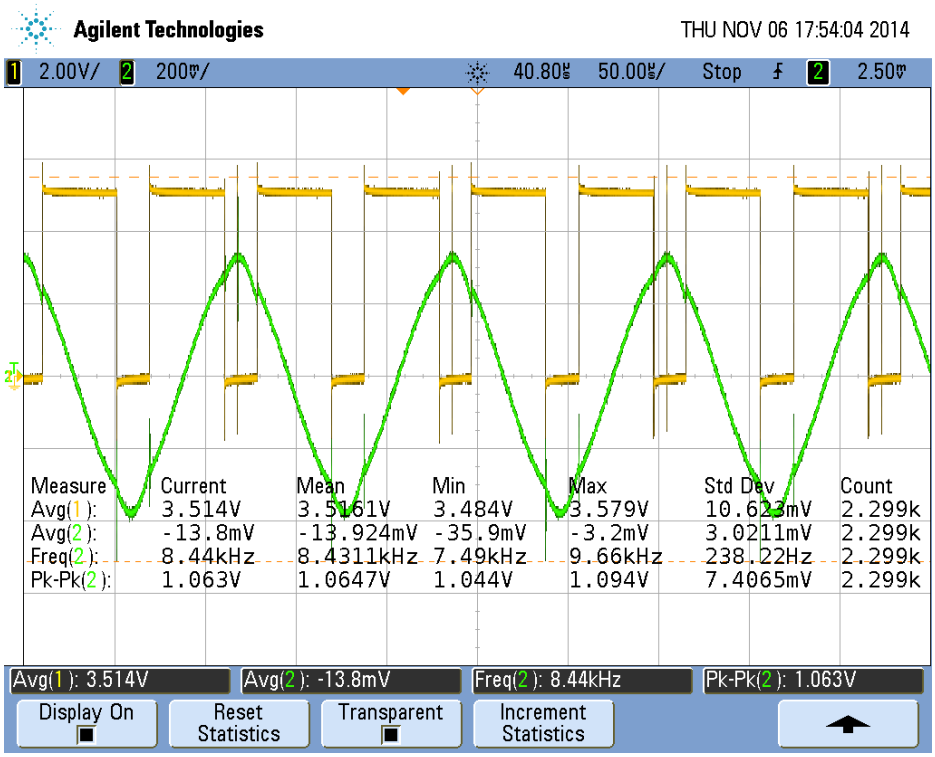

Figure 4-5: Breadboard operation of tuning at 8.43kHz. Yellow: switch enable, Green: V_c

It was found that the HV switch must operate for a minimum duration each cycle, in order to capture information about the resonant condition. Hence, it cannot remain fully open or fully closed, so there is a slight reduction in the practical tuning range maximum:minimum frequency to 1.43:1. The circuit to create V_{TUNE} from the tuning error must also not set V_{TUNE} outside the limits of V_{TR}, otherwise the HV switch will not open. Figure 4-6 shows operation the bottom and top end operating frequencies where the discrete circuit was able to self-tune correctly. An integrated system needs to enforce these requirements so that it does not go out of bounds and become unable to self-tune.

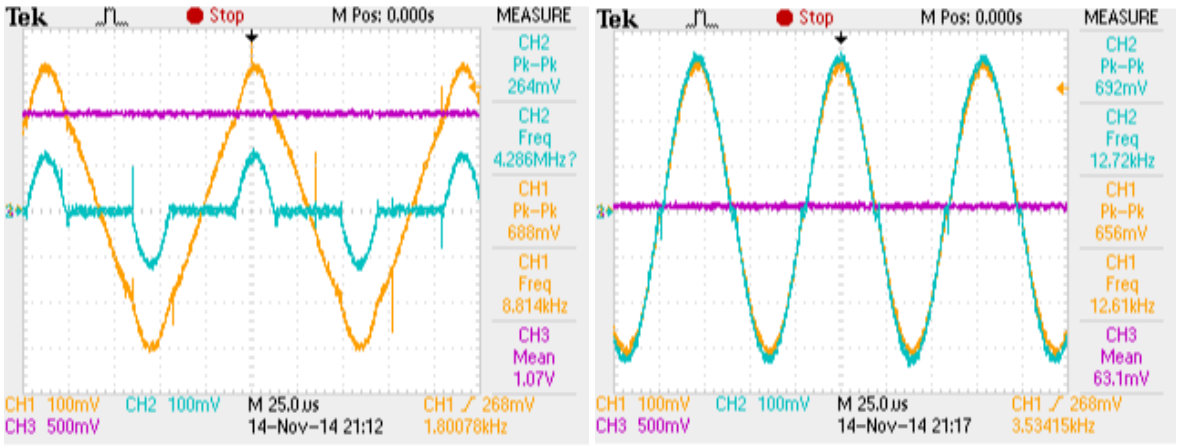

Figure 4-6: Breadboard self-tuning at 8.81kHz (left) and 12.61kHz (right). Orange: V_C. Blue: V_{SW}. Purple: V_{TUNE}

Figure 4-7 shows self-tuning once a step change in frequency occurs, stepping from the opposite near-extremes of the available tuning range. In each case, V_{TUNE} ramps up and down accordingly, taking approximately 2.4ms to stabilise on the new optimum tune setting in each case. V_{FREQ} is the VCO tuning input voltage used for triangle generation, being stepped by an external function generator at 100Hz. The V_{SW} signal has been scaled so that all waveforms may be visible. Figure 4-8 shows the transition from 12kHz to 8kHz and the increase in V_C as V_{TUNE} reaches the correct value for resonance.

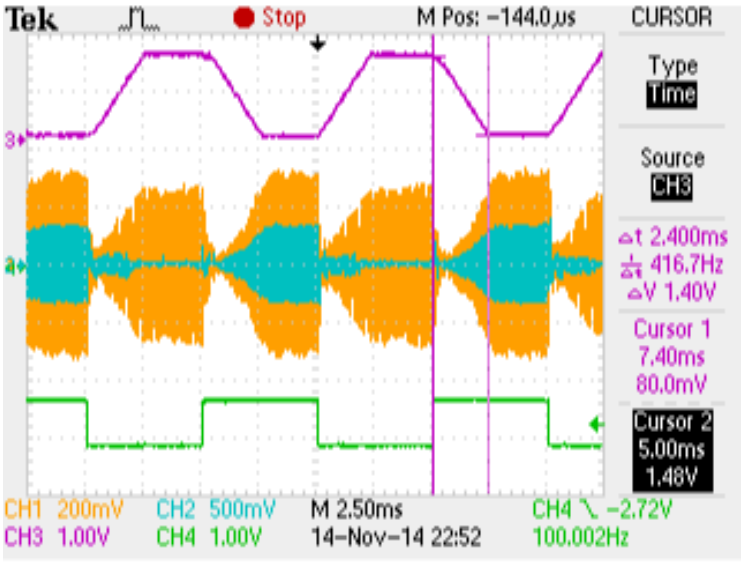

Figure 4-7: Breadboard self-tuning with wideband step frequency change. Orange: V_C. Blue: V_{SW}. Purple: V_{TUNE} Green: V_{FREQ}

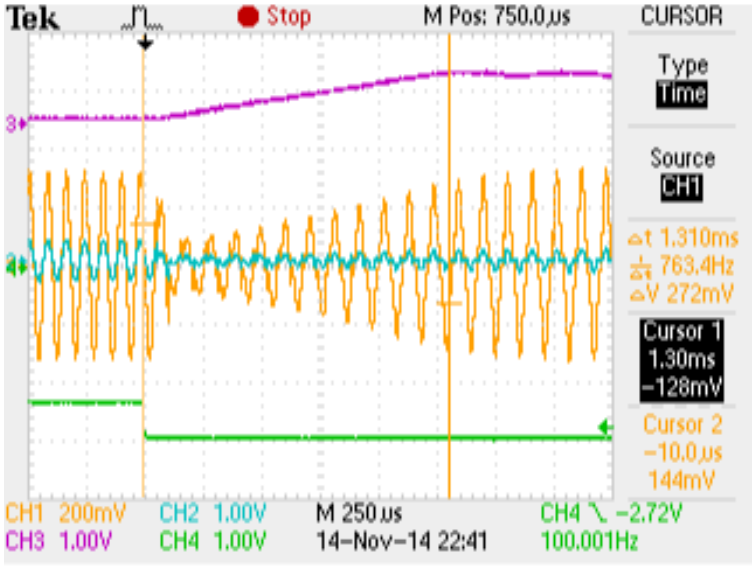

Figure 4-8: Close-up of frequency transition from approximately 12kHz to 8kHz on breadboard. Orange: V_c. Blue: V_{switch}. Purple: V_{tune}. Green: V_{freq}

4.2 125kHz implementation

From the simulation and breadboard experiments conducted, it is clear that the fractional capacitor technique is a viable method for tuning an LC tank. However, the operating frequency was quite low and not representative of a realistic WPC system, where the resonant frequency is usually higher (for example in the region of 125kHz [35]). At this higher frequency, the effect of propagation delays in the antenna and switch driver chains become more significant, requiring a different approach to timing generation. For this reason, a bench triangle wave generator was used to provide the triangular waveform, from which all other signals were derived. The additional circuitry for automatic tuning control was not necessary in this experiment, as the timing requirements for this had already been established, i.e. the sign of V_{SW} must be sampled immediately before the closure of the tuning switch. Focus was instead on the effect of timing mismatch between the switch control and antenna driver. A level shifted driver was instead considered for the antenna driver to explore the feasibility in an IC

implementation. Figure 4-9 shows the adjusted system diagram for basic tuning (i.e. no automatic tuning control). The full schematic is in appendix C.

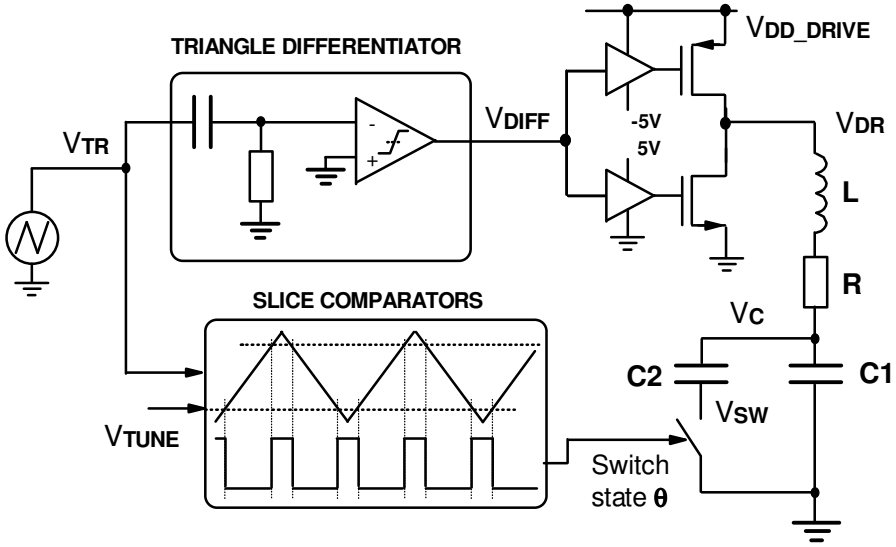

Figure 4-9: Circuit block diagram for 125kHz breadboard implementation with triangle differentiator and level-shifted antenna drive

Figure 4-10 shows the flow of signals between the triangle and the LC tank, listing the primary delay component of each stage and how much delay is created as result. The average timing offset between the tank drive and switch action per cycle was expected to be approximately 92ns, which equates to approximately 4.1 degrees of phase offset at 125kHz. This timing offset would ideally be completely balanced to minimise the tuning error.

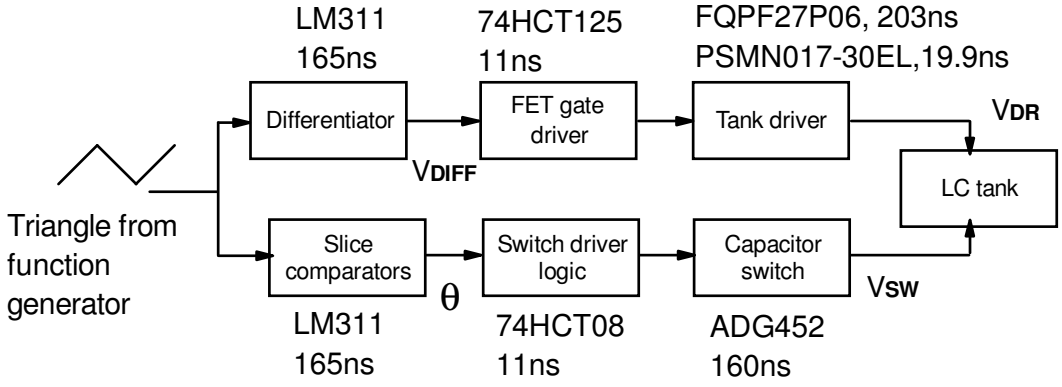

Figure 4-10: Critical timing chain for 125kHz breadboard

A new air-core inductor was manually wound using PVC piping as a former, allowing both easy construction and adjustment of the inductance (inductor design is covered in appendix A). An inductance of 134μH was experimentally obtained with a measured parasitic resistance of 1.3Ω at 100kHz on an LCR meter. The inherent Q factor of the tank was expected to be approximately 88 at 125kHz. Using the level-shifted drivers, the amplitude of V_{DR} was reduced to approximately 110mV, keeping the pk-pk amplitude of V_C below 10V to protect the ADG452 switch IC.

Figures 4-11 left and right show operation at the minimum and maximum frequencies respectively. At minimum frequency the switch voltage V_{SW} remains at zero for the entire cycle, whilst at maximum frequency it tracks the shape of V_C. Fixed and fractional capacitances of 6.1nF were used for a target tuning range of 1.41:1, however it was found that the tuning range was reduced to around 1.36:1

(maximum:minimum 155.7-114kHz resonant frequencies), meaning a parasitic capacitance of around 1.7nF to ground was present.

The phase offset between the tank drive and capacitor switching action was measured to be approximately 42ns, which was better than predicted and sufficient for visually-accurate tuning. However, it is still desirable to keep this phase error low, so the effect of propagation delays at each stage of timing generation must be considered in an IC implementation.

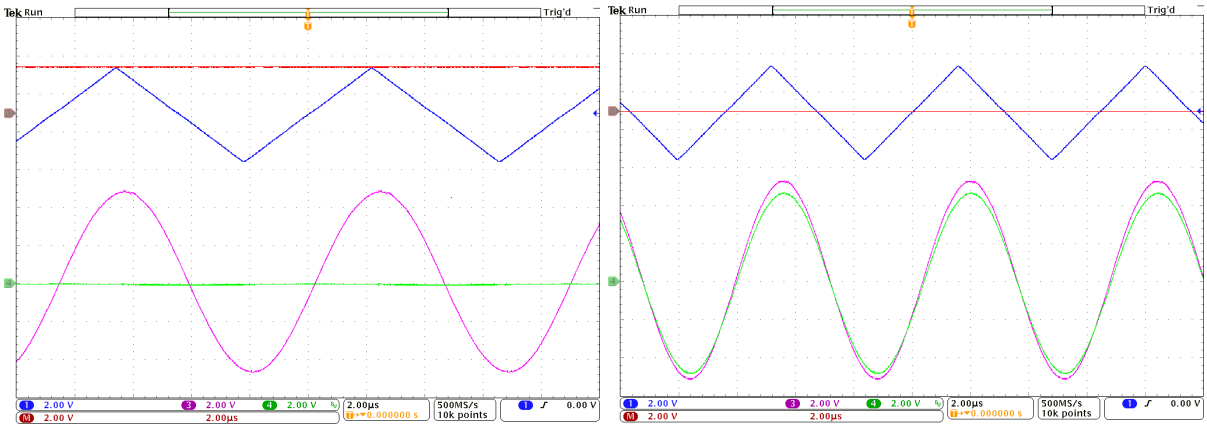

Figure 4-11: 125kHz breadboard running at 114kHz (left) and 155.7kHz (right): Blue: V_{TR}, Red: V_{TUNE+}, Pink: V_C, Green: V_{SW}

Figure 4-12 shows the system in tune at the mid-range frequency 134.85kHz, with off-tune condition in figures 4-13 left and right. The parasitic inductances and capacitances in the wires connecting the LC tank to the switch are made visible by the ringing which occurs at the moment the switch closes in the detuned examples. Since the switch is closing when there is a non-zero voltage across it, a high transient current briefly flows and excites the resonant frequency of the parasitic components.

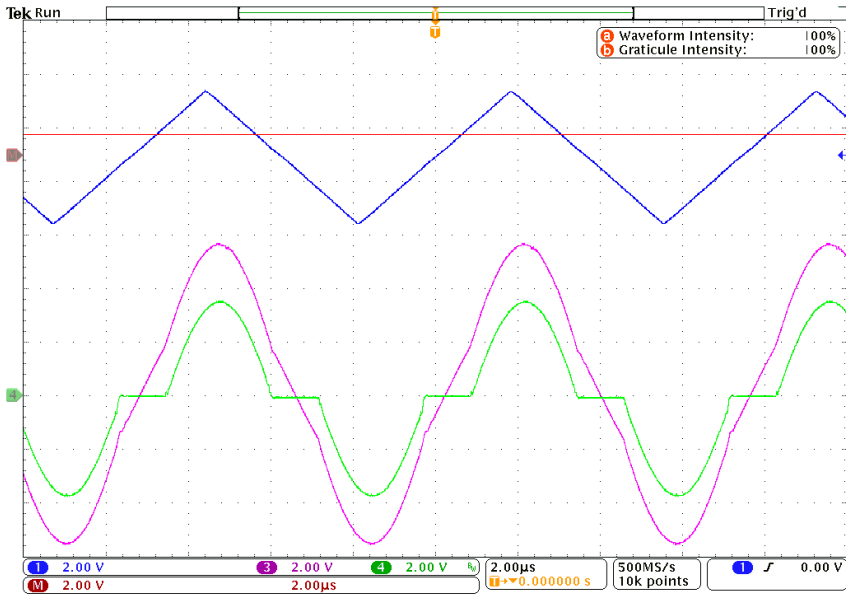

Figure 4-12: 125kHz breadboard in tune at mid-frequency 134.85kHz. Blue: V_{TR}, Red: V_{TUNE+}, Pink: V_C, Green: V_{SW}

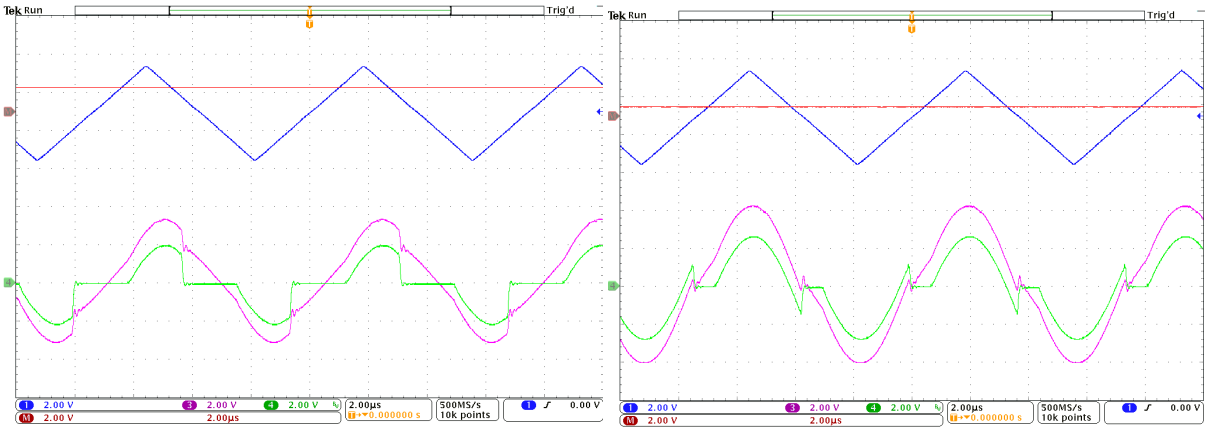

Figure 4-13: 125kHz breadboard detuned at mid-frequency 134.85kHz, left: V_{TUNE} is too high, right: V_{TUNE} is too low. Blue: V_{TR}, Red: V_{TUNE+}, Pink: V_C, Green: V_{SW}

4.3 Summary of breadboard construction

The construction of the 10kHz and 125kHz breadboards was an informative exercise, providing insight into the practical issues which can affect operation of the tuning system. A summary of system-level issues with each primary function is given in table 4-1, identified by the breadboard construction exercises. Each must be considered for integration into a monolithic IC. This is covered in the next chapter.

Function	Issue
Timing Generator	Need symmetry in V_{TR} rising/falling edges at all frequencies.
Capacitor Switching	Switch must withstand peak/trough V_C voltages and inductor currents. Switch must be low resistance to maintain high Q. Switch must be fast to prevent timing skew.
Tank Driver	Direct drive must be low impedance to maintain high Q. High side/low side driving must be symmetrical in delay to avoid timing skew.
Resonance Detection	Detection of V_{SW} must happen right before HV switch closure. Tuning setting must be keep without bounds of V_{TR}. Some V_{SW} excursion is necessary to determine resonant condition.

Table 4-1: Summary of system-level functional issues for zero-voltage switched fractional capacitance tuning

5 Integrated self-tuning implementation with CMOS HV process: 75kHz – 2MHz "lctune018"

This chapter details how the implementation issues raised from breadboard construction are translated into design requirements for full integration on silicon. An IC process technology is selected from basic specifications, followed by discussion of the architectural considerations for integration. The development of each system block is covered to achieve the desired functionality with the IC process technology available.

5.1 Functional requirements and system-level challenges

5.1.1 Top-level specification for process selection

In order to help select an appropriate commercial process for IC development, some basic system specifications had to be set. These were the operating frequency range, tuning accuracy, maximum antenna current and maximum capacitor switch voltage.

Commercial applications of WPC exist at a wide range of frequencies in addition to 125kHz. Low power WPC such as for RFID is often conducted on Industrial, Scientific and Medical (ISM) bands at 6.78MHz and above where no licencing is required for transmissions below a specified power limit [35]. By contrast, high power transfer systems for machine applications typically utilise frequencies up to 300kHz in order to convey significant amounts of energy over short distances without having the problem of free-space attenuation [7]. A maximum operating frequency in the region of 1-2MHz was chosen as a compromise maximum to avoid excessive circuit design time for speed optimisation. A target of less than 1^{O} phase offset between the antenna drive was set, i.e. approximately 1.38ns offset at 2MHz, so logic propagation delays for timing generation should ideally be sub-1ns.

The maximum capacitor voltage was in part set by the need to induce a sufficiently large voltage in an inductively-coupled test load. With an example coupling factor k = 0.1 between transmitter and receiver and target induced EMF of 1V in a purely inductive receiver (i.e. a non-resonant load, hence no Q multiplication of the voltage on a capacitor), an inductor voltage of 10V is required. Hence the integrated capacitor switch FETs had to withstand 10s of volts when open, hence the process had to provide suitable devices for this.

In addition, the breadboard exercise had demonstrated that it was straightforward to create inductors with Q = 50-100. With a 1V pk-pk drive, the HV switches may be exposed to peak voltages of 25-50V. Whilst a high voltage process may permit higher voltages for greater test flexibility, this would have presented additional safety considerations. Hence a limit of around 50V was considered a reasonable compromise between functionality and safety.

The antenna current target was also set by the effect of the Q factor in the intended frequency range. With an inductor in the range of 100µH at 2MHz, a resonant circuit with Q = 100 would draw approximately 80mA at resonance with a 1V drive, hence a target inductor current of 100mA was set. Hence the chosen process would need to provide both active devices and metal layers to support the resulting current density under nominal conditions.

Design parameter	Required max values (approximate)
Operating frequency	1-2MHz
Logic timing delay	Sub-1ns
Antenna current	100mA
Antenna voltage	25-50V

Table 5-1: Summary of top-level specifications for process choice

A process was sought which met these broad performance requirements. From the available range of affordable processes, an Austria Microsystems 0.18um geometry CMOS process (AMS018), which included 1.8, 5, 20 and 50V devices [36]. Logic cells were also provided with the process design kit, featuring logic gates with typically less than 0.1ns propagation delay when connected to other logic cells [37]. These features permit both high-speed timing generation for accuracy and high-voltage operation of the antenna for realistic test cases. Using this process, the idealised system architecture could be implemented, with circuit modifications as detailed in the subsequent sections.

5.1.2 Antenna capacitor switching

The switched fractional capacitor tuning method tested so far required an ideal bi-directional HV switch, operating with positive and negative excursions with respect to the 0V reference. This is problematic as the NMOS and PMOS devices used to form a transmission gate require careful control of the V_{GS} potentials to ensure the switch operates correctly. There is also the risk of forward conduction from the substrate if the body potential of the FETs is not carefully controlled, hence tracking of V_{SW} may be necessary, as per figure 5-1. With a combination of fast switching and high voltages, designing body voltage drivers becomes challenging.

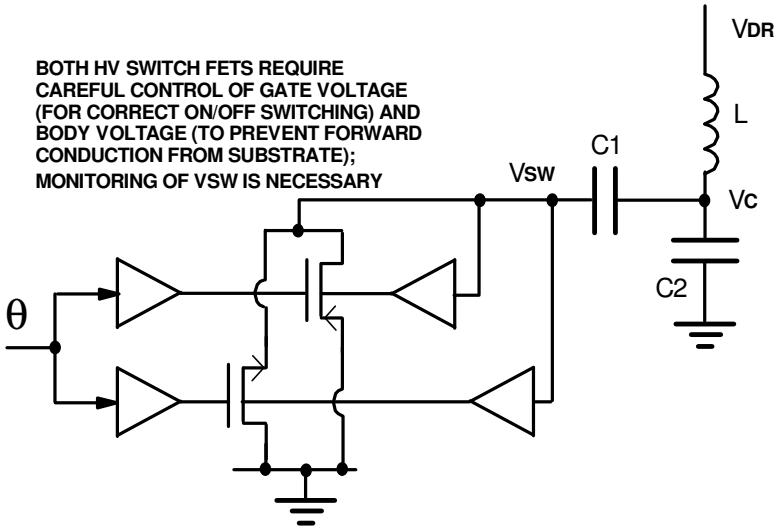

Figure 5-1: Transmission gate capacitor switch architecture requiring levelshifted gate and body drivers

Alternatively, the fixed and fractional capacitors may be re-arranged as separately switched capacitors. The positive and negative excursions of V_C are handled by independent NMOS and PMOS FETs respectively as per figure 5-2. The NMOS is controlled with respect to 0V, meaning only one HV supply and levelshift is now required for the PMOS, the positive supply voltage V_{DDHV} set by the peak voltage expected on V_C. It also permits the maximum V_C peak-peak to be the sum of the V_{DS} ratings of the two transistors, i.e. approximately doubling the allowable amplitude for the same HV FETs, since at any given time one switch is closed for at least half the cycle. Note that to maintain symmetrical switching durations on both excursions of V_C in this topology, both C_N and C_P must be the same value, constraining the max:min capacitance ratio to 2:1. The resulting tuning range available is 1.41:1. However earlier calculation showed that even ±20% variation in the LC values requires only a 1.2:1 tuning range, hence the unipolar switching method is appropriate for practical applications.

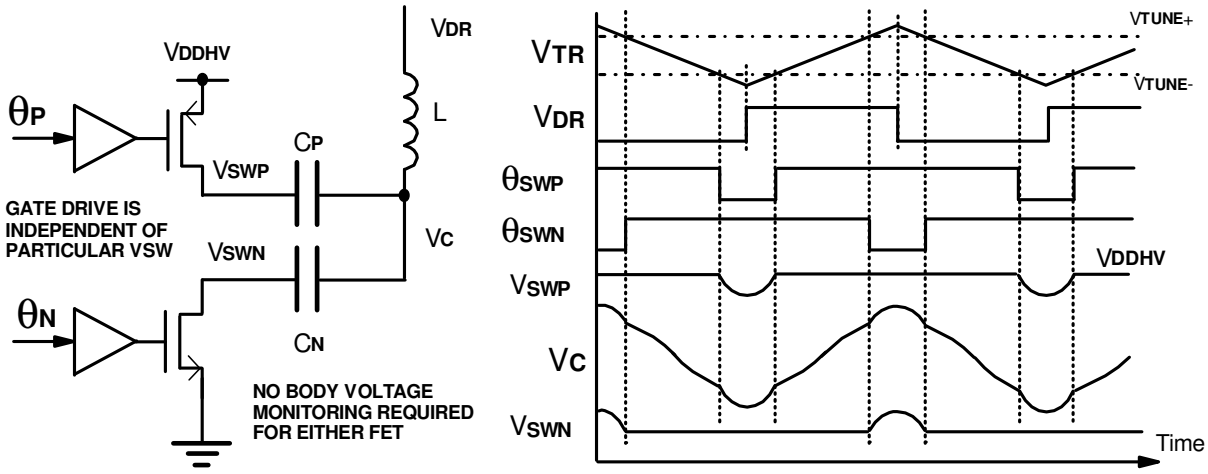

Figure 5-2: Unipolar capacitor switch architecture with no body drivers and simplified gate drivers

5.1.3 Resonance detection

Resonance of switched fractional capacitance tuning is determined by observing the voltage on the HV capacitor switches just before closure, and determining if it is above or below the corresponding supply potential, using a comparator. Given the possibility of 10s of volts on the switches when open, the resonance detection circuit had to safely operate under this condition.

The comparator for resonance detection could have been designed with HV FETs so that the input differential pair of the comparator operated on the same HV supplies as the tuning switches. However, the large LDMOS devices in the process occupy larger area and require greater current to operate quickly when compared with the available 1.8V and 5V devices in the process. Hence it was desirable to use lower voltage devices.

To reduce the HV voltage to a safe level without corrupting the sign information, a potential divider was used as per figure 5-3. The HV excursion on the switch is reduced to within the safe operating limits of a 1.8V/5V comparator. The particular magnitude of the excursion is not important, since only the sign of the voltage just before closure is required to obtain tuning information.

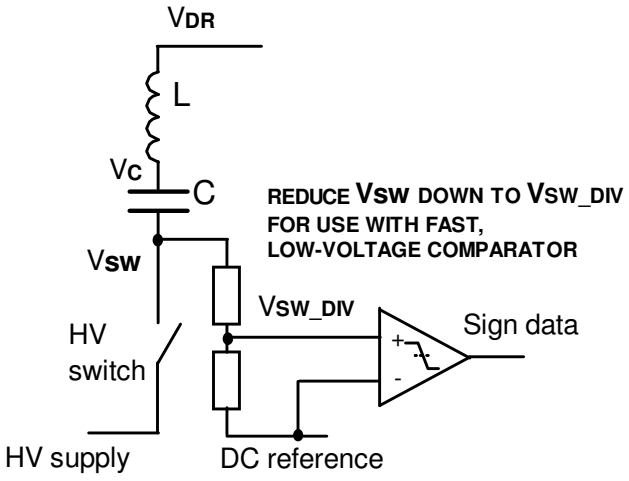

Figure 5-3: Voltage division of HV switch excursion using voltage division

Note that the complete IC required ESD protection devices, which clamp excursions outside the HV supplies to within approximately 0.5V of the supplies. Hence the comparator offset needed to be less than 0.5V to reliably detect the tuning state, which was considered to be easily attainable by using a symmetrical architecture and good layout matching. The design of the comparator is covered later in section 6.4.3.

5.1.4 Tuning error integrator

An analogue integrator as per the constructed breadboard was considered for self-tuning of the antenna. However, the time constant required was much larger as integration needed to occur over many cycles to ensure stability. At the lowest frequency of operation, integrating over 100 cycles at 75kHz would require an integration time constant of approximately 1.33ms. To integrate over a 1.5V range during this time would have required either a very small current or large integration capacitance. For example, a 100pF integration capacitor would need an integration current of 150nA, both of which would be difficult to create within an IC in the chosen process.

On the other hand, a digital solution for a self-tuning integrator was preferable for several reasons. Firstly, the maximum required clock frequency would be twice the maximum frequency of operation, in this case 4MHz. With sub-1ns propagation delays in the provided logic, this was easily attainable in the chosen AMS018 process.

Secondly, the gain of a digital counter can be easily adjusted for a response time which is faster (i.e. increment/decrement of more than 1 code) or slower (i.e. increment/decrement by 1 code less frequently).

Thirdly, a digital counter was very easy to control using a digital interface. Not only can the integration gain be easily adjusted, the counter may also be easily locked at a particular value to maintain a fixed tuning condition. It may also be read out from the IC very easily to assist with external control circuitry and measurement. Hence a digital solution was used for self-tuning.

5.1.5 Timing generator

The use of a triangle waveform for timing generation had been successful on breadboard and was considered for the IC system. The triangle size, integration current and capacitance determine what frequencies may be achieved. It is desirable to have a large peak-peak triangle voltage to relax the offset requirements of the comparators. A 3V pk-pk triangle, i.e. between 1V and 4V, within a 5V supply was set as a compromise between the comparator offset requirement and allowing sufficient headroom to allow for V_{DS} across the transistors of the comparator and up/down current source.

Using a 3V pk-pk triangle, 2MHz was attainable with a 50µA current source and 4.17pF capacitor according to equation 3.20. This current and capacitance were easily attainable within the AMS018 process, meaning analogue triangle generation was feasible.

With an analogue triangle generator, the phase resolution is limited by the comparator offset. With a 3V pk-pk triangle, the $V_{TUNE+/-}$ ranges would be 1.5V each. To create no more than 1^{O} of phase offset, the voltage offset of the comparator must be at no more than 8.33mV, which was deemed to be a realistic target within the scope of the AMS018 process using conventional matching techniques. Figure 5-4 shows how the phase resolution may be determined from the comparator offset, giving rise to equation 5.1, where the maximum permissible comparator offset V_{offset} can be determined by the maximum phase offset $\emptyset_{max}$.

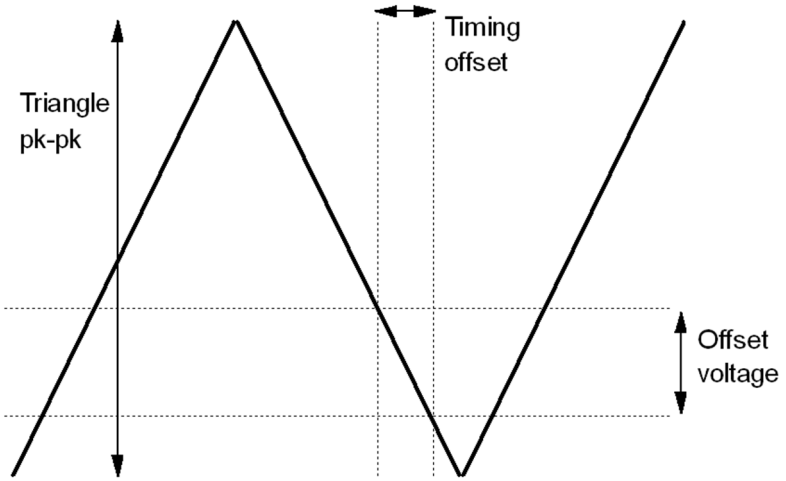

Figure 5-4: Effect of comparator voltage offset

$$V_{offset} = \frac{dV \times \emptyset_{max}}{\pi} \quad (5.1)$$

Alternatively, the triangle could be implemented by means of a digital up/down counter, the triangle's amplitude being the size of the counter. Slicing may be done instead by comparing the present value with a fixed value, and setting a flag if they match. The limiting factors for phase resolution of a digital triangle generator would therefore be the counter size and clock frequency. A large counter would allow high tuning resolution, since the timing position of the slicing signals may be finely adjusted, however it may need a very high clock frequency in order to achieve it. Figure 5-5 shows how a digital triangle may be implemented.

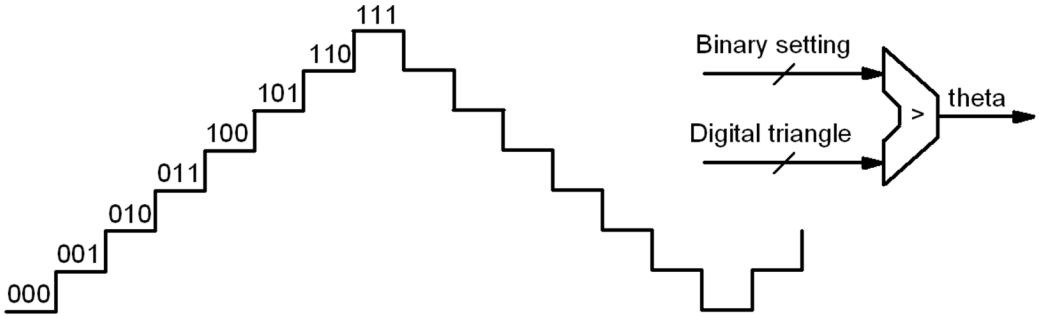

Figure 5-5: Digital triangle slicing concept

An 8-bit counter would provide 256 steps from peak to trough of the triangle, which would equate to 0.703 degrees of tuning resolution. At 2MHz this would require 512 clocks per cycle, meaning a clock of over 1GHz would be required. This was considered to be beyond the capability of the available logic devices in the process. By comparison, a 4-bit counter would only need a 64MHz clock, but would only allow 11.25 degree steps of tuning resolution, which is too coarse to achieve optimal tuning. It was clear that the analogue triangle generator was preferable with the available IC process.

5.1.6 Tuning voltage generation

Since the tuning error was to be digitally-integrated but the timing generation done with an analogue triangle, on-chip voltage DACs were required for setting the HV switch duty cycles. The DAC resolution requirement was set by the tuning accuracy requirement, i.e. to tune to within the 3dB bandwidth at any frequency for a Q factor of up to 100.

Using the triangle-based method of HV switch timing, the relationship between V_{TUNE} and the phase angle of switching Θ is linear. However, it was shown that the relation between Θ and the modified resonant frequency ω_{RES} is non-linear. Hence a linearly quantized range for V_{TUNE} would have non-linear behaviour in the tuning resolution, as per figure 5-6, hence the tuning resolution is lower at the lower end of the tuning range.

The use of a non-linear DAC was considered, i.e. the resulting output voltage coded to produce an even space between them in ω_{RES}, hence linearising the relation between V_{TUNE} and ω_{RES}. However, a linear DAC was much more straightforward to implement, i.e. the voltage higher bits are a 2^N multiple of the least significant bit (LSB). It was necessary to ensure that the linear DAC had sufficient resolution to meet the frequency resolution requirement at all points in the tuning range.

From visual inspection of figure 5-6 it can be seen that a linear V_{TUNE} resolution produces the lowest ω_{RES} resolution at the top end of the tuning range, i.e. near ω_{MAX}. Equation 5.2 gives the value of $\omega_{RES[1]}$, the modified resonant frequency at the first DAC code, i.e. Θ is one step above zero. N represents the DAC resolution in bits. Note that this takes account of the max:min ratio of ω_{MAX}:ω_{MIN} being root(2):1, enforced by the choice of unipolar capacitor switching for antenna tuning.

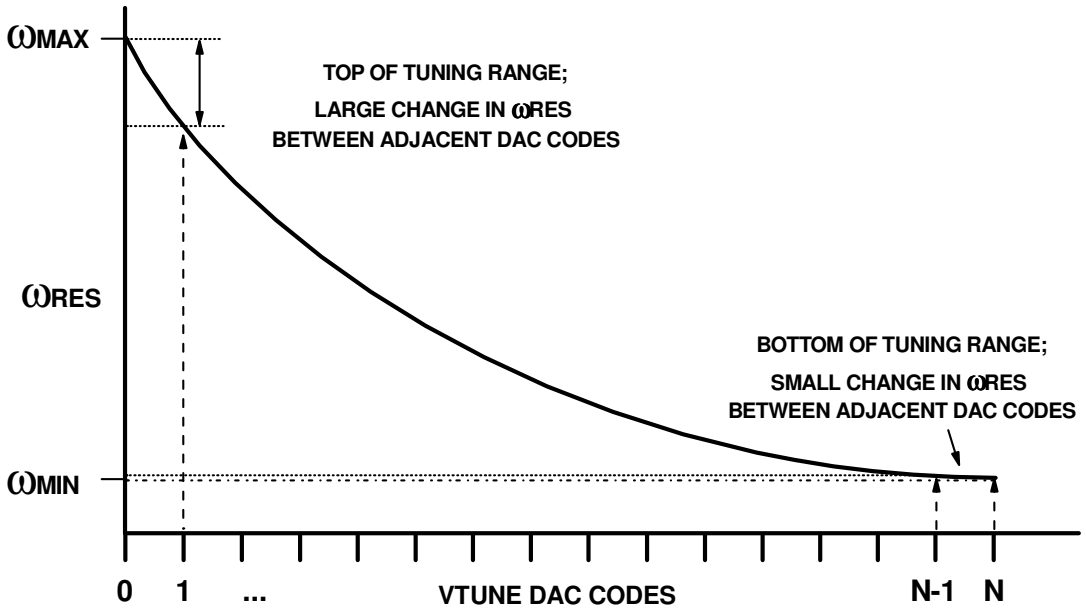

Figure 5-6: Modified resonant frequency resolution across the tuning range

The largest change in ω_{RES} is equal to the difference between ω_{MAX} and $\omega_{RES[1]}$, which must be smaller than the 3dB bandwidth at ω_{MAX} to guarantee the ability to tune to within this at any point in the tuning range (the equality is expressed in equations 5.3 and 5.4). It was found $N \geq 8$ to satisfy the equality when Q = 100, i.e. the DACs for V_{TUNE} required at least 8 bits, which was the chosen resolution.

$$\omega_{res[1]} = \frac{\pi}{2\left(\frac{\pi}{2^N} + \frac{1}{\sqrt{2}} tan^{-1}\left[\sqrt{2}\ cot\left(\frac{\pi}{2^N}\right)\right]\right)} \tag{5.2}$$

$$\omega_{res[0]} - \omega_{res[1]} = \omega_{max} - \omega_{res[1]} < \frac{\omega_{max}}{Q} \tag{5.3}$$

$$\sqrt{2} - \frac{\pi}{2\left(\frac{\pi}{2^N} + \frac{1}{\sqrt{2}} tan^{-1}\left[\sqrt{2}\ cot\left(\frac{\pi}{2^N}\right)\right]\right)} < \frac{\sqrt{2}}{Q} \tag{5.4}$$

5.1.7 Timing error compensation

Breadboard construction for 125kHz operation revealed that cumulative timing delays can cause a phase offset from the ideal phase positioning of the HV tuning switch operation with respect to the antenna drive. Given the designed system needed to operate at up to 2MHz, it was necessary to explore methods of correcting this phase offset. The trimming method needed to be precise enough to allow trimming to within the 1^{O} requirement at up to 2MHz, hence the trimming resolution needed to be smaller than approximately 1.38ns to permit accurate compensation as per figure 5-7.

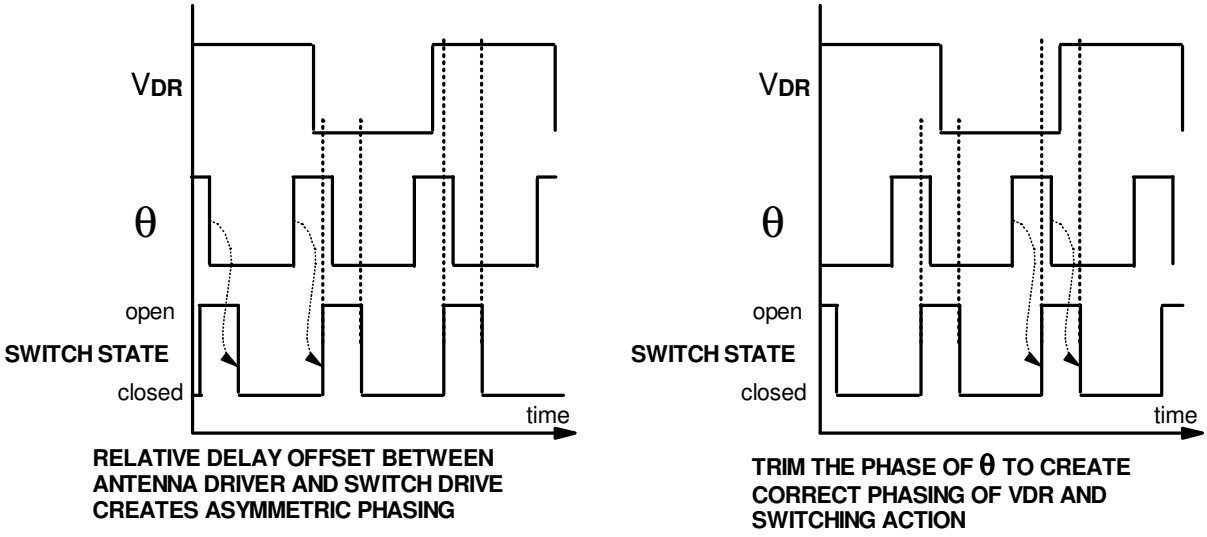

Figure 5-7: Phase trimming concept for correction of systematic time delay offset between antenna driver and HV switch driver

Figure 5-8 shows one possible solution, whereby unit delay elements are added or removed from the timing paths of the antenna drive and switch controls, so that correct phase alignment is achieved. This approach was feasible in the process to meet the trimming accuracy requirement; the typical propagation delay of the logic cells was around 100ps. However, the delay would change considerably with Process, Voltage and Temperature (PVT) variation and so would not be ideal for correcting systematic timing errors.

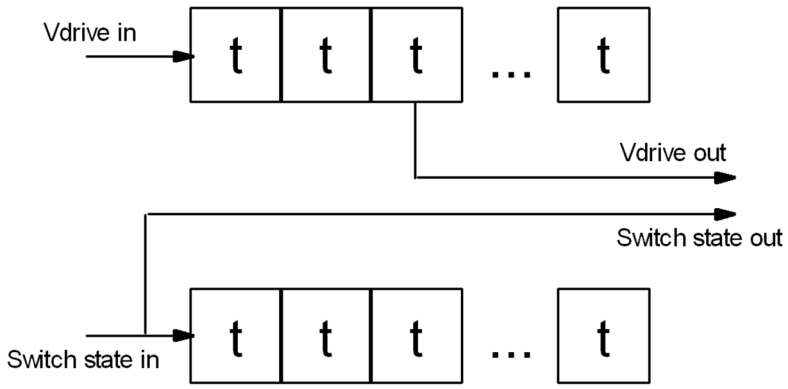

Figure 5-8: Phase trimming via tapped delay line

An alternative solution is to adjust the position of the $V_{TUNE+/-}$ voltages on the rising and falling edges of V_{TR}, such that the HV switch control signal Θ is adjusted in phase with respect to the drive V_{DR}. Figure 5-9 shows the concept. On the rising edge of V_{TR}, the $V_{TUNE\_RISE+/-}$ are used, but on the falling edge $V_{TUNE\_FALL+/-}$ are used. In this example, Θ is brought forward in phase to compensate for larger

delays in the HV switching action. In the case of a slower driver, the rising and falling voltages for $V_{TUNE+/-}$ may be swapped in polarity, creating a phase lag in Θ.

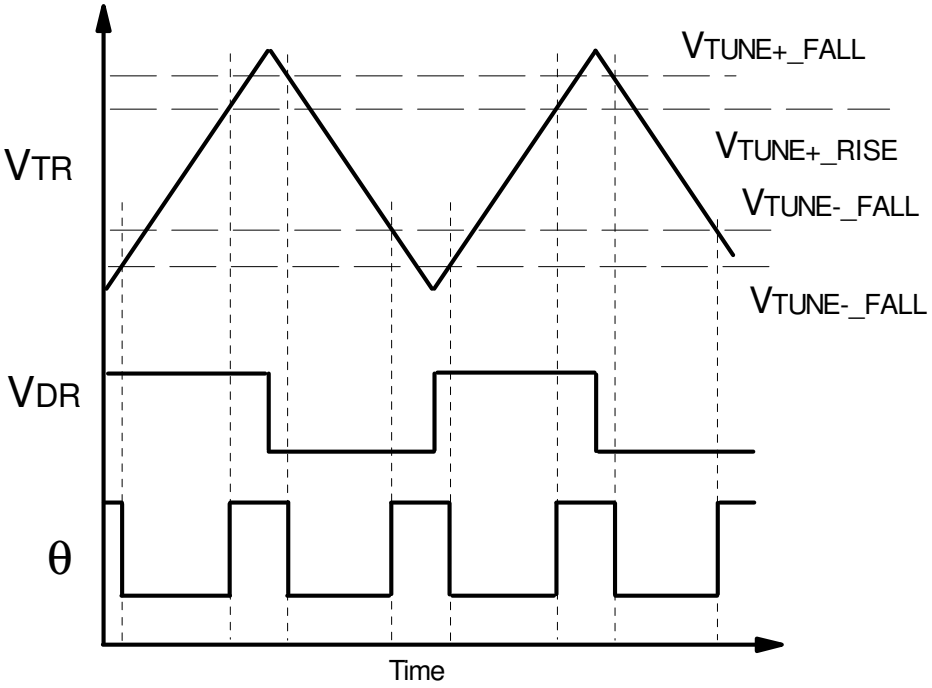

Figure 5-9: Phase trimming via adjustment of slice levels

This method of phase trimming is more consistent over PVT variation, since the offset voltage between the $V_{TUNE+/-}$ rising and falling voltages is fixed, hence the timing offset is a fixed proportion of the operating frequency. The trimming resolution is set by the resolution of the $V_{TUNE+/-}$ voltages. Each of the four tuning voltages controls switching for one quadrant of oscillation, so to achieve better than 1^{O} resolution with digitally-set voltages, a resolution more than 90 levels is required, i.e. at least 7-bits for a voltage DAC creating the $V_{TUNE+/-}$ levels. Since it had already been established that 8-bit DACs were needed for the tuning resolution, this method was suitable for phase trimming.

5.2 Top-level architecture

Using the design specifications and requirements, the IC architecture in figure 5-10 was developed. The system includes timing generation for both an on-chip antenna driver and unipolar HV tuning capacitor switches, a tuning error detection system and synchronous digital integrator to automatically tune the LC antenna to resonance. A digital control block is included to allow control parameters to be adjusted, such as the operating frequency and self-tuning error integrator gain.

The core circuitry operates on 1.8V and 5V supplies. Independent supplies for the analogue and digital domains are provided to reduce the effect of switching noise from the digital blocks creating glitches on the analogue timing reference. The HV PMOS capacitor switch is referred to a HV supply. Each supply voltage is provided off-chip, as is the master reference bias current for the analogue blocks. In a commercial product, additional blocks would be included on chip using band-gap references and internal regulators to create these references. However, including these additional blocks did not contribute to the primary research objectives and so they were not implemented to save system development time.

An “Analogue Test Bus” (ATB) was also included in the architecture to permit certain signals inside the IC to be observed for debug purposes. Each internal test point is connected to a high-impedance bus so that signals may be observed with an oscilloscope without detrimentally loading the node under test

or causing unwanted leakage to other nodes on the ATB. If need be, the observable signals may also be overdriven using an external supply.

The current integrator oscillator uses a V-to-I concept, using a voltage DAC to set a DC current for oscillation. The current can also be sourced off-chip to permit analogue frequency sweeps and manual trimming. Functionality was included to allow an abrupt step in the DC current, and hence the operating frequency, to demonstrate the behaviour of the self-tuning loop. The integration capacitance is a selectable array of capacitors, permitting a wide operating frequency range in the 75kHz-2MHz region. The V_{TR} wave is compared by continuous comparators to create the HV switch control signals. The comparator V_{TUNE} reference voltages may be set digitally on chip or connected to external pins for manual adjustment of the resonant setting.

To assist with correct phasing, a timing block is included to enforce the sampling of the HV switch excursions just before closure, creating the Θ_{SMP} (sample the HV switch sign) and Θ_{RST} (reset the error detection circuit) for the tuning error detector block. These occur just before the Θ_{SW} signals, which control the HV switch states.

The tuning error detector samples the HV excursions using a resettable capacitive division technique to reduce the 20V peak voltage to a safe operating range for lower voltage internal circuitry. The resulting digital error signals are fed to the error integrator to create a digital self-tune setting. The V_{TUNE} DACs can be connected directly to the error integrator output, instead to a manually-set digital setting.

Further detail on circuit design and simulations for individual blocks are considered in the relevant sub-sections. Top-level system simulation is provided at the end of the chapter.

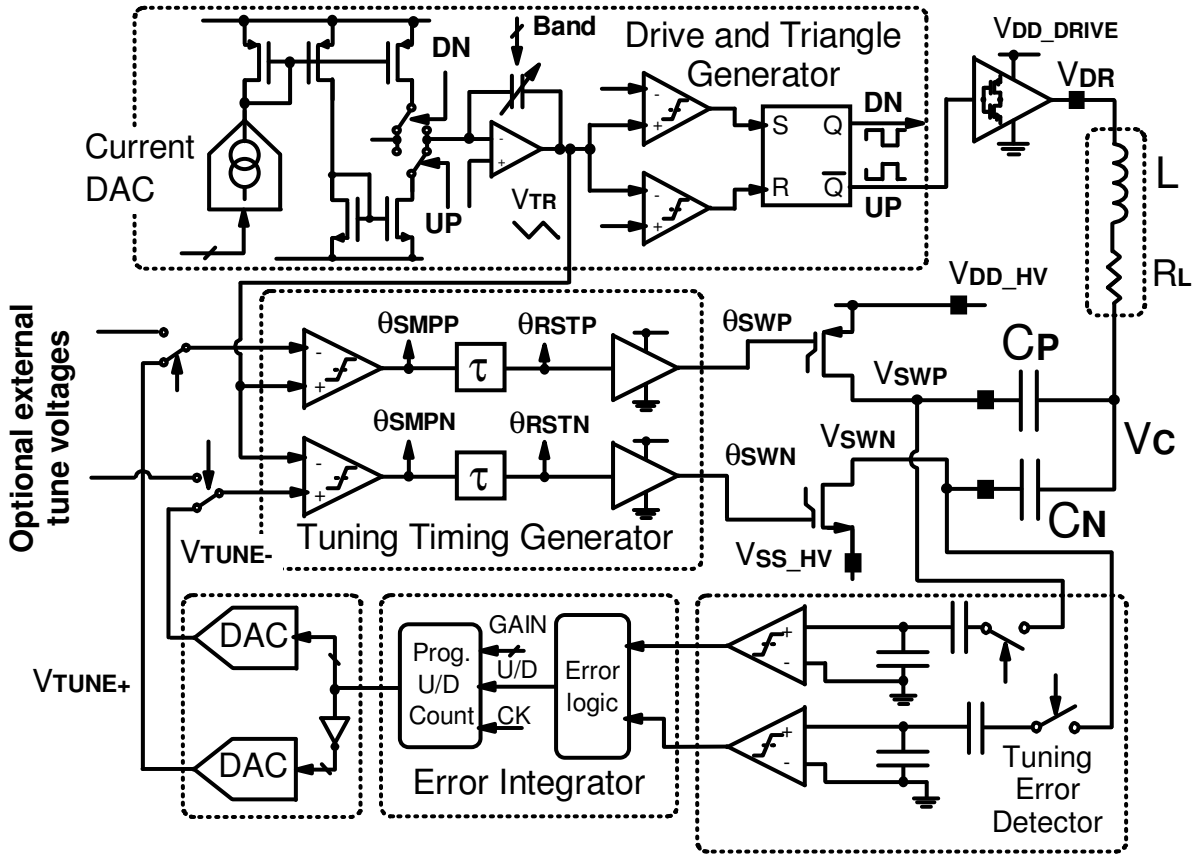

Figure 5-10: System-level IC conceptual architecture

5.3 Sub-block architectures

5.3.1 Triangle generator

It was decided to implement the triangle using analogue means, re-using the current integrator oscillator method for simplicity. Figure 5-11 shows the architecture used within the triangle generator.

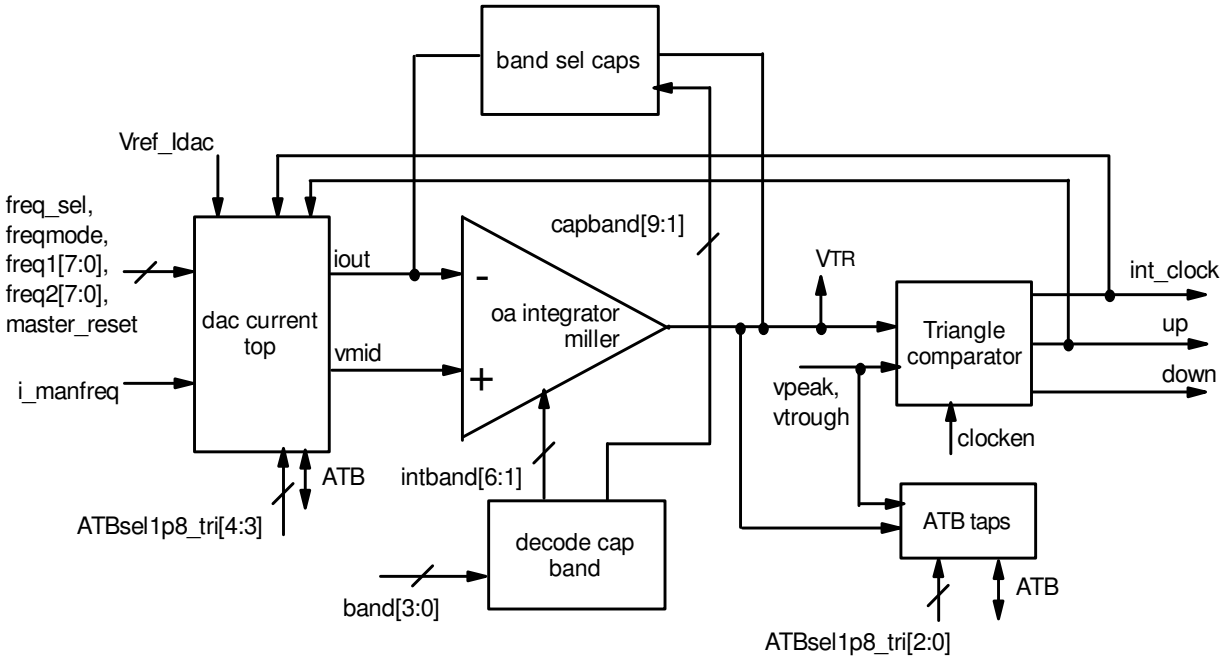

Figure 5-11: Triangle generator block diagram

As well as generating the triangle, the triangle generator had several other key functions. The signals indicating the direction of the triangle, *up* and *down* were made available to other system blocks. The clock for the digital integrator block *int_clock* was also created inside the triangle generator, as it was convenient to derive it from the local up and down signals.

Additionally, it was required that the triangle generator could switch between the two pre-programmed frequencies, depending upon the value of the *freq_sel* input.

5.3.1.1 Engineering parameter choices

As mentioned earlier, a 3V triangle pk-pk amplitude was chosen to permit easier design of comparators by allowing a greater tolerance of input-referred offset. With a fixed triangle amplitude, the current and capacitance needed to be chosen to permit operation at all frequencies from 75kHz to 2MHz. The engineering choices to be made are summarised in the block diagram in figure 5-12.

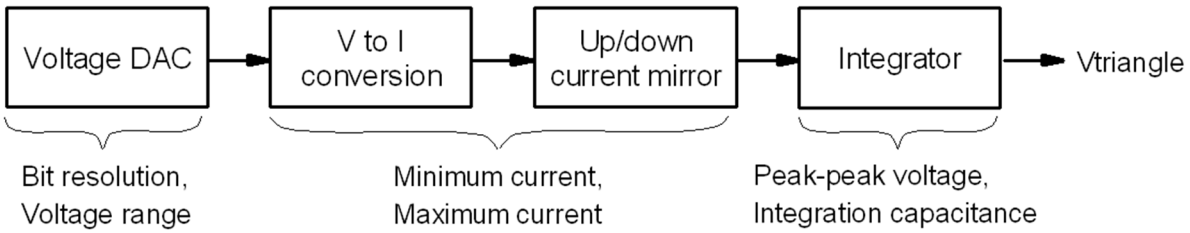

Figure 5-12: Triangle generator engineering parameters

Due to the wide frequency range of operation, it would have been impractical to have only the current being varied in order to change the frequency. For example, using an integration capacitance of 10pF would require a current of 4.6µA at 75kHz and 120µA at 2MHz. Making a current source with two

orders of magnitude range is difficult, as it requires that the current mirror circuitry remains in the saturation region for all desired current values. Since MOS saturation is dependent upon the drain-source current I_{ds}, a wide range of I_{ds} complicates the design.

To allow for a simpler current mirror design, it was decided to create bands of operation using a bank of tuning capacitors. The value of each capacitor within the bank should be set by the desired tuning range. Table 5-2 shows the bands of frequencies chosen. ΔC is the change in capacitance from the previous frequency band, indicating the additive capacitance required upon the total previous to achieve the correct value of $C_{integration}$.

F_{MAX}	F_{MIN}	$C_{integration}$	ΔC	Minimum bandwidth (Q = 50)	Resolution
2.00MHz	1.00MHz	4.17pF	4.17pF	20.0kHz	4.00kHz
1.50MHz	750kHz	5.56pF	1.39pF	15.0kHz	3.00kHz
1.13MHz	563kHz	7.41pF	1.85pF	11.3kHz	2.25kHz
844kHz	422kHz	9.88pF	2.47pF	8.44kHz	1.69kHz
633kHz	316kHz	13.2pF	3.29pF	6.33kHz	1.27kHz
475kHz	237kHz	17.6pF	4.39pF	4.75kHz	949Hz
356kHz	178kHz	23.4pF	5.85pF	3.56kHz	712Hz
267kHz	133kHz	31.2pF	7.80pF	2.67kHz	534Hz
200kHz	100kHz	41.6pF	10.4pF	2.00kHz	400Hz
150kHz	75.1kHz	55.5pF	13.9pF	1.50kHz	300Hz

Table 5-2: Triangle generator frequency bands

The width of each band was set to be 50% of the maximum frequency, meaning only a 2:1 ratio of current would be required, permitting simple current mirror design. Each band was also set to have a large overlap, such that wideband frequency tuning could be achieved without the need to adjust the integration capacitance during normal operation. Overlap was set such that the maximum frequency of a band would be equal to 1.5 times the minimum frequency of the band below.

The integration capacitance for each band was chosen by the use of 50μA of integration current at maximum band frequency, resulting in 25μA at minimum band frequency. These values would be small enough to prevent the need for excessively large transistors, whilst being large enough to ensure that induced noise from neighbouring circuitry would be negligible, providing a clean square wave of current.

The capacitor values were also chosen such that they would be large enough to not be significantly affected by random offset, but were still small enough to comfortably fit within the IC. In order to reduce area consumption, the capacitors were cumulatively configured, such that moving to from one frequency to another would add or remove a capacitor from the integrator feedback loop. Compared to using binary weighted capacitors, a cumulative approach permitted for simpler decoding in order to select the desired capacitors for the required band of operation.

The tuning resolution was determined by the resolution of the voltage DAC. It was therefore necessary to determine how many bits were required. This was dependent upon the bandwidth of the LC tank, as in order to be able to achieve resonance it is necessary to be able to tune within the 3dB bandwidth. The frequency resolution of the triangle generator frequency must therefore be better than the tank bandwidth. The values calculated in table 5-2 was based upon a Q factor of 50.

There is a direct linear relationship between integration current and frequency, so the resolution of the current DAC may be worked out from the frequency resolution required within the given bandwidth. Equation 5.5 shows how the number of DAC codes n may be determined from the integration band frequencies.

$$n = \frac{f_{max} - f_{min}}{f_{res}} = \frac{(I_{max} - I_{min})}{2\ C\ dv\ f_{res}} = \frac{I_{min}}{2\ C\ dv\ f_{res}} \tag{5.5}$$

The number of bits N required for the DAC may be therefore calculated as per equation 5.6.

$$N = log_2(n) = log_2\left(\frac{I_{min}}{2\ C\ dv\ f_{res}}\right) \tag{5.6}$$

Setting the frequency resolution as one fifth of the LC tank 3dB bandwidth yields N = 7.97 ≈ 8 bits. This was decided upon as the frequency resolution for several reasons. Firstly, it would ensure that the selected frequency would always fall within the LC tank 3dB bandwidth up to Q = 50. Secondly, using an 8-bit resolution meant that the voltage DAC blocks used for the slice voltage generation could be reused, saving development time. Thirdly, the use of an 8-bit DAC architecture would permit the use of an 8-bit controller architecture, which would make interfacing with the IC simpler.

5.3.1.2 Root 2 tune range

Since it was required to be able to change frequency quickly, the system was designed to have two pre-programmed frequencies, selectable via a dedicated input pin *freq_sel*. This removed the need to rewrite the frequency register every time a frequency change was necessary.

Since unipolar switches were chosen to implement the switched capacitors, it was required that both tuning capacitors have the same value for a symmetrical oscillation. Hence, the system is limited to a maximum tuning range of approximately 1.41:1. It was important therefore that the frequency range selectable by *freq_sel* would therefore fall within this range.

The current summation architecture used in figure 5-13 shows two architectures which were considered, given the requirement for a 2:1 input current range. The left-hand design would switch between one of two integration currents, whilst that on the right-hand side would add a small modification current to a fixed current.

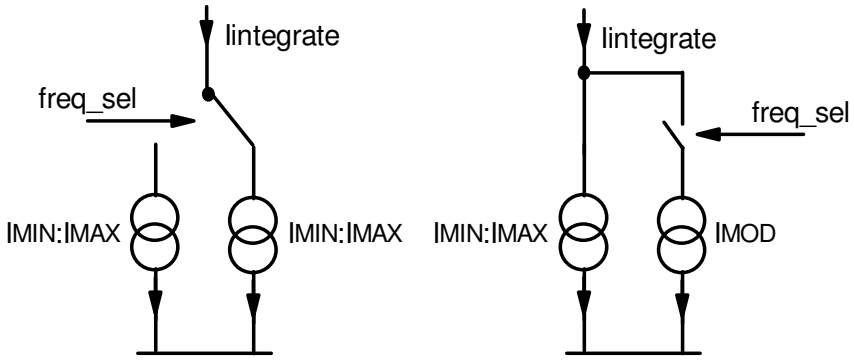

Figure 5-13: Rapid current adjustment topology choices

The left-hand topology would permit very small changes in frequency, i.e. the two integration currents may be made very similar. It also guarantees that a tune range of up to a factor 2 was possible, meeting the requirement for a root 2 range. However, during transition there would be a brief time period when neither current source is connected to the up/down current mirror. This was considered to be a risk, since even briefly removing the drain-source current of the up/down current mirror would potentially mean that it goes out of saturation and creates a distortion in the current, which in turn creates a misshapen triangle wave whenever the frequency is changed.

The right-hand topology has a constant current into the up/down current mirror, and so it does not risk the current mirror FETs leaving the saturation region. The minimum step in frequency would however be larger, depending on the chosen range of I_{mod}.

Choosing the range of I_{mod} to be 10µA - 20µA, the minimum tune range at minimum is given by the ratio in equation 5.7.

$$\frac{I_{min} + I_{mod\_min}}{I_{min}} = \frac{35\mu A}{25\mu A} = 1.4 \quad (5.7)$$

the maximum tune range at minimum frequency is given by

$$\frac{I_{min} + I_{mod\_min}}{I_{min}} = \frac{45\mu A}{25\mu A} = 1.8 \quad (5.8)$$

hence root 2 tuning is possible relative to the minimum frequency of each band. At maximum frequency, the minimum tune range is therefore given by

$$\frac{I_{max} + I_{mod\_min}}{I_{max}} = \frac{60\mu A}{50\mu A} = 1.2 \quad (5.9)$$

and the maximum tune range by

$$\frac{I_{max} + I_{mod\_min}}{I_{max}} = \frac{70\mu A}{50\mu A} = 1.4 \quad (5.10)$$

Although this is slightly less than root 2, it is nonetheless a significantly wide bandwidth to be able to demonstrate the concept. The current summation topology was therefore chosen to provide the integration current, using I_{mod} within a range of 10µA - 20µA.

5.3.1.3 Current DAC design

The current DAC was required to generate the up/down current for triangle generation. The basic concept of a voltage-to-current generator and up/down current mirror was reused from the 10kHz breadboard, however several changes were required to make the block function correctly within the IC. Figure 5-14 shows the architecture used.

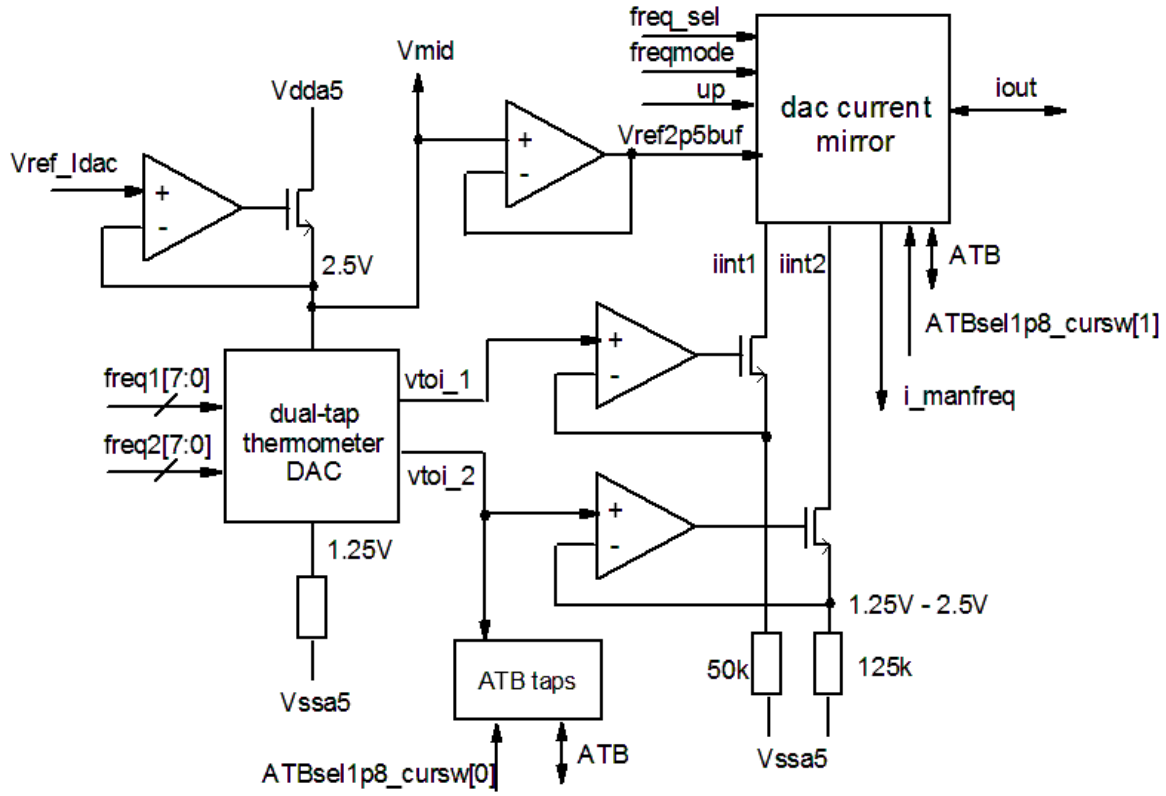

Figure 5-14: Current DAC block diagram

The voltage DAC was used to create voltages from which the integration currents would be derived. This was an architecture reused from the slice voltage DAC in order to reduce development time. The DAC output voltage range was set to be between 2.5V and 1.25V. This range was chosen because it was large enough that small offsets and noise interference would not create significant current offset. A 2.5V reference was also readily available in order to set the mid-point of the triangle, so it was convenient to reuse this as the maximum DAC voltage.

The chosen V-to-I voltage range meant that the 25µA - 50µA current needed a 50kΩ resistance, and the 10µA - 20µA source needed 125kΩ. These were both realistic to achieve using available polysilicon resistors from the provided design library.

5.3.1.3.1 Up-down current mirror design

It was necessary to create a clean triangle wave for V_{TR} to ensure that symmetrical tuning control signals are created from the V_{TUNE} voltages. Hence the current square wave had to be uniform, i.e. the high and low levels had equal and opposite magnitude derived from the fixed DC current reference. The previous architecture used for the 10kHz breadboard was not entirely suitable for this, as if implemented in CMOS it would cause the output transistors to move in and out of the saturation region. This continual transition would prevent a fast transition from positive to negative current, since the transistors' gate capacitances would be continually charging and discharging. Figure 5-15 shows the problem diagrammatically.

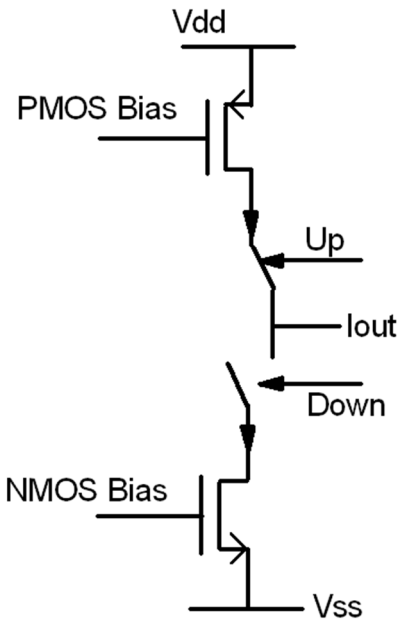

Figure 5-15: Up/down current supply. The disconnected FET has no current flowing through it, hence cannot be in saturation

At 10kHz, the time required to re-charge the capacitors would be negligible, however at 2MHz it would be far more noticeable. An architecture was therefore required which would keep a drain-source current flowing in the unused transistors, preventing them from turning off. The current steering topology in figure 5-16 was used. Since the output of the current mirror would be the common mode of the triangle integrator (i.e. 2.5V approximately), the unused path could simply be connected to an independent 2.5V source so that its operating condition is largely unchanged between the up and down current states.

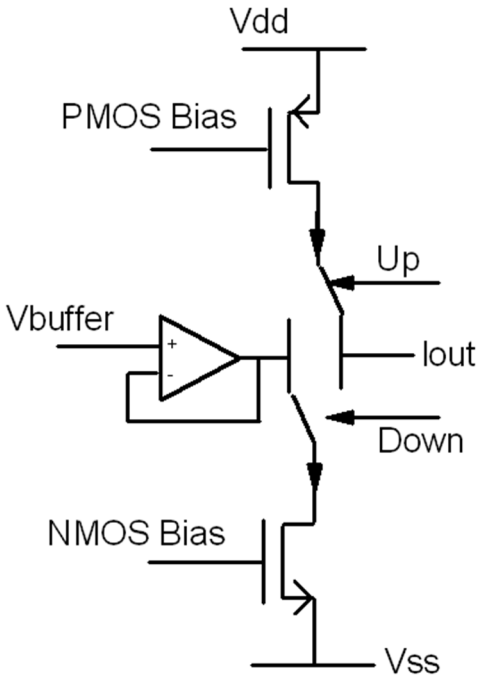

Figure 5-16: Current steering topology for up/down current source

Figure 5-17 shows a circuit diagram of the implemented current steering topology. To increase the output impedance of the current source, cascoding transistors were used. These were designed to be self-biasing, so that additional biasing circuitry would not be needed.

Since the cascoded devices were self-biasing, it was necessary to tie the body connection of the input PMOS devices to the local source, rather than the positive supply rail. This would ensure that the body-source voltage V_{bs} was small, and hence the device threshold voltage was kept close to a minimum, as per the body effect equation 5.11, where V_{t0} is the nominal threshold voltage, γ is the body effect coefficient and $\emptyset$ is the inherent bulk potential [38].

$$V_{th} = V_{t0} + \gamma\left[\sqrt{\emptyset - V_{sb}} - \sqrt{\emptyset}\right] \qquad (5.11)$$

A higher V_{th} would require a higher V_{gs} in order to maintain saturation, hence a higher V_{ds} would result since the gate and drain are tied together. The achievable output voltage range would reduce, potentially to a value below that of the common mode voltage of the triangle. This would prevent the current source from operating correctly, hence using a floating N-well was necessary in the absence of more complex biasing circuitry. Figure 5-17 shows also the DC node voltages of the circuit under static conditions. It can be seen that there is enough room left for the triangle common voltage of 2.5V at the output.

The current-steering FETs connected to the *up* and *down* signals were driven from one input. A driver chain of inverters was used to increase the drive to the gate, ensuring a sharp transition between the on and off state of each switch.

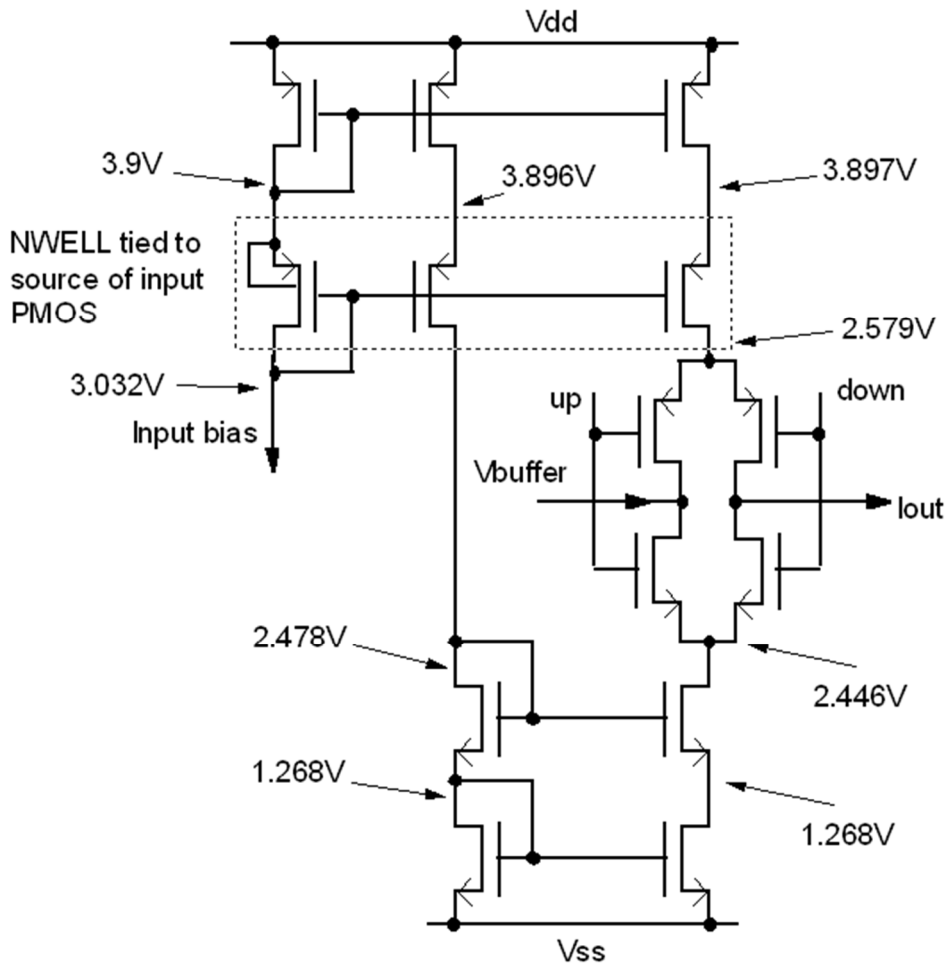

Figure 5-17: Up/down current mirror transistor-level implementation

Figure 5-18 shows the simulated transient response of the extracted up/down current mirror block in operation at 2MHz with 70µA current output. A time-domain numerical integration function is applied to the generated current to show the expected triangle shape. Once the transient from direction change has settled, the up and down current magnitudes are almost identical.

Also shown in figure 5-18 is the transition between one direction and another. The very peak of the triangle is slightly misshapen by the large transient input current, however this will have minimal effect on the tuning because it occurs only at the peak and trough, and is only 0.3% of the peak-peak triangle amplitude, hence it will not adversely affect the switch control action. The propagation delay between the digital direction setting change and the observed current direction change is 1.27ns under nominal conditions, which corresponds to 0.91^{O} of phase shift at 2MHz, which is acceptably small.

The measured percentage offset between the up and down DC currents was 0.016%, hence the up and down slew rates would have this amount of difference between them. This was also perfectly acceptable for triangle generation, meaning no phase compensation was necessary for the triangle waveform.

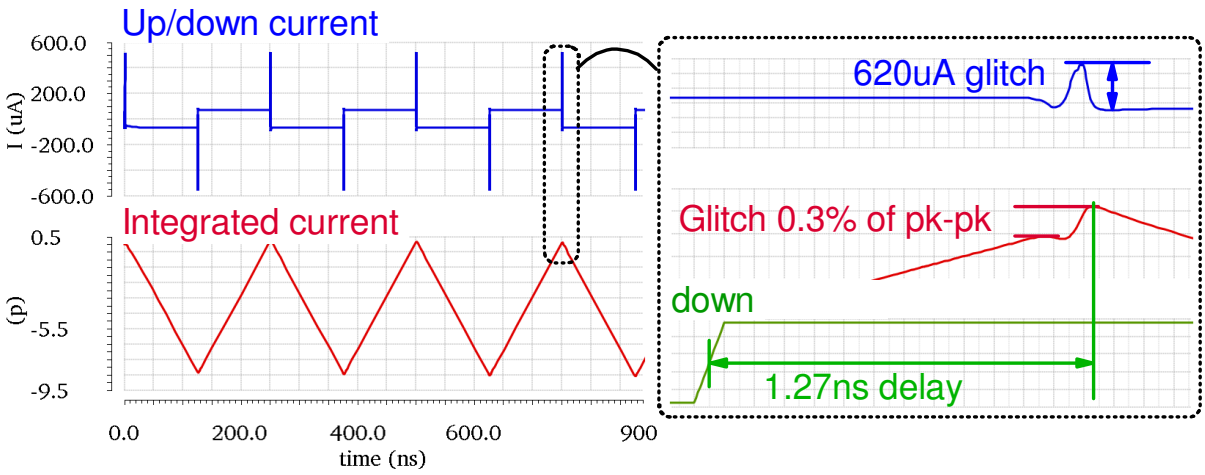

Figure 5-18: Up/down current mirror 70µA output at 2MHz

An additional function included in the up/down current block was a small flip-flop shift register. This was to latch the value of the externally-set *freq_sel* pin, such that the triangle would only change frequency at a peak or trough. This would prevent changes in frequency from causing the rising and falling edges to become misshapen, by keeping any distortion that may occur at the peak and trough. Figure 5-19 shows the circuit used to load in the value of *freq_sel*.

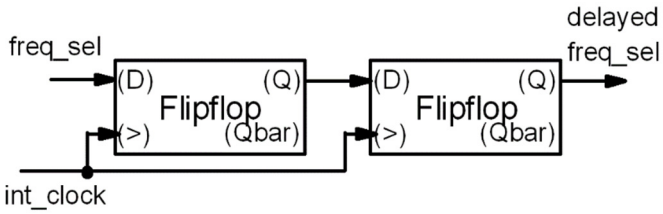

Figure 5-19*: freq_sel* delay circuit, using a pair of D-type flip-flops

Note that two flip-flops were used in series, in case the logical level of *freq_sel* is not well defined at the moment that the clock signal rising edge occurs. This might in turn cause the output of the flip-flop to enter into a poorly defined state, creating meta-stability within the system. Figure 5-20 shows the correct behaviour of the triangle frequency in relation to *freq_sel*.

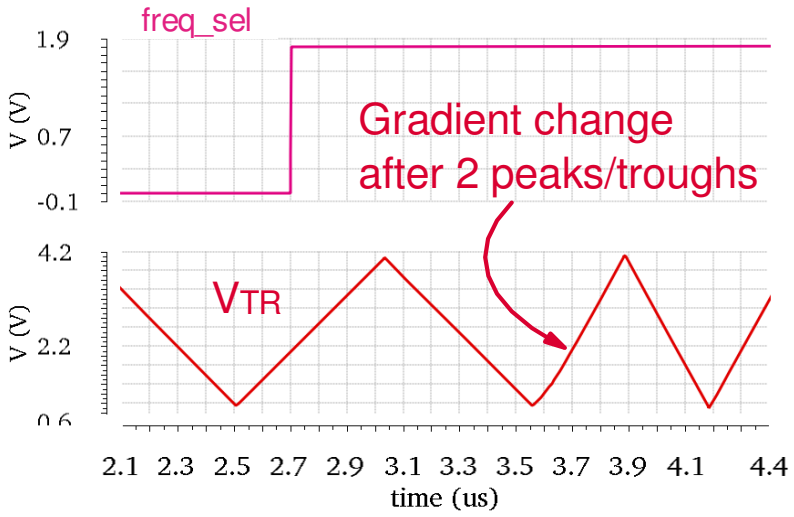

Figure 5-20: Operation of *freq_sel*: change in frequency occurs after two peaks/troughs have occurred after *freq_sel* goes high

5.3.1.3.2 Voltage-to-Current amplifier design

To generate the required reference current from a voltage, a simple op-amp was required. Since the current setting was intended to be static, it was not necessary to have a high bandwidth. In fact, a lower bandwidth was preferable in order to prevent amplification of high frequency noise. PMOS transistors were used for the differential pair input, as these typically have lower flicker noise compared with NMOS devices [39].

The amplifier was however required to have low voltage offset, ideally less than one voltage DAC LSB (i.e. less than 4.9mV). A target nominal systematic offset of less than 100µV was chosen, so that random offset due to layout mismatch would dominate. A target phase margin of 67 degrees was chosen for a critically damped step response, offering the best compromise between speed and overshoot.

A two-stage miller architecture was used as this allowed easy adjustment of the phase margin by means of a compensation capacitor. A two stage architecture also allowed for high voltage gain without the need for cascoding, meaning a larger output voltage swing was possible, making the op-amp more flexible for reuse within other blocks if need be. The schematic and simulation details of this block are in appendix E.

5.3.1.3.3 Buffer amplifier design

The previously designed V-to-I amplifier was not suitable to be used as the current steering buffer, as it was intended to be used with high impedance loads such as FET gates. The buffer amplifier by comparison was required to provide up to 70µA of current, with periodic transition between positive and negative current. A new amplifier was created for this purpose.

The buffer amplifier was not required to have high gain or low offset, since it was effectively acting as a supply of current rather than an absolute voltage and would only be used in unity-gain configuration, hence a single stage amplifier with no cascading was sufficient. Under high current load, it is expected that the output voltage will change due to the comparatively large current flowing through the impedance of the output devices.

Since the buffer was required to provide significant current and one stage was being used, the input differential pair controlling the g_m was therefore made of NMOS devices, due to the higher μC_{OX} allowing for higher transconductance. A full circuit diagram and details of simulation are provided in appendix E.

5.3.1.4 Integration op-amp design

The main amplifier of the triangle generator was designed with transconductance being the primary concern. Although a triangular voltage waveform was desired, this would not be achieved if the transconducance is too low. Figure 5-21 shows the integrating op-amp circuit. The negative feedback of the op-amp means that a voltage offset created by I_{in} is compensated for by the amplifier in order to maintain the virtual Earth condition $V_+ - V_- = 0$, meaning that the amplifier needs to match the current being supplied by I_{in}. By maintaining the virtual Earth condition, the output voltage will be triangular with respect to ground.

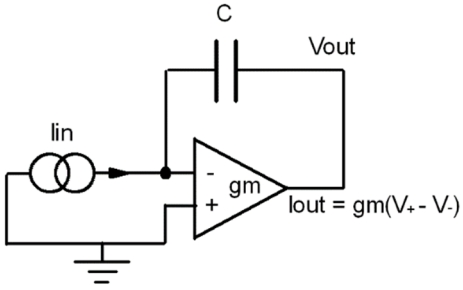

Figure 5-21: Integrator op-amp circuit

In order to achieve a perfect virtual ground, an infinite transconductance would be required. A finite transconductance results in some voltage offset existing at the input terminals of the amplifier, meaning an offset will be created on the triangle. So that the triangle was not significantly distorted, a maximum offset of 10mV was specified, meaning a transconductance of 7mS is required to match a current of 70µA.

In order to easily achieve a high transconductance, a two stage amplifier was used, as the usage of multiple stages would in effect multiply the available transconductance by the voltage gain of the second stage.

The voltage gain was not an important design consideration compared to the transconductance, but would in any case be reasonably high through the use of a two stage design. Since high open loop voltage gain was not required, the unity-gain frequency did not need to be much higher compared with the maximum frequency of operation, and as such was designed to be at least 10 times the maximum frequency of operation, i.e. 20MHz.

With regard to the phase margin, it was acceptable to have a lower phase margin, since the integrating function of the circuit would smooth out any overshoot in current output caused by a step current input change. A target minimum phase margin of 45 degrees was used, although higher values were permitted should they allow for convenient values of compensation capacitance. A full circuit diagram and details of simulation are provided in appendix E.

5.3.1.5 Triangle comparator design

Figure 5-22 shows the block diagram of the triangle comparator. This block was required to determine when the triangle was at the peak and trough voltage, and change direction accordingly. The comparators used were also used in the slice comparator block, where a full description of the architecture may be found. The RS latch comprised of two 1.8V NOR gates which were readily available from the provided logic library.

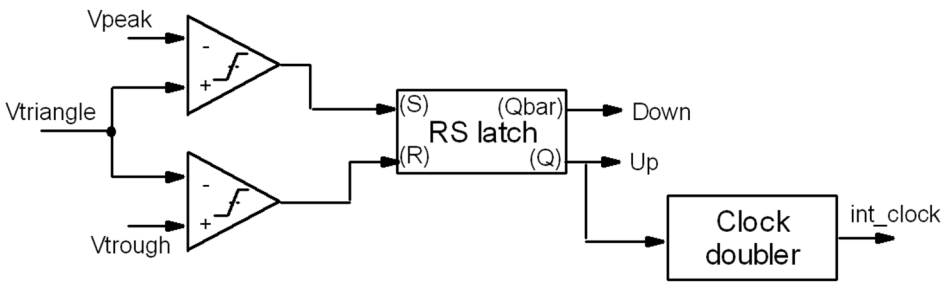

Figure 5-22: Triangle comparator block diagram

The triangle comparator block generated the clock signal for the digital integrator. The previously developed architecture used a continuous self-tuning integrator. However since a digital self-tuning system was used for this design, it was important to consider at what point the value should be updated.

It was desirable to update the digital integrator synchronously with the triangle, as this would avoid the introduction of potential race conditions caused by varying the phase position of a change in the self-tuning value. It was decided to update the digital integrator at the peak and trough of the triangle, as the signals to do this were readily available within the triangle comparator block.

In order to create a pulse from the up/down signals, the architecture in figure 5-23 was used. When settled, the inputs of the XOR gate are the same, hence its output will be 0. When the input signal changes, the XOR inputs will be a different state until the input signal has propagated through the delay block, creating a pulse on the output. A rising or falling edge on the input creates a pulse, hence this

system creates a clock at twice the frequency of the input. The propagation delay of the pulse is determined by that of the XOR gate, which is small compared with the maximum period of operation and hence the clock doubler architecture does not incur significant phase offset.

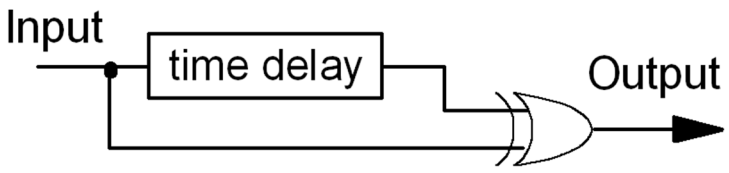

Figure 5-23: Clock doubler block diagram

The desired pulse width needed to be wide enough in order to guarantee that the hold time requirement of the digital integrator's clock is met. Note that the pulse width of the *int_clock* is independent of the operating frequency of V_{TR}. The propagation delay of the provided gates was typically sub-nanosecond. A pulse width of 25ns was therefore chosen so that it would be far longer than the propagation delay, but still small compared with the shortest oscillator period, ensuring that the flip-flop hold requirement would be met. The architecture was tested across all PVT corners and was found to work correctly in all cases.

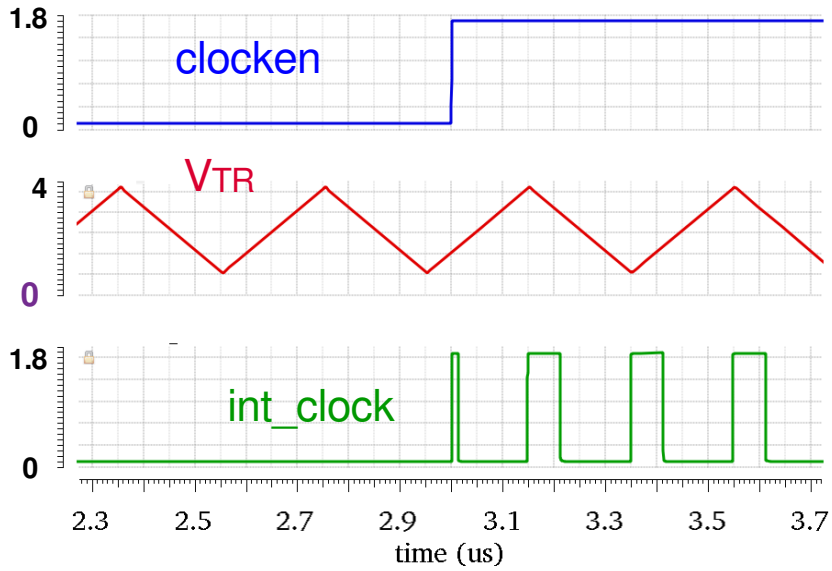

Figure 5-24: Clock doubler and *clocken* in operation

Since it was desired to be able to lock the tuning state with an external pin, the output of the clock doubler was connected to an AND gate. Figure 5-24 shows the clock doubler and *clocken* both in operation with a 2MHz triangle wave. The *int_clock* signal is only available when *clocken* = 1. In this particular test bench, *freq_sel* is being operated at half the frequency of *clocken* to check that *clocken* functions correctly for both values of *freq_sel*.

5.3.2 Voltage DAC

A voltage DAC was required for two purposes: for generating "digital" V_{TUNE} levels to allow for self-tuning by the digital integrator, and for voltage-to-current conversion for triangle generation. This DAC was not required to be high speed, since the levels being generated were for "static" tuning and setting of current levels, although it was preferable that the DAC would settle within one cycle at maximum frequency (i.e. 500ns) for the purposes of self-tuning.

From the perspective of triangle generation, high linearity was not highly critical, since it was already expected that frequency setting would require manual calibration for the purposes of testing and

demonstration. Self-tuning also does not require that the DAC be highly linear because the integrator would naturally converge onto whatever setting was optimal for the best tuning of the LC tank.

It was however necessary that the DAC was guaranteed to be monotonic. Otherwise, a decrease in DAC output with an increase in the input code could cause instability in the self-tuning control loop by turning negative feedback into positive feedback. In order to achieve guaranteed monotonicity, a thermometer DAC was used as per figure 5-25. A string of equal-sized resistors was used to generate a sequence of monotonic voltages, the desired output voltage being achieved simply by connecting to it with a switch.

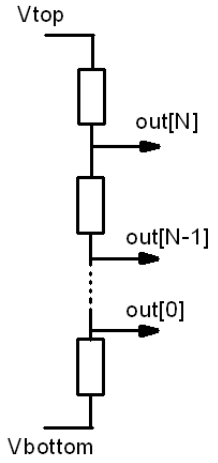

Figure 5-25: Thermometer DAC concept using a fixed unit resistance

Since symmetrical slice levels were required, both with 8 bits of resolution, the main voltage DAC block was created as two 8 bit thermometers connected in series. This would guarantee that the slice levels would not overlap. It also permitted easy re-use of the voltage DAC architecture in the current DAC for the triangle generator.

Transmission gate switches were connected to every tapping point on the thermometer so that charge injection would not cause the DAC voltage to become significantly offset during a code change. For phase trimming, the upper and lower halves of the DAC string were made “dual tap”, i.e. connected to two independent transmission gates with their own decode logic.

Although it was not critical, this DAC architecture is also capable of high linearity provided the resistors are well matched between one another, which may be achieved by making the resistors sufficiently large and using good layout techniques. Figure 5-26 shows conceptually how resistors were laid out to achieve this, by alternating device numbering in a zig-zag fashion. The resistor string numbering also begins and ends in the same corner of the layout, so the effect of process variation across the die is averaged across the string, improving the linearity.

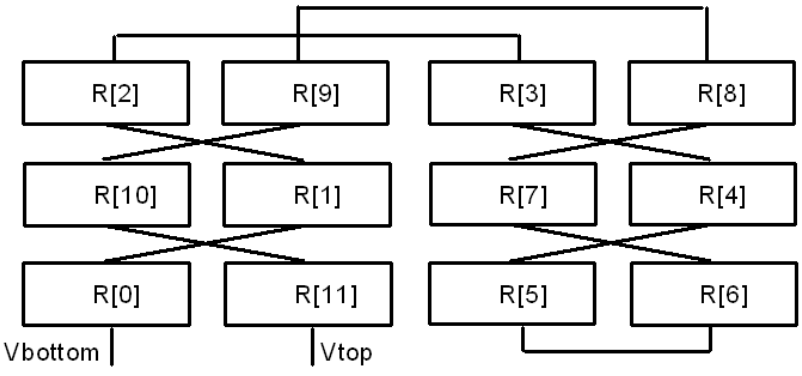

Figure 5-26: Thermometer DAC resistor layout technique to compensate for process gradient across the die area

Since the DAC thermometer had to operate across the entire voltage range of the triangle, i.e. 1V to 4V, the tapping switches were required to be 5V FETs. The decoding logic for selecting the correct switch could have been implemented with 1.8V logic and level shifters used on the decoded output. It was however decided to use level shifters on the DAC selection code and create the decode logic entirely in 5V, as this would require less area overall.

Due to the propagation delay of the decode logic, there was a brief time period when multiple output taps could be connected at the same time, which would short circuit part of the thermometer string. Given the relatively high resistance, this would therefore potentially cause a long time period for which the thermometer voltages need to recharge, distorting the slice levels and causing detuning.

To prevent decode logic propagation from perturbing the slice levels, it was decided to create an enable signal which would control every tap switch in parallel. Every DAC switch would be opened before the DAC code was updated, meaning that the settling glitches would not cause the thermometer to become short circuited at any point. A *break-before-make* signal was therefore required to implement this behaviour.

The *int_clock* signal was used to determine when the DAC code will change, since this is used by the self-tuning integrator that controls the DAC code. To prevent the switches from being closed unnecessarily, the *update* flag from the digital integrator was used to indicate if the slice level is about to change. The *int_clock* and *update* signals were fed through a NAND gate, creating an enable signal for the decode logic. Figure 5-27 shows the initial DAC architecture developed.

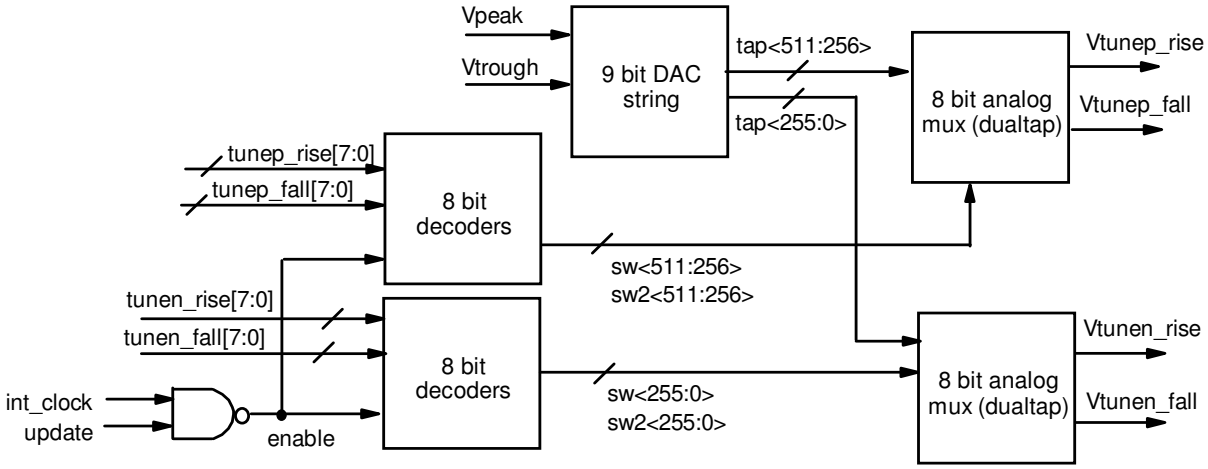

Figure 5-27: Initial voltage DAC architecture used

It was however found that with a conventional decoder the area required was extremely large. Figure 5-28 shows the completed layout, which was approximately 1.39mm tall and 0.59mm wide. The allocated space for the IC die was 5mm^2, which would also need to include the pad ring for connecting to the pins. Hence the DAC architecture needed to be changed in order to make it fit within the area.

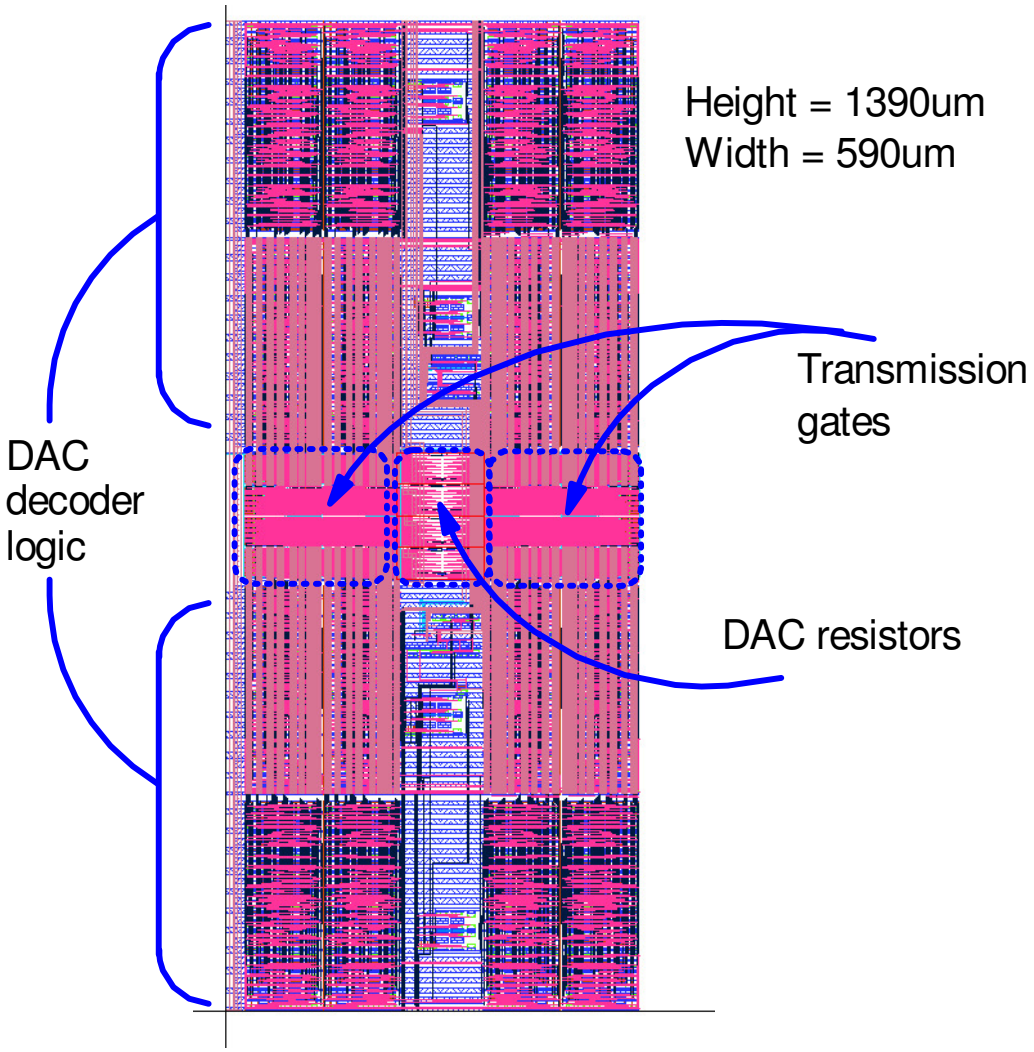

Figure 5-28:Annotated initial DAC block completed layout

By far the biggest consumption of area is due to the 5V decode logic. This was because of the minimum size requirements of the 5V FETs were much larger than those for 1.8V FETs. To reduce the size of the voltage DAC, it was important therefore to find a decode strategy which would require less area.

One area of improvement was to create 5V logic gates using only minimum sized FETs. The first set of gates created attempted to match the gain factors of the NMOS and PMOS by increasing the width/length ratio of the PMOS in order to have symmetrical rise and fall times. Upon further consideration, it was deemed to be unnecessary to try to match the rise and fall times, since the gates required were for static logic where this would not be a major concern. Given the large number of gates required, a small improvement in the area consumed by the logic gates would scale to produce larger area savings overall. Figure 5-29 shows examples that the older and newer logic gate layout produced, the area before and after being approximately 493μm^2 and 120μm^2 respectively.

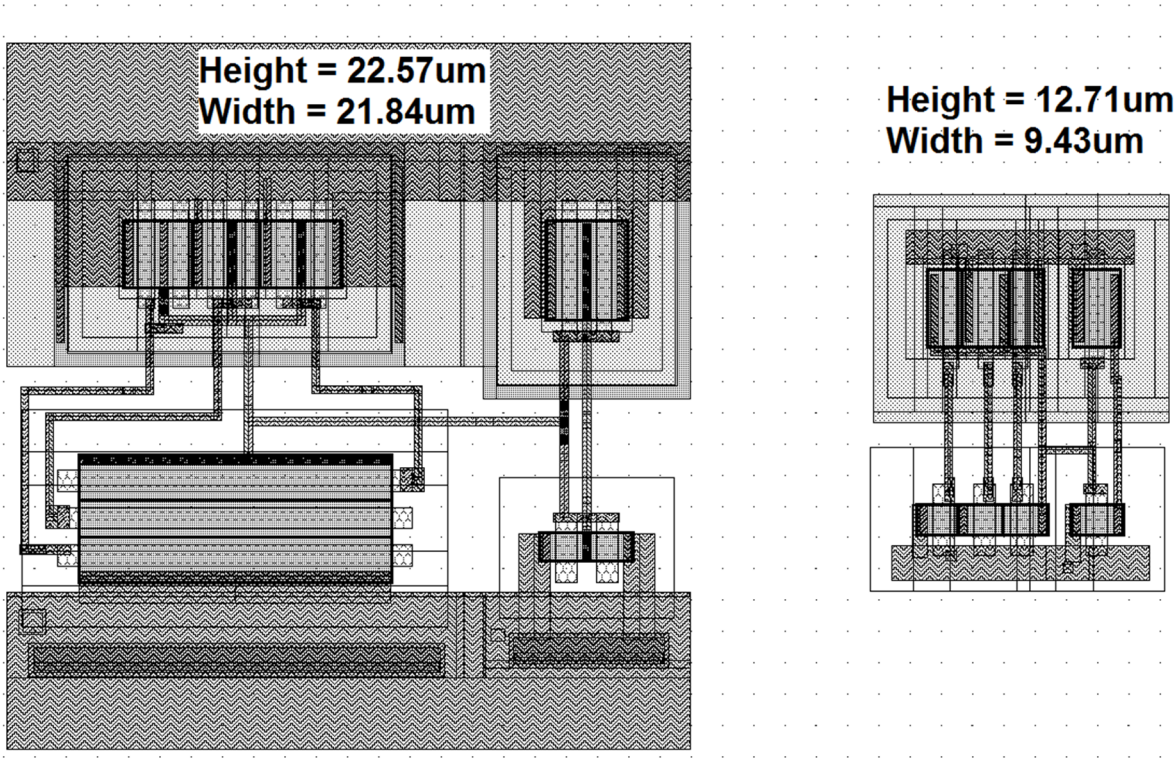

Figure 5-29: 3-input AND gate before (left) and after (right) layout area reduction. Area reduced from 493µm^2 to 120µm^2

Even with improvements in logic gate size, more area savings were required. A better decoder architecture was therefore required. It was decided to split up the decoder logic into smaller units. The DAC was further compartmentalised into 7 bit units as opposed to 8 bits to further speed up development time. Each 7 bit DAC would then use a combination of 5 bit and 2 bit decoders in a grid structure to implement decoding. This saved area because, with a simpler decoder architecture, the area required for each additional bit doubles, since twice as many gates are needed for each layer of logic used. Breaking the problem down as per figure 5-30 means two smaller decoders may be used, with a combined area which is smaller than a single 7 bit decoder.

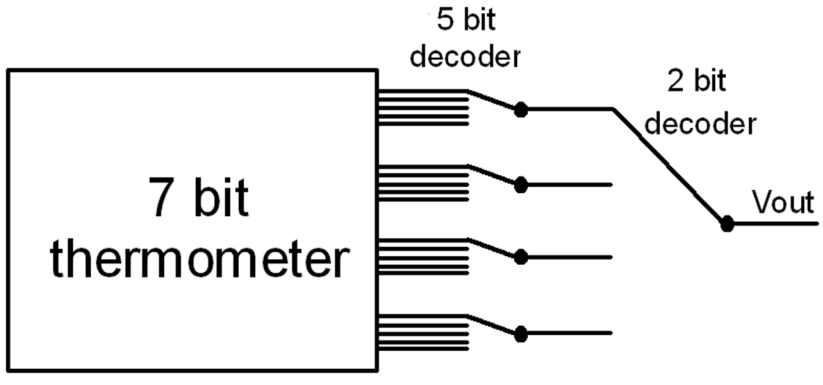

Figure 5-30: Two-stage decoder for a 7 bit thermometer DAC

To further simplify the decode logic, the transmission gate switches were replaced with PMOS-only for the upper half and NMOS-only for the lower half. This meant that complementary drive to the switches was not necessary, further reducing the area consumed. The break-before-make signal was split up, so that the rising and falling edge DAC values could be updated at different times, meaning any charge injection caused by the switches opening would not cause unwanted glitches on the slice levels.

The improved voltage DAC block layout shown in figure 5-31 had a height of approximately 0.5mm and width of approximately 0.28mm, the consumed area being approximately 5.8 times less than the first design. This significant improvement meant that the new DAC architecture could be realistically used with the rest of the system.

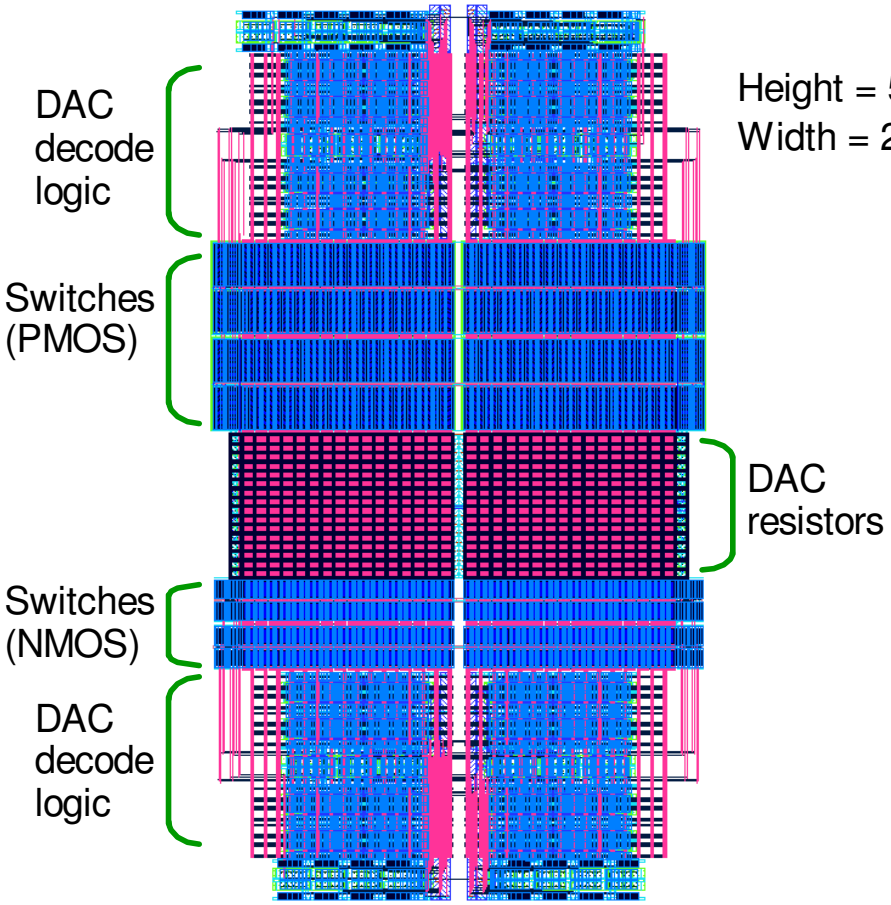

Figure 5-31: Improved DAC layout

Note that during breadboard testing, it was found that self-tuning would not work correctly if the tuning switches do not activate at all. This was caused by V_{TUNE} being too close to the peaks and troughs of triangle wave V_{TR}, preventing the HV switch from opening, and hence there was no closure event to use to determine the resonant condition. In the unipolar switching architecture, it was also important to prevent both HV switches from opening at the same time, as this would cause all tuning capacitance to be removed from the antenna and heavily detune it.

In order to solve these problems, additional limiting resistance was added at both the top and bottom of the DAC thermometer strings and in between the strings. This would prevent the V_{TUNE} voltages from becoming equal to each other or to the peak and trough voltages of V_{TR}. The tradeoff with this approach is that some tune range is lost because the switches can be neither completely closed for 100% of the cycle, nor can they be open for 50% of the cycle.

To prevent too much tune range from being lost whilst still ensuring self-tuning was attainable, it was decided to calculate the limit resistor sizes for operation at 1.5MHz. Above this frequency it cannot be guaranteed that the system will self-tune correctly, as at the Θ pulses at the peaks and troughs may not provide sufficient duration for the switch sign sampler flip-flop to operate correctly. It was deemed necessary to compromise at 1.5MHz to ensure that functionality could still be achieved above 1MHz at least.

The limiting resistor at the middle of the resistor string was required to create at least 20ns of margin to ensure that one switch would always close before the other. At 1.5MHz, the triangle gradient is 9MV/s, hence for 20ns of margin a voltage offset of 180mV is required.

At the peak and trough, the required amount of margin is determined by the minimum switch voltage excursion time. Figure 5-32 shows the critical event path, with times provided from the worst propagation delays of each block.

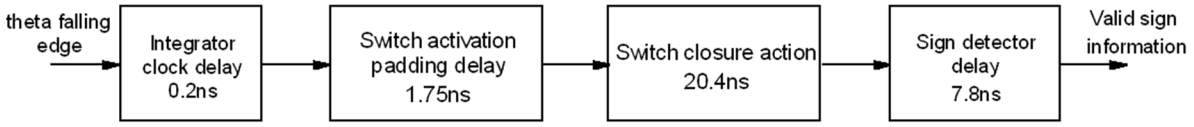

Figure 5-32: Critical timing path for obtaining valid sign information, total margin required 30.15ns

Note that the triangle generator inherently provides some of this margin, as there is approximately 5ns propagation delay between the peak or trough being detected and the triangle changing direction, creating a 10ns overshoot time. This provided margin may be subtracted from the time requirement for the switch control, meaning approximately 20ns must be provided by the limiting resistor. The 20ns required margin is partitioned across the rising and falling edges of the triangle as per figure 5-33, hence the peak and trough limiting resistors need to add 10ns on each edge.

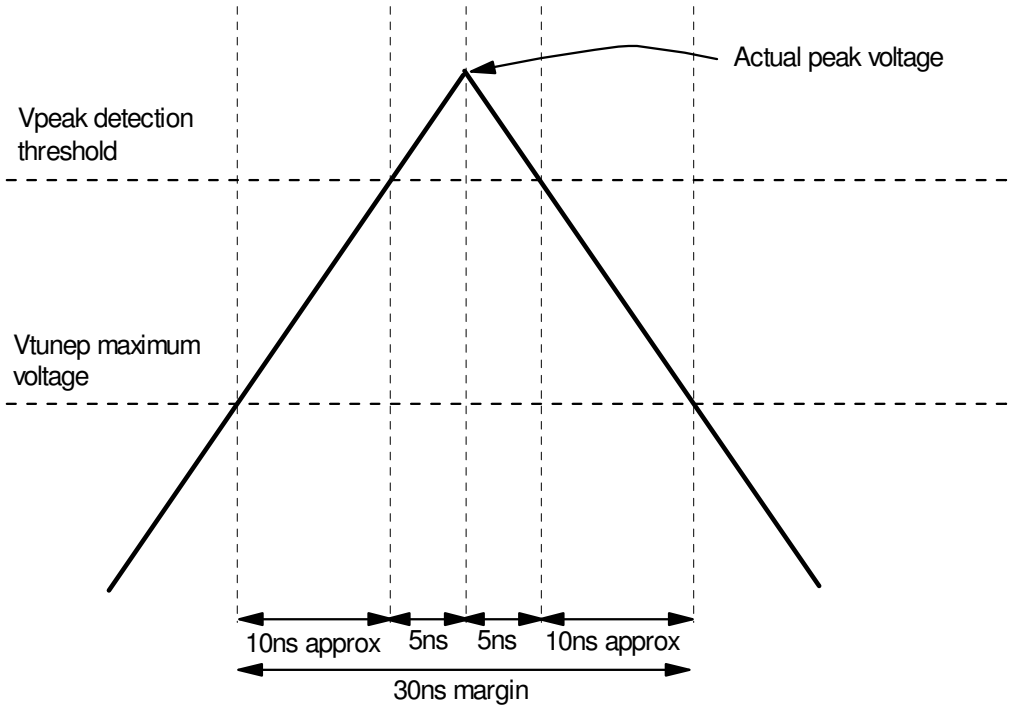

Figure 5-33: Timing margin allocation at triangle peak/trough

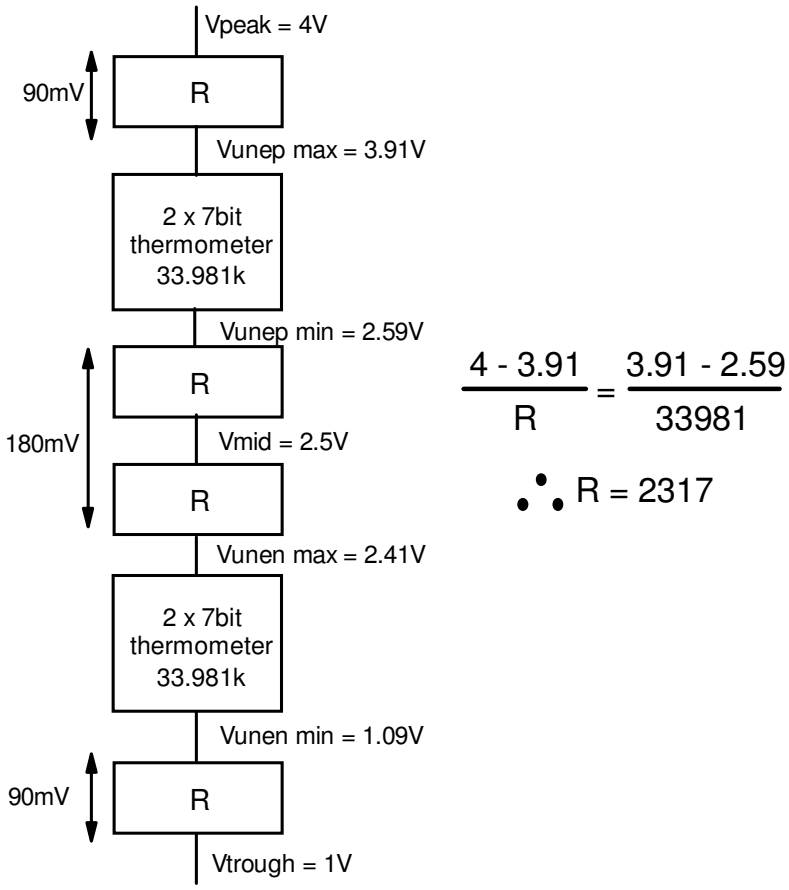

Figure 5-34: Limiting resistor value calculation method

Figure 5-34 shows how the limit resistance may be calculated. The calculated limit resistor value R was approximately equal to 18 unit resistor values of the DAC thermometer. It was decided to use 16 resistors as this allowed for fast layout creation. It meant however that the time margin would be reduced slightly, meaning that correct operation would not be guaranteed at all frequencies.

By using smaller limit resistors, the voltage from each resistor was reduced from 90mV to 80mV, meaning the maximum triangle slew rate of guaranteed correct operation was reduced to 8MV/s, leading to a frequency of 1.33MHz. This was still acceptable for demonstration of fractional capacitance self-tuning in the MHz region. Figure 5-35 shows the final block diagram of the voltage DAC architecture.

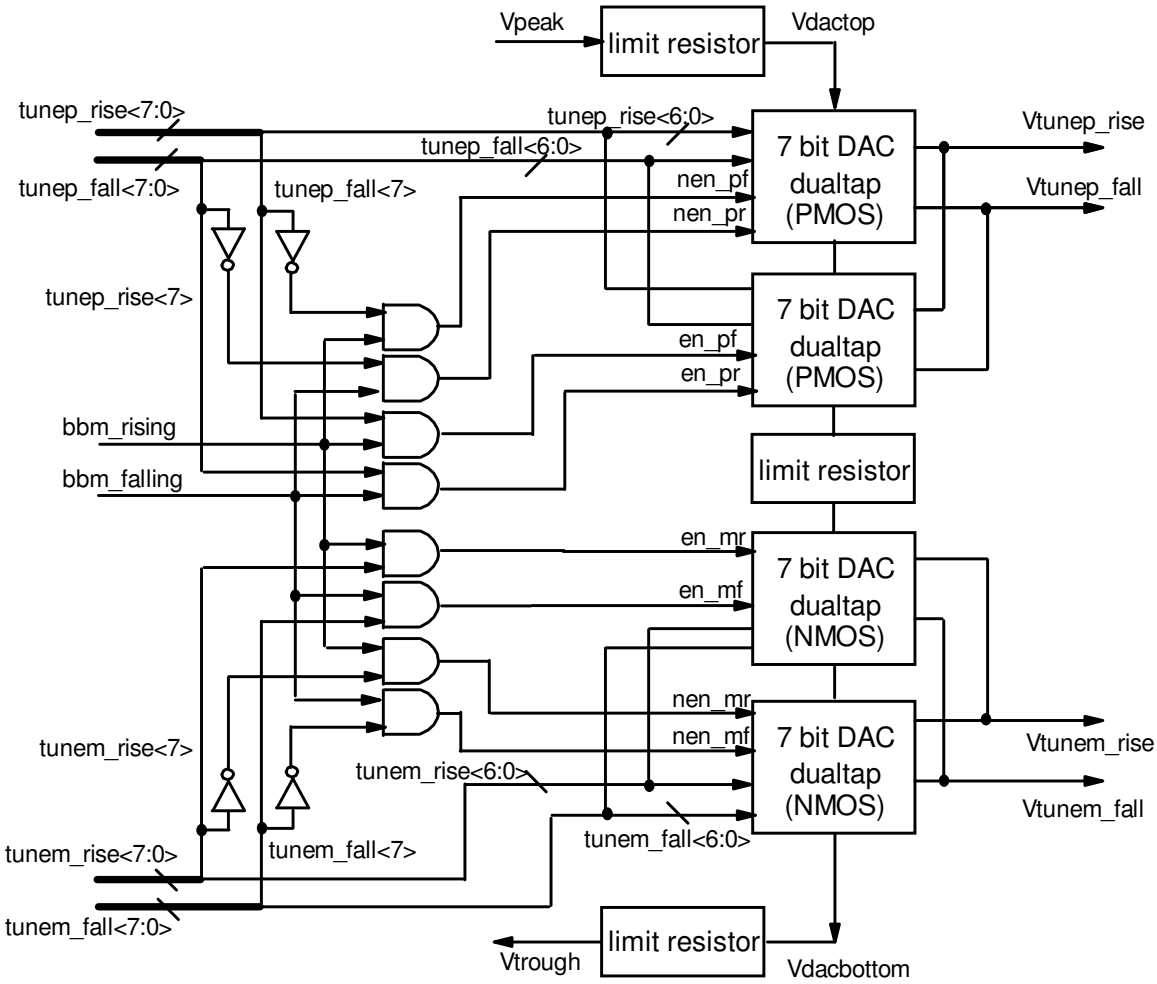

Figure 5-35:Voltage DAC final architecture

Figure 5-36 shows the output voltage of the extracted DAC layout when the input code is stepped between 0 and 255. The break-before-make is activated for 25ns, which is prototypical to normal operation. The slice comparator block is used as a dummy load to accurately model the load that would be observed by the DAC in normal operation. When connecting to the extremities of the DAC (i.e. towards 1V or 4V), the settling time is typically 13ns, however when connecting to the middle of the DAC (i.e. towards 2.5V), the settling time increases to around 740ns.

The difference in settling time is expected, since the input capacitance of the op-amp has to charge through the full DAC thermometer resistance when the tap at the midpoint is connected, whereas at the extremities this resistance is very small. A settling time of 740ns corresponds to operation at 1.35MHz, which is slightly higher than the maximum frequency of guaranteed correct operation. This settling time was therefore deemed to be acceptable.

Figure 5-37 shows the upper and lower half outputs of the voltage DAC, with the input values swept from 255 to 0. Note that symmetry in slicing levels must be done externally to the DAC. The response is linear, although the break-before-make causes charge injection, increasing the voltage at the output when the switches are opened. Provided the DAC voltage is updated on the half of the cycle where its output is not being compared, this charge injection will not cause detuning.

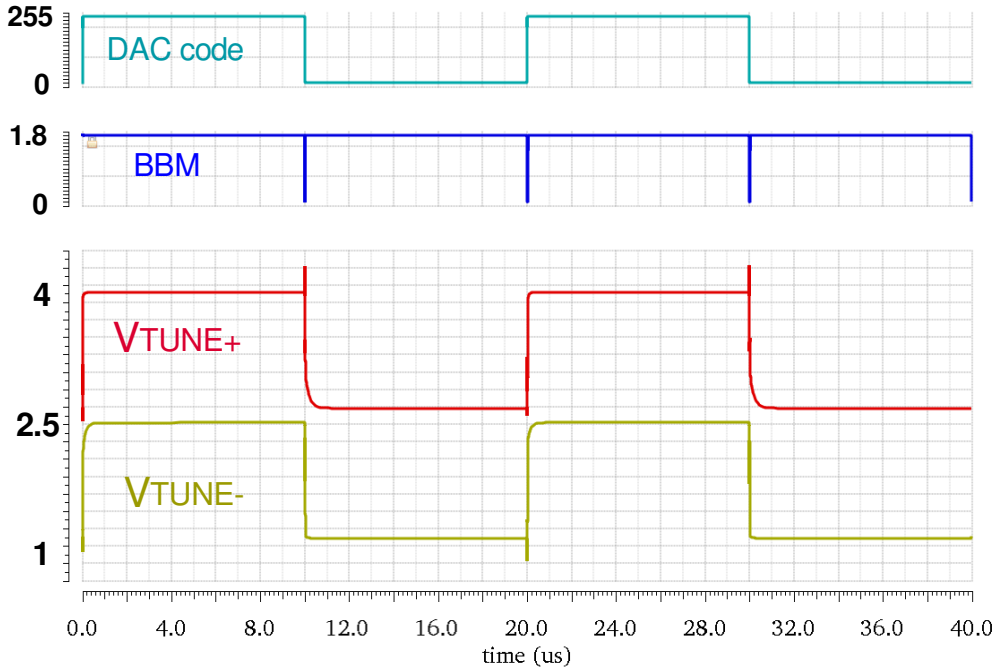

Figure 5-36: Voltage DAC stepping from one end of the thermometer to the other

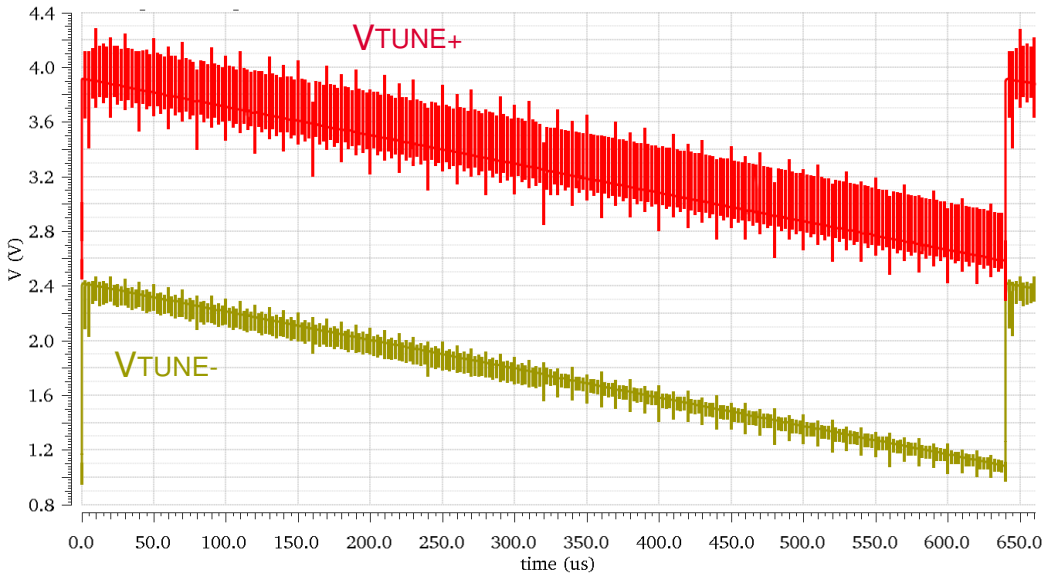

Figure 5-37: Sweep of DAC voltages (decreasing codes)

5.3.3 Slice comparator

The slice comparator generates the theta timing signals, used to both control the capacitor switches and the switch voltage sampling circuit. It should be noted that the triangle operated in the 5V domain to allow for reduced sensitivity to comparator voltage offset, however the switch control logic operated in the 1.8V domain to permit use of the fast and readily-available logic gate library. As such, it was necessary to create a comparator architecture which would accept a 5V input and generate a 1.8V output.

A two-stage architecture was developed, the first stage comprising of a 5V pre-amp and second formed of a 1.8V high-speed comparator. So that the comparator would not introduce unacceptable amounts of phase shift, a target propagation delay for the whole block was intended to be less than 1% of phase shift at maximum frequency, which at 2MHz is equivalent to 5ns.

5.3.3.1 *Pre-amp design*

The first stage was made fully differential so that it could easily drive the second stage. Figure 5-38 shows the architecture used.

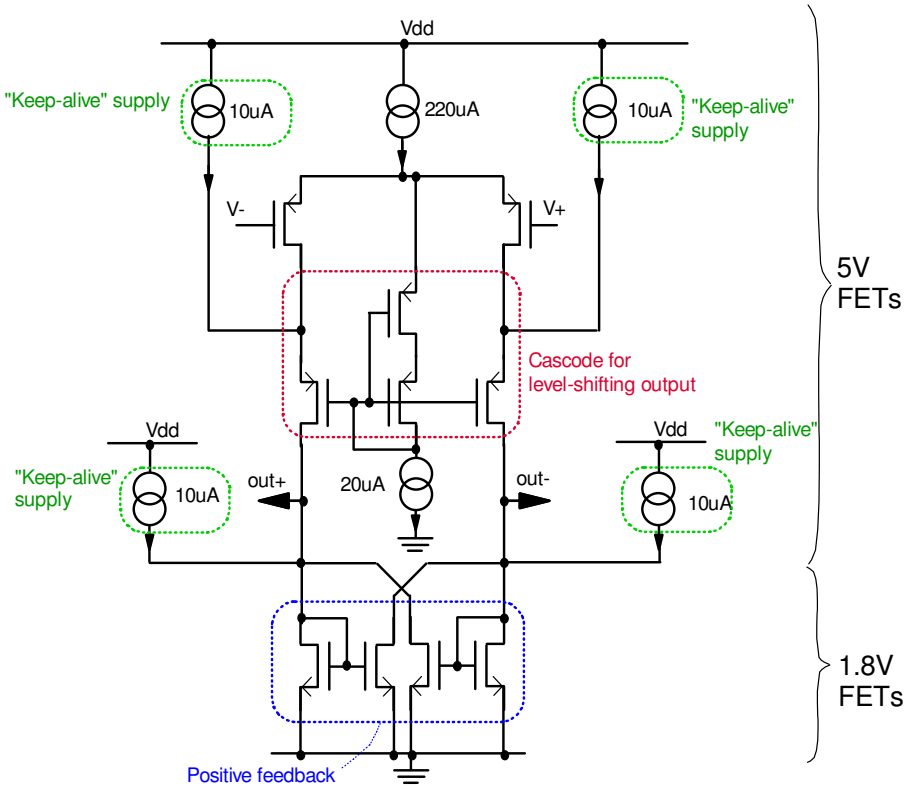

Figure 5-38: Comparator preamp simplified circuit, showing key functionality

The gain of the amplifier was made as large as possible by using positive feedback, implemented with cross-coupled NMOS transistors. Although the preamp had a 5V supply these cross-coupled devices were 1.8V FETs. This was possible due to the devices being diode connected and protected by the cascode for the PMOS input differential pair. The higher μC_{OX} of the 1.8V FETs compared with the 5V FETs helped increase the speed of the pre-amp.

Another important function of the pre-amp was to provide an output level that was compatible with the next stage. The output common mode was designed to be approximately 0.8V. This was achieved by cascoding the PMOS differential pair input but not the NMOS load. The NMOS load would also naturally have a low V_{ds} due to being diode connected.

To speed up the comparator further, it was necessary to inject small amounts of current to both sides to prevent device channels from discharging when the output voltage is low, as would occur for either the right or left hand side depending on which input is the greater. Otherwise, the channels would require re-charging each time a change in output occurs, slowing down operation of the comparator. Hence, a 10uA current was injected into the 1.8V positive feedback NMOS devices and the 5V PMOS cascode device, which was found to be enough to maintain saturation without significantly altering the output voltage.

The use of auto-zeroing techniques to cancel the systematic offset of the preamp was considered. However, the use of a symmetrical architecture resulted in a sufficiently small offset so that this was unnecessary. The measured random offset of the extracted layout from 300 Monte Carlo simulations had a mean of 99.9µV and sigma of 2.745mV. This sigma value was less than the maximum permitted

offset in order to achieve better than 1^{O} switching accuracy, hence the preamp would still yield sufficient parts meeting the specification even without auto-zeroing.

The nominal propagation delay of the pre-amp was 4.5ns. This is just below the 1% of maximum frequency target, although when considering the second stage of the comparator, the overall delay begins to exceed this target propagation speed for the block. Across process, voltage and temperature (PVT) corners, the worst propagation delay was 5.82ns. With further tweaking, this propagation delay could be reduced further, however the value was considered to be close enough to the target delay, with any excessive timing offset being manually compensated using the phase trimming function if need be.

5.3.3.2 Second stage design

The second stage of the continuous comparator was designed as a symmetrical cascoded amplifier. Since the preamp had level shifted down to a common-mode of 0.8V, the second stage was implemented entirely with 1.8V transistors for maximum speed. The symmetrical op-amp output will swing towards V_{DD} or 0V, depending upon the polarity of the inputs, i.e. only the PMOS or NMOS devices will be operating. To provide a path for the current to flow, a Traff current comparator was connected to the output of the symmetrical opamp. The input devices of the Traff comparator act as resistors with resistance of $1/g_m$, with only one switched on at a time, depending upon the sign of the input current [40]. When the opamp inputs change polarity, the opamp output current also changes polarity, causing the Traff comparator to switch its output state to continue providing current to the opamp. Figure 5-39 shows the circuit used for the second stage.

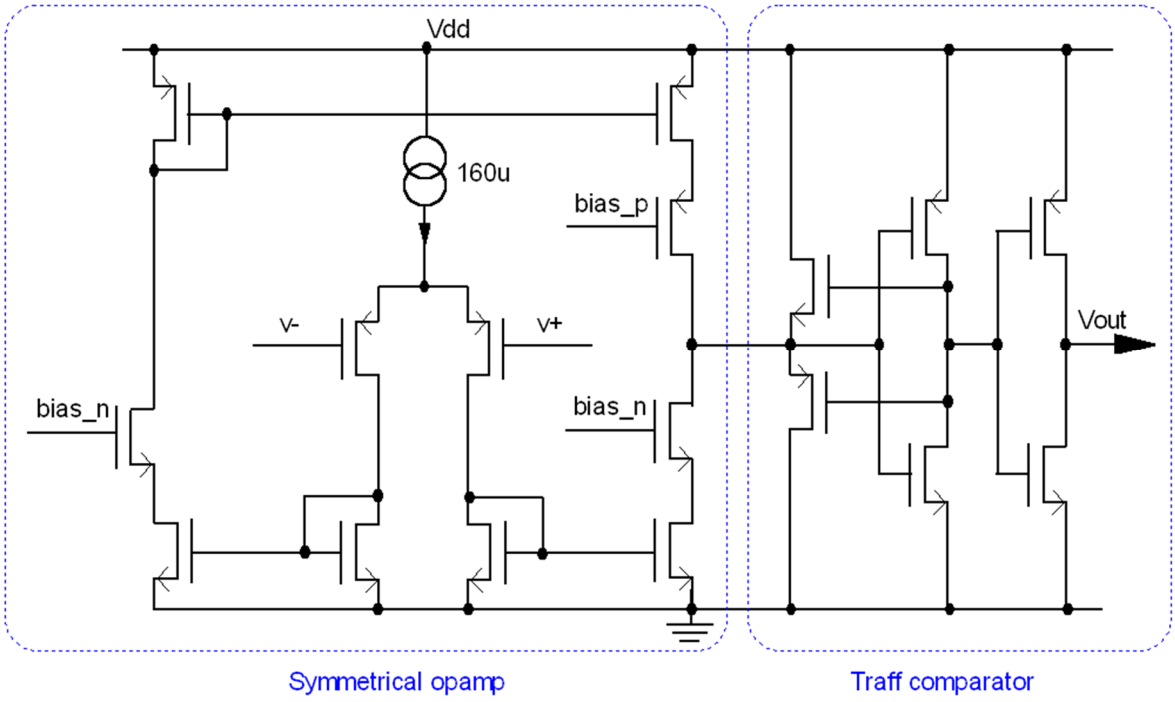

Figure 5-39: Comparator second stage: Symmetrical op-amp and Traff comparator

The systematic offset of this second stage was not critical as the first stage was dominant in this regard. The propagation delay was nominally 1.47ns, the worst PVT corner yielding a delay of 1.9ns. This is well within the 1% target at maximum frequency, although the comparator overall is slightly slower than this target. It was decided that further adjustment of the design would not be justifiable given the limited design time left.

Figure 5-40 shows the transient response of the first and second stages. Figure 5-41 shows a close-up of the triggering of the comparator. It can be seen that the majority of the delay is incurred by the preamp, with the second stage providing a very distinct logical output level.

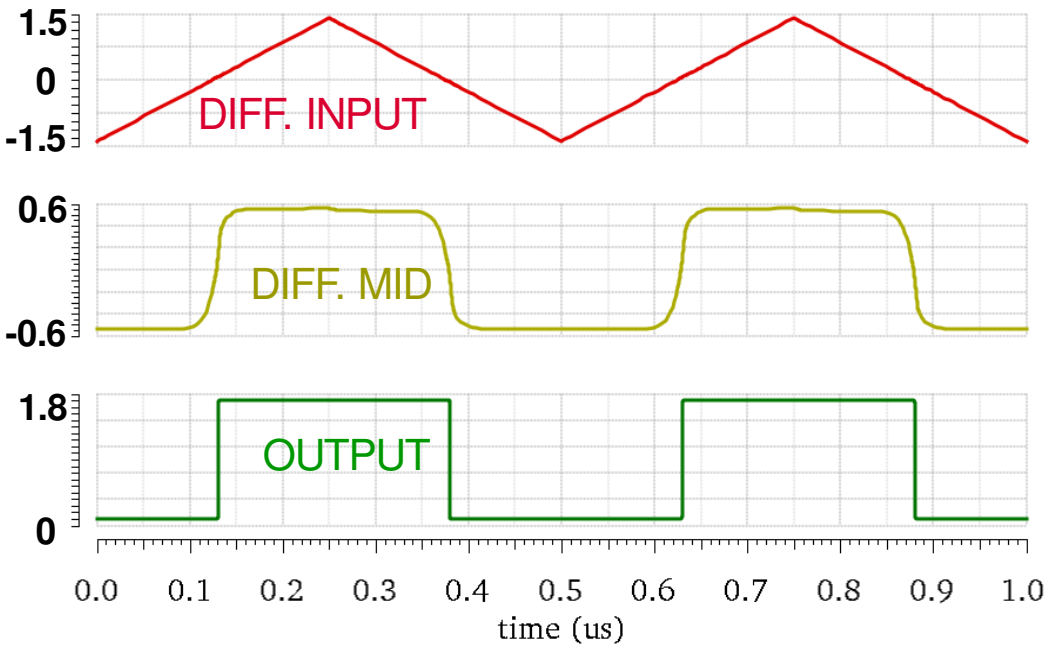

Figure 5-40: Complete comparator response, showing differential input, middle differential signal and binary output

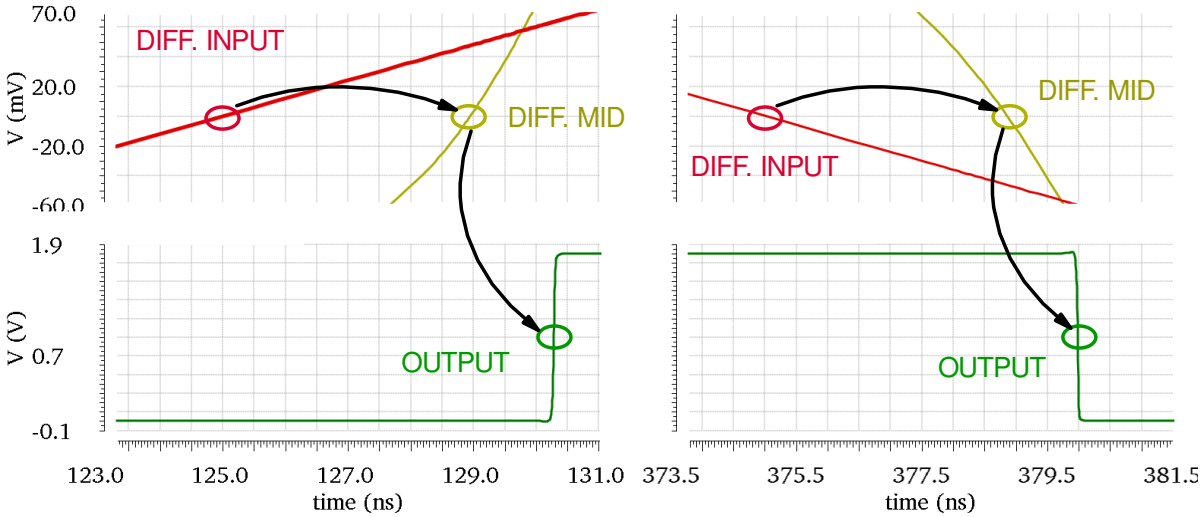

Figure 5-41: Complete comparator response, close-up of the rising (right) and falling (left) edge triggering events

5.3.3.3 Slice comparator architecture

As described in the digital control section, phase trimming by adjustment of triangle slicing levels is a desirable functionality in order to correct for timing offsets which may cause sub-optimal tuning. Phase trimming may be implemented by having different sets of slicing levels for the rising and falling edges of the triangle. One possible implementation is to switch between the slicing levels for two comparators, however the changeover between slice levels risks causing the comparator to generate a glitch, creating undesirable timing behaviour. It was therefore decided to have one comparator for each of the four independent slice levels, and multiplex between the outputs depending on the direction of the triangle. Figure 5-42 shows the slice comparator architecture.

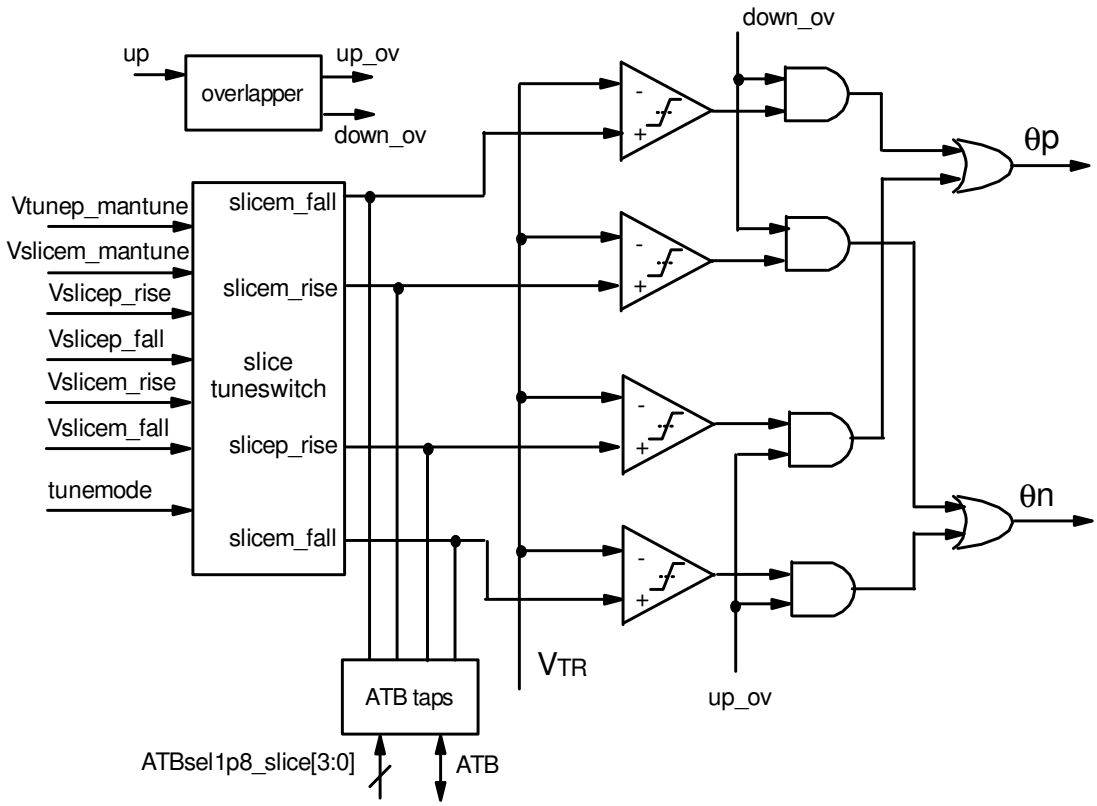

Figure 5-42: Slice comparator architecture

Note that although multiplexer blocks were readily available from the provided 1.8V logic library, it was necessary to create a custom version, whereby both inputs may be selected. During the transition between up and down, there is a brief time period where neither comparator may be selected, creating a glitch on the final output of the block. To prevent this problem from occurring, an "overlapper" was used to create replicas of the up and down control signals which would be guaranteed to have an overlapping phase whereby one of the outputs would always rise to logic 1 before the other fell to logic 0.

Figure 5-43 shows the circuit used to implement this. Figure 5-44 shows the simulated edges to show the overlapping behaviour in operation. Since the outputs are complementary, the circuit is suitable to create the required overlapping up and down signals.

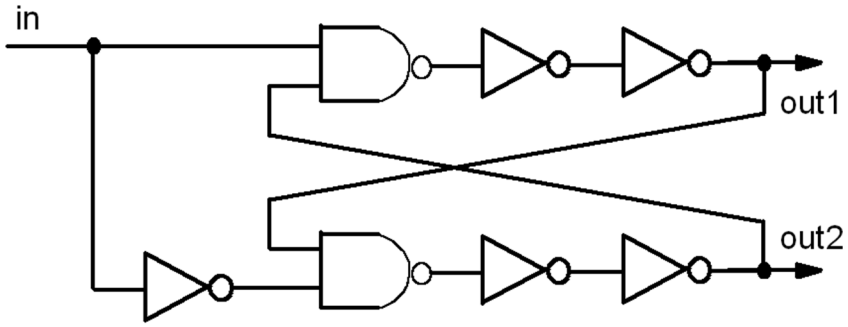

Figure 5-43: Overlapper architecture

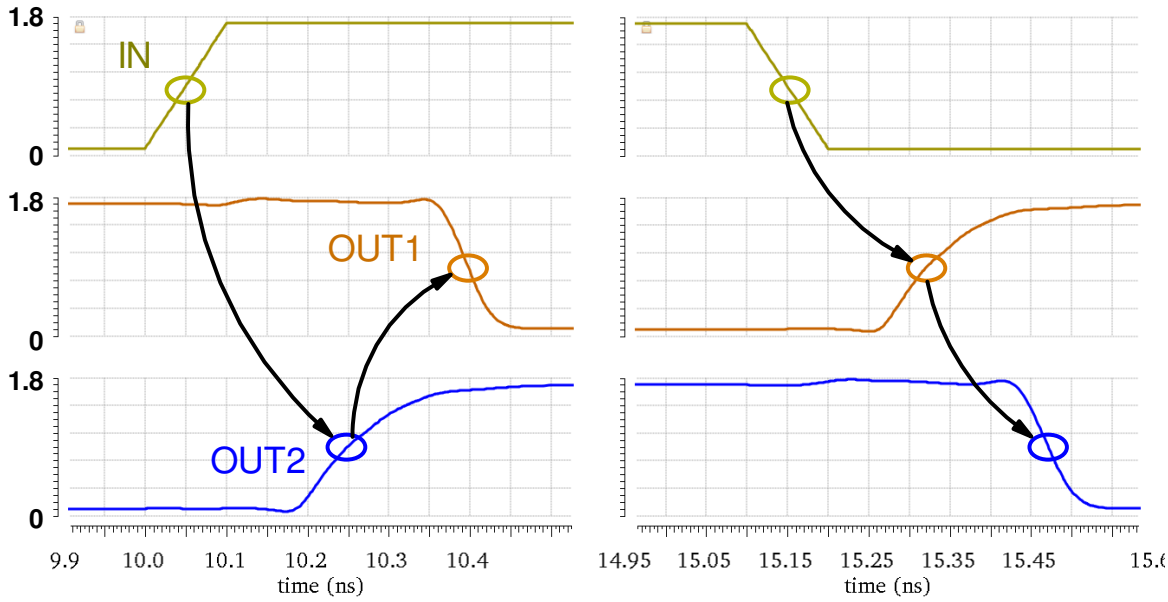

Figure 5-44: Overlapper block in operation, showing both outputs becoming logic 1 during both transitions

The measured worst-case propagation delay of the extracted layout of the overlapper across PVT corners was 462.5ps, equating to 0.33 degrees at 2MHz. Figure 5-45 shows the slice comparator block function in operation. The slice levels are shifted to show phase trimming operating correctly.

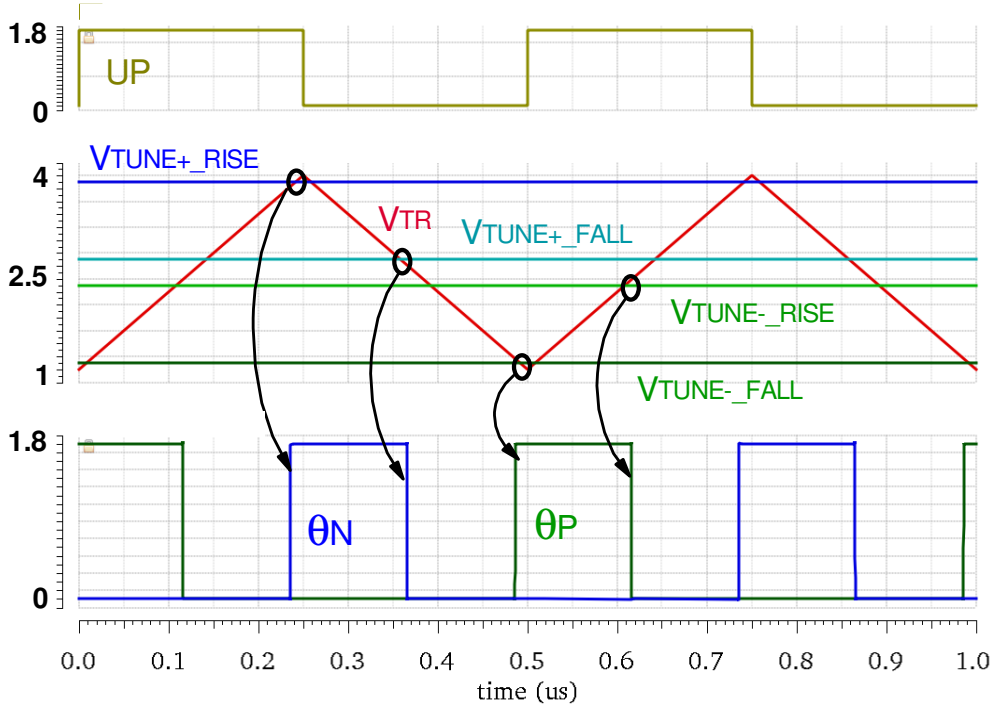

Figure 5-45: Slice comparator block operation at 2MHz, showing phase trimming in operation

5.3.4 Timing block

As has been shown in earlier descriptions, correct operation of the system was dependent on the correct sequence of several signals. The HV switch controls $\Theta_{N/P}$ generated by the slice comparators determined when the capacitor switches were activated, and also when the sampling of the capacitor switch voltage occurred. Figure 5-46 shows that a simple delay line is sufficient to enforce each event.

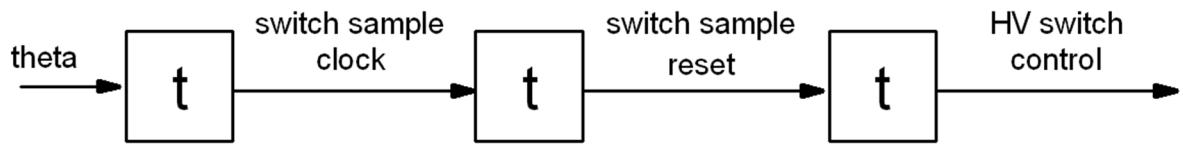

Figure 5-46: Timing block delay line

The switch sample clock was connected to a 1.8V logic flip-flop, with a sub-ns propagation delay. In order to guarantee that this flip-flop would correctly record the required data, the switch sample reset was specified to have a 1ns delay behind this clock signal.

The switching action had to occur after the switch voltage sampling, so a further delay block was added to ensure that this would occur. In practice, the propagation delay of the high-voltage switches was around 10ns, meaning that further delay was not in theory necessary. It was felt however that the timing block should nonetheless be included to guarantee the correct sequence of operation.

Additionally, the timing block contained level-shifters to drive buffers for the Θ*lvhs* and *lvls* outputs, which were derived from the HV switch control line. Figure 5-47 shows the timing sequence in operation. The reset signal has a lower rising edge due to its input being derived from a 1ns delay block, comprised of an RC circuit sized for a nominal propagation delay of 1ns.

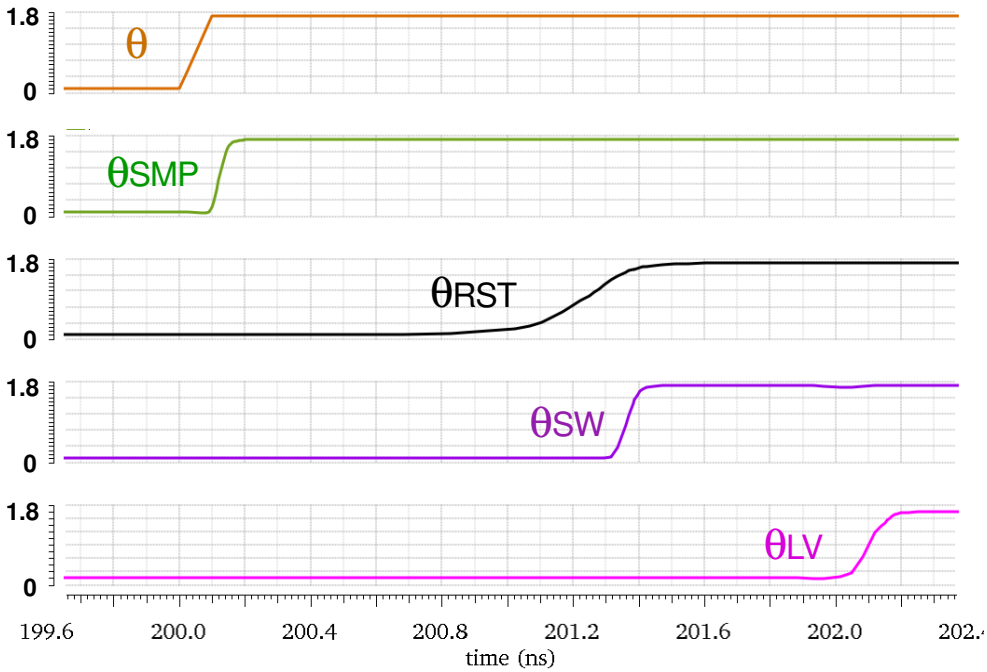

Figure 5-47: Timing block timing chain simulation, showing the correct signal sequence

As well as deriving system timings from the Θ signals, the timing block created the *break-before-make* signal required for the voltage DAC. To ensure correct operation, it was necessary to ensure that the DAC output switches were opened before the input codes were updated. The circuit in figure 5-48 was used to enforce this condition.

Regarding the logic of the *break-before-make* function, a code change at the input of the DAC is impending if the digital integrator's update flag is high when the *int_clock* is triggered. The active-low *break-before-mak*e is therefore the result of a NAND function on these two signals. A pair of OR gates are used to ensure that *break-before-mak*e is not activated on the DAC currently in use.

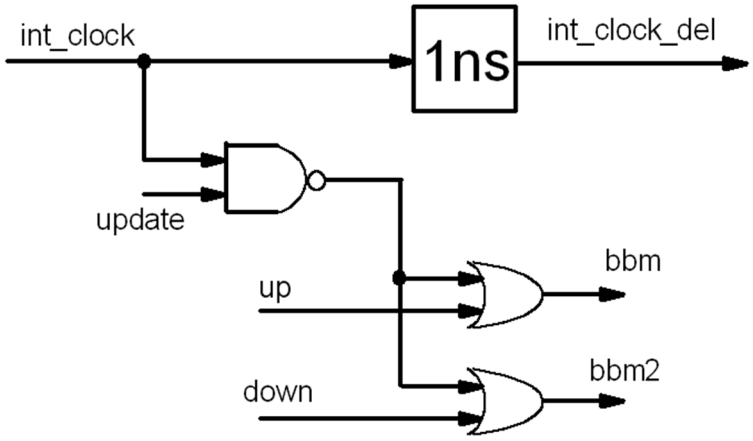

Figure 5-48: Timing block "break-before-make" control

Figure 5-49 shows the correct operation of *break-before-make* within the timing block. The delayed clock to the digital integrator occurs approximately 1ns after the input *int_clock*, by which time *break-before-make* has already been activated. This means that the switches on the DAC are all disconnected before a new code is presented, meaning the logic may settle without the risk of short-circuiting the resistor chain of the DAC and perturbing the slice levels.

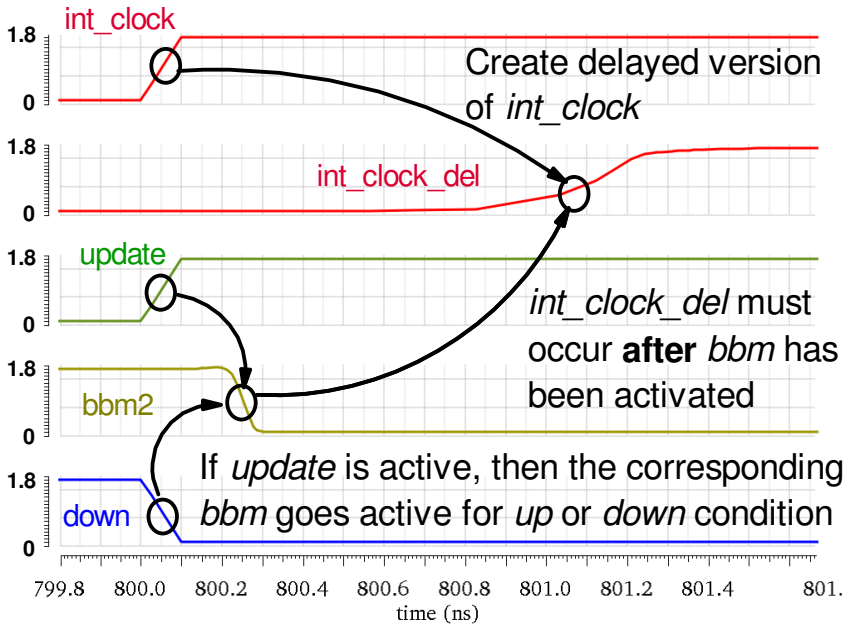

Figure 5-49: Break-before-make activation simulation

Table 5-3 shows the simulated PVT corner results of the timing block modules for the extracted layout. All delays are below 5ns, meeting the target 1% delay at 2MHz. The timing block will therefore not add excessive phase offset to the critical timings of the system.

Signal	Relative to	Slowest	Nominal	Fastest
Θ_{SMP} Switch sample clock	Θ	139ps	74.48ps	60.11ps
Θ_{RST} Switch sample reset	Θ	1.822ns	1.186ns	791.3ps
Θ_{SW} HV Switch control	Θ	2.640ns	1.317n	891.8ps
Θ_{LV} output buffer drive	Θ	3.863ns	2.058ns	1.241ns
Int_clock_del	Int_clock	1.650ns	1.076ns	720.2ps
BBM	Int_clock_del	1.373ns	844ps	524.7p

Table 5-3: Propagation delay for timing block across PVT corners

5.3.5 Tank driver

The tank driver was required to provide a sufficiently large current (100mA maximum) so that a high Q factor tank may be driven directly from the IC. Due to time constraints, it was necessary to design a simple buffer that would be able to provide this current, hence a simple CMOS inverter architecture was used, rather than a level-shifted driver as per the 125kHz breadboard.

The tank driver was implemented as a 5V CMOS inverter. This was a compromise between V_{ds} and on-resistance. A higher V_{ds} limit was preferable in case transient detuning caused a brief high voltage to be induced at the tank driver output. The available 20V and 50V FETs had a higher on-resistance and higher gate capacitance for a given transistor size compared with the 5V FETs. Whilst the 1.8V FETs available had an even lower gate capacitance, they would be less likely to withstand high transient V_{ds} and so were less suitable.

An advantage of using a 5V inverter to drive the tank was the ability to re-use the digital supply. This would not lead to significant amounts of noise propagating from the LC tank provided a high Q factor was used to filter out such transients. Furthermore, the majority of high-speed digital circuitry was on the 1.8V supply, not 5V, meaning there would in any case not be significant amounts of digital switching noise on the 5V digital supply.

With a 5V drive (i.e 2.5V RMS) and 100mA maximum RMS tank current, a tank resistance of 25Ω is required. The tank driver therefore had to have significantly less resistance than this, so that the Q could be reliably controlled by means of external resistance.

An inverter chain was created, with the width/length ratio of transistors increasing by a factor of three between each stage, until a sufficiently low output resistance was obtained. A fan-out of approximately 3 provides the best propagation delay of the inverter chain [41]. Figure 5-50 shows the resulting size ratios of the inverter chain created, with the final drive being 729 times larger than the first stage.

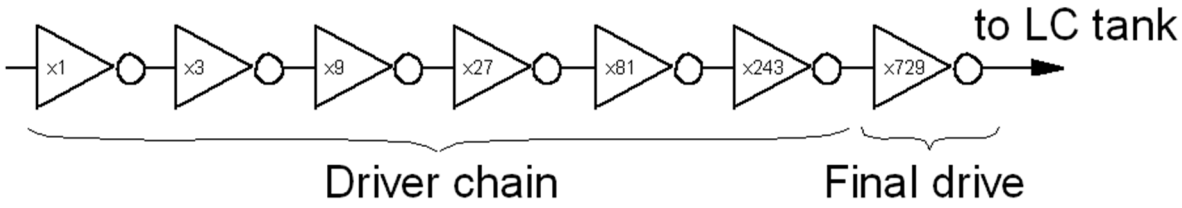

Figure 5-50: Driver chain for tank driver

A further consideration was the current density limits for both the driver FETs and the bondpads used to interface with the IC packaging. The design kit provided bondpads with a 100mA DC current rating which were sufficient to provide the required current. The maximum current density of the final FETs was several times the maximum intended current load, providing a safety margin in case of an accidental short circuit.

The placement of the tank driver was critical in determining its resistance. To minimise the resistance, the shortest path between the tank driver supply and output had to be created. This was possible by placing the bondpads for the tank driver output next to the 5V digital supply, with the tank driver final FETs in between. Figure 5-51 shows the layout used to achieve this. Given the high current density, multiple metal layers were needed to connect the driver FETs with the bondpads to prevent electromigration from degrading the lifetime of the circuit.

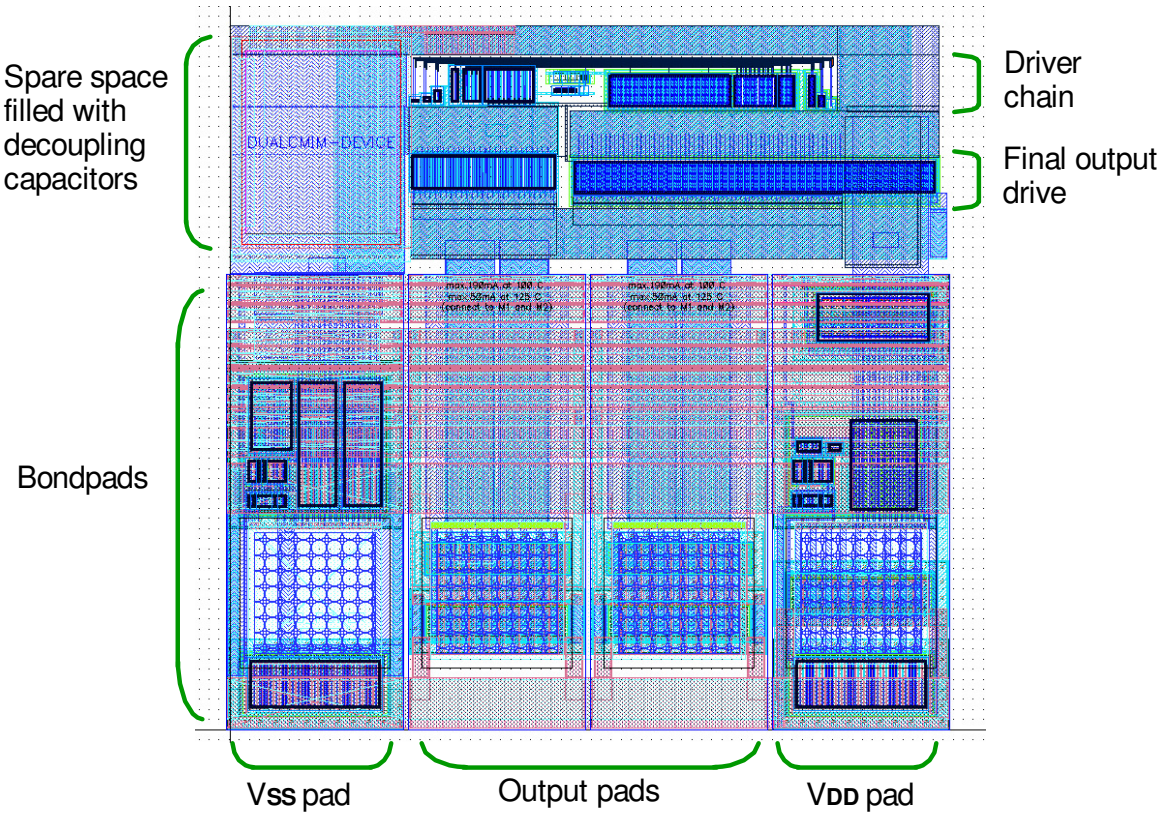

Figure 5-51: Tank driver layout, including bondpads

The extracted layout of the tank driver was simulated at 2MHz with an antenna circuit consisting of a 25Ω resistor, 99.47uH inductor and 63.5pF capacitor to achieve a Q factor of 50. The simulated RMS inductor current was 78.22mA RMS, meaning the combined resistance of the tank driver FETs and bondpads was approximately 7Ω. This was sufficient for achieving large oscillations, but may need to be accounted for during testing. Across PVT corners, the worst measured propagation delay of the tank driver was 3.22ns, below the target 5ns (for 1% phase shift at 2MHz).

5.3.6 Capacitor switches

For the required unipolar switching action on the antenna circuit, an NMOS device was used for the positive excursions of V_C and a PMOS device was used for the negative excursions. These were designed as separate modules to be placed side by side close to the bondpads to minimise added resistance to the LC tank.

For the NMOS switch, design was relatively straightforward. Of the available devices, a 25V-rated isolated mid-oxide device "nfeti25m" was selected to be the switch. This was because its on-resistance was approximately half of that for the 50V device of equivalent active area, meaning it would contribute less to the Q factor of the LC tank. It also had a threshold voltage of 0.66V meaning it could be driven with a 5V logic level, which conveniently meant that the driver chain for the tank driver could be reused to save layout time.

The PMOS switch design required greater consideration, since the V_{gs} had to be relative to the high-voltage supply rail. The 20V high-voltage symmetrical FETs ("pfet20hs") was chosen for the switch, as this had a 20V rating for both V_{ds} and V_{gs}, meaning it would be compatible with a 20V logic level drive. This meant that the high-voltage supply was limited to 20V, which in turn limits the V_c peak-peak voltage to 40V.

In order to create a level shift from the internal 1.8V logic, the pfet20hs and nfeti25m devices were used as per the circuit in figure 5-52. A direct conversion between the two power domains was possible due

to the 0.66V threshold voltage of the nfeti25m device. The driver chain for the PMOS switch comprised of pfet20hs and 50V symmetrical NMOS devices ("nfet50hs"), both of which could withstand a 20V gate voltage.

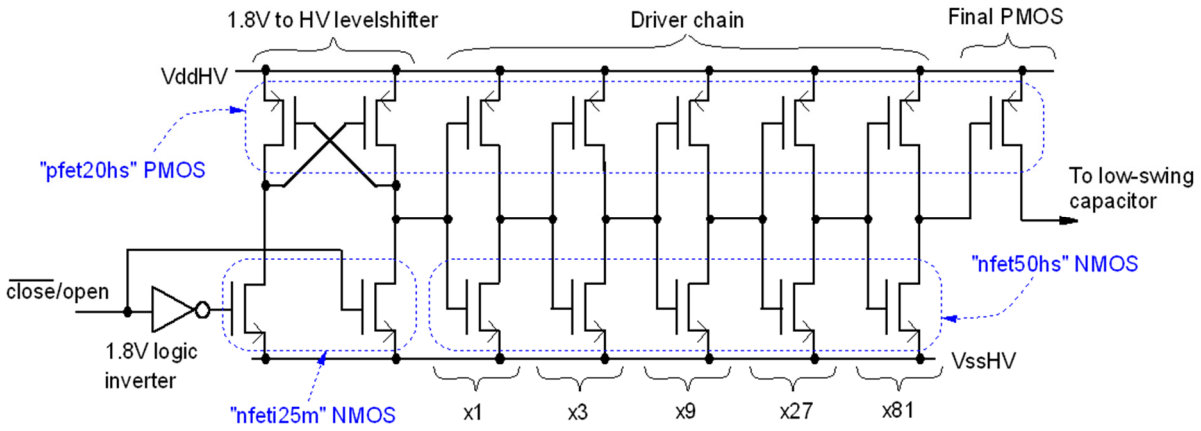

Figure 5-52: PMOS capacitor switch driver chain and logic level shifter

In order to minimise the added series resistance to the LC tank, the final FETs for both unipolar switches were merged into the high-voltage bondpads. Figure 5-53 shows the layout of the capacitor switches and bondpads. The unipolar switches were sized so that no more than two bondpads would be required for each switch, preventing excessive area usage.

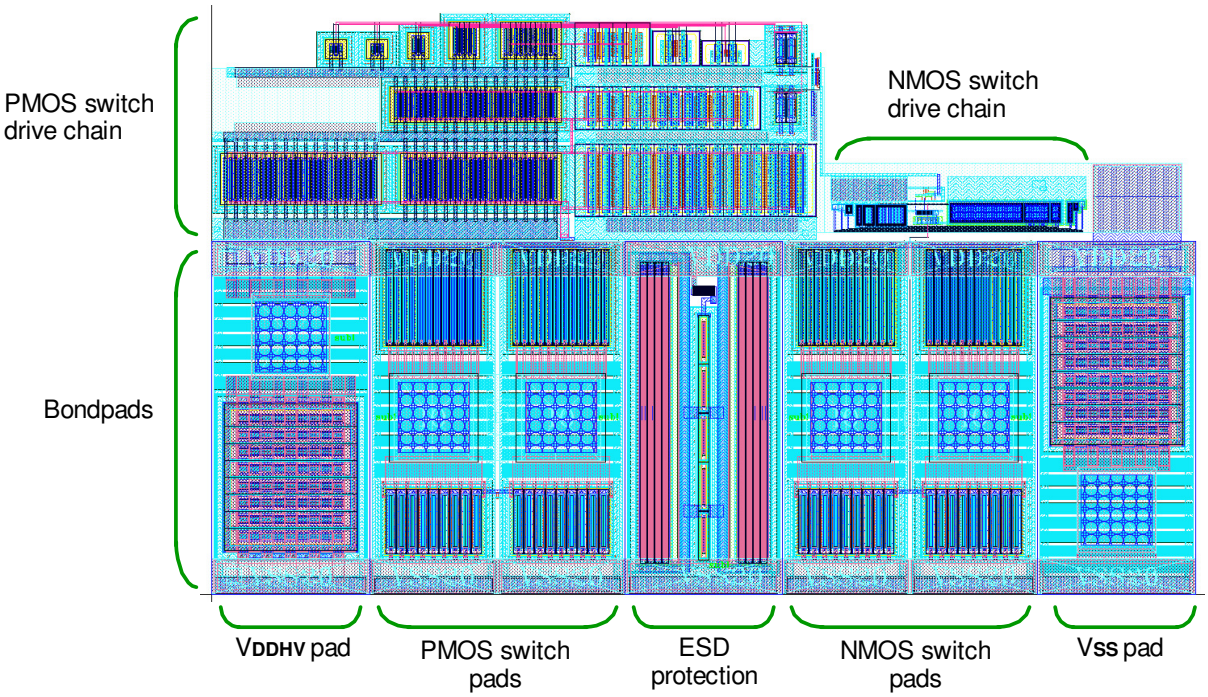

Figure 5-53: Capacitor switch and bondpad layout

The capacitor switches were simulated together with the tank driver in a typical test load circuit as per figure 5-54. The intention was to test for both high current through the switches and high voltage excursions across them, hence the tank was configured to have a Q factor of 50, using an 18Ω resistor and tank driver 7Ω to provide the correct resistance. A capacitive divider to reduce the switch voltage, as is shown to be possible in section 4.2.4 Note that a large tune range was not necessary for this simulation, since component values are ideal and can be set as required. The capacitive divider was

selected such that the maximum tank frequency would be 2MHz, whilst having a divider ratio of 0.16 to reduce the expected 125V peak V_c to the 20V limit of the switches.

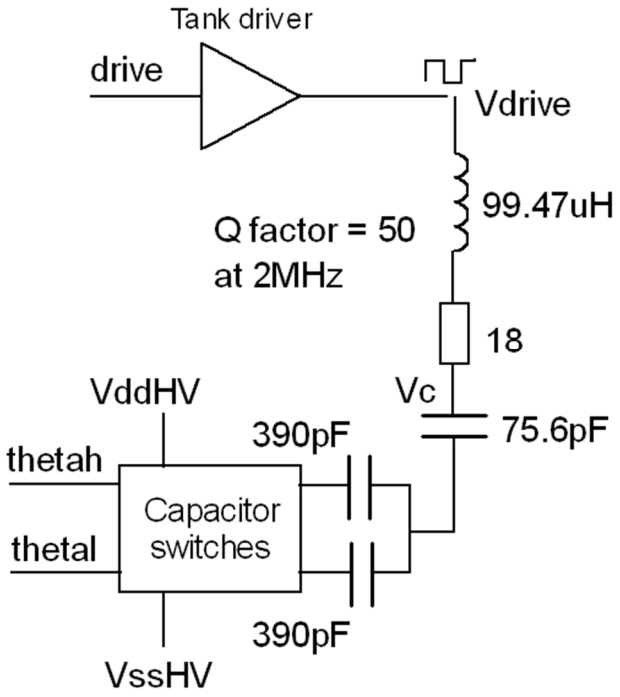

Figure 5-54: 2MHz high current, high voltage simulation test bench circuit for extracted tank driver and capacitor switch blocks

The worst-case propagation delay of the NMOS switch across PVT corners was simulated to be approximately 14.4ns, whilst the PMOS switch worst-case delay was 20.2ns. It was expected that the PMOS switch would be slower due to the use of the high voltage FET driver chain with larger gate capacitances.

Delay blocks were added so that the worst-case delay of the NMOS was increased to 20.4ns, meaning that the unipolar switch timings would be correctly phase aligned with respect to one another. Although 20ns is much higher than the target 5ns propagation at maximum frequency, it would be possible to compensate for this by phase trimming. In order to correctly achieve resonance, phase trimming was found to be necessary in the 2MHz test simulation. Figure 5-55 shows the tank being driven at this frequency. It can be seen that the amplitude of V_c is approximately 150V, but the amplitude of the switch voltages does not exceed 20V.

In order to quantify the simulated switch on-resistances, the voltage difference between the switch and supply voltages were observed during the conducting phase of operation. By this method, it was found that the NMOS switch had 7.3Ω resistance, whilst the PMOS had 5.5Ω. These are both comparable with that of the tank driver, and may need to be considered when choosing tank resistance.

The parasitic capacitance of the HV switches was also extracted from time-domain simulation. When a switch is open, the parasitic capacitances associated with it can be lumped as a fixed capacitance to ground at AC. This creates a capacitive division, making the V_{SW} excursion smaller than the V_C amplitude. Simulation of the extracted layout of the capacitor switches was done at 125kHz, with 50pF antenna capacitors and 21mH of inductance, with a Q of 50. The division on the $V_{SWP/N}$ excursions was equivalent to 7.3pF and 6.79pF on the NMOS and PMOS devices respectively. An ideal switch would have zero capacitance and any additional capacitance will create a reduction in the tuning range. In practice the antenna circuit should use tuning capacitors significantly greater than these values (i.e. at least 10x larger) so that they make a negligible contribution to the tuning range.

Note that enforcing a minimum value on the tuning capacitor sizes will create a practical limit on the maximum operating frequency that can be used. For a set operating frequency, a larger capacitance will require a smaller inductance to achieve resonance. This smaller inductance may in turn result in a limited Q factor, as the smaller dimensions of the inductor mean that it will have lower resistive losses, hence that the losses of the on-chip driver and HV switches will become the dominant limitation to the Q. For a given switch resistance and parasitic capacitance, there is hence a trade-off between the Q factor, tuning range and operating frequency in a given IC process. For the target operating frequency of around 2MHz, the chosen process and design was sufficient, however a system that operates at a higher frequency may require a more advanced process, with lower switch resistances and/or lower parasitic switch capacitances.

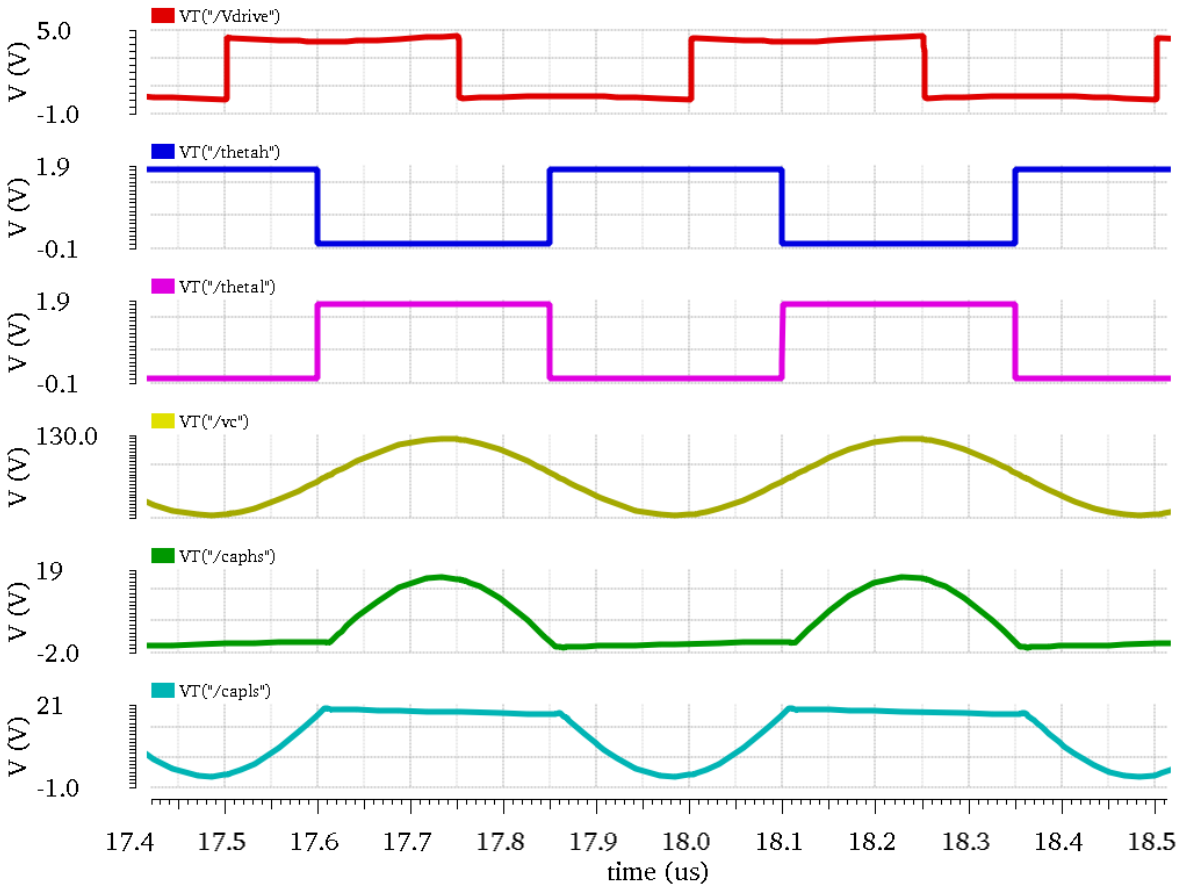

Figure 5-55: Simulation of tank driver and capacitor switch extracted layout at 2MHz

5.3.7 Switch sample

It was already established that the V_{SW} sign sampling circuitry was to operate in the 1.8V and 5V domains for speed, comparing a divided version of the V_{SW} excursion to make this comparison without damaging the comparator FETs. The exact circuitry of the divider still required design. One possible approach was a resistive divider as per figure 5-56. The voltage at the non-inverting input of the comparator is a scaled version of V_{SW}, with a DC offset applied so that the voltage is within the valid input range of the comparator. Note that when the switch is open, the resistive divider will permit continued current flow, meaning that some reduction of the antenna Q factor will occur due to energy being dissipated.

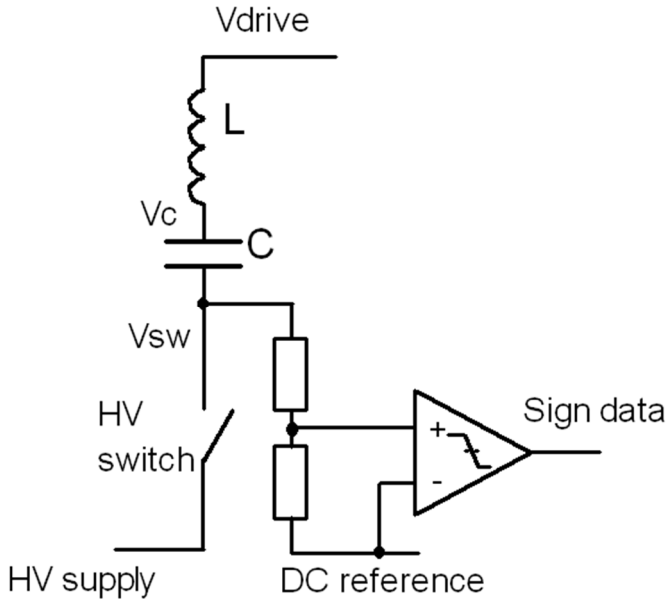

Figure 5-56: Resistive divider for switch voltage sign detection

An alternative solution is instead to use a capacitive divider as per figure 5-57. When the switch is opened, there is no DC path between the antenna tuning capacitor and the supply. Since there are no resistive components there is no significant reduction in Q factor. Provided that the total series capacitance is significantly less than that of the switched tuning capacitor, the circuit's contribution to detuning the antenna will be minimal.

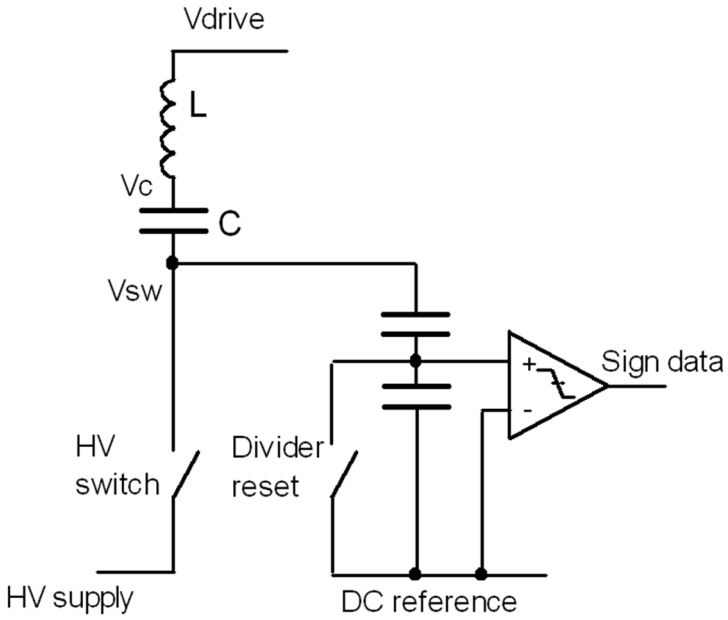

Figure 5-57: Capacitive divider for switch voltage sign detection

The output voltage of the capacitive divider tracks the shape of the switch voltage excursion. If the system is correctly tuned, the excursion will start and end at the same value. However, in the case of detuning, the final output value will be different. Over time this would cause the DC voltage in the capacitor divider to increase or decrease, eventually exceeding the safe operating voltage of the continuous comparator. In practice, leakage currents from local FETs and bondpad ESD devices will also lead to the accumulation of charge on the comparator input node.

To prevent a drift of the DC voltage at the output of the capacitive divider, it requires periodic resetting to a known voltage. By using two capacitive dividers, one for each antenna tuning switch, the circuit may be reset during the time that the respective high-voltage switch is closed. When the switch is opened, the capacitive divider is allowed to track the switch voltage. The comparator can then compare the switch voltage with the fixed 2.5V reference, leading to the architecture in figure 5-58.

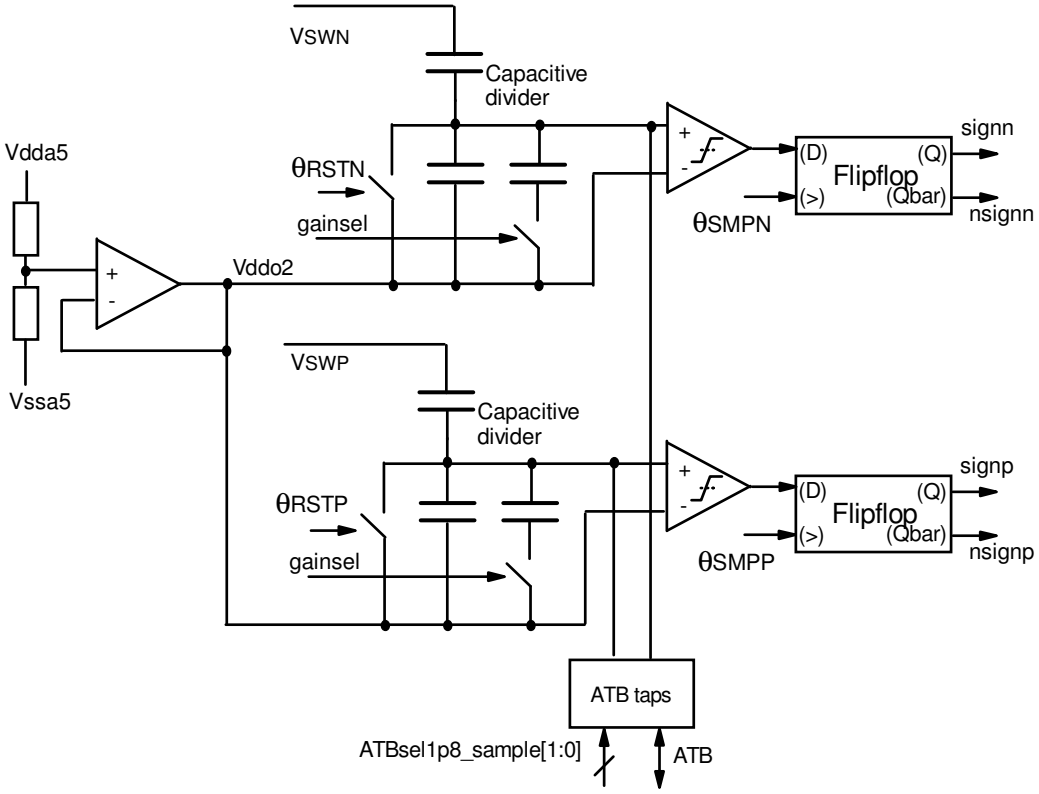

Figure 5-58: Switch sampler architecture

In order to sample the sign of the V_{SW}, a D-type flip-flop was connected to the output of the continuous comparator. This approach permitted re-use of the previously designed comparator circuit, reducing development time.

The input capacitor of each divider would be required to withstand the highest voltage, which given the 20V unipolar switch limit would be no more than 17.5V. From the available library, a 50V-rated vertical natural capacitor (VNCAP) was used for this purpose. In order to have the largest voltage drop, this capacitor would also have to be the smallest. A value of 500fF was chosen, as this would dominate the total series capacitance of the divider and ensure that it would not cause significant detuning for external capacitors greater than a few tens of picofarads.

The remaining capacitor size is chosen by the maximum safe voltage of the comparator. The maximum permitted divider output was 2.5V relative to the mid-supply voltage. With a maximum switch excursion voltage of 20V, the divider ratio had to be no greater than 0.125. A fixed capacitance of 6.2pF was chosen to provide a ratio of approximately 0.075, meaning that the maximum divider output voltage should always be within the supply range of the comparator. The larger capacitor of the divider was implemented as a dual metal-insultator-metal (dualmim) device as this had a greater capacitance density than the vncap, reducing area consumption.

To provide some flexibility, optional extra capacitance was added to the divider, increasing the second capacitance to 24.7pF, giving a smaller divider ratio of approximately 0.02. Whilst this should not be necessary, it allows the input voltage to the comparator to be further reduced should damaging it be considered a risk.

The 2.5V reference was generated by means of a potential divider on the supply rail. The resistors used were set to 375kΩ and decoupled with 3pF to form a low-pass filter with a cut-off frequency of approximately 280kHz. This was to remove high-frequency noise from the input of the voltage reference buffer. The DC value of the voltage reference on the capacitive divider did not have to be exactly 2.5V, it merely had to be stable. Hence, the current-steering mirror buffer circuit was reused for this purpose, as it was compact and capable of providing current to quickly reset the capacitive dividers.

The switch sampler block was simulated at 2MHz. Figure 5-59 shows the positive excursions being detected by the switch sampler, whilst figure 5-60 shows detection for the negative excursions. If the final switch voltage (i.e. before the instant it closes) is greater than the supply rail, this is indicated by a logic 1 output of the switch sampler block. Where the final switch voltage is less than the supply rail, a logic 0 output is provided.

Note that the rising edge of the flip-flop clock must occur before the capacitive divider is reset, otherwise valid sign information cannot be captured. This condition is enforced by the timing block, which provides the switch sample clock and reset signals Θ_{SMP} and Θ_{RST}.

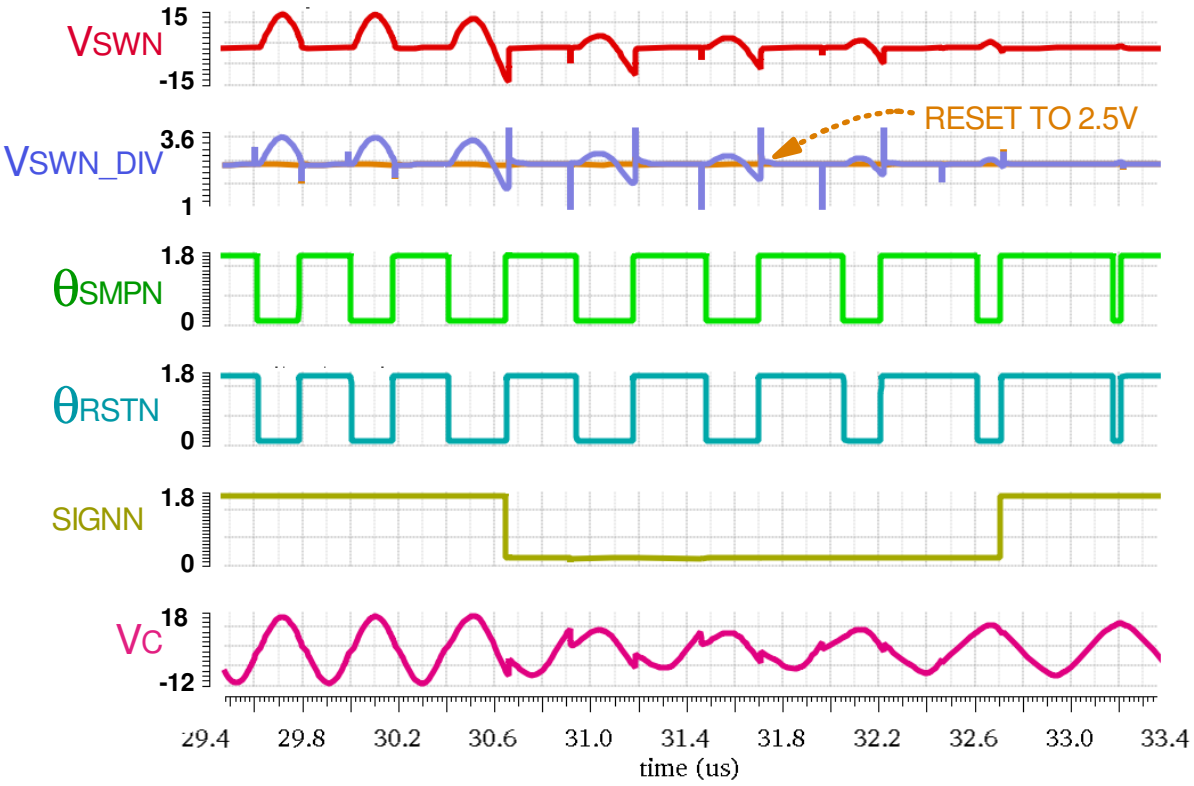

Figure 5-59: Positive switch voltage sign detection in response to 2.58MHz – 1.88MHz operating frequency step

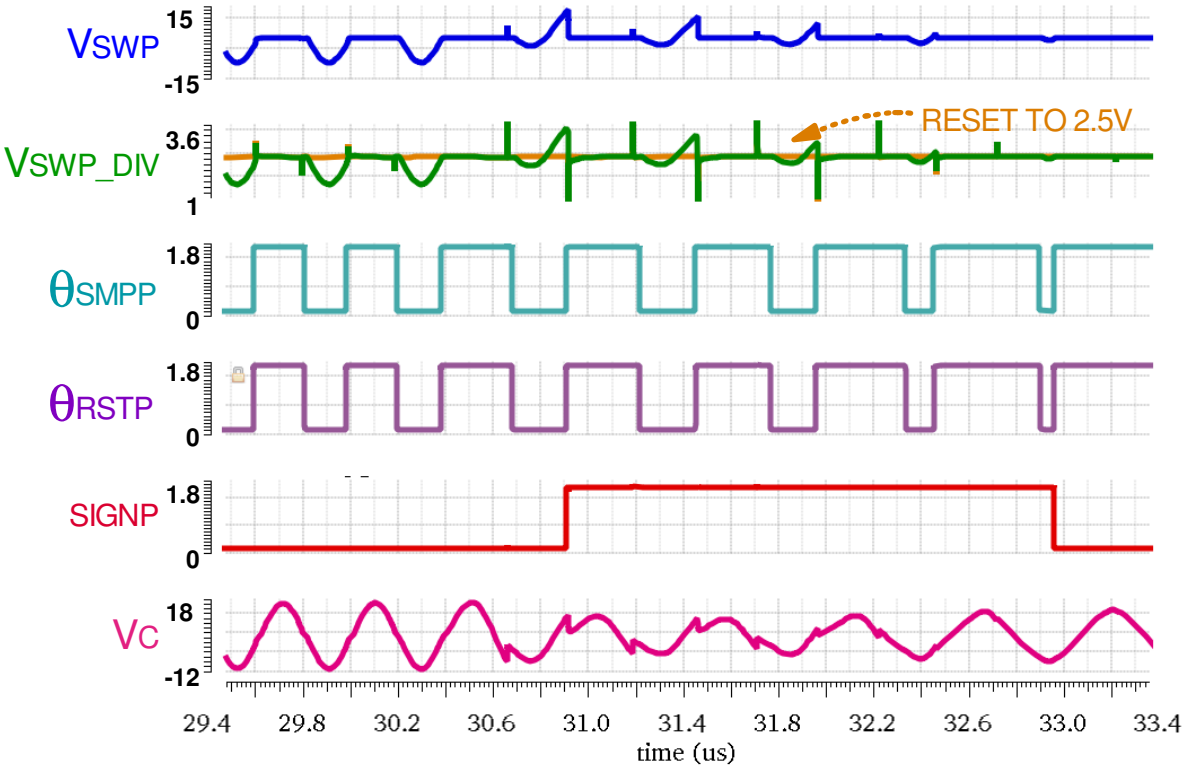

Figure 5-60: Negative excursion switch voltage detection in response to 2.58MHz – 1.88MHz operating frequency step

5.3.8 Digital integrator

As determined in the system architecture comparison, it was preferable to use a digital integrator for the purposes of self-tuning. One of the important features of the digital integrator was to have controllable gain, as this would allow control over the speed of self-tuning. One architecture investigated was that in figure 5-61, where an adder/subtractor determines the next value of the digital integrator.

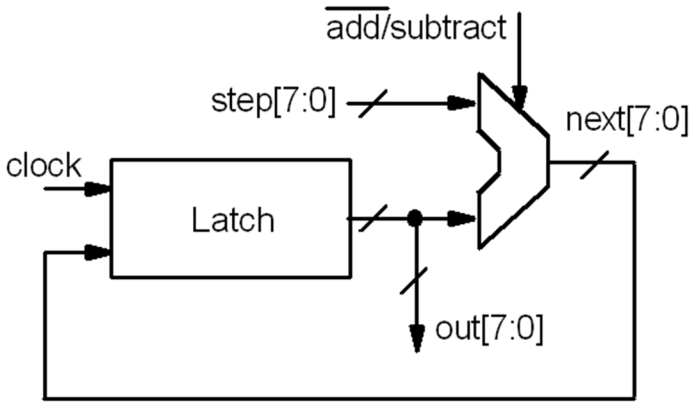

Figure 5-61: Adder/subtractor architecture for a variable-gain digital integrator

In order to change the gain, the value to be added or subtracted from the current value is changed. This approach allows a highly configurable gain, however additional logic is required to prevent overflow from occurring, as this would create instability in the self-tuning control loop.

An alternative approach was to use a counter with a bitshifted output. Shifting the value left or right would only provide gain settings which were multiples of two. It also meant that the tune range would be reduced for a gain of more than 1, since the LSB of the output would be below the LSB of the

counter. However, this meant that for a fixed clock frequency it was possible to have gain settings of less than one very easily. Since it was preferable to have very low gain for a slow control loop, the bit shifting approach was used. Figure 5-62 shows the implementation used, with *int_gain*[2:0] adjusting the position of the window.

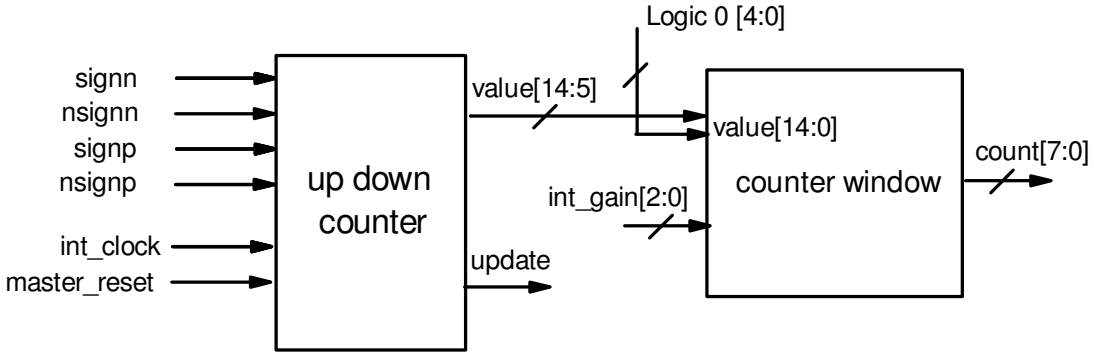

Figure 5-62: integrator gain implementation by output bit-shifting

It was decided that the digital integrator should be clocked twice per cycle, so that it would always have the most recent sign information. Rather than using the HV switch control signals $\Theta_{N/P}$, the integrator clock was derived from the peak and trough of the triangle wave, as described in the triangle generator section. This was to prevent race conditions from occurring due to the varying phase of the integrator clock.

The digital integrator output size was fixed at 8 bits by the resolution of the voltage DACs, but the counter size could be made larger than 8 bits since bit shifting was being used. The maximum gain was decided by the requirement to be able to move across the tune range within 5 cycles at maximum frequency to allow for rapid detuning effects.

With an 8-bit output, i.e. maximum value of 255, steps of at least 25 would be required at each integrator clock event in order to achieve this. A gain of x32 was therefore chosen, since it was the next available power of 2 which could be provided by the counter window bit-shifting function. A gain of x32 would require a 5-bit right shift of the counter value. Figure 5-63 shows that this would reduce the tuneable range by 31, i.e. approximately 12%. This tradeoff between gain and tune range was necessary with the bit-shifting architecture, however the amount of tune range reduction improved at lower gain. For gain settings of x1 and less, there would be no tune range reduction.

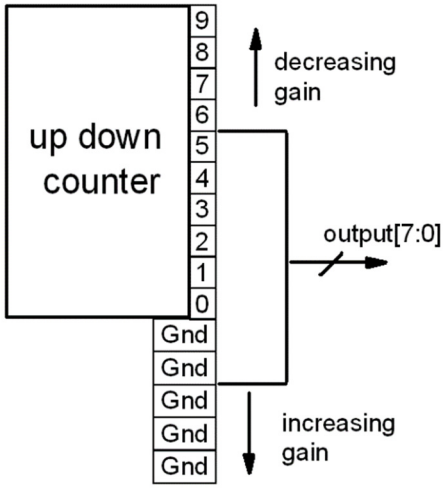

Figure 5-63: Bit-shifting technique permitting a gain of greater than 1

Considering the lowest gain setting, this occurs from a left-shift in the counter value, i.e. ignoring the LSBs of the counter. If 3 bits are used to store the gain setting, then the lowest gain achievable is x0.25, given the highest is already set as x32. A gain of x0.25 means that 512 cycles of operation would be required to sweep across the entire tune range. It would also require the use of a 10-bit counter. The use of an additional bit for gain setting would provide an extremely low gain of approximately x0.0004, meaning approximately 637k cycles would be needed to sweep the tune range. This was deemed to be excessively large, hence 3 bits would be sufficient in order to demonstrate slow self-tuning.

Figure 5-64 shows how multiplexers were used to implement the bit-shifting counter window block. This architecture permitted re-use of the multiplexers provided as part of the 1.8V logic library.

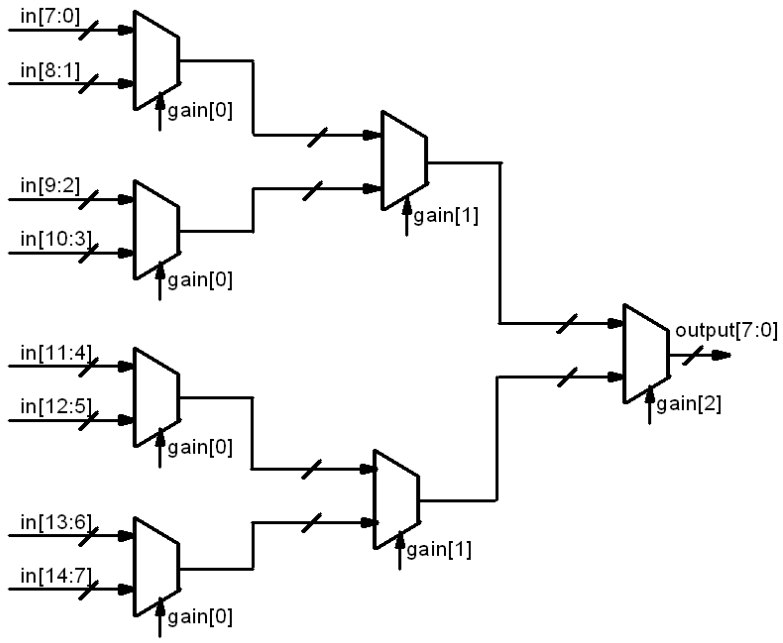

Figure 5-64: Multiplexer architecture for bit-shifting

A fully synchronous up/down counter architecture was used, so that the propagation delay of the counter would be minimised. The counter could therefore be comprised of the uniform blocks in figure 5-65 to permit modular construction, as per figure 5-66. The *signn* / *nsignp* signals are the sampled tuning data from the HV switch voltage sampling circuitry.

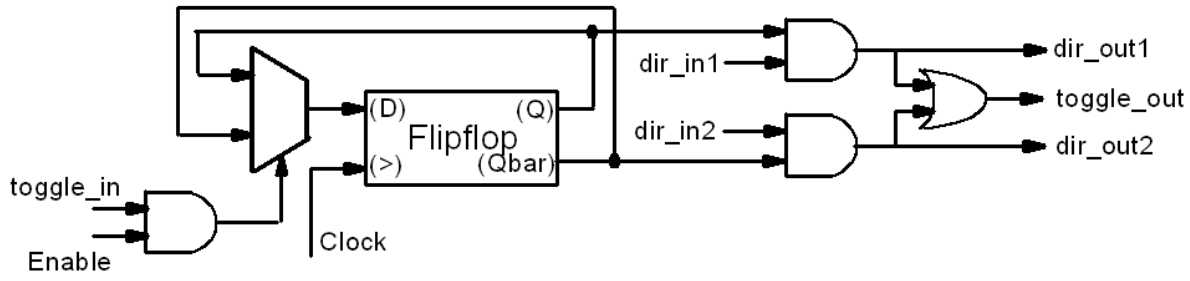

Figure 5-65: Single counter unit

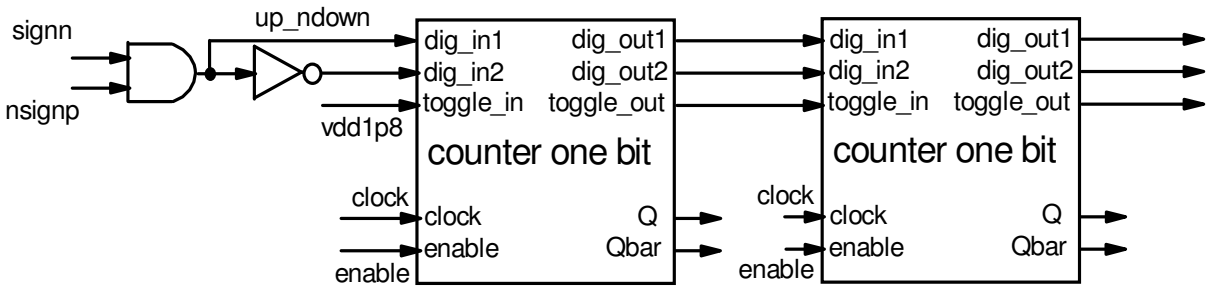

Figure 5-66: Counter chain concept, with count direction logic

The direction of the counter was determined by the information captured by the switch sampler block. If the switch voltage excursion time was too small, the integrator had to count upwards to increase the width of the theta pulses.

Additionally, some logic was needed to determine when the counter should be enabled. The counter should only be enabled when the captured sign information is consistent (i.e. both excursions indicate that the duty cycles of the HV switch control lines $\Theta_{N/P}$ are too wide or too narrow), and the digital integrator is not already at the end of the tune range. Additional logic was included to provide flags to indicated when the counter was at a maximum or minimum value. Furthermore, the *top* and *bottom* detection logic required the unused bits to bit masked, since the unused MSBs were not of concern and hence needed to be disregarded. The truth table 5-4 was used to determine logical equations for direction and enable.

sign_p	sign_n	top	bottom	enable	up_ndown
0	0	0	0	0	0
0	0	0	1	0	0
0	0	1	0	0	0
0	0	1	1	0	0
0	1	0	0	**1**	**1**
0	1	0	1	**1**	**1**
0	1	1	0	0	**1**
0	1	1	1	0	**1**
1	0	0	0	**1**	0
1	0	0	1	0	0
1	0	1	0	**1**	0
1	0	1	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Table 5-4: Digital integrator counter direction and enable flag truth table

Note that the enable control was a useful indicator that the digital integrator would update on the next clock edge, hence it was reused to control the voltage DAC *break-before-make* function previously described.

The extracted layout of the digital integrator was simulated to confirm that both the gain and overlap-prevention logic operated correctly. Figure 5-67 shows operation at minimum gain. The digital integrator counts up from 0 to 255, and then stops correctly. When the sign information is inverted, it counts down back to 0.

Figure 5-68 shows operation at maximum gain. Note that the *signn* / *signp* signals are being manually and independently driven to test all possible input combinations. The counter correctly reaches the maximum value of 224 and stay there until the sign information is completely reversed. When conflicting sign information is presented, the counter remains fixed. The update signal is also operating correctly, and is at logic 1 whenever the counter is changing value.

The worst-case measured propagation delay of the digital integrator across PVT corners was 1.406ns, which was well within the 5ns target and ensured that the latest self-tuning setting would be ready in time for the voltage DAC value update.

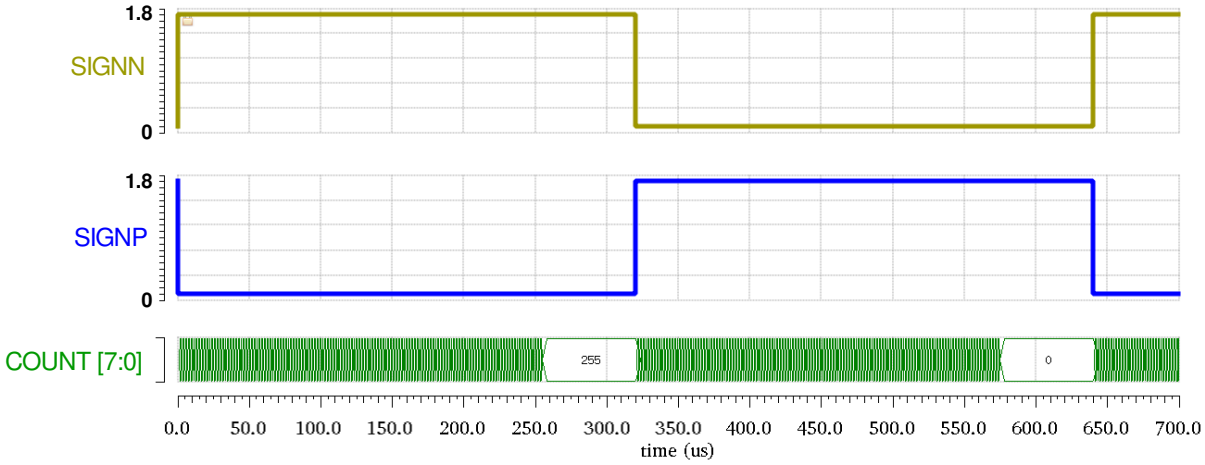

Figure 5-67: Digital integrator operation at minimum gain

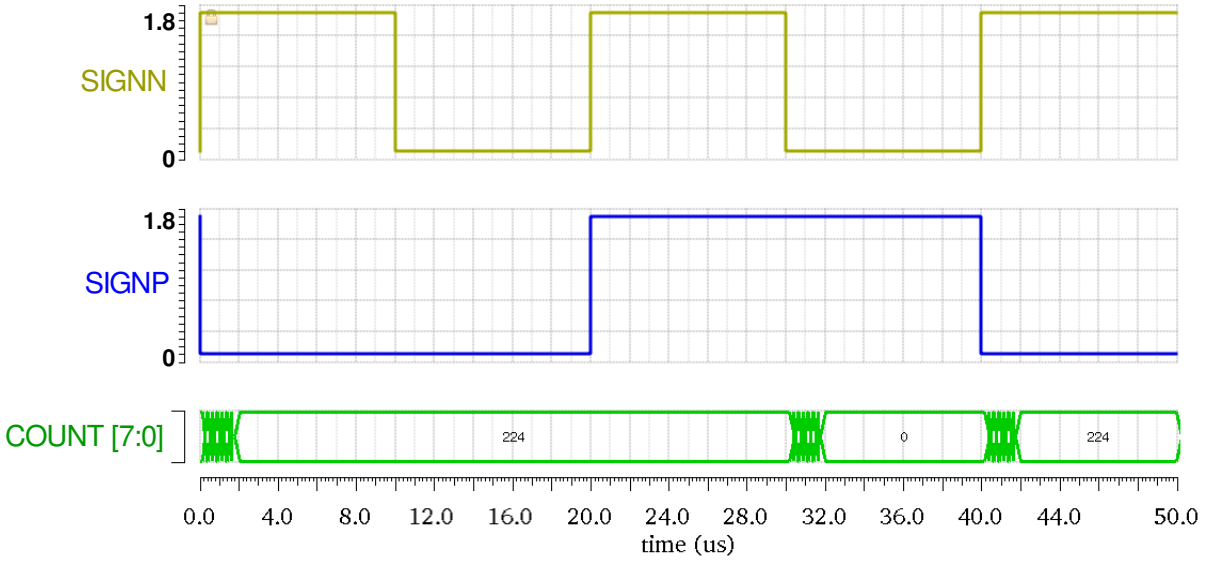

Figure 5-68: Digital integrator operation at maximum gain

5.3.9 Digital Control

The digital control block stores configuration settings and has simple digital functions for the whole system. The block diagram in figure 5-69 shows the signal flow.

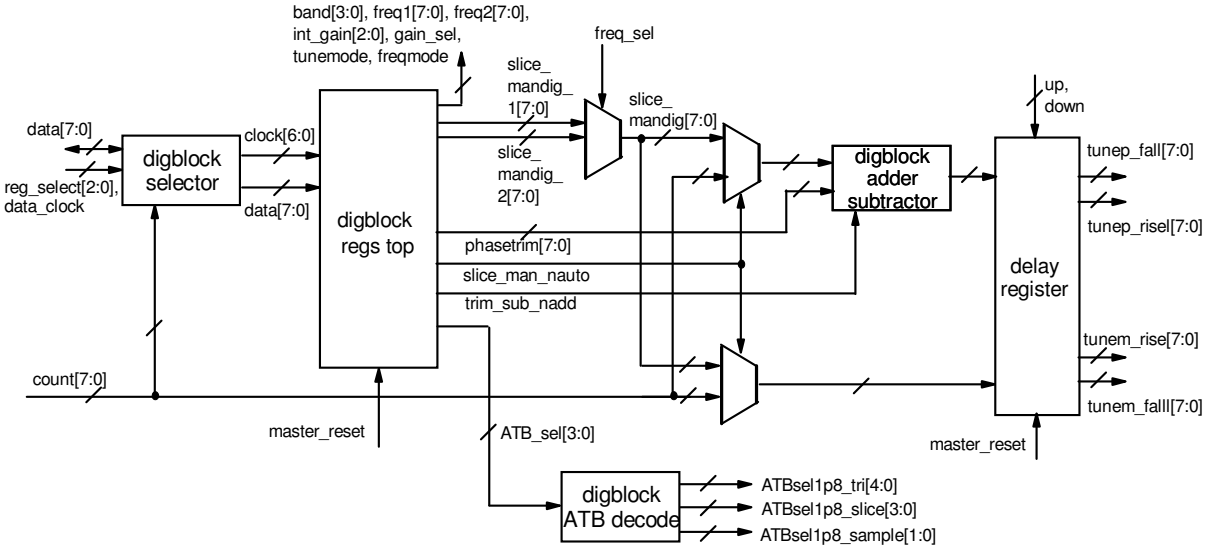

Figure 5-69: Digital control internal block diagram

An 8-bit data bus interfaces with the IC pins. This bus can be used to write to the control registers as well as read the self-tuning integrator's current value.

5.3.9.1 Digital Selector

Setting option	Internal name	Reg_sel [2:0]	R/W?	Notes
Frequency 1	freq1[7:0]	0	W	Used by triangle generator
Frequency 2	freq2[7:0]	1	W	Used by triangle generator
Phase trim	phasetrim[7:0]	2	W	Used by digital control
Slice setting 1	slice_mandig_1[7:0]	3	W	Used by digital control
Slice setting 2	slice_mandig_2[7:0]	4	W	Used by digital control
Config A	configa[7:0]	5	W	General config register
Config B	configb[7:0]	6	W	General config register
Digital Integrator value	count[7:0]	7	R	Output of digital integrator

Table 5-5: List of digital control registers

The selector determines what connections are made depending on the value of *reg_select*[2:0]. If a setting register is selected, the *data_clock* line is connected to the relevant register, so that upon a rising clock edge the value on the *data*[7:0] bus will be loaded into that register. A tristate buffer is used to isolate the digital integrator value *count*[7:0]. Table 5-5 lists the function selected by *reg_sel*[2:0].

Some of the setting register values are connected straight to other blocks. For example, the triangle generator uses *band*[3:0], *freq1*[7:0], *freq2*[7:0], *tunemode* and *freqmode* to determine the mode and frequency of operation. The exact details of digital controls are given in the relevant block description sections.

The digital control block was implemented in 1.8V logic, since a library of devices was provided with the AMS018 design kit for Cadence. The typical propagation delay of logical blocks from this library was sub-1ns, making it more than fast enough for on-line control of the system.

5.3.9.2 Analog Test Bus decoder

The ATB selection is also made within the digital control block, with a 4:16 decoder used to select which node should be connected to the ATB. Test points are located in the triangle generator, slice comparator and switch sampler blocks, as these were deemed to be of most interest for the purposes of debugging. The exact test points and the reasons for test point selection are described in more detail within the corresponding block descriptions.

5.3.9.3 Slice setting and phase trimming

The remaining settings are used within the digital control block, primarily for the purpose of adjusting the triangle tune settings. For each frequency setting, there is a tune setting available. This allows two frequencies to be pre-programmed with independent tune settings. A multiplexer is used to select the correct tune setting for a given value of *freq_sel*.

Note that the tune setting is not connected directly to the output of the digital control block. Additional logic is required to implement the phase trimming function, i.e. creating an offset between the tank drive and the switch action. In order to achieve phase trimming by V_{TUNE} level adjustment, a full adder block was used to create an offset version of the tune level digital setting. If no phase trimming is required, the full adder adds zero to the pre-programmed slice setting. Otherwise, the value stored in *phasetrim*[7:0] is added or subtracted from the selected slice value, depending on the value of *trim_sub_nadd* which is stored in the configuration registers.

Once the slice levels have been created, they are then loaded into the voltage DAC block, but not immediately. The slice settings for the rising edge of the triangle are loaded into the DAC at the beginning of the falling edge, and vice versa for the falling edge settings. Figure 5-70 shows how the update of the slice settings is staggered.

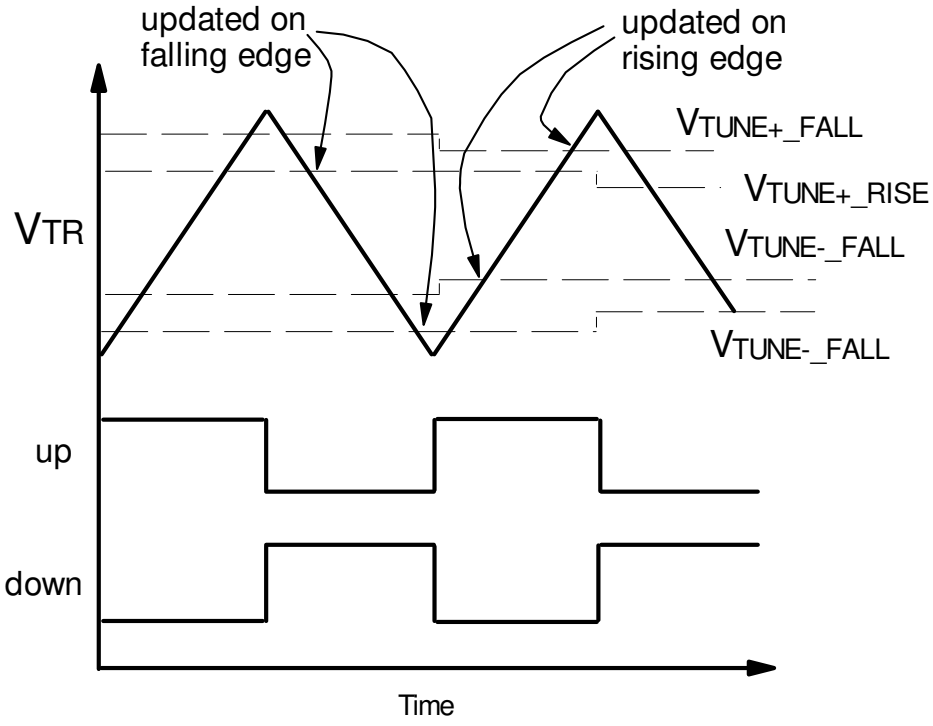

Figure 5-70: Staggered update of slice levels

The slice settings were updated on different edges to permit both the voltage DAC enough time to settle without adversely affecting the switching action. Otherwise, the DAC output may still be settling at the moment when a comparison needs to be made, meaning the switch state may glitch and cause detuning.

Staggering the slice level update in this manner meant that the DAC would always have at least one half of a cycle to update, i.e. 250ns at maximum frequency.

The up and down signals were readily available from the triangle generator, meaning that they could be used as clock signals for a delay register to implement the staggered loading of the slice levels into the voltage DAC.

5.4 Top level system simulation

This section shows simulation results of the complete IC architecture. Due to limitations in available compute power, simulation of the full schematic or extracted layout was not feasible, so simulation was undertaken with behavioural blocks. Additionally, simulation was done with one or two schematic level blocks at the top level to ensure that they functioned correctly, in case of race conditions between logic signals or analogue impedance problems preventing correct operation.

5.4.1 Analogue tune sweep

Figure 5-71 shows the tank voltage V_C along with the triangle wave and slice levels. This tune setting is achieved from manual setting of the slice levels externally, swept to find the optimal tune setting. For this test bench, a low-Q tank was used to make sure that V_C would remain within the safe limits of the HV switches without any attentuator: L = 80uH, R_{tank} = 250, C_N = C_P = 35pF, resulting in a Q factor of around 5 at the operating frequency of 2.57MHz. Figure 5-72 shows the effect of sweeping the slicing voltages from the peak and trough to the centre of the triangle. When off-tune, the amplitude of V_C is reduced as expected.

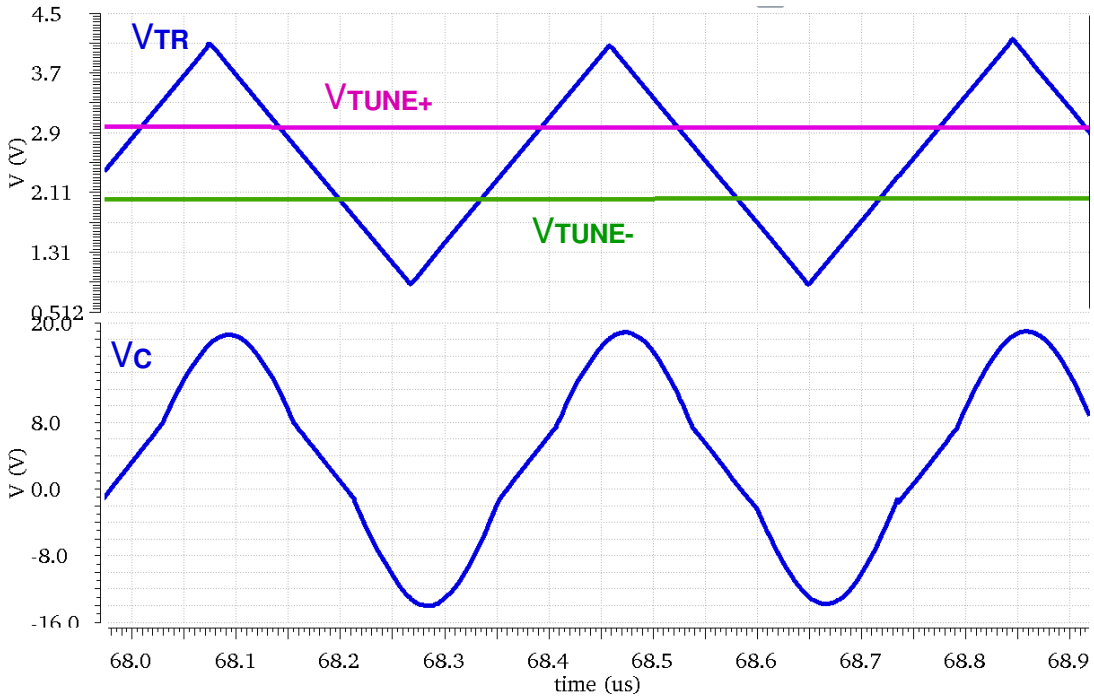

Figure 5-71: Switched capacitor tuning in operation at 2.57MHz

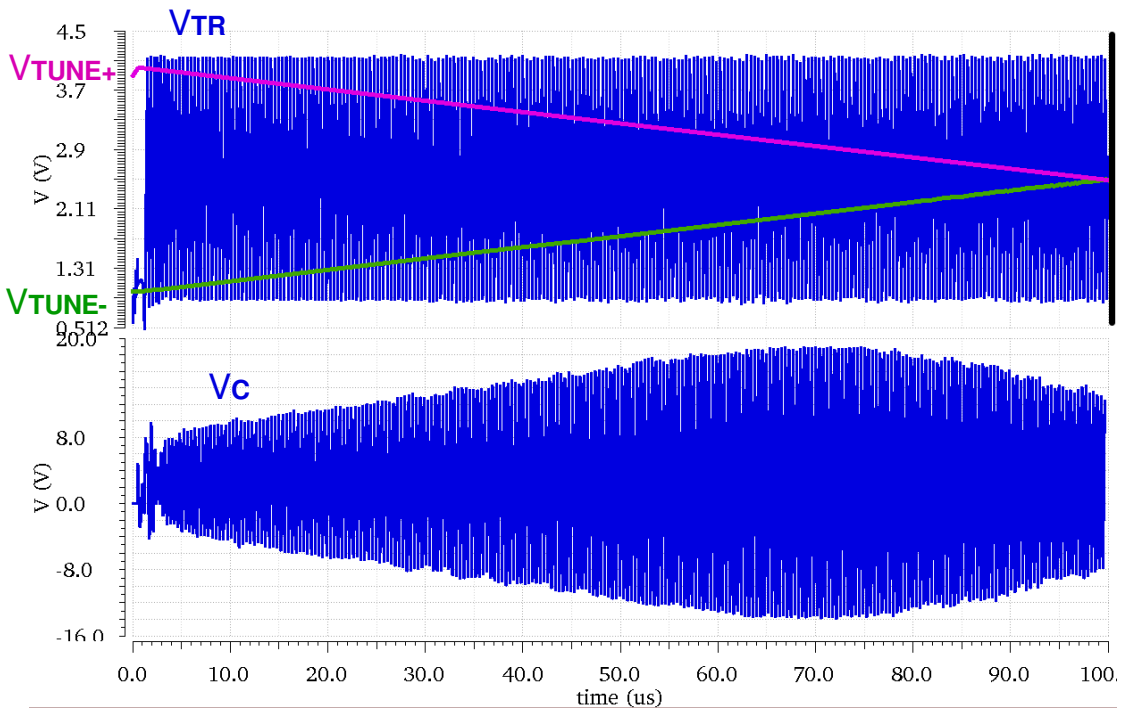

Figure 5-72: Switched capacitor tune sweep at 2.57MHz

5.4.2 Digital fixed tuning with pre-programmed resonant frequencies

Figure 5-73 shows a different test bench, where two digital slice and frequency settings have been pre-programmed in. The LC antenna circuit has been adjusted to show correct tuning at both frequencies ($C_N = C_P = 48pF$). For the first 4.5µs, the settings are being loaded into the digital controller's registers. Once this is complete, and digital tuning is enabled, the system is set up for operation at 2.57MHz. The excursions of the signal V_{SWN} represent the voltage across C_N. At 15µs, the frequency is dropped to 1.86MHz. The digital slice settings are adjusted at the same time, meaning the LC tank moves from one resonant frequency to the other with minimal perturbation of V_C.

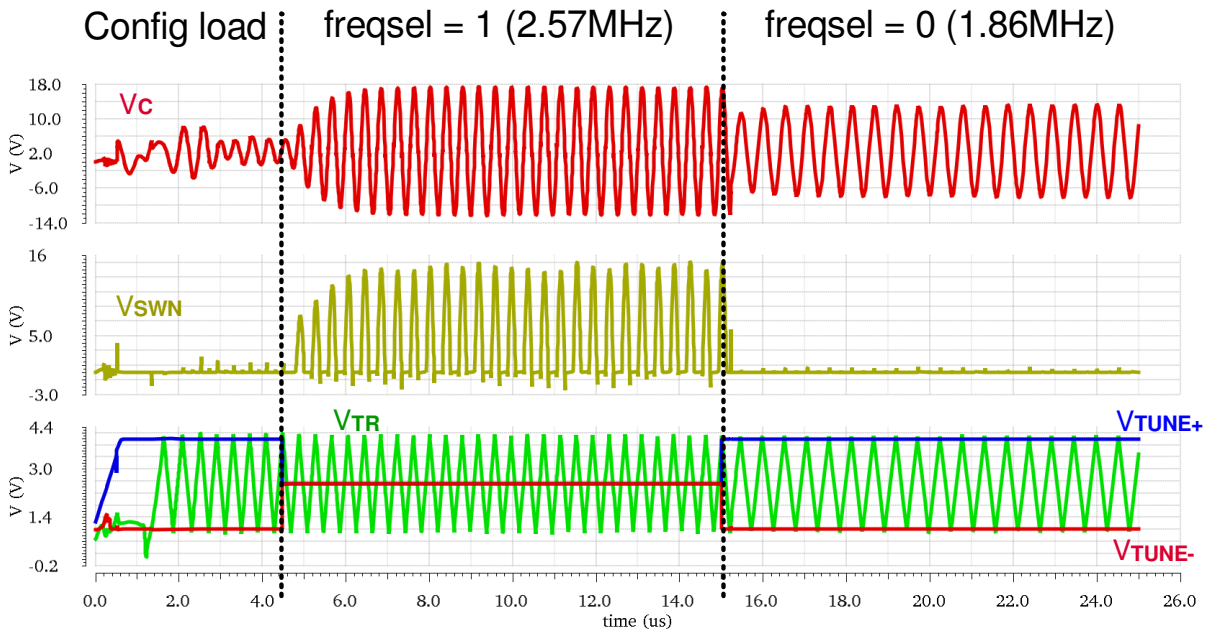

Figure 5-73: Digital fixed tuning in operation, stepping between 2.57MHz (4.5µs- 15µs) and 1.86MHz (15µs onwards)

5.4.3 Digital automatic tuning with frequency modulation

Use of the self-tuning functionality is shown in figure 5-74. Until 10.75µs, the system is operating at 1.86MHz. The operating frequency is then increased to 2.57MHz. Initially, the antenna is still configured for resonance at 1.86MHz, hence the excursions of the capacitor switch voltage V_{SWN} do not return to the supply rail potential before the switch closure. This is detected by the switch sample block, and the digital integrator begins to increase the time period for which the switch is open, increasing the resonant frequency. Eventually, the slice voltages reach the centre of the triangle and stop there, having reached the best possible tune condition for the drive frequency.

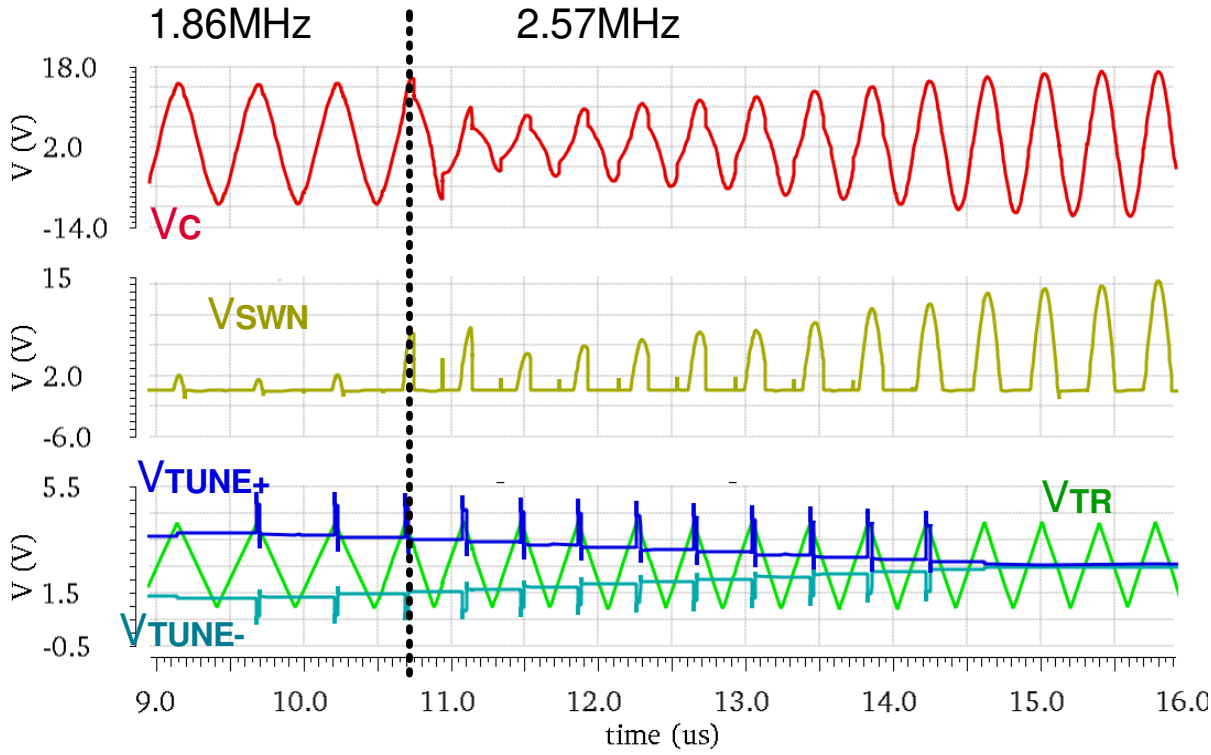

Figure 5-74: Digital auto-tuning in operation, showing system retune after stepping from 1.88MHz to 2.57MHz

5.5 Summary of "lctune018" design

An integrated circuit was designed to implement the zero-voltage switched fractional capacitance tuning method. A suitable IC process was chosen and used to create a mixed-signal architecture, compromising between the advantages of high-precision analogue timing generation and convenient digital control of the antenna tuning.

The entire core system functionality was integrated on chip including timing control, resonance detection and tuning, antenna drivers and HV tuning switches. The system architecture was evolved from the practical implementation issues which were raised from the breadboard construction. Manual phase trimming was included as an option to allow timing delays to be cancelled out at the highest operating frequency range.

The core functions were distilled into IC level blocks which could be designed and simulated independently to help verify the design. Behavioural versions of these blocks were created to help speed up top-level simulation.

The circuit was fabricated successfully and the next chapter details the design verification.

6 “lctune018” IC experimental results

The previously-described system design was fabricated into a batch of 40 samples. The variety of functions available was distilled into three main categories:

1) Static tuning tests
2) Transient tuning response
3) Phase trimming tests

A test board was designed with these requirements in mind, the design included in appendix F.

6.1 Static Tuning Tests

Testing of the self-tuning system was initially done in the 125kHz range, as this is a common frequency band for real applications. It is also the lower end of the designed system’s operating frequency range, hence it was expected that the tuning accuracy would not be so adversely affected by timing errors and offsets. An operating Q factor of around 30 was chosen for testing, which was low enough to be easily attainable without specialist construction, whilst being high enough to demonstrate the tuning accuracy of the designed IC. An air-core inductor of 1.34mH was designed for testing, with an approximate resistive loss of 22Ω, hence the target operating Q of 30 was achieved, once combined with the estimated losses of the tank driver and capacitor switches (amounting to approximately 14Ω worst-case in total).

In order to protect the HV capacitor switches from excessive stress, the peak-peak amplitude of the tank oscillation was limited to 40V, hence the switches would be guaranteed to be safe at all points in the tuning range. With an operating Q factor of 30, the drive amplitude was to be limited to around 1.3V. A resistive attenuator comprising of 6.2Ω : 2.2Ω was used, as this reduced the drive voltage to the safe level whilst avoiding too much additional degradation of the Q factor.

Tuning capacitors of 680pF were used to form the tank circuit for a target operating frequency range of 119.6kHz – 169.2kHz. To protect the IC in case of accidental overvoltage, Schottky rectifier diodes were added to the V_{SW} lines, connecting between ground and V_{DDHV} to clamp any excursions outside the HV supplies. These each had 100-200pF capacitance, creating a large parasitic capacitance to ground. This reduced the tuneable frequency range to around 99-126kHz, i.e. a tuning range of 1.27:1.

Figure 6-1 shows waves recorded at 125.9kHz, near the upper end of the tuning range. Self-tuning is enabled on the lowest gain setting to minimise the steady-state ripple. For the majority of the cycle, one capacitor switch is open, seen from the switch control status outputs θ_{SWN} and θ_{SWP}, with some overlap maintained by the system in order to prevent the condition of both switches being open at the same time. It is also clear that the system is very close to resonance as the rising and falling edges of the tank drive V_{DR} are closely aligned with the peaks and troughs of the capacitor voltage V_C. The switch voltage excursions V_{SWN} and V_{SWP} track the shape of V_C and terminate close to their respective supply potentials, which indicates that the self-tuning has correctly achieved zero-voltage switching.

Figure 6-2 shows operation near the lower end of the tuning range, where the $V_{SWN/P}$ excursions are much smaller. Nonetheless they correctly terminate at their supply potentials and the edges of V_{DR} align with the peaks and troughs of V_C.

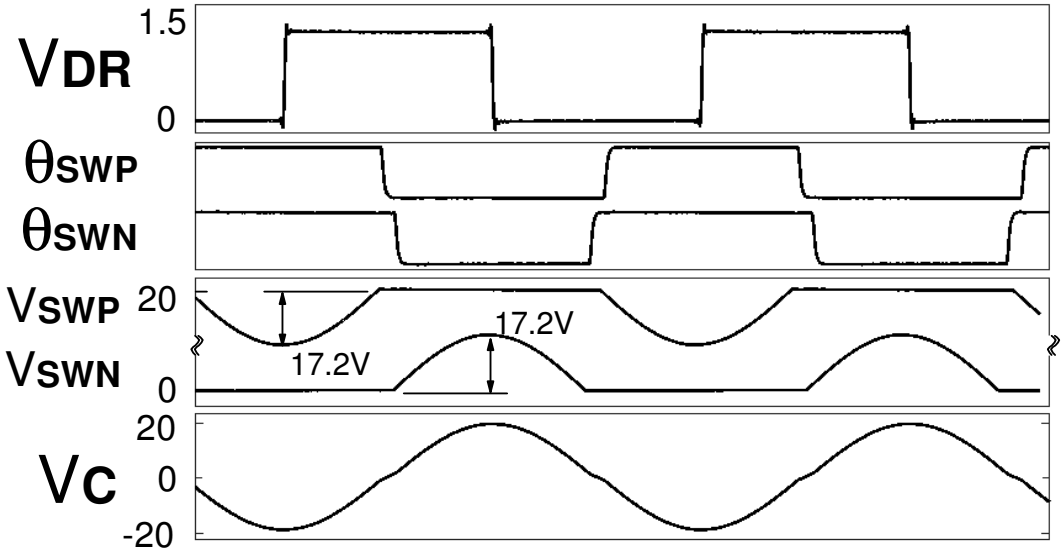

Figure 6-1: Fixed tuning at 125.9kHz

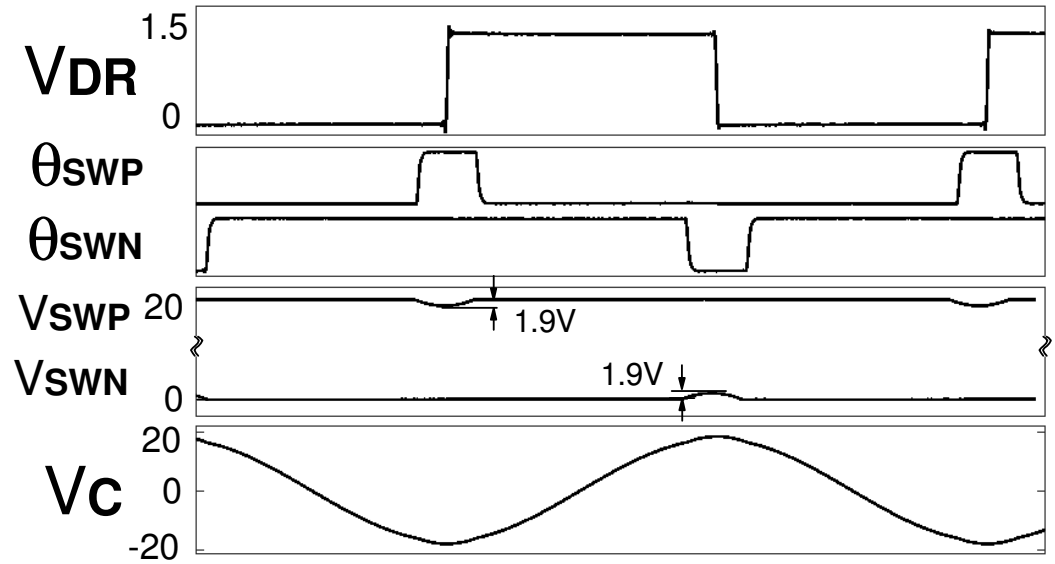

Figure 6-2: Fixed tuning at 99.36kHz

It was expected that the tuning accuracy would reduce as the operating frequency was increased, hence operation of the self-tuning was tested up to the maximum running frequency, approximately 2.6MHz. For this region, a smaller inductor was created (around 31μH with around 3Ω loss). For resonance at 2.6MHz, a capacitance of 120pF was required, hence the switched capacitors would ideally be in the range of 80-100pF. This was comparable with the protection diode capacitance; hence they were removed so they would no longer contribute to the antenna capacitance.

The parasitic C_{DS} of the HV switches (simulated to be around 7pF when open) was still present, expected to create a slight attenuation of the HV excursions but not otherwise contribute to the tuning range. It was found however that switched capacitors of 33pF were needed for operation in the 2.6MHz region, indicating a much larger parasitic capacitance than expected. With the 33pF capacitors used, it was also found that the capacitive division effect was much greater than expected (with the 7pF parasitic, a ratio of 0.825 was expected, however excursions of approximately 40V were being divided to 18V peak, giving a ratio of 0.45). Re-calculating the parasitic capacitance revealed that it was approximately 40pF, which when combined with the 33pF tuning capacitors in series created a fixed parasitic of 18pF to ground when the switch is open, reducing the tuning range and operating frequency.

In light of the extra capacitive division, the resistive attenuator was removed in order to increase the amplitude of the excursions, so that they were comparable with the tests done in the 125kHz region, whilst also maintaining the operating Q of approximately 30. The resulting amplitude of V_C is around 160V peak-peak. Note also that the excursions track the shape of V_C, however the change in the shape of V_C is less pronounced due to the reduced tuning range (from the comparatively large parasitics to ground) and the voltage division between the switched tuning capacitors and HV switch drain parasitics.

Figure 6-3 shows operation at around 2.61MHz with self-tuning enabled. The system is close to resonance as per the figures for 125kHz region operation, however the mid-point of the V_{DR} rising and falling edges is noticeably further from the peaks and troughs of V_C, which implies that the tuning error is greater. Driving the antenna directly creates dipping in the 0V/5V levels, caused by the sinusoidal current flowing through the driver resistance. Note that the $\theta_{SWN/P}$ signals are not shown, as their drivers were not strong enough to correctly reproduce the switching controls as present inside the IC at this frequency.

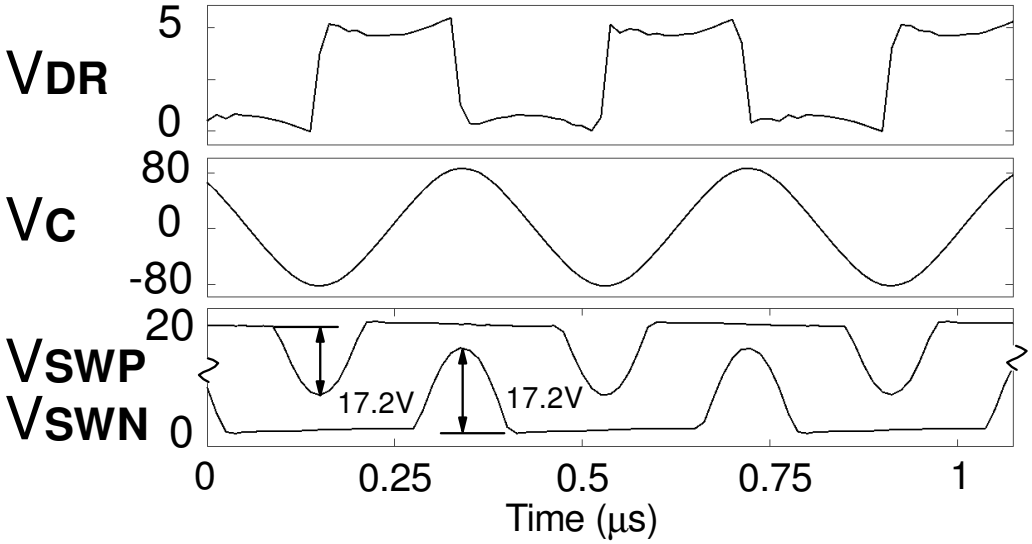

Figure 6-3: Fixed tuning at 2.61MHz

The tuning accuracy of the system across the tuning range was measured from a batch of 10 samples, done by measuring the phase error between V_{DR} and V_C with self-tuning enabled. Measurements were taken for the 110kHz, 1.3MHz and 2.6MHz regions. Table 6-1 shows a comparison of the results with an idealised tuning system using transmission gate switches. The comparison is in two parts, firstly the number of switches required to achieve an equivalent tuning accuracy to the constructed system. Secondly, the performance of system that can tune to within the 3dB bandwidth.

As the operating frequency increases, the tuning accuracy degrades. This is caused by an increased phase offset between the tank driver and HV capacitor switching action, since the relative offset between the propagation delays of these two system modules becomes larger.

The number of required switches was determined by simulating the equivalent frequency offset caused by the measured phase errors, and calculating the number of tuning capacitors needed using equation 3.22. Achieving an equivalent tuning accuracy in all three bands requires a considerably larger number of capacitors, IC package pins and increased die area consumption. The switched capacitor method still represents a saving even if the accuracy specification is relaxed to within 3dB at a Q factor of 30.

The required area for the HV switches in the equivalent system was estimated based on the size of the switches used for the constructed fractional capacitance system. Assuming that each transmission gate in the binary-weighted system has the same average resistance as one switch of the fabricated system, the approximate active area per switch is 680µm^2, hence the total active area can be found by

multiplying this by the number of capacitors needed to achieve the desired tuning accuracy. The other area use is calculated based on the drive chain sizes, assuming that identical drive chains are used for the weighted capacitor switches.

	Constructed system			Binary-weighted tuning			
	Average 10 samples			Equivalent accuracy			3dB bandwidth
Frequency range	110kHz	1.3MHz	2.6MHz	110kHz	1.3MHz	2.6MHz	Any
Tuning accuracy	0.97^{O}	2.26^{O}	11.3^{O}	$> 1^{O}$	$> 2.5^{O}$	$> 11^{O}$	$> 45^{O}$
Switches / package pins for tuning	2			11	10	7	5
R (PMOS)	4.89			10.6			
R (NMOS)	5.80			10.6			
HV switch area (μm^2)	1360			3740	3400	2380	1700
Other area (mm^2)	0.246			1.35	1.10	0.859	0.615

Table 6-1: Tuning accuracy comparison of the constructed system (Q = 30)

Another comparison which may be drawn is the system power consumption, i.e. the power overhead required for operation minus the power consumed by tank drivers. With no load connected, the power consumption of the fabricated system is approximately 79mW. Whilst this is dependent upon the particular internal circuitry used to achieve the system functionality, it can still be compared with real commercial products in order to give an impression of the current state-of-the-art. Table 6-2 shows this comparison of this system with recent commercial ICs for WPC. Integrated data modulators are common, however a method of tuning of the external LC circuit is not typically provided.

	Constructed system	Melexis MLX90109 [42]	M. Dudde BG744CI [43]	EM. Micro EM4095 [44]
Power Overhead (mW)	79	9	67.5	25
Self-tune functionality	Yes	No	No	No
Data modulation	No	Yes	Yes	Yes

Table 6-2: Idle power consumption comparison with commercial products

6.2 Transient Tuning Response

The transient tuning behaviour of the constructed system was also measured to investigate the trade-off between settling time and steady-state ripple. To observe the settling time and response to instantaneous detuning, a wide step change in frequency was used. Figure 6-4 shows the response of the system to a step increase from 100kHz to 130kHz, using an inductor of 1.3mH and Q = 30. The integrator gain is set to x8 in this scenario. Initially the system is resonant and stable at 100kHz, quickly becoming detuned after the increase in operating frequency. The θ_{SW} signals can be seen to increase in duty cycle until resonance is restored, denoted by V_C returning to approximately the same amplitude as before the change in frequency. The close-up of V_{SWN} demonstrates the effect on the tuning as the duty cycle of the Θ signals is increased; the earlier excursions do not have time to return to 0V, but the tuning error gets smaller with each cycle until the switch closure is brought close to ideal 0V closure potential.

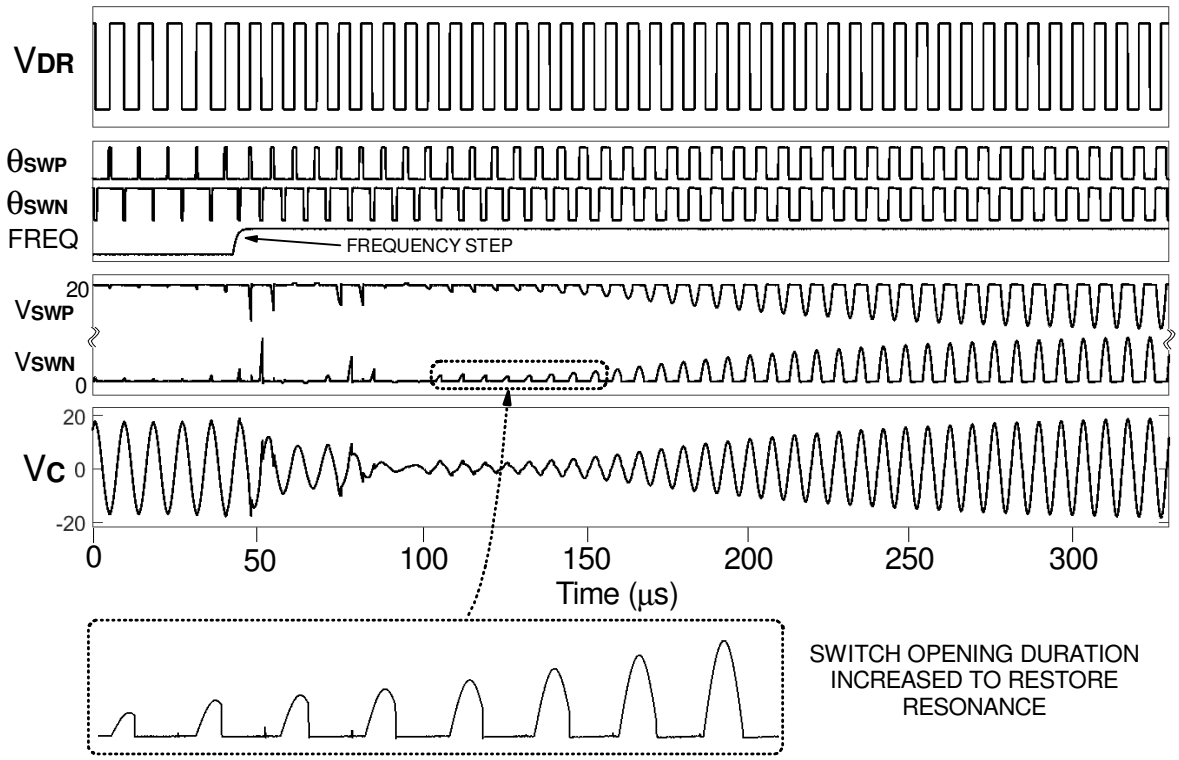

Figure 6-4: Self-tuning response to operating frequency from 100kHz to 130kHz at x8 integrator gain

Figure 6-5 shows the same step in frequency on the same LC antenna circuit, but comparing the response at x1 and x16 gain settings. The V_{TUNE-} tuning setting is shown to aid comparison. As is expected, the lowest integrator gain provides a slow response with almost negligible ripple in V_{TUNE}, whereas the highest gain allows a fast convergence with high ripple in the tuning setting, creating oscillatory detuning and hence ripple in the amplitude of $V_{TUNE.}$ Figure 6-6 compares the self-tuning settling times against the steady-state ripple in V_C for the available integrator gains. As per the early concept simulations, a higher self-tuning gain causes a large continuous ripple in the tuning setting, causing the system to spend significant time oscillating around the true resonant setting. Hence the amplitude of V_C becomes reduced due to this oscillatory detuning behaviour.

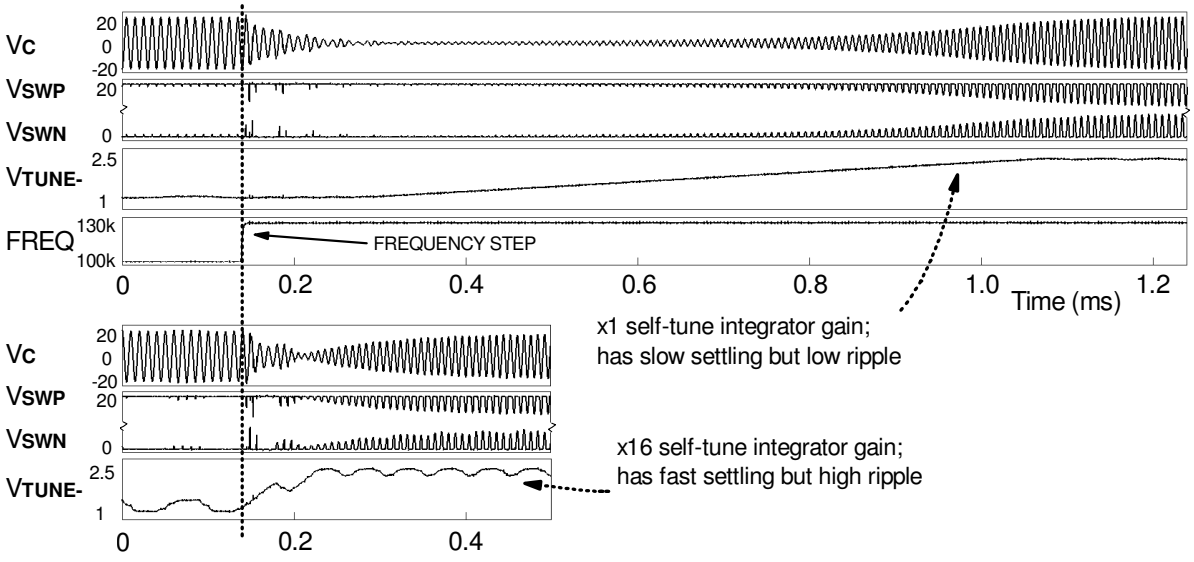

Figure 6-5: Self-tuning response to operating frequency from 100kHz to 130kHz, comparing x1 and x16 integrator gain settings (Q = 30)

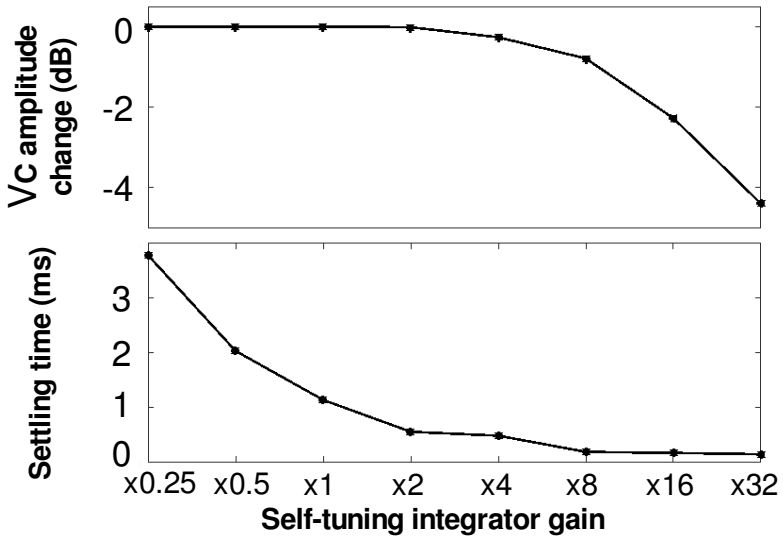

Figure 6-6: V_C amplitude reduction and self-tuning time comparison for different self-tuning gain settings (Q = 30)

In a practical scenario, transient detuning effects are likely to occur at much slower rate compared to the period of oscillation (for example, a human introducing a ferromagnetic material close to the inductor). Hence, a gradual frequency sweep is a useful method of investigating the self-tuning response. Figure 6-7 shows the response to a sweep from 130kHz to 100kHz, over approximately 1.4ms. The upper central figure is the case where self-tuning is disabled, creating a peak in V_C at resonance and reduced amplitude at other frequencies. The lower central figure is the case where self-tuning is enabled, with a roughly constant amplitude of V_C, indicating that the tuning loop is tracking the changing resonant condition in real-time.

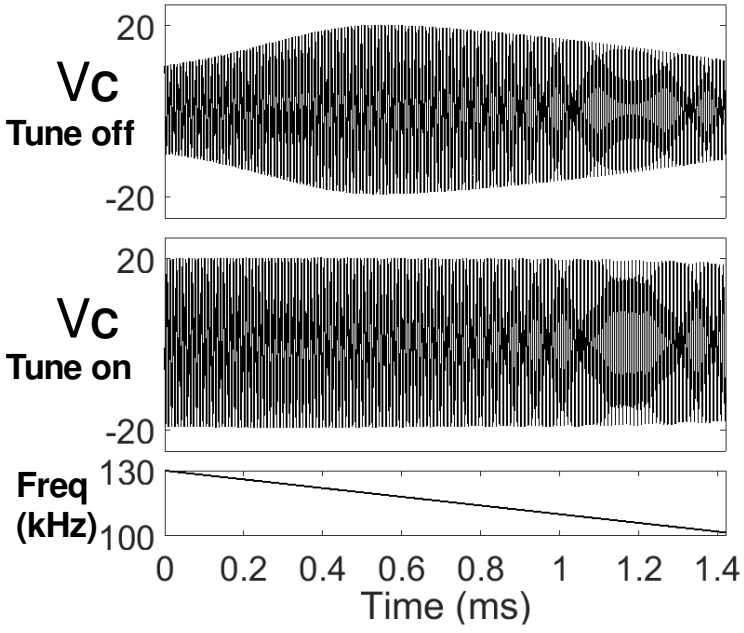

Figure 6-7: Self-tuning response gradual frequency sweep (130-100kHz in 1.4ms, Q = 30)

6.3 Delay Compensation with Phase Trimming

As shown in table 6-1, the self-tuning accuracy deteriorates as the operating frequency is increased. As the operating frequency increases, the delays of the HV switches and driver chains begin to create a considerable timing offset. This violates the ideal symmetrical switching criterion on V_C, creating a

phase offset relative to V_{DR}, hence the system is no longer strictly-speaking resonating even though zero-voltage switching may be possible.

In order to compensate for this error, the phase trimming functionality can be utilised. The phase position of the switching was manually trimmed to compensate for the timing error observed, reducing the phase error from 11.3^{O} to 0.4^{O} average. The amplitude is increased by approximately 0.6dB as a result.

In the constructed system the primary cause of error is the HV switch drivers, however a practical system could experience delays in the LC tank driver, requiring phase trimming in the opposite direction. To simulate this scenario, the operating frequency was reduced to approximately 109kHz and an artificial delay created externally for V_{DR} to create a V_{DR_late} signal, with which the LC circuit is driven. Figure 6-8 shows how phase trimming was applied, reducing the V_{DR_late} -V_C phase error from 25.1^{O} to 0.2^{O}. The amplitude is increased by approximately 1.2dB in this case.

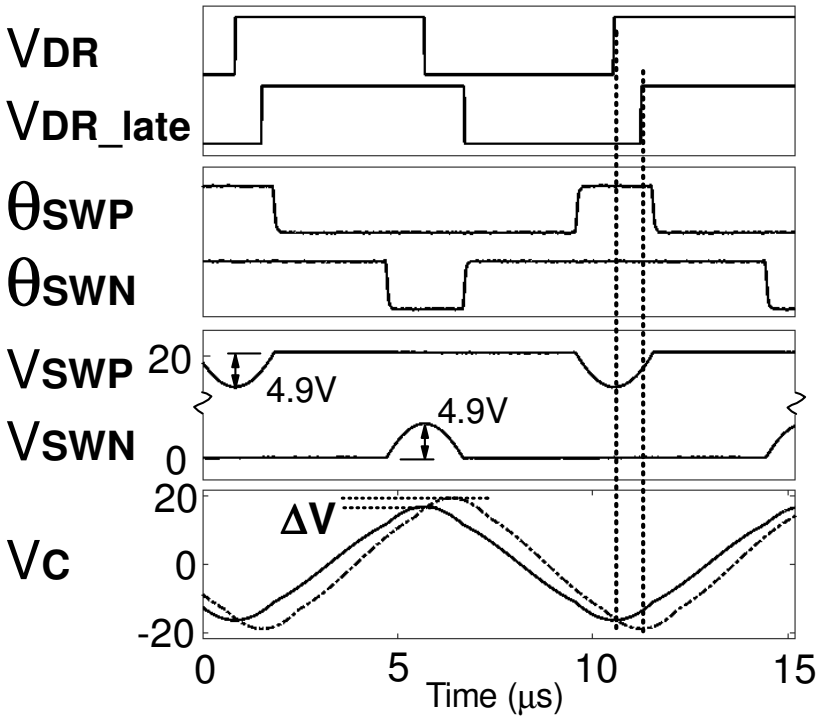

Figure 6-8: Tuning error correction for driver phase lag with phase trimming of HV switching action at 109kHz (Q = 30, solid line for V_C in untrimmed case, dotted line for V_C in trimmed case)

6.4 Summary of "lctune018" testing

The core functions of the constructed IC were tested and worked satisfactorily. The basic tuning method correctly creates the expected symmetrical tuning. The digital self-tuning functionality achieves a high tuning resolution and accuracy, significantly reducing the number of tuning capacitors compared to an equivalent conventional binary-weighted approach. As expected, the tuning accuracy degrades at higher operating frequencies, however the phase trimming functionality permits manual adjustment to compensate for the inherent timing delays of the system.

The constructed IC has a programmable gain for self-tuning, which when increased allows a fast response to a step in operating frequency. There is however transient detuning at the moment of the frequency shift, and ripple in the tuning setting in the steady state, due to the high integration gain. Ideally there would be no reduction in the amplitude of oscillation and low ripple in the self-tuning. The next chapter details how these problems can be overcome with phase-continuous adjustment of the antenna drive and resonant frequencies, giving rise to both FSK and PSK modulation.

7 Frequency/Phase-Shift Keying with Zero-Voltage Switched Fractional Capacitance

This chapter explains how a synchronous adjustment of the antenna drive and resonant frequencies can be achieved without losing circulating energy. It is shown how the zero-voltage switched fractional capacitance tuning method can also be used to achieve this, permitting modulation of the operating frequency in a driven LC circuit above the classical 3dB bandwidth limitation. This synchronous drive/resonance adjustment technique is then adapted to permit phase modulation. The existing system architecture for self-tuning with switched fractional capacitance is modified to provide adaptive tuning with multiple operating frequencies.

7.1 Maintaining data bandwidth at high-Q

In many applications, it is advantageous to be able to transmit both power and data simultaneously over the same medium, i.e. inductive coupling. As briefly discussed in the introduction, ASK is typically used in most applications, most commonly in the form of OOK, due to its relative simplicity allowing for cheaper circuitry with lower power consumption overhead at the receiver. A major disadvantage of OOK is the reduced average power delivered to the receiver, since the magnetic field from the transmitter is being disabled for part of the time.

An ideal system would use PSK or FSK so that there is no reduction in power delivery. However, a high-Q LC antenna circuit driven at resonance has significant amounts of circulating current which counteracts a forced change in the drive frequency or phase. This slows the overall response time for the circulating current to align with the new frequency or phase. It is also established that if the frequency is changed to be different from the resonant frequency then the amplitude of oscillation will be reduced.

If however the resonant frequency is synchronously adjusted with the drive frequency, the circulating current in the LC antenna circuit will not be counteracted by this change, since resonance is being maintained at all times. Figure 7-1 shows the concept, whereby the drive frequency and antenna resonant frequency are controlled by an incoming analogue data signal. The result is frequency modulation of the inductor current without any significant change in the amplitude of oscillation.

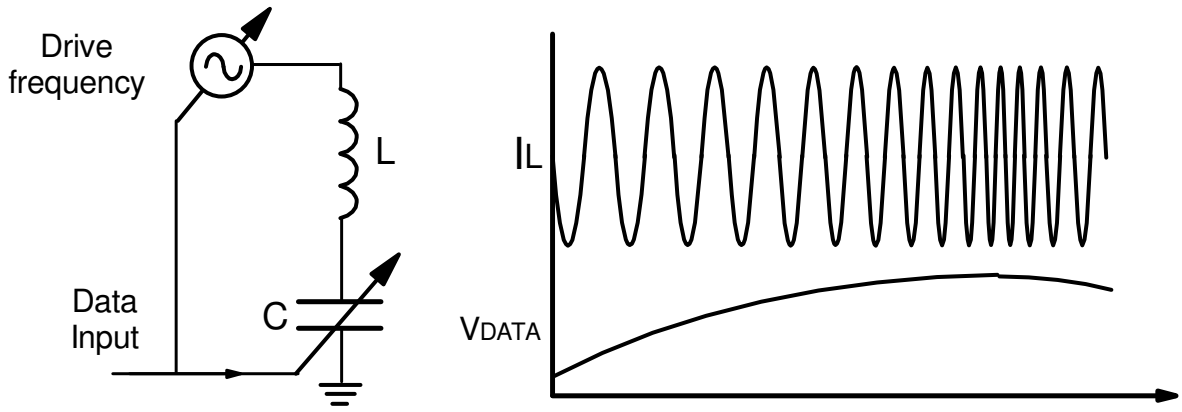

Figure 7-1: Synchronous drive and resonant frequency adjustment on LC circuit

In practical systems with digital architectures, FSK is preferred over analogue FM. This can be achieved on the LC circuit, provided the synchronism in drive and resonant frequency change is maintained. This approach has been proposed for conventionally-tuned system with weighted capacitors, with a dedicated FSK capacitor to provide a fast step in the antenna resonant frequency [45]. To minimise energy loss, this architecture requires observation of the antenna voltage V_C to prevent closure of the FSK capacitor switch when there is significant voltage across it. (figure 7-2).

The developed switched fractional capacitance tuning system can also achieve FSK with synchronous drive and resonant frequency adjustment. At resonance, the V_C waveform is ideally aligned with the internal timing reference V_{TR}. Observation of the timing reference is more convenient than an external HV voltage, facilitating the inclusion of FSK functionality with timings as per figure 7-3. Crucially, resonance has been maintained with no additional energy dissipation, therefore the Q factor remains high and the oscillating magnetic field around the inductor is not disturbed. The intended receiver therefore continues to have power delivered whilst simultaneously receiving data, in the form of a frequency shift. This circumvents the reduced power delivery problem caused by ASK, whilst also solving the problem of narrow bandwidth for FSK caused by the high-Q.

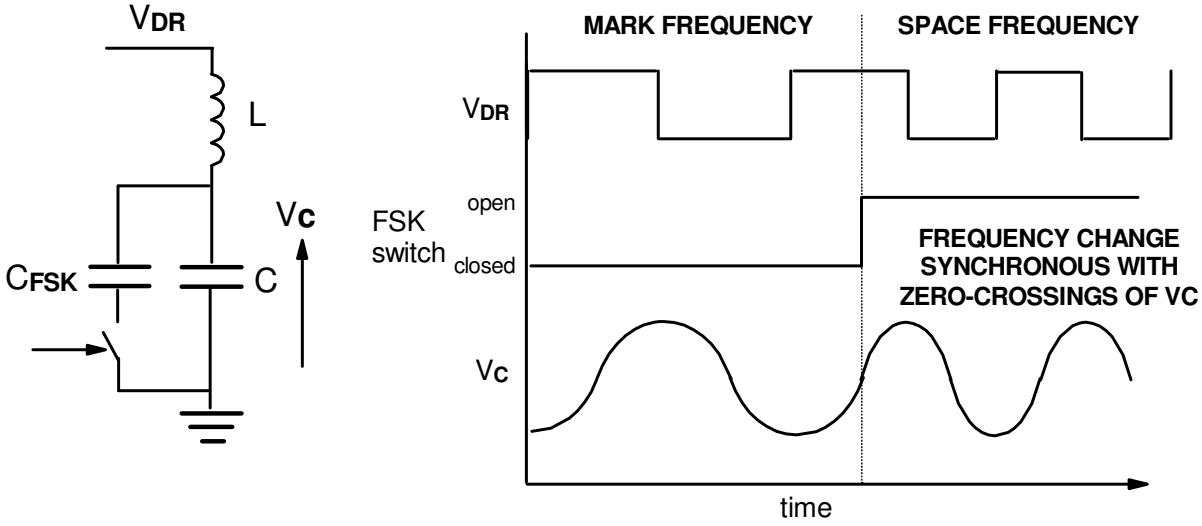

Figure 7-2: Resonant frequency step using modulation capacitor C_{FSK} [45]

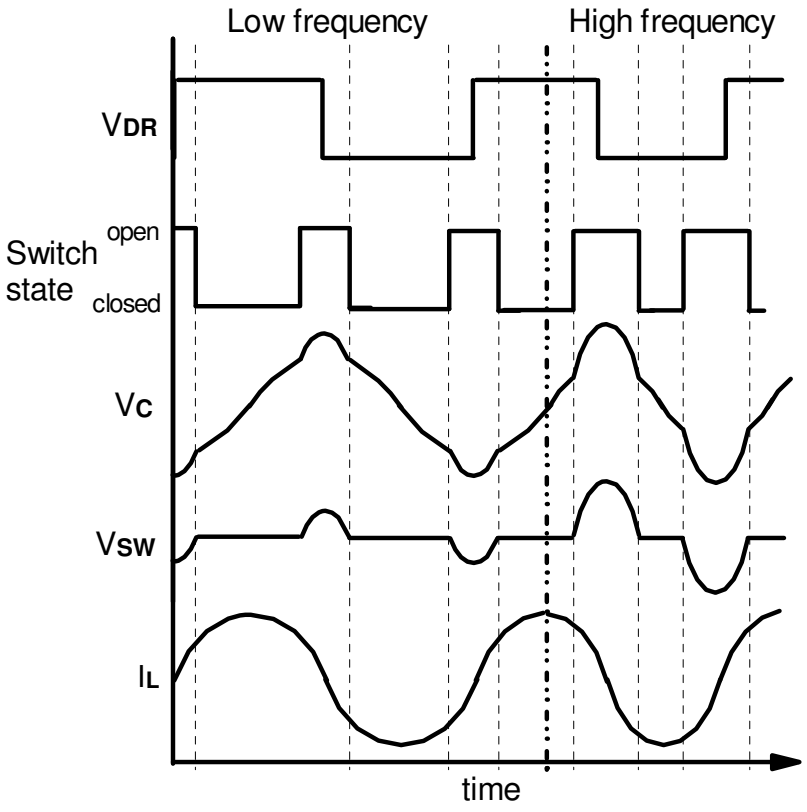

Figure 7-3: Resonant frequency step using switched fractional capacitance tuning

Whilst a receiver may use a lower-Q LC tank circuit to avoid the need for tuning, it is still generally preferable to avoid the use of FSK in order to maintain a singular carrier frequency. This can be avoided by using PSK, however the oscillation in the transmitter tank cannot change phase instantaneously. Commercial products exist which solve this problem by temporarily "pausing" the oscillation on the LC antenna circuit, using timings shown in figure 7-4 (method referred to as "quick-start control" in [46]). When the voltage on the capacitor reaches a maximum, the antenna is disconnected from the drive, storing all the energy in the capacitor charge. After a brief moment, the antenna circuit is re-connected and continues operating as before. The brief pause and restart of the oscillation on the antenna creates a phase offset relative to the previous position. For PSK, the time delay is set so that a precise phase angle is created.

This method creates a phase shift whilst avoiding an instantaneous phase change, preventing energy from being lost from the antenna. It can also be adapted provide OOK modulation with no rise or fall time, permitting a higher data bandwidth. However, both OOK and PSK with this method create a time interval where no EMF is being induced in the target receiver, so the problem of reduced power delivery is not completely solved.

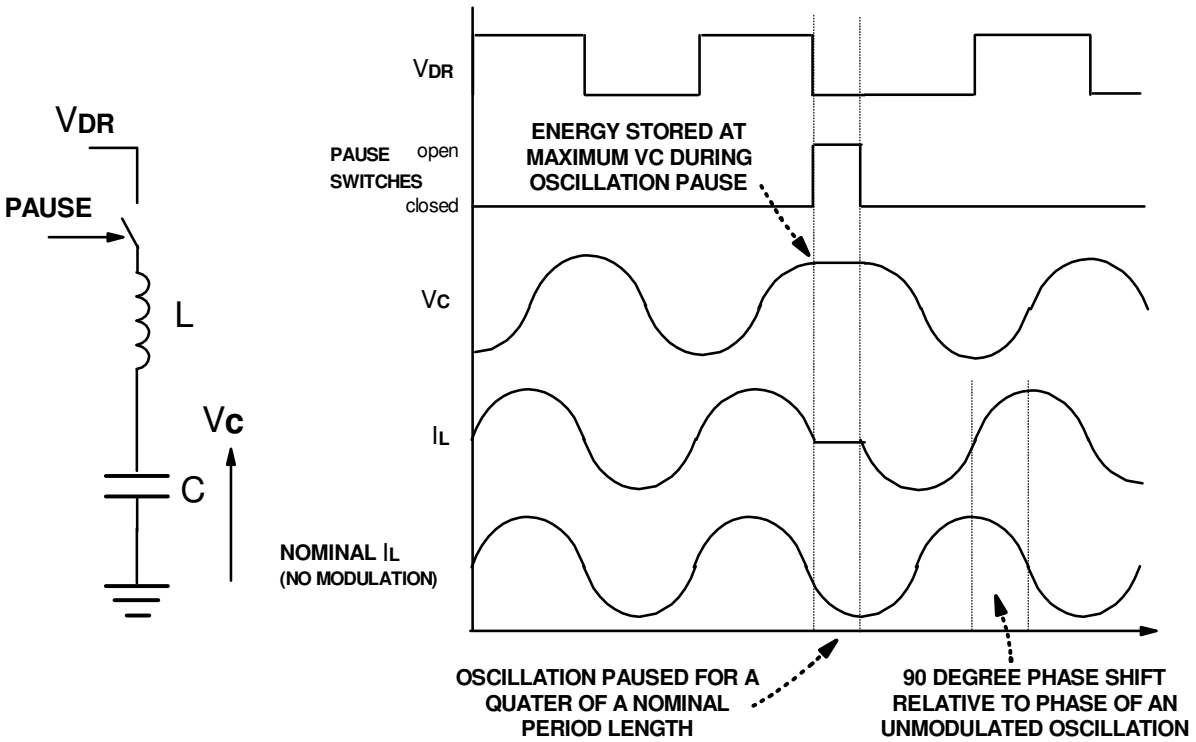

Figure 7-4: PSK of tank oscillation by means of oscillation pause "quick-start control" [46]

Using switched fractional capacitance tuning, the ability to step the resonant frequency as previously described also facilitates PSK [2]. Whilst an instantaneous phase change is not possible, it is instead possible to spread the phase adjustment over a number of cycles by switching to another frequency. Compared to the method of pausing the oscillation in [46], an oscillation is maintained on the antenna circuit at all times, hence power delivery to the receiver is continuous throughout the phase shift. When the tank switches back to the normal centre frequency, there is an apparent offset in the phase position relative to the oscillation before the change occurred, as shown in figure 7-5 for a phase lead, and figure 7-6 for a phase lag.

Note that the exact angle of phase shift is dependent upon the fast and slow frequencies used. If a particular angle of shift is required, then the shifting frequencies should be calibrated accordingly. As for FSK, the antenna must be tuned instantaneously to the shifting frequency to avoid energy loss.

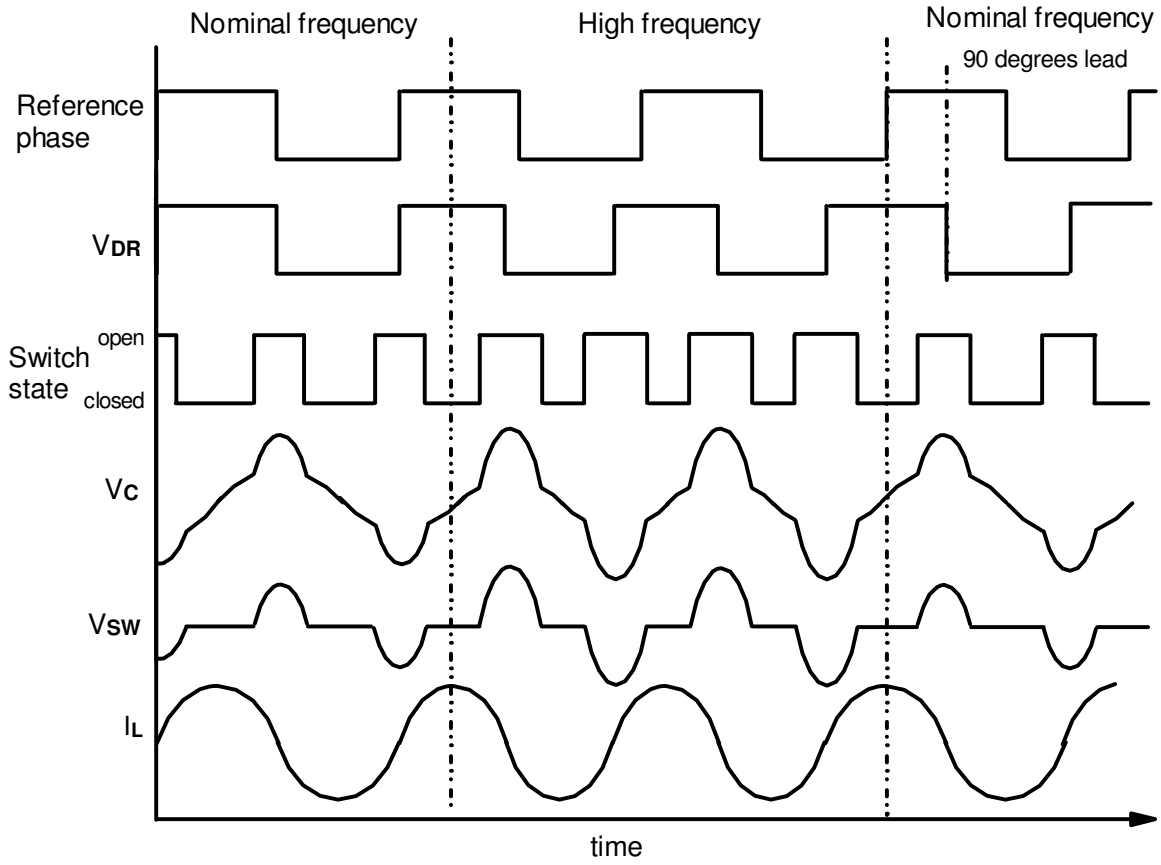

Figure 7-5: Phase advance of tank oscillation using step change in LC tank resonant frequency

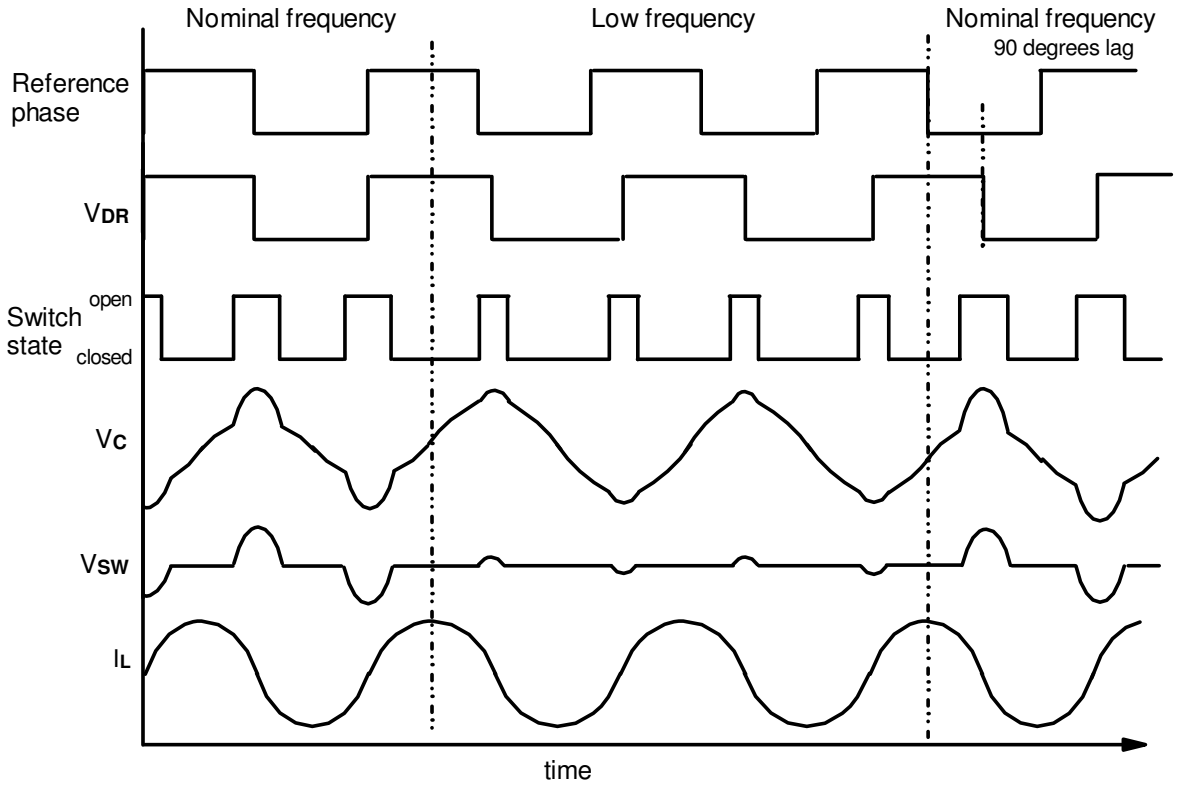

Figure 7-6: Phase reduction of tank oscillation using step change in LC tank resonant frequency

7.2 Required tuning range for PSK with switched fractional capacitance

In order to create an apparent change in phase, the tank must step to a higher or lower frequency for a period of time, at the very least half a cycle. The amount of shift possible depends entirely upon the tuning range of the tank, since a larger amount of phase shift per cycle requires a greater deviation from the original frequency, as shown in figure 7-7. Equations 7.1 and 7.2 arise from visual inspection of the waves, indicating the duration needed to create the intended amount of phase per cycle, hence the minimum tuning range required to achieve this is given by equation 7.3, this example for 90 degrees of shift / cycle requiring a tuning range of 1.67:1.

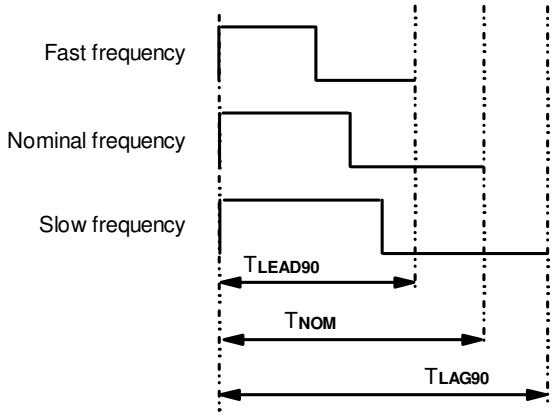

Figure 7-7: Required period durations for required phase shift/cycle

$$T_{lead90} = \frac{3}{4}T_{nom} \tag{7.1}$$

$$T_{lag90} = \frac{5}{4}T_{nom} \tag{7.2}$$

$$\frac{f_{max}}{f_{min}} = \frac{T_{lag90}}{T_{lead90}} = \frac{5}{3} \approx 1.67 \tag{7.3}$$

In practice, a larger tuning range would be required to compensate for detuning effects during normal operation as well as the desired PSK shifting frequencies. As per figure 7-8, including the additional tuning range per equations 7.4 7.5 and 7.6 yields a total tuning range in equation 7.7. In a numerical example of 90^{O}/cycle shift capability and a 1.22:1 tuning range to allow for ±20% combined component tolerances, the total range required would be approximately 2.03:1.

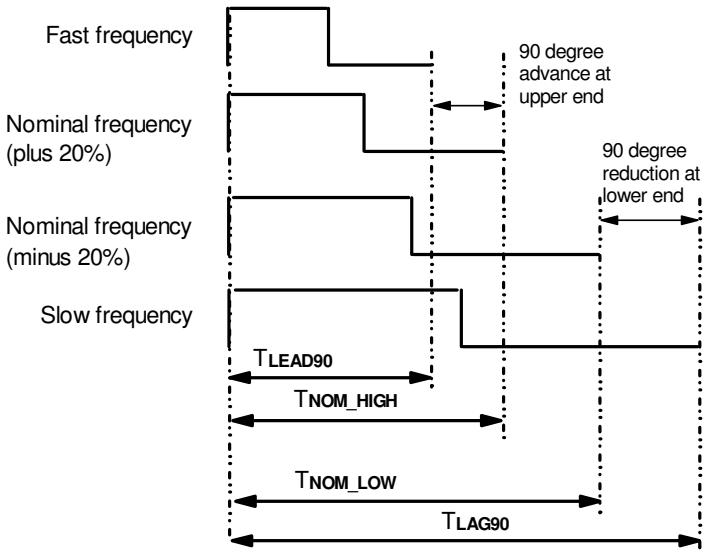

Figure 7-8: Required period durations for required phase shift/cycle, allowing for tuning tolerances

$$\frac{T_{lead}}{T_{nom\_high}} = \frac{\theta_{period} - \theta_{change}}{\theta_{period}} \tag{7.4}$$

$$\frac{T_{lag}}{T_{nom\_low}} = \frac{\theta_{period} + \theta_{change}}{\theta_{period}} \tag{7.5}$$

$$\frac{T_{nom\_low}}{T_{nom\_high}} = r \tag{7.6}$$

$$\frac{f_{max}}{f_{min}} = \frac{T_{lag}}{T_{lead}} = r\frac{360 + \theta_{change}}{360 - \theta_{change}} \tag{7.7}$$

With the previous 1.414:1 tuning range, maintaining a 1.22:1 range to compensate for detuning effects limits the phase change per cycle to around 26.5^{O}, hence limiting to 22.5^{O}/cycle means that 90^{O} of shift can be obtained in 4 cycles of tank oscillation.

7.3 FSK/PSK with self-tuning

Since the switched fractional capacitor method of tuning the LC tank is being used, the previously discussed and tested method of tuning by sign detection just before switch closure still applies. An important difference is the presence of multiple operating frequencies, each requiring independent tuning settings. The existing architecture can be built upon to allow this, as shown in figure 7-9, where each operating frequency utilises a separate tuning loop to track resonance at that frequency whilst it is being used. Otherwise, the last known tuning setting is stored.

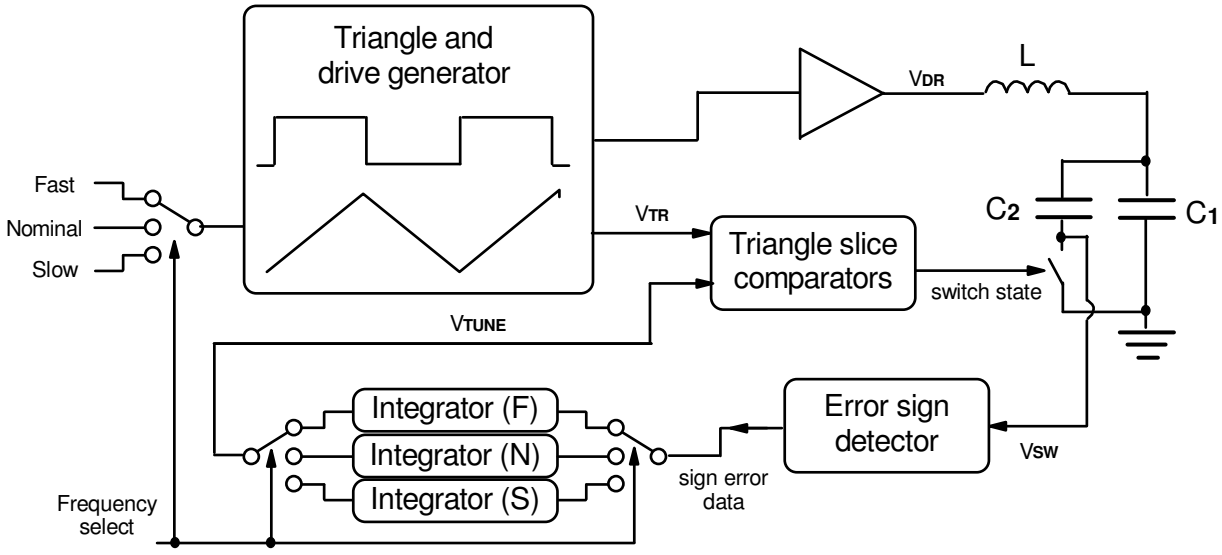

Figure 7-9: Self-tuning concept for multiple operating frequencies using switched fractional capacitance

Since the fast and slow frequencies used for the PSK modulation are used for comparatively short durations, it may take longer for these to be brought to resonance as per the nominal frequency. To combat this, a higher integrator gain can be used for these shifting frequencies, where the effect of higher ripple in their tuning settings has negligible effect on the power transferred compared to the nominal operating frequency.

Theoretically, all three tuning loops could be updated simultaneously. For example, if the inductance is increased by a particular amount, the modified resonant frequency setting requires an X% adjustment to compensate. This adjustment can be applied to the other operating frequency loops so that they will be close to the ideal resonant condition immediately when selected. Since the relationship between the

tuning setting and modified resonant frequency is highly non-linear, a calculation or reverse look up table is necessary to provide the appropriate scaling, as per figure 7-10. The max:min frequency range is also required for calculating the correct amount of compensation. Hence, there is cost in additional logic and processing to compensate for the detuning effect on all resonant frequency settings.

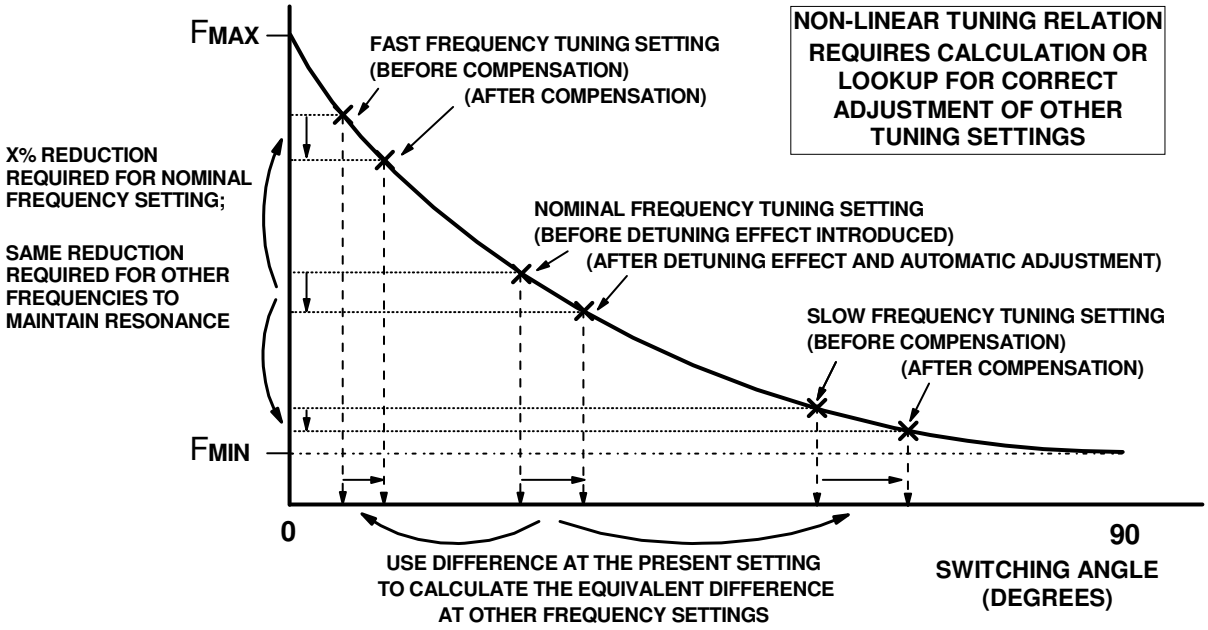

Figure 7-10: Simultaneous correction of all tuning frequencies, accounting for non-linear relation of tuning setting and modified resonant frequency

7.4 Summary of frequency/phase modulation with switched fractional capacitance

To overcome the limitation of data bandwidth at high Q, the operating frequency may be modulated by synchronously adjusting the drive frequency and resonant frequency of the antenna circuit. This results in the operating frequency being changed without any loss of energy from the resonant circuit, hence a large magnetic field is maintained for power transfer. This method of frequency modulation can be easily achieved with zero-voltage switched fractional capacitance tuning.

To permit phase modulation, the operating frequency can be temporarily increased or decreased and then returned to the nominal frequency, creating a net phase rotation without disrupting the oscillation. Hence phase shift keying is also possible whilst maintaining power delivery to the receiver.

For each intended modulation frequency, the optimum resonant tuning switch duty cycle is different. Therefore, the existing self-tuning architecture previously described and tested requires some form of memory to store the last known resonant tuning setting at each operating frequency until it is required.

Note that for precise phase angles of rotation, the shifting frequencies used for phase modulation must be precisely set with respect to the nominal frequency. Otherwise, the resulting phase shift will have an incorrect angle, leading to possible data corruption. An integrated implementation must have a way of calibrating this frequency. A solution which builds upon the existing architecture is described in the next chapter.

8 Implementation of combined tuner and PSK transmitter with CMOS HV process: 10kHz – 2MHz "lctune018_psk"

This chapter describes the development and testing of a modified IC architecture to include FSK and PSK modulation. Of particular importance is the development of a novel means of automatic frequency calibration, such that the PSK angle is calibrated for an ideal $90^O/180^O$ phase rotation.

8.1 Requirements

The overall user requirements of the second IC were similar to the first. The system must both drive and tune an external LC tank, with up to 100mA of tank current at up to 2MHz, using on-board drivers and switches. In terms of technology, it was most logical to proceed with the same 0.18µm HV process used previously, since it was clearly suitable and significant time had been invested in understanding how to use it. Given the scope of the work, it was again not necessary to include on-board voltage regulators and bias current sources.

The most important new requirement was the ability to generate the correct frequencies and timing for PSK. This required investigation into different solutions, which are detailed in the next section. The system should be able to achieve phase shifts of at least 90^O and 180^O, using at least 22.5^O/cycle of shift. (i.e. QPSK with transitions in 4 and 8 cycles respectively). It must also be able to generate the exact frequencies required without manual trimming, either by self-calibration or by being architecturally immune to PVT offsets.

8.2 Frequency generator architecture choices

The most important development of this design upon the previous is having some means of calibrating the shifting frequencies for PSK. If the shifting frequencies are not controlled, the phase angle of PSK becomes poorly defined and may cause data corruption. Different solutions for generating deterministic phase changes were investigated.

8.2.1 Fully digital approach

A digital triangle in the form of an up-down counter can be used to generate the capacitor switch timing and tank drive. For a fixed clock frequency, setting a higher peak and trough value in the counter will vary the operating frequency, i.e. more counter clock cycles are required to complete one cycle of LC tank oscillation. The triangle is compared with digital comparators to control the LC tank switches.

Figure 8-1 shows how a digital generator could operate. If the antenna drive V_{DR} is created from the peaks and troughs of the triangle, then any change in frequency must occur at the mid-point crossing of triangle, since at resonance the V_C mid-crossings are aligned with the mid-crossings of the triangular timing reference. Hence additional detection logic is included to fulfil this requirement.

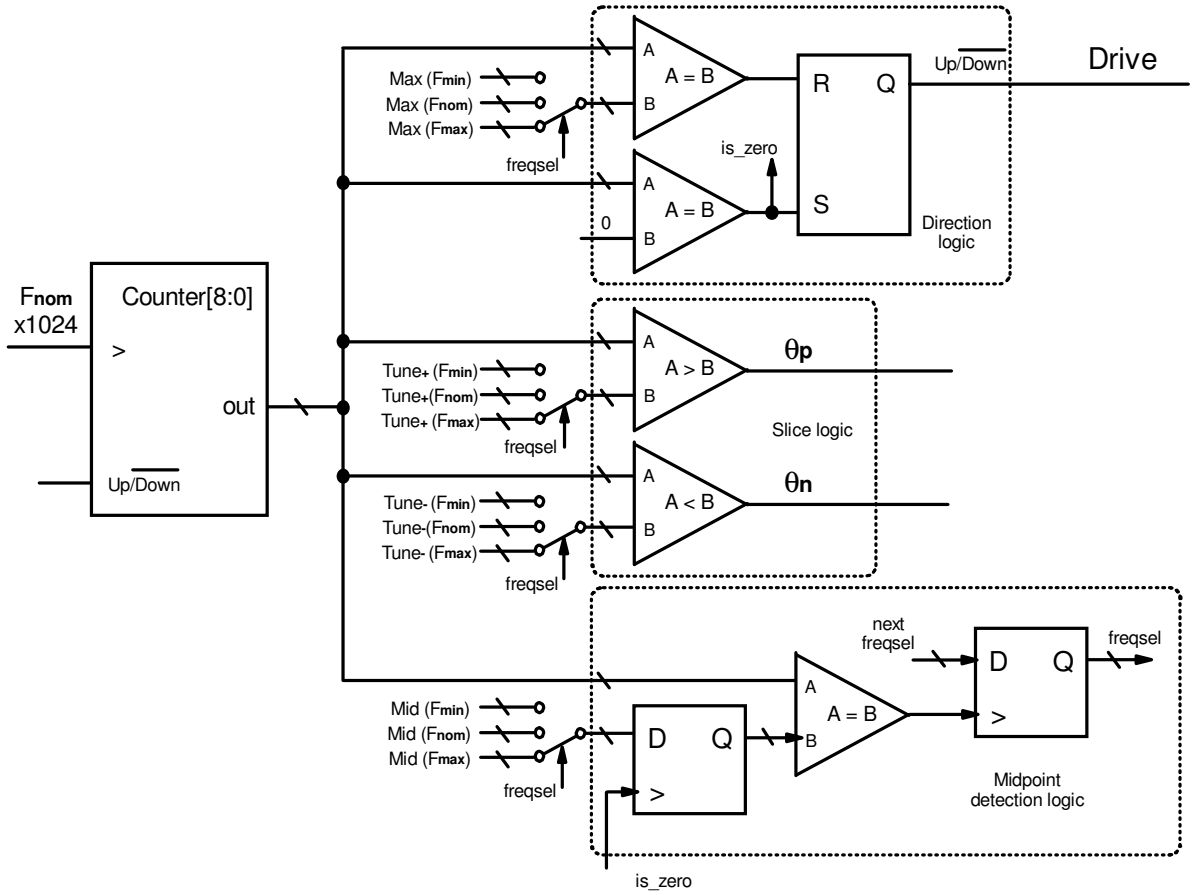

Figure 8-1: Digital frequency and tune timing generator for frequency shifting with switched fractional capacitance

8.2.1.1 Required slicing range

The slicing resolution is split across the digital triangle evenly, with more levels improving the tuning resolution of the LC tank. The previous IC used an 8-bit architecture was sufficient for high tuning accuracy, with two lots of 256 tuning settings spread across the triangle, hence a minimum of 512 levels would be required to obtain the same resolution, i.e. a 9-bit counter. 1024 clock cycles are hence needed to complete one cycle of LC tank oscillation.

8.2.1.2 Required frequency range

In order to meet the slicing accuracy requirements, the minimum size of the digital counter is set at the highest frequency, with additional levels needed to provide a longer duration of LC tank oscillation. The counter must also have a high enough resolution to ensure that the exact shifting frequency can be achieved, avoiding a net phase offset from being created. For a phase shift of 22.5^{O}/cycle, the equivalent period durations are as per table 8-1, which indicates from T_{fmin} that an 11bit counter is required.

Periods	T_{fmax}	T_{fnom}	T_{fmin}
Normalised to T_{fnom}	0.9375 T_{fnom}	T_{fnom}	1.0625 T_{fnom}
Normalised to T_{fmax}	T_{fmax}	1.0666 T_{fmax}	1.1333 T_{fmax}
Counter Maximum	512	546	580

Table 8-1: Table of frequency ratios for 22.5^{O}/cycle phase shifting in digital architecture

A fully digital timing generator does not require internal calibration, since an external known reference such as a crystal oscillator can be used. For integration in this process, and external signal generator could be used. To operate at 100kHz tank frequency, a clock frequency of up to 116MHz is needed. For operation at 2.6MHz tank frequency, the clock must be at least 3.02GHz. As per the first IC, the high frequencies required for the upper end of operation were considered to be impractical for

implementation in the available design time and chosen process, however may be suitable for an FPGA-based system.

8.2.2 Fully analogue approach

The previously-engineered architecture using an analogue triangular voltage wave integrated from a square wave current can be reused. The tuning resolution can be set to the same value as before by reusing the same DACs and comparator blocks. This significantly reduces schematic and layout assembly and verification time, making an analogue approach attractive in the context of this project.

8.2.2.1 Required frequency range

To implement the correct frequencies for phase shifting, either the magnitude of the square wave current or the value of the integration capacitors can be adjusted. Since the frequency control available from capacitor variation is coarse, accurate frequency control requires adjustment of the current. Assuming that 22.5^{O}/cycle of shift is required, current mirrors with set ratios of the nominal current can be used to create the shifting frequencies, based on copies of the nominal current. Equations 8.1 and 8.2 show how these are calculated.

$$T_{fmax} = T_{fnom} \times \frac{360 - 22.5}{360} = T_{fnom} \times \frac{15}{16} \tag{8.1}$$

$$T_{fmin} = T_{fnom} \times \frac{360 + 22.5}{360} = T_{fnom} \times \frac{17}{16} \tag{8.2}$$

In the analogue triangle-based architecture, the expression for the period can therefore be used to calculate the current mirror ratios required, as per equations 8.3, 8.4 and 8.5.

$$I_{nom} = \frac{2\ C\ dv}{T_{nom}} \tag{8.3}$$

$$I_{fmax} = \frac{2\ C\ dv}{\frac{15}{16} T_{nom}} = \frac{32\ C\ dv}{15\ T_{nom}} \tag{8.4}$$

$$I_{fmin} = \frac{2\ C\ dv}{\frac{17}{16} T_{nom}} = \frac{32\ C\ dv}{17\ T_{nom}} \tag{8.5}$$

Hence a 32/15 mirror for I_{fmax} and 32/17 mirror for I_{fmin} are required. For both of these fractions, producing a well-matched layout is non-trivial, hence some kind of calibration would be required to trim the current, should the mirror deviate from the ideal ratio. Furthermore, even with the best possible matching in layout, random mismatch will create a difference in the current, hence offsetting the shift frequency from the ideal value.

8.2.2.2 Frequency calibration

Whilst the exact ratios of the fast, nominal and slow frequency currents for QPSK can be computed and implemented in hardware, tolerances in the absolute values of the currents and mirror ratios necessitate some form of calibration. Ideally, this calibration should be automatic and occur periodically to compensate for temperature or voltage-based variations.

Figure 8-2 shows a system concept whereby the fast and slow frequencies can be calibrated with respect to the nominal. The phase of the nominal oscillation is stored in a Phase Locked Loop (PLL), and the target phase shifts are derived from this.

In order to achieve a phase shift, the system temporarily increases or decreases in operating frequency and then returns to the nominal. The target phase derived from the original oscillation i.e. before the

frequency shift occurred, is compared with the new phase after the transition, and the error is determined. If the new phase lags behind the target phase, then the shifting frequency must be increased. If the new phase leads in front of the target, then the shifting frequency must be decreased.

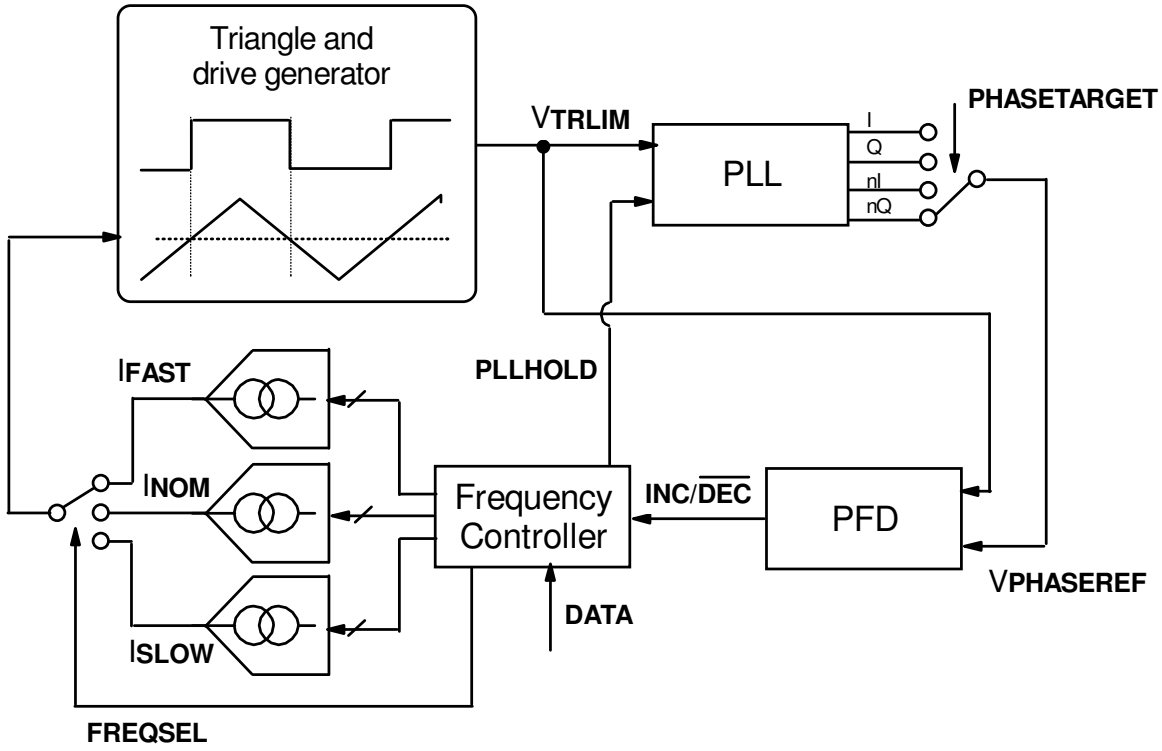

Figure 8-2: Automatic frequency calibration to achieve target phase shift by frequency shifting

A Phase-Frequency Detector (PFD) can be used to determine whether the new phase or the target have relative lead or lag. If the original architecture is used, whereby a DAC controls a voltage-to-current function to set the operating frequency, then the DAC code for the fast or slow frequency may simply be incremented or decremented by one code as is required to correct the error. Note that the phase comparisons are based upon a clipped version of the triangle wave, V_{TRLIM}, since the change in frequency needs to occur at the mid-point crossings of V_C to maintain symmetry of the V_{SW} excursions. Hence by extension V_{TR} must also change frequency only at its mid-point crossings.

Figure 8-3 shows a timing example of ideal operation of the system. The *DATA* signal instructs the system to perform a phase advance of 90^O for 4 cycles, so *FREQSEL* switches to the fast frequency. The *PLLHOLD* signal goes high, so that the PLL VCO setting is held in place in order to retain the original phase of the oscillator's nominal frequency. After 4 cycles on the fast frequency, the system switches back to the nominal frequency. Since we expect to see a 90^O phase error, *PHASETARGET* is set to select the inverted quadrature version of the original oscillation for the $V_{PHASEREF}$ comparison. The stored phase in the PLL is compared with the new phase using a PFD, creating an *INC/nDEC* signal. In this example, the shifting frequency is too low, and so the corresponding DAC code is incremented by one. After the frequency comparison is complete, the *PLLHOLD* is set low and the PLL begins to track the new phase in preparation for the next data symbol to be transmitted.

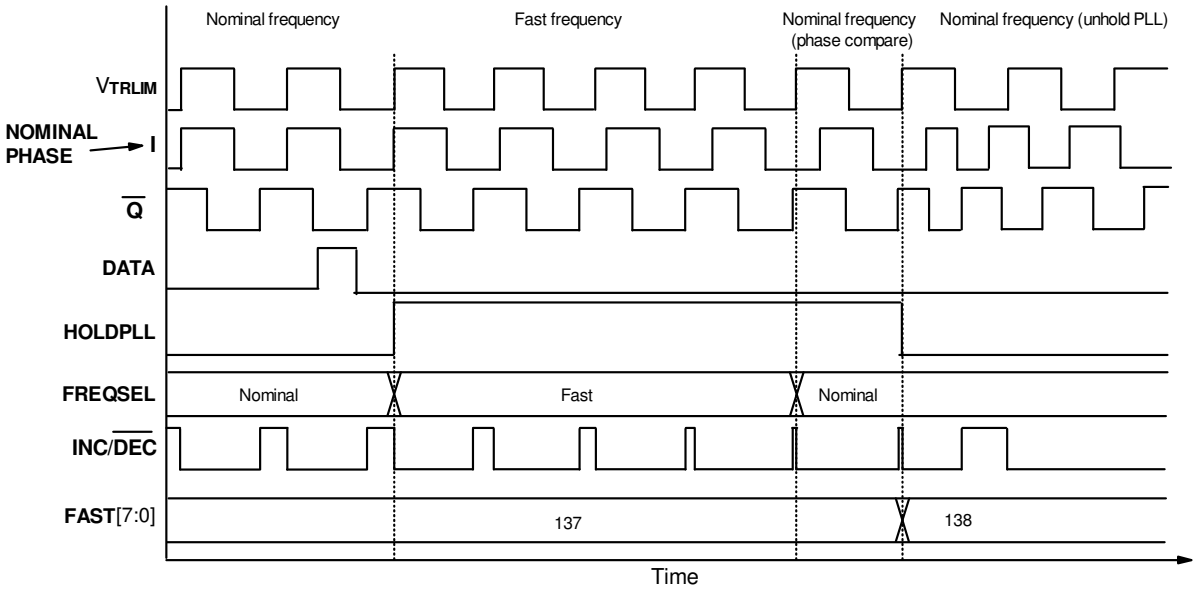

Figure 8-3: System frequency calibration loop: 90^{O} phase lead target example

As well as correcting for drift in frequency due to temperature or voltage variations, the system inherently does not require manual calibration of the shifting frequencies to begin with. Instead it will converge upon these after the transmission of multiple PSK data bits. The disadvantage of this behaviour is the need for an initial transmission burst in order to bring the shifting frequencies close to where they should be.

Another disadvantage is the time taken for the frequency tracking to operate. If the frequency setting DACs are only incremented or decremented by one code regardless of the magnitude of the error, the system will take many transmission symbols to converge. The problem is shown graphically in figure 8-4. The example system is initialised with both phase shift frequencies set to the same setting as the nominal. Each time a phase lead or lag occurs, the corresponding phase shifting frequency is calibrated one DAC code closer to the optimal setting.

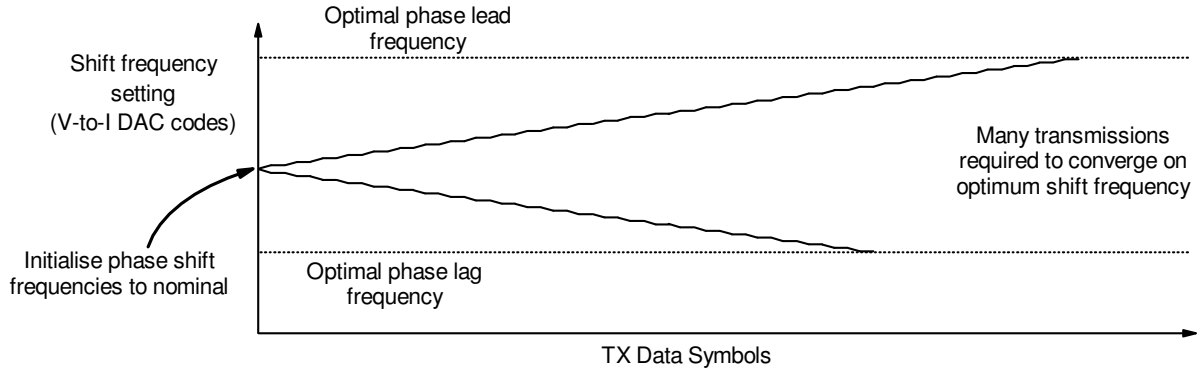

Figure 8-4: Increment/Decrement-by-one effect on convergence time to optimum shift frequency

In order to speed up convergence, the magnitude of the phase error can also be considered, using the architecture in figure 8-5. In this system, the same control sequence can be used, however the shifting frequency is directly generated by a charge pump to induce a voltage across a capacitor and feeding into a V-to-I function. If the phase error is larger, the change in the directly-generated voltage is also larger, significantly reducing the convergence time. Figure 8-6 shows the ideal control sequence, which is very similar to that in the previous *INC/nDEC* architecture.

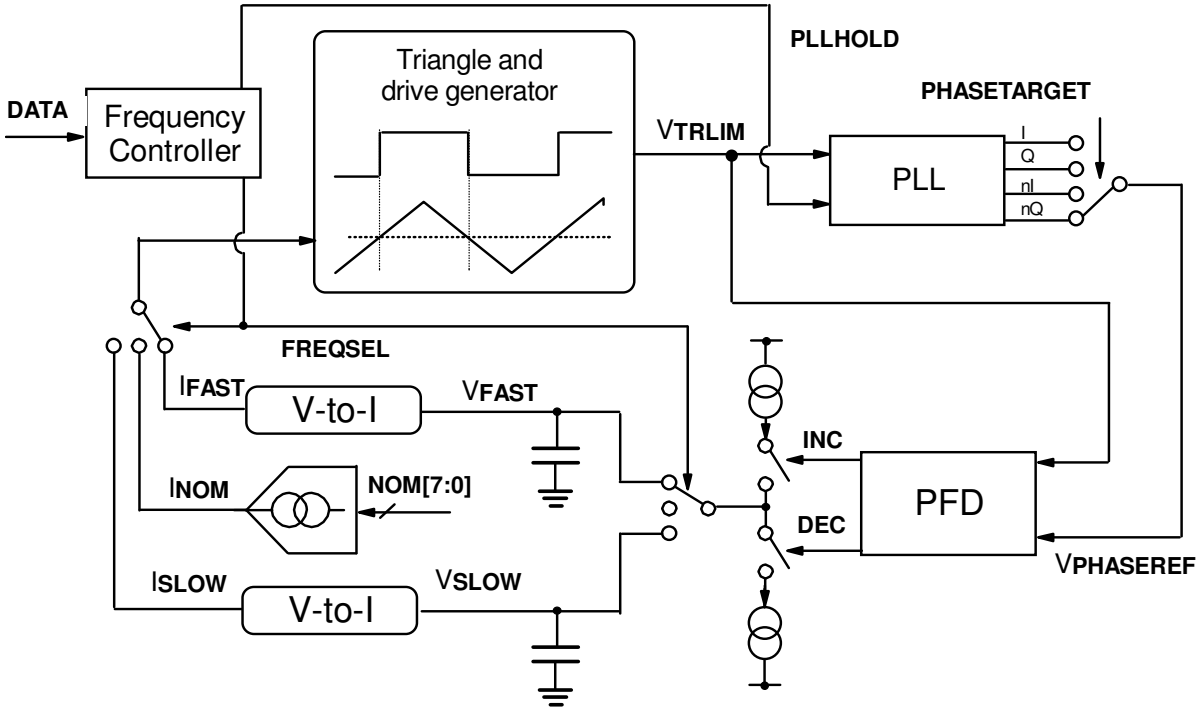

Figure 8-5: Charge-pump-based method for reduction of time to optimum shift frequency convergence

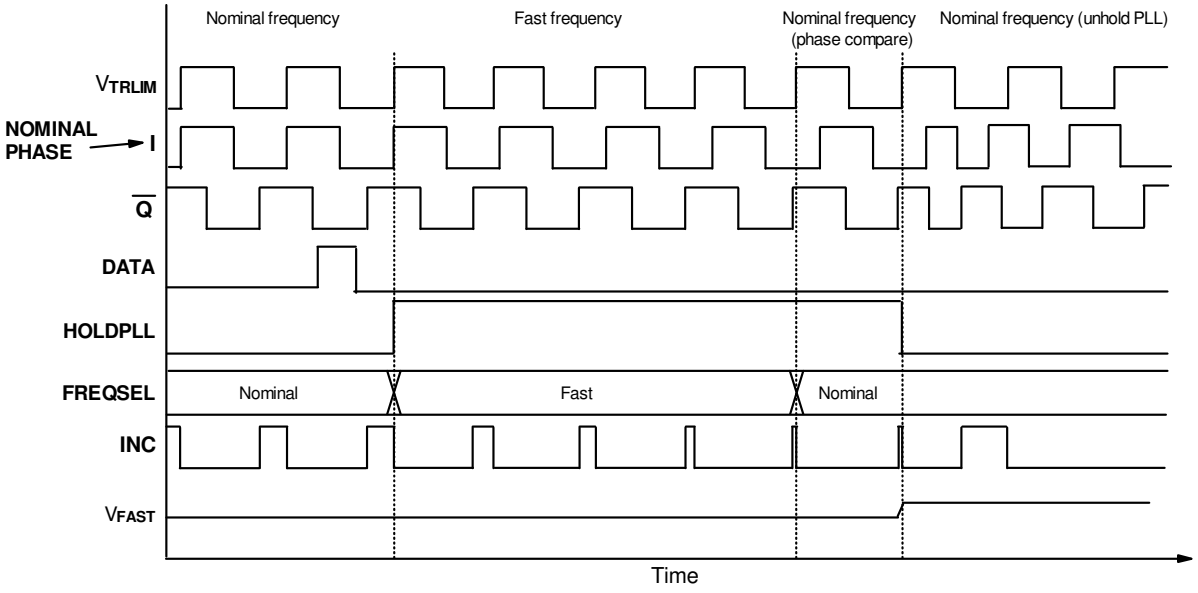

Figure 8-6: System frequency calibration loop: 90^{O} phase lead target example using direct generation of shift frequency voltage

Whilst this system will calibrate faster by having proportional control, over time the voltage stored on the capacitor will leak through the switches in the charge pump, causing the shift frequencies to slowly drift. This is particularly an issue if there are long periods in between data transmission bursts, since this is the only time when the calibration cycle runs. Every time a data burst occurs, the system will potentially need more time to fully re-calibrate than would otherwise be necessary, had the shift voltage stayed the same. The problem is shown graphically in figure 8-7, where a gradual drift over time means more calibration is needed during every data burst. This problem can be mitigated by careful design of the charge pump using low-leakage switches, but cannot be completely removed without an architecture change.

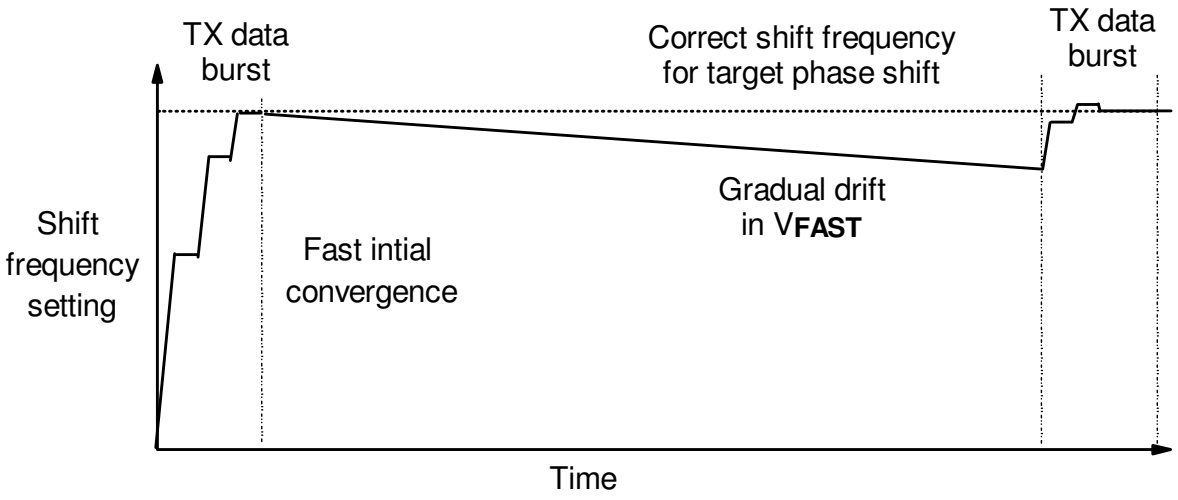

Figure 8-7: Charge leakage effect causing gradual drift in frequency shifting voltage over time

8.2.3 Mixed-signal approach

Of the two previously discussed approaches, the analogue solution is more attractive. However, the primary drawback is gradual drift due to the long durations in between self-calibration cycles. In order to solve this, the analogue charge pump can be re-configured to instead be used only phase error measurement, as per figure 8-8. In this case, the V_{ERR} is reset to a known potential using *ERRRST*, so that V_{ERR} can be easily quantised by an ADC after the measurement is complete. Figure 8-9 shows a timing example, based upon the same 90^{O} phase lead target scenario.

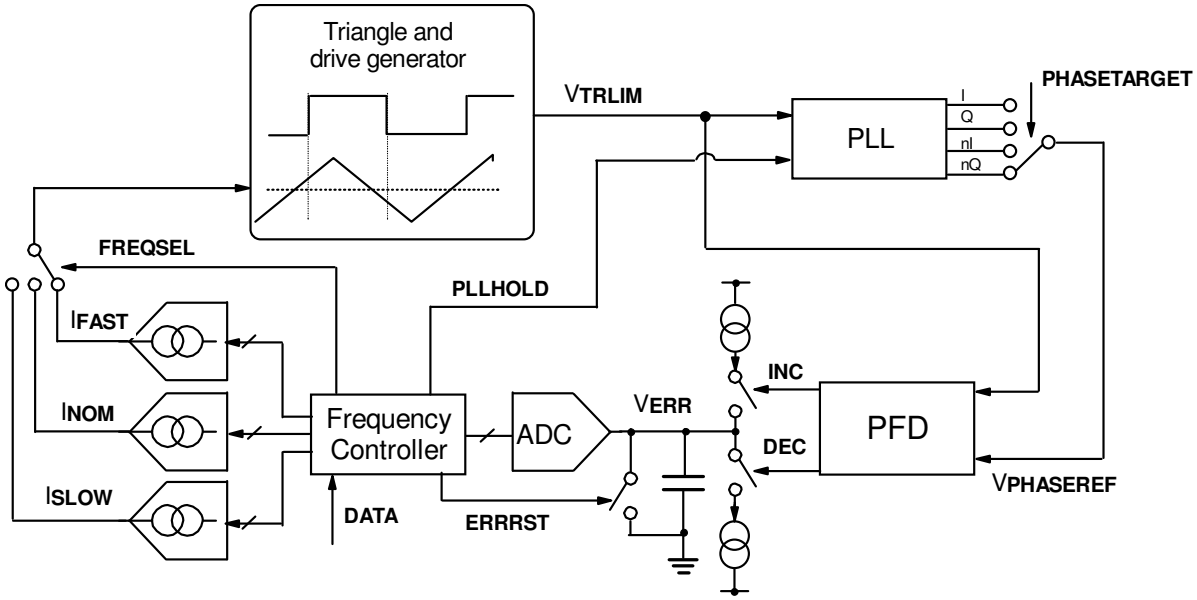

Figure 8-8: Mixed-signal system for shift frequency calibration, using charge pump and ADC

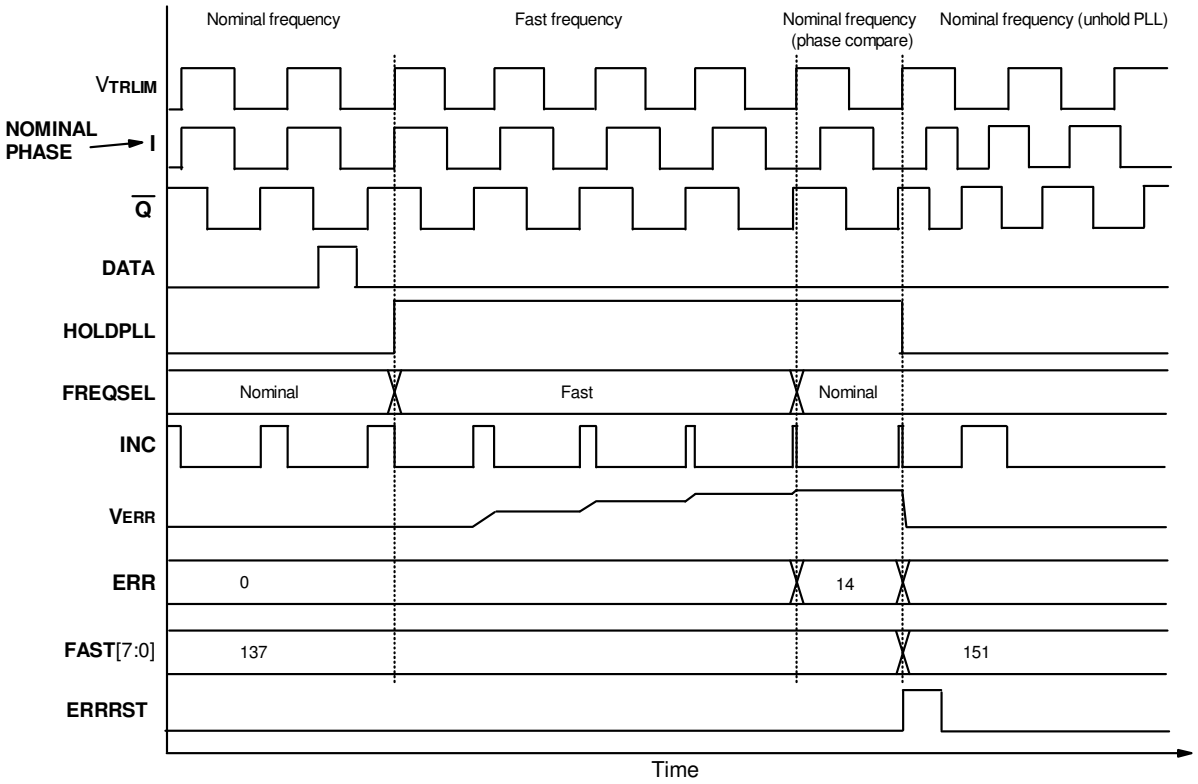

Figure 8-9: System frequency calibration loop: 90^{O} phase lead target example using phase error measurement using a charge pump and ADC

This system does not suffer from the charge leakage problem of a fully analogue solution, since the time for which charge is held by the error measurement capacitor is small, hence the effects of charge leakage are less important. However, the frequency convergence time is variable with the charge pump current and error capacitor. If the capacitor is larger than expected or the current is smaller, the loop will take longer than expected to converge. If the capacitor is smaller than expected or the current is larger, the calibration loop will over-compensate and there will be ripple in the settling response. This offset can be correct by either trimming the charge pump current or applying digital correction to the quantised error, however both of these require manual tuning.

An alternative solution to the use of a charge pump and ADC is to instead use a high frequency counter, as per figure 8-10. Provided the frequency is known, this makes the calibration loop response more consistent by removing the variation of an analogue charge pump and capacitor. Figure 8-11 shows the same example scenario of a 90^{O} phase advance, with a slightly modified control sequence to allow correct operation of the counter. After the system returns to the nominal frequency, the HF counter runs during the time that a phase error exists. Afterwards, the accumulated error is added to or subtracted from the digital code of the shift frequency and the counter is reset for the next data symbol transmission.

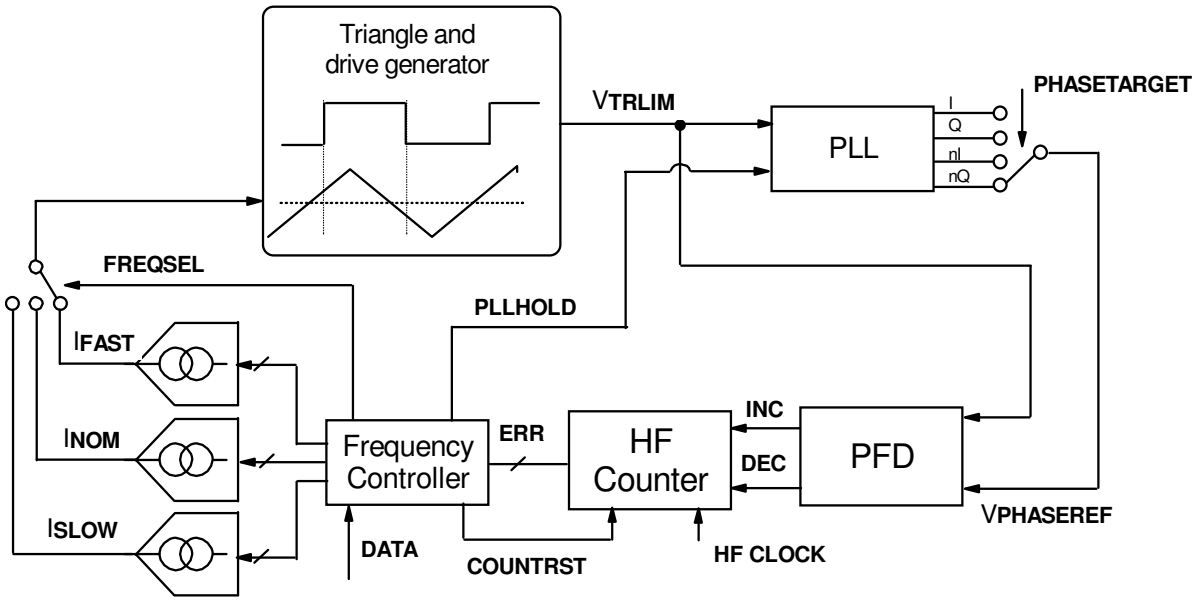

Figure 8-10: Mixed-signal system for shift frequency calibration, using high-frequency counter

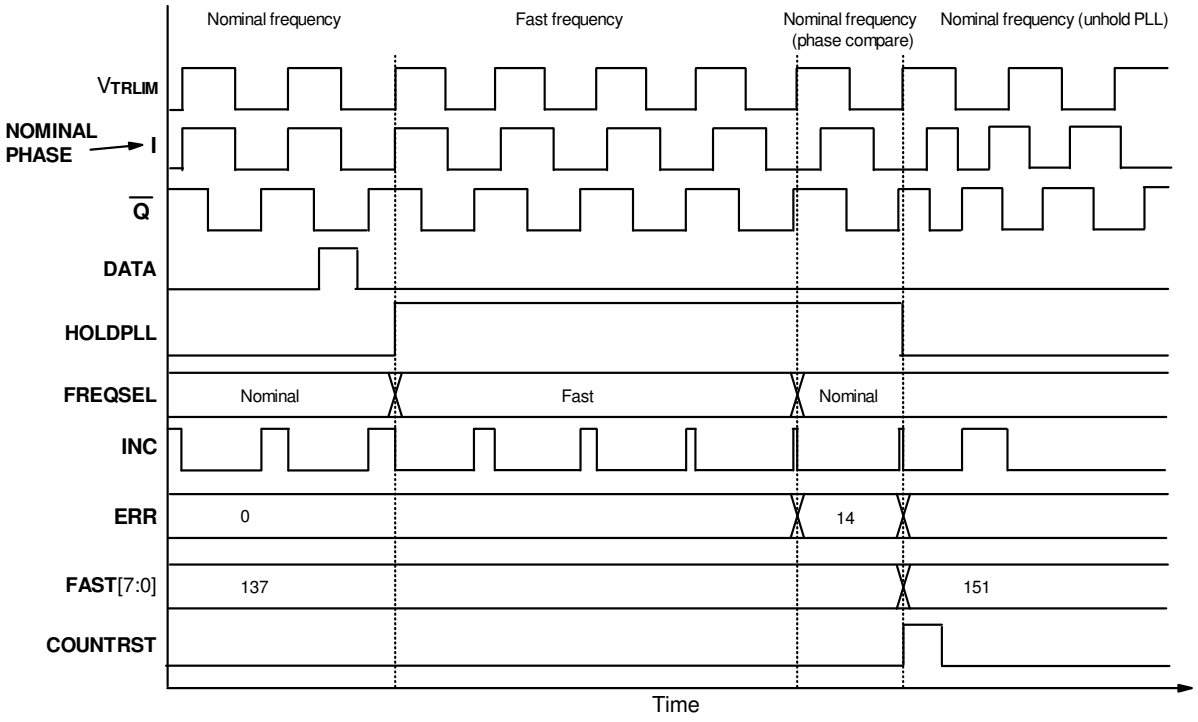

Figure 8-11: System frequency calibration loop: 90^{O} phase lead target example using phase error measurement using a HF counter

Some additional loop control can be implemented, by adding a PID (Proportional, Integral, Differential) control to the error measurements. For this, the HF counter clock frequency should ideally be known, as this allows the response of the system to be deterministic at different operating frequencies for a given set of PID parameters. In the above example in figure 8-11, the error counter measures an error of 14. Suppose that the operating frequency and counter clock frequency are both halved, then the same amount of phase angle error would translate to the same error measurement of 14. Hence, the overall frequency convergence response will be the same. This behaviour is desirable, as an optimised set of control parameters can be used at a range of frequencies.

A standalone internal or external clock reference would not be appropriate for the HF counter clock, since it would not be a guaranteed multiple of the nominal frequency. Since a PLL is already required for storing the nominal phase, this can serve additionally as the clock generator by using integer-N synthesis as per figure 8-12. The integer-N PLL still produces the required quadrature phase outputs, however the VCO inside operates at a frequency that is sufficiently high to allow accurate measurement of the phase offset, as shown in figure 8-13. Note that, after the *PLLHOLD* signal goes inactive, the *HFCLOCK* signal will dither in frequency whilst the PLL tracks the new phase of the nominal frequency. However, this is not an issue since the counter is not required for measurement during this time.

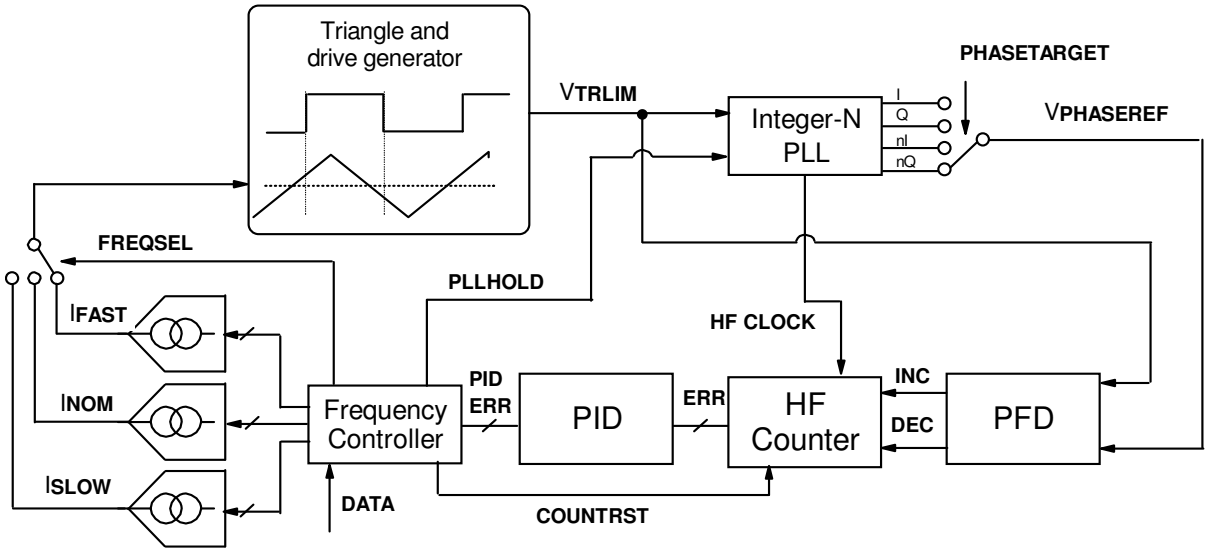

Figure 8-12: Mixed-signal system for shift frequency calibration, using high-frequency counter clocked by the phase-storage PLL, using integer-N synthesis

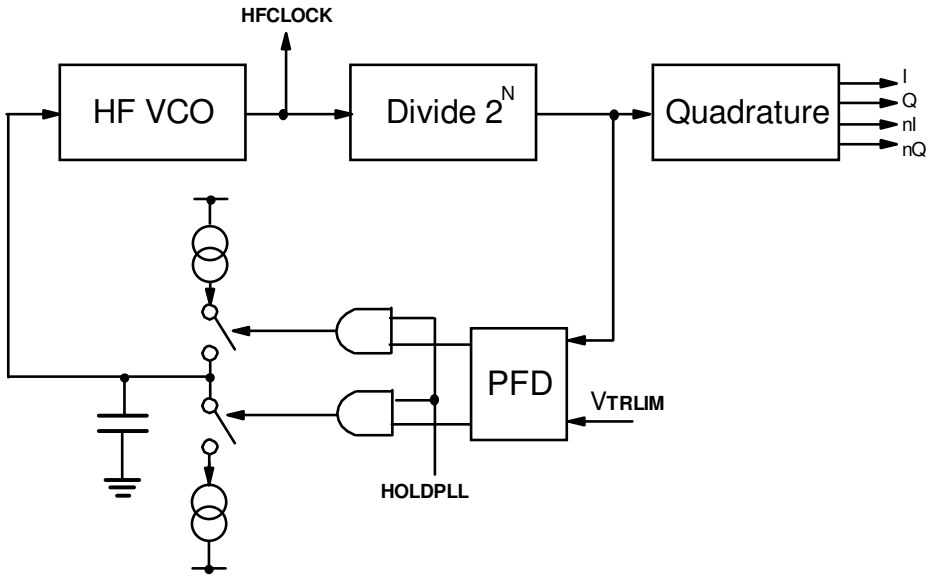

Figure 8-13: Integer-N PLL architecture for dual HF clock and quadrature phase reference generation

The mixed signal approach with a high-frequency counter and proportional control was chosen as the preferred method for frequency generation for PSK for this design. Integral and differential control were considered, however project time constraints prevented further development. Of all the solutions devised, it offered the best balance between rapid and consistent self-calibrating of the phase-shifting frequencies, and the need for creation of new circuit blocks in the available time and IC process.

8.3 Self-calibrating PSK architecture development

8.3.1 Summary of top-level requirements

The digital V-to-I triangle generator concept from the previous IC was re-used, as it was known to work and provide a sufficiently high frequency resolution for experimentation. Hence to reduce development time, it was desirable to re-use blocks from the first IC, subject to modifications in order to meet the new requirements.

The new system required additional currents for PSK modulation, both phase lead and phase lag. To avoid creating excessive phase error, a target of less than 1^O error was set, hence the current generation method must provide a sufficiently high resolution to meet this. The current integrator oscillator must be able to support the required PSK shift frequencies, as well as provide a seamless step between them at the correct moment.

The PLL for storing the phase must be able to accurately record the phase of the nominal frequency for at least the duration when the phase shift is taking place. It must be able to lock onto all possible nominal frequency settings of the main oscillator, hence requires a programmable loop filter.

The system must contain a state machine to control the PSK symbol transition (i.e. select the correct operating frequency according to a data control input). It must also control a phase error measurement block and determine if the PSK frequency requires adjustment.

8.3.2 Current Source

Since the triangle generator current is controlled digitally, there is a quantisation error between the ideal and achievable shifting frequency, creating a minimum phase angle error for PSK. The exact arrangement of the current sources for triangle generation is set by the error requirement of less than 1^O offset, hence expressions for phase offset in terms of current must be derived. Figure 8-14 shows how the phase angle error may be expressed as a delta time offset, ΔT_{lead} and ΔT_{lag} for positive and negative frequency offsets respectively.

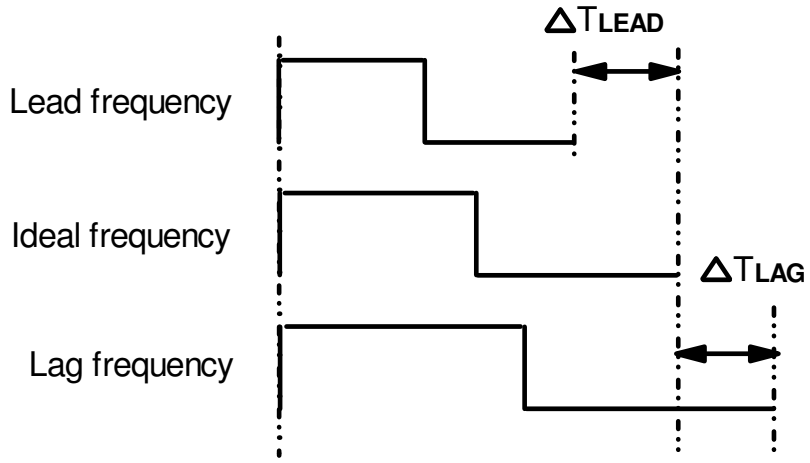

Figure 8-14: Lead and lag time durations caused by non-ideal shifting frequency current

For the triangle generation scheme used, the offsets ΔT_{lead} and ΔT_{lag} can be expressed in terms of currents as per equations 8.6 and 8.7 respectively (relative to the ideal current I_{ideal}). With the V-to-I architecture used, the largest current offset possible is equal to half a DAC code, i.e. equation 8.8. Hence the worst phase angle errors in terms of the available current range and resolution can be formulated in equations 8.9 and 8.10 respectively.

$$\Delta T_{lead} = \frac{2\ C\ dv}{I_{ideal}} - \frac{2\ C\ dv}{I_{lead}} \qquad (8.6)$$

$$\Delta T_{lag} = \frac{2\ C\ dv}{I_{lag}} - \frac{2\ C\ dv}{I_{ideal}} \quad (8.7)$$

$$\Delta I_{error} = \frac{I_{max} - I_{min}}{2^{N+1}} \quad (8.8)$$

$$\Delta\theta_{lead} = \frac{360\ \Delta T_{lead}}{T_{ideal}} = \frac{360\ (I_{lead} - I_{ideal})}{I_{ideal}} = \frac{360\ \Delta I_{error}}{I_{ideal}} = \frac{360\ (I_{max} - I_{min})}{2^{N+1}\ I_{ideal}} \quad (8.9)$$

$$\Delta\theta_{lag} = \frac{360\ \Delta T_{lag}}{T_{ideal}} = \frac{360\ (I_{ideal} - I_{lag})}{I_{ideal}} = \frac{360\ \Delta I_{error}}{I_{ideal}} = \frac{360\ (I_{max} - I_{min})}{2^{N+1}\ I_{ideal}} \quad (8.10)$$

Hence, the worst phase error per cycle will occur at the bottom of the tuning range, i.e. $I_{ideal} = I_{min}$. Re-using the previous architecture with I_{min} = 25µA, I_{max} = 50µA and N = 8, the worst phase error is approximately 0.703^{O}/cycle. If the number of cycles is increased, this error accumulates. For example, a target 90^{O} shift over 16 cycles could accumulate up to 11.2^{O} of lead or lag, which significantly exceeds the target error threshold.

In order to reduce this error, the fast and slow frequencies were not generated directly, rather from copies of the nominal frequency current with some current added or subtracted respectively, as per figure 8-15. This approach concentrates the available resolution of the 8-bit DACs to the region where it needed, i.e. purely for creating a phase lead or lag, hence a smaller frequency step is available for phase shifting and the error/cycle is reduced. Given the known requirements for maximum and minimum phase shift per cycle, the fast and slow shift currents can be calculated as per equations 8.11 and 8.12 respectively. The current DACs for the fast and slow current contributions can be programmable, set according to the required amount of phase shift per cycle (i.e. a larger amount of phase shift requires more current to be added or subtracted from the nominal current).

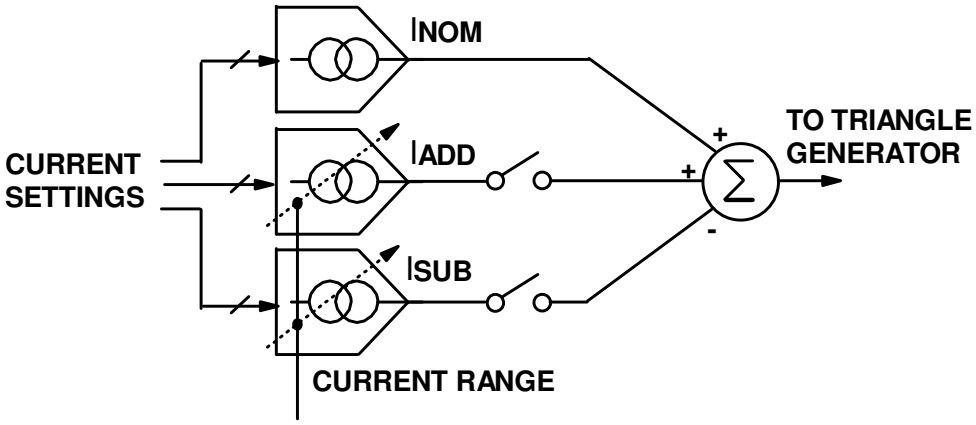

Figure 8-15: Current summation concept for improved frequency resolution

$$I_{fast} = \frac{720\ C\ dv}{360 - \theta_{cycle}} \quad (8.11)$$

$$I_{slow} = \frac{720\ C\ dv}{360 + \theta_{cycle}} \quad (8.12)$$

Tables 8-2 and 8-3 show the required current ranges for the additive and subtractive currents for fast and slow frequencies, , I_{ADD} and I_{SUB} respectively. These are calculated with the assumption of a 25µA - 50µA nominal current range. Whilst it had been earlier shown that 90^{O}/cycle phase shift was not practical for operation due to the limited antenna tuning range, it was included in the frequency generator to permit easier demonstration of the ideal phase shift behaviour in the time domain.

Simulation of the available resistors across IC process and temperature corners revealed a variation of ±13% in the resistance value from nominal. To allow for this variation and mismatch in the current mirror array, a ±20% margin was added to maximum and minimum theoretical currents, sacrificing some of the resolution improvement in order to ensure correct functionality. The tables also provide a comparison of the accuracy improvements, which get better as the phase shift per cycle gets smaller due to increasing focus of the available tuning resolution.

Phase Shift per Cycle (degrees)		90	45	22.5	11.25	5.625
Period Ratio		0.75	0.875	0.9375	0.96875	0.984375
Current Fraction		1/3	1/7	1/15	1/31	1/63
I_{ADD} Currents (μA)	I_{max}	16.7	7.14	3.33	1.61	0.794
	I_{min}	8.33	3.57	1.67	0.807	0.397
± 20% Margin (μA)	I_{max}	20.0	8.57	4.00	1.94	0.952
	I_{min}	6.67	2.86	1.33	0.645	0.317
I_{ADD} Current Resolution (nA)		52.1	22.3	10.4	5.04	2.48
Nominal Current Resolution (nA)		97.7				
Improvement Factor		1.86	4.38	9.38	19.4	39.4
Max Phase Error per Cycle (degrees)		0.375	0.161	0.0750	0.0363	0.0179

Table 8-2: Table of fast current ranges and phase errors for phase lead, using resolution focussing architecture

Phase Shift per Cycle (degrees)		90	45	22.5	11.25	5.625
Period Ratio		1.25	1.125	1.0625	1.03125	1.015625
Current Fraction		1/5	1/9	1/17	1/33	1/65
I_{SUB} Currents (μA)	I_{max}	10.0	5.56	2.94	1.52	0.769
	I_{min}	5.00	2.78	1.47	0.758	0.385
± 20% Margin (μA)	I_{max}	12.0	6.67	3.53	1.82	0.923
	I_{min}	4.00	2.22	1.18	0.606	0.308
I_{SUB} Current Resolution (nA)		31.3	17.4	9.19	4.73	2.40
Nominal Current Resolution (nA)		97.7				
Improvement Factor		3.13	5.63	10.6	20.6	40.6
Max Phase Error per Cycle (degrees)		0.225	0.125	0.0662	0.0341	0.0173

Table 8-3: Table of slow current ranges and phase errors for phase lag, using resolution focussing architecture

Figures 8-16 and 8-17 show the circuits used for the slow and fast current contributions. Given the large range of currents required, a current mirror with a programmable ratio was used to ensure that the mirror remained saturated across the entire operating range. Between each phase angle range, the current changes by approximately a factor of 2, hence 2^N integer ratios were used to facilitate good matching in layout. The branches are additive, such that more branches are switched in when more current is required for a greater amount of phase shift per cycle.

The factor between each current fraction is not exactly 2 (i.e. decreasing through 1/5, 1/9, 1/17, etc. for the slow current contribution), hence the V-to-I resistor must also be varied in order to create the exact current required. The NMOS-switch voltage DAC from the first design was re-used to reduce design time, hence the V-to-I voltage is constrained to be 2.5V or less. Tables 8-2 and 8-3 show the steps used to calculate the resistors based upon the required current in each range. To obtain the correct signs, I_{SUB} is created with a PMOS mirror and I_{ADD} is created with an NMOS mirror. Each current is directly

combined with a copies of the nominal current, created in a similar manner to the first design as per figure 8-18.

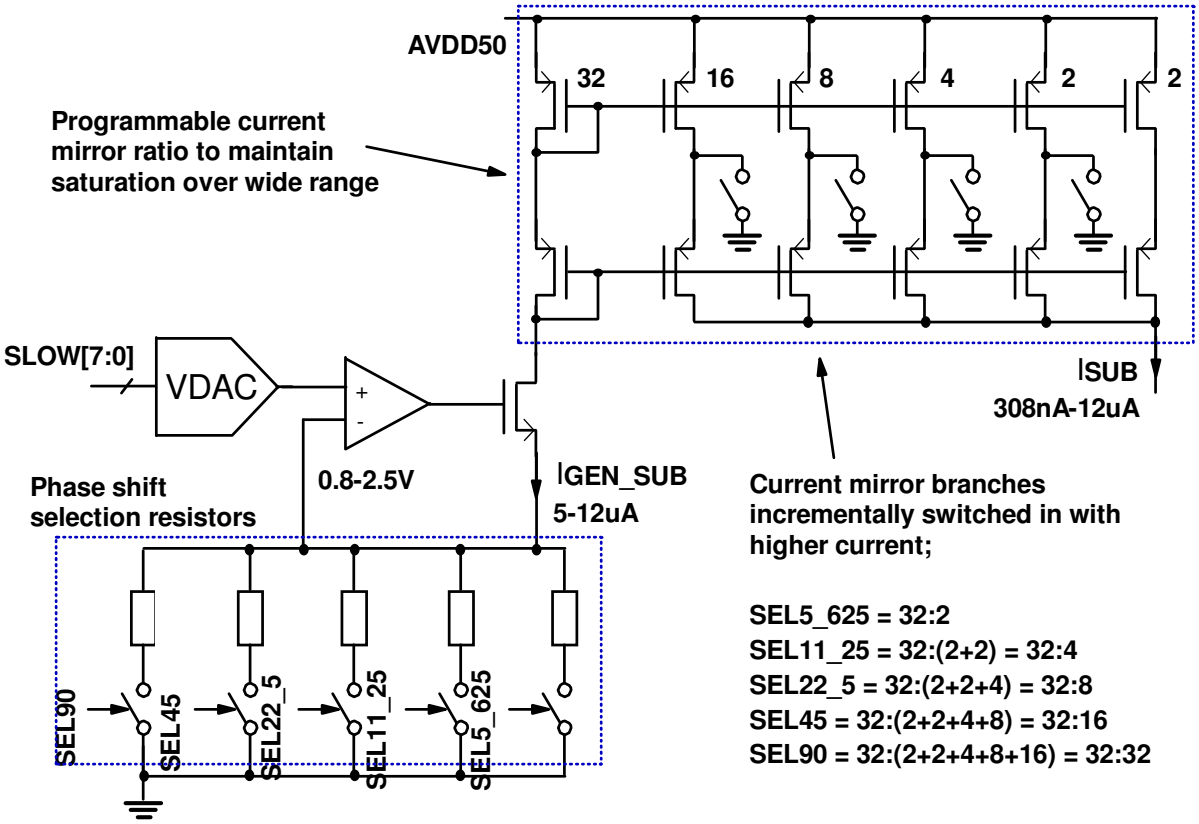

Figure 8-16: I_{SUB} current generation circuit with programmable range for varying phase shift angles

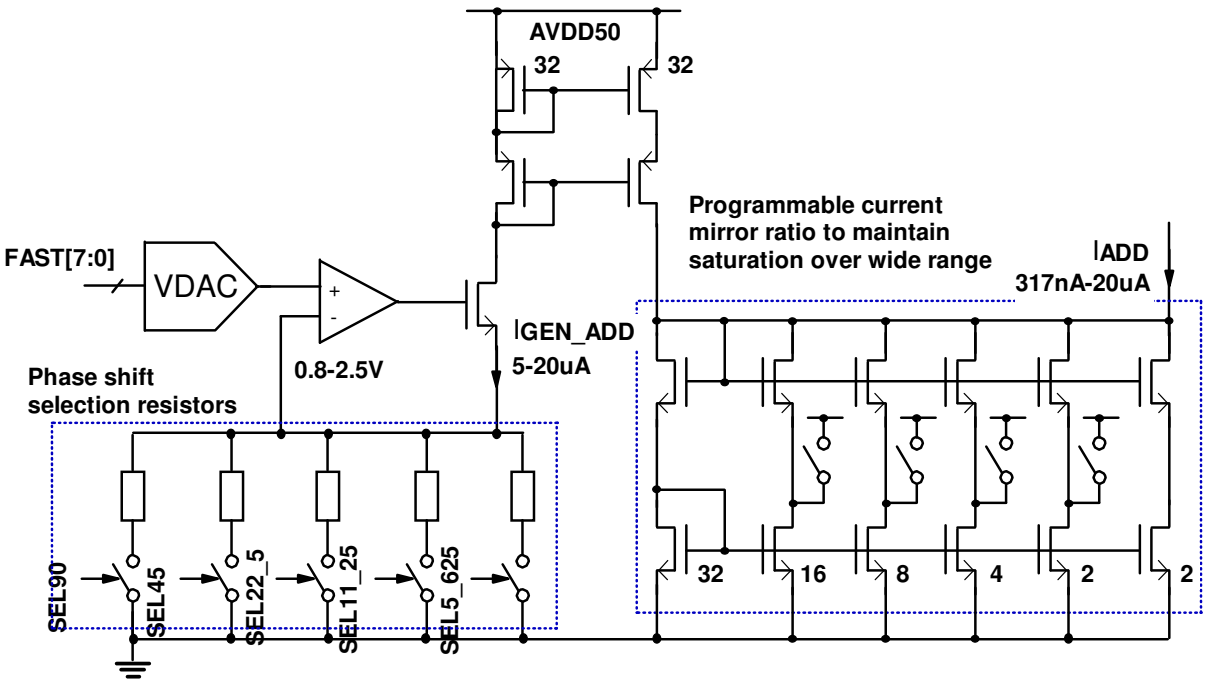

Figure 8-17: I_{ADD} current generation circuit with programmable range for varying phase shift angles

Phase Shift per Cycle (degrees)		90	45	22.5	11.25	5.625
I_{ADD} Currents (µA)	I_{max}	20.0	8.57	4.00	1.94	0.952
	I_{min}	6.67	2.86	1.33	0.645	0.317
Current mirror ratio		1	2	4	8	16
Scaled Currents (µA)	I_{max}	20.0	17.1	16.0	15.5	15.2
	I_{min}	6.67	5.71	5.33	5.16	5.08
Required DAC output (V)	V_{max}	2.50	2.50	2.50	2.50	2.50
	V_{min}	0.83	0.83	0.83	0.83	0.83
Required resistance (kΩ)		125	146	156	161	164

Table 8-4: Table of calculation for I_{ADD} current V-to-I parameters

Phase Shift per Cycle (degrees)		90	45	22.5	11.25	5.625
I_{SUB} Currents (µA)	I_{max}	12.0	6.67	3.53	1.82	0.923
	I_{min}	4.00	2.22	1.18	0.606	0.308
Current mirror ratio		1	2	4	8	16
Scaled Currents (µA)	I_{max}	12.0	13.3	14.1	14.5	14.8
	I_{min}	4.00	4.44	4.71	4.85	4.92
Required DAC output (V)	V_{max}	2.50	2.50	2.50	2.50	2.50
	V_{min}	0.83	0.83	0.83	0.83	0.83
Required resistance (kΩ)		208	188	177	172	169

Table 8-5: Table of calculation for I_{SUB} current V-to-I parameters

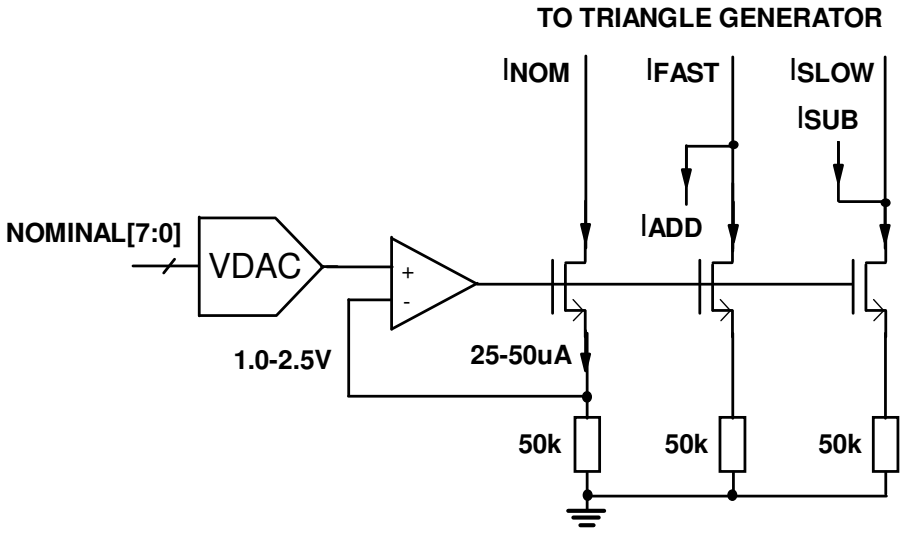

Figure 8-18: Nominal current generation and summation with I_{ADD} and I_{SUB} parts

8.3.3 Up/Down Current Mirror

An up/down current mirror was required to produce a symmetrical square wave current for triangle generation. To reduce design time, the up/down current mirror from the first design was re-used, since the nominal current range was the same (25µA – 50µA).

An important difference was the additional requirement for rapid changes in the DC value of the current whenever the operating frequency is switched. To avoid creating a gradual frequency shift, rather than instantaneous frequency step, a change in the DC input to the mirror should take no longer than 1% of the cycle duration at maximum frequency.

Simulation revealed that the previous design was far too slow to meet this requirement, as show in figure 8-19. With a step from 38-50µA DC current input, the circuit takes approximately 90ns to settle to within 1% of the final value under nominal conditions. This is equivalent to 18% of a cycle at 2MHz, creating an undesirable gradual frequency shift.

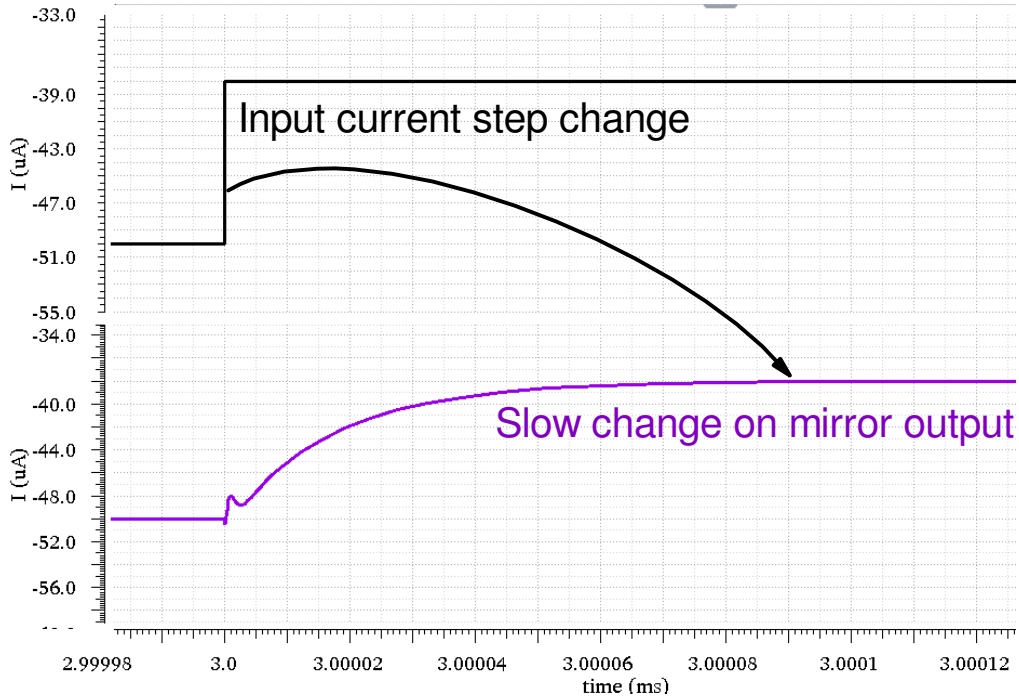

Figure 8-19: Current mirror output response to step input change from 50µA to 38µA

In order to speed up the transitions, three identical up/down mirrors were multiplexed for the slow, nominal and fast currents, using transmission gate switches to select the required current, as show in figure 8-20. When not in use for triangle generation, the unused up/down mirror is connected to a buffered 2.5V reference to maintain saturation, allowing for a very rapid transition.

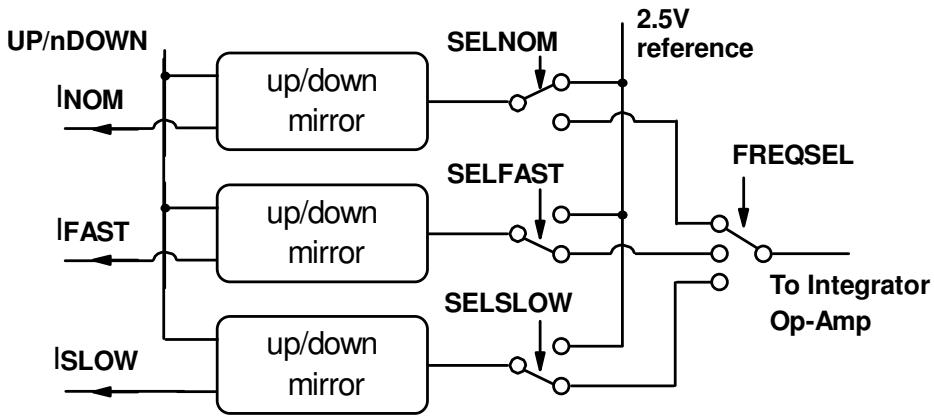

Figure 8-20: Improved architecture for faster current switching

Using this method, the worst case settling time in the current across PVT corners was reduced to approximately 4.5ns, or 0.9% of a cycle at 2MHz. The disadvantage of this approach is the increased power consumption and die area, approximately three times greater given the need for three sets of mirrors. This compromise was necessary to achieve correct functionality in the available design time. Copies of the nominal, fast and slow currents were provided for the analogue test bus. These were not required to be exact copies of the current, only indicative of the approximate values to permit

observation of the frequency calibration operation. Hence they were included around the edges of the up/down current mirrors and would not be as well matched.

8.3.4 Integrator Op-Amp

The triangle generator integrator op-amp from the first IC was also re-used as the triangle voltage swing and DC current were largely unchanged. The target operating frequency range was wider, i.e. the lowest frequency of operation was lower. This required the calculation of additional integration capacitance and also re-simulating the op-amp to check stability at the lower frequencies.

Table 8-6 shows the frequency bands, with the additional lower frequencies at 104kHz and below. The max:min ratio in each band is maintained the same as previously, in order to meet the requirement of tuning to within 3dB of an LC tank with a Q factor of 50, i.e. 8 bits of resolution required from the V-to-I DAC.

F_{MAX}	F_{MIN}	$C_{integration}$	ΔC	Minimum bandwidth (Q = 50)	Resolution
2.00MHz	1.00MHz	4.17pF	4.17pF	20.0kHz	4.00kHz
1.50MHz	750kHz	5.56pF	1.39pF	15.0kHz	3.00kHz
1.13MHz	563kHz	7.41pF	1.85pF	11.3kHz	2.25kHz
844kHz	422kHz	9.88pF	2.47pF	8.44kHz	1.69kHz
633kHz	316kHz	13.2pF	3.29pF	6.33kHz	1.27kHz
475kHz	237kHz	17.6pF	4.39pF	4.75kHz	949Hz
356kHz	178kHz	23.4pF	5.85pF	3.56kHz	712Hz
267kHz	133kHz	31.2pF	7.80pF	2.67kHz	534Hz
200kHz	100kHz	41.6pF	10.4pF	2.00kHz	400Hz
150kHz	75.1kHz	55.5pF	13.9pF	1.50kHz	300Hz
104kHz	52kHz	80.1pF	24.6pF	1.04kHz	208Hz
72kHz	36kHz	116pF	35.6pF	720Hz	144Hz
49.9kHz	24.9kHz	167pF	51.4pF	499Hz	99.7Hz
34.5kHz	17.3kHz	241pF	74.2pF	345Hz	69.1Hz
23.9kHz	12kHz	348pF	107pF	239Hz	47.8Hz
16.6kHz	8.28kHz	503pF	155pF	166Hz	33.1Hz

Table 8-6: Triangle generator frequency bands for second IC

For the additional frequency bands, the integration capacitance required becomes large, forcing re-consideration of the on-chip area requirements. To total integration capacitance has increased by a factor of approximately 9, hence approximately 9 times the area of that used by the first design is required (i.e. the area use increases from 52500μm^2 to 472500 μm^2). Given the additional system architecture and area budget, it was decided to provide an external connection for the required extra integration capacitance in parallel with the internal capacitors, as per figure 8-21. Additionally, a switch was included so that an off-chip triangle wave may be generated and inserted directly into the IC for debug purposes. The stability considerations of the increased frequency range are covered in appendix G.

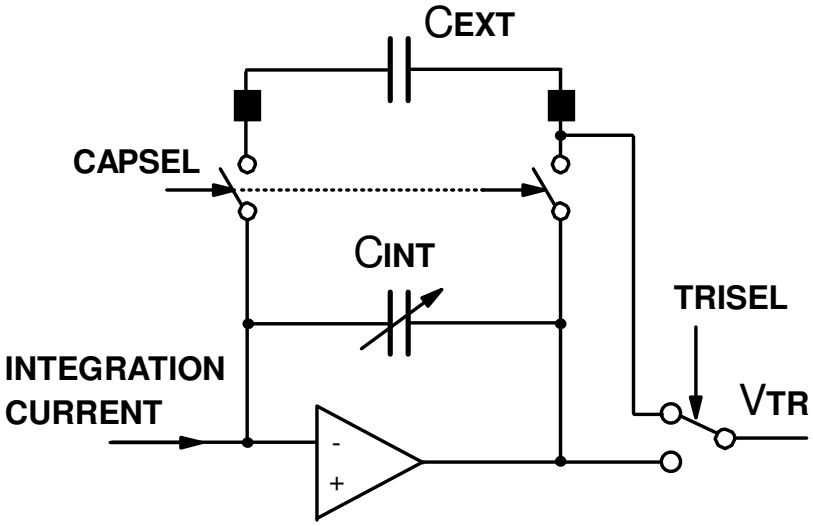

Figure 8-21: Current integrator architecture with optional off-chip capacitance select

8.3.5 Triangle Comparators

The previous comparator design was readily available for use. Since the core operating frequency had not increased, it was easy to re-use the previous design. An additional comparator was needed to detect mid-point crossings of the triangle wave, so that the control FSM can change the operating frequency synchronously with the oscillation in the external LC tank and maintain phase continuity.

For correct system functionality, it was important that the detection of the mid-point crossing was accurate and did not experience false triggering. Otherwise, the control FSM may follow an incorrect sequence. Simulation with behavioural current sources into the integrator op-amp revealed that the triangle wave can become discontinuous when the current is switched, which presented a risk of glitching on the output of the mid-point detection comparator. Figure 8-22 shows the problem observed in simulation using a behavioural comparator.

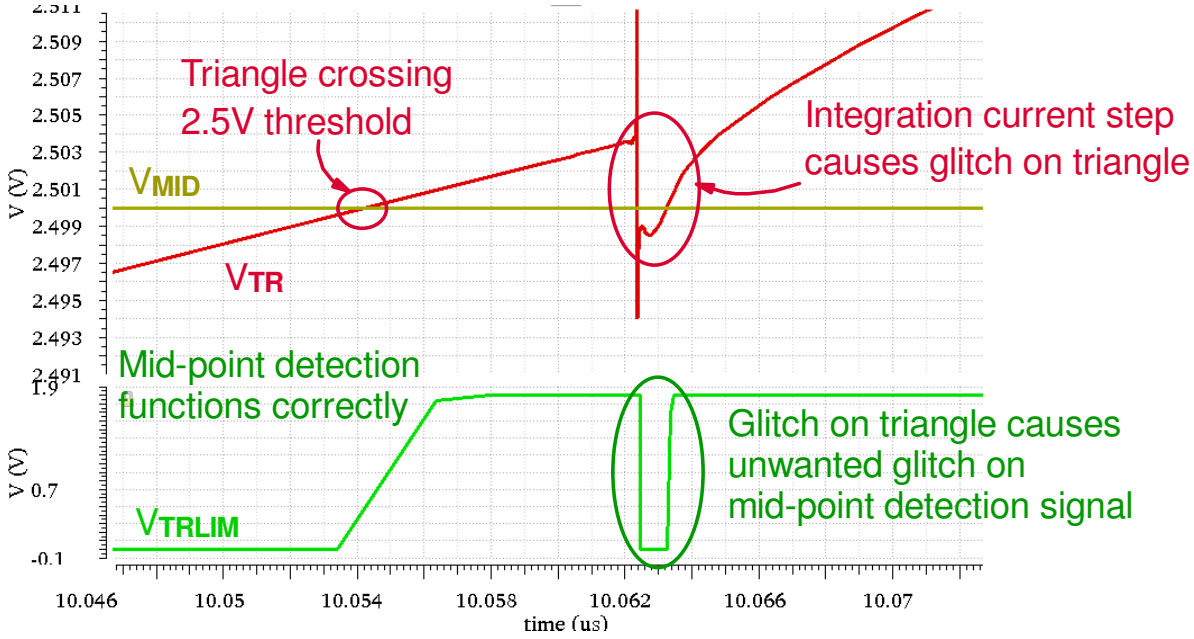

Figure 8-22: Glitching behaviour of V_{TR} when ideal input current is stepped, causing a glitch on V_{TRLIM}

To mitigate this problem, a de-glitch circuit was added to the output of the comparator as per figure 8-23, which shows the top level of the triangle comparator block in the oscillator. An RS latch is set

and reset by the comparator output and complement thereof. This is ANDed with the up/down signals for high/low detection respectively, meaning that the latch cannot be reset until the triangle wave has changed direction. Therefore, if the comparator output experiences a glitch, this will not cause V_{TRLIM} to glitch. Figure 8-24 shows the circuit operating correctly, preventing V_{TRLIM} from glitching erratically, despite the presence of kick-back on V_{TR} causing multiple activations of V_{TRHIGH}.

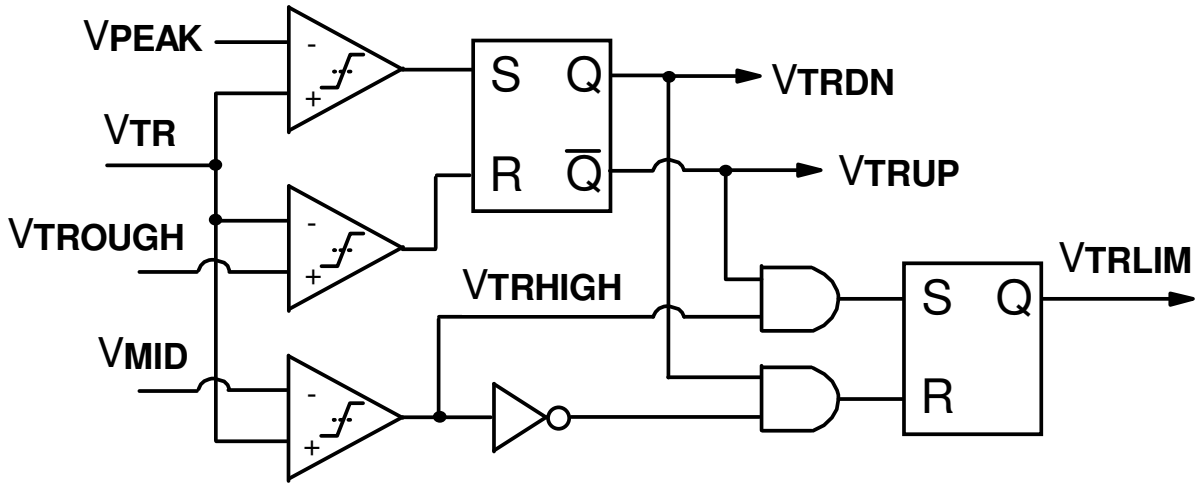

Figure 8-23: Triangle comparator with de-glitch circuit for V_{TRLIM}

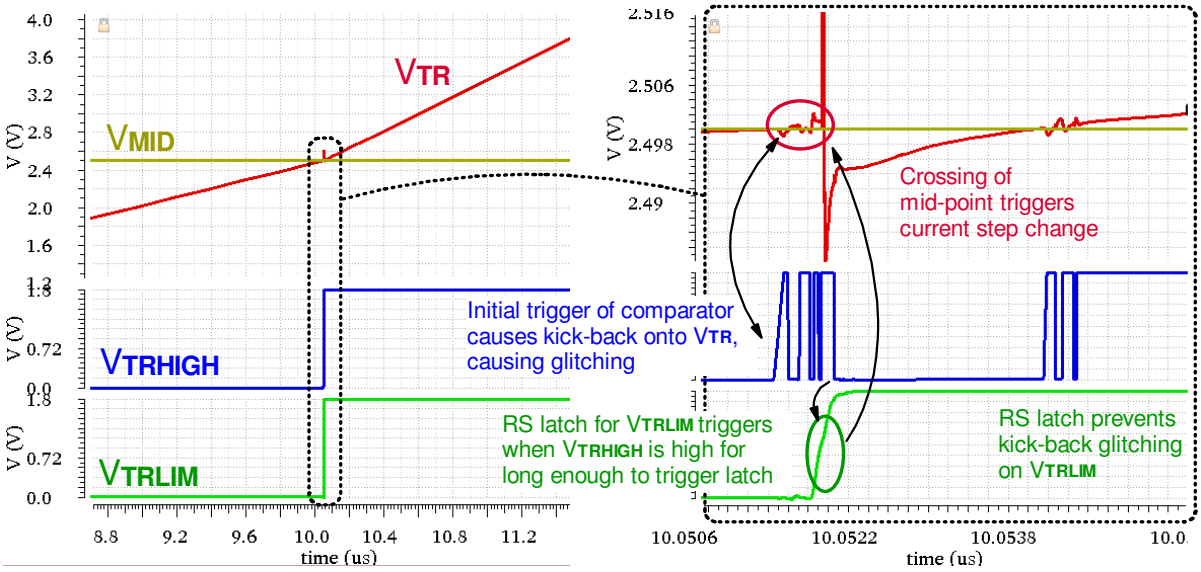

Figure 8-24: Triangle comparator de-glitch operation

8.3.6 Phase-Locked Loop

A PLL was created to store a reference phase whilst the external LC tank phase shift occurs. A type II PLL was used for lower steady-state ripple when compared to a type I PLL, as the type II operates as a tristate system (i.e. increase frequency, hold frequency, decrease frequency), so the VCO input is more stable. More importantly, it also has zero residual phase error when locked, which is necessary to provide a correct phase reference to calibrate the phase shifting frequencies.

8.3.6.1 Phase-Frequency Detector

A conventional PFD structure was used, using the available 1.8V logic cells. To ensure that the D-type flipflops were properly reset, a pulse-widener circuit was used, implemented with an RS latch and simple RC delay line as per figure 8-25. When both flipflop outputs *PUMPUP* and *PUMPDN* are high, the RS latch is triggered. The flipflops are reset by *FFRST*, causing *PUMPUP* and *PUMPDN* to go low, clearing the S input to the latch. At the same time, *FFRST* is fed through a buffered RC delay line to

the reset input *LATCHCLR*. After the propagation delay of the delay line, *LATCHCLR* triggers, causing the RS latch to be reset and de-asserting *FFRST*. This ensures that the reset event to the flipflops occurs quickly (longest delay on PVT corners 1.37ns) whilst the hold time on the reset is widened (9.63ns shortest on PVT corners). Figure 8-26 shows a simulation of the widener circuit in operation.

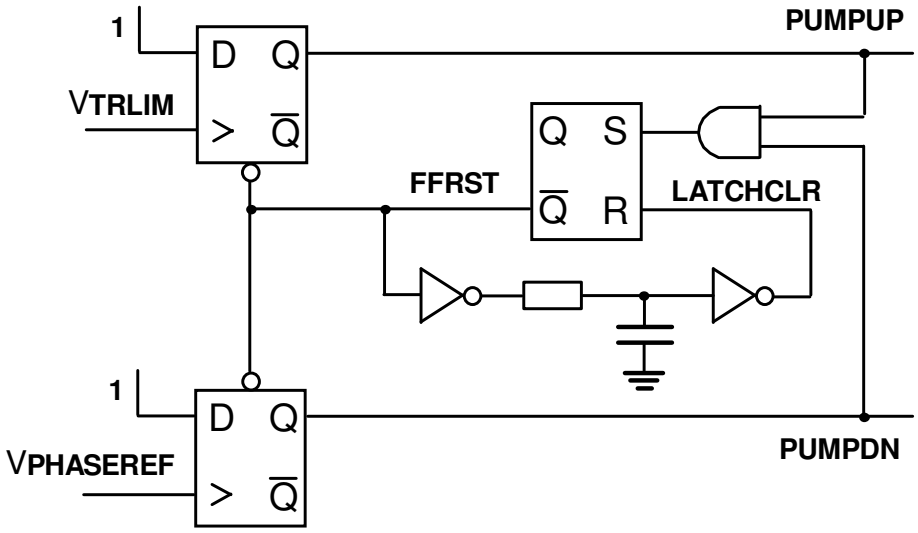

Figure 8-25: PLL PFD with reset pulse widener

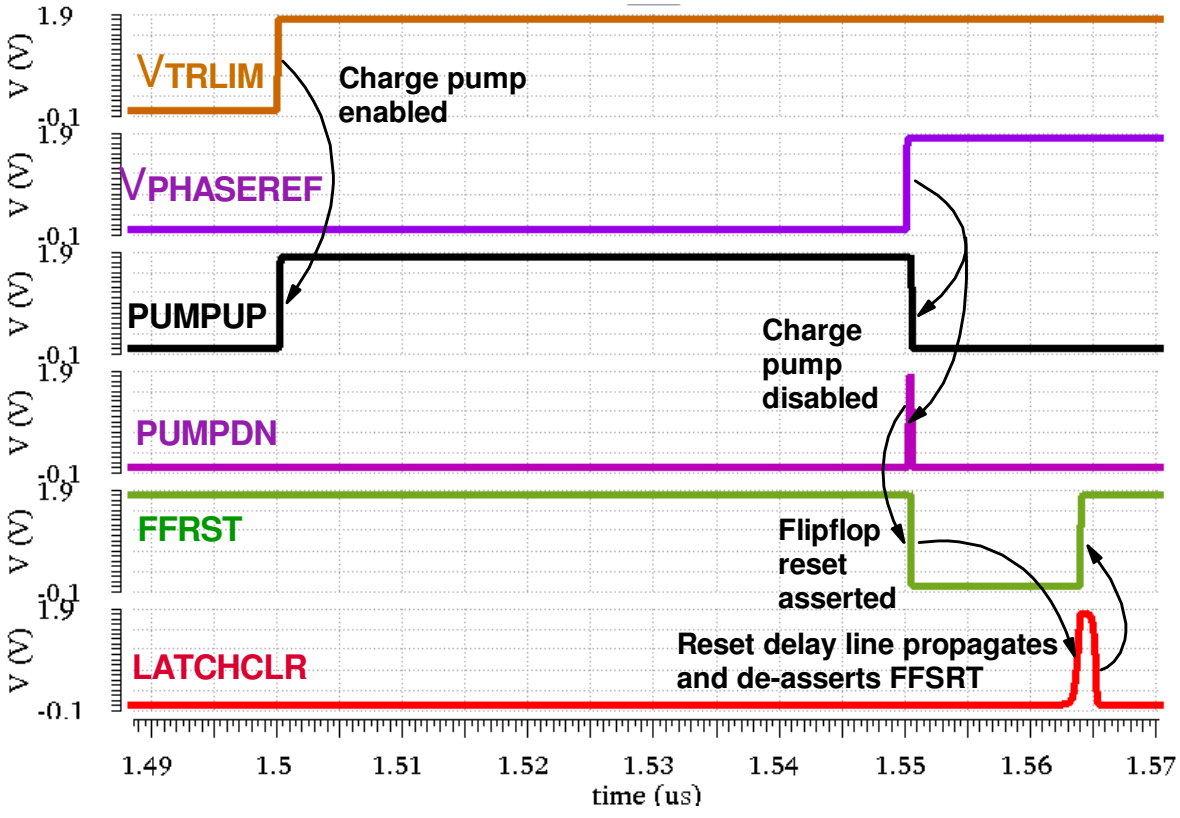

Figure 8-26: Simulation of PLL PFD pulse widener operation

Both outputs of the PFD flipflops were connected to the charge pump for the PLL. At the moment the PFD resets, both charge pump switches are briefly connected, causing an undesirable voltage change on the PLL capacitor. To prevent this, additional logic in figure 8-27 was used to prevent both switches from being activated (*PUMPP* and *PUMPN* control the PMOS and NMOS switches on the charge pump respectively, hence the *PUMPP* function requires a NAND gate). When one switch is activated, an

AND function prevents the other from becoming active until after the PFD has been reset. In addition, a pair of AND gates are provided to allow the charge pump functionality to be disabled whilst *HOLDPLL* is asserted. Figure 8-28 shows simulation of the desired behaviour, for an example where the *PUMPP* function is triggered first. In the event that *PUMPUP* and *PUMPDN* arrive at the exact same moment, both *PUMPP* and *PUMPN* will briefly activate for at least the duration of an inverter propagation delay (i.e. less than 1ns at nominal PVT). This is less than the propagation delay of the 5V levelshifters connected to *PUMPP* and *PUMPN*, so temporary activation of the charge pump FETs is still prevented.

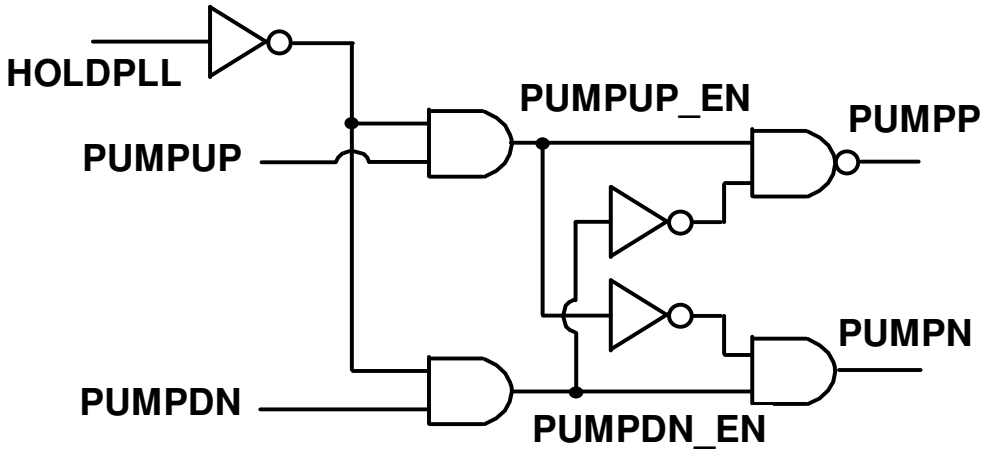

Figure 8-27: PLL PFD glitch prevention on charge pump

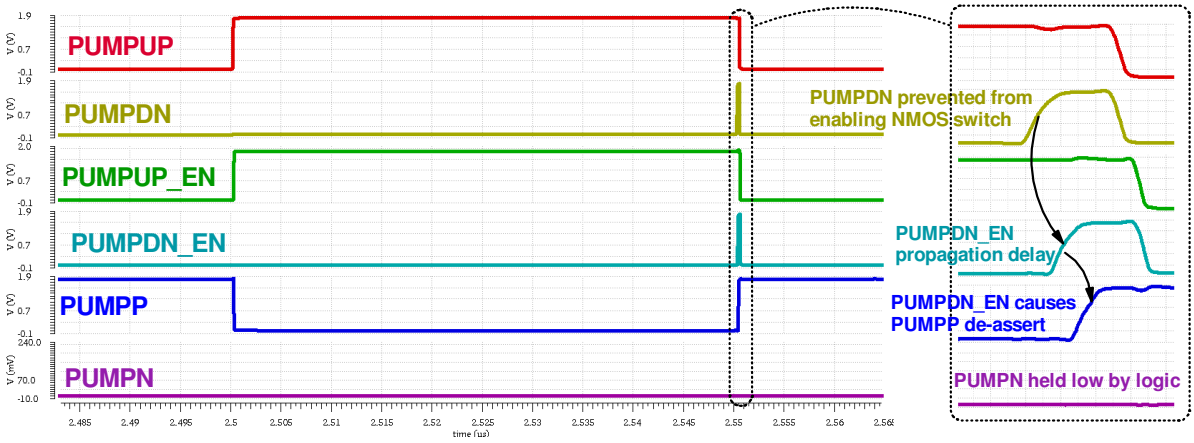

Figure 8-28: Simulation of PLL PFD de-glitch prevention on charge pump

8.3.6.2 High Frequency Oscillator

The PLL VCO has two primary functions. The first is to accurately store the phase of the nominal carrier frequency, to allow for comparison after a PSK symbol has been transmitted. The second function is to provide a high frequency clock for error measurement between the stored phase and target phase. For this reason, the VCO was designed with a high frequency core and frequency-divided output, as per figure 8-29.

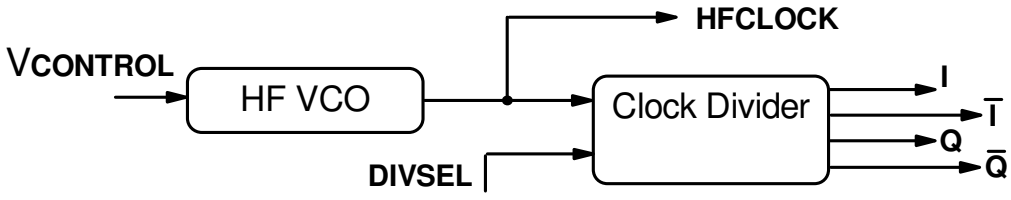

Figure 8-29: VCO block diagram

To improve the error measurement accuracy, the VCO core should operate at the highest frequency possible. In practice, it is limited by the propagation delay of the phase error measurement circuit. From simulation, this was 1.39ns on the slowest PVT corner, i.e. a frequency of approximately 720MHz could be theoretically tolerated. To allow a safety margin to prevent incorrect operation in case of PVT skew, the target maximum frequency for the VCO core was 500MHz.

To reduce sensitivity to noise on the input, the target linear max:min frequency range was set to be approximately 3:1. This is a large enough range to allow all operating frequency bands to be covered (i.e. better than a 2:1 range), however it is kept constrained to reduce sensitivity to noise at the input.

To achieve the high speed required, the VCO core was implemented as a ring oscillator in 1.8V devices, with a diode clamp included to protect them from accidental overvoltage if the current mirror provides too much current. Deep N-Well NMOS devices were used to reduce noise injection into the substrate. For a good voltage-frequency linear relationship, a current-fed design was used (figure 8-30). The constructed ring-oscillator had an internal supply voltage ranging from 0.5-1.1V, hence a levelshifter was required to permit correct operation with logic devices on the output. The levelshifter also provides buffering to isolate the core oscillator from capacitive loading, which would reduce its operating frequency.

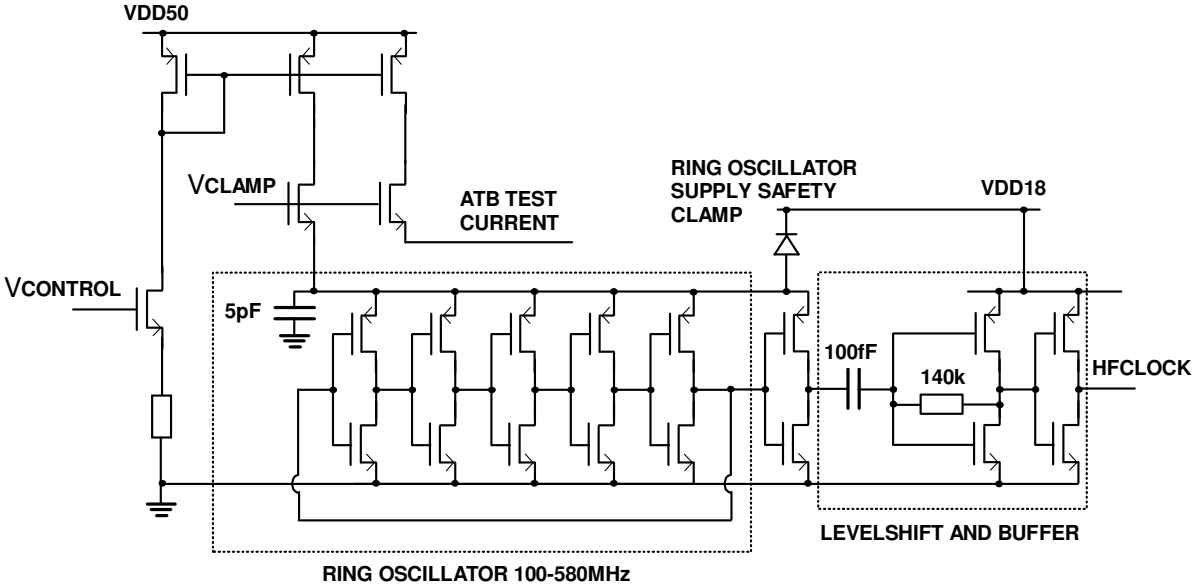

Figure 8-30: PLL core oscillator circuit

A capacitively-coupled inverter with resistor feedback was used to buffer and levelshift the oscillator output. The input capacitor forms a capacitive divider with the C_{GS} of the output inverters, so it must be large enough to avoid excessive division of the oscillator voltage and prevent the inverter from switching. Simulation revealed that as little as 10fF was sufficient for operation up to 500MHz on the worst PVT corner with the minimum oscillator core voltage of 0.5V, so a 100fF capacitor was used to provide a safety margin.

The core VCO frequency was divided down with a chain of D-type flipflops, with a programmable divider ratio as per figure 8-31 to allow operation over the wide range required. The selected output is then fed into a quadrature generator to create the target reference phases for self-calibration of the shifting frequencies for PSK.

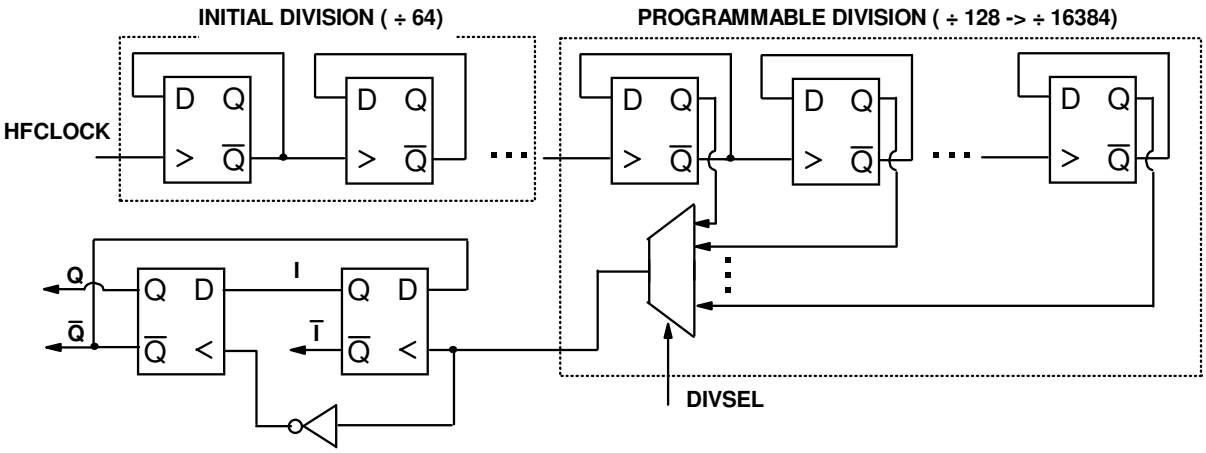

Figure 8-31: PLL frequency divider circuit

Figure 8-32 shows the operating voltage-frequency behaviour from post-layout simulation on nominal, slowest and fastest PVT corners. For all three cases, the voltage-frequency relationship is approximately linear between 1.5-4.5V, giving frequency-voltage gradient K_{VCO} values of approximately 79.7MHz/V, 66.4MHz/V and 97.5MHz/V for nominal, slow and fast corners respectively.

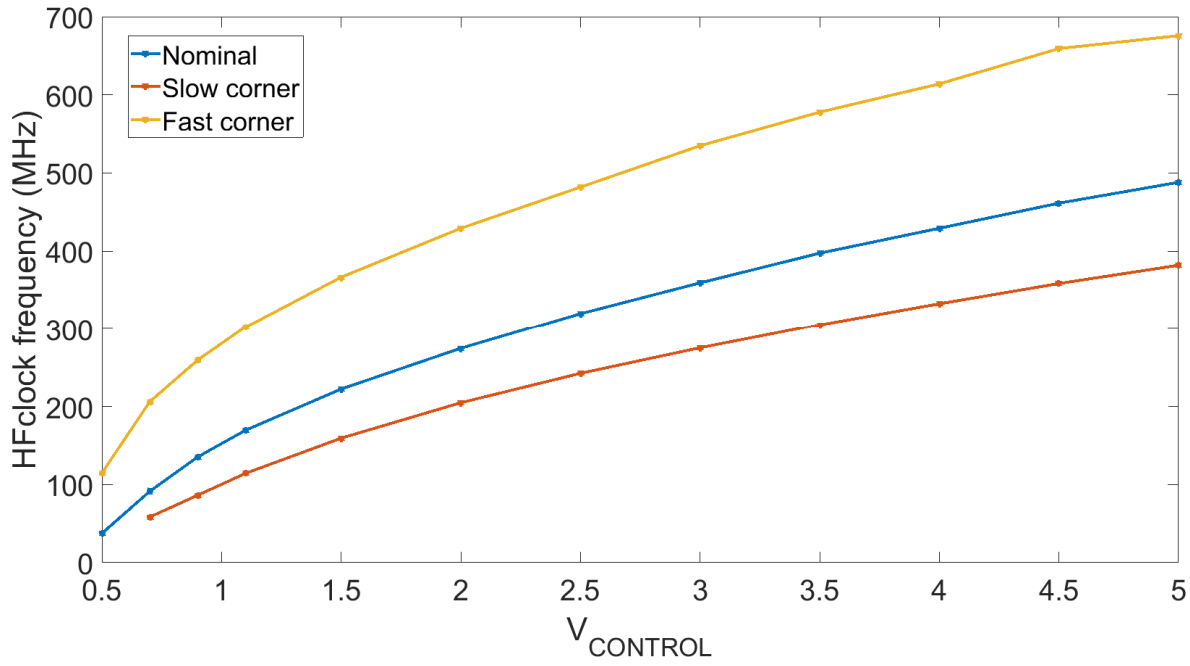

Figure 8-32: PLL VCO voltage-frequency curve on nominal, slow and fast PVT corners

8.3.6.3 Charge Pump and Filter Design

The settling time of the PLL is determined by the charge pump current, filter response and operating frequency. Hence, some programmability is required to allow for an optimal settling time across the operating frequency range. Equations 8.13 and 8.14 give the natural frequency ω_n and damping coefficient ζ in terms of K_{VCO}, charge pump current I, divider ratio M and filter parameters R_p and C_p. [47]. Also given in equation 8.15 is the PLL loop bandwidth ω_{-3dB}, which determines the maximum frequency at which the PLL will operate to track the input frequency; a higher loop bandwidth means the PLL will lock faster, however a lower loop bandwidth will mean less jitter when it is locked, so to compromise ω_{-3dB} can be set to be approximately one tenth of the input operating frequency [47]. With critical damping, i.e. $\zeta = 1$, this means that ω_n should be approximately 1/25 of the input frequency.

$$\omega_n = \sqrt{\frac{I_P\, K_{VCO}}{2\pi\, C_p\, M}} \tag{8.13}$$

$$\zeta = \frac{R_p}{2}\sqrt{\frac{I_P\, C_p\, K_{VCO}}{2\pi\, M}} \tag{8.14}$$

$$\omega_{-3dB} = \omega_n \sqrt{(2\zeta^2 + 1) + \sqrt{(2\zeta^2 + 1)^2 + 1}} \tag{8.15}$$

Ideally, the charge pump current should be as small as possible, both for conserving power and to allow for the smallest capacitors possible. On the other hand, a current which is too small may experience greater influence from noise and interference. Furthermore, generating a small current from a larger fixed input bias requires a large current mirror ratio, which may consume excessive area. Hence the nominal charge pump current was chosen to be in the range of 10-20μA, easily derived from the nominal system bias current. At 2MHz (obtained where M = 256), the required $\omega_n = 503\text{krads}^{-1}$, hence a capacitor of approximately 2.26pF is required with 10μA of current, an acceptable value for realisation.

To avoid reduce variation of the capacitance due to random offset, a minimum capacitance of 10pF was chosen. To allow for experimental trimming of the loop bandwidth and damping coefficient, the current mirror ratio was made programmable for currents of 5μA, 10μA, 15μA and 20μA. The pump was constructed with 5V devices to reduce leakage (when compared to the available 1.8V devices) and to allow for a larger input voltage range to the VCO to reduce sensitivity to noise. To maintain both the up and down devices in saturation, a buffered copy of the VCO input voltage was created to power the unused part of the charge pump, as per figure 8-33.

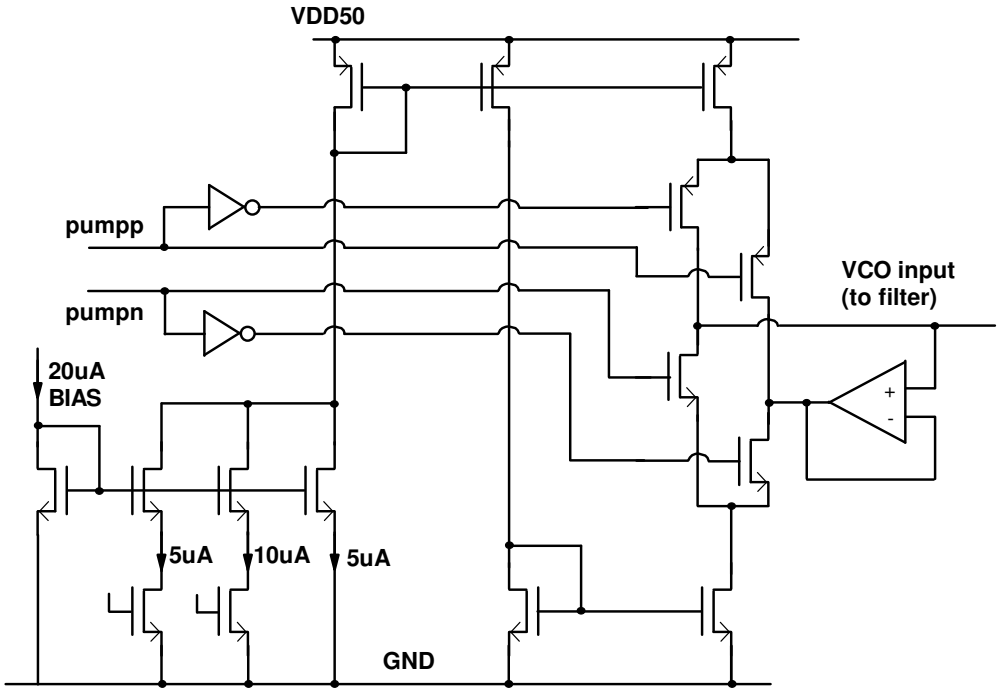

Figure 8-33: PLL charge steering pump with programmable DC current

With a 10pF set minimum capacitance, the required capacitance doubles between each band, as shown in table 8-7. In the most extreme case of a fast corner K_{vco} and maximum charge pump current, the required value of R for critical damping was found to be approximately 400kΩ. To avoid the need for multiple transmission gate switches, the resistor was not made programmable.

For the 350kHz frequency region and below, it was not practical to include a capacitor of the required size in the available space on-chip, hence an external connection for an off-chip capacitor was required. Note that the VCO input node is high impedance so the off-chip connection was isolated with a T-switch to reduce the effect of leakage or injected noise interfering with the operation of the PLL.

F_{Max}	C_1 (on-chip)	C_1 (off-chip)	C_2	R	ω_n	ζ
2.00MHz	10pF	0pF	2pF	400kΩ	338 krads^{-1}	0.676
1MHz	20pF	0pF	4pF	400kΩ	169 krads^{-1}	0.676
500kHz	40pF	0pF	8pF	400kΩ	84.6 krads^{-1}	0.676
250kHz	80pF	0pF	16pF	400kΩ	42.3 krads^{-1}	0.676
125kHz	160pF	0pF	32pF	400kΩ	21.1 krads^{-1}	0.676
62.5kHz	320pF	0pF	64pF	400kΩ	10.6 krads^{-1}	0.676
31.3kHz	320pF	320pF	64pF	400kΩ	5.28 krads^{-1}	0.676
15.7kHz	320pF	960pF	64pF	400kΩ	2.64 krads^{-1}	0.676

Table 8-7: PLL filter capacitor selection for different operating ranges (charge pump current 10µA)

In addition, a small capacitor C_2 was connected in parallel with the RC filter in order to reduce the effect of charge injection on the VCO input, thereby reducing the jitter. Doing so added an additional pole to the PLL loop response, so it was necessary to keep this extra capacitance small relative to C_p. Setting C_i to be between 1/10 and 1/5 of the value of C_p keeps the poles space sufficiently far apart so as to prevent instability, so a ratio of 1/5 was used to minimise the effects of charge injection.

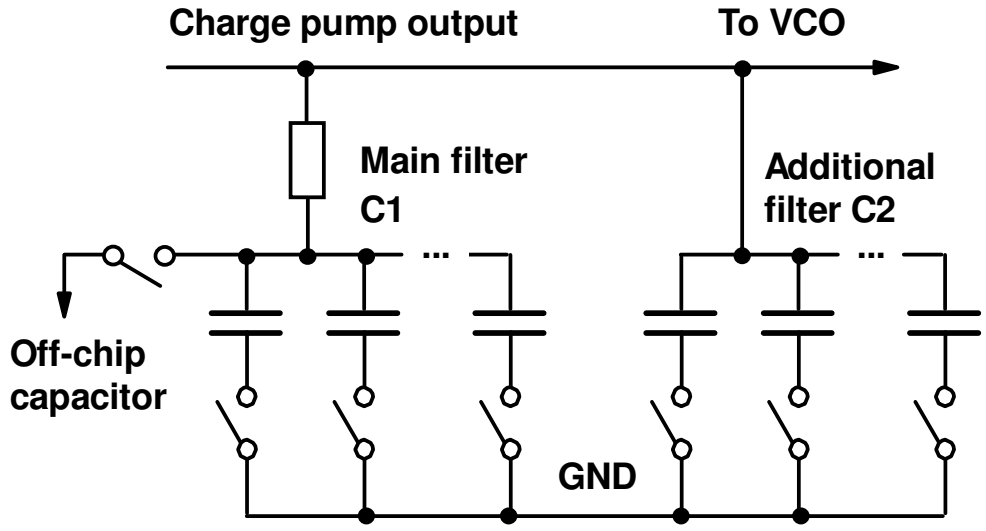

Figure 8-34: PLL programmable filter

Figure 8-35 shows a nominal simulation of the PLL settling in response upon initial power up, with a 2MHz input. The behaviour of the different charge pump current options are shown. Figure 8-36 shows the response to an abrupt 180 degree change in the input phase at 2MHz, representing the worst possible condition after a phase transition occurs. The settling times provided are to within 1% of the final value. In both cases, it can be seen that increasing the current from the default value of 5µA to 10µA reduces the settling time considerably. However, increasing the current further causes greater overshoot, resulting in a reduced proportionate improvement in the settling time (in the case of figure 8-36, an increase from 15µA to 20µA charge pump current causes an increase in settling time due to the excessive ripple).

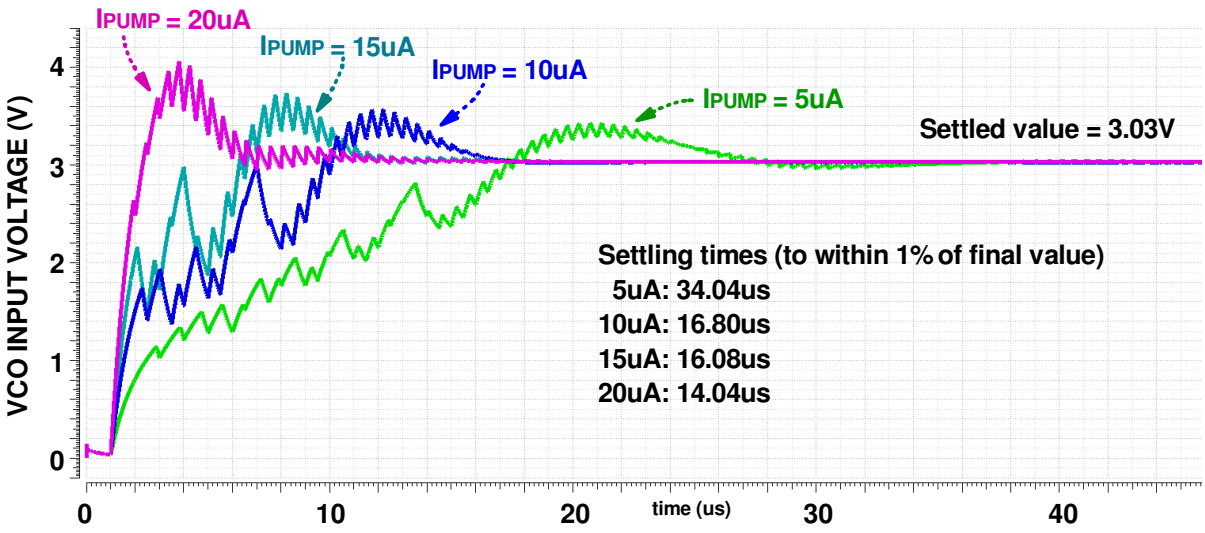

Figure 8-35: PLL settling time upon initial power up with different charge pump currents (2MHz input frequency)

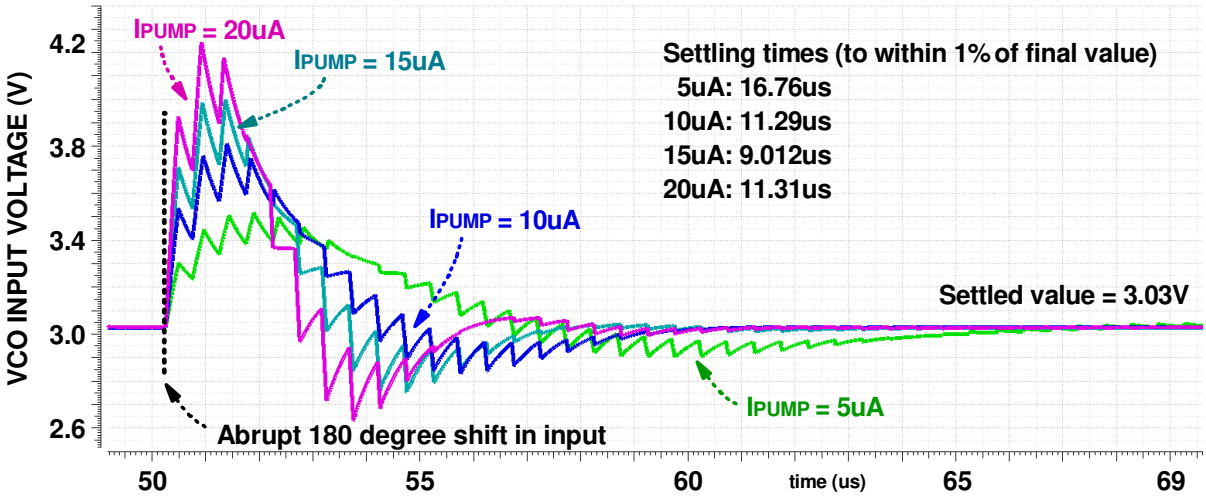

Figure 8-36: PLL settling time to a 180^{O} phase shift with different charge pump currents (2MHz input frequency)

8.3.6.4 Management FSM

In PSK mode, the PLL is used to store the phase of the drive before the phase transition begins, allowing a comparison to be made afterwards to determine if the shifting frequency requires adjustment. After the phase transition is complete, the PLL needs to align with the new phase of the carrier. To reduce the PLL settling time, the reference phase into the PLL can be switched to select the presently-selected output of the quadrature generator. This reduces the immediate phase error between the present phase angle and the target, hence reducing the time needed for settling. A state machine is required to determine the correct target phase, depending upon what phase change occurred.

Figure 8-38 shows a flow chart for the FSM. The state machine has four states, one for each quadrature output. For 90^{O} phase shifts, rotating clockwise between each state on the diagram represents a phase lag between symbols and anticlockwise represents a phase lead. For 180^{O}, the system needs to jump to the opposite side of the diagram, for either lead or lag. The transitions are determined by the phase mode selected (i.e. 90^{O} or 180^{O} mode), and the input phase rotation control (*TXDATA_ADV* or *TXDATA_RED*). For example, if a 90^{O} phase lag is required and the current selected reference is *I*, then the next reference should be *Q*.

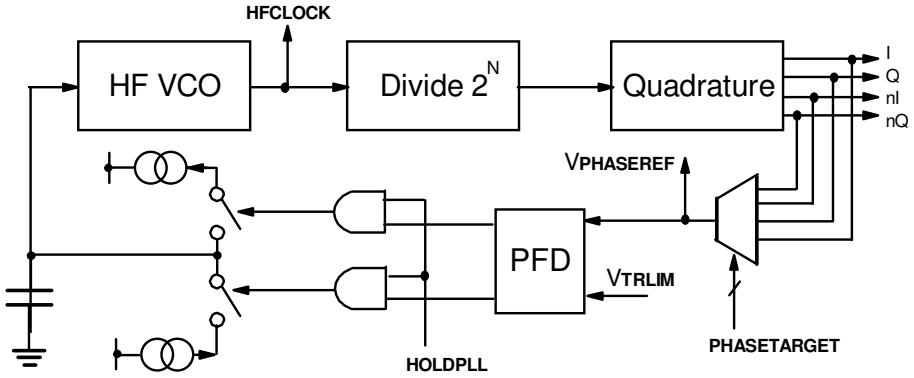

Figure 8-37: Integer-N PLL architecture with selectable input phase reference for faster settling

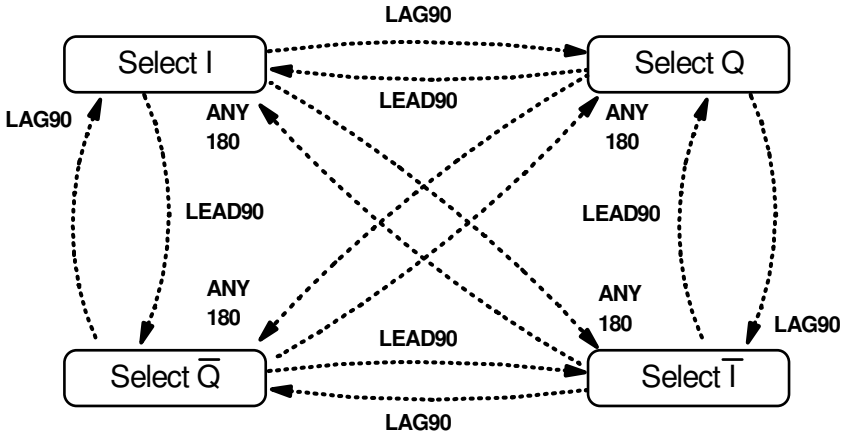

Figure 8-38: Reference selection FSM for PLL

8.3.7 Frequency Generator Logic

8.3.7.1 Top Level

The frequency generator logic block oversees the correct operation of the frequency transitions (i.e. only changing frequency at triangle mid-point crossings, and also for the correct number of cycles) and frequency calibration (i.e. measuring the phase offset where required and adjusting the modulation frequencies to correct this error). For these purposes, a management FSM was created to control both the operating frequency and also the flow of signals through the phase error measurement blocks. These consisted of a PFD, HF counter, Error Gain and Error Accumulator, as per figure 8-39.

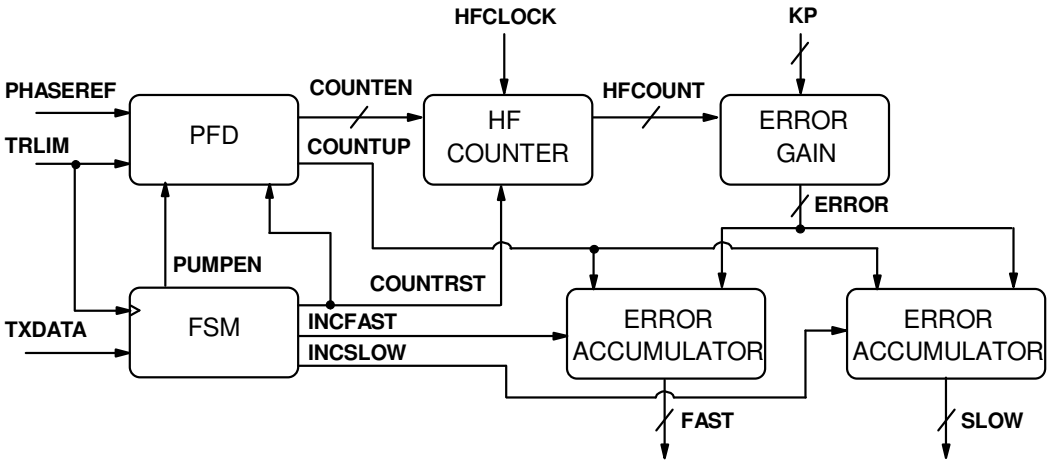

Figure 8-39: Frequency Generator control logic flow

8.3.7.2 *Phase-Frequency Detector*

In order to compare the phases of the V_{TRLIM} and $V_{PHASEREF}$, another PFD circuit was required. Two outputs are required, one to indicate when a phase offset exists (*COUNTEN*) and another to indicate the sign (*COUNTUP*), as shown in figure 8-40. *PUMPEN* indicates that the phase error measurement cycle is active. Since the system is clocked on the rising edges of V_{TRLIM}, the phase comparison is made around the falling edge of the two input signals so that a comparison can be made within one cycle of V_{TRLIM}. When *COUNTEN* is high, the HF counter is enabled and accumulates the phase error. *COUNTUP* indicates the error sign, to determine if the accumulated error should be added or subtracted from the digital shift-frequency setting. Unlike a conventional PFD, the phase offset sign must be held until add/sub operation has occurred, so a separate reset line *COUNTRST* is provided by the control FSM to reset the latches.

Note that additional logic is needed to ensure that the phase error measurement does not start until both *PHASEREF* and *TRLIM* are high, which occurs in the case that *TRLIM* lags behind *PHASEREF* (indicated by the shaded area of figure 8-40, right panel). The reverse scenario does not occur because *PUMPEN* is controlled synchronously with TRLIM. Figure 8-41 shows the circuit diagram.

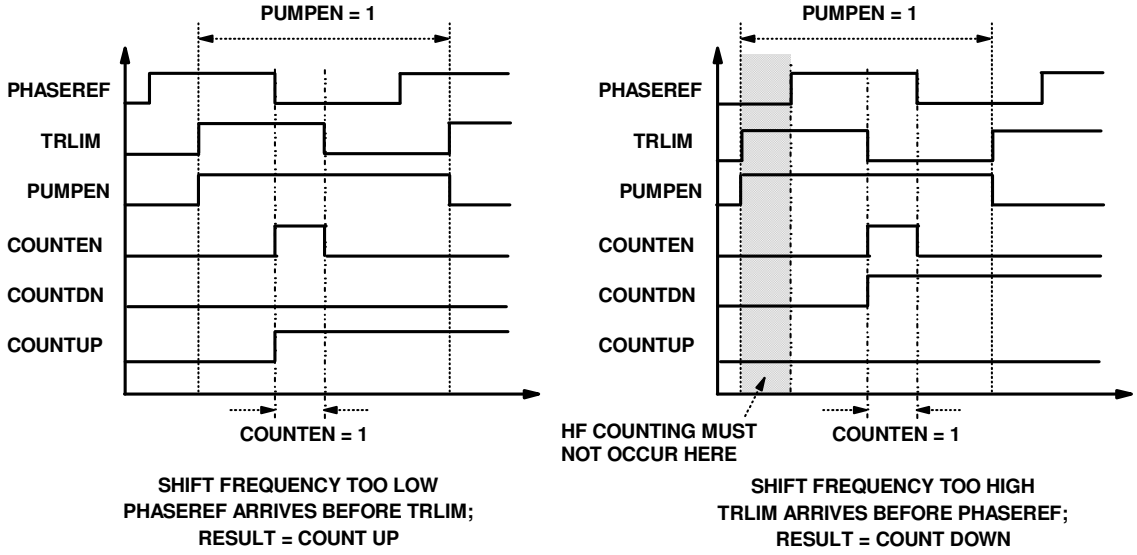

Figure 8-40: Phase error measurement PFD timings

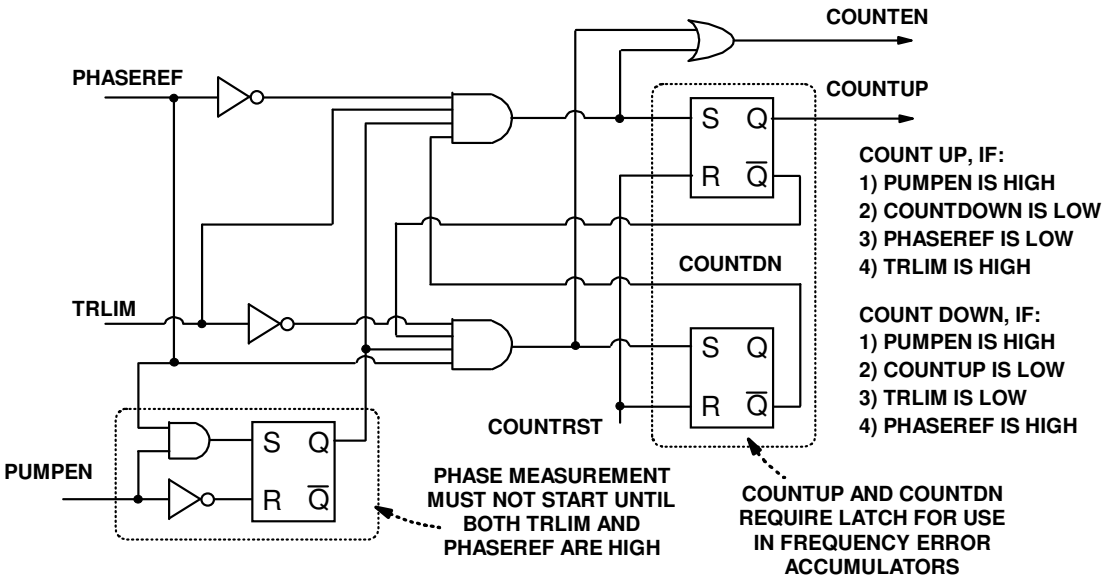

Figure 8-41: Phase error measurement PFD logic diagram

8.3.7.3 *High Frequency Counter*

The high-frequency counter accumulates the phase error between V_{TRLIM} and $V_{PHASEREF}$ using a clock frequency derived from the nominal operating frequency by the VCO of the phase-storing PLL. It was implemented as a synchronous architecture, using one-bit counter cells as per figure 8-42. Each cell uses a flipflop, the propagation delay being approximately 1.39ns on the slowest PVT corner, hence setting the upper limit of the clock frequency to be around 500MHz (allowing for safety margin). The counter cell reset is also synchronous, as this is controlled by the system FSM.

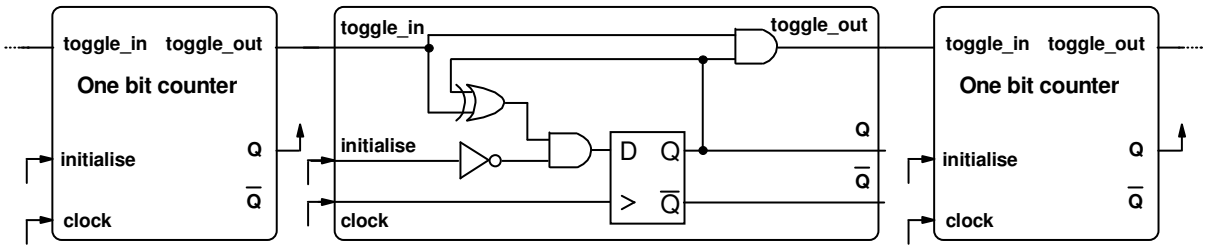

Figure 8-42: One bit counter cell with synchronous reset

The worst phase angle offset possible is 180 degrees, which at the lowest tank drive frequency of 8.28kHz is equivalent to 60.4µs. With a clock frequency of 500MHz maximum, the largest counter size required is 30200, hence the counter must be at least 15 bit to avoid overflow. A 16-bit architecture was used to permit a margin of safety, and also to allow for possible lower frequencies to be used in future testing. Additional logic is included to prevent overflow, with a programmable clamp value to limit the accumulator maximum value as per figure 8-43, providing additional experimental control of the frequency calibration loop.

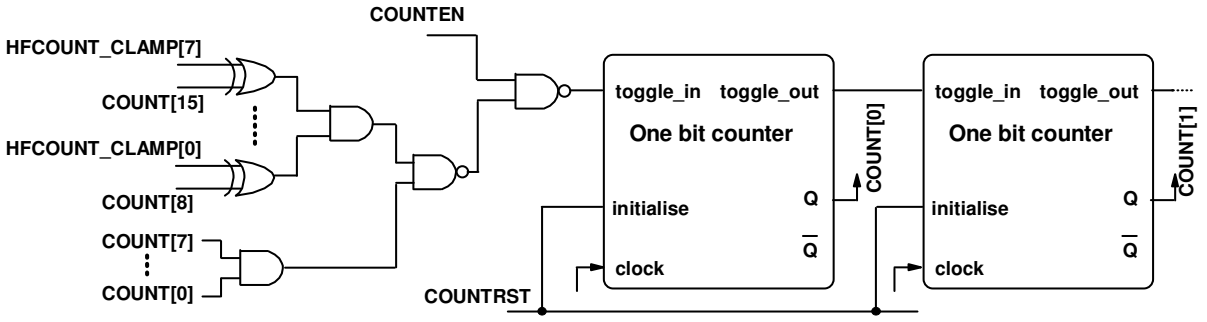

Figure 8-43: 16 bit error accumulator with synchronous reset and value clamp

8.3.7.4 *Proportional Gain*

To allow the self-calibration loop response to be adjusted, a proportional element was included in the feedback loop. This allows the accumulated phase error to be scaled up or down by a fraction to make the loop more or less responsive to phase error, allowing speed and accuracy to be traded-off. Elements of Integral and Differential control were considered to allow for faster convergence, however these were not developed due to limited project time.

To avoid the need for an arbitrary integer multiplier, a left/right shifter was utilised to multiply/divide the accumulated error by 2^N. This was implemented with multiplexers as per figure 8-44, where the appropriate bits of the accumulator are selected for phase shifting. The range of K_P options was limited to 4 bits, i.e. 4 multiplexer stages, with options for no shifting, up to 7 bits of left shift and 8 bits of right shift.

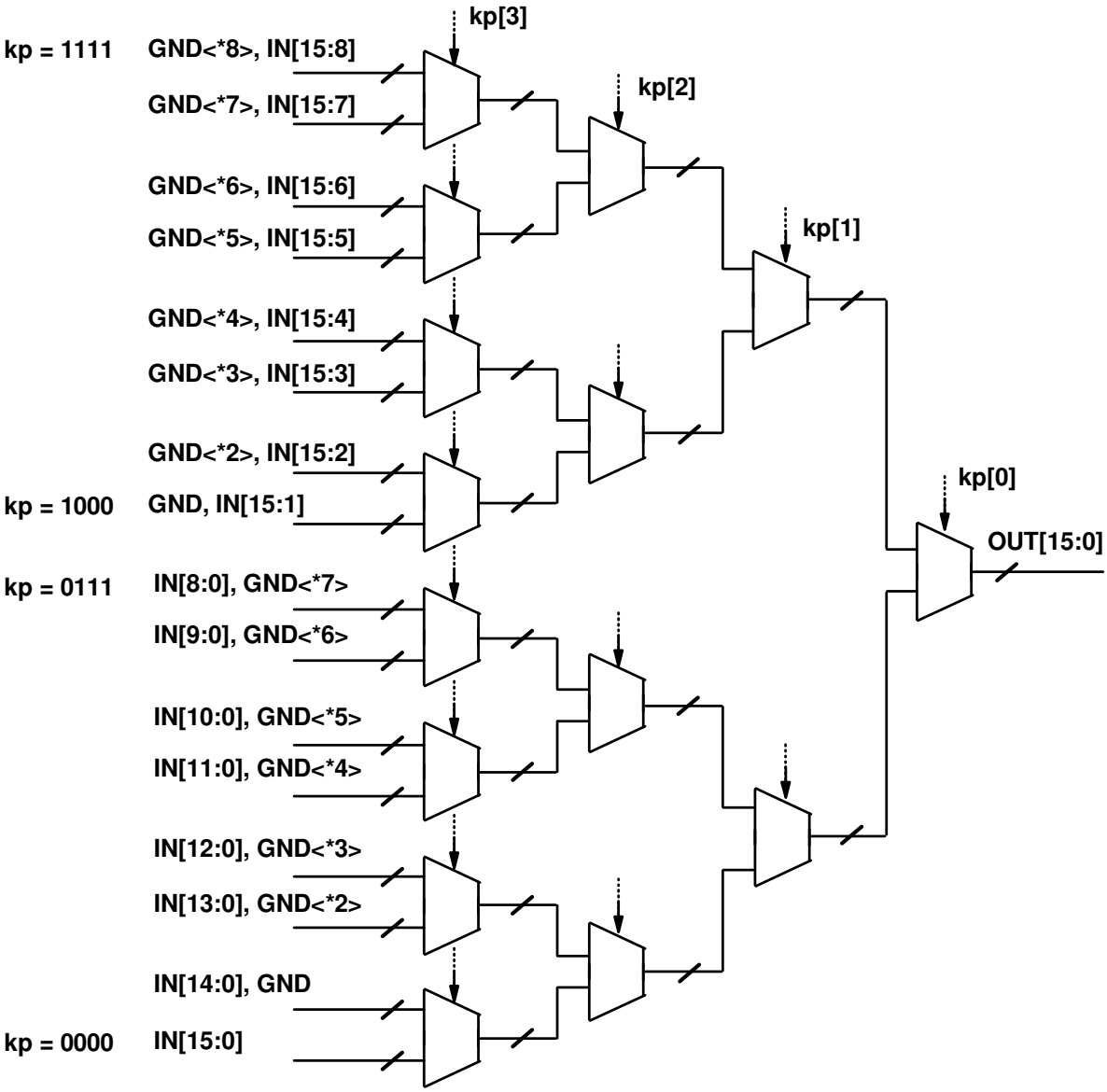

Figure 8-44: Programmable K_P gain multiplexer circuit

8.3.7.5 Error Accumulator

The error accumulator was implemented as a D-type flipflop register, taking the current value and adding or subtracting an input value, according to the control data. A 16-bit architecture was used to fully accumulate the error in the counter, although only the 8 MSBs were used for the frequency settings. Additional logic was included to prevent the accumulator overflow or underflow. The adder/subtractor block includes an overflow/underflow detection, implemented by taking the XOR of the most significant carry and input sign, according to table 8-8. If overflow or underflow has occurred, the register output is fed back into the input with no added or subtracted error. Otherwise, the new computed value is stored. The resulting adder/subtractor logic is shown with full adder cells in figure 8-45.

SUB_NADD	*CARRY_MSB*	*OVERFLOW*	**Condition**
0	0	0	Result is inside range
0	1	1	Result will overflow (> 65535)
1	0	1	Result will overflow (< 65535)
1	1	0	Result is inside range

Table 8-8: Positive/negative overflow detection logic, proof of XOR requirement

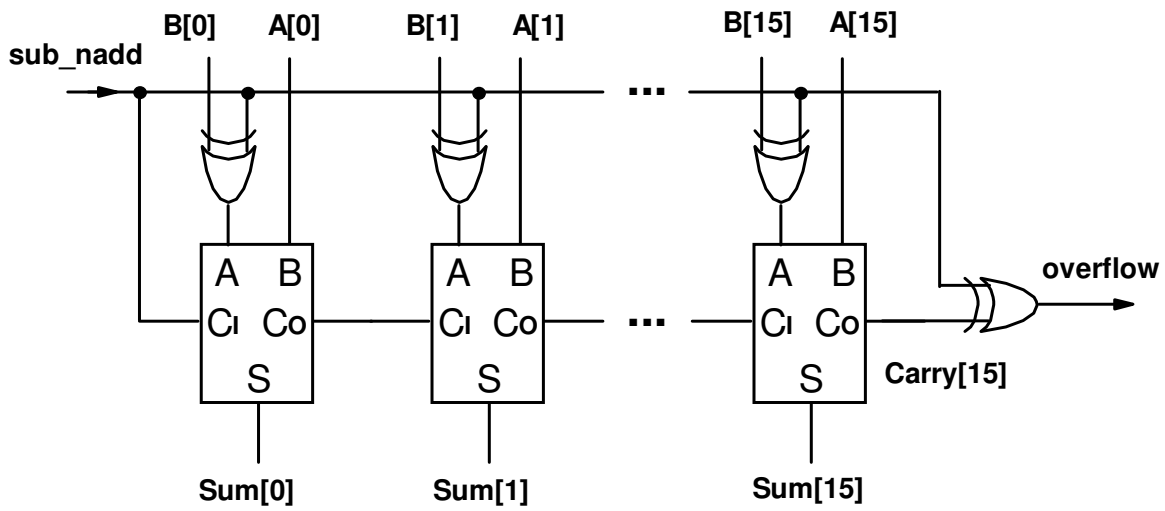

Figure 8-45: Full adder/subtractor with overflow/underflow detection logic

The option to preload a value into the accumulator was included, to allow manual override and also an initialisation value for experimental testing and debug. An additional multiplexer allows the choice between the next calculated frequency setting or a value stored in the main control registers, which may be set by the user. Figure 8-46 shows the resulting accumulator block diagram.

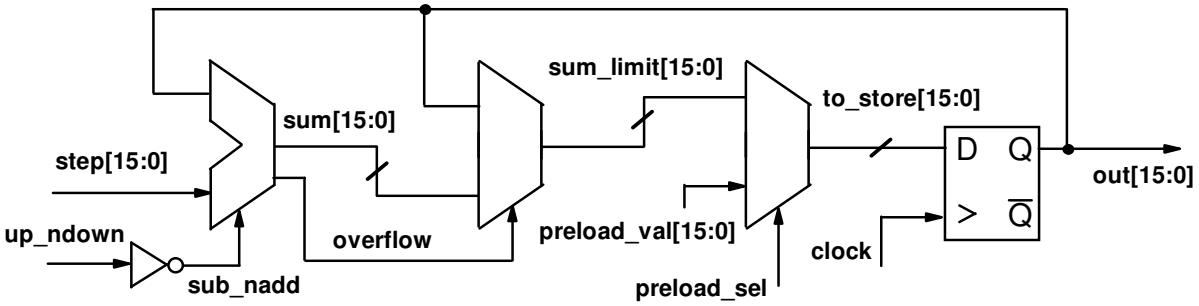

Figure 8-46: Phase error accumulator architecture with overflow prevention and manual preload

8.3.7.6 Management FSM

The management FSM controls the frequency setting and phase error measurement, depending upon what operation mode is selected. Figure 8-47 shows a flow chart for the basic control functionality. The FSM begins in an initialised state 0, keeping the HF counter and PFD reset. When a *TXDATA* input is activated, the system moves to the frequency shift state 1, where a shifting frequency is selected, the phase reference PLL is held (*HOLDPLL* = 1) and a cycle counter is started. In auto-calibration PSK mode (*MODMODE* = 0 and *AUTOPSK* = 1), the counter expiry (noted by *SHIFTEND* = 1) causes a transition to the phase measurement state 2. When in fixed-frequency PSK mode (*MODMODE* = 0 and *AUTOPSK* = 0), the counter expiry causes a jump to the accumulator update state 4. When in FSK mode (*MODMODE* = 1), the system jumps ahead to the accumulator update state 4, when *TXDATA* is de-asserted.

In the phase measurement state 2, the PFD is enabled (*PUMPEN* = 1) so that a phase error measurement is made, using the HF counter (*COUNTRST* = 0). The system proceeds to the propagation state 3, allowing the accumulator to settle once the HF counter has stopped running. Next, the accumulators are clocked in the update state 4 (*INC* = 1). The phase reference PLL is unheld (*HOLDPLL* = 0) to allow it to re-align with the phase of the nominal frequency. In auto-calibration PSK mode, this state represents the shift frequency being calibrated to correct a phase offset error. In fixed-frequency PSK and FSK

modes, this state loads the digital user-set shift frequency into the accumulators from the digital IO registers.

Finally, the system transitions into a reset state, forcing the *TXDATA* latches to clear.

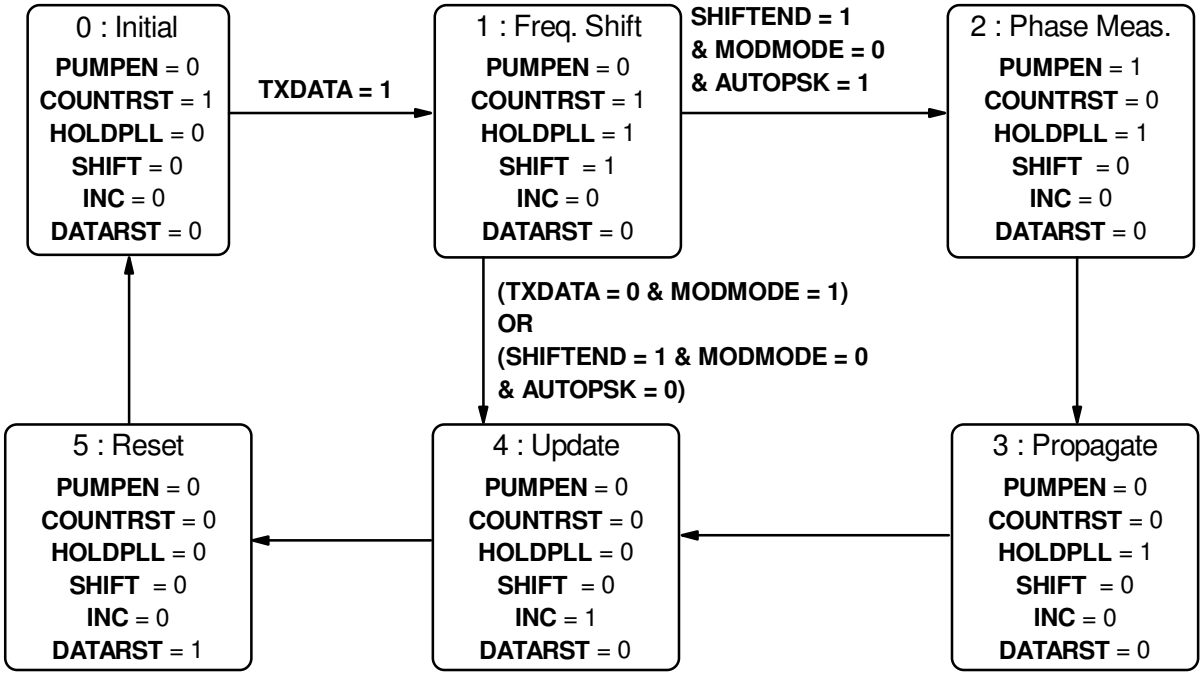

Figure 8-47: Frequency generator control FSM for combined FSK/PSK modulation

The FSM schematic and layout was implemented manually as opposed to compiled directly from Verilog, as design complexity did not justify the set up time for the required CAD tools. It was desirable nonetheless to reduce the complexity to reduce schematic and layout entry time. The shifting sequence was implemented generically, with the phase lead or lag control for the shift frequencies being controlled by a latch and AND gate. Furthermore, the number of cycles for which the PSK transition may occur is 2, 4, 8 or 16. Rather than create a system with at least 16 states, a separate counter (enabled when *SHIFT* = 1) and comparison logic (producing a *SHIFTEND* signal) were utilised.

The FSM is clocked by mid-point crossings of V_{TR}, so that all transitions in frequency occur at this point. There is a slight delay between the mid-point crossing occurring and the FSM output changing, caused by the propagation delay FSM flipflops and output logic, however this is small compared to the period of V_{TR} at maximum frequency (i.e. less than 1.39ns compared to a period of 500ns) and so will cause a negligible detuning effect. *TXDATA_ADV* and *TXDATA_RED* are buffered through a pair of flipflops that are also clocked by V_{TR} mid-crossings, to ensure that the FSM is not clocked whilst an input is transitioning between states. Figure 8-48 shows how the asynchronous logic is operated by the FSM.

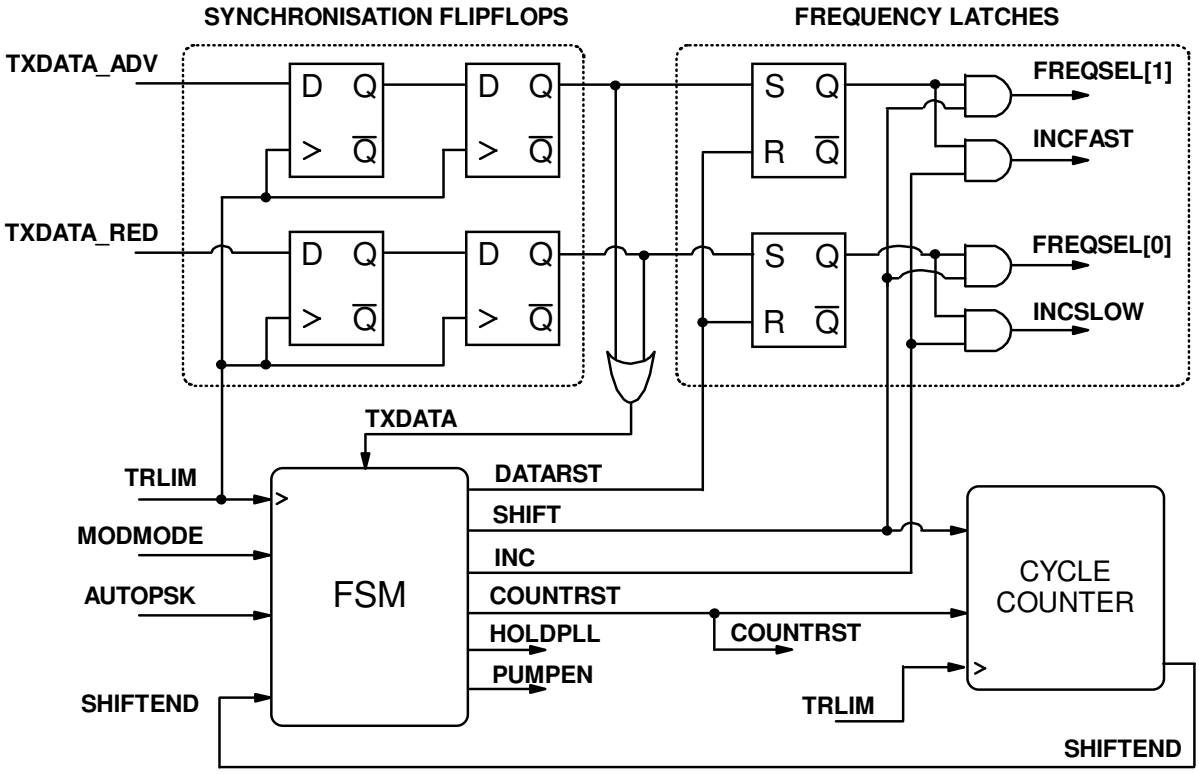

Figure 8-48: Frequency generator control FSM and associated logic

Figure 8-49 shows the FSM operating correctly in FSM mode. The *FREQSEL* controls operate two rising edges of *TRLIM* after the corresponding *TXDATA* input has been asserted or de-asserted.

Figure 8-50 shows the system operating in PSK mode with automatic frequency calibration enabled. For each *TXDATA* control the corresponding *FREQSEL* value is enabled for four cycles to activate the respective shift frequency (state 1). *HOLDPLL* is also asserted during this time to store the nominal phase reference. After four cycles have elapsed, the system returns to the nominal frequency by setting *FREQSEL[1:0]* = 00 and the phase error measurement commences (state 2). When the error measurement is complete, the system waits for one cycle to allow the error accumulator inputs to settle (state 3), then the corresponding accumulator is updated using *INCFAST* or *INCSLOW* accordingly (state 4). The system resets itself (state 5) and returns to idle (state 0).

Figure 8-51 shows fixed-shift frequency PSK mode. Operation is as above, however the system jumps to state 4 after the phase shift, bypassing the phase error measurement. The error accumulators are still clocked using *INCFAST* and *INCSLOW*, forcing the accumulators to preload the digitally-set value loaded in by the user. Note that a small glitch in *COUNTRST* which occurs during the transition from state 5 to 0 (observed in both fixed shift frequency and automatic calibration PSK modes). This is a static hazard behaviour, however is not a concern for operation, since quickly returns to the asserted state. It controls the reset of the HF counter and PFD, both of which have multiple cycles (i.e. more than 500ns at maximum frequency), which is more than enough time for these circuits to fully reset.

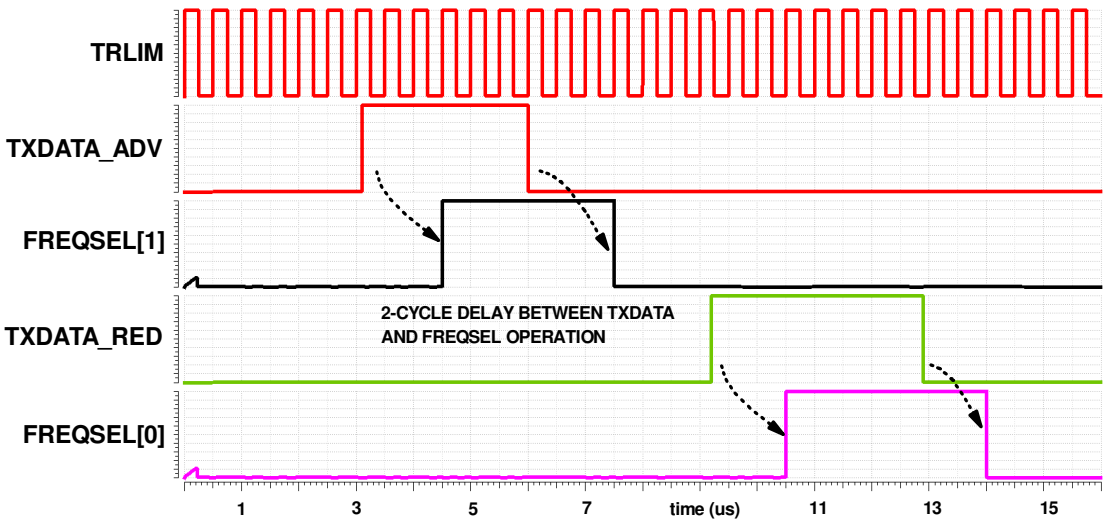

Figure 8-49: Frequency generator control FSM operation in FSK mode

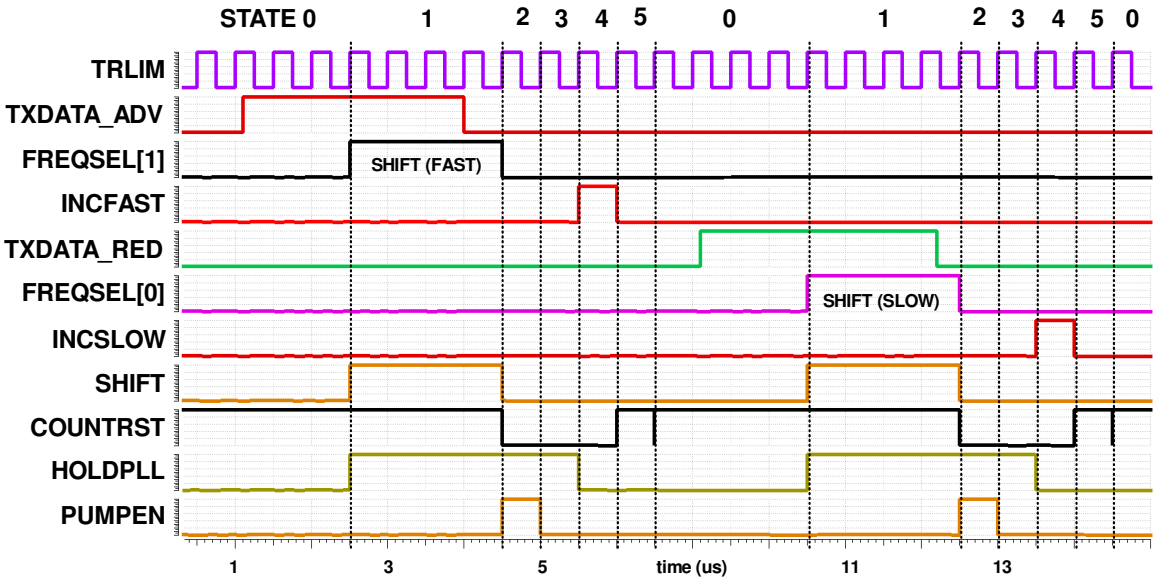

Figure 8-50: Frequency generator control FSM operation in PSK mode (automatic calibration)

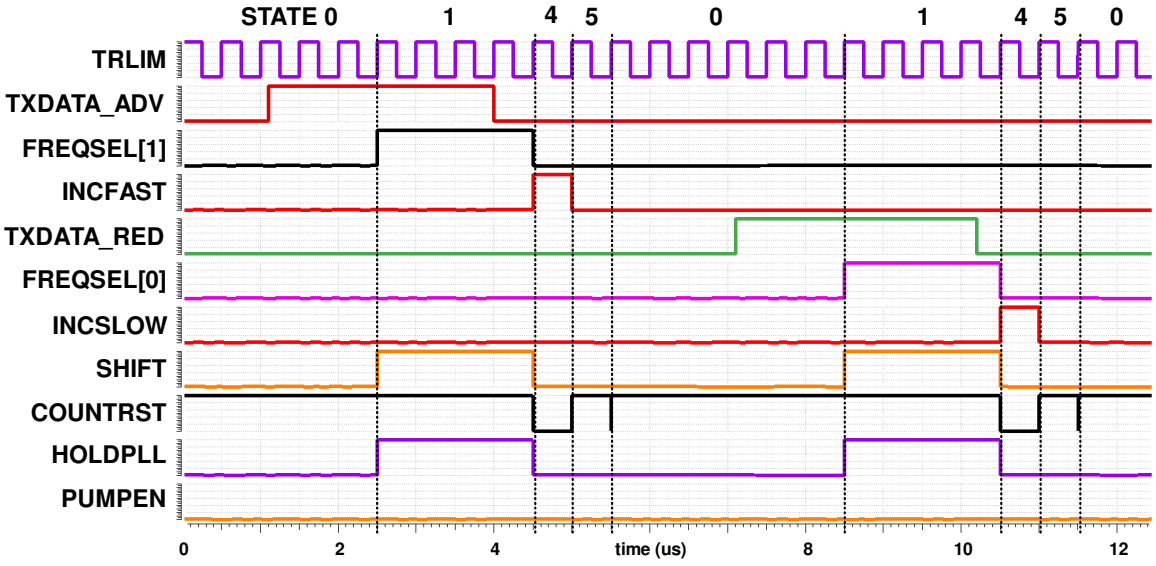

Figure 8-51: Frequency generator control FSM operation in PSK mode (no calibration)

8.3.8 Self-calibrating PSK simulation

This section demonstrates the full functionality of the self-calibrating PSK system. Some behavioural blocks were used to speed up simulation. Simulation was done in the 2MHz region to reduce the number of required cycles of the high frequency counter, further reducing simulation time.

8.3.8.1 Automatic calibration of PSK frequencies

Figure 8-52 shows the self-calibration loop operating for a 180^{O} phase lead scenario from an initialised state. In practice, a 180^{O} phase rotation in only 2 cycles is not preferable from an operational point of view, but is more useful in demonstrating the ideal functionality of the system than a smaller phase angle over more cycles. Both the digital value of *FREQFAST[7:0]* and V-to-I voltage V_{FREQF} are provided to show how the system converges upon the optimal shift frequency. With each pulse on *TXDATA_ADV*, the shift frequency is adjusted. A large step in operating frequency occurs at the first phase transition, with decreasing subsequent steps as the phase error is reduced. Note that this scenario is using the largest K_P error gain setting in order to speed up simulation time, at the expense of settled tuning accuracy.

Figures 8-53 shows the first cycle of the calibration sequence. The system has been powered for sufficient time such that *TRLIM* and *PHASEREF* are aligned, meaning that the PLL is providing an accurate phase reference for comparison later. A rising edge on *TXDATA_ADV* causes *FREQSEL[1]* to be raised high two cycles later, causing the V_{TR} oscillator to switch to the fast frequency. At the same time, the target output phase from the PLL is selected, causing *PHASEREF* switch to the 180^{O} reference. At this moment the comparison is not yet occurring, so the transient switching of *PHASEREF* is not important. *HOLDPLL* is active, preventing the PLL charge pump from operating and maintaining a constant frequency of the PLL VCO. The system then operates at the fast frequency exactly two cycles.

After two cycles of *TRLIM* have elapsed, the nominal frequency is selected and the V_{TR} can be seen reducing to the nominal frequency. The phase error measurement is activated with *PUMPEN* and the HF counter is armed by disabling *COUNTRST*. In this case, the shift frequency was too low, so the falling edge of *PHASEREF* arrives first. This activates triggers the *COUNTEN* signal to activate the phase measurement counter and sets the count direction using *COUNTUP*. When the falling edge of *TRLIM* occurs, *COUNTEN* is disabled. A rest cycle takes place to allow the HF counter output *HFCOUNT[15:0]* to fully propagate through the error accumulator, which is then clocked on the next cycle, causing *FREQFAST[7:0]* to step in value. Note that, although the value of *HFCOUNT[15:0]* has a gain applied in the form of K_P, the *FREQFAST[7:0]* setting is taken from the upper 8-bits of the 16-bit accumulator. Hence the shown step in *FREQFAST[7:0]* is considerably smaller than the *HFCOUNT[15:0]* value shown. *HOLDPLL* is disabled in the same cycle to permit the PLL to re-align with the new phase of the nominal frequency.

Figure 8-54 shows the activation of the phase transition error measurement after 32 previous similar phase transitions, where the phase error is much smaller. The operating sequence is exactly the same. However the accumulated error is much smaller, such that the value of *FREQFAST[7:0]* does not change at all. In this case, it can be seen visually that the phase angle at the end of the phase shift is approximately 180^{O}, i.e. the calibration loop has functioned correctly. In this case, the time offset between *TRLIM* and *PHASEREF* is 1.32ns, which corresponds to 0.895^{O} phase error at the nominal frequency.

Figures 8-55, 8-56 and 8-57 show the equivalent behaviour for a 180^{O} phase lag scenario with the same control parameters, which also correctly converges. The error in this case is less than 0.954^{O}.

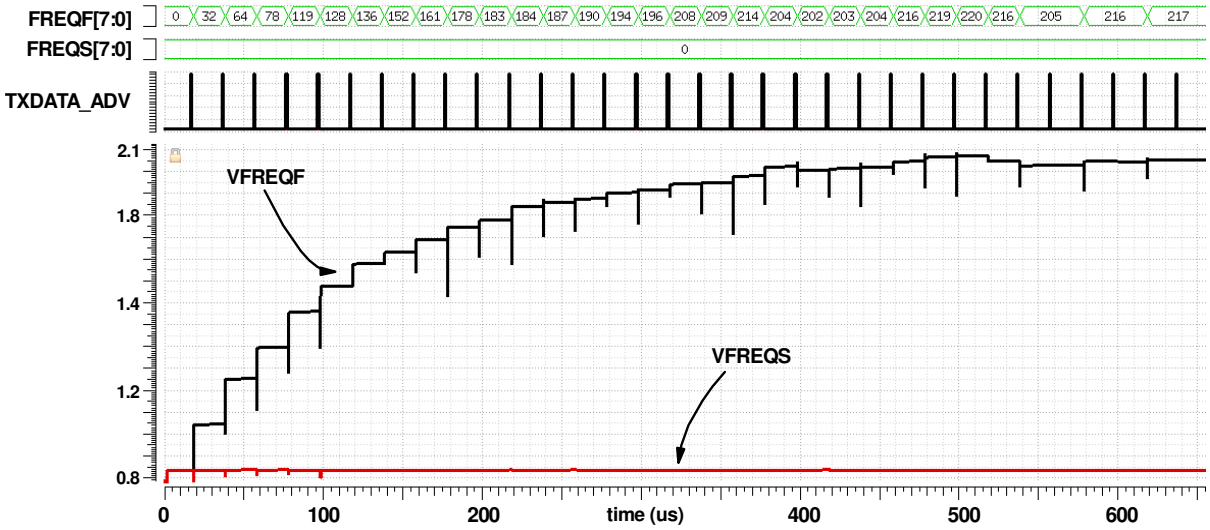

Figure 8-52: Frequency generator self-calibration: 180^{O} phase lead, 2MHz nominal frequency

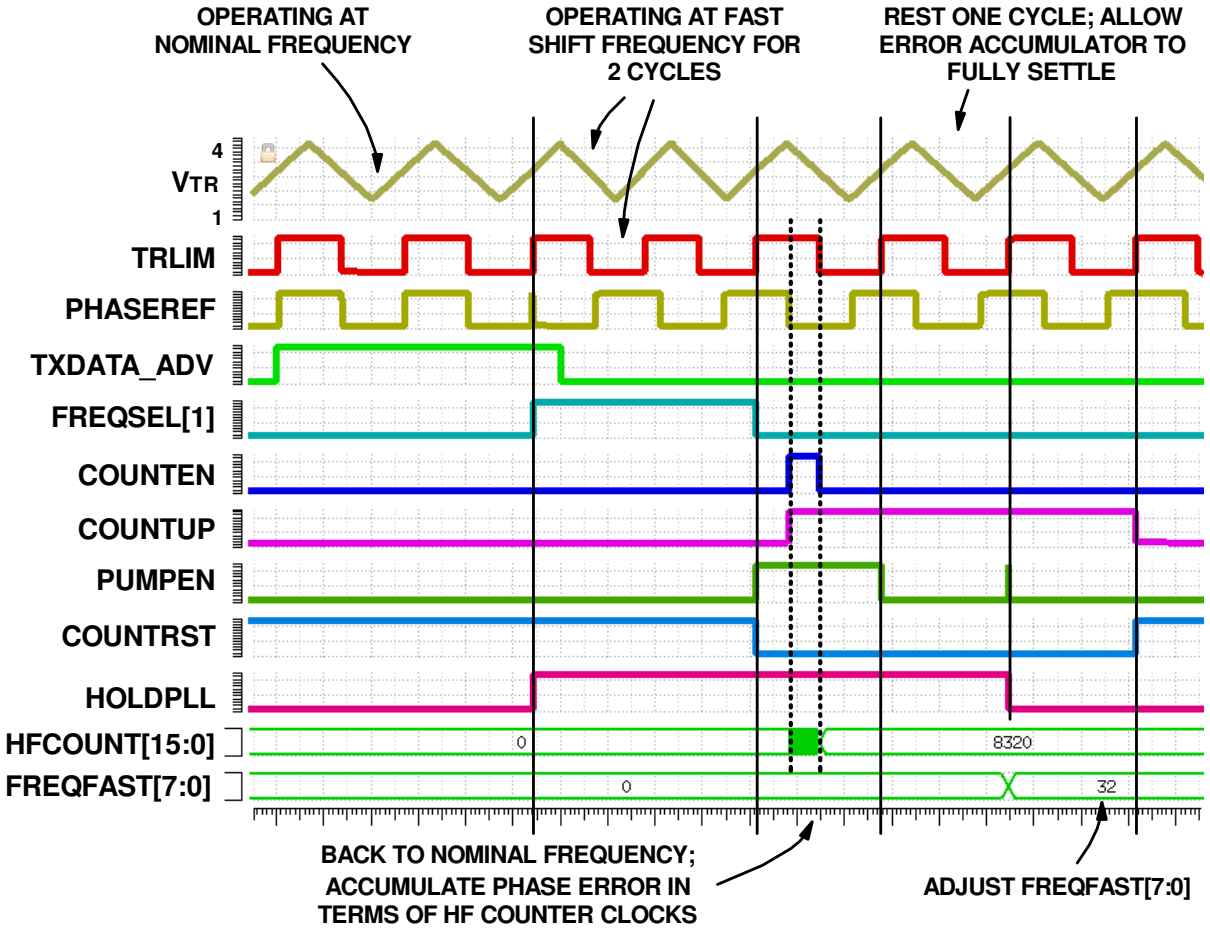

Figure 8-53: Frequency generator self-calibration, first calibration cycle, 180^{O} phase lead, 2MHz nominal frequency. Phase lead setting is too low; phase error is large.

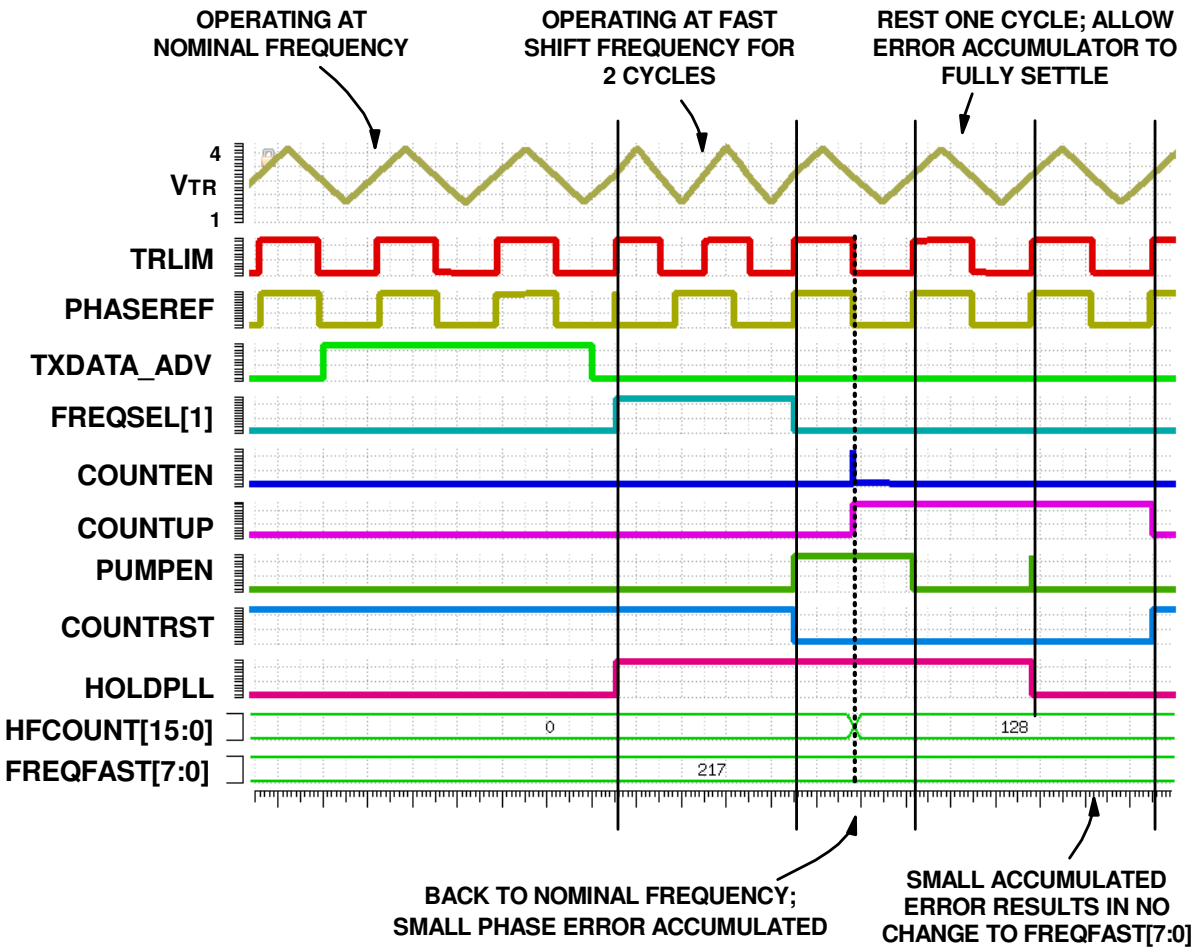

Figure 8-54: Frequency generator self-calibration, 32nd calibration cycle, 180O phase lead, 2MHz nominal frequency. Phase lead setting is near close to ideal; phase error is small.

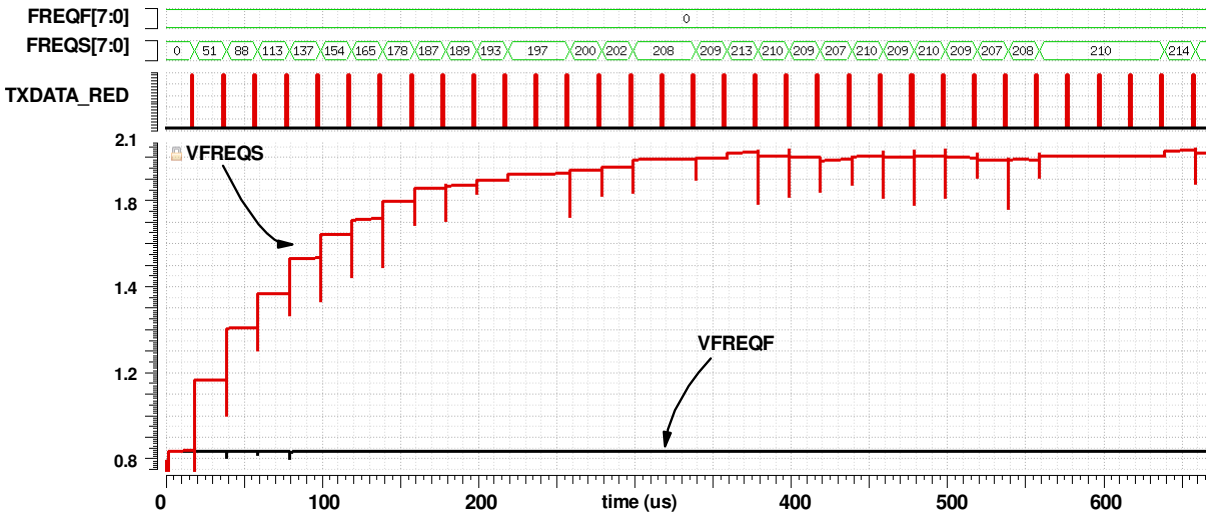

Figure 8-55: Frequency generator self-calibration: 180O phase lag, 2MHz nominal frequency

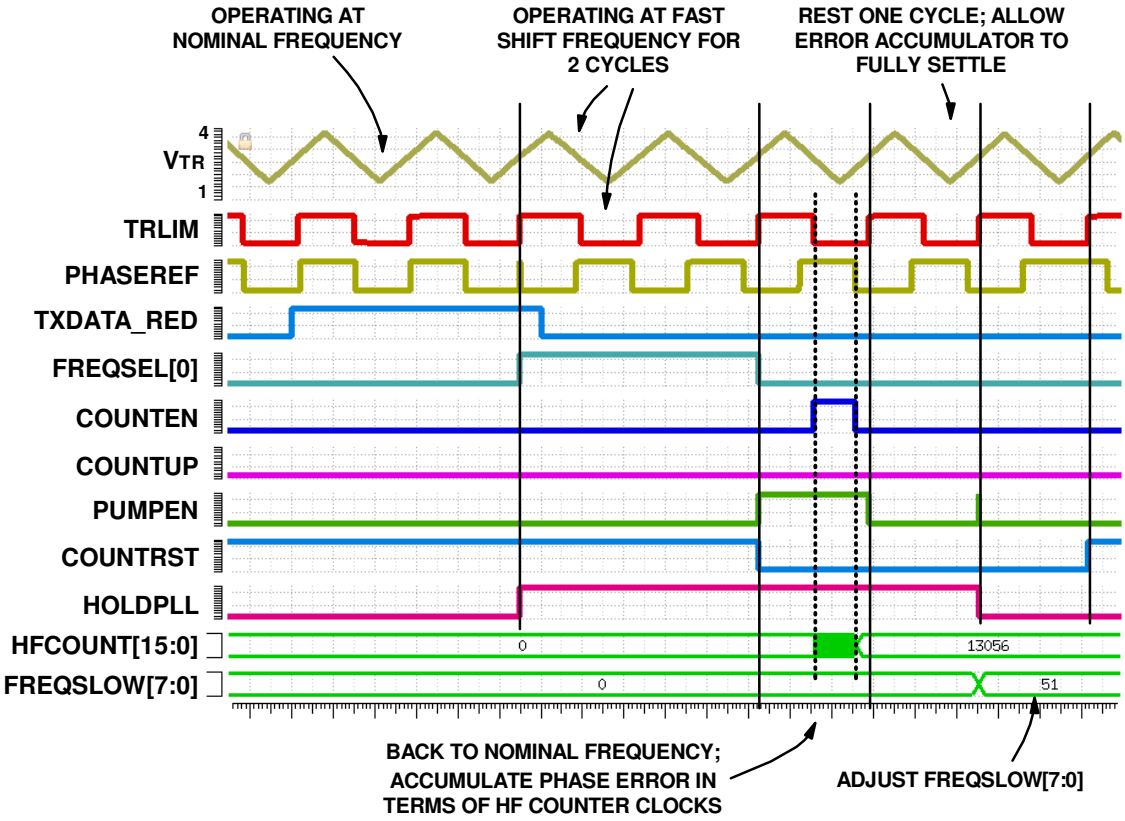

Figure 8-56: Frequency generator self-calibration, first calibration cycle, 180^{O} phase lag, 2MHz nominal frequency. Phase lag setting is too low; phase error is large.

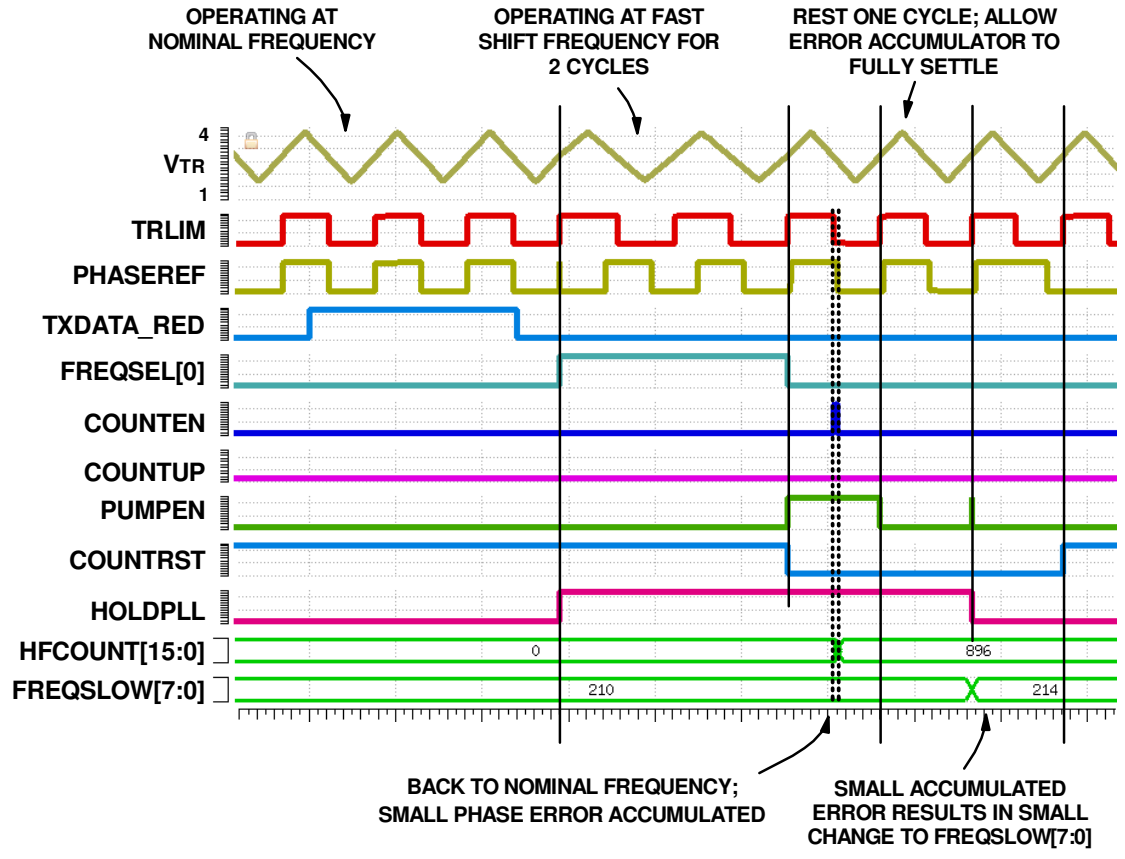

Figure 8-57: Frequency generator self-calibration, 32nd calibration cycle, 180^{O} phase lag, 2MHz nominal frequency. Phase lag setting is near optimal; Phase error is small.

8.3.8.2 *Varying the angle of phase shift*

Figures 8-58 and 8-59 show the results of simulations for 90^{O} PSK in 2 cycles, both having converged upon optimal shift frequencies for the respective phase shifts. Note that the value of *CYCLESHIFT[2:0]* is set to 45^{O}/cycle to restrict the current range and improve the calibration accuracy.

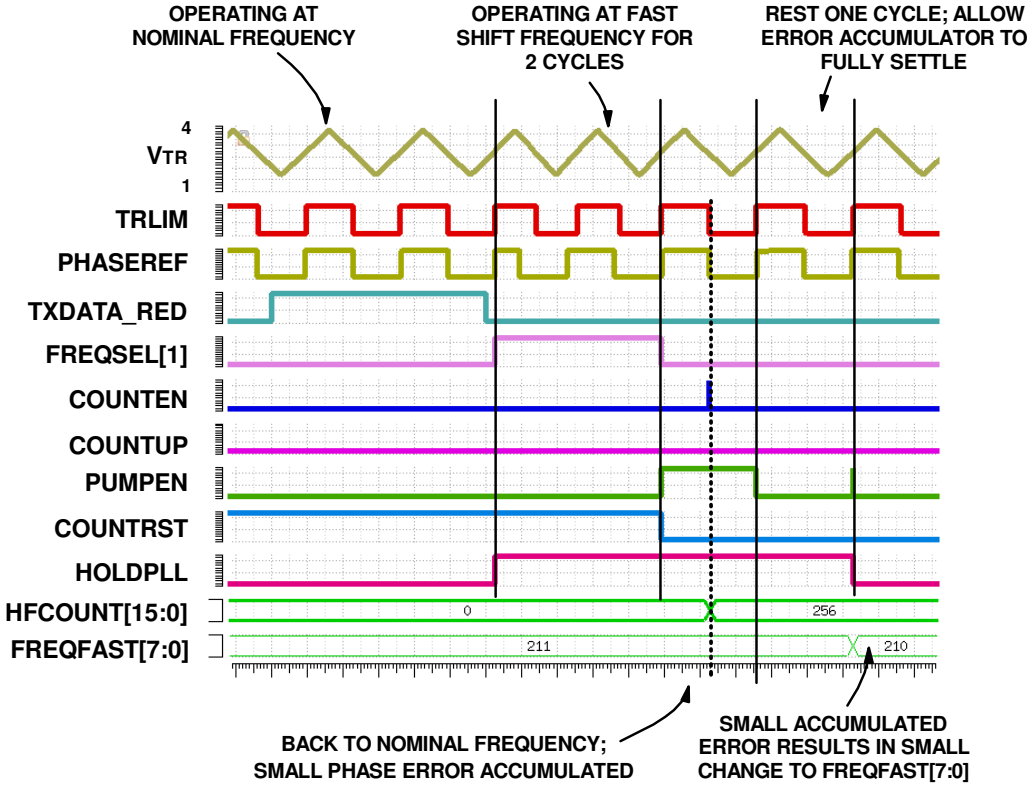

Figure 8-58: Frequency generator self-calibration, near settled condition, 90^{O} phase lead, 2MHz nominal frequency

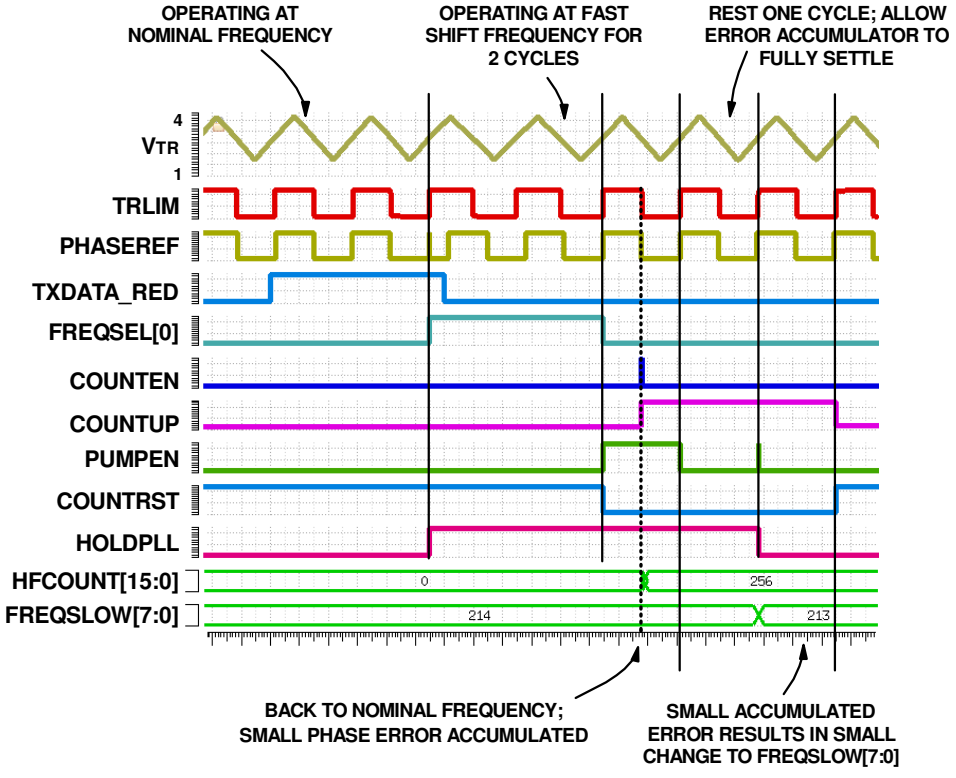

Figure 8-59: Frequency generator self-calibration, near settled condition, 90^{O} phase lag, 2MHz nominal frequency

8.3.8.3 *Varying error accumulator gain*

Figure 8-60 shows how varying the self-tuning gain K_P changes the settling time. The settling times and steady-state ripple values are provided in table 8-9. As expected, the use of a larger loop gain reduces the time taken for convergence, but visibly creates greater ripple in the steady-state setting. Whilst lower gain settings were available, simulation was not feasible in the available project time due to the excessive number of HF cycles required to obtain a result. It may however be inferred that the steady state ripple will further decrease if the lower settings are used. Whilst a diverse range of self-calibration loop gains is useful for system evaluation, in practice a very slow calibration gain may be undesirable. Parametric drift and long intervals between data transmissions may require fast re-calibration of the shift frequencies for accurate PSK angles.

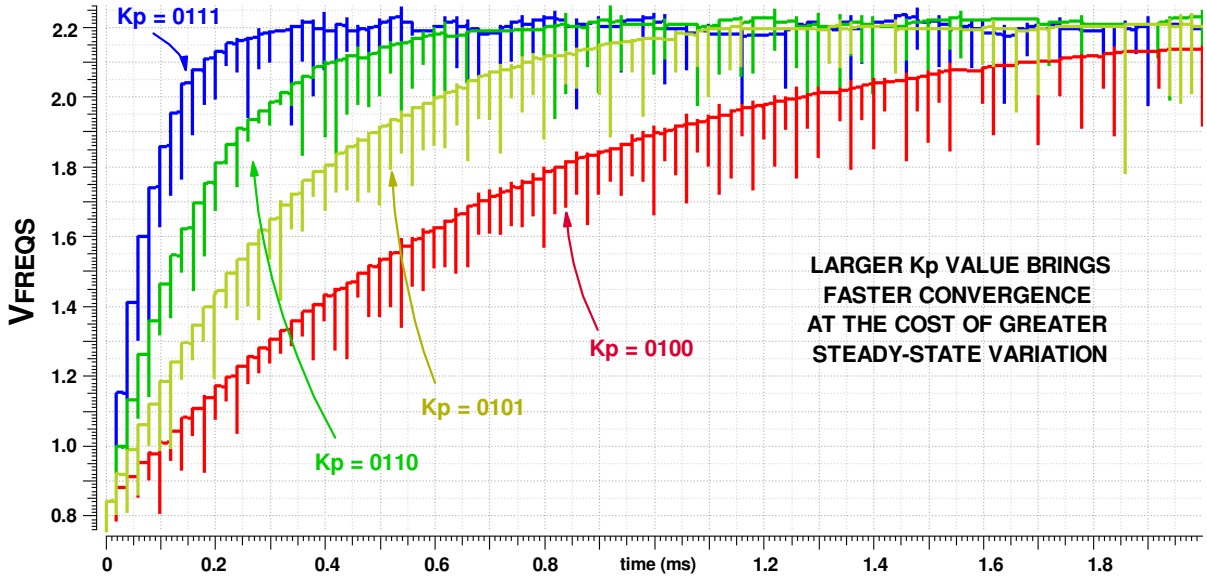

Figure 8-60: V_{FREQS} settling behaviour with varying K_P values (2MHz nominal frequency, 180^O PSK in 2 cycles, TXDATA_RED pulse at 50kHz)

K_P	Effective Gain	Settling time (2%)		Steady-state ripple	
		Time (µs)	TXDATA pulses	Voltage (mV)	DAC codes
0111	128	227	12	58.78	8.85
0110	64	662	34	39.76	5.99
0101	32	845	43	19.63	2.96

Table 8-9: Automatic frequency calibration settling time to within 2% of final V_{FREQS} voltage

8.4 Other design changes

Whilst significant work was done to develop a self-calibrating architecture for correct PSK functionality, modifications were made to the other system blocks. Some were necessary whilst others were the inclusion of additional functions to facilitate future experimentation. A brief description of the required changes is provided here, with further detail about the changes to each block provided in subsequent sub-sections. A summary of changes is provided in table 8-10.

8.4.1 Required changes for PSK modulation

It was established that multiple tuning loops would be required for the different operating frequencies. Hence the digital integrator required changes to allow storage of different resonant settings for the antenna tuning capacitors.

The change between multiple frequencies required a rapid change in the tuning setting to maintain resonance. It was therefore necessary to re-evaluate the previously-used voltage DACs and triangle comparator architectures to ensure that the change in antenna tuning remained synchronous with the change in operating frequency.

8.4.2 Required changes for IC process changes

Between the fabrication of the previous "lctune018" test IC, some changes to the AMS018 process were made. In particular, some process layers were no longer available, meaning that thick oxide gates for HV LDMOS FETs were no longer available, meaning that NMOS and PMOS HV devices required either 1.8V or 5V V_{GS} maximum. The previously fabricated IC had used 20V V_{GS} rated drivers and PMOS switch for antenna tuning, so a re-design of the driver stage was essential.

Additionally, the DUALCMIM capacitors were no longer available, forcing the use of the CMIM capacitors with a lower capacitance density. Any part of the system which used these capacitors required a re-design, most notably the triangle generator integration capacitors and the tuning error detection circuit capacitive divider.

8.4.3 Required changes for improved functionality

The method of phase trimming of the antenna drive and tuning capacitor switching phases on "lctune018" did not include any logic to prevent overflow. I.e., when the tuning setting was close to maximum or minimum, the phase trim applied could create an overflow or underflow in the digital tuning value and cause the switch duty cycle to be incorrect. Additional logic in the phase trimming was required to clamp the digital tuning settings and prevent this overflow to ensure correct behaviour across the tuning range.

Additionally, the previous digital tuning error integrators were limited to gain settings of 2^N. For more precise setting of the self-tuning gain, the tuning architecture was changed to instead operate as an accumulator with arbitrary gain, i.e. the integrator increments or decrements by a user-defined step, as opposed to a multiple of 2.

With the presence of multiple tuning loops, it was desirable to be able to observe multiple V_{TUNE} voltages concurrently during experimentation. This would help verify that only the correct antenna tuning loop was being activated at any given operating frequency, and also permit the voltages to be easily overridden with an external voltage source for debug and experimentation. The previous system provided observation of one V_{TUNE} voltage at a time using the analogue test bus. For the new system, it was decided to provide all V_{TUNE} voltages on separate output pins.

8.4.4 Additional functions for future experimentation

Since the digital error integrators, voltage DACs and triangle slice comparators required some changes, the opportunity was taken to include some additional experimental tuning options for the antenna. These were not directly related to the data modulation function but including them would provide greater value for money and effort, given the cost and design time required to produce an entire system. The following functions were included, disabled by default but could be switched on digitally if needed.

8.4.4.1 V_{SW} error detection sample point trimming

To measure the antenna tuning error, the sign of V_{SW} must be determined immediately before the tuning switch is closed. The moment at which sampling occurs must be as close as possible to the switch closure in order to obtain the most correct tuning information. In practice, the comparator used to determine the sign of the HV switch has some propagation delay, hence at the sampling instant the information about the tuning condition is out of date. Close to the resonant condition, this can cause incorrect sensing of the switch voltage, limiting the tuning accuracy.

To overcome this issue, the phase of the sampling instant can be trimmed to bring the sampling of the sign data closer to the true value. This approach was used in this system; the timing delay being generated with the HV switch drivers.

8.4.4.2 *Independent operation of V_{TUNE+} and V_{TUNE-}*

The unipolar switching configuration of the antenna tuning capacitors is necessary due to difficulties in producing an ideal HV bi-directional switch in silicon. For exactly symmetrical positive and negative excursions of V_{SWP} and V_{SWN}, the tuning capacitors C_P and C_N should be precisely equal. In practice, manufacturing tolerances mean that this may not be the case. The capacitors may be manually picked to be within a minimum tolerance of one another, but this incurs cost in the manufacturing stage.

If the tuning capacitors have different values but their switching durations are made equal, the system will be unable to achieve the ideal zero-voltage switching condition, since at all points in the tuning range at least one switch will be unable to close at its corresponding supply potential. To resolve this, the switching durations must be made different, as per figure 8-61. This can be implemented by allowing V_{TUNE+} and V_{TUNE-} to be different.

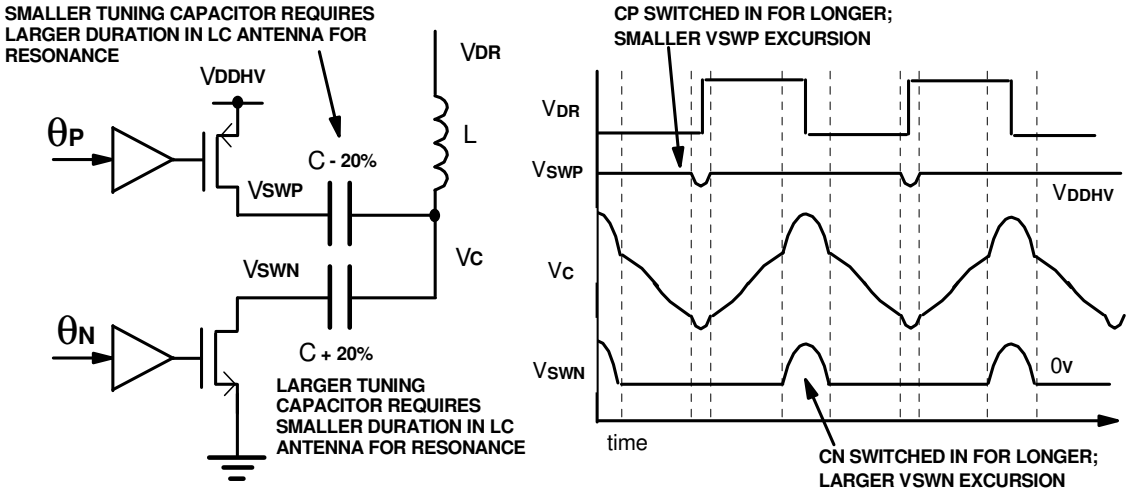

Figure 8-61: Asymmetrical switching of tuning capacitors to compensate for C_N/C_P mismatch

To allow the system to tune both switches to resonance, independent tuning loops were included, one for V_{TUNE+} and one for V_{TUNE-}. By operating independently, they could determine the optimum resonant condition for their corresponding antenna tuning capacitors.

8.4.4.3 *Control of off-chip HV switches*

The previously constructed IC contained logic outputs to indicate the state of the HV tuning switches. Whilst these were primarily for debugging and measurement, they could theoretically be used to control large off-chip HV MOSFETs for a very high voltage system. However, self-tuning required the excursions to be sensed using the on-chip $V_{SWN/P}$ connections, forcing some kind of additional voltage division to reduce the very high voltage external LC voltage to the safe 20V limits of the system. If a bipolar switch is used, additional logic is required to re-combine the off-chip $\Theta_{SWP/N}$ signals.

To facilitate future experimentation, additional logic was included so that the HV switch controls could be re-combined on chip to reduce external circuitry, as per figure 8-62. The bipolar switch control can be included as an option on one of the existing switch state indicators. Additionally, the on-chip integrators could accept an externally-driven logic signal to indicate the HV switch state, making the error detection more general to allow greater design flexibility in the off-chip error sensing circuitry.

Another external switching configuration to be explored was NMOS-only switching, i.e. only using an NMOS device to tune the circuit to resonance. This may be desirable to avoid a HV supply for a PMOS device, reducing the number of supplies needed and simplifying the HV switch driver circuits. With the proposed independent tuning loop control, this feature could be added quite easily, by simply providing a control line to lock the PMOS switch closed. The NMOS switch will naturally tune the circuit to resonance by meeting the zero-voltage switching criterion.

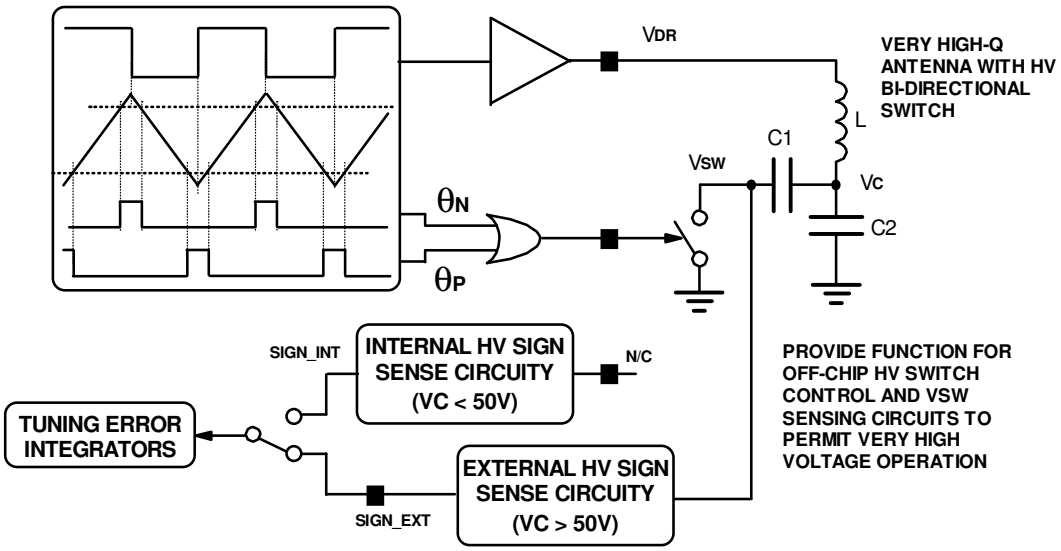

Figure 8-62: Asymmetrical switching of tuning capacitors to compensate for C_N/C_P mismatch

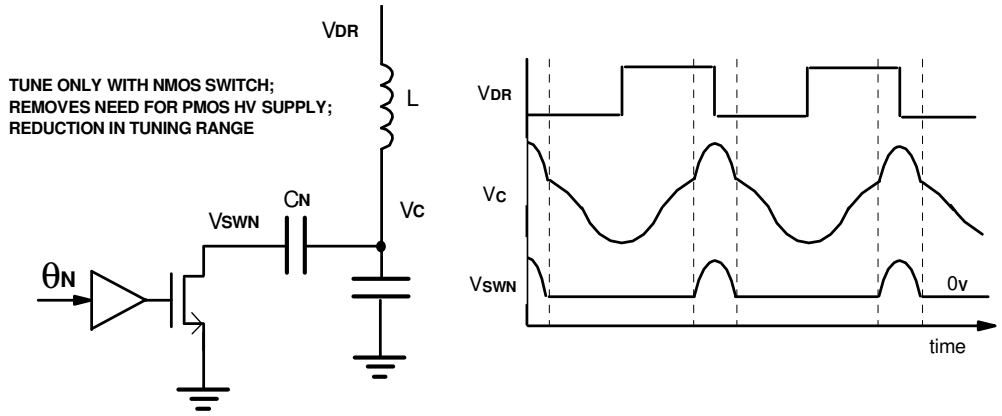

Figure 8-63: Asymmetrical switching using only NMOS switch

Sub-block	Change	Reason	Summary
Capacitor switches	Error sample phase trimming	Future experimentation	Trim phase of V_{SW} sign sampling for more accurate self-tuning
Capacitor switches	LDMOS devices	Process change	Design gate drivers for new devices
Error integrators	Independent $V_{TUNE+/-}$ loops	Future experimentation	Independent tuning loops for $C_{N/P}$ switching to compensate mismatch
Error integrators	NMOS only / bi-polar switching	Future experimentation	Different error detection logic for different antenna tuning methods
Error integrators	Accumulator approach	Improved functionality	Change to adder/subtractor for greater gain flexibility
Error integrators	Phase trim value clamp logic	Improved functionality	Prevent overflow/underflow in phase-trimmed tuning settings
Error integrators	Multiple tuning loops	PSK modulation	Independent tuning loops needed for nominal, lead and lag frequencies
Slice comparators	NMOS only / bi-polar switching	Future experimentation	Additional switching configurations to tune external LC antenna
Switch sampler	Capacitive divider	Process change	Change capacitive divider due to original device being unavailable
Voltage DACs	Multiple V_{TUNE} external IO	Improved functionality	Make all V_{TUNE} voltages independently observable.
Voltage DACs	More voltages	PSK modulation	Three pairs of V_{TUNE} required

Table 8-10: Summary of new system features and changes

8.4.5 Slice Comparators and voltage DACs

The standalone comparator blocks developed for the first IC could be re-used in this design, since there was to be no increase in the maximum operating frequency or triangle peak-peak voltages. The only new requirement was that the comparators need to have three sets of thresholds, for the nominal, slow and fast frequencies. There was still a requirement for phase trimming of the HV capacitor switch action, so each switch required two comparators.

Ideally, the comparators for the tune switches should be configured as per figure 8-64, to reduce area and power consumption. For this to operate correctly, the voltage at the input of the comparator should switch quickly between references, in order to prevent false detection against the triangle wave. In practice there is a RC time constant with the thermometer DAC resistance and comparator input capacitance, as shown in figure 8-65. This constrains the settling time of the DAC, hence constrains the maximum operating frequency.

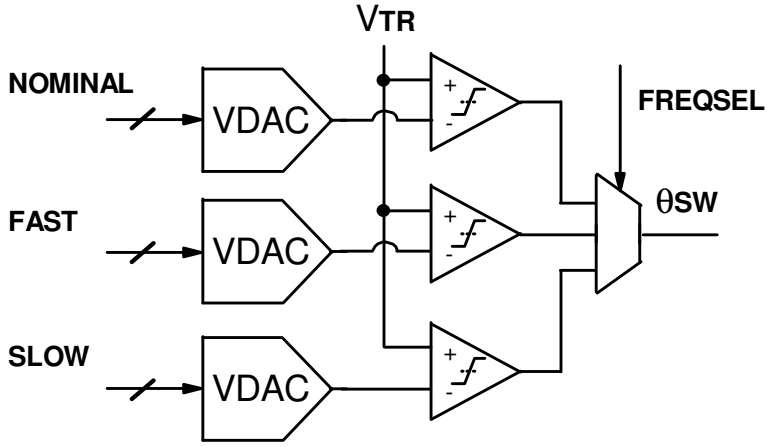

Figure 8-64: Voltage DAC and slice comparator with selectable input code for different operating frequencies

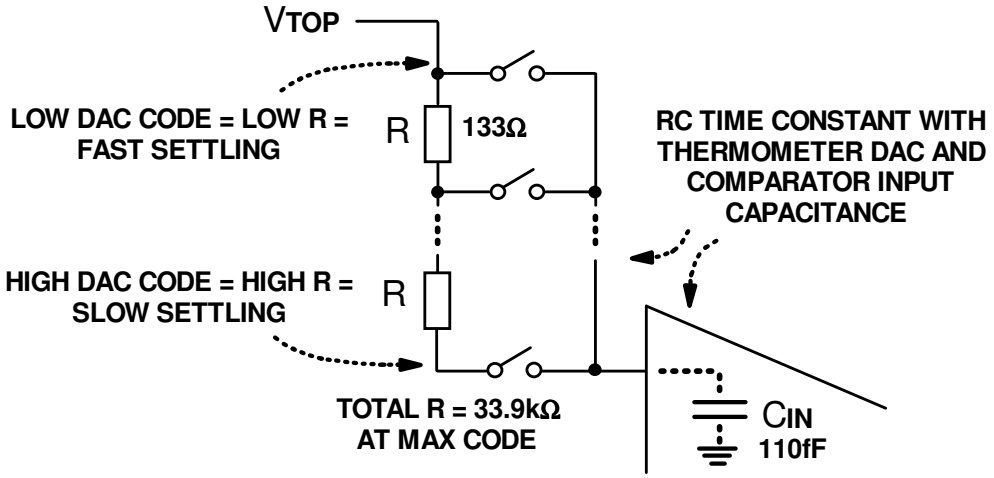

Figure 8-65: Tune voltage delay from RC time constant on DAC (left) and comparator (right)

The worst case settling time of a step input can be found by calculating the RC time constant between the Voltage DAC (a resistive string) and the input capacitance of the comparators. The worst possible step is from the lowest code to the highest, which could feasibly occur where the operating frequencies are at opposite ends of the LC tank tuning range. From extracted layout simulation, the maximum resistance of the DAC is 33.9kΩ and input capacitance of the comparator is 110fF. Including the propagation delay of the DAC logic and additional parasitic capacitances in the layout, the total settling time for a code step from minimum to maximum is 863.7ns. To create less than 1^{O} of phase error at the

maximum triangle frequency of 2MHz, this settling time needs to be 5ns, hence the approach of a code step and the DAC input will fail this requirement by a significant margin.

For a faster switching time, multiple DAC outputs and comparators were required, with a multiplex on the outputs to select the correct switch control for the operating frequency in use. To reduce development time, it was necessary to use multiple copies of the entire DAC as per figure 8-66, creating an area penalty of approximately 3x compared to the ideal approach in figure 8-64. The worst-case time required for switching between tuning settings was reduced to the switching time of the multiplexer (approximately 142ps on the slowest PVT corner), which is comfortably within the 5ns requirement.

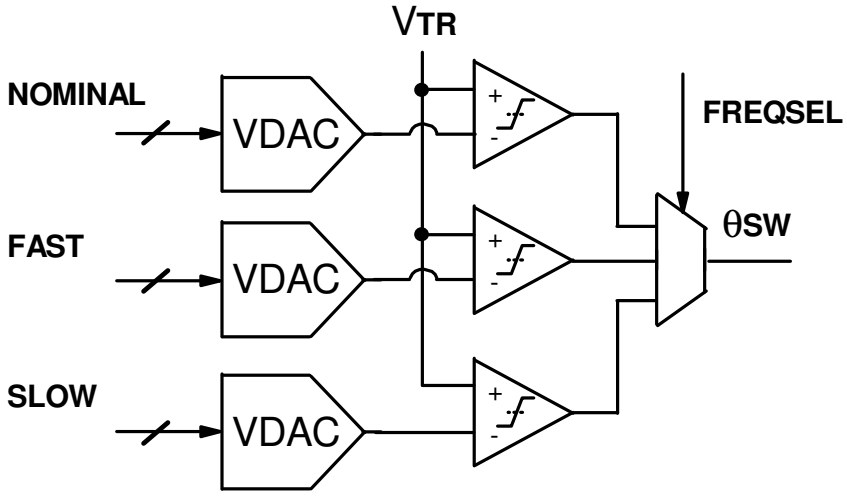

Figure 8-66: System-level DAC architecture with improved settling time

Additional logic was added to provide the NMOS-only and bipolar switch functionality, the logic given in the complete voltage DAC and slice comparator diagram figure 8-67. Note that a high state on θ_{SWP} and θ_{SWN} indicates that the corresponding switch is closed. For the NMOS-only mode, θ_{SWP} is held in the closed state with an OR gate to the *LOCKPMOS* control. For bi-polar switch mode, θ_{SWN} is connected to both the V_{TUNE+} and V_{TUNE-} slicing outputs, using the *DOUBLENMOS* control, so that it activates twice per cycle. Correct operation at 2MHz in normal mode, and *LOCKPMOS* and *DOUBLENMOS* modes is shown in figures 8-68, 8-69 and 8-70 respectively.

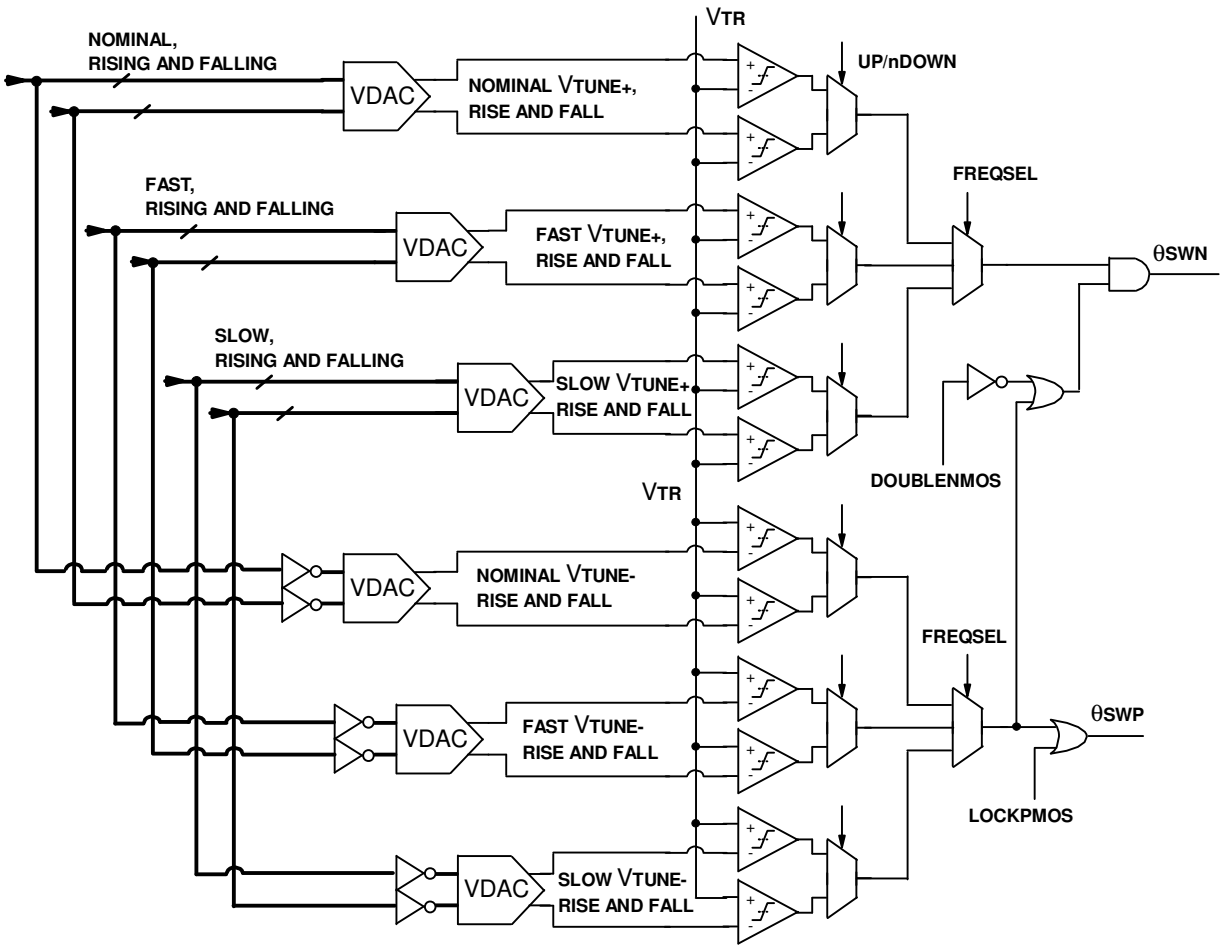

Figure 8-67: System-level DAC architecture with improved settling time

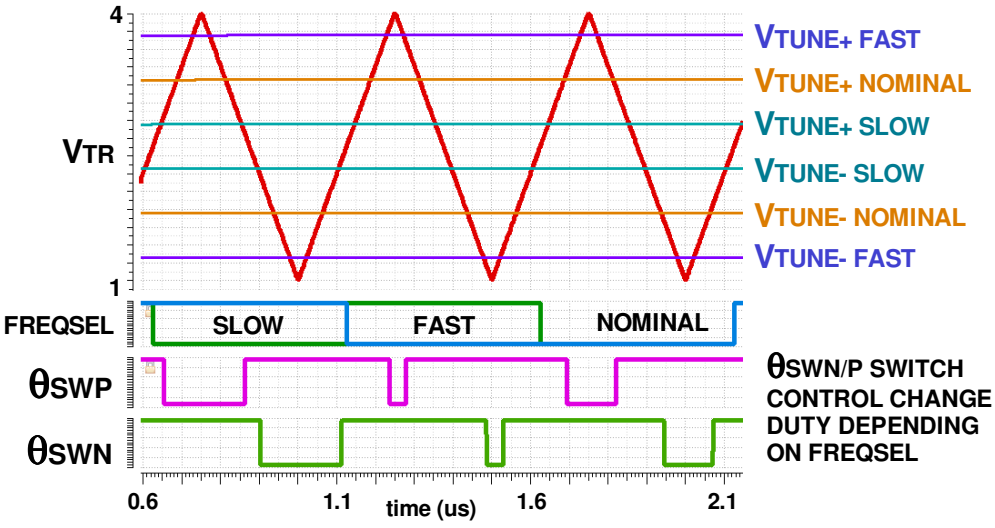

Figure 8-68: Slice comparator operation at different *FREQSEL* settings

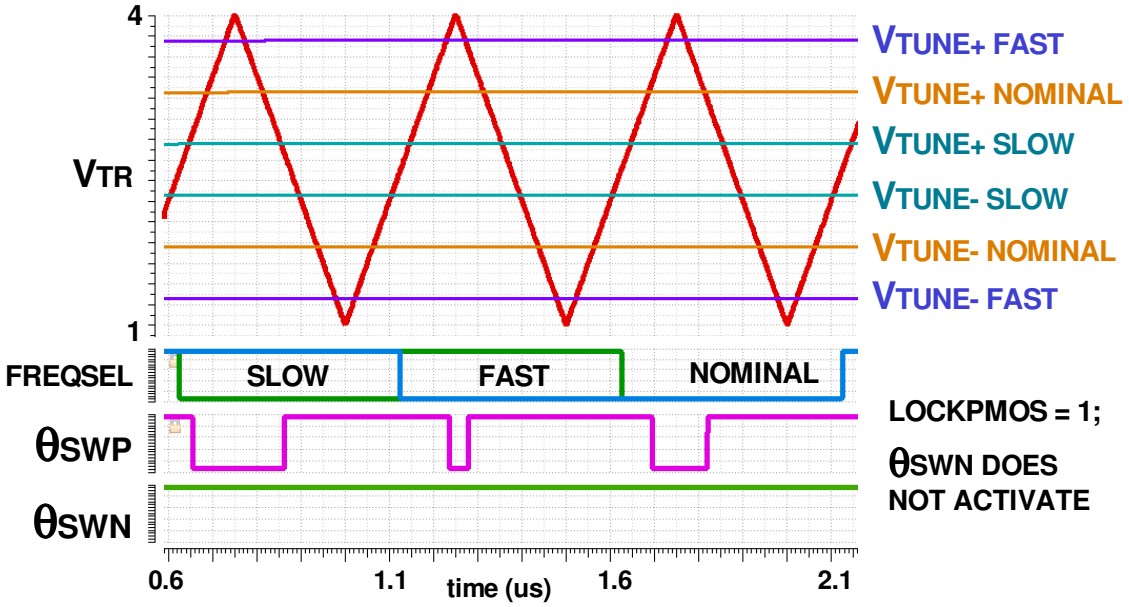

Figure 8-69: Slice comparator operation at different *FREQSEL* settings with *LOCKPMOS* enabled

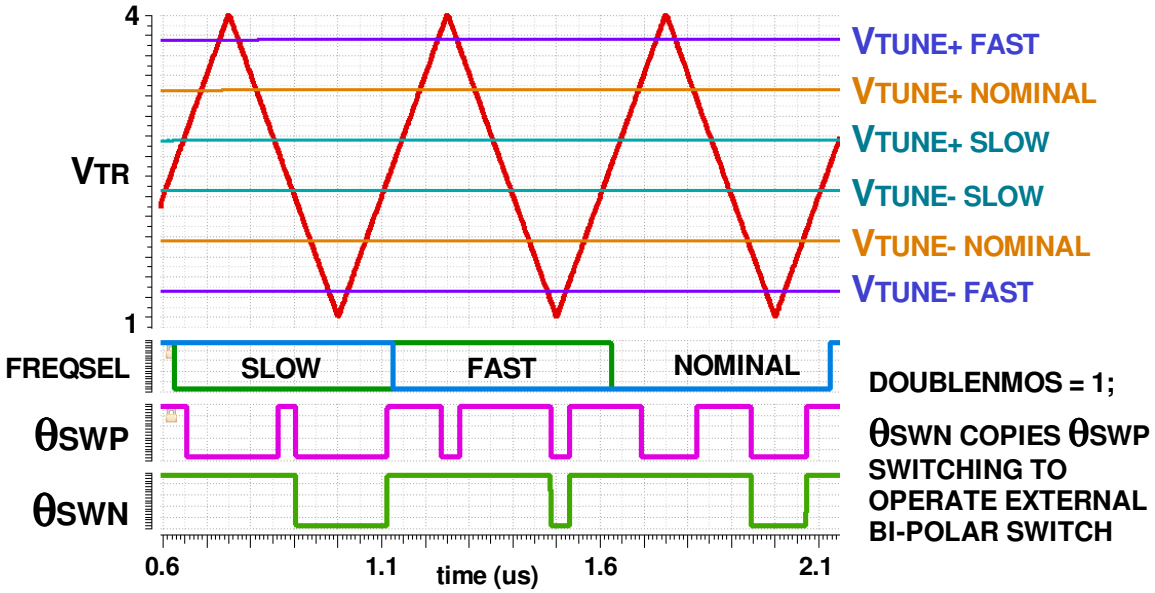

Figure 8-70: Slice comparator operation at different *FREQSEL* settings with *DOUBLENMOS* enabled

To allow the slice voltages to be set and observed externally, a set of analogue switches were added to fulfil this requirement, shown in figure 8-71. This allows the comparators to use either an internal or external voltage (using the *SLICEMODE* control), and also the internal voltages to be made visible externally for debug purposes (using the *PASSTHROUGH* control). There is also functionality to determine if the rising or falling edge voltages should be passed through (using the *PASSTHROUGH_SEL* control), allowing verification of the phase trimming voltages. The final layout of the voltage DACs, slice comparators and associated logic are shown in figure 8-72.

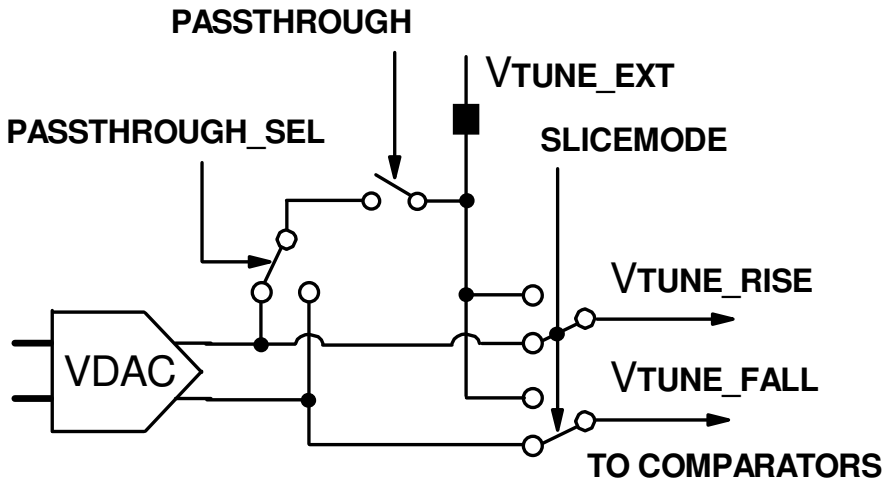

Figure 8-71: Comparator reference selection switch configuration

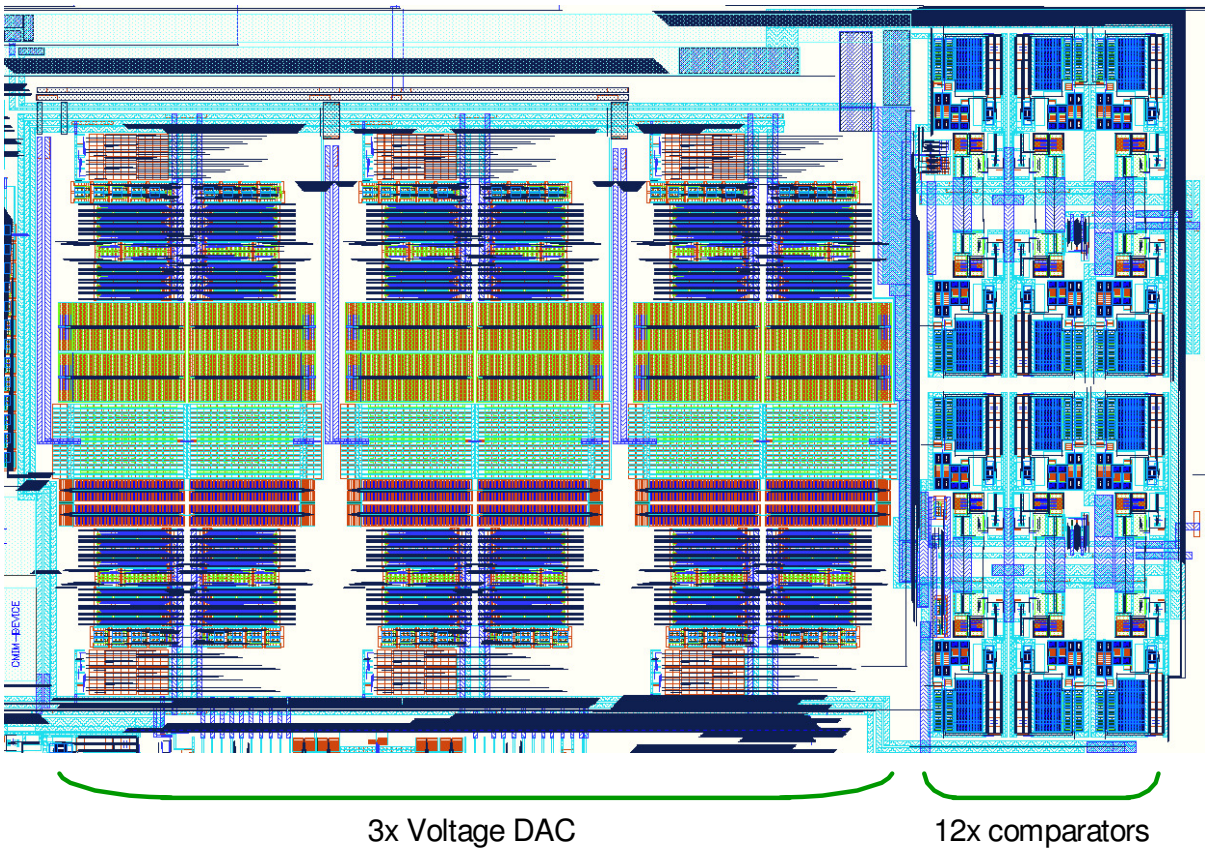

Figure 8-72: Layout of voltage DACs and switch control comparators

8.4.6 Tank Driver

The previous design used a 5V level driver for the external LC tank circuit, which often required to the use of a lossy attenuator or reduction in the operating Q factor in order to protect the HV switches. The driver also shared the digital 5V supply, meaning the amplitude could not be easily varied. For this design, it was decided to use a variable drive made from 1.8V devices, in order to allow greater flexibility during testing whilst still protecting the capacitor switches from excessive voltages.

The previous driver had resistances of 2.03Ω and 2.33Ω for the NMOS and PMOS respectively. To maintain a high Q, these were not to be exceeded in the new design. The driver should also support at least the same RMS load current of 100mA. At minimum length, the calculated required widths for

NMOS and PMOS were 729µm and 2.186mm respectively. Figure 8-73 shows the driver circuitry used, with a x3 change in strength between adjacent stages for a near-optimal trade-off between the drive strength and input capacitance of each stage [41]. The gates of the final drive devices are rated to 1.8V, hence it was not necessary to use any additional level shifting in order to reduce the driver supply.

Since the supply was made variable, it was necessary to check the variation of the propagation delay with varying V_{DDDR} under load. An LC circuit resonant at 2MHz with a Q factor of 50 was used to model a realistic load. At 1.8V, the nominal propagation delay of the extracted layout was 767ps, which is sufficient the avoid significant delay at the maximum operating frequency of 2MHz. Figure 8-74 shows the delay increasing exponentially as the supply is reduced towards the threshold of the PMOS device (0.405V nominal), below which the driver ceased to function correctly.

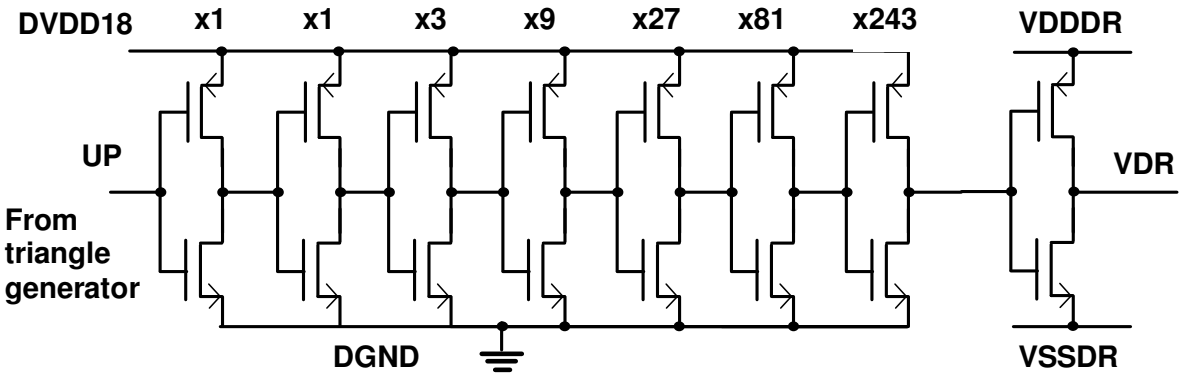

Figure 8-73: 1.8V tank driver chain

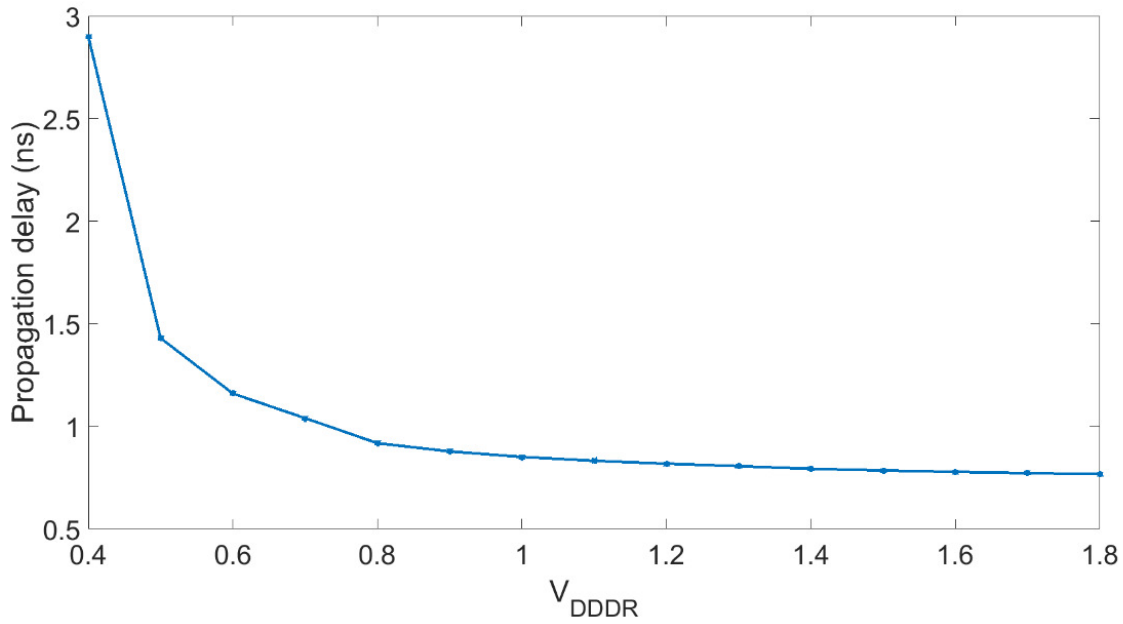

Figure 8-74: Tank driver propagation delay vs V_{DDDR} potential

8.4.7 Capacitor Switches

Shortly after the previous IC was fabricated, the list of available devices from AMS was changed. The 20V V_{GS} rated LDMOS FETs used in the first design were no longer available. The previously implemented NMOS switch was already operating on a 5V mid-oxide V_{GS}, hence little adjustment was needed for the process change. However, the restriction of a 5 PMOS V_{GS} limit necessitated greater change to the corresponding switch driver. Since the resulting switches themselves require layout changes, the opportunity was taken to move to 50V V_{DS} rated NMOS and PMOS devices. This

permitted a greater V_C peak-peak amplitude of 100V. With a driver amplitude of 1.8V, an external tank Q of over 50 could be supported with no additional protection or attenuation required.

The available devices had thin (1.8V) and medium (5V) oxides. For safety, it was decided to use the mid-oxide devices, in order to minimise the chance of destructive voltage levels on the gates occurring during power up from cold start. Driving the NMOS was straightforward, as this is referred to ground and the substrate potential.

To drive the PMOS switch safely, the gate must not exceed more than 5V relative to the source. Hence a 5V drive level is required, but at the HV supply and a second HV supply which is set 5V lower. To reduce development time, this supply was provided off chip, however the drive chain still required development. To shift from 0/5V to 45/50V logic levels, the θ_{SWP} signal is capacitively coupled between two inverters, one on the 5V logic supply and another on a dedicated 45/50V supply, as per figure 8-75.

The driver devices in the HV domain are NFETIM/PFETIM types in the process. The active areas of these devices are isolated from the substrate and permit a well-substrate potential of up to 50V. Hence the source and drain terminals inside the well may float above the substrate potential. The FETs in this domain otherwise operate like 5V devices, with similar μC_{OX} parameters to the NFETM/PFETM equivalent devices used in the 5V domain.

The coupling capacitor forms a capacitive divider with the C_{GS} at the input of the strong inverter in the HV domain on the $V_{SHIFTIN}$ node. Hence it must be large enough in order to avoid reducing the amplitude of the coupled $V_{\theta SWP}$, thereby preventing the strong inverter from operating. From simulation on PVT corners, it was found that the minimum size of this coupling capacitor for correct operation was approximately 150fF, hence a value of 300fF was used to guarantee correct operation on all corners and tolerances.

Since the switch control signal must have a well-defined value, i.e. high or low, a weak inverter is used to provide positive feedback from $V_{SHIFTOUT}$ to $V_{SHIFTIN}$. A rising or falling edge from $V_{\theta SWP}$ to $V_{SHIFTIN}$ via the coupling capacitor causes $V_{SHIFTOUT}$ to transition from high or low respectively via the strong inverter. The weak inverter is then triggered by the change in $V_{SHIFTOUT}$, pulling $V_{SHIFTIN}$ towards the respective low or high supply. The weak inverter is implemented in near-minimum dimensions, since it only needs to provide a weak connection to keep the value of $V_{SHIFTIN}$ well defined once the transient edge of a change in $V_{\theta SWP}$ has passed. Figure 8-76 shows the rising and falling edges of the levelshifter for correct operation of V_{SWP} with respect to θ_{SWP}, using a 100Ω load resistor to ground on V_{SWP}.

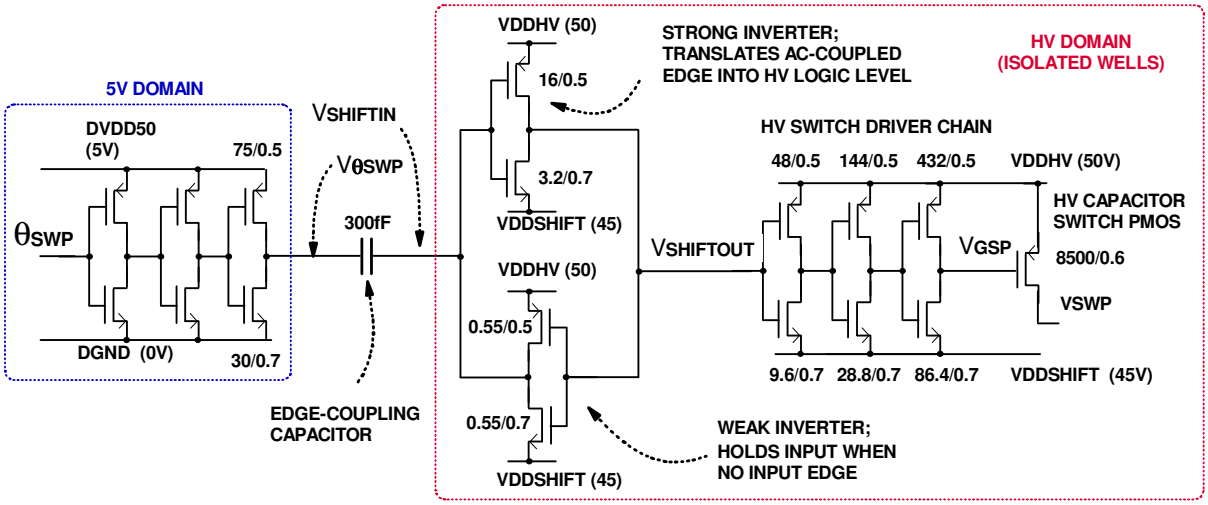

Figure 8-75: Circuit diagram of HV levelshifter for 50V mid-oxide PMOS HV switch

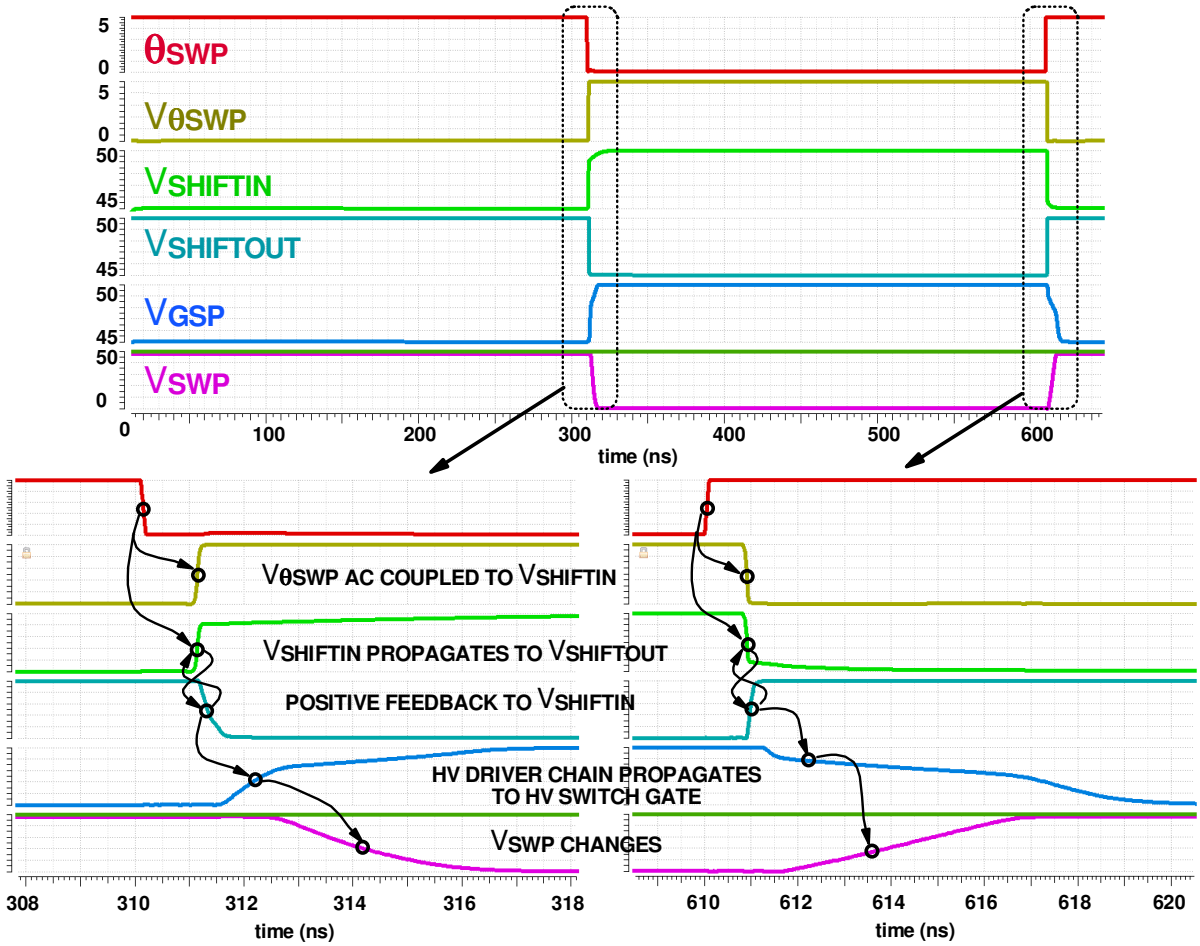

Figure 8-76: Operation of HV levelshifter and driver for 50V PMOS switch (opening on bottom left, closure on bottom right)

On PVT corners, the worst propagation delays for the HV NMOS/PMOS switch chains were 5.18ns/3.47ns respectively, both acceptable for creating negligible timing offset. In the previous design, the switch voltage excursion sign sampling was triggered from the same control as that for the switches, with a small time delay inserted into the switch control to ensure that sampling always occurs before switch closure. In practice, the time delay is subject to PVT skew, so the option to trim the delay is desirable, especially as the operating frequency is increased and this delay becomes more significant.

To provide experimental trimming of the sample point, additional timing options were created, selected with a multiplexer as per figure 8-77. The default option remained as a direct trigger from $\theta_{SWP/N}$, with signals derived from the gates of the HV switches for a later trigger. Additional delays of up to 2ns and 6ns are also included to account for information propagation in the sign detector comparator, i.e. valid sign data still propagating through the comparator after the HV switch has already closed.

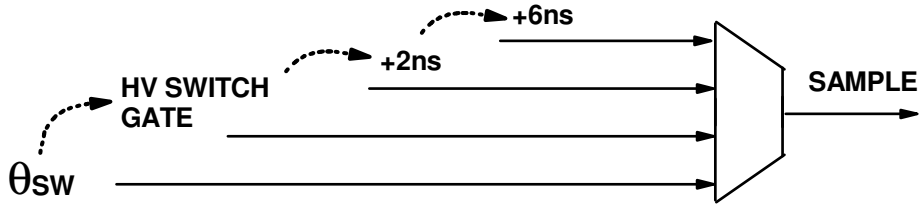

Figure 8-77: HV switch sample control trimming options

8.4.8 Switch Sign Sampler

As per the first design, the sampling of the sign of the HV switch voltage excursions just before closure was implemented using a capacitive divider, allowing the safe re-use of a standard comparator cell. However, further simulation of the cell, shown in figure 8-78 revealed non-ideal operation of the buffered comparator reference V_{DDO2}. It was found to be crudely tracking the HV capacitor switch $V_{SWN/P}$ voltage excursions, due to the buffer having too much output impedance. The divided HV excursions V_{SWN/P_DIV} eventually cross V_{DDO2} to produce correct voltages at the comparator input, however there is insufficient time for this to propagate through the comparator. Hence the sampled sign upon switch closure is not always correct, creating a tuning error.

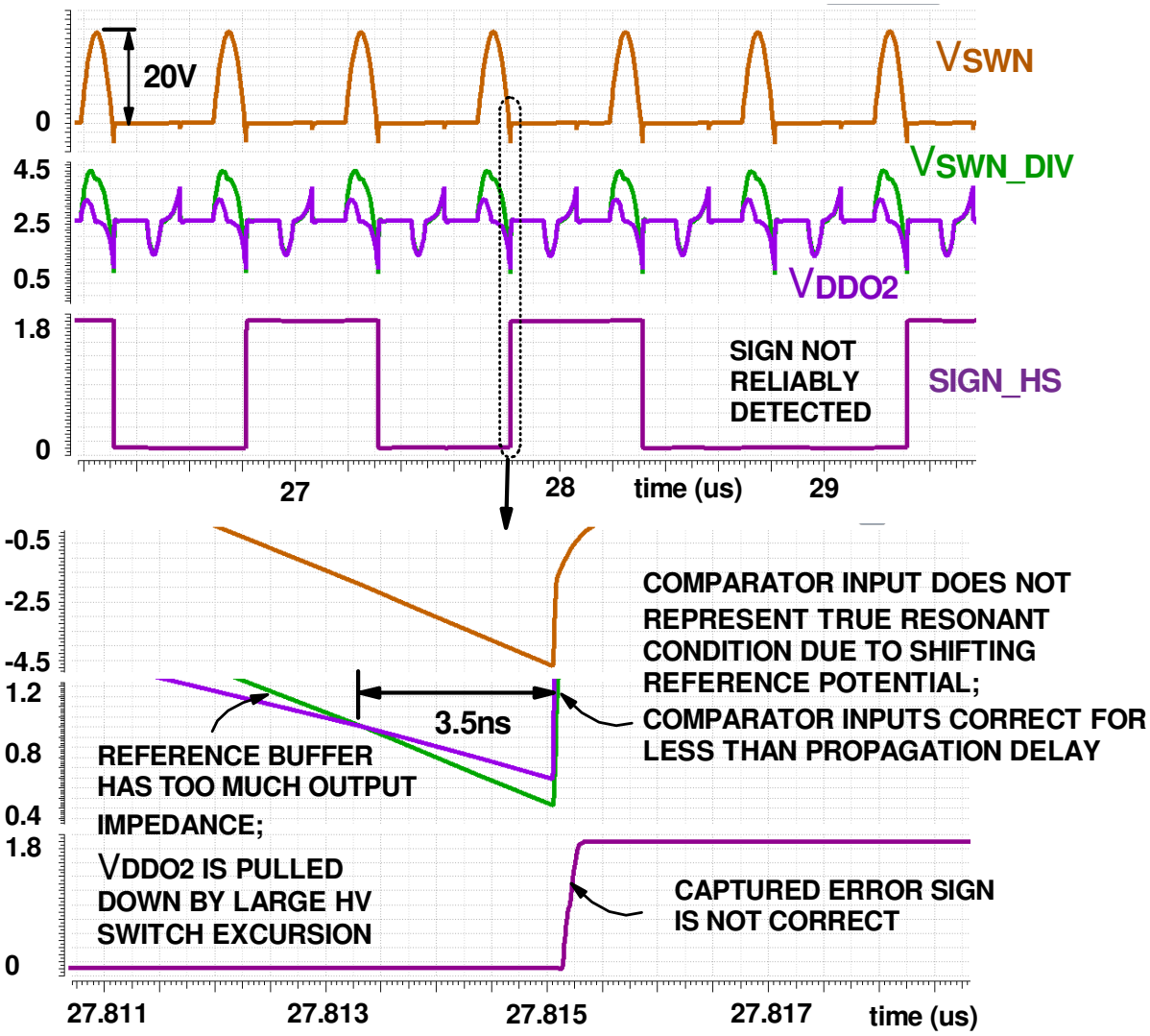

Figure 8-78: HV switch sampler tuning error at 2MHz created by variation of closed-state reference potential

Whilst the overall contribution to the tuning error was small, this problem had an increasingly significant effect as the operating frequency was increased. At higher frequencies, the impedance between the HV excursions and V_{DDO2} is reduced, meaning the buffer has to provide additional current to keep V_{DDO2} stable compared to lower frequencies.

Figure 8-79 shows the considered solutions to this problem. The first was to simply decrease the output impedance of the buffer (option 1), however this would only mitigate the amount of variation in V_{DDO2} and not remove it completely. Alternatively, the comparator input could be shared with the reference for the V_{DDO2} buffer (option 2), however, this is sensitive to input-output offset of the buffer, creating a new source of tuning error.

The buffered supply can instead be sampled and held at the comparator input during the closed state of the switch (option 3). This allows comparison with the true switch-closed potential, whilst avoiding the need for the design of a new buffer, hence this option was chosen to solve the tuning error problem.

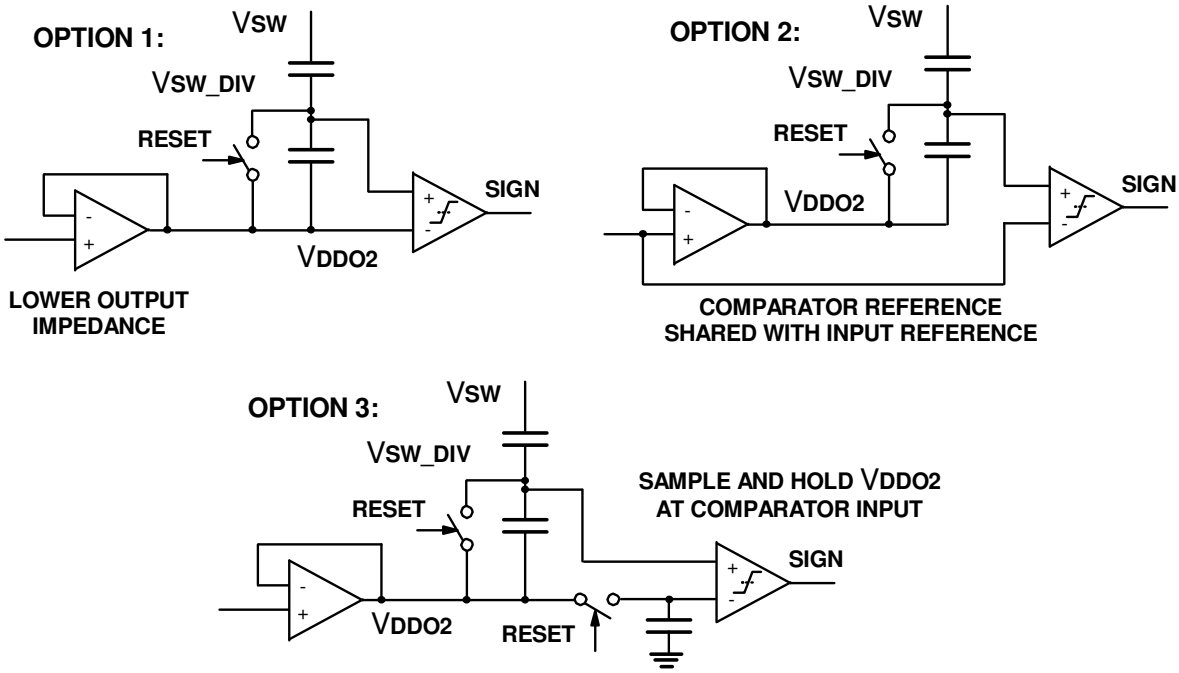

Figure 8-79: HV switch sample circuit options for accuracy improvement

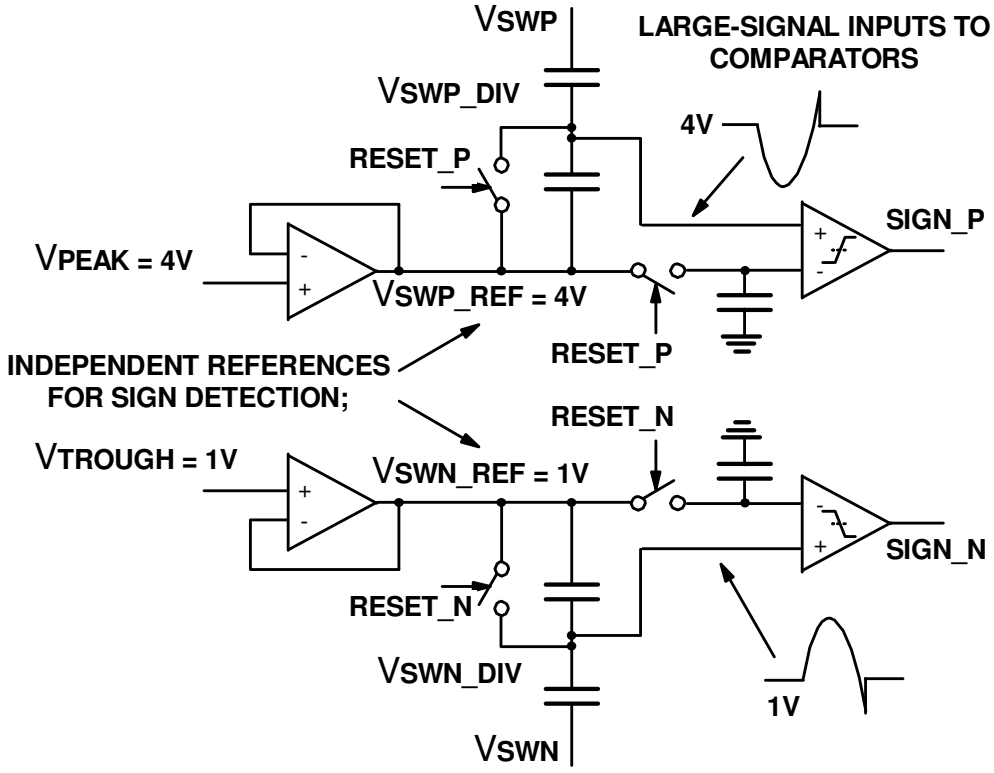

Figure 8-80: HV switch sample circuit with sample-hold on comparator inputs and independent references

At the highest frequency setting, the HV switches are each open for almost 50% of the period of oscillation. Hence the V_{DDO2} reference on a single buffer may have insufficient time to restore the switch potential to a well-defined potential. This problem can be seen in figure 8-78, where the V_{DDO2} reference

is being perturbed by the HV excursion of V_{SWP}. If the reference is not settled before the opening of the opposite excursion, then the sampled and held reference at the comparator input will not represent the switch-closed state.

To solve this problem, two independent reference supplies were used as per figure 8-80, so that each has at least 50% of a cycle (250ns at 2MHz maximum frequency) to restore the comparator input and capacitive divider potential. Having separate references allows the voltages to be different, i.e. V_{SWN_DIV} compared against 1V and V_{SWP_DIV} compared against V_{SWP_DIV}. This permits larger amplitudes on the HV switches without changing the capacitive divider ratio for error measurement, permitting large-signal comparison at the comparator input to reduce the effect of offset error. Figure 8-81 shows the improved circuit operating with the same HV switch excursions, correctly detecting the error sign.

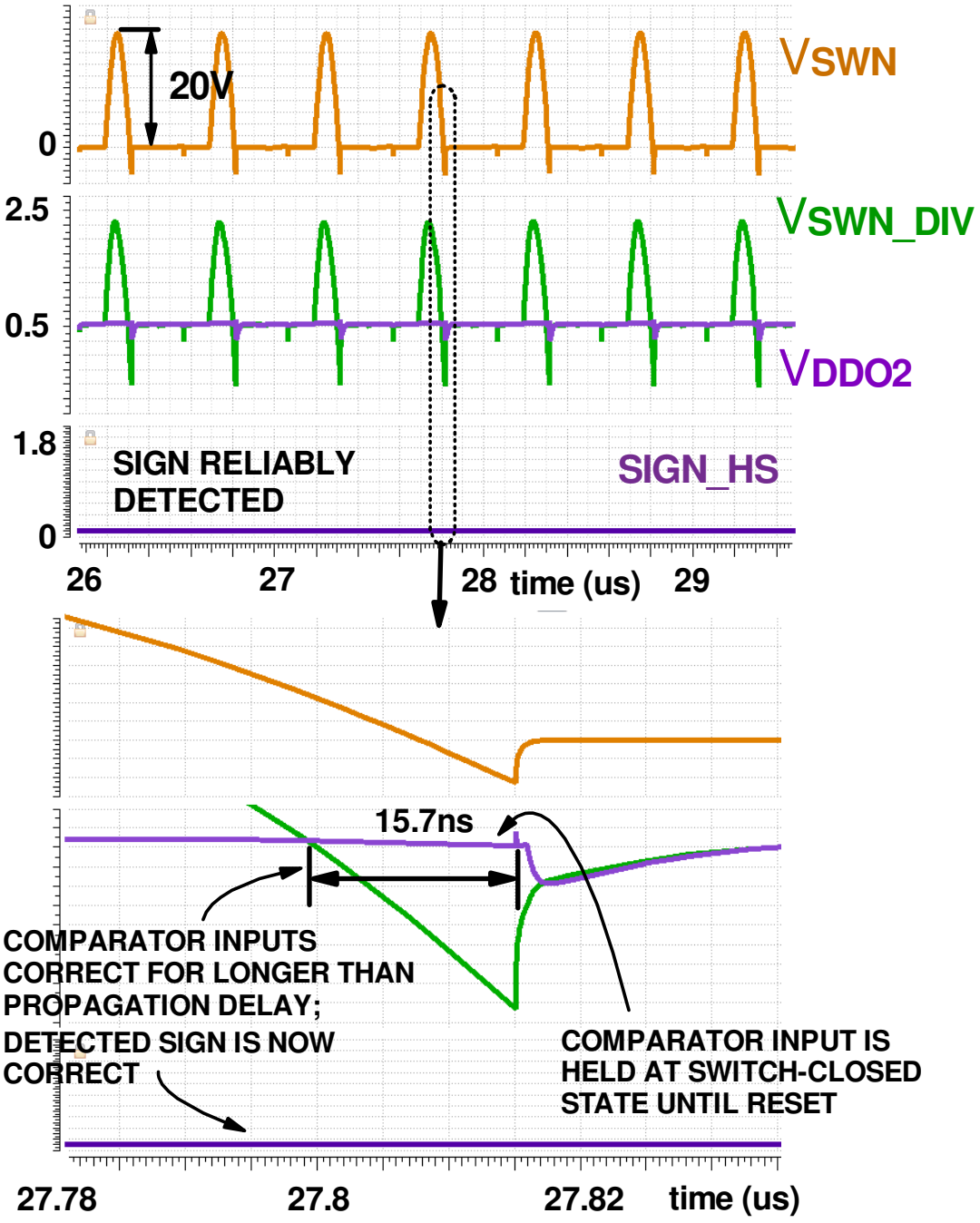

Figure 8-81: HV switch sample circuit accuracy improvement using sample-hold method

8.4.9 Digital Integrators

The architecture for the digital integrators for setting the V_{TUNE} levels from the sampled sign of V_{SWN} from the previous design formed the basis of the next, with some improvements. The development of a digital accumulator for the PSK phase measurements provided a convenient block to re-use for tuning by sign detection, with the additional advantage of greater flexibility on the gain control (i.e., specifying an exact integer value for phase shifting, rather than a coarse left/right shift multiplier). The 16-bit architecture also permitted the option of a very low unit gain for a very smooth tank tuning response.

In the previous design, phase trimming was implemented as an adder/subtractor block on the output of the digital integrators, with no overflow/underflow prevention. Hence it was possible to cause the slice voltage levels to wrap-around and cause incorrect tuning. In this design, the 16-bit accumulator has built-in overflow/underflow prevention, hence this was re-used to implement phase trimming as part of the digital integrators. Figure 8-82 shows the design of one integrator block. Note that *PRELOAD_VAL[7:0]* (manual digital tuning setting), *TRIM_VAL[7:0]* (amount of phase trimming in terms of DAC codes) and *GAIN[7:0]* (the integrator increment/decrement step) are padded in order to operate with the 16-bit architecture. The padding arrangements are given in table 8-11.

Logic was included so that an overflow in the phase-trimmed tuning value is masked from the output of the integrator, by instead selecting the last-known good value. If the integrator for one edge of V_{TR} experiences a clamp condition due to overflow, this is indicated by *TRIMCLAMP_OUT*, which connects to the *TRIMCLAMP_IN* input of the integrator for the corresponding edge. Without this protection, the integrator for the opposite edge comparison on V_{TR} may continue to vary in output value, altering the phase trimming position of the capacitor switching signals. This problem is demonstrated in figure 8-83. When the clamp condition passes, i.e. the sampled switch voltage sign changes, *TRIMCLAMP_OUT* is de-asserted and both integrators are able to continue operating as normal.

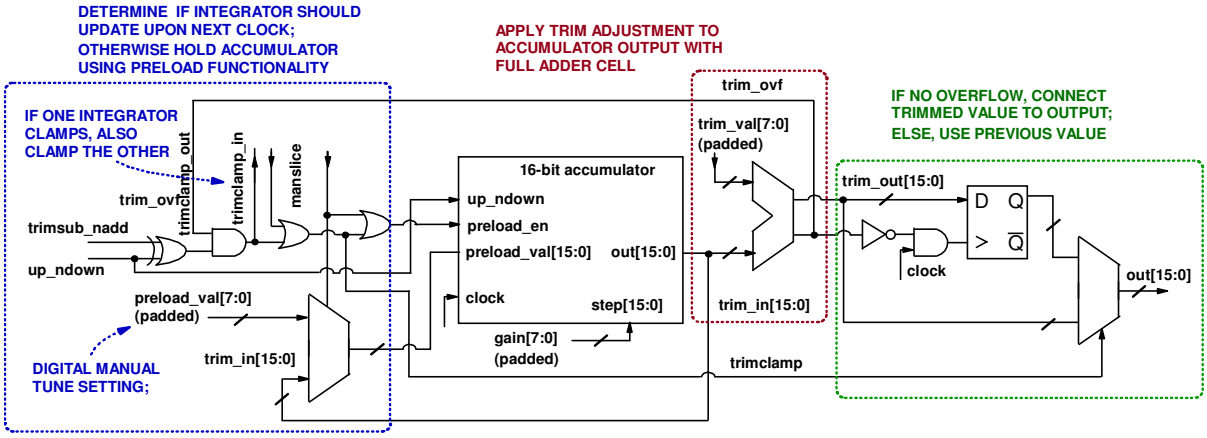

Figure 8-82: Digital integrator with phase trimming and overflow protection

Input	Padding format	Reason
Gain	00, GAIN[7:0], 00 0001	MSBs = 00 for maximum integrator gain LSB = 1 for very slow integration
Preload_Val	PRELOAD_VAL[7:0], 0000 0000	8 MSBs taken for DAC code
Trim_Val	0, TRIM_VAL[7:0], 000 0000	MSB = 0 to limit trim amount to half of DAC code range

Table 8-11: Input padding arrangements for digital integrator

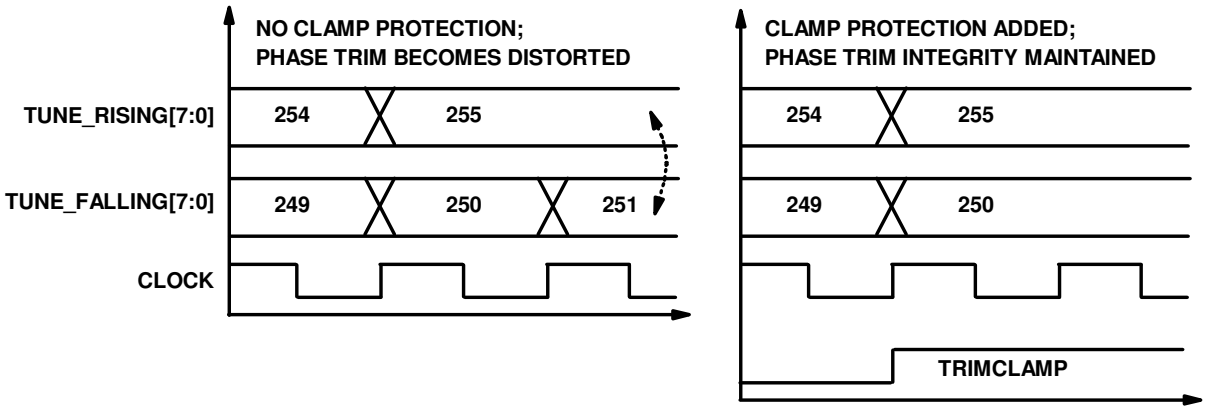

Figure 8-83: Digital integrator phase trim distortion condition (left), phase trim integrity maintained (right)

Since there were multiple operating frequencies, multiple integrator blocks were required. In addition, the requirement for rising & falling edge comparisons and independent settings for the PMOS and NMOS switches (for non-symmetrical slicing testing) meant that in total 12 integrators were needed. Integrators were paired together as per figure 8-84 to process the incoming sign data for a particular rising/falling edge of V_{TR}, for a particular N or P switch at a particular operating frequency. The integrator pairs were then arranged as per figure 8-85 to form the complete digital integrator block.

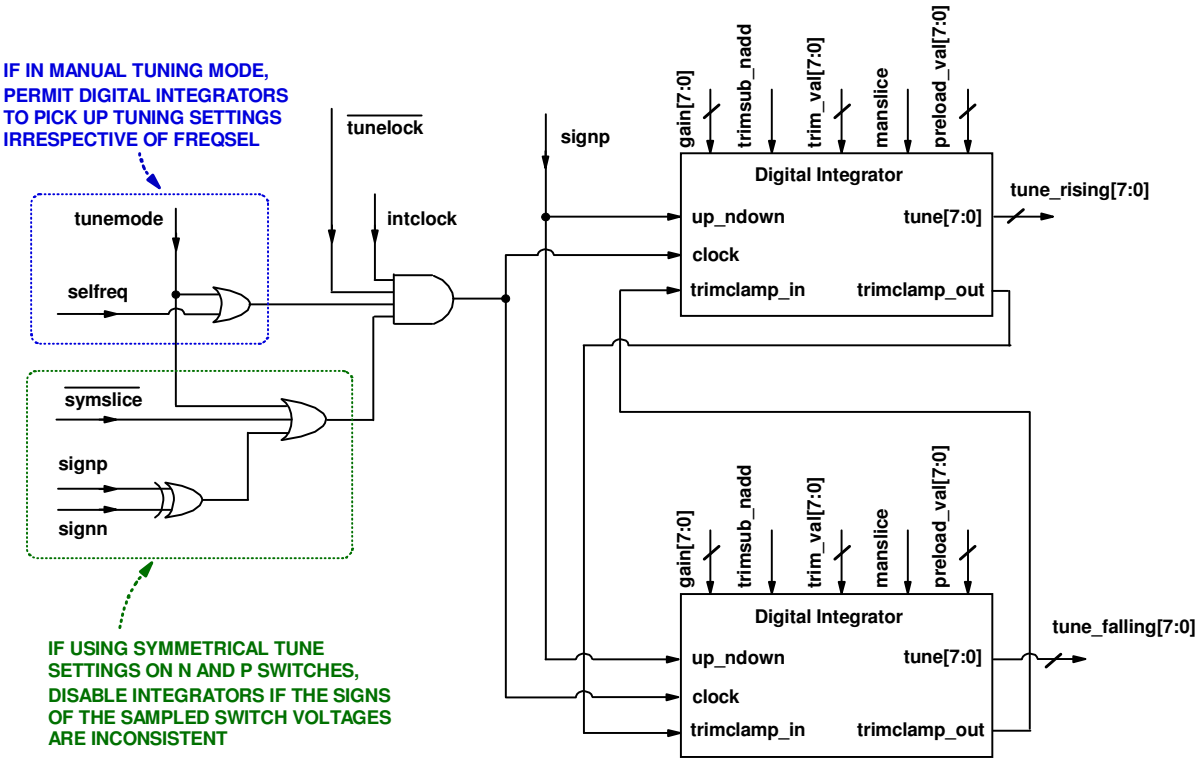

Figure 8-84: Digital integrator pair connectivity (PMOS switch example)

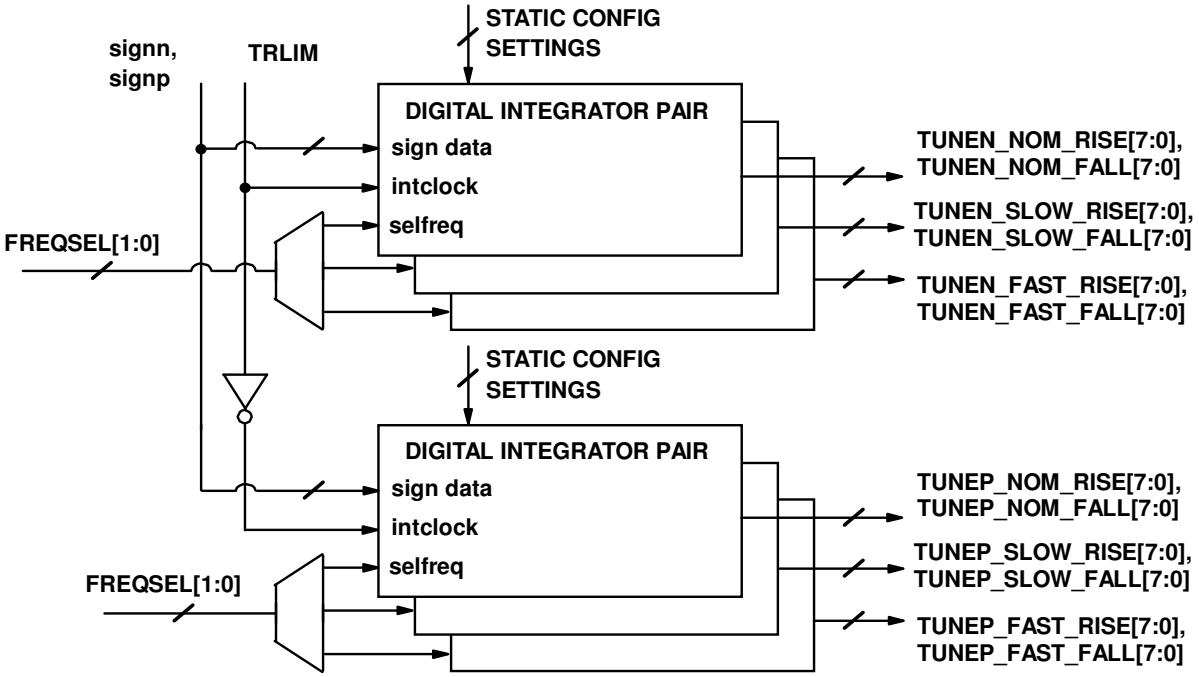

Figure 8-85: Digital integrator top level architecture

8.4.10 Digital Controller

The large number of control options for this design meant that a digital controller was necessary to store settings, as well as to permit read-out of internally-generated settings for the tank tuning and frequency calibration. In order to reduce the number of pins required, a serial IO approach using a First-In First-Out (FIFO) buffer was used as per figure 8-86, compared to the parallel approach used in the first design. The register address and 8-bit data value are clocked in together on *DATAIN* with *FIFOCLOCK*. The *LOAD* signal then either copies the 8-bit data value into the internal register or copies an 8-bit value from an internal self-calibration setting to the FIFO, depending on if the address set is for a write or read address. The FIFO contents can then be read out through *DATAOUT* with *FIFOCLOCK*. A full address map and read/write timings is provided in appendix G.

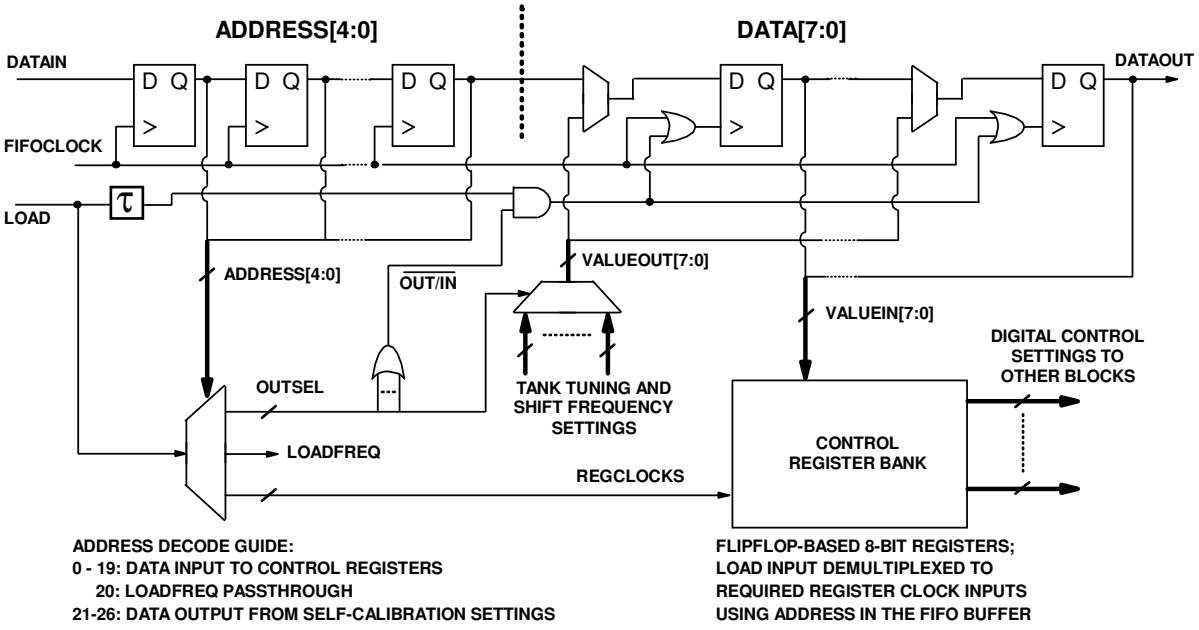

Figure 8-86: Digital setting IO and register control circuitry

8.5 Top Level Simulations

This section details top-level simulation of the architecture under nominal conditions. Given the high complexity of the system, it was necessary to replace some core blocks with behavioural equivalents to speed up simulation. This was deemed to be an acceptable trade-off, given that the individual constituent sub-blocks were tested at extracted layout level.

8.5.1 Nominal tuning behaviour

8.5.1.1 Unipolar switching

Figure 8-87 shows the system self-tuning the LC tank circuit with a low-moderate integrator gain. The LC circuit compromises of an inductor of 150µH and a Q factor of 50 at 125kHz. Resonance is achieved after approximately 1.5ms, indicated by $V_{SWP/N}$ terminating at the corresponding supply potentials, and the rising/falling edges of V_{DR} being aligned with the troughs/peaks of V_C. The system in set to symmetrical tuning mode, i.e. both $V_{SWP/N}$ have equal duration.

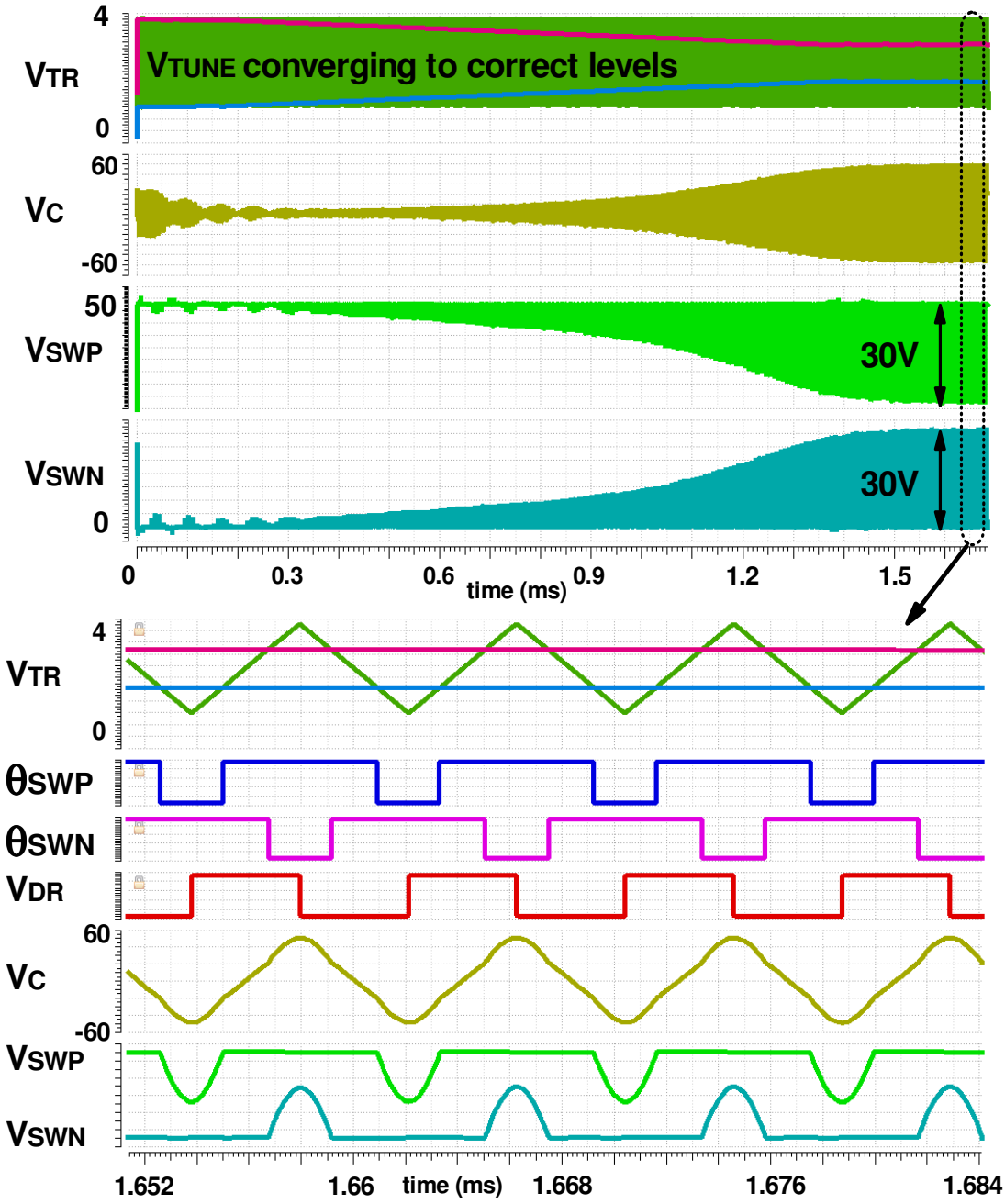

Figure 8-87: Self-tuning of LC tank at 125kHz nominal frequency, intgain = 4

8.5.1.2 Independent unipolar tuning loops

Figure 8-88 shows the system operating with independent tuning loops for $V_{SWP/N}$ calibration with a low-moderate self-tuning gain. The system converges on a resonant condition, however a closer visual inspection of the waveforms indicates that the duty cycle of switch control signals θ_{SWP} and θ_{SWN} is not the same. Both V_{SWP} and V_{SWN} terminate at their corresponding supply potentials, however the different duty cycles on V_{SWP} and V_{SWN} create an asymmetrical shape of V_C. The peaks/troughs of V_C align also with the falling/rising edges of V_{DR}, meaning that the system is resonating despite the asymmetrical switching action. The inductor current is also shown at resonance and is still essentially sinusoidal, although will contain greater harmonic content due to the uneven shape.

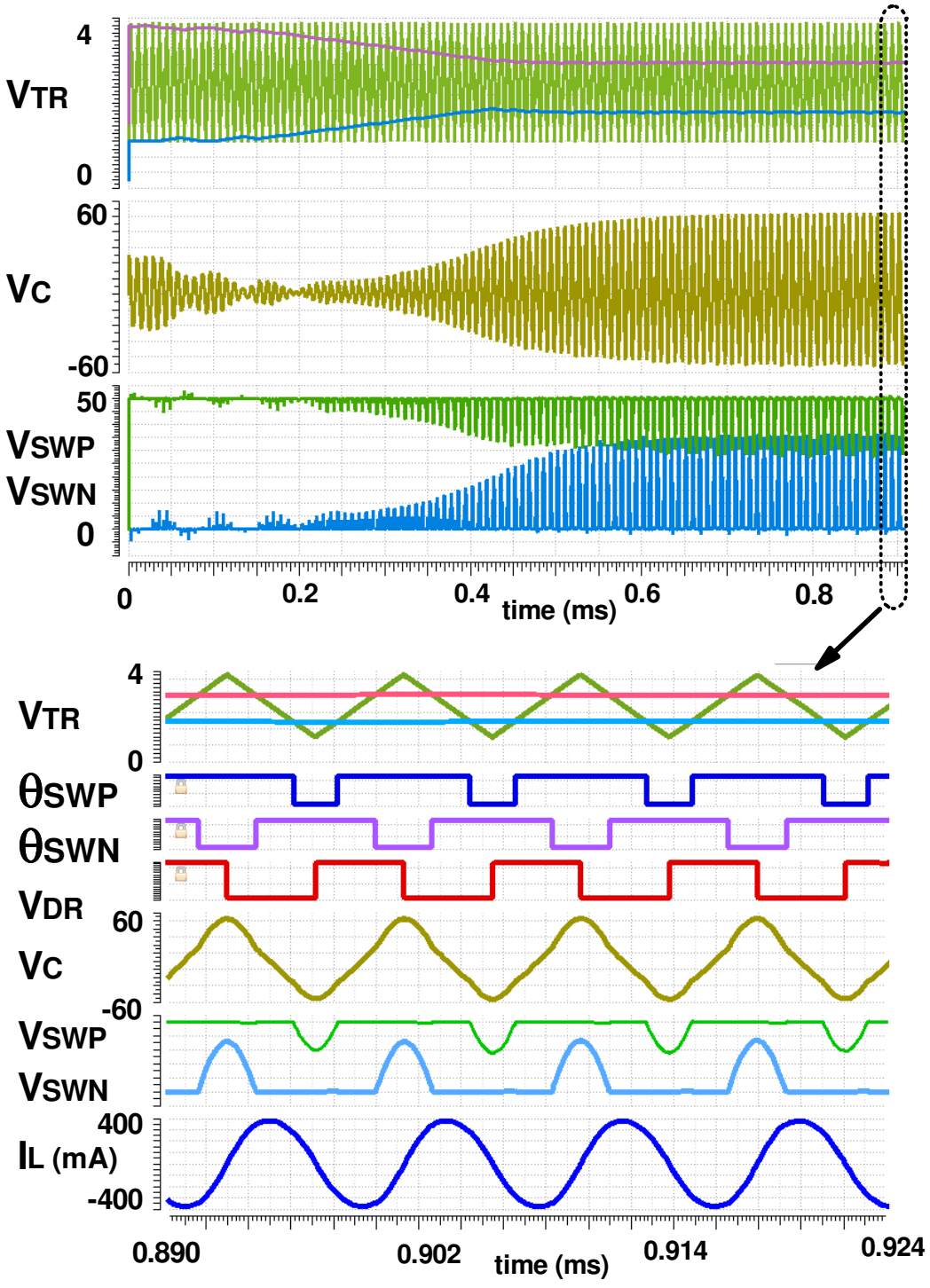

Figure 8-88: Self-tuning of LC tank at 125kHz nominal frequency with asymmetrical tune switching, intgain = 16

8.5.1.3 NMOS-Only mode

Figure 8-89 shows the system operating in NMOS-only mode. The PMOS switch is held closed by setting *LOCKPMOS* = 1 in the system registers. The system self-tunes using only the NMOS switch, creating an asymmetrical shape on V_C and I_L. The PMOS integrator does not change, since the θ_{SWP} signal is never activated. To create the correct time-averaged resonant frequency, the opening duration on θ_{SWN} needs to be larger compared to previous simulations, creating larger excursions of V_{SWN}.

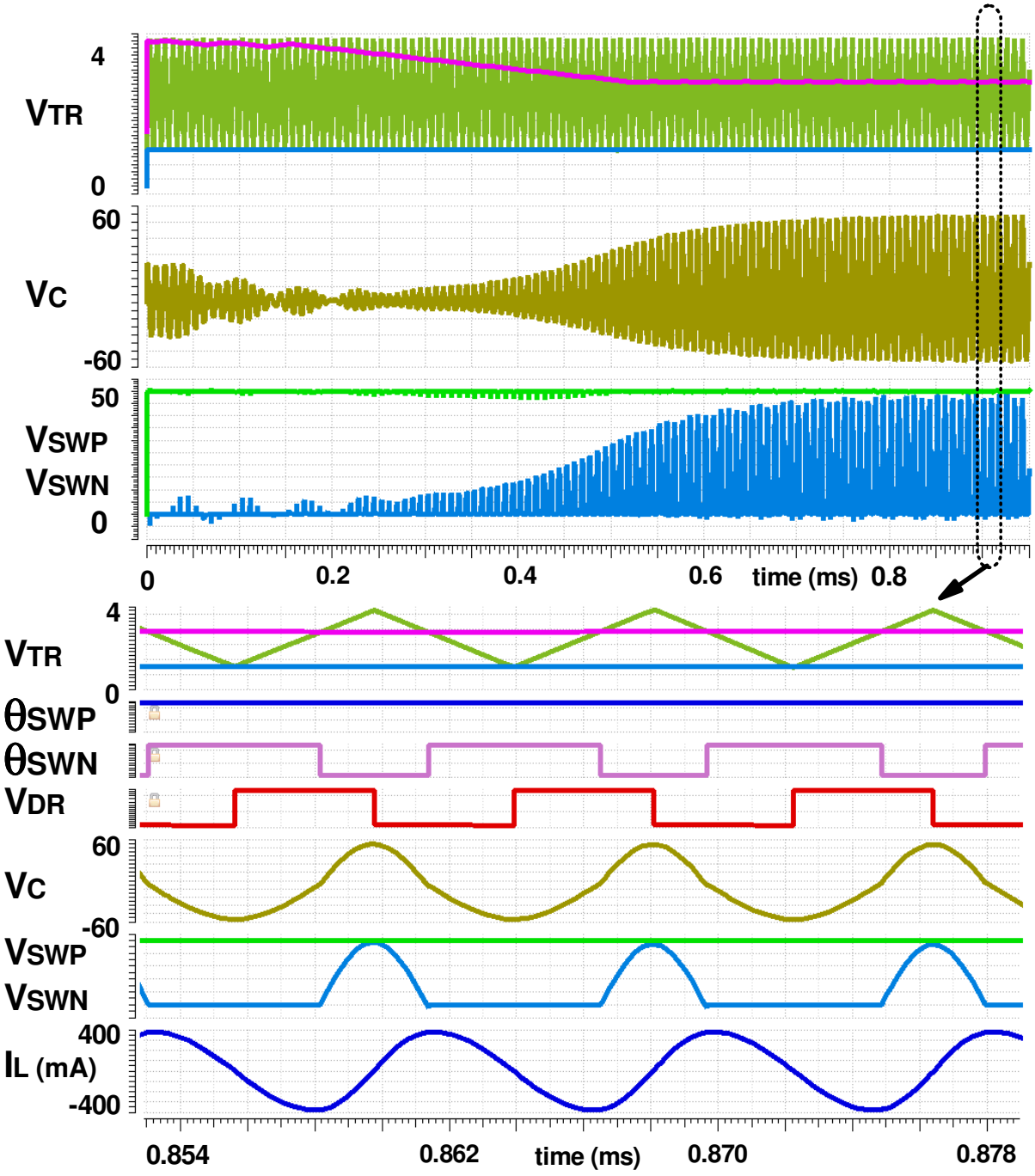

Figure 8-89: Self-tuning of LC tank at 125kHz nominal frequency with NMOS-only switching, intgain = 16

8.5.2 FSK operation

Figure 8-90 shows the system operating FSK mode with an antenna Q of 50 at 125kHz, alternating between digitally-set nominal, fast and slow frequencies (125kHz, 134.8kHz and 104.4kHz respectively), alternating at 80µs intervals. The system begins from an initialised state, i.e. all three antenna tuning loops start from an untuned condition. A low-moderate tuning gain is used at all frequencies to slow the system gradually coming into resonance.

At each operating frequency, the corresponding tuning loop is activated, slowly adjusting towards the resonant condition. The slow frequency antenna tuning loop settles first at around 1.3ms, since the resonant setting is closest to the initial condition for this frequency. The nominal loop follows closely after at around 1.4ms, since this is being selected twice as often, updating the nominal loop more frequently. The fast frequency loop settles much later, at approximately 5.9ms, since the tuning voltage required for resonance is much closer to the middle of V_{TR}.

Figures 8-91 - 8-94 show seamless transitions between slow/fast to nominal and vice versa once all three loops have settled. In each example, *FREQSEL* can be seen to correctly change at the mid-crossing of V_{TR}, creating a synchronous step in both the frequency of V_{DR} and the switch controls $\Theta_{SWP/N.}$ A large amplitude of oscillation is maintained on V_C and I_L between operating frequencies in all four cases, with a slight variation due to the varying Q factor as the operating frequency is adjusted.

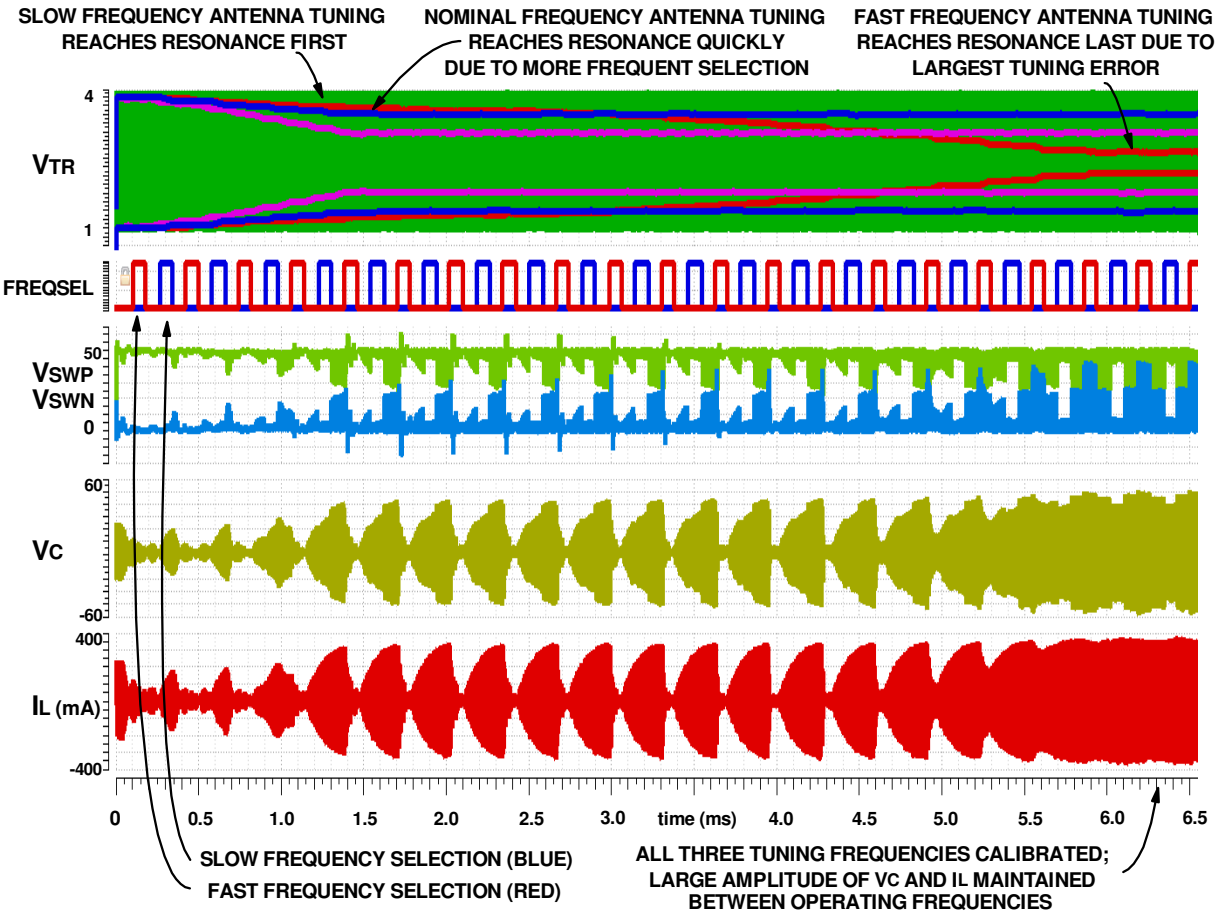

Figure 8-90: Operation of independent antenna tuning loops (F_{SLOW} = 104.4kHz, F_{NOM} = 125kHz, F_{FAST} = 134.8kHz, intgain = 4)

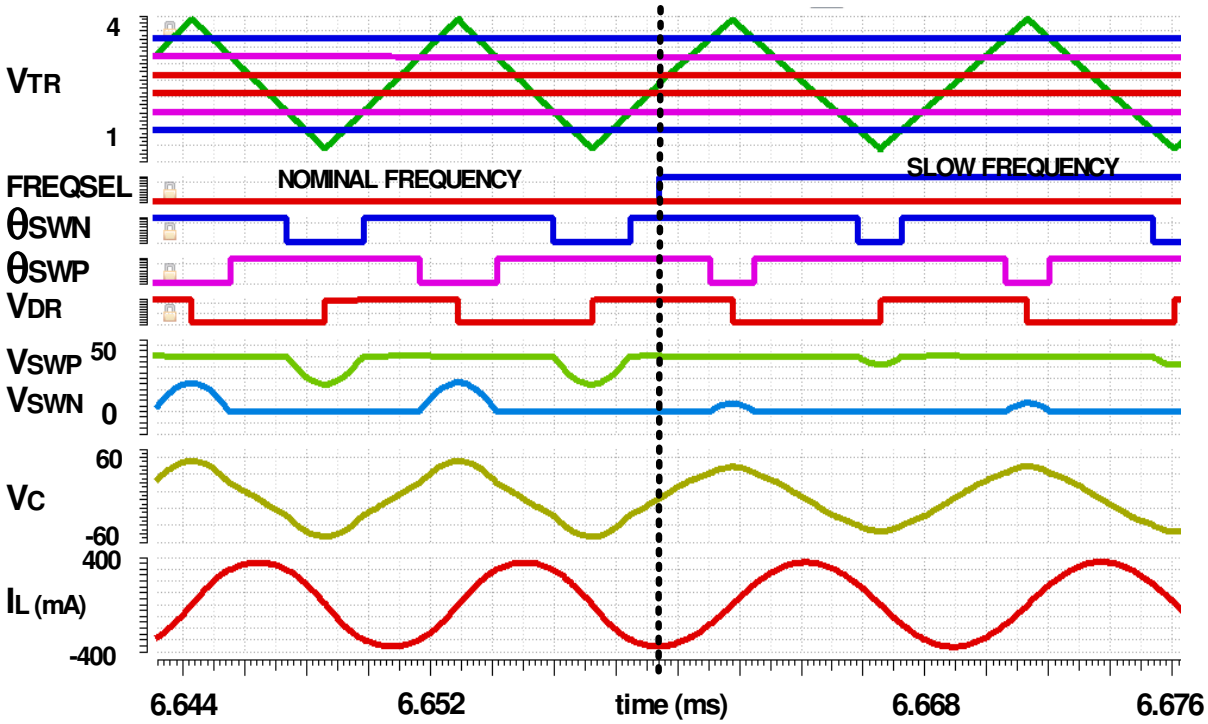

Figure 8-91: Transition from nominal to slow operating frequency (in tune, F_{SLOW} = 104.4kHz, F_{NOM} = 125kHz) (On V_{TR}, lag V_{TUNE} in blue, nominal V_{TUNE} in pink, lead V_{TUNE} in red)

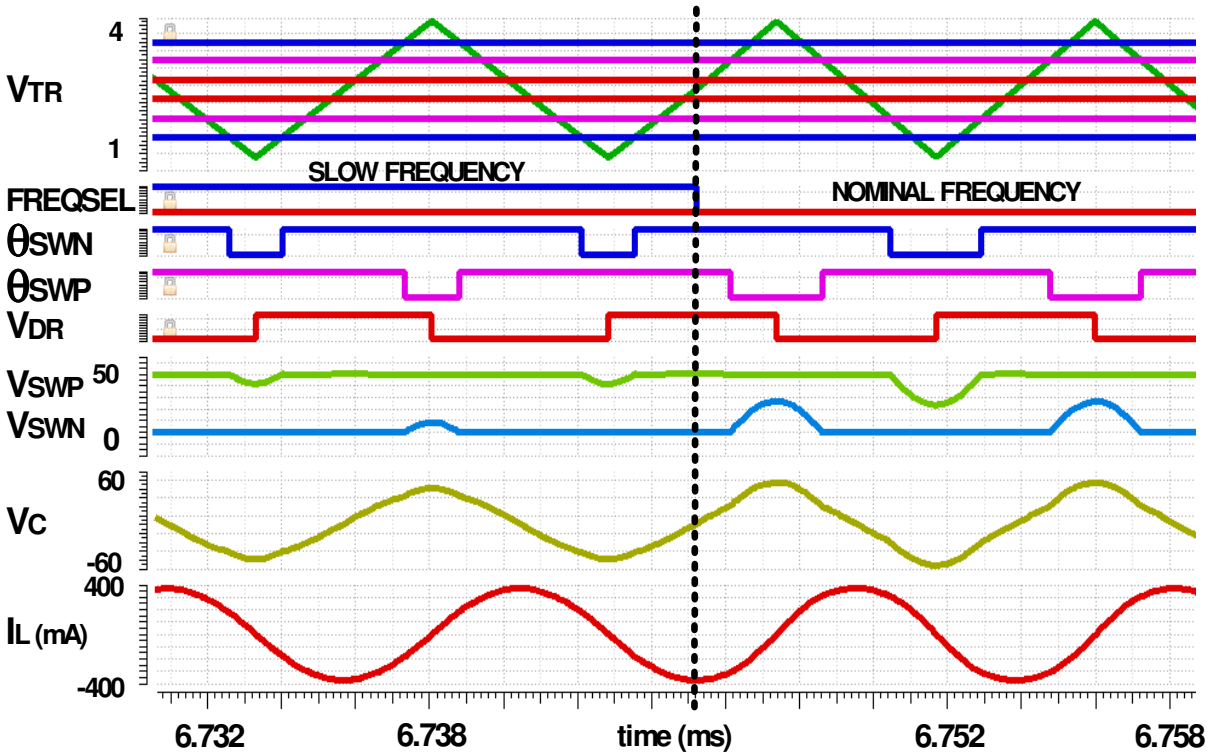

Figure 8-92: Transition from slow to nominal operating frequency (in tune, F_{SLOW} = 104.4kHz, F_{NOM} = 125kHz) (On V_{TR}, lag V_{TUNE} in blue, nominal V_{TUNE} in pink, lead V_{TUNE} in red)

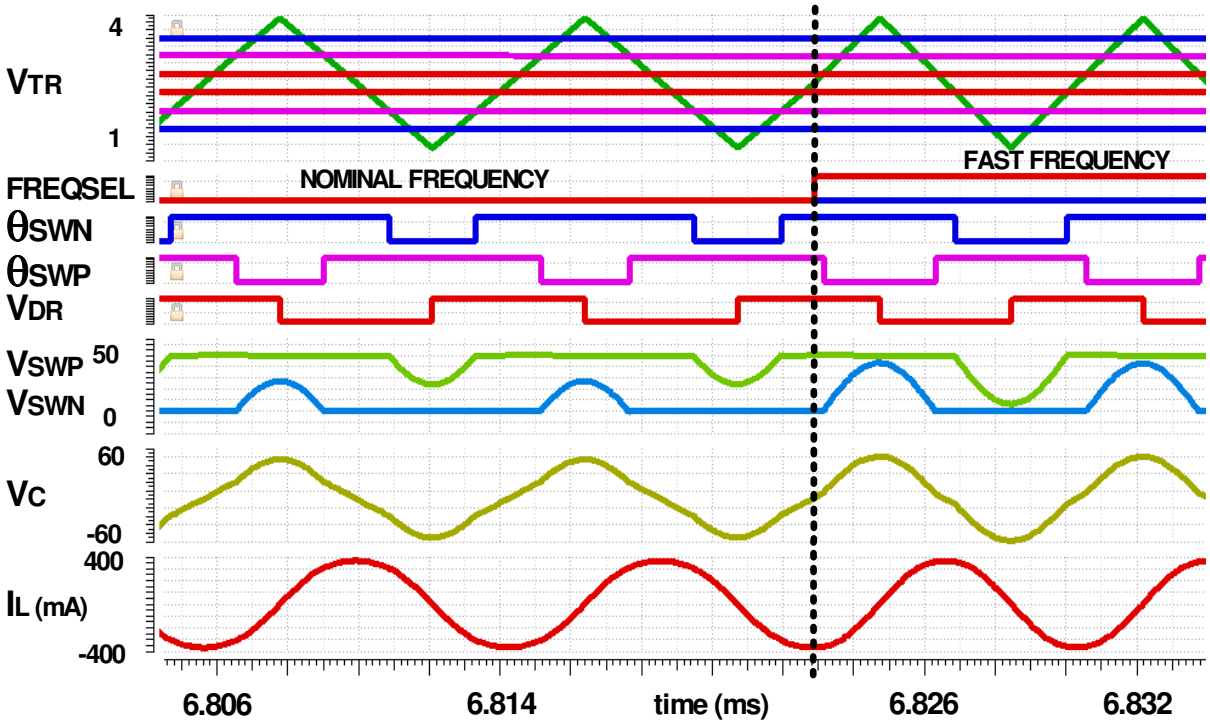

Figure 8-93: Transition from nominal to fast operating frequency (in tune, F_{NOM} = 125kHz, F_{FAST} = 134.8kHz) (On V_{TR}, lag V_{TUNE} in blue, nominal V_{TUNE} in pink, lead V_{TUNE} in red)

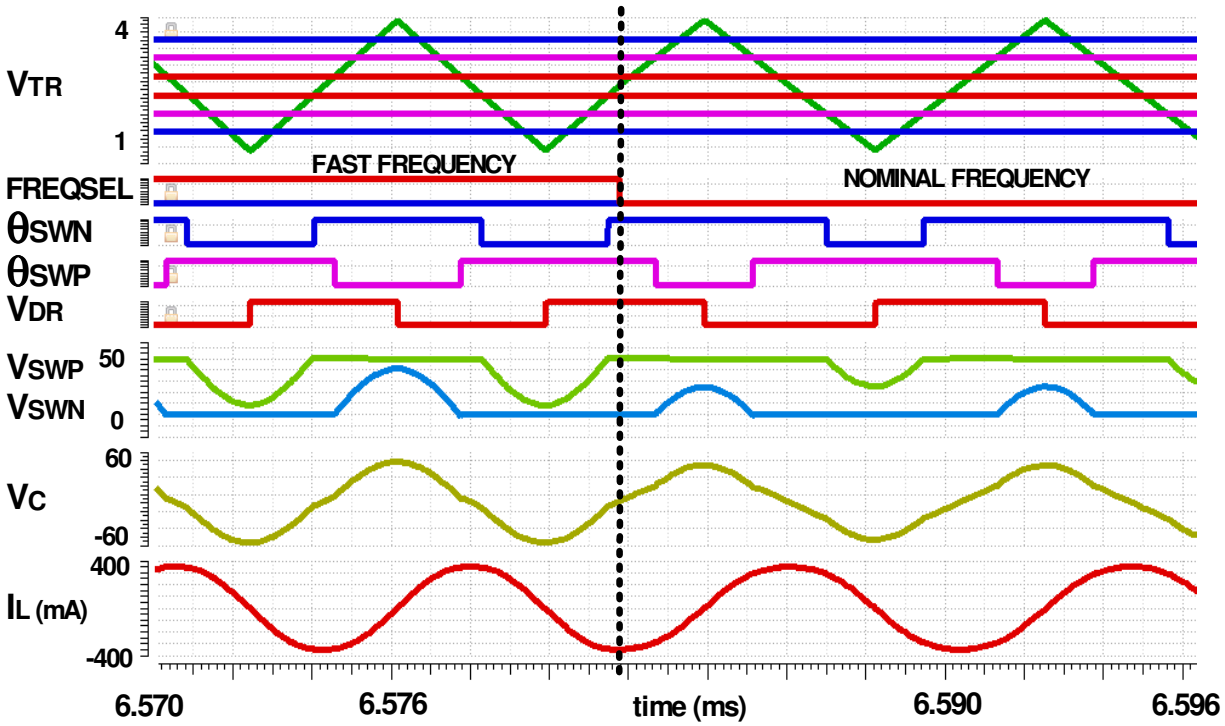

Figure 8-94: Transition from fast to nominal operating frequency (in tune, F_{NOM} = 125kHz, F_{FAST} = 134.8kHz) (On V_{TR}, lag V_{TUNE} in blue, nominal V_{TUNE} in pink, lead V_{TUNE} in red)

8.5.3 PSK operation

Full automatic operation of the system is demonstrated by simulating the system in automatic shift frequency calibration and antenna tuning mode. Given the ~500MHz operation of the phase measurement clock, this is demonstrated in the 2MHz region in order to reduce simulation time. A low antenna tuning gain of x4 is used, however a higher setting x8 is used for the tuning loops at the shift frequencies so that they will converge in a reasonable time (given that their respective loops are activated less often, compared to the nominal frequency).

A symbol period of 16µs is used, i.e. pulses are sent to the *TXDATA* control inputs every 16µs, allowing sufficient time for the phase-reference PLL to settle on the nominal phase after each symbol transition. 90^O PSK in 4 cycles is selected in so that both fast and slow shift frequencies will be achievable on the same antenna circuit, spaced on either side of the nominal resonant frequency of 1.752MHz. The antenna circuit has a Q factor of 50. The expected fast and slow shift frequencies for these conditions are 1.869MHz and 1.649MHz respectively.

Figure 8-95 shows the system calibrating for the slow frequency. On the antenna tuning, the nominal frequency reaches resonance first, increasing the amplitude of V_C. The antenna tune loop at the slow shift frequency takes longer to reach resonance, causing transient energy loss upon each symbol transition whilst it is detuned. However, it reaches resonance after approximately 7 symbol transitions (i.e. 28 periods at the slow frequency), so that a large amplitude is maintained on V_C thereafter.

V_{FREQS} is the voltage into the voltage-to-current circuit for the slow frequency to create the phase lag. At initialisation, the setting of V_{FREQS} and corresponding shift frequency result in a large phase error. As the phase error reduces with each preceding symbol transition, so does the step V_{FREQS}. The optimal value is found after approximately 28 symbols.

Note that the antenna tune loop for the slow frequency can be seen tracking the changing slow frequency itself, indicated by an increasing difference between the V_{TUNE} voltages for nominal and slow frequencies. Hence resonance is maintained on the LC antenna circuit, even though the shift frequency is not yet calibrated (i.e. the PSK angle has not yet exactly 90^O).

Figure 8-96 shows a close up of a symbol transition once the optimal shift frequency has been achieved. A brief pulse on *TXDATA_RED* is clocked into the control FSM, activating the phase lag sequence. The system synchronously switches to the slow operating frequency and corresponding antenna tuning loop for 4 cycles, switching back to nominal afterwards. A large amplitude is maintained on V_C and I_L throughout the transition. The slow frequency is measured to be 1.657MHz (in error by 0.48%).

Figures 8-97 and 8-98 show the same process for phase lead, activated by *TXDATA_ADV*. In this case the system has converged after approximately 35 symbols. In this case, the self-calibrated shift frequency is 1.857MHz (0.58% error).

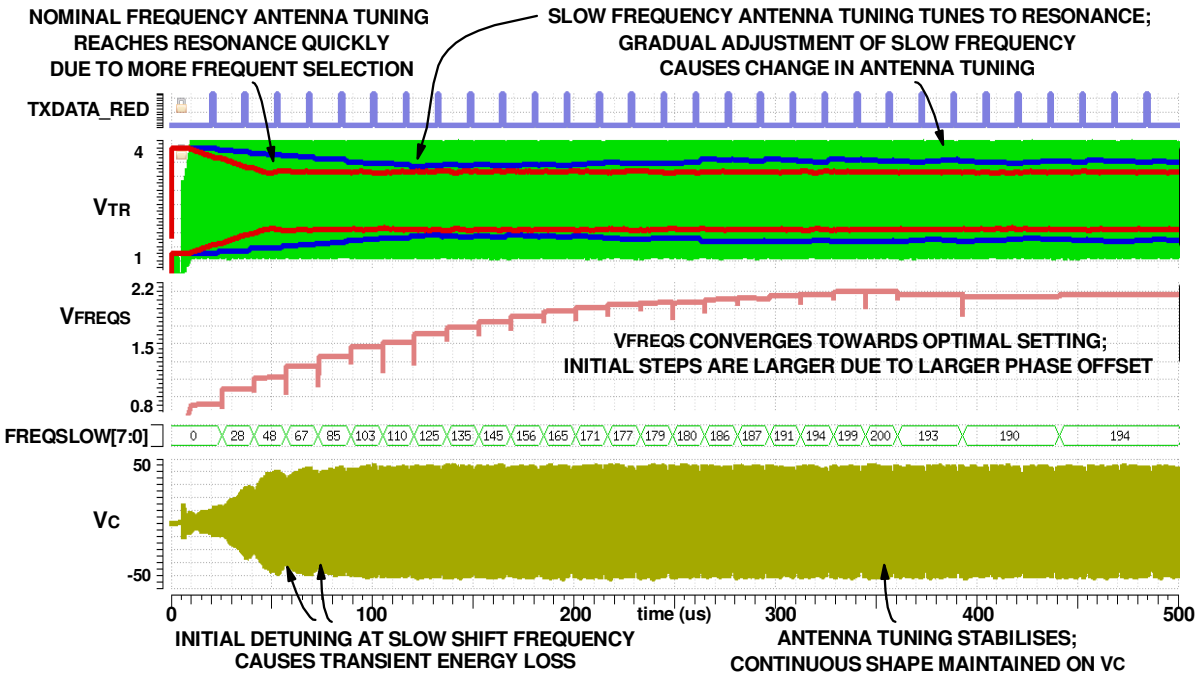

Figure 8-95: Fully automatic operation of antenna tuning and shift frequency calibration loops (90^{O} PSK in 4 cycles, phase lag, 2MHz, Q = 50)

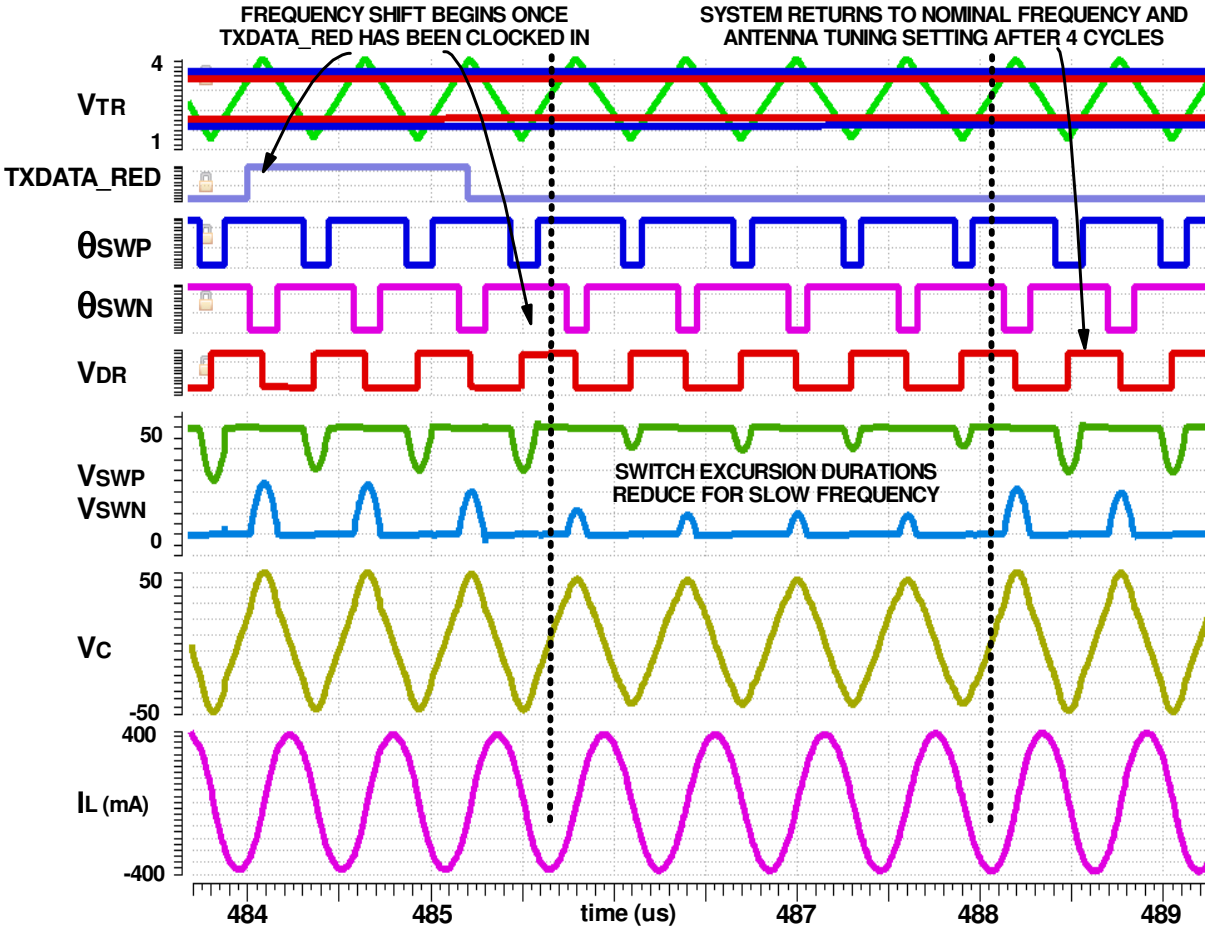

Figure 8-96: Calibrated shift frequency and antenna tuning loops (90^{O} PSK in 4 cycles, phase lag, 2MHz, Q = 50)

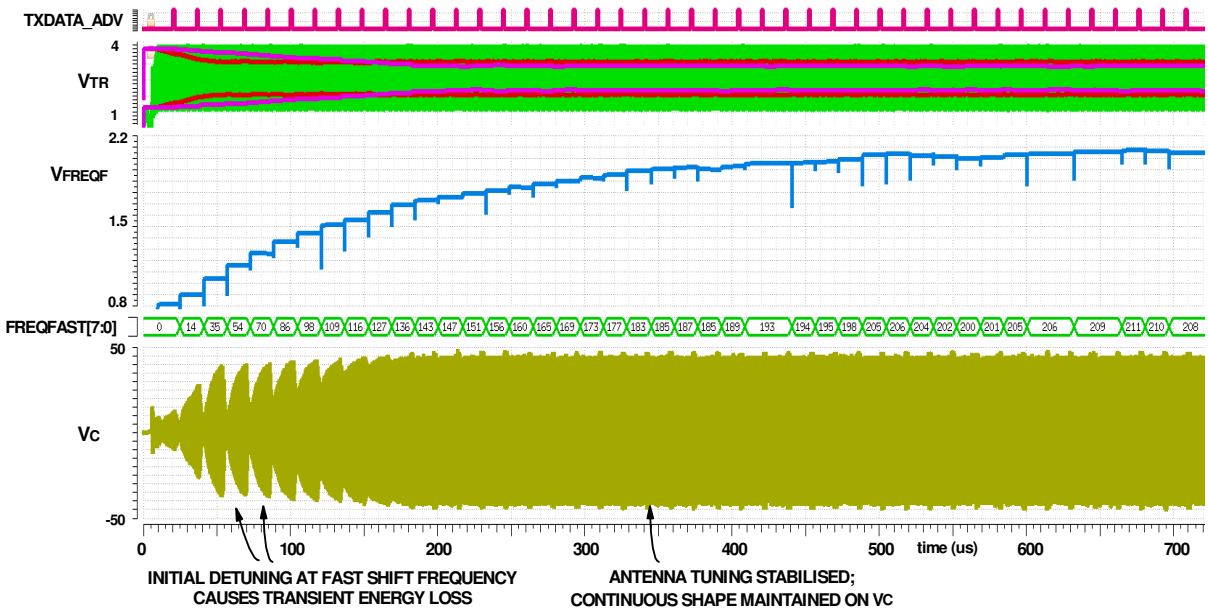

Figure 8-97: Fully automatic operation of antenna tuning and shift frequency calibration loops (90^{O} PSK in 4 cycles, phase lead, 2MHz, Q = 50)

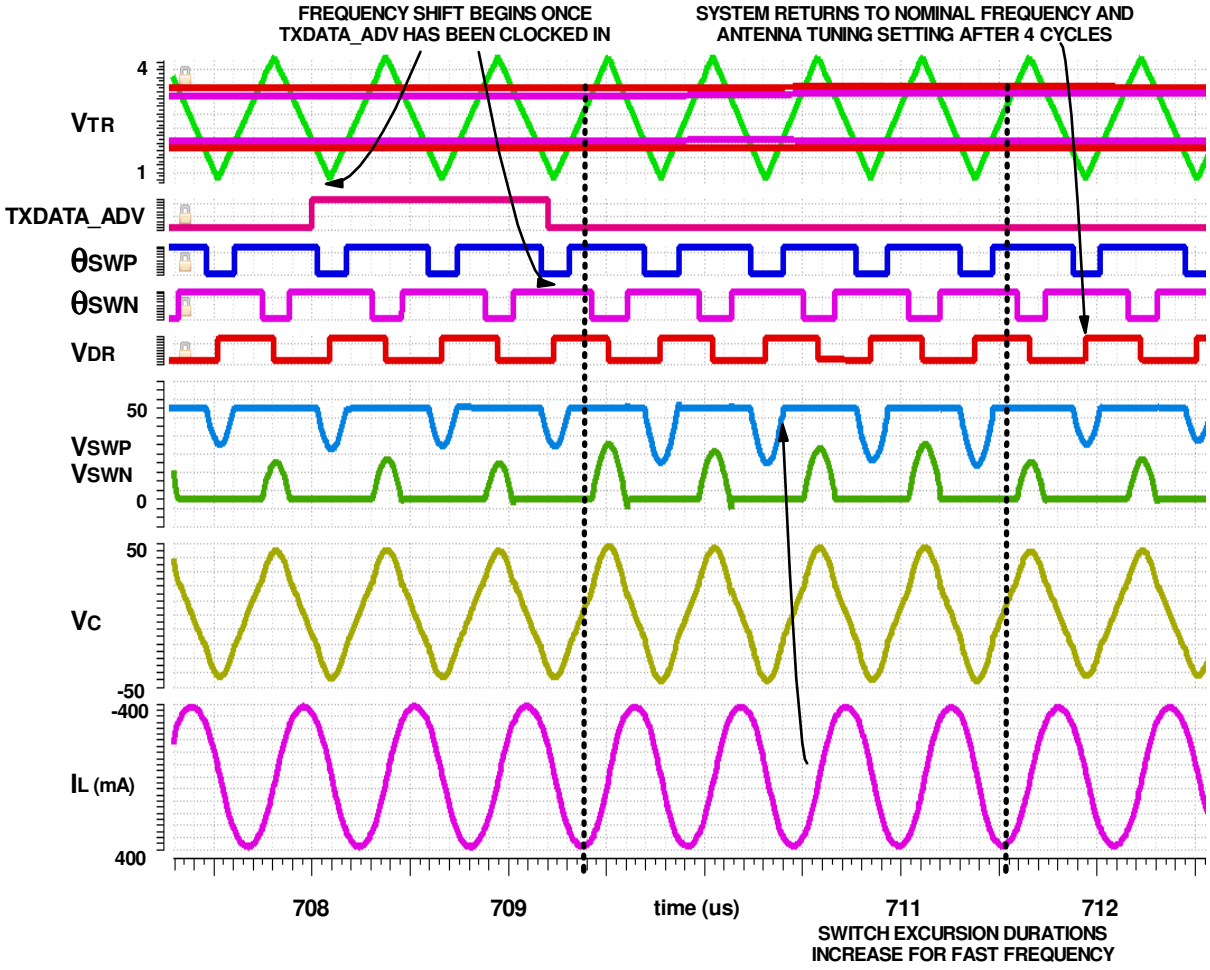

Figure 8-98: Calibrated shift frequency and antenna tuning loops (90^{O} PSK in 4 cycles, phase lag, 2MHz, Q = 50)

8.6 Summary of "lctune018_psk" design

A combined antenna driver/tuner/modulator was designed and simulated in the same 0.18µ process. Considerable design effort was focussed on the modulator. An architecture was devised to achieve accurate calibration of the shifting frequencies for phase modulation, building upon the existing architecture of the previous "lctune018" design.

The modulator stores the phase of the nominal frequency in a PLL, which is held at a fixed phase/frequency when the phase rotations occur. Quadrature phases are provided so that the resulting phase of the main oscillator is compared with respect to the ideal phase. The time offset between the actual and target phase is quantised using a high-frequency counter, determining the direction and amount by which the shifting frequency should be adjusted.

The rest of the design required changes to facilitate the FSK/PSK modulation, for example, synchronous adjustment of the antenna drive and resonant frequencies and keeping separate antenna tuning information for each operating frequency. Each system block was analysed for the required changes and designs updated accordingly.

Some changes to the design from the previous "lctune018" were necessary due to changes to the available process, with some devices being no longer available, for example the thick-oxide LDMOS devices for the HV switches. The opportunity was also taken to make other improvements to the design, for example improving the accuracy of the antenna tuning error detector to mitigate against reference drift.

To maximise the research value of the design, other additional features were included to facilitate future experimentation. For example, controls for interfacing with off-chip HV tuning switches and tuning error detection circuitry were added. The option of manually trimming the delay in the antenna tuning circuitry was included to investigate options for improving the tuning accuracy to compensate against inherent time delays.

Each design change was verified with simulation and the new system laid out. The design was fabricated and testing is detailed in the next chapter.

9 “lctune018_psk” IC experimental Results

This chapter describes the testing of the “lctune018_psk” design. The test board had to support the established functionality of antenna tuning as well as the newer FSK/PSK functions. The full board design is discussed in appendix H. The testing of the new modulation functions was distilled into the following categories:

1) FSK operation
2) PSK operation (manual frequency setting)
3) PSK operation (automatic frequency calibration)

Note that observation of the system operation was most logical in the time domain to show correct switching and adjustment of the operating frequencies and antenna tune stepping. Additionally, the accuracy of the PSK angle of rotation is easier to visualise in a constellation diagram. A demodulation circuit was constructed to facilitate this, the design described in appendix I.

9.1.1 FSK operation

Figure 9-1 shows V_C on a fixed-tuned antenna (2MHz resonant frequency) and V_C on a continuously tuned antenna, where the tuning loop for each frequency has been tuned to resonance. The antenna circuit is driven directly from the constructed IC in both cases. The fractional capacitance tuning for latter is provided using the on-board unipolar HV switches. A large frequency step was chosen for FSK, using mark and space frequencies of 2MHz and 1.8MHz respectively, using an antenna Q factor of 50 at 2MHz. The system operates with *TXDATA_RED* connected to a function generator, operating at approximately 15kHz, providing an effective bit rate of 30kbps.

With Q = 50, the antenna circuit has a 3dB bandwidth of approximately 40kHz. As is expected, the fixed-tuned antenna experiences a significant drop in amplitude at the space frequency. By comparison, the large amplitude of oscillation is maintained on V_C, hence the inductor current is also being maintained at a large amplitude for power delivery. When the *TXDATA_RED* is switched, the on board FSM ensures that the operating frequency and tuning loop selection are switched synchronously, avoiding any significant energy loss.

Figure 9-2 shows the independent operation of the tuning loops from an initialised state, in this case using 1.9MHz and 2.1MHz mark and space frequencies with an antenna Q = 50. The tuning voltages are connected to the outside world in order to show the behaviour. The lowest tuning gain setting is used, since the connections to V_{TUNE} are low bandwidth and hence a high antenna tuning gain may not produce correct ramping behaviour on these voltages.

At first, the tuning loops are disabled and neither is at resonance for its corresponding operating frequency. The data signal is now connected to *TXDATA_ADV*, operating at 50Hz. When *TUNELOCK* is disabled, the independent loops begin to adjust their corresponding V_{TUNE} voltages until resonance is achieved. Both loops are calibrated after approximately 70ms.

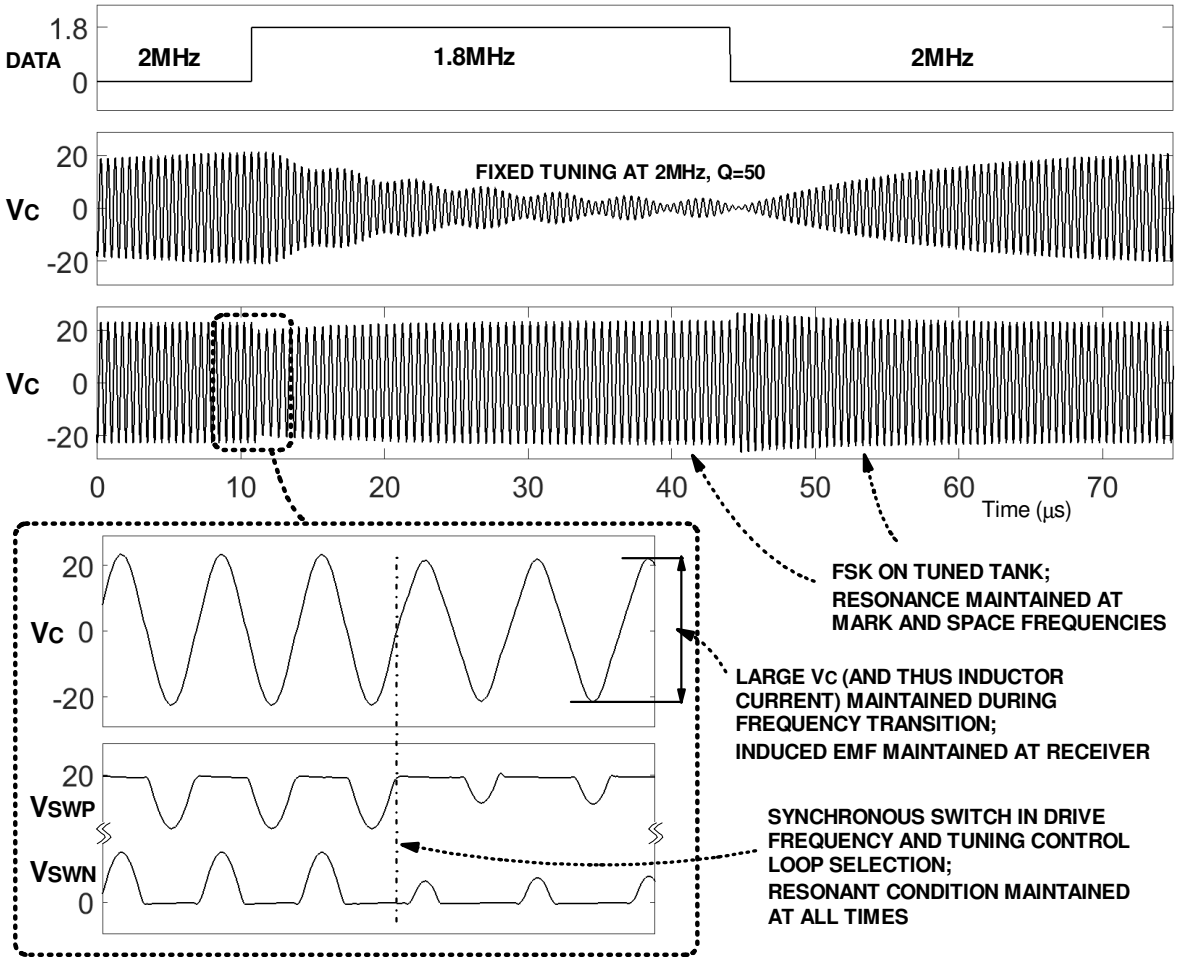

Figure 9-1: Comparison of FSK symbol transition on fixed-tuning antenna circuit and continuous tuning (1.8MHz and 2MHz operating frequencies, Q = 50)

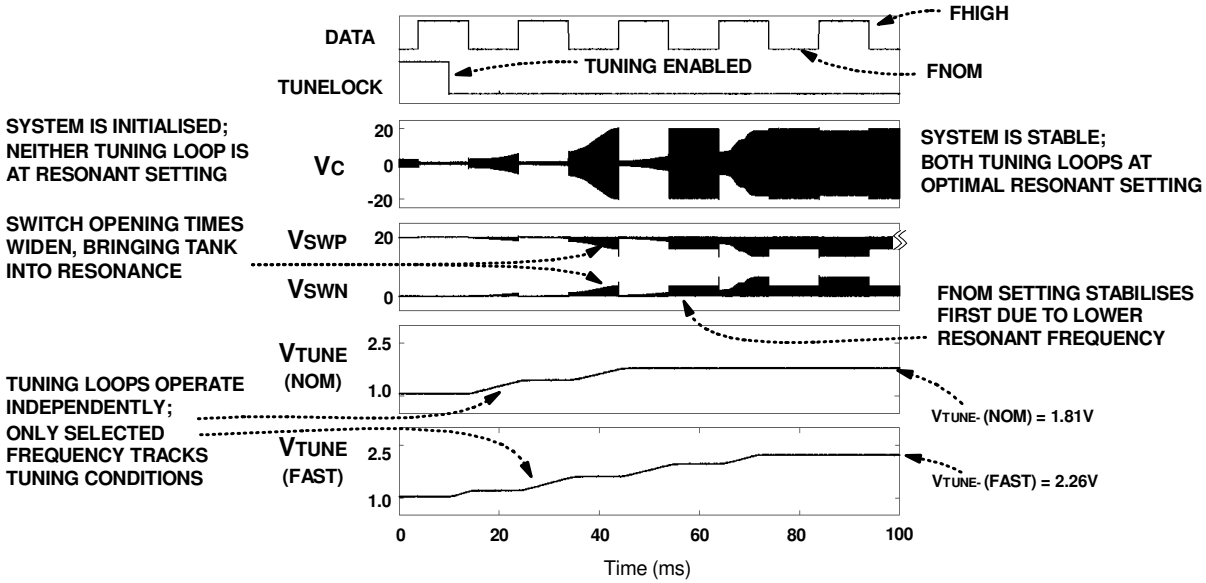

Figure 9-2: Operation of independent tuning loops for multiple operating frequencies from initialisation (minimum integrator gain, 1.9MHz and 2.1MHz operating frequencies, Q = 50)

The frequency control FSM needs at least 4 cycles to switch from the nominal frequency to the shift frequency and back. With a nominal frequency of 2MHz this limits the maximum rate of *TXDATA* in FSK mode to 500kHz (i.e. a data rate of 500kbps). Figure 9-3 shows the system operating correctly under this condition, where the nominal and shift frequency antenna tuning loops have successfully converged for operation at 2MHz and 1.8MHz respectively.

Most importantly, the data rate of 500kHz is more than an order of magnitude larger than the conventional 3dB bandwidth of 40kHz for this antenna circuit. The difference between the mark and space frequencies is also considerably greater than the 3dB bandwidth. At the same time, a large amplitude of V_C is maintained, meaning the combined modulation and tuning method circumvents the classical trade-off between power-efficient energy transfer and high-bandwidth data modulation.

Note that the amplitude of V_C changes slightly between the two frequencies, caused by the variation in Q factor. For a fixed inductance, the 10% reduction in operating frequency causes an equivalent reduction in Q, reducing the peak amplitude of V_C from 22V to around 20V.

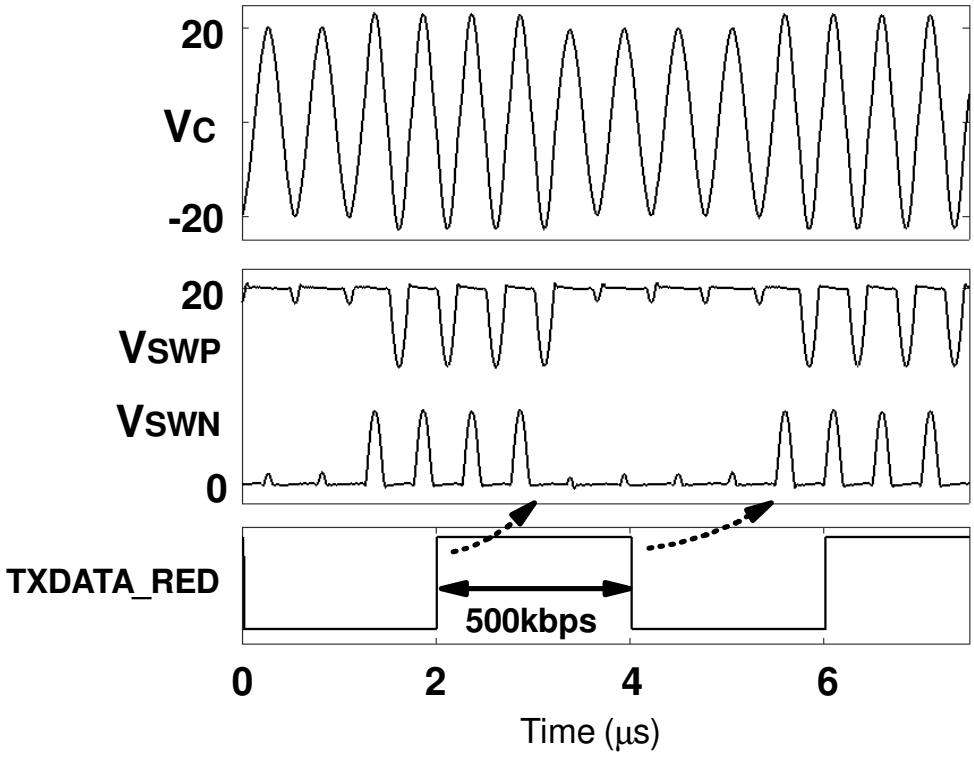

Figure 9-3: FSK at maximum data rate of 500kbps (mark and space frequencies 2MHz and 1.8MHz, Q = 50)

9.1.2 PSK operation

9.1.2.1 Manual PSK frequency setting

Figure 9-4 shows 90^{O} lead and lag transitions in 4 cycles at 2MHz nominal frequency. The shift frequencies are manually tuned to achieve the correct phase angle, determined by measurement on an oscilloscope and trimming the values to the ideal calculated values of 2.13MHz and 1.88MHz for lead and lag respectively. The shift frequency antenna tuning loops are tuned to resonance to ensure that a large amplitude is maintained in both phase lead and lag transitions, as is clearly the case.

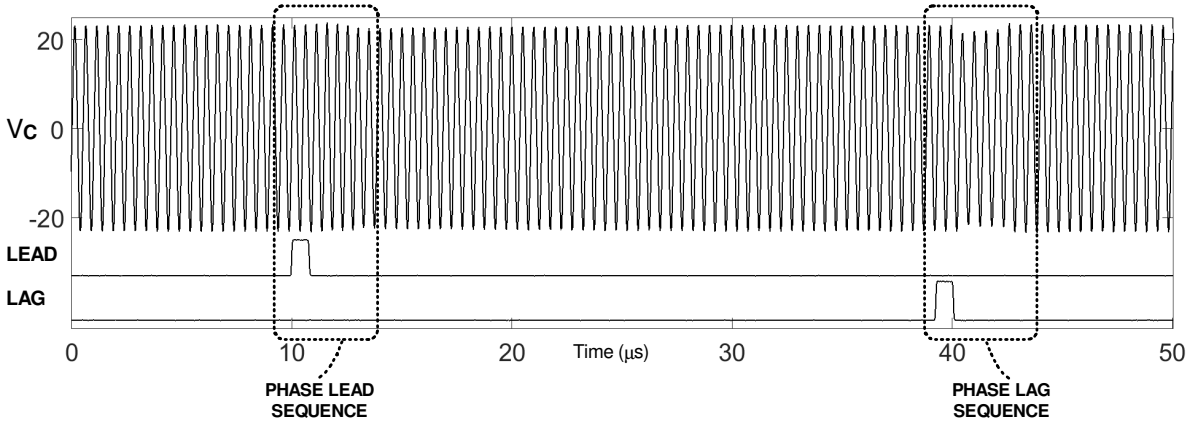

Figure 9-4: PSK 90^{O} lead and lag at 2MHz nominal frequency (4 cycle transition, Q = 50)

Figures 9-5 and 9-6 show close ups of the lead and lag transitions respectively. The PLL phase reference is not provided off chip, however can be reconstructed using periods of the nominal frequency. This permits a comparison of the phase angle of V_{DR} after the phase transitions (top panels). The second and third panels show the switch from the nominal to shift frequency and back, with antenna resonance being maintained at all times. The fourth panel is the phase angle rotation, extrapolated from the time difference between the rising and falling edges of V_{DR} and the REF signal. Both indicate that a rotation of approximately 90^{O} occurs over the four cycles for both lead and lag.

Figure 9-7 shows a comparison between a 90^{O} phase lead transition with the presented architecture and on a fixed-tuning system. The left panel shows the effect of an instantaneous 90^{O} shift applied to a fixed-tuned antenna circuit. As expected, the amplitude drops during the transition, and the phase angle rotates slowly due to the high Q factor limiting the bandwidth. By comparison, the right panel shows phase-continuous switching of both operating frequency and antenna tuning, which creates a controlled phase transition. The transition both occurs much faster (allowing for higher data bandwidth than classically permitted by the Q factor), and maintains a large amplitude of oscillation (allowing for more efficient power delivery).

Figure 9-8 shows PSK operation at the maximum data rate, for a phase lead scenario. As with FSK mode, the data rate is constrained by the need for the system FSM to clock through each state at the operating frequency. The system requires at least 7 cycles minimum to propagate through the sequence, including operating at the shifting frequency for at least 2 cycles. The maximum data rate is therefore constrained by the time taken for 5 nominal periods and 2 fast frequency periods, which comes to approximately 296kHz (using a realistic scenario of 90^{O} phase rotations). If O-QPSK mode is used, this translates to 296kbps data rate.

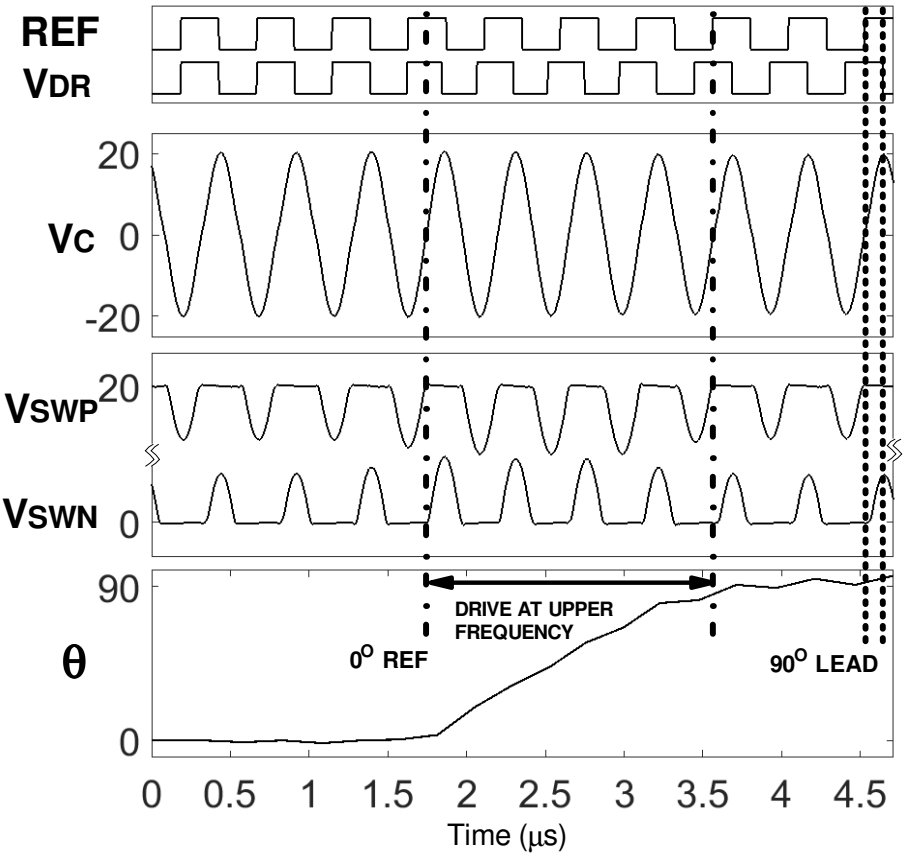

Figure 9-5: PSK 90^{O} lead transition close up (2MHz nominal frequency, 4 cycle transition, Q = 50)

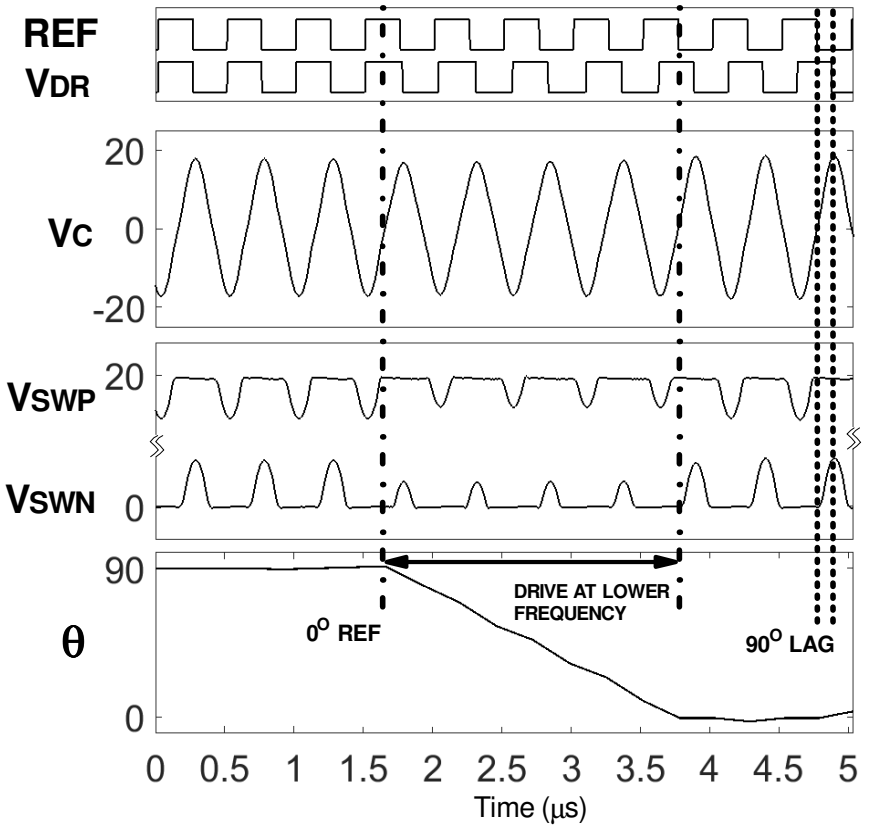

Figure 9-6: PSK 90^{O} lag transition close up (2MHz nominal frequency, 4 cycle transition, Q = 50)

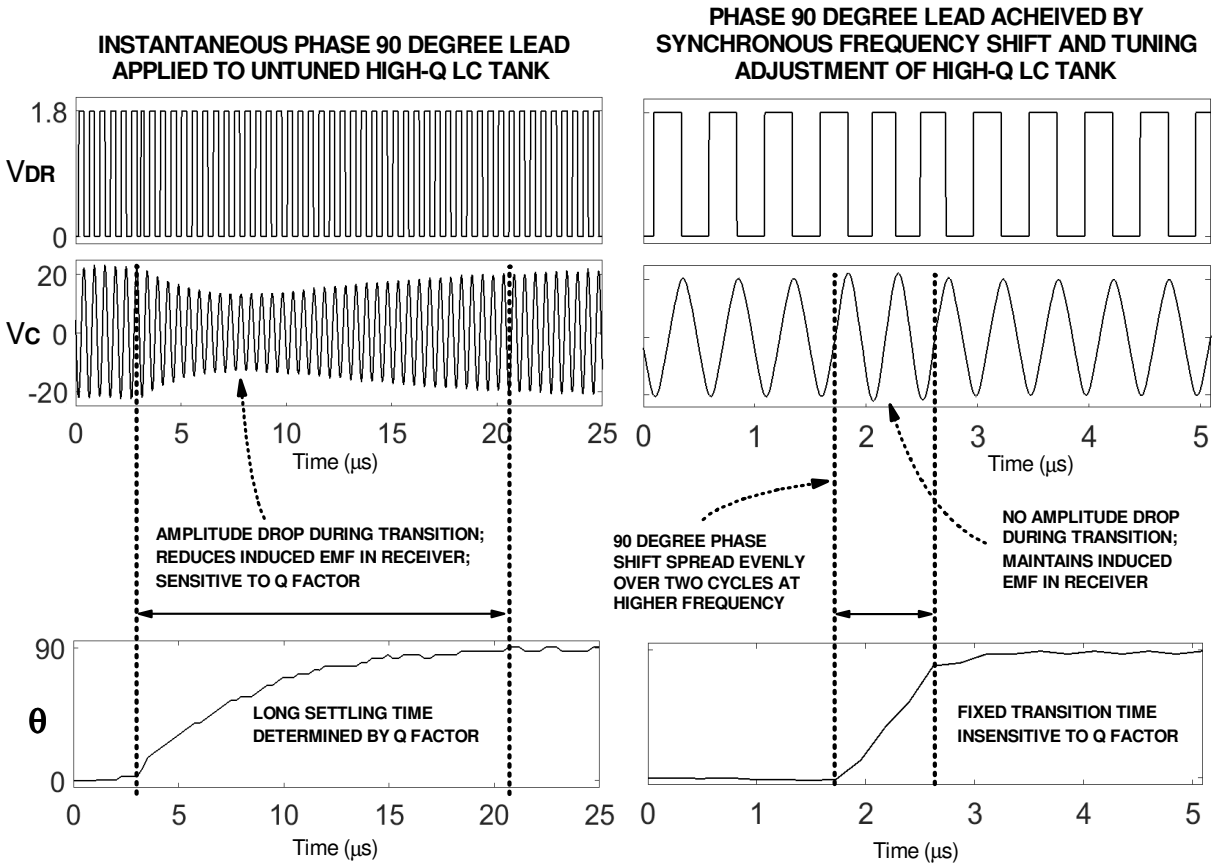

Figure 9-7: PSK 90^{O} lead transition at 2MHz. Response on fixed-tuning antenna (left) and continuous tuning antenna (2 cycle transition, right) (Q = 50)

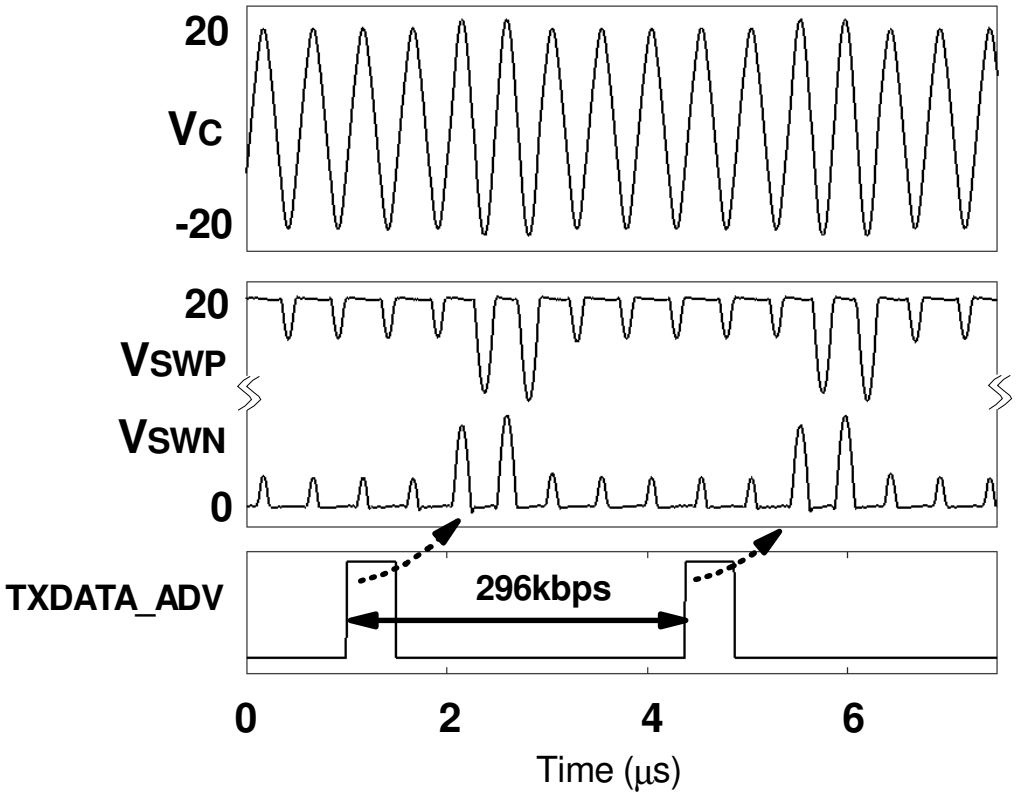

Figure 9-8: PSK 90^{O} lead transitions at 2MHz at maximum data rate of 296kbps. (Q = 50)

9.1.2.2 Automatic PSK frequency calibration: time-domain measurements

The previous PSK measurements used manually calibrated shift frequencies, however it was necessary to verify the functionality of the automatic frequency calibration. Correct functionality can be determined by visual inspection of waveforms captured at phase transitions when frequency calibration is enabled. Measurements were taken in the 1MHz region, since the default PLL filter parameters are already configured for this band. The frequency calibration loop gain K_P was left at nominal, i.e. a factor of x1 is applied to the internally-measured phase error.

Figure 9-9 shows the calibration of the shift frequency on V_{DR} by comparing it with a sample of the nominal frequency. The system is set to operate with 180^O transitions in 2 cycles, in order to assist with visual clarity. The very first transition (txcount = 1) shows that, whilst a phase transition occurs in the correct number of cycles, it does not produce the correct phase rotation, denoted by a misalignment with the opposite edge of V_{DR} at the end of the transition. A mid-calibration sample is shown next (txcount = 70), where the timing offset has decreased, i.e. the phase error has reduced. Finally, the system converges upon the correct shifting frequency after enough transitions (txcount = 140).

A similar behaviour is visible for a 180^O phase lead in 2 cycles, shown in figure 9-10.

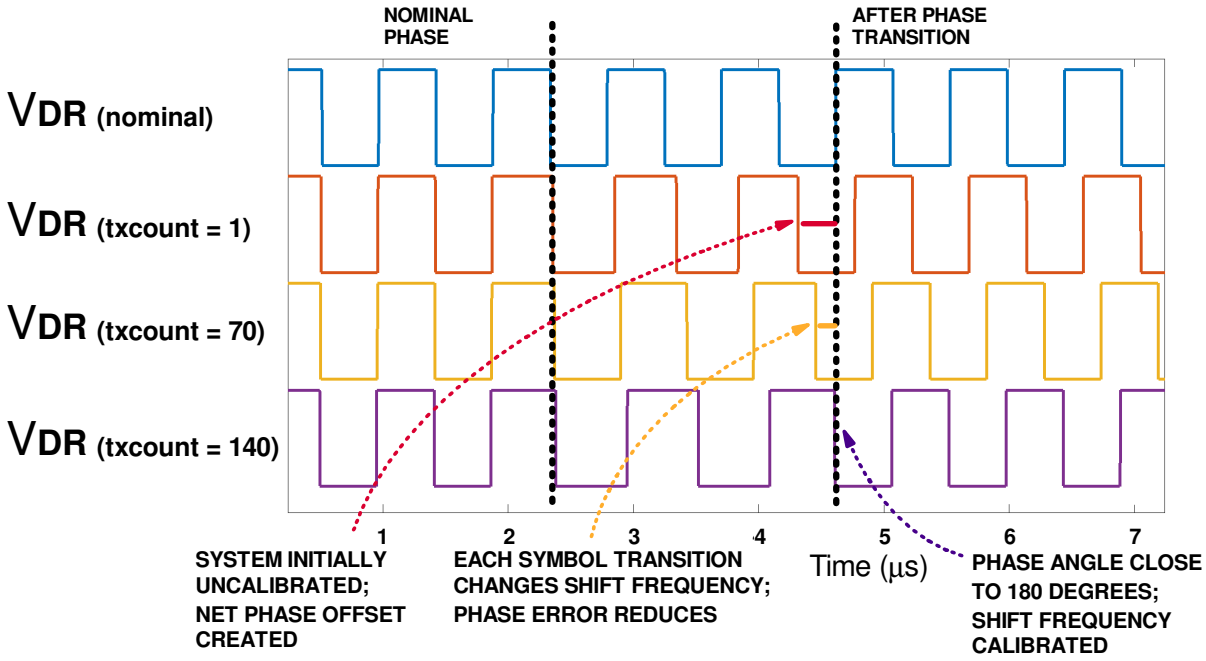

Figure 9-9: Time domain view of self-calibration in operation (180^O phase lag, 2 cycles)

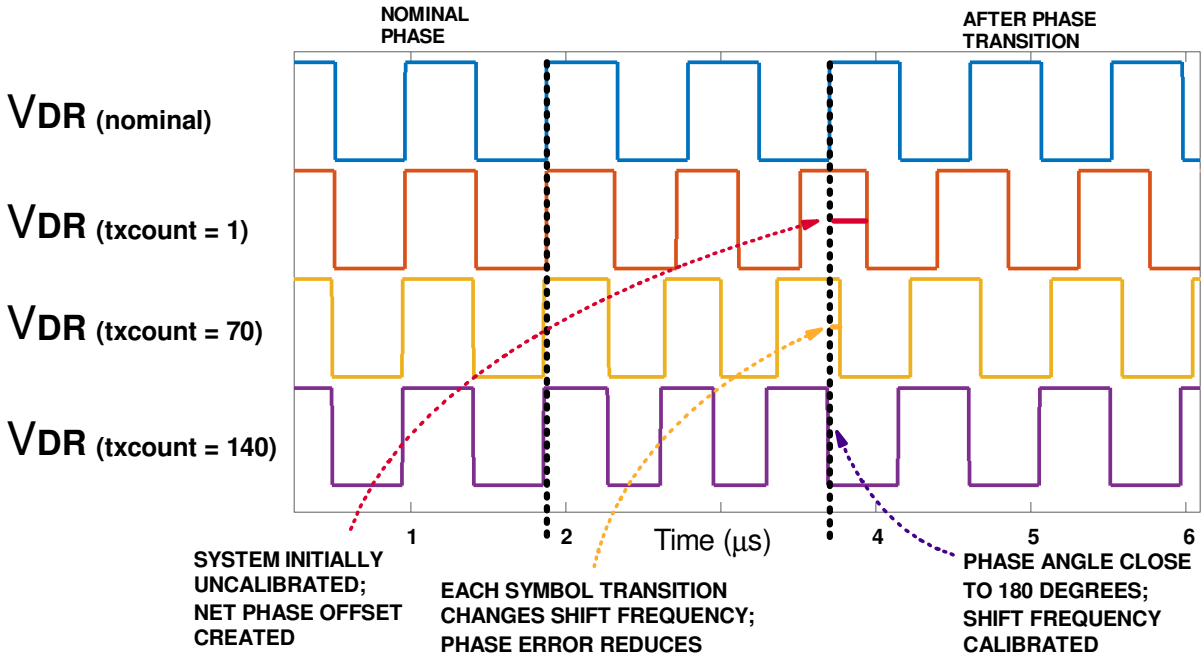

Figure 9-10: Time domain view of self-calibration in operation (180^{O} phase lead, 2 cycles)

The frequency calibration may also be viewed in terms of number of symbol transitions, allowing the settling behaviour to be visualised. Using the nominal self-calibration loop gain, bursts of 10 phase transitions from an initialised state were captured on a high frequency oscilloscope. The burst rate was sub 1Hz in order to guarantee that the phase reference PLL had settled and there was no deviation of the shift frequency setting, even after many cycles of the nominal frequency had elapsed (i.e. the system did not drift).

The nominal and shift frequencies at the end of each burst were extracted using a high frequency oscilloscope, with the ideal shift frequency calculated to compare the accuracy of the calibration. Figure 9-11 shows the case of phase lead in 90^{O} in 2 cycles. With a 1.1MHz nominal frequency, the required fast frequency is approximately 1.26MHz. It can be seen that each burst of symbols is causing the fast frequency to increase until it converges upon the ideal shift frequency. The shift frequency error at each point can be translated into a resultant phase error for that symbol transition, shown in figure 9-12. The phase error settles near zero after approximately 100 symbol transmissions.

Figures 9-13 and 9-14 show the same measurements but for phase lag, where the shift frequency is decreased from its initial setting until the phase offset is minimised. In this case, approximately 110 symbol transitions are required for full calibration of the slow shift frequency.

Additional time-domain measurements were made by varying the angle of phase shift and number of cycles of phase shift. The average settled frequency offsets and resulting phase errors are listed in table 9-1. The average frequency offset tends to reduce as the phase transition is spread over a greater number of cycles, due to the available 8-bit DAC resolution becoming focussed onto a smaller frequency range. However, the increased frequency accuracy for a smaller per-cycle phase error is counteracted by the larger number of cycles, resulting in the phase error being reasonably consistent across the available PSK modulation settings.

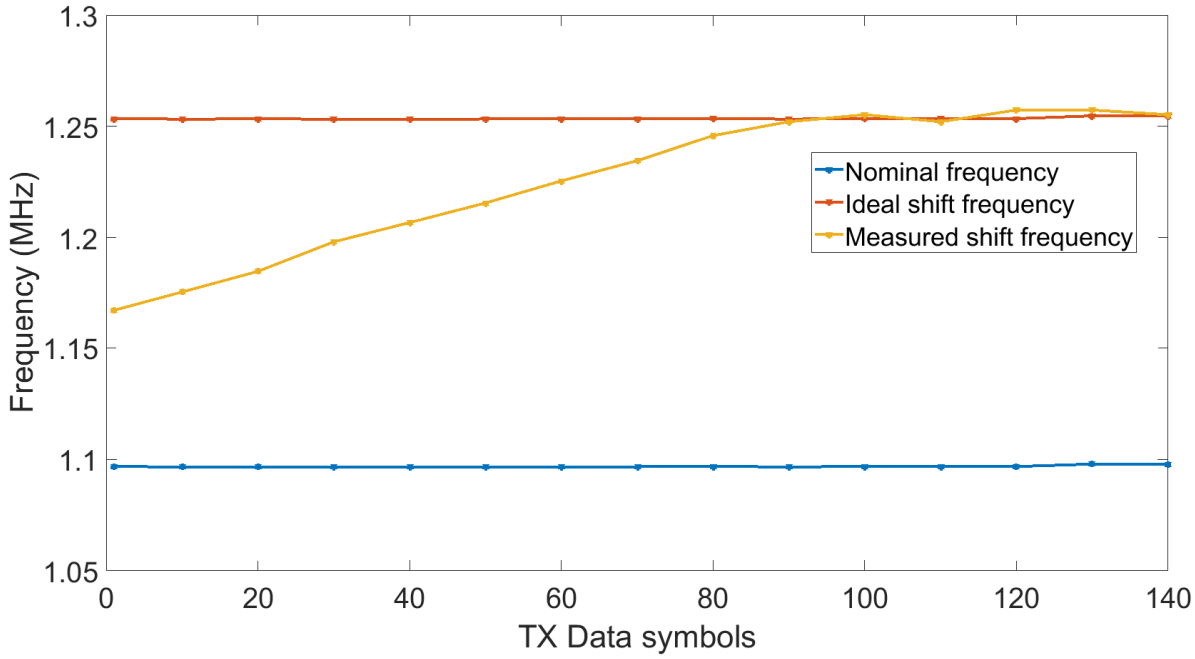

Figure 9-11: Self-calibration frequency offset with transmitted PSK symbols (90^{O} phase lead, 2 cycles, 1MHz nominal frequency)

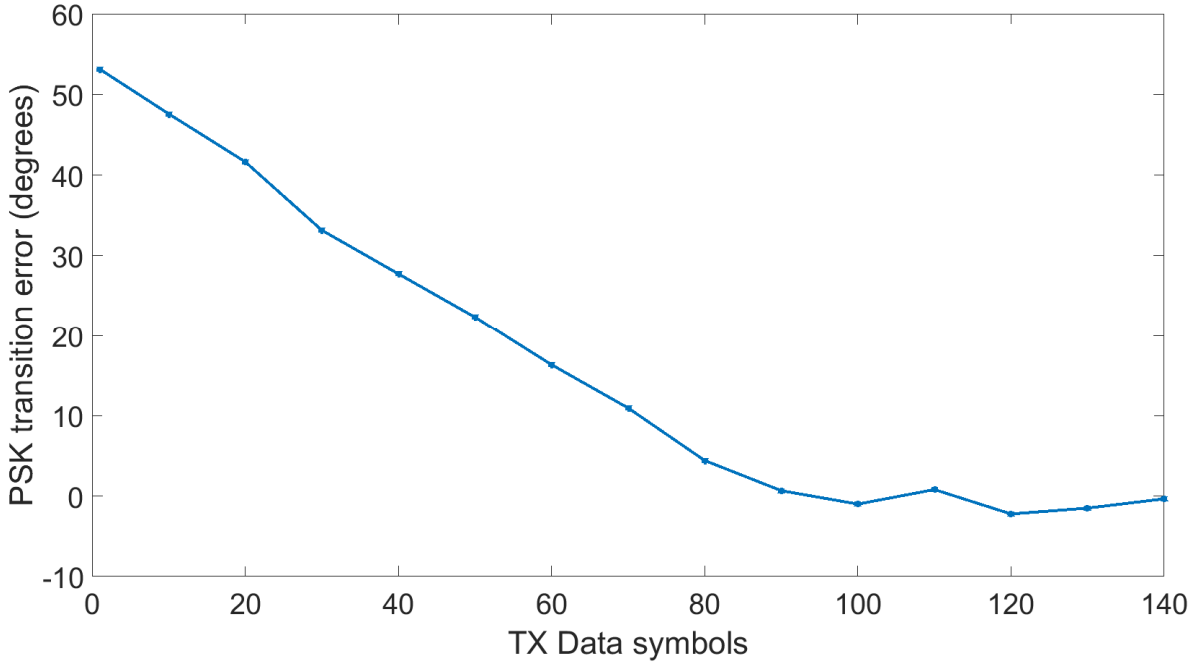

Figure 9-12: Self-calibration calculated phase error with transmitted PSK symbols (90^{O} phase lead, 2 cycles, 1MHz nominal frequency)

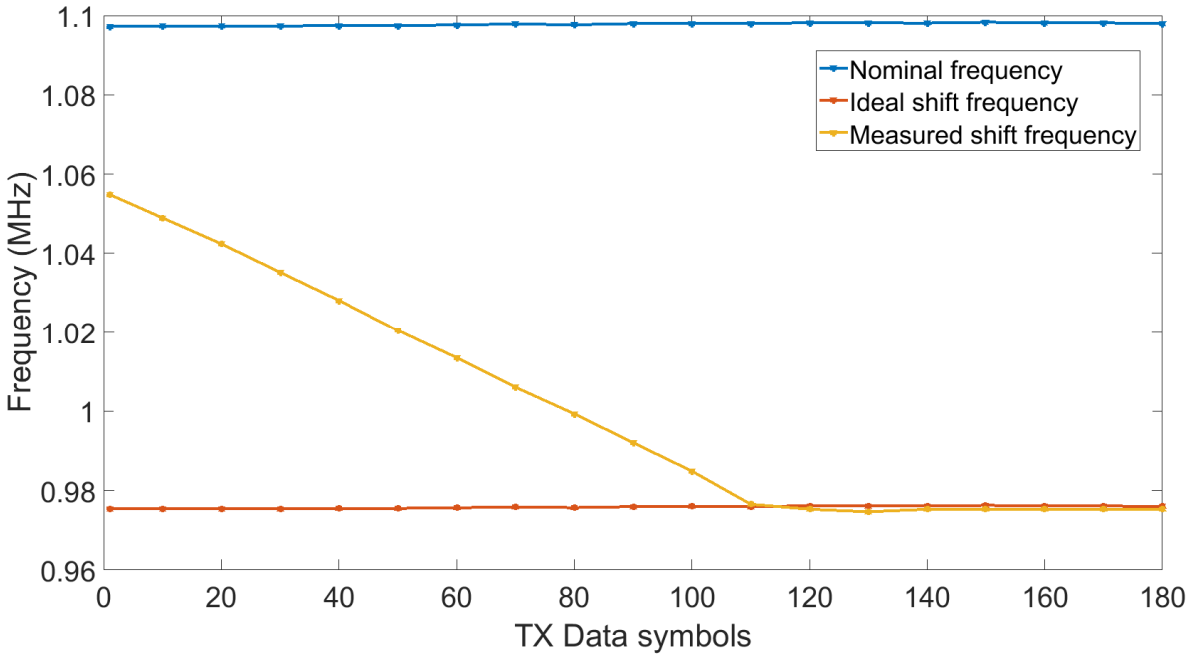

Figure 9-13: Self-calibration frequency offset with transmitted PSK symbols (90^{O} phase lag, 2 cycles, 1MHz nominal frequency)

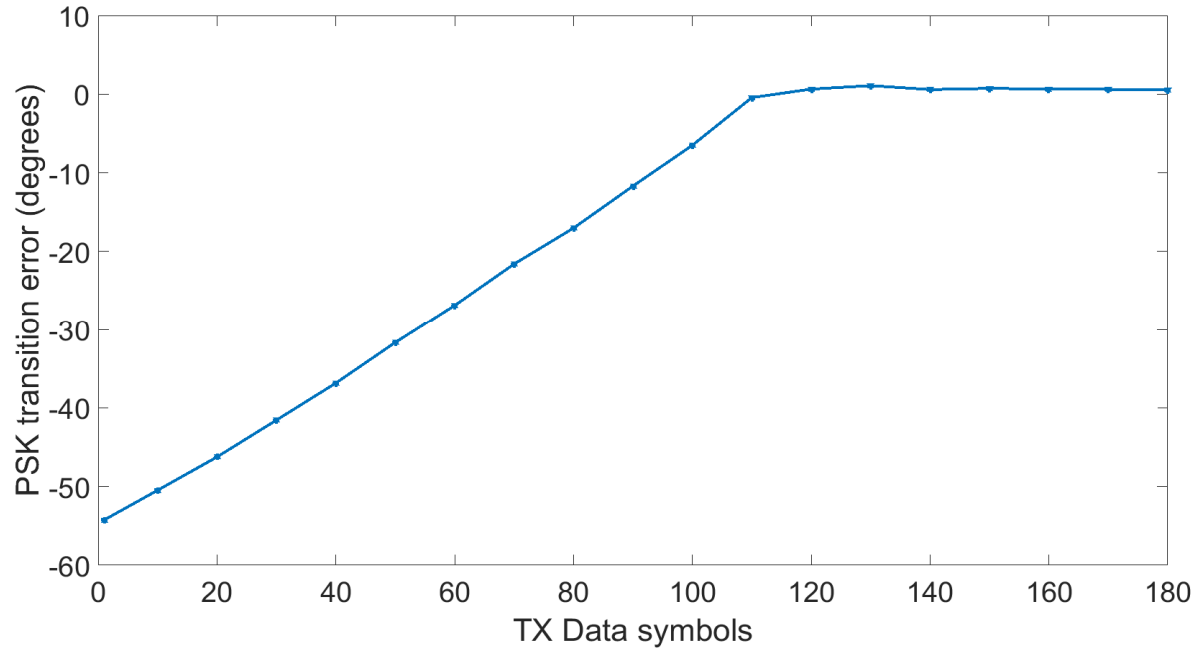

Figure 9-14: Self-calibration calculated phase error with transmitted PSK symbols (90^{O} phase lag, 2 cycles, 1MHz nominal frequency)

PSK angle	Cycles	Lead/lag?	Frequency error (kHz)	Phase error (degrees)
90	2	Lead	1.82	1.03
90	2	Lag	3.57	2.64
90	4	Lead	1.44	1.76
90	4	Lag	-1.50	-2.09
90	8	Lead	0.440	1.09
90	8	Lag	-0.772	-2.09
180	2	Lead	-1.88	-1.54
180	2	Lag	-0.993	-0.486
180	4	Lead	-1.73	-1.44
180	4	Lag	-0.796	-1.17
180	8	Lead	0.958	2.35
180	8	Lag	-0.774	-1.43

Table 9-1: Fast and slow shift frequencies and corresponding phase offsets extracted from time-domain measurements at 1MHz nominal frequency

Another way to verify that the shifting frequencies are calibrated is to observe the internally-generated copies of the fast and slow currents available on the ATB. For a given nominal current, the shifting currents for the phase lead and lag can be calculated from the required phase shift angle and number of cycles for the shift. The shifting currents for different scenarios were measured, listed in table 9-2. The current for each case was measured from the ATB using the circuitry in figure 9-15.

Note that the measured error by this method is larger than the error in equivalent scenarios taken from time domain measurements. A larger error is to be expected; whilst the frequency generator current sources are co-located on the IC, they are not well matched to each other. Additional mismatch is created by the current mirrors for the up/down currents, even though these are better matched in layout. This emphasises the need for automatic calibration to trim out the offset and achieve the correct PSK angle of rotation.

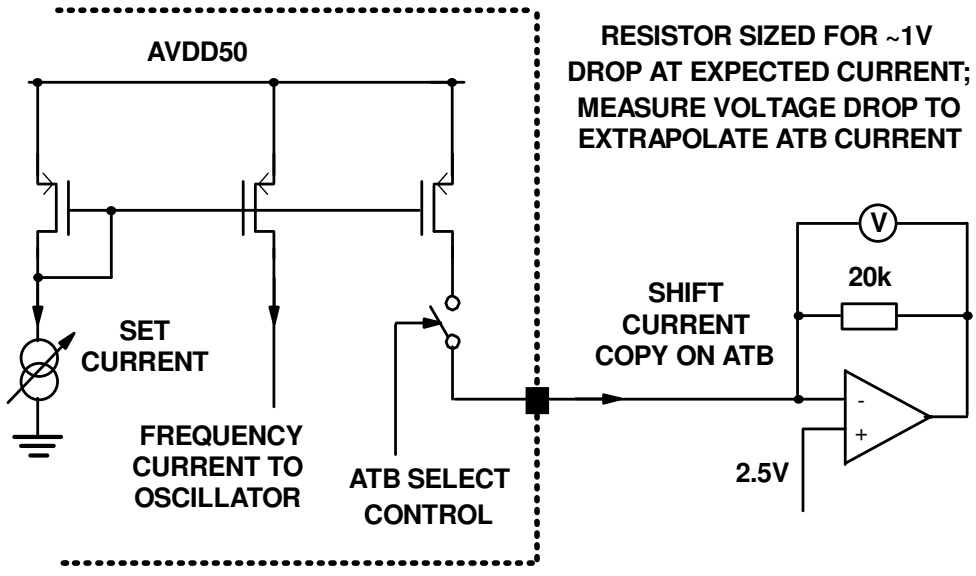

Figure 9-15: ATB frequency current measurement circuit, showing interaction with IC internal circuitry

PSK angle	Cycles	Lead/lag?	Current error (%)	Phase error (degrees)
90	2	Lead	0.295	2.12
90	2	Lag	-1.62	-11.7
90	4	Lead	0.162	2.33
90	4	Lag	-1.02	-14.7
90	8	Lead	-0.214	-6.16
90	8	Lag	-0.615	-17.7
180	2	Lead	-0.943	-6.79
180	2	Lag	-2.12	-15.3
180	4	Lead	-0.118	-1.70
180	4	Lag	-1.67	-24.1
180	8	Lead	0.156	4.49
180	8	Lag	-1.01	-29.1
180	16	Lead	-0.331	-19.1
180	16	Lag	-0.346	-19.9

Table 9-2: Fast and slow shift current errors measured on ATB with resulting accumulated phase errors

9.1.2.3 Automatic PSK frequency calibration: phase-domain measurements

In order to demonstrate that the modulator can both calibrate the shift frequencies at a high data rate and maintain calibration once settled, a demodulator was constructed as per the concept in figure 9-16 to produce reference IQ signals to create a constellation diagram. Circuit details of the demodulator are provided in appendix I. Note that at antenna resonance, the phase behaviour of the antenna drive and capacitor voltages is identical, so the phase is extracted from V_{DR} for a simpler interface with the demodulator.

A pseudo-random sequence of *TXDATA_ADV/RED* pulses at 50kHz was used at 1MHz to create the constellation diagram in figure 9-17. With a hypothetical antenna circuit with a Q of 50, this is approximately 2.5x the 3dB bandwidth of the antenna. The ideal constellation points are indicated in red, with black points for the sampled phase angle at the end of each phase rotation.

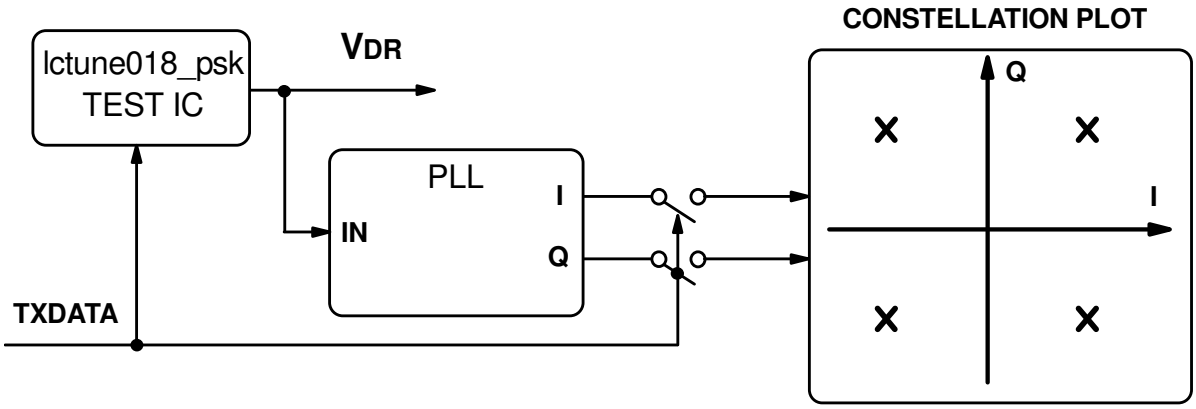

Figure 9-16: ATB frequency current measurement circuit, showing interaction with IC internal circuitry

The Error Vector Magnitude of the constellation was calculated to be 14.52%. The average phase error between the ideal and sampled symbol positions was 1.36^{O}, the worst case measured as 6.76^{O}. This is higher than the error extracted by time-domain measurements, which are more accurate due to the high frequency resolution used to extract them. On the other hand, the demodulator circuit introduces additional error in the form of phase noise on the reference PLL VCO and creating the slight rotation at each constellation point.

In practice, this much variation of the phase angle is not as problematic when compared with a typical RF signal chain. If there is a sufficiently large EMF at the receive coil to activate its circuits, then the amplitude of the modulated signal is likely to be much greater than background Gaussian noise. Hence, the channel is not noise-limited in the same way as a classical RF system, thus a larger error in the PSK angle may be tolerated than would otherwise be normally acceptable.

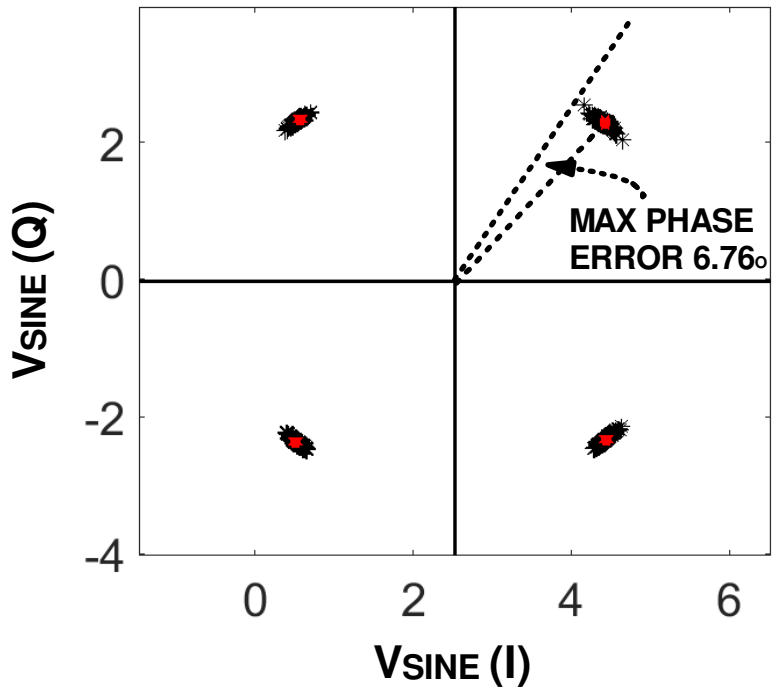

Figure 9-17: Constellation diagram for self-calibrated PSK (90^{O} lead/lag 512 symbol pseudo-random sequence, 2 cycles, 1MHz nominal frequency, 50kHz symbol rate)

9.1.2.4 Concurrent PSK frequency and antenna tuning calibration

To verify that the PSK shift frequency calibration and automatic antenna tuning operate concurrently, careful observation of both the phase of V_C and the HV switch excursions is necessary. Figure 9-18 shows a 90^{O} lag scenario at 1MHz, with different symbol transitions selected (the 1st, 16th, 30th and 120th). The nominal phase waveform of V_C is included to assist with visual inspection of the phase alignment.

Initially, the antenna tuning is not calibrated, causing a significant drop in V_C amplitude during the phase shift, however the antenna tuning has achieved resonance by the 30th symbol. The shift frequency is not yet calibrated (indicated by the non-90^{O} alignment of V_C after the phase shift and the reference waveform, the shift frequency must be further reduced), hence more symbol transmissions are required. By the 120th symbol, the system has achieved a near-ideal 90^{O} phase lag. At the same time, the amplitude of $V_{SWP/N}$ excursions has reduced, indicating that the antenna tuning has correctly tracked the reducing shift frequency to maintain resonance at all times. Therefore, both frequency calibration and antenna tuning are operating concurrently.

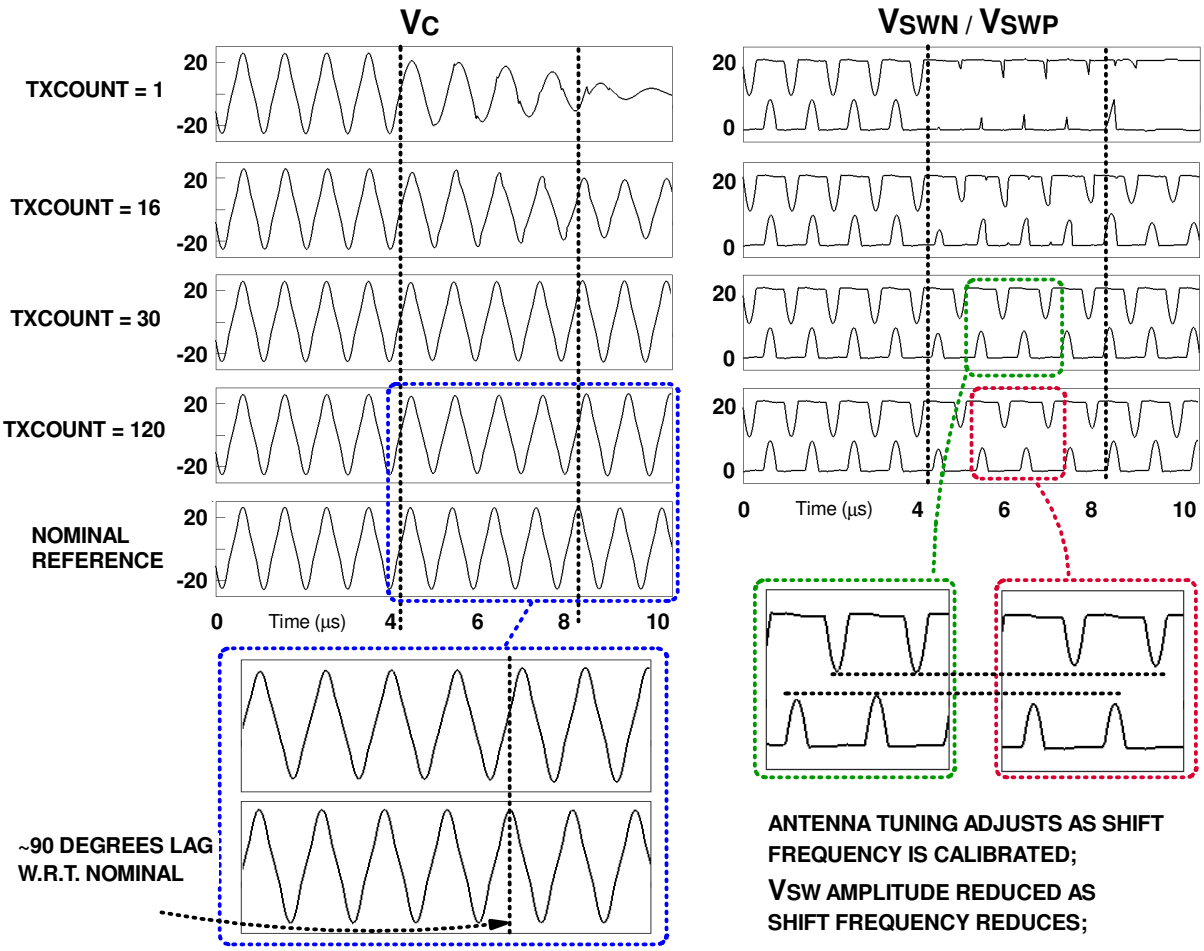

Figure 9-18: Concurrent PSK shift frequency and antenna tuning calibration (Q = 50, 1MHz, 90^{O} 4-cycle phase lag)

9.2 Summary of "lctune018_psk" testing

The new features introduced with the "lctune018_psk" design were tested and achieved their intended goals. The frequency modulation functionality synchronously adjusts the antenna drive frequency and tuning setting, so that each frequency can be tuned independently. When all operating frequencies are tuned to resonance, the frequency modulation causes negligible change to the amplitude of oscillation. Hence, power delivery to the intended receiver can be maintained during data transfer.

The phase modulation functionality correctly adjusts the operating frequency for a set number of cycles, spreading the phase rotation out in a controlled fashion to avoid an instantaneous phase shift in the antenna drive. In both FSK and PSK mode, the constructed system can achieve data rates which exceed the 3dB bandwidth limitation of the high-Q antenna, allowing both high data rate and high power transfer efficiency.

The shift frequency calibration loop was measured in the 1MHz region for both phase lead and lag scenarios and works correctly in both cases. Observation is in both the time domain (allowing visual demonstration of the calibration method) and phase domain (resulting in a constellation diagram of the transmitted data). Concurrent operation of the shifting frequency calibration and automatic antenna tuning is shown, demonstrating that the loops operate independently.

10 Conclusions and Future Work

This thesis has demonstrated the benefit of the quadrature-symmetric phase-switch fractional capacitance tuning method for large-signal LC antenna circuits for inductive coupling applications. Such applications demand high Q-factor LC circuits for high efficiency, creating the need for high accuracy tuning. However, detuning caused by component tolerances, parametric drift and magnetic effects necessitates many tuning components in order to maintain resonance. Furthermore, the use of a high-Q factor puts a constraint on the data bandwidth between the transmitter and receiver.

Classical tuning methods like statically-switched arrays of tuning capacitors incur a significant cost in the form of multiple tuning capacitors and HV switches required for tuning. On the other hand, the fractional capacitance method significantly reduces the number of components and switches by creating a time-averaged resonant frequency using a single continuously-switched capacitor in the LC antenna circuit.

The tuning resolution of the classical tuning method is determined by the number of capacitors available. On the other hand, the tuning range of the switched fractional capacitance method essentially continuous, limited by the precision of timing generation. This permits a very high tuning resolution and hence accurate tuning for the required high Q factor. Furthermore, observation of the sign of the tuning capacitor switch voltage immediately before closure permits unobtrusive detection of the resonant condition, providing frequent opportunities to adjust the tuning setting to compensate for detuning effects in real time.

The system concepts for switched fractional capacitance tuning have been translated into a monolithic IC, as the benefits are best realised when the system is integrated, requiring fewer pins on an IC package and less HV die area on silicon when compared to classical tuning methods. The relative advantages and disadvantages of digital and analogue architectures on chip were considered, resulting in a mixed-signal approach to combine high current and voltage antenna drivers and switches with fast timing generation circuits, permitting realistic inductor currents at operating frequencies typically used in commercial and industrial applications (100mA RMS current, up to the 2MHz region).

The ideal fixed and fractional tuning capacitances are realised as independently switched tuning capacitances on N and P LDMOS devices, avoiding the difficult challenge of providing a HV low resistance bi-directional switch function within the IC. Whilst this arrangement of the architecture constrains the max:min tuning range to approximately 1.4:1, it is enough to compensate for most practical detuning effects.

The system includes circuitry to sense the switch voltage error sign, reducing the HV excursion to the safe operating region of a fast, LV comparator. The gain of the self-tuning loop can be modified to follow moderate bandwidth FM in the antenna drive frequency, providing a trade-off between self-tuning time and ripple in the steady state value. The system also includes a method of phase trimming to correct the HV switch timings to achieve accurate tuning of the LC antenna up to 2MHz at high Q. The measured IC had a tuning accuracy of less than 2.5^{O} at up to 1.3MHz, and with similar performance levels at up to 2MHz when phase trimming is applied. This is a higher tuning accuracy compared to realistic implementations of classical tuning methods, whilst simultaneously requiring less die area and few IC package pins for tuning.

The classical limitation of data bandwidth may be overcome by synchronously adjusting the antenna drive and resonant frequencies, such that resonance is maintained at all times. Provided that the drive and antenna resonant frequencies always match, there is theoretically no limitation on how quickly or how often they may be changed, hence the data bandwidth for frequency modulation may easily exceed the classical 3dB bandwidth of the high-Q antenna circuit. The switched fractional capacitance method inherently provides the facility for such a synchronous change, without disrupting the circulating

current. Hence FSK is possible whilst maintaining a large magnetic field to power the receiver during data transmission, alleviating the requirements for bulk capacitance on the receiver power supplies.

To provide a synchronous change in drive and resonant frequencies, multiple antenna tuning loops were added to the previous system architecture, one loop for each operating frequency. Each antenna tuning loop is activated when the corresponding operating frequency is selected, holding the previous tuning values ready for the abrupt change and updating with the instantaneous error signals, hence with a sufficient number of cycles all loops may be tuned to resonance and a large magnetic field maintained at all times. The change in operating and resonant frequency must comply with the zero-voltage switching criterion of the tuning method, so the timing of the frequency transitions is made synchronous with the mid-crossings of timing reference waveform. Hence it is synchronous with the zero-crossings of the antenna voltage V_C at resonance. The system was measured to operate at up to 500kHz FSK bandwidth in the 2MHz region with an antenna Q of 50 (i.e. an antenna 3dB bandwidth of 40kHz).

The method used to enable FSK was adapted to permit PSK, by temporarily increasing or decreasing the drive frequency and at the same time as the antenna inductor resonant frequency to create a net rotation in the phase of the oscillating magnetic field. By spreading the phase rotation over a few cycles, a large amplitude of oscillation can be maintained to continuously deliver power to the receiver.

To create a precise PSK angle, i.e. for QPSK, the shifting frequency and duration must be controlled precisely. A timing architecture was developed, modifying the existing mixed-signal IC architecture to automatically adjust the shifting frequency, creating the desired phase angle of rotation within a given number of cycles. The method stores the phase of the nominal carrier frequency immediately prior to a phase transition, using an auxiliary PLL function. Once the transmission of a PSK symbol has taken place, the stored and actual phase of the drive are compared. The shift frequency is increased or decreased to reduce the phase error, hence the system can adaptively adjust itself for the optimum phase angle from an indeterminate starting point. The magnitude of the phase error is accumulated to allow a proportional response, reducing the calibration time. Across different configurations of $90^O/180^O$ rotations in 2-16 cycles, a phase error of less than 3^O at 1MHz was observed when using the adaptive frequency calibration method.

10.1 Experimentation with higher voltages

The first and second fabricated ICs can withstand up to 20V and 50V peak excursions respectively on the integrated HV switch devices. For higher power levels with the current ICs, larger voltages would be present and hence off-chip tuning switches would become essential. Functionality was included in the second IC for operation of off-chip HV switches and resonance detection, allowing the chip to be used for tuning and resonance control. However, these external functions were not tested due to time limitations. A logical extension of this project would be the evaluation of these controls. External HV devices may have very large propagation delays, so use of the phase trimming functionality may also be essential to achieve accurate tuning.

A further extension with higher voltages and frequencies would be to redesign the system in a more advanced process, for example Gallium Nitride, which has been demonstrated in high power and high frequency DC-DC converters [48]. This would allow the system to remain fully integrated whilst being able to withstand the higher peak voltages on the antenna. Furthermore, the higher electron mobility in the technology may permit faster timing circuits, leading to a higher timing accuracy for a given operating frequency or operation at a higher frequency band, such as 6.78MHz or 13.56MHz.

10.2 Automatic Delay Compensation with Phase Trimming

As shown in section 7.4, compensation for phase delay to maintain accurate tuning becomes essential as the operating frequency is increased. The systems implemented in this project required manual phase trimming to achieve the ideal resonant condition at 2MHz, however commercial systems for inductive coupling may operate at much higher frequency bands such as 6.78MHz and 13.56MHz, hence phase trimming compensation becomes even more critical.

Most of the tuning error in the fabricated ICs is caused by the propagation delay of the HV switch drivers, since the capacitor switches are likely to be large LDMOS devices with higher gate capacitances when compared to 1.8V or 5V antenna driver circuits. Hence an automatic phase trimming system must take account of the propagation delay of the HV switch driver chains to align the actual switching action symmetrically around the rising and falling edges of the antenna drive waveform.

10.3 Simultaneous compensation of multiple antenna tuning settings

As mentioned in section 8.4, simultaneous adjustment of the antenna tuning for multiple operating frequencies may be possible. This allows the antenna tuning loops for the data modulation frequencies to be at or close to the ideal resonant condition even when not in immediate use, so that minimal disturbance will be observed on the magnetic field strength when they are activated.

However, the non-linear relation between the antenna tune setting and resonant frequency introduces a processing overhead. The system also needs to be aware of the available tuning range in order to apply the correct amount of scaling to the inactive tuning loop settings. A system architecture which reduces the complexity of this operation could be investigated to make the concept feasible.

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12 Appendices

12.1 Appendix A: Design of Test Inductors

The inductors used for antenna circuits in this project were required to have a high Q factor, so that they would represent a realistic implementation in a commercial system. The required inductance varied depending upon the operating frequency, i.e. smaller inductances are required at higher frequencies for a given capacitance in the resulting LC circuit. Hence, it was necessary to construct inductors manually and tune them to the required range for testing.

To maximise the Q factor, the ratio between the inductance and the resistance of the coil must be as large as possible. The equation for the inductance L of a cylindrical inductor is given by equation 12.1, where μ_0 is the permeability of free space, N is the number of turns, r is the radius and l is the length, as per figure 12-1. The ohmic resistance of the coil of wire is given by equation 12.2, where ρ is the resistivity and A is the cross sectional area of the wire. Substituting these two expressions into the Q factor relation in equation 12.3 reveals that Q is proportional to the inductor radius and number of turns of wire. Hence both of these should be maximised in order to achieve the highest Q factor possible.

$$L = \frac{\pi \mu_0 r^2 N^2}{l} \tag{12.1}$$

$$R = \frac{2\pi \rho r N}{lA} \tag{12.2}$$

$$Q = \frac{\omega L}{R} = \frac{\pi \mu_0 r^2 N^2 / l}{2\pi \rho r N / lA} = \frac{\omega \mu_0 r N A}{2\rho} \tag{12.3}$$

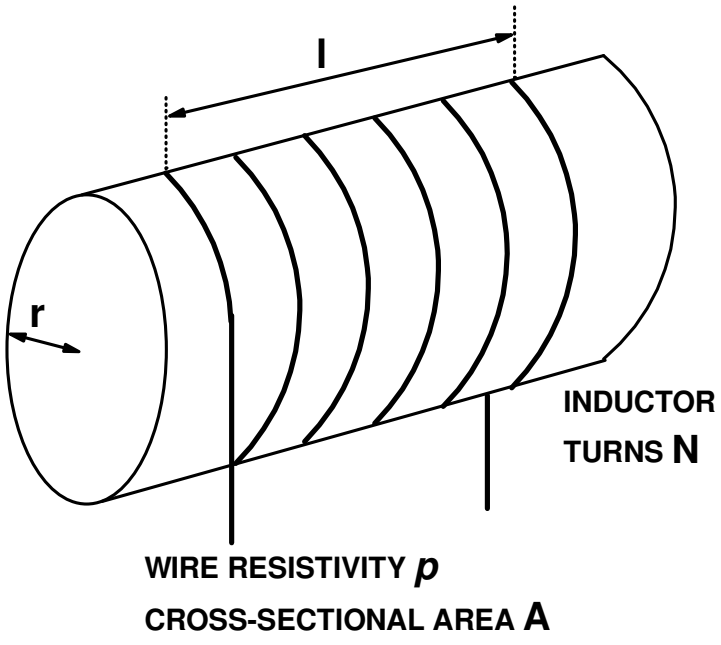

Figure 12-1: Inductor parameters for calculating the Q factor

For a given resistivity, the ohmic resistance of the coil can also be reduced by increasing the cross-sectional area A of the wire. Note that this conductive area must take account of the skin effect, whereby high-frequency signals will be conducted along only the outer edge of a conductor. Thus a multi-stranded conductor such as Litz wire should be used to maximise the effective cross-sectional area

without significantly increasing the insulated wire diameter. Otherwise, the number of turns of the coil could be reduced by the unusable cross-sectional area of a single-core wire as per figure 12-2.

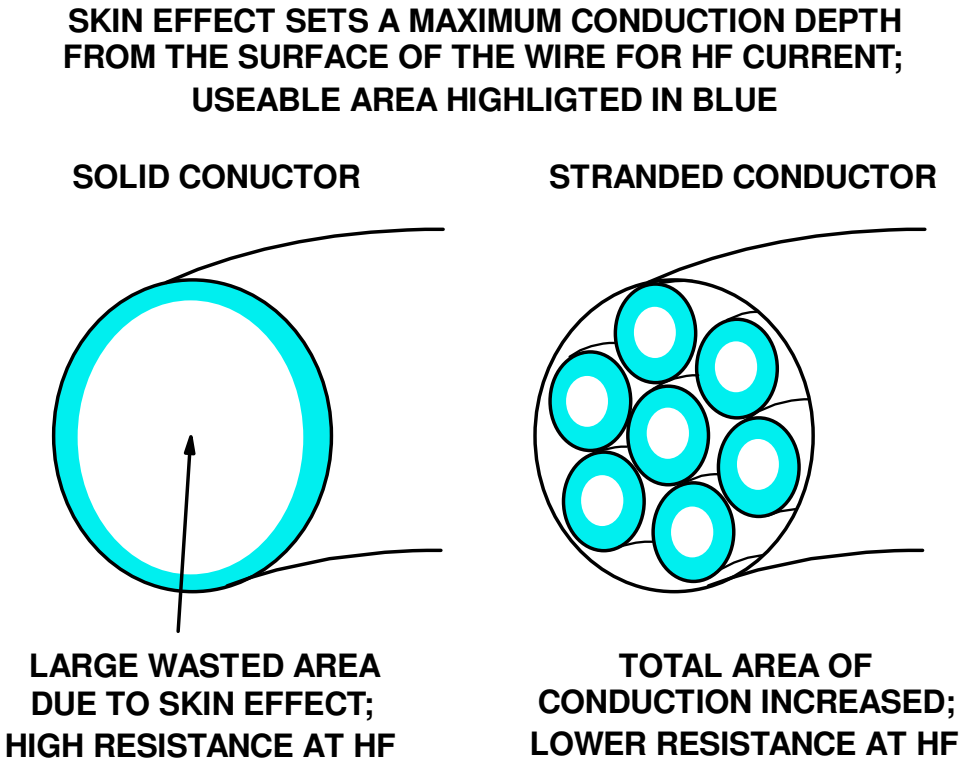

Figure 12-2: Solid vs stranded conductor behaviour with the skin effect

Adding a ferrous core with a high permeability to the coil will increase the inductance without the need for changing the dimensions [49]. However, two effects reduce the viability of this approach for wireless power. Firstly, “eddy currents” may be induced in cores made of conductive materials such as iron, which causes some energy to be dissipated in the electrical resistance of the core [50]. Secondly, if the inductor current is large enough, magnetic saturation in the core may limit its flux density and hence limit the magnetic field strength, which in turn limits the amount of energy stored [51]. Hence a practical wireless power system is more likely to use an air-cored cylinder inductor, as per the earlier derivations.

12.2 Appendix B: LTSpice simulation schematics

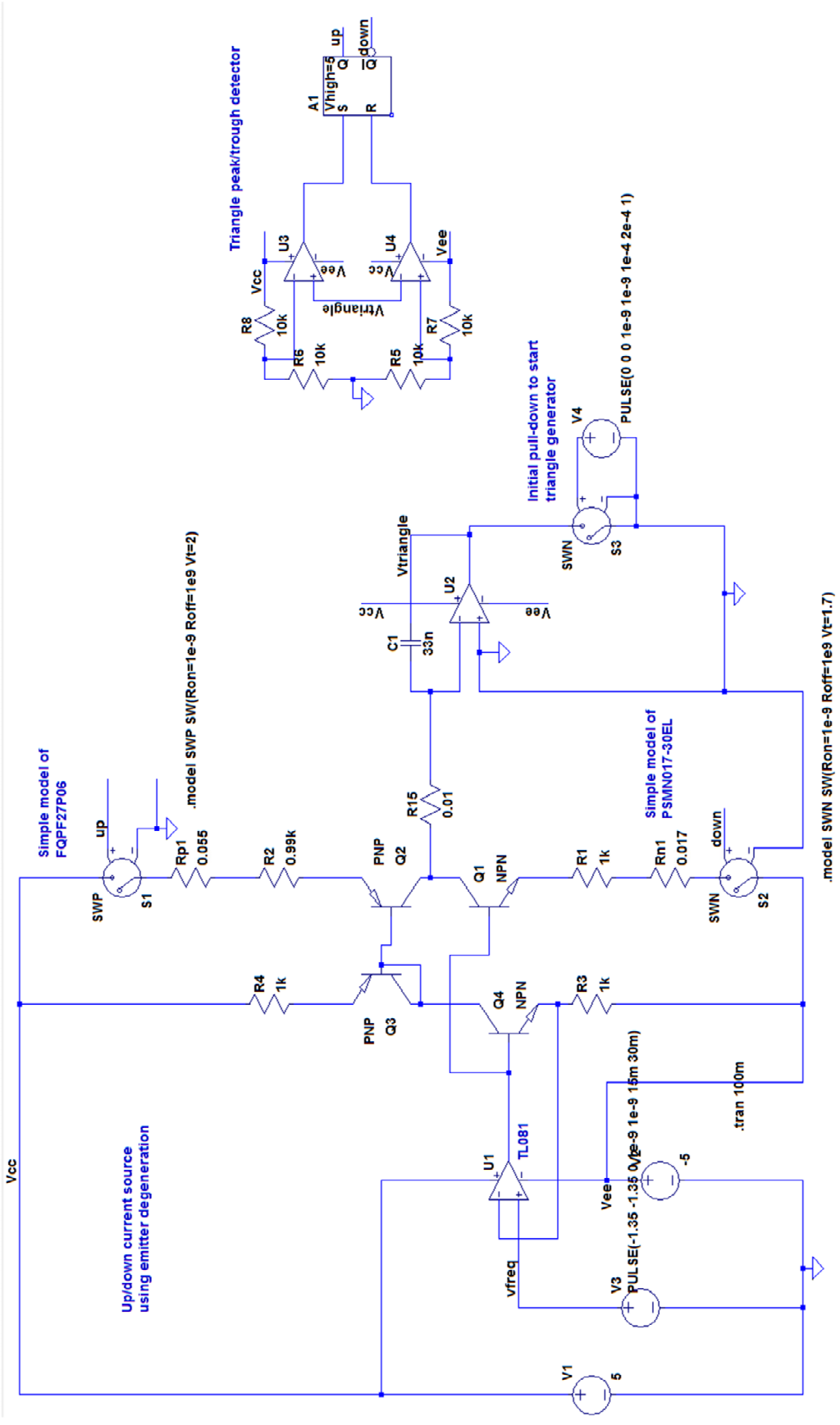

Figure 12-3: Triangle integrator oscillator behavioural simulation, using BJT up/down current mirror with emitter degeneration (see Appendix D).

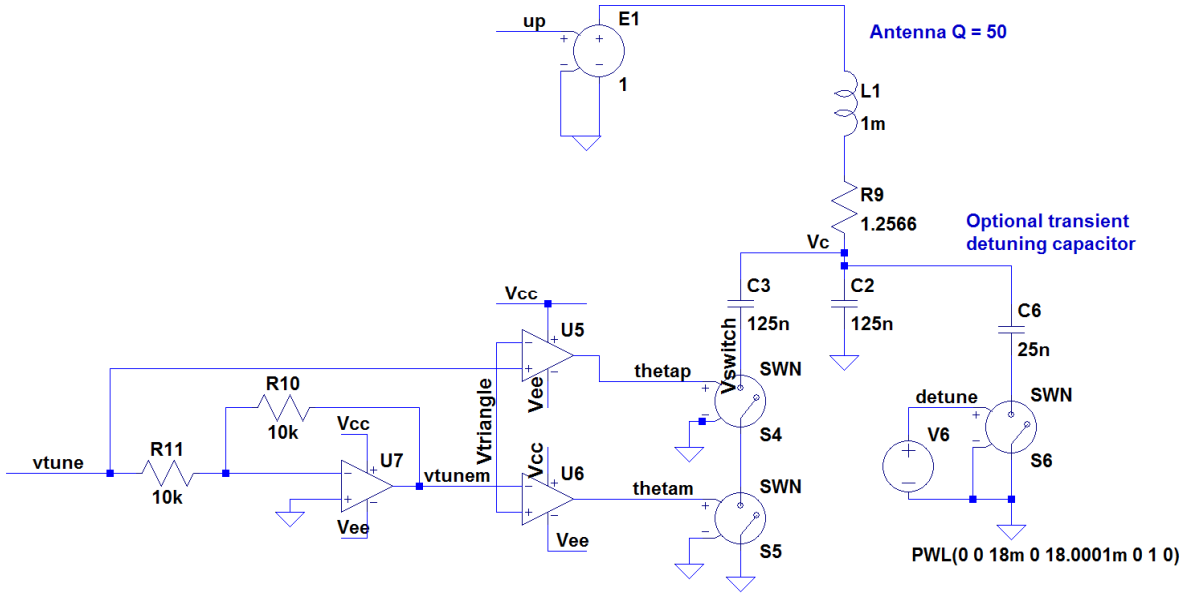

Figure 12-4: LTSpice behavioural LC antenna with switched fractional capacitor tuning, and behavioural transient detuning capacitor for self-tuning behavioural simulation

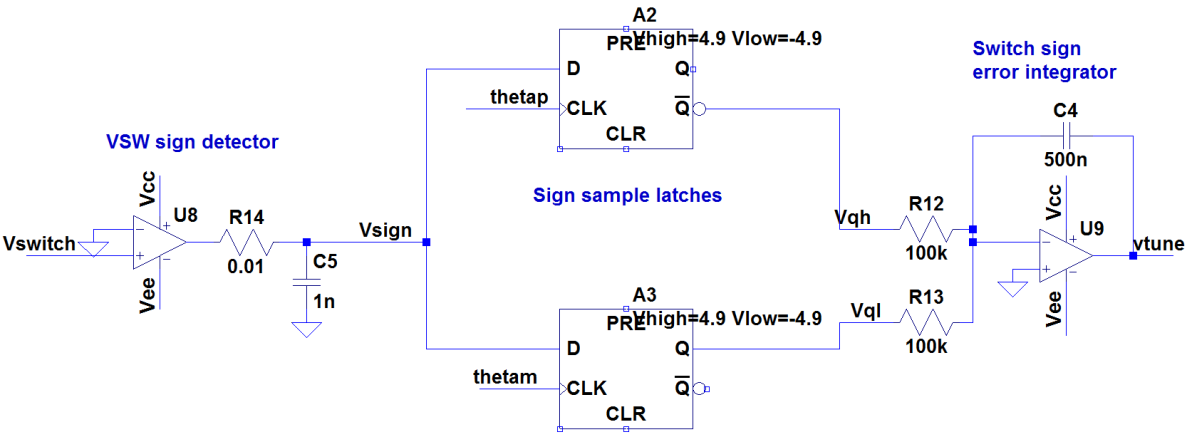

Figure 12-5: LTSpice behavioural generation of V_{TUNE} by integration of V_{SW} error sign

12.3 Appendix C: Breadboard schematics and design

12.3.1 Implementation of triangle generator and LC tank (10kHz)

Implementation into physical components was done on a copper clad board with small cut sections of strip-board glued on for circuit nodes. This "Manhattan" style layout meant that the copper clad board could be used as the ground node for all components and that the ground resistance would be very low between any two points on the board. All ICs on the board were also fitted with 100nF decoupling capacitors on each power pin to avoid transient loading of the supply rail from causing false triggering or other undesirable behaviour in of the system.

Figure 12-7 shows the final breadboard implementation of the triangle generator. The up/down current source for creating the triangle voltage was done using BJTs with emitter degeneration (see appendix D). The peak and trough of the triangle were set using 22kΩ potentiometers whose output was decoupled with 100nF capacitors. LM311 comparators were used for their convenient level-shift output control, allowing logic levels to be adjusted if need be. [52]

The RS latch was implemented using a pair or NOR gates, using a quad 2-input NOR 74HCT02. The LM311 datasheet specifies that the typical propagation delay is around 165ns, which is negligible compared with the maximum operating frequency of 12.78kHz. The datasheet recommends that the pull-up resistors be around 1kΩ, although a lower value of 560Ω was used to increase the slew rate.

LM311 comparator was used as a driver for the MOSFETs, using a potential divider between V_{cc} and ground as the reference. Decoupling of the reference was not necessary here as the input was entirely digital, e.g. slight variations in the threshold due to transient loading on the supply would not be detrimental to operation. Given the gate capacitance of the MOSFETS (1.1nF for the NMOS [53] and 0.552nF for the PMOS [54]), a lower pull-up resistor of 100Ω was used for the MOSFET driving comparator to provide more current during the transition period.

The LC tank driven using a 74HCT125 single rail quad buffer, with all four buffers in parallel to maximise the drive current, with the total rated output current of 70mA [55]. From simulation, the tank current during resonance was no more than approximately 4mA making the quad buffer more than sufficient. The output resistance of the buffer was also not an issue since it would be dominated by the 1kΩ resistor in the attenuator.

The capacitor switch was implemented with an ADG452 quad transmission gate IC. On a dual-rail 5V supply the typical output resistance of a single switch is approximately 7Ω [34], so all four switches were placed in parallel so that the overall resistance would be under 2Ω so that it would not contribute greatly to the Q factor. Figure 12-6 shows the schematic of the breadboard LC tank.

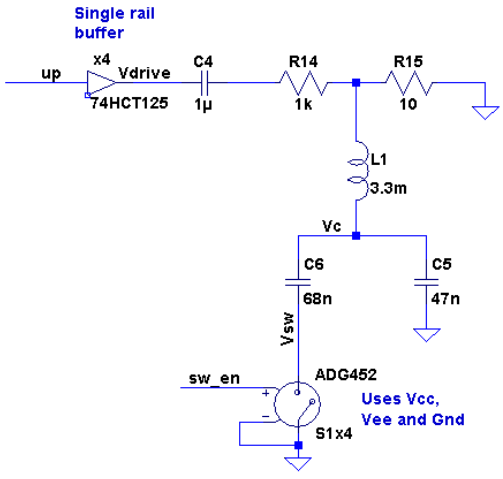

Figure 12-6: Breadboard LC tank circuit with driver and switched tuning capacitor

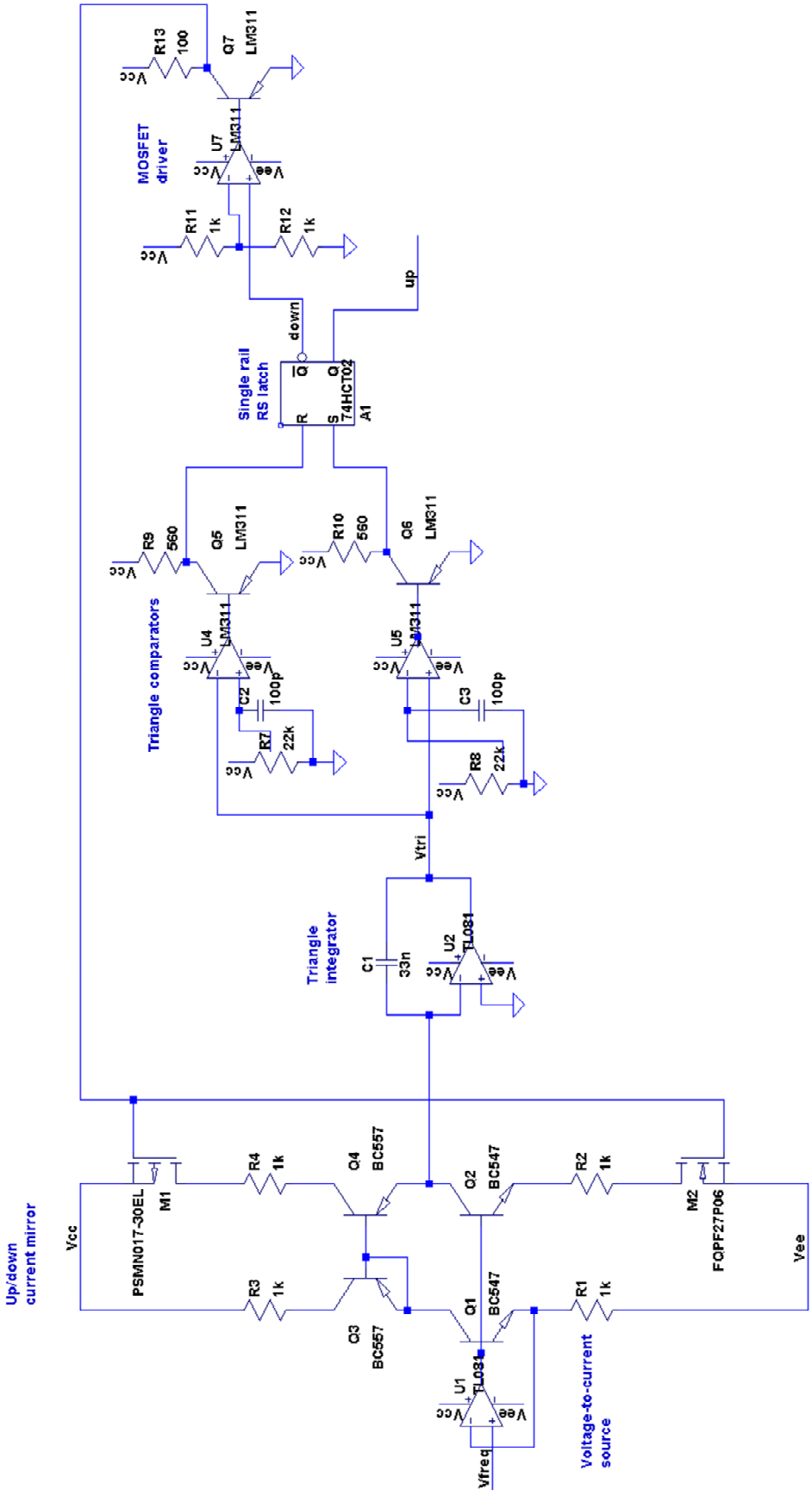

Figure 12-7: Breadboard triangle generator for 10kHz regio

12.3.2 Implementation of basic tuning (10kHz)

For basic tuning, LM311 comparators with 560Ω pull-ups were used to drive a 74HCT08 AND gate. A TL081 was configured as an inverting amplifier using 1kΩ resistors to produce symmetrical slicing levels. Figure 12-8 shows the triangle slicing circuit used.

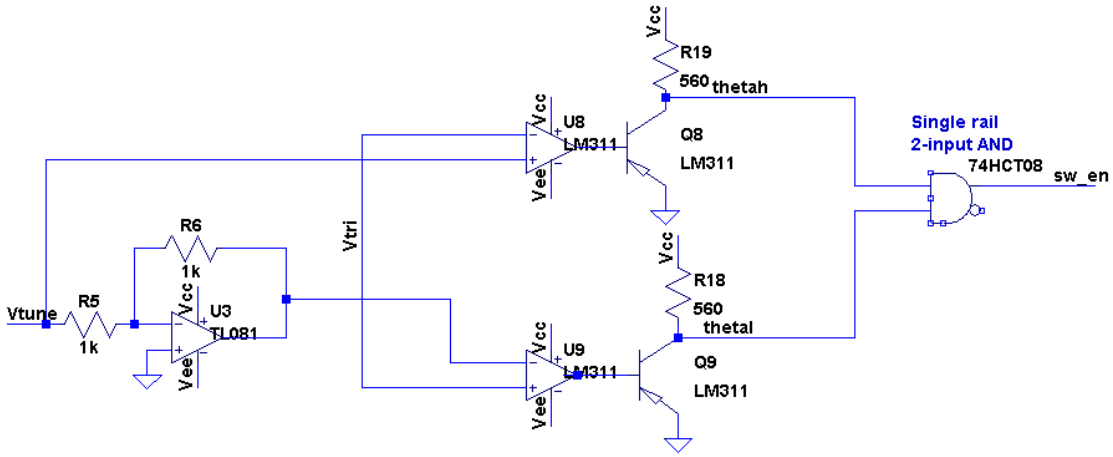

Figure 12-8: Breadboard triangle slicer

12.3.3 Implementation of automatic tuning (10kHz)

Continuous self-tuning was implemented using the circuit in figure 12-9. The LM311 was used again as the sign-detecting comparator, connecting to a pair of dual rail D-type flip-flops, to capture the signs of the end voltages on the positive and negative excursions respectively. The use of dual rail flip-flops meant that the self-tuning integrator could use the ground rail as its reference voltage.

To level shift from the single rail logic level of the theta signals, a 1uF capacitor and 1MΩ resistor to ground was used as a crude level shift, removing the DC component and shifting the +5V/0V logic to +2.5V/-2.5V, which was sufficient to trigger the D-type flip-flops.

Note that as per the LTSpice simulations, no additional time delay was explicitly added to either the switch control or the sign-detecting comparator output. The propagation delay of the switch-enabling AND gate and the delay of the LM311 produced a combined delay that was large enough to ensure that the sign information at the input of the D-type is valid at the moment it is clocked.

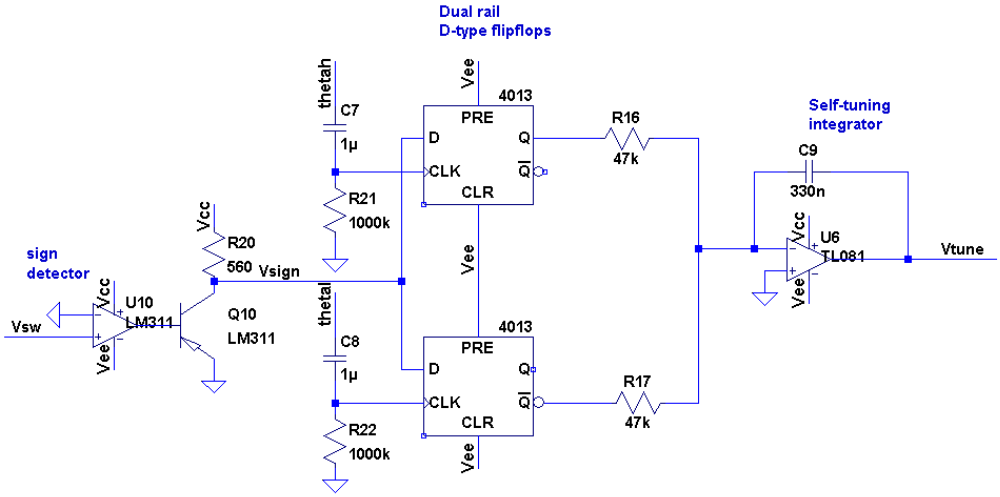

Figure 12-9: Breadboard switch voltage sign detector and self-tuning integrator

12.3.4 Implementation of basic tuning (125kHz)

Figure 12-10 shows the circuit used for the 125kHz band breadboard, although components such as pull up resistors are omitted for clarity. In order to produce clean waveforms, the supplies of the comparators and the logic ICs were filtered using 10Ω resistors combined with local decoupling and bulk capacitance, reducing the appearance of high-bandwidth switching noise on the tank signals. The pull up resistors on the LM311 comparators were increased to 1kΩ from the previous design in order to reduce the inrush current caused by switching, which further reduced the switching noise on the supply rails.

To implement the tank driver, the FQPF27P06 (PMOS) and PSMN017-30EL (NMOS) in the previous up/down current mirrow were re-used. It was necessary to level shift the gate drive voltage for the PMOS device, since V_{drive} was small compared with the V_{th} of the MOSFETs. 5V/0V gate levels were used for the NMOS, whilst V_{drive}/-5V levels were used for the PMOS. These voltages were sufficiently large ensure that the MOSFETs did not remain in their linear region.

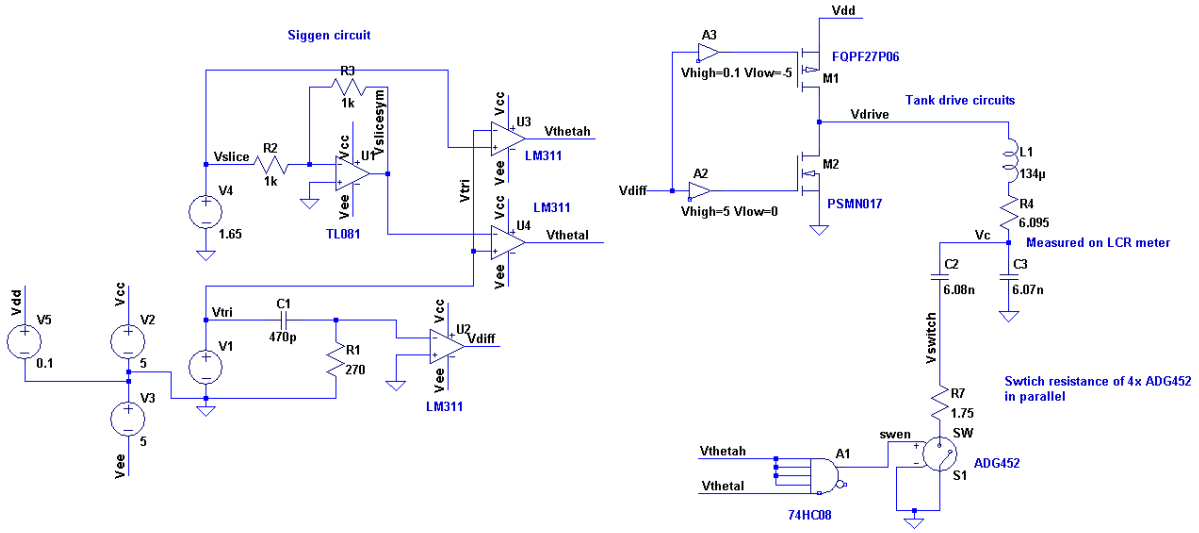

Figure 12-10: Circuit used for 125kHz breadboard

12.4 Appendix D: Up/down current source emitter degeneration approach

The current source itself could have been implemented with an RC circuit, as per figure 12-11. Due to the virtual Earth theorem, the current is set by the input reference voltage divided by the resistor value R. If the two selectable reference voltages have equal magnitude, then a symmetrical triangle wave may be produced.

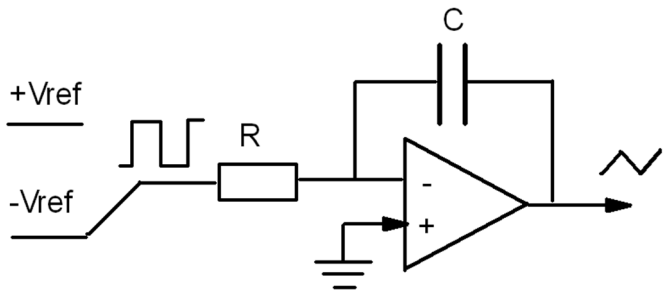

Figure 12-11: RC triangle generator

An alternative method of generating the symmetrical up and down currents was to use an up/down current mirror, using a single reference, as per figure 12-12. A fixed DC current is mirrored using a PNP and an NPN transistor. The direction of current is determined by switching on the required output branch whilst switching off the other. The up/down current mirror architecture was chosen for the 8-12kHz breadboard as it allowed for convenient control of the frequency from a single voltage source.

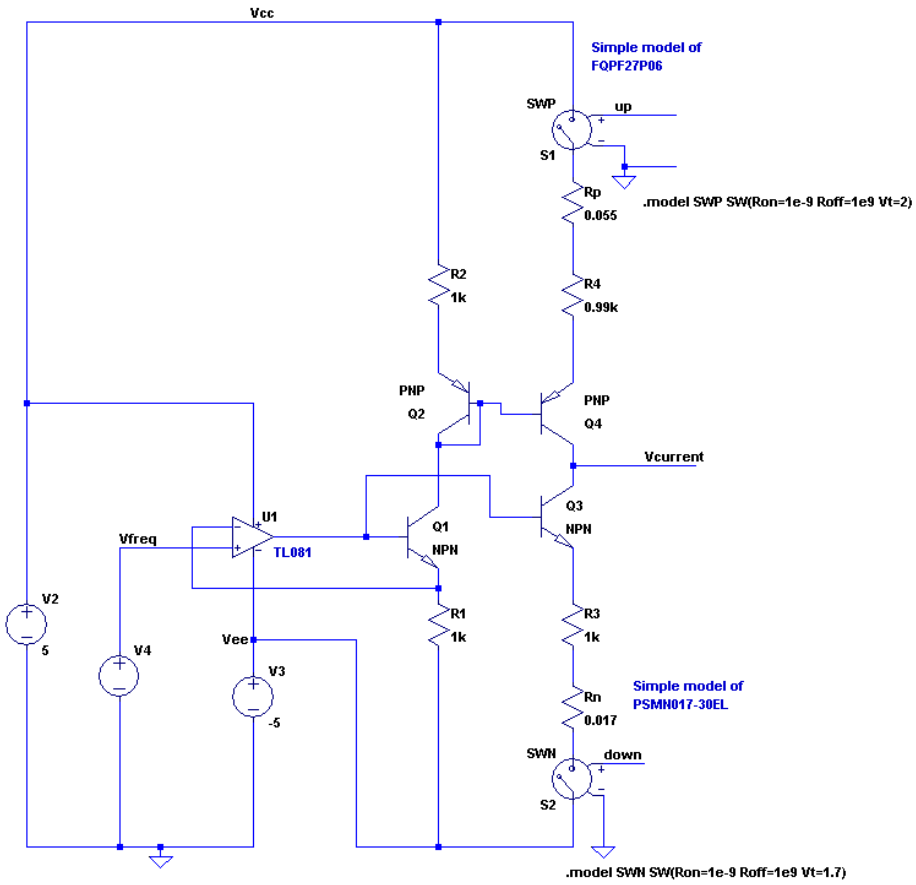

Figure 12-12: Up/down current mirror used for triangle generation. The MOSFETs are modelled as ideal switches with a drain-source resistance.

BC547 and BC557 bipolar junction transistors (BJTs) were used for the up/down current source. The voltage to current converter amplifier was not required to be high speed and so a TL081 was used as it was readily available.

Emitter degeneration resistors was used for the current mirror. This increases the output impedance of the current source and makes it behaviourally closer to an ideal current source. It also mitigates the effect of differences between each transistor caused by the temperature dependency of the thermal voltage which affects the current gain, which may in turn lead to current mismatch between the input and output.

Figure 12-13 shows the circuit and DC behavioural models for a BJT with emitter degeneration. The intention is that the voltage V_B is well controlled, as this sets the bias for both the input and output device in a current mirror. Equations 12.4 and 12.5 show that the base voltage may be expressed in terms of the base current, scaled by the emitter resistor and the thermal voltage.

$$V_B = V_E + V_{BE} = I_E R_E + \frac{kT}{q} Ln\left(\frac{I_B}{I_S}\right) \tag{12.4}$$

$$V_B = R_E I_S(\beta + 1) e^{\frac{qV_{BE}}{kT}} + \frac{kT}{q} Ln\left(\frac{I_B}{I_S}\right) = R_E I_B(\beta + 1) + \frac{kT}{q} Ln\left(\frac{I_B}{I_S}\right) \tag{12.5}$$

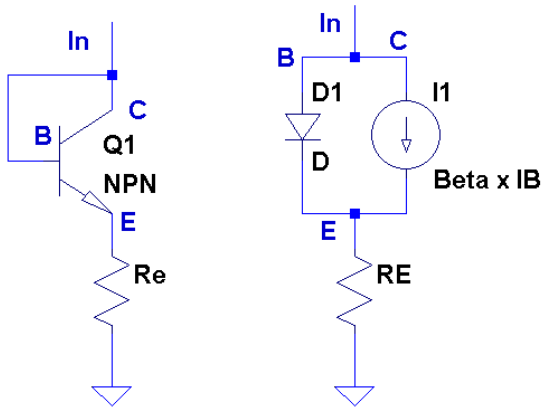

Figure 12-13: Left: NPN BJT with emitter degeneration resistor. Right: equivalent DC model of left-hand circuit

For the emitter resistor to dominate the base voltage, it is recommended to set the voltage drop across the emitter degeneration resistance according to equation 12.6. To achieve this with the minimum current of 2.7mA in this system, R_E should be at least approximately 96Ω.

$$V_{R_e} = 10\frac{kT}{q} \approx 260mV \; at \; room \; temperature \tag{12.6}$$

The emitter degeneration resistor was also used for the voltage-to-current converter circuit. Although only approximately 96Ω was required for mitigating the effect of the thermal voltage, a 1k resistor was chosen, as this allowed for a wider voltage range to control the current whilst still meeting the thermal voltage requirement. The desired frequency range is available with an input voltage from 2.7V to 4.2V above the reference rail, set by the product of the emitter degeneration resistor and the current required.

To switch between up and down currents, PMOS and NMOS devices were used so that complementary control of the current direction could be easily implemented, i.e. only one input is required to set the direction. The FQPF27P06 was selected for PMOS and PSMN017-30EL for NMOS as these both had low drain-source resistances (R_{ds}), 0.055Ω and 0.019Ω respectively. For simulation, these were modelled as ideal switches with a threshold voltage and constant drain-source resistance.

12.5 Appendix E: Circuit Schematics and test benches for "lctune018" IC modules

12.5.1 Voltage to current amplifier

Figure 12-14 shows the schematic of the voltage-to-current amplifier. A standard 2-stage architecture with compensation capacitance was used.

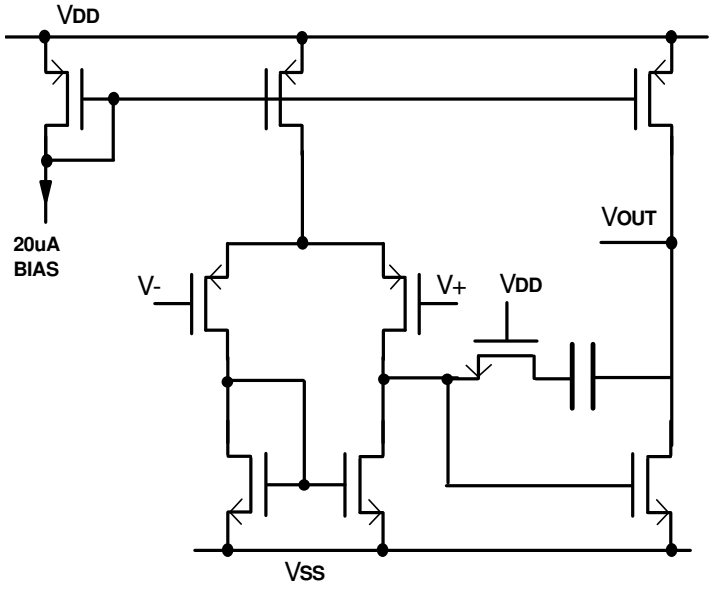

Figure 12-14: Test configuration for Voltage-to-Current conversion op-amp

From process corner simulation, the designed V-to-I amplifier had a minimum open-loop DC gain of 88dB, a maximum unity gain frequency of 4.219MHz and minimum phase margin of 66.31 degrees. The nominal systematic offset was tested using the V-to-I circuit in figure 12-15, as this was the typical operating setup for the op-amp. The obtained systematic offset was 24.17μV.

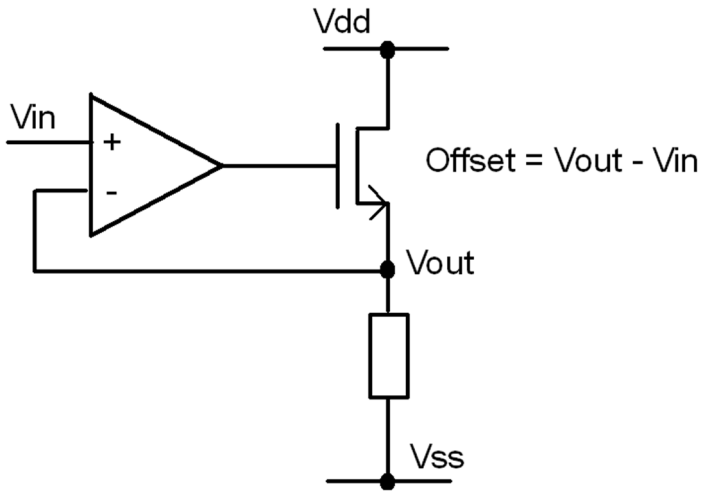

Figure 12-15: Test configuration for Voltage-to-Current conversion op-amp

12.5.2 Current buffer amplifier

Figure 12-16 shows the schematic of the current buffer amplifier.

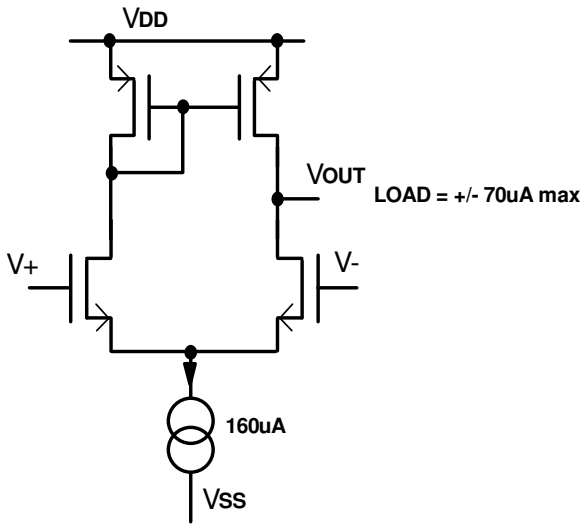

Figure 12-16: Current buffer amplifier circuit schematic

Figure 12-17 shows the test configuration of the buffer op-amp, whereby a current source is stepped between fixed positive and negative magnitude at 2MHz.

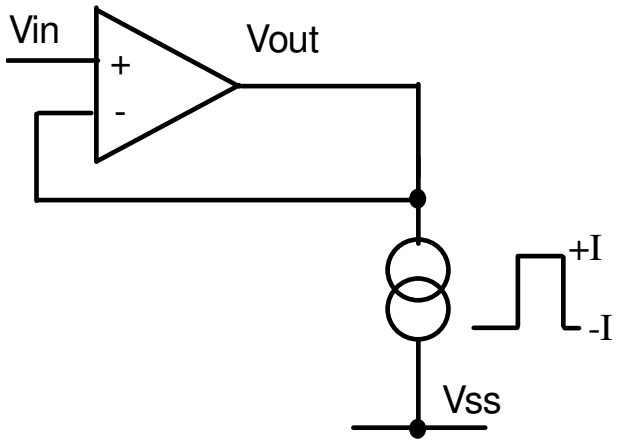

Figure 12-17: Test configuration of voltage buffer amplifier

Figure 12-18 shows the output voltage offset for varying load current. The worst case offset is under 80mV, hence the operating condition of the current steering mirror will not be vastly different depending on where it is connected to the output or the buffer amplifier.

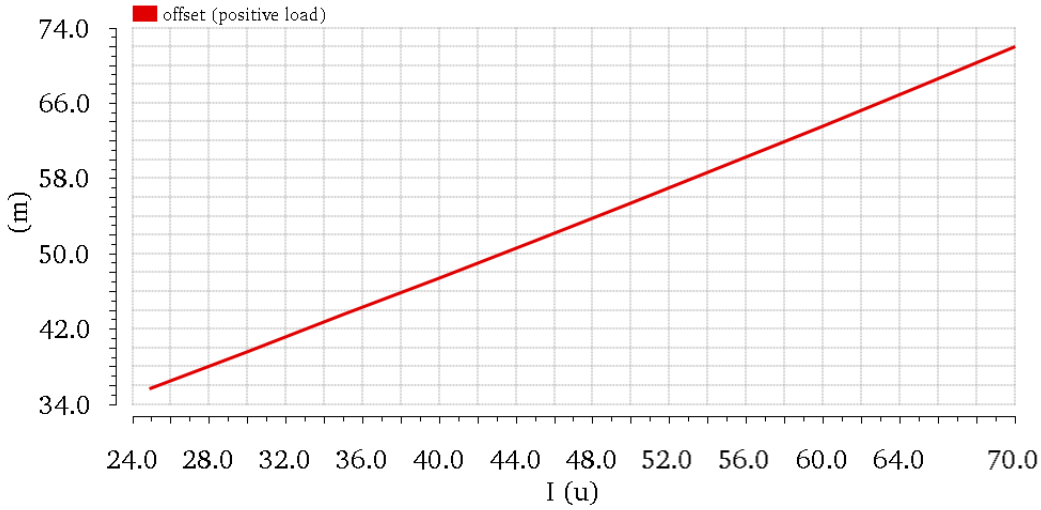

Figure 12-18: Output offset voltage of buffer amplifier under varying test load current

The settling time of the output voltage to within 1% of the final value is shown in figure 12-19. Settling time increases with load current, since a greater voltage offset is being created by the higher current load. The worst case settling time is less than 4ns under maximum load, which is more than fast enough to ensure that the current mirror is kept saturated.

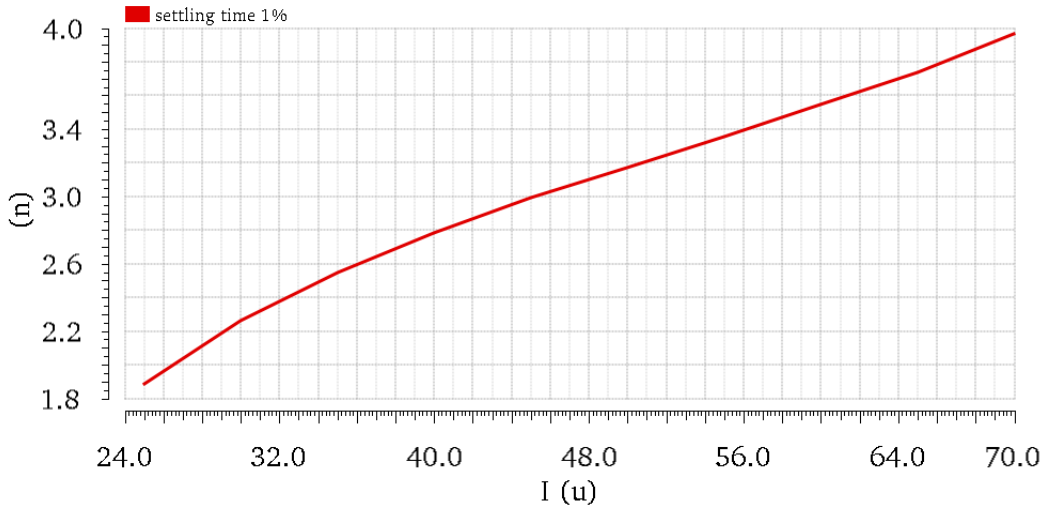

Figure 12-19: Voltage buffer amplifier output voltage settling time (to within 1% of final value)

12.5.3 Current integrator amplifier

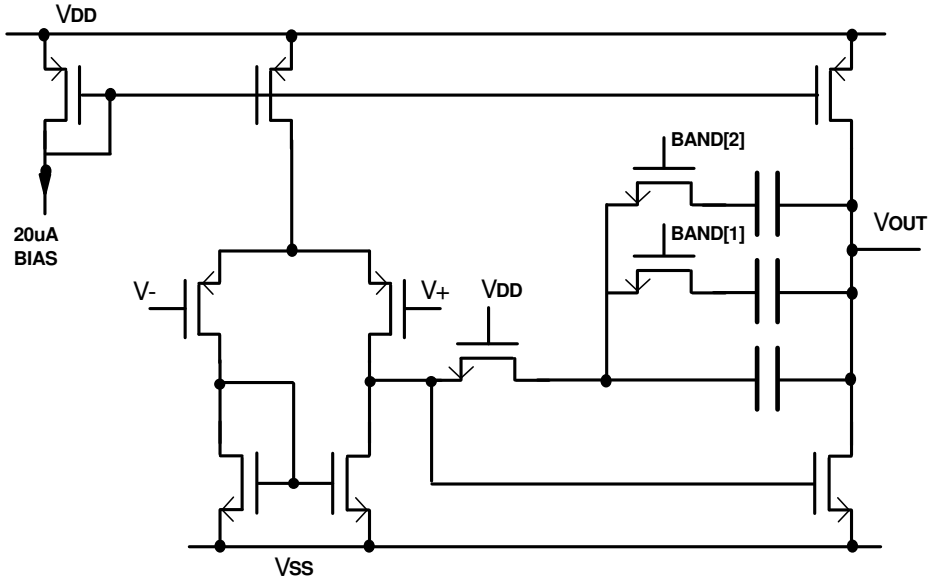

Figure 12-20: Triangle integrator opamp with programmable miller capacitance for wider operating range.

Note that since the integration amplifier had to work across a wide bandwidth (100kHz – 2MHz), it was important to ensure that the phase margin remained roughly constant across the entire range. Measurement of the AC response of the integrator op-amp was done using the test circuit in figure 12-21. Each band was tested by performing an AC sweep with the feedback capacitance set to the band integration capacitance. A 100MΩ feedback resistor and 1mF capacitor between V_- and ground were also connected in the simulation test bench to assist with DC operating point convergence.

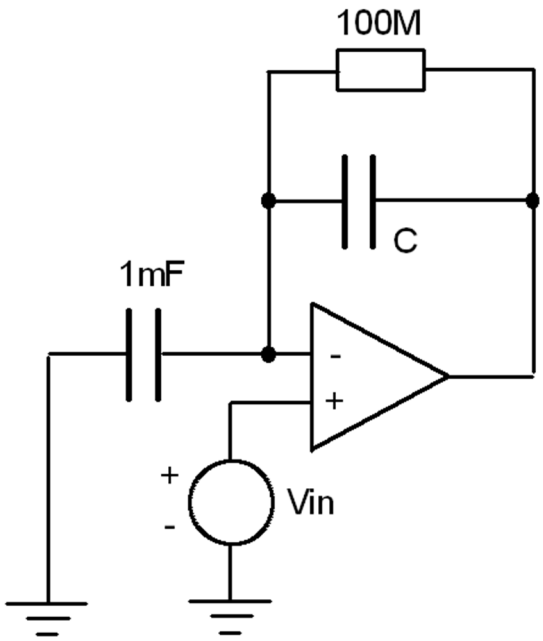

Figure 12-21: Test circuit for AC analysis of integrator op-amp

It was found to be necessary to increase the compensation capacitance C_c as frequency increased. Table 12-1 shows the frequency ranges, required compensation and resulting phase margin. The additional capacitors were aligned with the integration capacitance decode logic.

f_{max}	f_{min}	$C_{feedback}$	C_c	Phase margin	f_0
2MHz	1MHz	4.17pF	2.50pF	69.8	94.3MHz
1.5MHz	750kHz	5.56pF	2.50pF	64.4	87.4MHz
1.13MHz	563kHz	7.41pF	2.50pF	58.5	79.5MHz
844kHz	422kHz	9.88pF	4.00pF	69.3	55.8MHz
633kHz	316kHz	13.2pF	4.00pF	62.9	50.3MHz
475kHz	237kHz	17.6pF	4.00pf	56.8	45.0MHz
356kHz	178kHz	23.4pF	5.50pF	60.1	33.7MHz
267kHz	133kHz	31.2pF	5.50pF	54.0	29.9MHz
200kHz	100kHz	41.6pF	5.50pF	48.3	26.4MHz
150kHz	75.0kHz	55.5pF	5.50pF	43.2	23.1MHz

Table 12-1: Integrator op-amp compensation capacitance and extracted AC analysis parameters for each band of operation

Figure 12-22 shows the triangle being generated at 2.57MHz, using the extracted layout of the integrator op-amp with the schematic level current DAC, integration capacitors and slice comparators. The difference between the positive and negative slew rates is 0.6%, which was more than symmetric enough to keep signals derived from the triangle in phase to less than one degree.

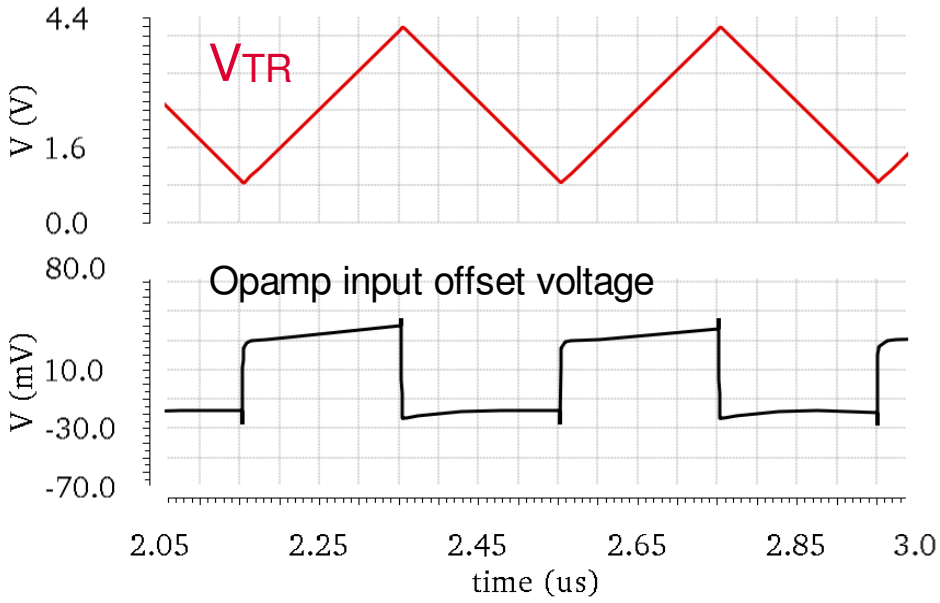

Figure 12-22: Triangular output and op-amp input offset voltage at 2.57MHz

The measured input offset voltage was up to 40mV with an input current of 70µA, meaning that the designed op-amp had a transconductance of 2mS. Whilst this was less than specified, it was deemed acceptable since the triangle was visibly not very distorted. Furthermore, the fact the offset is only visible on the peaks and troughs meant that its effect on slicing was minimal in any case.

12.6 Appendix F: Test Board Design for lctune018 IC

A custom test board was required for evaluation of the lctune018 system. The board needed to permit the test of both the IC system functionality (i.e. tuning an LC tank circuit with large-signal amplitude) and the individual block functionality. To determine the circuitry required, an exhaustive test plan was devised as per table 12-2.

Test	Name	Purpose	New requirements
0	Board test	Determine that the test PCB is functioning correctly without an IC present	IC must be removable → A chip holder is preferred
1	IC power-up test	Measure the IC power consumption and power-up functionality with no load	Need power supplies and bias currents. Need filtering and ability to measure power consumption. Load LC circuit must be removable → Use headers to permit quick reconfiguration.
2	ATB test	Check that all ATB nodes behave as we expect	Need digital interface to control the IC registers → Option for on-board or off-board control of logic signals. Need adjustable output/input for ATB node for voltage/current observation/injection.
3	Operating frequencies	Check that main oscillator can operate at all bands	Need ability to set *freqsel* input high or low
4	Digital fixed tuning	Check that digital tuning operates and adjusts HV switch duty cycle	Need to observe *swls* and *swhs* lines (high impedance)
5	Analog operation	Adjust tuning duty cycle with external slice voltages. Adjust operating frequency with external oscillator current.	Need to be able to set *mslicel* and *msliceh* (low impedance voltage inputs). Need to be able to adjust *imfreq* current.
6	LC tank tune (manual, analog)	Drive and tune LC tank circuit. Test manual tuning with analog setting of slice levels and currents)	Need high-Q LC tank circuit → Require inductor construction. Need attenuator to control amplitude to protect HV switches → Require schottky diodes to reference potentials to provide additional protection.
7	LC tank tune (manual, digital)	Re-create resonant condition using digital frequency and tuning settings.	
8	LC tank tune (automatic)	Check that self-tuning of LC tank operates correctly	Control on *clocken* pin to enable or disable automatic tuning (high impedance)

Table 12-2: Test modes and PCB requirements for lctune018 IC

Figure 12-23 shows a simplified schematic of the PCB developed to help perform the above tests. Where possible, through-hole components were selected for easy board construction and modification in case of errors or additional functionality being required. Every pin except the power supplies had a Schottky diode to 0V and the corresponding supply to provide additional protection in case of ESD or accidental over-voltage/under-voltage during testing. This was particularly important on the tank driver output and HV switch drains, where excessive voltage could be present when driving an external LC circuit.

Each power supply is derived from an off-board power supply, with bulk capacitor and decoupling capacitor filtering to provide the smoothest reference possible. Rail-to-rail low-bandwidth opamp buffers were selected to provide the 2.5V and DAC references to provide a low noise bandwidth reference from the supply. Potentiometers with a fixed series resistance were used to set bias/test currents to allow easy setting and measurement.

The digital interface pins were controlled by tri-state switches to tie the inputs to 0V, 1.8V or a high-impedance pin for off-board connections. Tie resistors were provided to pull each one to the normal state when the high-impedance pin is selected. A series resistance is also provided to help limit the input current incase of accidental over-voltage/under-voltage.

Functionality was provided for a resistive attenuator on the output of the tank driver. The option for an additional series capacitor was provided in the LC circuit to permit testing of capacitor divider configurations. With the use of through-hole components, these could be easily bypassed to permit different test arrangements.

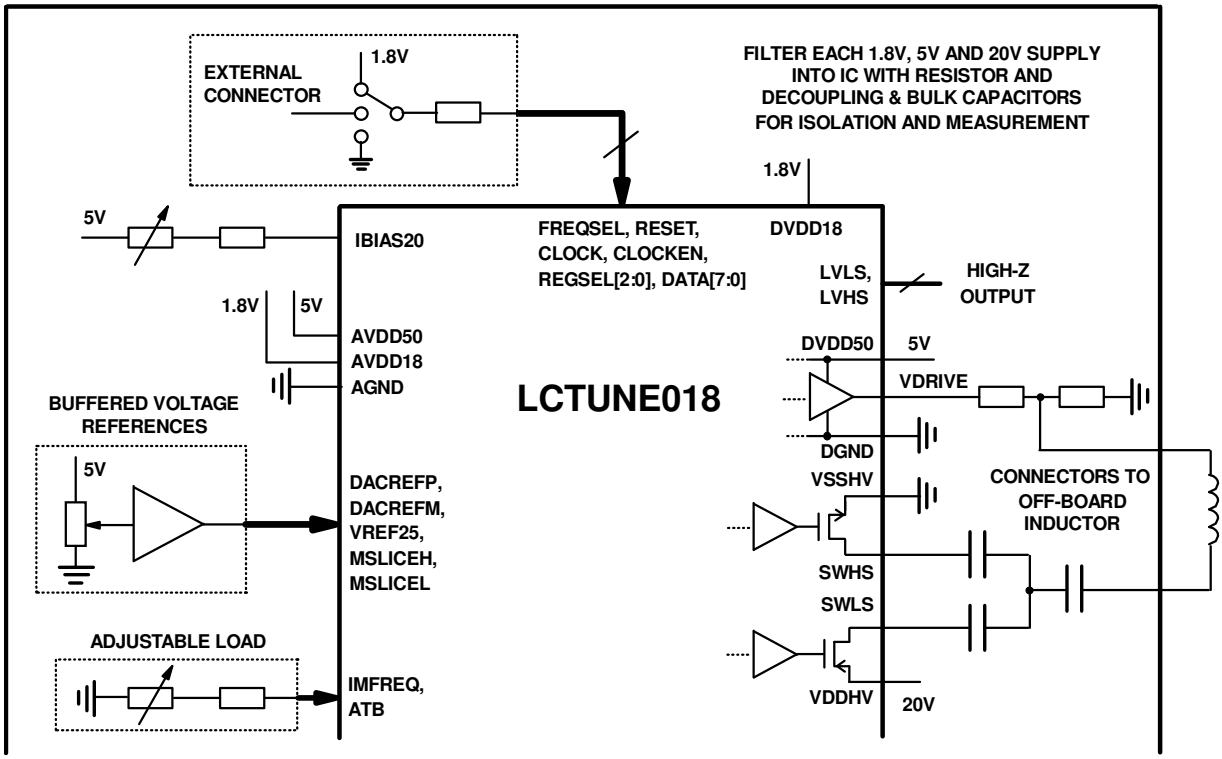

Figure 12-23: Simplified schematic of test board for lctune018

The PCB layout (figure 12-24) were entered into Eagle. The lctune018 test IC shares the same package as another project, hence additional circuitry is present on the lower half of the schematic for this. The layout was implemented as a 2-sided PCB; additional layers were not necessary and could hinder debug functionality.

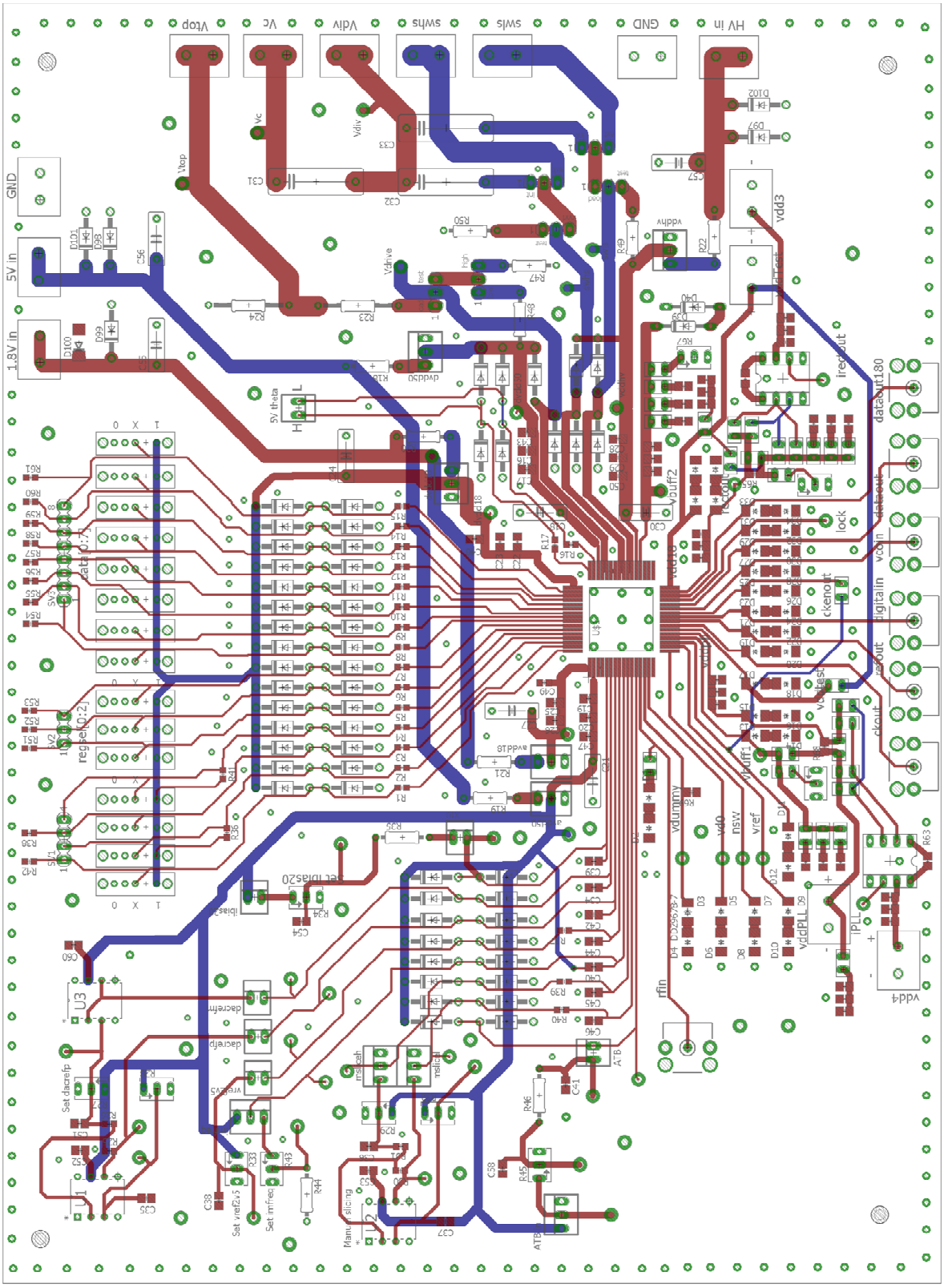

Figure 12-24: PCB layout of lctune018 test PCB (top and bottom layers shown)

12.7 Appendix G: "lctune018_psk" IC module details

12.7.1 Current integrator amplifier

With a lower minimum operating frequency, the largest integration capacitance expected to increase from 55.5pF to 503pF (approximately one order of magnitude), hence it was necessary to re-simulate the integrator op-amp for stability with this increased capacitive load. It was expected that the available compensation should also increase by one order of magnitude in order to maintain a uniform spacing of the poles of the op-amp when the larger capacitive load is used. Table 12-3 shows simulation results and required compensation capacitance. Additional compensation capacitors of 10pF and 40pF were included into the integrator op-amp to maintain an acceptable phase margin of at least 45^{O}.

F_{max}	F_{min}	$C_{feedback}$	C_c	Phase margin	f_0
2.00MHz	1.00MHz	4.17pF	2.5pF	68.9^{O}	93.2MHz
1.50MHz	750kHz	5.56pF	2.5pF	63.8^{O}	86.7MHz
1.13MHz	563kHz	7.41pF	2.5pF	58.3^{O}	78.3MHz
844kHz	422kHz	9.88pF	4.0pF	68.7^{O}	54.8MHz
633kHz	316kHz	13.2pF	4.0pF	62.9^{O}	50.7MHz
475kHz	237kHz	17.6pF	4.0pF	57.1^{O}	45.8MHz
356kHz	178kHz	23.4pF	5.5pF	60.2^{O}	34.4MHz
267kHz	133kHz	31.2pF	5.5pF	54.0^{O}	30.1MHz
200kHz	100kHz	41.6pF	5.5pF	48.7^{O}	26.9MHz
150kHz	75.1kHz	55.5pF	15.5pF	69.5^{O}	14.1MHz
104kHz	52kHz	80.1pF	15.5pF	60.9^{O}	12.1MHz
72kHz	36kHz	116pF	55.5pF	86.5^{O}	5.00MHz
49.9kHz	24.9kHz	167pF	55.5pF	77.0^{O}	4.25MHz
34.5kHz	17.3kHz	241pF	55.5pF	68.0^{O}	3.73MHz
23.9kHz	12kHz	348pF	55.5pf	59.0^{O}	3.11MHz
16.6kHz	8.28kHz	503pF	55.5pF	51.5^{O}	2.68MHz

Table 12-3: Integrator op-amp compensation capacitance and extracted AC analysis parameters for each band of operation

12.7.2 Digital control register map and IO timings

Table 12-4 is a full list of registers for the lctune018_psk IC. Timings for write and read cycles are provided in figure 12-25. The timings given are observed from simulation of the extracted layout on the worst-case PVT corner (125^{O}C, slow process, -10% reduction in DVDD18 supply). Timings assume an impedance consisting of 100Ω and 7nH in series with 10pF to ground at the input to model the effects of bondwires, internal path resistance and capacitance (see figure 12-26).

Addr	Bits	W/R?	Name	Function
0	[7:0]	W	gain_nom	Antenna tuning integrator gain (nominal frequency)
1	[7:0]	W	gain_fast	Antenna tuning integrator gain (fast frequency)
2	[7:0]	W	gain_slow	Antenna tuning integrator gain (slow frequency)
3	[7:0]	W	freqnom	Main oscillator frequency (nominal)
4	[7:0]	W	freqfast	Main oscillator frequency (fast, manual setting)
5	[7:0]	W	freqslow	Main oscillator frequency (slow, manual setting)
6	[7:4]	W	band	Main oscillator frequency band
6	[3]	W	freqmode	Use internal oscillator current (0) or external (1)
6	[2]	W	modmode	PSK modulation (0) or FSK modulation (1)
6	[1]	W	trimode	Use internal V_{TR} (0) or external (1)
6	[0]	W	capmode	Use internal integrator oscillator capacitors (0) or external capacitor (1)
7	[7:5]	W	pllcapsel	Phase reference PLL filter capacitor value: 000: 1-2MHz, 001: 500kHz-1MHz,

				010: 250-500kHz, 011: 125-250kHz 100: Below 125kHz (use off-chip capacitor)
7	[4:3]	W	pllcursel	Phase reference PLL charge pump current: 00: 5µA, 01: 10µA, 10: 15µA, 11: 20µA
7	[2]	W	pskangle	90^O PSK (0) or 180^O PSK (1)
7	[1:0]	W	cyclecount	PSK phase transition cycles: 00: 2 cycles, 01: 4 cycles, 10: 8 cycles, 11: 16 cycles
8	[7:5]	W	cycleshift	PSK phase shift / cycle: 000: 90^O/cycle, 001: 45^O/cycle, 001: 22.5^O/cycle, 010: 11.25^O/cycle, 100: 5.625^O/cycle
8	[4:2]	W	plldiv	Phase reference PLL integer-N divider ratio: 000: 256, 001: 512, 010: 1024, 011: 2048, 100: 4096, 101: 8192, 110: 16384, 111: 32786
8	[1]	W	autofreq	PSK manual shift frequency (0) or automatic shift frequency calibration (1)
8	[0]	W	NOT USED	Bit not wired
9	[7:4]	W	KP	Shift frequency calibration loop gain: 0000: Gain = 1 (no shift) 0001 – 0111 = Gain > 1 (left shift error 1-7 places) 1000 – 1111 = Gain < 1 (right shift error 1-8 places)
9	[3]	W	signmode	Antenna tuning loop use internal V_{SW} error sign (0) or externally-provided sign data (1)
9	[2]	W	tunemode	Antenna tuning loop automatic calibration (0) or use manually set tuning settings (1)
9	[1]	W	symslice	0: Do not enforce symmetrical operation of HV switches (independent antenna tuning loops) 1: Enforce symmetrical operation of HV switches
9	[0]	W	NOT USED	Bit not wired
10	[7:0]	W	hfcount_clamp	Limit HF counter MSBs to this value
11	[7:0]	W	slicefn_man	Manual antenna tuning setting (fast frequency, NMOS switch)
12	[7:0]	W	slicefp_man	Manual antenna tuning setting (fast frequency, PMOS switch)
13	[7:0]	W	slicenn_man	Manual antenna tuning setting (nominal frequency, NMOS switch)
14	[7:0]	W	slicenp_man	Manual antenna tuning setting (nominal frequency, PMOS switch)
15	[7:0]	W	slicesn_man	Manual antenna tuning setting (slow frequency, NMOS switch)
16	[7:0]	W	slicesp_man	Manual antenna tuning setting (slow frequency, PMOS switch)
17	[7]	W	slicemode	Use internally-generated (0) or externally-generated (1) antenna tuning voltages.
17	[6]	W	lockPMOS	Allow PMOS HV switch operation (0) or force PMOS HV switch closed (1)
17	[5]	W	passthrough	Do not connect (0) or connect (1) internal tune voltages to external pins
17	[4]	W	passthrough_sel	Select falling (0) or rising (1) edge comparison voltages to connect to external pins
17	[3]	W	doubleNMOS	0: Operate NMOS HV switch control on negative excursion of V_{TR} only (unipolar switching) 1: Operate NMOS HV switch control on both excursions of V_{TR} (off-chip bipolar switch control)

17	[2]	W	trimsub_nadd	Add (0) or subtract (1) phase trim value from antenna tuning setting
17	[1:0]	W	sample_point	Adjust sample point of internal V_{SW} error sampler: 00: Sample on switch closure (before drive chain) 01: Sample on switch closure (end of drive chain) 10: Sample on end drive chain +2ns 11: Sample of end of drive chain +6ns
18	[7:0]	W	phasetrim	Amount of phase trim adjustment of HV switch control timings relative to V_{TR}
19	[7]	W	sample_capsel	Select V_{SW} capacitive divider
19	[6:5]	W	atbsel1p8_smpl	Connect V_{SW} capacitive divider to ATB 0: V_{SWN} divider, 1: V_{SWP} divider
19	[4]	W	atbsel1p8_inom	Connect copy of nominal frequency current to ATB
19	[3]	W	atbsel1p8_ifast	Connect copy of fast frequency current to ATB
19	[2]	W	atbsel1p8_islow	Connect copy of slow frequency current to ATB
19	[1]	W	atbsel1p8_hfoscc	Connect copy of PLL oscillator current to ATB
19	[0]	W	NOT USED	Bit not wired
20	[7:0]	W	loadfreq	Manual clock for shift frequency accumulators. Input value is not considered. Connects LOAD input to shift frequency accumulator clocks to manually load the set manual shift frequencies.
21	[7:0]	R	slicefn_rise	Antenna tuning setting (fast frequency, NMOS switch)
22	[7:0]	R	slicefp_rise	Antenna tuning setting (fast frequency, PMOS switch)
23	[7:0]	R	slicenn_rise	Antenna tuning setting (nominal frequency, NMOS switch)
24	[7:0]	R	slicenp_rise	Antenna tuning setting (nominal frequency, PMOS switch)
25	[7:0]	R	slicesn_rise	Antenna tuning setting (slow frequency, NMOS switch)
26	[7:0]	R	slicesp_rise	Antenna tuning setting (slow frequency, PMOS switch)
27	[7:0]	R	freqf	Fast shift frequency accumulator value
28	[7:0]	R	freqs	Slow shift frequency accumulator value

Table 12-4: System control register address map

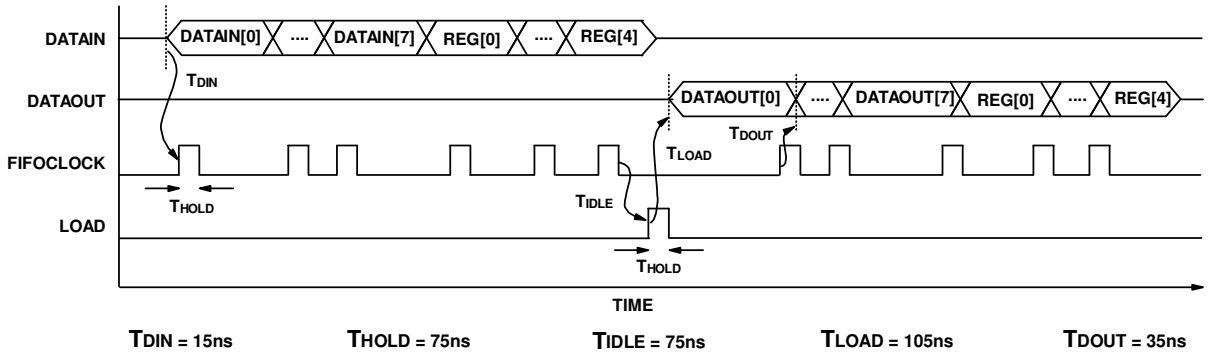

Figure 12-25: Digital IO recommended timing diagram (absolute minimum timings)

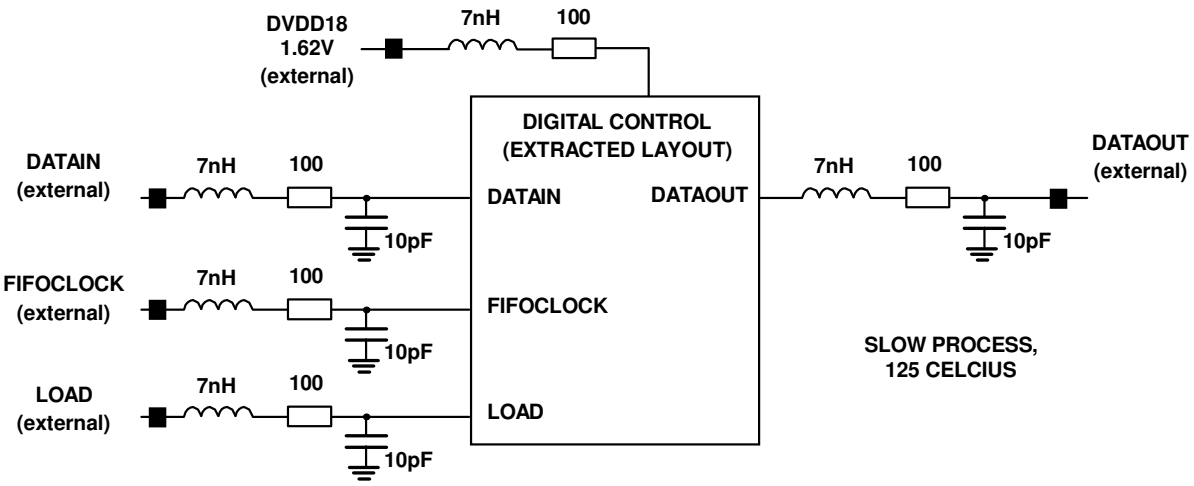

Figure 12-26: Digital IO simulation circuit for worst case timing extraction (timings taken from "external" nodes)

12.7.3 Analogue Test Bus connectivity

Whilst this design had more internal nodes with dedicated external override pins (for example, the antenna tuning voltages), an ATB was included in this design to assist debug and testability. Table 12-5 lists the test points and what the test node indicates.

Test point register name	Description
atbsel1p8_smpl	Connect V_{SW} capacitive divider. Permits observation of the divided switch excursions.
atbsel1p8_inom	Connect copy of nominal frequency current. Permits debug of main oscillator.
atbsel1p8_ifast	Connect copy of fast frequency current. Permits confirmation of frequency calibration loop operation.
atbsel1p8_islow	Connect copy of slow frequency current. Permits confirmation of frequency calibration loop operation.
atbsel1p8_hfoscc	Connect copy of PLL oscillator current. Permits HF oscillator frequency changes to be observed.

Table 12-5: List of ATB points

12.8 Appendix H: Test Board Design for "lctune018_psk" IC

The second test PCB was derived from the first, given the similarities in basic operation. However, there were many differences, requiring adjusted or additional circuits. A new test plan was devised to determine what changes should be made, listed in table 12-6.

Test	Name	Purpose	New requirements
0	Board test	Determine that the test PCB is functioning correctly without an IC present	IC must be removable → A chip holder is preferred
1	IC power-up test	Measure the IC power consumption and power-up functionality with no load	Need power supplies and bias currents. Need filtering and ability to measure power consumption. Load LC circuit must be removable → Use headers to permit quick reconfiguration.
2	Digital IO check	Check that the registers be written to and read with the serial interface.	Need digital interface to control the IC registers → Option for on-board or off-board control of logic signals.
3	Analog IO check	Check that ATB nodes can be observed	Need to source/sink ATB currents/voltages → Multiple impedance options required
4	Static PSK/FSK	Check that modulation of tank driver operates	Need circuit to generate *TXDATA* control pulses for PSK. Must allow on-board or off-board control.
5	Auto PSK	Check that shift frequencies will self-calibrate	
6	New LC tank tuning modes	Check that additional features of LC tank tuning (doubleNMOS, lockPMOS, signmode) work correctly	Need connections for off-board LC circuit and HV bi-directional switch controls.
7	LC tank automatic tuning	Tune LC tank circuit normally using on-chip HV switches	Need connections for off-board inductor. Need protection diodes for HV excursions.
8	Combined LC tank tuning and modulation	Check that automatic tuning of LC tank circuit and modulation features operate together.	

Table 12-6: Test modes and PCB requirements for lctune018_psk IC

The change from 20V HV devices to 50V necessitated a change in Schottky diode. A surface mount component was chosen in order to reduce board area consumption. A lot of the bias circuitry was common to the previous test board and was hence re-used, for example the IC voltage and current references.

For PSK mode to operate correctly on the lctune018_psk IC, the *TXDATA* inputs required brief pulses every time a phase lead or lag was required. The pulse must be at least one cycle in length (so that it will be detected by the control FSM) and a maximum of four cycles (to prevent incorrect operation of the FSM). A pulse generator was developed, which would take rising-edge pulses from a switch and create synchronised controls for *TXDATA_ADV* and *TXDATA_RED*.

Figure 12-27 shows the pulse generator, with a timing diagram provided in figure 12-28. The rising edge of a voltage is AC coupled to create a brief pulse. This is fed into the clock input of a flipflop, triggering it and setting the Q output to be high. The Qbar output is connected to a buffered RC delay line, creating a time delay before forcing the flipflop to reset. The RC delay sets the pulse width, which

must be equal to at least one period at the operating frequency. The pulse is synchronised with the oscillation inside the IC, using an inverted version of the tank driver as a clock reference.

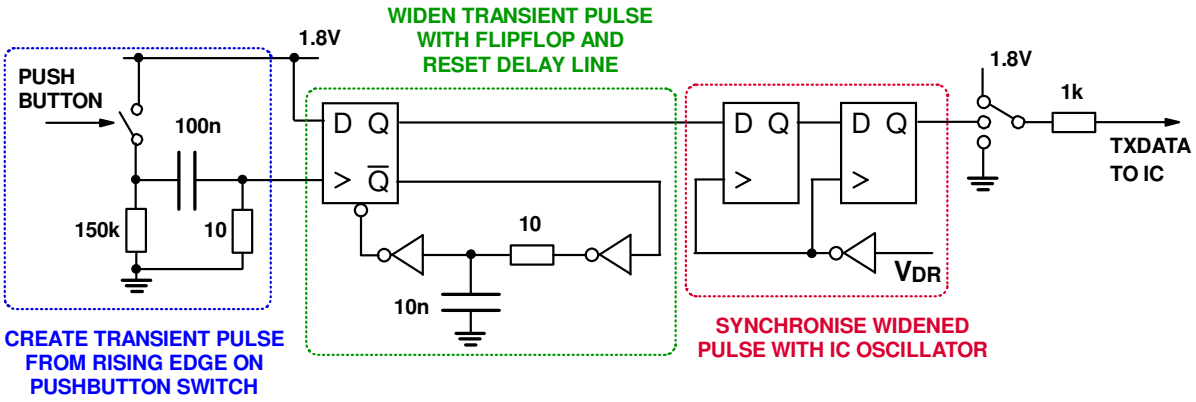

Figure 12-27: Synchronised pulse generator for lctune018_psk test board

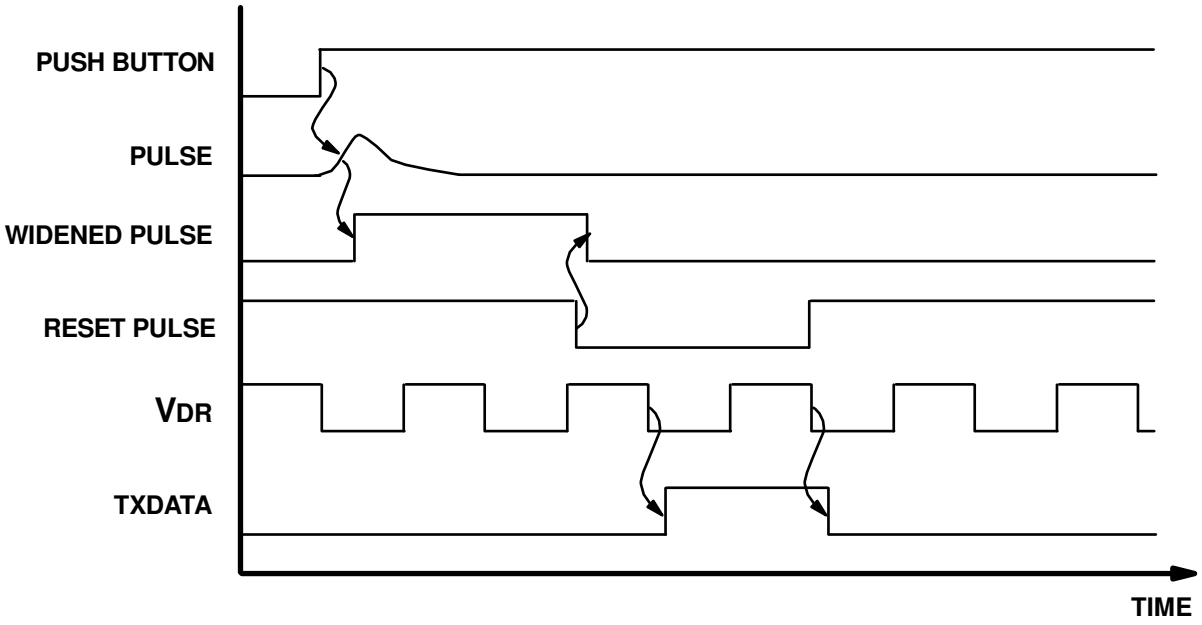

Figure 12-28: Timing diagram for pulse generator

A leadless package was used for the new IC, hence a daughterboard rather than IC holder solution was preferred to allow test ICs to be swapped to avoid the need for an expensive IC holder for leadless packages. The daughterboard would contain the lctune018_psk IC and local decoupling capacitors, whilst the main test PCB would have the reference supply and signal generation features needed for testing, as per figures 12-29 and 12-30.

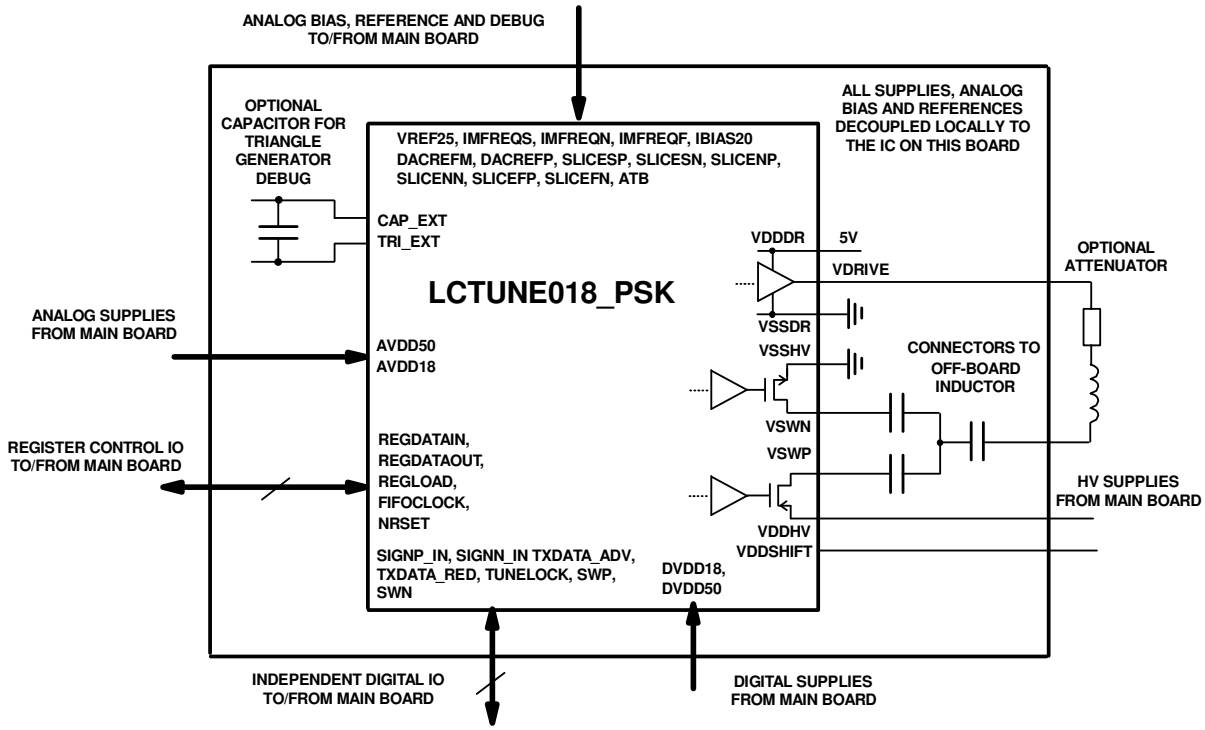

Figure 12-29: lctune018_psk daughter board block simplified schematic

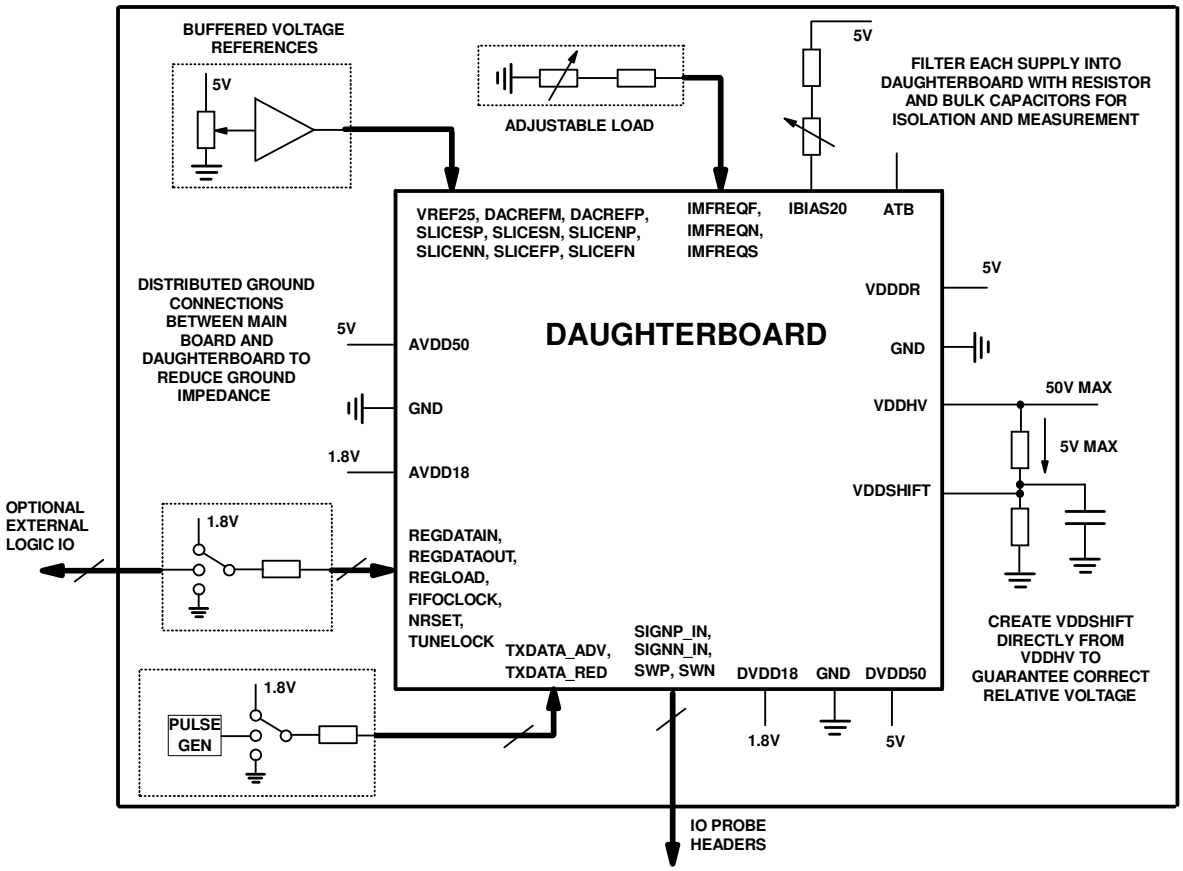

Figure 12-30: lctune018_psk main test board simplified schematic

The resulting layout for the daughterboard is shown in figure 12-31 and 12-32 . Figure 12-33 shows the main test board layout.

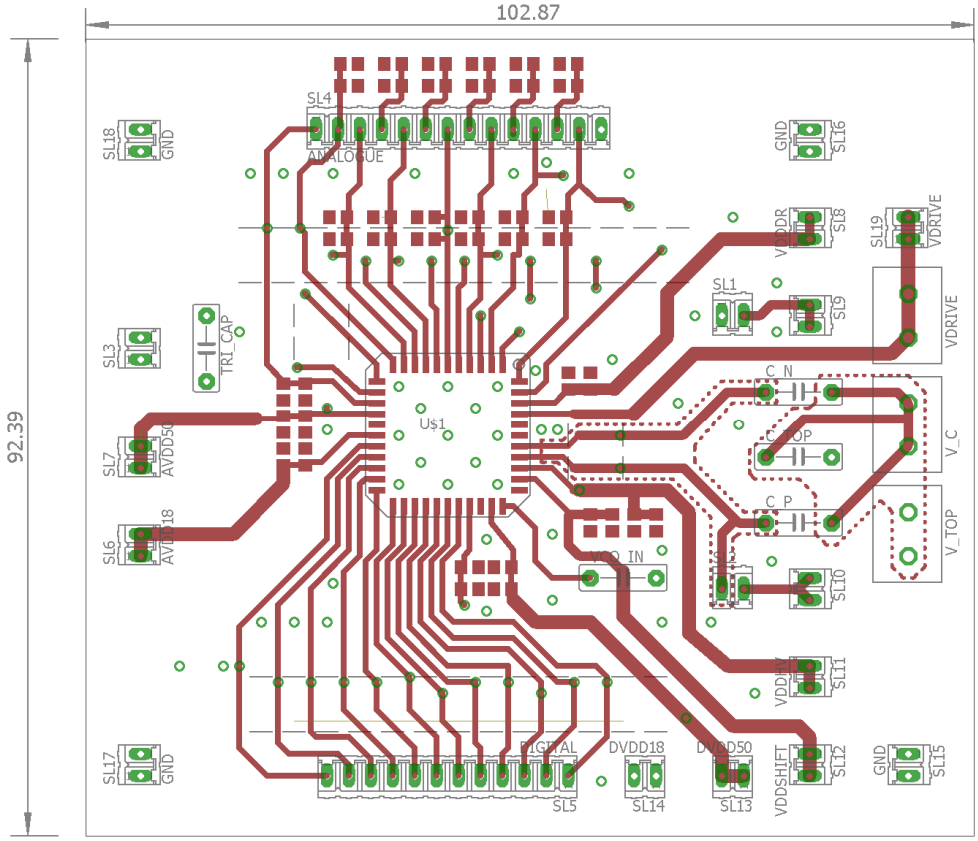

Figure 12-31: lctune018_psk daughter board layout (top layer)

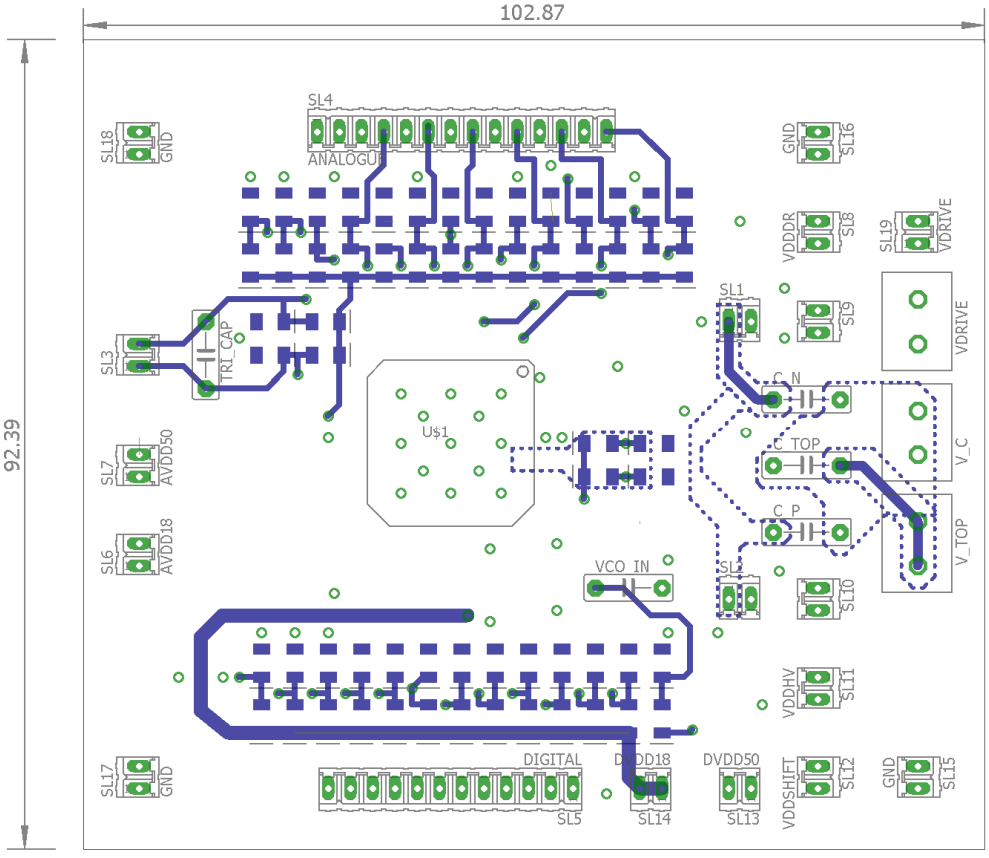

Figure 12-32: lctune018_psk daughter board layout (bottom layer)

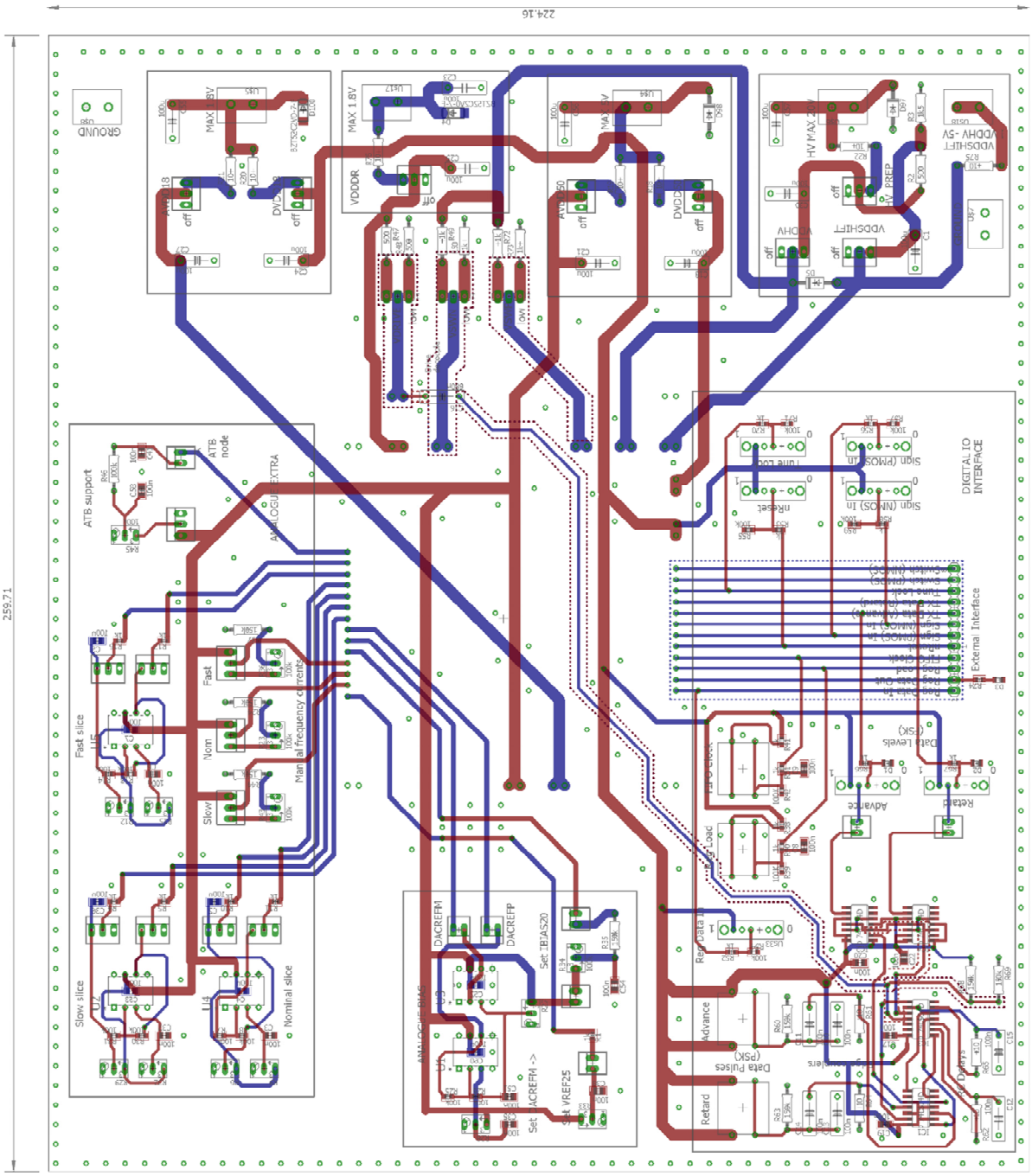

Figure 12-33: lctune018_psk main board (top and bottom layers shown)

12.9 Appendix I: Design of PSK demodulator

An off-chip demodulator circuit was required to create a constellation diagram, allowing the accuracy of repeated phase lead/lag transitions to be shown visually. Previous phase measurements were acquired using a high frequency time-domain oscilloscope, operating at up to 1GS/s, resulting in a phase resolution of 0.36^{O}. However, the oscilloscope was not ideal for capturing a large burst of rapid transitions (i.e. thousands of PSK rotations). A lower frequency Picoscope was available, permitting the acquisition of a high-frequency burst of waveforms directly to a PC, however the sampling rate of 80MS/s was inadequate for accurate extraction of the phase error (providing a phase resolution of 4.5^{O} at 1MHz signal frequency).

The voltage resolution of the Picoscope was 12 bits, i.e. 4096 DAC codes. If this much resolution becomes available in a time-domain sense, i.e. 4096 of samples per period of oscillation of the nominal transmit frequency, the representation of the phase error becomes much more accurate, reducing to less than 0.08^{O}. A system was therefore required which could allow extraction of the phase error by measurement of a voltage at a fixed time instant.

In order to directly extract the phase angle, the V_{DR} signal from the lctune018_psk test IC was used to create a sine IQ wave pair as per figure 12-34. The phase of the IQ waves is aligned with V_{DR}, and held in place whilst the phase shift occurs. Plotting the continuous IQ waves on X and Y axis creates a circle, however sampling the instantaneous voltage of the IQ waves at the end of the phase transition creates a data point which represents the phase angle of rotation.

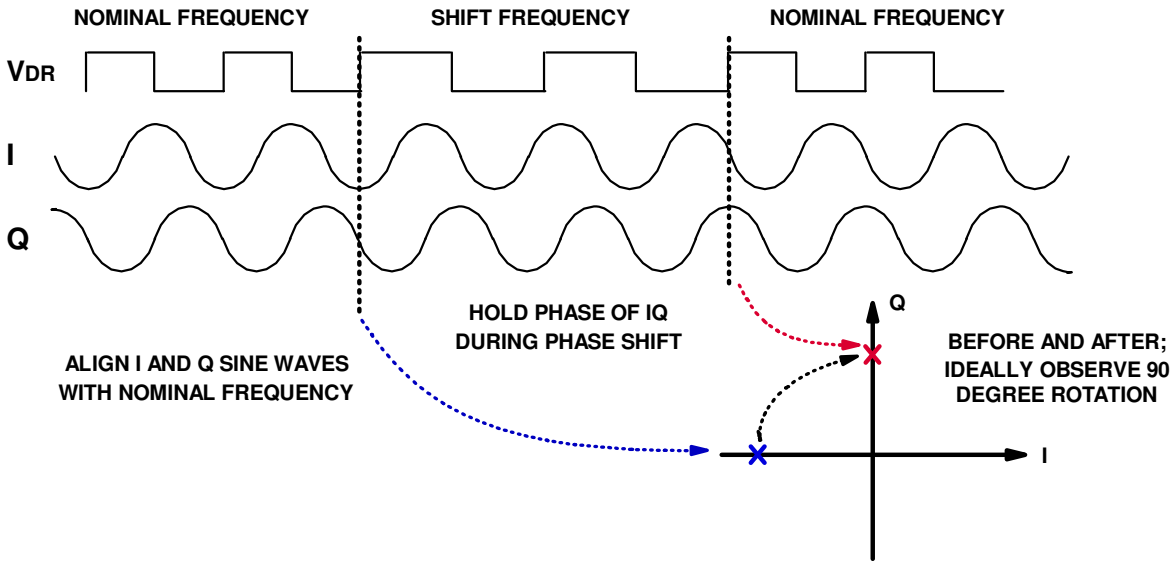

Figure 12-34: lctune018_psk phase rotation measurement using IQ phase reference

Figure 12-35 shows the implemented hardware for the test circuitry, which was implemented onto breadboard with discrete components. The overall topology was based upon the internal circuitry used for shift frequency calibration inside the lctune018_psk IC (i.e. using a PLL to store a phase reference and making a comparison afterward). In this case, additional circuits are needed to create an IQ sine wave pair for creating a constellation.

Note that once the phase transition is complete, the IQ sine reference needs to track the new phase of the nominal carrier, whilst retaining the new absolute phase relative to the initial position. To do this, the PLL reference is switched at the end of the transition to the expected position. If the phase rotation of V_{DR} was correct, then there should be negligible phase error at the end of the phase shift, so the PLL should not need to adjust significantly.

An external function generator provides a square wave at the desired data rate, which is fed through a pseudo-random test pattern generator, activating one of the phase lead and lag controls on the lctune018_psk test PCB. The *TXDATA_ADV* and *TXDATA_RED* controls are fed into a tapped delay line, implemented with a series of flipflops and clocked by V_{DR}, with enough delay elements to accommodate both the FSM/input delay overhead and the PSK transition itself. Output taps are selected and OR-ed together, such that a *HOLDPLL* signal is created to indicate when the phase transition is occurring.

When *HOLDPLL* goes high, the VCO input to the off-chip PLL is held at the present voltage, storing the phase of V_{DR} just before the phase transition begins. At the same time, the PLL reference is adjusted to select the ideal target phase, using an up/down counter which is controlled by the input lead/lag controls. A small time delay is inserted to ensure that the reference is not switched until the PLL VCO is properly held at its present setting.

The PLL VCO output is used as a drive control to a fixed-frequency LC circuit, tuned to resonance at the nominal frequency of V_{DR}, producing a sine wave. The output is connected to an RC polyphaser, formed of a low pass and high pass filter, both with cut-off frequencies set to the nominal frequency of V_{DR}. Each single stage filter causes 45^{O} of phase shift at the cutoff frequency, hence a 90^{O} is created between the outputs two filters, creating the IQ sine waves required for generating the constellation.

Bursts of high-frequency phase transitions were captured using the Picoscope. To avoid the need for a high speed sample and hold circuit, a Matlab script is used to post-process the captured phase transitions and extract the instantaneous value of the IQ waves at the moment when *HOLDPLL* goes low, indicating the phase transition is complete. The IQ values are then plotted on an XY axis. Additional processing to calculate the EVM and maximum phase error are also performed. Figure 12-36 shows the ideal timings for operation. Figure 12-37 shows an example Picoscope capture of the PLL charge pump output, IQ sine waves and *HOLDPLL* at a 1MHz nominal frequency on V_{DR}. The resultant constellation from many data bursts like this is provided in section 8.7.2.2.

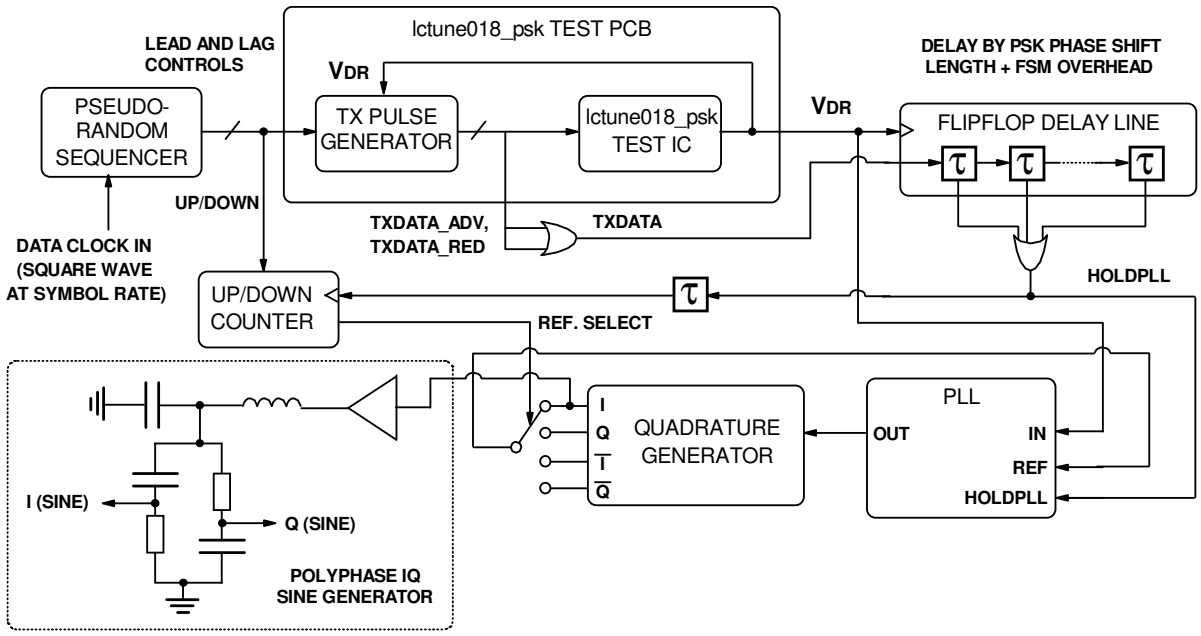

Figure 12-35: Block diagram for lctune018_psk demodulator

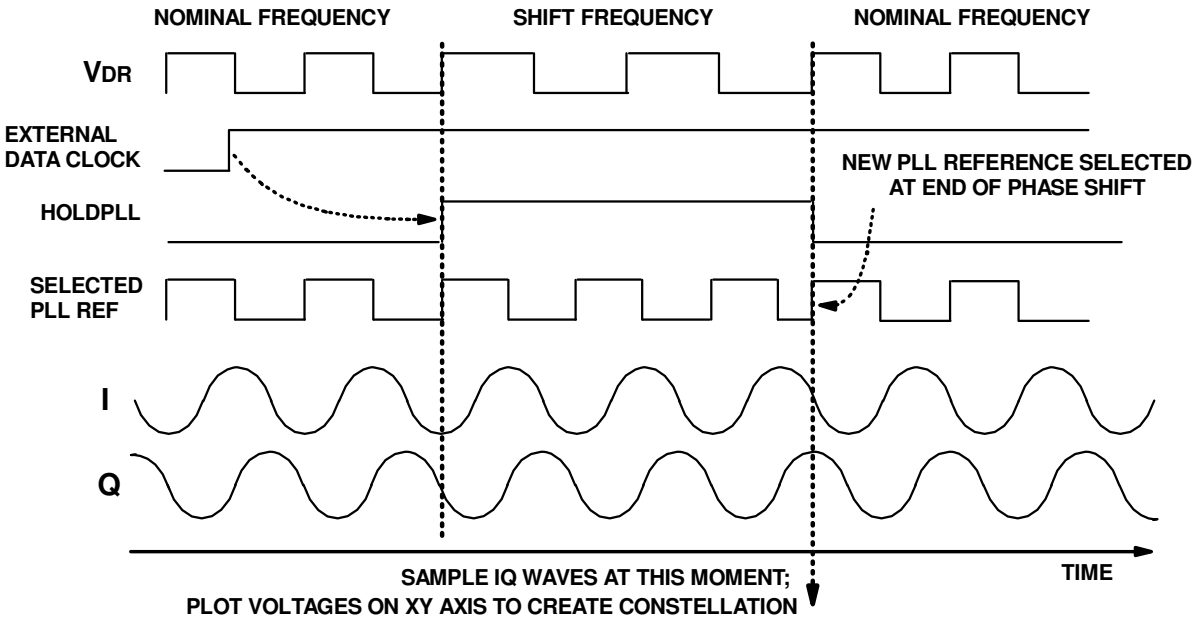

Figure 12-36: Timing diagram for lctune018_psk phase demodulator

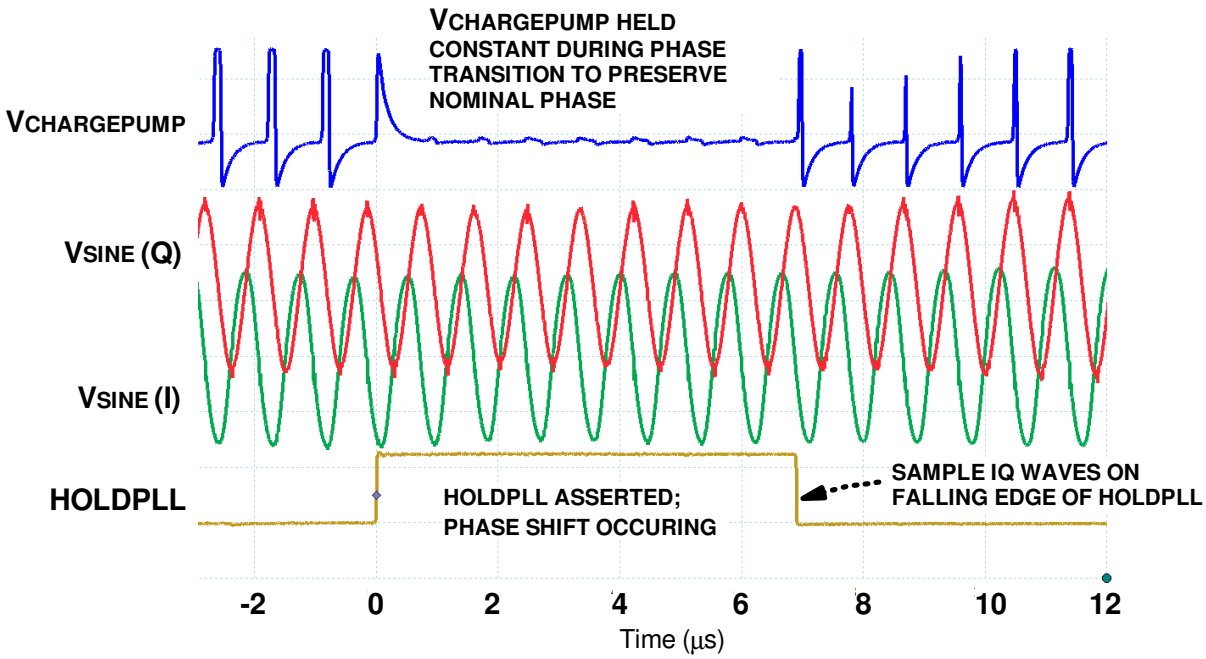

Figure 12-37: Picoscope waveforms captured for IQ sampling

The PLL VCO is implemented as an NPN astable oscillator as per figure 12-38. The RC values were manually adjusted to achieve the nominal frequency of the test IC with a mid-supply input voltage, i.e. approximately 2.5V. A TL081-based voltage buffer was used to isolate the VCO input voltage from the charge pump to prevent drift when *HOLDPLL* is asserted. The VCO supply is isolated from the rest of the circuit to mitigate against drift due to switching noise on the supply. The charge pump was implemented using a tri-state buffer and resistor to permit an increase, decrease or hold in the VCO input voltage.

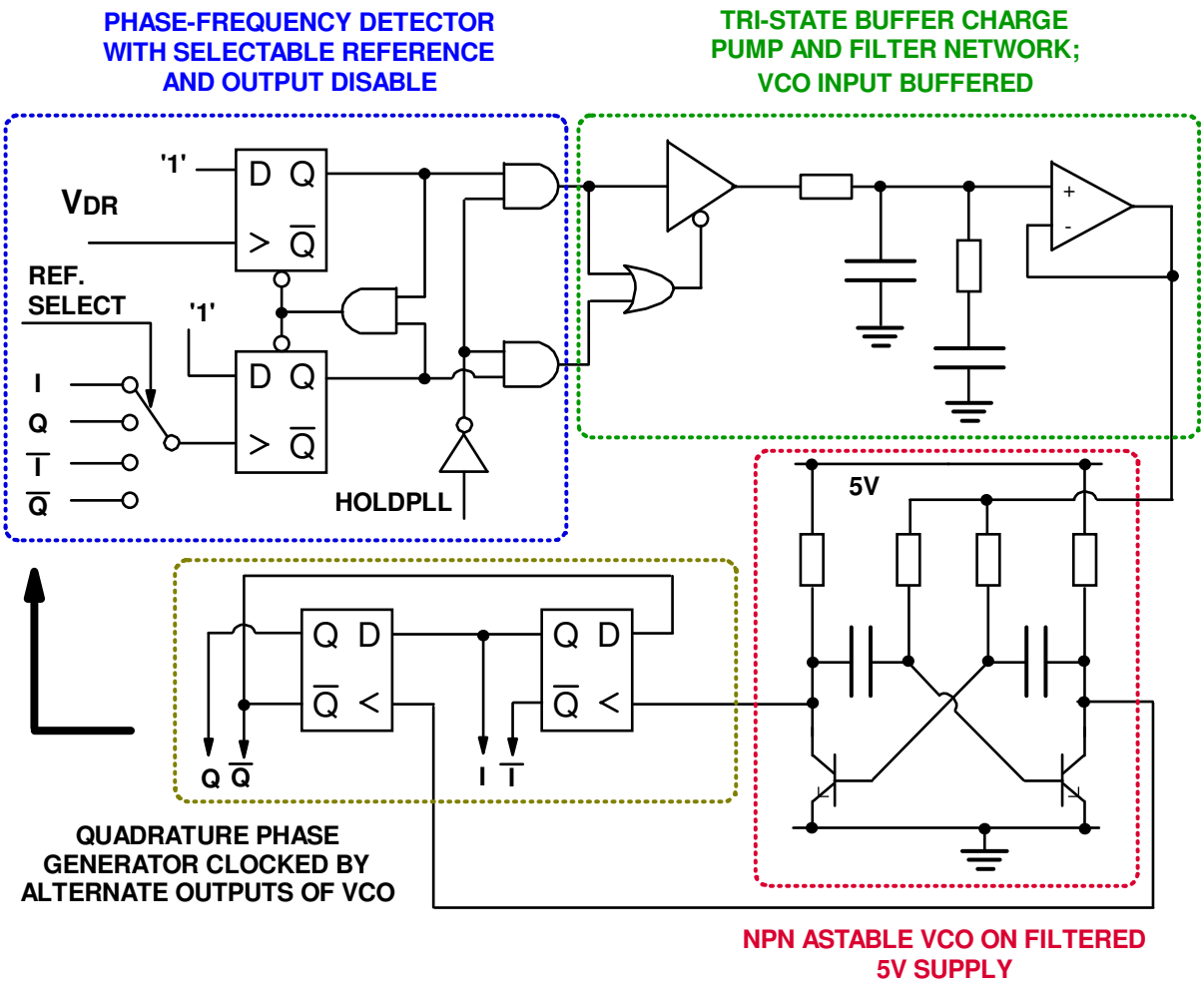

Figure 12-38: PSK demodulator PLL and VCO architecture