READ ME file for DATA set for thesis titled ‘Tunable spin and charge transport using

CMOS-compatible silicon quantum dots for quantum information applications’

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This dataset supports the publication: ‘Tunable spin and charge transport using

CMOS-compatible silicon quantum dots for quantum information applications’ PhD thesis, by Joseph William Hillier

This dataset contains:

Raw data for measurement to plot a figure requiring data is located in the folder “Raw\_data” and the sub-divided into chapters.

\*\*\*\*Chapters 1 and 2 contain no experimental data, since they are the introduction and literature review\*\*\*\*

\*\*\*\*\*Chapter 3\*\*\*\*\*

Figure 3.3

The following data were used;

BD 10um\_0.060um B2-14 high O2 before.csv

For figure 3.3 (a) and (b) file ‘BD 10um\_0.060um B2-14 high O2 before.csv’ was used for a single Vg sweep at VSD = 50 mV ((a)) and over a -50 mV to 50 mV VSD range ((b)). All of the terminals and fixed voltages are labelled in the file.

Figure 3.8

The following data were used;

RT to 190K sample.csv

190K to 11K sample.csv

11K to 2.6K sample.csv

For figure 3.8 (a) the initial cooldown data in RT to 190K sample.csv was plotted, followed by 190K to 11K sample.csv for (b) and 11K to 2.6K sample.csv for (c). For each file, ColumnA is time (nonzero start, offset required) and ColumnB is temperature in K.

Figure 3.11

The following data were used;

Preandpostbondingntests.opj

For figure 3.11 the raw csv file contents is copied to the opj file and plotted within origin.

 \*\*\*\*\*Chapter 4\*\*\*\*\*

Figure 4.2

Data for Figure 4.2 (a)-(c) was collected at 1.6 K by biasing the gate and source terminals whilst measuring drain current and then plotted using Matlab. Figures 2.(d)-(f) are simplified diagrams based on the data shown in Figures 2.(a)-(c) created in PowerPoint. Figures (g)-(i) are energy band diagrams created on PowerPoint.

The following data were used;

1 V well CSD\_-640mV\_-700mV\_Vg\_301\_10^-10A.csv

2 V well CSD\_-690mV\_-750mV\_Vg\_301\_10^-10A.csv

3 V well CSD\_-725mV\_-785mV\_Vg\_301\_10^-10A.csv

(a)

The following data were used;

1 V well CSD\_-640mV\_-700mV\_Vg\_301\_10^-10A.csv

The differential conductance matrix was generated in MATLAB by the change in drain current divided by change in source voltage and plotted against gate voltage at a well voltage of 1 V.

A matrix for gate voltage (-0.640 V to -0.7 V in 0.0002 V increments for 301 1x301 strings), source voltage (column A, row 1-end) for 301 1x301 strings and drain current (column B, row 1-end) for 301 1x301 strings was created using file:

1 V well CSD\_-640mV\_-700mV\_Vg\_301\_10^-10A.csv

The entire data set was plotted in (a).

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.3 V = -0.03 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-10 A, which must be used to convert.

(b)

The following data were used;

2 V well CSD\_-690mV\_-750mV\_Vg\_301\_10^-10A.csv

The differential conductance matrix was generated in MATLAB by the change in drain current divided by change in source voltage and plotted against gate voltage at a well voltage of 2 V.

A matrix for gate voltage (-0.690 V to -0.750 V in 0.0002 V increments for 301 1x301 strings), source voltage (column A, row 1-end) for 301 1x301 strings and drain current (column B, row 1-end) for 301 1x301 strings was created using file:

2 V well CSD\_-690mV\_-750mV\_Vg\_301\_10^-10A.csv

The entire data set was plotted in (b).

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.3 V = -0.03 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-10 A, which must be used to convert.

(c)

The following data were used;

3 V well CSD\_-725mV\_-785mV\_Vg\_301\_10^-10A.csv

The differential conductance matrix was generated in MATLAB by the change in drain current divided by change in source voltage and plotted against gate voltage at a well voltage of 3 V.

A matrix for gate voltage (-0.690 V to -0.750 V in 0.0002 V increments for 301 1x301 strings), source voltage (column A, row 1-end) for 301 1x301 strings and drain current (column B, row 1-end) for 301 1x301 strings was created using file:

2 V well CSD\_-725mV\_-785mV\_Vg\_301\_10^-10A.csv

The entire data set was plotted in (c).

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.3 V = -0.03 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-10 A, which must be used to convert.

(d)-(f)

Simplified charge stability diagrams based on Figures 2.(a)-(c), created in Powerpoint.

(g)-(i)

Energy band diagrams created in PowerPoint.

TABLE 4.1

The charging properties displayed in this table were calculated using Figure 2.(a)-(c) by the Coulomb diamond peaks (for Ec) and estimating the gate voltage width between each Coulomb diamond (for Cg).

Figure 4.3

Figures 4.3 (a)-(b) was collected at 1.6 K by biasing the gate and source terminals whilst measuring drain current, converted into a matrix and then plotted using MATLAB. Figures 3 (c)-(f) are energy band diagrams created in PowerPoint.

The following data were used;

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

(a)

The following data was used;

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

A current matrix for gate voltage (-0.7 V to -0.775 V in 0.0001 V increments for 601 1x751 strings), source voltage (column A, row 1-end) for 751 1x601 strings and drain current (column B, row 1-end) for 751 1x601 strings was created using file:

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

Using the 751x601 matrix, the row corresponding to a source voltage of 12.5 mV for a gate voltage of -0.740 V to -0.700 V was plotted in origin.

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.3 V = -0.03 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

(b)

The following data was used;

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

A current matrix for gate voltage (-0.7 V to -0.775 V in 0.0001 V increments for 601 1x751 strings), source voltage (column A, row 1-end) for 751 1x601 strings and drain current (column B, row 1-end) for 751 1x601 strings was created using file:

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

Using the 751x601 matrix, the column corresponding to a gate voltage of -725 mV for a source voltage of 6 mV to 18 mV was plotted in origin.

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.3 V = -0.03 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

(c)-(f)

Energy band diagrams, created in PowerPoint.

Figure 4.4

The following data were used;

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

The differential conductance matrix was generated in MATLAB by the change in drain current divided by change in source voltage and plotted against gate voltage at a well voltage of 2 V.

A matrix for gate voltage (-0.7 V to -0.775 V in 0.0001 V increments for 601 1x751 strings), source voltage (column A, row 1-end) for 751 1x601 strings and drain current (column B, row 1-end) for 751 1x601 strings was created using file:

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

Only 0 V to 0.02 V source voltage and -0.740 V to -0.705 V gate voltage was plotted .

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.3 V = -0.03 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

Figure 4.5

Figures 4.5 (a)-(b) were collected at 1.6 K by biasing the gate and source terminals whilst measuring drain current and then plotted using MATLAB. Figure 4 (c) and (d) are energy band diagrams created on PowerPoint.

The following data were used;

2 V well\_-2T\_2T\_B-field\_15mV\_Vsd\_-705mV\_-725mV\_Vg\_10^-11A.csv

2 V well -1T\_1T\_B-field\_15mV\_Vs -722 to -732mV\_Vg\_10^-11A.csv

(a)

The following data was used;

2 V well CSD\_-700mV\_-775mV\_Vg\_301\_10^-11A.csv

(a)

The following data was used;

2 V well\_-2T\_2T\_B-field\_15mV\_Vsd\_-705mV\_-725mV\_Vg\_10^-11A.csv

The current matrix was generated in MATLAB by plotting the magnetic field against gate voltage at a well voltage of 2 V and source voltage of 0.015 V.

A matrix for magnetic field (-2 T to 2 T in 0.008 T increments for 201 1x501 strings), gate voltage (column A, row 1-end) for 501 1x201 strings and drain current (column B, row 1-end) for 501 1x201 strings was created using file:

2 V well\_-2T\_2T\_B-field\_15mV\_Vsd\_-705mV\_-725mV\_Vg\_10^-11A.csv

Only -0.715 V to 0.725 V gate voltage against -2T to 2T B-field was plotted in (b).

N.B Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

(b)

The following data was used;

2 V well -1T\_1T\_B-field\_15mV\_Vs -722 to -732mV\_Vg\_10^-11A.csv

The current matrix was generated in MATLAB by plotting the magnetic field against gate voltage at a well voltage of 2 V and source voltage of 0.015 V.

A matrix for magnetic field (-1 T to 1 T in 0.008 T increments for 101 1x251 strings), gate voltage (column A, row 1-end) for 251 1x101 strings and drain current (column B, row 1-end) for 251 1x101 strings was created using file:

2 V well -1T\_1T\_B-field\_15mV\_Vs -722 to -732mV\_Vg\_10^-11A.csv

Only -0.723 V to 0.728 V gate voltage against -1T to 1T magnetic-field was plotted in (c).

N.B Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

(c) and (d)

Energy band diagrams, created in PowerPoint.

Figure 4.6

The following data was used;

D2018-11-30\_017 15mV Vs -724mV VG -1 to 1 T.csv

D2018-11-30\_023 15mV Vs -723mV Vg test.csv

D2018-11-30\_024 15mV Vs -723.5mV Vg test.csv

D2018-11-30\_030 15mV Vs -725mV Vg.csv

The current profiles in Figure 4.6 (a)-(d) were generated in MATLAB by plotting the magnetic field against drain current at a fixed source voltage of 0.015 V and gate voltages varying from of -0.723 V to -0.725 V.

An array for magnetic field in (column A, row 1-end) for 1 1x1001 string and drain current (column B, row 1-end) for 1 1x1001 string was created and plotted.

Figure 4.6

The following data was used;

HR -650-750mV 1000-3000mV CSD SB WS 15 mV Vs [(1) ; 05\_09\_2020 08\_28\_30].csv

MR -650-750mV 1000-3000mV CSD SB WS 15 mV Vs(1) [(1) ; 10\_09\_2020 08\_59\_31] 0.4T.csv

A current matrix was generated in MATLAB and plotted for gate voltage against well voltage at 0 T (a) and 0.4 T (b). The terminals and fixed voltages are labelled in these csv files.

Figure 4.7

The following data was used;

HR -700-775mV CSD SB SS 2000mV well [(1) ; 04\_09\_2020 22\_05\_27].csv

HR -710-740mV CSD SB SS 2000mV well [(1) ; 05\_09\_2020 03\_08\_10].csv

HR -710-740mV CSD SB SS 2000mV well [(1) ; 10\_09\_2020 03\_40\_36] 0.4T.csv

A current matrix was generated in MATLAB and plotted for gate voltage against source voltage at 0 T (a), 0 T (zoomed in (b) and 0.4 T (c). The terminals and fixed voltages are labelled in these csv files.

Figure 4.9

The following data was used;

2 V well profile\_-1T\_1T\_B-field\_-724mV\_Vg\_15mV\_Vsd\_10^-11A.csv

The current profile was generated in MATLAB by plotting the magnetic field against drain current at a well voltage of 2 V, source voltage of 0.015 V and gate voltage of -0.724 V.

An array for magnetic field in (column A, row 1-end) for 1 1x2001 string and drain current (column B, row 1-end) for 1 1x2001 string was created using file:

2 V well profile\_-1T\_1T\_B-field\_-724mV\_Vg\_15mV\_Vsd\_10^-11A.csv

A fitting (red) was then applied to the peaks within the plot using equation (1) in the manuscript to extract a tunnelling coupling (t).

\*\*\*\*\*Chapter 5\*\*\*\*\*

Figure 5.1

(a), (b) and (c) were generated via Inkscape. (d) The graph was plotted for line Vsd = 0.5 mV using file: 'Initial -550-750mV stress CSD PLC1 [(2) ; 28\_10\_2020 00\_33\_15]'.

Figure 5.2

(a) was created using 'pMOS\_stress\_-4.0V\_Vg [(1) ; 17\_03\_2021 19\_15\_32] by plotting Ig, Isub and Ig-Isub.

(b) Illustration was created using Inkscape.

Figure 5.3

The following data were used;

pMOS\_IdVg 600-720mV.initial.xlsx

pMOS\_IdVg 600-720mV.after-4Vg.xlsx

pMOS\_IdVg 600-720mV.after-4.4Vg.xlsx

pMOS\_IdVg 600-720mV.after-4.6Vg.xlsx

(a-d) Current-voltage matrix was generated in MATLAB and plotted using GateV(column C, row 223-end), Drain\_V(column B, row 223-end) and Source\_I(column D/F, row 223-end) for each file.

Figure 5.4

The following data were used;

Initial pMOS\_IdVg -630-790mV CSD.csv

-4 V stress (1) pMOS\_IdVg -630-790mV CSD.csv

After thermal cycle pMOS\_IdVg -630-790mV CSD.csv

-4 V stress (2) pMOS\_IdVg -630-790mV CSD.csv

(a)(i-ii) and (b)(i)-(ii) Current-voltage matrix was generated in MATLAB and plotted using GateV(column C, row 261-end), Drain\_V(column B, row 261-end) and Source\_I(column H, row 261-end) for each file. Figures were then annotated in PowerPoint.

Figure 5.5

(a)(i)-(v) Charge stabilitity diagrams were generated by plotting Vsd and Id using the following data:

Initial -550-750mV stress CSD PLC1 [(2) ; 28\_10\_2020 00\_33\_15]

-4.0 V -550-750mV stress CSD PLC1 [(1) ; 29\_10\_2020 00\_27\_41]

-4.2 V -550-750mV stress CSD PLC1 [(1) ; 29\_10\_2020 15\_43\_34]

-4.4 V -550-750mV stress CSD PLC1 [(3) ; 29\_10\_2020 21\_56\_34]

-4.6 V-550-750mV stress CSD PLC1 [(4) ; 30\_10\_2020 12\_02\_14]

(b)(i)-(v) Charge stabilitity diagrams were generated by plotting Vsd and Id using the following data:

After 1st TC Initial -550-750mV stress CSD PLC1 [(2) ; 12\_12\_2020 14\_09\_14]

After 1st TC -4 V-550-750mV stress CSD PLC1 [(2) ; 12\_12\_2020 14\_09\_14]

After 1st TC -4.2 V-550-750mV stress CSD PLC1 [(1) ; 12\_12\_2020 19\_36\_23]

After 1st TC -4.4 V-550-750mV stress CSD PLC1 [(1) ; 13\_12\_2020 00\_46\_05]

After 1st TC -4.6 V-550-750mV stress CSD PLC1 [(1) ; 13\_12\_2020 06\_05\_46]

(c)(i)-(v) Charge stabilitity diagrams were generated by plotting Vsd and Id using the following data:

After 2nd TC initial-550-750mV stress CSD PLC1 [(1) ; 17\_03\_2021 13\_27\_52]

After 2nd TC -4 V -550-750mV stress CSD PLC1 [(1) ; 17\_03\_2021 21\_43\_08]

After 2nd TC -4.2 V -550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 00\_18\_23]

After 2nd TC -4.4 V -550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 02\_54\_11]

After 2nd TC -4.6 V -550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 05\_29\_02]

Figure 5.6

The following data were used;

pMOS\_IdVg 600-720mV.after-4.6Vg.xlsx

(a) Current-voltage matrix was generated in MATLAB and plotted using GateV(column C, row 80624-end), Drain\_V(column B, row 80624-end) and Source\_I(column F, row 80624-end) using pMOS\_IdVg 600-720mV.after-4.6Vg.xlsx.

(b) Current profile was generated using MATLAB and plotted with |Source\_I| vs GateV -660 mV to -720 mV and DrainV fixed at -12.4 mV using pMOS\_IdVg 600-720mV.after-4.6Vg.xlsx.

Figure 5.7

(a)(i)-(iii) Charge stability diagrams were generated by plotting Vsd and Id using the following data:

After 2nd TC -4.8 V-550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 08\_06\_13]

After 2nd TC -5.0 V-550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 10\_48\_47]

After 2nd TC -5.2 V -550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 14\_45\_59]

(b) Plot generated using 'After 2nd TC -5.2 V -550-750mV stress CSD PLC1 [(1) ; 18\_03\_2021 14\_45\_59]' for Vsd = 5, 10, 15, 20 and 25 mV.

(c) Plot generated using data:

After 2nd TC initial-550-750mV stress CSD PLC1 [(1) ; 17\_03\_2021 13\_27\_52]

pMOS\_stress\_-4.0V\_Vg [(1) ; 17\_03\_2021 19\_15\_32]

pMOS\_stress\_-4.2V\_Vg [(1) ; 17\_03\_2021 21\_50\_50]

pMOS\_stress\_-4.4V\_Vg [(1) ; 18\_03\_2021 00\_26\_38]

pMOS\_stress\_-4.6V\_Vg [(1) ; 18\_03\_2021 03\_02\_20]

pMOS\_stress\_-4.8V\_Vg [(1) ; 18\_03\_2021 05\_38\_05]

pMOS\_stress\_-5.0V\_Vg [(1) ; 18\_03\_2021 08\_16\_50]

pMOS\_stress\_-5.2V\_Vg [(1) ; 18\_03\_2021 12\_16\_09]

pMOS\_stress\_-5.4V\_Vg [(1) ; 18\_03\_2021 14\_53\_34]

pMOS\_stress\_-5.6V\_Vg [(1) ; 18\_03\_2021 17\_32\_14]

Where the difference in the threshold voltage (greater than 1nA) between each Vg,max and the inital data at Vsd= -10 mV was calculated and plotted for each Vg,max value.

(d) Plot generated using:

pMOS\_stress\_-4.0V\_Vg [(1) ; 17\_03\_2021 19\_15\_32]

pMOS\_stress\_-4.2V\_Vg [(1) ; 17\_03\_2021 21\_50\_50]

pMOS\_stress\_-4.4V\_Vg [(1) ; 18\_03\_2021 00\_26\_38]

pMOS\_stress\_-4.6V\_Vg [(1) ; 18\_03\_2021 03\_02\_20]

pMOS\_stress\_-4.8V\_Vg [(1) ; 18\_03\_2021 05\_38\_05]

pMOS\_stress\_-5.0V\_Vg [(1) ; 18\_03\_2021 08\_16\_50]

pMOS\_stress\_-5.2V\_Vg [(1) ; 18\_03\_2021 12\_16\_09]

pMOS\_stress\_-5.4V\_Vg [(1) ; 18\_03\_2021 14\_53\_34]

pMOS\_stress\_-5.6V\_Vg [(1) ; 18\_03\_2021 17\_32\_14]

Where the average integration time per point (0.175 seconds), together with the surface gate area (10\*0.06 um), Ig-Iwell current (electrons) and Iwell (holes) was using in equation (1) in the paper to calculate the total charge fluence for each stress double sweep.

Figure 5.8

(a)(i) Plot generated using:

pMOS\_IdVg HR Arr 10K [(4) ; 20\_12\_2020 15\_01\_26]

pMOS\_IdVg HR Arr 12K [(5) ; 20\_12\_2020 15\_18\_24]

pMOS\_IdVg HR Arr 14K [(6) ; 20\_12\_2020 15\_31\_12]

pMOS\_IdVg HR Arr 16K [(7) ; 20\_12\_2020 15\_44\_18]

pMOS\_IdVg HR Arr 18K [(8) ; 20\_12\_2020 15\_57\_41]

pMOS\_IdVg HR Arr 20K [(9) ; 20\_12\_2020 16\_21\_47]

pMOS\_IdVg HR Arr 25K [(10) ; 20\_12\_2020 16\_35\_48]

pMOS\_IdVg HR Arr 30K [(11) ; 20\_12\_2020 16\_50\_22]

pMOS\_IdVg HR Arr 35K [(12) ; 20\_12\_2020 17\_04\_51]

pMOS\_IdVg HR Arr 40K [(1) ; 20\_12\_2020 17\_20\_49]

For Vsd = -5 mV over the Vg range.

(a)(ii) Plot generated using:

pMOS\_IdVg HR mArr -4V 10K [(1) ; 21\_12\_2020 10\_45\_16]

pMOS\_IdVg HR mArr -4V 12K [(2) ; 21\_12\_2020 10\_50\_52]

pMOS\_IdVg HR mArr -4V 14K [(3) ; 21\_12\_2020 10\_56\_15]

pMOS\_IdVg HR mArr -4V 16K [(4) ; 21\_12\_2020 11\_02\_17]

pMOS\_IdVg HR mArr -4V 18K [(5) ; 21\_12\_2020 11\_07\_59]

pMOS\_IdVg HR mArr -4V 20K [(6) ; 21\_12\_2020 11\_13\_07]

pMOS\_IdVg HR mArr -4V 25K [(7) ; 21\_12\_2020 11\_22\_19]

pMOS\_IdVg HR mArr -4V 30K [(8) ; 21\_12\_2020 11\_28\_38]

pMOS\_IdVg HR mArr -4V 35K [(9) ; 21\_12\_2020 11\_34\_49]

pMOS\_IdVg HR mArr -4V 40K (2) [(11) ; 21\_12\_2020 11\_45\_08]

For Vsd = -5 mV over the Vg range.

(b)(i)-(iii) The above data in (a)(i) was used, where the QD peak Id values corresponding to the labelled quantum dots in Figure 5.(a)(i), together with equation (2) to estimate the activation energy via the gradient in the thermal emission regime at each Vg,max.

(b)(iv)-(vi) The above data in (b)(i) was used, where the QD peak Id values corresponding to the labelled quantum dots in Figure 5.(a)(ii), together with equation (2) to estimate the activation energy via the gradient in the thermal emission regime at each Vg,max.

TABLE I

The QD properties displayed in this table were calculated using Figure 3.(a) by measuring the Coulomb diamond dimensions (for negative Vsd) and estimating the activation energy via the same method as Figure 5. (b)(i)-(vi) using data:

Initial -550-750mV stress CSD PLC1 [(2) ; 28\_10\_2020 00\_33\_15]

-4.0 V -550-750mV stress CSD PLC1 [(1) ; 29\_10\_2020 00\_27\_41]

-4.2 V -550-750mV stress CSD PLC1 [(1) ; 29\_10\_2020 15\_43\_34]

-4.4 V -550-750mV stress CSD PLC1 [(3) ; 29\_10\_2020 21\_56\_34]

-4.6 V-550-750mV stress CSD PLC1 [(4) ; 30\_10\_2020 12\_02\_14]

pMOS\_IdVg HR Arr 10K [(4) ; 20\_12\_2020 15\_01\_26]

pMOS\_IdVg HR Arr 12K [(5) ; 20\_12\_2020 15\_18\_24]

pMOS\_IdVg HR Arr 14K [(6) ; 20\_12\_2020 15\_31\_12]

pMOS\_IdVg HR Arr 16K [(7) ; 20\_12\_2020 15\_44\_18]

pMOS\_IdVg HR Arr 18K [(8) ; 20\_12\_2020 15\_57\_41]

pMOS\_IdVg HR Arr 20K [(9) ; 20\_12\_2020 16\_21\_47]

pMOS\_IdVg HR Arr 25K [(10) ; 20\_12\_2020 16\_35\_48]

pMOS\_IdVg HR Arr 30K [(11) ; 20\_12\_2020 16\_50\_22]

pMOS\_IdVg HR Arr 35K [(12) ; 20\_12\_2020 17\_04\_51]

pMOS\_IdVg HR Arr 40K [(1) ; 20\_12\_2020 17\_20\_49]

pMOS\_IdVg HR mArr -4V 10K [(1) ; 21\_12\_2020 10\_45\_16]

pMOS\_IdVg HR mArr -4V 12K [(2) ; 21\_12\_2020 10\_50\_52]

pMOS\_IdVg HR mArr -4V 14K [(3) ; 21\_12\_2020 10\_56\_15]

pMOS\_IdVg HR mArr -4V 16K [(4) ; 21\_12\_2020 11\_02\_17]

pMOS\_IdVg HR mArr -4V 18K [(5) ; 21\_12\_2020 11\_07\_59]

pMOS\_IdVg HR mArr -4V 20K [(6) ; 21\_12\_2020 11\_13\_07]

pMOS\_IdVg HR mArr -4V 25K [(7) ; 21\_12\_2020 11\_22\_19]

pMOS\_IdVg HR mArr -4V 30K [(8) ; 21\_12\_2020 11\_28\_38]

pMOS\_IdVg HR mArr -4V 35K [(9) ; 21\_12\_2020 11\_34\_49]

pMOS\_IdVg HR mArr -4V 40K (2) [(11) ; 21\_12\_2020 11\_45\_08]

pMOS\_IdVg HR mArr -4.2V 10K [(1) ; 21\_12\_2020 15\_26\_37]

pMOS\_IdVg HR mArr -4.2V 12K [(2) ; 21\_12\_2020 15\_31\_43]

pMOS\_IdVg HR mArr -4.2V 14K [(3) ; 21\_12\_2020 15\_37\_12]

pMOS\_IdVg HR mArr -4.2V 16K [(4) ; 21\_12\_2020 15\_42\_38]

pMOS\_IdVg HR mArr -4.2V 18K [(5) ; 21\_12\_2020 15\_48\_24]

pMOS\_IdVg HR mArr -4.2V 20K [(6) ; 21\_12\_2020 15\_53\_15]

pMOS\_IdVg HR mArr -4.2V 25K [(7) ; 21\_12\_2020 15\_59\_04]

pMOS\_IdVg HR mArr -4.2V 30K [(8) ; 21\_12\_2020 16\_05\_10]

pMOS\_IdVg HR mArr -4.2V 35K (2) [(10) ; 21\_12\_2020 16\_19\_30]

pMOS\_IdVg HR mArr -4.2V 40K [(11) ; 21\_12\_2020 16\_29\_01]

pMOS\_IdVg HR mArr -4.4V 10K [(1) ; 21\_12\_2020 21\_04\_52]

pMOS\_IdVg HR mArr -4.4V 12K [(2) ; 21\_12\_2020 21\_09\_47]

pMOS\_IdVg HR mArr -4.4V 14K [(4) ; 21\_12\_2020 21\_20\_42]

pMOS\_IdVg HR mArr -4.4V 16K [(5) ; 21\_12\_2020 21\_25\_32]

pMOS\_IdVg HR mArr -4.4V 18K [(6) ; 21\_12\_2020 21\_30\_07]

pMOS\_IdVg HR mArr -4.4V 20K [(8) ; 21\_12\_2020 21\_38\_34]

pMOS\_IdVg HR mArr -4.4V 25K [(9) ; 21\_12\_2020 21\_44\_33]

pMOS\_IdVg HR mArr -4.4V 30K [(10) ; 21\_12\_2020 21\_52\_00]

pMOS\_IdVg HR mArr -4.4V 35K [(11) ; 21\_12\_2020 21\_58\_57]

pMOS\_IdVg HR mArr -4.4V 40K [(1) ; 21\_12\_2020 22\_20\_24]

pMOS\_IdVg HR mArr -4.6V 10K [(1) ; 22\_12\_2020 11\_08\_30]

pMOS\_IdVg HR mArr -4.6V 12K [(2) ; 22\_12\_2020 11\_16\_56]

pMOS\_IdVg HR mArr -4.6V 14K [(3) ; 22\_12\_2020 11\_22\_30]

pMOS\_IdVg HR mArr -4.6V 16K [(4) ; 22\_12\_2020 11\_28\_45]

pMOS\_IdVg HR mArr -4.6V 18K [(5) ; 22\_12\_2020 11\_35\_23]

pMOS\_IdVg HR mArr -4.6V 20K [(6) ; 22\_12\_2020 11\_44\_07]

pMOS\_IdVg HR mArr -4.6V 25K [(8) ; 22\_12\_2020 11\_56\_53]

pMOS\_IdVg HR mArr -4.6V 30K [(9) ; 22\_12\_2020 12\_03\_29]

pMOS\_IdVg HR mArr -4.6V 35K [(10) ; 22\_12\_2020 12\_13\_28]

pMOS\_IdVg HR mArr -4.6V 40K [(11) ; 22\_12\_2020 12\_36\_19]

\*\*\*\*Chapter 6\*\*\*\*

Figure 6.15

The following data was used;

W4ChipBX01Y03XX03YY04\_BFG\_TFGfloating\_TG\_0\_5prober

W4ChipBX01Y03XX03YY04\_TFG\_BFGfloating\_TG\_0\_5prober

W4ChipBX01Y03XX03YY04\_TG\_FG1and2\_0\_5prober

The current profiles in Figure 6.15 (a)-(c) were generated in MATLAB by plotting each respective gate sweep against drain current at a fixed source voltage of 0.05 V. All terminals and fixed voltages are labelled in the files.

Figure 6.16

The following data was used;

SET057\_W5A\_X04Y02\_FG1\_rest\_floating\_; 10\_04\_2019 11\_21\_35]

SET057\_W5A\_X04Y02\_FG2\_rest\_floating\_; 10\_04\_2019 11\_22\_55]

SET057\_W5A\_X04Y02\_TG\_rest\_floating\_; 10\_04\_2019 11\_19\_55]

The current profiles in Figure 6.16 (a)-(c) were generated in MATLAB by plotting each respective gate sweep against drain current at a fixed source voltage of 0.05 V. All terminals and fixed voltages are labelled in the files.

Figure 6.22

The following data was used;

D2018-10-16\_086.csv

A current matrix for drain voltage (-20 mV to 20 mV in 0.1 mV increments for 402 1x401 strings), source voltage (column A, row 1-end) for 402 1x401 strings and drain current (column B, row 1-end) for 402 1x401 strings

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.2 V = -0.02 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

Figure 6.23

The following data was used;

D2018-10-17\_116.csv

A current matrix for drain voltage (-20 mV to 20 mV in 0.1 mV increments for 202 1x401 strings), source voltage (column A, row 1-end) for 202 1x401strings and drain current (column B, row 1-end) for 202 1x401 strings

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.2 V = -0.02 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

Figure 6.24

The following data was used;

D2018-10-18\_001

A current matrix for drain voltage (-25 mV to 25 mV in 0.1 mV increments for 502 1x501 strings), source voltage (column A, row 1-end) for 502 1x501strings and drain current (column B, row 1-end) for 502 1x501 strings

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.2 V = -0.02 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.

Figure 6.25

The following data was used;

D2018-10-18\_014.csv

A current matrix for drain voltage (-25 mV to 25 mV in 0.1 mV increments for 1002 1x501 strings), source voltage (column A, row 1-end) for 1002 1x501strings and drain current (column B, row 1-end) for 1002 1x501 strings. Only the TG voltage window from 2 V to 2.3 V was plotted.

N.B source voltage is in Volts and saved a factor of 10 larger than applied, due to a converter used for higher resolution, i.e -0.2 V = -0.02 V. Drain current is saved in Volts with a negative polarity from amplifier output where 1 V = -10^-11 A, which must be used to convert.