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Mechatronics Engineering Group

Model Predictive Control of NPC Inverters for Different Scenarios

by

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ABSTRACT

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Multilevel inverters have undergone a period of rapid development recently and, as a result of the progression of contemporary industry, a range of commercial applications have attained the megawatt standard, thereby meaning that there is a requirement for medium- or high-power conversion mechanisms. At the same time, several energy-generating technologies that can be renewed including solar power, bio-energy, tidal power, wind power, and geothermal power have emerged as critical areas of development in global energy production initiatives, hence creating a situation where the multilevel inverter is becoming increasingly investigated by scholars. It is possible to use multilevel inverters with renewable energy sources and, at the same time, these devices can contribute to high-power rating standards. In light of these considerations, the purpose of the present thesis is to address the control algorithms of multilevel inverters and, to be specific, the thesis will chiefly examine the neutral point clamped (NPC) inverters.

The main challenge regarding the modulation and control of NPC inverters is that the entire system is nonlinear due to the utilisation of power switches. Conventional approaches are mainly based on the average state-space modelling and related modulation techniques such as pulse width modulation (PWM) and sinusoidal pulse width modulation (SPWM). However, the limitations of these conventional methods are clear. The model must be linearised based on a specific operating point. The tuning procedure of the controller is complex, and this complexity increases yet further when the operating point is adjusted. Due to the development of the fast microprocessor and digital signal processors (DSP), some novel control methods such as hysteresis current control, sliding mode control and model predictive control (MPC) have been applied to NPC inverters. Among these methods, MPC stands out for its fast response and handling multiple constraints, and MPC has achieved great success in power electronics applications. Therefore, novel MPC algorithms for 3-level NPC inverters have been proposed to improve energy efficiency for different scenarios in this thesis.

Firstly, an MPC algorithm with reduced switching frequency for 3-level NPC inverters is proposed. The proposed method can reduce the switching frequency through the optimisation of switching sequences while keeping the advantages of the conventional MPC method, such as its fast response and ability to handle multiple constraints. The performance of this proposed method is verified by simulation results with 3-level NPC inverters. Based on this MPC algorithm, two additional extended MPC algorithms are proposed to reduce computational burden, including a multistep model predictive control (MMPC) algorithm and a model predictive control algorithm for grid-connected NPC inverters. The effectiveness of the proposed MPC algorithms has been identified.

Furthermore, an MPC algorithm for NPC grid-connected inverters is proposed with automatic selection of weighting factors. The main objective of this proposed algorithm is to reduce switching frequency and to provide for the automatic selection of weighting factors without the need for trial-and-error across different working conditions. The algorithm can also achieve active power tracking and maintain neutral point balancing. These various objectives are achieved through the use of a modified three-part cost function and the adoption of a two-dimensional fuzzy logic control scheme. The effectiveness of the proposed algorithm is verified using the results of grid-connected NPC inverters simulations, which show that the switching frequency can be reduced by at least 30% when compared to conventional MPC methods.

In addition, a new proposed current slope-related control objective is added to the cost function of the proposed MPC algorithm. This control objective aims to make predicted slope values approach slope reference values. By doing this, the proposed algorithm can reduce the total harmonic distortion (THD) of the output currents and, when compared to a conventional MPC algorithm, can reduce the switching frequency by more than 30%. A case study of a grid-connected NPC inverter system is used to assess the effectiveness of the proposed MPC algorithm under conditions of nominal operation and dynamic operation (with the active power reference, P^*, being stepped down from $31kW$ to $24kW$ at $0.3s$, then increased to $41kW$ at $0.5s$) and with different degrees of parameter sensitivity (at +25%, +50%, and −75% variation in inductance).

Contents

List of Figures

List of Tables

Abbreviations

AC	alternating current
AF	active filter
ANN	artificial neural network
ANPC	active neutral point clamped
APOD-PWM	alternate phase opposition disposition pulse width modulation
BJT	bipolar junction transistor
CHB	cascaded H-bridge
CM	common-mode
CSI	current source inverter
DC	direct current
DPC	direct power control
DSP	digital signal processors
DTC	direct torque control
DVR	dynamic voltage restorer
EMC	electromagnetic compatibility
EMPC	explicit model predictive control
EMI	electromagnetic interference
FACTS	flexible alternating current transmission system
FC	flying capacitor
FCS-MPC	finite control set model predictive control
FOC	field-oriented control
FPGA	field-programmable gate arrays
GPC	generalised predictive control
HDL	hardware description language
HIL	hardware-in-the-loop
HVDC	high-voltage direct current
IGBT	insulated-gate bipolar transistor
IGCT	integrated gate-commutated thyristor
KVL	Kirchhoff's voltage law
LC	inductor-capacitor
Mag	magnitudes
MMC	modular multilevel converter
MMPC	multistep model predictive control
MOSFET	metal-oxide-semiconductor field-effect transistor
MPC	model predictive control
NB	negative big
NM	negative medium
NPC	neutral point clamped
NS	negative small
PB	positive big

PD-PWM	phase disposition pulse width modulation
PF	power factor
PI	proportional-integral
PID	proportional-integral-derivative
PM	positive medium
PMSM	permanent magnet synchronous motor
POD-PWM	phase opposition disposition pulse width modulation
PR	proportional-resonant
PS	positive small
PS-PWM	phase shifted pulse width modulation
PV	photovoltaic
PWM	pulse width modulation
RL	resistor-inductor
RMS	root-mean-square
SDCs	separate direct current source
SHE	selective harmonic eliminated
SM	sub-module
SPWM	sinusoidal pulse width modulation
STATCOM	static synchronous compensator
SVM	space vector modulation
SVPWM	space vector pulse width modulation
THD	total harmonic distortion
UPFC	unified power flow controller
UPS	uninterruptible power supply
VOC	voltage-oriented control
VSI	voltage source inverter
ZO	zero

Declaration of Authorship

I, Mu LI , declare that the thesis entitled *Model Predictive Control of NPC Inverters for Different Scenarios* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as:

1. 'Model Predictive Control of Neutral Point Clamped Inverter with Reduced Switching Frequency,' *2019 10th IEEE International Conference on Power Electronics (2019 ECCE Asia)*, Busan, Korea (South), 2019, pp. 1090-1096.
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3. 'Model Predictive Control of 3-level NPC Inverters based on Current Slope Control Objective.' (drafting)
4. 'Voltage Vector Based Model Predictive Control of 3-level NPC Inverters with Reduced Computational Complexity.' (drafting)
5. 'A Novel Multiple Model Predictive Control Algorithm for Managing Current Variation in 3-Level NPC Inverters in Renewable Power Generation.' (drafting)

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Chapter 1

Introduction

1.1 Research Motivations

Direct current (DC), first generated by Italian physicist Alessandro Volta in 1800, denotes the unidirectional flow of an electrical charge, whereas alternating current (AC), initially produced by French instrument maker Hippolyte Pixii in 1832, denotes as an electric current that periodically reverses direction. Although DC was supported by Thomas Edison (1847-1931) as a more effective way to supply electrical power, AC, backed by Nikola Tesla (1856-1943), ultimately won the 'War of the Currents' and has been adopted for worldwide applications and delivered to every industry and residence since 1892. However, there are many real-world cases where DC is the current used; for example, renewable energy generation, such as photovoltaic methods, produces DC currents that need to be transformed using power inverters into AC forms before transmitting to grids.

A power inverter (also known simply as an inverter or DC-AC inverter) is an electronic device or circuitry that changes DC to AC [1]. DC-AC inverters consist of either 2-level [1] or multilevel forms [2]. 2-Level DC-AC inverters output paired positive and negative level voltages, whereas multilevel inverters output positive, negative, and zero voltages. DC-AC inverters have been extensively employed for large-volume DC power sources [3][4], AC motor drives [5][6], uninterruptible power supplies [7][8], among many other applications.

Multilevel DC-AC inverters consist of cascaded H-bridges, flying capacitors, and neutral point clamped (NPC) inverters. They have been gaining increasing interest worldwide due to the fact that they produce outputs with lower distortion [2][9] compared with 2-level inverters when applied to interfaces for renewable energy generation, such as photovoltaic, bio-energy, wind, tide, wave and geothermal energy production. In addition, an increasing number of high-power applications and renewable resource integrations into grids [2][9] demand the use of multilevel power inverters for connecting a power semiconductor to high-power and medium-voltage supplies [10][11] over 2-level inverters in order to reduce the component stress. Furthermore, multilevel inverters can produce lower switching frequencies [2][10][11] than 2-level inverters when they output the same power level.

NPC based multilevel DC-AC inverters, which are the focus of this thesis, allow for the easier splitting DC-link voltages and have reduced switching losses and smaller output current ripples [12][13]. Accordingly, there are two major research directions associated with NPC inverters: topology and modulation or control. Most newly developed topologies are challenging to implement in industrial environments because they are complex and require extra efforts in re-deigning and manufacturing their associated components. Therefore, updating control algorithms seems to be a more efficient and cost-effective way to improve these NPC inverters; thus, proposing and designing new NPC inverter control methods to improve energy efficiency is therefore the research focus of this PhD thesis.

Previous NPC control methods have been underpinned by linear modulation approaches based on the average state-space modelling and related modulation techniques such as pulse width modulation (PWM) [14] and sinusoidal pulse width modulation (SPWM) [15], leading to a problem in which the model must be linearised based on a specific operating point [16]. Consequently, the tuning procedure regarding the controller is complicated, and this complexity increases when the operating point is adjusted. In addition, employing linear control methods does not capture the fact that NPC systems are nonlinear systems due to the utilisation of power switches. Due to the development of fast microprocessors and digital signal processors, some nonlinear control methods such as hysteresis current control [17], sliding mode control [18], and model predictive control (MPC) [19] have now been applied to NPC inverters.

The primary function of the MPC method is to find an optimal control input for power switches through solving an online optimisation problem and to then implement the resulting optimal control in a receding horizon way [20]. MPC methods, compared to hysteresis current control and sliding mode control approaches, stand out due to their fast response and ability to handle multiple constraints [21]. MPC methods have thus achieved great success in power electronics applications [19][22]. Therefore, the MPC of 3-level NPC inverters to improve energy efficiency will be investigated in this thesis.

Increasing energy efficiency of 3-level NPC inverters means reducing their conduction losses and switching losses [23][24]. Under the same operating condition, conduction losses are related to device materials and layouts, whereas switching losses depend on not only materials and layouts but also switching frequencies [25]. Higher switching frequencies will result in higher switching losses [26][27], as well as generating heat which may have a negative effect on the lifetime of switches [28]. Moreover, high switching frequencies result in unreliability in the control behaviour of more complex systems [29]; therefore, it is desirable to reduce MPC switching frequencies.

However, there has been a limited account of work reported addressing this switching frequency reduction problem associated with 2-level inverters [26][27][30] and multilevel inverters [31][32][33]. For 2-level inverters, one current MPC-based approach for high-power voltage-source inverters used a graph algorithm to select the voltage vectors [30]. This approach, when applied to 2-level voltage-source inverters, was able to reduce the switching frequency when compared to a linear controller approach combined with pulse width modulation. For 2-level inverters, it is easy to find the graph algorithm for eight possible voltage vectors. Conversely, when this method is extended to multilevel inverters, the graph algorithm is different to determine, because no mathematical guideline is provided. Another approach [26] used a model predictive direct power control method to reduce switching frequency. Two different cost functions (one for the steady-state and the other for the transient-state) were introduced for 2-level grid-connected voltage source converters. The two different cost functions could achieve a low switching frequency under steady-state conditions, but provide a fast response if the state becomes transient. However, this method does increase the complexity and computation burden of the system. On the other hand, when this method is applied to 3-level NPC inverters, the DC-link capacitor voltage fluctuation problem is not considered in the proposed voltage controller of this algorithm. A third approach involving a modified two-step MPC algorithm for 2-level grid-connected inverters in photovoltaic systems has also been proposed in [27], which was also able to reduce the switching frequency and enable flexible power regulation. Overall, the above methods for 2-level inverters all increased the complexity and computational burden of the system; however, when they are extended to 3-level NPC inverters, the DC-link capacitor voltage fluctuation problem was not considered. For multilevel inverters, in [31] a quadratic weighted cost function was proposed to reduce the switching frequency, compared to a robust sliding mode controller at the same total harmonic distortion (THD) of the output AC current. Furthermore, [32] and [33] both employed a long prediction horizon to reduce the switching frequency. Although the above methods all reduced the switching frequency, they either increased the computational burden or had no consideration for reducing the computational burden, and despite these existing control strategies for reducing switching frequency, the topic remains an open issue. Therefore, in aiming to solve this problem, novel MPC algorithms to reduce switching frequency with the reduced computational burden and neutral point balance of the DC-link capacitor voltage are proposed in this thesis.

Another research issue associated with MPC methods is to tune weighting factors to facilitate performance optimisation. Weighting factor optimisation is currently a topic of intense research interest because of the lack of rigorous systematic design methodologies [22][34]. As it stands, it is not easy to find suitable weighting factors for desired system behaviour. In fact, most commonly-used methodologies relied on trial-and-error approaches to test the effect of different weighting factors [22]. Guidelines, based on the branch and bound algorithm, have also been proposed in [34], which can reduce the need for simulations by trial-and-error to achieve appropriate weighting factors. However, this approach still depends upon determining the appropriate weighting factors empirically. An automated process for selecting weighting factors, based on the use of genetic algorithms, was then proposed [35]; however, the process was time-consuming because it required the running of a set of simulations for every design objective. An artificial neural network (ANN)- based approach was developed [36], which enabled the automatic selection of weighting factors in the cost function. This approach has been shown to achieve a powerful and fast optimisation of weighting factors selection; however, ANNs, unfortunately, require data from extensive simulations for their initial training. The automatic selection of weighting factors in the cost function therefore remains an ongoing research challenge for the MPC of power electronics converters [36]. Accordingly, a novel MPC algorithm based on the automatic selection of weighting factors in order to reduce switching frequency is proposed in this thesis.

Total harmonic distortion (THD) reduction of the output current is another key research focus. THD is the summation of all harmonic components of current or voltage waveforms compared to their fundamental components [37]. The harmonic currents that are injected into a power system can affect the voltage of the power system and subsequently its applications for customers [38]. With regard to the power system itself, harmonic currents are one of the main sources of disturbances, causing equipment overheat and the performance of electronic equipment to deteriorate [38]. With regard to customer applications, the performance of equipment such as motor drives and electric vehicle power supplies can also be adversely affected by harmonics. Focusing on the THD of the output current, a few MPC methods can be used to address this problem [39] and [40]. In [39], modulated model predictive control which was proposed in [41], was applied to 3-level NPC inverters to produce fixed switching frequencies. The proposed method also employed a space vector modulation (SVM) algorithm to synthesise the waveforms at the converter output, and as a result achieved THD of less than 2%. [40] also proposed a modified MPC algorithm based on a rearranged control set: by adding synthetic virtual voltage vectors to rearrange the finite control set of 3-level NPC inverters, the frequency spectrum of output leg voltage became concentrated, which benefits by decreasing the THD of the output currents. The former method [39] was used to optimise the structure of MPC while the latter method [40] was used to optimise the optimisation process of MPC in order to reduce the THD of the output currents. However, the optimisation of control objectives among existing literatures have not yet been considered, nor has the hypothesis of using current slope as a control objective in the cost function of MPC algorithms. From the existing literature, tracking the reference current had been considered. However, tracking the slope of the reference current has never been considered. For 3-level NPC inverters, the reference AC currents are sinusoidal; thus, tracking the slope of the reference current may improve the overall performance of the

MPC methods. In detail, when the current slope is added into the cost function, the fluctuation of the current may be suppressed, and in that case, lower THD values of output currents and switching frequencies may be obtained. Therefore, a novel control objective involving the current slope will be investigated in the thesis.

1.2 Research Aim and Objectives

This PhD thesis aims to investigate energy efficiency improvement strategies using MPC algorithms for 3-level NPC inverter systems to achieve reduced switching frequency, reduced computational burden, automatic selection of weighting factors, and reduced THD of output currents. To fulfil the research aim, the following objectives are identified:

- To investigate and develop an MPC algorithm for 3-level NPC inverters with a newly designed cost function to reduce switching frequencies and another two extended MPC algorithms, i.e. a novel multistep model predictive control algorithm and an MPC algorithm for 3-level grid-connected NPC inverters, to reduce computational burden (see Chapter 3).

  The first MPC algorithm is expected to have the superior performance of switching frequency reduction, capacitor voltage balance, and multiple constraints. The second algorithm is expected to 1) manage current variation, 2) efficiently reduce the THD of the current output, and 3) decrease the computational burden. In order to reduce the computational burden of prediction, the third MPC algorithm, which is applied for 3-level grid-connected NPC inverters, is expected to reduce current predictions by 27 times compared to conventional MPC algorithms.

- To investigate and develop a novel MPC algorithm for automatic selection of weighting factors for 3-level NPC inverters without the need for trial-and-error methods across different dynamic working conditions (see Chapter 4).

  The proposed algorithm is expected to reduce switching frequencies, and achieve active power tracking and maintain neutral point balancing.

- To investigate and develop a newly control objective considering current slope in the cost function (see Chapter 5).

  Reduced THD of output currents and switching frequencies are expected benefits of this proposed MPC algorithm compared to conventional MPC algorithms.

These three MPC algorithms proposed in objective 1 are simpler and easier to be implemented (no high requirement for digital controllers due to reduced computational burden) than the two methods proposed in objective 2 and 3. The methods mentioned in objective 1 are suitable for projects with limited funding or commercial projects in terms of the low associated hardware costs. The method introduced in objective 2 is suitable for dynamic systems or in particular distributed systems such as renewable energy resource ones as they are unstable. The method put forward in objective 3 will be applied to low currents' THD scenarios such as large ships, medical equipment, semiconductor industries, and airports.

1.3 Research Contributions

This PhD thesis has, therefore, the following research contributions or novelties:

- The development of three MPC algorithms for 3-level NPC inverters with stand-alone and grid-connected loads in terms of a newly designed cost function, multistep model predictive control, and reducing the computational burden. This contribution highlights the need for the investigation into switching frequency reduction, capacitor voltage balancing, current variation management, and computational burden reduction (see Chapter 3).
- The development of a novel MPC algorithm for 3-level grid-connected NPC inverters to facilitate the automatic selection of weighting factors without the need for trial-and-error methods across different dynamic working conditions. This contribution highlights the need to reduce switching frequency, achieve active power tracking, and maintain neutral point balancing of NPC inverters (see Chapter 4).
- The development of a newly control objective with the current slope added into the cost function of the proposed MPC algorithm. This contribution can be used to promote the advancement of reducing THD of the output currents and significantly reduce switching frequency (see Chapter 5).

1.4 Thesis Structure

The thesis has been divided into six chapters based on the objectives identified in section 1.2. The content of this thesis is outlined as follows.

Research flowchart of the thesis is demonstrated in Figure 1.1.

In Chapter 1, the motivation, aim, objectives, contributions and novelties, and the structure of the PhD thesis were detailed.

In Chapter 2, a literature review will be presented in which the fundamentals and basic principles of DC-AC inverters and multilevel inverters, modulation and control strategies, and applications of multilevel inverters are summarised. Among them, a review

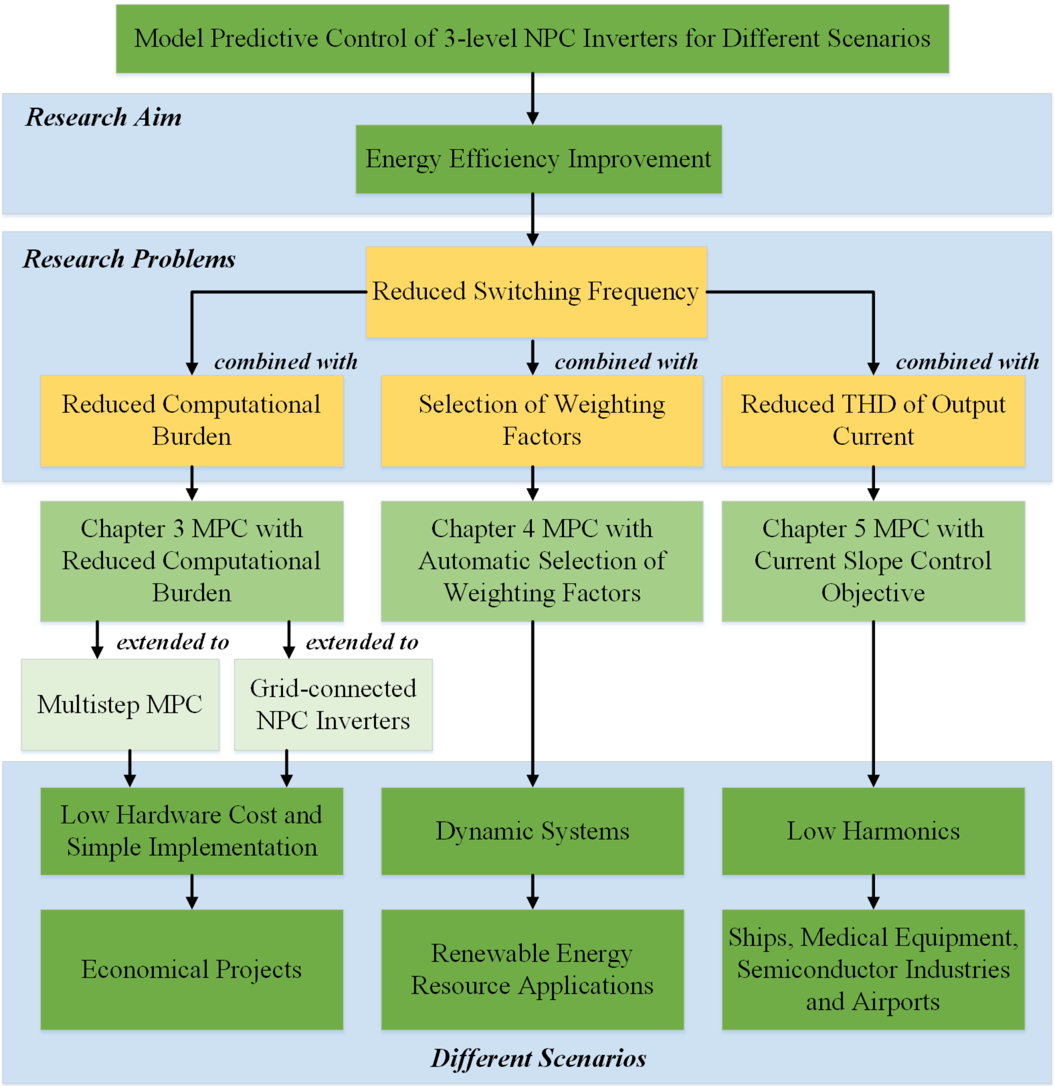


Figure 1.1: Research flowchart of the thesis

of modelling and modulation of 2-level and 3-level grid-connected inverter system will be reported for readers to understand the following content and bridge the knowledge of 3-level NPC inverters. A summary of conventional control methods for inverters is also provided. This will be followed by a comprehensive literature review of the existing work on model predictive control for power converters. From this review, it can be seen that the research into model predictive control has produced significant progress in power electronics; however, problems still exist with regard to reduced switching frequency, design difficulties in weighting factors, reduced computational burden and reduced THD of the output currents. Therefore, the research conducted in this thesis will primarily focus on closing these current research gaps.

In Chapter 3, MPC algorithms with reduced computational burden will be proposed, and this chapter will consist of three key parts. In the first part, an MPC algorithm with a novel design cost function for 3-level NPC inverters with resistor-inductor (RL) load will be put forward. Then, in the second part, the proposed MPC algorithm will be extended to a multistep model predictive control (MMPC) algorithm designed to handle current variation in 3-level NPC inverters with RL load. In the final part, the MPC algorithm of the first part will again be extended to 3-level grid-connected NPC inverters concerning reduced the computational burden of prediction.

In Chapter 4, an MPC algorithm for 3-level grid-connected NPC inverters based on the automatic selection of weighting factors will be proposed. The particular contribution of this algorithm is the use of a two-dimensional fuzzy logic control scheme that eliminates the need for trial-and-error methods which are typical of existing approaches to MPC-based multilevel inverter design. This section will also detail how the proposed algorithm can decrease the switching frequency in comparison to conventional MPC methods. Furthermore, the proposed MPC algorithm will be investigated under dynamic working conditions and parameter sensitivity, and the effectiveness of the proposed algorithm will be verified as well as its potential viability in renewable energy resource applications.

In Chapter 5, a new control objective based on the current slope will be proposed for the MPC algorithm. The current slope as the control objective can allow the slope of the currents to approach the slope of the reference currents, and the fluctuation of the currents can then be better suppressed compared to the conventional MPC algorithms. Case studies of the 3-level grid-connected NPC inverter system, considering nominal operation, dynamic operation and parameter sensitivity will also be analysed to validate the effectiveness of the proposed MPC algorithm.

In Chapter 6, conclusions are presented, and possible future work is identified.

Chapter 2

Literature Review

2.1 Introduction

In this chapter, a comprehensive literature review of the fundamentals and existing work on NPC inverters and model predictive control will be conducted. In addition, a literature review from multilevel inverters, conventional control methods, and modelling and modulation of 2-level and 3-level grid-connected inverter systems are summarised for the reader to understand better the work presented in the following chapters. Accordingly, this review chapter is divided into four parts detailing DC-AC inverters and multilevel inverters in section 2.2, modulation and control strategies in section 2.3, applications of multilevel inverters in section 2.4 and summary for this chapter in section 2.5. A short chronological literature review of this chapter is also presented in Figure 2.1.

2.2 DC-AC Inverters and Multilevel Inverters

2.2.1 DC-AC Inverters

A power inverter (or inverter) can convert a direct current (DC) supply to a single or polyphase alternating current (AC) at the demand of output voltage or frequency [42]. The desired power handling, including the output voltage and frequency and the input voltage, can be obtained using specific circuitries and semiconductor devices, and the desired power output is provided by the DC supply, which does not come from the power inverter. In general, there are two methods of acquiring the desired variable output voltage: One approach is to keep the gain of the inverter constant and change the input (DC voltage); the other approach is to use pulse width modulation (PWM) to achieve a variable output voltage, which changes the gain of the inverter constant.

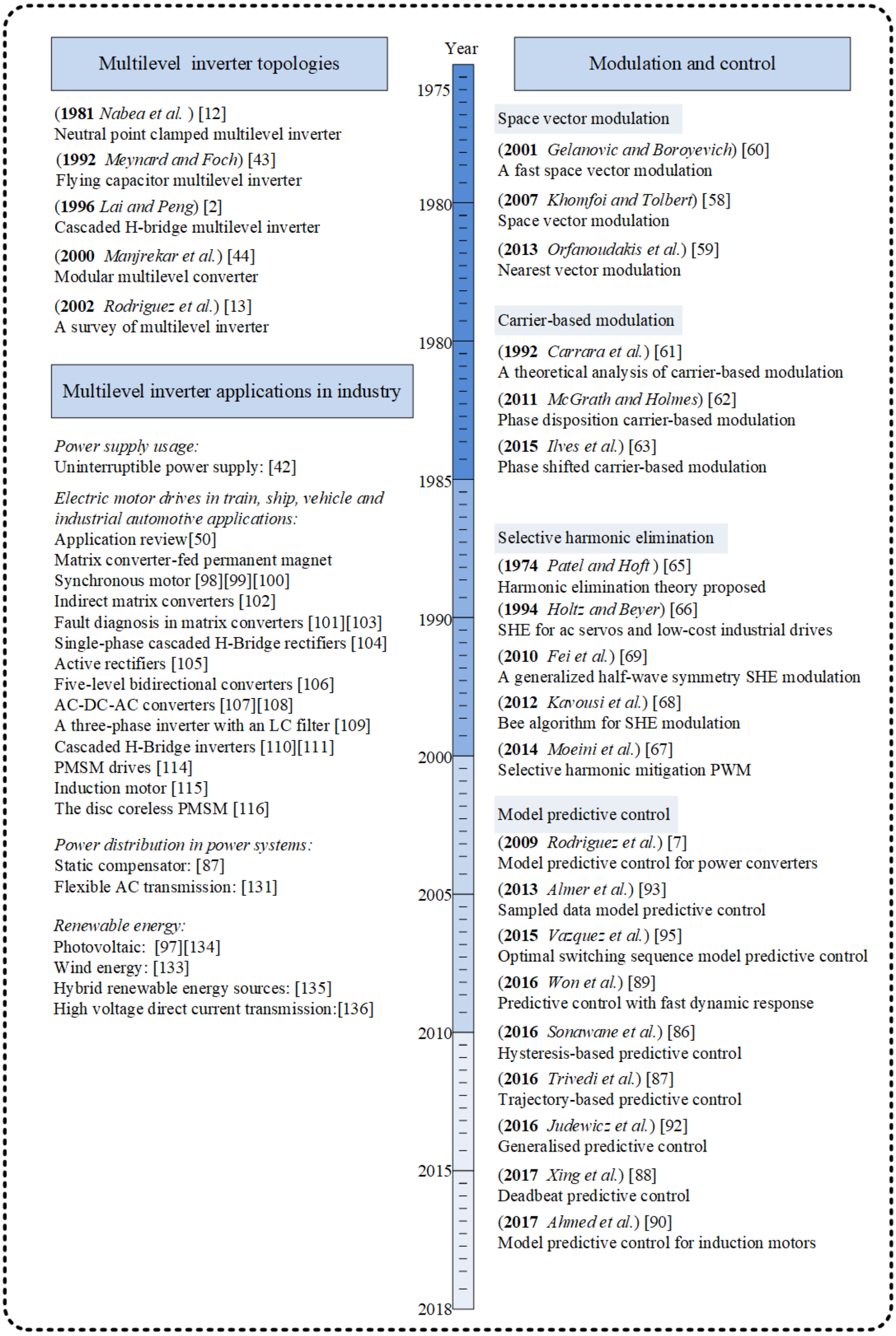


Figure 2.1: A short chronological literature review

Inverters then can be classified into voltage source inverters (VSI) and current source inverters (CSI), according to the operational process used. A voltage source inverter maintains the DC voltage at a constant value, whilst a current source inverter maintains the input current at a constant value. A comparison between voltage source and current source inverters is shown below in Table 2.1.

Table 2.1: Comparison between VSI and CSI

Voltage Source Inverter	**Current Source Inverter**
Input voltage remains constant	Input current remains constant but adjustable
Output voltage depends on the load	Output current does not depend on the load
VSI requires feedback diodes	CSI does not require feedback diodes
The circuit is complex	The circuit is simple since it requires only capacitors

2.2.2 Multilevel Inverters

The concept of multilevel inverters began with 3-level inverters [12]. Subsequently, new multilevel inverters were introduced in 1975. Since then, various topologies for multilevel inverters have been proposed. In general, there are three different topologies: the cascaded full bridge or cascaded H-bridge (CHB) multilevel inverters [2]; the diode clamped or neutral point clamped (NPC) multilevel inverters [12][13]; and the flying capacitor or capacitor clamped (FC) multilevel inverters [12][43]. Figure 2.2 illustrates the simplified and most common configurations of these three multilevel inverter topologies.

In recent years, the modular multilevel converters (MMC) have become a popular choice from the range of inverters available; its structure is presented in Figure 2.3. MMCs are used extensively in commercial applications and are also the focus of a great deal of research [44][45]. Half-bridges are usually made of the cascaded connection of submodules [45]. An arm is connected by SMs in series. Two arms, including upper and lower arms, are comprised of one phase-leg. The inductors L are inserted in this MMC circuit to limit the fault currents and control the circulating currents.

Classification and Advantages of Multilevel Inverters

The classification of multilevel inverter topologies [16] is shown in Figure 2.4. The three topologies that can be categorised as multi-cell topologies are the cascaded H-bridge inverters, the modular multilevel inverters and the flying capacitor inverters; all of these use an array of inverter cells to meet the demand for currents from controllers. These inverters have various advantages such as flexible modularity, low cost redundancy, multiple output voltage levels and low harmonic content. Due to the simple cell structures of the multi-cell inverters, the manufacturing costs are also reduced. As for NPC inverters, they achieved almost instant commercial success, and are widely used in industrial applications [10][11]. NPC inverters keep the same advantages of multi-cell topologies such as low cost redundancy, multiple output voltage levels and low harmonic content.

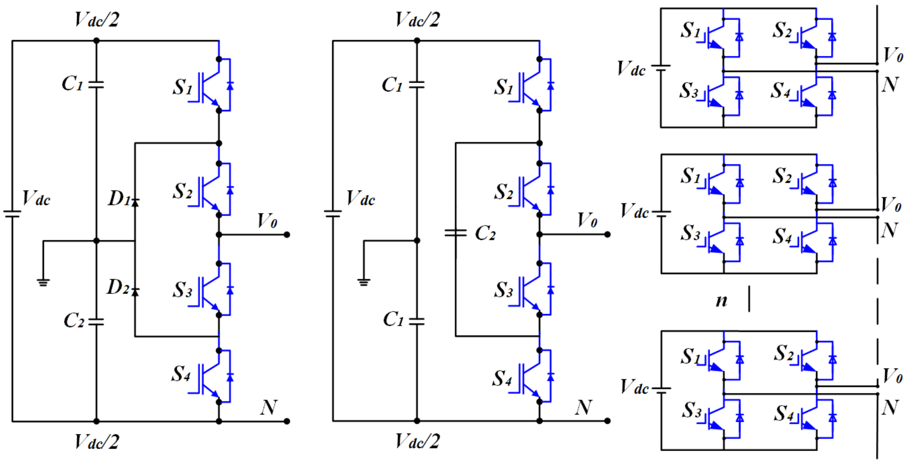


Figure 2.2: Configurations of neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB) multilevel inverters (from left to right), (V_{dc} for DC voltages, C_1 and C_2 for DC-link capacitors, D_1 and D_2 for diodes and S_1-S_4 for switches)[13]

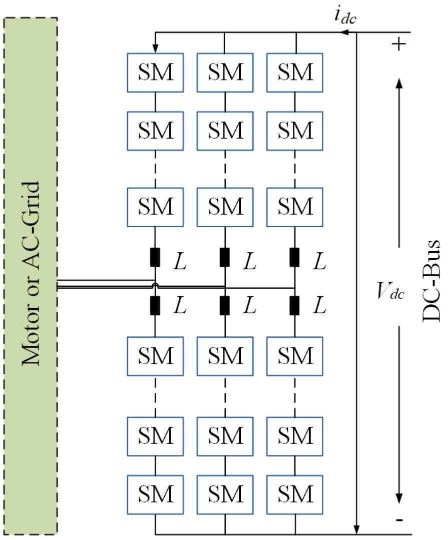


Figure 2.3: Structure of MMCs (SM for sub-modules, V_{dc} for DC voltages and L for inductors)[45]

Compared to the multi-cell topologies, NPC inverters require ordinary transformers for rectifier circuit configurations and have lower power semiconductor counts, especially in the number of capacitors [12].

The demand for medium- and high-power supplies are increasing in modern applications. Multilevel inverters can commonly achieve both medium and high power ratings. Moreover, it has several advantages over conventional 2-level inverters, which are listed below:

- Multilevel inverters can produce output currents with low distortion.

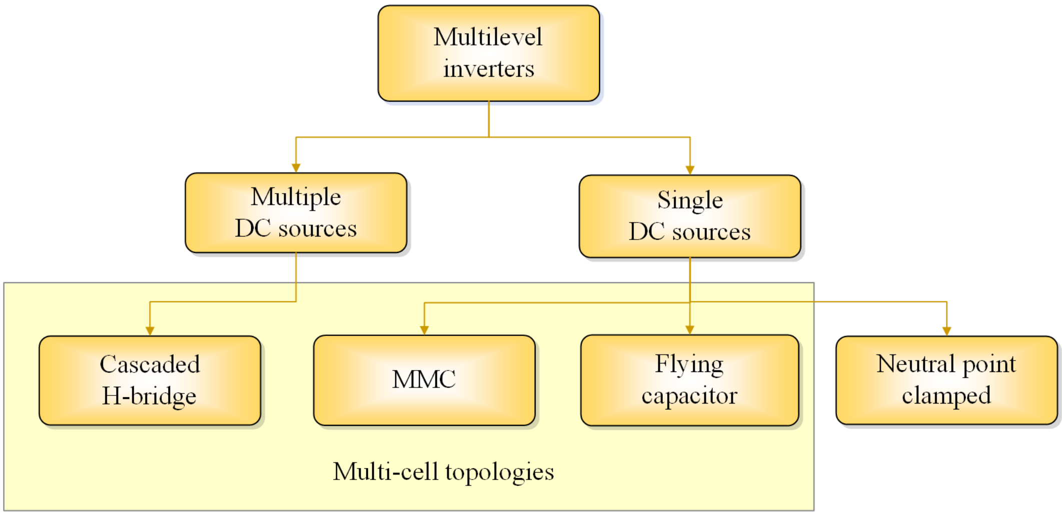


Figure 2.4: Classification of multilevel inverter topologies [16]

- Multilevel inverters are able to not only generate output voltages with low distortion but can also reduce the stress of $\frac{dv}{dt}$, reducing in turn the influence of electromagnetic compatibility (EMC). Further, the needs for filtering are reduced or eliminated.

- Multilevel inverters can produce smaller common-mode (CM) voltages. As a result, the stress in motor bearing can be reduced or even eliminated.

- Multilevel inverters can work at fundamental frequencies or high frequencies; however, it should be noted that lower switching frequencies can generate lower switching losses and achieve higher efficiency. Conventional 2-level inverters and multilevel inverters can both work at fundamental switching frequencies and high switching frequencies; nevertheless, for the same output voltage level, the conventional 2-level inverters require higher switching frequencies than the multilevel inverters since the conventional 2-level inverters have single output voltage level. In contrast, multilevel inverters can generate multiple output voltage levels and therefore require lower switching frequencies for the same output voltage level.

The multilevel inverters do, however, also have its disadvantages: they require numerous power semiconductor switches, such as bipolar junction transistor (BJT), metal-oxide-semiconductor field-effect transistor (MOSFET), and insulated-gate bipolar transistor (IGBT). Although the power semiconductor switches in multilevel inverters can use lower switching frequencies, each power switch needs a corresponding gate driver circuit which may make the whole system more complicated and expensive.

Development of Multilevel Inverters

Progress in the design of the multilevel inverters has been made over two distinct stages, which can be divided into the classic topology used for many years, and more recent developments. In 1981, [12] introduced a modified topology for multilevel inverters, that were able to generate multiple output voltage levels from a single DC source. This modified multilevel inverter topology added extra diodes compared with cascaded H-bridge multilevel inverters, whose diodes were connected to the neutral point. These modified multilevel inverters were termed neutral point clamped (NPC) inverters or diode clamped inverters. The NPC inverters became popular since the 1980s as this kind of topology could effectively double the DC source without requiring precise voltage matching [13]. Although cascaded H-bridge inverters were invented earlier, they did not draw much attention from industry and academia until the late 1980s, whilst the work on CHB [2][13] was more extensively read. In a similar manner, the theory underlying the flying capacitor inverters was first introduced for low-power inverters in 1971 [46], and today's flying capacitor inverters, which can be used at a medium voltage level, was introduced in the 1990s [47].

The topologies of the classic multilevel inverters (cascaded H-bridge, neutral point clamped and flying capacitor) have all been used in industrial applications for the last two decades. Some power electronics manufacturers such as ABB, SIEMENS, Schneider, Eaton and Alstom offer various kinds of multilevel power inverter applications involving different power ratings, power semiconductor switches, configurations, control methods, and cooling systems. The applications of these will be discussed in section 2.4.

In the past few decades, numerous published studies have accelerated the development of multilevel inverters. From an industrial perspective, it is clear that the most extensively used types of multilevel inverters are cascaded H-bridge and 3-level NPC inverters. Consequently, an evaluation of the cascaded H-bridge and NPC multilevel inverters can be made using this published research. Firstly, CHB inverters feature low voltage insulated-gate bipolar transistor (IGBT) power switches, while NPC inverters use medium or high voltage power switches such as IGBTs and integrated gate commutated thyristors (IGCTs). When compared, NPC inverters are more suitable for back-to-back regenerative applications since CHB inverters require a greater number of power semiconductor devices before they have the regenerative capability. CHB inverters, however, can achieve more output voltages in commercial environments, although these two topologies have the same output voltage levels when they use the same numbers of power semiconductor switches. In addition, CHB inverters can achieve higher voltage and power levels; however, when they are used in a thirty-six-pulse rectifier system, a phase-shifting transformer is required in CHB inverters, which is more expensive and increases the volume of applications. Finally, NPC inverters have much simpler circuit configurations than CHB inverters.

Comparison of Multilevel Inverters

A large proportion of the established literatures focus on the relative losses and quality of output voltages within specific devices of the three common multilevel inverter topologies

[48][49]. CHB, NPC, and FC inverters will therefore be discussed separately. For CHB inverters, the modular structures can use low voltage power semiconductors to work at a high level, so that they are suitable for high power applications. The frequency harmonics are also changed by the phase shift in the carrier signals, becoming higher, and combined with a large number of levels, and this allows the average frequencies of device-switching to become lower ($500Hz$). This implies lower losses in the device and enables air-cooling to be carried out. CHB inverters also require a large number of single DC sources, which are fed by single-phase-shifting transformers, and compared with normal transformers that are used in NPC inverters, these are more expensive and have a larger volume [48]. However, this is useful for reducing the harmonics of input currents and improving input power factors of these inverters.

3-Level NPC multilevel inverters achieved almost instant commercial success, and are widely used in industrial applications. They require ordinary transformers for rectifier circuit configurations, and also have lower power semiconductor counts, especially in the number of capacitors. When 3-level NPC inverters are expanded to more levels, they will produce higher loss and also unbalanced distribution of loss [48]. The function of the clamping diodes, which are connected in series, is to block the higher voltage levels; however, when the clamping diodes are under working conditions, they produce conduction loss and reverse recovery currents, which could even influence the switching losses of other power semiconductors [50]. In addition, capacitor voltages of DC-link are required to balance in the higher-level topologies, when conventional modulation strategies are used [51].

Compared with CHB and NPC inverters, FC inverters are not as extensively used in industrial applications. FC topology needs higher switching frequencies to keep voltages of the capacitors balanced, although they do have modular structures like CHB inverters. When they are applied in a control-assisted or self-balancing modulation mode, the switching frequencies will be increased higher [50]. The switching frequencies of high-power applications are usually limited and are therefore not suitable for high power applications.

Many novel multilevel inverter topologies have also been proposed in relevant published literatures in addition to the classical topologies; these are generally referred to as recent advances in multilevel inverters. Most of these topologies are variations of the mixed structure of the classical multilevel inverters; however, very few have been accepted by industry and commerce. Therefore, this PhD thesis will focus solely on the classical multilevel inverters. Reviews of the recent literatures [45][52] suggest that there are two primary trends in multilevel inverters: the applications-oriented multilevel inverters, and the reduced device count multilevel inverters. The three classical multilevel inverters have their intrinsic characteristics; hence, no unique topology can meet the requirements for all of their industrial applications and cost constraints. Therefore, the recommended solution in each instance is determined by the requirements of the application. Depending on the requirements of various projects, academic researchers will then continue to explore the recent advances in multilevel inverter topologies using the classic multilevel inverters as reference points. However, when regarding the meaning of the technical term multilevel inverters, it should be noted that multilevel implies an increase in of the power semiconductor counts, the cost, the volume and the complexity of controllers, although these also increase the output voltage levels. Multilevel inverters can use low voltage rated power semiconductor switches; however, each switch needs a corresponding gate driver, heat abstractor and protective circuit, making the system as a whole more complex, expensive and bulky. As a result, over recent years, many researchers have focused on reducing the power semiconductor switches, which is another modern trend in multilevel inverter topologies. In the following sections, the details of the three multilevel inverters will be provided.

Cascaded H-bridge Multilevel Inverter

The cascaded H-bridge multilevel inverter does not require extra voltage balancing capacitors and clamping diodes but does require separate DC sources (SDCs), unlike neutral point clamped inverters and flying capacitors inverters [53]. Figure 2.5 shows the topology of m-level single-phase cascaded H-bridge multilevel inverters: each SDC is connected with a single-phase H-bridge (full bridge) inverter, and the various AC output voltage terminals are connected in a series. Each of these AC terminals is capable of producing three levels of output, $+V_{dc}$, 0, and -V_{dc}. This is made possible by associating the separate DC sources to the AC output sides through various combinations of the four power semiconductor switches: S_1, S_2, S_3 and S_4.

As can be seen in from Figure 2.5, turning power switches S_1 and S_4 on gives an output of $+V_{dc}$, and turning on S_2 and S_3 gives an output voltage of -V_{dc}. Since each H-bridge inverter is connected in a series, the output AC voltages are the sum of the output voltages of each H-bridge inverter. It can therefore be demonstrated that the number of output phase voltage levels (m) is calculated from $m = 2s + 1$, where s represents the number of SDCs. For instance, an eleven-level cascaded H-bridge multilevel inverter will require five separate DC sources and five H-bridge inverters.

Figure 2.6 demonstrates an example of output phase voltage waveform in eleven-level cascaded H-bridge multilevel inverters. The output phase voltage V_{an} is equal to the sum of V_{a1}, V_{a2}, V_{a3}, V_{a4} and V_{a5}. The general formula for this type of staircase waveform with s steps, as shown in Figure 2.6, is derived in references [10][54]. The Fourier Series for the waveform is given below:

$$V(\omega t) = \frac{4V_{dc}}{\pi} \sum_{n} [cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(n\theta_s)] \frac{sin(n\omega t)}{n} \tag{2.1}$$

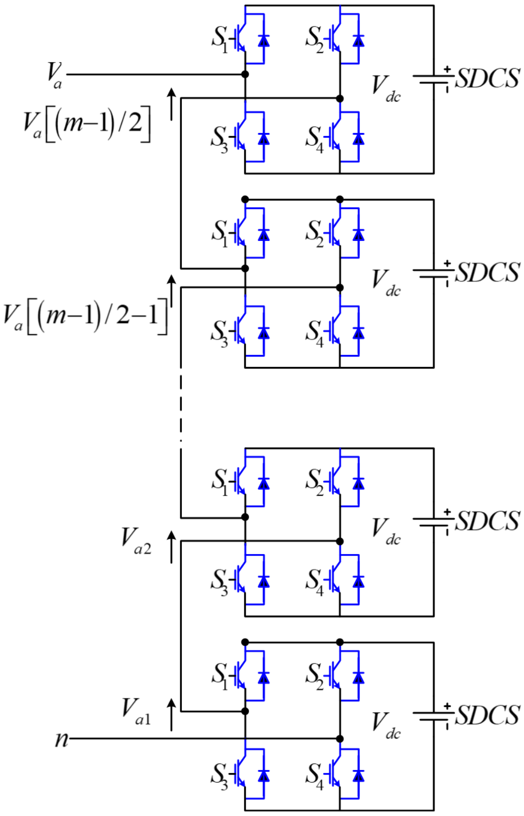


Figure 2.5: Single-phase cascaded H-bridge multilevel inverters (SDCs for separate DC sources) [10]

where n=1,2,3. . .

When it is normalised with respect to V_{dc}, the magnitudes of the Fourier coefficients are as follows:

$$H(n) = \frac{4}{\pi n}[cos(n\theta_1) + cos(n\theta_2) + \cdots + cos(n\theta_s)] \tag{2.2}$$

where n=1,2,3. . .

From Equation 2.2, it can be seen that the total voltage harmonic distortion can be minimised by selecting the conducting angles (θ_1,θ_2,. . . ,θ_s). In [10], the output voltages of the cascaded H-bridge multilevel inverters exclude the 5^{th}, 7^{th}, 9^{th}, 11^{th} and 13^{th} predominant harmonics by using selective conducting angles. Section 2.3.1 will provide a review of selective harmonic elimination methods.

Cascaded H-bridge multilevel inverters are used in many commercial applications such as renewable energy interfaces, static var generation and battery-based applications. In a three-phase system, output voltage levels can be connected in either wye- or star-configurations [55].

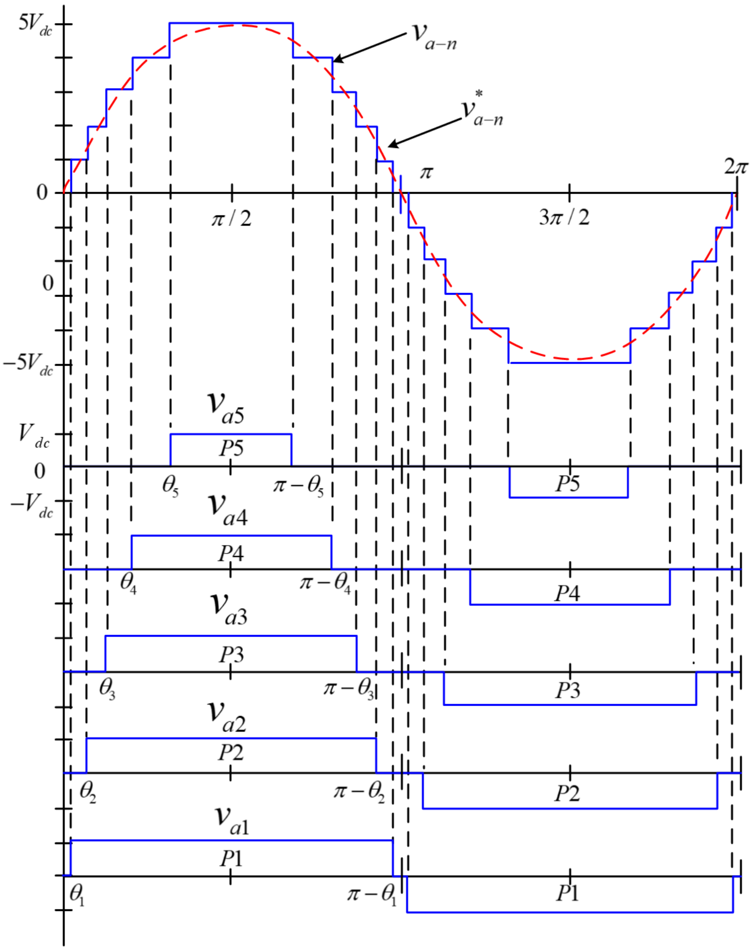


Figure 2.6: Output waveform of eleven-level CHB inverters [10]

A configuration diagram of three-phase Y-connection cascaded H-bridge multilevel inverters for battery charging applications and electric vehicle motor drives [10] is shown in Figure 2.7. Multilevel cascaded static var generators, connected in parallel, can generate and absorb reactive currents in an electrical system [55][56]. When cascaded H-bridge multilevel inverters are connected in series for static var compensation in an electrical system, the function of CHB inverters is to regulate the power factor of the currents from the bus voltage or the source. In real power conversion applications, cascaded H-bridge multilevel inverters are the optimum choice for connecting the various renewable energy sources and the AC grids since they require SDCs, such as photovoltaic panels and fuel cells. In addition, CHB inverters have also been proposed for motor drives in electric vehicles, in which ultra-capacitors and batteries serve as the separate DC sources [10][57]. CHB inverters have come to prominence in both academia and industry, due to the current levels of research interest in electric vehicles. When an electric vehicle is charging from AC supply, cascaded H-bridge multilevel inverters can serve as both charger and rectifier for batteries in Figure 2.7. During regenerative braking of an electric vehicle, a rectifier is required, and CHB inverters can fulfil this need.

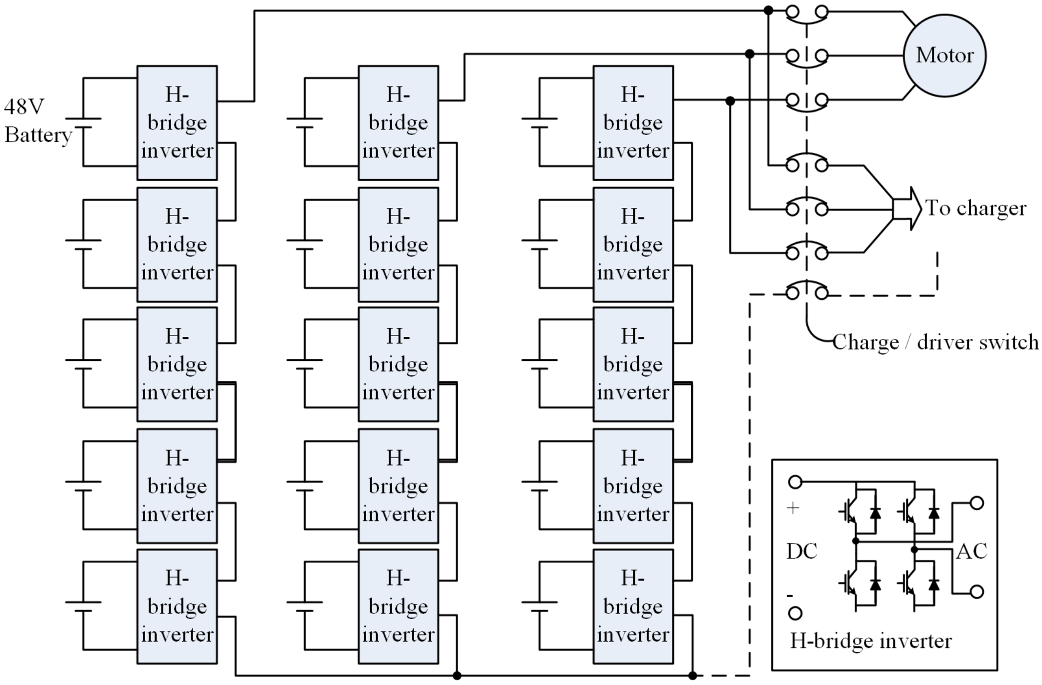


Figure 2.7: Y-connection in cascaded H-bridge multilevel inverters [10]

Cascaded H-bridge multilevel inverters have particular advantages among these multilevel inverters [2][10][11]. Namely, the same configuration of each H-bridge inverter is easy to produce in modular form for assembly, which tends to increase the speed and reduce the cost of production. Moreover, no additional voltage balancing capacitors or clamping diodes are required; however, the requirement for SDCs tends to restrict the practical applications of CHB inverters.

Neutral Point Clamped Inverters

Diode clamped multilevel inverters are also known as the neutral point clamped inverters. M-level neutral point clamped multilevel inverters, which consist of $(m-1)$ capacitors in DC-link, have an m-level output phase voltages and $(2m-1)$ levels of output line voltages. A configuration of a three-phase six-level neutral point clamped multilevel inverters is shown in Figure 2.8. In this figure, a common DC source, which is shared by each of the three phases in the NPC inverters, has been divided into six levels by the five capacitors, C_1 to C_5. The voltage stress in each power switch is limited to V_{dc} through the clamping diodes, and the voltage across each capacitor is V_{dc}.

Table 2.2 details the output voltage levels and their corresponding power switch states. The DC-rail voltage V_0 acts as a reference, and a switch state of 1 means that the switch is on and a switch state of 0 means that the switch is off.

Furthermore, there are five complementary switch pairs in each phase. In phase leg a, the five complementary switch pairs are $(S_{a1}, S_{a'1})$, $(S_{a2}, S_{a'2})$, $(S_{a3}, S_{a'3})$, $(S_{a4}, S_{a'4})$, and $(S_{a5}, S_{a'5})$. When one of these switches is turned on, its complement switches are

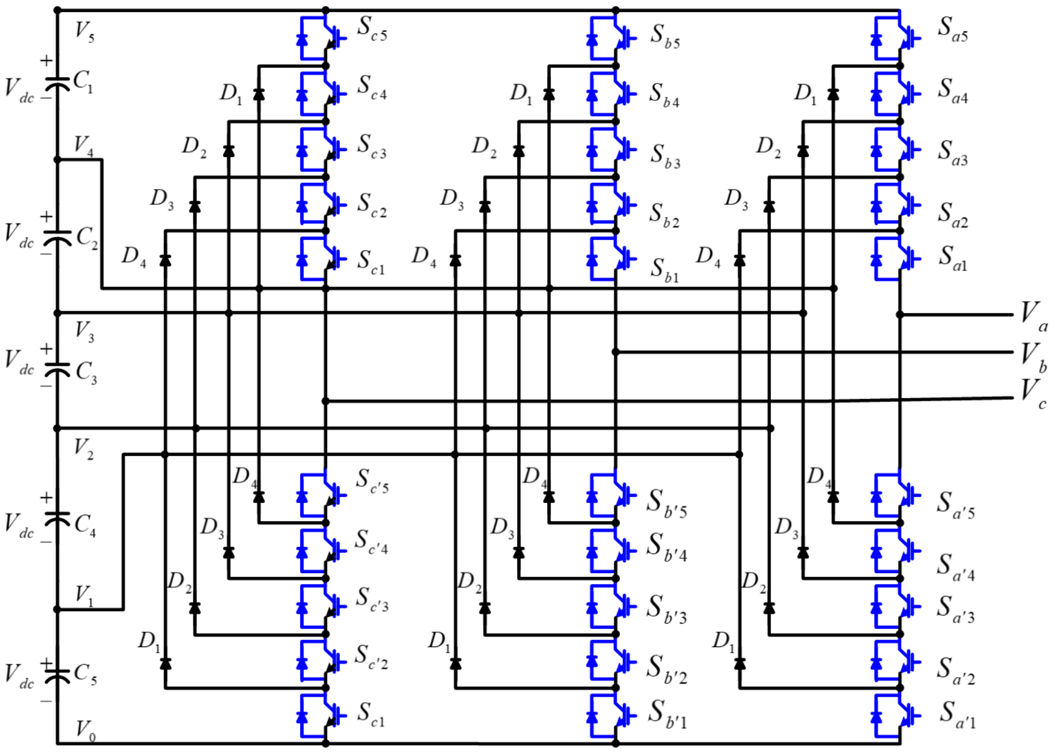


Figure 2.8: Three-phase six-level NPC inverters [10]

Table 2.2: Voltage Levels and corresponding Switch States of Six-level NPC Inverters

Voltage V_{a0}	**Switch State**									
	S_{a5}	S_{a4}	S_{a3}	S_{a2}	S_{a1}	$S_{a'5}$	$S_{a'4}$	$S_{a'3}$	$S_{a'2}$	$S_{a'1}$
$V_5 = 5V_{dc}$	1	1	1	1	1	0	0	0	0	0
$V_4 = 4V_{dc}$	0	1	1	1	1	1	0	0	0	0
$V_3 = 3V_{dc}$	0	0	1	1	1	1	1	0	0	0
$V_2 = 2V_{dc}$	0	0	0	1	1	1	1	1	0	0
$V_1 = V_{dc}$	0	0	0	0	1	1	1	1	1	0
$V_0 = 0$	0	0	0	0	0	1	1	1	1	1

turned off. In this six-level NPC inverters, a suite of five switches is turned on at any given time. Figure 2.9 exhibits one of the three line-to-line voltage waveforms of the example six-level inverters. In the NPC multilevel inverters, each active switch is only needed to block a voltage level of V_{dc}, although the clamping diodes require different ratings for reverse voltage blocking. For example, when all the lower switches from S_{a1} to S_{a5} are turned on, the diode D_4 blocks $4V_{dc}$ (four voltage levels), likewise D_3 blocks $3V_{dc}$, D_2 blocks $2V_{dc}$, and D_1 blocks $1V_{dc}$. If the NPC inverters are designed so that each blocking diode has the same voltage rating as the active power switches, then D_n will need n blocking diodes in a series. Therefore, the number of diodes required for each phase would be $(m-1) \times (m-2)$. Accordingly, the design of NPC inverters is limited by a high (m), i.e. a high number of levels, since its implementation becomes more difficult with a higher number of diodes.

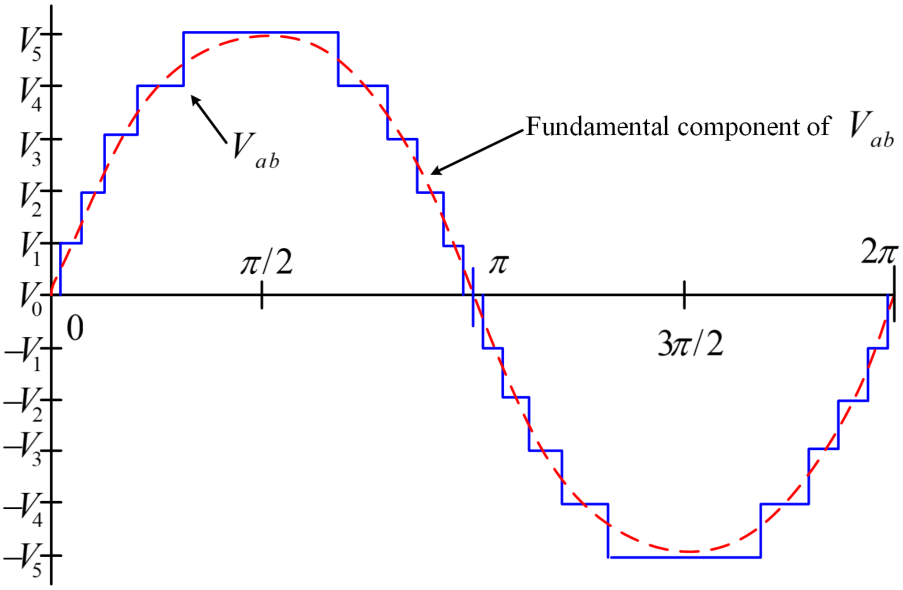


Figure 2.9: Line voltage waveform of six-level NPC inverters [10]

There are three primary applications using NPC multilevel inverters: they can be used to interface between an AC transmission line and an high-voltage direct current (HVDC) transmission line; as a variable speed drive connection for high power 2.4kV to 13.8kV medium-voltage motors; and as static var compensation [58].

Overall, all the phases of NPC multilevel inverters share a common DC bus, which minimises the capacitance requirements. Its efficiency, however, is highly dependent on the design of controllers since all the power semiconductor devices can operate at the fundamental frequency. In addition, the capacitors in a series can be pre-charged simultaneously. However, when the levels of NPC inverters are high, the number of clamping diodes needed increases quadratically with respect to the number of levels. Furthermore, power flow is difficult to control for a single inverter in real-life applications, since the intermediate DC levels will discharge or overcharge without precise control and monitoring.

Flying Capacitor Multilevel Inverters

The configuration of flying capacitor multilevel inverters is similar to NPC multilevel inverters. FC multilevel inverters, however, use capacitors in place of clamping diodes of NPC inverters, whilst the structure of each phase leg in FC multilevel inverters are fairly similar. A configuration of three-phase six-level flying capacitor multilevel inverters is shown in Figure 2.10. All the phase legs in Figure 2.10 share several serial DC-link capacitors from C_1 to C_5.

In terms of FC multilevel inverter topologies, the DC-link side capacitors have a staircase structure in which the voltage of each capacitor is different from the voltage of the next one. The rise or fall of the output voltage is therefore controlled by differences

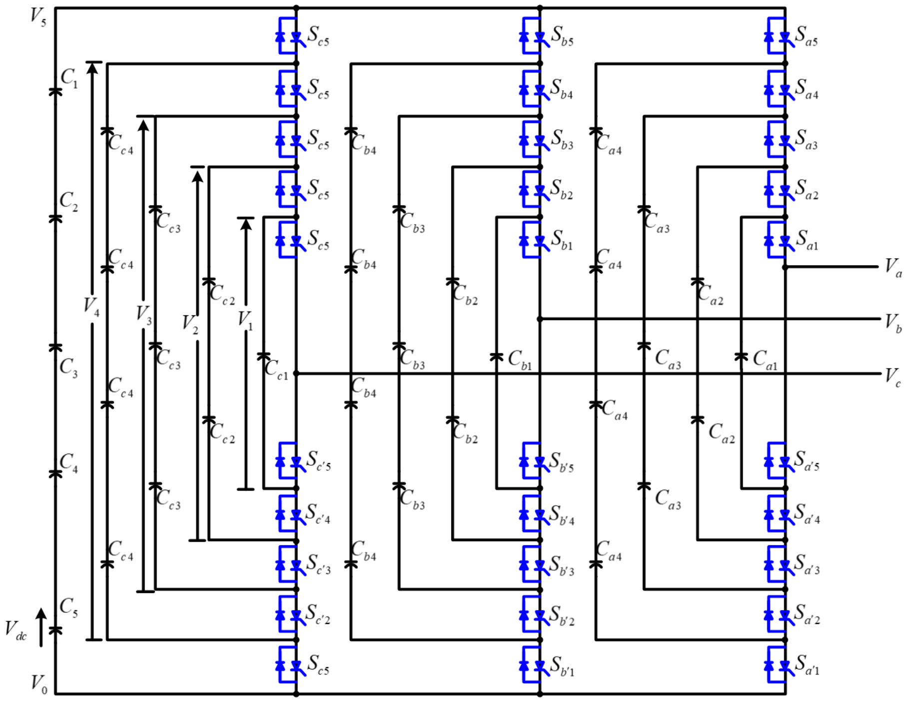


Figure 2.10: A configuration of three-phase six-level flying capacitor multilevel inverters [58]

between adjacent capacitor legs. The output voltage levels of FC multilevel inverters are the same as NPC inverters. M-level FC multilevel inverters will require m-level phase voltages, $(2m-1)$ line voltages, $[(m-1)\times(m-2)]/2$ auxiliary capacitors per phase leg and $(m-1)$ main DC capacitors. The synthesis of the FC output voltage is more flexible than NPC multilevel inverters. In contrast to NPC inverters, flying capacitor multilevel inverters, therefore, do not require the switches to be turned on sequentially. FC multilevel inverters not only have redundancies for inner voltage levels but also have phase redundancies, unlike NPC inverters [2][10][58].

In FC multilevel inverters, both reactive and active power flow can be controlled, and the large numbers of storage capacitors enable FC multilevel inverters to ride through during deep voltage stages and voltage outage. In addition, the redundancies in switch combinations are able to balance various levels. However, there are also some disadvantages to FC multilevel inverters: the production of FC inverters is complex and costly due to a high number of storage capacitors required. Moreover, the control methods of FC inverters are complex due to the need to track all capacitors voltage levels of the capacitors and initialisation and pre-charging of the capacitors to the same voltage are also difficult to carry out. Switching losses and switching frequencies are also high for real power transmission applications [58].

2.3 Modulation and Control Strategies

2.3.1 Modulation Strategies

Pulse width modulations (PWM) for multilevel inverters are usually an extension of a conventional inverter modulation. However, modulation strategies of multilevel inverters can be sophisticated in comparison with the modulation strategies of 2-level inverters, since the multilevel inverters have a high number of power electronic devices and switching states. Due to the structure of multilevel inverters, the modulation strategies need to reduce switching frequencies, balance DC-link voltages, and minimise common-mode voltages. PWN strategies are generally divided into two types, based on their switching frequencies, and these are known as fundamental switching frequency and high switching frequency PWN strategies. In established literatures, multilevel space vector PWM, multilevel carrier-based PWM and selective harmonic elimination strategies have received the most attention from academic researchers. These three modulation strategies form the overwhelming majority of those used in practical applications; therefore, this section 2.3.1 will focus on these three modulation strategies.

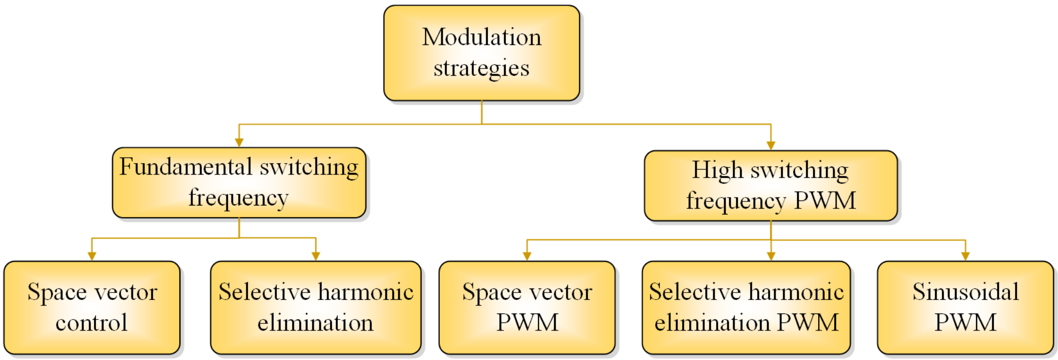


Figure 2.11: Classification of PWM strategies [58]

Space Vector PWM Strategy

Switching control signals for three-phase inverters are created using space vector PWM (SVPWM) method. In comparison with the more typical sinusoidal PWM inverter, the SVPWM inverter provides a 15% improvement in the utilisation of the DC-link voltage and decreases the harmonic distortion of the signals [58]. The SVPWM inverters use a voltage or frequency control system that was developed from space vector modulation methods. The space vector PWM strategy is applicable to all types of 3-level inverters, including the cascaded H-bridge, neutral point clamped [59], and flying capacitor inverters. The technique of space vector modulation employs a geometrical and mathematical process to determine the sequence of switching states for the VSI gate drivers, and the associated duty cycles over a set period, thus creating the control signals [60]. The process can also be further developed for use with multiphase converters.

The benefits of space vector PWM methods include improved utilisation of DC-link voltage, reduced current ripple, and, due to the use of a digital signal processor (DSP), comparatively simple hardware implementation. Space vector methods are therefore appropriate choices for high-voltage, high-power systems. The number of redundant switching states and the difficulty in choosing switching states for multilevel inverters is much higher than for inverters with fewer levels. In order to simplify calculations, some researchers have broken down five-level space vector diagrams into a combination of two 3-level diagrams, and a phase shift was introduced in order to minimise ripples. Other researchers have also used a simplified space vector selection method that does not take into account the duty cycle of the neighbouring three vectors [13].

Carrier-Based PWM Strategy

Sinusoidal PWM (SPWM) is one of the most prominent modulation methods employed in industrial applications given its widespread advantages, such as its simple structure and easy implementation [61]. This method compares a sinusoidal reference waveform naming modulating waveform with a triangular carrier waveform for the production of gate signals alluding to switches for multilevel inverters. The achievement of the modulation goal is considered to be less demanding relative to alternative modulation methods, and the fundamental frequency SPWM is also able to implement the minimisation of power dissipation, especially for the switching losses. Furthermore, the multi-carrier sinusoidal PWM exhibits superior performance compared to the fundamental frequency sinusoidal PWM. Literatures report describe various multi-carrier SPWM modulation methods, including phase disposition (PD-PWM) [62], phase opposition disposition (POD-PWM), alternate phase opposition disposition (APOD-PWM), and phase shifted (PS-PWM) [63]. Figure 2.12 illustrates the PD-PWM, POD-PWM, APOD-PWM, and PS-PWM strategies, respectively. Typically, the PD-PWM strategy is effectively applied to NPC inverters [62], while PS-PWM strategy is only employed by cascaded H-bridge and flying capacitors multilevel inverters [64].

Selective Harmonic Elimination Strategy

The selective harmonic elimination method is also known as the fundamental switching frequency method and is based on the harmonic elimination theory proposed by Patel [65]. A typical 11-level multilevel converter output with a fundamental frequency switching scheme is shown in Figure 2.6. The conducting angles θ_1, θ_2, ..., θ_s, can be chosen to minimise THD in the voltage, and the lower-frequency harmonics are generally required to be cancelled by the careful selection of these angles [13].

For the 11-level case, the 5_{th}, 7_{th}, 11_{th}, and 13_{th} harmonics can be eliminated with the appropriate choice of conducting angles. V_L* can be defined as representing the amplitude command of the inverter for a sine wave output phase voltage, and V_{Lmax} (V_{Lmax} = sV_{dc}) represents the maximum amplitude of the inverter. Therefore, the magnitude of modulation index m_a, which is the fundamental waveform corresponding

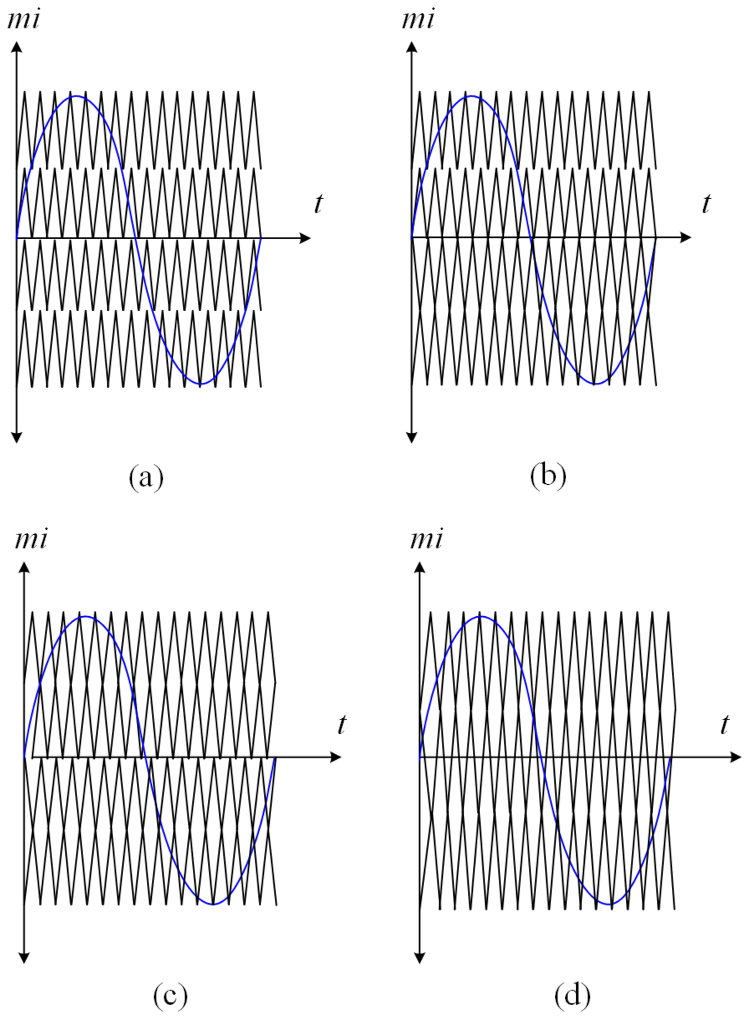


Figure 2.12: Multi-carrier SPWM: (a) PD, (b) POD, (c) APOD, (d) PS [64]

to the amplitude of the reference waveform, is $V_L* \ / \ V_{Lmax}$. Equation 2.2 can thus be written as follows:

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \tag{2.3}$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \tag{2.4}$$

$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \tag{2.5}$$

$$\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0 \tag{2.6}$$

$$\cos(\theta_1) + \cos(\theta_2) + \cos(\theta_3) + \cos(\theta_4) + \cos(\theta_5) = 5m_a \tag{2.7}$$

Equation 2.7 can be solved by the Newton-Raphson method since they are nonlinear transcendental equations. When the modulation index is m_a=0.8, it can be shown that θ_1=6.57, θ_2=18.94, θ_3=27.18, θ_4=45.14, and θ_5=62.24. Consequently, when the output of the inverter is symmetrically switched during the positive half-cycle of the fundamental voltage, this gives $+V_{dc}$ at 6.57°, $+2V_{dc}$ at 18.94°, $+3V_{dc}$ at 27.18°, $+4V_{dc}$ at 45.14°, and $+5V_{dc}$ at 62.24°. Similarly, in the negative half-cycle the inverter output is symmetrically switched to $-V_{dc}$ at 186.57°, $-2V_{dc}$ at 198.94°, $-3V_{dc}$ at 207.18°, $-4V_{dc}$ at 225.14° and $-5V_{dc}$ at 242.24°. This selection of conducting angles therefore cancels the 5th, 7th, 11th, and 13th harmonics [13][58]. In fact, a microcontroller can store pre-calculated switching angles to produce the PWM signals.

This method for selective harmonic modulation within the fundamental switching frequency control strategy is governed by the Fourier decomposition of the PWM waveform and the formulation of the waveform and its properties [66]. Three types of formulation for waveforms have since been put forward in published literatures, and these are known as the bipolar, unipolar, and stepped multilevel waveforms.

The output waveform is dependent on the switching pattern (bipolar, unipolar, or stepped multilevel PWM), Figure 2.13 demonstrating the output waveform using unipolar switching. Overall, one DC voltage is involved in the event of the unipolar programmed PWM modulating multilevel inverters.

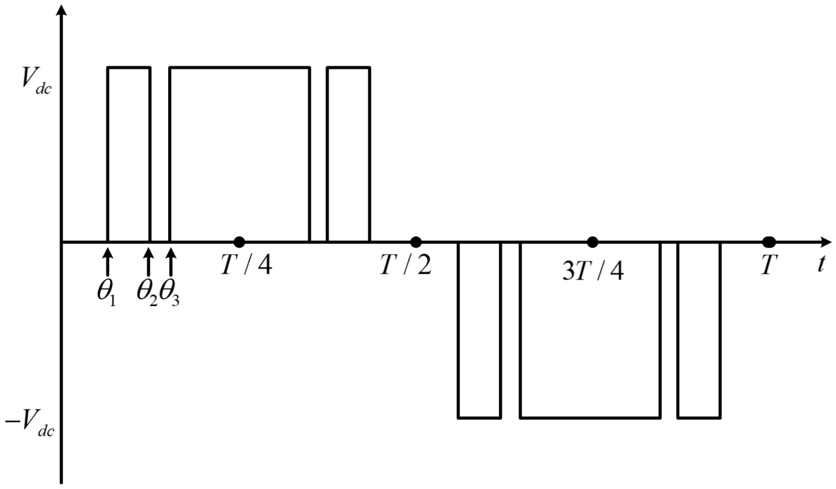


Figure 2.13: An unipolar switching output waveform

A stepped multilevel waveform is illustrated in Figure 2.14, which is a combination of the fundamental frequency switching scheme and the unipolar programmed PWM. Figure 2.14 demonstrates the application of two DC voltages and four switching angles. However, the number of switching angles and DC sources are equal with respect to the fundamental switching frequency scheme. Bipolar programmed PWM, unipolar programmed PWM and stepped multilevel PWM are all applicable for low modulation indices, although the output waveform of the stepped multilevel PWM has the lowest THD [67].

The primary challenge presented by the selective harmonic elimination PWM method is the identification of an analytical solution of the waveform and resolution of the transcendental equations for switching angles. The above example applies the Newton-Raphson

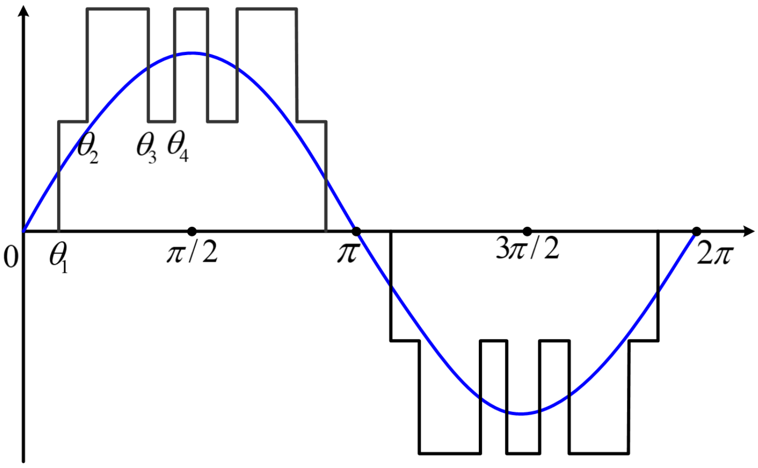


Figure 2.14: An output waveform of stepped multilevel PWM

method to solve the transcendental equations; nevertheless, this method also presents certain shortcomings, such as demanding accurate initial guesses and uncertainty solutions. In previous decades, several solving methods have been proposed, including the Bee algorithm for SHE [68], half-wave symmetry SHE [69], and the resultant method [58][67].

2.3.2 Modelling and Modulation of 2-level and 3-level Grid-connected Inverters

This section 2.3.2 will describe the modelling and modulation of three-phase grid-connected inverter systems. Before looking into the MPC of 3-level NPC inverter systems, the modelling and modulation of three-phase grid-connected inverter system with respect to the continuity of knowledge must first be reviewed. Both a low and a high frequency modelling are employed to the system, and the performance of sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) strategies is verified.

The modelling of three-phase grid-connected inverter systems will therefore be presented from two aspects: low frequency and high frequency modelling. The low frequency model of the three-phase grid-connected inverter system actually ignores the high frequency harmonics and can be used to design systems; however, it cannot express the working principle of the three-phase grid-connected inverter system. Therefore, a high frequency model should be applied to the system as it can demonstrate each switching working operation in every switching period and therefore provide precise descriptions of the relationship between the switching process and the state variable. This is highly useful when simulating waveforms and analysing the harmonics.

Accordingly, the structure of this section 2.3.2 modelling and modulation of 2-level and 3-level grid-connected inverters will be as follows. Firstly, the details of the three-phase grid-connected inverter system mathematical model from both a low frequency and high frequency perspective will be provided. Then, SPWM and SVPWM are applied to the three-phase grid-connected inverter system. Finally, comparative results will be presented.

Low Frequency Modelling

The low frequency mathematical model for a three-phase grid-connected inverter system can be obtained from an analysis of the inverter's fundamental waveform, while it ignores the high harmonic related to the switch. The low frequency mathematical model can clearly express the working principle of the system and interaction between the system's physical qualities; thus, it can be successfully employed in the design of the system controller.

In the low frequency model of the three-phase grid-connected inverter system, there are three main assumptions, which are as follows:

- Grid electromotive force is a three-phase balanced sinusoidal wave.
- All inductors and capacitors are ideal power semiconductor devices.
- All of the power switches are ideal and can ignore dead-band time.

Low Frequency Mathematical Model in ABC Static Three-phase Coordinates

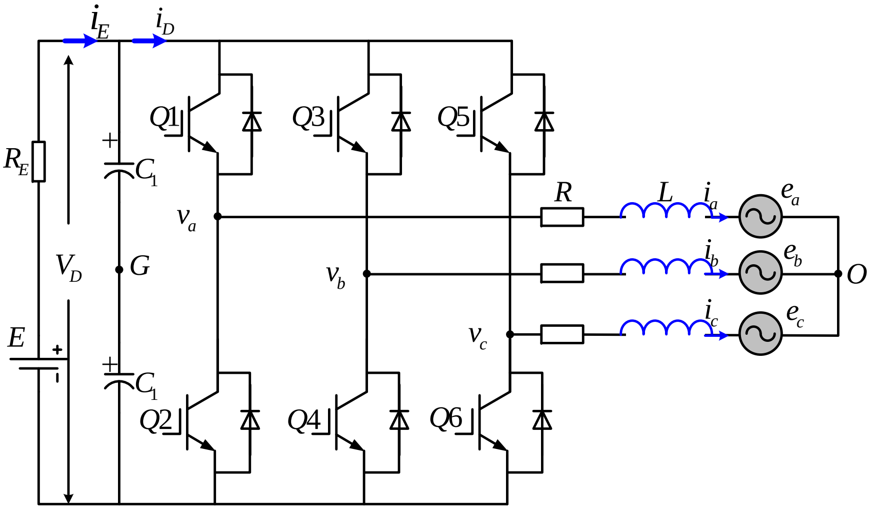


Figure 2.15: The configuration of a three-phase grid-connected inverter system

Figure 2.15 displays the configuration of a three-phase grid-connected inverter system. e_a, e_b, and e_c represent the three-phase grid voltages and the neutral point of the three-phase grid voltages is expressed as O. The grid-connected currents are i_a, i_b and i_c, and the currents' positive directions are illustrated in Figure 2.15. The filter inductance of the system is L, and the equivalent resistance is R. The output voltages of the system are v_a, v_b and v_c and G represents the assumed neutral point of input capacitance. When grid electromotive force is a three-phase balanced sinusoidal wave, the voltage level between the neutral point of the three-phase grid voltages, O, and the neutral point of input capacitance, G, are equal [70]. It can also be seen that the three-phase circuits are operationally independent; therefore, the system assumes an equivalent configuration of the three-phase grid-connected inverter system shown in Figure 2.16.

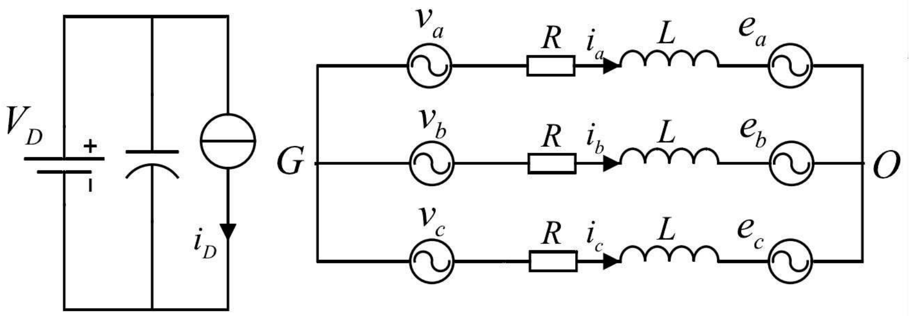


Figure 2.16: The equivalent configuration in ABC static three-phase coordinates

The voltage of a three-phase grid-connected system can be represented by three equations [70]:

$$e_a = E_m \cos(\varphi t) \tag{2.8}$$

$$e_b = E_m \cos(\varphi t - 2\pi/3) \tag{2.9}$$

$$e_c = E_m \cos(\varphi t + 2\pi/3) \tag{2.10}$$

In the above equations, E_m is the amplitude of the grid phase voltage. When the three-phase grid-connected inverter system is working with a unity power factor of $PF = 1$, the grid connected currents can be obtained:

$$i_a = I_m \cos(\varphi t) \tag{2.11}$$

$$i_b = I_m \cos(\varphi t - 2\pi/3) \tag{2.12}$$

$$i_c = I_m \cos(\varphi t + 2\pi/3) \tag{2.13}$$

In Equation 2.11 - Equation 2.13, I_m is the amplitude of the grid-connected current. According to Kirchhoff's voltage law (KVL), it can get:

$$\begin{aligned}\begin{bmatrix} L\frac{di_a}{dt} \\ L\frac{di_b}{dt} \\ L\frac{di_c}{dt} \end{bmatrix} = \begin{bmatrix} -R & 0 & 0 \\ 0 & -R & 0 \\ 0 & 0 & -R \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \\ \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} - \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \end{bmatrix}\end{aligned} \tag{2.14}$$

Equation 2.14 shows the low-frequency equation of state for the three-phase grid connected inverter system based on ABC static three-phase coordinates.

Low Frequency Mathematical Model in Static Two-phase Coordinates

In order to simplify the mathematical model, the low frequency state equation for the three-phase grid-connected inverter system can be transformed from an ABC static three-phase coordinate to an $\alpha\beta$ static two-phase coordinate on the basis of the Clarke transformation principle [70], which is presented in Figure 2.17. When the α axis of the $\alpha\beta$ static two-phase coordinate overlaps the A axis of the ABC static three-phase coordinate, the transformation matrix from the ABC static three-phase coordinate to $\alpha\beta$ static two-phase coordinate is:

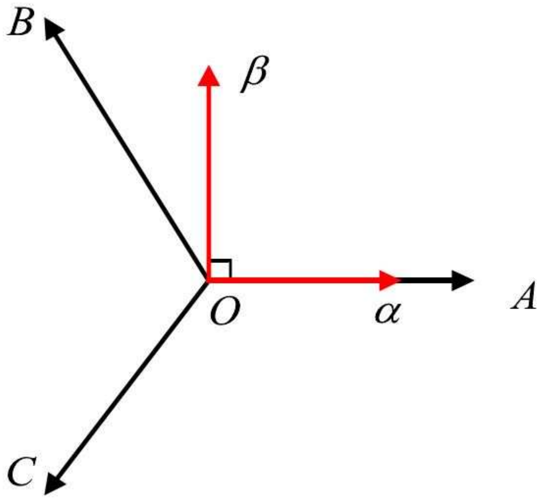


Figure 2.17: The Clarke transformation principle

$$T_{abc/\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -1/2 & -1/2 \\ 0 & \sqrt{3}/2 & -\sqrt{3}/2 \end{bmatrix} \tag{2.15}$$

In addition, a transformation matrix can be obtained from the $\alpha\beta$ static two-phase coordinates to produce the ABC static three-phase coordinates:

$$T_{\alpha\beta/abc} = \begin{bmatrix} 1 & 0 \\ -1/2 & \sqrt{3}/2 \\ -1/2 & -\sqrt{3}/2 \end{bmatrix} \tag{2.16}$$

Considering the equations presented above, the equation relating to the state of the inverter system can be obtained from the $\alpha\beta$ static two-phase coordinates.

$$\begin{bmatrix} L\frac{di_\alpha}{dt} \\ L\frac{di_\beta}{dt} \end{bmatrix} = T_{abc/\alpha\beta} \begin{bmatrix} -R & 0 & 0 \\ 0 & -R & 0 \\ 0 & 0 & -R \end{bmatrix} T_{abc/\alpha\beta} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + T_{abc/\alpha\beta} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} T_{\alpha\beta/abc} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} - T_{abc/\alpha\beta} \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} T_{\alpha\beta/abc} \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \tag{2.17}$$

Simplifying Equation 2.17 shows the equation of the state for the low frequency equation of state in the three-phase grid connected inverter system based on $\alpha\beta$ static two-phase coordinates.

$$\begin{bmatrix} L\frac{di_\alpha}{dt} \\ L\frac{di_\beta}{dt} \end{bmatrix} = \begin{bmatrix} -R & 0 \\ 0 & -R \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} e_\alpha \\ e_\beta \end{bmatrix} \tag{2.18}$$

Low Frequency Mathematical Model in dq Rotary Two-phase Coordinate

On account of the coordinate transformations, the $\alpha\beta$ static two-phase coordinates can be transferred to the dq rotary two-phase coordinates. This kind of coordinate transformation is also referred to as the Park transformation. The principle of the Park transformation is illustrated in Figure 2.18.

Below is the transformation matrix for $\alpha\beta$ static two-phase coordinates to dq rotary two-phase coordinates:

$$T_{\alpha\beta/dq} = \begin{bmatrix} \cos\omega t & \sin\omega t \\ -\sin\omega t & \cos\omega t \end{bmatrix} \tag{2.19}$$

In the same way, the transformation matrix can be established from the dq rotary two-phase coordinates to the $\alpha\beta$ static two-phase coordinates:

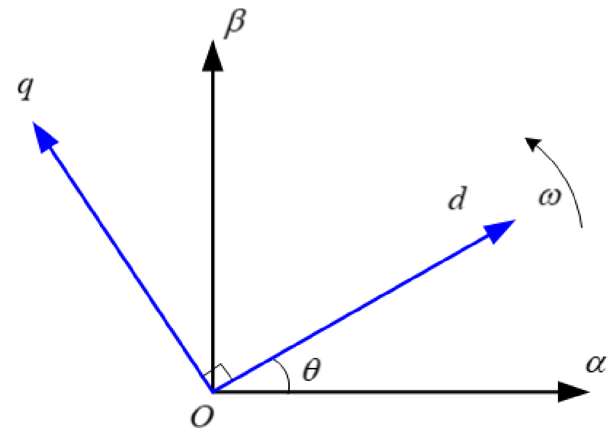


Figure 2.18: The Park transformation principle

$$T_{dq/\alpha\beta} = \begin{bmatrix} \cos\omega t & -\sin\omega t \\ \sin\omega t & \cos\omega t \end{bmatrix} \tag{2.20}$$

The relationship of the current between the two kinds of coordinates is therefore:

$$\begin{aligned} T_{\alpha\beta/dq} L \frac{d}{d_t} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} &= L \frac{d}{d_t} (T_{\alpha\beta/dq} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix}) - L \frac{dT_{\alpha\beta/dq}}{d_t} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} \\ &= L \frac{d}{d_t} \begin{bmatrix} i_d \\ i_q \end{bmatrix} - \begin{bmatrix} 0 & \omega t \\ -\omega L & 0 \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} \end{aligned} \tag{2.21}$$

Consequently, the equation indicates that it is possible to obtain the equation of state in the *dq* rotary two-phase coordinates:

$$\begin{bmatrix} L\frac{di_d}{dt} \\ L\frac{di_q}{dt} \end{bmatrix} = \begin{bmatrix} -R & \omega L \\ -\omega L & -R \end{bmatrix} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} v_d \\ v_q \end{bmatrix} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} e_d \\ e_q \end{bmatrix} \tag{2.22}$$

Looking at Equation 2.22, it is easy to implement the system design and analysis using the *dq* coordinate transformation; however, the components in the *d* axis and *q* axis are coupling. Therefore they do not serve to benefit the degree of stability and the dynamic character of the system as a whole. In the following section, action will therefore be taken to decouple them.

High Frequency Modelling

As previously mentioned, the low frequency model of the three-phase grid-connected inverter system ignores the high frequency harmonics. As a result, the low frequency model can still be used to design systems; however, it cannot express the working principle of the three-phase grid-connected inverter system [71]. It is therefore necessary to formulate a high frequency model for use within the system [71][72]. Furthermore, given that the high frequency mathematical model can demonstrate each switching working operation in every switching period, it can precisely describe the relationship between the switching process and the state variable. This is of great utility when simulating waveforms and analysing the harmonics.

The high frequency model of the three-phase grid-connected inverter system is also required to make the three following assumptions:

- Electromotive grid force is a three-phase balanced sinusoidal wave.
- All of the inductors and capacitors are ideal semiconductor power devices.
- All of the power switches are ideal and can be ignored in the dead-band time.

High Frequency Mathematical Model in ABC Static Three-phase Coordinates

An ABC static three-phase coordinates can be used to build a high frequency mathematical model. The input voltage in the DC side is represented as E. V_D is the capacitor voltage in the DC side, and R_E is the equivalent impedance of the DC power supply. Considering the high switching condition, S_a, S_b and S_c are the switching functions of the ABC three-phase leg, and 1 and 0 represent the up leg conduction and the down leg conduction, respectively. According to the definition of the switching function, the following equations can be obtained:

$$v_{aN} = S_a V_D \tag{2.23}$$

$$v_{bN} = S_b V_D \tag{2.24}$$

$$v_{cN} = S_b V_D \tag{2.25}$$

Depending on the Kirchhoff's voltage law, the voltage equation can also be obtained in the A phase:

$$L\frac{di_a}{d_t} + Ri_a = v_{ao} - e_a = v_{aN} + v_{No} - e_a \tag{2.26}$$

According to the definition of the switching function, Equation 2.26 can then be simplified to:

$$L\frac{di_a}{d_t} + Ri_a = S_a V_D + v_{No} - e_a \tag{2.27}$$

In the same way, the model can obtain a comparable equation in the B and C phase:

$$L\frac{di_b}{d_t} + Ri_b = S_b V_D + v_{No} - e_b \tag{2.28}$$

$$L\frac{di_c}{d_t} + Ri_c = S_c V_D + v_{No} - e_c \tag{2.29}$$

Considering the balanced three-phase system, the following equations can be obtained:

$$e_a + e_b + e_c = 0 \tag{2.30}$$

$$i_a + i_b + i_c = 0 \tag{2.31}$$

According to the above equations, the equation can be presented as follows:

$$v_{No} = -\frac{1}{3}V_D(S_a + S_b + S_c) = -\frac{1}{3}V_D \sum_{k=a,b,c} S_k \tag{2.32}$$

In the three-phase grid-connected inverter system, there are always three switches under the conduction state; thus, the DC side current, i_D, can be described as follows:

$$i_D = i_a S_a + i_b S_b + i_c S_c \tag{2.33}$$

For the positive point of capacitor P, the Kirchhoff's circuit law is then applicable:

$$C\frac{dV_D}{d_t} = i_E - i_D = \frac{E - V_D}{R_E} - (i_a S_a + i_b S_b + i_c S_c) \tag{2.34}$$

When combining Equation 2.28, Equation 2.29, Equation 2.30, Equation 2.32 and Equation 2.34, the state variable mathematical model of the three-phase grid-connected system can be obtained in an ABC static three-phase coordinates:

$$\begin{bmatrix} L\frac{di_a}{dt} \\ L\frac{di_b}{dt} \\ L\frac{di_c}{dt} \\ C\frac{dV_D}{dt} \end{bmatrix} = \begin{bmatrix} -R & 0 & 0 & S_a - \frac{1}{3}V_D\sum_{k=a,b,c} S_k \\ 0 & -R & 0 & S_b - \frac{1}{3}V_D\sum_{k=a,b,c} S_k \\ 0 & 0 & -R & S_c - \frac{1}{3}V_D\sum_{k=a,b,c} S_k \\ -S_a & -S_b & -S_c & -\frac{1}{R_E} \end{bmatrix} \begin{bmatrix} i_a \\ i_b \\ i_c \\ V_D \end{bmatrix} + \begin{bmatrix} -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & \frac{1}{R_E} \end{bmatrix} \begin{bmatrix} e_a \\ e_b \\ e_c \\ E \end{bmatrix} \tag{2.35}$$

The voltage between the assumed neutral point of the output capacitor, G, and the neutral point of the grid, O, is therefore:

$$V_{GO} = V_{GN} + V_{NO} \tag{2.36}$$

In terms of Equation 2.35, the input current of each phase can be decided together by the three-phase switching function. This inverter system is the coupling of a multi-order nonlinear time-varying system. In Equation 2.36, it is apparent that the three-phase is coupling; therefore, the equivalent configuration of the three-phase grid-connected inverter system based on ABC static three-phase coordinates from the high frequency aspect is shown in Figure 2.19.

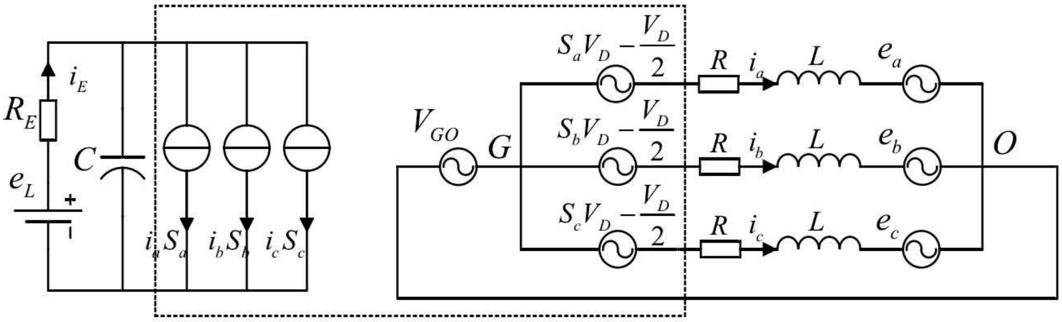


Figure 2.19: The equivalent configuration from the high frequency aspect

High Frequency Mathematical Model in Static Two-phase Coordinate

According to the formula for coordinating transformation equations, Equation 2.35 can be transformed from the ABC static three-phase coordinate to the $\alpha\beta$ static two-phase coordinates. The high frequency mathematical model for the $\alpha\beta$ static two-phase coordinates is thus shown as the following:

$$\begin{bmatrix} Ldi_a \\ Ldi_b \\ C\frac{dV_D}{dt} \end{bmatrix} = \begin{bmatrix} -R & 0 & S_\alpha \\ 0 & -R & S_\beta \\ -S_\alpha & -S_\beta & -\frac{1}{R_E} \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \\ V_D \end{bmatrix} + \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & \frac{1}{R_E} \end{bmatrix} \begin{bmatrix} e_\alpha \\ e_\beta \\ E \end{bmatrix} \tag{2.37}$$

In Equation 2.37, input currents i_α and i_β only have a relationship with their own switching function; thus, they are not coupling. However, the following the coordination transformation, the two-phase voltage and current are still sinusoidal. The output voltage in the inverter leg can therefore be expressed as:

$$v_\alpha = S_\alpha V_D \tag{2.38}$$

$$v_\beta = S_\beta V_D \tag{2.39}$$

The input current of the inverter can then be represented as follows:

$$i_D = S_\alpha i_\alpha + S_\beta i_\beta \tag{2.40}$$

The equivalent electronic circuit of the three-phase grid-connected inverter system based on the static two-phase coordinates from the high frequency aspect is shown in Figure 2.20.

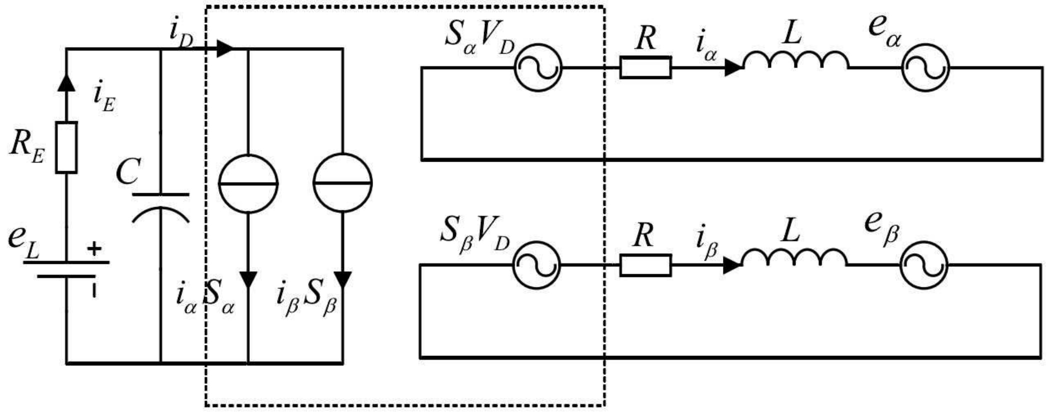


Figure 2.20: The high frequency equivalent model in the static two-phase coordinates

High Frequency Mathematical Model in dq Rotary Two-phase Coordinates

Through coordinate transformation, the $\alpha\beta$ static two-phase coordinate can be transformed to the dq rotary two-phase coordinates. The voltage of the three-phase grid-connected system is therefore as follows [70]:

$$e_a = E_m \cos(\varphi t) \tag{2.41}$$

$$e_b = E_m \cos(\varphi t - 2\pi/3) \tag{2.42}$$

$$e_c = E_m \cos(\varphi t + 2\pi/3) \tag{2.43}$$

Furthermore, the following is the three-phase grid voltage vector [72]:

$$\vec{e} = \frac{2}{3}(e_a \cdot e^{j0} + e_b \cdot e^{j\frac{2\pi}{3}} + e_c \cdot e^{j\frac{4\pi}{3}}) = E_m \cos(\varphi t + j \sin \omega t) \tag{2.44}$$

From Equation 2.44, the vector of the three-phase grid voltage is a rotation vector in the complex plane, where the magnitude of the vector is E_m, and the angle between the vector and the A axis is θ. Therefore, the projection of the grid voltage vector in the ABC static three-phase coordinate is the instantaneous value of the three-phase grid voltage. The vectors in dq rotary two-phase coordinates are presented in Figure 2.21. In the decomposition of the vector, i_d is an active current in the d axis, and i_q is the reactive current in the q axis. In the initial condition, the d axis and the A axis overlap.

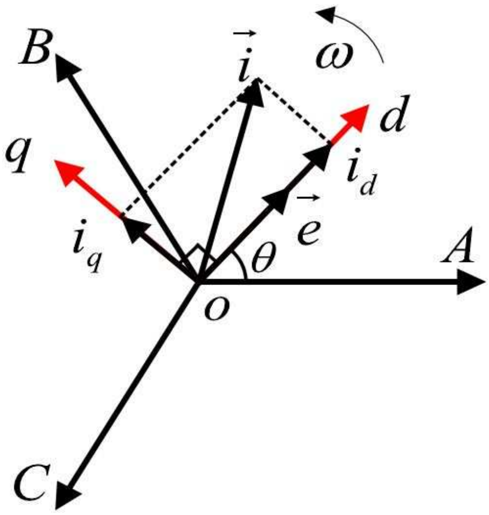


Figure 2.21: The vectors in the dq rotary two-phase coordinates

According to Equation 2.21 and Equation 2.37, the high frequency mathematical model of the three-phase grid-connected inverter system in the dq rotary two-phase coordinates can be achieved.

$$\begin{bmatrix} L\frac{di_d}{dt} \\ L\frac{di_q}{dt} \\ C\frac{dV_D}{dt} \end{bmatrix} = \begin{bmatrix} -R & \omega L & S_d \\ -\omega L & -R & S_q \\ -S_d & -S_q & -\frac{1}{R_E} \end{bmatrix} \begin{bmatrix} i_d \\ i_q \\ V_D \end{bmatrix} + \begin{bmatrix} -1 & 0 & 0 \\ 0 & -1 & 0 \\ 0 & 0 & \frac{1}{R_E} \end{bmatrix} \begin{bmatrix} e_d \\ e_q \\ E \end{bmatrix} \tag{2.45}$$

From Equation 2.45, the output voltage from the inverter leg in dq rotary two-phase coordinates is:

$$v_d = S_d V_D \tag{2.46}$$

$$v_q = S_q V_D \tag{2.47}$$

And the input current of the inverter is:

$$i_D = S_d i_d + S_q i_q \tag{2.48}$$

From Equation 2.45, it is apparent that the high frequency model is also coupling in the dq rotary two-phase coordinates. The output currents i_d and i_q influence each other, so they may also influence the design of the system controller to some extent. From another perspective, the systems control variables become direct current values, while the number of the active power components and reactive components also becomes clear. The high frequency configuration of the equivalent circuit in dq rotary two-phase coordinates is shown in Figure 2.22.

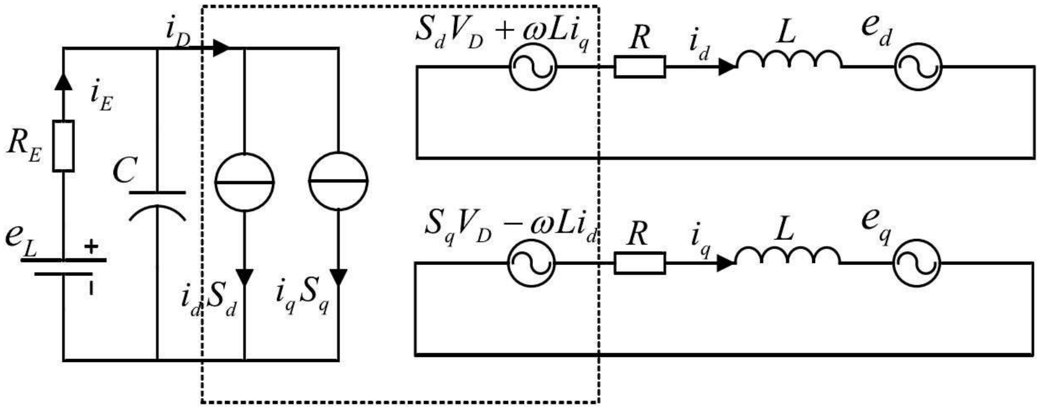


Figure 2.22: The high frequency configuration of the equivalent circuit

SPWM Algorithm

In this section, the establishment of a system model is employed to assess the performance of sinusoidal pulse width modulation (SPWM) and space vector pulse width modulation (SVPWM) algorithms. More specifically, the three-phase grid-connected inverter system model was constructed in MATLAB Simulink, which was accomplished by analysing both the low frequency and high frequency mathematical models. In turn, the SPWM was then applied to the 2-level and three-phase grid-connected systems, as was the SVPWM. Following this, simulator-based investigations were undertaken for the purpose of gathering initial findings. These findings indicate that the higher performing system is the SVPWM algorithm, which is facilitated on the basis of the 3-level NPC inverters. Moreover, from these different simulations, it was revealed that the SVPWM control algorithm produces more effective results when compared to the SPWM in the context of an identical inverter system level. Furthermore, it was also noted that multilevel inverters produce output currents that are linked to a reduced level of distortion when applied to the 2-level inverters.

Principle of the SPWM Algorithm for 2-level Inverters

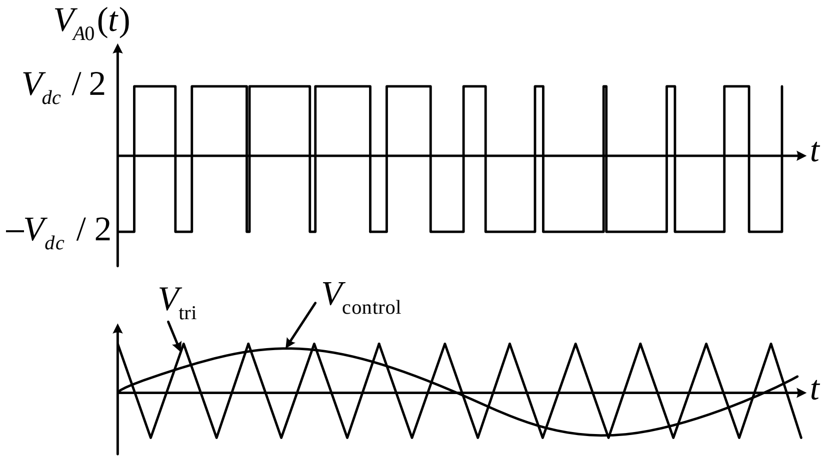


Figure 2.23: The basic principle of SPWM

Figure 2.23 shows the basic principle of sinusoidal PWM. SPWM is one of the most widely applied modulation techniques used in power switching inverters. Given that power loss is quite an important issue, especially in high power applications, the fundamental frequency SPWM method has been applied to minimise the switching losses. In Figure 2.23, the SPWM method allows for a comparison of the reference voltage signal with the triangular carrier signal to produce the rectangular signal. The resultant signal was then used in the gate pole of switches in the power inverter; therefore, the output voltage of the inverter is determined as follows:

When $V_{control} > V_{tri}, V_{AO} = V_{dc}/2$
When $V_{control} < V_{tri}, V_{AO} = -V_{dc}/2$

SPWM Simulation Results for 2-level Inverters

The system parameters and value are shown in Table 2.3. In this section, the system parameters and value remain constant. At the simulation time $1s$, the reference of i_d stepped up from $30A$ to $60A$. Meanwhile, the reference of i_q kept $0A$; thus, the results of the simulation had been achieved in Figure 2.24.

Table 2.3: System Parameters and Value

Parameter Name	**Symbol**	**Value**
DC source voltage	V_{DC}	$800\,V$
Inductor	L	$0.006\,H$
Resistance	R	$0.01\,\Omega$
AC peak voltage	V_{peak}	$311\,V$
Grid frequency	f_p	$50\,Hz$

Total harmonic distortion (THD) is a measurement of the harmonic distortion present in a signal. THD is the summation of all harmonic components of current or voltage waveforms compared to their fundamental components [37]. The harmonic currents that are injected into a power system can affect the voltage of the power system and subsequently its applications for customers [38]. Regarding the power system itself, harmonic currents are one of the main sources of disturbances, causing equipment to overheat and the performance of electronic equipment to deteriorate [38]. With regard to customer applications, the performance of equipment such as motor drives and electric vehicle power supplies can also be adversely affected by harmonics. Therefore, the THD of the output current is an indicator of the system performance.

The THD calculating equation is:

$$THD = \frac{\sqrt{I_2^2 + I_3^2 + I_4^2 + \dots}}{I_1^2} \tag{2.49}$$

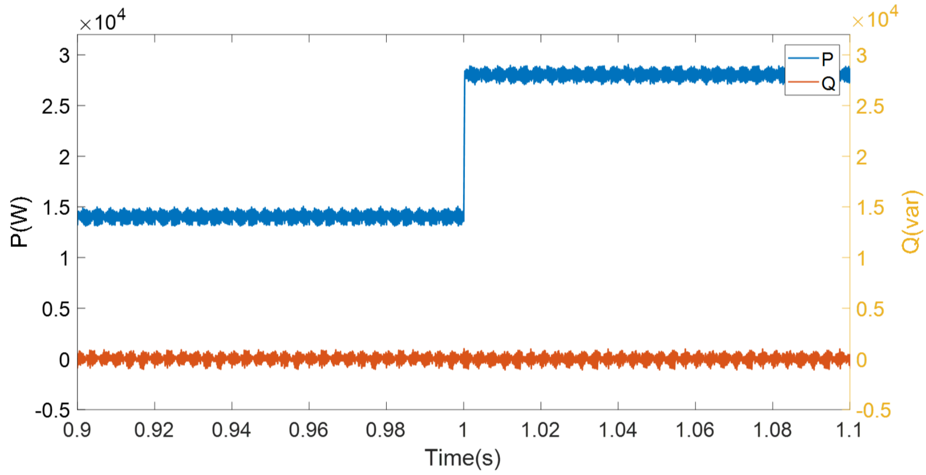
In this equation, I_n is the RMS current of the nth harmonic and $n = 1$ is the fundamental value.

SVPWM Algorithm

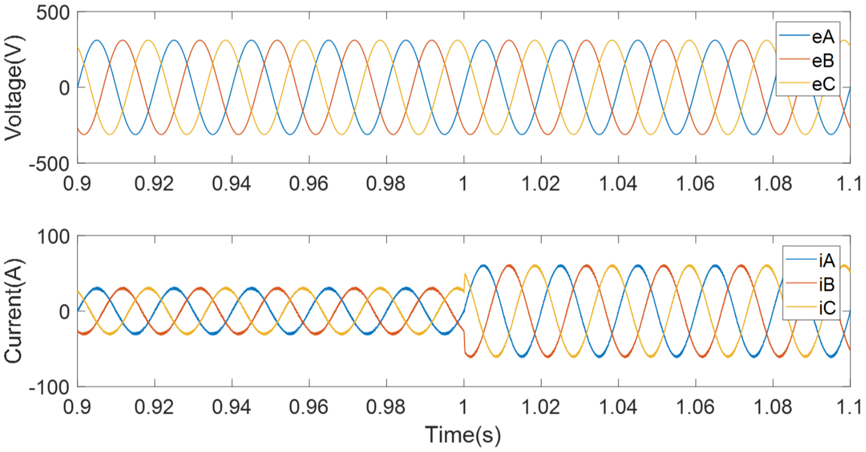
In the three-phase grid-connected inverter system, space vector pulse width modulation (SVPWM) is one of the most attractive modulation techniques. It is also most commonly implemented in industrial applications. SVPWM controls the output voltage vectors of inverters and generates an optimum switching pattern, which helps to decrease power losses and switching frequencies. Moreover, a comparison of the simulation results of SPWM and SVPWM in Table 2.4 indicates that the SVPWM method has lower harmonic content than the conventional SPWM method.

Principle of SVPWM Algorithm for 2-level Inverters

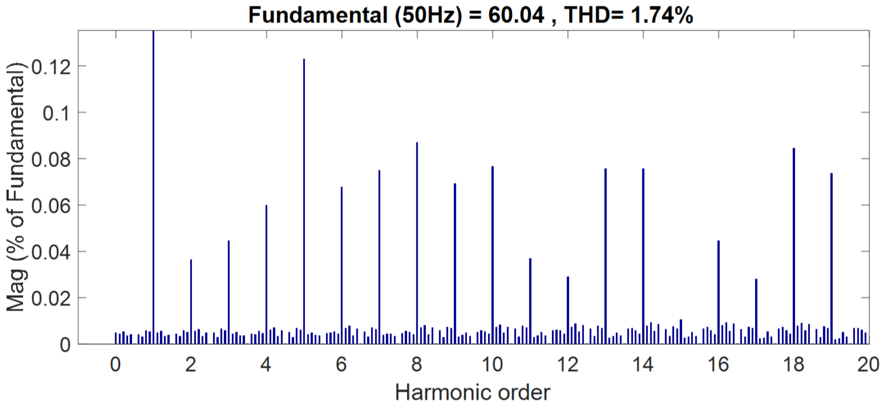
The space vector PWM requires a combination of eight different space vectors, as shown in Figure 2.25 to synthesise the reference voltage vector $\vec{V_s}$. In detail, it combines two effective vectors and one zero vector to synthesise the reference voltage vector. In order to implement SVPWM, there are four key steps:



(a)



(b)



(c)

Figure 2.24: Simulation results of the SPWM for 2-level inverter: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The THD of output currents.

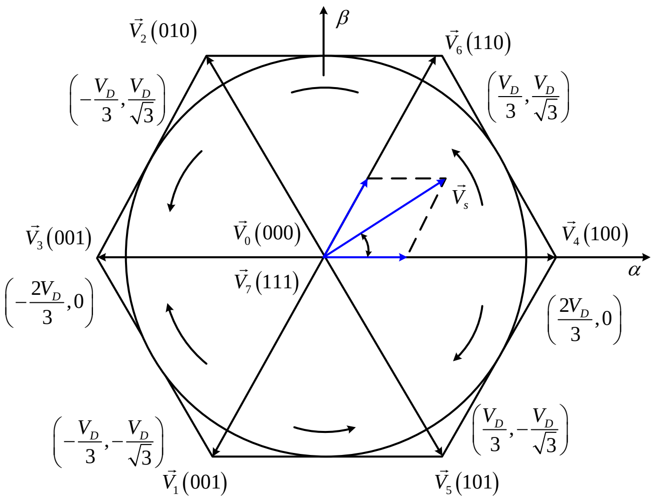


Figure 2.25: Eight basic space voltage vectors

- Determine the space vector.
- Select sector.
- Calculate the switching time of the two adjacent vectors.
- Synthesise the three-phase PWM signal.

More details can be referred to [71].

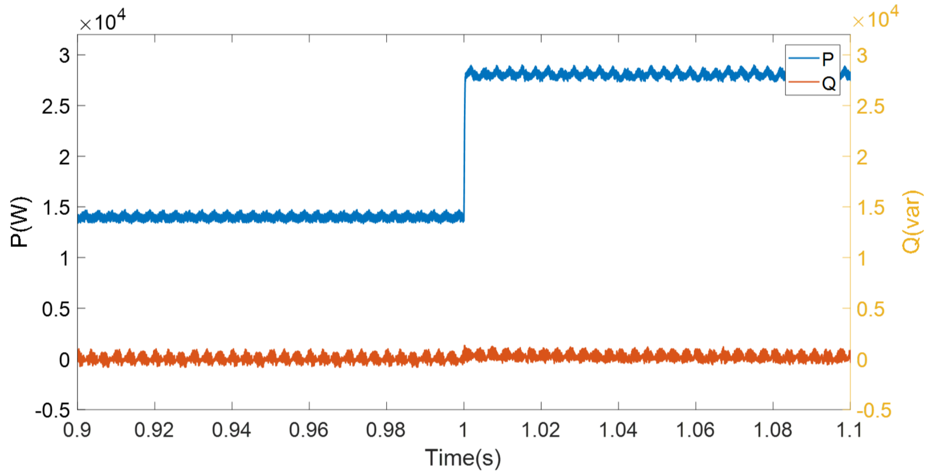
SVPWM Simulations for 2-level Inverters

A 2-level three-phase grid-connected system was employed to assess the performance of space vector pulse width modulation (SVPWM) in this section. To be specifical, the three-phase grid-connected inverter system model was built in MATLAB Simulink on the basis of the low frequency mathematical model and the high frequency mathematical model established in the previous part. Subsequently, the SVPWM method was applied to the 2-level three-phase grid-connected system. The key steps in implementing the SVPWM simulation models are the selecting sector model, calculating the switching time of the two adjacent vectors, and synthesising the signal wave.

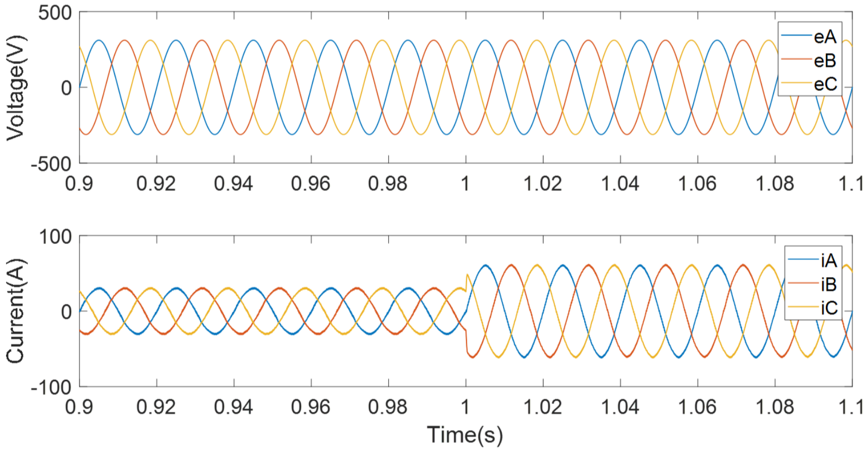
From the simulation results, the harmonic order in SVPWM and the waveform of output voltage and current were able to be acquired in Figure 2.26(b) and Figure 2.26(c), respectively. The total harmonic distortion (THD) value was measured at 1.47%, well below the 5% limit tolerated according to the *IEEE Standard 519*.

SVPWM Algorithm for 3-level Grid-connected Inverter Systems

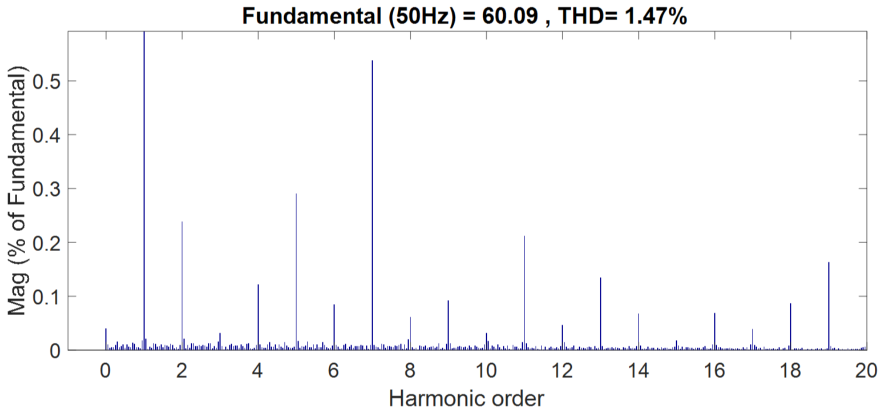
Although the principle of the SVPWM simulation model in a 3-level grid-connected inverter system is the same, the particular modulation method is more complicated.



(a)



(b)



(c)

Figure 2.26: Simulation results of the SVPWM for 2-level inverter: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The THD of output currents.

More details can be referred to [73]. Figure 2.27(c) shows the harmonic order of waveform in SVPWM for 3-level inverters. Of the three simulations covered, in this section, this algorithm was seen to demonstrate the highest level of performance. The waveforms of the output three-phase voltages and currents are also shown in Figure 2.27(b).

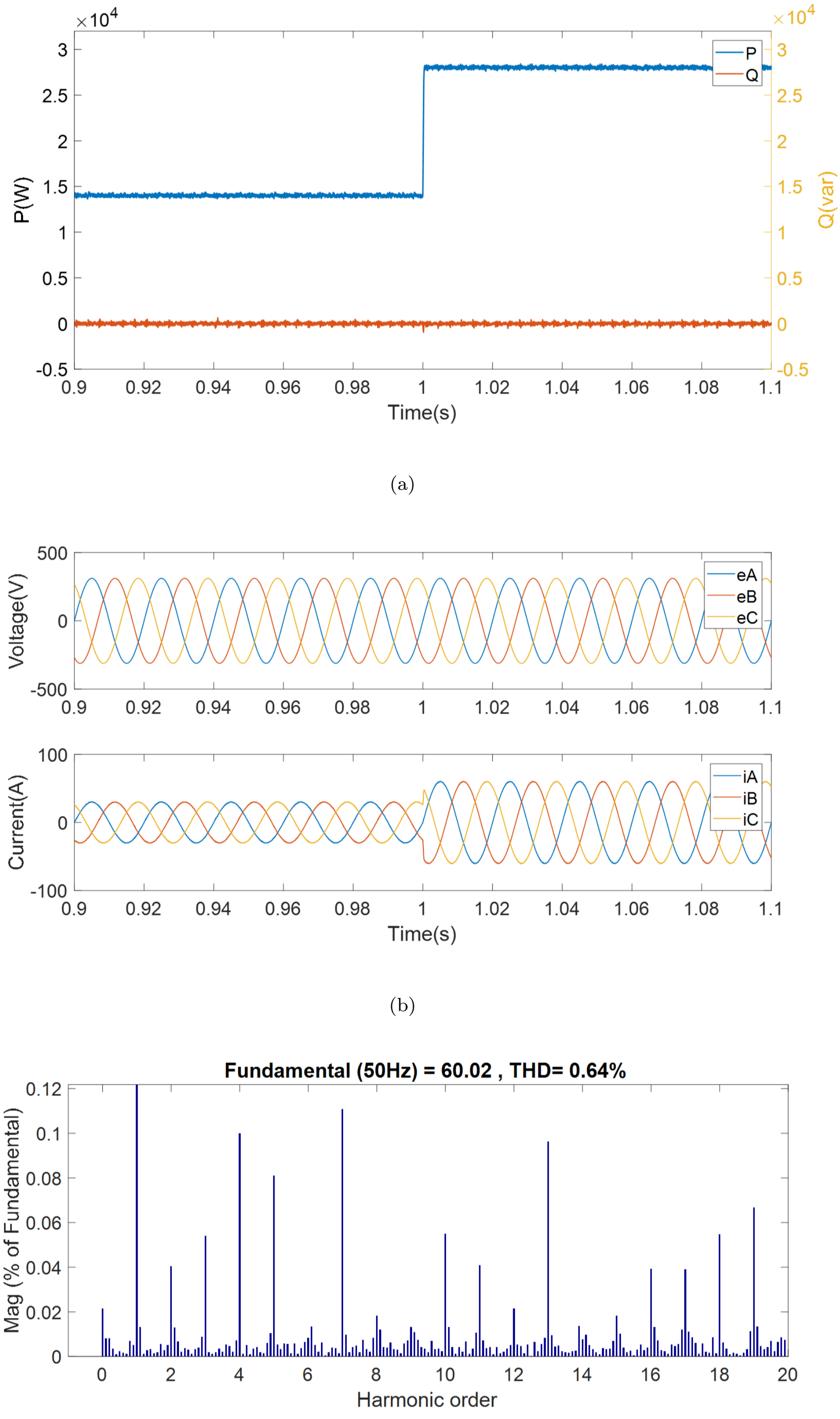
Comparative Results for Modulation Strategies

The performance of the output currents' THD using SPWM and SVPWM in 2-level and 3-level inverter systems are summarised in Table 2.4. From the simulation results, it is possible to derive two findings. Firstly, by comparing the THD of SPWM in the 2-level inverter (1.74%) into the SVPWM in the 2-level inverter (1.47%), the SVPWM control algorithm was seen to outperform the SPWM in the 2-level inverter. Secondly, by comparing the THD (1.47%) of SVPWM control in the 2-level inverter and the THD (0.64%) in the 3-level inverters, it is clear that the multilevel inverters produce fewer harmonics than the 2-level inverters. More importantly, this is the primary reason why multilevel inverters are rising in popularity. In conclusion, it is clear that in terms of efficacy, the SVPWM control algorithm, which is based on the 3-level NPC inverters, exhibits the most optimal performance.

Table 2.4: THD Comparisons of SPWM and SVPWM in 2-level and 3-level Three-phase Inverter Systems

Modulation and Inverter	**THD**
SPWM in two-level	1.74%
SVPWM in two-level	1.47%
SVPWM in three-level	0.64%

Regarding the modulation and linear control methods, inverters are primarily controlled via modulation methods, such as pulse width modulation (PWM) and sinusoidal pulse width modulation (SPWM), as well as linear controllers underpinned by a time-average model. However, such methods present a number of difficulties because the use of semiconductor elements, such as power switches, results in the power inverter system exhibiting a hybrid character. In terms of control, power inverters involve nonlinear systems that comprise continuous as well as discrete components. The state-space averaged method is therefore usually adopted in the design of linear controllers. Still, it also presents major shortcomings, such as the fact that a particular operating point must be used to linearise the model. Furthermore, there is a great deal of complexity inherent in the tuning procedure of the controller, which is increased even more after adjusting the operating point. Moreover, the controller cannot be effectively tuned in the absence of substantial expertise.



(a)

(b)

(c)

Figure 2.27: Simulation results of the SVPWM for 3-level inverters: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The THD of output currents.

2.3.3 Conventional Control Methods

Both the inverter, along with its control methods, have been developed through technological evolutions and industrial application, including power semiconductors, new inverter topologies, and digital signal processors. Although control efforts previously focused on the inverters' strength and stability, there is now a greater need for flexibility in the inverters' control systems as inverters have more complex applications. There are two typical types of well-known control methods for inverters, which are:

- Linear control (based on the time-average model and PWM modulation).
- Hysteresis control.

The remainder of this section will examine established literature concerning these two types of control methods for inverters.

The first category of control method is linear control, wherein the linearisation of the converter model is controlled, and the error between the measured and reference values is adjusted by a linear controller to obtain a pulse width modulation (PWM) wave, which is modulated to obtain the switching state. An example of linear control is voltage-oriented control (VOC) [74]. Furthermore, the number of power switches involved has led to the implementation of modulation methods, such as space vector PWM [59] and carrier-based PWM [75]. Field-oriented control (FOC) is a particularly popular linear control theory-based control scheme because of the widespread utilisation of inverters in motor drives [76][77]. An FOC control diagram concerning AC motor drive control [76] is presented in Figure 2.28, along with a three-phase inverter. The voltage references to the space vector modulation (SVM) requires the use of two proportional-integral (PI) controllers, and this control scheme requires further coordinate changes. In terms of motor drive application, multiple technical limitations are present in the control design, such as maximum current and total harmonic distortion (THD). Therefore, it can be challenging to design PI controllers as it is not possible to directly include these.

The other category of control method is hysteresis control, which uses the nonlinear characteristics of the converter to set the loop width for the hysteresis comparator in order to limit the error between the measured and reference values. The hysteresis comparator directly outputs the switching state based on the relationship between the error and the loop width. Examples of this are current hysteresis control [17], direct power control (DPC) [78] and direct torque control (DTC) [79][80]. These three types of controls have their own advantages with respect to their application; however, they also have some distinct problems with high sampling frequency. DTC has widely been used in torque control and motor speed accuracy control [81]. DTC, unlike FOC, does not need to coordinate transformation, as illustrated in Figure 2.29 [81]. To produce the

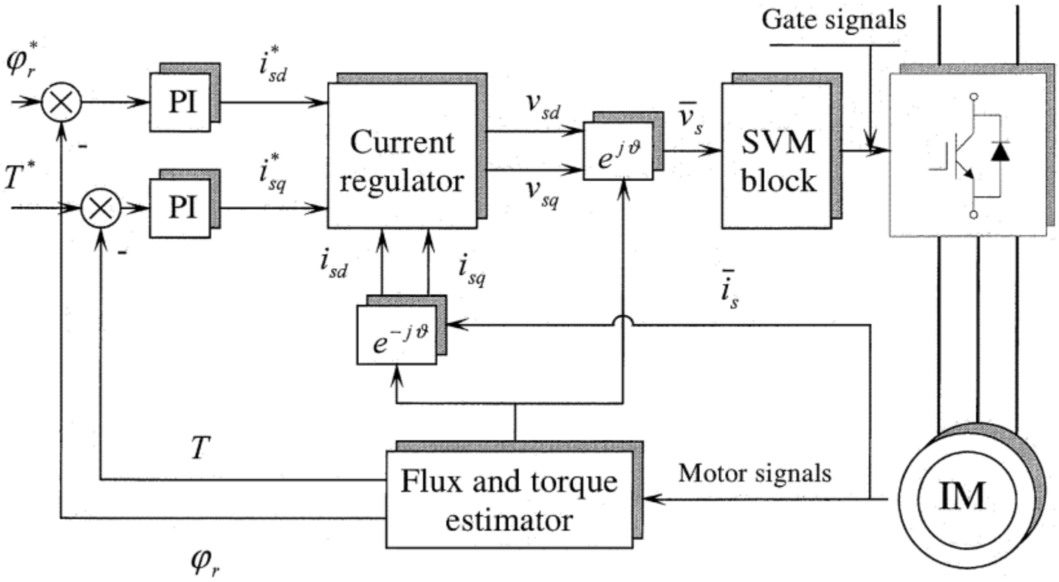


Figure 2.28: Field oriented control (FOC) control scheme [76]

inverters switching states, the flux and motor torque are compared to their references in terms of a specific hysteresis band. Using such a method on a digital platform, however, using such a method on a digital platform requires a high sampling frequency.

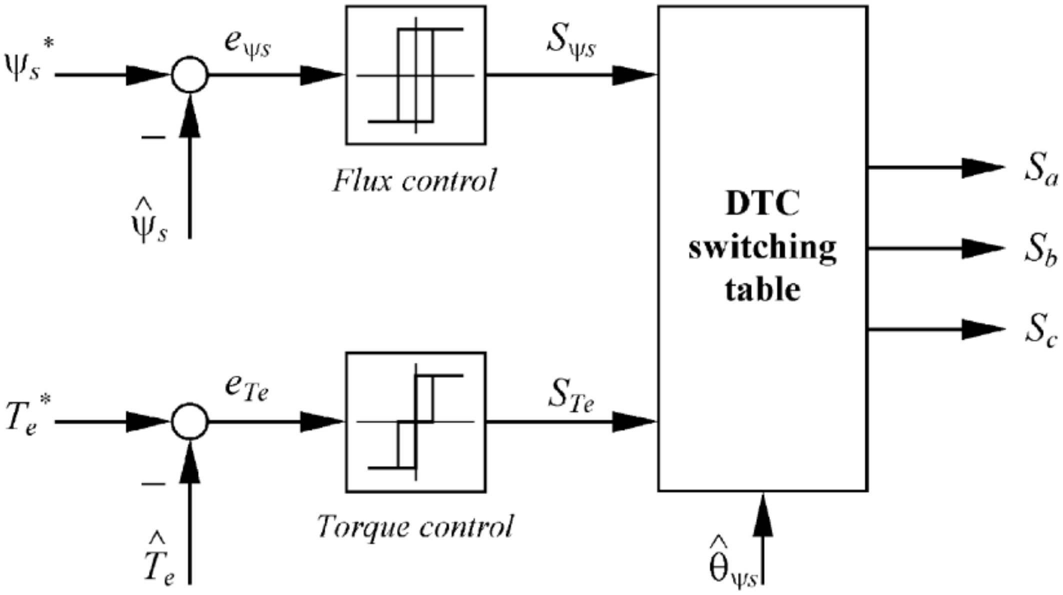


Figure 2.29: Direct torque control scheme [81]

A comparison of the two different control categories mentioned above is provided in Table 2.5, from which it can be seen that hysteresis control is based on a simple principle, namely that of directly outputting the switching state, as it has a fast dynamic response. Only the loop width of the hysteresis controller needs to be designed; however, the switching frequency is not fixed and is determined by the load parameters, loop width, and operating environment. To improve the control performance, it therefore requires a

Table 2.5: Comparison of Classical Control Methods

	Linear Controller	**Hysteresis Controller**
Model	Linear model with approximation	No model
Controller design	Compensator parameter tuning (pole placement or root locus)	Hysteresis width
Modulation	PWM	No modulation
Switching frequency	Fixed	Variable
Steady state response	Good	Better
Transient state response	Normal	Fast
Sampling frequency	Normal	High
Control flexibility	Constraints inclusion is not straightforward	Constraints inclusion is not straightforward

smaller loop width and a higher sampling frequency. Linear control, on the other hand, is based on a linear model of the converter; however, this approximate linearisation process does not meet the requirements of high-precision control. The PI parameter settings also have a significant effect on control performance; thus, the functioning of the control system is greatly affected by the PI constraints. Furthermore, because a modulation unit is used to ensure that the switching frequency matches the modulation frequency, the dynamic performance of the control system is affected. Moreover, due to the requirements of contemporary industrial applications, there is a greater need for flexibility in the inverter control systems today as inverters have more complex applications. Accordingly, the main limitation of conventional control methods is their limited control flexibility.

Based on the limitations of the conventional control methods and the sudden increased demand for greater efficiency and performance of power converters and drives, new developments in control methods should take the real nature of power converters and drives into account [22]. In detail, converters are nonlinear systems of a hybrid nature that include both linear and nonlinear parts and a finite number of switching devices. Furthermore, the input signals command the power electronics devices switch, which must be discrete signals. Based on these inherent characteristics of power devices and security reasons, some constraints need to be considered. For example, the maximum output voltage of the inverter is inherent to the system, and the limitation on the current protects the loads and the converter. At the same time, digital control platforms like DSPs have become state of the art and have been widely used in industrial applications. Recently, field-programmable gate arrays (FPGAs) have received particular attention because of their ability to allow users to build efficient and dedicated hardware architecture by means of flexible software.

Due to the rapid development of these digital control platforms, which offer an increase in computational capability, calculation based control methods are more feasible in the current day, which are particularly suited to model predictive control. In the next section 2.3.4, model predictive control will be reviewed. The key characteristics of control methods are summarised in Figure 2.30. Depending on the inherent characteristics of power converters and the development of digital control platforms, model predictive control can largely be seen to be suited to power converters.

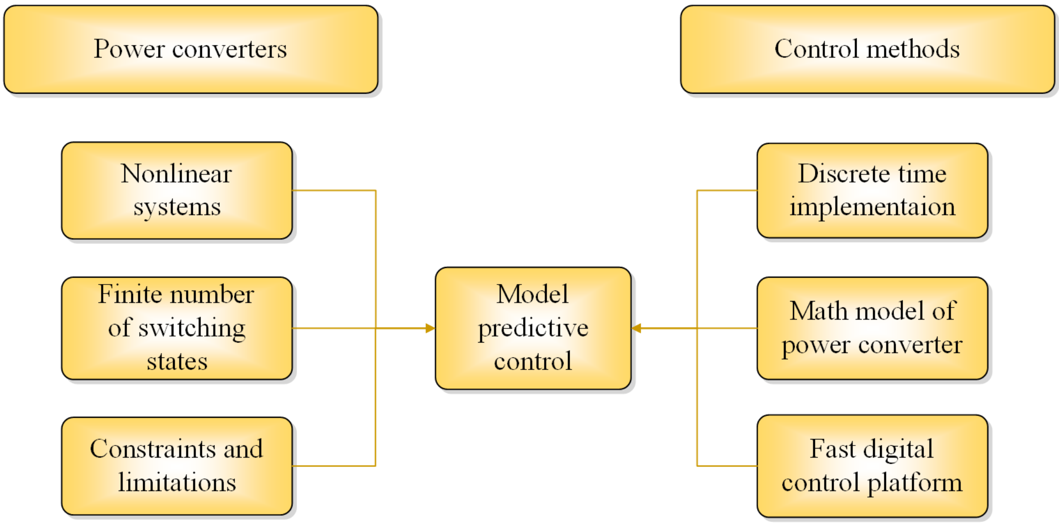


Figure 2.30: Model predictive control is suited to power converters [21]

2.3.4 Model Predictive Control

In recent years, model predictive control, which is applied in power electronics, stands out from many modulation (PWM, SVPWM, etc.) and control methods (PI, hysteresis control, and sliding mode control) due to its fast dynamic response, allowing for easy implementation in digital platforms and handling of multiple system constraints [82]. As a result, model predictive control has drawn much attention from academia and industry. Accordingly, in this section 2.3.4, model predictive control (MPC), including the development of MPC, the fundamental of MPC, the applications of MPC, and the existing problems of MPC are reviewed, respectively. From the literature review, it can be seen that research into model predictive control has allowed for significant progress in power electronics, but switching frequency reduction, computational burden reduction, automatic selection of weighting factors, and novel control objective selection problems still exist. Therefore, the research focus of this thesis will largely be related to closing these current knowledge gaps.

In Figure 2.31, a general model predictive control block diagram for inverters is given. In this figure, inverters can adopt arbitrary topologies. The general load application shown in the figure can be motor, grid or some other active or passive load. In this method, $i(k)$ is the measured current value, and $i(k+1)_p$ is the predicted value of current calculated by the prediction model. Then, the cost function is used to evaluate these predicted values, taking into account the reference value $i(k)_r$ and the corresponding constraint. The optimal operation (S_a, S_b and S_c) are finally selected and applied to the inverter.

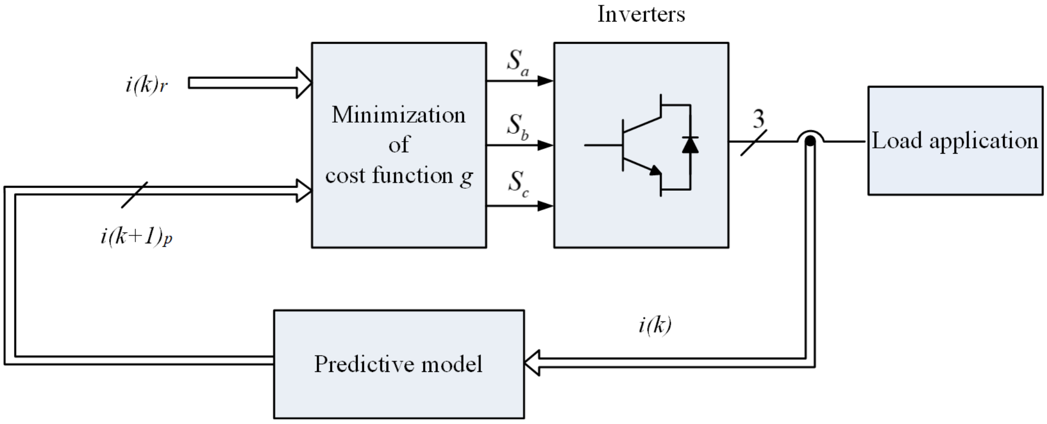


Figure 2.31: A general model predictive control block diagram for inverters.

The Development of MPC

The modern control theory was developed in the early 1960s and gradually perfected, with the subsequent development of the optimal performance index and the precise system design method [22], which obtained remarkable achievement in aerospace. However, when the modern control theory applied to industrial process control, it did not have the same desired effect. In investigating its reasons behind this, modern control theory was seen to be based on accurate model parameters, while industrial processes generally involve nonlinearity, time variability, strong coupling, and uncertainty. Consequently, it is difficult to obtain accurate mathematical models, and the control effect is therefore significantly reduced. Faced with this issue of incongruity between theory development and practical application, people began to examine the characteristics and requirements of industrial process control and explore the high-quality control method, which did not need a high accuracy mathematical model. Model predictive control in this context resulted in a new type of control algorithm. Once available, it achieved great success and developed rapidly in the oil and chemical industry and the field of aerospace [22]. It can be seen that the emergence of predictive control is not the product of some kind of theoretical research, but it was developed as a kind of effective control method to be applied to industrial practice. Model predictive control used in current industrial applications, such as oil and gas industry, distillation columns for crude oil separation, continuous digester of cellulose fibre or pulp and flotation machine [22].

Nowadays, model predictive control is widely used in various industrial production processes, aerospace, oil refining, and petrochemical and pharmaceutical production. However, it is unfortunate that the application of model predictive control is not very popular in all industrial fields; the proportion of the model predictive control software market being quite small. This is mainly due to the fact that the existing model predictive control methods applied to the professional field are narrow. In addition, most of these softwares embedded in the research and development unit dedicated platform, and it has been difficult to extend this to other platforms. In light of these issues, scientific researchers, with regard to specific industrial applications, put forward the economic, practical, and reliable model predictive control algorithm. This algorithm has since proven to be significant due largely to its effect on computational burden.

Thanks to the rapid development of microprocessors and digital signal processors, model predictive control had already been widely studied and applied in process industries for decades. Now, it is being considered in other areas, such as power electronics and drives. Model predictive control primarily uses a model of the system to predict the future behaviour of the controlled signal [20]. Before model predictive control was applied to power electronics, PID (proportional-integral-derivative) controllers were also largely used due to the modeless nature of controlled objects and the advantages of easily adjustable parameters [83], and were also considered a universal controller in industrial process control. Nevertheless, PID controllers also have some key drawbacks. In large engineering applications, although a PID controller can maintain high efficiency regulation in a single-loop system [84], it is difficult to ensure the global performance of the system on account of a lack of coupling information when the single-loop system extends to a multi-loop system. Furthermore, PID makes it difficult to assess the constraints of input and the intermediate and output variables in a multi-loop system [84]. With the development of industry, high requirements (multivariable and multiple constraints) are proposed for an industrial optimisation control system; thus, it is a clear that a PID controller cannot meet these kinds of requirements.

The Fundamental of MPC

MPC is a kind of process control strategy in which its principal objective is to solve an optimisation problem for each sampling period [85]. In order to control the current sampling period, it needs to implement the control function in the current sampling period while repeating the optimisation for the next sampling period. This optimisation problem is solved by taking by specific control objectives. In detail, it is realised by taking the cost function minimum value to determine the future control function according to the control objectives and requirements [19]. Figure 2.32 shows MPC control trajectories in the past and future.

The main characteristic of predictive control is the use of the system model to predict the future behaviour of the controlled variables through a prediction horizon [21]. In general, model predictive control uses the control action by minimising a cost function to describe the desired system behaviour. The cost function can then compare a reference with the predicted outputs computed by the system model. In fact, model predictive control solves an open-loop control problem by providing a feedback loop and potential robustness with respect to system uncertainties, by repeating in a receding horizon at each sampling period.

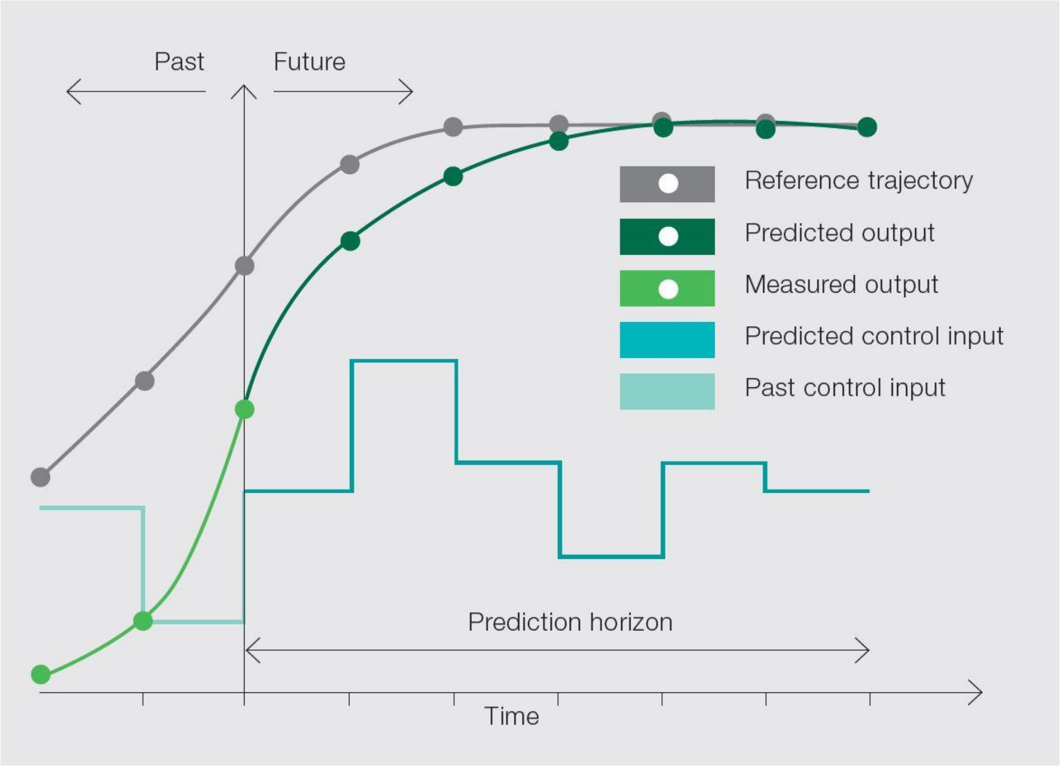


Figure 2.32: MPC control trajectories in the past and future [source: new.abb.com/model predictive control]

Model predictive control comprises the following three essential elements [20]:

- Prediction model: The prediction model is the fundamental characteristic of model predictive control. The prediction model form is not fixed, but must be able to reflect the dynamic state process of a controlled system accurately.
- Dynamic optimisation: Model predictive control calculates the optimal solution for the performance metrics which contain the controlled state variables. Performance indexes are set by the system's control target, which can be easily realised by changing the performance index of different control objectives, which dramatically increases the flexibility of the model predictive control. However, model predictive control of the local optimisation of optimisation control is limited to the time domain, not the global optimal; thus, the rolling optimisation process ensures that the system run eventually has an optimal tendency.
- Feedback correction: Model predictive control is a closed-loop control method, which can determine the optimal control signal in the time domain through rolling optimisation. In order to prevent interference or failure of the system state, the model predictive control just uses the current period of the control sampling signal. When it enters the next sampling period, the controller first corrects the predicted value, which is then followed by optimisation of the control signal.

Given the above, predictive control is popular in power electronics, which can be divided into four categories, according to their controlled variables: model predictive control (MPC), trajectory-based predictive control, hysteresis-based predictive control, and deadbeat control [21]. Figure 2.33 summarises the classification of different predictive control methods according to a predefined optimisation criterion. The predictive controller then uses this criterion to obtain the optimal actuation. For model predictive control, the cost function is used as the optimisation criterion to be minimised [20]. The controlled signal within the boundaries of the hysteresis area is used as the optimisation criterion in hysteresis-based predictive control [86], while the controlled variables are kept to follow a predefined trajectory in trajectory-based predictive control [87]. In deadbeat control, the optimal actuation is similar to the MPC, which renders the error equal to zero in the next sampling period [88]; however, deadbeat control requires a modulator and has a fixed switching frequency [21]; and the fact that it cannot include constraints must also be considered [21]. Model predictive control with a finite control set, trajectory-based predictive control and hysteresis-based predictive control can directly generate the switching signals for the power converters and will present a flexible switching frequency [21]. However, model predictive control with a continuous control set and deadbeat predictive control needs a modulator to generate the required voltage, which will result in having a fixed switching frequency.

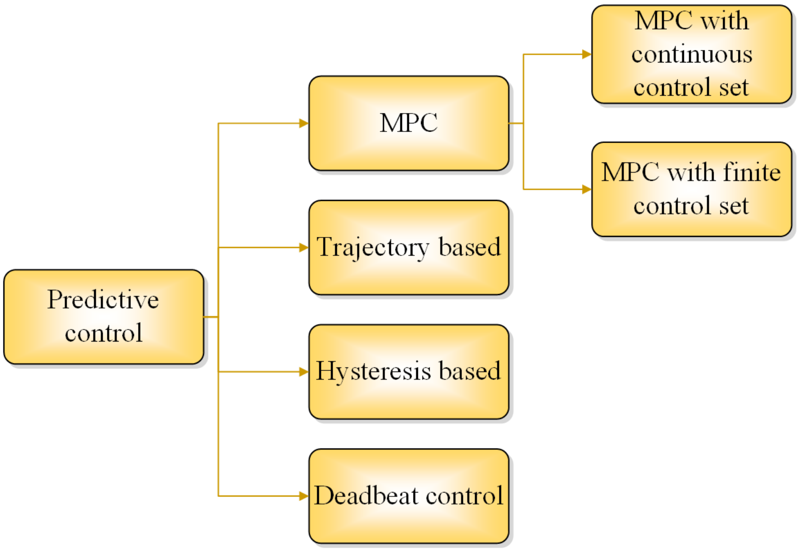


Figure 2.33: Predictive control methods for power electronics [21]

The main advantages of model predictive control are its fast response, the nature of its hybrid model (linear and nonlinear), its ability to include constraints in its variables and intuitive concepts [20]. With regard to the advantage of its fast response rate, MPC can achieve a faster response than the cascaded structure [89], which is mostly used in linear control systems. In order to avoid linearising the model at a fixed operating point, MPC can be modelled as nonlinear, thus improving the performance of the operating system. When designing a controller, it is also possible to include constraints and restrictions in variables; thus, the preponderance can easily be obtained in model predictive control, whereas it is hard to gain through deadbeat control. Furthermore, the concepts of model predictive control are intuitive and simple as it uses a model of the system to predict the future behaviour of the controlled variables.

A new control strategy chapter of the modern power electronics system was revealed when a finite control set model predictive control was put forward in [82][85]. MPC begins with the discrete characteristic of power electronics and uses the cost function to evaluate the control variables. It then minimises the cost function during the w-hole sampling period. In contrast to conventional PI (proportional-integral) and PR (proportional-resonant) control methods, it has the following advantages: fast response, multiple constraints and no PWM (Pulse Width Modulation) module; thus, it is now regarded as a universal advanced control algorithm in power electronics.

However, the main drawback of model predictive control is its computational burden. Digital microcontrollers, such as dSPACE and FPGA (field-programmable gate array), can now meet the requirements for large calculations during small sampling periods due to recent improvements. At the same time, these digital platforms can also be successfully applied to the control of power electronics. From these developments, the technology of predictive control has since developed rapidly and a significant amount of relevant literatures have been produced.

Model predictive control, especially finite control set model predictive control, has drawn significant attention due to the fact that it is suitable for power converter control. A power converter system is nonlinear and has a finite number of switching states. Meanwhile, some constraints and limitations such as maximum output current or capacitor voltage balance may also be added. Model predictive control allows for the easy implementation of these requirements, because it has the characteristics of discrete time implementation and can build a hybrid model. In addition, it can run fast on a digital control platform. In the following section, model predictive control will be reviewed with regards to three key aspects: the classification of MPC depending on the different control sets, the applications of MPC and the existing problems within MPC in power electronics.

Depending on the differences in control sets, there are two main categories for model predictive control: MPC with a finite control set and MPC with a continuous control set [21]. The classification of MPCs is shown in Figure 2.34.

This classification is based on the process type of the optimisation problem. An MPC with a continuous control set handles a continuous control signal and then uses a modulator to generate the desired output voltage for power electronics and drives [90]. The main benefit of an MPC with a continuous control set is that it allows the user to obtain a fixed switching frequency [91]. In general, two main MPC controllers are featuring continuous control set methods: generalised predictive control (GPC) [92] and explicit

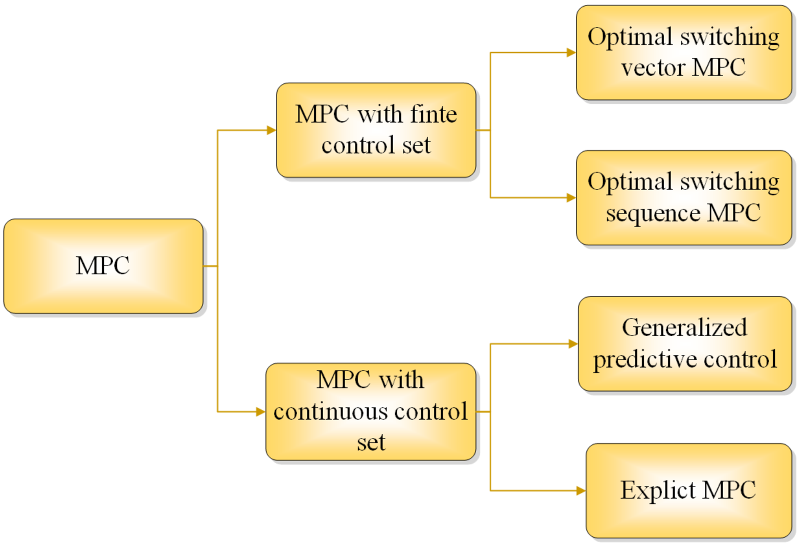


Figure 2.34: Classification of MPC [22]

model predictive control (EMPC) [93]. GPC can be used for long prediction horizons and online solutions and is therefore usually used for linear and unconstrained systems. It should be noted that the main problems of both GPC and EMPC are in expressing the complex formulation of the MPC problem.

The discrete nature of power converters can be considered by an MPC with a finite control set. As such, an MPC with a finite control set (FCS-MPC) does not require an external modulator [94], while an MPC with an optimal switching vector only calculates predictions for this control set, which makes the formulation of an MPC method highly intuitive. Furthermore, an MPC with an optimal switching sequence considers a limited number of possible switching sequences per switching period [95]. Therefore, when comparing these two methods, an MPC with optimal switching sequences method has higher computational cost than an MPC with optimal switching vectors [95].

Operating Principles of Model Predictive Control

The basic operating principles of model predictive control are: building a mathematical system model for system prediction, representing the constraint requirements and desired behaviour of a system by employing the cost function, and minimising the cost function to obtain the optimal actuation. The mathematical model for system prediction is a discrete time model, which can be indicated as a state-space model given by:

$$x(k+1) = Ax(k) + Bu(k) \tag{2.50}$$

$$y(k) = Cx(k) + Du(k) \tag{2.51}$$

In these two equations, u, x and y represent input, state, and output variables, respectively. Equation 2.52 denotes the cost function which can describe the desired behaviour of the system, such as current error, torque error, and power error, as well as the references, future states and actuation, and N denotes a predefined horizon. In each sampling period, through minimising the cost function the model predictive control obtains a control action sequence, but only the first element of this control action sequence is applied to the system in Equation 2.53. The model predictive control algorithm therefore offers potential robustness and a feedback loop in regard to system uncertainties via the method of repeating in a receding horizon at every sampling period [22]. Through this method, the controller uses the new measured data and gains a new sequence of optimal actuation each time when solving the optimisation problem for each sampling period.

$$J = f(x(k), u(k), \ldots, u(k+N)) \tag{2.52}$$

$$u(k) = [1, 0, \ldots, 0]\, arg\, min_u\, J \tag{2.53}$$

Figure 2.32 describes the working principle of model predictive control. The prediction can be made up to $k + N$ in the horizon of time using the system model and the available measurements until the time k. The optimisation process is repeated with these measurements each time [96].

Cost Function

Model predictive control implements the cost function to obtain the desired system behaviour by comparing the reference values and the predicted values. Cost function has any form, but usually it can be written as:

$$J = \sum_{i=1}^{m} K_i f_i(x) \tag{2.54}$$

In this equation, J expresses the cost function. m is the total number of control objectives. $f_i(x)$ represents the cost function of each item and K_i is its corresponding weight factor [22].

Applications of MPC

The use of MPC across varied power electronics applications will be reviewed in this section. As for DC-DC topology [97], MPC is applied to control a buck-boost topology for the DC side in a photovoltaic (PV) system to improve the efficiency of the PV system.

With regards to AC-AC topology, MPC is mainly applied to matrix converter-fed PMSM (permanent magnet synchronous motor) [98][99][100], direct matrix converters [98]-[101], indirect matrix converters [102], and fault diagnosis in matrix converters [101][103]. However, the computational burden is an ongoing issue for model predictive control. [98] uses a lookup table to activate computational efficiency for matrix converter-fed

PMSM on the basis of reducing the redundant voltage vectors. Similarly, [99] simplifies MPC to reduce computational burden in matrix converter-fed PMSM. [100], on the other hand, uses a speed MPC method to control speed and currents, which reduces oscillations and improves dynamic response. [101][103] both focus on an open-switch fault-diagnosis strategy for a matrix converter; however, they approach different control variables. The former used load current, whilst the latter employs error voltage.

For AC-DC topology, MPC is used in single-phase cascaded H-Bridge rectifiers [104], active rectifiers [105], five-level bidirectional converters [106], and AC-DC-AC converters [107][108]. In [104], MPC was seen to reduce the heavy computational burden and improve steady-state current performance in a single-phase cascaded H-Bridge rectifier. In [105], MPC was successfully applied in a single-phase seven-level active rectifier, which enables power conversion with a unity power factor. A five-level bidirectional converter , which is connected to the grid through a second-order LC (inductor and capacitor) passive filter operating as an active rectifier and as a grid-tie inverter, was also controlled by MPC in order to achieve high efficiency and a lower current THD (total harmonic distortion) [106]. For [107] and [108] with AC-DC-AC topologies, [108] put forward a simple and high performance controller based on MPC for AC-DC-AC power conversion using nine-switch topology, whereas [107] places emphasis on faults occurring in the converter, especially with regards to a five-leg converter.

For DC-AC topology, MPC is also widely used. In [109], MPC was used in the combination of modulated optimal vector and finite control options for a three-phase inverter with an LC filter, which was able to demonstrate increased robustness to parameter uncertainties and faster responses. In [110][111], MPC was applied to NPC inverters and cascaded H-Bridge inverters, respectively. In [110], DC-bus voltage was also controlled by MPC, which was conventionally governed by a PI-based control loop. [111] proposes a long prediction horizon MPC formulation for cascaded H-bridge inverters, and the formulation in [111] showed low current distortion and was able to minimise the common-mode voltage and the symmetry of inverter voltages. Due to variable switching frequency in conventional MPC, [112][113] improved MPC with fast and fixed switching frequencies; however, the multiple constraints in the cost function feature, as well as the complexity of a control method, was lost. In addition, MPC is widely used in inverter-based electric machines: PMSM drives [114], induction motors [115] and disc coreless permanent magnet synchronous motors [116]. Overall, the above literature review shows that MPC has achieved great success over a range of different applications and power converter topologies.

Existing Problems within MPC

Although MPC has achieved great success in the field of power electronics (as demonstrated in the previous section), some research problems still remain. Accordingly, this section will detail these problems, including switching frequency reduction, computational burden reduction, automatic selection of weighting factors, and novel control objective selection.

Switching Frequency Reduction

One research problem in model predictive control is lowered switching frequency [30][117]. A higher switching loss will be caused by a higher switching frequency [26][27]. A significant factor to consider in enhancing multilevel inverters efficiency is the lowering of the switching frequencies. They are currently renowned for having high switching frequencies which ultimately cause energy loss through the power semiconductors. This feature restricts the effectiveness of MPC methods, particularly in relation to medium-voltage high-power systems. The high switching frequency will also generate heat, and this heat will have a negative effect on the lifetime of the switches [28]. Moreover, the higher switching frequencies may also lead to lower reliability in the control behaviour of more complex systems [29].

This issue has been investigated by [26][27][30]. A model predictive direct power control technique was employed in [26], in which grid-connected voltage source converters were laden with two cost functions (steady-state and transient-state). The use of both cost functions can lessen the switching frequency in steady-state conditions, and also allow for a quicker reaction if transient state occurs. Meanwhile, when this method is extended to 3-level NPC inverters, the DC-link capacitor voltage fluctuation problem is not considered in the proposed voltage controller of this algorithm. Furthermore, in another approach [27] two-step MPC algorithm for 2-level grid-connected inverters was recommended for use in photovoltaic systems. This approach could limit the switching frequency whilst simultaneously enabling flexible power regulation. In [30], a graph algorithm was employed in one existing MPC-based approach when using high-power voltage-source inverters to choose the most suitable voltage vectors. This approach used in 2-level voltage source inverters was able to reduce the switching frequency. This can generate 70% reduction in switching frequency over linear control methods when used collaboratively with pulse width modulation. In 2-level inverters, eight possible voltage vectors make it easy to find the graph algorithm; however, when this method is extended to multilevel inverters, the graph algorithm is challenging to be determined because no mathematical guideline is provided. Nevertheless, the above methods all increased the complexity and computational burden of the system and did not consider the DC-link capacitor voltage fluctuation problem. Therefore, the topic is still one of debate, regardless of the current techniques proposed for lowering the switching frequency.

Computational Burden Reduction

The reasons why the computational burden for MPC is so high have also been explored as it often results in a considerable burden on the digital controller. At present, researchers are attempting to reduce the number of control sets, the number of predictions, and the number of optimisations.

A previous study [118] proposed an MPC simplification algorithm that reduces the number of control sets. [118] also implemented a reduction in switching redundancies to reduce the computational burden. Because the switching redundancies are defined by the different switching combinations that produce the same output voltage per phase, this was able to reduce the alternative voltage vector control set significantly. However, this method may also delete the optimal control variables, and the alternative control set may not contain the optimal control variables, thus affecting the control performance. A second study [119] focusing on modular multilevel converters used a submodule (SM) capacitor voltage balancing controller to reduce the calculation burden of the MPC. In this case, the proposed MPC algorithm determined the number of inserted and bypassed SMs within each arm of the MMC, while the sorting algorithm was used to keep the SM capacitor voltages balanced. Using this strategy, only the summation of SM capacitor voltages of each arm was required for control purposes, which simplifies the communication among the SMs and the central controller. Although this method reduced the calculation load, the impact of each predictive controller on the other control variables was not investigated. As the control variables depend upon each other, this method also did not provide the flexibility of maintaining a trade-off among AC-side current tracking error, minimising circulating current and capacitor voltage ripple. [120] applied a specialised sector distribution method to reduce the computational burden. Without modulation in the general MPC, the applied vectors behaved somewhat like how vectors did in space vector pulse width modulation (SVPWM). This implied the possibility that the prediction and optimisation in a sampling period were not necessary for all the possible vectors in steady-state operation. For the above reasons, the number of the voltage vectors used for prediction and optimisation in the general MPC can be reduced to a subset of adjacent vectors with the sector information of the rotating voltage space vector. The limitation of [120], however, was that it did not provide the mathematical guideline for the candidate vectors for each sector; therefore, it is hard to generalise the findings to multilevel converters with more levels.

Compared with conventional MPC, the existing MPC algorithms for reducing the computational burden have several limitations. Furthermore, they are only suitable for use with an accurate model that is sensitive to changes in the system model parameters as well as the sampling period, which increases the chances of finding the optimal voltage vector. Moreover, with the development and use of multilevel converters, the computational complexity of MPC-based control systems will also increase, and the existing algorithms may not be able to meet the actual needs of the industry. With the continuous development of digital controllers, combining MPC controllers with digital signal processing (DSP) and field-programmable gate arrays FPGA is another research direction for realising fast MPC. In fact, as studies [121][122] were able to achieve better control based on MPC by combining it with FPGA.

Automatic Selection of Weighting Factors

Moreover, the MPC approach has the capacity to tune the weighting factors, and this is a further benefit to consider. Due to the absence of a rigorous design methodology in this area, the optimisation of weighting factors is a subject of rapidly-growing research attention [22][34]. Currently, it is very challenging to identify appropriate weighting factors for specific system behaviours. Actually, the methodologies most frequently adopted depend on trial-and-error testing to measure the impacts of weighting factors [22]. A number of guidelines have been put forward that are developed according to branch-and-bound algorithms [34], and these may be able to eliminate the requirement of such trial-and-error testing. Meanwhile, [34] proposed allocation principles for the weighting coefficient in that it used the weighting method to deal with multiple objectives. In addition, another study [123] suggested an optimised weighting coefficient configuration method for a specific application. This method calculated the torque ripple to obtain the weighting factor that minimised the ripple, thereby suppressing it. In [123], the conventional weighting method was abandoned, and the concept of average ordering was adopted to control the unweighted coefficients for two control targets, namely, the torque and flux linkage of the induction motor. This method is not only simple but results in good control performance. However, it is only suitable for systems with these two specific control targets. Nonetheless, the fact remains that the approach will require an effective method for identifying suitable weighting factors. Now, an automated selection process developed according to genetic algorithms is suggested [35]. This will, however, be a long drawn-out process given that a set of simulations must be tested for each design objective. To allow for weighting factors in the cost function to be automatically identified, an artificial neural network (ANN)- based approach was proposed [36]. Such an approach may facilitate quick and effective optimisation of weighting factors. Nevertheless, data from big simulations are needed by ANNs during the initial training process. This process of choosing suitable weighting factors in the cost function thus continues to be a challenging topic in the field of MPC power electronics converters [36].

Novel Control Objective

MPC techniques can resolve issues of optimisation through the use of a control signal. Since the behaviour required by the system is represented in the cost function, MPC can reach optimum actuation through the lowering of the cost function. Prior research that has implemented control objectives in cost functions of NPC inverters is outlined in Table 2.6. Such control objectives show that voltage, current, power, torque and flux are implemented.

The broad applicability of MPC is attributable to the increased flexibility of its control objectives. An overview of the control objectives for the NPC inverter system is available

Table 2.6: Control Objectives in Cost Function of MPC

Application	**Reference**	**Control Objectives in Cost Function**
Resistor-inductor load	[124]	Current
Grid-connected system	[125]	Power and capacitor voltage
	[126]	Power
	[127]	Voltage
	[128]	Current and capacitor voltage
Induction motor	[129]	Torque and flux
Wind turbine system	[130]	Torque, current, power and capacitor voltage

in Table 2.6. These control objectives have only one constraint. As different constraints have different physical implications, when multiple constraints are present in the cost function, a coupling effect may be induced. Changing the control coefficient of a specific constraint may also cause the performance of the other control variables to decrease. Generally, the forms of control objectives are relatively simple and fixed, and other constraints are not added without considering the control performance comprehensively. Furthermore, in conventional MPC, standalone calculations are performed for the control objective during each sampling period, and there is no correlation between the optimal control objective for adjacent sampling periods. The optimal value for each control period refers to the optimal local value, and there is no guarantee that different cycles will yield the same optimal value. However, the challenge that remains is improving the control performance of MPC by defining the novel control objective with a new mathematical structure and physical meaning such that one can establish the correlation between the optimisation processes of the different control cycles. This, in turn, will help improve the control performance of MPC.

2.4 Applications of Multilevel Inverters

Multilevel inverters are extensively used in industry and have been since their introduction. There are four primary applications for multilevel inverters, as set out below:

- Power supply usage: A power inverter can transfer a DC electricity source (for example, a fuel cell or battery) to AC power, which can be produced at the required voltage level. An uninterruptible power supply (UPS) is also a ubiquitous electrical device that can provide emergency AC power to a load when input power is not available [42]. Many data centres, computers, and telecommunications use UPS to protect their equipment since power disruption would cause data loss or economic loss.
- Electric motor drives in rail traction, ship propulsion, electric vehicles, and industrial automotive applications: A power inverter can convert a full range of output

voltage levels for electric motor drives. With the development of modern industry, numerous industrial applications use medium-voltage supplies, especially rail traction and ship propulsion, which have begun to demand a high power range, high performance and high speed [50]. As per usual, high switching frequencies are needed to achieve high speed; however, multilevel inverters are used in these applications to achieve an apparent higher frequency, which cannot increase the application average switching frequency.

- Power distribution control and management applications in power systems: Currently, flexible AC transmission systems (FACTS) play an essential role in enhancing controllability and increasing the power transfer capacity [131]. FACTS technology methods include the active filter (AF), dynamic voltage restorer (D-VR), static synchronous compensator (STATCOM), unified power flow controller (UPFC), and unified power quality conditioners. These can provide support for voltage stability through their flexible and instantaneous compensation for power fluctuations [132].

- Renewable energy generation and transmission: Renewable energy sources such as wind, solar and hydropower have been the focus of intense development in many countries over recent decades. For the generation of wind energy, the multilevel inverters, especially the back-to-back 3-level neutral point clamped inverters (NPC inverters), have become the most researched topology [133]. Due to the decoupling of the generator and grid, the 3-level NPC inverters can obtain maximum power through generator side control and can regulate reactive and active power through grid side control. Given the rapid development in renewable energy generation, this review will provide some specific applications for renewable energy generation (the grid-tie solar power system, hydropower energy system and HVDC transmission system) in the following content.

  Solar energy generation and transmission systems are classified into two types: the grid-tie system and the off-grid (standalone) system. Power inverters provide an interface between the power energy which is produced by the photovoltaic (PV) array and the power grid or specific applications. Use of the grid-tie system, which is now producing megawatt levels of power, has undergone rapid expansion [134]. The traditional 2-level inverter has therefore been unable to deliver the high-quality power, high switching frequency, high-voltage operation and filter size reduction that the multilevel inverter can supply. Figure 2.35 shows the neutral point clamped (NPC) multilevel inverter for the grid-tie solar power system.

  Figure 2.36 illustrates a back-to-back active neutral point clamped (ANPC) multilevel inverter for hydropower energy system and shows the large energy generation and transmission system [135]. This extensive hydropower system not only pumps water from oceans, lakes or rivers to reservoirs on higher ground but also uses the flowing water from a higher reservoir to a low-lying position to generate electricity.

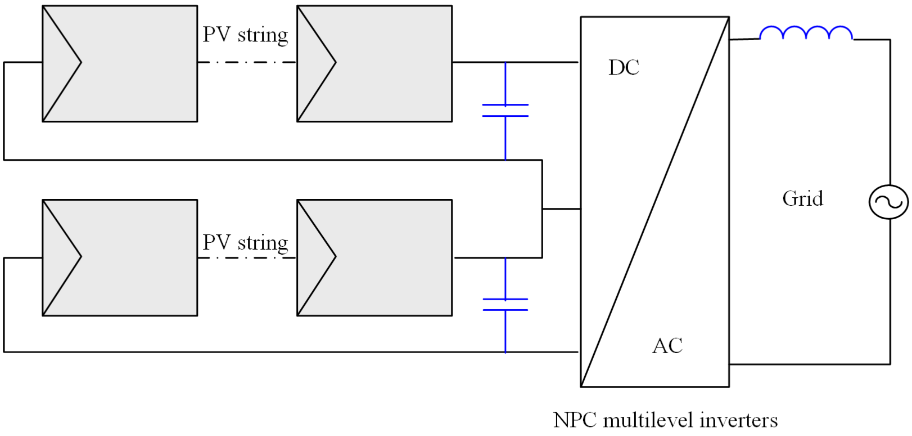


Figure 2.35: CHB inverters and NPC inverters for the grid-tie solar power system [50]

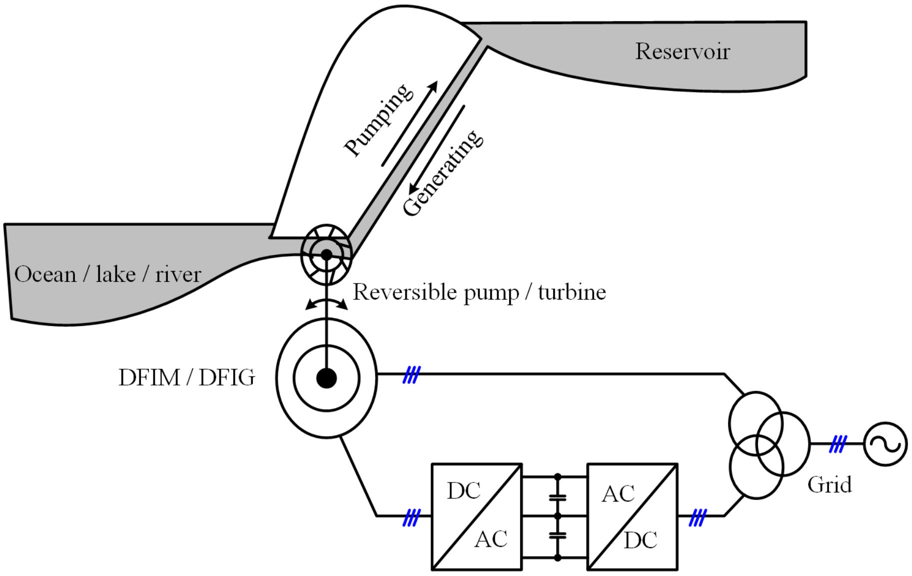


Figure 2.36: ANPC multilevel inverters for hydropower energy system [50]

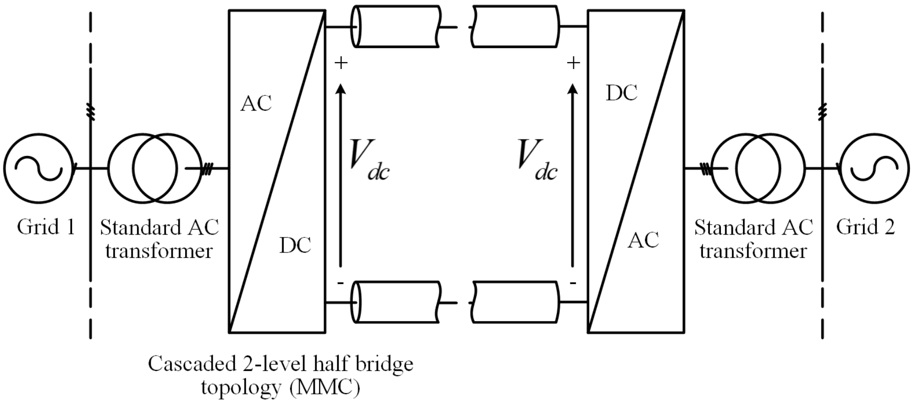


Figure 2.37: A graphical depiction of an HVDC transmission system [50]

High voltage direct current (HVDC) transmission was originally developed in Sweden. It is commonly used for transmitting offshore wind power, transmitting hydro power to significant power centres, decoupling large AC power networks and dynamically stabilising AC networks [136]. A graphical depiction of an HVDC transmission system is given in Figure 2.37. An input of AC power is rectified to produce a high-power DC output between the sending and receiving sides. On the receiving side, a 2-level half-bridge modular multilevel converter (MMC) inverts the high DC power back to AC power.

2.5 Summary

In this chapter, a review of necessary DC-AC inverters and multilevel inverters, modulation and control strategies multilevel inverter applications was conducted. Furthermore, two major issues were raised through the review of multilevel inverters, which concerned topologies and control algorithms. Recently, many new topologies have been developed; however, only a small number of these topologies have practical industrial applications. This is because cost and manufacturing are two factors that must always be taken into account when considering industrial production, and new topologies are always complex and not easy to build. When industry adopts a new topology, all applications related to the new topology require modifications. Therefore, updating the control algorithm seems a more efficient way of achieving high performance using multilevel inverters compared with developing new topologies. Moreover, the promotion of the control algorithm can significantly affect the arrival of a new topology. Thus, this thesis was devoted to investigating control methods for multilevel inverters.

Through the review of multilevel inverter topologies, the neutral point clamped inverter topology was selected for the research application because of its wide application in industry. As for the modulation and control method, modulation techniques (pulse width modulation, sinusoidal pulse width modulation and so on) and linear control based on a time-average model with modulation were firstly applied in the control of inverters. However, the main challenge for these methods is the issues arising from the hybrid nature of the power inverter system when using semiconductor components as power switches. However, thanks to the development of the fast microprocessor and digital signal processors (DSP), some novel control methods such as hysteresis current control, sliding mode control and model predictive control (MPC) can now be applied to power inverters. Among these methods, model predictive control stands out for its fast response, multiple constraints control in a single control loop, and the advantages of its simple and intuitive implementation of nonlinearities. Nevertheless, some research problems of model predictive control still exist, which include switching frequency reduction, computational burden reduction, weighting factors design problems, and novel control objective design. Therefore, in aiming to solve these problems, this thesis proposes novel MPC algorithms to improve the energy efficiency for 3-level NPC inverters.

Chapter 3

Model Predictive Control of 3-level NPC Inverters with Reduced Computational Burden

A novel model predictive control (MPC) algorithm with reduced switching frequency for Neutral Point Clamped (NPC) inverters is proposed in this chapter. The proposed method can be used to reduce switching frequency through optimising switching sequences while keeping the advantages (such as fast response and handling multiple constraints) of conventional MPC methods. The performance of the method is verified by simulation results with 3-level NPC inverters. In order to reduce the computational burden, two additional extended MPC algorithms are proposed: a multistep model predictive control (MMPC) algorithm and a model predictive control algorithm for grid-connected NPC inverters.

3.1 Introduction

In recent years, multilevel inverters have drawn extensive attentions from both academia and industries due to an increasing number of high-power applications and the integration of renewable resources into the grid [2][9]. Among different topologies of multilevel inverters, the neutral point clamped (NPC) inverters have attracted great interest for its ability to split DC-link voltages, reduce switching losses, and produce smaller output current ripples [12][13].

The main challenge to modulating and controlling NPC inverters is that the entire system is nonlinear due to the utilisation of power switches. Conventional approaches are mainly based on the average state-space modelling and related modulation techniques such as pulse width modulation (PWM), and sinusoidal pulse width modulation (SPWM). However, the limitations of these conventional methods are obvious. The model must be linearised based on a specific operating point [16]. The tuning procedure of the controller is complex, and this complexity increases yet further when the operating point is adjusted. Due to the development of the fast microprocessor and digital signal processors (DSP), some novel control methods such as hysteresis current control, sliding mode control, and model predictive control (MPC) have been applied to NPC inverters. Among these methods, MPC stands out for its fast response and ability to handle multiple constraints [21], and MPC has achieved great success in power electronics applications [19][22].

However, one research problem of model predictive control is switching frequency reduction [30][117]. Higher switching frequency will lead to higher switching loss [26][27]. At the same time, the lifetime of switches will be reduced by a high switching frequency. Moreover, it may lead to unreliability in the control behaviour for more complex systems [29]. Therefore, in aiming to solve this problem, this chapter proposes the first MPC algorithm with the optimisation of switching sequences to reduce switching frequency through the prediction of switching times for different voltage vectors in a cost function.

Recent trends in the growth of renewable generation in the UK are shown in Figure 3.1. Instabilities in the power generation from renewable resources such as photovoltaics can lead to inverter systems being damaged by variations in the current. This chapter proposes a novel multistep model predictive control (MMPC) algorithm (the second MPC algorithm) for 3-level NPC inverters (in section 3.7) that is capable of solving this problem by considering current variation.

The development of MMPC algorithms has been complicated by a range of computational issues [137]. Large calculation burden demanded by MMPC algorithms requires high-performance micro-controllers. This significantly increases the cost for both experimental and practical applications. Several solutions have been proposed to address this problem. These include employing a sphere decoding algorithm as an optimiser [111][138] and adding modulators between the controller and the converter [139][140]. Whilst these are sensible approaches, they necessitate the use of extremely complex algorithms. [141] provides a way of simplifying the MMPC algorithm by introducing same space voltage vectors into the cost function.

The MMPC algorithm for a 3-level NPC inverter system proposed in section 3.7 builds upon the direct evaluation of the output voltage vectors by a three-phase inverters cost function suggested originally in [141]. To do this, the maximum current needs to be limited in the cost function. In section 3.7, the inverter is extended to 3-level NPC inverters and the output voltage vectors are made relative to the current through a mathematical model of the inverter. The cost function of the proposed algorithm

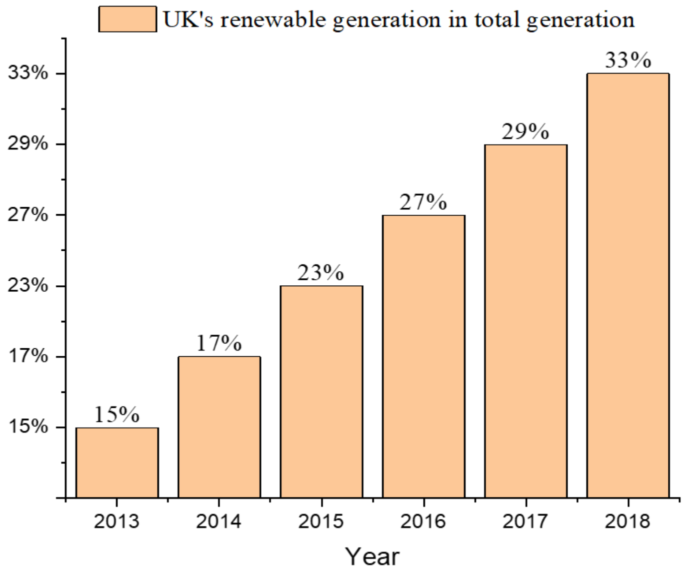


Figure 3.1: Growth trend in renewable power generation in the UK [source:GOV.UK renewables statistics collection].

evaluates the current to enable selection of the corresponding output voltage vector. As a result, the cost function does not treat the maximum current as a separate constraint.

Section 3.7 makes five primary contributions to MMPC development: 1) unlike conventional MPC algorithms and their one-time predictive horizon, the proposed algorithm is able to make multistep predictions. This decreases the THD of the output currents. 2) The proposed algorithm reduces the computational burden. An increased prediction horizon can result in large calculations. To deal with this, the proposed MMPC algorithm can reduce the number of calculations from 729 to 54 when compared to a conventional long-horizon MPC algorithm [142], a 93% reduction. 3) The proposed algorithm is extremely robust in handling of current variation. When the DC source is from renewable, such as photovoltaics or wind energy, it is unstable impacting the inverter system. 4) The MMPC algorithm combines current control and modulation in a single stage, thus, offering a solid alternative to conventional control schemes such as PI controllers. The controller manipulates the inverter switching patterns, obviating the need for a modulator. 5) Unlike other MPC algorithms [21][82], this algorithm does not require weighting factors to tune in the cost function.

The second MPC algorithm in section 3.7 is based on multistep predictions to reduce the computational burden. It does not solve the computational burden in a one-step predictive horizon. Therefore, the third MPC algorithm in section 3.8, which is based on the first MPC algorithm, is proposed to solve this research problem. At the same time, the application is extended to 3-level grid-connected NPC inverters. The third MPC algorithm in section 3.8 is presented for grid-connected NPC inverters that can reduce the computational complexity involved in predicting currents. The proposed algorithm can assess the minimum cost function between 27 voltage vectors and expected voltage vectors so as to be able to select the most appropriate voltage vectors for NPC inverters. This can thus reduce the number of current predictions typically necessitated by conventional MPC algorithms by a factor of 27, thereby significantly reducing the computational burden. The proposed algorithm is fully tested in actual grid-connected NPC inverters, and the results clearly indicate its effectiveness.

This chapter is organised as follows: The problem formulation and modelling the load of 3-level NPC inverters are in section 3.2. Then, the proposed MPC algorithm for the 3-level NPC inverters is designed in section 3.3. The optimisation process is given in section 3.5, and the simulation results are indicated in section 3.6, including nominal operation, current variation, switching frequency reduction and comparison with an industrial PI controller. Two additional extended MPC algorithms are demonstrated in section 3.7 and section 3.8.

3.2 Problem Formulation

Figure 3.2 shows the configuration of three-phase NPC inverters connected to a resistor-inductor (RL) load. R and L stand for load resistor and inductor, respectively. i_a, i_b, and i_c represent the load currents of the three-phases A, B and C, respectively. For the DC-link terminal, V_{dc} is the input DC voltage. Each phase of the NPC inverters consists of four switches and two diodes. In any one phase, S_{a1}, S_{a2}, S_{a3}, and S_{a4} are the four switches, while D_1 and D_2 are the two diodes. The neutral point of the DC-link terminal connects with the two capacitors, C_1 and C_2. The operation of each switch for one phase is defined in Table 3.1. S_x expresses the switching device. x is phase, where $x = \{a, b, c\}$. ON and OFF express the switch conduction states turn-on and turn-off, respectively. In each phase of NPC inverters, the switch has three possible statuses: P, 0 and N. The values of these three possible states are +1/2 V_{dc}, 0 and -1/2 V_{dc}, respectively.

Table 3.1: State Definition for Each Phase

S_X	S_{x1}	S_{x2}	S_{x3}	S_{x4}
P($+\frac{1}{2}V_{dc}$)	ON	ON	OFF	OFF
0(0)	OFF	ON	ON	OFF
N($-\frac{1}{2}V_{dc}$)	OFF	OFF	ON	ON

In consideration of all the possible switching states in the three-phases, there are 19 different output voltage vectors generated by 27 switching states in Figure 3.3. Voltage vector V_0 has three redundant switching states and $V_1 - V_6$ have two redundant switching states. Others from V_7 to V_{18} have only one switching state. The 27 switching patterns

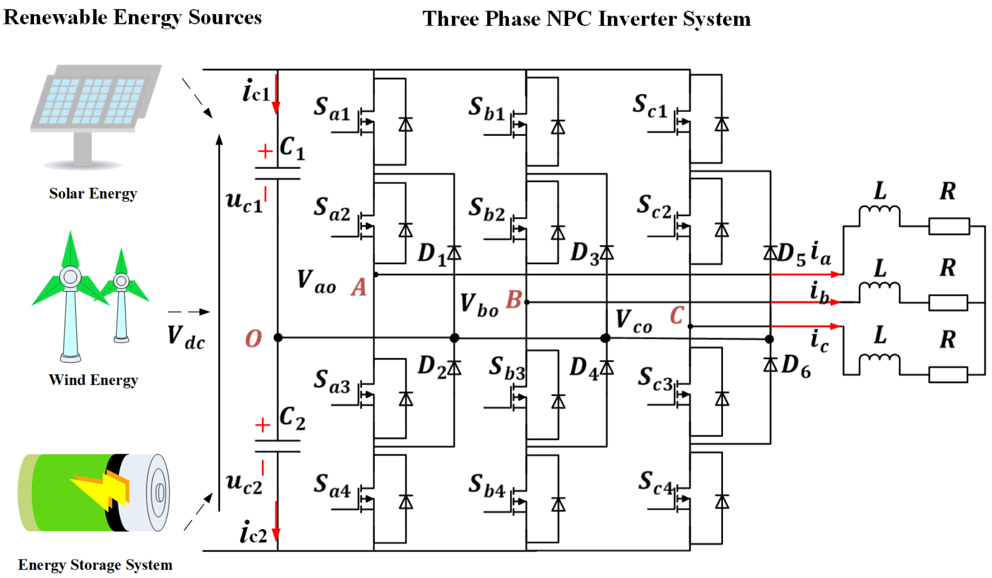


Figure 3.2: Circuit schematic of 3-level NPC inverters with passive RL load.

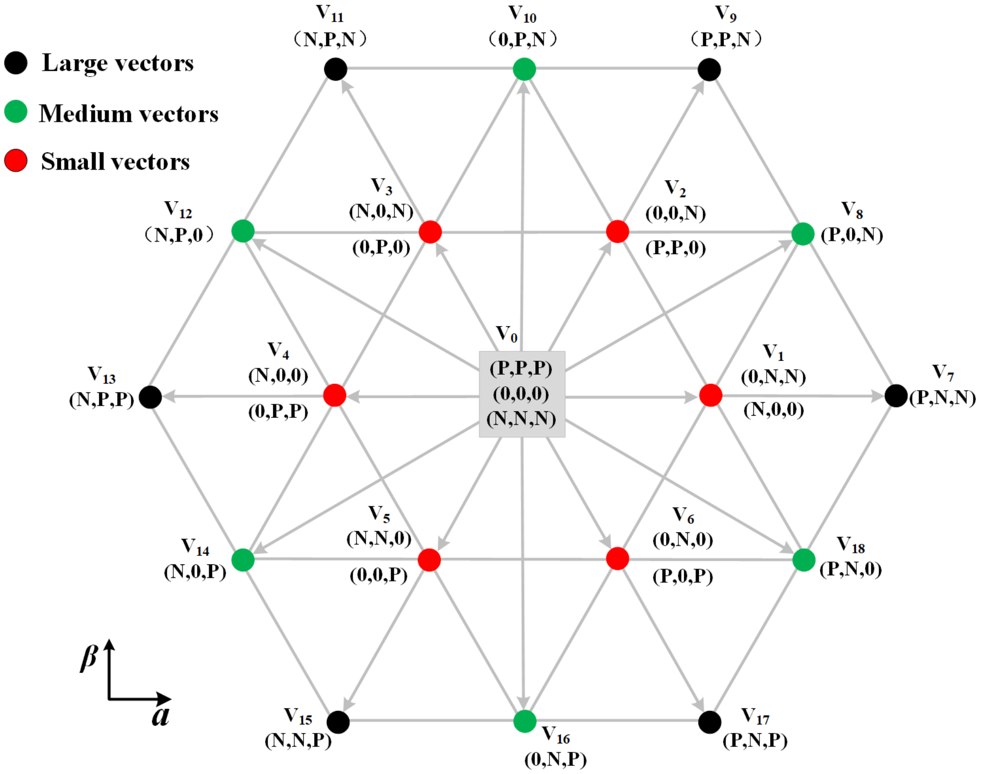


Figure 3.3: Space vector diagram for possible voltage vectors and switching states in NPC inverters

(SP) u_i, $i = \{1, 2, \ldots, 27\}$ correspond to the 19 voltage space vectors (SV) V_n, $n = \{0, 1, \ldots, 18\}$. On the basis of space vector definition, the space voltage vector:

$$V_n = \frac{2}{3}\left(V_{ao} + aV_{bo} + a^2 V_{co}\right) \tag{3.1}$$

where, the unitary vector a:

$$a = -\frac{1}{2} + \frac{\sqrt{3}}{2} j = e^{\frac{2\pi}{3} j} \tag{3.2}$$

V_{ao}, V_{bo}, and V_{co} are the output voltages. Table 3.2 provides the switching states corresponding to the voltage space vectors.

Table 3.2: Switching States corresponding to Voltage Space Vectors

Switching States (u_i)	**Voltage Space Vector** (V_n)
NNN 000 PPP	$V_0 = 0$
P00 0NN	$V_1 = \frac{1}{3} V_{dc}$
PP0 00N	$V_2 = \frac{1}{3} V_{dc} e^{\frac{\pi}{3} j}$
0P0 N0N	$V_3 = \frac{1}{3} V_{dc} e^{\frac{2\pi}{3} j}$
0PP N00	$V_4 = \frac{1}{3} V_{dc} e^{\pi j}$
00P NN0	$V_5 = \frac{1}{3} V_{dc} e^{\frac{4\pi}{3} j}$
P0P 0N0	$V_6 = \frac{1}{3} V_{dc} e^{\frac{5\pi}{3} j}$
P0N	$V_7 = \frac{\sqrt{3}}{3} V_{dc} e^{\frac{\pi}{6} j}$
0PN	$V_8 = \frac{\sqrt{3}}{3} V_{dc} e^{\frac{\pi}{2} j}$
NP0	$V_9 = \frac{\sqrt{3}}{3} V_{dc} e^{\frac{5\pi}{6} j}$
N0P	$V_{10} = \frac{\sqrt{3}}{3} V_{dc} e^{\frac{7\pi}{6} j}$
0NP	$V_{11} = \frac{\sqrt{3}}{3} V_{dc} e^{\frac{3\pi}{2} j}$
PN0	$V_{12} = \frac{\sqrt{3}}{3} V_{dc} e^{\frac{11\pi}{6} j}$
PNN	$V_{13} = \frac{2}{3} V_{dc}$
PPN	$V_{14} = \frac{2}{3} V_{dc} e^{\frac{\pi}{3} j}$
NPN	$V_{15} = \frac{2}{3} V_{dc} e^{\frac{2\pi}{3} j}$
NPP	$V_{16} = \frac{2}{3} V_{dc} e^{\pi j}$
NNP	$V_{17} = \frac{2}{3} V_{dc} e^{\frac{4\pi}{3} j}$
PNP	$V_{18} = \frac{2}{3} V_{dc} e^{\frac{5\pi}{3} j}$

From the three-phase NPC inverter load model in Figure 3.2, the following equation can be obtained [143]:

$$L\frac{di_x(t)}{dt} = V_{xo}(t) - Ri_x(t) \tag{3.3}$$

$$i_x(t) = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}, \; V_{xo}(t) = \begin{bmatrix} V_{ao}(t) \\ V_{bo}(t) \\ V_{co}(t) \end{bmatrix} \tag{3.4}$$

where, $x \in \{a, b, c\}$ represents the three phases.

The discrete time model can be obtained by applying a forward Euler approximation with sampling period T_s to the derivative.

$$\frac{di(t)}{dt} \approx \frac{i(k+1) - i(k)}{T_s} \tag{3.5}$$

Then, replacing Equation 3.5 in Equation 3.3, it can derive as:

$$i(k+1) = \left(1 - \frac{RT_s}{L}\right) i(k) + \frac{T_s}{L} V(k) \tag{3.6}$$

The dynamic equations of the capacitor voltages in DC-link are given in Equation 3.7 and Equation 3.8:

$$\frac{du_{c1}}{dt} = \frac{i_{c1}}{c} \tag{3.7}$$

$$\frac{du_{c2}}{dt} = \frac{i_{c2}}{c} \tag{3.8}$$

where i_{c1} and i_{c2} denote the currents flowing two DC-link capacitors C_1 and C_2. C is the capacitor value. The same approximation of the derivative can be applied to the capacitor voltages for a sampling period T_s, that is,

$$\frac{du_{c1}}{dt} \approx \frac{u_{c1}(k+1) - u_{c1}(k)}{T_s} \tag{3.9}$$

$$\frac{du_{c2}}{dt} \approx \frac{u_{c2}(k+1) - u_{c2}(k)}{T_s} \tag{3.10}$$

Then, Equation 3.9 and Equation 3.10 are substituted in Equation 3.7 and Equation 3.8. They can derive as:

$$u_{c1}(k+1) = u_{c1}(k) + \frac{1}{C} i_{c1}(k) T_s \tag{3.11}$$

$$u_{c2}(k+1) = u_{c2}(k) + \frac{1}{C} i_{c2}(k) T_s \tag{3.12}$$

where $i_{c1}(k)$ and $i_{c2}(k)$ are the currents flowing through the capacitor C_1 and C_2. Thus, the relation between capacitor current C_1 and C_2 and three-phase output current can be got:

$$i_{c1}(k) = i_{dc}(k) - H_{1a} i_a(k) - H_{1b} i_b(k) - H_{1c} i_c(k) \tag{3.13}$$

$$i_{c2}(k) = i_{dc}(k) + H_{2a} i_a(k) + H_{2b} i_b(k) + H_{2c} i_c(k) \tag{3.14}$$

In Equation 3.13 and Equation 3.14, i_{dc} is current in DC terminal, and H_{1x} and H_{2x} express switching state variables which are expressed as:

$$H_{1x} = \begin{cases} 1, & \text{if } S_x = P \\ 0, & \text{otherwise} \end{cases} \tag{3.15}$$

$$H_{2x} = \begin{cases} 1, & \text{if } S_x = N \\ 0, & \text{otherwise} \end{cases} \tag{3.16}$$

Equation 3.11, Equation 3.12, Equation 3.13 and Equation 3.14 are used for getting predictions for capacitor voltages from the present currents and voltages. For the sake of simplicity, the output currents of the NPC inverters are expressed as a current vector in using a stationary orthogonal $\alpha\beta$-framework [143]. Thus,

$$i = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.17}$$

$$T_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.18}$$

The output currents in $\alpha\beta$-framework can be expressed as follows:

$$i_\alpha = \frac{2}{3}(i_a - \frac{1}{2} i_b - \frac{1}{2} i_c) \tag{3.19}$$

$$i_\beta = \frac{\sqrt{3}}{3}(i_b - i_c) \tag{3.20}$$

Using the same $\alpha\beta$-framework transformation, the output voltage can be expressed in the same v_α and v_β form:

$$v_\alpha = \frac{2}{3}(v_{ao} - \frac{1}{2} v_{bo} - \frac{1}{2} v_{co}) \tag{3.21}$$

$$v_\beta = \frac{\sqrt{3}}{3}(v_{bo} - v_{co}) \tag{3.22}$$

The control objectives of the 3-level NPC inverters are reference tracking, neutral point balancing, and switching frequency reduction. Reference tracking means minimising the error between the reference current value and the predicted current value. As for the neutral point balancing, the objective is to balance the capacitor voltages, namely, minimising $|u_{c1} - u_{c2}|$. The voltage balancing is a critical issue for the NPC inverters as the unbalanced voltage may damage the power electronic components. The last control objective is to reduce the switching frequency of power switches. Higher switching frequency may generate some undesirable issues such as common-mode currents, electromagnetic interference (EMI), shaft voltages and bearing current [144]. Higher switching frequency will also lead to higher switching loss [26][27]. Moreover, it may lead to unreliability in the control behaviour for more complex systems [29]. Therefore, in the next section, the MPC controller is designed in terms of the above objectives.

3.3 Cost Function Design

In this section, a novel cost function is put forward. This new cost function is designed with a number of constraints, including controlling neutral point balance, maintaining capacitor voltage stability and output power stability, reducing switching frequency, decreasing switching loss, and limiting maximum current. In addition, this cost function also in a novel manner optimises the switching sequences to reduce switching frequency by predicting the switching times for the different voltage vectors in the cost function. In section 3.6, simulation results show good performance, when this novel cost function is applied to an NPC inverter system.

Model predictive control implements the cost function to get the desired system behaviour. Cost function is a most important part of model predictive control, because different designs of the cost function can reflect significant control performance. The flexibility of cost function makes model predictive control easily obtain multiple constraint requirements and be different from direct power control (DPC) [145] and direct torque control (DTC) [146], which are widely used for NPC inverter systems. In consideration of multiple constraints, they are always different units of measurements and different precision of requirements. For instance, the unit of capacitor voltage is *volt*, whereas the unit of output current is *ampere*. Besides, these multiple constraints even may have time-varying and conflicting characteristics, such as reducing the switching frequency and increasing the current control accuracy of the system.

In this section, a multifactor weighting method is used to build cost function, which reduces multiple constraint optimisation problems into a single cost function optimisation problem. The model predictive control strategy is carried out by optimising weighting factors of the cost function, instead of using the cascade control structure in DPC and DTC.

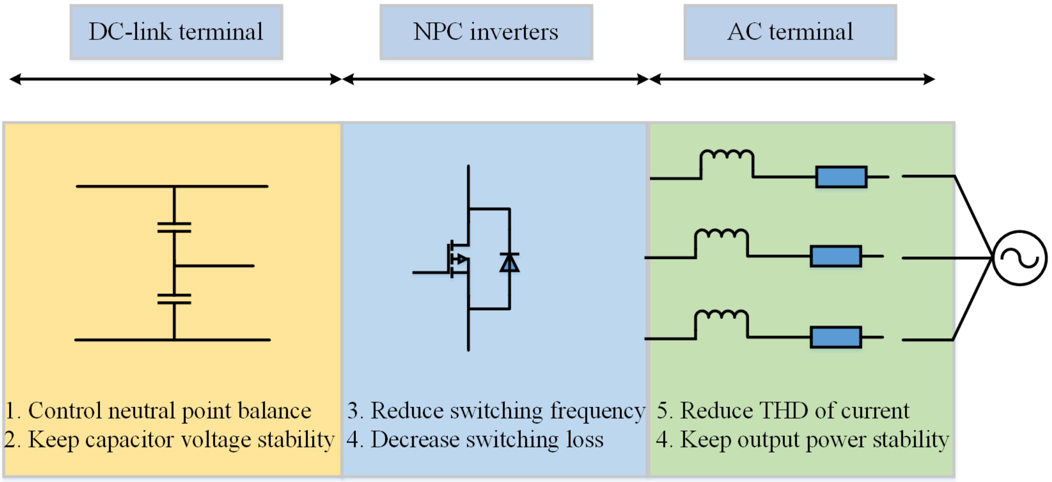


Figure 3.4: Multiple constraints for NPC inverter system

Figure 3.4 shows the six constrained objectives for this NPC inverter system. In general, it can be divided into three parts according to the structure of this NPC inverter system: DC-link terminal, NPC inverters and AC terminal. The control objectives of the three parts are different:

- In the first part, the requirements of the DC-link are controlling the neutral point balance and keeping capacitor voltage values stable and equivalent (up and down capacitors in the DC-link terminal). The imbalance capacitor voltages of the neutral point are an inherent problem for NPC inverters. The DC-link capacitors (up and down) voltages keep continually charging and discharging under working conditions, which can cause the neutral point of the capacitors to float resulting in capacitor voltages imbalance. In addition, there are some other reasons causing the neutral point capacitor voltage imbalance such as the asymmetry of the power electronics semiconductors and the cumulative error of the modulation and control methods applying in the NPC inverters. The neutral point imbalance not only influences the working performance of the NPC inverter system but also damages the power electronics semiconductors. Therefore, the first objective of this newly designed model predictive control is to keep the capacitor voltages balanced.

- In the second part, the control requirement for the NPC inverters is to reduce switching frequency and decrease switching loss. Switching loss sharply increases with the development of the application's power. In industrial applications, the high power application of IGBT will produce a great switching loss, which is usually expressed as heat [147]. As a result, when designing the cost function, controlling the switching frequencies of the NPC inverter system need to be considered. In the last section modelling of the NPC inverters, 27 switching vectors could apply to the

NPC inverter system. However, these 27 switching vectors could not all be used directly in one specific working condition. Accordingly, a novel cost function is designed to optimise the switching sequence of this NPC inverter system to reduce switching frequency. This can be illustrated by the switching state $(0, P, N)$ in Figure 3.5. The optional switching states for V_{10} are V_0, V_2, V_3, V_9, and V_{11}. Therefore, a cost function for predicting the switching sequence can be obtained.

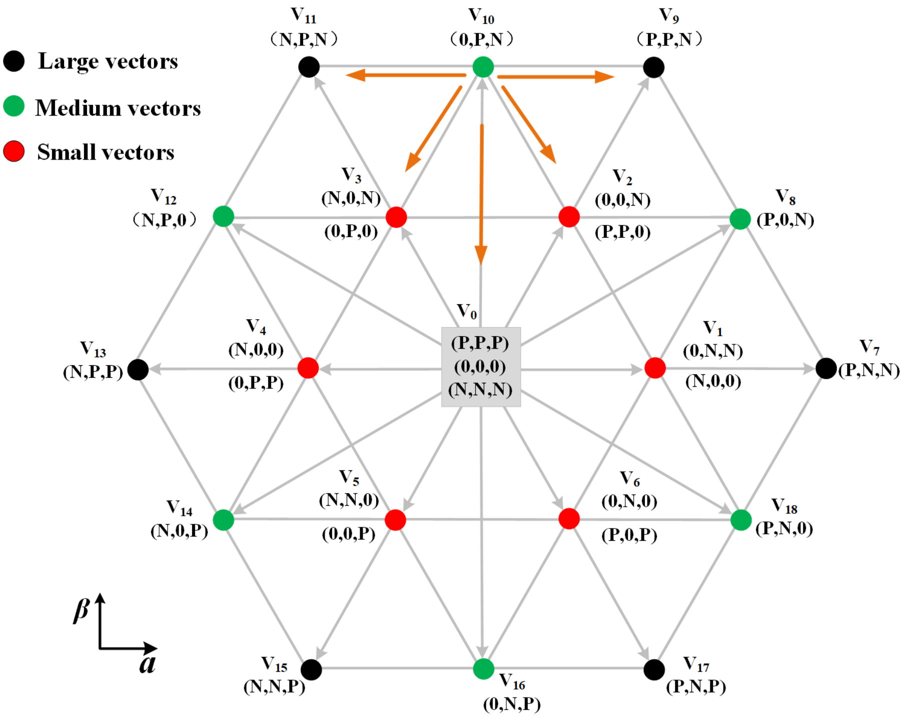


Figure 3.5: Predicting the switching sequence of NPC inverters

- Lastly, applications will be added to the AC terminal. Thus, the requirements of limiting maximum current and keeping output power stable for application safety should be considered. In this proposed cost function, the MPC controller can predict the future values of the AC terminal currents to track the reference currents.

Therefore, a novel cost function is proposed. This new cost function J is designed with a number of constraints, including tracking the output currents in the first part J_1, controlling neutral point voltage and maintaining capacitor voltage stability in the second part J_2, and reducing switching frequency and decreasing switching loss in the last part J_3.

The main idea of the MPC is to find an optimal control input for power switches through solving an online optimisation problem and implementing the resulting optimal control in a receding-horizon way [19][21]. In general, the objective function of the optimisation problem is related to system performance. In this section, cost function J is as follows, involving three parts:

$$J(k+1) = n_1 J_1(k+1) + n_2 J_2(k+1) + n_3 J_3(k+1) \tag{3.23}$$

where n_1, n_2, and n_3 are the weighting factors for J_1, J_2, and J_3 in this cost function. The weighting factors (n_1, n_2, and n_3) design will be shown in the next section 3.4. The first item of this cost function J_1 achieves current tracking.

$$J_1(k+1) = |i_\alpha(k+1) - i_\alpha^*(k+1)|^2 + |i_\beta(k+1) - i_\beta^*(k+1)|^2 \tag{3.24}$$

where $i_\alpha(k+1)$ and $i_\beta(k+1)$ represent the current predictions in terms of the system model; $i_\alpha^*(k+1)$ and $i_\beta^*(k+1)$ stands for the reference current, which can be obtained from Equation 3.19 and Equation 3.20.

Then, the DC-link is required to control the neutral point voltage and keep capacitor voltage values stable, which can be achieved by the following cost function J_2:

$$J_2(k+1) = |u_{c1}(k+1) - u_{c2}(k+1)|^2 \tag{3.25}$$

In the last item of the cost function, the control requirement for the NPC inverters is to reduce switching frequency and decrease switching loss. The cost function J_3 is expressed as follows:

$$J_3(k+1) = |S_a(k) - S_a(i_{opt})|^2 + |S_b(k) - S_b(i_{opt})|^2 + |S_c(k) - S_c(i_{opt})|^2 \tag{3.26}$$

where, $S_x(k)$ and $S_x(i_{opt})$ $(x = a, b, c)$ express the optimal switching states in the time interval, k, and the last time interval, $k-1$, respectively. J_3 concentrates on limiting the number of power switch commutations.

3.4 Weighting Factors Design

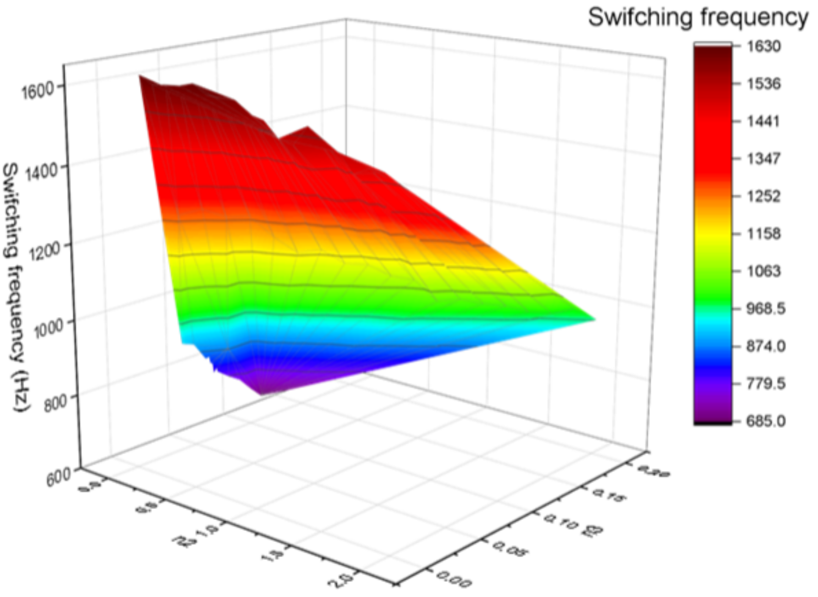
In a model predictive control algorithm, one single cost function can implement multiple control objectives, variables, and constraints simultaneously, which is one of its main strengths to replace cascaded control architectures. In this way, additional control requirements (such as switching frequency reduction, common mode voltage reduction and DC-link capacitor voltages balance) can be met, and typical variables (current, voltage, power, torque and magnetic flux) can also be controlled. Control of the objectives can be achieved simply by introducing an additional control objective to evaluate the cost function. However, these different variables include different units and different orders of magnitude. Merging two or more variables into one cost function would be a complex and challenging task. In cost function, each control objective has a specific weighting factor that is able to regulate the importance of the item to other control objectives or the weight relationship of the cost function. For example, in this chapter, n_1, n_2, and n_3 are the weighting factors for J_1, J_2, and J_3 in this cost function.

These weighting factors need to be designed correctly to achieve the desired performance requirements. However, there is a lack of appropriate analysis, numerical method or control design theory that can guide the adjustment of such weighting factors, determining the weighting factors based on the trial-and-error. This challenge has not been detracted from its success in implementing model predictive control in a variety of power converters. However, there is still a strong desire to develop a set of procedures or identify some basic guidelines to reduce the uncertainty in the adjustment and improve the efficiency of the adjustment.

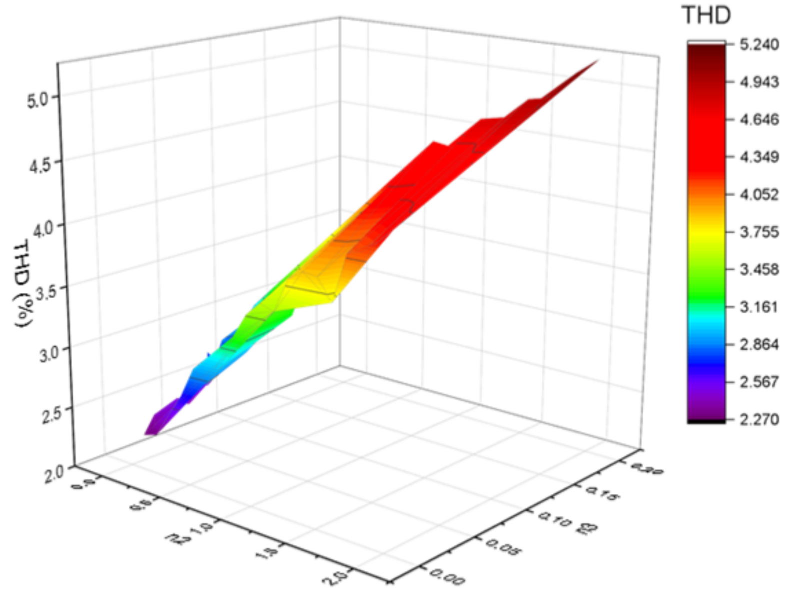
The control objectives have been detailed analysis in section 3.3. In the cost function of this chapter, this new cost function J is designed with a number of constraints, including tracking the output currents in the first part J_1, controlling neutral point voltage and maintaining capacitor voltage stability in the second part J_2, and reducing switching frequency and decreasing switching loss in the last part J_3. n_1, n_2, and n_3 are the weighting factors for J_1, J_2, and J_3 in this cost function. As for the first part J_1 tracking, the output currents relates to the system performances and should be a hard constraint. Therefore, the weighting factor n_1 for J_1 is given the highest priority among the three weighting factors. The second part J_2, controlling neutral point voltage and maintaining capacitor voltage stability,is a hard constraint or not depending on the specific case (the size of the capacitance in DC-link), so the weighting factor n_2 is regulated on a case-by-case basis. In engineering practice, the large size of the capacitance is tended to be used, so the performance index of this is not taken into account in this section. The last part J_3 (reducing switching frequency and decreasing switching loss) is a soft constraint, whose weighting factor n_3 is given the lowest priority. By experimental study, the measured value of the performance index (switching frequency of NPC inverters and total harmonic distortion of the output currents) achieved by weighting factors are indicated in Figure 3.6.

3.5 Optimisation Process

ψ is introduced to express switching states.



(a)



(b)

Figure 3.6: The relationship between weighting factors and performance indexes: (a) The relationship between weighting factors and switching frequencies; (b) The relationship between weighting factors and total harmonic distortion (THD) of output currents.

$$\psi \triangleq \left\{ u = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \in \mathbb{R}^3 \mid u_x \in \{-1, 0, 1\}, x = a, b, c \right\} \tag{3.27}$$

In fact, $\psi = \{u_1, u_2, \ldots, u_{27}\}$ in NPC inverters, which are shown in Table 3.2 and a, b, and c represent the three phases.

The optimal control can be stated as:

$$\begin{aligned} u_{opt}(k) = \arg \min_{u(k) \in \psi} \quad & \tilde{J}\left(u_i(k)\right) \triangleq J(k) \\ \text{subject to} \quad & (Equation\ 3.3) \ \ (Equation\ 3.6) \\ & (Equation\ 3.11) \ \ (Equation\ 3.12) \end{aligned} \tag{3.28}$$

Cost function J is used to find the selected voltage vector, $u_{opt}(k)$, which minimises the cost function as the control input.

3.6 Simulation Results

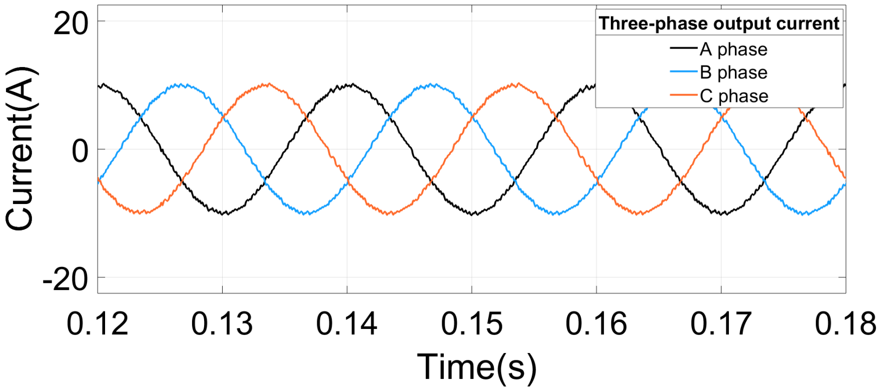
The simulation parameters and value are shown in Table 3.3. The simulation time is from $0.0\,s$ to $0.3\,s$. The DC voltage is $600\,V$. The load resistor and inductor are $8\,\Omega$ and $23\,mH$, respectively. The sampling period is $T_s = 100\,\mu s$. The performance of this control algorithm and comparison results with conventional MPC controller [82] and industrial PI controller [148] are shown in the following.

Table 3.3: Simulation Parameters and Value in MPC Control

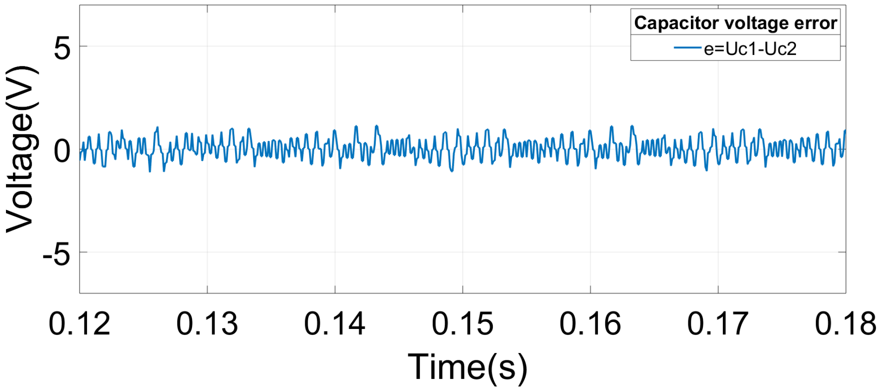
Parameters	**Value**
Start time	$0.0\,s$
Stop time	$0.3\,s$
DC voltage	$600\,V$
Load resistance	$8\,\Omega$
Load inductance	$23\,mH$
Sampling period	$100\,\mu s$

3.6.1 Nominal Operation

In this section, n_1, n_2 and n_3 were 1, 0.1, and 0.01, respectively. Firstly, the controller was verified under the nominal working mode of the 3-level NPC inverters. The performance of the response is illustrated in Figure 3.7. The three-phase output currents with moderate ripples are illustrated in Figure 3.7(a). The THD of the output currents was 2.42%. The capacitor voltages u_{c1} and u_{c2} are balanced with the proposed MPC



(a)



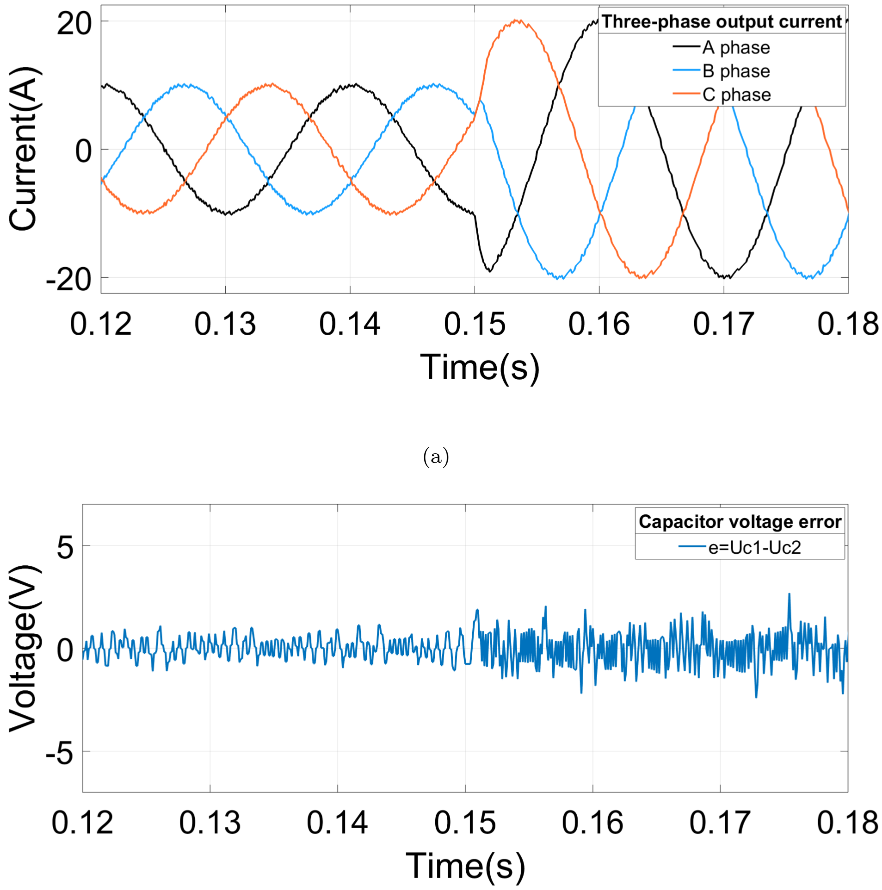
(b)

Figure 3.7: Nominal operation: (a) The three-phase output current (b) The DC-link capacitor voltage error.

algorithm in Figure 3.7(b). The maximum fluctuation value of the DC-link capacitor voltage was 1.248 V, which accounted for 0.208% of the total DC voltage. Consequently, based on the results noted above, the performance of the proposed MPC algorithm was at an effective level with respect to both the quality of the output current and the neutral point balance.

3.6.2 Current Variation

The robustness of this proposed MPC algorithm was verified in this section with respect to the current variation. The weighting factors n_1, n_2, and n_3 were 1, 0.1, and 0.01, respectively. In Figure 3.8, the reference currents increase dramatically from 10 A to 20 A during the last 0.15 s. In Figure 3.8(a), with the proposed MPC algorithm, the three-phase output currents follow the change of the reference currents with fast dynamic response and the rise time is 0.8 ms. The THD of the output current was 1.35%. In the interim, this proposed MPC algorithm enables the maintenance of the capacitor voltage



(a)

(b)

Figure 3.8: Current variation: increased from 10A to 20A from 0.15s to 0.3s: (a) The three-phase output current (b) The DC-link capacitor voltage error.

at a balanced level, as illustrated in Figure 3.8(b). The maximum fluctuation value of the DC-link capacitor voltage was $2.759\,V$, which accounted for 0.460% of the total DC voltage. Therefore, the proposed MPC algorithm indicates good robustness for current variation.

3.6.3 Switching Frequency Reduction

In this section, the simulation results showed the proposed MPC algorithm effectively reduced the switching frequency when compared with a successful and conventional MPC approach [82].

It is important to note in particular that the finite control set associated with the MPC algorithm will generate a variable switching frequency. This has previously been discussed in terms of an average switching frequency [21]. An average switching frequency, f_{sw}, was achieved by computing the cumulative number of switch changes in one time period. Thus, it can be defined as follows [21]:

$$f_{sw} = \sum_{i=1}^{4} \frac{f_{s_{ai}} + f_{s_{bi}} + f_{s_{ci}}}{12} \tag{3.29}$$

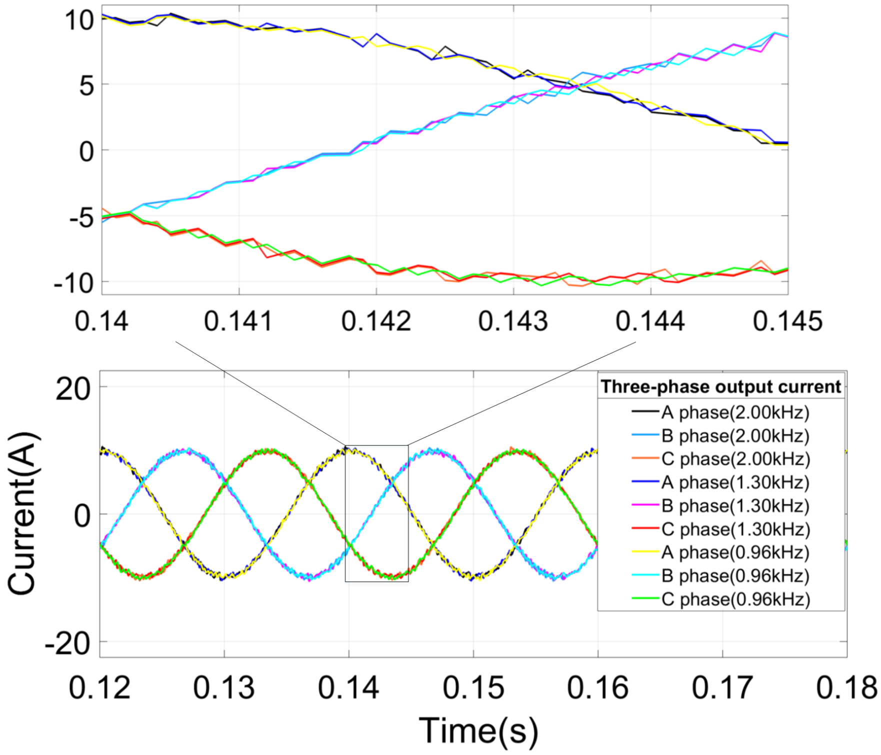
where, $f_{s_{ai}}$, $f_{s_{bi}}$, and $f_{s_{ci}}$ are the average switching frequencies for the period over three phases A, B, and C.

In order to make a fair comparison, the conventional MPC algorithm in [82] was implemented in the same working condition as the proposed MPC algorithm. The performance of the conventional MPC algorithm is shown in Figure 3.9. The simulation results in Figure 3.9 are summarised in Table 3.4. With the selected weighting factors ($n_1 = 1$, $n_2 = 0.7$, and $n_3 = 0.05$), the switching frequency of the proposed MPC decreased by 35% compared to the conventional MPC method [82]. The root-mean-square (RMS) error of the DC-link capacitor fluctuation increased by $0.047\,V$ from $0.238\,V$ to $0.285\,V$, and they accounted for 0.0397% and 0.0475% of the total DC-link voltage, respectively. Although the RMS error increased slightly ($0.047\,V$), the error was still maintained at a lower level. At the same time, the THD of the proposed MPC method of 3.40% was lower than the THD of the conventional MPC with a value of 3.54%.

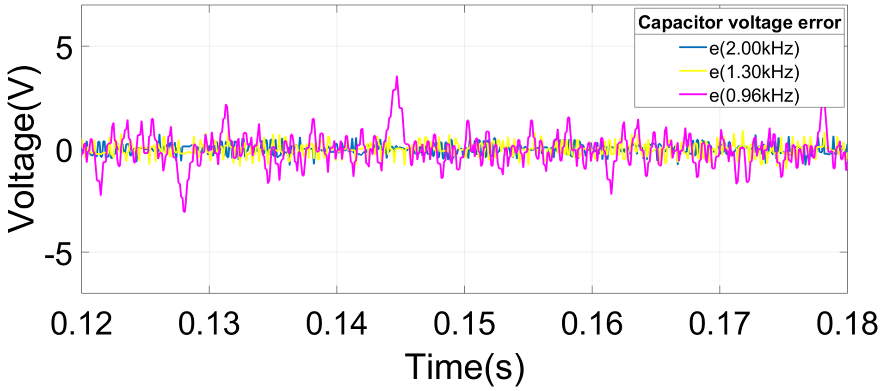
Table 3.4: Comparison Results of Switching Frequency Reduction with Conventional MPC

	Conventional MPC[82]	**Proposed MPC**	
Weighting factor (n_3)	N.A.	0.05	0.08
Switching frequency *(kHz)*	2.00	1.30	0.96
THD of output current	3.54%	3.40%	3.16%
RMS error of DC capacitor fluctuation voltage *(V)*	0.238	0.285	0.961

When the weighting factor n_3 was increased further, the switching frequency decreased further to 48% of the conventional MPC method. The weighting factors n_1, n_2, and n_3 were 1, 0.35, and 0.08, respectively. The RMS error of the DC-link capacitor voltage fluctuation value increased to $0.961\,V$, which was 0.160% of the total DC-link voltage. Meanwhile, the THD of output current was 3.16%, which was still lower than the THD of the conventional MPC method with switching frequency of $2.00\,kHz$. The proposed MPC algorithm indicated good performance with low harmonic distortion, despite the compromise attained between the switching frequency and the harmonic distortion. To further illustrate its benefits, the outcomes of the simulation will be evaluated against the performance of industrial PI control in the next section.



(a)



(b)

Figure 3.9: Comparison results for the conventional MPC in switching frequency 2.00 kHz and the proposed MPC in switching frequency 1.30 kHz and 0.96 kHz: (a) The three-phase output current (b) The DC-link capacitor voltage error.

3.6.4 Comparison with Industrial PI Controllers

In this section, the comparison results of the industrial PI controllers [148] and the proposed MPC algorithm are shown in Figure 3.10-Figure 3.12 under different switching frequencies. Through this reduced switching frequency aspect, the proposed MPC method showed better superiority than the industrial PI controller in terms of the lower THD of output current and fast response with current variations.

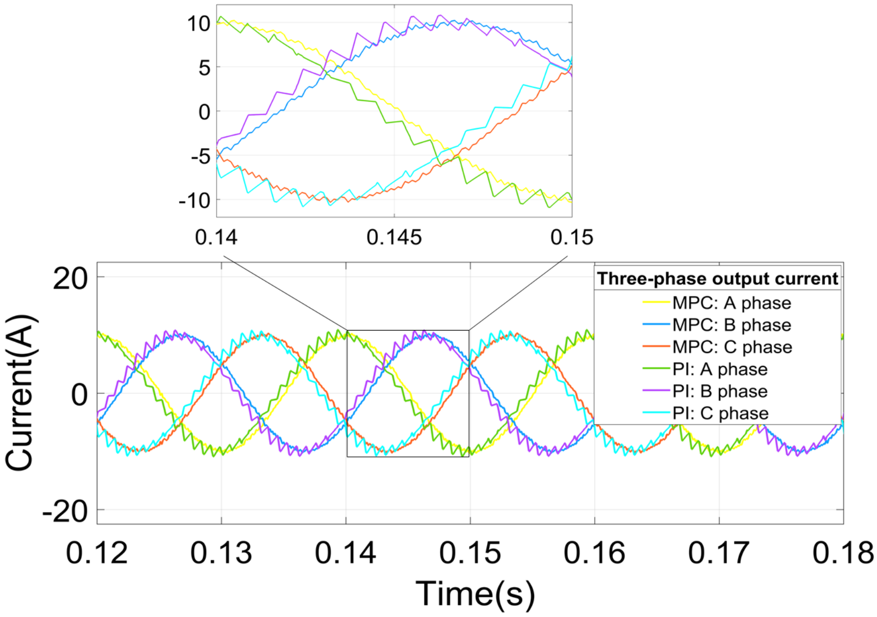
There are four criteria that determine the industrial power electronics PI controllers parameter design: optimal modulus criterion, optimal symmetry criterion, rule of thumb, and damping factor selection [148]. Concerning the step change of reference, though the optimal modulus criterion demonstrates good response with 4% overshoot, its disturbance rejection is quite slow [149]. The optimal symmetry criterion, on the other hand, demonstrates quick disturbance rejection as well as a high overshoot response of 43% [148][149]. Hence, an input filter that can add more components to the circuit is required. As opposed to the aforementioned methods, we observed that the damping factor selection was adequately damped [148]. Rule of thumb is only for rough design or used by experienced engineers. Therefore, the damping factor selection for the industrial PI controllers parameter design was applied in this section. K_1 was proportional gain and K_2 was integrated gain.

Due to the damping factor selection [148] $\xi = 0.707$ and when the switching frequency $f_{sw} = 0.96\,kHz$: $K_1 = 1, K_2 = 1724$; when the switching frequency $f_{sw} = 1.30\,kHz$: $K_1 = 1$, $K_2 = 2344$. Therefore, the simulation results are shown in the following Figure 3.10 and Figure 3.11, which are summarised in Table 3.5.

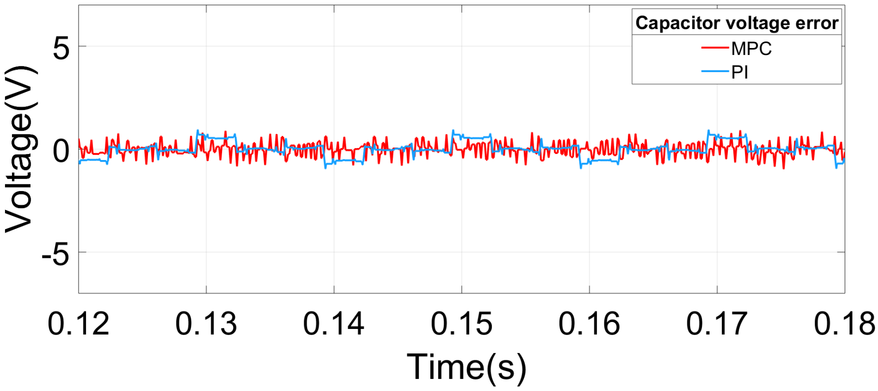
Table 3.5: Comparison Results of MPC and PI

	Proposed MPC		**PI** [148]	
Switching frequency *(kHz)*	1.30	0.96	1.30	0.96
THD of output current	3.40%	3.16%	7.42%	9.89%
RMS error of DC capacitor fluctuation voltage (V)	0.285	0.961	0.388	0.374

The simulation results of the PI controller combining with the PWM method, are shown in Figure 3.10 and Figure 3.11 under the different switching frequencies of $1.30\,kHz$ and $0.96\,kHz$. When the switching frequency is $1.30\,kHz$ in Figure 3.10, the performance of the output current in this proposed MPC algorithm is much better than the PI controller in Figure 3.10(a). The THD of the output currents were 3.40% and 7.42% for the MPC and PI methods. Therefore, the quality of the output current in the MPC method was superior to that of the PI method. In Figure 3.10(b), both methods maintain the neutral point of DC-link voltage balance while also maintaining low DC-link capacitor fluctuation voltage. The RMS errors of the DC-link capacitor fluctuation voltage were $0.285\,V$ and $0.388\,V$, respectively, for the MPC and PI method.



(a)

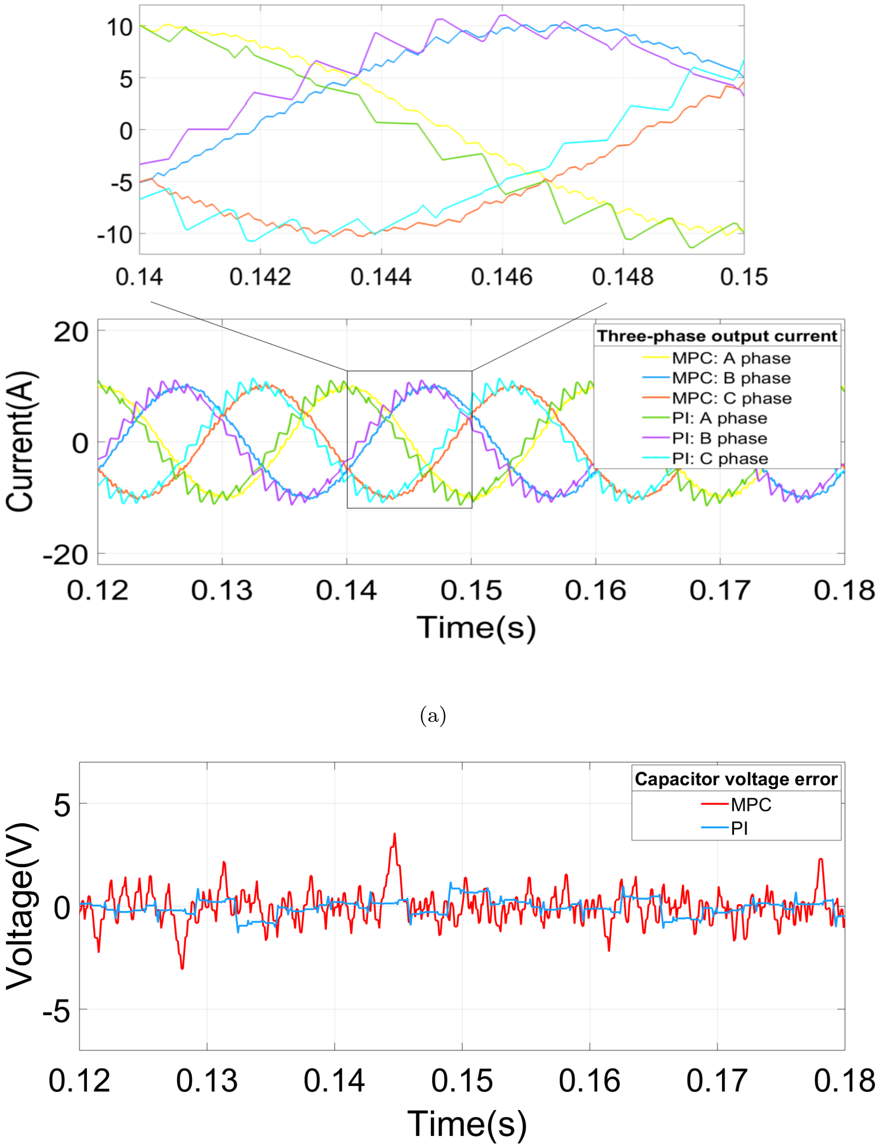


(b)

Figure 3.10: MPC and PI comparison results in switching frequency $1.30\,kHz$: (a) The three-phase output current (b) The DC-link capacitor voltage error.

Figure 3.11 illustrates the results of the MPC and PI controller when the switching frequency reduces to $0.96\,kHz$. The output currents THD were 3.16% and 9.89% for each of the MPC and PI methods, respectively. Meanwhile, the RMS error of the DC capacitor fluctuation voltage were $0.961\,V$ and $0.374\,V$ for the MPC and the PI method. Overall, when employing this reduced switching frequency condition, the proposed MPC method shows better superiority than the PI controller.

The robustness of the proposed MPC algorithm and the PI controller was verified in this section. In Figure 3.12, with respect to the current variation, the reference current is dramatically increased from $10\,A$ to $20\,A$ during the last $0.15\,s$. From the perspective of the three-phase output currents in Figure 3.12(a), the output current performance of

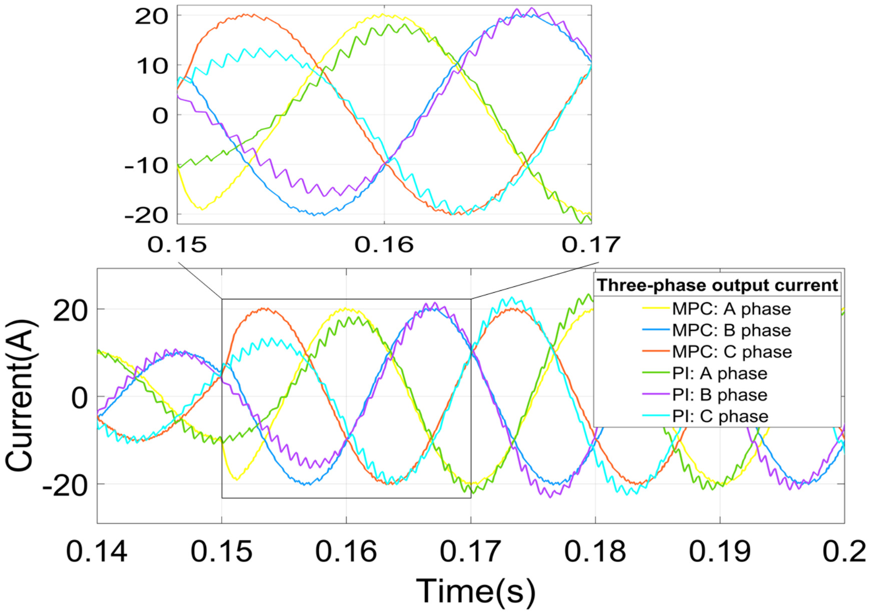


(a)

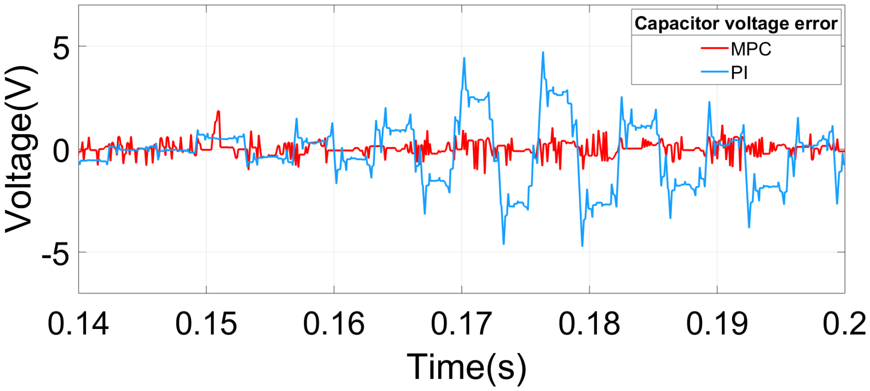
(b)

Figure 3.11: MPC and PI comparison results in switching frequency 0.96 kHz: (a) The three-phase output current (b) The DC-link capacitor voltage error.

the MPC controller has less fluctuation than the PI controller. When the two systems, the MPC and the PI controller, reached a steady state, the THD of the output currents was 2.01% and 4.70%, respectively. Therefore, the proposed MPC controller revealed the higher quality output currents than the PI controller. Then, from the perspective of DC-link capacitor voltage error in Figure 3.12(b), both controllers have good performance for balancing the neutral point of DC-link capacitor voltage. When the system was added to 100% current variation from 10 A to 20 A, the DC-link capacitor fluctuation voltage error of the MPC controller was smaller than that of the PI controller. At this level, the MPC controller displayed a better performance for control of the neutral point of DC-link capacitor voltage than the PI controller. Regarding the dynamic response of both



(a)



(b)

Figure 3.12: MPC and PI comparison results for current variation: current changed from $10\,A$ to $20\,A$ from $0.15\,s$ to $0.3\,s$: (a) The three-phase output current (b) The DC-link capacitor voltage error.

system at the 100% current variation from $10\,A$ to $20\,A$, the MPC controller indicated a more rapid response compared to that of the PI controller. From the simulation results in Figure 3.13, it can be noted that the rise time for MPC and PI controllers are $1\,ms$ and $18.5\,ms$, respectively. Thus, the proposed MPC algorithm shows fast dynamic response and good robustness.

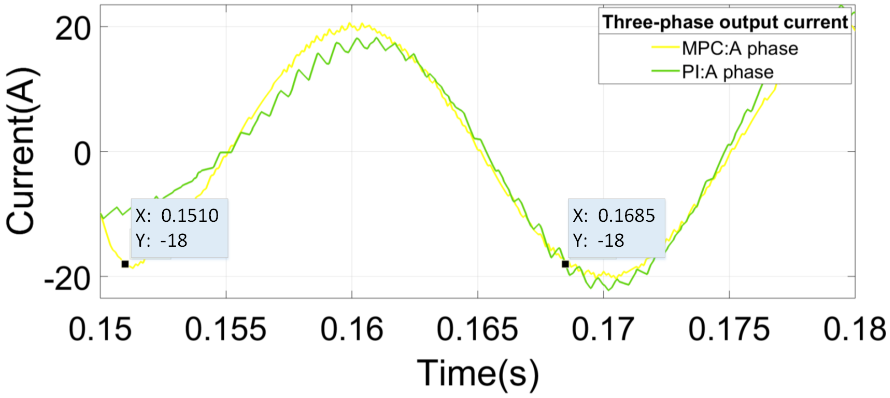


Figure 3.13: Rise time of MPC and PI comparison results for the current variation

3.7 Extended to Multistep Model Predictive Control

This section proposed a novel multistep model predictive control (MMPC) algorithm for 3-level Neutral Point Clamped (NPC) inverters that can manage current variation. The algorithm can efficiently reduce the total harmonic distortion (THD) of the current output, decrease the computational burden associated with other similar algorithms, and provide for the robust handling of current variation. Additionally, this algorithm also dispenses with the need for weighting factors tuning, while maintaining the advantages of the conventional MPC algorithms, such as a capacity to handle multiple constraints (capacitor voltage balancing) and to respond rapidly to the current variation. The performance of the proposed algorithm is verified using a simulation of 3-level NPC inverters and is compared with a conventional MPC algorithm. This section is organized as follows: Control objectives are provided firstly in section 3.7.1. The conventional MMPC algorithm is indicated in section 3.7.2. Then, the proposed MMPC algorithm is detailed in section 3.7.3, including the design of the cost function, a comparison between the space voltage vectors in a conventional algorithm and the proposed algorithm, and the optimisation process. Simulation results (for nominal operation and with current variation) are presented in section 3.7.6.

3.7.1 Control Objectives

In order to reduce the THD of the output currents, an MMPC algorithm based on a two-step prediction is proposed in this section. This procedure also ensures neutral point balancing. So, the main control objectives of this 3-level NPC inverters can be described as current tracking and neutral point balancing. Current tracking focuses on minimising the error between the reference current and the predicted value. Neutral point balancing aims to balance the capacitor voltages by minimizing $|u_{c1} - u_{c2}|$. Voltage balancing is critical for NPC inverters. An unbalanced voltage can damage the power-related electronic components. The design of the MMPC algorithm is described in the next section. In the following section, the process associated with a conventional MMPC algorithm is firstly presented. Then, the proposed MMPC algorithm is given.

3.7.2 Conventional MMPC

The conventional MMPC algorithm [137] works with different space voltage vectors. However, it has a revised cost function, which can be expressed as follows:

$$J_{mmpc1}(k+1) = J_1(k+1) + J_2(k+1) \tag{3.30}$$

$$J_1(k+1) = \|i^*_{\alpha\beta}(k+1) - i_{\alpha\beta}(k+1)\|_2^2 + \|i^*_{\alpha\beta}(k+1) - i_{\alpha\beta}(k+2)\|_2^2 \tag{3.31}$$

$$J_2(k+1) = |u_{c1}(k+1) - u_{c2}(k+1)|^2 \tag{3.32}$$

where, $i_{\alpha\beta}(k+1)$ represent the current predictions in terms of the system model; and $i^*_{\alpha\beta}(k+1)$ stand for the current reference in the next sampling period. $u_{c1}(k+1)$ and $u_{c2}(k+1)$ are DC-link capacitor voltages.

3.7.3 Proposed MMPC

The proposed MMPC algorithm considers the same space voltage vectors. The cost function is indicated as follows:

$$J_{mmpc2}(k+1) = J_1(k+1) + J_2(k+1) \tag{3.33}$$

$$J_1(k+1) = \|i^*_{\alpha\beta}(k+1) - i_{\alpha\beta}(k+1)\|_2^2 + \|i_{\alpha\beta}(k+1) - i_{\alpha\beta}(k+2)\|_2^2 \tag{3.34}$$

$$J_2(k+1) = |u_{c1}(k+1) - u_{c2}(k+1)|^2 \tag{3.35}$$

The proposed MMPC algorithm consists of the following five steps:

Step one: The load current $i(k)$ is measured.

Step two: The model of the 3-level NPC inverters (Equation 3.3, Equation 3.5, and Equation 3.6) is used to arrive at the value of the load current for the first-next sampling period, $i(k+1)$, for each of the 27 different voltage vectors expressed in Equation 3.1 and Equation 3.2. The relationship between the voltage vectors and the corresponding currents from according to Equation 3.1, Equation 3.3, and Equation 3.4 is thus established. The first-next sampling period for the two algorithms is identical.

Step three: At the second-next sampling period $k + 2$, the algorithms differ according to the second-next voltage vector selected. In the conventional MMPC algorithm, a different voltage vector was considered. Here, the same space voltage vectors are used for the second-next sampling period.

Step four: The cost function, J_{mmpc1}, for the conventional MMPC algorithm and the cost function, J_{mmpc2}, for the proposed MMPC algorithm are used to evaluate the error between the reference and prediction in the first-next sampling period and the second-next sampling period for each voltage vector. At this point, the constraint condition for capacitor voltage balancing is added into both cost functions.

Step five: The voltage vectors that minimise the cost function are selected, and the corresponding switching states are generated and applied in the 3-level NPC inverters.

3.7.4 Selection of Space Voltage Vectors in the Original MPC, Original MMPC and Proposed MMPC

When conventional MPC with one-step prediction is applied, the effect of applying a space voltage vector is evaluated via the cost function. Only 27 space voltage vectors are considered in this situation.

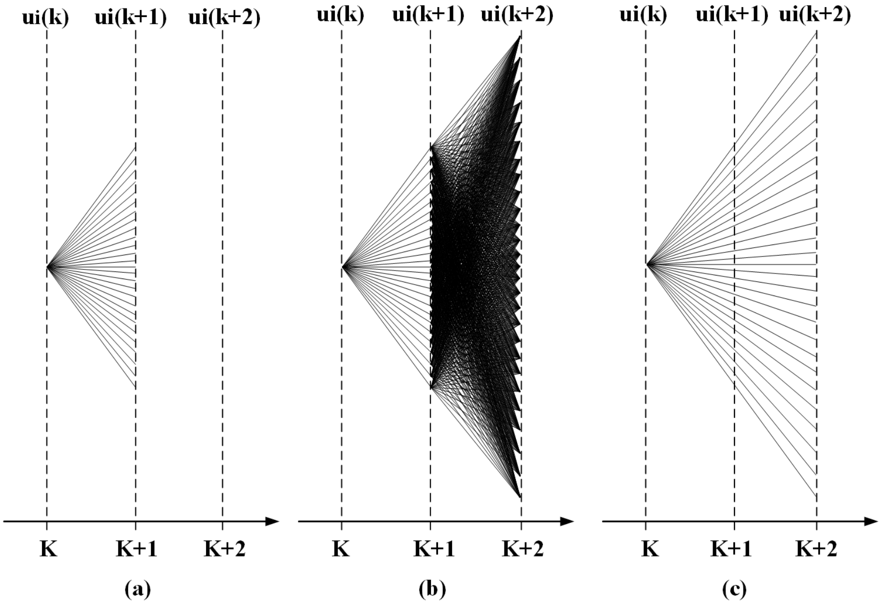


Figure 3.14: Prediction of the space voltage vectors: (a) Original MPC with one-step prediction; (b) Original MMPC with two-step prediction considering different space voltage vectors; and (c) The proposed MMPC with two-step prediction considering the same space voltage vectors.

In the original MMPC algorithm, when undertaking two-step prediction for the different space voltage vectors, the first space voltage vector is applied for the first sampling period, $(k+1)$. The second different space voltage vector is then applied for the second sampling period, $(k+2)$. By doing this, the algorithm generates a total of $27^2 = 729$ possible sequences of two-step predictions for different space voltage vectors. Numbers such as this result in extremely large calculations. Handling this in either experimental or practical applications necessitates a high-performance microcontroller, substantially increasing the cost.

To reduce these large calculations, the construction cost function for the same space voltage vector can be calculated during the two-step prediction. The proposed MMPC algorithm essentially simplifies the original MMPC algorithm and can reduce the computational burden by 93%, i.e., from 729 sets of calculations to 54. The results of a simulation applying the proposed algorithm are shown in section 3.7.6.

3.7.5 Optimisation Process

ψ is introduced to express switching states.

$$\psi \triangleq \left\{ u = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \in \mathbb{R}^3 \mid u_x \in \{-1, 0, 1\}, x = a, b, c \right\} \tag{3.36}$$

In fact, $\psi = \{u_1, u_2, \ldots, u_{27}\}$ in NPC inverters, which are shown in Table 3.2 and a, b, and c represent the three phases.

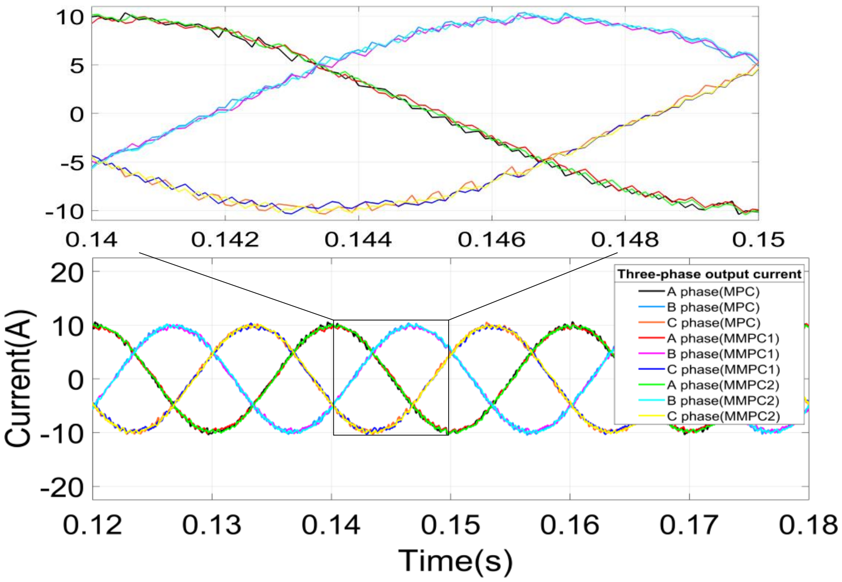
The optimal control can be stated as:

$$\begin{aligned} u_{opt}(k) = \arg \min_{u(k)\in\psi} \quad & \tilde{J}\left(u_i(k)\right) \triangleq J_{mmpc}(k) \\ \text{subject to} \quad & (Equation\ 3.3) \ \ (Equation\ 3.6) \\ & (Equation\ 3.11) \ \ (Equation\ 3.12) \end{aligned} \tag{3.37}$$

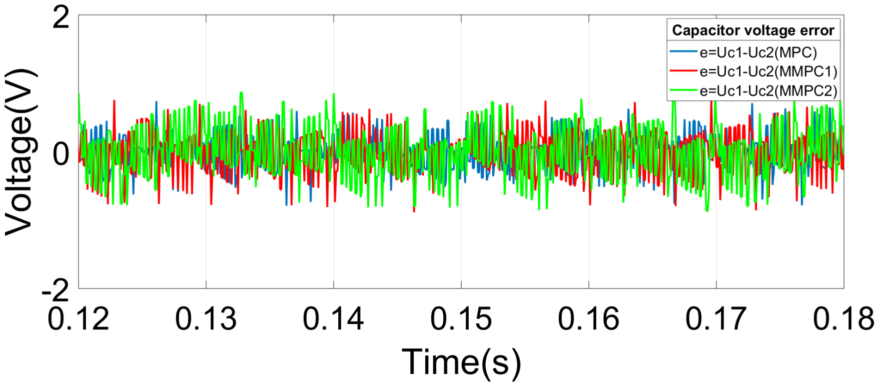
The cost function J_{mmpc} stands for J_{mmpc1} and J_{mmpc2}, which are used to find the selected voltage vector, $u_{opt}(k)$, that minimises the cost function.

3.7.6 Simulation Results

This section demonstrates the effectiveness of the proposed MMPC algorithm. Two-part testing was conducted using MATLAB Simulink to evaluate its performance for: 1) nominal operation; and 2) current variation. The simulation time ranged from $0\,s$ to $0.3\,s$. The DC-link voltage was $600\,V$. The load resistance and inductance were $8\,\Omega$ and $23\,mH$, respectively. The sampling period was $T_s = 100\,\mu s$.



(a)

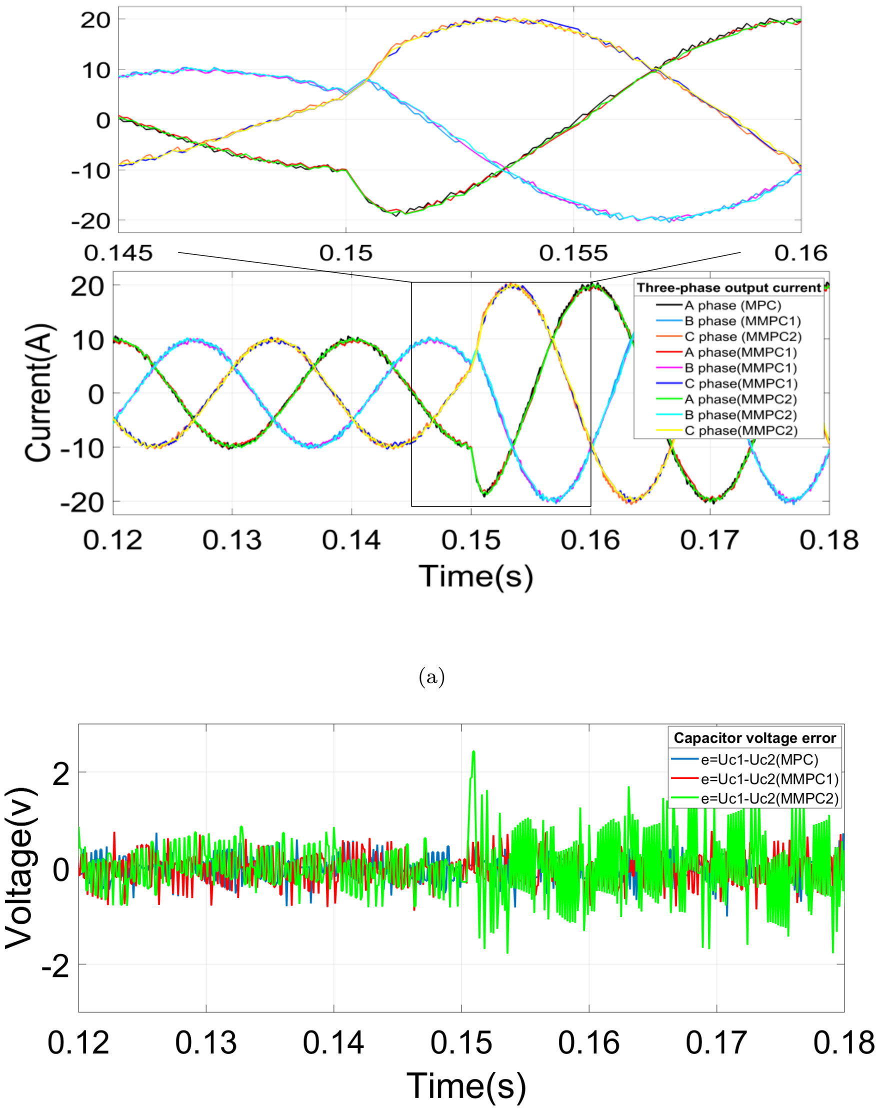


(b)

Figure 3.15: Nominal operation: (a) The three-phase output currents for the conventional MPC, MMPC1 and MMPC2; and (b) The DC-link capacitor voltage errors for the conventional MPC, MMPC1 and MMPC2.

For nominal operation, the 3-level NPC inverter system was assumed to be working under steady-state conditions, without current variation. The performance of the three algorithms, the conventional MPC, the conventional MMPC (MMPC1) and the proposed MMPC (MMPC2), is illustrated in Figure 3.15.

The three-phase output currents, showing moderate ripples, are shown in Figure 3.15(a). The THD for MMPC1 was 2.77%, which was the lowest of the three algorithms. The THDs for the conventional MPC and MMPC2 were 3.54% and 2.82%, respectively. For the capacitor voltage balancing, the three algorithms were all capable of controlling fluctuating values in the DC-link capacitor voltage under $1.5\,V$. Based on the simulation



(a)

(b)

Figure 3.16: Current variation: (a) The three-phase output currents for the conventional MPC, MMPC1 and MMPC2; and (b) The DC-link capacitor voltage errors for the conventional MPC, MMPC1 and MMPC2.

results shown in Figure 3.15(b), Both MMPC1 and MMPC2 performed effectively in terms of the quality of output currents.

To assess the performance of the algorithms under conditions of the current variation, in the final 0.15 s of the simulation, the reference currents rose by 100%, from 10 A to 20 A. The resulting output currents are shown in Figure 3.16(a). It can be seen that all three algorithms were able to produce a fast-dynamic response to the changes in the reference current (with within 0.001 s). The quality of the output current for MMPC1 was still the best, with a THD value of 1.70%. However, under conditions of current variation, the THD for the conventional MPC (2.07%) was larger than the THDs for MMPC1

(1.70%) and MMPC2 (1.76%). While significantly reducing the computational cost, the proposed MMPC was still able almost to match the performance of the conventional MMPC, the difference between them being just 0.07%.

The THD values for the three algorithms and other output performances, including rise time for current variation, switching frequency, RMS error of DC-link capacitor fluctuation voltage, generated during the simulations are summarised in the following table Table 3.6:

Table 3.6: Comparison of THD Values for the Conventional MPC, Conventional MMPC and Proposed MMPC

	Conventional MPC[82]	**Conventional MMPC1[137]**	**Proposed MMPC2**
THD nominal operation	3.54%	2.77%	2.82%
THD 100% current variation during the last 0.15s	2.07%	1.70%	1.76%
Rise time (s)	0.0008	0.0008	0.0010
Switching frequency (kHz)	2.07	1.95	2.02
RMS error of DC capacitor fluctuation voltage(V)	0.23	0.49	0.35

3.8 Extended to Grid-connected NPC Inverters

This section presents a model predictive control algorithm for 3-level grid-connected NPC inverters that can reduce the computational complexity involved in predicting currents. The proposed algorithm can assess the minimum cost function between 27 voltage vectors and expected voltage vectors to select the most appropriate voltage vectors for NPC inverters. This can thus reduce the number of current predictions typically necessitated by conventional MPC algorithms by a factor of 27, thereby significantly reducing the computational burden. The proposed algorithm was fully tested in actual grid-connected NPC inverters, and the results clearly indicated its effectiveness.

3.8.1 Problem Formulation

Figure 3.17 shows the configuration of a three-phase NPC grid-connected inverters. R and L stand for load resistor and inductor, respectively. i_a, i_b and i_c represent the load current of the three-phases A, B and C, respectively. For the DC-link terminal, V_{dc} stands for the input DC voltage. Each phase of the NPC inverters consists of four switches and two diodes. For example, in phase A, S_{a1}, S_{a2}, S_{a3} and S_{a4} are the four switches, while D_1 and D_2 are the two diodes. The neutral point of the DC-link terminal connects to two capacitors C_1 and C_2. The state definition for each phase is defined in Table 3.7. S_x expresses the switching device. x is phase, where $x = \{a, b, c\}$. ON and OFF express the switch conduction states turn-on and turn-off, respectively. In each phase of NPC inverters, the switch has three possible statuses: P, 0 and N. The values of these three possible states are +1/2 V_{dc}, 0 and -1/2 V_{dc}, respectively.

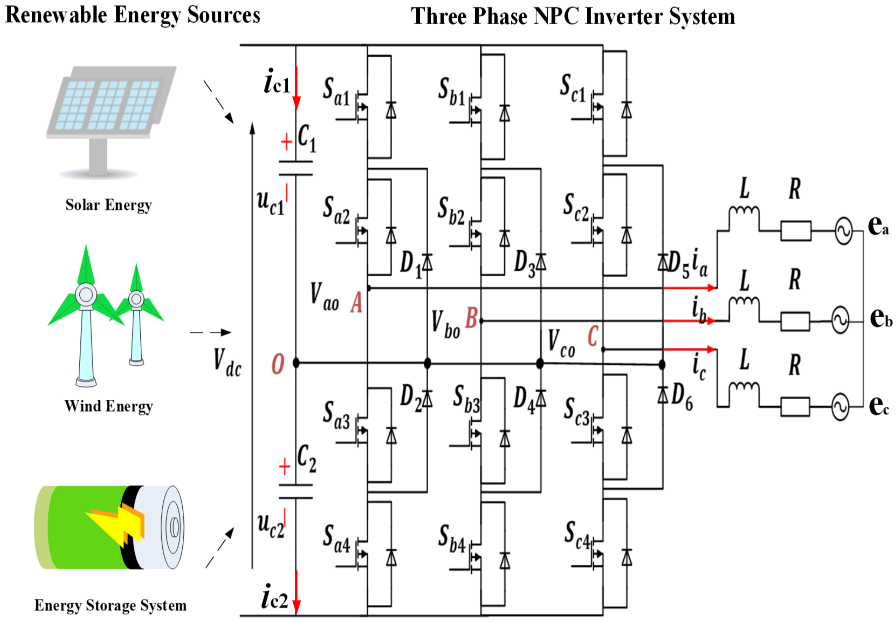


Figure 3.17: Circuit schematic of a 3-level grid-connected NPC inverter system.

Table 3.7: State Definition for Each Phase

S_X	S_{x1}	S_{x2}	S_{x3}	S_{x4}
P($+\frac{1}{2}V_{dc}$)	ON	ON	OFF	OFF
0(0)	OFF	ON	ON	OFF
N($-\frac{1}{2}V_{dc}$)	OFF	OFF	ON	ON

Taking into account all possible switching states for the three-phases, there are 19 different possible output voltage vectors generated by the 27 states. The voltage vector, V_0, has three redundant switching states and V_1-V_6 have two redundant switching states. The others, from V_7 to V_{18}, only have one switching state. On the basis of the definition of a space vector, the output vector will be:

$$v_n = \frac{2}{3}(V_{aN} + aV_{bN} + a^2V_{cN}) \tag{3.38}$$

where for the voltage space vectors (SV) V_n, $n = \{0, 1, \ldots, 18\}$. V_{ao}, V_{bo} and V_{co} are the output voltages in Figure 3.17. The output load current vector is:

$$i = \frac{2}{3}(i_a + a i_b + a^2 i_c) \tag{3.39}$$

where the coefficient unitary vector is $a = -\frac{1}{2} + \frac{\sqrt{3}}{2} j = e^{\frac{2\pi}{3} j}$. On the basis of the three-phase NPC inverter load model in Figure 3.17, the following equation can be obtained:

$$L\frac{di_x(t)}{dt} = V_{xo}(t) - Ri_x(t) - e_x(t) \tag{3.40}$$

$$i_x(t) = \begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix}, \; V_{xo}(t) = \begin{bmatrix} V_{ao}(t) \\ V_{bo}(t) \\ V_{co}(t) \end{bmatrix}, \; e_x(t) = \begin{bmatrix} e_a(t) \\ e_b(t) \\ e_c(t) \end{bmatrix}$$

where $x \in \{a, b, c\}$ represents the three phases. In an MPC model, a discrete time model is applied to predict the future value of the load current from measured currents at the kth sampling period. A forward Euler approximation can then be employed to ascertain an appropriate discrete time model for the prediction calculations. For the NPC inverter system in Figure 3.17, the load can be modelled as a first order system. However, for high order passive filters such as LC or LCL, this simple approximation may generate errors in the prediction model. So, a discrete time model can be obtained by applying a forward Euler approximation with a sampling period of T_s to the derivative:

$$\frac{di(t)}{dt} \approx \frac{i(k+1) - i(k)}{T_S} \tag{3.41}$$

Then, substituting Equation 3.40 into Equation 3.41 yields that:

$$i(k+1) = \left(1 - \frac{RT_s}{L}\right) i(k) + \frac{T_s}{L}(V(k) - e(k)) \tag{3.42}$$

The dynamic equations for the capacitor voltages in the DC-link are:

$$\frac{du_{c1}}{dt} = \frac{i_{c1}}{c} \tag{3.43}$$

$$\frac{du_{c2}}{dt} = \frac{i_{c2}}{c} \tag{3.44}$$

where, i_{c1} and i_{c2} denote the currents flowing between the two DC-link capacitors, C_1 and C_2, respectively. C is the capacitor value. u_{c1} and u_{c2} are the DC-link capacitor voltages. The same approximation of the derivative can be applied to the capacitor voltages, i.e.:

$$u_{c1}(k+1) = u_{c1}(k) + \frac{1}{C} i_{c1}(k) T_s \tag{3.45}$$

$$u_{c2}(k+1) = u_{c2}(k) + \frac{1}{C} i_{c2}(k) T_s \tag{3.46}$$

From Figure 3.17, i_{c1} and i_{c2} can be expressed as follows:

$$i_{c1}(k) = i_{dc}(k) - H_{1a} i_a(k) - H_{1b} i_b(k) - H_{1c} i_c(k) \tag{3.47}$$

$$i_{c2}(k) = i_{dc}(k) + H_{2a} i_a(k) + H_{2b} i_b(k) + H_{2c} i_c(k) \tag{3.48}$$

where, i_{dc} is the current from the DC terminal; and H_{1x} and H_{2x} express the switching state variables, which are given by:

$$H_{1x} = \begin{cases} 1, & \text{if } S_x = P \\ 0, & \text{otherwise} \end{cases} \tag{3.49}$$

$$H_{2x} = \begin{cases} 1, & \text{if } S_x = N \\ 0, & \text{otherwise} \end{cases} \tag{3.50}$$

The primary concept of MPC is to determine an optimal control input for power switches by solving an online optimisation problem and implementing the resulting optimal control solution, using a one-step receding horizon control method. For the sake of simplicity, in this section, the output currents of the NPC inverters are expressed as a current vector in using a stationary orthogonal $\alpha\beta$-framework [143]. Thus,

$$i = \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = T_{\alpha\beta} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} \tag{3.51}$$

$$T_{\alpha\beta} = \frac{2}{3} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.52}$$

The output currents in $\alpha\beta$-framework can be expressed as follows:

$$i_\alpha = \frac{2}{3}(i_a - \frac{1}{2} i_b - \frac{1}{2} i_c) \tag{3.53}$$

$$i_\beta = \frac{\sqrt{3}}{3}(i_b - i_c) \tag{3.54}$$

Using the same $\alpha\beta$-framework transformation, the output voltage can be expressed in the same v_α and v_β form:

$$v_\alpha = \frac{2}{3}(v_{ao} - \frac{1}{2} v_{bo} - \frac{1}{2} v_{co}) \tag{3.55}$$

$$v_\beta = \frac{\sqrt{3}}{3}(v_{bo} - v_{co}) \tag{3.56}$$

Table 3.8 provides the switching states corresponding to the voltage space vectors.

Table 3.8: Switching States corresponding to Voltage Space Vectors

Switching States (u_i)	**Voltage Space Vector**V_n
NNN 000 PPP	$V_0 = 0$
P00 0NN	$V_1 = \frac{1}{3}V_{dc}$
PP0 00N	$V_2 = \frac{1}{3}V_{dc}e^{\frac{\pi}{3}j}$
0P0 N0N	$V_3 = \frac{1}{3}V_{dc}e^{\frac{2\pi}{3}j}$
0PP N00	$V_4 = \frac{1}{3}V_{dc}e^{\pi j}$
00P NN0	$V_5 = \frac{1}{3}V_{dc}e^{\frac{4\pi}{3}j}$
P0P 0N0	$V_6 = \frac{1}{3}V_{dc}e^{\frac{5\pi}{3}j}$
P0N	$V_7 = \frac{\sqrt{3}}{3}V_{dc}e^{\frac{\pi}{6}j}$
0PN	$V_8 = \frac{\sqrt{3}}{3}V_{dc}e^{\frac{\pi}{2}j}$
NP0	$V_9 = \frac{\sqrt{3}}{3}V_{dc}e^{\frac{5\pi}{6}j}$
N0P	$V_{10} = \frac{\sqrt{3}}{3}V_{dc}e^{\frac{7\pi}{6}j}$
0NP	$V_{11} = \frac{\sqrt{3}}{3}V_{dc}e^{\frac{3\pi}{2}j}$
PN0	$V_{12} = \frac{\sqrt{3}}{3}V_{dc}e^{\frac{11\pi}{6}j}$
PNN	$V_{13} = \frac{2}{3}V_{dc}$
PPN	$V_{14} = \frac{2}{3}V_{dc}e^{\frac{\pi}{3}j}$
NPN	$V_{15} = \frac{2}{3}V_{dc}e^{\frac{2\pi}{3}j}$
NPP	$V_{16} = \frac{2}{3}V_{dc}e^{\pi j}$
NNP	$V_{17} = \frac{2}{3}V_{dc}e^{\frac{4\pi}{3}j}$
PNP	$V_{18} = \frac{2}{3}V_{dc}e^{\frac{5\pi}{3}j}$

The instantaneous active and reactive powers can be calculated on the basis of the procedure outlined in [150]:

$$P = i_\alpha v_\alpha + i_\beta v_\beta \tag{3.57}$$

$$Q = i_\beta v_\alpha + i_\alpha v_\beta \tag{3.58}$$

For Equation 3.57 and Equation 3.58, the current references can be obtained according to the desired active and reactive power, P^* and Q^*, supplied to the grid:

$$i_\alpha^* = \frac{P^* v_\alpha - Q^* v_\beta}{v_\alpha^2 + v_\beta^2} \tag{3.59}$$

$$i_\beta^* = \frac{P^* v_\beta + Q^* v_\alpha}{v_\alpha^2 + v_\beta^2} \tag{3.60}$$

In conventional MPC algorithms, Equation 3.41 and Equation 3.42 necessitate 27 current predictions. If higher-level topologies for multilevel inverters are a feature of an application, the disadvantages of using a conventional MPC algorithm (i.e., the computational burden) will become more prominent. The modified MPC algorithm detailed below implements expected voltage vector tracking to replace current tracking in the cost function. Thus, it reduces the number of current predictions required by a factor of 27, significantly bringing down the computational cost.

3.8.2 Expected Voltage Vector

On the basis of Equation 3.42, the voltage vector, $V(k)$, can be expressed as follows:

$$V(k) = \frac{L}{T_s} i(k+1) + (R - \frac{L}{T_s}) i(k) + e(k) \tag{3.61}$$

In this equation, $i(k+1)$ represents the desired current for the next sampling period. If $i(k+1)$ is replaced by $i^*(k+1)$ which means using the reference current to replace the desired current in the next sampling period, then the expected voltage vector, V_e, is generated by the system instead, i.e.:

$$V_e(k) = \frac{L}{T_s} i^*(k+1) + (R - \frac{L}{T_s}) i(k) + e(k) \tag{3.62}$$

3.8.3 Cost Function Design

MPC is primarily concerned with determining an optimal control input in relation to power switches. This is done by addressing an online optimisation problem, which is then used as a form of receding horizon control [21][30]. The overall objective function of the optimisation problems concerns system performance. As indicated above, the cost function, J, has three parts:

$$J(k+1) = J_1(k+1) + J_2(k+1) + J_3(k+1) \tag{3.63}$$

In the modified cost function, J_1 is designed to track the difference between the expected voltage vector and the 27 voltage vectors that are generated by the NPC inverters. J_2 and J_3 retain the same objectives mentioned above (in section 3.3). Thus, J_2 maintains the neutral point balance of the capacitor voltages in DC-link and J_3 reduces the switching frequency. Looking at each part in more detail:

$$J_1(k+1) = |V_{e\alpha}(k+1) - V_{n\alpha}(k+1)|^2 + |V_{e\beta}(k+1) - V_{n\beta}(k+1)|^2 \tag{3.64}$$

where, the 27 voltage vectors generated by the NPC inverters are represented by V_n, as in Table 3.8. V_e is the expected voltage vector. J_1 in the modified cost function is the key difference from a conventional MPC algorithm. This is the part that can reduce the computational burden associated with current predictions by a factor of 27.

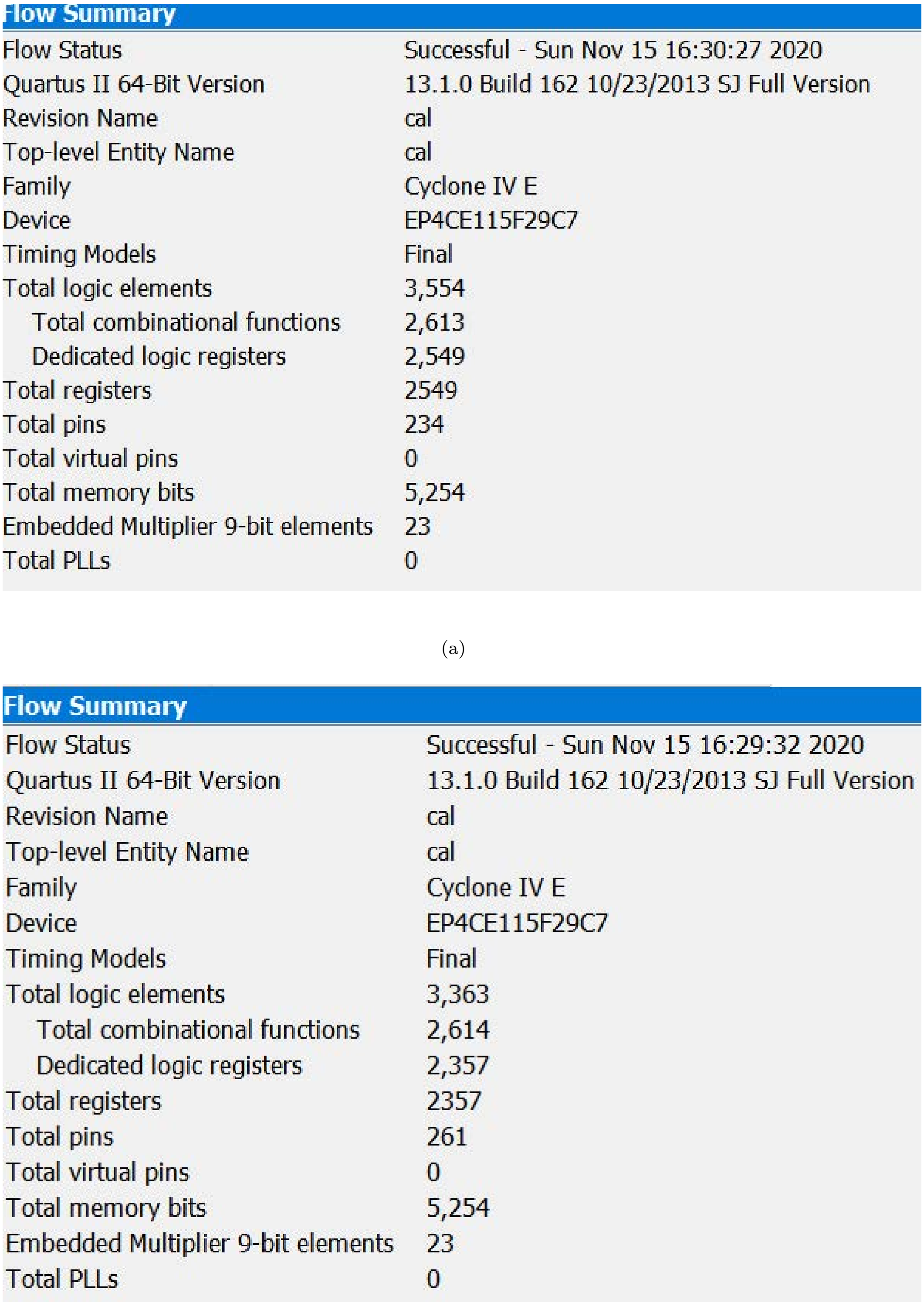
In the hardware controller (FPGA), resources and time consumed by J_1 in the proposed algorithm can be quantified compared to J_1 in the conventional algorithm. The FPGA model is Intel EP4CE115F29C7, and the development environment is Quartus II 64-Bit. The calculation precision is single-precision floating-point type. By computing in this hardware FPGA controller, the resources consumed by J_1 in the proposed algorithm and J_1 in the conventional algorithm are indicated in Figure 3.18. The experiment results in Figure 3.18 show that the total logic elements consumed by J_1 in the conventional algorithm are 3554, which are more than the 3363 total logic elements consumed by J_1 in the proposed algorithm. Thus, J_1 in the proposed algorithm can save the resources in FPGA controller. Due to the time consumed, Table 3.9 is obtained from this experiment. During this experiment in FPGA controller, J_1 in the proposed algorithm consumes 109 clock cycles, while J_1 in the conventional algorithm consumes 2565 clock cycles. The proposed algorithm takes much less time than the conventional algorithms. Therefore, the modified algorithm can reduce the computational burden from the resources and time consumed two points.

Table 3.9: Time consumed by J_1 in conventional algorithm and J_1 in the proposed algorithm based on FPGA controller

	Conventional method	**Proposed method**
Clock Cycle	2565	109

$$J_2(k+1) = |u_{c1}(k+1) - u_{c2}(k+1)|^2 \tag{3.65}$$

$u_{c1}(k+1)$ and $u_{c2}(k+1)$ are the DC-link capacitor voltages. This part of the cost function focuses on keeping the DC-link capacitor voltages stable.



```
low Summary
Flow Status                          Successful - Sun Nov 15 16:30:27 2020
Quartus II 64-Bit Version            13.1.0 Build 162 10/23/2013 SJ Full Version
Revision Name                        cal
Top-level Entity Name                cal
Family                               Cyclone IV E
Device                               EP4CE115F29C7
Timing Models                        Final
Total logic elements                 3,554
    Total combinational functions    2,613
    Dedicated logic registers        2,549
Total registers                      2549
Total pins                           234
Total virtual pins                   0
Total memory bits                    5,254
Embedded Multiplier 9-bit elements   23
Total PLLs                           0
```

(a)

```
Flow Summary
Flow Status                          Successful - Sun Nov 15 16:29:32 2020
Quartus II 64-Bit Version            13.1.0 Build 162 10/23/2013 SJ Full Version
Revision Name                        cal
Top-level Entity Name                cal
Family                               Cyclone IV E
Device                               EP4CE115F29C7
Timing Models                        Final
Total logic elements                 3,363
    Total combinational functions    2,614
    Dedicated logic registers        2,357
Total registers                      2357
Total pins                           261
Total virtual pins                   0
Total memory bits                    5,254
Embedded Multiplier 9-bit elements   23
Total PLLs                           0
```

(b)

Figure 3.18: Resources consumed by J_1 in the proposed algorithm and J_1 in conventional algorithm based on FPGA controller: (a) The resources consumed by J_1 in the conventional algorithm, and (b) The resources consumed by J_1 in the proposed algorithm.

$$J_3(k+1) = |S_a(k) - S_a(i_{opt})|^2 + |S_b(k) - S_b(i_{opt})|^2 + |S_c(k) - S_c(i_{opt})|^2 \tag{3.66}$$

Here, $S_x(k)$ and $S_x(i_{opt})$ $(x = a, b, c)$ express the optimal switching states in the time interval k and the previous time interval $k-1$, respectively. J_3 concentrates on limiting the number of power switch commutations. In this final part of the cost function, the switching state that involves the fewest power switch commutation is given priority.

The control process for the grid-connected NPC inverters involves solving a constrained multi-freedom and multi-objective optimisation problem. The 27 switching states corresponding to the voltage space vectors are the multi-freedom control actions. The control objectives include current tracking, neutral point balancing and switching frequency reduction. Thus, the process does not focus on attaining single optimal performance, but rather upon inclusive consideration of multiple-objectives. Within these multiple control objectives, current tracking and neutral point balancing are hard constraints, while switching frequency reduction is a soft constraint. For the current tracking, the proposed MPC algorithm considers the grid-side current to be the control target in case of any overcurrent problems. The neutral point voltages of the DC-link capacitors are allowed some fluctuation, depending on the size of the capacitors and any specific system requirements.

3.8.4 Optimisation Process

ψ is introduced to express switching states.

$$\psi \triangleq \left\{ u = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \in \mathbb{R}^3 \mid u_x \in \{-1, 0, 1\}, x = a, b, c \right\} \tag{3.67}$$

In fact, $\psi = \{u_1, u_2, \ldots, u_{27}\}$ in NPC inverters, which are shown in Table 3.2 and a, b, and c represent the three phases.

The optimal control can be stated as:

$$\begin{aligned} u_{opt}(k) = \arg \min_{u(k) \in \psi} \quad & \tilde{J}\left(u_i(k)\right) \triangleq J(k) \\ \text{subject to} \quad & (\textit{Equation } 3.40) \quad (\textit{Equation } 3.42) \\ & (\textit{Equation } 3.45) \quad (\textit{Equation } 3.46) \end{aligned} \tag{3.68}$$

The cost function J is used to find the selected voltage vector, $u_{opt}(k)$, which minimises the cost function as the control input.

3.8.5 Simulation Results

The proposed MPC algorithm was verified by using a simulated $600\,V$ $32\,kVA$ system. The parameters of the system are given in Table 3.10. Both the grid-connected NPC inverters and the proposed MPC algorithm were implemented in MATLAB Simulink. To test the robustness of the proposed MPC controller, the active power reference P^* was stepped down from $32\,kW$ to $23\,kW$ at $0.3\,s$, then increased to $42\,kW$ at $0.5\,s$. At the same time, the reactive power reference, Q^*, was maintained at zero to ensure a unity power factor.

Table 3.10: System Parameters and Value

Parameters	**Value**
DC-link voltage V_{dc}	$600\,V$
Load resistance R	$0.02\,\Omega$
Load inductance L	$1.5e-3\,H$
DC-link capacitance C	$4.7e-4\,F$
Grid voltage (phase-to-phase RMS) V_g	$380\,V$
Grid frequency f_g	$50\,Hz$
Sampling period T_s	$8e-5\,s$

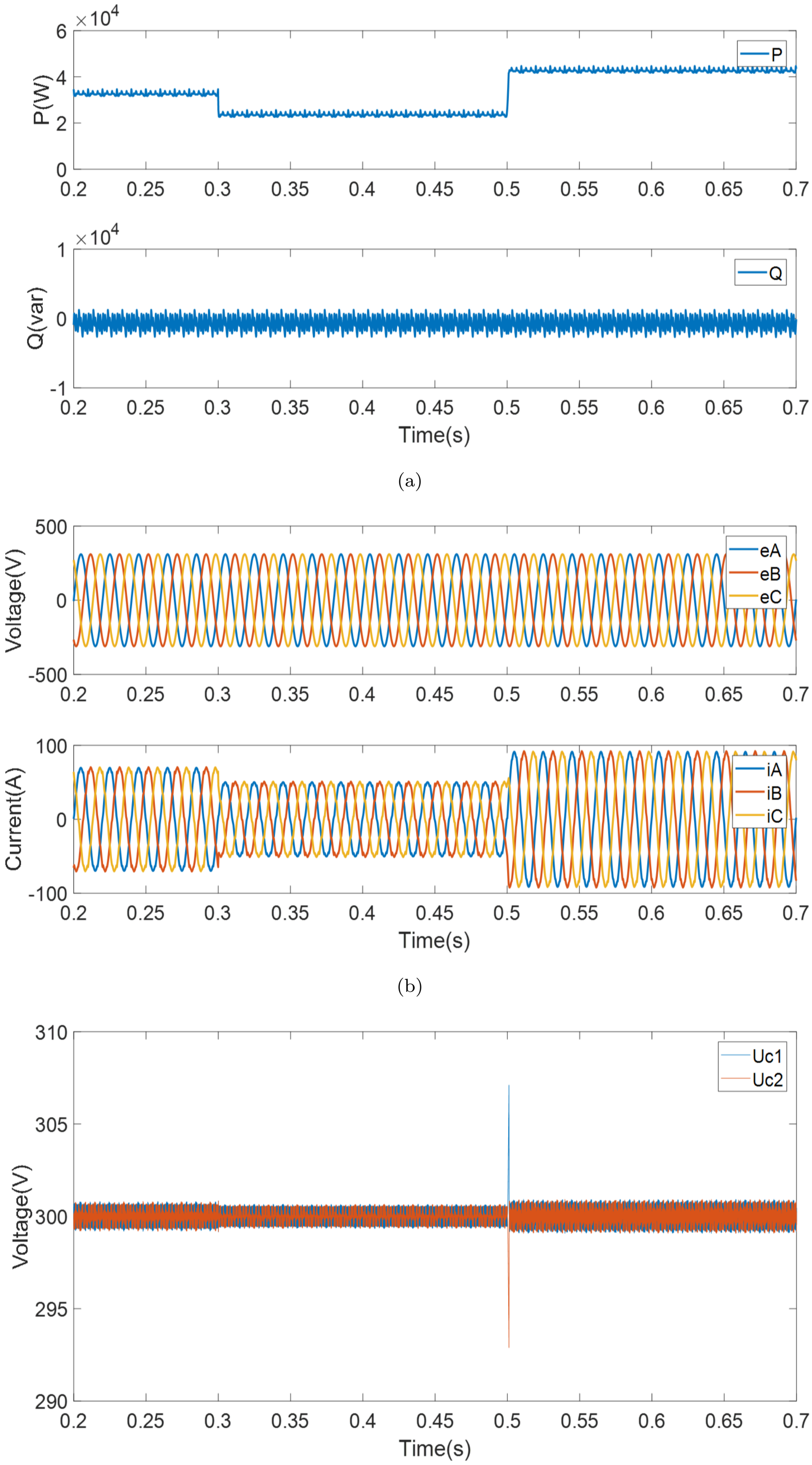
The simulation results are shown in Figure 3.19. Figure 3.19(a) shows the active power, P, and the reactive power, Q. From this figure it can be seen that the proposed MPC algorithm was able to track the active and the reactive power even when the active power reference changed (i.e., stepping down from $32\,kW$ to $23\,kW$ at $0.3\,s$, then increasing to $42\,kW$ at $0.5\,s$).

The grid voltages, e_A,e_B,e_C, and the grid currents, i_A,i_B,i_C, are shown in Figure 3.19(b). The total harmonic distortion (THD) values for the grid currents are summarised in Table 3.11. For each different active power reference, they met the requirements of the $IEEE\ Standard\ 519-2014$. Thus, the proposed MPC algorithm can implement high-quality output currents and voltages.

The voltages of the DC-link capacitors , U_{c1} and U_{c2}, are shown in Figure 3.19(c). The RMS error for the DC-link capacitor fluctuation was $1.173\,V$. At $0.5\,s$, the active power reference stepped up from $23\,kW$ to $42\,kW$, an increase of 82.6%. At that instant, there was a ripple of $7.1\,V$ in the DC-link capacitor voltage. Then, the proposed MPC algorithm quickly (0.00123s) balanced the DC-link capacitor voltages. Thus, it can be

Table 3.11: The THD Values of the Grid Currents

Period (s)	0-0.3	0.3-0.5	0.5-1
Power (kW)	32	23	42
THD	2.85%	3.93%	2.81%
RMS(V)	1.173		
Switching frequency(kHz)	19.74		



(a)

(b)

(c)

Figure 3.19: Simulation results for the proposed MPC algorithm: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

seen that the proposed method is able to keep the DC-link capacitor voltages balancing during dynamic operating conditions.

3.9 Different Plants with Representative Parameters

A set of two different plants with representative parameters (Case A and Case B) have been used for the proposed algorithms in the thesis to verify performance. The two cases are representative of practical applications in industry and our daily life. Through these two different plants with representative parameters, the performance of the proposed MPC control algorithm can be better displayed. The contents of different plants with representative parameters (Case A and Case B) would be given in the following.

Case A: 3kV 1MW HVDC (high-voltage direct current) system, source from: [New 4.5 kV IGBT and diode chip set for HVDC Transmission Applications in infineon.com].

Case B: 600V 400kW UPS (uninterruptible power supply) application system, source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com].

Three MPC methods were suggested in this chapter, but only the third was validated. The first two proposed MPC algorithms use RL load as its load application. They are not utilised as a load in real life. The majority of studies begin with RL load to get preliminary findings. In Chapter 3, the third suggested MPC algorithm was expanded to a grid-connected situation. As a result, this section evaluated the third proposed MPC algorithm.

3.9.1 Case A

In Case A, the proposed MPC algorithm was verified by using a simulated $3\,kV$ $1\,MW$ system. The parameters of Case A are from the HVDC system, source from [New 4.5 kV IGBT and diode chip set for HVDC Transmission Applications in infineon.com]. To test the robustness of the system, the active power reference P^* was stepped down from $1\,MW$ to $0.6\,MW$ at $0.2\,s$, then went down to $0.22\,MW$ at $0.4\,s$. At $0.6\,s$, it would increase to $0.3\,MW$. At the same time, the reactive power reference, Q^*, was maintained at zero to ensure a unity power factor.

The results of Case A are shown in Figure 3.20 and Table 3.12. Figure 3.20(a) shows the active power, P, and the reactive power, Q. From this figure, it can be seen that the proposed MPC algorithm was able to track the active power and the reactive power even when the active power reference changed (i.e., stepping down from $1\,MW$ to $0.6\,MW$ at $0.2\,s$, then going up from $0.22\,MW$ at $0.4\,s$ to $0.4\,MW$ at $0.6\,s$). The grid voltages, e_A, e_B, e_C, and the grid currents, i_A, i_B, i_C, are shown in Figure 3.20(b). The total harmonic distortion (THD) values for the grid currents are summarised in Table 3.12.

Table 3.12: The Case A

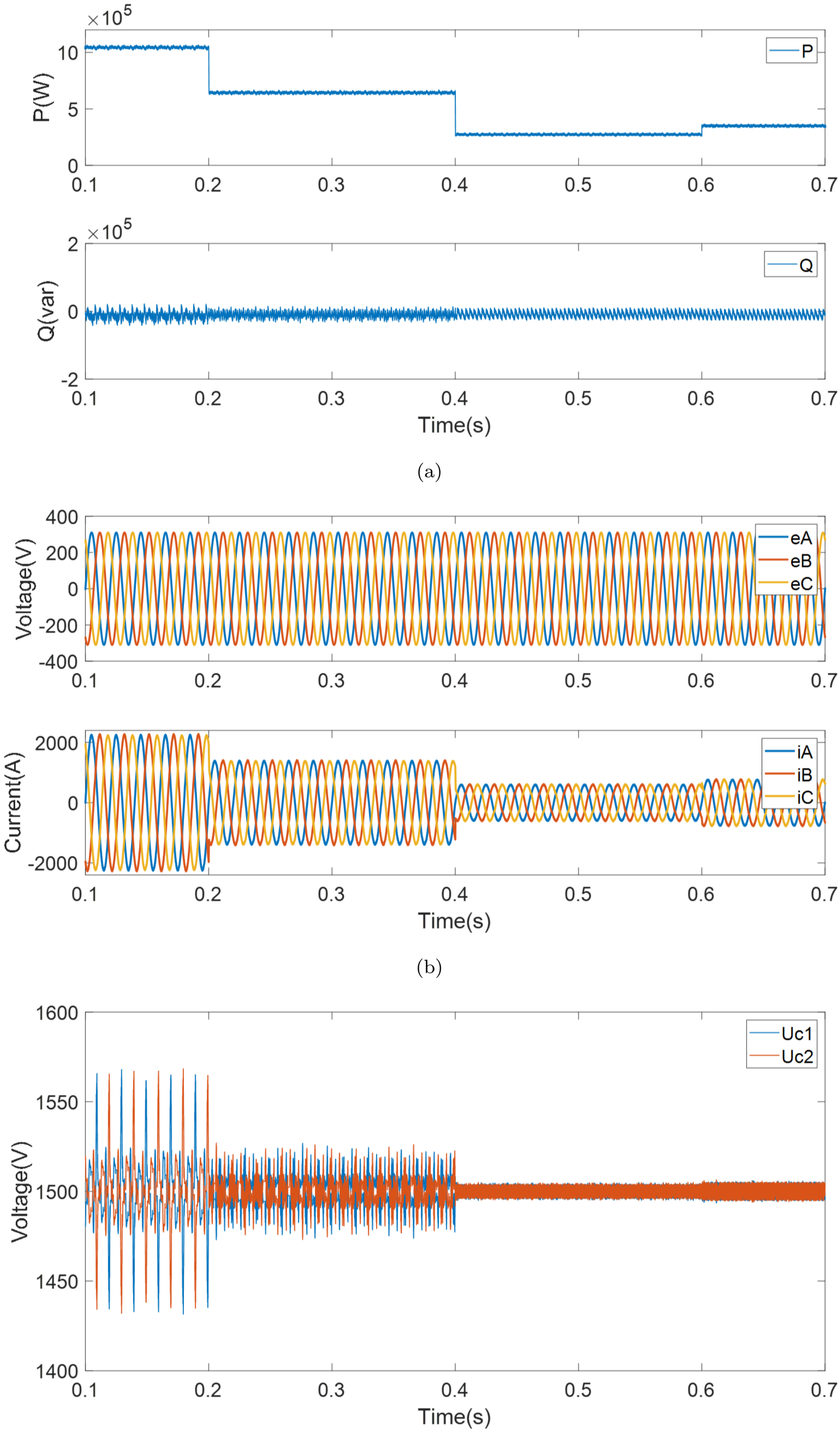
Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (MW)	1	0.6	0.22	0.4
THD	1.06%	1.59%	3.13%	2.45%
RMS(V)	19.32			
Switching frequency(kHz)	8.675			

The values of the THD are 1.06% at $1\,MW$, 1.59% at $0.6\,MW$, 3.13% at $0.22\,MW$, and 2.45% at $0.4\,MW$. For each different active power reference, they met the requirements of the $IEEE\ Standard\ 519-2014$. Thus, the proposed MPC algorithm can implement high-quality output currents and voltages. The voltages of the DC-link capacitors, U_{c1} and U_{c2}, are shown in Figure 3.20(c). The RMS error for the DC-link capacitor fluctuation was $19.32\,V$. The waveform of the DC-link capacitor fluctuation is shown in Figure 3.20(c).

3.9.2 Case B

In Case B, the proposed MPC algorithm was verified using a simulated $600\,V$ $400\,kW$ system. The parameters of Case B are from UPS application system Source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com]. In order to test the robustness of the system, the active power reference P^* was stepped down from $400\,kW$ to $450\,kW$ at $0.2\,s$, then went down to $250\,kW$ at $0.4\,s$. At $0.6\,s$, it would go up to $300\,kW$. At the same time, the reactive power reference, Q^*, was maintained at zero to ensure a unity power factor.

The waveform results of Case B are shown in Figure 3.21, and the summarised data results are indicated in Table 3.13. Figure 3.21(a) shows the active power, P, and the reactive power, Q. In terms of this figure, the proposed MPC algorithm was able to track the active power and the reactive power even when the active power reference changed (i.e., stepping up from $400\,kW$ to $450\,kW$ at $0.2\,s$, then going up from $250\,kW$ at $0.4\,s$ to $300\,kW$ at $0.6\,s$). The grid voltages, e_A, e_B, e_C, and the grid currents, i_A, i_B, i_C, are shown in Figure 3.21(b). From the waveforms of the grid currents and the grid voltages, the stable output was obtained. The total harmonic distortion (THD) values for the grid currents are summarised in Table 3.13. The values of the THD are 2.82% at $400\,kW$, 2.51% at $450\,kW$, 4.35% at $250\,kW$, and 3.70% at $300\,kW$. They met the requirements of the $IEEE\ Standard\ 519-2014$ for each different active power reference. Thus, the high-quality output currents and voltages were implemented in the proposed MPC algorithm. The voltages of the DC-link capacitors, U_{c1} and U_{c2}, are shown in Figure 3.21(c). The waveform of the DC-link capacitor fluctuation is shown in Figure 3.21(c). The RMS error for the DC-link capacitor fluctuation was $7.74\,V$.



(a)

(b)

(c)

Figure 3.20: Results for the Case A: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

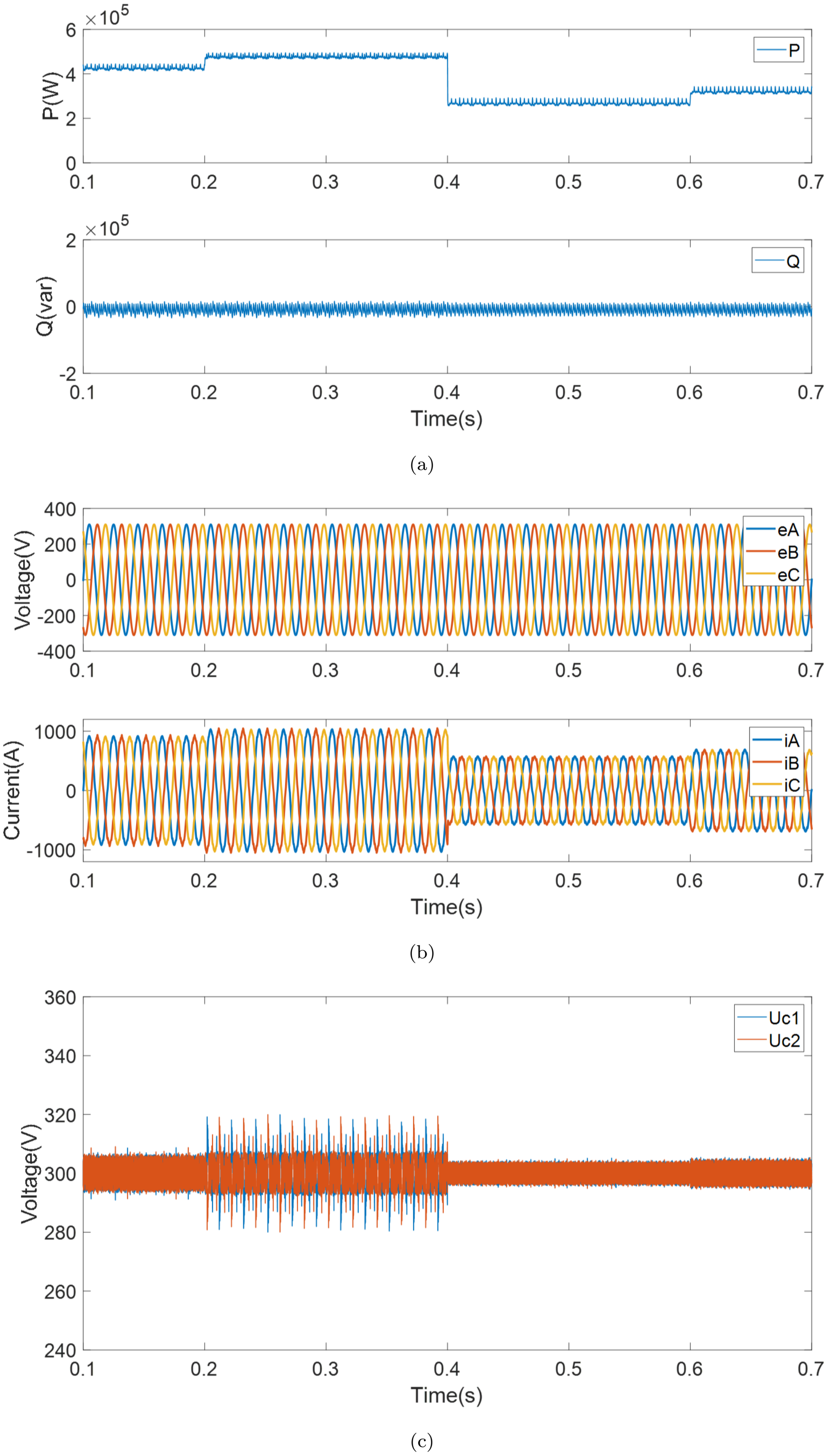


Figure 3.21: Results for the Case B: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 3.13: The Case B

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	400	450	250	300
THD	2.82%	2.51%	4.35%	3.70%
RMS(V)	7.74			
Switching frequency(kHz)	10.200			

3.10 Summary

In this chapter, an MPC algorithm with reduced switching frequency has been firstly proposed for 3-level NPC inverters. Then, this MPC algorithm was extended to a multi-step MPC algorithm with the reduced computational burden to handle current variation in a 3-level NPC inverter system. Finally, this MPC algorithm continued to be extended to 3-level grid-connected NPC inverters with the reduced computational burden of prediction. The effectiveness of the proposed MPC algorithms has been identified. The key findings from this chapter are:

- An MPC algorithm with reduced switching frequency has been proposed for 3-level NPC inverters. Compared with a conventional MPC algorithm, the proposed method can efficiently reduce switching frequency and improve the quality of output currents. Moreover, compared with the industrial linear PI controller, this proposed MPC algorithm not only retains the advantages of the conventional MPC such as fast response and handling multiple constraints, but also indicates better performance than the industrial linear PI controller with respect to the THD of the output current. Finally, the robustness of the proposed MPC algorithm is verified by the current reference variation, which illustrates its fast dynamic response and good robustness.
- A multistep MPC algorithm designed to handle current variation in a 3-level NPC inverter system has been presented. The results of a conventional MMPC algorithm and the proposed MMPC algorithm indicate that the proposed algorithm can achieve almost the same output current THD under conditions of both nominal operation and current variation. However, the proposed algorithm reduces the number of calculations from 729 to 54 while still considering the same space voltage vectors in the cost function. In addition, the proposed algorithm does not need to be tuned with weighting factors and can maintain advantages associated with the original MPC algorithm, such as the handling of multiple constraints (current tracking and capacitor voltage balancing) and a rapid response to current variation.
- A model predictive control algorithm for reducing the computational burden of prediction has been proposed in this chapter. In this algorithm, a desired voltage

vector is applied to replace the current prediction in the cost function. Therefore, the algorithm can reduce the number of currents predictions in the optimisation process by a factor of 27. The proposed algorithm was applied in a simulated grid-connected NPC inverter-based system to assess its effectiveness. During dynamic operation, the active power reference P^* was stepped down from $32\,kW$ to $23\,kW$ at $0.3\,s$, then increased to $42\,kW$ at $0.5\,s$. The THD values of the output currents in relation to these stepped changes were 2.85% at $32\,kW$, 3.93% at $23\,kW$ and 2.81% at $42\,kW$, respectively. This meets the requirements of the $IEEE\ Standard\ 519-2014$. Alongside this, the RMS error for the DC-link capacitor fluctuation was only $1.173\,V$. Thus, the proposed MPC algorithm is able to effectively implement high-quality output in terms of low harmonic currents and active and reactive power tracking, and capacitor voltage balancing.

Chapter 4

Model Predictive Control of 3-level NPC Inverters based on Automatic Selection of Weighting Factors

In this chapter, an MPC algorithm for NPC grid-connected inverters is proposed with automatic selection of weighting factors. The main objective of this proposed algorithm is to reduce switching frequency and to provide for the automatic selection of weighting factors without the need for trial-and-error across different dynamic working conditions. The algorithm can also achieve active power tracking and maintain neutral point balancing functionalities. These various objectives are achieved through the use of a modified, 3-part cost function and the adoption of a two-dimensional fuzzy logic control scheme. The effectiveness of the proposed algorithm is verified using the results of grid-connected NPC inverters simulation, which show that the switching frequency can be reduced by at least 30% when compared to conventional MPC methods.

4.1 Introduction

Multilevel inverters are a vital aspect of being able to meet the emerging requirements for high-power applications and the incorporation of renewable resources in the grid [22][151]. Innovation in the field of renewable energy generation is moving at a rapid pace. However, renewable sources, including photovoltaics, are often unstable, making it essential that an inverter grid-connected system is able to actively monitor the active power in an efficient manner [152][153]. As a result, they have begun to attract an increasing amount of attention from both industry and academia.

Neutral Point Clamped (NPC) inverters offer the advantages of being able to split DC-link voltages, while minimizing switching losses and inducing smaller output current ripples [12][152]. They have therefore become a particular focus for research. Unfortunately, the use of power switches in grid-connected NPC inverters makes the system nonlinear, thus generating unwanted complexity in the control process. Conventional solutions to this have been mainly based on average state-space modelling and related modulation techniques, which include cascaded control structures. These standard methodologies are associated with a number of explicit constraints. In particular, when modelling, the linearisation has to be associated with a specified operating point [154]. The tuning procedure for the controller is already complex, so any further alterations to the operating point compound the problem. However, recent advances in fast microprocessors and DSP technologies offer the possibility of some novel solutions, including hysteresis current control, sliding mode control and model predictive control (MPC) [152]. Amongst these methodologies, MPC provides a means of overriding the cascaded control structures that limit the effectiveness of the most standard methods. It also presents a straightforward way of merging the optimisation specifics and dispensing with the other limitations associated with existing systems [22]. When directly compared to established methods, these benefits of using MPC result in a clearly enhanced system performance.

A key aspect of improving the efficiency of multilevel inverters is to reduce their switching frequencies [30][117]. At present, they are associated with a high switching frequency, resulting in a loss of energy from the power semiconductors. This characteristic limits the scope for applying MPC methods, especially in medium-voltage high-power systems. A certain amount of research works has been devoted to this problem [26][27][30]. Despite these existing control strategies for reducing switching frequencies, the topic remains an open issue.

Another aspect of the controls available through MPC that can also facilitate performance optimisation is its ability to tune weighting factors. Weighting factor optimisation is currently a topic of intense interest in research because of the lack of rigorous systematic design methodologies [22][34]. Some methods [22][34][35][36] addressed this problem, but these approaches still determined the appropriate weighting factors empirically or by extensive simulations. The automatic selection of weighting factors in the cost function therefore remains an ongoing research challenge for the MPC of power electronics converters [36].

To resolve these issues, this chapter proposes a distinct MPC algorithm based on the automatic selection of weighting factors for grid-connected NPC inverters to reduce switching frequency. Unlike a conventional MPC algorithm, the proposed MPC algorithm is able to automatically select the weighting factors online without resorting to trial-and-error. The algorithm's main objective is to obtain a lower switching frequency by monitoring the active power across a variety of working situations. The approach centres upon the use of a two-dimensional fuzzy logic control technique that is used to systematically identify the weighting factors within the cost function. Two-dimensional fuzzy logic is a robust method that makes it possible to avoid the use of a constant for the weighting factor that typically features in standard MPC algorithms. The input for a normal fuzzy logic control technique is the error between a controlled variable and its given input value. This error can differ to reflect the dynamic characteristics of a process. The inputs for a two-dimensional fuzzy logic control scheme are the errors between the controlled variable and their given input values and the rates of error change. This correlates more closely with the constantly changing output of a control process. The design of the two-dimensional fuzzy logic control scheme being used here will be described in the following part. To date, the automatic selection of weighting factors using a two-dimensional fuzzy logic control scheme has not been reported for grid-connected NPC inverter systems. In addition to reducing the switching frequency, through the newly formulated cost function, the proposed MPC algorithm can provide active power tracking across various working conditions. A simulation of a grid-connected NPC inverter system was used to assess the performance of the proposed MPC algorithm, and this confirmed its effectiveness. The proposed algorithm therefore offers a new way of dealing with the complexity typically associated with the use of grid-connected NPC inverters and thus potentially enhancing their performance in the context of renewable energy resource applications.

The rest of this chapter is organised as follows: Control objectives are introduced in section 4.2. A description of the proposed MPC algorithm is provided in section 4.3. Next, the simulation results are presented by nominal operation, dynamic operation and parameter sensitivity in section 4.4. The last part gives the conclusions of this chapter in section 4.6.

4.2 Control Objectives

The proposed MPC algorithm has three control objectives: reference tracking; neutral point balancing; and switching frequency reduction. Reference tracking aims to minimise the error between the reference current value and the predicted current value. Neutral point balancing aims to create a balance across the capacitor voltages by minimising $|u_{c1} - u_{c2}|$. It is essential to balance the voltage in NPC inverters to avoid any possible damage to the power electronic components. The key control objective, though, is to reduce the switching frequency of the power switches. In the following section, the relationship between the design of the MPC controller and these objectives will be examined more closely.

4.3 Model Predictive Controller Design

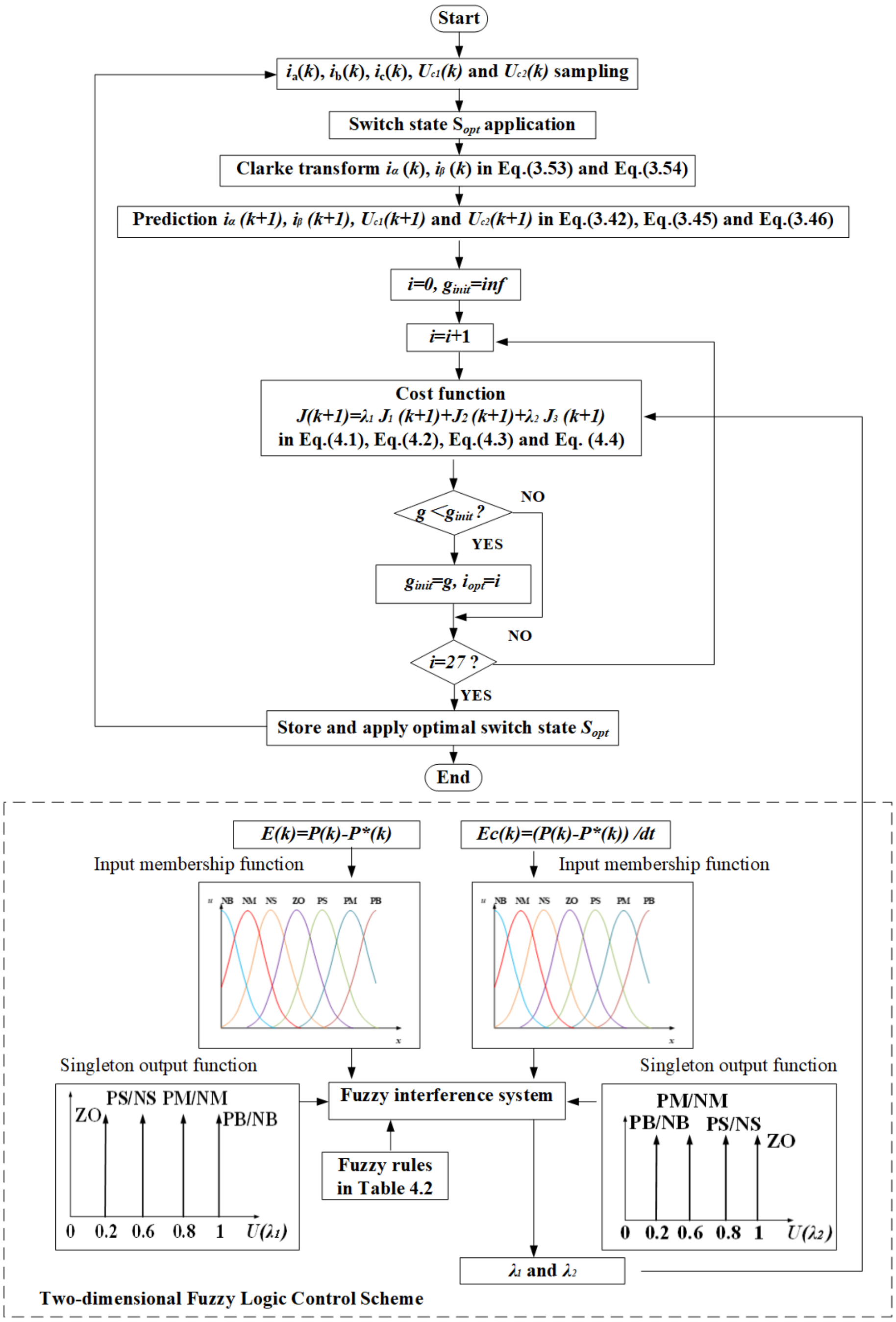


Figure 4.1: Proposed MPC algorithm with automatic selection of weighting factors across different working conditions.

4.3.1 Proposed Model Predictive Control Algorithm

This section presents a novel cost function in which the weighting factors are selected automatically using a two-dimensional fuzzy logic control scheme across the different working conditions. The overall system model of a grid-connected NPC inverter system was presented in section 3.8.1. The state definition for each phase and the switching states corresponding to voltage space vectors are shown in Table 3.7 and Table 3.8 separately. The proposed MPC algorithm is shown in Figure 4.1. There are multiple constraints in the new cost function, J. The first part, J_1, focuses on tracking the output currents. The second part, J_2, maintains the stability of the capacitor voltage and controls the neutral point voltages. The last part, J_3, decreases the switching frequency and limits the switching loss.

MPC is primarily concerned with determining an optimal control input in relation to the power switches. This is done by addressing an online optimisation problem, which is then used as a form of receding horizon control [21][30]. The overall objective function of the optimisation problems concerns system performance. As indicated above, the cost function, J, has three parts:

$$J(k+1) = \lambda_1 J_1(k+1) + J_2(k+1) + \lambda_2 J_3(k+1) \tag{4.1}$$

Within this, λ_1 and λ_2 are the weighting factors for J_1, which tracks the output currents, while J_3 decreases the switching frequency. So, taking each part more specifically:

$$J_1(k+1) = |i_\alpha(k+1) - {i_\alpha}^*(k+1)|^2 + |i_\beta(k+1) - {i_\beta}^*(k+1)|^2 \tag{4.2}$$

where, $i_\alpha(k+1)$ and $i_\beta(k+1)$ represent the current predictions in terms of the system model; and $i_\alpha^*(k+1)$ and $i_\beta^*(k+1)$ stand for the reference current. As noted, this part is dedicated to tracking the output currents.

$$J_2(k+1) = |u_{c1}(k+1) - u_{c2}(k+1)|^2 \tag{4.3}$$

$u_{c1}(k+1)$ and $u_{c2}(k+1)$ are the DC-link capacitor voltages. This part focuses on keeping the DC-link capacitor voltages stable.

$$J_3(k+1) = |S_a(k) - S_a(i_{opt})|^2 + |S_b(k) - S_b(i_{opt})|^2 + |S_c(k) - S_c(i_{opt})|^2 \tag{4.4}$$

where $S_x(k)$ and $S_x(i_{opt})$ $(x = a, b, c)$ express the optimal switching states in the time interval, k and the last time interval, $k-1$, respectively. J_3 concentrates on limiting the number of power switch commutations. In this final part of the cost function, the switching state that involves the fewest power switch commutations is given priority.

The proposed control process for the grid-connected NPC inverters involves solving a constrained multi-freedom and multi-objective optimisation problem. The 27 switching states corresponding to the voltage space vectors are the multi-freedom control actions.

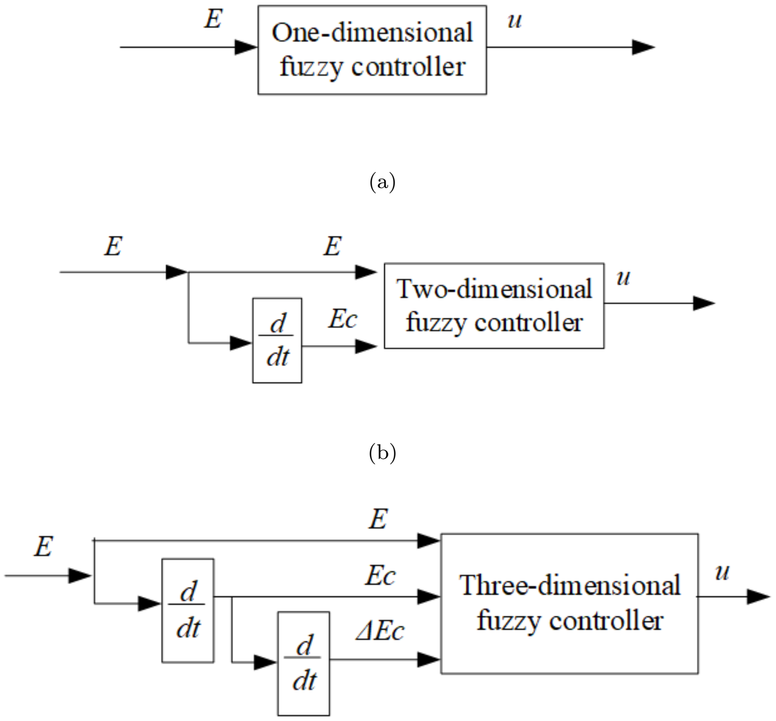
The control objectives include current tracking, neutral point balancing and switching frequency reduction. Thus, the process does not focus on attaining single optimal performance, but rather upon inclusive consideration of multiple objectives. Within these multiple control objectives, current tracking and neutral point balancing are hard constraints, while switching frequency reduction is a soft constraint. For the current tracking, the proposed MPC algorithm considers the grid-side current to be the control target in case of any overcurrent problems. The neutral point voltages of the DC-link capacitors are allowed some fluctuation, depending on the size of the capacitors and any specific system requirements. Once the above-mentioned hard constraints have been fulfilled, the soft constraint regarding switching frequency reduction comes into operation, assuming the system still has any multi-freedom control actions available. The optimal control quantity that satisfies this soft constraint can be considered as the final system control quantity. In the next section, the design of the automatic selection scheme for the weighting factors, λ_1 and λ_2, is explained.

4.3.2 Automatic Selection of Weighting Factors in Different Working Conditions

This section focuses on the automatic selection of weighting factors in the cost function. A two-dimensional fuzzy logic control scheme was developed for choosing these. In a conventional MPC algorithm, the weighting factors cannot adjust automatically across different working conditions. In the proposed algorithm, the appropriate weighting factors are determined dynamically online following a set of mathematical guidelines, obviating the need for trial-and-error or large-scale simulation. As a result, unlike conventional MPC algorithms, the proposed MPC algorithm can reduce the switching frequency and maintain robust parameter sensitivity to meet different operational circumstances as they arise.

Structure of the Two-Dimensional Fuzzy Logic Control Scheme

In the fuzzy logic control scheme, the number of input variables is defined as a dimension of the controller structure. There are three main structural forms [155], one-dimensional, two-dimensional and three-dimensional as shown in Figure 4.2. The input for a one-dimensional fuzzy controller is the error, E, between the value of the controlled variable and the given value of the input. This is not really able to reflect the dynamic characteristics of the process, so it is best used for first-order controlled systems. In a two-dimensional fuzzy controller, the input is the error, E, and the error change rate, E_c. This is much better able to reflect the dynamic characteristics of the output in the control process. In Figure 4.2, the error E, the error change rate, E_c, and the change rate of the error change rate, ΔE_c, are the inputs for the three-dimensional fuzzy logic control scheme. This kind of fuzzy controller has a complex structure and takes a long time to calculate. The proposed system therefore uses a two-dimensional fuzzy logic



(a)

(b)

(c)

Figure 4.2: Structure of fuzzy logic control scheme: (a) one-dimensional fuzzy controller, (b) two-dimensional fuzzy controller and (c) three-dimensional fuzzy controller.

control scheme, which can adequately reflect the dynamic characteristics and without imposing any excessive computational burden.

Mathematical Model of the Two-Dimensional Fuzzy Logic Control Scheme

The ranges of the error, E, and the error change rate, E_c, are: $[-E_{max}, E_{max}]$ and $[-E_{cmax}, E_{cmax}]$. The maximum values of the ranges are dependent on the system requirements and the rated operational state of the applications.

The quantitative range of the error, E, can be defined as:

$$X = \{-x, -x+1, \ldots, 0, \ldots, x-1, x\} \tag{4.5}$$

The quantitative range of the error change rate, E_c, can be defined as:

$$Y = \{-y, -y+1, \ldots, 0, \ldots, y-1, y\} \tag{4.6}$$

where, x and y refer to the error and the error change rate, quantifiable as $[0-E_{max}]$ and $[0-E_{cmax}]$, respectively. In fuzzy logic applications for the electric drives and power electronics [156][157], the output is a value in the range $[0, 1]$, while the input is from the interval $[-a, a]$, where $a > 0$ (e.g.,$a = 12$ or $a = 6$, as in [157]). As the choice of a does not make a significant difference to the final results, we have fixed it at $a = 12$, for simplicity. In most cases, $E_{max} \neq x$, and $E_{cmax} \neq y$, so the quantification factors K_E and K_{Ec} are defined as:

$$K_E = \frac{2x}{E_{max}} \tag{4.7}$$

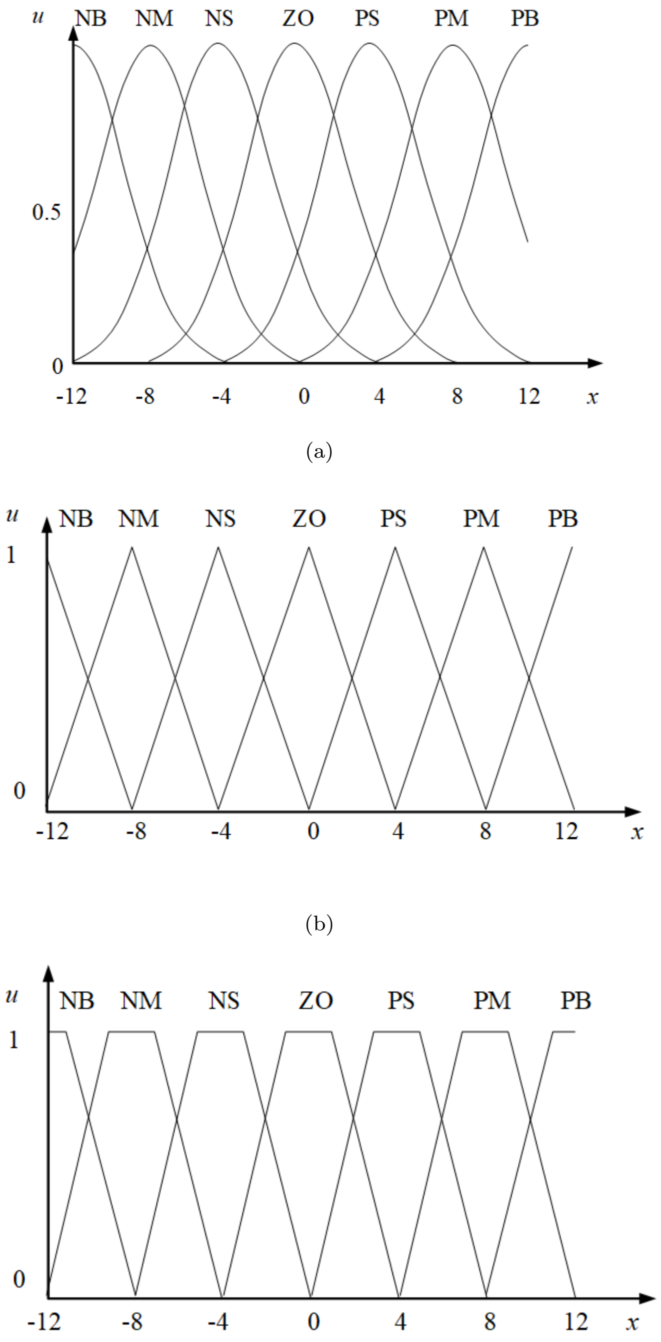
$$K_{Ec} = \frac{2y}{E_{cmax}} \tag{4.8}$$

In the simulation of the proposed grid-connected NPC inverter system, the active power reference stepped up from $1.5\,kW$ to $5\,kW$ at $0.3\,s$, subsequently decreased to $3.5\,kW$ at $0.4\,s$, and finally dropped to $2\,kW$ at $0.5\,s$. So, the maximum changes in the active power reference were at a kilowatt level. According to Equation 4.7- Equation 4.8 and [155][156], K_E and K_{Ec} are 0.00685 and 0.000000685, respectively. Therefore, any error, in this system, is always converted from Equation 4.7 - Equation 4.8 to Equation 4.5 - Equation 4.6.

Membership Function of the Two-Dimensional Fuzzy Logic Control Scheme

The proposed control scheme incorporates a Gaussian membership function. This is a robust algorithm in terms of classification and regression. A significant advantage of this function is its ability to provide a dependable estimate concerning its own uncertainty. In [156], a Gaussian membership function, triangular membership function and trapezoidal membership function were applied to electric drives and power electronics [157]. These three kinds of membership function are shown in Figure 4.3. When the membership function has a sharp peak, the resolution of the system control is higher. This is the case with triangular and trapezoidal membership functions [158]. Here, a small change in the input will result in a significant change in the output, because the sensitivity of the system is high. Thus, these kinds of membership functions (triangular or trapezoidal) are not suitable for the proposed system. When the shape of the curve of the membership function is relatively flat, as is the case with the Gaussian membership function, the resolution of the system control is low. When the input changes, changes in the output are not very drastic. Thus, the control characteristics are relatively flat, which offers good system stability [157][158]. Singleton membership functions are applied for the output u, which are recommended to use in power electronics applications [157][158].

The comparative results of application of the Gaussian, triangular and trapezoidal membership functions to the system are shown in Table 4.1. The results relate to the THD of the output currents, the cumulative three-phase switch changes and the switching frequency according to different working conditions (i.e., with active power references of: $40\,kW$, $60\,kW$, $22\,kW$ and $30\,kW$). In the case of the THD of the output currents,



(a)

(b)

(c)

Figure 4.3: Membership functions: (a) Gaussian membership function, (b) triangular membership function and (c) trapezoidal membership function.

the three kinds of membership functions achieved more or less the same performance. At 40 kW, the trapezoidal membership function had the lowest THD, 2.71%, with a difference between the Gaussian and triangular membership functions of 0.02% and 0.01%, respectively. At 60 kW and 22 kW, the Gaussian and trapezoidal membership functions attained the same THD values 1.82% and 4.86%, respectively, which were both less than the THD values for the triangular membership function (1.82% and 4.88%). In the 30 kW condition, the Gaussian membership function obtained the best THD value (3.58%), with the other two membership functions producing values of 4.88% (triangular) and 3.59% (trapezoidal).

Table 4.1: Comparative Performance of Different Membership Functions

Membership Function	**THD of Output Current Across Different Active Power Reference**			
	40 kW	**60 kW**	**22 kW**	**30 kW**
Gaussian	2.73%	1.82%	4.86%	3.58%
Triangular	2.72%	1.83%	4.88%	3.61%
Trapezoidal	2.71%	1.82%	4.86%	3.59%
	Cumulative Switch Changes Across Different Active Power Reference (times)			**Switching Frequency (kHz)**
	A Phase	**B Phase**	**C Phase**	
Gaussian	16490	16490	17000	4.164
Triangular	17720	17690	18840	4.488
Trapezoidal	17970	17990	18610	4.547

When it came to the cumulative three-phase switch changes and the switching frequencies, the Gaussian membership function obtained the lowest cumulative switch changes for each phase (16490 in A, 16490 in B and 17000 in C) and the lowest switching frequency (4.164 kHz). The difference between the triangular and trapezoidal membership functions was small: the switching frequencies (4.488 kHz and 4.547 kHz) and cumulative switch changes (17720 times in A phase, 17720 times in B phase, 17970 times in C phase and 17970 times in A phase, 17990 times in B phase, 18610 times in C phase). Above all, the Gaussian membership function performed best, so, a Gaussian membership function was applied in the proposed system.

Design of the Two-Dimensional Fuzzy Logic Control Scheme

The two-dimensional fuzzy logic control scheme is shown in Figure 4.4. As can be seen, the inputs of the scheme indicate the error (E) between the controlled variable (the measured active power, P_m) and the given input value (the active power, P) as well as the rate of change in the error (Ec). K_E and K_{Ec} are quantification factors. The online optimised weighting factors, λ_1 and λ_2, are defined to be the outputs of the two-dimensional fuzzy logic control scheme. The input and the output both include a fuzzy set. This control scheme also involves a Gaussian membership function, which is a robust algorithm in terms of classification and regression. A significant advantage of this function is its ability to provide a dependable estimate of its uncertainty. Finally, the control actions, u, are obtained from the two-dimensional fuzzy logic control scheme.

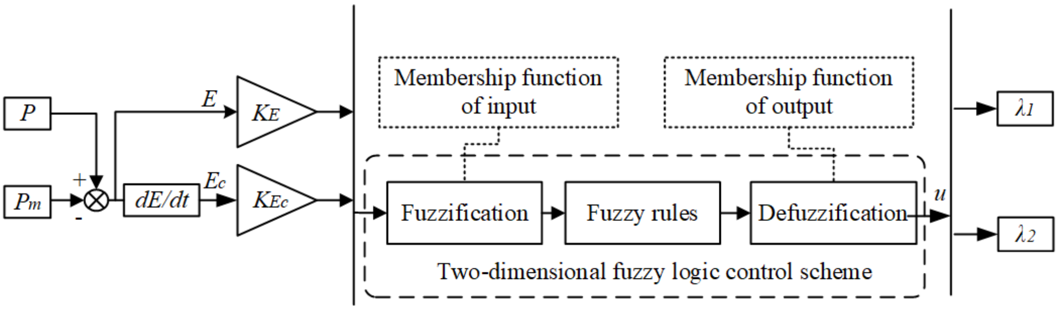


Figure 4.4: Two-dimensional fuzzy logic control scheme.

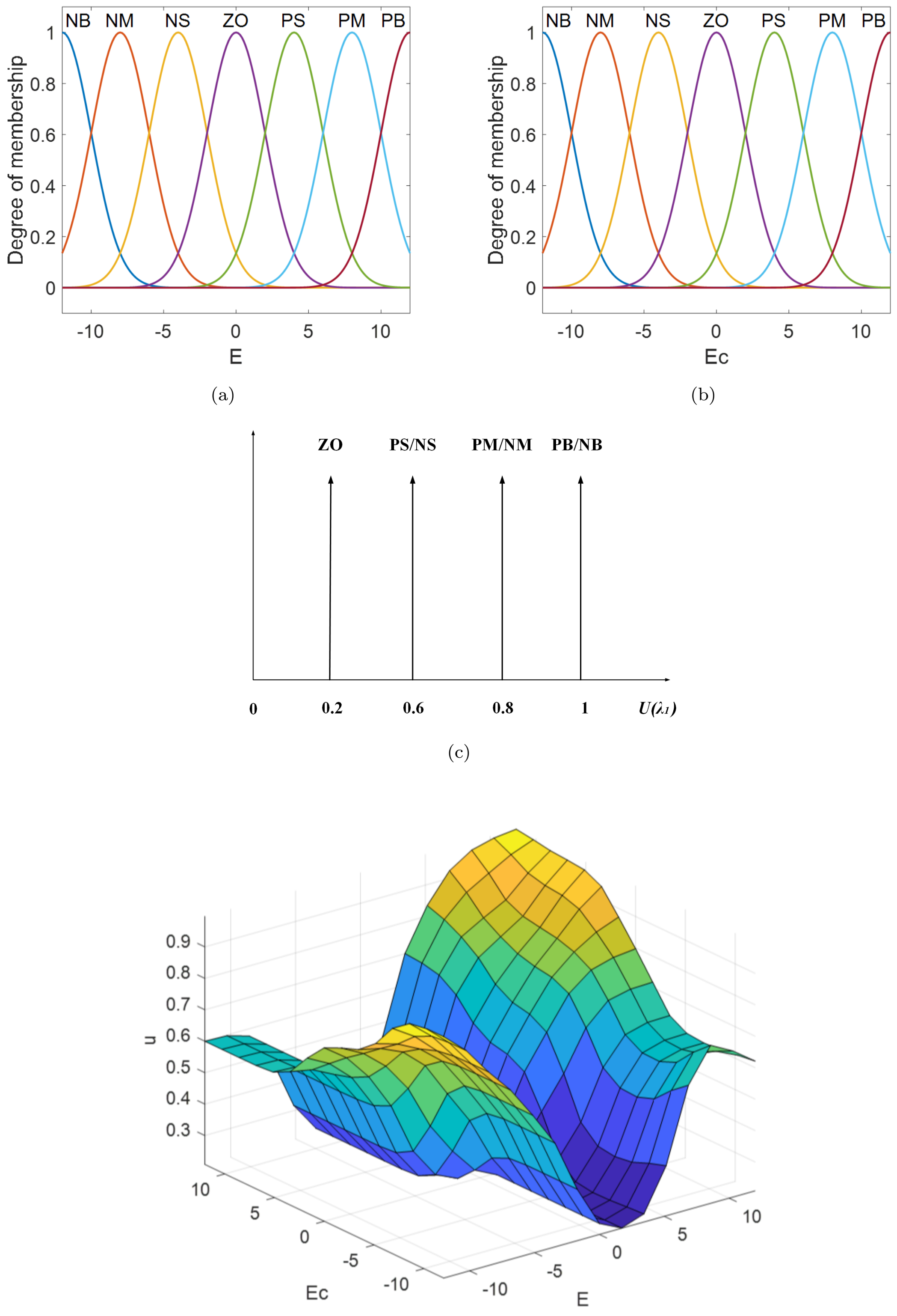
Design of the Fuzzy Rules

In order to achieve the automatic selection of weighting factors, the two-dimensional fuzzy logic control technique is developed. By following this control process, the appropriate values of the weighting factors λ_1 and λ_2 are dynamically determined by the two-dimensional fuzzy logic control scheme.

The current fuzzy rules should be consistent with the function of the weighting factors λ_1 and λ_2. The weighting factors λ_1 is applied to tracking the output currents, which can meet the requirements of limiting maximum current and keeping the output power stable for application safety in the cost function. At the same time, it brings into operation to predict the future values of AC terminal currents to track the reference currents. This constraint, which the weighting factors λ_1 is applied to, can be related to the normal operation of the system. If not satisfied, it will cause damage to the application equipment. Therefore, the weighting factors λ_1 is applied to a hard constraint. When the fuzzy rules are determined, the priority for the weighting factors λ_1 is given to meet the hard constraint.

As for the weighting factors λ_2, it is applied for the soft constraint, which can reduce switching frequency and decrease switching loss. The reduced switching frequency of the NPC inverters can be implemented by a low computational cost digital controller. Meanwhile, the decrease switching loss can help to improve the energy efficiency of the system. In terms of the system, when the current fuzzy rules are determined, the constraint applied by the weighting factors λ_2, no more than the priority of the constraint applied by the weighting factors λ_1.

In this proposed two-dimensional fuzzy logic control scheme, the inputs of the fuzzy controller are E and E_c. The automatic selection of weighting factors λ_1 and λ_2 are defined as the outputs of the controller. The input and output have a fuzzy set, shown in Figure 4.1, Figure 4.5 and Figure 4.6. The fuzzy set can be expressed as NB, NM, NS, ZO, PS, PM, PB, where: NB = negative big; NM = negative medium; NS = negative small; ZO = zero; PS = positive small; PM = positive medium and PB = positive big.



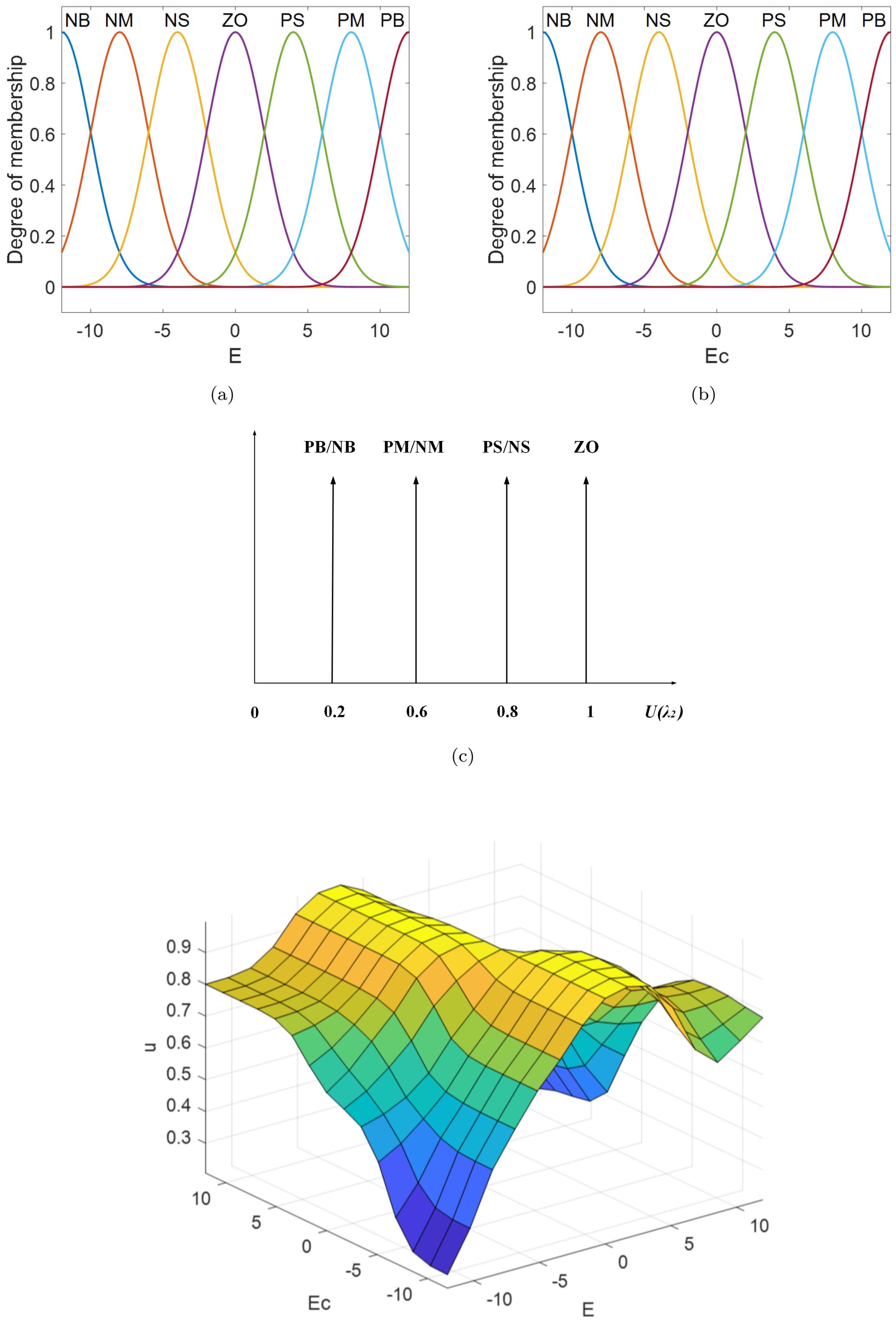
(a)

(b)

(c)

(d)

Figure 4.5: The degree of membership function and the curve of input and output changes in this two-dimensional fuzzy logic control scheme: (a) the degree of membership function for E in λ_1, (b) the degree of membership function for Ec in λ_1, (c) the degree of output membership function for u in λ_1 and (d) the curve of input and output changes for λ_1.



(a)

(b)

(c)

(d)

Figure 4.6: The degree of membership function and the curve of input and output changes in this two-dimension fuzzy logic control scheme: (a) the degree of membership function for E in λ_2, (b) the degree of membership function for Ec in λ_2, (c) the degree of output membership function for u in λ_2 and (d) the curve of input and output changes for λ_2.

This control scheme also involves a Gaussian membership function for the input variable, a robust algorithm in terms of classification and regression. A significant advantage of this function is its ability to provide a reliable estimate of its uncertainty. Meanwhile, the Singleton membership function is selected for the output variable due to its simplicity. Therefore, if the error, E, and the error change rate, E_c, are over a specific size, the weighting factor for λ_1 will implement a heavier penalty when tracking the currents. At the same time, the weighting factor for λ_2 will implement a reduced penalty for the switching frequency. This process makes sure that priority is given to meeting the hard constraints. Once the requirements of the hard constraints are fulfilled, the soft constraint comes into operation. Therefore, the fuzzy rules are obtained in Table 4.2. Taking the five rules for example: If E is NB and E_c is NB, then λ_1 is 1and λ_2 is 0.2; If E is NB and E_c is NM, then λ_1 is 1 and λ_2 is 0.2; If E is NB and E_c is NS, then λ_1 is 0.8 and λ_2 is 0.6; If E is NB and E_c is ZO, then λ_1 is 0.8 and λ_2 is 0.6; If E is NB and E_c is NS, then λ_1 is 0.6 and λ_2 is 0.8.

Two-Dimensional Fuzzy Logic Control Scheme Optimisation Process for D-ifferent Working Conditions

By following this control process, the two-dimensional fuzzy logic control scheme is able to automatically select the weighting factors, λ_1 and λ_2. The degree of the membership function and the curves for the input and output changes in the control scheme are shown in Figure 4.5 and Figure 4.6. From the relationship of the input membership functions and the output membership functions, the fuzzy rules are obtained in Table 4.2.

As a part of this process, if the error, E, (between the active power and the active power reference) and the error change rate, E_C, are over a certain size, the weighting factor for λ_1 will implement a heavier penalty when tracking the currents. At the same time, the weighting factor for λ_2 will implement a reduced penalty for the switching frequency. This process makes sure that priority is given to meeting the hard constraints. Once the requirements of the hard constraints are fulfilled, the soft constraint comes into operation. For example, if the error $E = NB$ and the error change rate $E_C = NB$, the weighting factors will be $\lambda_1 = 1$ and $\lambda_2 = 0.2$ as shown in Table 4.2.

Table 4.2: Fuzzy Rule

Error	**Error Change Rate**	**Weighting Factors**	
(E)	(E_C)	λ_1	λ_2
NB	NB	1	0.2
NB	NM	1	0.2
NB	NS	0.8	0.6
NB	ZO	0.8	0.6
NB	PS	0.6	0.8

Continued 4.2

Error	**Error Change Rate**	**Weighting Factors**	
NB	PM	0.6	0.8
NB	PB	0.6	0.8
NM	NB	0.8	0.6
NM	NM	0.8	0.6
NM	NS	0.8	0.6
NM	ZO	0.6	0.8
NM	PS	0.6	0.8
NM	PM	0.6	0.8
NM	PB	0.6	0.8
NS	NB	0.6	0.8
NS	NM	0.6	0.8
NS	NS	0.6	0.8
NS	ZO	0.2	1
NS	PS	0.2	1
NS	PM	0.2	1
NS	PB	0.2	1
ZO	NB	0.2	1
ZO	NM	0.2	1
ZO	NS	0.2	1
ZO	ZO	0.2	1
ZO	PS	0.2	1
ZO	PM	0.2	1
ZO	PB	0.2	1
PS	NB	0.2	1
PS	NM	0.2	1
PS	NS	0.2	1
PS	ZO	0.6	0.8
PS	PS	0.6	0.8
PS	PM	0.8	0.6
PS	PB	0.8	0.6
PM	NB	0.8	0.6

Continued 4.2

Error	Error Change Rate	Weighting Factors	
PM	NM	0.6	0.8
PM	NS	0.6	0.8
PM	ZO	0.8	0.6
PM	PS	0.8	0.6
PM	PM	0.8	0.6
PM	PB	1	0.2
PB	NB	0.6	0.8
PB	NM	0.6	0.8
PB	NS	0.6	0.8
PB	ZO	0.8	0.6
PB	PS	1	0.2
PB	PM	1	0.2

4.3.3 Fuzzy Rule Tuning

In this section, the fuzzy rule has been tuned to improve the output's performance. The design principle of the fuzzy rule has not changed. They all meet the Mathematical Model of the Two-Dimensional Fuzzy Logic Control Scheme and the Membership Function of the Two-Dimensional Fuzzy Logic Control Scheme in section 4.3.2. Therefore, the fuzzy rule in this section was tuned within reasonable limits (in section 4.3.2) to achieve better performance.

In the two-dimensional fuzzy logic control scheme, the outputs are λ_1 and λ_2. The fuzzy rule for λ_1 was tuned firstly. In order to show the changes of the fuzzy rules in λ_1, λ_2 is fixed as the same fuzzy rule in section 4.3.2. Four types of fuzzy rules were shown in Figure 4.7. Figure 4.7(a) was the original fuzzy rule of the curve of input and output changes for λ_1 in this two-dimensional fuzzy logic control scheme in section 4.3.2, named as plan A. Figure 4.7(b), Figure 4.7(c) and Figure 4.7(d) are newly tuned in this section 4.3.3 and named as plan B, plan C and plan D. In these four plans, including the plan A, the plan B and the plan C and the plan D, it should be noted that the average value of the plan B is large within the same value range. In the plan C, the curve of input and output changes for λ_1 is smooth. In terms of the plan D, the curve is relatively sharp. These four plans represent four different tuning styles. Then, the four types of fuzzy rules are implemented in the system to assess the effects of these changes.

The comparative results of applying the four types of fuzzy rules to the system are indicated in Table 4.3. Table 4.3(a) - Table 4.3(d) show the performance of the plan A - the plan D, respectively. The results (in Table 4.3) relate to the THD of the output currents, the switching frequencies and the RMS values of the DC-link capacitor voltages according to different working conditions (i.e., with active power references of: $300\,kW$, $600\,kW$, $250\,kW$, and $350\,kW$).

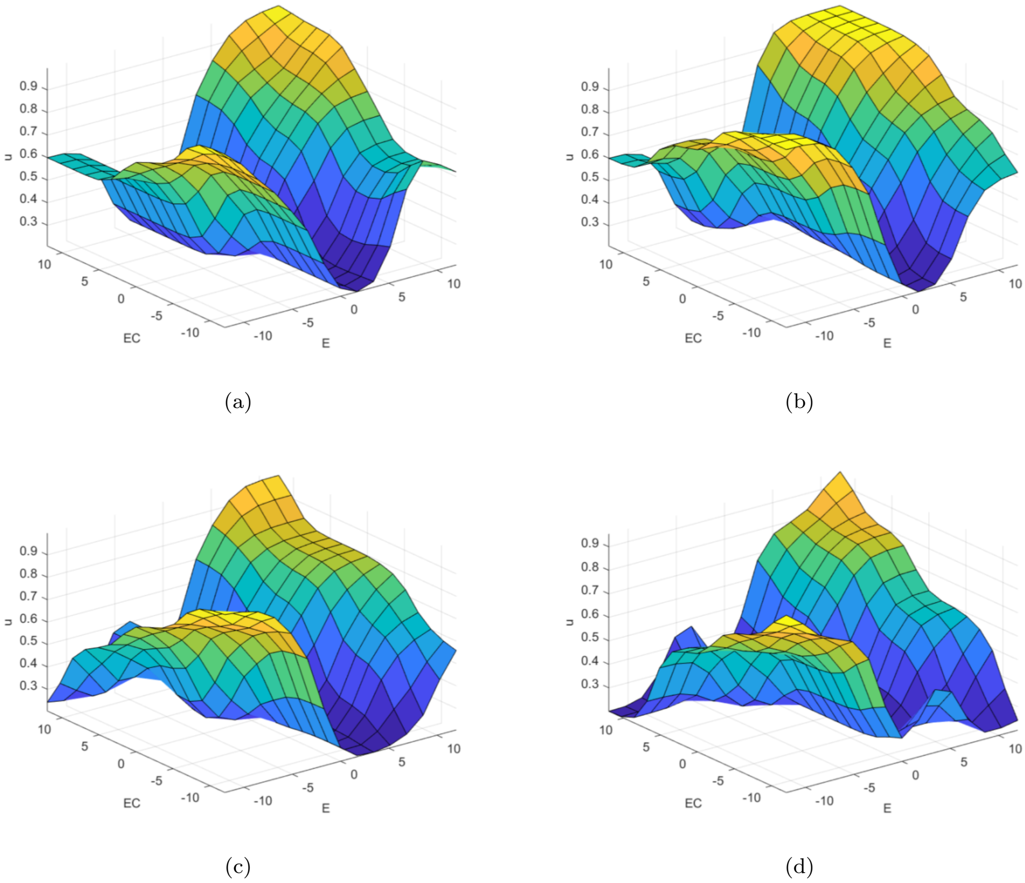
The four types of fuzzy rules achieved more or less the same performance in the THD of the output currents. At $300\,kW$, the fuzzy rule of the plan D had the lowest THD, 3.60%, with a difference between the plan A, the plan B and the plan C of 0.08%, 0.02% and 0.08%, respectively. At $600\,kW$ and $350\,kW$, the plan A and the plan C attained the same THD values 1.91% and 3.17%, respectively, which were both larger than the THD values for the plan B (1.90% and 3.11%) and the plan D (1.89% and 3.09%). In the $250\,kW$ condition, the plan D obtained the best THD value (4.30%), with the other three plans producing values of 4.39% (the plan A), 4.32% (the plan B) and 4.40% (the plan C).

The performance of the RMS value of the DC-link capacitor voltages has similar characteristics with the THD of the output currents. They achieved more or less the same performance in terms of different working conditions. The plan A and the plan C obtained the lowest RMS values of $17.18\,V$ and $17.19\,V$, respectively. In contrast, the plan B and the plan D produced the RMS values of $17.37\,V$ and $17.36\,V$, respectively.

When it came to the switching frequencies, the plan A and the plan C obtained the lowest switching frequency $10.89\,kHz$ and $10.88\,kHz$. The difference between the plan A and the plan C was slight, just $0.01\,kHz$. The plan B and the plan D attained $12.96\,kHz$ and $12.67\,kHz$, respectively. Above all, although the plan C performed best, the plan A achieved a similar performance with the plan C.

The above part of this section is about tuning λ_1 in the two-dimensional fuzzy logic control scheme, and the following part of this section is about λ_2. In order to show the progressions of the fuzzy rules in λ_2, λ_1 is also fixed as the same fuzzy rule in section 4.3.2. Four types of fuzzy rules were shown in Figure 4.8. Figure 4.8(a) was the original fuzzy rule of the curve of input and output changes for λ_2 in this two-dimensional fuzzy logic control scheme in section 4.3.2, named as plan E. Figure 4.8(b), Figure 4.8(c) and Figure 4.8(d) are newly tuned in this section 4.3.3 and named as plan F, plan G and plan H.

The concepts behind the fuzzy rule tuning for λ_2 are identical to those underlying the tuning for λ_1. It should be observed that the average value of the plan F is large within the same value range as the average value of the plan E, the plan F, the plan G, and the plan H. The curve of input and output changes for λ_2 is smooth in plan G. The curve is rather steep in terms of the plan H. Four distinct tuning styles are represented by these



(a) (b) (c) (d)

Figure 4.7: The curve of input and output changes for λ_1 in this two-dimensional fuzzy logic control scheme: (a) the plan A, (b) the plan B, (c) the plan C and (d) the plan D.

four designs. The system is then configured to use four different kinds of fuzzy rules to evaluate the impact of these modifications.

The comparative results of applying the four types of fuzzy rules to the system are indicated in Table 4.4. The results include the THD of the output currents, the switching frequencies and the RMS values of the DC-link capacitor voltages according to different working conditions (i.e., with active power references of: $300\,kW$, $600\,kW$, $250\,kW$, and $350\,kW$) in Table 4.4. Table 4.4(a) - Table 4.4(d) show the performance of the plan E - the plan H, respectively.

The four types of fuzzy rules on the output performance would be analysed in the following section. The four types of fuzzy rules achieved more or less the same performance in the THD of the output currents. At $300\,kW$, the four types of fuzzy rules (the plan E, the plan F, the plan G and the plan H) attained the same THD values of 3.68%. Then, at $600\,kW$, the plan E, the plan F and the plan G achieved the same THD values of 1.91%. Furthermore, the plan H achieved a little bit higher THD values of 1.92%. In the $350\,kW$ condition, the plan E, the plan F and the plan G also have the same THD values

Table 4.3: Fuzzy rule tuning for λ_1

(a) Plan A

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.68%	1.91%	4.39%	3.17%
RMS(V)	17.18			
Switching frequency(kHz)	10.89			

(b) Plan B

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.62%	1.90%	4.32%	3.11%
RMS(V)	17.37			
Switching frequency(kHz)	12.96			

(c) Plan C

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.68%	1.91%	4.40%	3.17%
RMS(V)	17.19			
Switching frequency(kHz)	10.88			

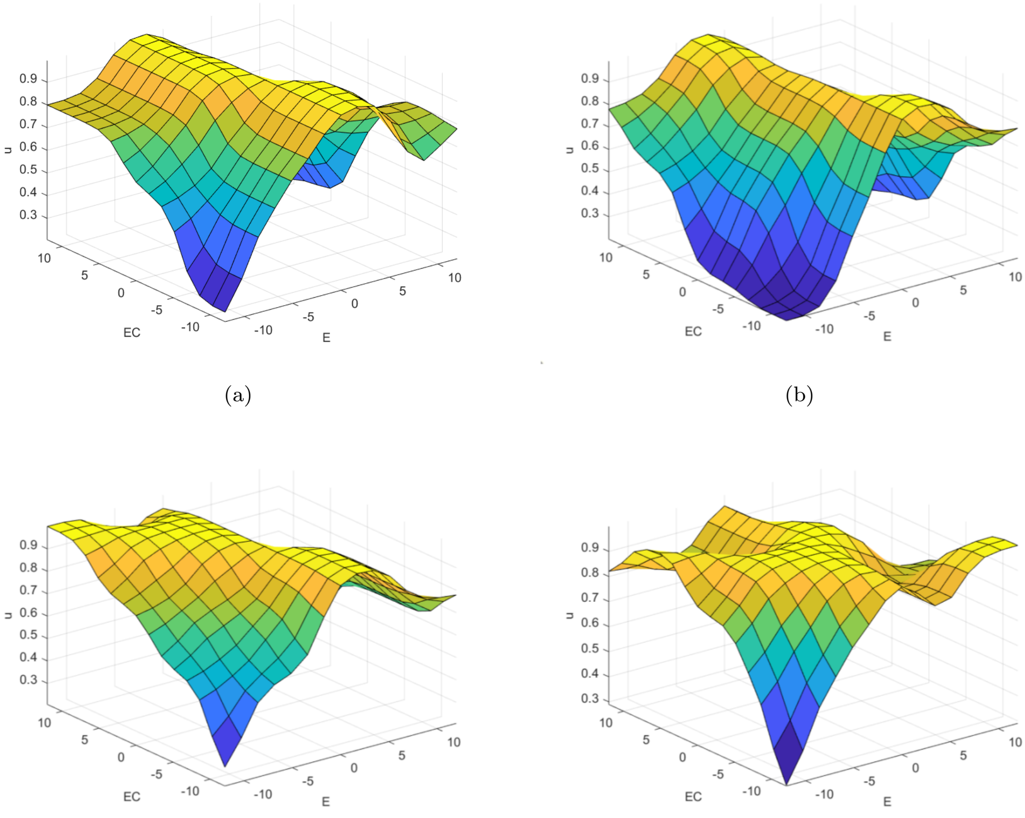
(d) Plan D

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.60%	1.89%	4.30%	3.09%
RMS(V)	17.36			
Switching frequency(kHz)	12.67			

with the number of 4.39%. Simultaneously, the plan H had the THD values of 4.38%. In 250 kW, the plan E, the plan F and the plan H obtained the best THD value of 3.17%. The plan G obtained the THD value of 3.18%. Overall, The four types of fuzzy rules for λ_2 achieved similar performance on the THD values of the output currents.

The performance of the RMS value of the DC-link capacitor voltages has different characteristics in terms of the four types of fuzzy rules. The plan F achieved the lowest RMS values of 16.98 V. The plan E and the plan G obtained the same RMS values of 17.18 V, which is higher than the plan F. The plan H produced the highest RMS values of 17.31 V among the four types of fuzzy rules.

When it came to the switching frequencies, the plan H had the lowest switching frequency 10.81 kHz. The plan E and the plan G obtained 10.89 kHz and 10.88 kHz, respectively. The difference between the plan E and the plan G was small, just 0.01 kHz. The plan



(a) (b) (c) (d)

Figure 4.8: The curve of input and output changes for λ_2 in this two-dimensional fuzzy logic control scheme: (a) the plan E, (b) the plan F, (c) the plan G and (d) the plan H.

F got the highest switching frequency among the four types of fuzzy rules, with the number of 11.53 kHz.

4.4 Simulation Results

In this section, the effectiveness of the proposed MPC algorithm was assessed. Both the 3-level grid-connected NPC inverters shown in Figure 3.17 and the proposed algorithm were implemented in MATLAB Simulink. The parameters and value are provided in Table 4.5.

4.4.1 Nominal Operation

The first simulation focused upon the performance of the proposed MPC algorithm under nominal operating conditions in Figure 4.9. The active power of reference ($P\ reference$)

Table 4.4: Fuzzy rule tuning for λ_2

(a) Plan E

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.68%	1.91%	4.39%	3.17%
RMS(V)	17.18			
Switching frequency(kHz)	10.89			

(b) Plan F

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.68%	1.91%	4.39%	3.17%
RMS(V)	16.98			
Switching frequency(kHz)	11.53			

(c) Plan G

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.68%	1.91%	4.39%	3.18%
RMS(V)	17.18			
Switching frequency(kHz)	10.88			

(d) Plan H

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	300	600	250	350
THD	3.68%	1.92%	4.38%	3.17%
RMS(V)	17.31			
Switching frequency(kHz)	10.81			

Table 4.5: Parameters and Value

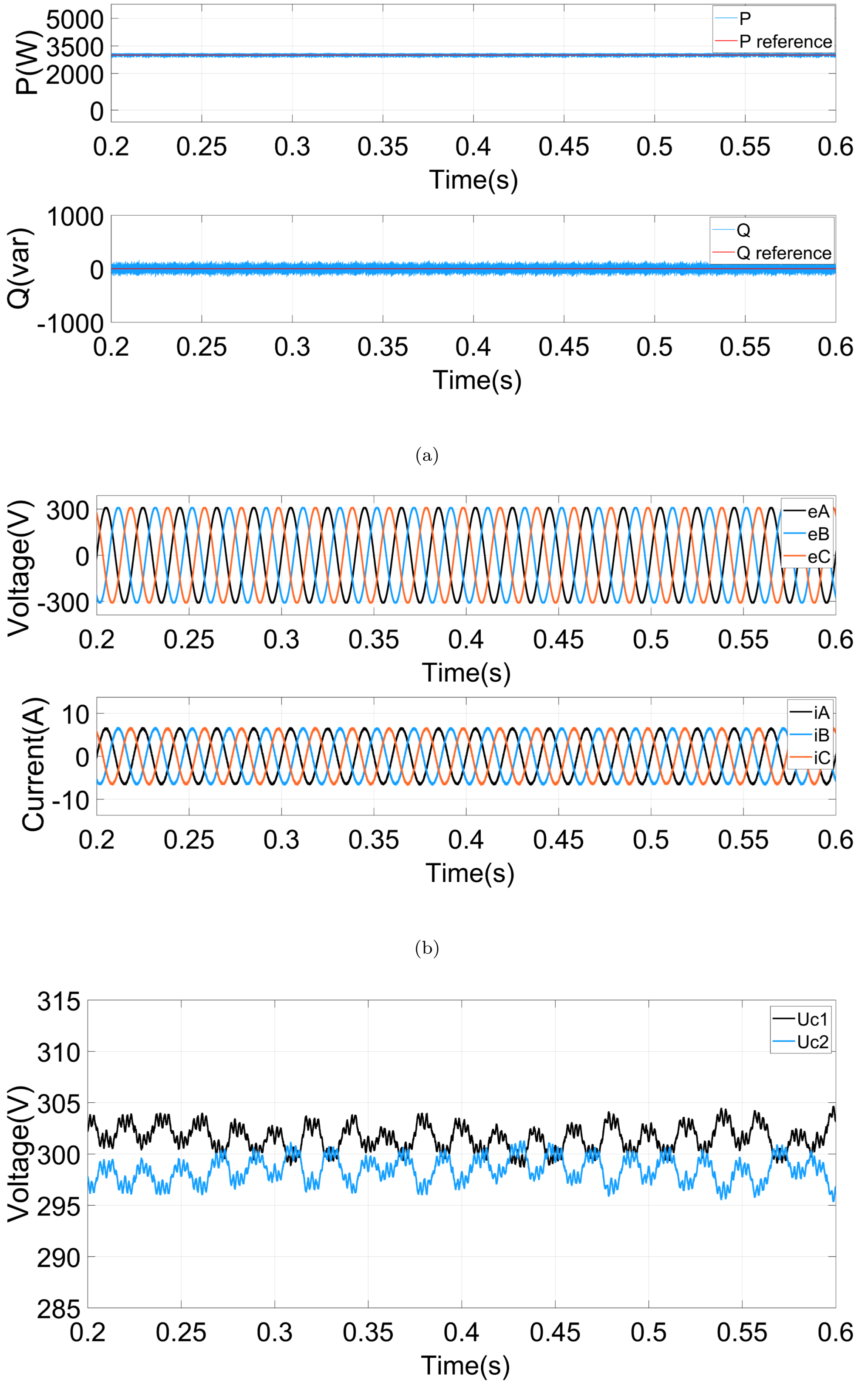
Parameters	**Value**
DC-link voltage V_{dc}	$600\,V$
Load resistance R	$0.02\,\Omega$
Load inductance L	$1.5e-3\,H$
DC-link capacitance C	$4.7e-4\,F$
Grid voltage (phase-to-phase RMS) V_g	$380\,V$
Grid frequency f_g	$50\,Hz$
Sampling period T_s	$1e-4\,s$

was $3.5\,kW$, and the reactive power of reference ($Q\ reference$) was $0\,VAR$, so as to ensure a unity power factor. In Figure 4.9(a), the active power, P, and the reactive power, Q, both tracked the reference powers. In Figure 4.9(b), e_A, e_B, and e_C represent the output grid phase voltages, whose peak values were $310V$. i_A, i_B, and i_C are the output grid currents. So, from Figure 4.9(b), it can be concluded that the system's output currents and voltages were stable. In Figure 4.9(c), U_{c1} and U_{c2} are the voltages of the DC-link capacitors. The root-mean-square (RMS) value of the DC-link capacitor fluctuating voltage was $1.5\,V$, which was 0.26% of the total DC-link voltage. This indicates that the proposed MPC algorithm maintained neutral point balancing with reasonable ripples. Therefore, under steady-state working conditions, the proposed MPC algorithm can achieve active and reactive power tracking, stable current and voltage output, and neutral point balancing.

4.4.2 Active Power Tracking in Dynamic Operation

The robustness of the proposed MPC algorithm was also assessed. The active power of reference ($P\ reference$) was stepped up from $1.5\,kW$ to $5\,kW$ at $0.3\,s$, decreased to $3.5\,kW$ at $0.4\,s$, then decreased again to $2\,kW$ at $0.5\,s$. Under these dynamic working conditions, the proposed MPC algorithm was able to achieve active power tracking and reduce the switching frequency. The simulation results are analysed in this section.

The transient-state performances of the proposed MPC algorithm are shown in Figure 4.10(a). From the figures, it can be seen that the active power (P) is able to rapidly track to these steps. At the same time, the reactive power (Q) is maintained at zero across the whole duration of the simulation. Figure 4.10(b) shows that the output grid voltage was able to maintain a steady three-phase output. At the same time, the output currents were able to quickly respond to the different steps across the whole transition period without overshooting. For the first step change, where the active power of reference stepped up from $1.5\,kW$ to $5\,kW$ at $0.3\,s$, the response time of the output grid current was $0.0003\,s$. In Figure 4.10(c), it can be seen that the RMS value of the DC-link capacitor fluctuating voltage was also $1.5V$, which was 0.26% of the total DC-link voltage, while maintaining normal operation. The total harmonic distortion (THD) of the grid currents was 4.31% ($P = 1.5\,kW$), 1.3%($P = 5\,kW$), 1.85%($P = 3.5\,kW$) and 3.26%($P = 2\,kW$) respectively, as depicted in Figure 4.11. So, the proposed MPC algorithm kept the RMS value of the output grid currents sufficiently low that they all met the $IEEE\ Standard\ 519-2014$ requirements. Zoomed waveforms are shown in Figure 4.12 for the period from $0.25\,s$ to $0.35\,s$.

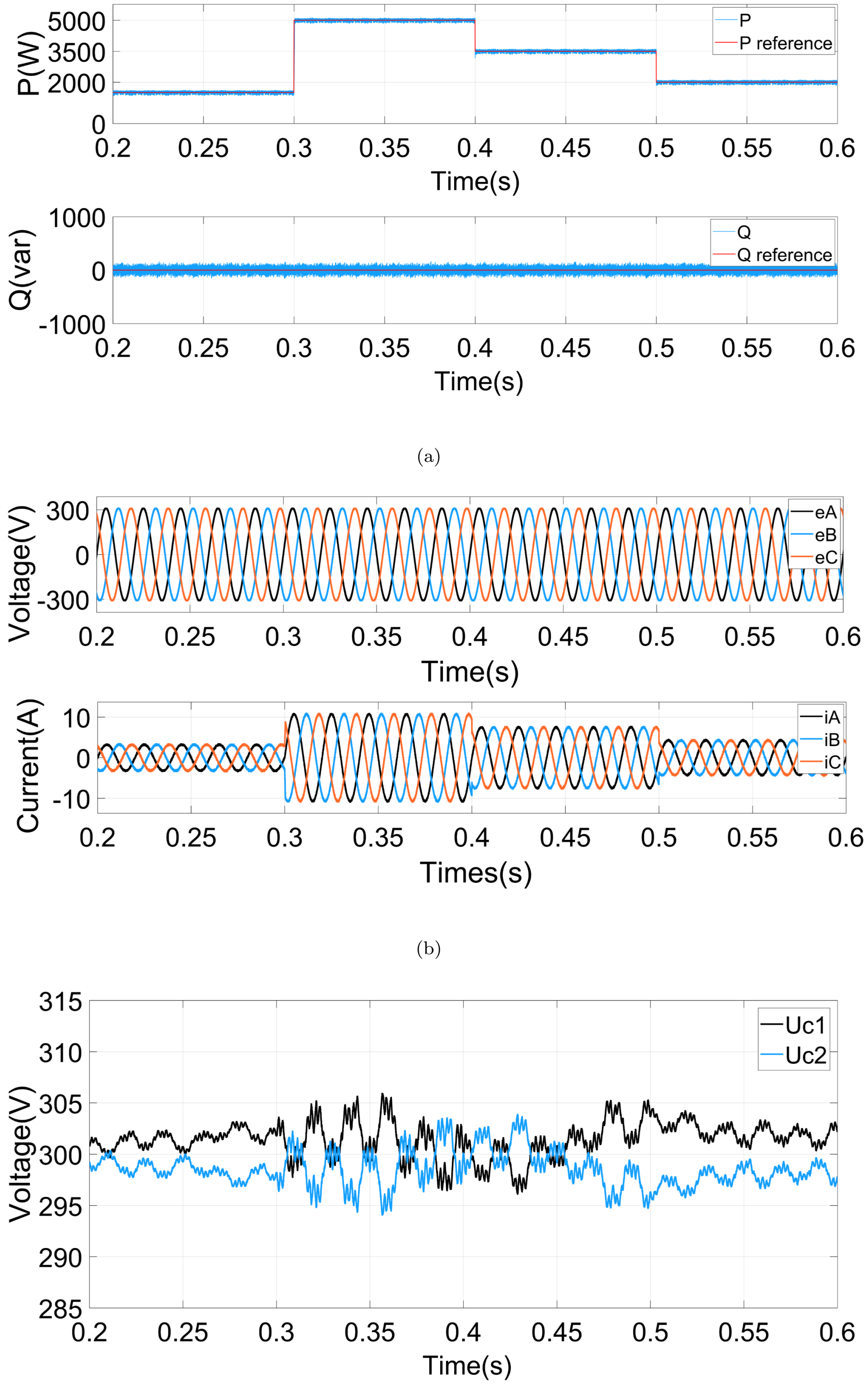


(a)

(b)

(c)

Figure 4.9: Simulation results for the proposed MPC algorithm under nominal operation conditions: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

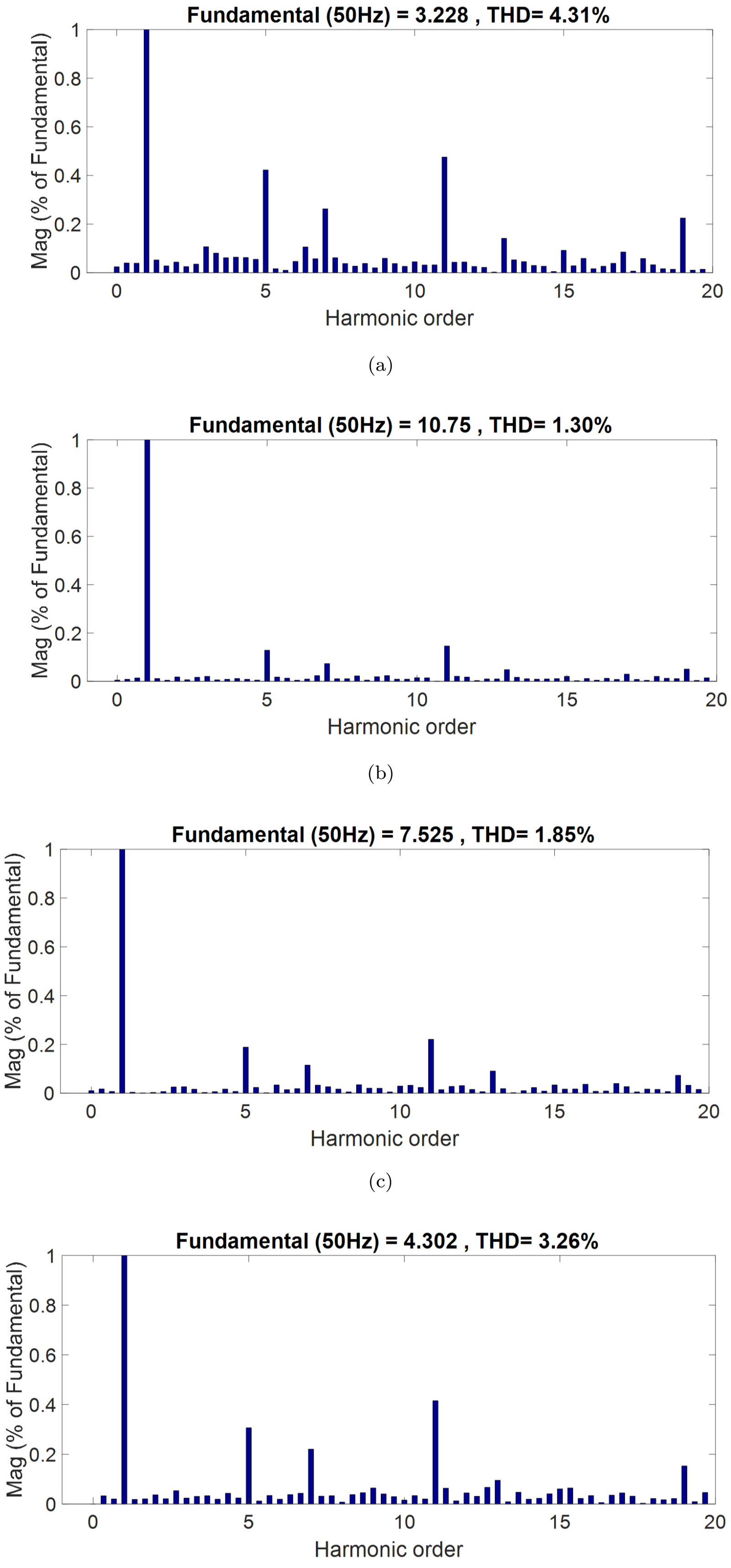


(a)

(b)

(c)

Figure 4.10: Simulation results for the proposed MPC algorithm under dynamic operation conditions: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.



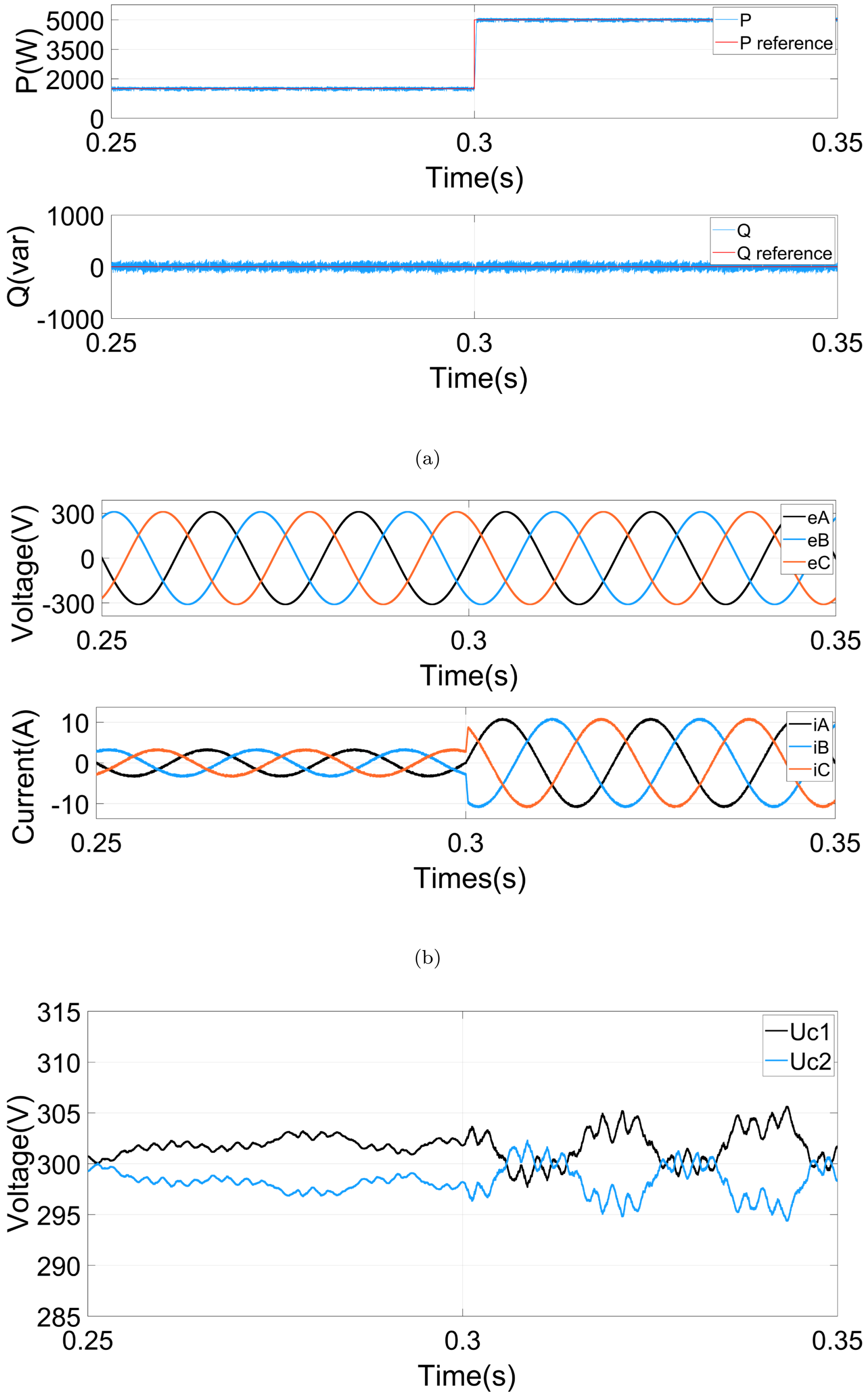
(a)

(b)

(c)

(d)

Figure 4.11: Total Harmonic Distortion (THD) of the grid current: (a) $P = 1.5\,kW$ and $THD = 4.31\%$, (b) $P = 5\,kW$ and $THD = 1.30\%$, (c) $P = 3.5\,kW$ and $THD = 1.85\%$ and (d) $P = 2\,kW$ and $THD = 3.26\%$



(a)

(b)

(c)

Figure 4.12: Zoomed results between 0.25s and 0.3s: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

4.4.3 Switching Frequency Reduction in Dynamic Operation

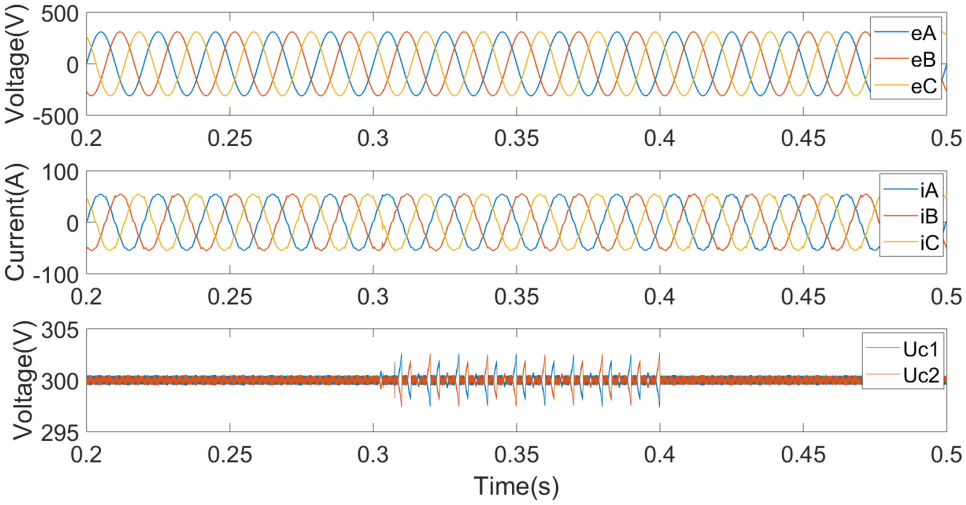
During the dynamic process of the active power of reference ($Preference$) being stepped up from $1.5\,kW$ to $5\,kW$ at $0.3\,s$, then down to $3.5\,kW$ at $0.4\,s$, then down again to $2\,kW$ at $0.5\,s$, the f_{sw} was $9.75\,kHz$. Over the same dynamic period of operation, the switching frequency using the conventional MPC method [82] would have been $13.96\,kHz$. Thus, the proposed MPC algorithm reduced the switching frequency by 30.16% compared to the conventional MPC algorithm [82]. In addition, the cumulative switch changes of the proposed MPC for each phase were also lower than the conventional MPC. The switching frequency and cumulative switch changes for each phase are shown in Table 4.6. The proposed MPC algorithm was able to implement reductions in the switching frequency because the appropriate weighting factors were determined online across different working conditions. The conventional MPC algorithm, however, had to employ fixed weighting factors while the system was in operation.

Table 4.6: Switching Frequency and Cumulative Switch Changes

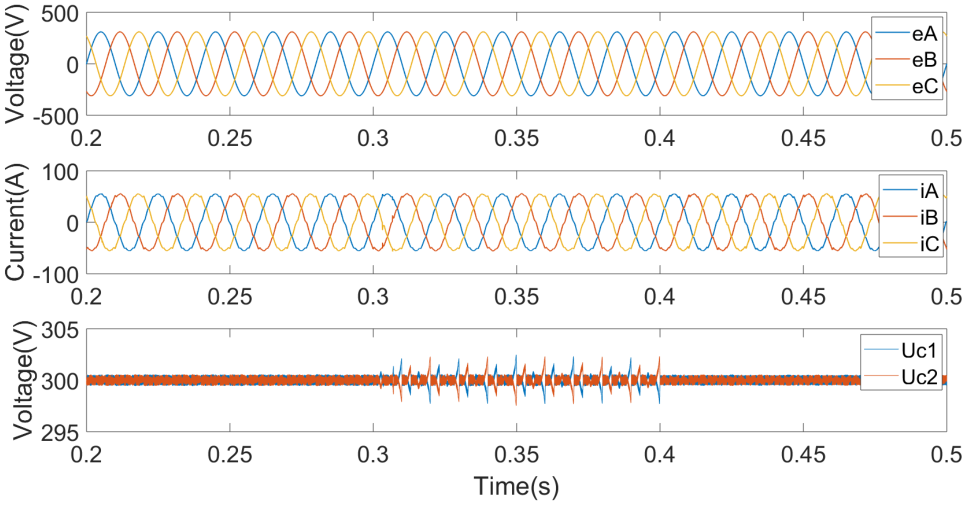
	Conventional [82]	**Proposed method**
Switching Frequency	$13.96\,kHz$	$9.75\,kHz$
Cumulative Switch Changes in A Phase	$55790\,times$	$33430\,times$
Cumulative Switch Changes in B Phase	$56020\,times$	$41720\,times$
Cumulative Switch Changes in C Phase	$55770\,times$	$41850\,times$
THD	$3.47\,\%$	$3.26\,\%$
RMS of Capacitor Voltage Error	$1.02\,V$	$5.35\,V$

4.4.4 Parameter Sensitivity

In this section, the parameter (inductance) sensitivity of the proposed MPC algorithm was analysed and compared to the conventional MPC algorithm. With regard to parameter sensitivity, the proposed MPC algorithm can automatically select the weighting factors, because its two-dimensional fuzzy logic control scheme can detect changes in the power and select appropriate weighting factors for the cost functions. In the case of a conventional MPC algorithm, however, fixed weighting factors are applied to the cost function even if the parameters of the system are subject to variation. Comparative results for the conventional MPC algorithm [82] and the proposed MPC algorithm are provided in Table 4.7. The waveforms relating to the simulation results are shown in Figure 4.13. From the results, it can be seen that the proposed MPC algorithm can overcome misidentification of the inductances with variations in the parameter having no significant effect on the system. Thus, the performance of the proposed MPC algorithm was better than the conventional MPC algorithm in terms of the output current's THD, cumulative switch changes, switching frequencies and RMS values of DC-link capacitor voltage errors.



(a)



(b)

Figure 4.13: Simulation results under parameter sensitivity conditions: (a) Conventional MPC:e_A,e_B, and e_C=the grid voltages; i_A,i_B, and i_C=the grid currents; and U_{c1},U_{c2}=the DC-link capacitor voltages, and (b) Proposed MPC:e_A,e_B, and e_C=the grid voltages; i_A,i_B, and i_C=the grid currents; and U_{c1},U_{c2}=the DC-link capacitor voltages.

Table 4.7: Parameter Sensitivity Comparison Results for Conventional MPC and Proposed MPC

Period (s)	**Inductances (H)**	**Conventional MPC (THD value)**[82]	**Proposed MPC (THD value)**
0.2-0.3	2e-3 (+25%)	3.51%	3.51%
0.3-0.4	3e-3 (+50%)	3.33%	3.27%
0.4-0.5	7.5e-4 (-75%)	3.84%	3.80%
Cumulative Switch Changes (Times)	**A Phase**	47800	23240
	B Phase	47060	22350
	C Phase	46770	22810
Switching Frequency (kHz)		11.8	5.7
RMS Values of Capacitor Voltage Error (V)		1.264	1.204

In this simulation, the active power reference was 25 kW, and the reactive power reference was 0 VAR. The load inductance, L, was $1.5e-3\,H$. Over the period of 0.2 s to 0.3 s in the simulation, the value of the inductance increased to $2e-3H$, i.e., 25%. The THD values for the conventional MPC and the proposed MPC were the same at 3.51%. Over the next 0.1 s, from 0.3 s to 0.4 s, the value of the inductance continued to increase to $3e-3\,H$ i.e., 50% greater than the initial inductance of $1.5e-3\,H$. It can be seen from the results in Table 4.7 that the output current for the proposed MPC algorithm (THD: 3.27%) was of better quality than it was for the conventional one (THD: 3.33%). From 0.4 s to 0.5 s, the inductance was reduced to $7.5e-4\,H$ i.e., -75%. The proposed MPC algorithm's output current was still better than that of the conventional one, with THD values of 3.80% for the conventional MPC algorithm and 3.84% for the proposed MPC algorithm, respectively. So, the proposed MPC algorithm achieved consistently lower THD values than the conventional MPC algorithm, indicating a systematically improved parameter sensitivity.

With regard to the cumulative switch changes, switching frequencies and capacitor voltage error RMS values, the performance of the proposed MPC algorithm was repeatedly better than the conventional MPC algorithm, especially for the switching frequencies. In Table 4.7, the switching frequency was reduced by more than 51% with the conventional MPC algorithm generating a frequency of 11.8 kHz, while the proposed MPC algorithm generated just 5.7 kHz under the same working conditions.

4.5 Different Plants with Representative Parameters

Two distinct sets of plants with typical parameters (Case A and Case B) were used to validate the suggested MPC methods in Chapter 4. These two examples illustrate how

Table 4.8: The Case A

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (MW)	1	0.6	0.22	0.4
THD	0.81%	1.38%	3.10%	2.42%
RMS(V)	12.25			
Switching frequency(kHz)	6.903			

practical applications could be found in industry and everyday life. The performance of the proposed MPC control algorithm may be better shown using these two distinct plants with typical characteristics. The next sections would detail the contents of several plants with typical characteristics (Case A and Case B).

Case A: 3kV 1MW HVDC (high-voltage direct current) system, source from: [New 4.5 kV IGBT and diode chip set for HVDC Transmission Applications in infineon.com].

Case B: 600V 400kW UPS (uninterruptible power supply) application system, source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com].

4.5.1 Case A

The proposed MPC algorithm was validated in Case A by simulating a $3\,kV$ $1\,MW$ system. The characteristics for Case A are taken from a high-voltage direct current system, as described in [New $4.5\,kV$ IGBT and diode chip set for HVDC Transmission Applications in infineon.com]. To evaluate the system's resilience, the active power reference P^* was reduced from $1\,MW$ to $0.6\,MW$ at $0.2\,s$ and subsequently to $0.22\,MW$ at $0.4\,s$. It would rise to $0.4\,MW$ at $0.6\,s$. Simultaneously, the reactive power reference, Q^*, was kept at zero to preserve a power factor of unity.

The output waveform findings for Case A are shown in Figure 4.14, and the different performance indicators are summarised in Table 4.8. The active power, P, and the reactive power, Q, are shown in Figure 4.14(a). The suggested MPC algorithm was able to monitor the active and reactive power based on this figure, even when the active power reference varied. At $0.2\,s$, the active power reference decreased from $1\,MW$ to $0.6\,MW$, then increased from $0.22\,MW$ to $0.3\,MW$ at $0.4\,s$. Figure 4.14(b) illustrates the grid voltages, e_A, e_B, e_C, and grid currents, i_A, i_B, i_C. Table 4.8 summarises the total harmonic distortion (THD) values for grid currents. The THD is 0.81% at $1\,MW$, 1.38% at $0.6\,MW$, 3.10% at $0.22\,MW$, and 2.42% at $0.4\,MW$. As a result, the proposed MPC algorithm, which is based on automated weighting factor selection, can provide high-quality output currents and voltages. Figure 4.14(c) illustrates the voltages of the DC-link capacitors, U_{c1} and U_{c2}. The RMS error for the fluctuation in the DC-link capacitors was $12.25\,V$.

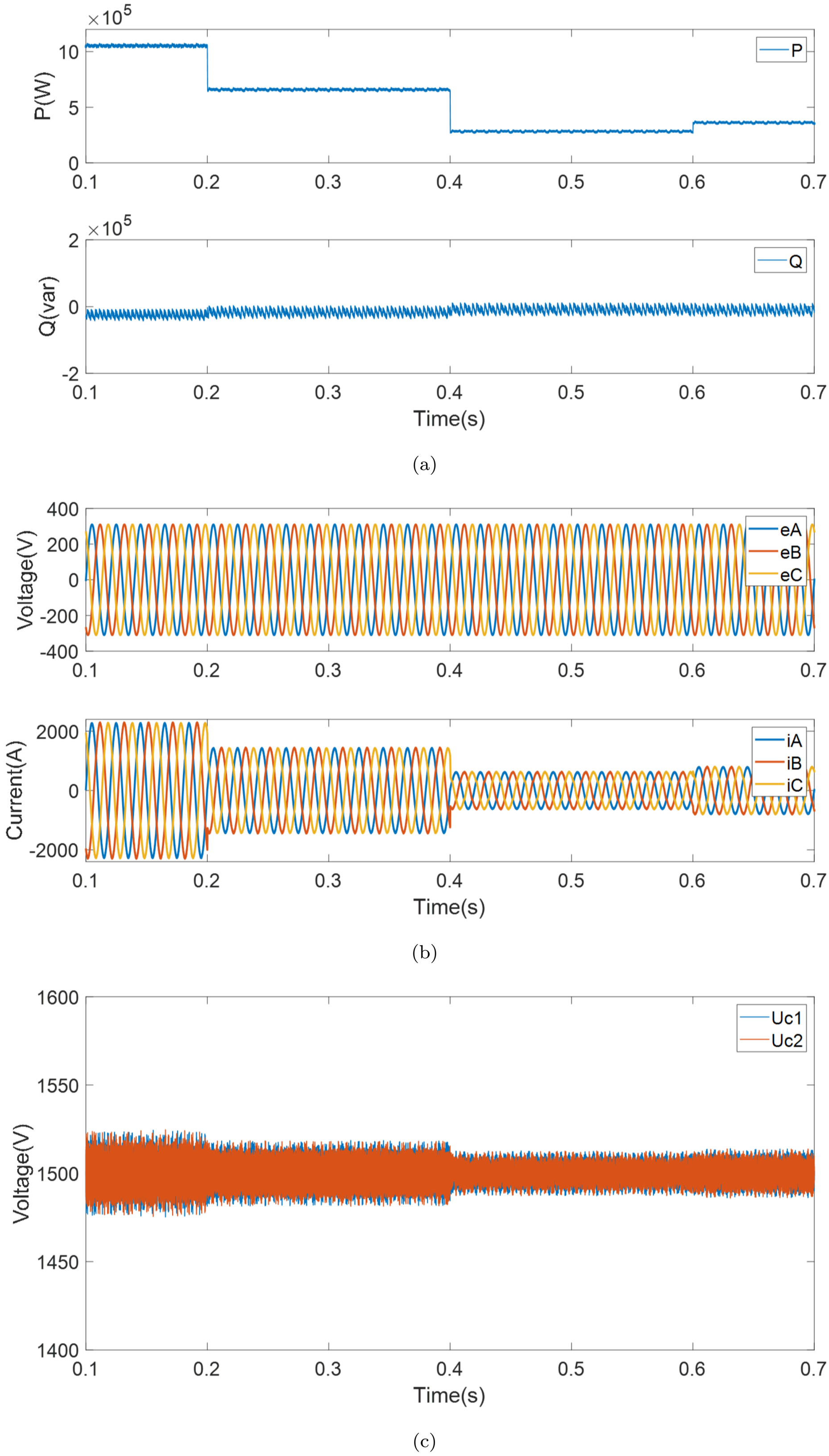


Figure 4.14: Results for the Case A: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 4.9: The Case B

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	400	450	250	300
THD	2.72%	2.44%	4.32%	3.60%
RMS(V)	11.88			
Switching frequency(kHz)	4.953			

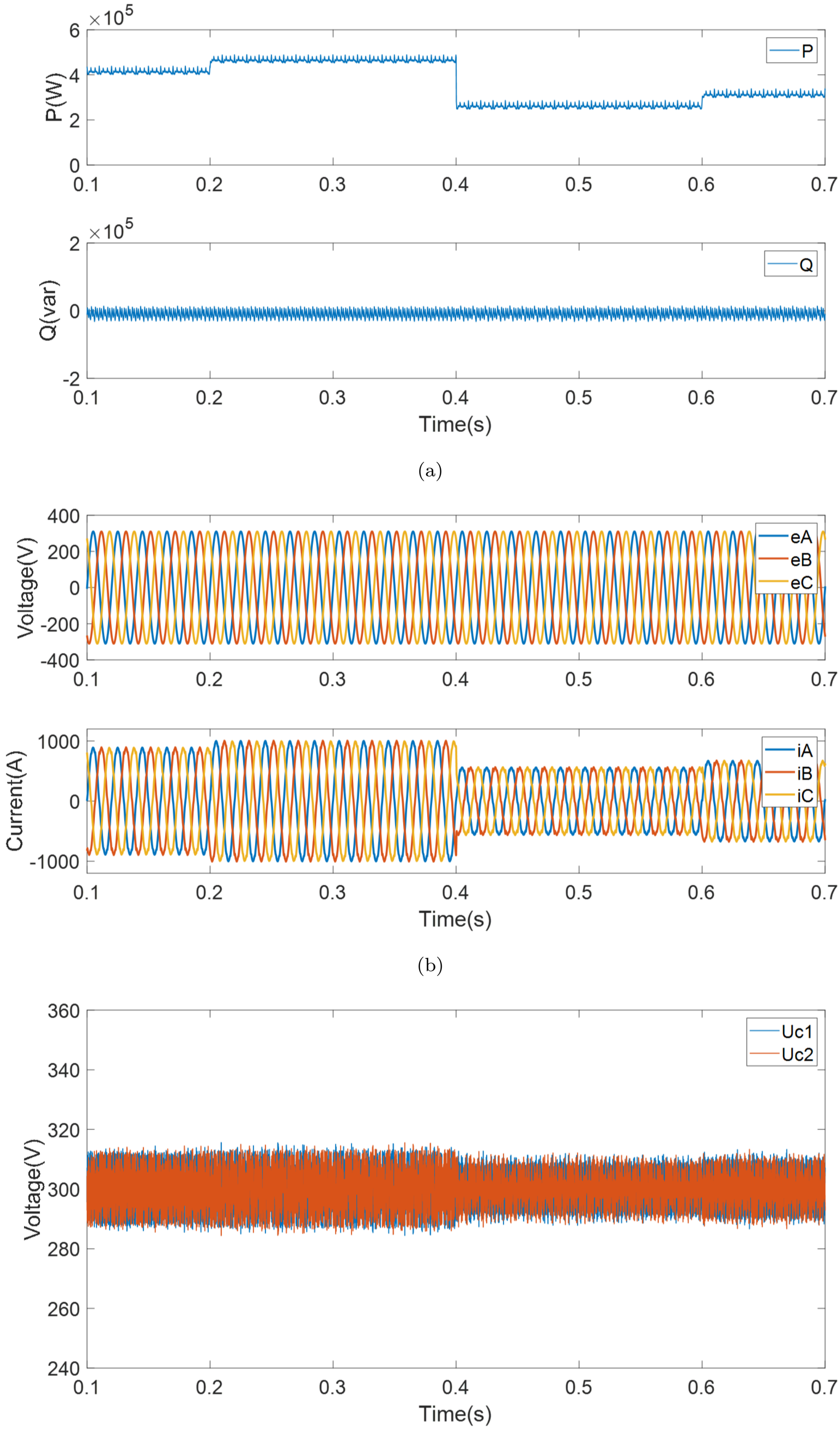
4.5.2 Case B

The proposed MPC method was validated in Case B by simulating a $600\,V$ $400\,kW$ system. Case B's parameters are taken directly from the UPS application system, source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com]. To evaluate the system's resilience, the active power reference P^* was ramped down $400\,kW$ to $450\,kW$ in $0.2\,s$ and subsequently to $250\,kW$ in $0.4\,s$. It would then rise to $300\,kW$ at $0.6\,s$. Simultaneously, the reactive power reference, Q^*, was kept at zero to preserve a power factor of unity.

Figure 4.15 and Table 4.9 illustrate the findings of Case B. The active power, P, and the reactive power, Q, are shown in Figure 4.15(a). As shown in this image, the proposed MPC algorithm was capable of tracking both active power and reactive power even when the active power reference changed (i.e., stepping up from $400\,kW$ to $450\,kW$ at $0.2\,s$, then going up from $250\,kW$ at $0.4\,s$ to $300\,kW$ at $0.6\,s$). Figure 4.15(b) illustrates the grid voltages, e_A, e_B, e_C, and grid currents, i_A, i_B, i_C. Table 4.9 summarises the total harmonic distortion (THD) values for grid currents. At $400\,kW$, the THD is 2.72%, 2.44% at $450\,kW$, 4.32% at $250\,kW$, and 3.60% at $300\,kW$. Figure 4.15(c) illustrates the voltages of the DC-link capacitors, U_{c1} and U_{c2}. The RMS error for the fluctuation in the DC-link capacitor was $11.88\,V$. Figure 4.15(c) depicts the waveform of the DC-link capacitor fluctuation. As a result, the suggested MPC algorithm can provide high-quality output currents and voltages.

4.6 Summary

An MPC algorithm for grid-connected NPC inverters based on the automatic selection of weighting factors has been proposed. The algorithm incorporates a novel cost function that is able to track output currents, maintain the stability of the capacitor voltages, control the neutral point voltages, decrease the switching frequency and limit the switching loss. Its particular contribution is the use of a two-dimensional fuzzy logic control scheme that eliminates the need for trial-and-error that is typical of existing approaches to MPC-based multilevel inverter design. The results have thus verified the effectiveness of the proposed algorithm and its potential viability for renewable energy resource applications. The key findings from this chapter are:



(a)

(b)

(c)

Figure 4.15: Results for the Case B: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

- A two-dimensional fuzzy logic control scheme was investigated for automatic selection of weighting factors in the MPC algorithm. Through comparative performance results of different membership functions (Gaussian, Triangular and Trapezoidal) for the NPC inverter system in Table 4.1, Gaussian membership function was applied in the system due to its lower THD of output current and switching frequency.

- In nominal operation, the proposed MPC algorithm maintained neutral point balancing with reasonable ripples. The RMS value of the DC-link capacitor fluctuating voltage was $1.5\,V$, which is 0.26% of the total DC-link voltage. A stable output, including active power, reactive power, current and voltage were obtained in Figure 4.9.

- Under dynamic working conditions, it can automatically select appropriate weighting factors without any need for a process of trial-and-error. It has been determined that the proposed algorithm can decrease the switching frequency by at least 30% in comparison to conventional MPC methods. In addition, the algorithm was found to be capable of active power tracking (from $1.5\,kW$ to $5\,kW$ at $0.3\,s$, down to $3.5\,kW$ at $0.4\,s$, down again to $2\,kW$ at $0.5\,s$). It can also maintain neutral point balancing (fluctuations in the DC-link capacitor voltage then accounting for just 0.26% of the total DC-link voltage).

- The parameter (inductance) sensitivity of the proposed MPC algorithm was analysed and compared to the conventional MPC algorithm. The load inductance, L, was $1.5e-3\,H$. Over the period of $0.2\,s$ to $0.3\,s$, the value of the inductance increased to $2e-3\,H$, i.e., 25%. From $0.3\,s$ to $0.4\,s$, the value of the inductance continued to increase to $3e-3\,H$ i.e., 50% greater than the initial inductance of $1.5e-3\,H$. From $0.4\,s$ to $0.5\,s$, the inductance was reduced to $7.5e-4\,H$ i.e., -75%. The switching frequency was reduced by more than 51% with the conventional MPC algorithm generating a frequency of $11.8\,kHz$, while the proposed MPC algorithm generated just $5.7\,kHz$ under the same working conditions. Meanwhile, the proposed MPC algorithm achieved consistently lower THD values than the conventional MPC algorithm

Chapter 5

Model Predictive Control of 3-level NPC Inverters based on Current Slope Control Objective

In this chapter, a new proposed current slope-related control objective is added to the cost function of the proposed MPC algorithm. This control objective aims to make predicted current slope values approach reference current slope values. By doing this, the proposed algorithm can reduce the total harmonic distortion (THD) of the output currents and, when compared to a conventional MPC algorithm, can reduce the switching frequency by more than 30%. A case study of a grid-connected NPC inverter system is used to assess the effectiveness of the proposed MPC algorithm under conditions of nominal operation and dynamic operation (with the active power reference, P^*, being stepped down from $31\,kW$ to $24\,kW$ at $0.3\,s$, then increased to $41\,kW$ at $0.5\,s$) and with different degrees of parameter sensitivity (at +25%, +50%, and −75% variation in inductance).

5.1 Introduction

Total harmonic distortion (THD) reduction of the output current is another research focus for control of power electronics. Total harmonic distortion, or THD, is the summation of all harmonic components of the current or voltage waveform compared against the fundamental component of the current or voltage wave [37]. Low THD of output currents is required in some scenarios such as large ships, medical equipment, semiconductor industries and airports. In large ships, large-capacity power converters are installed, and harmonics pose a significant risk to the system due to power supply capacity restrictions. Another scenario for low THD of output currents is in hospitals where all kinds of critical and sensitive equipment are installed, and any small disturbance could bring unforeseen risks to the patient. In these kinds of environments, the harmonic requirements of the inverter are stringent. Thus, the low harmonic inverters are needed for the occasion. Next scenario is in semiconductor industries, which have an extremely stringent requirement of the harmonics of a power system and require low harmonics for high-power inverters. The same scenario applies to airports, which have a variety of sensitive control equipment and therefore high requirements regarding harmonics and many airports are equipped with low harmonic converters.

Focusing on the research problem (low THD of the output current), a few MPC methods can address this problem [39] and [40]. The former method [39] is to optimise the structure of MPC, and the latter method [40] is to optimise the optimisation process of MPC in order to reduce the THD of the output currents. However, optimisation of control objective in the existing literature is not considered. Thus, the current slope as a new control objective in the cost function is proposed in this chapter.

This is the first time the current slope has been considered as a control objective in the cost function of the proposed MPC algorithm. MPC strategies can help with addressing an optimisation problem so that the control signal which will be used in the system is defined. As the cost function indicates the systems required behaviour, MPC obtains the optimal actuation by minimising the cost function. In the previous studies for NPC inverters, control objectives in the cost function are presented in Table 2.6. From these control objectives, it is clear that current, voltage, torque, power, and flux as control objectives are taken into consideration, whilst the current slope as a control objective in the cost function of MPC algorithms has not yet been studied. When the current slope is added in the cost function, the fluctuation of the current may be suppressed. Therefore, a new proposed current slope-related control objective for the MPC algorithm is investigated in this chapter.

The rest of this chapter is organised as follows. The design of the proposed MPC algorithm with the control objective of the current slope is in section 5.2. Then, the results verified the effectiveness of the proposed MPC algorithm by nominal operation, dynamic operation and parameter sensitivity in section 5.3. Finally, the main conclusions of this chapter are given in section 5.6.

5.2 A Model Predictive Control Algorithm with Current Slope Control

5.2.1 Cost Function Design

Section 3.8.1 provided an overall of the system model for a grid-connected NPC inverter system. Table 3.7 and Table 3.8, respectively, illustrate the state definition for each phase and the switching states associated with voltage space vectors. The following section focused on the cost function design of the proposed MPC algorithm. In this chapter, a new control objective relating to the current slope is going to be added to the cost function. Thus, the new proposed cost function will have one more part (for the current slope) than a conventional MPC algorithm [82]. This newly-introduced part not only reduces the THD of the output currents but also lowers the switching frequency. The other control objectives in the cost function relate to tracking current reference and balancing the DC-link capacitor voltages. Including these control objectives, the cost function, J, has the following three parts:

$$J(k+1) = J_1(k+1) + J_2(k+1) + J_3(k+1) \tag{5.1}$$

The MPC algorithm is primarily concerned with determining an optimal controlled input concerning the power switches. This is done by solving an online optimisation problem that provides a sort of receding horizon of control [21][30]. The overall objective function for this optimisation problems concerns system performance. In the cost function, the first part, J_1, focuses on tracking the output currents. The second part, J_2, tracks the slope of the reference current. The last part, J_3, maintains the stability of the capacitor voltage. Looking at each part more specifically:

$$J_1(k+1) = |i_\alpha(k+1) - {i_\alpha}^*(k+1)|^2 + |i_\beta(k+1) - {i_\beta}^*(k+1)|^2 \tag{5.2}$$

where, $i_\alpha(k+1)$ and $i_\beta(k+1)$ represent the current predictions in terms of the system model; and $i_\alpha^*(k+1)$ and $i_\beta^*(k+1)$ stand for the reference current of the next sampling step. As noted, this part is dedicated to tracking the output currents.

$$\begin{aligned} J_2(k+1) = &\left|\frac{i_\alpha^*(k+1) - i_\alpha^*(k)}{T_s} - \frac{i_\alpha(k+1) - i_\alpha(k)}{T_s}\right|^2 + \\ &\left|\frac{i_\beta^*(k+1) - i_\beta^*(k)}{T_s} - \frac{i_\beta(k+1) - i_\beta(k)}{T_s}\right|^2 \end{aligned} \tag{5.3}$$

where, T_s is the sampling period. This part is concerned with tracking the slope of the reference current. By using this part in the cost function, the THD values of the output currents and the switching frequencies will be reduced.

$$J_3(k+1) = |u_{c1}(k+1) - u_{c2}(k+1)|^2 \tag{5.4}$$

$u_{c1}(k+1)$ and $u_{c2}(k+1)$ are the DC-link capacitor voltages. This part maintains the DC-link capacitor voltages stable.

5.2.2 Optimisation Process

ψ is introduced to express switching states.

$$\psi \triangleq \left\{ u = \begin{bmatrix} u_a \\ u_b \\ u_c \end{bmatrix} \in \mathbb{R}^3 \mid u_x \in \{-1, 0, 1\}, x = a, b, c \right\} \tag{5.5}$$

In fact, $\psi = \{u_1, u_2, \ldots, u_{27}\}$ in NPC inverters, which are shown in Table 3.2 and a, b, and c represent the three phases.

The optimal control can be stated as:

$$\begin{aligned} u_{opt}(k) = \arg \min_{u(k) \in \psi} \quad & \tilde{J}\left(u_i(k)\right) \triangleq J(k) \\ \text{subject to} \quad & (\mathit{Equation}\ 3.40) \quad (\mathit{Equation}\ 3.42) \\ & (\mathit{Equation}\ 3.45) \quad (\mathit{Equation}\ 3.46) \end{aligned} \tag{5.6}$$

The cost function J is used to find the selected voltage vector, $u_{opt}(k)$, which minimises the cost function.

5.3 Simulation Results

A $600\,V$ $31\,kVA$ system is used for validating the proposed MPC algorithm. The parameters of the system are presented in Table 5.1. Both the grid-connected NPC inverter system and the proposed MPC algorithm with the current slope control objective were implemented in MATLAB Simulink. To test the effectiveness of the proposed MPC controller, three working conditions were considered: nominal operation, dynamic operation (where the active power reference, P^*, was stepped down from $31\,kW$ to $24\,kW$ at $0.3\,s$, then increased to $41\,kW$ at $0.5\,s$); and changes in the parameter sensitivity (+25%, +50%, and −75% variations in the inductance). Throughout the various tests, the reactive power reference, Q^*, was set at zero to achieve a unity power factor.

5.3.1 Nominal Operation

Initially, the simulation focused on verifying the performance of the proposed MPC algorithm with the current slope control objective under nominal operating conditions. It can be seen in Figure 5.1 that the active power reference was $31\,kW$ and the reactive power reference was $0\ VAR$, so as to ensure a unity power factor. In Figure 5.1(a), the active power, P, and reactive power, Q, both stabilized and tracked the reference powers.

Table 5.1: Parameters and Value

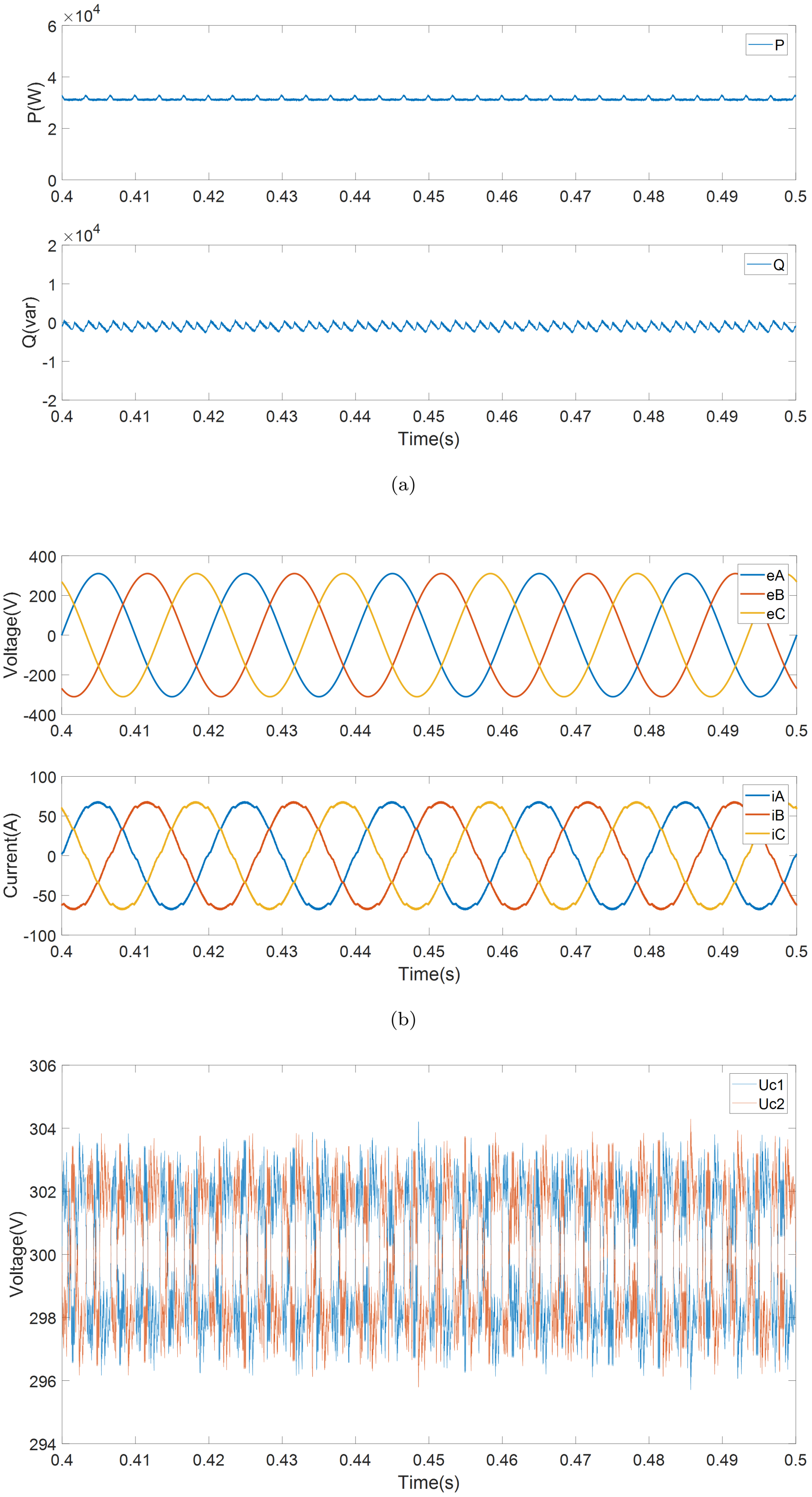
Parameters	**Value**
DC-link voltage V_{dc}	$600\,V$
Load resistance R	$0.02\,\Omega$
Load inductance L	$1.5e-3\,H$
DC-link capacitance C	$4.7e-4\,F$
Grid voltage (phase-to-phase RMS) V_g	$380\,V$
Grid frequency f_g	$50\,Hz$
Sampling period T_s	$8e-5\,s$

In Figure 5.1(b), e_A, e_B, and e_C represent the output grid phase voltages, whose peak values were $310\,V$. i_A, i_B, and i_C are the output grid currents. The THD value of the output currents was 2.82%. So Figure 5.1(b) shows that can be seen that the system's output currents and voltages were stable. In Figure 5.1(c), U_{c1} and U_{c2} are the voltages of the DC-link capacitors. The root-mean-square (RMS) value of fluctuation in the DC-link capacitor voltage was $4.155\,V$, which is 0.69% of the total DC-link voltage. Thus, the proposed MPC algorithm was able to maintain neutral point balancing with only minor ripples. So, under steady-state working conditions, the proposed MPC algorithm can achieve active and reactive power tracking, stable current and voltage output, and neutral point balancing.

5.3.2 Active Power Tracking under Dynamic Conditions

The robustness of the proposed MPC algorithm was also assessed. The active power reference was stepped down from $31\,kW$ to $24\,kW$ at $0.3\,s$, then increased to $41\,kW$ at $0.5\,s$. Under these dynamic conditions, the proposed algorithm was able to achieve active power tracking, reduce the switching frequency and lower THD of output currents compared to a conventional MPC algorithm in [82]. The results of this dynamic simulation are analysed in the following subsections.

The performance of the proposed algorithm under dynamic conditions is shown in Figure 5.2. From the simulation results, it can be seen that the active power (P) was able to track to the step changes rapidly. At the same time, the reactive power (Q) remained at zero across the whole duration of the simulation. Figure 5.11(b) shows that the output grid voltage was able to maintain a steady three-phase output. Alongside this, the output currents were able to quickly respond to the different steps across the whole transition period without significant overshooting. In Figure 5.11(c), the RMS value of fluctuations in the DC-link capacitor voltage was $4.330\,V$, which was 0.721% of the total DC-link voltage. Thus, it can be seen that the proposed MPC algorithm is able to keep the DC-link capacitor voltages balanced across dynamic changes. The



(a)

(b)

(c)

Figure 5.1: Simulation results for the proposed MPC algorithm under nominal operating conditions: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

THD of the grid currents was, variously, 2.78% ($P = 31\,kW$), 3.62%($P = 24\,kW$), and 2.13%($P = 41\,kW$) (see in Figure 5.3). So, the proposed algorithm was able to keep the RMS value of the output grid current fluctuations sufficiently low that they all met the $IEEE\ Standard$ $519 - 2014$ requirements. Blown-up depictions of the waveforms for the last active power step (from $24\,kW$ to $41\,kW$ at $0.5\,s$) are shown in Figure 5.4 for the period from $0.49\,s$ to $0.51\,s$.

5.3.3 Reduction of Switching Frequency under Dynamic Conditions

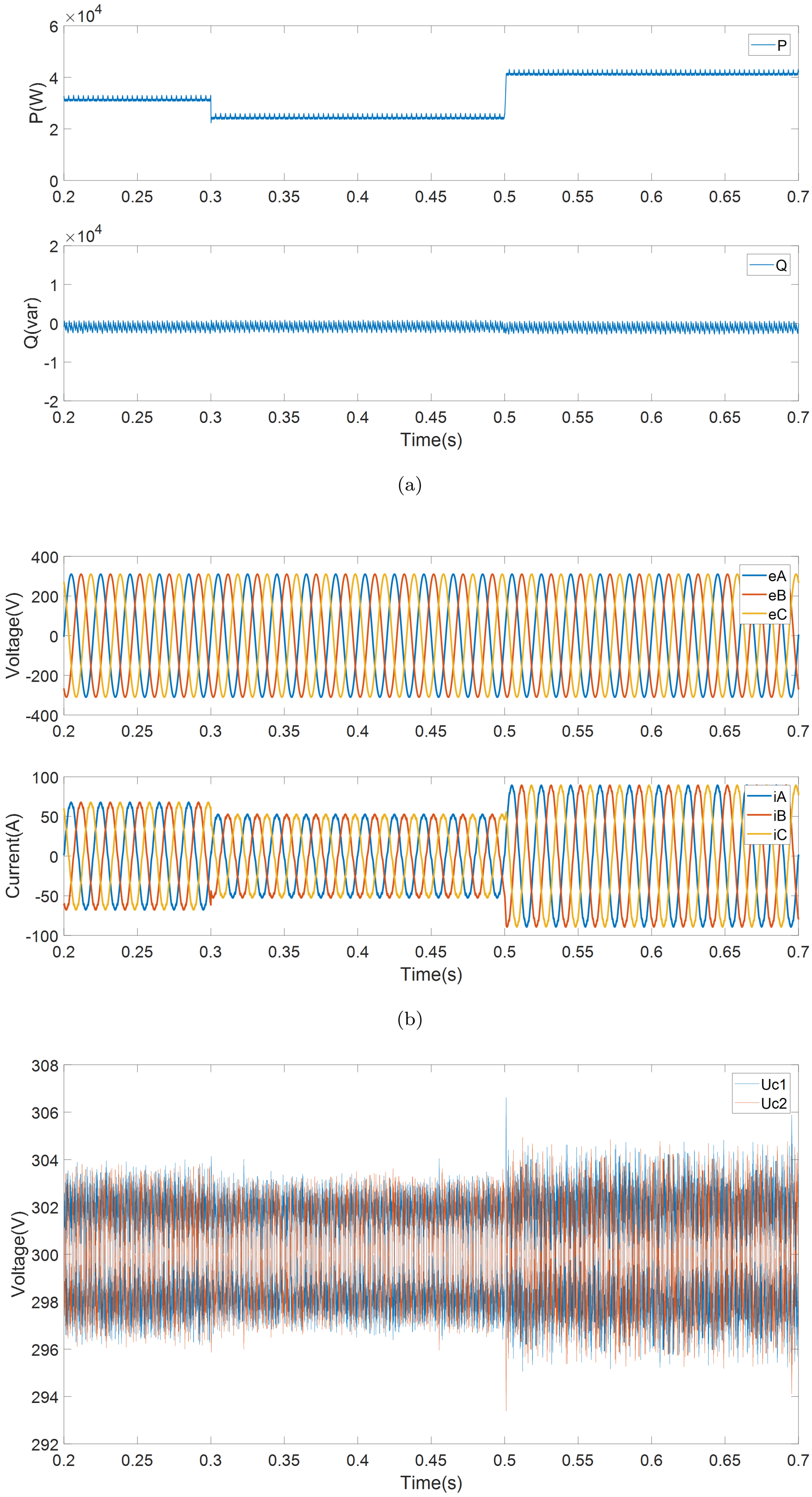
The switching frequency associated with the conventional MPC algorithm was defined in [21], as indicated in Equation 3.29. During the dynamic simulation, the active power reference was stepped down from $31\,kW$ to $24\,kW$ at $0.3\,s$, then up to $41\,kW$ at $0.6\,s$. Over the same dynamic period of operation, the switching frequency using the conventional MPC method [82] would have been $3.815\,kHz$. Over the same period, the proposed MPC algorithm reduced the switching frequency by 30.22% to $2.662\,kHz$. The cumulative switch changes for each phase for the proposed MPC were also lower than the conventional MPC. The switching frequency and cumulative switch changes for each phase are shown in Table 5.2. The proposed algorithm is able to significantly reduce the switching frequency because the current slope control can suppress current fluctuations so that they only fall within a small range, enabling the current slope to follow the reference current slope closely. This results in a remarkably reduced switching loss when compared to the conventional MPC algorithm.

Table 5.2: Switching Frequency and Cumulative Switch Changes

	Conventional [82]	**Proposed method**
Switching Frequency	$3.815\,kHz$	$2.662\,kHz$
Cumulative Switch Changes in A Phase	$15250\,times$	$10670\,times$
Cumulative Switch Changes in B Phase	$15240\,times$	$10630\,times$
Cumulative Switch Changes in C Phase	$15300\,times$	$10650\,times$

5.3.4 Output Current THD Reduction during Dynamic Conditions

The proposed MPC algorithm can also reduce the THD of the output currents, thus improving their quality. Figure 5.3 shows the THD values for the proposed algorithm during dynamic operation. They all met the $IEEE\ Standard$ $519 - 2014$ requirements. Comparison results for the conventional MPC algorithm in [82] are provided in Table 5.3. It will be noted from these that the THD values of the output currents for the proposed algorithm are lower than they are for the conventional MPC algorithm across all three different power steps, $31\,kW$, $24\,kW$ and $41\,kW$. The results are also graphically displayed in Figure 5.5. The zoomed portion of the figure shows the active power



(a)

(b)

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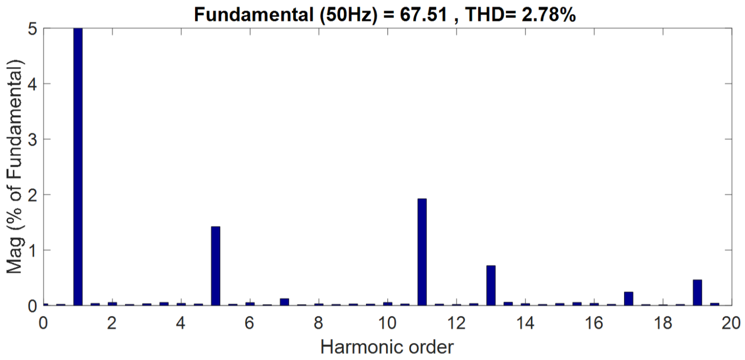
Figure 5.2: Simulation results for the proposed MPC algorithm under dynamic operating conditions: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.



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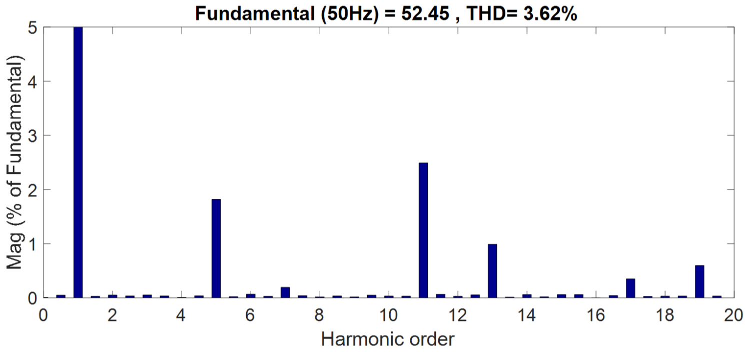

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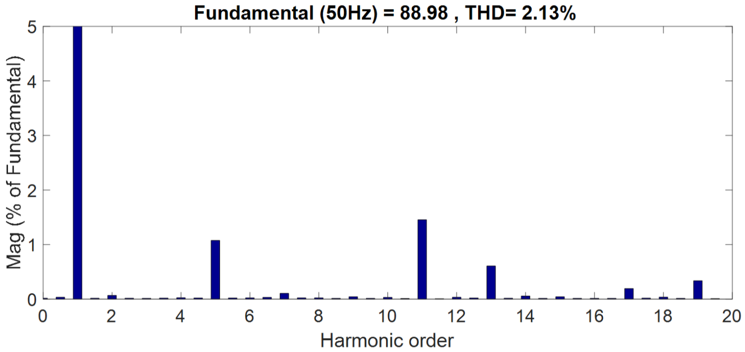
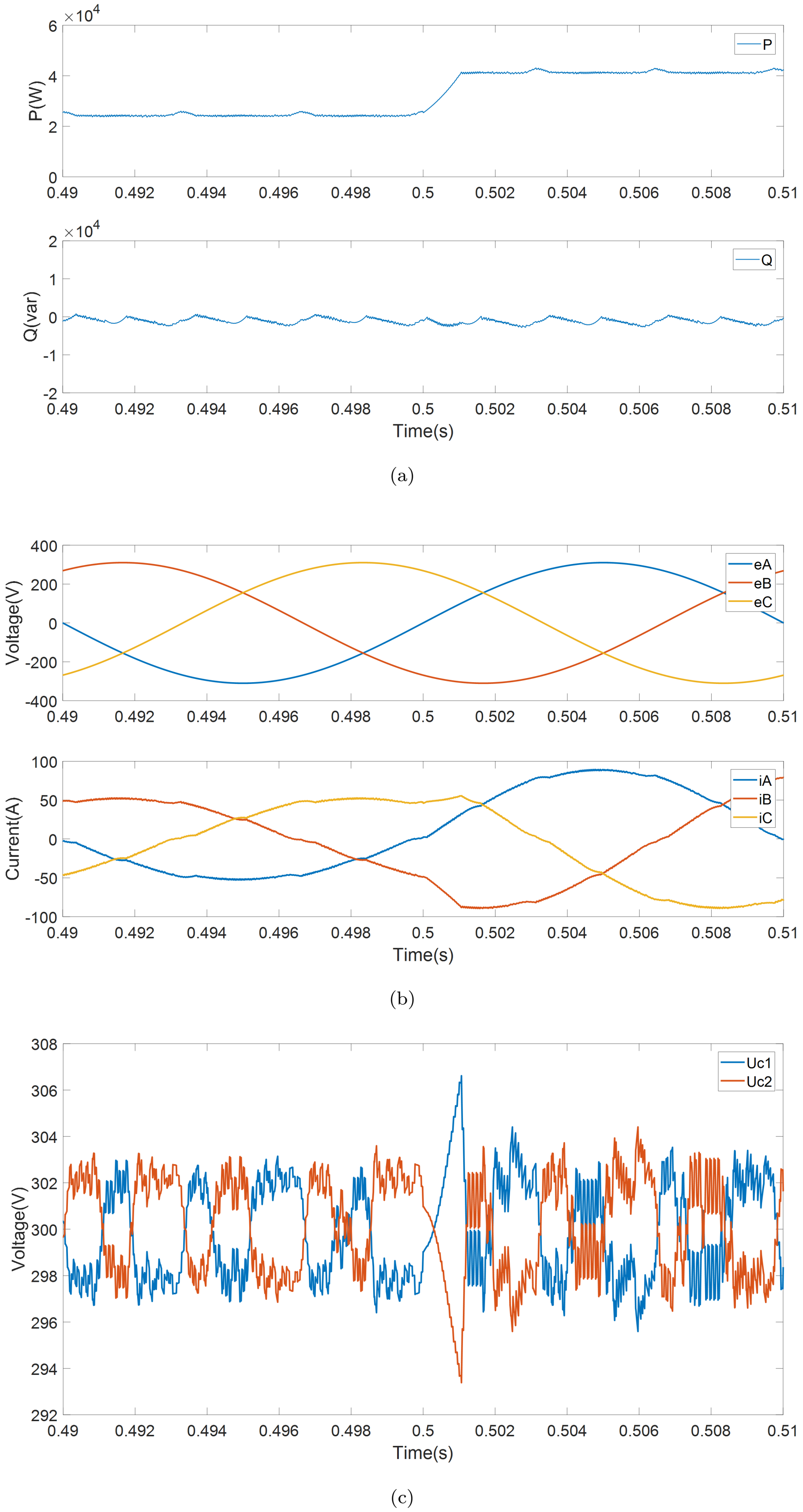


(c)

Figure 5.3: THD of the output currents under dynamic conditions: (a) $P = 31\,kW$ and THD=2.78%, (b) $P = 24\,kW$ and THD=3.62%, and (c) $P = 41\,kW$ and THD=2.13%



(a)

(b)

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Figure 5.4: Zoomed results between 0.49 s and 0.51 s: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

increasing from $24\,kW$ to $41\,kW$ at $0.5\,s$. The blue line (the A phase output current for the proposed algorithm) fluctuates less than the red line (the A phase output current for the conventional algorithm). This is a direct consequence of the current slope control which can select the optimal voltage vectors, keeping the output current smooth. The comparative results effectively serve to confirm that the proposed MPC algorithm with a current slope control objective can achieve lower THD values than the conventional MPC algorithm.

Table 5.3: Comparative Results for the THD of Output Currents under Dynamic Conditions

Period (s)	**Power (kW)**	**Conventional MPC (THD value)**[82]	**Proposed MPC (THD value)**
0.0-0.3	31 (+31%)	2.87%	2.78%
0.3-0.5	24 (-23%)	3.68%	3.62%
0.5-1.0	41 (+71%)	2.20%	2.13%
Cumulative Switch Changes (Times)	**A Phase**	15250	10670
	B Phase	15240	10630
	C Phase	15300	10650
Switching Frequency (kHz)		3.815	2.662
RMS Values of Capacitor Voltage Error (V)		4.041	4.155

5.3.5 Parameter Sensitivity

In this subsection, the parameter sensitivity of the proposed MPC algorithm (in this case, inductance) was analysed and compared to the conventional MPC algorithm [82]. The waveforms relating to the simulation results are shown in Figure 5.6. From the results, it can be seen that the proposed MPC algorithm can overcome misidentification of the inductances with variations in the parameter having no significant effect on the system. Thus, even when confronted with parameter variability, the performance of the proposed MPC algorithm remains better than the conventional MPC algorithm in terms of the THD of the output current and switching frequencies.

In this simulation, the active power reference was $31\,kW$, and the reactive power reference was $0\,VAR$. The load inductance, L, was initially $1.5e-3\,H$. Over the period of $0.2\,s$ to $0.3\,s$, the value of the inductance was increased to $2e-3\,H$, i.e., by 25%. The THD values for the conventional MPC and the proposed MPC were 2.88% and 2.80%, respectively. Over the next $0.1\,s$, from $0.3\,s$ to $0.4\,s$, the value of the inductance continued to increase to $3e-3\,H$ i.e., to 50% greater than the initial inductance of $1.5e-3\,H$. It can be seen from the results in Table 5.4 that, at that point, the output current for the proposed MPC algorithm and the conventional one were the same (2.78%). From

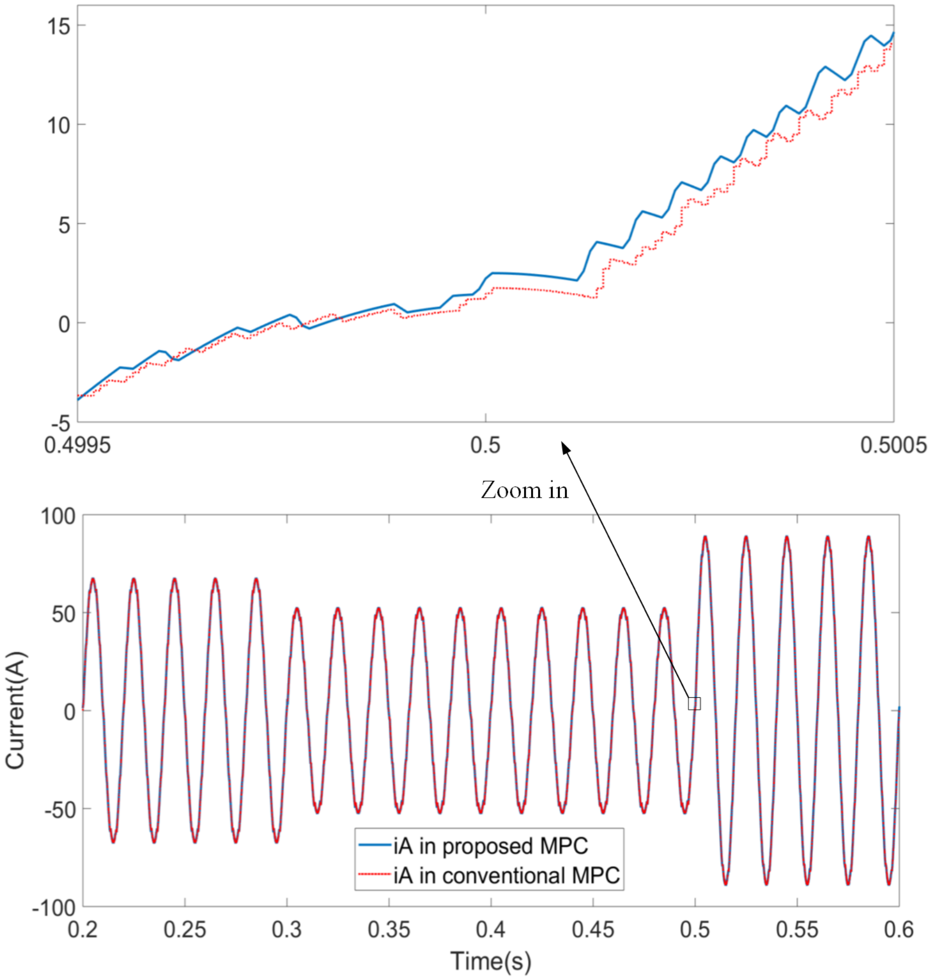
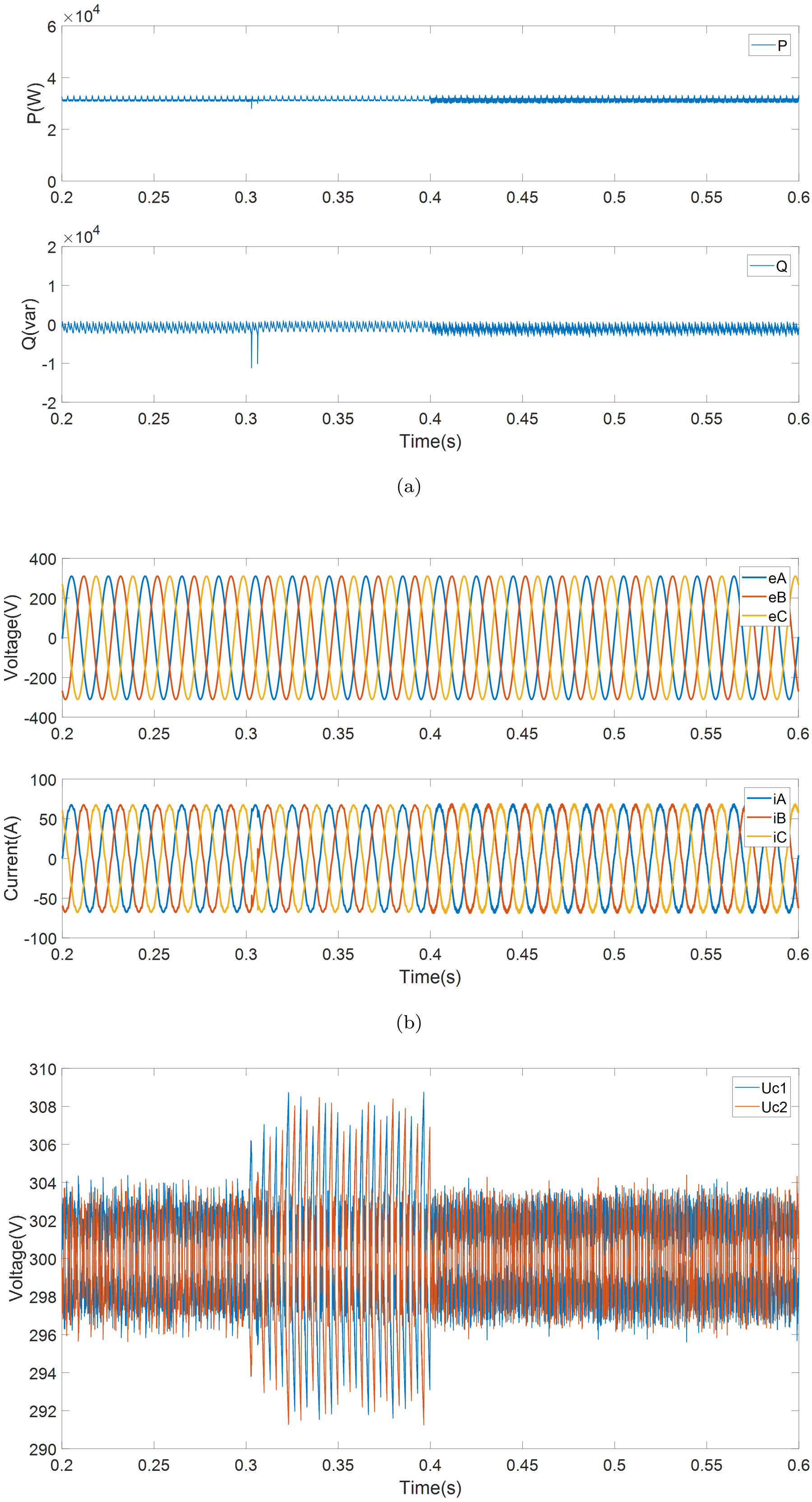


Figure 5.5: Comparative results for the output currents during phase A of the dynamic operation

$0.4\,s$ to $0.5\,s$, the inductance was reduced to $7.5e-4\,H$ i.e., to -75% of the original value. Under these circumstances, the proposed MPC algorithm's output current was slightly better than the conventional one's, with a THD value of 2.92% for the conventional MPC algorithm and 2.91% for the proposed MPC algorithm, respectively. So, overall, the proposed MPC algorithm achieved consistently lower THD values than the conventional MPC algorithm, indicating a generally improved parameter sensitivity.

With regard to the switching frequency and capacitor voltage RMS error values, the performance of the proposed MPC algorithm was consistently better than the conventional MPC algorithm, especially in relation to the switching frequency. The switching frequency was more than 30.678% lower than the conventional MPC algorithm, which generated a frequency of $3.804\,kHz$, while the proposed MPC algorithm generated just $2.637\,kHz$ under the same operating conditions. The RMS value for the DC-link capacitor voltage errors when using the proposed MPC algorithm was $4.658\,V$. This was slightly higher than the RMS value for the DC-link capacitor voltage errors when using the conventional MPC algorithm, which was $4.443\,V$.



(a)

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Figure 5.6: Simulation results for the proposed MPC algorithm under parameter sensitivity conditions: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 5.4: Comparative Results for the THD of the Output Currents in Parameter Sensitivity

Period (s)	**Inductance (H)**	**Conventional MPC (THD value)**[82]	**Proposed MPC (THD value)**
0.2-0.3	2e-3 (+25%)	2.88%	2.80%
0.3-0.4	3e-3 (+50%)	2.78%	2.78%
0.4-1.0	7.5e-4 (-75%)	2.92%	2.91%
Cumulative Switch Changes (Times)	**A Phase**	15230	10570
	B Phase	15130	10520
	C Phase	15290	10550
Switching Frequency (kHz)		3.804	2.637
RMS Values of Capacitor Voltage Error (V)		4.443	4.658

5.4 Different Plants with Representative Parameters

Two sets of different plants with representative parameters (Case A and Case B in the following list) have been used for the proposed algorithms based on the current slope control objective in order to verify performance. The two cases are representative of practical applications in industry and our daily life. Through these two different plants with representative parameters, the performance of the proposed MPC control algorithm can be better displayed. The contents of two different plants with representative parameters (Case A and Case B) would be given in the following.

Case A: 3kV 1MW HVDC (high-voltage direct current) system, source from: [New 4.5 kV IGBT and diode chip set for HVDC Transmission Applications in infineon.com].

Case B: 600V 400kW UPS (uninterruptible power supply) application system, source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com].

5.4.1 Case A

The proposed MPC algorithm was validated in Case A by simulating a $3\,kV$ $1\,MW$ system. The characteristics for Case A are taken from HVDC system, as described in [New 4.5 kV IGBT and diode chip set for HVDC Transmission Applications in infineon.com]. To evaluate the system's resilience, the active power reference P^* was reduced from $1\,MW$ to $0.6\,MW$ at $0.2\,s$ and subsequently to $0.22\,MW$ at $0.4\,s$. At $0.6\,s$, it would rise to $0.4\,MW$. Simultaneously, the reactive power reference, Q^*, was kept at zero to preserve a unity power factor.

The outcomes of Case A are shown in Figure 5.7 and in Table 5.5. Figure 5.7(a) shows the active power, P, and the reactive power, Q. As shown in this figure, the proposed MPC

Table 5.5: The Case A

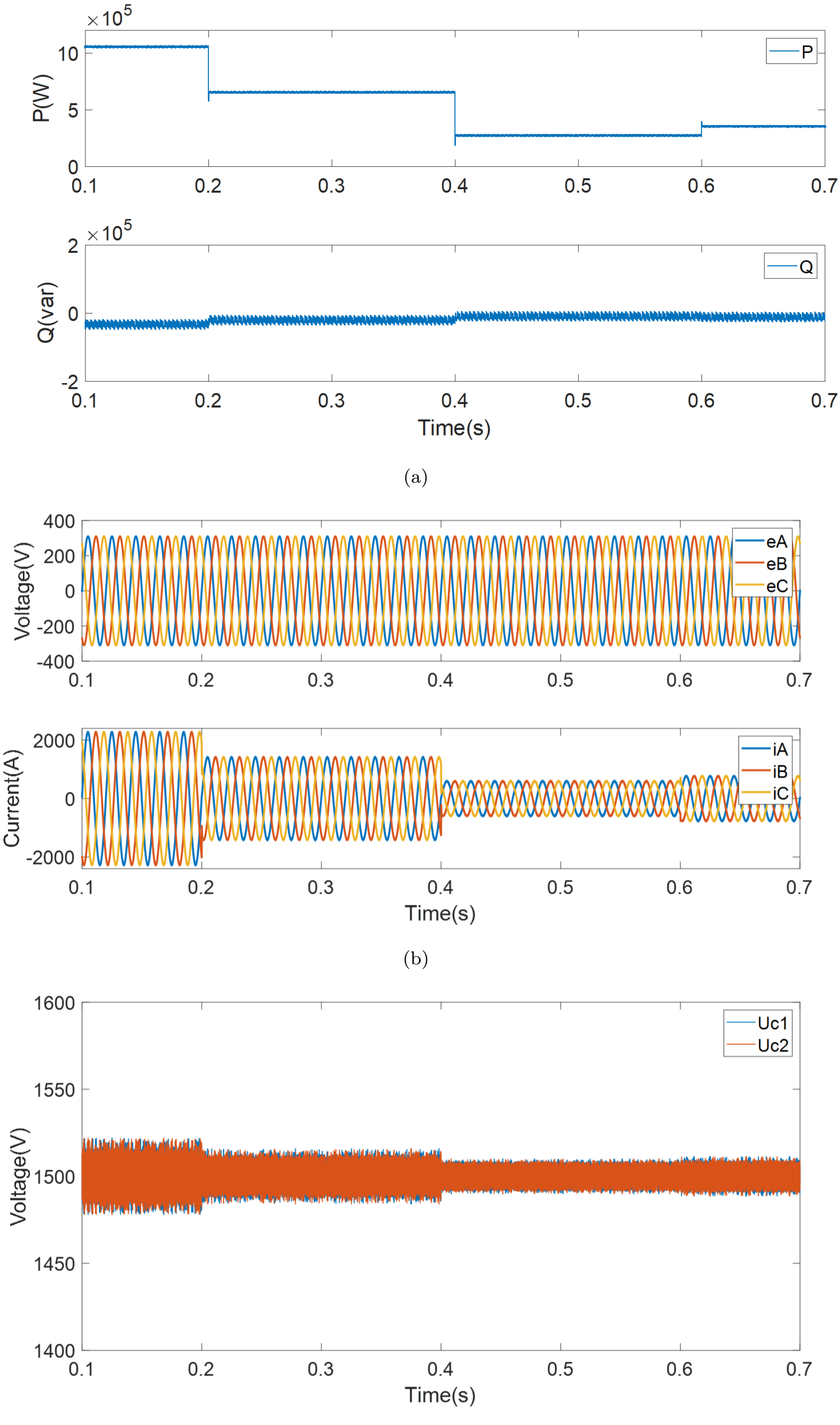
Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (MW)	1	0.6	0.22	0.4
THD	0.77%	1.25%	3.03%	2.34%
RMS(V)	10.29			
Switching frequency(kHz)	6.878			

algorithm was capable of tracking both the active power and the reactive power even when the active power reference changed (i.e., stepping down from 1 MW to 0.6 MW at 0.2 s, then going up from 0.22 kW at 0.4 s to 0.4 MW at 0.6 s). Figure 5.7 illustrates the grid voltages, e_A, e_B, e_C, and the grid currents, i_A, i_B, i_C. Table 5.5 summarises the total harmonic distortion (THD) values for the grid currents. The THD values of 0.77% at 1 MW, 1.25% at 0.6 MW, 3.03% at 0.22 MW, and 2.34% at 0.4 MW are reported. As a result, the suggested MPC algorithm can provide high-quality output currents and voltages. The voltages of the DC-link capacitors , U_{c1} and U_{c2}, are shown in Figure 5.7(c). The RMS error for the DC-link capacitor fluctuation was 10.29 V. Figure 5.7(c) depicts the waveform of the DC-link capacitor fluctuation.

5.4.2 Case B

In Case B, a simulated 600 V 400 kW system was used to validate the proposed MPC algorithm. The UPS application system provides the specifications for Case B, source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com]. To evaluate the robustness of the system, the active power reference P^* was reduced from 400 kW to 450 kW at 0.2 s and subsequently to 250 kW at 0.4 s. It would reach 300 kW at 0.6 s. At the same time, the reactive power reference, Q^*, was held constant to preserve a unity power factor.

Case B's findings are shown in Figure 5.8 and Table 5.6. The active power, P, and the reactive power, Q are shown in Figure 5.8(a). As shown in this figure, the proposed MPC algorithm was able to track the active power and the reactive power even when the active power reference changed (i.e., stepping up from 400 kW to 450 kW at 0.2 s, then increased from 250 kW at 0.4 s to 300 kW at 0.6 s). Figure 5.8(b) depicts the grid voltages, e_A, e_B, e_C, and the grid currents, i_A, i_B, i_C. Table 5.6 summarises the total harmonic distortion (THD) values for the grid currents. The values of the THD are 2.30% at 400 kW, 2.05% at 450 kW, 3.61% at 250 kW, and 3.04% at 300 kW. Thus, the proposed MPC algorithm is capable of generating output currents and voltages of excellent quality. Figure 5.8(c) illustrates the voltages of the DC-link capacitors , U_{c1} and U_{c2}. The RMS error for the fluctuation of the DC-link capacitors was 10.88 V.



(a)

(b)

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Figure 5.7: Results for the Case A: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

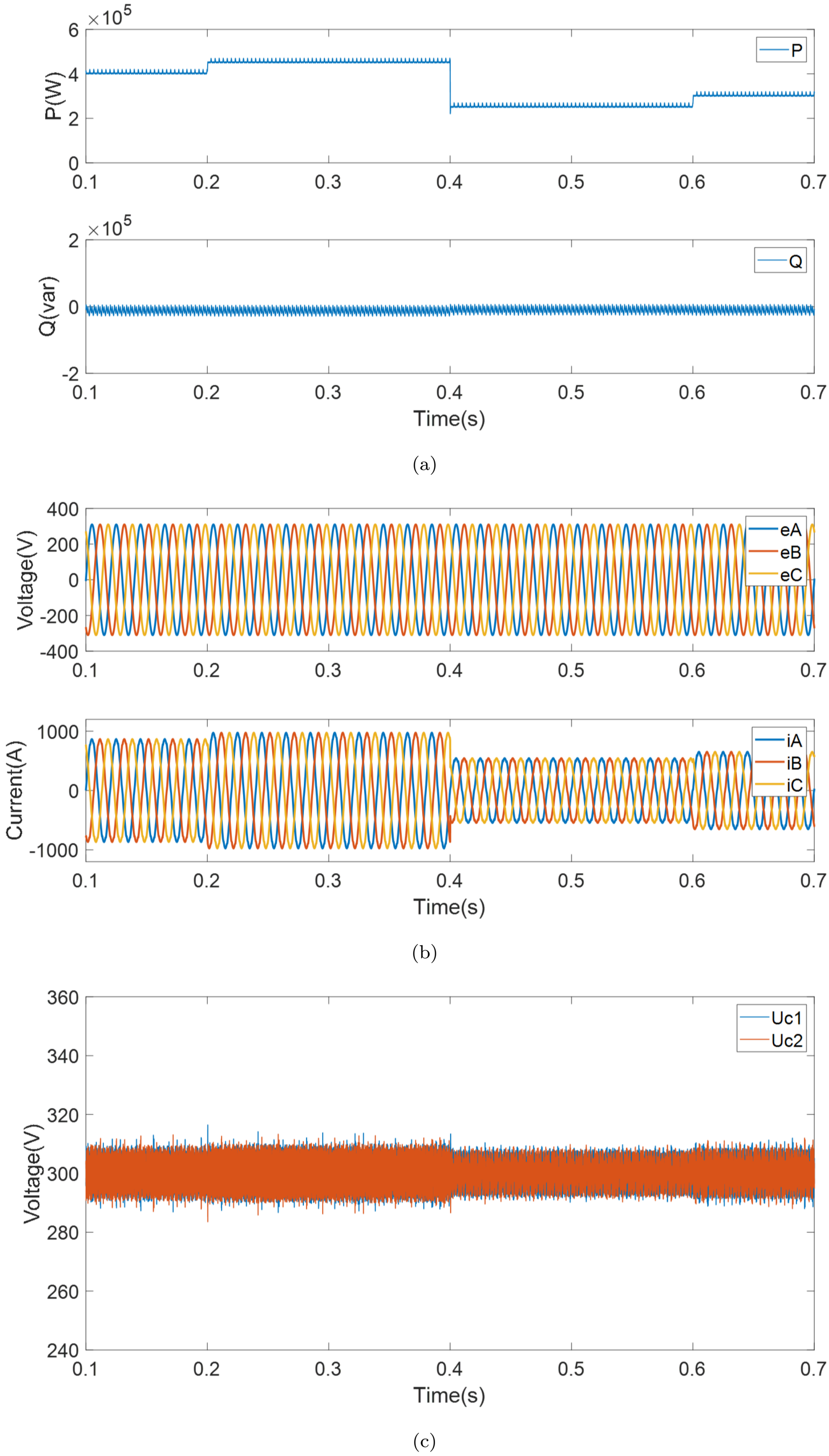


Figure 5.8: Results for the Case B: (a) The active power, P, and the reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 5.6: The Case B

Period (s)	0-0.2	0.2-0.4	0.4-0.6	0.6-1.0
Power (kW)	400	450	250	300
THD	2.30%	2.05%	3.61%	3.04%
RMS(V)	10.88			
Switching frequency(kHz)	5.867			

5.5 Comparison among Different Control Algorithms in the Thesis

In this section, the comparison results among different control algorithms in the thesis, including the control algorithms in Chapter 3, in Chapter 4, and in Chapter 5, are demonstrated. Three MPC algorithms were proposed in Chapter 3, but the third MPC algorithm was applied to the grid-connect NPC inverter system. The load applications of the first two proposed MPC algorithms are RL load. Therefore, the third proposed MPC algorithm was assessed here. The comparison results show the improvement of each method.

The simulation parameters and value are shown in Table 5.7. Both the grid-connected NPC inverters and the proposed MPC algorithms were implemented in MATLAB Simulink. The simulation time is from $0.0\,s$ to $1.0\,s$. To test the robustness of the proposed MPC controllers, the active power reference P^* was stepped up from $400\,kW$ to $600\,kW$ at $0.2\,s$, then decreased to $220\,kW$ at $0.4\,s$. Finally, it increased to $300\,kW$ at $0.6\,s$. At the same time, the reactive power reference, Q^*, was maintained at zero to ensure a unity power factor. The load resistor and inductor are $0.002\,\Omega$ and $0.15\,mH$, respectively. The sampling period is $T_s = 100\,\mu s$. The performance of the control algorithms in Chapter 3, in Chapter 4 and in Chapter 5 are shown in the following. The results of the performance are summarized in Table 5.8.

Table 5.7: Simulation Parameters and Value in Comparison among Different Control Algorithms in the Thesis

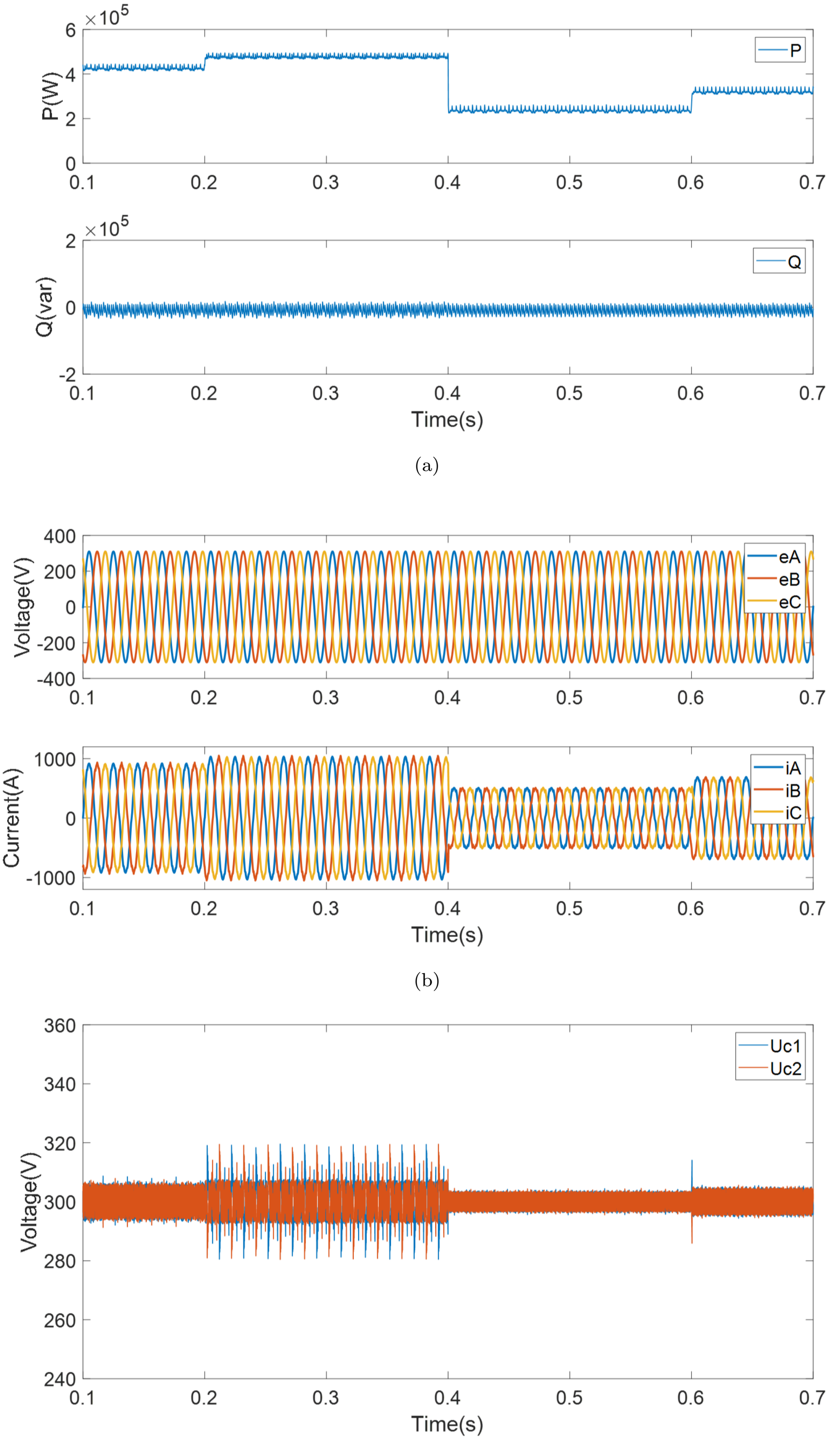
Parameters	**Value**
Start time	$0.0\,s$
Stop time	$1.0\,s$
DC voltage	$600\,V$
Load resistance	$0.002\,\Omega$
Load inductance	$0.015\,mH$
Sampling period	$100\,\mu s$
Grid voltage (phase-to-phase RMS) V_g	$380\,V$
Grid frequency f_g	$50\,Hz$

Table 5.8: Comparative Results for Different Control Algorithms in Chapter 3, in Chapter 4 and Chapter 5

Period (s)	**Power (kW)**	**Chapter 3 (THD value)**	**Chapter 4 (THD value)**	**Chapter 5 (THD value)**
0.2-0.4	450 (+13%)	2.50%	2.44%	2.06%
0.4-0.6	220 (-51%)	4.86%	4.86%	4.10%
0.6-1.0	300 (+36%)	3.70%	3.61%	3.04%
Cumulative Switch Changes (Times)	**A Phase**	41880	20240	23430
	B Phase	39992	19600	23330
	C Phase	40590	19590	23450
Switching Frequency (kHz)		10.20	4.952	5.851
RMS Values of Capacitor Voltage Error (V)		7.713	11.790	10.860

In terms of the performance results in Table 5.8, the proposed MPC algorithms can be made comparisons and seen improvements for each method in different scenarios. The proposed MPC algorithm in Chapter 3 is simpler and easier to be implemented than the two methods proposed in Chapter 4 and Chapter 5. The method mentioned in Chapter 3 is suitable for projects with limited funding or commercial projects in terms of the low associated hardware costs. From the results in Table 5.8 and Figure 5.9, the THD values of the output currents (2.50% in 450kW, 4.86% in 220kW and 3.70% in 300kW), the cumulative switch changes (41880 in A phase, 39992 in B phase and 40590 in C phase) and the switching frequency (10.20kHz) of the proposed MPC algorithm in Chapter 3 are larger than the values of the proposed MPC algorithms in Chapter 4 and Chapter 5. Although the first two performance indexes (the THD value of the output currents and the switching frequencies) are not good, the RMS value of the capacitor voltage error (7.713V) is the smallest. The smallest RMS value of the capacitor voltage error can further demonstrate that this method reduces the hardware costs, which can be used for limited funding or commercial projects.

The proposed MPC algorithm in Chapter 4 is suitable for dynamic systems or in particularly distributed systems such as renewable energy resource ones as they are unstable. The proposed MPC algorithm in Chapter 4 is able to automatically select the weighting factors online without resorting to trial-and-error. The approach centres upon the use of a two-dimensional fuzzy logic control technique that is used to systematically identify the weighting factors within the cost function. The algorithm's main objective is to obtain a lower switching frequency. Regarding to the results in Table 5.8 and Figure 5.10, the switching frequency of the proposed MPC algorithm (4.952kHz) in Chapter 4 is the lowest among these three methods, which is a 51% reduction compared to the proposed MPC algorithm in Chapter 3. The THD values of the output currents (2.44% in 450kW, 4.86% in 220kW and 3.61% in 300kW) are lower than the proposed MPC



(a)

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Figure 5.9: Simulation results for the proposed MPC algorithm in Chapter 3: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

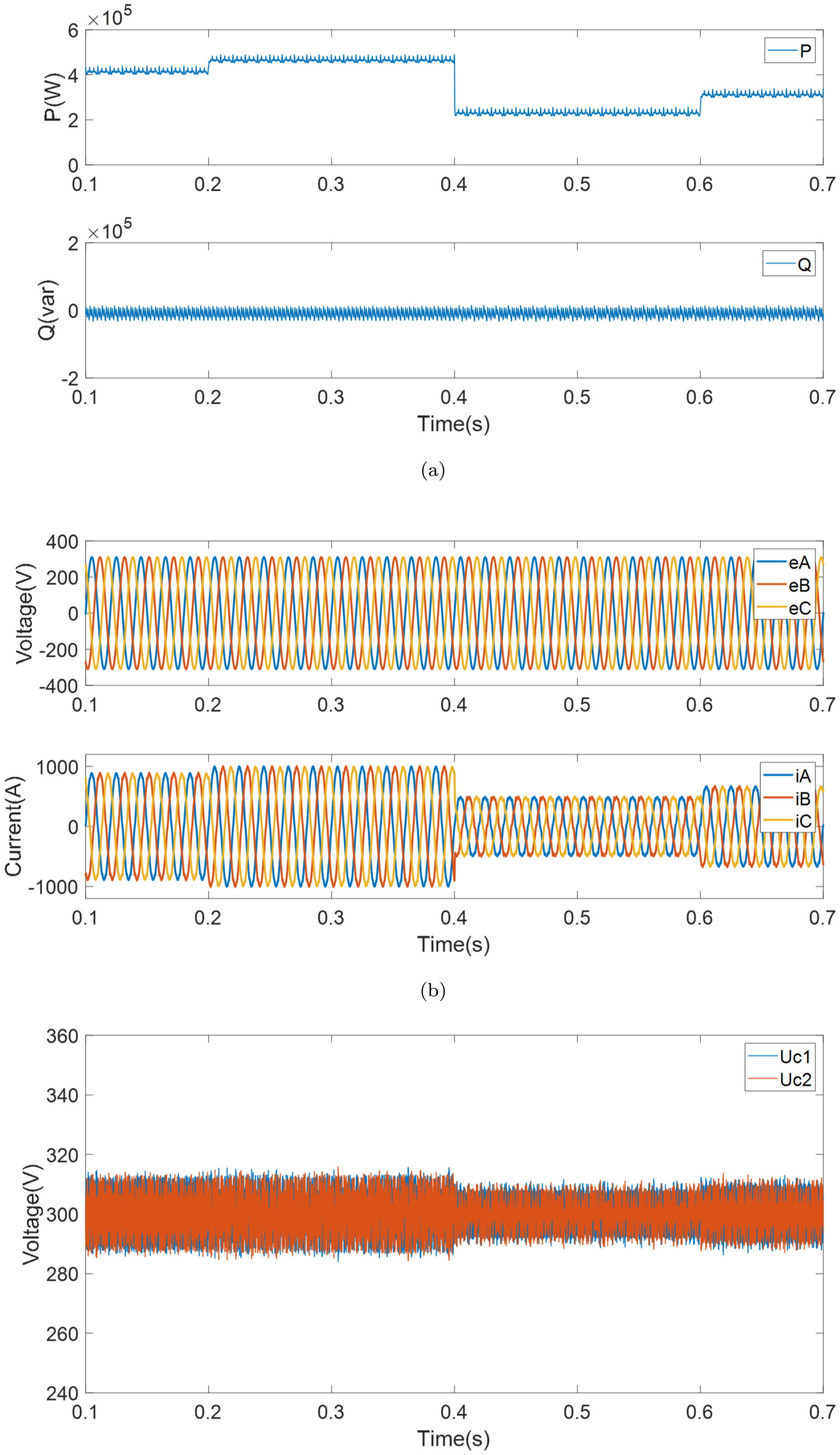
algorithm in Chapter 3 and higher than the proposed MPC algorithm in Chapter 5. The RMS value of the capacitor voltage error ($11.790V$) is the largest for the proposed MPC algorithms in Chapter 4. Therefore, the proposed MPC algorithm in Chapter 4 can effectively reduce the switching frequency and the switching loss. At the same time, this method offers a new way of dealing with the complexity typically associated with grid-connected NPC inverters and thus potentially enhancing their performance in the context of renewable energy resource applications.

The MPC algorithm put forward in Chapter 5 will be applied to low currents' THD scenarios such as large ships, medical equipment, semiconductor industries, and airports. The current slope has been considered a control objective in the cost function of the proposed MPC algorithm in Chapter 5. When the current slope is added in the cost function, the current slope control can suppress current fluctuations. They only fall within a small range, enabling the current slope to follow the reference current slope closely. From the results, this method achieves the lowers THD values of the output currents (2.06% in $450kW$, 4.10% in $220kW$ and 3.04% in $300kW$) among these three proposed MPC algorithms. The switching frequency of the proposed MPC algorithms in Chapter 5 ($5.861kHz$) is a bit higher by 18% than the proposed MPC algorithm in Chapter 4 and much lower by 43% than the proposed MPC algorithm in Chapter 3. The RMS value of the capacitor voltage error for the proposed MPC algorithm in Chapter 5 ($10.860V$) is close to the RMS value of the proposed MPC algorithm in Chapter 4 and higher than the RMS value of the proposed MPC algorithm in Chapter 3. Thus, the MPC algorithm in Chapter 5 is suitable for low currents' THD scenarios.

5.6 Summary

In this chapter, a novel MPC algorithm with the current slope as a control objective has been proposed for 3-level grid-connected NPC inverters. This is the first time the current slope is considered as a control objective in an MPC algorithm. The control objective enables the current slope to match the reference current slope, thus keeping current fluctuations to within a small range. This method not only improves the quality of the output current but also reduces the switching frequency. The following conclusions can be made:

- The results in Figure 5.2 verified the performance of the proposed MPC in nominal operation. Both the active power, P, and reactive power, Q, tracked the reference powers. The proposed MPC algorithm obtained stable output currents and voltages. The THD of the output currents was 2.82%, which met the requirement of $IEEE\ Standard\ 519-2014$. The neutral point of the DC-link capacitor's voltage was kept in balance. The RMS value of the DC-link capacitor fluctuating voltage was $4.155\,V$, which is 0.69% of the total DC-link voltage.



(a)

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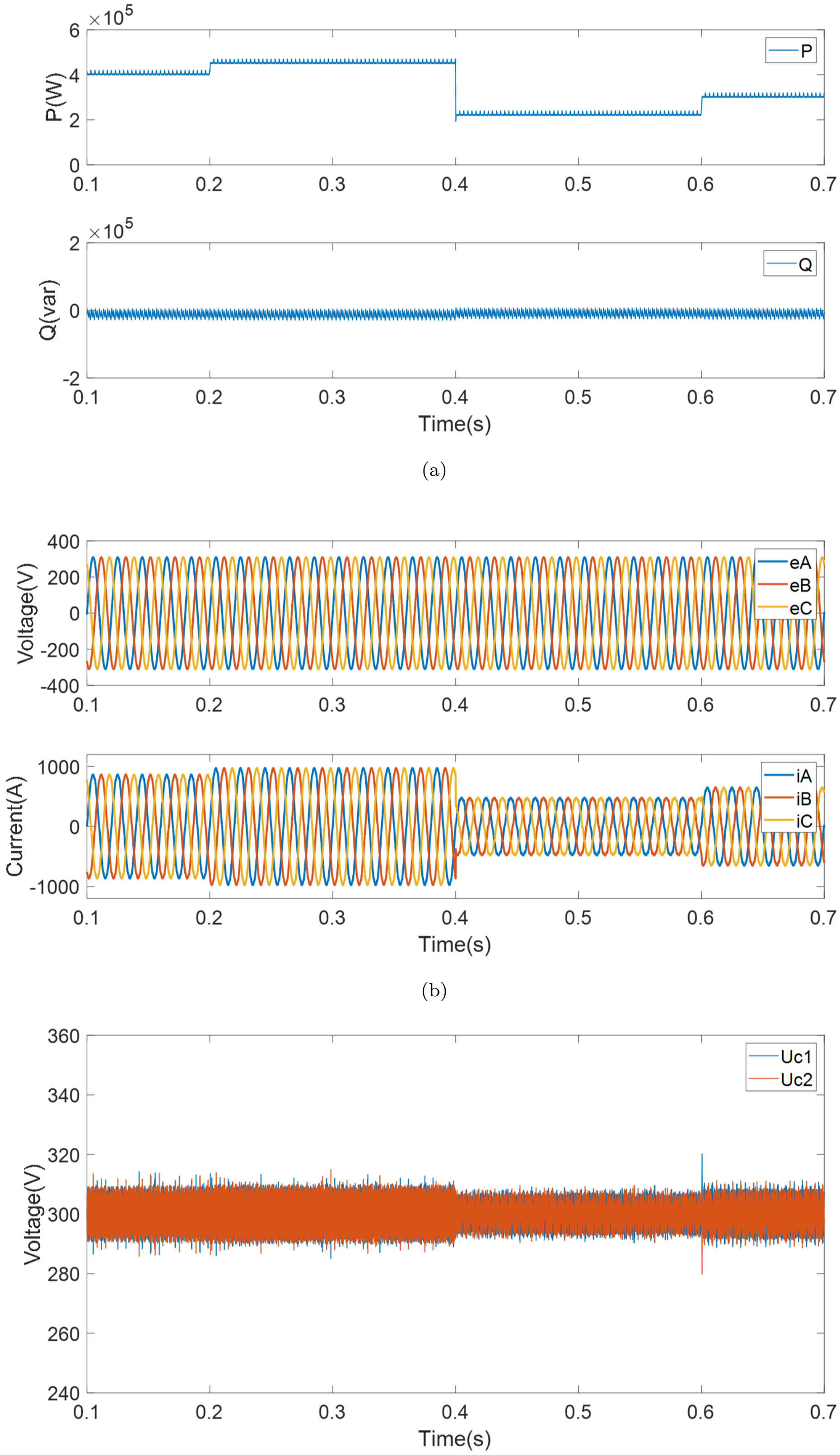
Figure 5.10: Simulation results for the proposed MPC algorithm in Chapter 4: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.



(a)

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Figure 5.11: Simulation results for the proposed MPC algorithm in Chapter 5: (a) The active power, P, and reactive power, Q, (b) The grid voltages, e_A,e_B,e_C, and the grid currents i_A,i_B,i_C, and (c) The voltages of the DC-link capacitors, U_{c1} and U_{c2}.

- The robustness of the proposed MPC algorithm was also assessed in dynamic conditions. The active power reference was stepped down from $31\,kW$ to $24\,kW$ at $0.3\,s$, then increased to $41\,kW$ at $0.5\,s$. Under such dynamic operating conditions, the proposed algorithm was able to maintain active power tracking, reduce the switching frequency by 30.22% and lower THD of output currents, if compared to the performance of the conventional MPC algorithm.

- With regard to parameter sensitivity, the performance of the proposed MPC algorithm was better than the conventional MPC algorithm in terms of the output current's THD and the switching frequencies. For +25%, +50%, and −75% variations in the inductance, the switching frequency of the proposed algorithm was 30.678% lower, and the output current's THD slightly lower compared to the conventional MPC algorithm. Thus, the proposed MPC algorithm offers consistently good performance when confronted with parameter fluctuations.

The effectiveness of the proposed MPC algorithm with the current slope control objective has been identified. The proposed MPC algorithm can implement switching frequency and output current's THD reduction across different operation conditions including nominal operation, dynamic operation and parameter sensitivity.

Chapter 6

Experiment Validation

In order to validate the model predictive control algorithms proposed in Chapter 3, Chapter 4 and Chapter 5, experiments have been carried out. The application of NPC inverters in the high-power industrial case is emphasised in the thesis. Since the safety level of the laboratory was substandard for the high-power scenario, hardware-in-the-loop (HIL) testing [159] was carried out. This chapter is firstly introduced with the experimental setup in section 6.2. Next, experimental results for the proposed model predictive control algorithms in Chapter 3, Chapter 4 and Chapter 5 are demonstrated in section 6.3, section 6.4 and section 6.5. At last, the summary of this chapter is given.

6.1 Hardware-in-the-Loop

Hardware-in-the-Loop (HIL) test system uses a real-time processor to run the system model to implement the operating state of the controlled object, connect with the tested electronic control unit through the I/O interface and perform comprehensive and systematic testing [159][160][161]. Considering safety, reasonable cost, feasibility and efficiency, Hardware-in-the-Loop (HIL) testing has become an important step in the engineering development process [159][160].

For the purpose of safety, the three-level NPC inverter system was tested at hardware-in-the-loop (HIL) experimental environment in Figure 6.1. MATLAB simulation of the whole system was generated hardware description language (HDL) codes on desktop. The plants's power source, inverters and load were operated as a real-time model on this target desktop. Real-time target machine from Pxi box (CPU) to execute the HDL codes generated from MATLAB Simulink. The inverter controller FPGA was tested under nominal, dynamic and parameter sensitivity circumstances, allowing for experimental validation of the proposed MPC algorithms without causing damage to the power equipment. Figure 6.2 shows the laboratory setup for the real-time HIL testing environment.

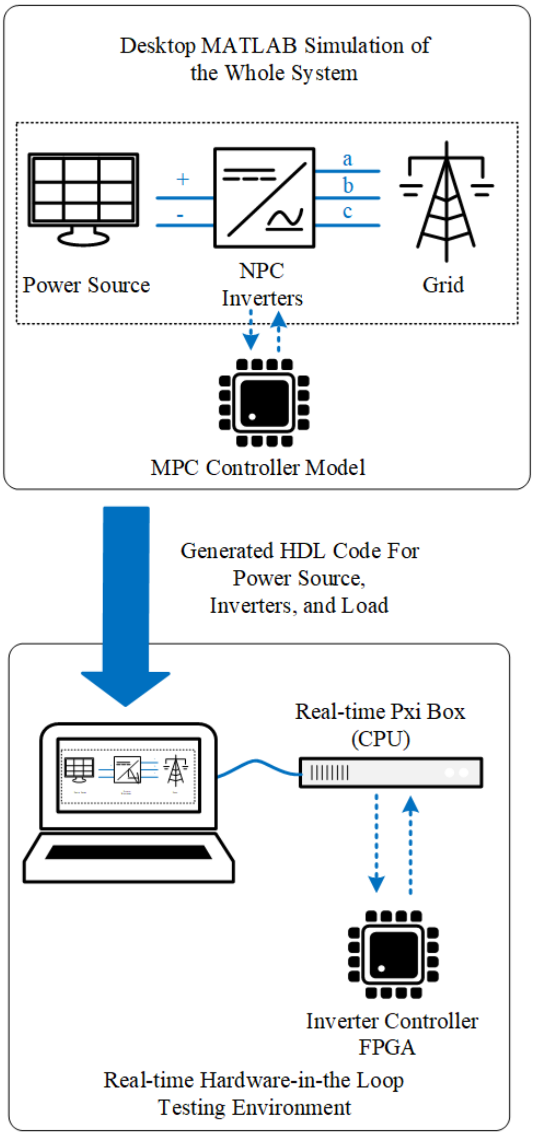

Figure 6.1: The schematic diagram for the Real-time HIL testing environment, source from: [White Paper:HIL Testing for Power Electronics Control Design]

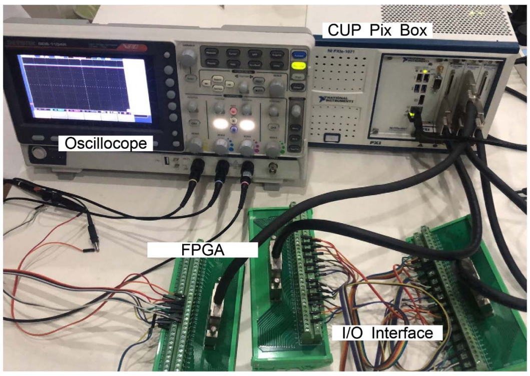

Figure 6.2: The laboratory setup for the Real-time HIL testing environment

6.2 Experimental Setup

A set of two different plants with representative parameters (Case A and Case B) have been used for the proposed algorithms in the thesis to verify the performance of the proposed model predictive control algorithms. These two different plants have been applied in section 3.9, section 4.5 and section 5.4. The two cases are representative of practical applications in industry and our daily life. Through these two different plants with representative parameters, the performance of the proposed MPC control algorithm can be better displayed. The contents of different plants with representative parameters (Case A and Case B) would be given in the following:

Case A: 3kV 1MW HVDC (high-voltage direct current) system, source from: [New 4.5 kV IGBT and diode chip set for HVDC Transmission Applications in infineon.com].

Case B: 600V 400kW UPS (uninterruptible power supply) application system, source from: [PowerWave 33 S2 IEC 160-500 kW UPS in abb.com].

The parameters and values for Case A and Case B are provided in Table 6.1 and Table 6.2.

Table 6.1: Parameters and Value in Case A

Parameters	**Value**
DC-link voltage V_{dc}	$3000\,V$
Load resistance R	$0.02\,\Omega$
Load inductance L	$1.5e-3\,H$
DC-link capacitance C	$4.7e-3\,F$
Grid voltage (phase-to-phase RMS) V_g	$380\,V$
Grid frequency f_g	$50\,Hz$
Sampling period T_s	$1e-4\,s$

Table 6.2: Parameters and Value in Case B

Parameters	**Value**
DC-link voltage V_{dc}	$600\,V$
Load resistance R	$0.001\,\Omega$
Load inductance L	$5e-4\,H$
DC-link capacitance C	$4.7e-3\,F$
Grid voltage (phase-to-phase RMS) V_g	$380\,V$
Grid frequency f_g	$50\,Hz$
Sampling period T_s	$1e-4\,s$

The process of the experimental validation is the same for the MPC algorithms (in Chapter 3, Chapter 4 and Chapter 5) of the 3-level NPC inverter system. During the experimental process, the performance of MPC algorithms for a 3-level NPC inverter grid-connected system was firstly verified under nominal operating conditions. Then, the robustness of the MPC algorithms was also assessed under dynamic operating conditions. In the dynamic process, the active power of reference had been changed. As to Case A, the active power of reference was stepped down from 1MW to 600kW. For Case B, the active power of reference was stepped down from 500kW to 400kW. The last part of the experimental process was parameter sensitivity (load inductance). In Case A, the value of the load inductance went down from 1.5e-3H to 1e-3H. In Case B, the value of the load inductance was reduced from 5e-4H to 4e-4H. The experimental results were described in the following sections.

In order to make the experimental results more convincing, some most salient and highly related MPC algorithms [31][82][137] were picked up to make comparisons. The optimal MPC in [31] is highly related MPC technique and also used for NPC inverters. [82] is a successful and conventional MPC approach. Most researchers use this algorithm [82] to compare results. [137] is the new and most salient multistep MPC algorithm. It should be noted that the predictive horizon of all the proposed MPC algorithms in experiments, [31] and [82] is one-step, while the predictive horizon of [137] is multistep. Even in this case, some output performances of the proposed MPC are still better than that of [137]. The output waveforms and data would be shown in the following sections. By comparing these three MPC methods, the effectiveness of the results can be fully demonstrated.

6.3 Experimental Results for the Proposed Control Algorithms in Chapter 3

In this section, the effectiveness of the proposed MPC algorithm in Chapter 3 was assessed. Three MPC algorithms were proposed in Chapter 3, but the third MPC algorithm was verified experimentally. The load applications of the first two proposed MPC algorithms are RL load. In real life, they are not used as a load. Most researchers use RL load to get preliminary results. The third proposed MPC algorithm in Chapter 3 was extended to the grid-connected scenario. Therefore, the third proposed MPC algorithm was assessed in this section.

Meanwhile, a set of two different plants with representative parameters has been used to validate the performance of the proposed MPC algorithms. They are Case A and Case B, which were described in section 6.2. The parameters and value of the Case A and Case B are listed in Table 6.1 and Table 6.2.

6.3.1 Case A (Nominal Operation)

The 3-level NPC inverter system with the representative parameters of Case A is used for validating the proposed MPC algorithm of Chapter 3. The parameters of the system are presented in Table 6.1. In order to test the effectiveness of the proposed MPC controller, three working conditions were considered: nominal operation, dynamic operation (where the active power reference was stepped down from $1\,MW$ to $600\,kW$; and changes in the parameter sensitivity (-33.3% variations in the inductance from $1.5e-3\,H$ to $1e-3\,H$). Throughout the various tests, the reactive power reference was set at zero to achieve a unity power factor.

The first experiment focused upon the performance of the proposed MPC algorithm under nominal operating conditions in Figure 6.3. The active power of reference was $1\,MW$, and the reactive power of reference was $0\,VAR$ to ensure a unity power factor. In Figure 6.3, it can be seen that the active power, P, and the reactive power, Q, both tracked the reference powers. In Figure 6.3, e_A, e_B, and e_C represent the output grid phase voltages, whose peak values were $310V$. i_A, i_B, and i_C are the output grid currents. So, from Figure 6.3, it can be concluded that the system's output currents and voltages were stable. U_{c1} and U_{c2} are the voltages of the DC-link capacitors. The root-mean-square (RMS) value of the DC-link capacitor fluctuating voltage was $57.467\,V$, which was 1.92% of the total DC-link voltage. This indicates that the proposed MPC algorithm maintained neutral point balancing with reasonable ripples. Therefore, under steady-state working conditions, the proposed MPC algorithm can achieve active power and reactive power tracking, stable current and voltage output, and neutral point balancing.

Comparative results for the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC algorithm in Chapter 3 are provided in Table 6.3. The waveforms relating to the experimental results are shown in Figure 6.4, Figure 6.5 and Figure 6.6. With regards to the results in Table 6.3, the experimental results are analysed from three aspects, including the THD value of the output current, switching frequency and the RMS value of the DC-link capacitor voltage error. The THD values of the output currents 3.54% are lower than the conventional MPC algorithms in [82] (3.88%) and the optimal MPC algorithm in [31] (4.08%), which are higher than the multistep MPC algorithm in [137] (2.29%). The switching frequency of the proposed MPC algorithm ($4.187kHz$) in Chapter 3 is the lowest among these four methods. The switching frequency of the other three methods are $4.680kHz$ the conventional MPC algorithms in [82], $4.645kHz$ the optimal MPC algorithm in [31] and $4.528kHz$ the multistep MPC algorithm in [137]. The RMS value of the capacitor voltage error ($57.465V$) for the proposed MPC algorithm is smaller than the optimal MPC algorithm in [31] ($59.417V$), and larger than the conventional MPC algorithms in [82] ($56.385V$) and the multistep MPC algorithm in [137] ($54.403V$).

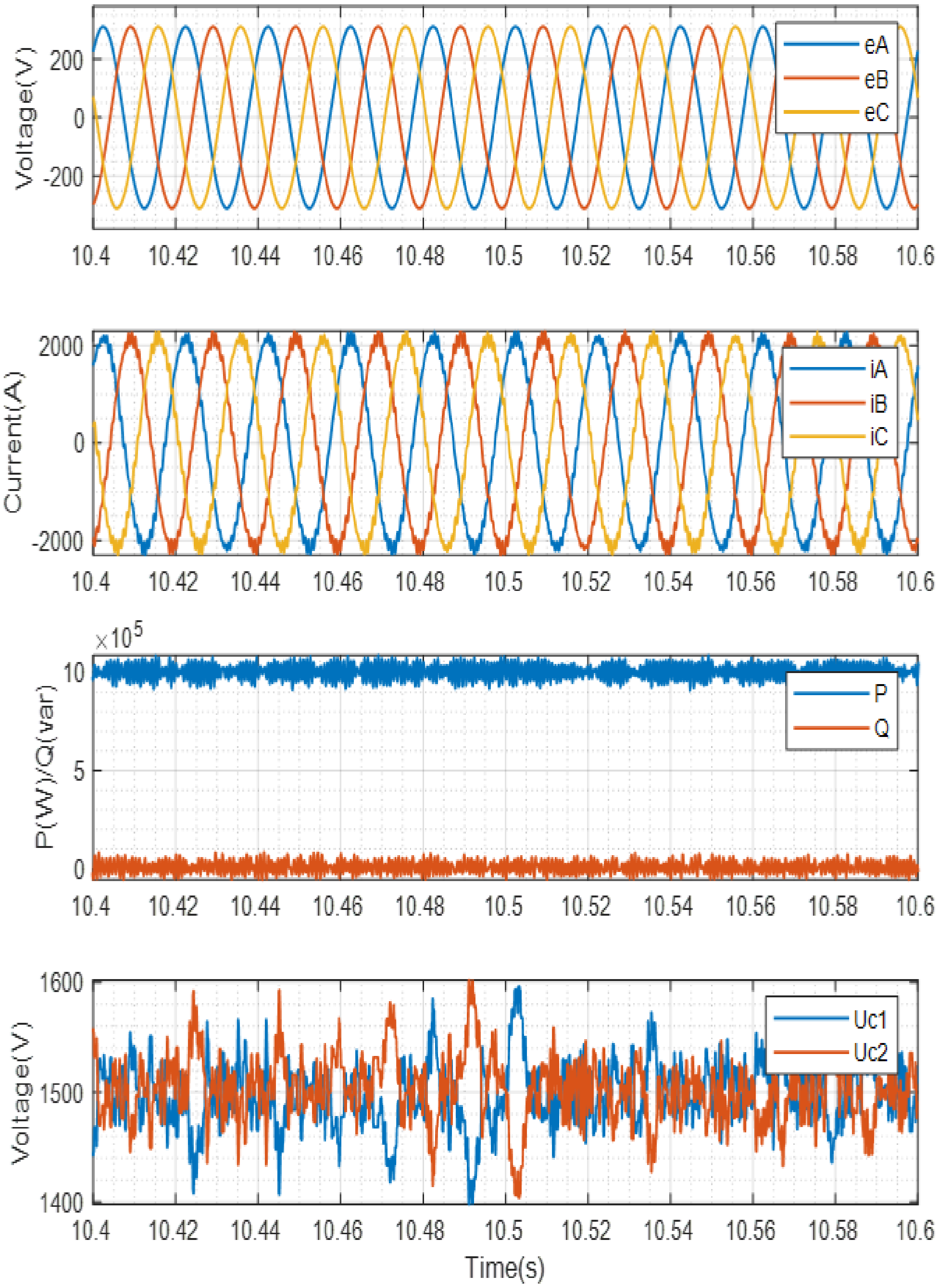

Figure 6.3: Experiment validation results for the proposed MPC algorithm of Chapter 3 under nominal operating conditions (1MV) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

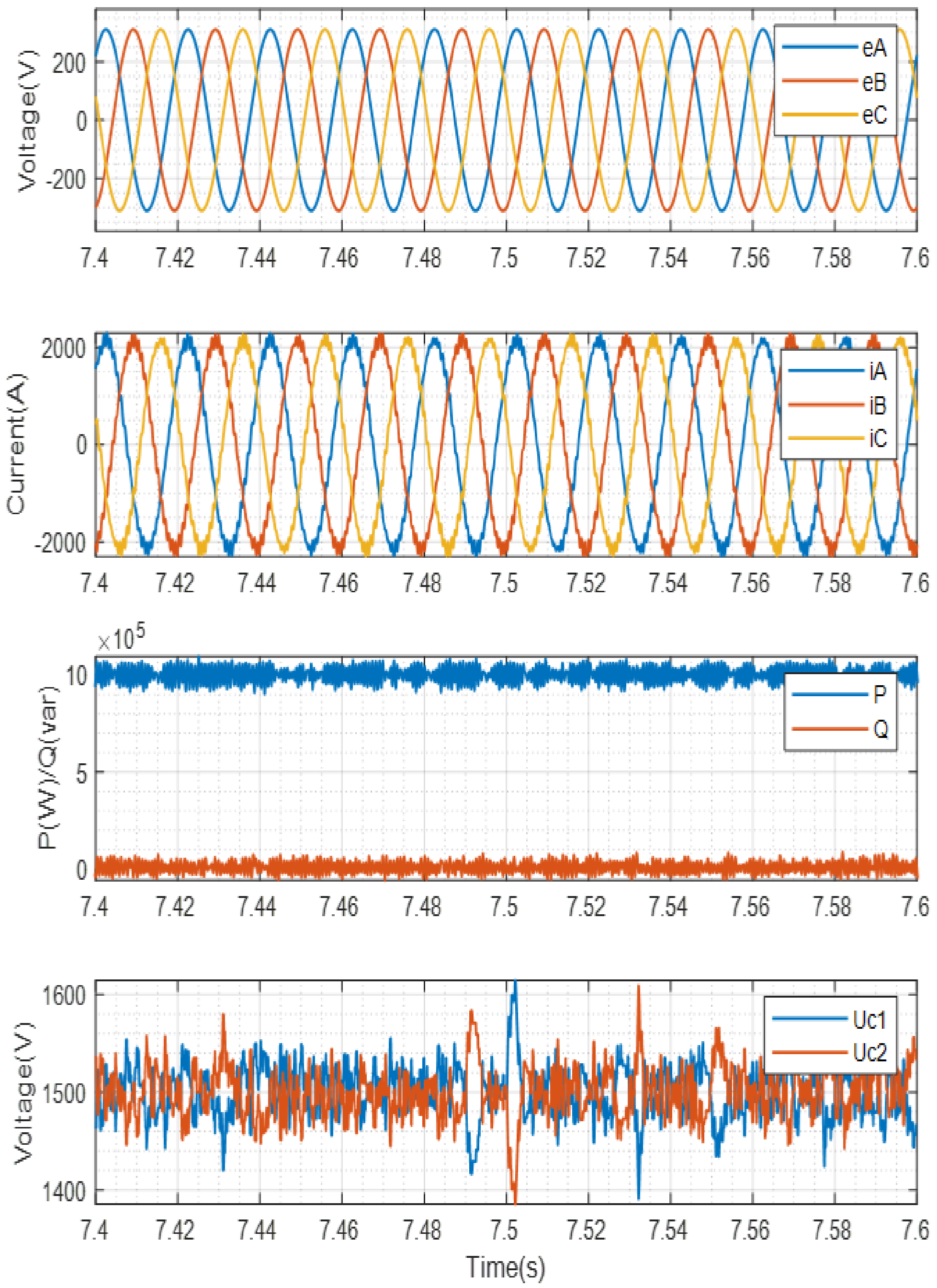

Figure 6.4: Experiment validation results for the MPC algorithm in [82] under nominal operating conditions (1MV) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

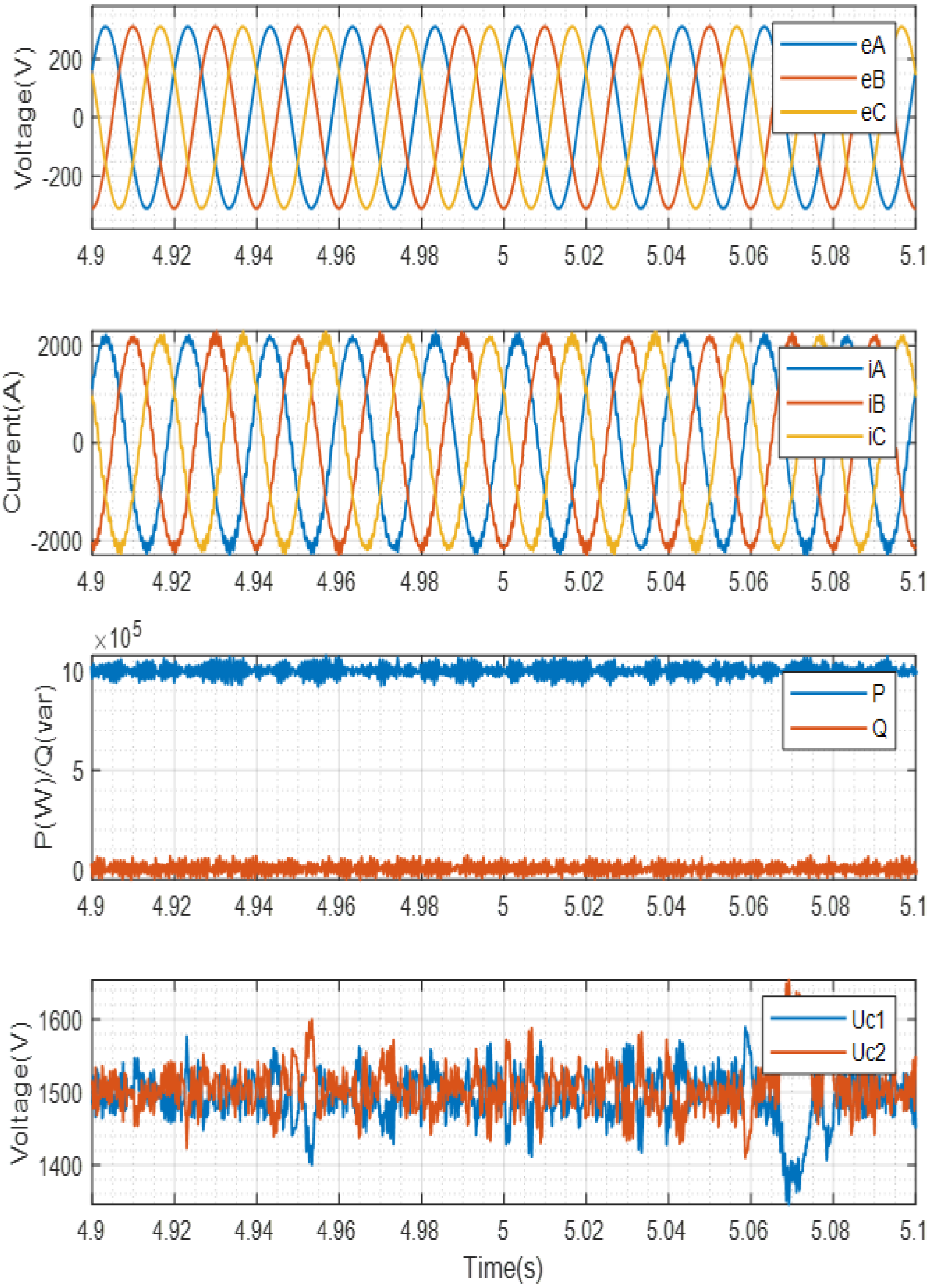

Figure 6.5: Experiment validation results for the MPC algorithm in [31] under nominal operating conditions (1MV) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

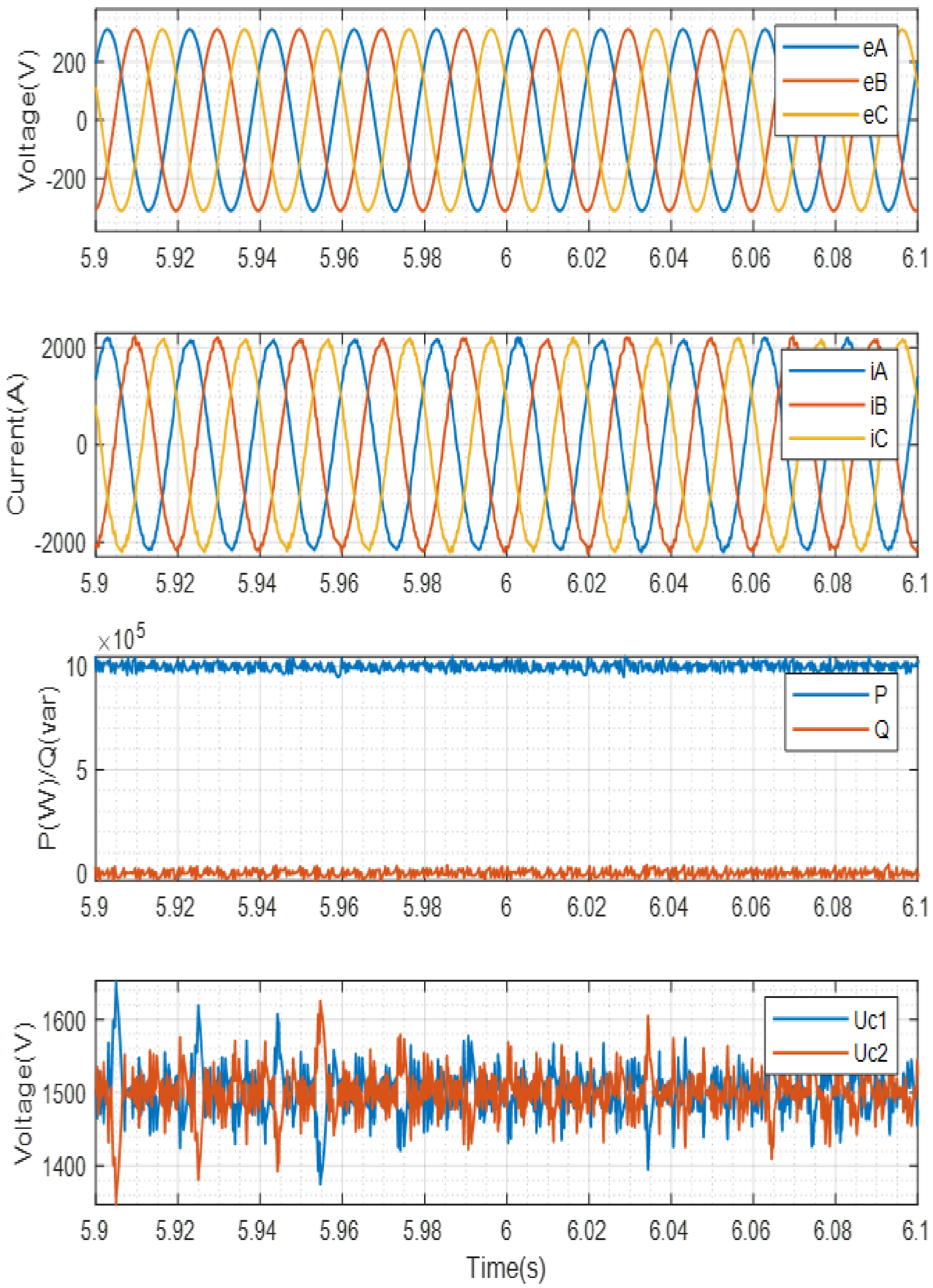

Figure 6.6: Experiment validation results for the MPC algorithm in [137] under nominal operating conditions (1MV) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.3: Comparative Results of Chapter 3 for Different Control Algorithms under nominal operation conditions in Case A (1MW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.54%	3.88%	4.08%	2.29%
Switching Frequency(kHz)	4.187	4.680	4.645	4.528
RMS Values of Capacitor Voltage Error (V)	57.465	56.385	59.417	54.403

6.3.2 Case A (Dynamic Operation)

The robustness of the proposed MPC algorithm was assessed in this section. The active power of reference was stepped down from $1\,MW$ to $600\,kW$. Under these dynamic working conditions, the proposed MPC algorithm achieved active power tracking and reduced the switching frequency.

The transient-state performances of the proposed MPC algorithm are shown in Figure 6.7. From the figures, it can be seen that the active power (P) is able to track the step-change rapidly. At the same time, the reactive power (Q) is maintained at zero across the duration. The output grid voltage was able to maintain a steady three-phase output. At the same time, the output currents were able to quickly respond to the step-change across the whole transition period without overshooting. In Figure 6.7, it can be seen that the RMS value of the DC-link capacitor fluctuating voltage was $29.992V$, which was 1.00% of the total DC-link voltage while maintaining normal operation.

Comparative results for the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC algorithm in Chapter 3 are provided in Table 6.4 under dynamic operating conditions (the active power of reference decreasing from $1\,MW$ to $600\,kW$). The waveforms relating to the experimental results are shown in Figure 6.8, Figure 6.9 and Figure 6.10. The total harmonic distortion (THD) of the grid currents was 3.39% in the proposed MPC algorithm, 5.28% in [82], 4.85% in [31] and 3.40% in [137], respectively, as depicted in Table 6.4. The proposed MPC algorithm achieved the lowest THD value of the output currents. In terms of switching frequency, the proposed MPC algorithm also obtained the lowest value ($4.219kHz$). Others were $4.747kHz$ the conventional MPC algorithms in [82], $4.929kHz$ the optimal MPC algorithm in [31] and $4.528kHz$ the multistep MPC algorithm in [137]. When it came to the RMS value of the capacitor voltage error, the multistep MPC algorithm in [137] ($18.476V$) had the smallest value. The proposed MPC algorithm ($29.992V$) achieved a similar value with the conventional MPC algorithm in [82] ($30.806V$) and the optimal MPC algorithms in [31] ($29.026V$).

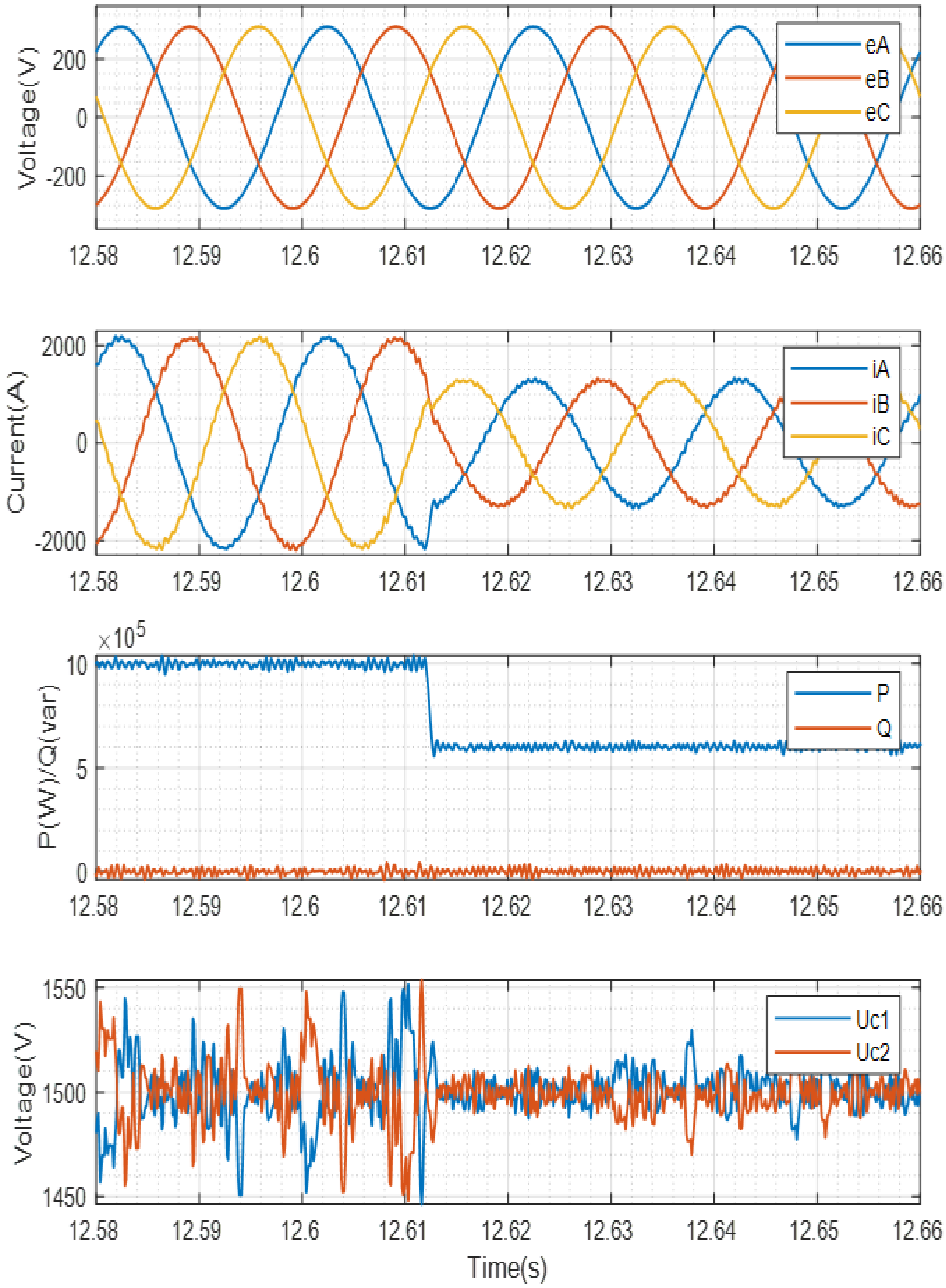

Figure 6.7: Experiment validation results for the proposed MPC algorithm of Chapter 3 under dynamic operating conditions (600kW) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

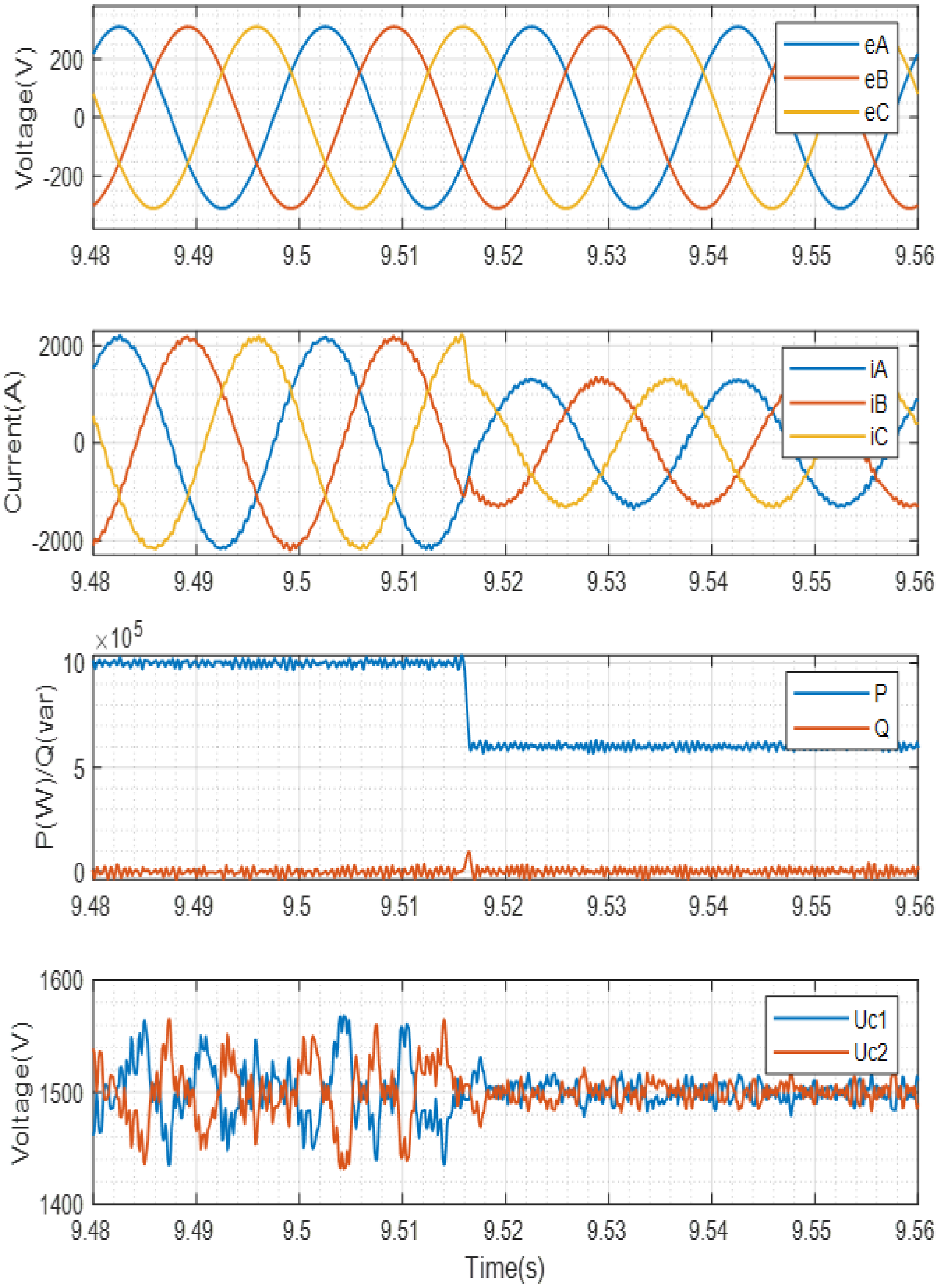

Figure 6.8: Experiment validation results for the MPC algorithm in [82] under dynamic operating conditions (600kW) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

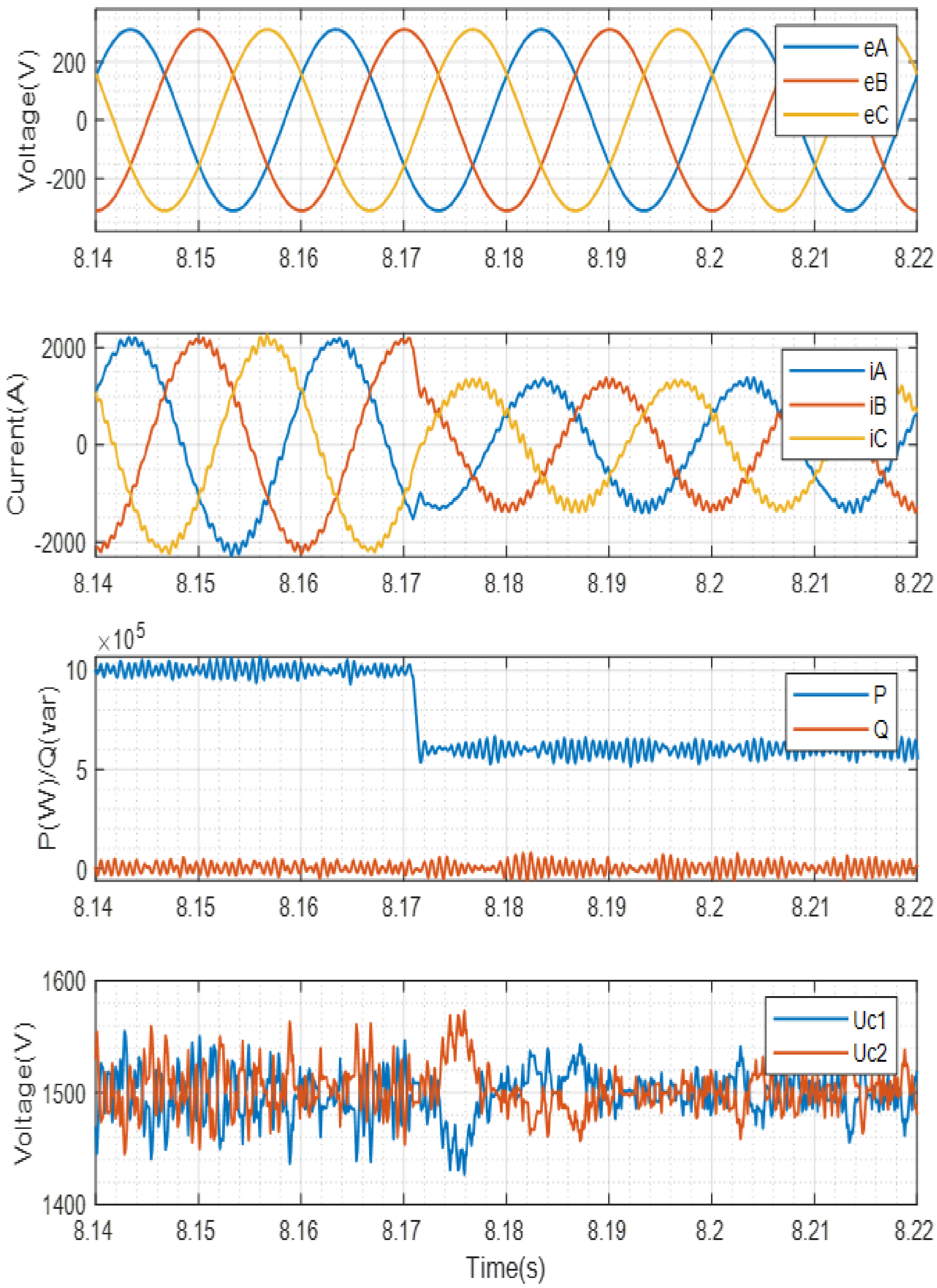

Figure 6.9: Experiment validation results for the MPC algorithm in [31] under dynamic operating conditions (600kW) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

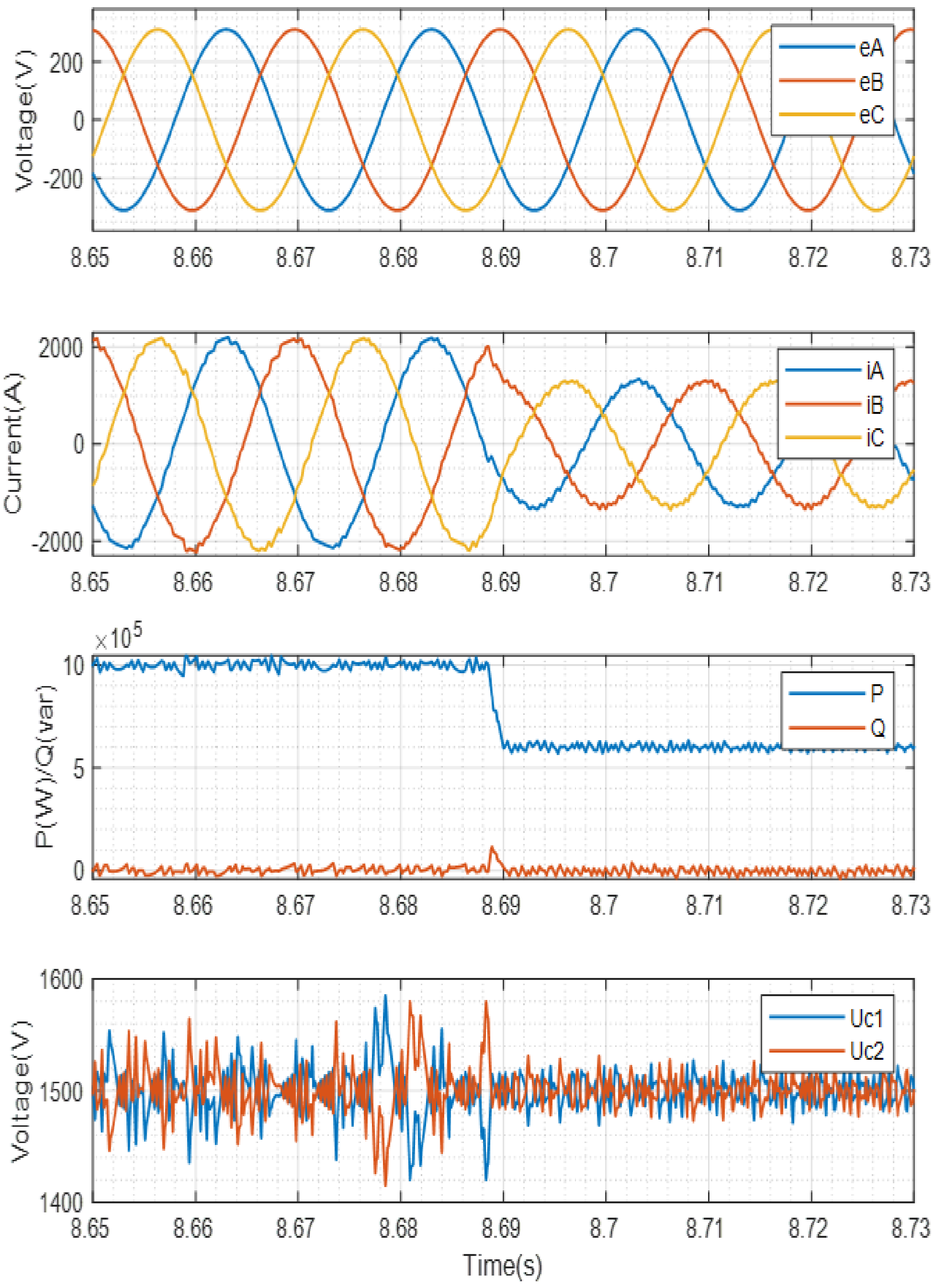

Figure 6.10: Experiment validation results for the MPC algorithm in [137] under dynamic operating conditions (600kW) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.4: Comparative Results of Chapter 3 for Different Control Algorithms under dynamic operation conditions in Case A (600kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.39%	5.28%	4.85%	3.40%
Switching Frequency(kHz)	4.219	4.747	4.929	5.115
RMS Values of Capacitor Voltage Error (V)	29.992	30.806	29.026	18.476

Table 6.5: Comparative Results of Chapter 3 for Different Control Algorithms in Case A (Parameter Sensitivity)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	2.09%	3.30%	3.41%	2.16%
Switching Frequency(kHz)	4.231	4.749	4.783	4.999
RMS Values of Capacitor Voltage Error (V)	63.120	60.642	61.870	51.104

6.3.3 Case A (Parameter Sensitivity)

In this section 6.3.3, the parameter (inductance) sensitivity of the proposed MPC algorithm in Chapter 3 was analysed and compared to the conventional MPC algorithm [82], the optimal MPC algorithms in [31] and the multistep MPC algorithm in [137]. The parameter sensitivity had -33.3% variations in the inductance from $1.5e-3\,H$ to $1e-3\,H$ during this experimental process. Comparative results are provided in Table 6.5. The waveforms relating to the experimental results are indicated in Figure 6.11, Figure 6.12, Figure 6.13 and Figure 6.14. From the above results, it can be seen that the proposed MPC algorithm can overcome misidentification of the inductances with variations in the parameter having no significant effect on the system.

The parameter sensitivity performances of the proposed MPC algorithm in Chapter 3 are shown in Figure 6.11. From the figures, the active power (P) is able to keep stability when the inductance had -33.3% variations from $1.5e-3\,H$ to $1e-3\,H$. At the same time, the reactive power (Q) was maintained at zero. The output grid voltages and grid currents were able to maintain a steady three-phase output. In Figure 6.11, it should be noted that the RMS value of the DC-link capacitor fluctuating voltage was $63.120V$, which was 2.10% of the total DC-link voltage.

Considering the comparative results in Table 6.5, the proposed MPC algorithm in Chapter achieved the lowest THD of the output currents, with THD values of 2.09% for the proposed MPC algorithm, 3.30% for the conventional MPC algorithm in [82], 3.41% for the optimal MPC algorithms in [31] and 2.16% for the multistep MPC algorithm in [137], respectively. The proposed MPC algorithm's switching frequency was still lower than the other three MPC algorithms. The switching frequency of the proposed MPC algorithm was reduced by more than 12% with the conventional MPC algorithm in [82] generating a frequency of $4.749\,kHz$, the optimal MPC algorithms in [31] generating a frequency of $4.783\,kHz$, the multistep MPC algorithm in [137] generating a frequency of $4.999\,kHz$, while the proposed MPC algorithm in Chapter 3 generated $4.231\,kHz$ under the same working conditions. Concerning the capacitor voltage error RMS values, the proposed MPC algorithm was $63.120\,V$, while the other three methods were $60.642\,V$ for the conventional MPC algorithm in [82], $61.870\,V$ for the optimal MPC algorithms in [31] and $51.104\,V$ for the multistep MPC algorithm in [137].

6.3.4 Case B (Nominal Operation)

In the following three sections, the 3-level NPC inverter system with the representative parameters of Case B is used for validating the proposed MPC algorithm of Chapter 3. Compared to Case A, the system's parameters are different, which is presented in Table 6.1. To test the effectiveness of the proposed MPC controller, three working conditions were considered: nominal operation, dynamic operation (where the active power reference was stepped down from $500\,kW$ to $400\,kW$; and changes in the parameter sensitivity (-20% variations in the inductance from $5e-4\,H$ to $4e-4\,H$). Throughout the various tests, the reactive power reference was set at zero to achieve a unity power factor.

The experimental results focused on the performance of the proposed MPC algorithm with the representative parameters of Case B under nominal operating conditions, as indicated in Figure 6.15. The active power of reference was $500\,kW$, and the reactive power of reference was $0\,VAR$ to ensure a unity power factor. In Figure 6.15, it can be seen that the active power, P, and the reactive power, Q, both tracked the reference powers. Meanwhile, e_A, e_B, and e_C represented the output grid phase voltages, whose peak values were $310V$. i_A, i_B, and i_C are the output grid currents. So, from the output waveform of Figure 6.15, it should be noted that the system's output currents and voltages were stable. U_{c1} and U_{c2} were the voltages of the DC-link capacitors. The RMS value of the DC-link capacitor fluctuating voltage was $67.775\,V$. This indicated that the proposed MPC algorithm in Chapter 3, with the representative parameters of Case B, maintained neutral point balancing with reasonable ripples. Therefore, the proposed MPC algorithm can achieve active and reactive power tracking, stable current and voltage output, and neutral point balancing under steady-state working conditions.

Comparative results, including the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC

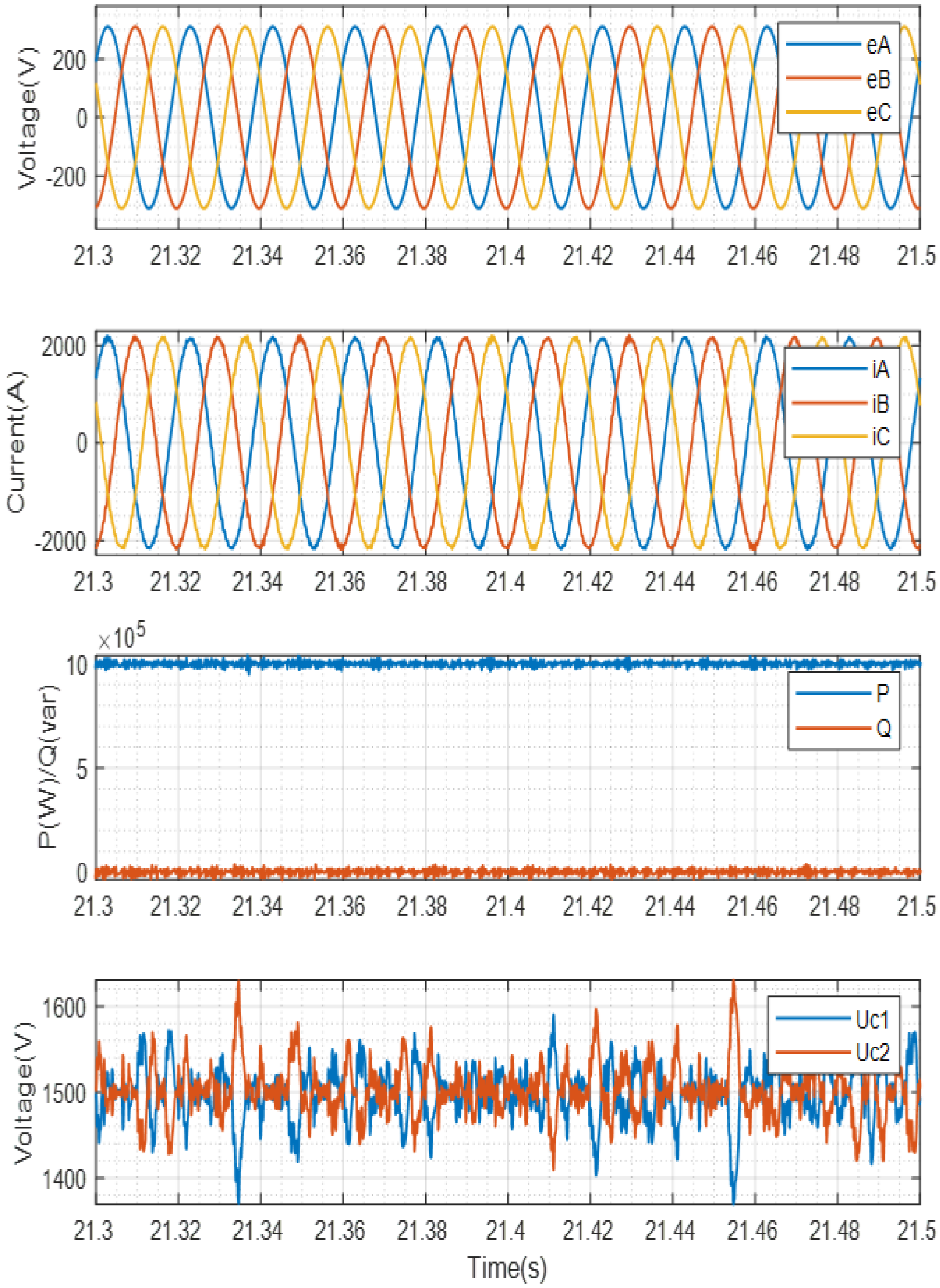

Figure 6.11: Experiment validation results for the proposed MPC algorithm of Chapter 3 under parameter sensitivity conditions in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

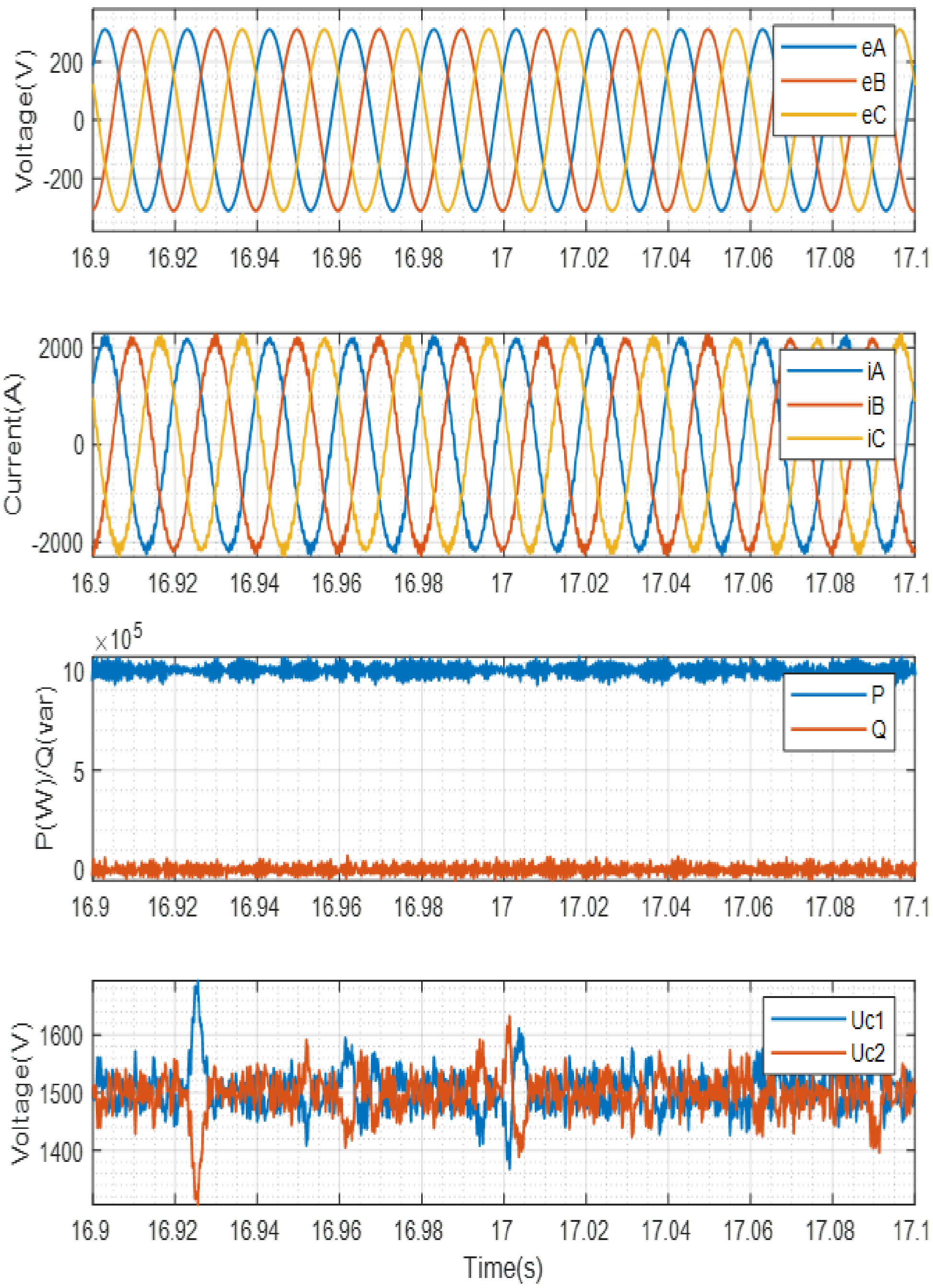

Figure 6.12: Experiment validation results for the MPC algorithm in [82] under parameter sensitivity conditions in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

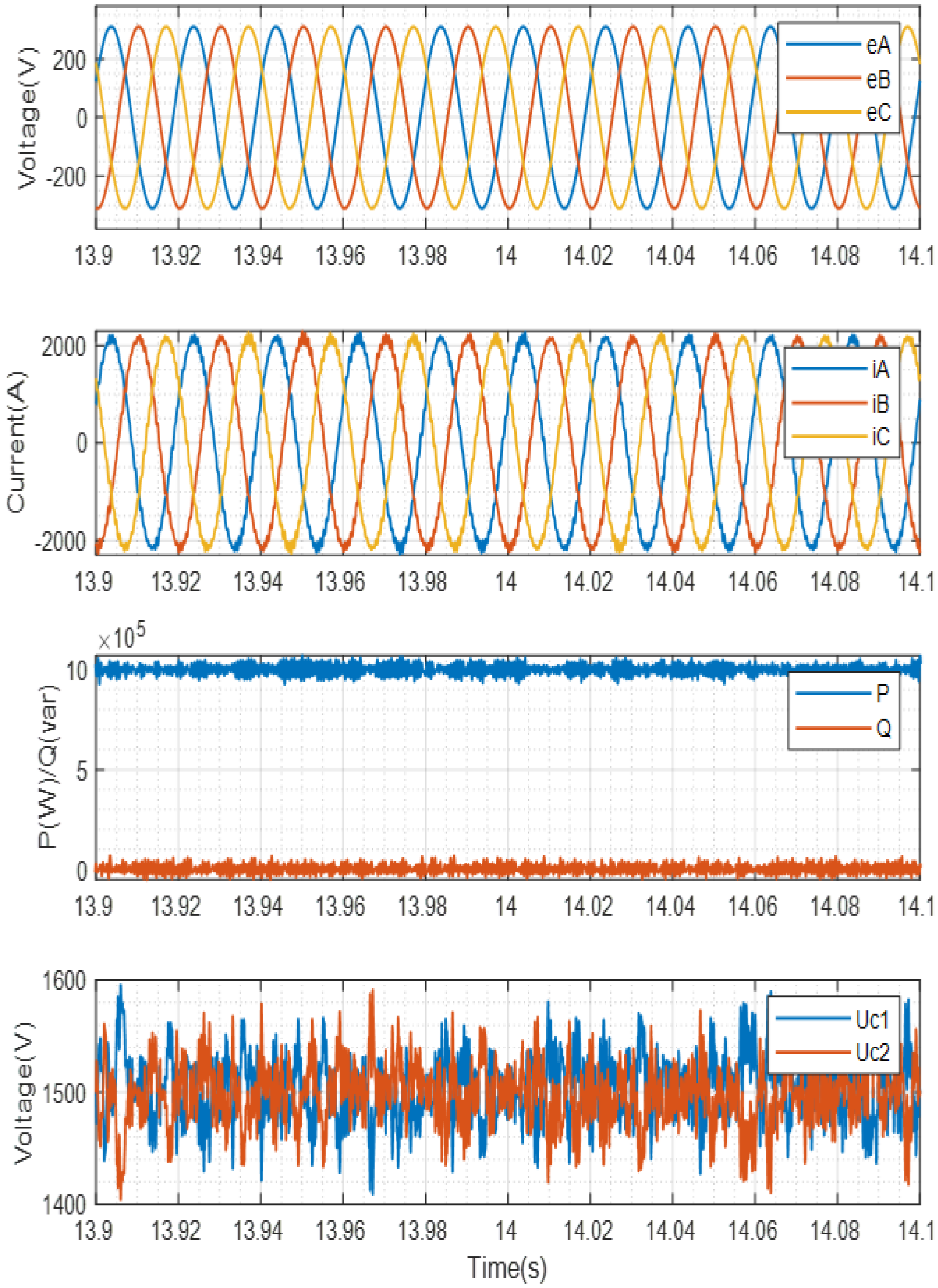

Figure 6.13: Experiment validation results for the MPC algorithm in [31] under parameter sensitivity conditions in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

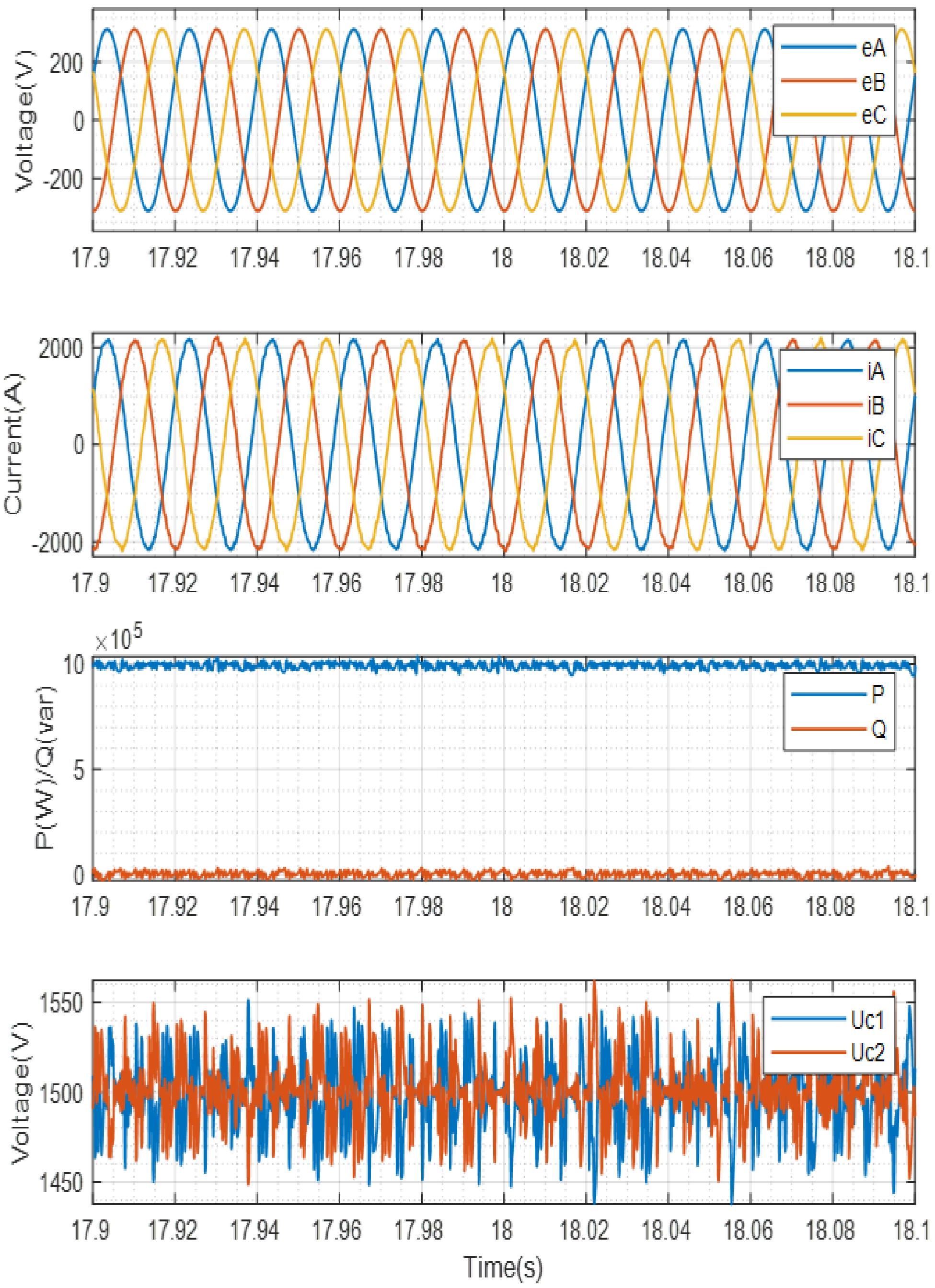

Figure 6.14: Experiment validation results for the MPC algorithm in [137] under parameter sensitivity conditions in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

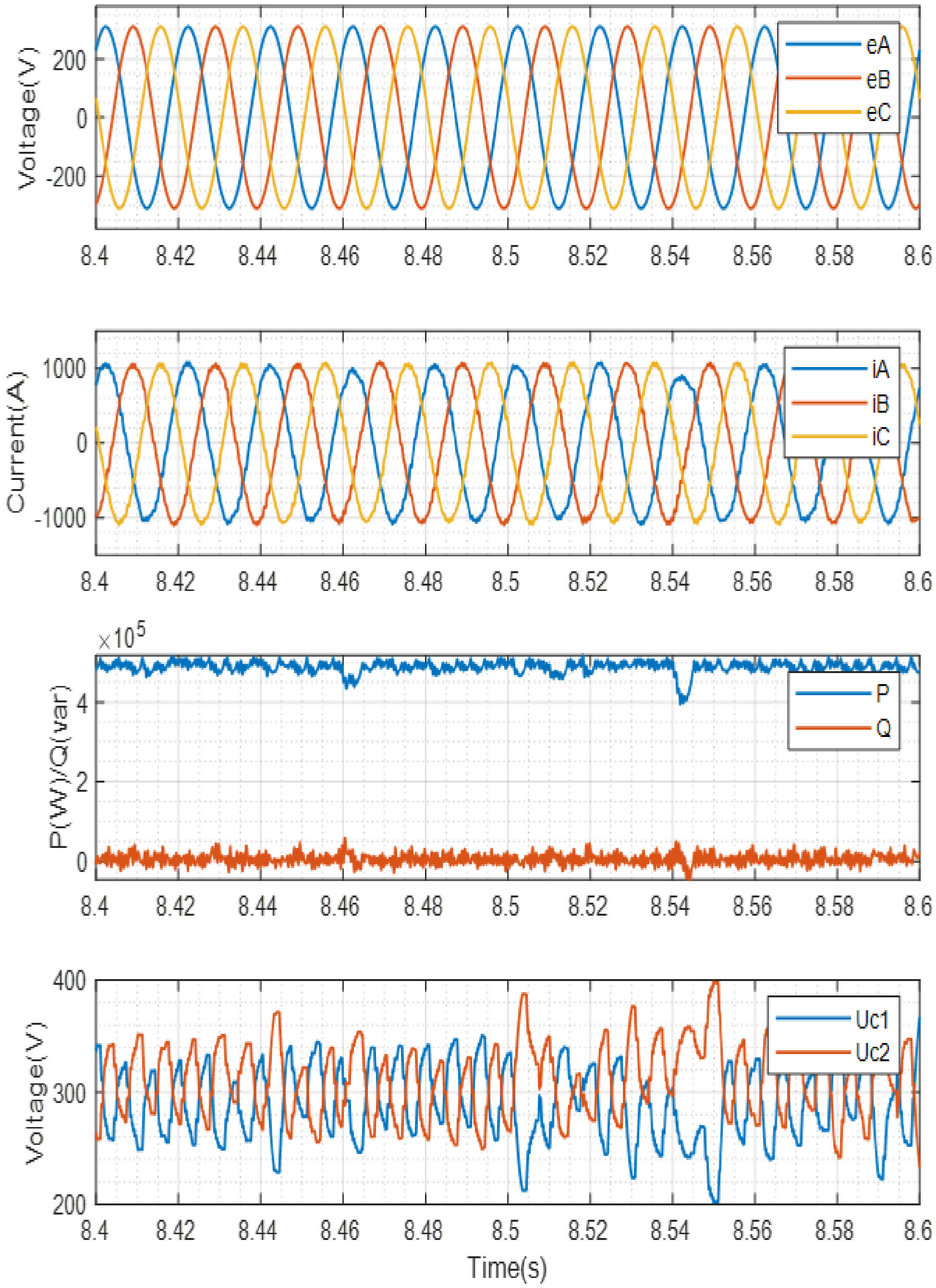

Figure 6.15: Experiment validation results for the proposed MPC algorithm in Chapter 3 under nominal operating conditions (500kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.6: Comparative Results of Chapter 3 for Different Control Algorithms under nominal operation conditions in Case B (500kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.62%	4.83%	3.44%	3.30%
Switching Frequency(kHz)	1.475	1.532	1.746	1.407
RMS Values of Capacitor Voltage Error (V)	67.775	65.865	69.866	87.725

algorithm in Chapter 3, are provided in Table 6.6. The waveforms relating to the experimental results are shown in Figure 6.16, Figure 6.17 and Figure 6.18. In terms of the results in Table 6.6, three aspects, including the THD value of the output current, switching frequency and the RMS value of the DC-link capacitor voltage error, would be analysed. The THD values of the output currents for the proposed MPC algorithms 3.62% were lower than the conventional MPC algorithms in [82] (4.83%) and the optimal MPC algorithm in [31] (3.44%), which were a bit higher than the multistep MPC algorithm in [137] (3.30%). The switching frequency of the proposed MPC algorithm ($1.475kHz$) in Chapter 3 was lower than $1.532kHz$ in the conventional MPC algorithms in [82] and $1.746kHz$ in the optimal MPC algorithm in [31]. The switching frequency of the proposed MPC algorithm was just $0.068kHz$ behind $1.407kHz$ the multistep MPC algorithm in [137]. The RMS value of the capacitor voltage error ($67.775V$) for the proposed MPC algorithm was smaller than the multistep MPC algorithm in [137] ($87.725V$) and the optimal MPC algorithm in [31] ($59.417V$), but it larger than the conventional MPC algorithms in [82] ($69.866V$).

6.3.5 Case B (Dynamic Operation)

In this section, the proposed MPC algorithm's robustness was assessed. The active power of reference went down from $500\,kW$ to $400\,kW$. The proposed MPC algorithm was able to achieve active power tracking and reduce the switching frequency under these dynamic working conditions.

The transient-state performances of the proposed MPC algorithm in Chapter 3 are shown in Figure 6.19. In the figures, the active power (P) could rapidly track the step-change (the active power of reference decreasing from $500\,kW$ to $400\,kW$). Meanwhile, the reactive power (Q) was maintained at zero across the duration. The output grid voltage was able to maintain a steady three-phase output. Simultaneously, the output currents could quickly respond to the step-change across the whole transition period without overshooting. In Figure 6.19, it can be seen that the RMS value of the DC-link capacitor fluctuating voltage was $46.443V$.

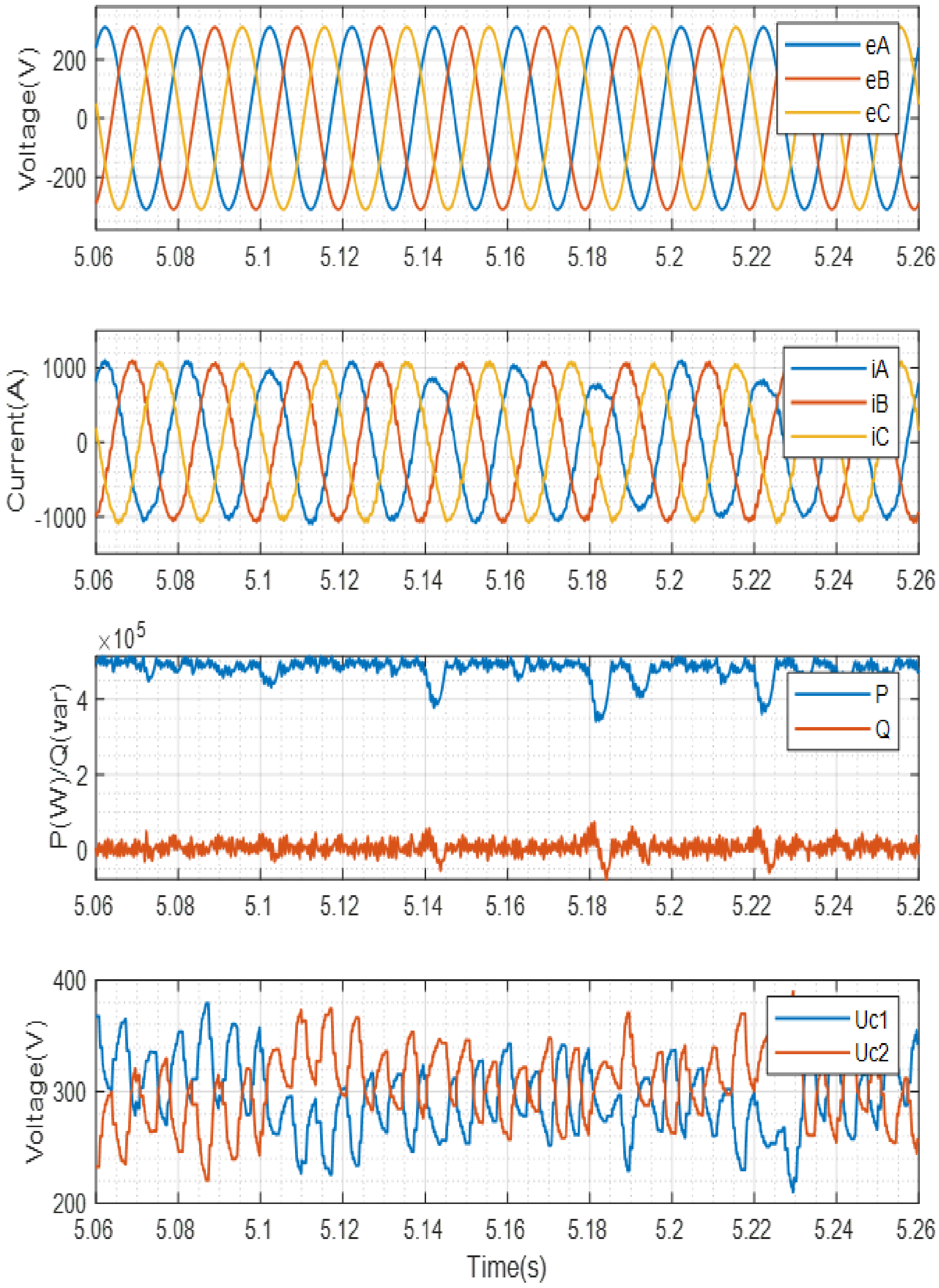

Figure 6.16: Experiment validation results for the MPC algorithm in [82] under nominal operating conditions (500kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

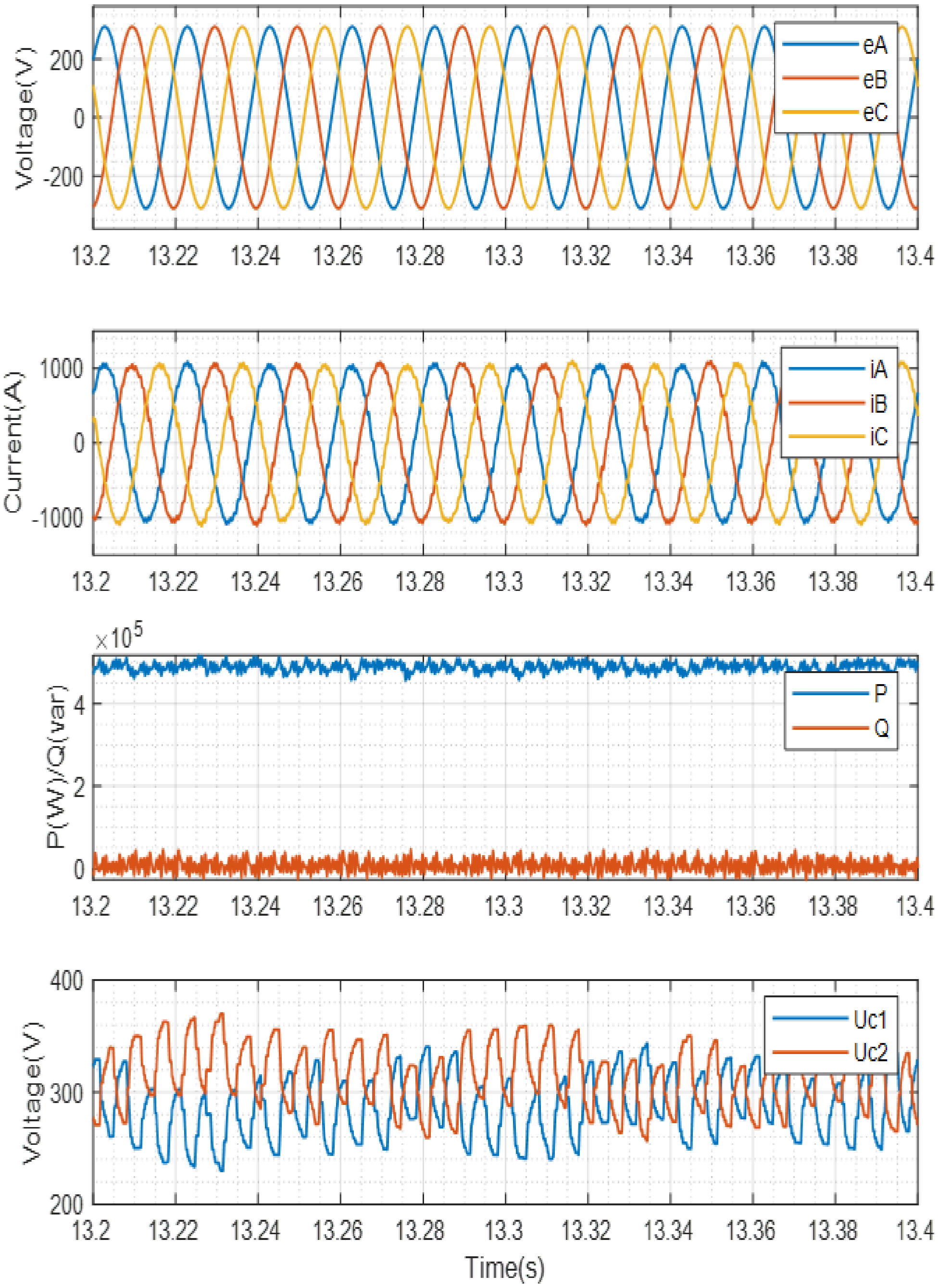

Figure 6.17: Experiment validation results for the MPC algorithm in [31] under nominal operating conditions (500kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

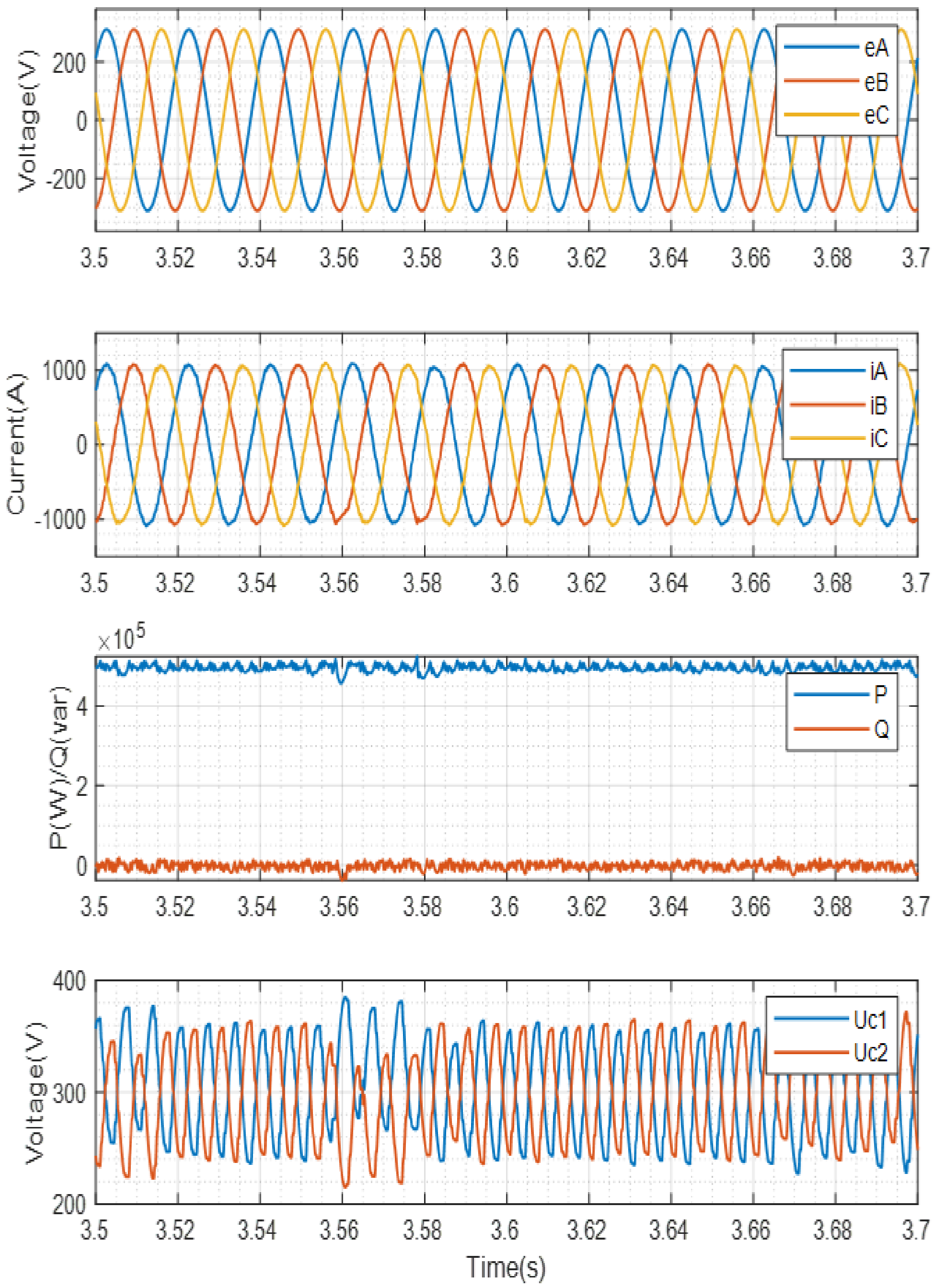

Figure 6.18: Experiment validation results for the MPC algorithm in [137] under nominal operating conditions (500kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

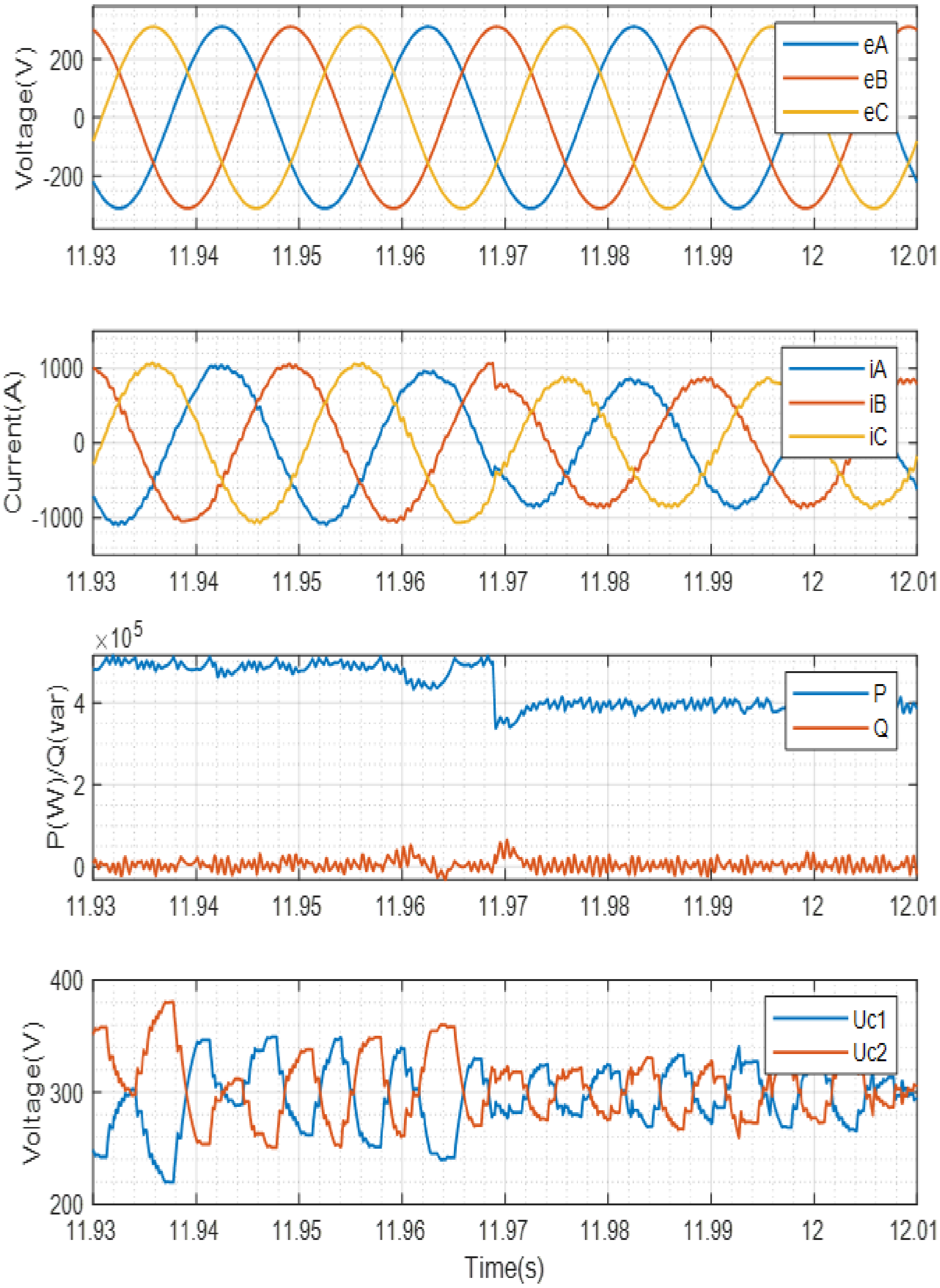

Figure 6.19: Experiment validation results for the proposed MPC algorithm in Chapter 3 under dynamic operating conditions (400kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.7: Comparative Results of Chapter 3 for Different Control Algorithms under dynamic operation conditions in Case B (400kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.99%	4.75%	3.70%	3.22%
Switching Frequency(kHz)	1.612	1.694	1.751	1.432
RMS Values of Capacitor Voltage Error (V)	46.443	46.365	48.898	60.728

Comparative results, for the proposed MPC algorithm in Chapter 3, the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], and the multistep MPC algorithm in [137], are provided in Table 6.7 under dynamic operating conditions (the active power of reference decreasing from 500 kW to 400 kW). The waveforms relating to the comparative results are shown in Figure 6.20, Figure 6.21 and Figure 6.22, which are the waveforms of the conventional MPC algorithm in [82], the optimal MPC algorithms in [31] and the multistep MPC algorithm in [137]. The total harmonic distortion (THD) of the grid currents was 3.99% in the proposed MPC algorithm, 4.75% in [82], 3.70% in [31] and 3.22% in [137] respectively, as described in Figure 6.7. In terms of switching frequency, the proposed MPC algorithm obtained ($1.612kHz$), which was lower than the conventional MPC algorithms in [82] $1.694kHz$ and the optimal MPC algorithm in [31] $1.751kHz$. When it came to the RMS value of the capacitor voltage error, the multistep MPC algorithm in [137] ($60.728V$) had the biggest value, while the conventional MPC algorithm in [82] had the lowest value ($46.365V$). The proposed MPC algorithm ($46.443V$) achieved the approximate value with the conventional MPC algorithm [82].

6.3.6 Case B (Parameter Sensitivity)

In this section, the parameter (inductance) sensitivity of the proposed MPC algorithm in Chapter 3 with the representative parameters of Case B was analysed and compared to the conventional MPC algorithm [82], the optimal MPC algorithms in [31] and the multistep MPC algorithm in [137]. The parameter sensitivity had -20% variations in the inductance from $5e-4\,H$ to $4e-4\,H$ during this experimental process. The waveforms relating to the experimental results are demonstrated in Figure 6.23, Figure 6.24, Figure 6.25 and Figure 6.26. Comparative results are provided in Table 6.8. Through the above results, it can be seen that the proposed MPC algorithm can overcome misidentification of the inductances with variations in the parameter. The parameter sensitivity had no significant effect on the system.

The performances of the proposed MPC algorithm in Chapter 3 are indicated in Figure 6.23 under parameter sensitivity conditions. Considering the figures, the active

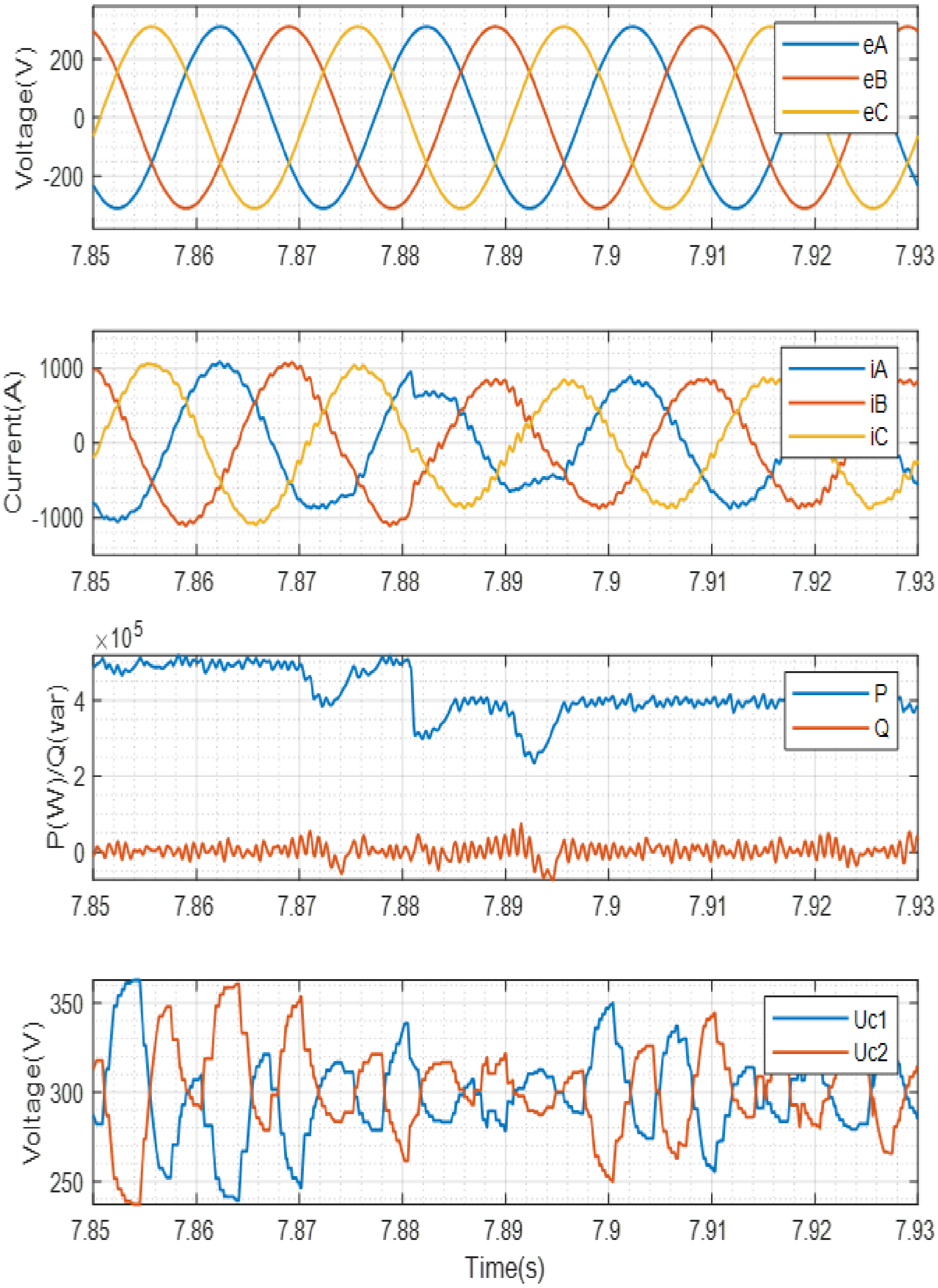

Figure 6.20: Experiment validation results for the MPC algorithm in [82] under dynamic operating conditions (400kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

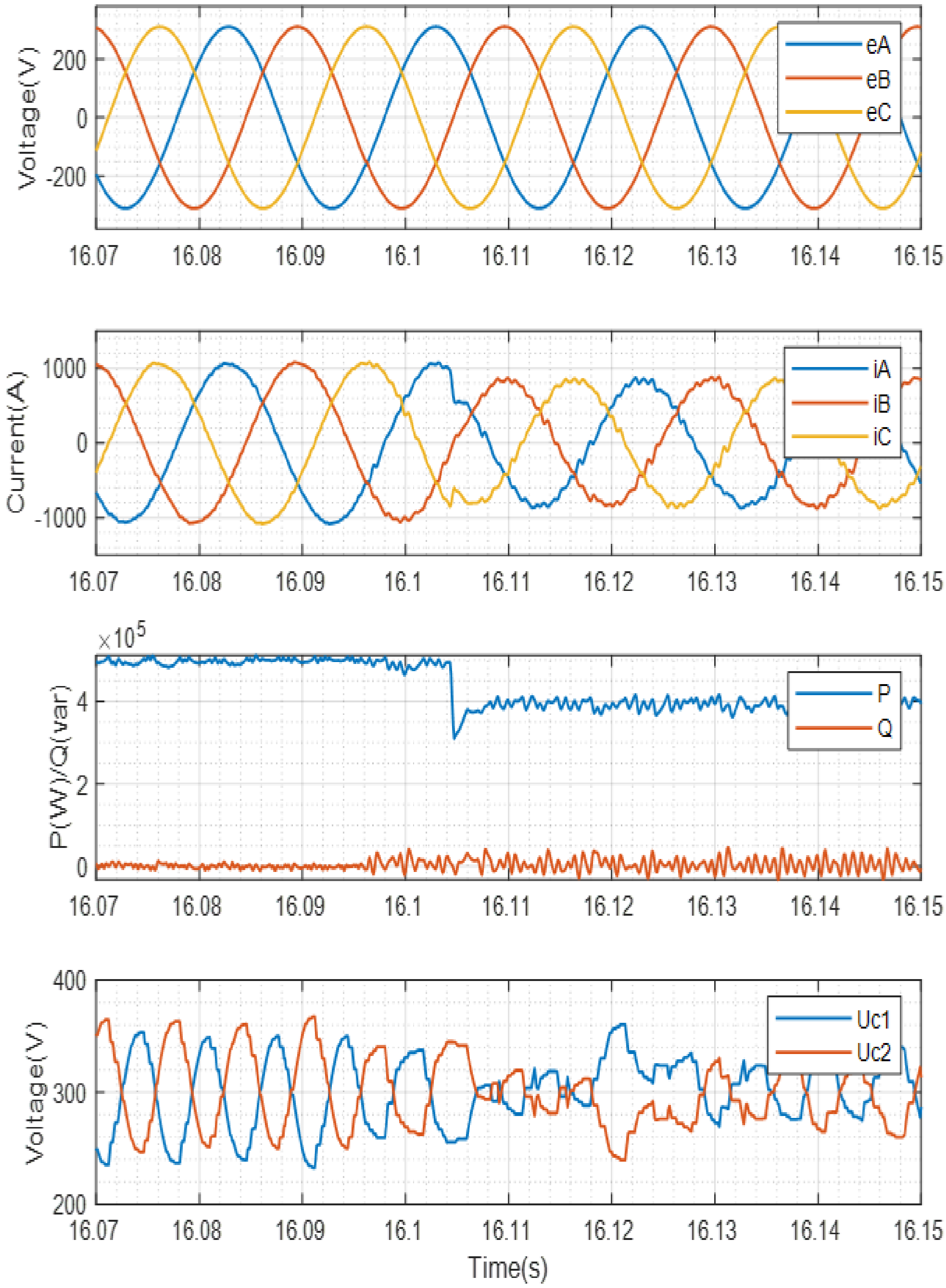

Figure 6.21: Experiment validation results for the MPC algorithm in [31] under dynamic operating conditions (400kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

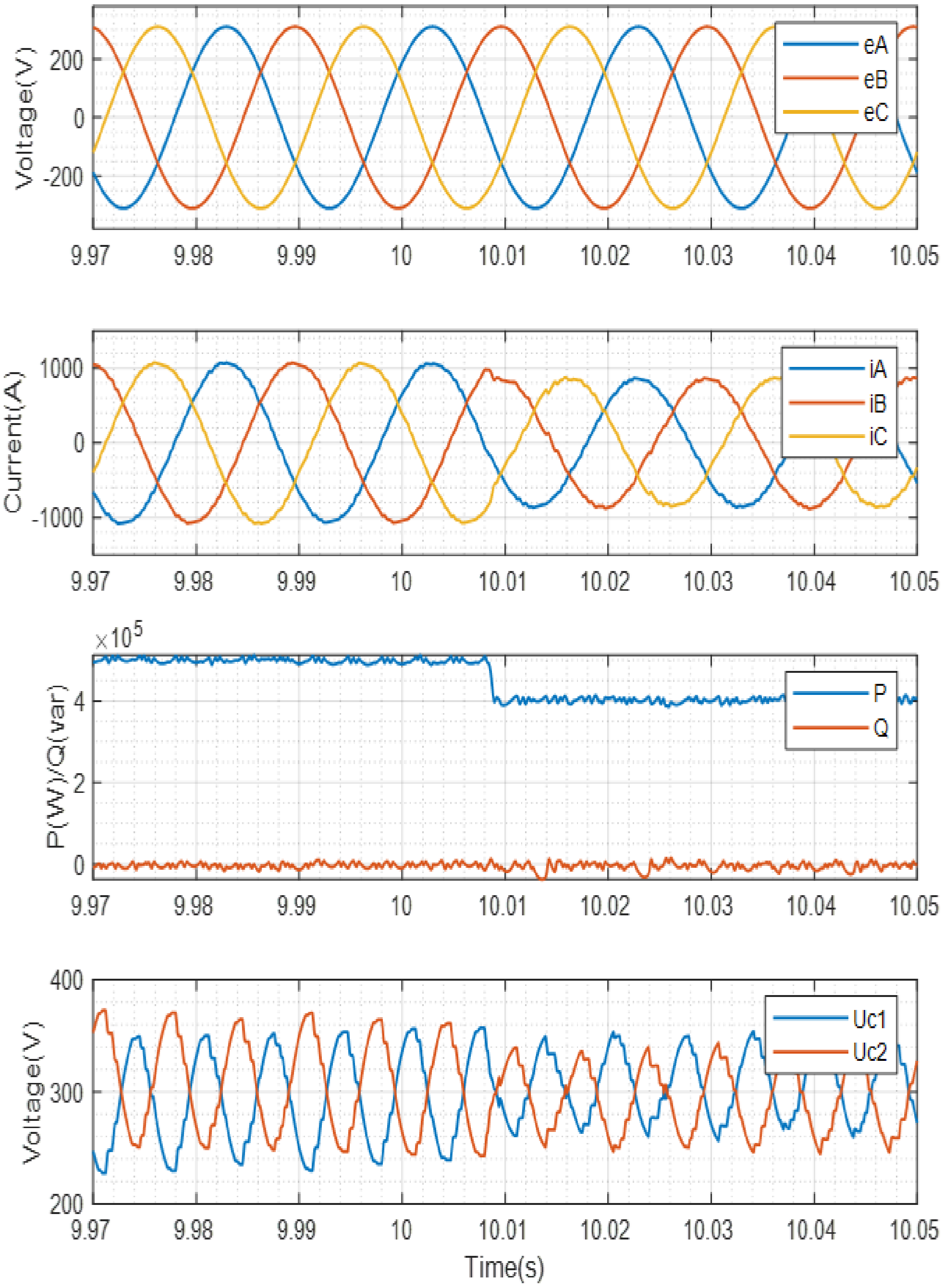

Figure 6.22: Experiment validation results for the MPC algorithm in [137] under dynamic operating conditions (400kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

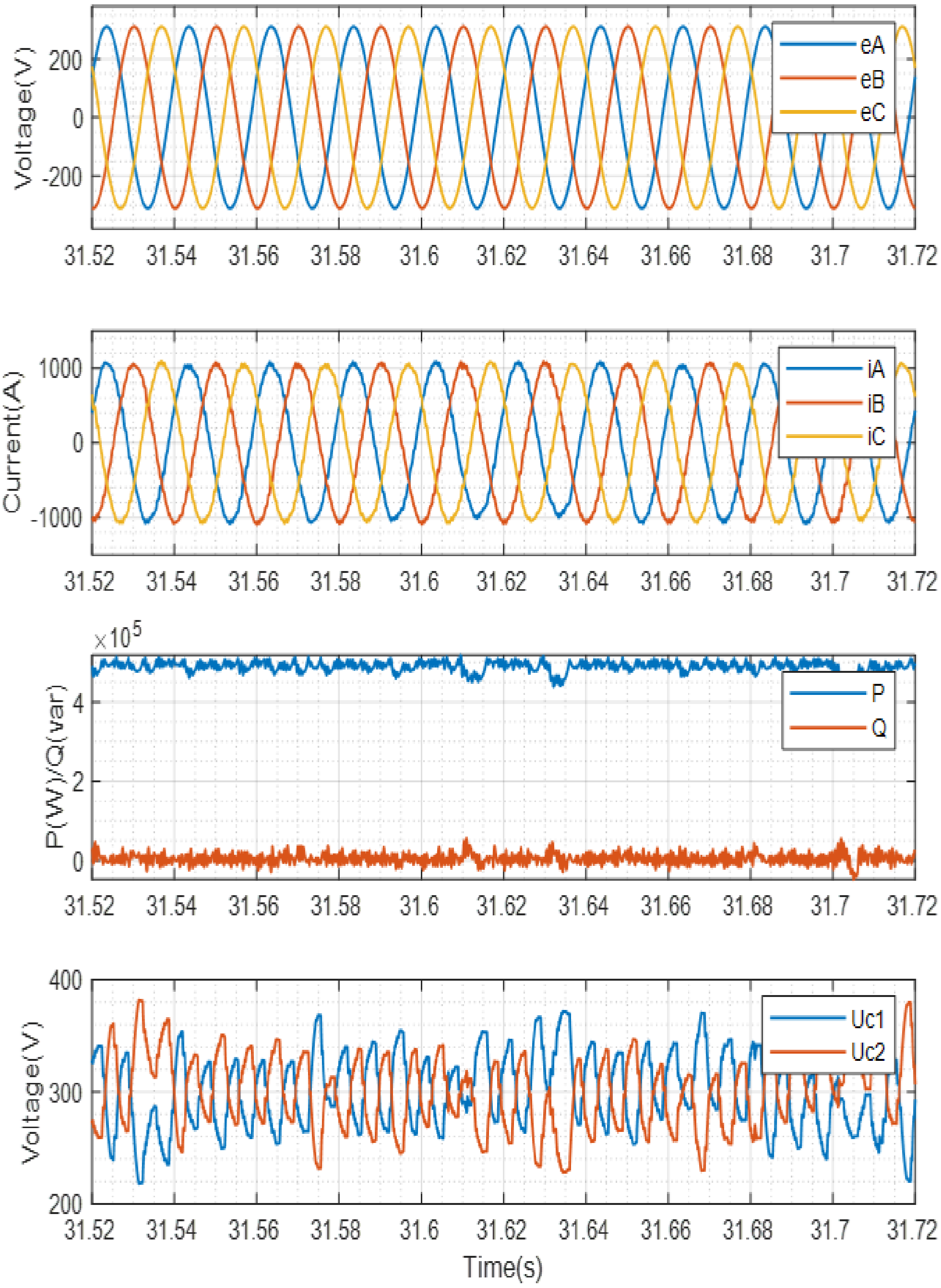

Figure 6.23: Experiment validation results for the MPC algorithm in Chapter 3 under parameter sensitivity conditions in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

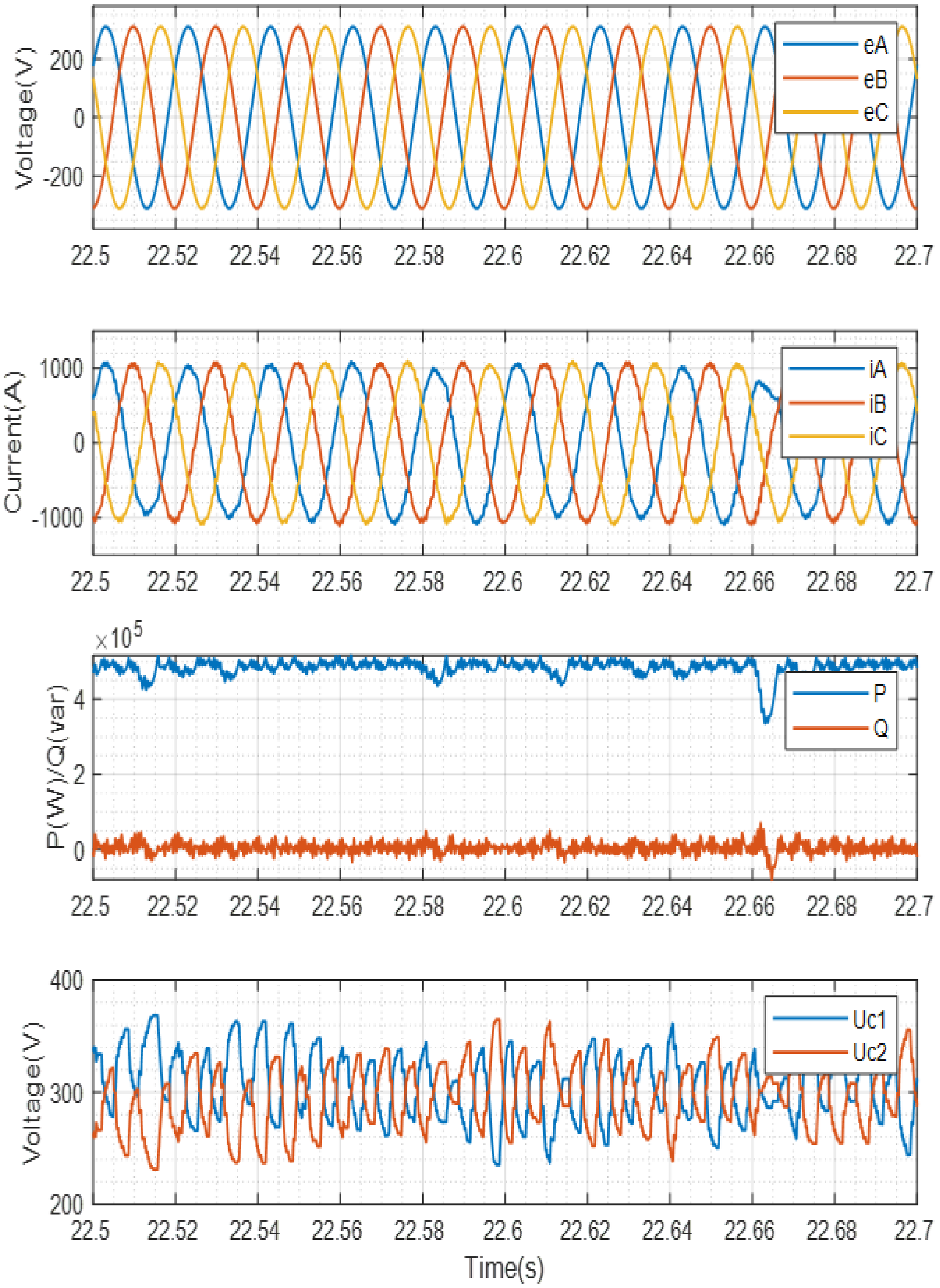

Figure 6.24: Experiment validation results for the MPC algorithm in [82] under parameter sensitivity conditions in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

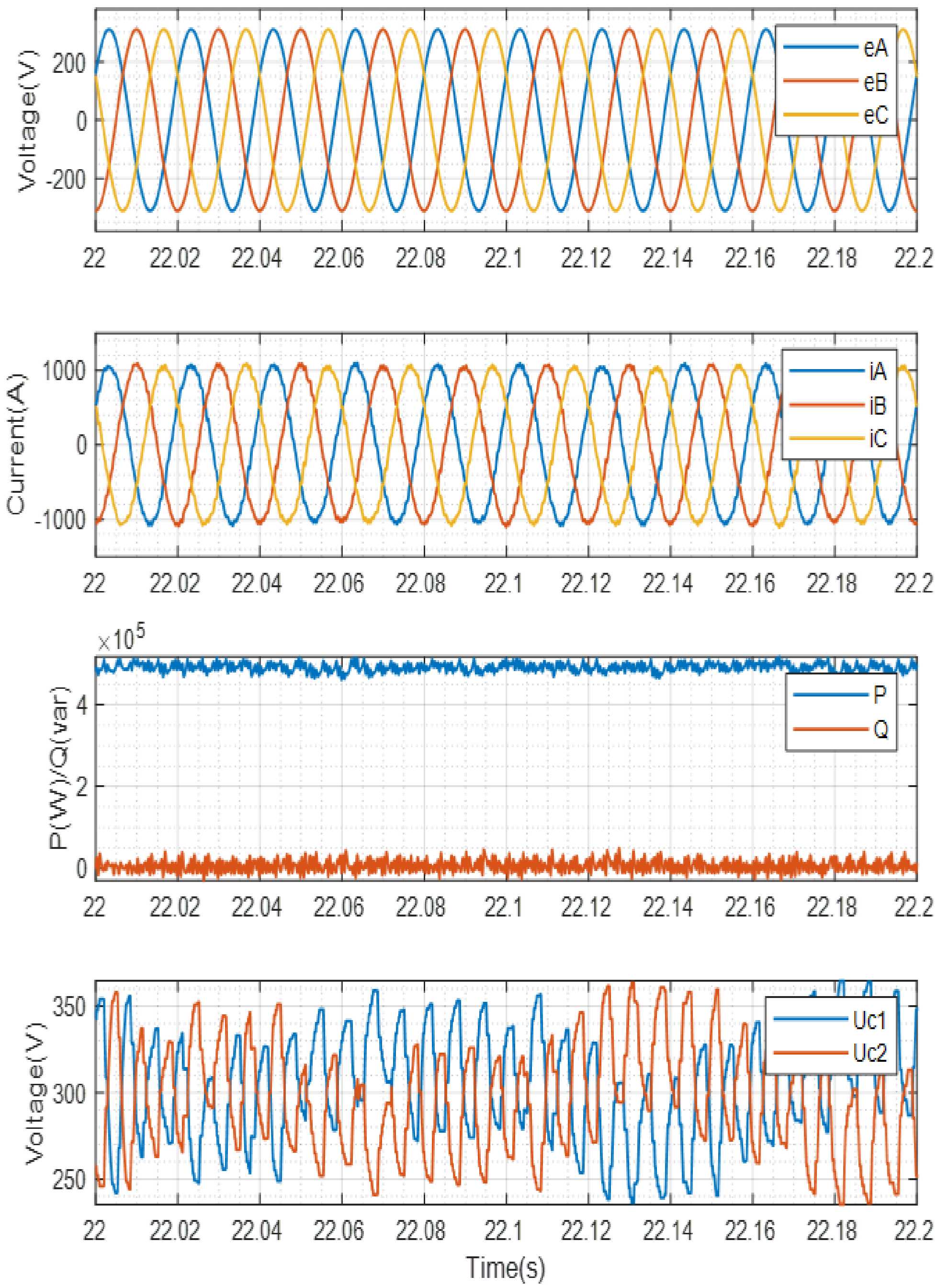

Figure 6.25: Experiment validation results for the MPC algorithm in [31] under parameter sensitivity conditions in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

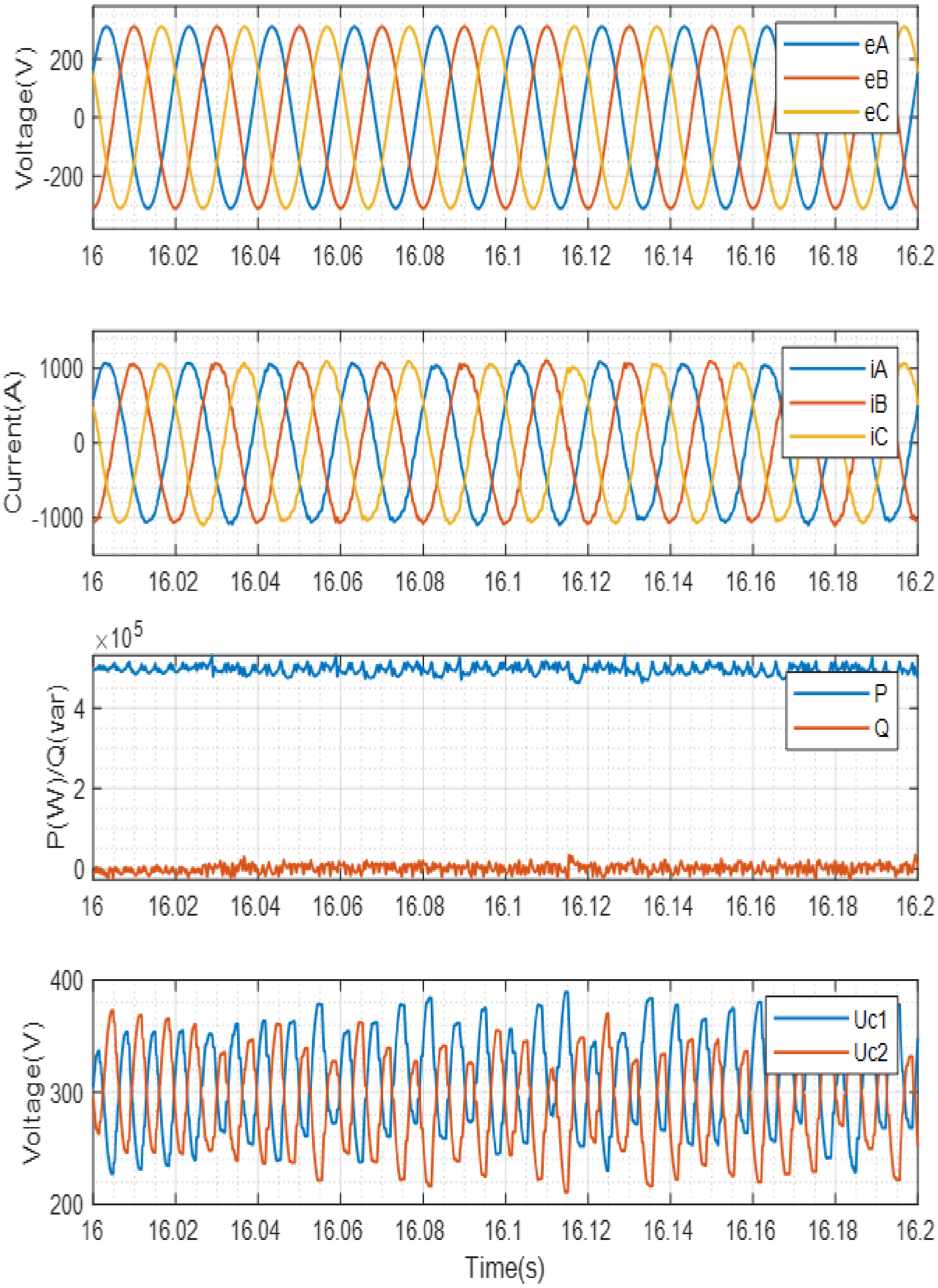

Figure 6.26: Experiment validation results for the MPC algorithm in [137] under parameter sensitivity conditions in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.8: Comparative Results of Chapter 3 for Different Control Algorithms in Case B (Parameter Sensitivity)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.84%	4.19%	3.95%	2.69%
Switching Frequency(kHz)	1.663	1.675	1.676	1.500
RMS Values of Capacitor Voltage Error (V)	64.403	57.224	64.903	77.289

power (P) can keep stability when the inductance had -20% variations from $5e-4\,H$ to $4e-4\,H$. Meanwhile, the reactive power (Q) is maintained at zero. Both the output grid voltages and grid currents were able to maintain a steady three-phase output in parameter sensitivity conditions. In Figure 6.23, the RMS value of the DC-link capacitor fluctuating voltage was $64.430V$.

Relating to the comparative results in Table 6.8, the proposed MPC algorithm in Chapter 3 under parameter sensitivity conditions achieved the THD values of 3.84%, which was lower than 4.19% for the conventional MPC algorithm in [82] and 3.95% for the optimal MPC algorithms in [31]. The multistep MPC algorithm in [137] had a 2.69% THD value of the output currents. As for the switching frequency, the proposed MPC algorithm's switching frequency ($1.663\,kHz$) was still lower than the conventional MPC algorithm ($1.675\,kHz$) in [82] and the optimal MPC algorithms ($1.676\,kHz$) in [31]. The multistep MPC algorithm in [137] generated a frequency of $1.500\,kHz$. In terms of the capacitor voltage error, the proposed MPC algorithm and the optimal MPC algorithm in [31] achieved more or less the same values. They were $64.403\,V$ and $64.903\,V$, respectively. The conventional MPC algorithm in [82] obtained the smallest RMS value $57.224\,V$, while the multistep MPC algorithm in [137] achieved the biggest RMS value $77.289\,V$.

6.4 Experimental Results for the Proposed Control Algorithms in Chapter 4

The effectiveness of the proposed MPC algorithm in Chapter 4 was examined in this section. A set of two different plants with representative parameters (Case A and Case B) has been used to validate the performance of the proposed MPC algorithms in Chapter 4, which were described in section 6.2. The parameters and value of the setup for Case A and Case B are described in Table 6.1 and Table 6.2. To validate the effectiveness of the proposed MPC algorithm in Chapter 4, three working conditions, including nominal operation, dynamic operation (where the active power reference stepping down from $1\,MW$ to $600\,kW$ in Case A, and the active power reference decreasing from $500\,kW$ to

400 kW in Case B); and changes in the parameter sensitivity (-33.3% variations in the inductance from $1.5e-3\,H$ to $1e-3\,H$ in Case A, and -20% variations in the inductance from $5e-4\,H$ to $4e-4\,H$ in Case B), were considered in this section 6.4. The reactive power reference was set at zero to achieve a unity power factor during the various tests.

6.4.1 Case A (Nominal Operation)

The first results of Case A were focused upon the performance of the proposed MPC algorithm in Chapter 4 under nominal operating conditions in Figure 6.27. The active power of reference was 1 MW, and the reactive power of reference was 0 VAR, so as to ensure a unity power factor. In Figure 6.27, it can be noted that the active power and the reactive power can both track the reference powers. Then, it can be concluded that the system's output currents and voltages were stable. In this figure, U_{c1} and U_{c2} represent the voltages of the DC-link capacitors. The RMS value of the DC-link capacitor fluctuating voltage was 64.711 V. This indicates that the proposed MPC algorithm maintained neutral point balancing with reasonable ripples. Therefore, under steady-state working conditions, the proposed MPC algorithm can achieve active and reactive power tracking, stable current and voltage output, and neutral point balancing.

Comparative results, including the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC algorithm in Chapter 4, are provided in Table 6.9. The output waveforms of the experimental results are indicated in Figure 6.27, Figure 6.4, Figure 6.5 and Figure 6.6, which represent experimental results of the proposed MPC algorithm in Chapter 4, the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], and the multistep MPC algorithm in [137]. Based on Table 6.9, the experimental results are analysed from the THD value of the output current, switching frequency and the RMS value of the DC-link capacitor voltage error. Firstly, the THD values of the output currents (the proposed MPC algorithm in Chapter 4) 2.85% are lower than the conventional MPC algorithms in [82] (3.88%) and the optimal MPC algorithm in [31] (4.08%), which are a bit higher than the multistep MPC algorithm in [137] (2.29%). The THD value of the proposed MPC algorithm in Chapter 4 achieved a similar value with the multistep MPC algorithm in [137]. Then, the switching frequency of the proposed MPC algorithm (3.052kHz) in Chapter 4 is the lowest among these four methods. The switching frequency of the other three methods are 4.680kHz the conventional MPC algorithms in [82], 4.645kHz the optimal MPC algorithm in [31] and 4.528kHz the multistep MPC algorithm in [137]. The proposed MPC algorithm reduced 34.8% switching frequency, comparing to the switching frequency of the conventional MPC algorithm in [82]. The proposed MPC algorithm for grid-connected NPC inverters based on the automatic selection of weighting factors effectively decreases the switching frequency and limits the switching loss. At last, the RMS value of the capacitor voltage error (64.711V) for

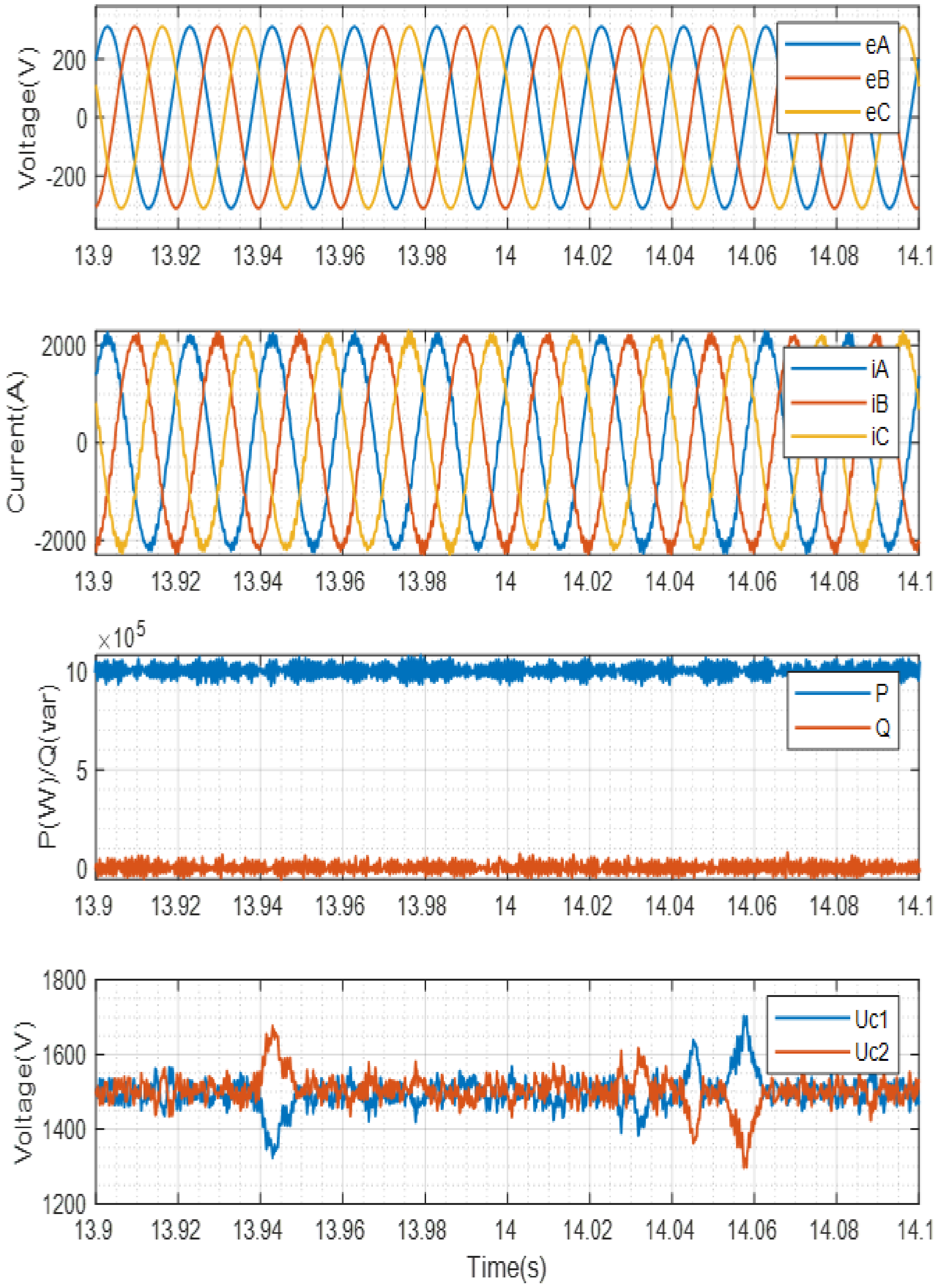

Figure 6.27: Experiment validation results for the proposed MPC algorithm in Chapter 4 under nominal operating conditions (1MV) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.9: Comparative Results of Chapter 4 for Different Control Algorithms under nominal operation conditions in Case A (1MW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	2.85%	3.88%	4.08%	2.29%
Switching Frequency(kHz)	3.052	4.680	4.645	4.528
RMS Values of Capacitor Voltage Error (V)	64.711	56.385	59.417	54.403

the proposed MPC algorithm is a bit bigger than the conventional MPC algorithm in [82] (56.385V), the optimal MPC algorithms in [31] (59.417V) and the multistep MPC algorithm in [137] (54.403V).

6.4.2 Case A (Dynamic Operation)

The robustness of the proposed MPC algorithm in Chapter 4 with with the representative parameters of Case A was also assessed in this section 6.4.2. In these dynamic working conditions, the active power of reference went down from 1 MW to 600 kW. The experimental results show that the proposed MPC algorithm was able to achieve active power tracking and reduce the switching frequency.

The performances of the proposed MPC algorithm in Chapter 4 are shown in Figure 6.28. From the figures, the proposed MPC algorithm can implement the active power (P) rapidly track to the step-change. In the meantime, the reactive power (Q) is maintained at zero across the duration. The output grid voltage could maintain a steady three-phase output. During the dynamic operation, the output currents quickly responded to the step-change without overshooting. The RMS value of the DC-link capacitor fluctuating voltage was 36.737V, which was 1.23% of the total DC-link voltage.

Comparative results are summarised in Table 6.10. The waveforms relating to the experimental results for the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC algorithm in Chapter 3 are provided in Figure 6.8, Figure 6.9 and Figure 6.10 and Figure 6.28, respectively, under dynamic operating conditions (the active power of reference decreasing from 1 MW to 600 kW). The proposed MPC algorithm in Chapter 4 achieved the lowest THD value of the output currents 2.76%. Other three methods are 5.28% in [82], 4.85% in [31] and 3.40% in [137] respectively. As for the switching frequency, the proposed MPC algorithm also obtained the lowest value (3.355kHz), while 4.747kHz the conventional MPC algorithms in [82], 4.929kHz the optimal MPC algorithm in [31] and 4.528kHz the multistep MPC algorithm in [137]. The proper weighting factors were

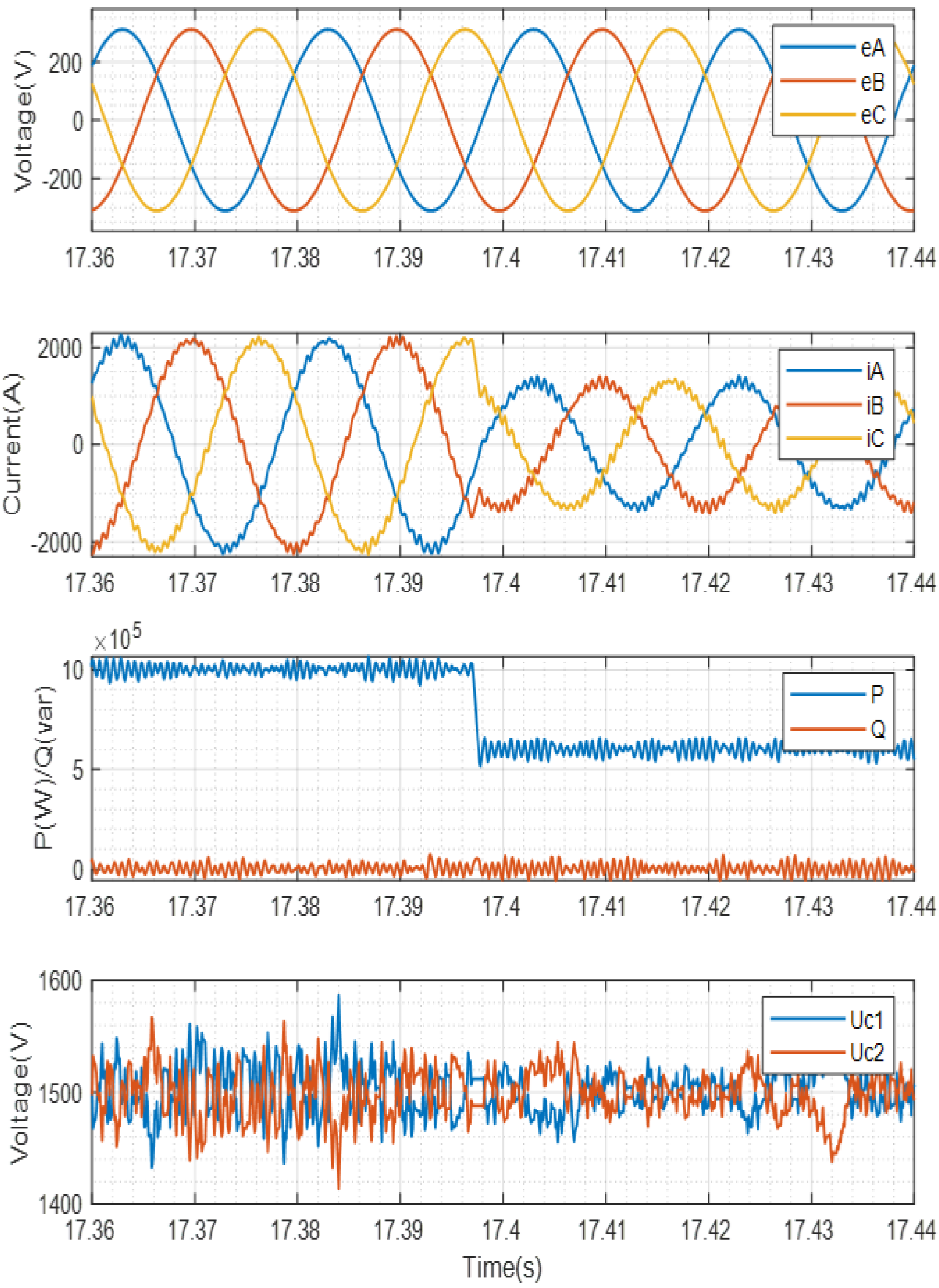

Figure 6.28: Experiment validation results for the proposed MPC algorithm in Chapter 4 under dynamic operating conditions (600kW) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.10: Comparative Results of Chapter 4 for Different Control Algorithms under dynamic operation conditions in Case A (600kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	2.76%	5.28%	4.85%	3.40%
Switching Frequency(kHz)	3.355	4.747	4.929	5.115
RMS Values of Capacitor Voltage Error (V)	36.737	30.806	29.026	18.476

Table 6.11: Comparative Results of Chapter 4 for Different Control Algorithms in Case A (Parameter Sensitivity)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.31%	3.30%	3.41%	2.16%
Switching Frequency(kHz)	3.486	4.749	4.783	4.999
RMS Values of Capacitor Voltage Error (V)	70.454	60.642	61.870	51.104

computed online across various working circumstances, the proposed MPC algorithm was able to accomplish switching frequency reductions. In terms of the RMS value of the capacitor voltage error, the multistep MPC algorithm in [137] got the smallest value $18.476V$. The proposed MPC algorithm achieved $36.737V$, while the conventional MPC algorithm in [82] and the optimal MPC algorithms in [31] were $30.806V$ and $29.026V$, respectively.

6.4.3 Case A (Parameter Sensitivity)

The parameter (inductance) sensitivity of the proposed MPC algorithm in Chapter 4 was described and analysed in this section. The parameter sensitivity had -33.3% variations in the inductance from $1.5e-3\,H$ to $1e-3\,H$ during this experimental process. The waveforms of the experimental results are indicated in Figure 6.29, Figure 6.12, Figure 6.13 and Figure 6.14, which are the proposed MPC algorithm in Chapter 4, the conventional MPC algorithm [82], the optimal MPC algorithms in [31] and the multistep MPC algorithm in [137], respectively. The comparative results are summarised and provided in Table 6.11. From these results, it can be concluded that the proposed MPC algorithm can overcome the inductances misidentification and have no substantial influence on the system.

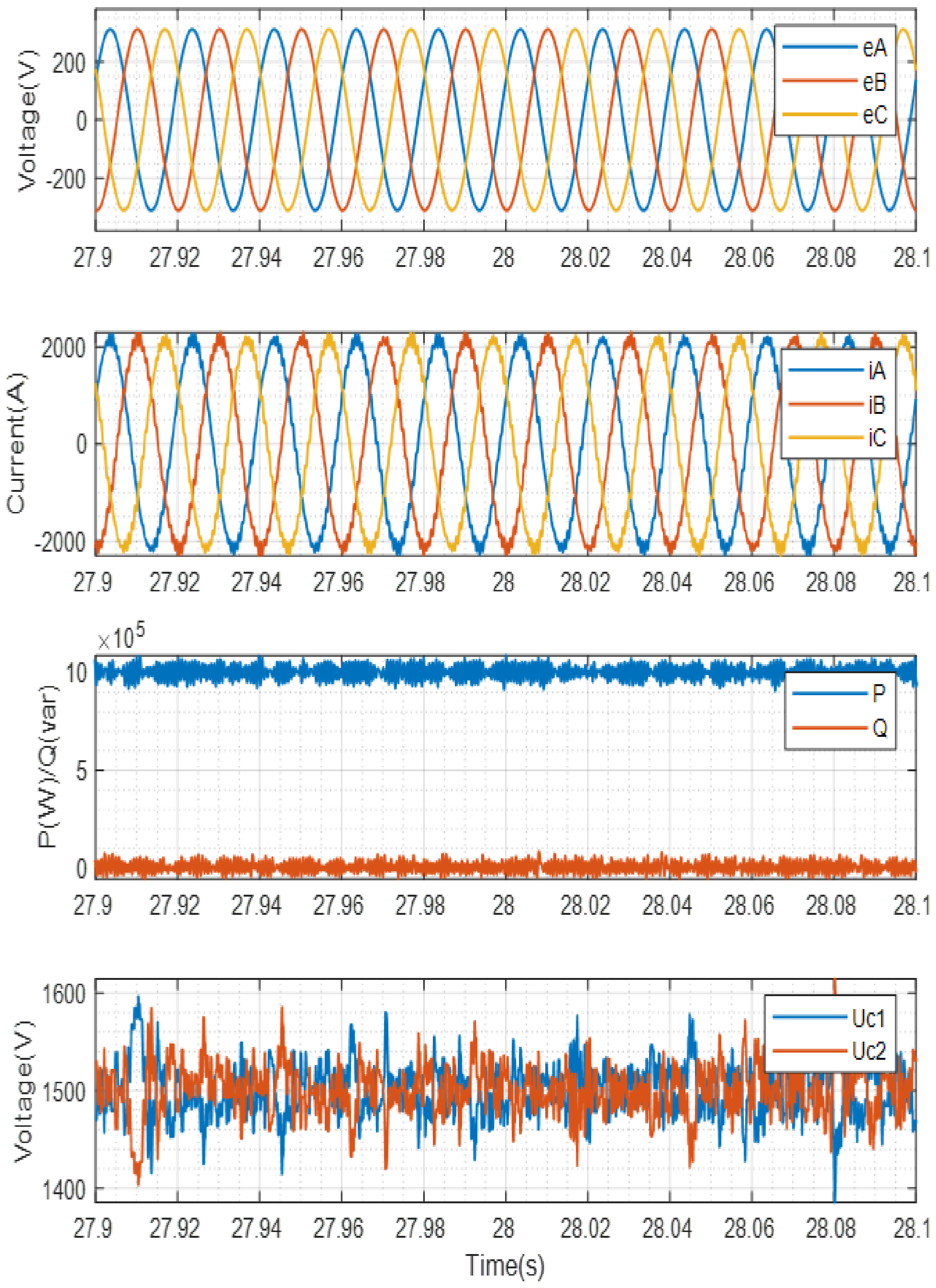

Figure 6.29: Experiment validation results for the proposed MPC algorithm in Chapter 4 under parameter sensitivity conditions in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Considering the comparative outcomes in Table 6.11, the proposed MPC algorithm in Chapter 4 achieved almost the same THD values of the output currents as the the conventional MPC algorithm [82]. They were 3.31% for the proposed MPC algorithm and 3.30% for the conventional MPC algorithm [82]. The multistep MPC algorithm in [137] obtained the lowest THD values 2.16%, while the optimal MPC algorithms in [31] had the highest THD values 3.41%. As for the switching frequency, the proposed MPC algorithm's switching frequency was the lowest among the four MPC algorithms, which was $3.486\,kHz$. The other three methods generated $4.749\,kHz$ the conventional MPC algorithm in [82], $4.783\,kHz$ the optimal MPC algorithms in [31], $4.999\,kHz$ the multistep MPC algorithm in [137]. In terms of the capacitor voltage error, the proposed MPC algorithm was $70.454\,V$. In comparison, other three methods were $60.642\,V$ for the conventional MPC algorithm in [82], $61.870\,V$ for the optimal MPC algorithms in [31] and $51.104\,V$ for the multistep MPC algorithm in [137].

6.4.4 Case B (Nominal Operation)

The proposed MPC algorithm of Chapter 4 was validated using the 3-level NPC inverter system with the representative parameters of Case B. The system's parameters differ from those in Case A, as shown in Table 6.1. Three working circumstances, including nominal operation, dynamic operation (where the active power reference was stepped down from $500\,kW$ to $400\,kW$; and changes in the parameter sensitivity (-20% variations in the inductance from $5e-4\,H$ to $4e-4\,H$), were selected to test the effectiveness of the proposed MPC controller in Chapter 4. In order to obtain a unity power factor, the reactive power reference was set to zero throughout the experiments.

The experimental results were shown in Figure 6.30 and focused on the performance of the proposed MPC algorithm with the parameters of Case B under nominal operating circumstances. The active power of reference was $500\,kW$, and the reactive power of reference was $0\,VAR$ to ensure a unity power factor. The active power, P, and the reactive power, Q, tracked the reference powers, as shown in Figure 6.30. The output grid phase voltages, with peak values of $310V$, are represented by e_A, e_B, and e_C. At the same time, the output grid currents are represented by i_A, i_B, and i_C. As can be seen from the output waveform of Figure 6.30, the system's output currents and voltages were stable. The voltages of the DC-link capacitors are represented by U_{c1} and U_{c2}. As a result, under steady-state operating circumstances, the proposed MPC algorithm can accomplish active power and reactive power tracking, stable current and voltage output, and neutral point balancing.

Comparative results are provided in Table 6.12, for the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC algorithm in Chapter 3. The waveforms corresponding to the experimental results are depicted in Figure 6.16, Figure 6.17 and Figure 6.18. Three

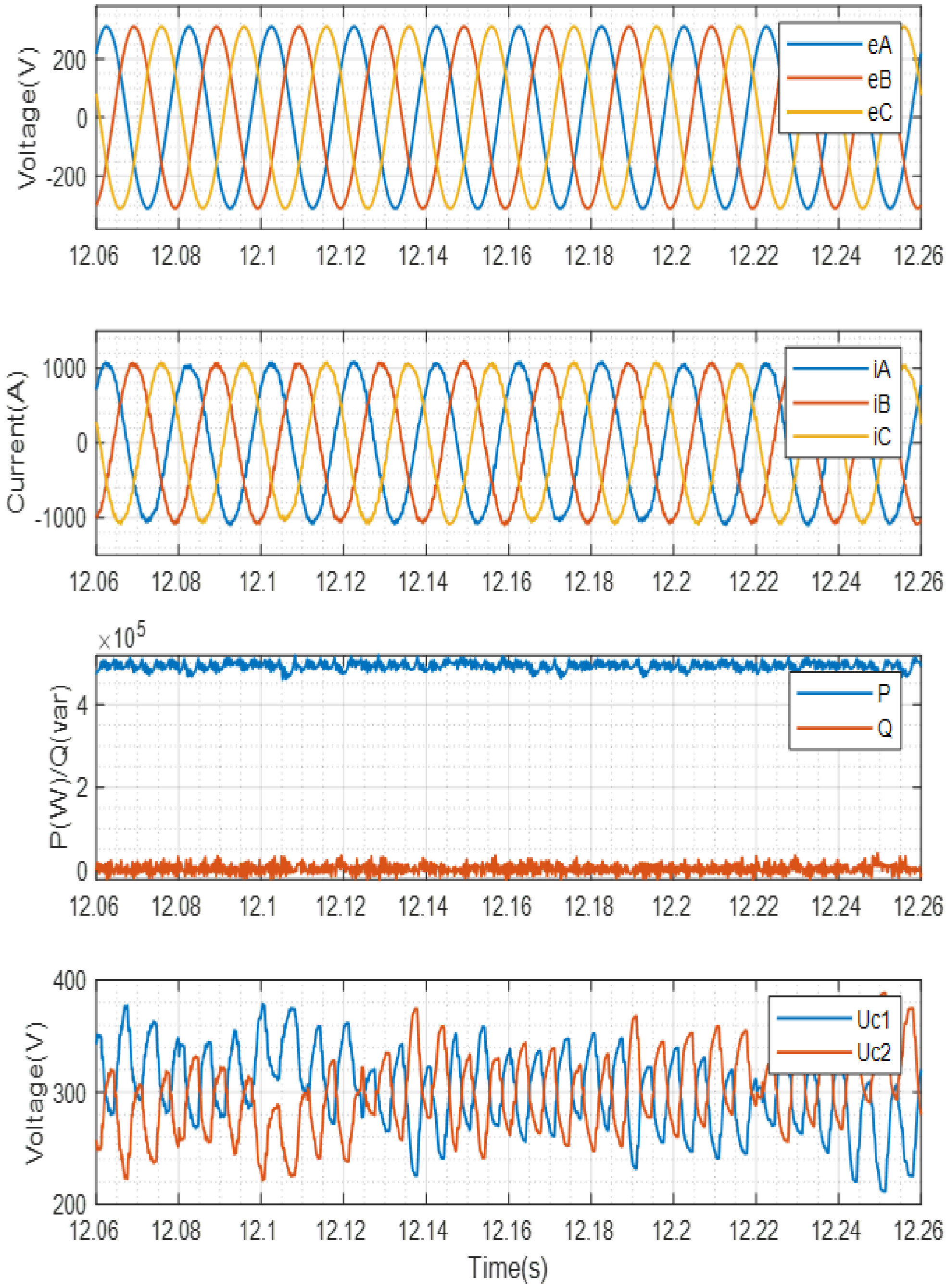

Figure 6.30: Experiment validation results for the proposed MPC algorithm in Chapter 4 under nominal operating conditions (500kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.12: Comparative Results of Chapter 4 for Different Control Algorithms under nominal operation conditions in Case B (500kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	2.72%	4.83%	3.44%	3.30%
Switching Frequency(kHz)	1.474	1.532	1.746	1.407
RMS Values of Capacitor Voltage Error (V)	71.953	65.865	69.866	87.725

elements, including the THD value of the output current, the switching frequency, and the RMS value of the DC-link capacitor voltage error, would be analysed in light of the experimental data in Table 6.12. The THD values of the output currents for the proposed MPC algorithms 2.72% were the lowest among the four methods. Compared to the conventional MPC algorithms in [82] (4.83%), the proposed MPC algorithm reduced 44% of switching frequency. The optimal MPC algorithm in [31] and the multistep MPC algorithm in [137] obtained 3.44% and 3.30%. As to switching frequency, the proposed MPC algorithm in Chapter 4 ($1.474kHz$) had a lower value than $1.532kHz$ the conventional MPC algorithms in [82] and $1.746kHz$ the optimal MPC algorithm in [31]. The proposed MPC algorithm's switching frequency was just $0.067kHz$ behind $1.407kHz$ the multistep MPC algorithm in [137]. The RMS value of the capacitor voltage error for the proposed MPC method was ($71.953V$), which was less than the multistep MPC method in [137] ($87.725V$), but more significant than the conventional MPC algorithms in [82] ($65.865V$) and the optimal MPC algorithm in [31] ($69.866V$).

6.4.5 Case B (Dynamic Operation)

The robustness of the suggested MPC algorithm was evaluated in this section. The reference's active power was reduced from $500\,kW$ to $400\,kW$. Under these dynamic operating conditions, the suggested MPC algorithm was able to accomplish active power tracking and decrease switching frequency.

The proposed MPC algorithm's transient-state performance is illustrated in Figure 6.31. The active power (P) in the figures could swiftly track the step-changes (the reference active power dropping from $500\,kW$ to $400\,kW$). Throughout the period, the reactive power (Q) was maintained at zero. The output grid voltage was sufficiently stable to maintain a three-phase output. Simultaneously, the output currents rapidly adapted to the step-change without overshooting during the transition time. As seen in Figure 6.31, the RMS value of the DC-link capacitor fluctuation voltage was $49.079V$.

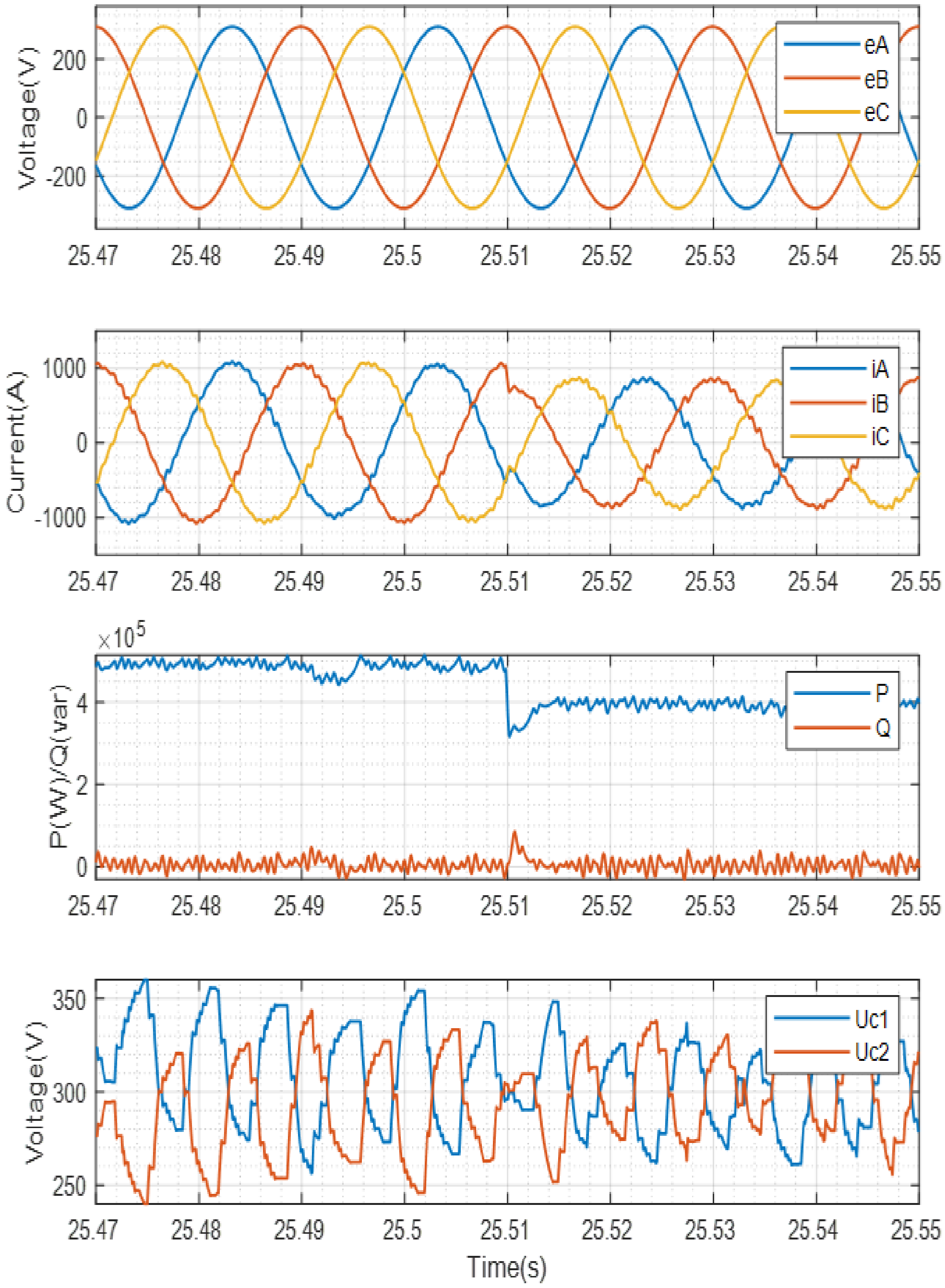

Figure 6.31: Experiment validation results for the proposed MPC algorithm in Chapter 4 under dynamic operating conditions (400kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.13: Comparative Results of Chapter 4 for Different Control Algorithms under dynamic operating conditions in Case B (400kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.14%	4.75%	3.70%	3.22%
Switching Frequency(kHz)	1.530	1.694	1.751	1.432
RMS Values of Capacitor Voltage Error (V)	49.079	46.365	48.898	60.728

Comparative results are provided in Table 6.13 for the proposed MPC algorithm in Chapter 4, the conventional MPC algorithm in [82], the optimal MPC algorithm in [31], and the multistep MPC algorithm in [137] under dynamic operating conditions (reference active power decreasing from 500 kW to 400 kW). The waveforms corresponding to the comparative results are shown in Figure 6.20, Figure 6.21, and Figure 6.22, respectively. These are the waveforms for the conventional MPC algorithm described in [82], the optimal MPC algorithm described in [31], and the multistep MPC algorithm described in [137]. According to Table 6.13, the total harmonic distortion (THD) of grid currents is 3.14% in the proposed MPC algorithm, 4.75% in [82], 3.70% in [31], and 3.22% in [137]. The proposed MPC algorithm achieved $1.530kHz$ switching frequency, which was lower than the conventional MPC methods in [31] ($1.694kHz$) and the optimal MPC algorithm in [31] ($1.751kHz$). When the RMS value of the capacitor voltage error was calculated, the multistep MPC method described in [137] had the highest value ($60.728V$). In contrast, the conventional MPC algorithm in [82] had the lowest value ($46.365V$). The proposed MPC algorithm' RMS value was $49.079V$.

6.4.6 Case B (Parameter Sensitivity)

This section analyses and compares the sensitivity of the proposed MPC algorithm in Chapter 4 to parameter (inductance) variations using representative parameters from Case B, with the comparison of the conventional MPC algorithm [82], the optimal MPC algorithm [31], and the multistep MPC algorithm [137]. During this testing process, the parameter sensitivity varied by -20% inductance from $5e-4\,H$ to $4e-4\,H$. Figure 6.32, Figure 6.24, Figure 6.25 and Figure 6.26 illustrate the waveforms associated with the experimental outcomes. Table 6.14 contains comparative findings. As demonstrated by the findings, the proposed MPC algorithm is capable of overcoming misidentification of inductances due to parameter changes. The sensitivity of the parameters had no discernible influence on the system.

The proposed MPC algorithm's performance under parameter sensitivity circumstances is shown in Figure 6.32. According to the figures, the active power (P) can remain stable

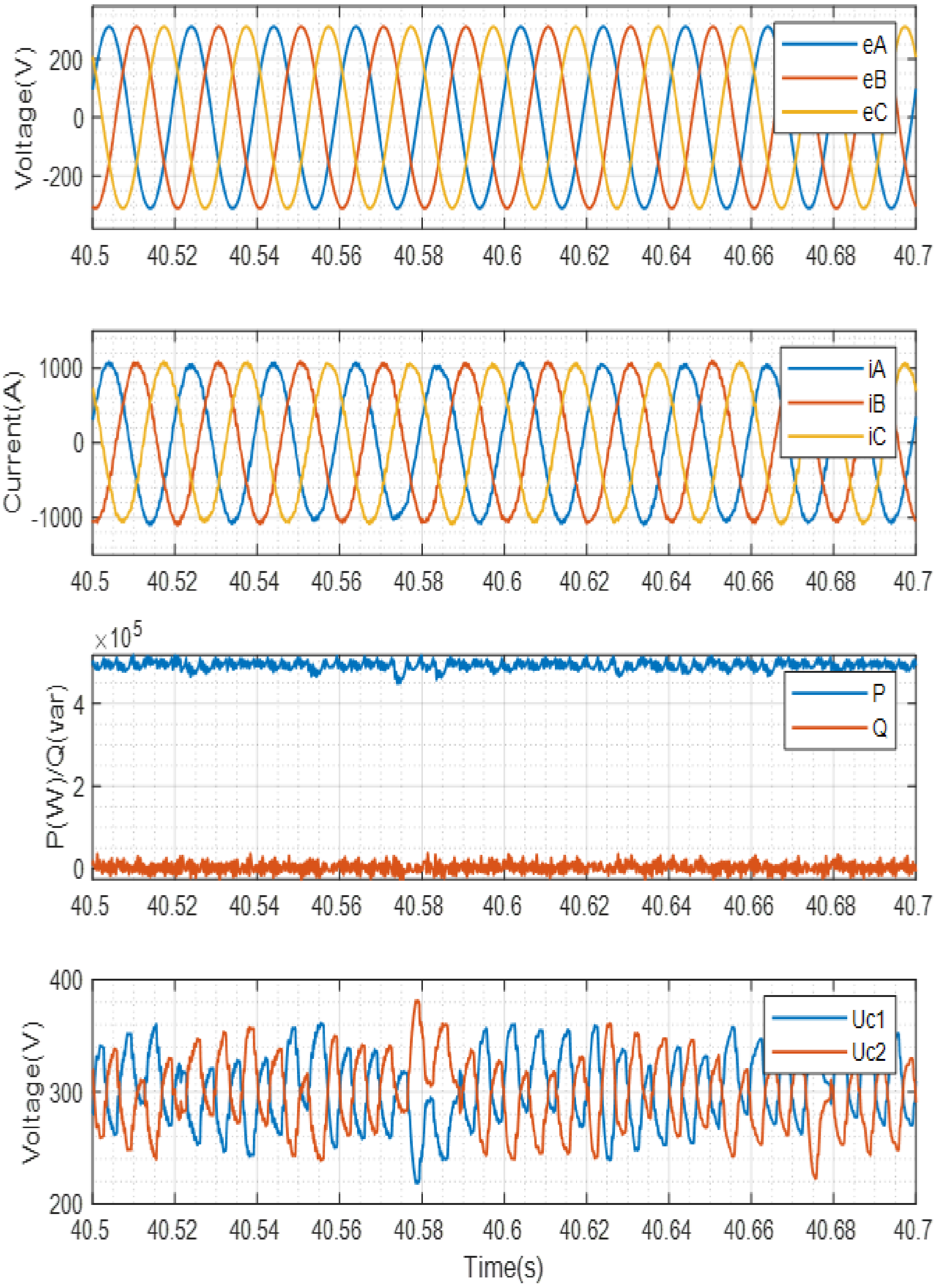

Figure 6.32: Experiment validation results for the proposed MPC algorithm in Chapter 4 under parameter sensitivity conditions in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.14: Comparative Results of Chapter 4 for Different Control Algorithms in Case B (Parameter Sensitivity)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	2.47%	4.19%	3.95%	2.69%
Switching Frequency(kHz)	1.595	1.675	1.676	1.500
RMS Values of Capacitor Voltage Error (V)	58.463	57.224	64.903	77.289

even when the inductance varies by -20% between $5e-4\,H$ and $4e-4\,H$. The output grid voltages and currents were both capable of maintaining a constant three-phase output under parameter sensitivity circumstances. The RMS value of the fluctuating DC-link capacitor voltage was $58.463V$ in Figure 6.32.

In comparison to the results in Table 6.14, the proposed MPC algorithm in Chapter 4 achieved THD values of 2.47% under parameter sensitivity conditions, which is less than the 4.19% for the conventional MPC algorithm in [82] and 3.95% for the optimal MPC algorithms in [31]. The output currents of the multistep MPC method described in [137] had a THD value of 2.69%. In terms of switching frequency, the proposed MPC algorithm ($1.595\,kHz$) was still lower than the standard MPC method ($1.675\,kHz$) described in [82] and the optimal MPC algorithm ($1.676\,kHz$) described in [31]. The frequency produced by the multistep MPC method described in [137] was $1.500\,kHz$. In terms of the capacitor voltage error, the proposed MPC method and the conventional MPC algorithm in [82] obtained almost identical capacitor voltage error levels, which are respectively $58.463\,V$ and $57.224\,V$. The optimal MPC algorithm in [31] and the multistep MPC algorithm in [137] achieved the bigger RMS values $64.903\,V$ and $77.289\,V$, respectively.

6.5 Experimental Results for the Proposed Control Algorithms in Chapter 5

This part evaluated the efficacy of the suggested MPC algorithm in Chapter 5. The performance of the proposed MPC algorithms was validated in Chapter 5. A set of two distinct plants with representative parameters (Case A and Case B) was utilised. The setup settings and values for Case A and Case B are detailed in Table 6.1 and Table 6.2. To demonstrate the effectiveness of the proposed MPC algorithm in Chapter 5, three operating conditions were considered in this section: nominal operation, dynamic operation (where the active power reference stepping down from $1\,MW$ to $600\,kW$ in Case A, and from $500\,kW$ to $400\,kW$ in Case B) and changes in parameter sensitivity

(-33.3% variation in inductance from $1.5e-3\,H$ to $1e-3\,H$ in Case A, and -20% variation in inductance from $5e-4\,H$ to $4e-4\,H$ in Case B). The reactive power reference was adjusted to zero in order to maintain a power factor of unity throughout the various tests.

6.5.1 Case A (Nominal Operation)

The proposed MPC algorithm's performance was examined under nominal operating circumstances in Figure 6.33. To achieve a unity power factor, the reference active power was $1\,MW$, and the reference reactive power was $0\,VAR$. As seen in Figure 6.33, both the active and reactive powers, P and Q, tracked the reference powers. e_A, e_B, and e_C in Figure 6.33 reflect the output grid phase voltages, which peaked at $310V$. The output grid currents are denoted by the variables i_A, i_B, and i_C. Thus, it can be noted from Figure 6.33 that the system's output currents and voltages were steady. U_{c1} and U_{c2} are the voltages of the DC-link capacitors. The DC-link capacitor fluctuation voltage had a root-mean-square (RMS) value of $75.437\,V$, which was 2.51% of the overall DC-link voltage. This shows that the proposed MPC algorithm successfully balanced neutral points with acceptable ripples. As a result, the proposed MPC algorithm can accomplish active and reactive power tracking, stable current and voltage output, and neutral point balancing under steady-state operating circumstances.

The conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137], and the proposed MPC algorithm described in Chapter 5 are all compared in Table 6.15. Figure 6.4, Figure 6.5 and Figure 6.6 illustrate the waveforms associated with the experimental outcomes. Regarding the data in Table 6.15, the experimental results are analysed from three perspectives: THD of the output current, switching frequency, and RMS of the DC-link capacitor voltage error. The THD values of the output currents 3.55% are less than those of the conventional MPC algorithms in [82] (3.88%) and the optimal MPC algorithm in [31] (4.08%), but are more than those of the multistep MPC algorithm in [137] (2.29%). Chapter 5's proposed MPC algorithm ($3.176kHz$) has the lowest switching frequency of these four approaches. The switching frequency of the other three techniques is $4.680kHz$ for conventional MPC algorithm, $4.645kHz$ for optimal MPC algorithm, and $4.528kHz$ for multistep MPC algorithm. The RMS value of the capacitor voltage error ($75.437V$) for the proposed MPC algorithm is bigger than the optimal MPC algorithm described in [82] ($59.417V$), the conventional MPC algorithms described in [31] ($56.385V$) and the multistep MPC algorithm described in [137] ($54.403V$).

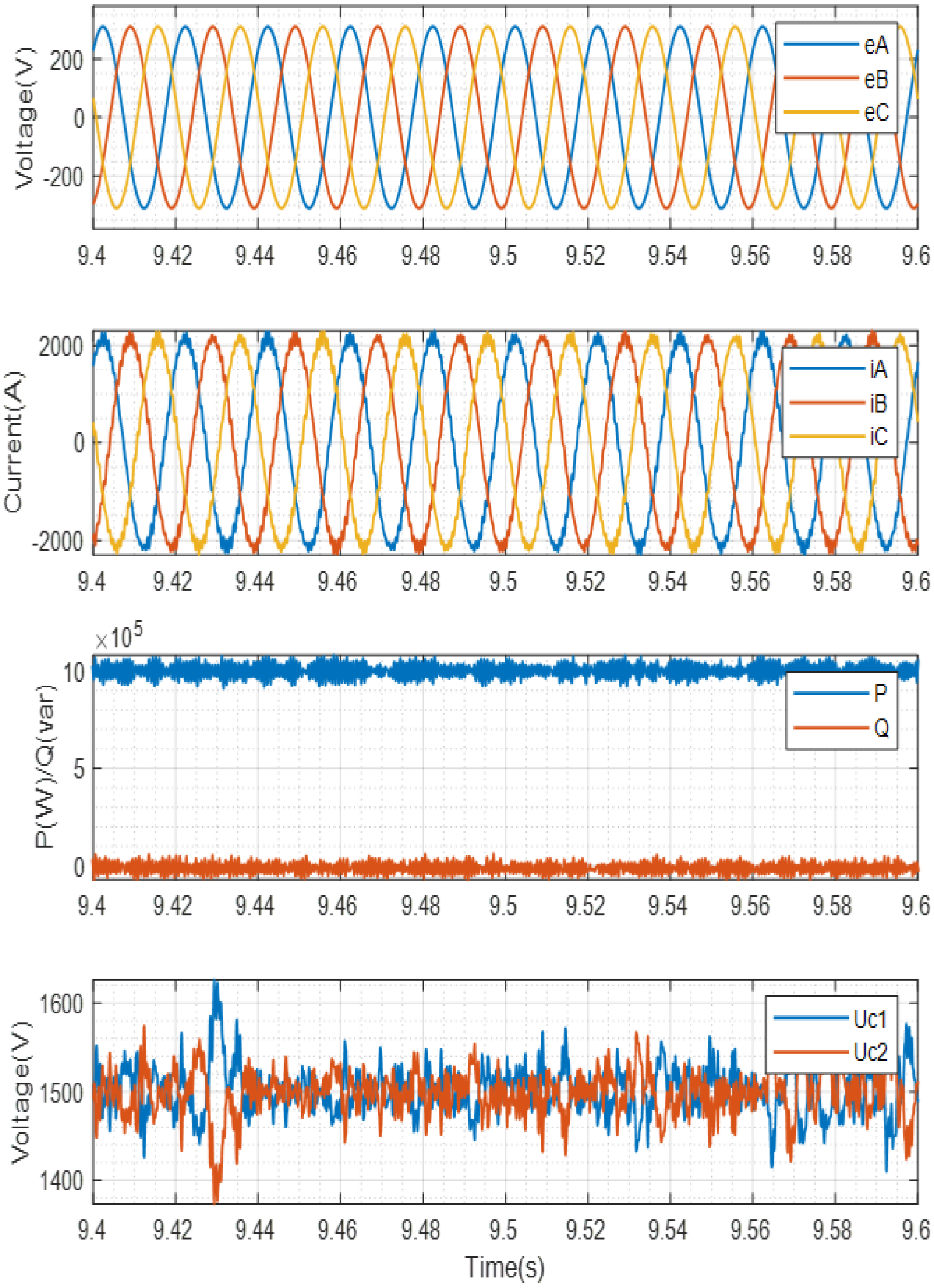

Figure 6.33: Experiment validation results for the proposed MPC algorithm in Chapter 5 under nominal operating conditions (1MV) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.15: Comparative Results of Chapter 5 for Different Control Algorithms under nominal operating conditions in Case A (1MW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.55%	3.88%	4.08%	2.29%
Switching Frequency(kHz)	3.176	4.680	4.645	4.528
RMS Values of Capacitor Voltage Error (V)	75.437	56.385	59.417	54.403

6.5.2 Case A (Dynamic Operation)

This section evaluated the suggested MPC algorithm's robustness. The reference's active power was reduced from 1 MW to 600 kW. The suggested MPC algorithm was able to accomplish active power tracking and minimise switching frequency under these dynamic operating circumstances. The suggested MPC algorithm's transient-state performance is illustrated in Figure 6.34. As seen in the figures, the active power (P) is capable of swiftly tracking the step-change. Simultaneously, the reactive power (Q) is kept constant during the period. The output grid voltage was sufficiently stable to maintain a three-phase output. Simultaneously, the output currents responded rapidly to the step-change throughout the transition period without overshooting. As seen in Figure 6.34, the RMS value of the DC-link capacitor fluctuating voltage was 41.590V, which was equal to 1.39% of the overall DC-link voltage while the system was operating normally.

The conventional MPC algorithm described in [82], the optimal MPC algorithm described in [31], the multistep MPC algorithm described in [137], and the proposed MPC algorithm described in Chapter 5 are all compared in Table 6.16 under dynamic operating conditions (reference active power decreasing from 1 MW to 600 kW). In Figure 6.8, Figure 6.9, and Figure 6.10, the waveforms corresponding to the experimental findings are displayed. The total harmonic distortion (THD) of grid currents was 4.78% in the proposed MPC algorithm, 5.28% in [82], 4.85% in [31], and 3.40% in [137], as shown in Table 6.16. The suggested MPC algorithm produced output currents with a lower THD value than the conventional MPC algorithm in [82] and the optimal MPC algorithms in [31]. Additionally, the suggested MPC algorithm got the lowest switching frequency (3.208kHz). Others include the conventional MPC methods 4.747kHz described in [82], the optimal MPC algorithm 4.929kHz described in [31], and the multistep MPC algorithm 5.115kHz described in [137]. The suggested method is capable of considerably reducing switching frequency because the current slope control suppresses current variations to a narrow range, allowing the current slope to closely track the reference current slope. The multistep MPC technique described in [137] (18.476V) has the least RMS value for the capacitor voltage error. The suggested MPC algorithm (41.590V)

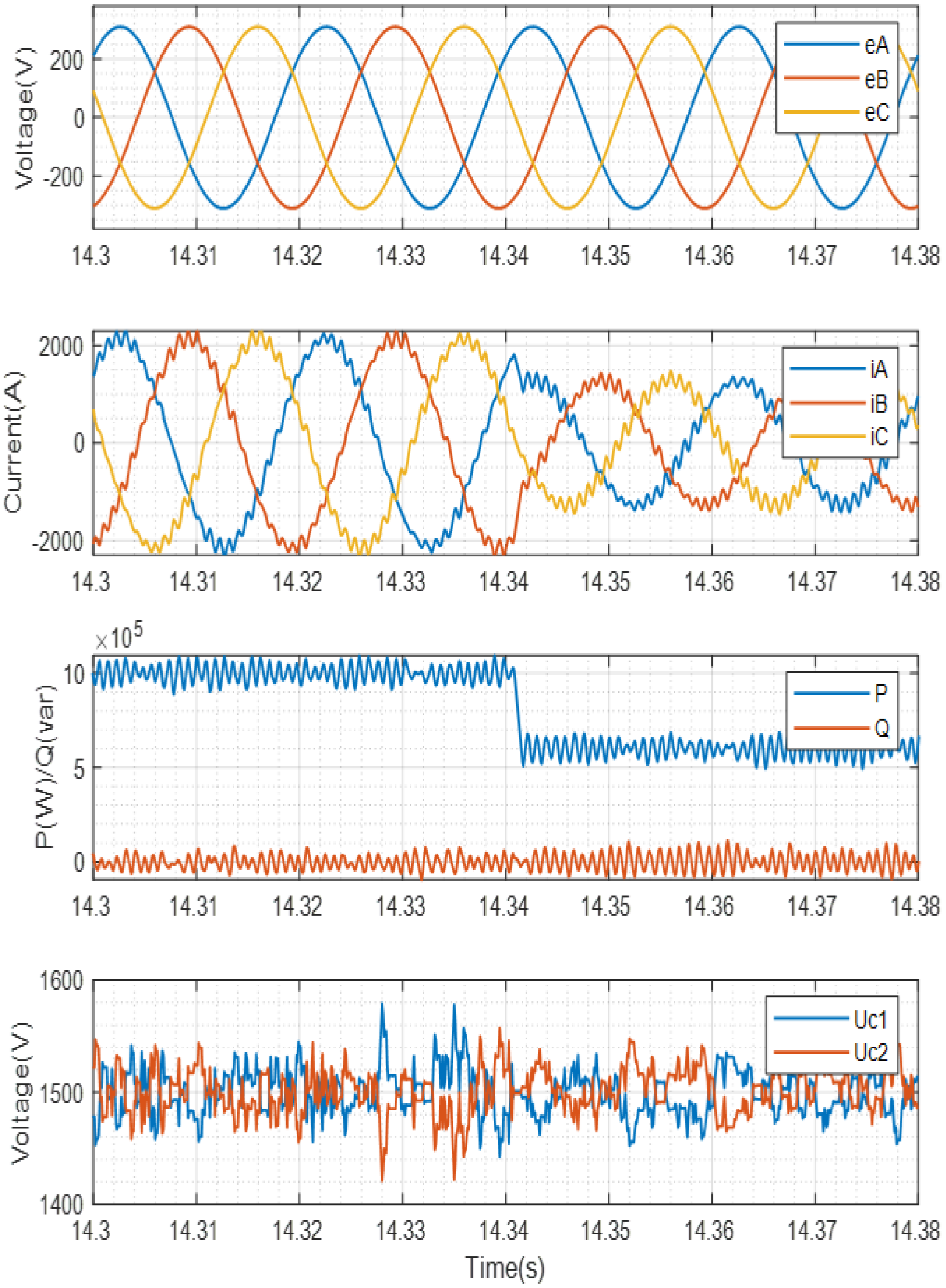

Figure 6.34: Experiment validation results for the proposed MPC algorithm in Chapter 5 under dynamic operating conditions (600kW) in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.16: Comparative Results of Chapter 5 for Different Control Algorithms under dynamic operating conditions in Case A (600kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	4.78%	5.28%	4.85%	3.40%
Switching Frequency(kHz)	3.208	4.747	4.929	5.115
RMS Values of Capacitor Voltage Error (V)	41.590	30.806	29.026	18.476

Table 6.17: Comparative Results of Chapter 5 for Different Control Algorithms in Case A (Parameter Sensitivity)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.00%	3.30%	3.41%	2.16%
Switching Frequency(kHz)	3.237	4.749	4.783	4.999
RMS Values of Capacitor Voltage Error (V)	75.437	60.642	61.870	51.104

obtained a value comparable to that of the conventional MPC method described in [82] (30.806V) and the optimum MPC algorithm described in [31] (29.026V).

6.5.3 Case A (Parameter Sensitivity)

The sensitivity of the suggested MPC algorithm in Chapter 5 to parameters (inductance) was analysed and compared to the conventional MPC algorithm [82], the optimal MPC algorithms in [31] and the multistep MPC algorithm in [137]. During this testing procedure, the parameter sensitivity varied by −33.3% inductance from $1.5e-3\,H$ to $1e-3\,H$. Table 6.17 contains comparative findings. In Figure 6.35, Figure 6.12, Figure 6.13 and Figure 6.14, the waveforms corresponding to the experimental findings are indicated. As can be seen from the above findings, the proposed MPC algorithm is capable of overcoming inductance misidentification when parameter modifications have no significant influence on the system.

In comparison to the results in Table 6.17, the proposed MPC algorithm in Chapter 5 achieved the second-lowest THD of the output currents, with THD values of 3.00% for the proposed MPC algorithm, 3.30% for the conventional MPC algorithm in [82], 3.41% for the optimal MPC algorithms in [31] and 2.16% for the multistep MPC algorithm in [137], respectively. The switching frequency of the suggested MPC algorithm remained lower than the other three MPC methods. The switching frequency of the proposed MPC

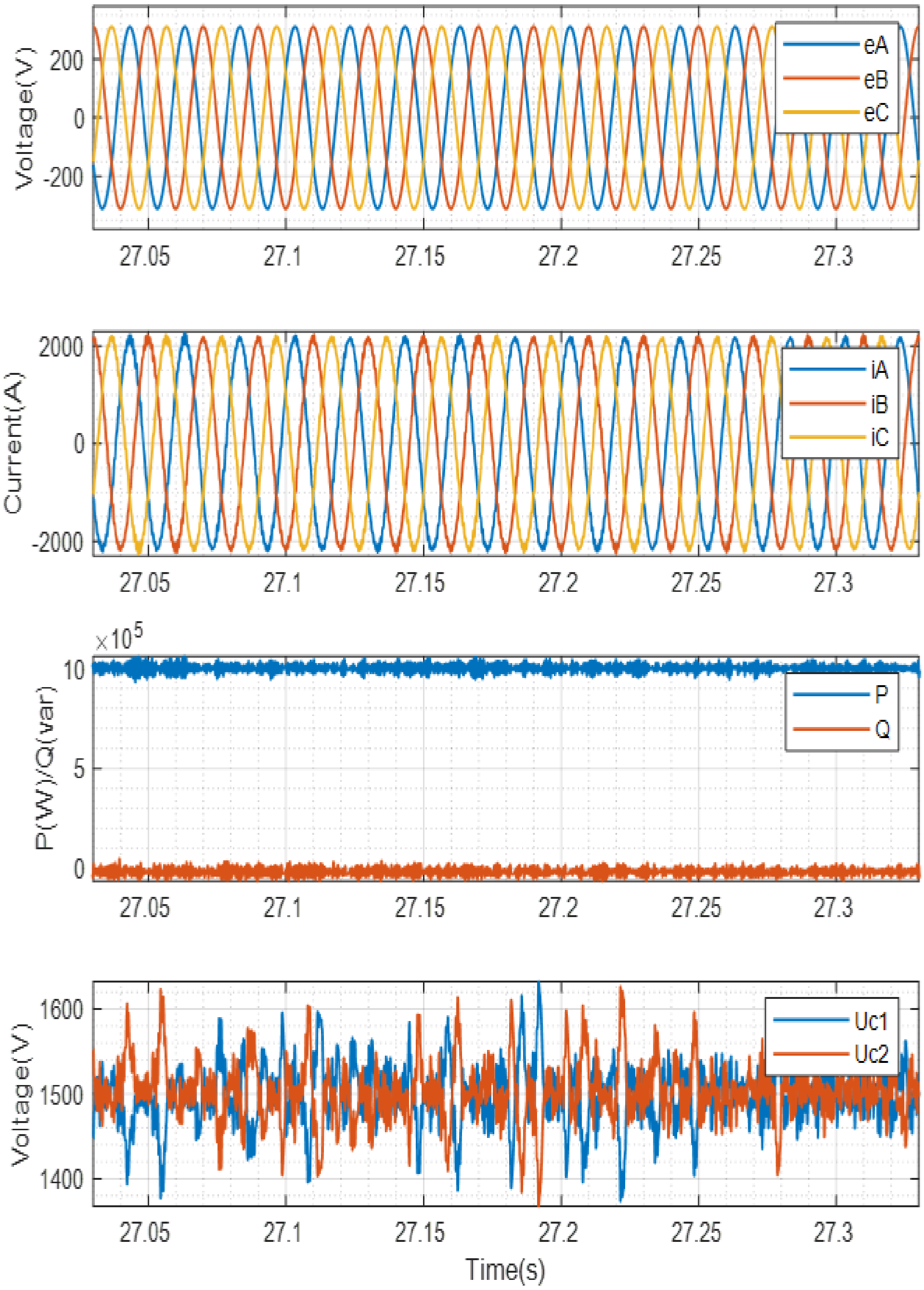

Figure 6.35: Experiment validation results for the proposed MPC algorithm in Chapter 5 under parameter sensitivity conditions in Case A: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

algorithm was reduced by more than 35%, compared to the multistep MPC algorithm in [137], which generates a frequency of $4.999\,kHz$. The conventional MPC algorithm in [82] generated a frequency of $4.749\,kHz$, and the optimal MPC algorithms in [31] generated a frequency of $4.783\,kHz$. In terms of capacitor voltage error RMS values, the proposed MPC algorithm was $75.437\,V$, while the other three methods were $60.642\,V$ for the conventional MPC algorithm in [82], $61.870\,V$ for the optimal MPC algorithm in [31], and $51.104\,V$ for the multistep MPC algorithm in [137].

6.5.4 Case B (Nominal Operation)

The following three sections validate the proposed MPC algorithm in Chapter 5, applying for a three-level NPC inverter system with representative characteristics from Case B. In comparison to Case A, the system's parameters are changed, as shown in Table 6.1. Three operating conditions were used to evaluate the proposed MPC controller's effectiveness: nominal operation, dynamic operation (with the active power reference stepped down from $500\,kW$ to $400\,kW$), and changes in parameter sensitivity (-20% variations in inductance from $5e-4\,H$ to $4e-4\,H$). Throughout the different tests, the reference for reactive power was set to zero to obtain a unity power factor.

The experimental findings focusing on the proposed MPC algorithm's performance with typical Case B parameters under nominal operating circumstances are shown in Figure 6.36. In order to guarantee a unity power factor, the reference's active power was $500\,kW$ while the reference's reactive power was $0\,VAR$. As shown in Figure 6.36, both the active and reactive powers, P and Q, followed the reference powers. Meanwhile, e_A, e_B, and e_C denote the output grid phase voltages, which reached a maximum value of $310V$. The output grid currents are denoted by the variables i_A, i_B, and i_C. Thus, it should be noticed from the output waveform of the Figure 6.36 that the system's output currents and voltages were steady. U_{c1} and U_{c2} are the voltages of the DC-link capacitors. The RMS value of the fluctuating voltage across the DC-link capacitor was $68.066,V$. This shows that the suggested MPC method in Chapter 5 maintained neutral point balancing with acceptable ripples when used with the representative parameters from Case B. Thus, under steady-state operating circumstances, the proposed MPC algorithm can accomplish active and reactive power tracking, constant current and voltage output, and neutral point balancing.

Comparative results are given in Table 6.18 for the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], the multistep MPC algorithm in [137] and the proposed MPC algorithm in Chapter 5. Figure 6.16, Figure 6.17 and Figure 6.18 illustrate the waveforms associated with the experimental findings. Three elements, including the THD value of the output current, the switching frequency, and the RMS value of the DC-link capacitor voltage error, would be analysed in light of the findings in Table 6.18.

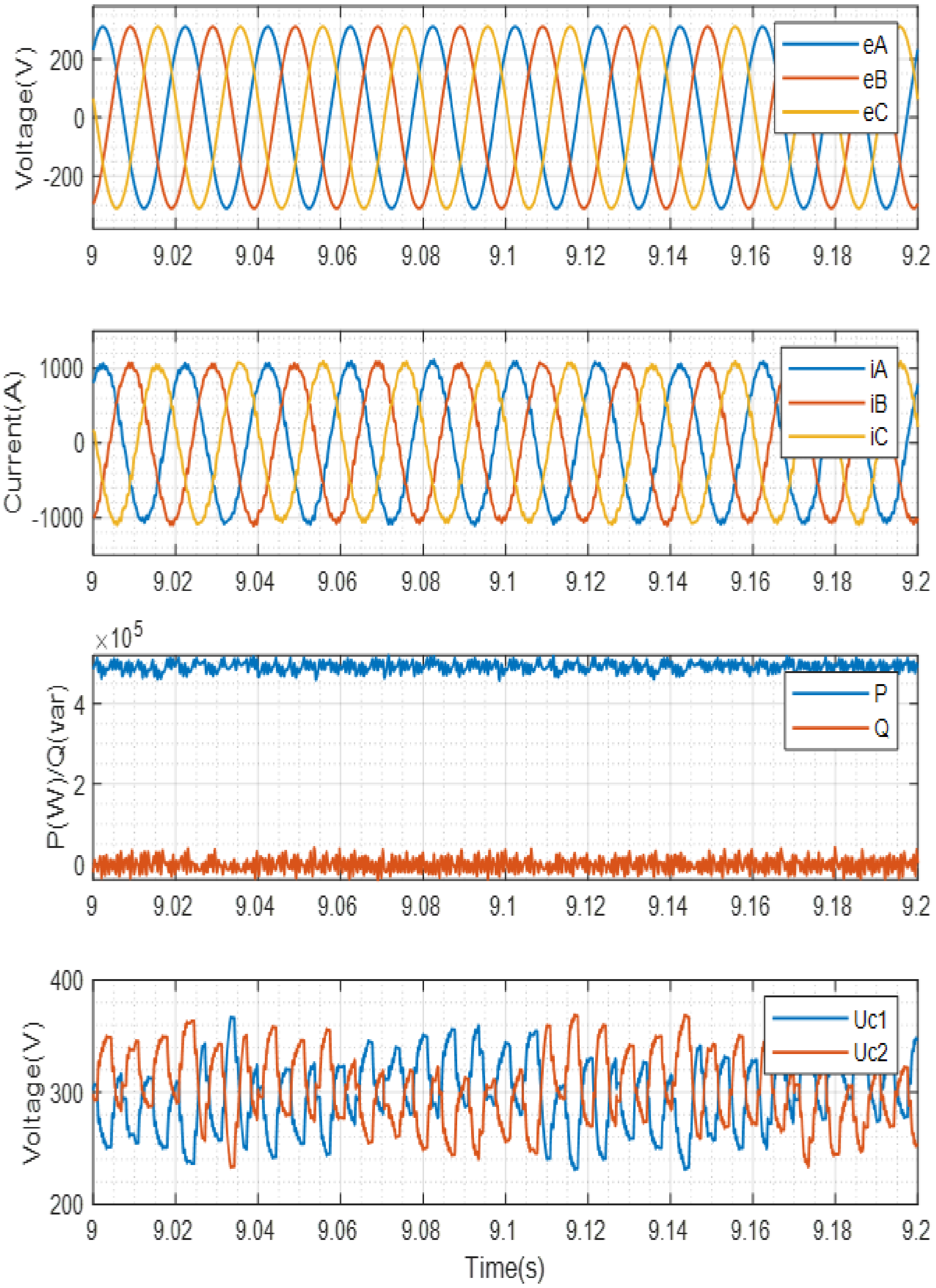

Figure 6.36: Experiment validation results for the proposed MPC algorithm in Chapter 5 under nominal operating conditions (500kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.18: Comparative Results of Chapter 5 for Different Control Algorithms under nominal operating conditions in Case B (500kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.30%	4.83%	3.44%	3.30%
Switching Frequency(kHz)	1.326	1.532	1.746	1.407
RMS Values of Capacitor Voltage Error (V)	68.066	65.865	69.866	87.725

The proposed MPC algorithms had the same THD value as the multistep MPC algorithm in [137], which was 3.30%. This THD value was lower than the conventional MPC algorithms in [82] (4.83%) and the optimal MPC algorithm in [31] (3.44%). The suggested MPC algorithm ($1.326kHz$) in Chapter 5 has switching frequency lowest than the conventional MPC method ($1.532kHz$) in [82], the optimal MPC algorithm ($1.746kHz$) in [31], and the multistep MPC method ($1.407kHz$) in [137]. The RMS value of the capacitor voltage error ($68.066V$) for the proposed MPC algorithm is less than that of the multistep MPC algorithm described in [137] ($87.725V$) and the conventional MPC algorithm described in [82] ($65.865V$), but is greater than that of the optimal MPC algorithms described in [31] ($69.866V$).

6.5.5 Case B (Dynamic Operation)

This section evaluates the robustness of the proposed MPC algorithm in Chapter 5. The reference system's active power was reduced from $500\,kW$ to $400\,kW$. Under these dynamic operating circumstances, the proposed MPC algorithm achieved active power tracking and decreased switching frequency.

The suggested MPC algorithm's transient-state performance is shown in Figure 6.37. The active power (P) in the figures followed the step-change quickly (the reference active power dropping from $500\,kW$ to $400\,kW$). Throughout the period, the reactive power (Q) is kept constant at zero. The output grid voltage was stable enough to support a three-phase output. Simultaneously, the output currents could rapidly react to the step shift without overshooting the transition time. The RMS value of the DC-link capacitor fluctuation voltage was $50.850V$, as shown in Figure 6.37.

Comparative results are provided in Table 6.19 for the proposed MPC algorithm in Chapter 5, the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], and the multistep MPC algorithm in [137] under dynamic operating conditions (reference active power decreasing from $500\,kW$ to $400\,kW$). The waveforms corresponding to the comparative results are shown in Figure 6.20, Figure 6.21 and Figure 6.22, respectively.

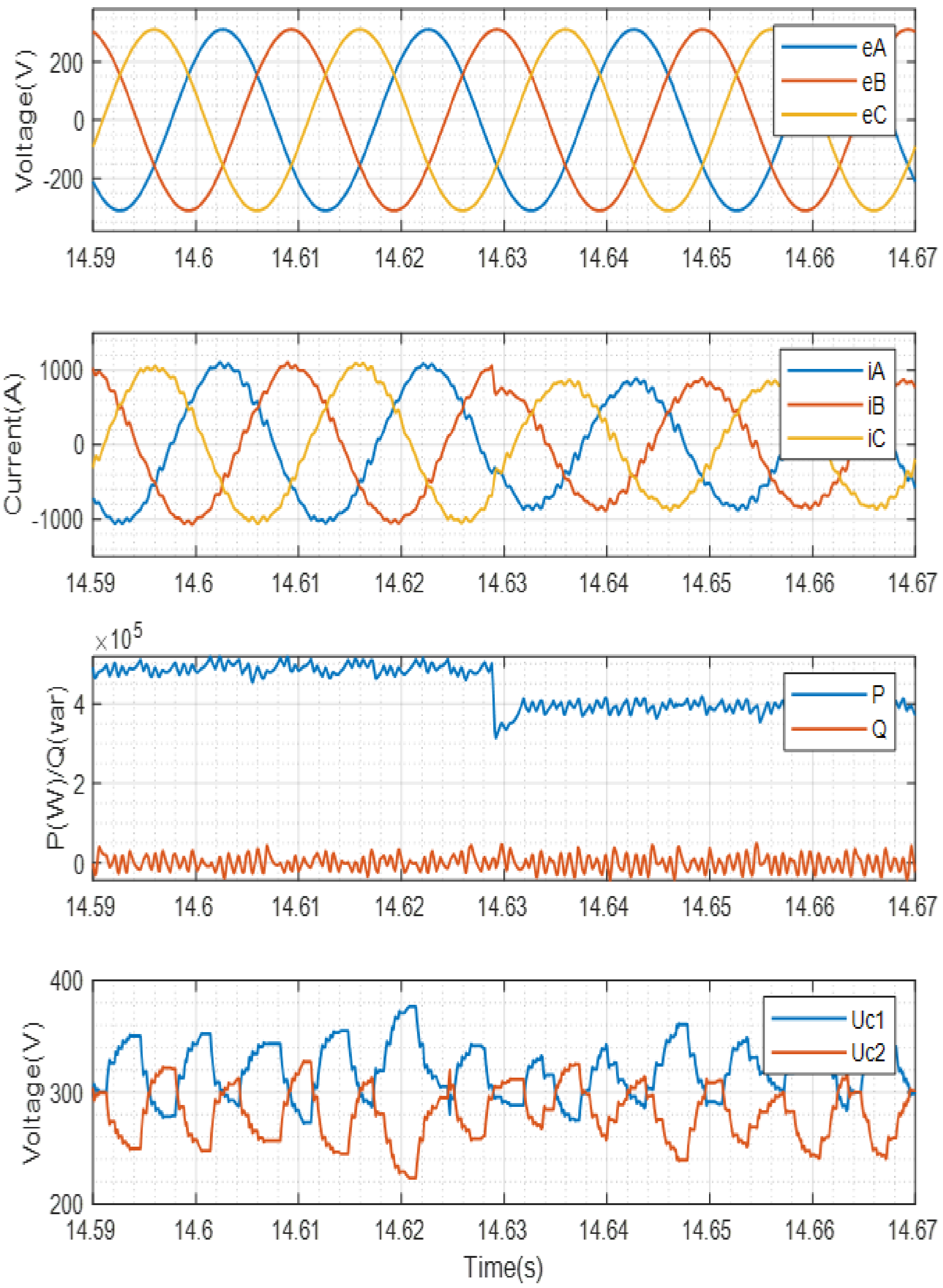

Figure 6.37: Experiment validation results for the proposed MPC algorithm in Chapter 5 under dynamic operating conditions (400kW) in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.19: Comparative Results of Chapter 5 for Different Control Algorithms under dynamic operating conditions in Case B (400kW)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	4.36%	4.75%	3.70%	3.22%
Switching Frequency(kHz)	1.360	1.694	1.751	1.432
RMS Values of Capacitor Voltage Error (V)	50.850	46.365	48.898	60.728

They correspond to the waveforms of the conventional MPC algorithm in [82], the optimal MPC algorithm in [31], and the multistep MPC algorithm in [137]. According to Table 6.19, the total harmonic distortion (THD) of grid currents was 4.36% in proposed MPC algorithm, 4.75% in [82], 3.70% in [31] and 3.22% in [137], respectively. In terms of switching frequency, the proposed MPC algorithm achieved the lowest switching frequency 1.360kHz, while 1.694kHz for the switching frequency of the conventional MPC algorithm described in [82], 1.751kHz for that of the optimal MPC algorithm in [31], and 1.432kHz for that of the multistep MPC algorithm in [137]. When the RMS value of the capacitor voltage error was calculated, the multistep MPC algorithm in [137] produced the highest result (60.728V), while the conventional MPC algorithm in [82] produced the lowest value 46.365V. The proposed MPC algorithm in Chapter 5 and the optimal MPC algorithms in [31] generated 50.850V and 48.898V, respectively.

6.5.6 Case B (Parameter Sensitivity)

This section analyses and compares the parameter (inductance) sensitivity of the proposed MPC algorithm in Chapter 5 to the conventional MPC algorithm in [82], the optimal MPC algorithms in [31], and the multistep MPC algorithm in [137]. Throughout this experimental procedure, the parameter sensitivity varied by -20% inductance from $5e-4\,H$ to $4e-4\,H$. The waveforms corresponding to the experimental findings are shown in Figure 6.38, Figure 6.24, Figure 6.25 and Figure 6.26. Table 6.20 contains comparative data. As shown by the preceding findings, the suggested MPC method is capable of overcoming inductance misidentification caused by parameter changes. The system was unaffected by the parameter sensitivity.

The proposed MPC algorithm's performance under parameter sensitivity circumstances is shown in Figure 6.38. According to the statistics, the active power (P) can maintain stability even when the inductance varies by -20% from $5e-4\,H$ to $4e-4\,H$. In the meanwhile, the reactive power (Q) is held constant at zero. Both output grid voltages and currents were capable of maintaining a constant three-phase output under parameter

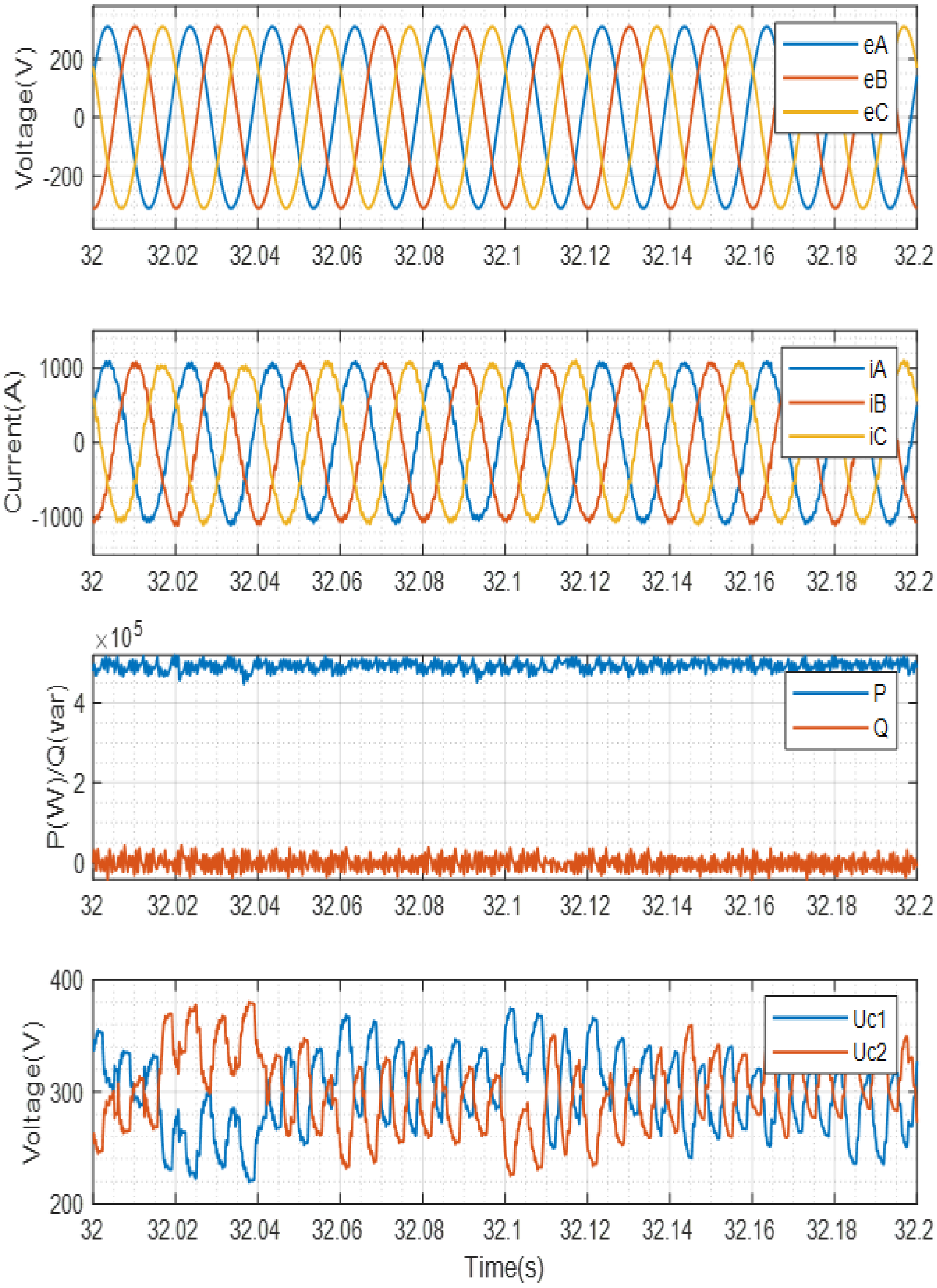

Figure 6.38: Experiment validation results for the proposed MPC algorithm in Chapter 5 under parameter sensitivity conditions in Case B: the grid voltages, e_A,e_B,e_C, the grid currents i_A,i_B,i_C, the active power, P, and reactive power, Q, and the voltages of the DC-link capacitors, U_{c1} and U_{c2}.

Table 6.20: Comparative Results of Chapter 5 for Different Control Algorithms in Case B (Parameter Sensitivity)

	Proposed MPC	**MPC in [82]**	**MPC in [31]**	**MPC in [137]**
THD	3.29%	4.19%	3.95%	2.69%
Switching Frequency(kHz)	1.383	1.675	1.676	1.500
RMS Values of Capacitor Voltage Error (V)	71.108	57.224	64.903	77.289

sensitivity circumstances. The RMS value of the DC-link capacitor fluctuation voltage was $71.108V$ in Figure 6.38.

In terms of the comparative results in Table 6.20, the proposed MPC algorithm in Chapter 5 achieved THD values of 3.29% under parameter sensitivity conditions, which is less than the 4.19% for the conventional MPC algorithm in [82] and 3.95% for the optimal MPC algorithms in [31]. The multistep MPC algorithm in [137] has a THD value of 2.69%. As for switching frequency, the proposed MPC algorithm ($1.383\,kHz$) achieved the best value among these four methods. The other three methods were $1.675\,kHz$ for the conventional MPC algorithm in [82], $1.676\,kHz$ for the optimal MPC algorithms in [31] and $1.500\,kHz$ for the multistep MPC algorithm in [137]. As for the capacitor voltage error, the proposed MPC method in Chapter 5 and the multistep MPC algorithm in [137] obtained the similar voltage error, which are respectively $71.108\,V$ and $77.289\,V$. The conventional MPC algorithm in [82] attained the lowest RMS value of $57.224\,V$. The optimal MPC algorithms in [31] produced the RMS value of $64.903\,V$.

6.6 Summary

This chapter discusses in depth the verification of the proposed model predictive control algorithms, including in Chapter 3, Chapter 4 and Chapter 5, on a three-level NPC inverter grid-connect system. To begin, the experiential method for the Hardware-in-the-Loop (HIL) test system was described in detail. Following that, the experimental setup utilised in the experiment was shown. To validate the performance of the proposed model predictive control algorithms, a set of two distinct plants with representative parameters (Case A and Case B) was implemented in the thesis. Additionally, three operating circumstances were examined to determine the efficacy of the proposed MPC algorithms: nominal operation, dynamic operation and parameter sensitivity. Finally, experimental results, including the data and the output waveforms, are presented to illustrate the effectiveness of the proposed MPC algorithms, comparing to some more salient and highly related MPC algorithms.

Chapter 7

Conclusions and Future Work

This chapter draws conclusions from the research model predictive control algorithms for 3-level NPC inverters and suggests future work.

7.1 Conclusions

Multilevel inverters are a vital aspect of being able to meet the emerging requirements for high-power applications and the incorporation of renewable resources into the grid. NPC inverters offer the advantages of being able to split DC-link voltages while minimising switching losses and inducing smaller output current ripples. They have therefore become a particular focus for research. Unfortunately, the use of power switches in NPC inverters renders the system nonlinear, thus generating unwanted complexity in the control process. Conventional solutions to this are mainly based on average state-space modelling and related modulation techniques, which include cascaded control structures. These standard methodologies are associated with a number of explicit constraints. In particular, when modelling, the linearisation has to be associated with a specified operating point. The tuning procedure for the controller is already complicated, so any further alterations of the operating point compound the problem. However, recent advances in fast microprocessor and digital signal processor (DSP) technologies offer the possibility of some novel solutions, including hysteresis current control, sliding mode control and model predictive control (MPC). Amongst these methodologies, MPC provides a means of overriding the cascaded control structures that limit the effectiveness of the most standard methods. It also presents a straightforward way of merging the optimisation specifics and dispensing with the other limitations associated with existing systems. When directly compared to established methods, these benefits from the use of the MPC result in visible enhanced system performance.

The main focus of this PhD thesis is to develop model predictive control algorithms to improve the energy efficiency of 3-level NPC inverters for different scenarios. After meeting the main aim, the proposed MPC algorithms can also implement computational burden reduction in Chapter 3, automatic selection of weighting factors in Chapter 4, and control objective optimisation with the current slope control objective in Chapter 5.

In Chapter 3, an MPC algorithm with a reduced switching frequency was initially proposed concerning 3-level NPC inverters. After this, the MPC algorithm was expanded into a multistep MPC algorithm, which had a reduced computational burden in order to manage current variation and lower THD of output current in the 3-level NPC inverter system. Lastly, extensions of the MPC algorithm were consistently made to the 3-level grid-connected NPC inverters with a reduced computational burden of prediction. The primary findings of this chapter are presented below.

- An MPC algorithm for 3-level NPC inverters with reduced switching frequency was proposed. In contrast to the conventional MPC algorithm, the newly-introduced method may be able to effectively lower the switching frequency, as well as enhancing the output currents' quality in terms of the THD. Furthermore, in comparison to industrial linear PI controllers, the newly proposed algorithm can uphold the key benefits of conventional MPCs. Such advantages include quick responses and the implementation of multiple constraints. Furthermore, the new algorithm should enhance performance in order to make it better than that of the industrial linear PI controller. Lastly, the current reference variation can ensure that the newly-suggested MPC algorithm is sufficiently robust.
- A multistep MPC algorithm with the reduced computational burden that can manage the variations that occur at present in a 3-level NPC inverter system has been presented. Based on the findings of the various investigations, the algorithm is believed to be as effective in terms of the THD of output current and the DC-link capacitor voltage error. Although the number of calculations involved in the new algorithm is only 54 (a decrease of 729 from the conventional algorithm), the same space voltage vectors will be applied to the cost function. Moreover, there is no need to align the new algorithm with weighting factors, and the benefits of the original MPC algorithm will still be upheld, including the ability to handle multiple constraints and to react quickly to current changes.
- The MPC algorithm for 3-level grid-connected NPC inverters with the reduced predictive computational burden presented here involves the expected voltage vectors to replace the predictive currents as far as cost functions are concerned. The algorithm is thus capable of reducing by 27 times the current predictions during the process of optimisation. The suggested algorithm was tested in the 3-level grid-connected NPC inverter system in order to investigate how effective it is. The $IEEE\ Standard$ $519 - 2014$ was followed when establishing the THD values for output currents (2.85% at $32\,kW$, 3.93% at $23\,kW$ and 2.81% at $42\,kW$) when

the dynamic operating conditions were carried out (the active power reference P^* was reduced to $23\,kW$ from $32\,kW$ at $0.3\,s$, after which it was increased to $42\,kW$ at $0.5\,s$.). Furthermore, the RMS value of the DC-link capacitor fluctuation was $1.173\,V$. High-quality results can be achieved using the suggested MPC algorithm, with added benefits for balancing capacitor voltages and tracking power (active and reactive).

A novel MPC algorithm for 3-level grid-connected NPC inverters was proposed in Chapter 4. This new algorithm is developed according to the automatic selection of weighting factors. This involves an innovative cost function allowing for output currents to be tracked, capacitor voltage stability to be ensured, neutral point voltages to be managed and finally, switching frequency and switching loss to be minimised. A vital feature of the algorithm is that it employs a two-dimensional fuzzy logic control mechanism that removes any requirement for trial-and-error testing, the latter being common in existing MPC algorithms for multilevel inverter design. The effectiveness of the proposed new algorithm was therefore supported by the results of the research, meaning it could potentially be a viable renewable energy source. The key findings of this chapter are as follows:

- This chapter explored the effectiveness of a two-dimensional fuzzy logic control mechanism designed to implement the process of automatic weighting factors selection in MPC. Comparisons were made between the performance of the various membership functions (Gaussian, Triangular and Trapezoidal), presented in Table 4.1. To make such comparisons, a Gaussian membership function was entered into the system.

- The proposed MPC algorithm maintained a neutral balancing point generating reasonable ripples under nominal operation. In addition, $1.5\,V$ was identified as the RMS value of the DC-link capacitor fluctuating voltage, representing 0.26% of the total DC-link voltage. Figure 4.9 presents the findings on stable output (such as active power, reactive power, current and voltage).

- Under dynamic working conditions, the proposed algorithm is able to automatically select the appropriate weighting factors without any need for a process of trial-and-error. The proposed algorithm can decrease the switching frequency by at least 30% compared to conventional MPC methods. Moreover, the algorithm is able to track active power (from $1.5\,kW$ to $5\,kW$ at $0.3\,s$, down to $3.5\,kW$ at $0.4\,s$, down again to $2\,kW$ at $0.5\,s$). Another benefit is that is can sustain a neutral point balance, meaning that changes to the DC-link capacitor voltage make up only 0.26% of the total DC-link voltage.

- Comparisons were made between the parameter (inductance) sensitivity of proposed algorithms and the traditional algorithm. The load inductance, L, was

$1.5e-3\,H$. Between $0.2\,s$ and $0.3\,s$, there was a rise in inductance to $2e-3\,H$, i.e., 25%. This increase continued between $0.3\,s$ and $0.4\,s$, rising to $3e-3\,H$ i.e., a 50% increase from the initial inductance of $1.5e-3\,H$. A -75% decrease in the inductance from $7.5e-4\,H$ was observed between $0.4\,s$ to $0.5\,s$. Over 51% decrease in switching frequency was seen in the proposed algorithm. The conventional MPC algorithm produced an $11.8\,kHz$ switching frequency, compared to only $5.7\,kHz$ seen in the proposed algorithm under the same operating conditions. Furthermore, the proposed MPC algorithm consistently achieved lower THD values than the conventional MPC algorithm

In Chapter 5, a novel MPC algorithm, which adds a novel control objective with the current slope, has been proposed for the 3-level grid-connected NPC inverter system. Never before has the current slope been explored as a control objective in an MPC algorithm. The current slope as a control objective can achieve the current slope follow after the reference current slope, which is able to suppress the current fluctuation in a small range. The effectiveness of the suggested algorithm using the current slope control objective has been verified. Decreased switching frequencies and output currents' THD in a variety of functions can be achieved. These functions include nominal operation, dynamic operation and parameter sensitivity. It is thus fair to draw the following conclusions:

- The findings presented in Figure 5.2 show the proposed MPC algorithm with the current slope as the control objective to be effective when employed in nominal operation. Both the active power, P, and reactive power, Q, became stable, and the reference could be tracked. Furthermore, the stable output currents and voltages were obtained, the THD of the output currents being identified by 2.82%. This thus fulfilled requirements of the $IEEE\ Standard\ 519-2014$. A balance was maintained between the neutral point of the DC-link capacitor voltage. The DC-link capacitor fluctuation volume has an RMS value of $4.155\,V$, totalling 0.69% of the total DC-link voltage.
- Moreover, an evaluation of the algorithm's robustness was also carried out. A reduction of active power reference to $24\,kW$ from $31\,kW$ at $0.3\,s$ was established, which was then increased to $41\,kW$ at $0.5\,s$. This allowed the proposed MPC algorithm with the slope current as the control objective to track active power, minimise the switching frequency by 30.22% and reduce the output currents' THD to a greater extent than conventional MPC methods.
- The proposed algorithm is more effective than conventional algorithms in parameter sensitivity and produces lower output current THD and switching frequencies. According to the new algorithm, there was a 30.678% decrease in the switching frequency at +25%, +50%, and -75% variation of inductance with the output

currents' THD also being less than that of the conventional MPC algorithm. The proposed MPC algorithm is able to obtain the good robustness of parameter sensitivity.

In Chapter 6, this chapter covers in detail the verification of the proposed model predictive control algorithms on a three-level NPC inverter grid-connect system, as discussed in Chapter 3, Chapter 4, and Chapter 5. To begin, a detailed description of the experiential approach for the Hardware-in-the-Loop (HIL) test system was provided. Following that, the experimental setup was shown. To demonstrate the effectiveness of the proposed model predictive control algorithms, the thesis built a set of two different plants with representative parameters (Case A and Case B). Additionally, the suggested MPC algorithms were evaluated under three operating conditions: nominal operation, dynamic operation, and parameter sensitivity. Finally, experimental findings, including data and output waveforms, are given to demonstrate the suggested MPC algorithms' efficacy in comparison to other more well-known and closely similar MPC algorithms.

7.2 Future Work

There are a number of future research work arising from this thesis that could be pursued in the future.

- Investigation of the stability of model predictive control for the 3-level NPC inverter system.

  Although the simulation results showed the positive performance, the stability of the system should also be considered theoretically. Lyapunov stability is the most common way of analysing the stability of the system. As this NPC inverter system is a hybrid system, Lyapunov stability can be used in continuous time systems and discrete time systems [162]. The research gap remains because the MPC uses the rolling optimisation mode, the optimisation processes corresponding to adjacent control cycles have no correlation, and the selected objective function is generally not a Lyapunov function. Thus, it is impossible to analyse its stability and transient response characteristics using conventional control theory. The steady-state response characteristics are mostly verified through simulations and experiments, and some additional treatments are needed. It is evident that the analysis theory for MPC is lagging. When faced with more complex systems or systems with higher control requirements, currently available theoretical analysis methods may have an impact on the design process for a specific system predictive controller. Some scholars have begun to study this, such as [163], which focuses on the stability of MPC.

- Investigation of parameter identification for model predictive control in the 3-level NPC inverter system.

  Disturbance attenuation and ageing may cause changes in semiconductor devices. Effective parameter identification methods, such as the finite element method and the least square algorithm, will be explored. The robustness of the model predictive control will be investigated considering changes in semiconductor devices. Power electronic systems may be affected by various uncertainties during actual operations, such as time-varying and unknown disturbances, external uncertainties, measurement errors, and changes or mismatches in the model parameters. Moreover, these various uncertainties may cause the prediction results to diverge from the real function. When a prediction controller based on a mathematical model design is used in an actual situation, the system performance may degrade, and the system may even become unstable. Nowadays, industrial development is increasingly demanding on operating conditions for power electronic systems, and it has become essential to study the parameter identification of the model predictive control.

- Investigation of using real-life hardware to conduct to verify the effectiveness of the proposed methods.

  When the proposed methods are tested in real-life hardware, the results are more convincing. Unfortunately, because there is no corresponding real-life hardware in our laboratory, this part of verification cannot be done at the moment. In the future work, the effectiveness of the proposed methods will be verified in real-life hardware.

- Investigation of constructing a fuzzy system with normalised inputs.

  In Chapter 4, an MPC algorithm based on automated weighting factor selection had be presented for three-level grid-connected NPC inverters. This algorithm makes a unique addition by using a two-dimensional fuzzy logic control strategy, which removes the requirement for trial-and-error techniques that are prevalent in current approaches to MPC-based multilevel inverter design. The future work will be a focus on constructing a fuzzy system with normalised inputs. Working together with input scaling factors, such a system can be implemented more widely.

- Investigation of extending all the proposed control methods to higher level inverter applications.

  In the thesis, all the control methods were designed for 3-level NPC inverters. In future work, all the proposed MPC algorithms would be extended to higher level inverter applications. This may result in a rise in the popularity of the proposed MPC algorithms.

Appendix A

Appendix Simulation Model

Figure A.1 shows the SPWM simulation model in MATLAB.

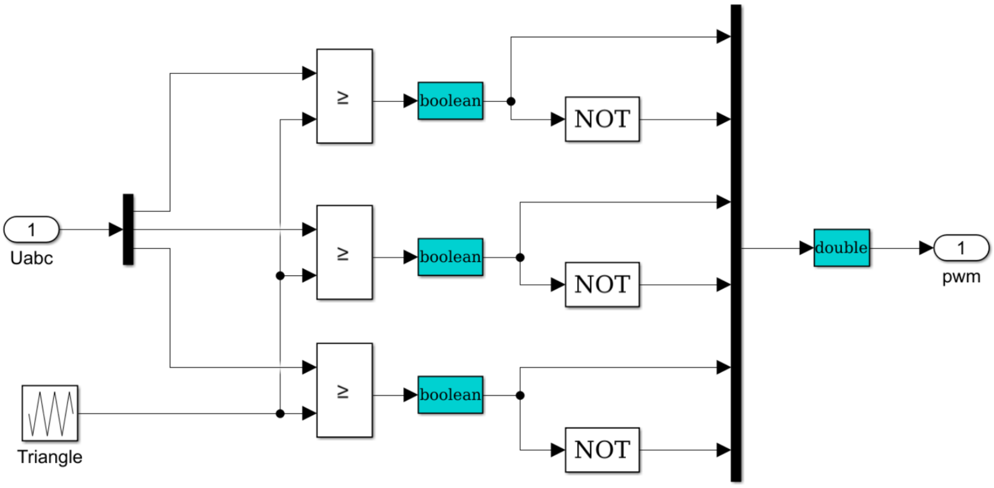

Figure A.1: SPWM simulation model in MATLAB

The SVPWM simulation model is built according to the principle of the SVPWM algorithm for a 2-level inverter as set out in Figure A.2. In this figure, the main steps for the SVPWM algorithm are labelled in the bottom of Matlab Simulink blocks, which select the sector, calculate the switching time of the two adjacent vectors and synthesise the three-phase PWM signal.

The SVPWM method is then applied to the 2-level three-phase grid-connected system. The simulation model is shown in Figure A.2. In the following, some significant steps of the SVPWM simulation models are shown in the selecting sector model Figure A.3, the calculation of the switching time of the two adjacent vectors in Figure A.4 and Figure A.5 and the synthesis of the signal wave in Figure A.6 and Figure A.7.

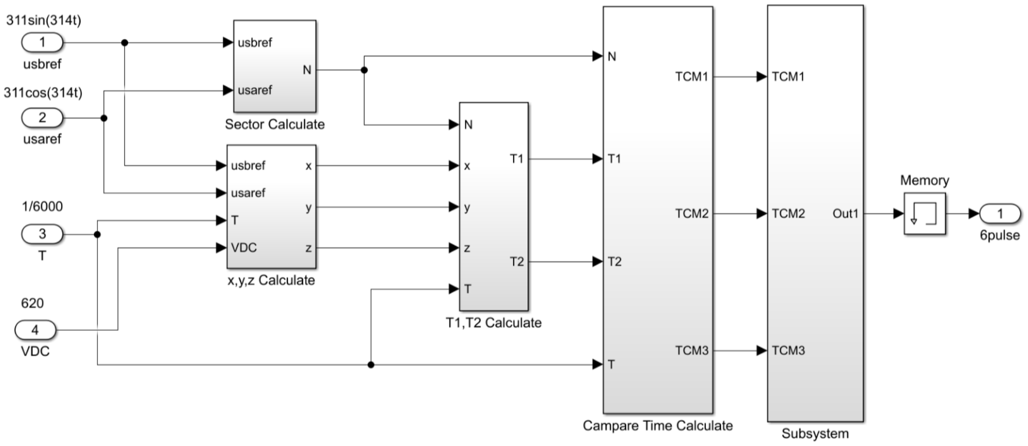

Figure A.2: SVPWM simulation model in MATLAB

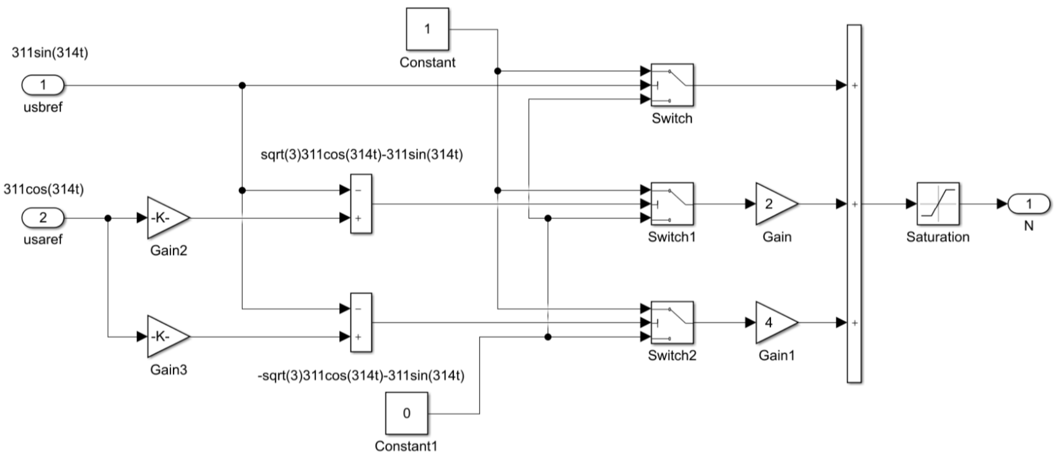

Figure A.3: Select sector model

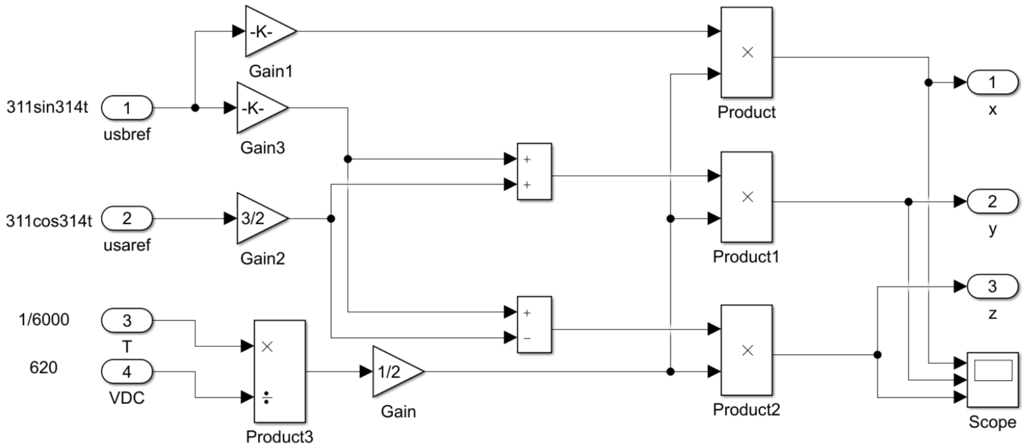

Figure A.4: X, Y, Z calculation model

Figure A.8 shows the SVPWM simulation model in a 3-level grid-connected inverter system. Although the principle is the same, the detail modulation method is more complicated.

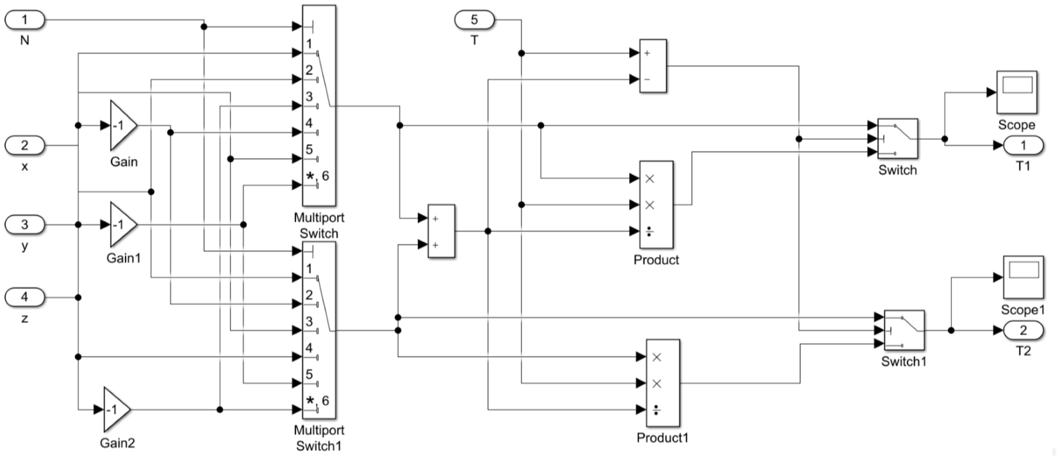

Figure A.5: T_1 and T_2 calculation model

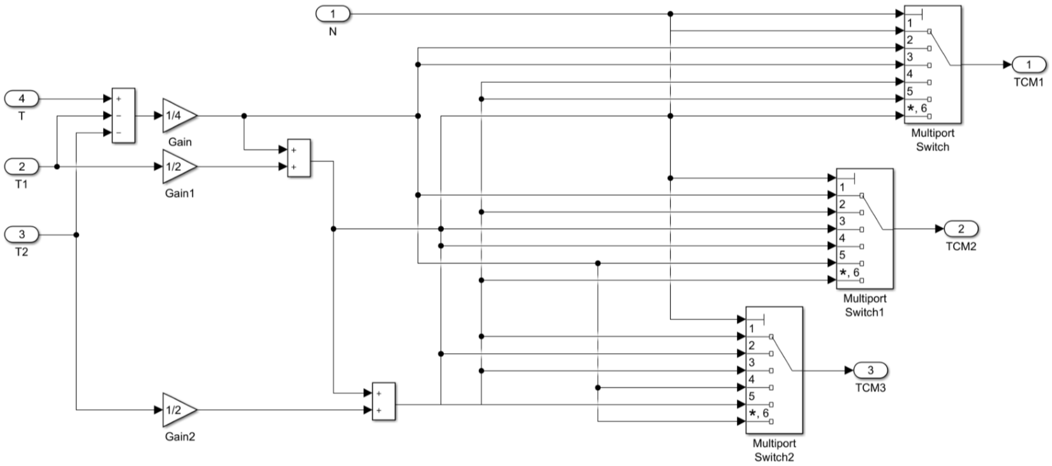

Figure A.6: Comparing time calculation model

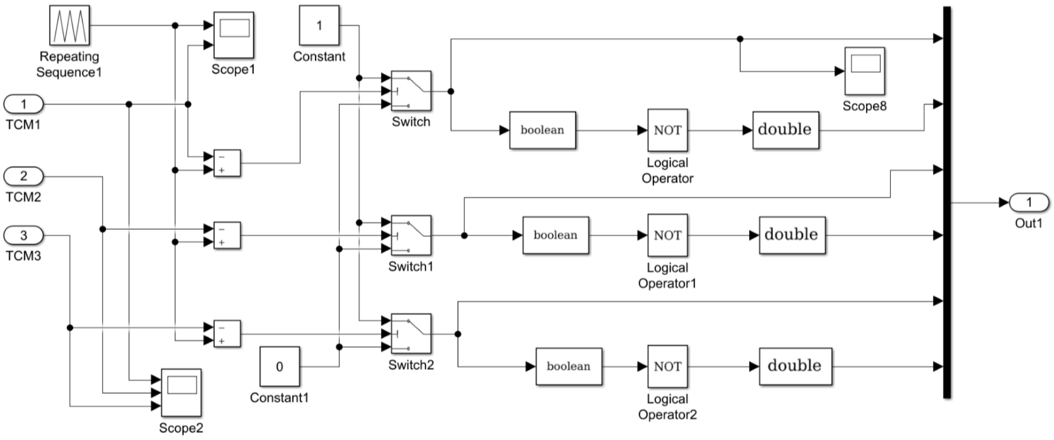

Figure A.7: The synthesis of the signal wave

Figure A.9 shows the primary simulation model of MPC for the NPC inverters.

Figure A.10 shows the model of the MPC controller.

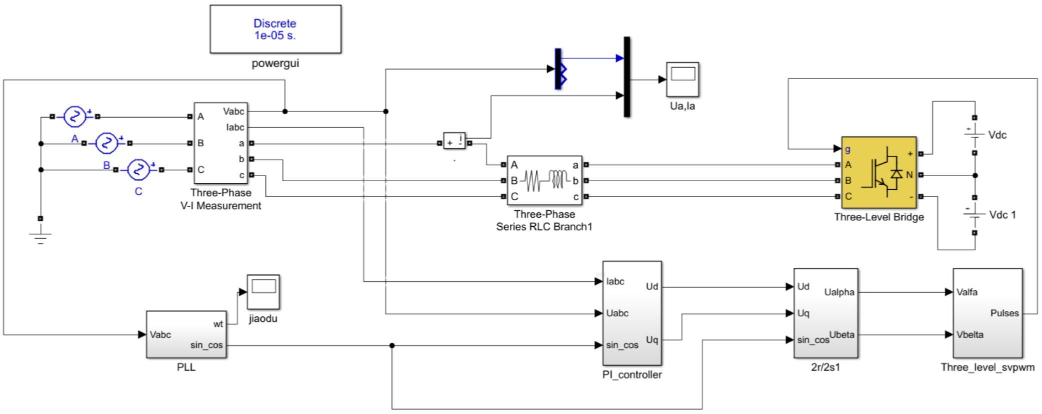

Figure A.8: The SVPWM simulation model in 3-level grid-connected inverters

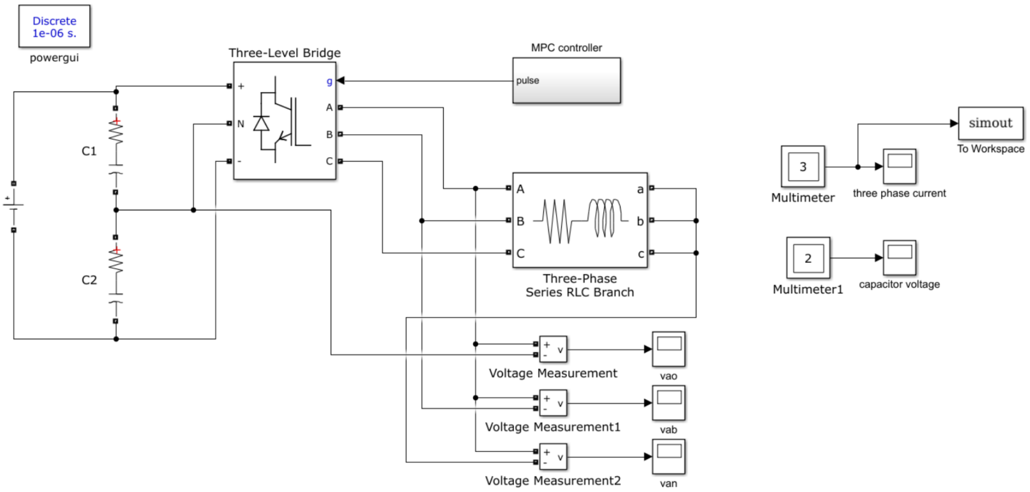

Figure A.9: The main simulation model of the MPC

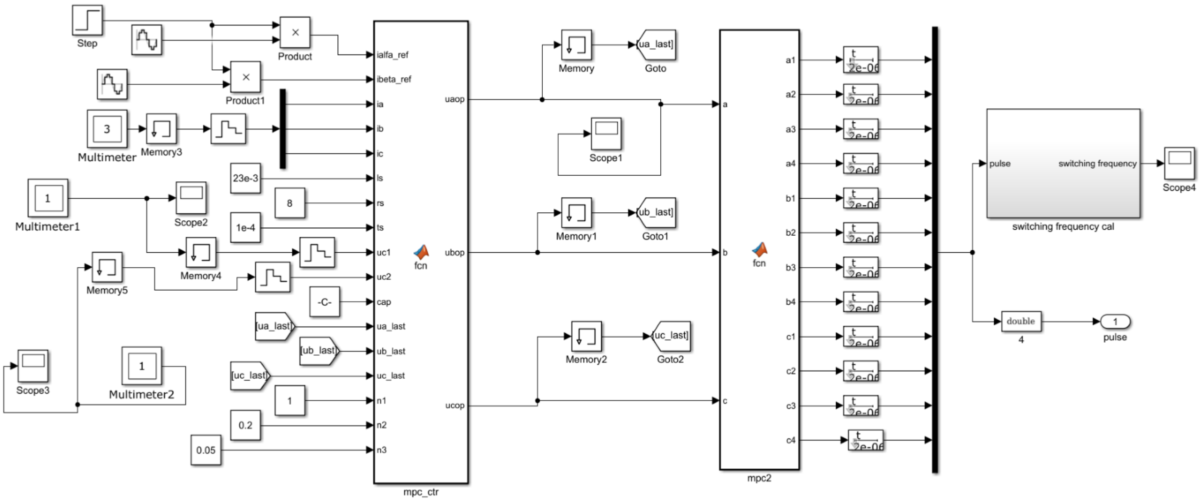

Figure A.10: The model of the MPC controller

Figure A.11 shows the main model of PI control for the NPC inverters.

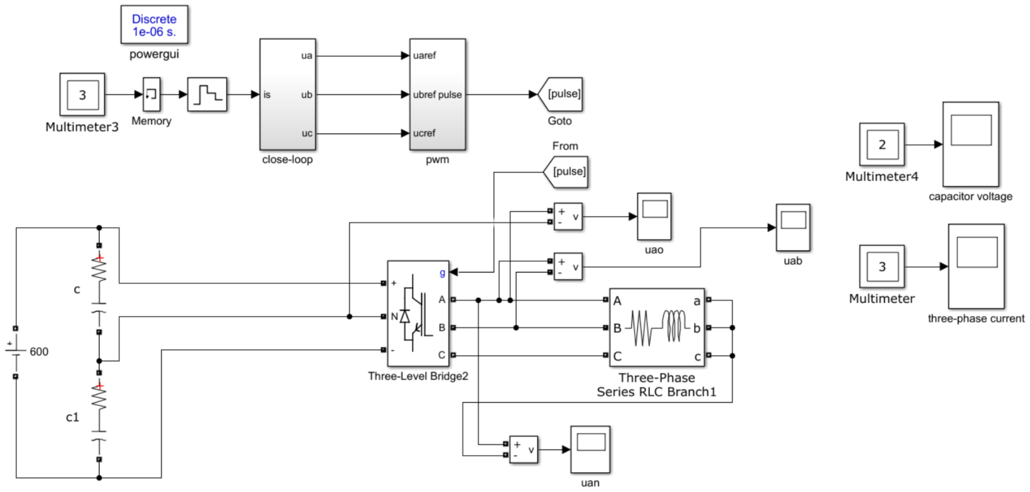

Figure A.11: The main model of the PI control

Figure A.12 shows the model of the PI controller.

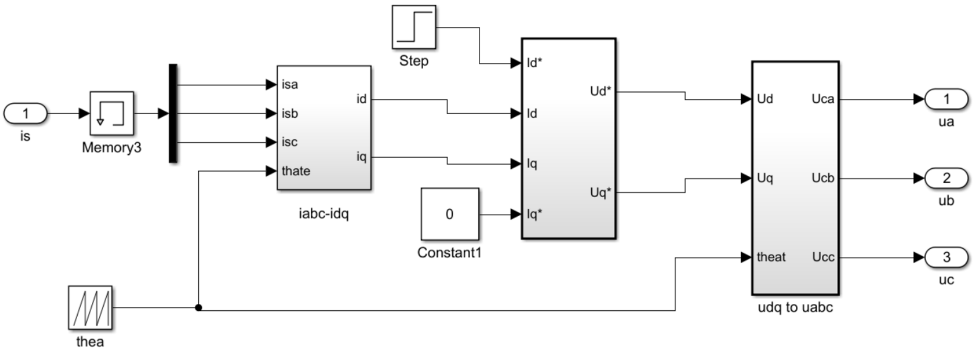

Figure A.12: The model of the PI controller

Figure A.13 shows the model of the NPC inverters.

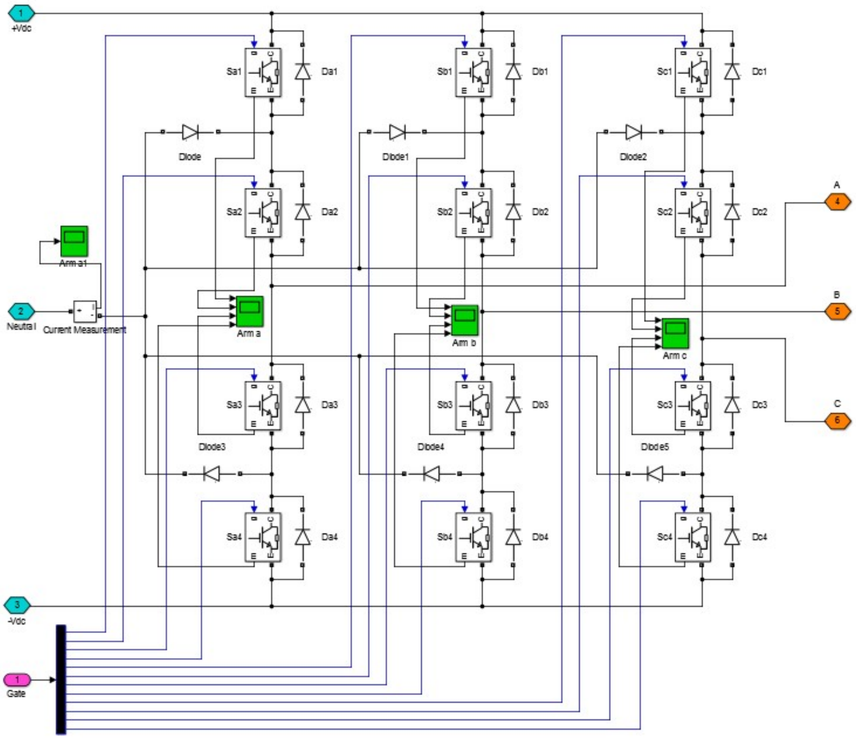

Figure A.13: The model of the NPC inverters

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