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Plasma Enhanced Chemical Vapour Deposited Silicon Carbide For Back-End-Of-Line Resistive Memory

by

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MEng

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Abstract

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Resistive random-access memory (RRAM) are one of the most promising candidates for the next generation of memory technologies. Silicon Carbide-based memories are investigated in this thesis due to its heavy use as a back-end-of-the-line (BEOL) dielectric. This means that such devices could be fabricated directly on top of transistors, reducing the interconnect delay, and would be compatible with current commercial fabrication processes. This makes integration easier and cost effective. Our group has previoulsy shown that Silicon Carbide-based RRAM show zero degradation up to 2MRad of γ irradiation. However, the fabrication process used yields devices with a low cyclability of around 10 switching cycles. Therefore, this thesis focuses on developing a new fabrication process that increases the performance and reliability of such memory cells. This is so that we can be assured that any measured failures in future life-time testing is due to the applied ion bombardment, instead of the inherent failures in the electronic properties of such a device.

In this work I have developed a plasma enhanced chemical vapour deposition (PECVD) based SiC resistive memory which shows both volatile and non-volatile switching. The resistive memory devices showed reproducible and reliable switching across an entire 4-inch wafer. Both the On and Off state of the W/SiC/Cu devices were found to be dominated by Schottky emission with a change in the barrier height, which can be controlled with the applied voltage and number of sweeps. The volatile behaviour was characterised using varying pulse parameters and analyses of the change in conductance and the On state decay with time. The measured characteristics show emulation of short-term potentiation (STP) which takes place between the synapse of neurons. This work is the first to have a detailed analysis of STP in SiC-based RRAM memory cell. STP is understood to be key in information processing in the brain and this emulation can be used for brain-inspired computing. By varying the interval between 5ms and 30ms, we can further tune the peak conductance of our resistive memory cell and

show that our decay between the input stimuli is in the order of milliseconds. The control in the conductance state is thought to be due to the ion migration caused by the applied pulses and the spontaneous diffusion of the conductive filament. It was also found that applying multiple STP potentiation and decay cycles showed that the overall peak conductance increased with cycle number. Therefore, taking a single conductance point of 181μS it was found that this specified conductance state could be re-learned exponentially quicker with each cycle, which has been seen in other neuromorphic based devices. The simple BEOL-compatible fabrication process and their ability to emulate STP functions in the brain make these memory cells a perfect candidate for embedded neuromorphic computing.

I developed Si/SiC bilayer memory cells deposited by PECVD with 50nm of amorphous-Si layer followed by a silicon rich 50nm of amorphous-SiC. These W/Si/SiC/Cu devices showed a similar switching mechanism to previously reported sputtered SiC-based dielectrics with the off state dominated by Schottky emission and the On state by Ohmic conduction. The Set and Reset voltages were measured to be around 2.1V and -0.8V respectively, with an average resistive ratio of 10^3 across 100 cycles. Using an external compliance current circuit, a pulsed measurement scheme was implemented to analyse the long-term endurance capabilities. Using a 200μs pulse, it is possible to Set and Reset the memory cells at 4V and -3V over a billion times. Analysing the average resistance and deviation across this billion cycle range, it was found that the memory cells showed no degradation and instead improved with cycle number. The endurance and stability is one of the highest recorded endurance for conductive bridge based resistive memory (CBRAM) and outperforms current commercially available RRAM devices targeted specifically for radiation hardened applications. These samples were also re-fabricated to determine if the devices were reproducible. These devices showed near identical inherent characteristics, displaying the reproducible fabrication process that was developed. This work presents the potential for a scalable and BEOL compatible embedded memory solution.

Typically, high performance memory is fabricated in a Crosspoint array. In this work I have investigated the fabrication process flow for Crosspoint structures for the optimum device characteristics. I have also fabricated the first recorded SiC-based Crosspoint structure. By embedding cells using e-beam lithography and a SiO_2 isolation layer, the endurance of the cells increased from 12 to over 100 cycles. Both devices exhibited high resistive ratio of around 10^6, in keeping with previous SiC-based resistive memory. By analysing the read and write schemes across a 2x2 array, the sneakpath was investigated which showed the potential issues that can arise in the form of bit errors. This demonstrates how the high endurance memory cells that are developed require the use of a selector device when combined into a Crosspoint structure.

Contents

Declaration of Authorship

I declare that this thesis and the work presented in it is my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. None of this work has been published before submission

Signed:..... Date:.....

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List of Publications

Peer reviewed journal publications

J.Fan, **O**.**Kapur**, R. Huang, S. W. King, C. H. de Groot, L. Jiang (2018) *"Back-End-Of-The-Line a-SiO$_x$C$_y$ Dielectrics for Resistive Memory"*, American Institute of Physics Advances, 8(9), 095215

O.**Kapur**, J.Fan, J.Reynolds, Yisong Han, Richard Beanland, Ruomeng Huang, Liudi Jiang, C.H. Kees de Groot *"High endurance amorphous SiC resistive memory by chemical vapour deposition"* (submitted to IEEE Transactions on Electron Devices)

O.**Kapur**, Dongkai Guo, Jamie Reynolds, Yisong Han, Richard Beanland, Ruomeng Huang, Liudi Jiang, C.H. Kees de Groot *"Analysis of Short-Term Potentiation in Schottky Barrier-Switching Cu/SiC/W"* (in preparation)

Conference Attendance

O.**Kapur**, J. Fan, L. Jiang, C.H. de Groot (2018) *"Passive Resistive Random Access Memory Matrices Using Amorphous Silicon Carbide"*, Micro and Nano Engineering (MNE) Copenhagen, Denmark.

O.**Kapur**, J. Fan, L. Jiang, C.H. de Groot (2018) *"Passive Amorphous Silicon Carbide Resistive Random Access Memory Arrays"*, Non-Volatile Memory Symposium (NVMTS) Sendai, Japan.

O.**Kapur**, J. Fan, L. Jiang, C.H. de Groot (2018) *"Passive Resistive Random Access Memory Matrices Using Amorphous Silicon Carbide"* Defence and Security Doctoral Symposium (DSDS) Swindon, UK.

Chapter 1

Introduction

Non-volatile memory can retain bit states when power to the system is taken away. Such technologies like FLASH has seen widespread adoption due to their continuously increasing capacity and low cost [1]. However, current FLASH devices cannot be reliably used in radiation harsh environments with data loss showing to occur around 10krad to 100krad of exposure [2]. Reliable radiation-hardened memory cells are important for a wide range of applications, for example, defence and space exploration.

There are several candidates that can be used for the next generation of non-volatile memory [3]. The most promising of these candidates are Resistive Random-Access Memory (RRAM) cells. This is because resistive memory can be fabricated using back-end of the line (BEOL) materials. This means that such memory could be fabricated directly on top of transistors, reducing the interconnect delay, and would be compatible with current commercial fabrication processes. Our group has previously shown that silicon carbide-based resistive random access memory (ReRAM) cells have shown large resistive ratios of up to 10^{10} and successful data retention at radiation doses up to 2MRad [4,5]. However, these radiation tolerant devices suffer from poor performance with an extremely low cyclability, being able to switch on/off 10 times. For reliable and secure data storage in harsh environments, data must be able to be written and stored continuously without the fear of any loss of information. The improvement in switching performance is the focus of this thesis. This work will look at the fabrication of PECVD memory cells which have the ability to be written and read continuously without fear of losing information. The endurance and stability of resistive memory will be analysed in depth.

Furthermore, will also discuss the use of a single thin film, that can exhibit both volatile and non-volatile behaviour. Such behaviour is useful for Neuromorphic computing, which is inspired by the highly efficient parallel processing of the brain. By using resistive memory to emulate synapse functions it is possible to create highly dense neural

networks. This thesis focuses on the analysis of Short-term potentiation (STP). Understanding STP with a given dielectric is key aspect in creating a neuromorphic computing system and is the first in-depth analysis for SiC-based devices.

The final part of this project will look at the fabrication of Crosspoint structures. Crosspoint structures are the method in which multiple bits of non-volatile memory are connected together, to produce highly dense arrays. These Crosspoint structures suffer from parasitic currents, known as sneakpath, which reduce the possible size of the arrays. This work looks at the optimum fabrication process and the effects of different Crosspoint structures on the electrical characteristics of RRAM memory cells. There is also a detailed analysis of sneakpath to To do this there needs to be a fabrication process that would allow for 100nm Crosspoint structures and an analysis of the current sneakpath problem.

The entire objectives of this project are broken down in the section below.

Objectives

- Development and characterisation of Silicon Carbide based resistive memory.
  - Develop a fabrication process that will enable the emulation of synapse functions
  - Characterise analogue switching resistive measurements using DC switching
  - Characterise synapse functions using precise pulsing for both the strengthening and weakening of connections between neurons.
- Development and characterisation of Bilayer Silicon Carbide based resistive memory.
  - Develop a fabrication process flow that can produce devices with reliable switching characteristics.
  - A detailed comparison of IV characteristics using both DC and pulsed switching
- Fabrication and Characterisation of the first SiC based Crosspoint Structure.
  - Fabricate Crosspoint structures with 100nm devices
  - Analyse Sneakpath in a Crosspoint structure
  - Fabricate a 1kb SiC based Crosspoint chip

Chapter 2

Resistive Memory Background and Literature Review

This chapter will present the general operation of resistive memory. This is followed by an in-depth literature review of Silicon Carbide (SiC) based resistive memory. After this details on the operation of bilayer memory, neuromorphic computing and the effects of radiation harsh environments on resistive memory will be presented.

2.1 Resistive Random Access Memory

There are several candidates that can be used for the next generation of non-volatile memory [3]. Phase Change Memory (PCM) utilise the change in resistivity that occurs when transitioning between an amorphous and crystalline phase [6]. Ferroelectric tunnelling junction (FTJ) and Spin-Transfer Torque Magnetic RAM (STT-MRAM) have also been investigated and utilise the change in the tunnelling current depending on the direction of the ferroelectric or the spin polarisation, which can be changed through an applied voltage [7, 8]. However, the most promising of these candidates are Resistive Random-Access Memory (ReRAM) cells. This is because resistive memory can be fabricated using back-end of the line (BEOL) materials. This means that such memory could be fabricated directly on top of transistors, reducing the interconnect delay, and would be compatible with current commercial fabrication processes. This makes integration easier and cost effective. This is in contrast to memories such as phase-change, which require rare-earth elements such as tellurium. Resistive memory have also been shown to be a good candidate for radiation hard memory [9]. Its radiation hardness can be attributed to the use of a ruptured/formed conductive bridge to store information compared to charges in a floating gate that is currently employed in commercially available non-volatile memory technologies [10].

Resistive switching is the characteristic that enables a device with certain materials to change its electrical resistance when exposed to a voltage stress [11]. Studies on this phenomenon have been reported as far back as the early 1960s [12]. The differing resistances can be used to represent logic states, making these devices useful for information storage and computation. A device in the High Resistance State (HRS) usually represents a bit 0. To store a bit 1 the device must be in a Low Resistance State (LRS). Some materials have been found to achieve multiple resistances states, which could be used for processing applications [13–18].

These resistive switching devices possess a similar metal-insulator-metal (MIM) structure to a capacitor. This design allows for the use of simple fabrication techniques to create highly dense memory arrays that can achieve $4F^2/n$ effective area, where F is the feature size and n is the number of stacking layers [19,20]. This high density allows for it to be a good competitor against current commercially available alternatives.

Many different electrode and dielectric materials have been investigated, which can significantly alter the resistive switching mechanisms and I-V characteristics. The most common electrodes that have been investigated include Pt, Ag, Cu, TiN and W [11,18, 21–24]. These metals can be split in terms of their use as an active or inert electrode [25]. An inert metal acts as a standard electrode while an active electrode allows the diffusion or drift of ions to the dielectric which alters the resistance state.

A large range of dielectric materials has also been investigated including chalcogenides, perovskites and 2D materials [26,27]. Research has focused on tuning these materials to achieve a highly efficient performance. Some devices even utilise multiple stacked layers between the electrodes to achieve their desired characteristics [28,29]. The most promising combination of materials are based on a TaO_x bilayer dielectrics with Pt electrodes. These devices have shown unmatched performance with 10ns switching times, greater than 10^{12} endurance and retention of 10 years at 85^oC [30]. This will be further discussed in Chapter 5.

Depending upon the materials chosen for both the electrodes and the dielectric the resistive switching mechanism can be classed into either an interfacial or filamentary device. The latter has a single filament in its On state. The former is attributed to the change in the Schottky barrier height, caused by the accumulation and depletion of carriers at the interface between the electrode and the dielectric [31–33].

A filamentary device, also known as Conductive Bridge Resistive Random Access Memory (CBRAM), utilises the formation and rupture of a conductive bridge through the movement of ions. The device has two resistance states depending upon whether the top and bottom electrodes are connected or disconnected by this filament. This means that the resistance of the cell is not dependent upon the area of the capacitor, but instead, the area of the filament [34]. This filament formation is separated by either cation or anion migration. Anion based CBRAM is referred to as Valence Change Memory

(VCM) and it involves the migration of oxygen ions to create a conductive pathway. Cation migration utilises the migration of ions donated from the top electrode and is known as Electrochemical Metallisation (ECM) [35]. This donation of ions requires the use of an active electrode, described above, and a bottom inert electrode. On the other hand, VCM devices require the use of inert electrodes as the anions are donated from the dielectric material.

To understand the movement of ions in a CBRAM device we will consider an ECM mechanism with Cu as an active electrode. In its initial state, ECM cells are in the HRS and are usually referred to as being in a Pristine state, as the conductive bridge requires forming. This formation utilises the ion migration described above and requires a voltage bias across the cell. This voltage causes the active electrode to undergo oxidation resulting in mobile cations that can be used to form the conductive bridge. This oxidation is presented in equation 2.1.

$$Cu \rightarrow Cu^{+} + e^{-} \tag{2.1}$$

Through the presence of a high electric field, due to the applied voltage bias, the cations drift through the solid electrolyte forming a bridge towards the inert electrode [36]. Through electro-crystallisation the Cu ions are reduced on the surface of the inert electrode as shown by equation 2.2.

$$Cu^{+} + e^{-} \rightarrow Cu \tag{2.2}$$

Once the two metal plates have been connected together the resistance of the cell is reduced and now is dominated by Ohmic conduction. This is known as the Formation of a cell and often requires a higher voltage than is used for subsequent cycles. The lower voltage in the subsequent cycles is due to the conductive bridge being only partially ruptured when moving from the Formation to the HRS. Therefore the conductive bridge requires less overall energy to reform the bridge. This process is also known as a partial dielectric breakdown due to its reversible nature and use of a programming current (I_{prog}). I_{prog} is used to prevent a hard dielectric breakdown which makes the subsequent rupture of the filament impossible. This hard dielectric breakdown is a permanent change.

ReRAM devices can also have two operating modes known, depending on the polarity used to reset the device, known as Unipolar and Bipolar switching. Each mode is defined by the method in which the conductive bridge is partially ruptured causing a change in resistance from a LRS to a HRS, as shown in figure 2.1. Operating in a Unipolar mode, the Reset and Set voltages are dependent on the current applied to the cell and not on the voltage polarity [34,37]. Let us consider a device that is currently in

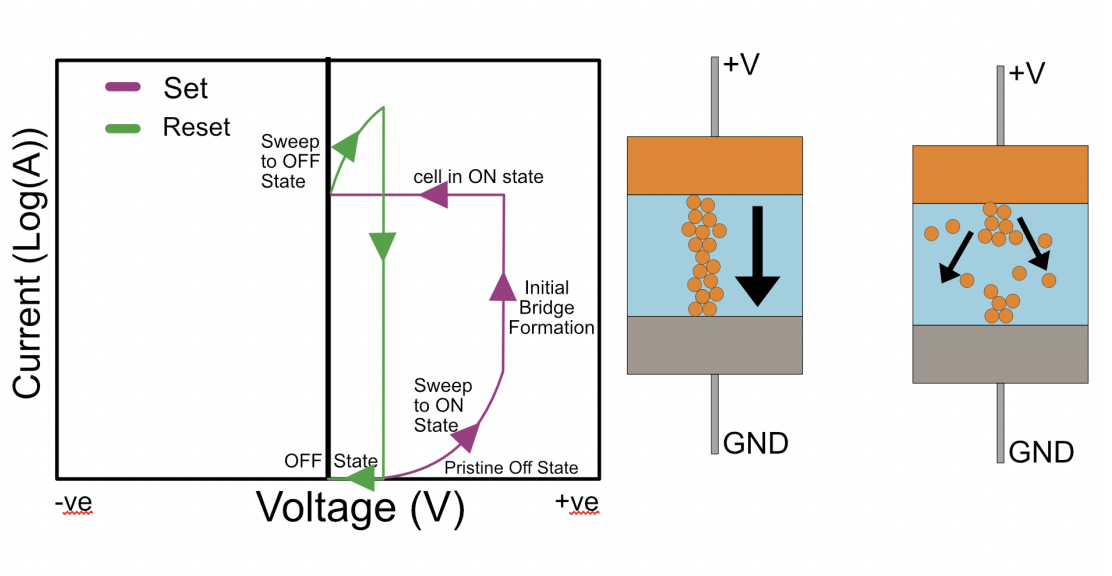
the HRS. If we were to form the conductive bridge, described above, using a positive voltage bias the state of the cell would alter from a HRS to a LRS. The reset for unipolar switching is dominated by a thermal chemical mechanism (TCM). To rupture the filament, a voltage with the same polarity is applied without I_{prog}. As the current passes the original I_{prog}, the conductive bridge increases in temperature, due to Joule heating. This rise in temperature within the conductive bridge allows for a thermally-activated Reset though the partial breakdown of the conductive bridge. This breakdown is said to occur in a diffuse manner, as unlike the formation process the ions do not electromigrate [38]. This diffusive rupture of the filament forces the memory cell back into a HRS. Even though this process does not require an I_{prog}, it is self-limiting due to the rupture of the filament.

The diffusive rupture of the filament is not completely destroyed during this reset process. This is because the whole conductive bridge does not need to be ruptured to switch the cell into a HRS. This means that any subsequent Set voltages applied to the cell would be lower than the initial formation voltage, keeping the overall power consumption lower.

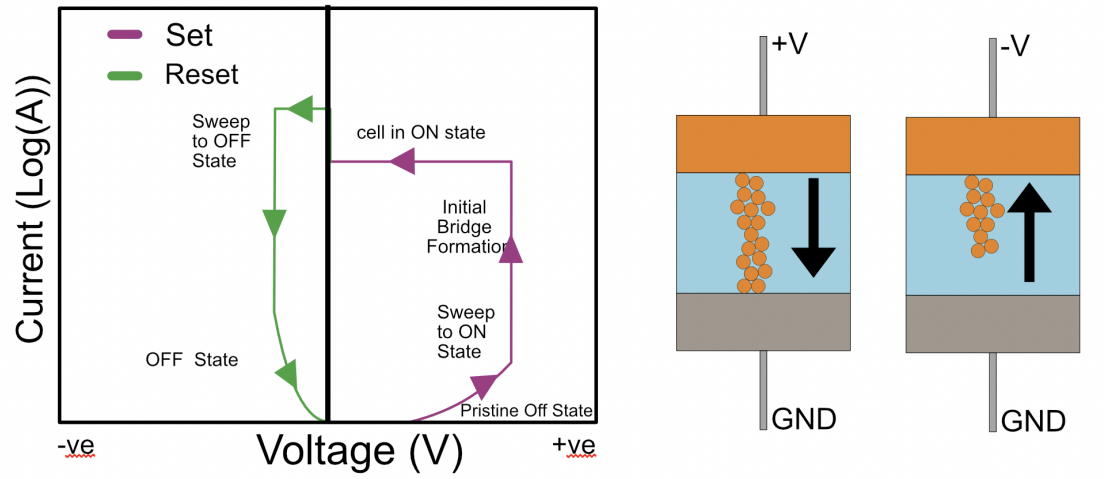
The Bipolar switching mechanism differs from Unipolar in that it is dependent upon the applied polarity between the Set and Reset voltages [39]. Rupturing of the conductive bridge occurs from the electro-migration of ions away from the inert metal plate instead of thermal diffusion. In this method, the opposite voltage polarity is needed to reverse the ion migration that initially formed the conductive bridge. Therefore, if we were to initially use a positive voltage to form the conductive bridge a negative voltage would be required to rupture the filament in a Bipolar switch, to switch the device from a LRS to a HRS. This method enables a lower power operation than Unipolar switching. This method also maintains the partial rupture of the filament meaning that Set voltages after the initial formation are kept lower.

With both of these switching mechanisms in mind, it must be mentioned that a material can exhibit both Unipolar and Bipolar switching. This is known as nonpolar switching and enables the cell to diversify its use in terms of its peripheral circuits [40, 41].

Operating these devices using a DC voltage is extremely slow and requires a large amount of energy when cycling through states. This also provides a large amount of stress to the device which can cause premature failure [42]. Alternatively, short pulses can provide a fast and low-stress method of measuring resistive switching properties. This can also help measure large cycle numbers with devices with high endurance and using this method is also closer to real-world applications. Therefore, investigations in the scalability of these devices can be conducted by reviewing the optimum characteristics of a memory device. These requirements can be broken down into 4 separate categories [37].



(A)



(B)

FIGURE 2.1: Representation of the two operating modes of resistive switching device (A) Unipolar switching (i) I-V graph showing the same voltage polarity used without an I_{prog} (ii) Thermally activated diffusive movement of ions which ruptures the filament between the metal electrodes. (B) Bipolar switching (i) I-V graph showing the same voltage polarity being used for the Set and Reset process. (ii) Drift movement through electro-migration of ions which ruptures the filament.

- The voltages required for the read and write operation. The voltage required to turn the device On/Off should be lower than 5V and allow for overall low power consumption.
- The resistive ratio, which describes the difference in the On/Off current. A large resistive ratio is preferable as it increases the sense margin which makes the potential for reading errors lower.
- The endurance of a memory device is the estimated number of On/Off cycles that can be achieved before a breakdown occurs and the memory can no longer change state. This failure mechanism can be estimated with cycle number by looking at the change in the resistive ratio over cycle number. As the device starts to fail this ratio should reduce. This endurance should be more than 10^7 cycles to compete with Flash.
- Retention of the device measures the stability of a device to hold its bit state. The requirement for a non-volatile memory device is the ability to hold its state for 10 years at 85^oC .

These requirements will be investigated in this thesis to accurately determine the potential of the operation of the device for use as a next-generation technology. Notable resistive memories that achieve these requirements are presented in table 2.1. The Ta_2O_5/TaO_2 has shown the highest ever endurance for resistive memory. SiO_2 is a valence change memory that shows a large resistive ratio between its on and off state, with a much lower endurance. HfO_x shows a stable resistive memory with its ability to withstand 150^{o}C for 10 years. The sputtered SiC shows the largest endurance recorded for SiC (other than this this thesis). The PECVD Si(O)C is a electro-chemical metallization memory that shows one of the highest resistive ratios recorded.

TABLE 2.1: Varying dielectrics that have been investigated for resistive switching devices and their associated ratio, endurance and retention characteristics

Dielectric	Resistance Ratio	Endurance	Retention
Ta_2O_5/TaO_2 [30]	$\sim$10	10^{12}	10 years at 85^{o}C
SiO_2 [43]	10^7	10^5	6.8 years at RT
HfO_x [44]	$\sim$10	10^6	10 years at 150^{o}C
Sputtered SiC [45]	10^2	10^5	10 years at 85^{o}C
PECVD Si(O)C [4]	10^{10}	5	10^5 at RT

2.2 SiC-based Resistive Memory Performance

Silicon carbide (SiC) is a material with a low dielectric constant that has been widely investigated for different semiconductor applications, due to its wide bandgap, high

operational temperatures, as well as its mechanical strength, higher chemical and radiation resistance compared to Silicon [46]. SiC is also a promising candidate for Resistive Random Access Memory, due to it already being used in the back-end-of-the-line (BEOL) processes as an interconnect dielectric because it acts as a high diffusive barrier to Cu^+ ions [47]. Utilising BEOL materials such as SiC mean that the fabrication of these cells would be simple and cost-effective, but would also mean the potential for ReRAM to be fabricated directly on top of transistors, reducing the interconnect delay. Therefore, a significant research into BEOL resistive switching materials have been conducted [48–50]. Below is a discussion on the different SiC-based resistive memory devices that have been investigated and are separated in terms of their deposition techniques.

Sputtered Amorphous SiC

Initial investigations within our group were conducted on Cu/SiC/Au ReRAM devices. This work shows that 40nm SiC-based memory can achieve nonpolar characteristics, as shown in figure 2.2 [41]. This means that the device exhibit both unipolar and bipolar switching. Bipolar switching is controlled through the reversal of electromigration be changing the applied polarity of the voltage bias. Unipolar switching is achieved by increasing the applied current compliance and allowing for the thermal rupture of the filament to take place. It was shown that switching was possible with both a positive or a negative Set for either mechanism. This due to the ion migration of both the Cu and Au, depending upon polarity. This was confirmed through extracting the temperature coefficient of the filaments for both mechanisms. These devices were estimated to able to retain their bit state for over 10 years at 85^oC with no loss to information at a resistive ratio of 10^7. Further investigation also showed that these devices could achieve some of the highest resistive ratios known to ReRAM, at 10^9 between the on and off state [51]. These extremely high resistive ratios are advantageous as it reduces the chances of reading errors and is thought to originate from the presence of a Schottky barrier between the Cu and SiC layers.

The conduction mechanisms of the On and Off state was analysed, with the former dominated by Ohmic conduction, due to its linear I-V nature. The latter is dominated by Schottky emission and its relationship was found through the Schottky emission equation which can be shown by equation 2.3, where I is the current, A is the area, T is the temperature, A^* is the Richardson's constant, q is the charge of one electron, k is the Boltzmann constant, E i the electric field, ϵ_I is the permittivity and ϕ_B is the energy barrier height. A^* is equal to $4\pi mek^2/h^3$, where m is the mass of electron, e is elementary charge, and h is Plank's constant. It should be noted that this constant is multiplied by a correction factor which depends on the material.

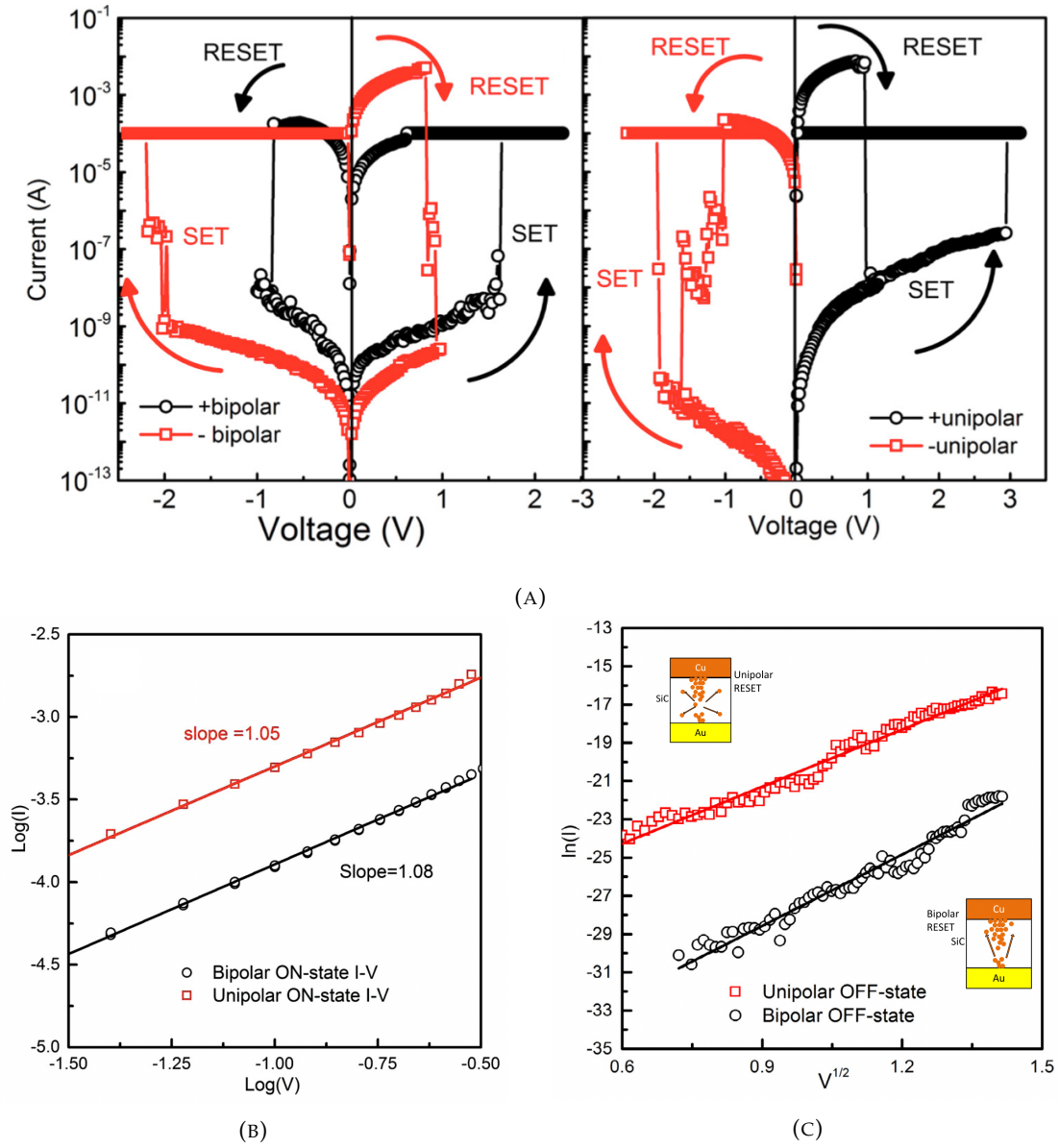


FIGURE 2.2: Characteristics of sputtered SiC resistive memory (A) nonpolar resistive switching characteristics, with the device being able to Reset using both the same and opposite voltage polarity [41]. (B) Log(I)-Log(V) graph showing that Ohmic conduction is the dominant mechanism in the LRS [51] (C) ln(I)-$\sqrt{V}$ graph showing that Schottky emission is the dominant mechanism in the HRS [51]

$$I = AA^*T^2exp[q(\phi_B - \frac{\sqrt{\frac{qE_I}{4\pi\epsilon_I}}}{kT})] \tag{2.3}$$

The above equation can be rearranged to form equation 2.4, where V is the voltage and d is the distance between the top and bottom electrode in the pristine state, or the distance between the filament and the bottom electrode at the subsequent state. This equation can can be used to see if the off-state fits a linear curve when plotting ln(I/AA^*T^2)-$\sqrt{V}$ graph. This is expected as the SiC dielectric in the device is also widely used for Schottky diode applications [52].

$$ln(\frac{I}{AA^*T^2}) = \frac{q\sqrt{\frac{q}{4\pi\epsilon_i d}}}{kT}\sqrt{V} - \frac{q\phi_B}{kT} \tag{2.4}$$

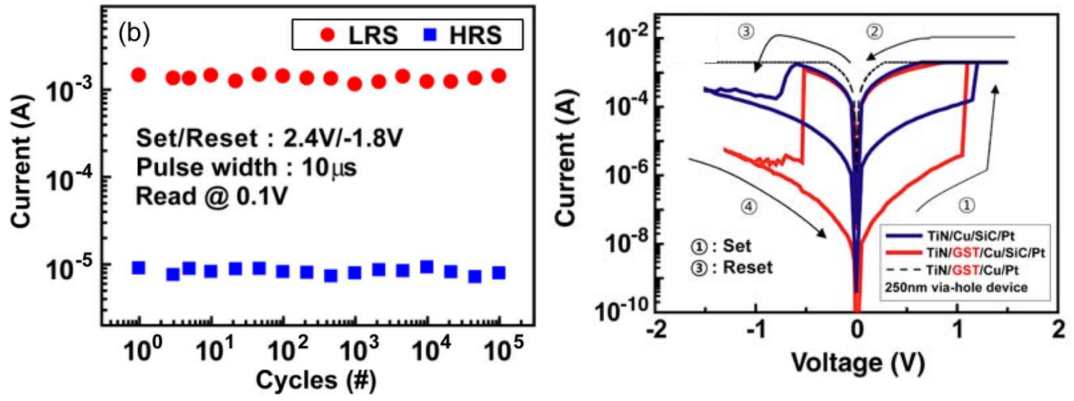
Characteristics of these devices were also investigated with an alteration of the inert electrode. By using W instead of Au it was found that the Off state resistance could be further increased [18]. This is thought to be due to a possible Oxide barrier that could have formed on the W/a-SiC surface, due to its high affinity to O_2 than Au. This not only produces ultra-high ratios but can also enable low power use.

Both the Au and W electrodes devices were also shown to have multi-level states that were controlled by the I_{prog} in the Set operation [53]. By varying the applied current compliance during the Set process, the LRS can be controlled between 10MΩ and 1KΩ. The diameter of the filament was extracted to be around 1nm for the W and 4nm for the Au electrode. The lack of area dependency in the On state confirmed the filamentary nature of these devices.

Further analysis of the Cu/a-SiC/Au device show extreme radiation-hardened characteristics, with no changes to the resistive ratio and conduction mechanisms against up to 2MRad of γ-radiation [5]. It indicates that this form of memory is well suited for such extreme environments and that the radiation-sensitive areas within such a memory system would be the peripheral circuitry.

Looking at the varying thicknesses of sputtered SiC dielectrics, between 50 and 100nm, it has been shown that an increase in the thickness increases the formation voltage [54]. This is due to the increase in the distance required, for the initial formation of the conductive bridge. Pt, W and Ag were investigated as top electrodes, with the bottom electrode being Au, however, these devices suffered from extremely low endurance of fewer than 60 cycles.

Currently the most promising sputtered SiC-based ReRAM in literature is based on 40nm of sputtered SiC with an active Cu and an inert Pt electrode, as shown in Figure 2.3a. These devices on their own have shown 10^5 switching cycles with two orders of



(A) (B)

FIGURE 2.3: (A) Largest endurance measured of SiC-based resistive memory [45] (B) I-V graph showing the increase in resistive ratio and reduction in the switching voltages by adding a $Ge_2Sb_2Te_5$ thermal barrier [55]

magnitude On/Off ratio [45]. By adding a $Ge_2Sb_2Te_5$ thermal barrier layer the switching voltages were decreased, as shown in figure 2.3b. These devices also showed reduced switching times from 10μs to 500ns [55]. As SiC is usually seen as a slow form of memory for ReRAM devices, this opens the possibility to be able to significantly reduce the switching times.

Chemical Vapour deposition of SiC, SiOC and SiCN

Other deposition method have been investigated for SiCN using both PECVD and ALD. 10nm of SiCN sandwiched between Indium Tin Oxide (ITO) and AZO has shown switching characteristics with resistive ratios larger than 10^3 for 10^6 cycles [56]. These devices exhibited ion migration as its switching control mechanism, with confirmation from TEM images. A similar dielectric with Cu/Ta as the top electrode show resistive switching, however, with an extremely poor endurance with DC switching failing before 200 cycles [57]. With the addition of an Al_2O_3 thin film in between the dielectric, the endurance is enhanced and the cell is able to switch up to 1.6x10^4 times.

15nm of SiC_xN_y deposited through plasma-enhanced atomic layer deposition (PEALD) at 30W provided resistive switching characteristics with a ratio of 2 orders of magnitude for 30 cycles [58]. Depositing the same thin film at 50W, however, provided volatile threshold switching. This type of switching can be used for a device known as a selector. Selectors will be discussed in depth in chapter 6, but it is important to note that SiC-based devices can exhibit both volatile and non-volatile behaviour.

Previous work has been conducted in our group, in collaboration with Intel [4]. PECVD SiO_xC_y films were provided by Intel and the top electrodes were patterned and deposited in Southampton. I contributed to the measurement of the resistive switching

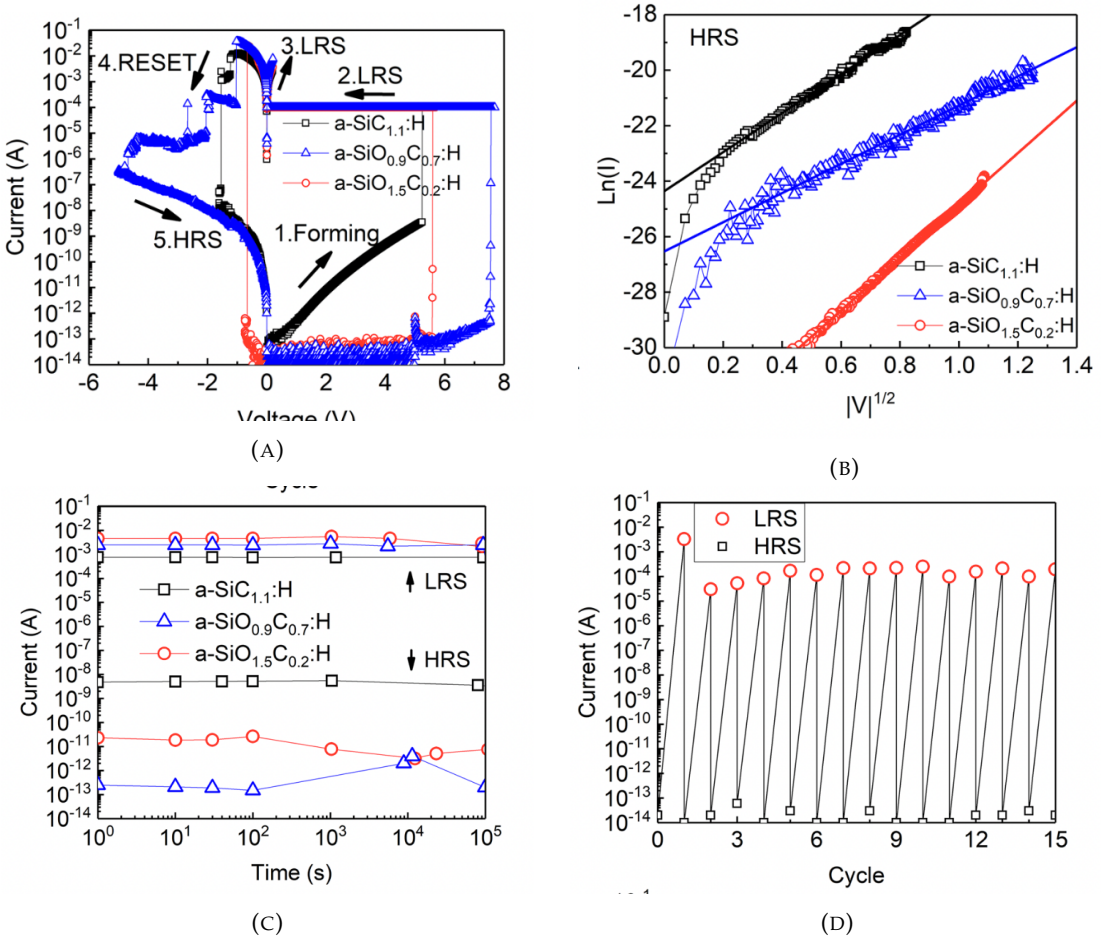


FIGURE 2.4: Resistive switching devices with dielectrics of varying oxygen content. (A) Formation of each device (B) ln(I)-$\sqrt{V}$ showing Shottky conduction is the dominant mechanism in the HRS (C) Retention of the LRS and HRS (D) Endurance of 15 cycles. [4]

characteristics of these devices, which have a simple $Cu/SiO_xC_y/W$ structure that allow for Cu ion migration. Varying levels of oxygen was investigated with x equal to 0, 0.9 and 1.5, and y equal to 1.1, 0.7 and 0.2 respectively.

It was shown that the lowest formation voltage was achieved for devices without oxygen, as shown by the formation graph in figure 2.4a. The Set voltages were also lower for these devices. However, the dielectric with the highest oxygen content had the lowest reset voltages. It was also shown that as we increase the oxygen content the resistive ratio also increases from 10^6 up to 10^{10}. This is due to an alteration of the HRS caused by a change in the Schottky barrier, as shown in figure 2.4b.

These devices show promising performances with some of the highest resistive ratios recorded and with retention measured at 10^5 seconds. However, these devices show poor cyclability with the largest number measured being 15. Therefore, further improvement to these types of dielectrics need to be made.

Physical deposition of SiC and derived structures

Other methods of ReRAM based SiC has been investigated using polymeric composites embedding SiC powders, which were fabricated from a tire recycling process [59]. These devices, however, only had a ratio of 1 to 2 orders of magnitude change and endurance of 10 cycles, with extremely large switching voltages around $\pm$25V.

Alternate SiC structures have also been investigated, which shows that there is the potential for increased performance, compared to previously mentioned devices. Cu was co-sputtered with the SiC dielectric to see if there were any effects to the switching mechanisms, depending upon concentration [60, 61]. The percentage of Cu nanoparticles in the thin film was controlled by adjusting the target RF and DC power. It was found that an increase in the concentration provided reduced formation and Set voltages. It was also found that an increase in the concentration also increases the endurance of the devices from 12 to 60 cycles, with a change of $0 - 30\%$ of the nanoparticles.

Silicon oxycarbide (SiOC) has also been investigated using sputtered films [62]. Sputtered SiOC with varying amounts of oxygen increasing 0 to 2% has shown an increase in the resistive ratio by 8 times and all samples were able to reach over 200 DC switching cycles. However, the device structure $Ag/SiC_xO_y/p^+ - Si/Al$ requires the use of a heavily boron-doped substrate in between the metal electrodes. This can cause scalability issues, especially considering that standard ReRAM structures can be fabricated on any type of substrates.

Similar research has also shown the effects of Boron doping within the SiC based dielectrics in Ag/Si_xC_{1-x}/p-Si resistive switching cells [63]. The Boron doped devices show reduced switching voltages with a similar resistive ratio of around 10^4. However, in this case the silicon substrate is being utilised as a back contact, which still provides the same scalability issues.

Tri-layer stacked Al/SiC/Ag/SiC/Al was also investigated to look at an enhanced performance [28, 64]. 10nm of SiC was used for both layers with the Ag thickness varied. It should be noted that these devices were not sputtered but instead utilised a pulsed laser deposition technique. These devices showed electro-free forming characteristics with ratios of 10^2 and endurance of over 100 cycles. The HRS is dominated by electron trapping/de-trapping and the switching voltages vary depending upon the concentration of the Ag nanoparticles.

Other methods of altering the SiC dielectric have also be investigated, for example using SiCN [65]. SiCN that was sputtered with a device structure of Cu/SiCN/Pt has shown bipolar switching with an endurance of 10^5 cycles at a ratio of 10^3 and retention of 10^4s at 200^oC. As with the previous dielectrics 40nm was deposited and the LRS was shown to be due to Ohmic conduction, however, detailed analysis of the HRS showed

no Schottky emission and instead space charge limited conduction (SCLC) mechanism. This means that the formation and rupture of the filament would not involve the movement of Cu ions, but instead of electron trapping/de-trapping caused by the Nitrogen ions. This was confirmed with temperature dependent tests.

Further investigations looked at using 30nm of the sputtered SiCN dielectric with W and Ag top electrodes [13]. It was shown that the device using W as the top electrode exhibited similar properties to the previously described measurements, with SCLC dominating in the HRS. The device with Ag as the top electrode, however, exhibited 3 separate resistance states. The first two are attributed to the electron charge trapping and de-trapping, while the third state is attributed to the formation of an Ag filament. This was confirmed through temperature dependent tests and shows the large change in characteristics and mechanisms that can occur with small alterations in the device structure.

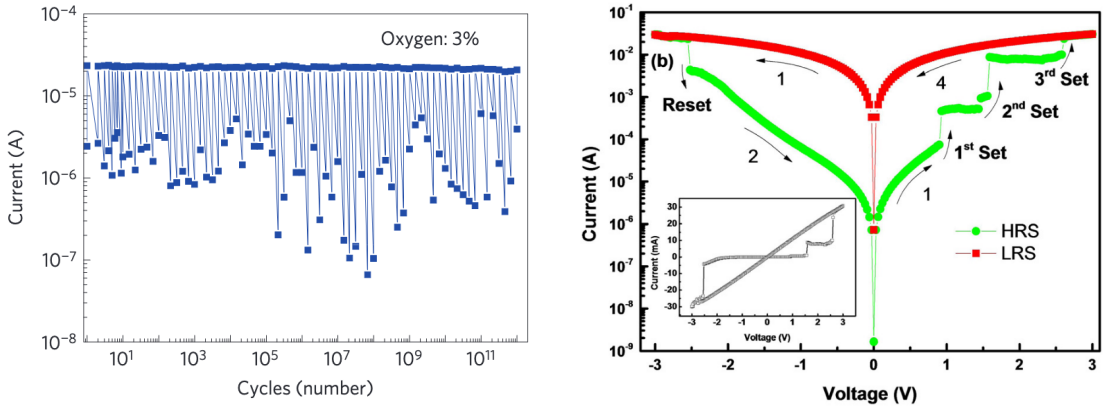
A summary of the best SiC-based resistive memory is shown in table 2.2. This table includes memories with the highest reported endurance, ratios and retention for SiC-based devices. We can see that overall the retention properties of SiC is great for all SiC-based memories, due to the stable nature of the conductive filament. The resistive ratios are also greater than or equal to 2 orders of magnitude. However, there is no resistive switching memory with an endurance greater than 10^6 cycles. For operational memory we must have an endurance greater than this value, to be able to write continuously without the fear of loss of information. To improve this, bilayer resistive memory can be investigated. The theory of this is presented in the next section.

TABLE 2.2: Summary of the best SiC-based resistive memory from literature and their characteristics

Structure	Deposition	Resistive Ratio	Endurance	Retention
Cu/SiC/Pt	Sputtered	100	10^5	150^oC for 10^4s [45]
Cu/SiCN/Pt	Sputtered	10^3	10^5	200^oC for 10^5s [65]
Cu/Si(O)C/W	PECVD	10^6-10^{10}	15	RT for 10^5s [4]
ITO/SICN/AZO	PECVD	10^3	10^6	130^oC for 10^5s [56]

2.3 Bilayer Resistive Memory

Depositing multiple dielectrics in between two metal electrodes can provide a variety of performance enhancements to RRAM devices. In the above section we discussed how GST was used as a thermal barrier layer to reduce the switching time from μs to ns, of sputtered SiC based devices [55]. As well as this, a comparison of Ti/SiC/Pt and Ti/HfO_x/SiC/Pt has also been conducted [66]. These devices utilise 45 nm of SiC, which was deposited by RF magnetron sputtering. The HfO_x layer was utilised a



(A) (B)

FIGURE 2.5: Switching characteristics of Oxide-based Bi-layer RRAM devices (A) Enhanced endurance of 10^{12} cycles using Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt [30] (B) Multi-state switching controlled through the SET operation Au/TiO_x/TiO_{2-x}Au/ [68]

solution based spin coating technique. Both devices were able to switch over 500 cycles using DC sweeps and the addition of the HfO_x layer increased the resistive ratio from 2.78 to 14. The increased in resistive ratio using the bi-layer dielectric is due to the increase in resistance of the HRS, which is inherent to the properties of the dielectrics used. The switching voltages also seem to lower slightly by adding the HfO_x layer. However, this change is small with the single and bilayer having an average Set voltage of 1.05 V and 0.92V, and Reset of -0.99V and -0.83V respectively.

Other uses of bi-layer structures are found heavily in oxide-based RRAM. Utilising an Oxygen rich and poor layer has shown to give an unmatched endurance for resistive switching memory using Pt/Ta_2O_{5-x}/TaO_{2-x}/Pt. This is shown in figure 2.5a which shows the endurance of such a memory which switches on and off 10^{12} times and is currently the world record for resistive memory [30].

This enhancement in performance was analysed using both electrical characterisation and numerical modelling in TiN/Ti/TiO_{2-x}/TiO_{2-y}/Au RRAM devices [67]. Through increasing the oxygen concentration of the top layer and keeping the bottom layer constant, it was possible to tune the resistive switching characteristics, for example altering the resistive ratio. Further investigations into Au/TiO_x/TiO_{2-x}/Au devices show that by altering the compliance current, the conductive filament will form multi-level states controlled in the SET process [68,69]. These multi-level switching steps also have a self-compliance behaviour, as seen in figure 2.5b. This figure shows that through increasing the voltage bias in the Set process, we are able to achieve 3 stable states.

These multi-level steps are thought to be the alteration in the number of vacancies in the oxygen poor thin film. This is presented in figure 2.6 and also applies to electrochemical metallization, but instead of oxygen vacancies it is the movement of metal ions. The first image shows the resistive switching cell to be in the pristine state. By

applying a voltage across the device we are able form the conductive bridge through the bilayers. Reversing this polarity ruptures the filament in the oxygen poor thin film. This HRS state would be interfacial, as the resistance depends upon the area the entire top thin film. With a small increase in bias we are able to move a small amount of oxygen vacancies back through the top layer. The effective doping reduces the barrier height and we end up with a new multi-state, that is still interfacial. By further increasing this bias we are able to connect the two electrodes with a thin conductive bridge, allowing us to be in a second multi-state. This is no longer interfacial as the conduction is occurring directly through the filament. Increasing the width of this filament, through increasing the bias, provides us with the final multi-state, which is the same as the initial LRS after electroforming. This shows that the bilayer allows for a region in which the ion migration can be manipulated and hence allow for precise control of the resistance state. This control and fine tuning increases the stability of our RRAM memory cell overall, as we see below.

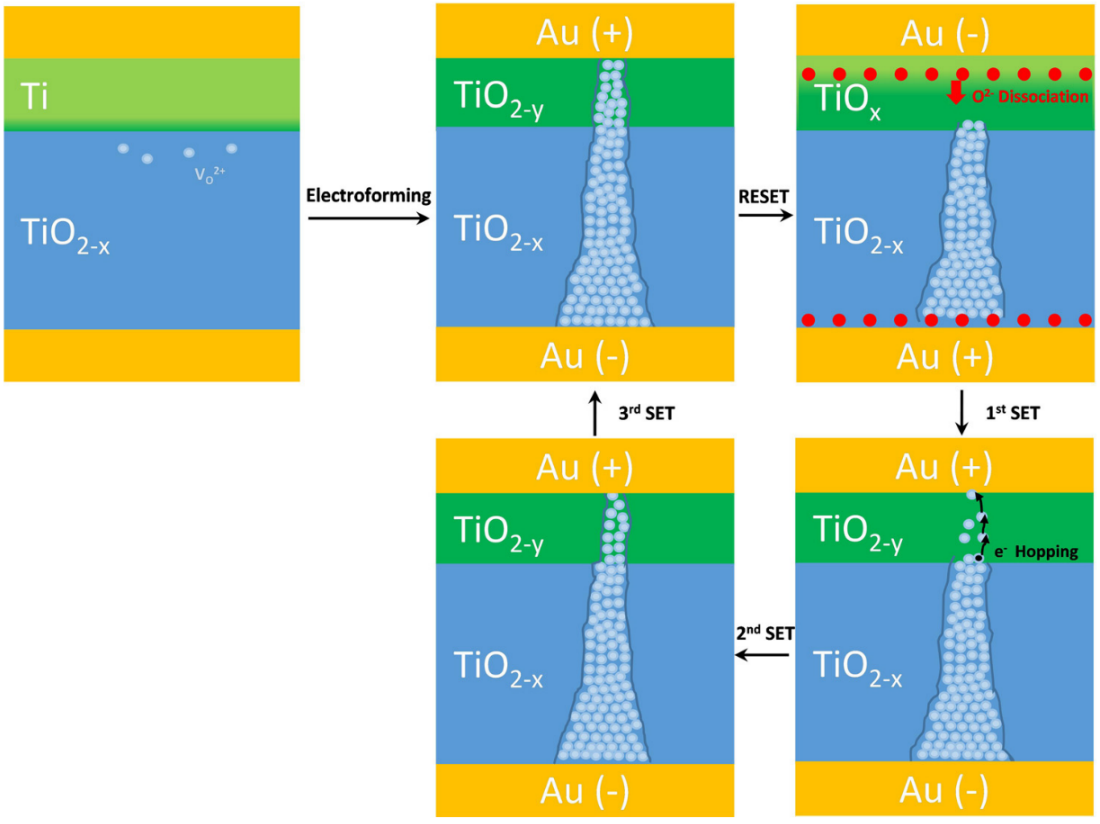


FIGURE 2.6: Representation of the different filament growth from multi-state switching from pristine state to each subsequent multi-level state [68]

A direct comparison of the a single and bi-layer device was also conducting, using Pt/HfO_2/TiO_2/ITO and Pt/HfO_2/ITO RRAM devices [70]. It was found that the bilayer reduced the voltages for both the Set operation. As well as this, the cumulative probability plot in figure 2.7 shows that the bilayer causes the gradient of the plot to

become steeper. This means that the standard deviation between the measured switching voltages improves drastically. The uniformity of the resistive switching states was also greatly improved, due to the stabilised filament formation and rupture at the interface of the two dielectrics. TiN/ZrO_{2-x}/ZrO_2/TiN based devices showed the ability

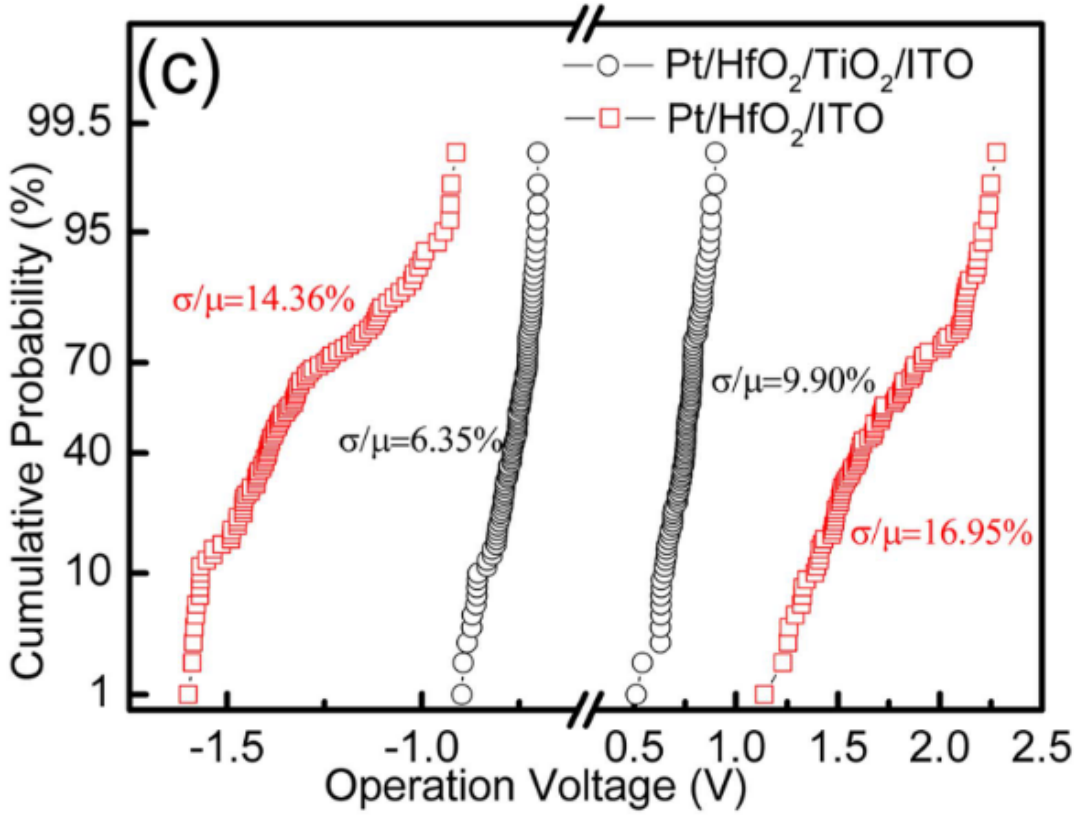


FIGURE 2.7: Increase in uniformity of the resistance states of a bi-layer (Pt/HfO_2/TiO_2/ITO) compared to a single thin film RRAM device (Pt/HfO_2/ITO) [70]

to be switched using both a positive or negative SET polarity, through bipolar switching [71]. The positive polarity provided a greater uniformity in both the switching voltages and the distribution of the resistance states, compared to the negative polarity. As well as this, the negative polarity and a single layer device of the same materials (TiN/ZrO_2/TiN) showed near identical switching characteristics. This was thought to be due to the possibility of being able to form a stronger filament when connecting a conductive bridge at directly to the metal electrode. The depleted Oxygen thin film allows for confinement of the filament size. It was also found that by adjusting the oxygen content of the depleted thin film, the switching characteristics could be tuned. By decreasing x the resistive ratio increased.

Pt/Ga_2O_{3-x}/SiC/Pt has also been investigated and showed that the conduction mechanism still utilised oxygen vacancies [72]. It is thought that these vacancies drift through the SiC layer due to both diffusion and drift. In comparison with a previously reported Pt/$GaO_{1.3}$/Pt device, there is an increase in the resistive ratio from 2 to 10^3 [73]. The

retention of the device also greatly improve, with no degradation observed over 10^4 seconds.

There have also been investigations into poly-crystalline SiC bi-layer based RRAM devices. Au/SiO_2/SiO_x/3C-SiC/n-Si/Al based devices showed an endurance of 10^4 cycles, whilst Au/Al_2O_3/$3C-SiC/n-Si$/Al devices have an endurance of 10^5 cycles [74, 75]. Even though these devices exhibit good cyclability, their resistive ratios were less than 10.

Other materials have also been investigated, for example TaN/ZrO_2 / HfO_x/TiN, which has shown fast switching speeds of 40ns with 10^7 cycles, along with the multi-SET process [76]. As well as this, multi-layer devices can also be used to alter I-V characteristics, so that they show a diode-like behaviour [29, 77, 78]. This characteristic is preferable when combining individual bits together into Crosspoint structures. These types of devices will be discussed in depth in Chapter 6.

Investigations into Tri-layers have also shown promising characteristics, with metal nanoparticles being co-deposited with their corresponding dielectrics. A study on SiC/Ag/SiC showed that depositing Ag for 100 and 200 seconds yielded forming free devices highly asymmetrical characteristics suitable for Crosspoint structures [28].

TiN/ZrO_2/ZrO_{2-x}/ZrO_2/TiN devices also exhibited forming free switching and both interfacial and filamentary switching was observed [31]. The two mechanisms were controlled depending upon the applied voltage bias. The interfacial devices exhibited improved deviation of the resistance states, while also exhibiting lower currents with similar resistive ratios.

With all this in mind, it can be clearly seen that by utilising bi-layer dielectrics in resistive switching devices, it is possible to both improve and tune varying electrical characteristics. This chapter looks at the use of Si/SiC bi-layers for enhanced endurance, for the use in radiation harsh testing. The next section will look at the characterisation setup that was developed to measure these devices.

2.4 Theory of Neuromorphic Computing

Neuromorphic computing is inspired by the highly efficient and unmatched parallel performance of the brain. Current computer architectures separate its memory and processor, therefore, time and energy are spent fetching data, computing the necessary information and writing it back to storage. This constant movement between processor and memory can limit the efficiency and overall computation power of a system. This is known as the Von-Neumann bottleneck [79, 80].

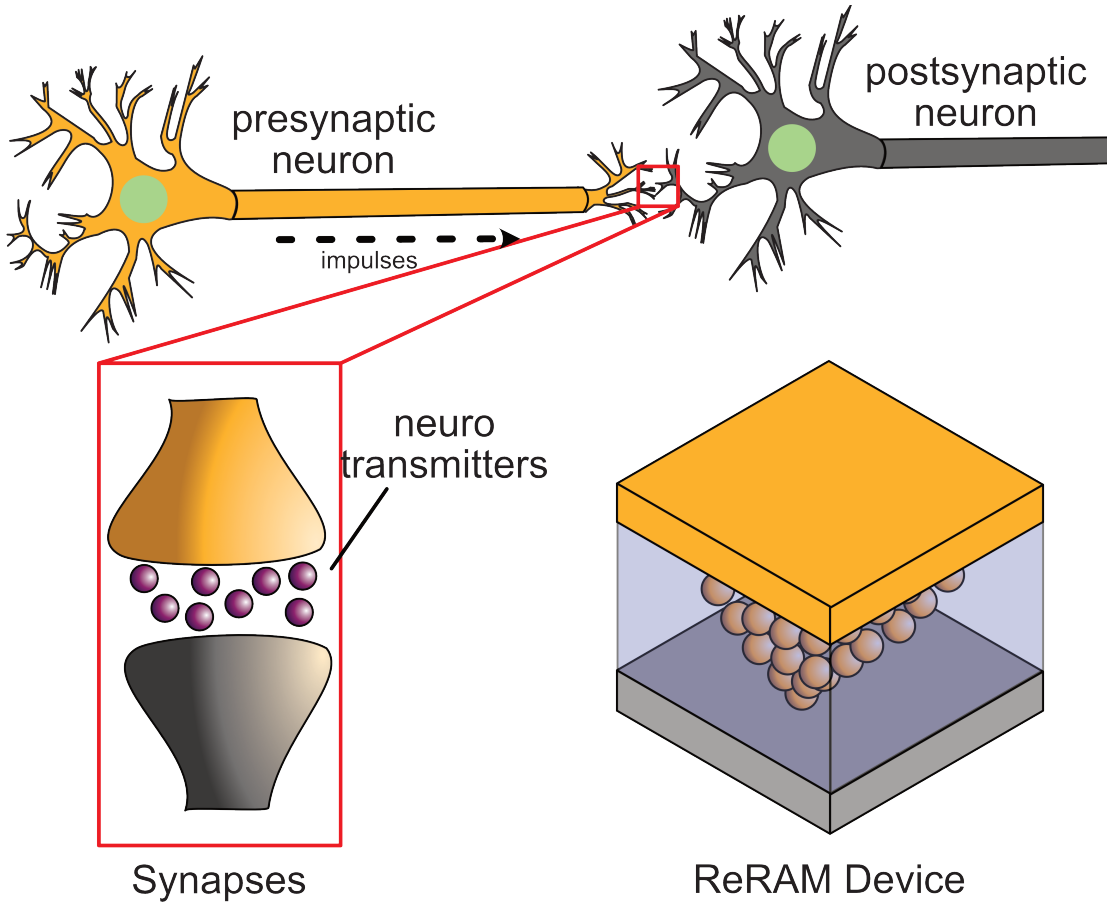
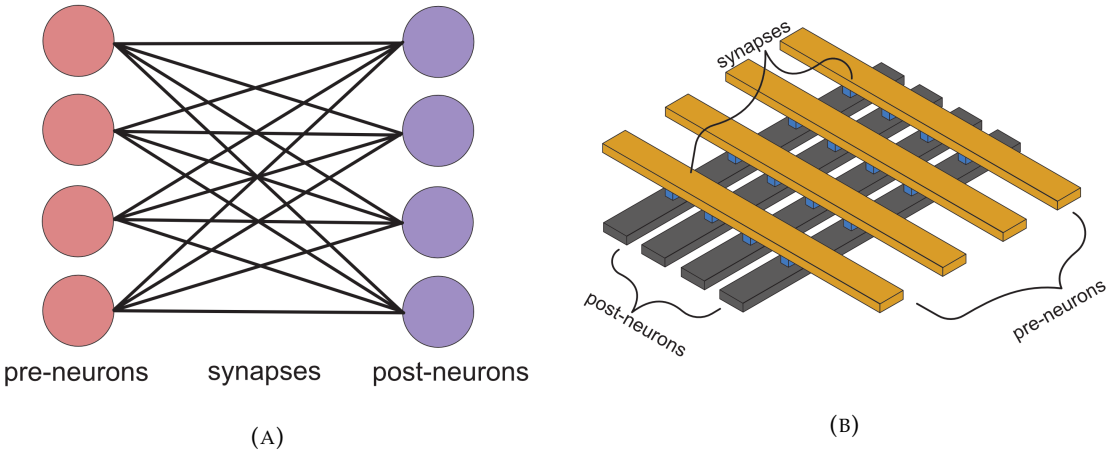


FIGURE 2.8: Illustrations showing the pre and postsynaptic neurons and the direction in which the impulses of the action potentials move across a neuron. The zoomed-in portion shows the synapse connects ion with neuro-transmitters diffusing across to alter the conductance state. Next to this is a RRAM device with Cu ions diffusing to change its conductance state.

The brain manages to store information and compute complex problems, such as language processing, in parallel while only utilising around 20W of energy. For context, the BERT supercomputer is designed as a state of the art neural network for language processing and can train for 80 hours, using around 1000kWh of energy, whilst the brain would use the same amount of energy over 6 years [81]. Therefore, we can see that the future of high-performance computing is to emulate the functions of the brain. This type of system is known as neuromorphic computing and has the potential for highly efficient and fast artificial intelligence (AI) processing [82].

To understand how neuromorphic computing works we first must understand how the brain functions. The brain consists of neurons that are connected by synapses, as shown by figure 2.8. Neurons communicate through electrical signals known as action potentials. These are alterations in the voltage across the membrane due to the movement of potassium and sodium ions. These action potentials reach the synapse which regulates the flow of information in the brain. This is done by the formation of new, discarding redundant or altering the strength of pre-existing synapses. This is done



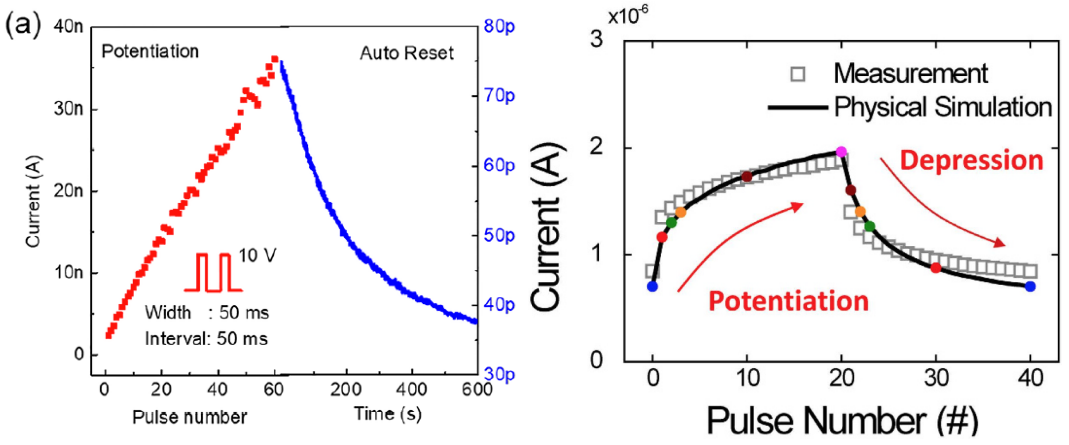
(A) (B)

FIGURE 2.9: Representation of neuromorphic computing with neurons and synapses shown in (A) standard model used to describe synapse connections in AI processing (B) Crosspoint structures with the same functionality

through the use of neurotransmitters which are calcium gated channel ions. These calcium ions are also known as neurotransmitters and move between the synapses to alter the strength of their connections. It has been shown that the ion migration used in RRAM devices can emulate the movement of the Ca^{2+} neurotransmitters to produce artificial synapses [83–88]. By combining these device together we could potentially emulate the brain through neuromorphic computing, through a large number of synapses that are connected to groups of neurons [89]. A Crosspoint structure, as discussed in Chapter 6, can perfectly emulate this with each word/bit line connecting neurons (CMOS connections) and each bit acting as a synapse (RRAM device) figure 2.9 [90].

The strengthening and weakening of synapses between depend upon the levels of activity, this is known as synaptic plasticity [91]. These responses require the application of an appropriate input pulse that can effectively emulate the effects of the action potentials generated from a neuron under a stimulus. By increasing the number (N), duration (D), the interval (I) and the amplitude (A) of the pulses, we can simulate a varying degree of stimulation that reaches the synapse to strengthen or weaken connections by altering the conductance of the device [92].

Synaptic plasticity is separated according to the duration in the change in the strength of the synapse [93]. For RRAM devices this change in strength can be associated with the change in resistance, with a strong connection being equivalent to a low resistance state, although in neuromorphic systems it is usual to talk about conductance rather than resistance. When a brief high-frequency train of stimuli is applied to the synapse an increase in the conductance is observed with each input pulse. If the synaptic change in plasticity is short-lasting and eventually falls back to its original conductance state it is known as short-term potentiation (STP). An example of this is shown in figure 2.10a [94], which shows STP with a measured auto reset. Initially, pulse widths and



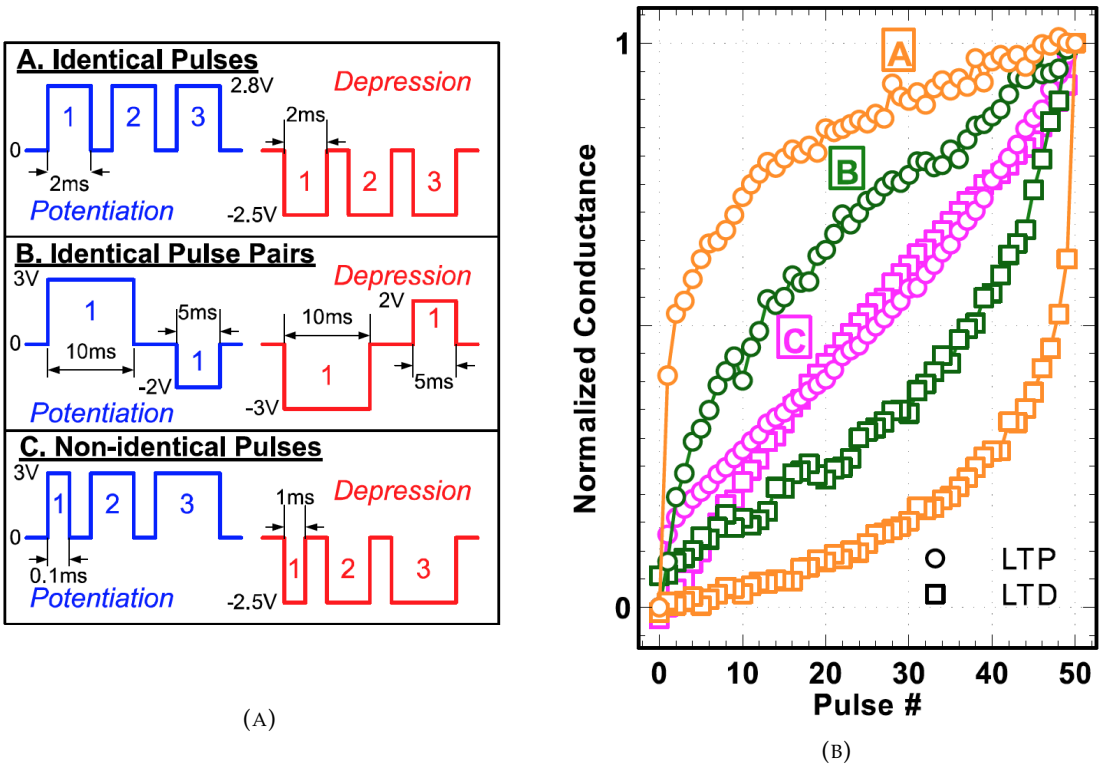
(A) (B)

FIGURE 2.10: Current-pulse graphs showing how alteration in the input stimuli can create (A)Short-term potentiation, in which the input stimuli is not enough to retain the information for long periods [94] (B) Long-term potentiation, in which the synapse remembers its state and must undergo depression to return to its original state [95].

intervals of 50ms are applied to the memory cell and the increase in conductance is observed. Once the pulse train has been taken away the conductance is continually measured, without appling any further input stimuli. The conductance gradually falls back down to its steady state, which can also be considered an observable volatile change in resistance.

If the increase in conductance remains after the input stimuli is taken away, which for RRAM would be a non-volatile change in resistance, we can say that the synapse has undergone long-term potentiation (LTP), figure 2.10b. This is similar to the standard resistive switching process in which a change in the filament has decreased the resistance of the device semi-permanently. Therefore, to weaken the synapse and return it to its original conductance we can employ a similar mechanism to the bipolar switching discussed in chapter 2. Through reversing the polarity and applying another set of pulse trains we can control the dissolution of the conductive bridge and alter the conductance to its original state. This is known as long-term depression (LTD). An example of these plasticity mechanisms is shown in figure 2.10b, which shows LTP and LTD in a resistive switching device [95]. Initially, single pulse trains are applied and there is an increase in the conductance. As the potentiation occurs there is a non-volatile change in the resistance and so the memory cell is able to keep this bit-state when power is taken away. This is the potentiation of the memory cell. Separate input stimuli is then applied, with a reversal in the polarity. This reduces the current with pulse number and causes the depression back to the original conductance. LTP and LDP have been thought to provide the necessary tools for memory and learning, whilst STP can support different types of computation [96].

It should be noted that in a RRAM device, the change in conductance is done through

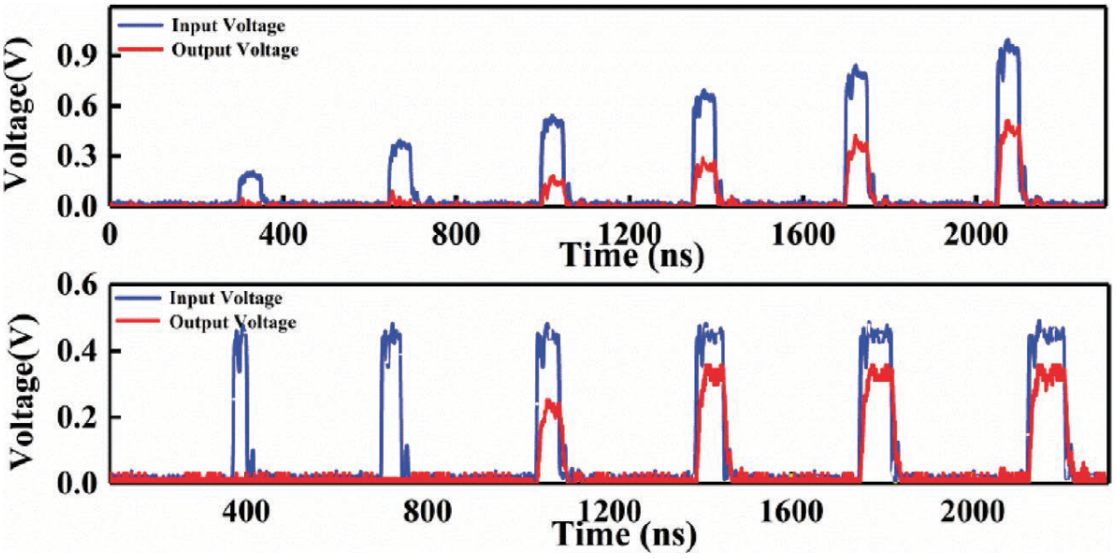


(A) (B)

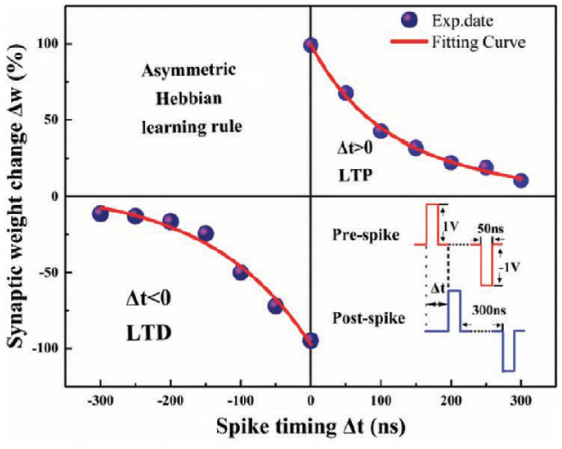
FIGURE 2.11: (A) Voltage-time graphs of different potentiation and depression schemes to improve the linearity of the change in conductance (B) Associated Conductance-pulse number graph showing the change in linearity when altering the parameters of the input pulses [98]

the controlled formation of the conductive bridge. However, due to the nature of this switching mechanism it has been shown that these devices alter their conductance in a non-linear mechanism. To successfully emulate a neuron a linear alteration in its conductance is required. This linear trend is possible through the use of a diffusion limiting layer or by having a dual gated RRAM structure that enables control over the ion migration [27, 97]. A simpler method, however, is to use differing input pulses to force a linear change in the conductance. This can be done by using an identical pair pulse, in which a small pulse is applied with the opposite polarity to force a linear change. Another method is to use non-identical pulses which will allow for a gradual linear change in the potentiation. Both these methods are shown in figure 2.11 showing the pulse input and its respective alteration in the conductance [98].

Finally, both LTP and LTD inputs can be used as pre and post-synaptic weights for spike-timing-dependant plasticity (STDP), which is believed to be the route of learning and information storage in the brain, known as Hebbian learning [99]. If the pre-synaptic signal precedes the post-synaptic one, LTP will be induced and if the signals are reversed LTD will be induced [100]. By also altering the timing between the pre and post-synaptic signals the overall weight on the device will alter. There are four possible types of the Hebbian learning mechanism which depend upon the time between the pre- and post-synaptic signals.



(A)



(B)

FIGURE 2.12: Neuromorphic behaviour from a sputtered SiC dielectric (A) Effects of varying amplitude and duration of the input pulse (blue) on the device conductance (red) (B) measured Asymmetrical Hebbian Learning behaviour [101]

A 10nm SiC dielectric has been shown to exhibit synaptic behaviour and Hebbian learning, [101]. The memory cells are sputtered using radio frequency magnetron sputtering and shows bipolar resistive switching characteristics below $\pm$1V and switching times below 40ns, using Ag as the top electrode. Figure 2.12a shows that by altering the amplitude of the applied voltage pulse, the measured voltage also increased. By increasing the width of the applied voltage, the measured output voltage also increases until it plateaus. Figure 2.12 shows the Asymmetric Hebbian learning that was measured, which is when the weight of the conductance increases while decreasing the time in between the pre- and post-synaptic signals. There is a sharp alteration between strengthening and weakening connections as the time differences crosses zero. However, these results do not provide a detailed analysis of the effects of input stimuli on the relaxation caused by STP.

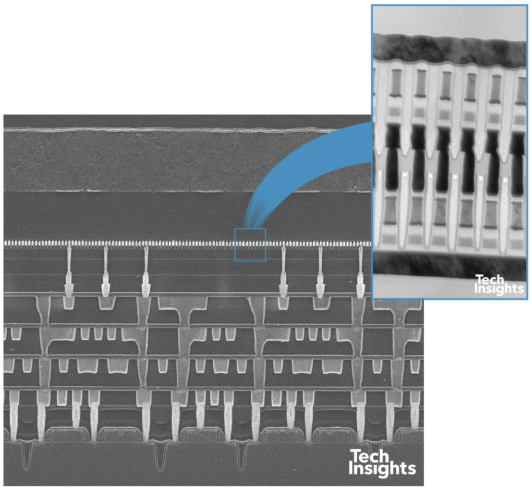


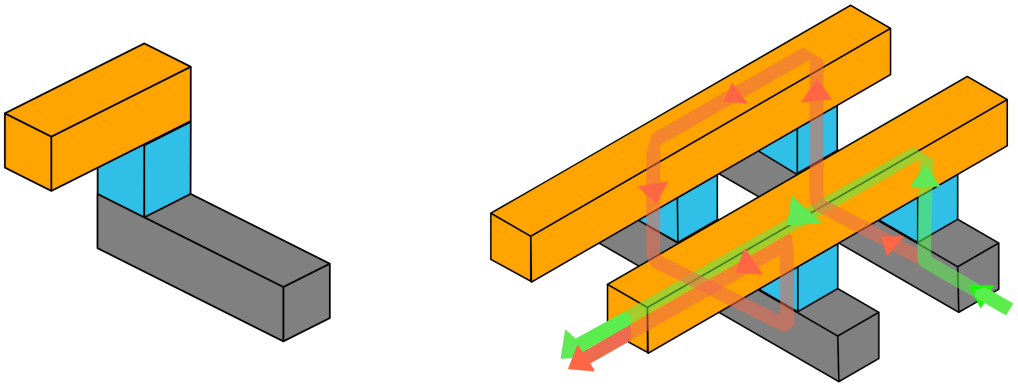
FIGURE 2.13: Cross-section SEM and TEM images taken of Intel's 3D Xpoint memory arrays which show a phase change cells in series with an Ovonic threshold selector. [103]

2.5 System Architecture

To achieve a scalable technology, for both consumer and radiation harsh memory, the individual SiC devices must be combined into Crosspoint Structures. These structures position individual bits in arrays that can be independently accessed and such as structure has become commercially available with the release of Optane 3D Xpoint memory from Intel and Micron Technology [102]. However, this type of memory storage is based on phase change memory, which utilises rare materials such as tellurium to achieve its memory performance, shown in figure 2.13 [103]. This is reflected in the commercial price with a 1.5TB Optane P4800x SSD costing over $5000 [104]. Comparatively, both silicon and carbon are extremely cheap and abundant materials, making them a desirable option for the future of Crosspoint structures.

In a Crosspoint structure, devices are connected through rows and columns which are also known as word and bit lines. By selecting a specific word and bit line individual memory devices can be accessed, as shown by the green arrow in figure 2.14b. The red arrow shows parallel leakage paths through unselected cells which are known as sneakpath [105]. The presence of sneakpath, as well as series, interconnect resistances, can cause limited sizes of the Crosspoint structures and also reduce the sense margins of the resistance states. Therefore, research must be conducted to analyse this phenomenon to counteract its effect.

Sneakpath in a Crosspoint structure with N number of devices can be simplified into the 2x2 array shown in figure 2.14b [106]. Therefore, this structure will be the focus of this chapter, however, as discussed in section 6.1 larger arrays have also been fabricated.



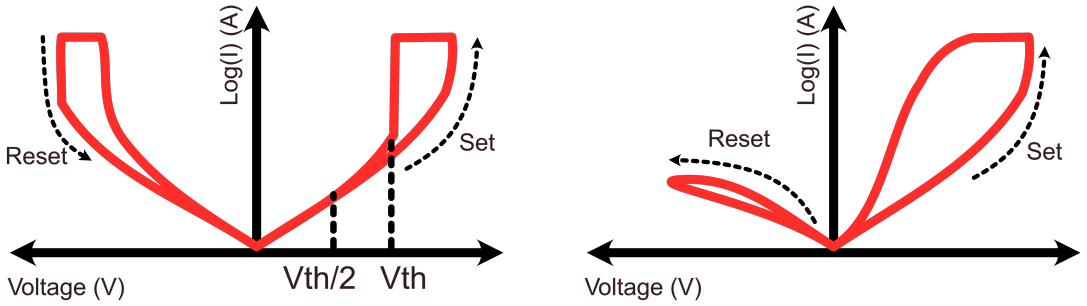
(A) (B)

FIGURE 2.14: Representation of Non volatile memory:(A) a single ReRAM cell with a two metal contacts in between a dielectric. (B) a 2x2 Crosspoint structure with the word and bit lines acting as the top and bottom electrodes. The green arrow shows a device being selected and the red arrow shows parasitic leakages through unselected devices.

To counteract sneakpath the individual devices need to be confined from each other by including a selector device. Selectors are separated into two different categories, which are known as active and passive arrays. Active arrays utilise an external selector, for example, a MOSFET to connect the word and bit line. This is often called 1T1R and it can eliminate sneakpath from the Crosspoint structure as the current can only flow through the selected device when the transistor is turned on through the gate. This method, however, increases the overall size of the chip and increases the complexity of the fabrication process.

Alternatively, passive arrays utilise selectors built into each memory device. This reduces the fabrication complexity as it only requires the deposition of materials between the top and bottom electrodes of each ReRAM device. This means that extra lithography steps do not have to take place to include these types of selectors. This form of a selector is known as 1S1R and are classified according to their effects on the I-V characteristics when in series with a memory device. The first method requires a threshold voltage (V_{th}) for the read/write operation, causing a non-linear I-V characteristic to the ReRAM device,figure 2.15a. When a read or write scheme is applied, at V_{th}, to a specific device the voltage through the unselected devices is equivalent to $\frac{V_{th}}{2}$. This effectively counteracts the problems associated with sneakpath, as the unselected cells cannot reach the V_{th} during a read/write operation.

The second method is known as a self-rectifying selector. A representation of a self-rectifying Reset is presented in figure 2.15(B). In this method, the I-V characteristics of the Set operation are as expected and the device alters its state. Once the polarity of the applied voltage is reversed, the measured current is suppressed significantly compared to the standard I-V characteristic, however, its resistance state is still altered.



(A) (B)

FIGURE 2.15: Representation of I-V characteristics of a selector in series with a ReRAM device providing non-linear switching to counteract sneakpath through (A) threshold switching (B) self-rectifying switching.

This asymmetric non-linear I-V characteristic eliminates sneakpath by counteracting the possibility for the parasitic leakages through the unselected devices.

The final method of counteracting sneakpath is known as complementary switching. This utilises two resistive switching cells that are connected anti-serially, as shown by figure 2.16. The simplicity of this structure allows for a similar fabrication process as the passive arrays while giving the ability to stack crossbars on top of each other [107]. These stacked layers operate by superimposing the IV characteristics of both devices. This also assumes that the switching voltages are consistent while using either a positive or negative polarity for the Set operation.

The complimentary devices cannot be read in the same manner as a standard ReRAM device. There are four different states that the complimentary device can be in and are given in table 2.3. The initial OFF state only occurs at the pristine state of the devices, just after fabrication. To switch the complimentary cell into a bit 0 or 1 a voltage is applied that is just above V1 or below V3 as shown in figure 2.16. This would switch cell 1 or cell 2, depending on which state is chosen. For this example, if a bit 0 is desired cell 1 would have to be in the HRS and cell 2 in the LRS. As the complimentary device acts as a voltage divider when a standard read voltage is applied, the majority of the voltage drops across the single cell in the HRS, in this case, cell 1. Therefore, whether the complimentary device is in bit 1 or 0 the overall resistance of the stacked layers will appear to be in the HRS. Therefore, the system operates at low power consumption and also halts sneakpath across the Crosspoint structure.

To accurately read the resistance state of the device a destructive reading must take place. Using the previous example of cell 1 being in the HRS and cell 2 in the LRS, if a Set voltage is applied to cell 2, as it is already in the LRS, there is no change to the overall resistance and the complimentary device remains in the HRS. If a Set voltage is applied to cell 1 it would cause the entire complimentary device to now read as being

in the LRS state. This means that we know that cell 1 was previously in the HRS and cell 2 in the LRS, corresponding to bit 0.

The destructive reading of the complimentary devices means that the peripheral circuitry required would be more complex than a standard Crosspoint structure using a 1T1R or 1S1R [108]. As well as this the read endurance would also be equal to the write endurance, while also utilising a higher power consumption [109].

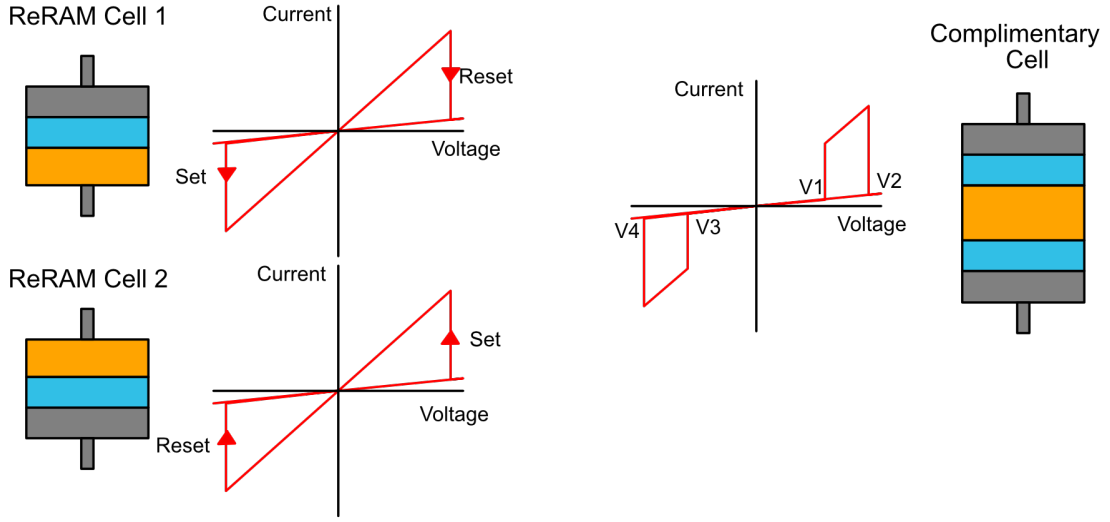


FIGURE 2.16: Representation of the IV characteristics of Complimentary switching. The left shows both the individual bits in its anti-serial configuration. On the Right presents the combined characteristics of two ReRAM cells into a complimentary device.

TABLE 2.3: Bit states of the individual ReRAM devices, cell 1 and cell 2, that make up a complimentary device. Also shown is their corresponding effect on the overall state of the complimentary device.

Complimentary state	ReRAM cell 1	ReRAM cell 2	Overall Resistance
OFF (Pristine cells)	HRS	HRS	HRS
HRS (Bit 0)	HRS	LRS	HRS
LRS (Bit 1)	LRS	HRS	HRS
ON(Only when reading)	LRS	LRS	LRS+LRS

It should be noted that it is also possible to use inherent non-linear I-V characteristics of ReRAM devices to reduce the impact of sneakpath, without the need for physical selectors. This is done by using an intrinsic self-rectifying ReRAM device, which has been previously shown to be successful, for example, a study using amorphous silicon in a 40 x 40 integrated Crosspoint structure [110]. However, this study had a large error rate, with around 75% of the measured resistance values only reaching 50% of the targeted value and required the device to already have these non-linear characteristics. As the Neuromorphic devices exhibit some non-linear I-V characteristics, it might be possible in the future to fabricate these into Crosspoint structures without the need for any form of selectors.

Other types of selector-less arrays include the use of a differential amplifier, with the effective sneakpath current used as a reference input [111]. However, this utilises a complex peripheral circuitry for the standard operation of the matrix.

To design and fabricate selectors for SiC devices it is important to first understand sneakpath in Crosspoint structures to accurately determine the best possible method to counteract these effects. The next section focuses on the design and fabrication of Crosspoint structures without selectors, so that this sneakpath effect can be analysed.

2.6 Resistive Memory and Radiation Harsh Environments

It was the original purpose of this research to study the radiation hardness of resistive memory. Unfortunately, due to COVID-19 the radiation facility was closed and such measurements could not be performed as part of this thesis. However, here we discuss the literature of radiation effects and resistive memory. The planned experiments are included in Chapter 5 and this section should be viewed as context for why reliable information storage is important in harsh environments.

2.6.1 Types of Radiation Effects

Radiation effects on electronic components is an important parameter to consider for systems used in space, defence and medical applications. This is especially true for semiconductor-based technologies as the effects from ionising radiation can severely impact dielectrics, as well as the interface between the materials [9]. These effects from radiation can cause a partial or full breakdown of whole electronic systems. A NASA document has recommended that memory devices should be able to withstand greater than 1 MRad of radiation for deep space and up to 10 MRad to survive Jovian missions [112, 113]. Rad is the unit that describes the amount of radiation dose absorbed, with 1Rad being 0.01J/kg [114].

Standard NAND and NOR technology show little resistance to radiation harsh environments, with degradation in performance occurring below 100kRad [10, 115, 116]. Commercially available CBRAM technology from Adesto, however, has shown no loss of stored information up to 450kRad gamma radiation and 10-20MRad in other studies [2,117]. These ReRAM devices, though promising for radiation harsh environments, show low endurance capabilities. This means they are only suitable as EEPROM memory, in which data is read significantly more times than it is written. The highest endurance of these chips is around 10^5 cycles [118]. Therefore, there is still a need for a reliable and stable form of memory that can withstand radiation harsh environments.

There are several different types of radiation that can affect semiconductor devices. Single Event Effects (SEE) occurs due to the passing of a single ionising particle through an electronic system. The high energy particle can cause electron-hole pairs that induce transient currents and alters bit states [119, 120]. These transient currents can cause destructive or non-destructive effects on electronic systems. It has been shown that ReRAM devices are extremely resilient to SEE, with only two forms of failure mechanisms. The first requires a direct strike of a high energy ion to the conductive filament, which is often only a few nanometres wide making the probability of a bit error extremely low [121, 122]. This is shown by figure , which shows the mapping of conductive filaments through the application of high energy ions.

The second method is due to external peripheral circuits in which high energy ions strike connected transistors, inducing a transient current that alters the bit state [123–126]. The need for these transistors are described in chapter 6 as a 1T1R system. This means that passive Crosspoint structures are more viable for radiation harsh environments, however, this will be briefly discussed later in this chapter.

Displacement-dose damage arises from the interaction of particles that cause lattice defects. This due to the displacement of atoms within a lattice structure. These effects are caused by the interaction of ions, protons, neutrons or even electrons with energies above 150keV [127]. These damages over time can impact the electronic characteristics of the devices, through the alteration of the dielectric properties [128, 129].

Finally, Total ionising dose (TID) are the effects due to the cumulative energy deposition of ionising radiation that interact with matter, causing electron-hole pairs or ionic species and the effects of the charge based carriers on the electronic systems. TID can be measured using photons, electrons, protons or ions. TID tests are often focused on the types of materials used to compare their radiation properties that would be best suited for a given environment, however, there has only been a single investigation on the impact of TID radiation on the electrical characteristics of SiC-based ReRAM. This investigation focuses on a sputtered dielectric using a device structure Cu/a-SiC/Au and shows that there is no change to the switching properties of the devices up to 2MRad of γ irradiation [5].

Even though the TID of SiC has been previously demonstrated, it has been shown that by purely changing the manufacturing processes the TID of a ReRAM device can be severely different, even with a similar dielectric [130,131]. In this instance, it was shown that TID of radiation impacted the devices, with a complete breakdown over 4.5 Mrad of one process. Comparatively, a device with a similar dielectric, produced using an altered fabrication method, were still able to function after 10 Mrad. Looking at the SEM images from this investigation, in figure 2.17, there are clear indications that damage to the device has occurred. Therefore, this Chapter aims at looking at the full electrical

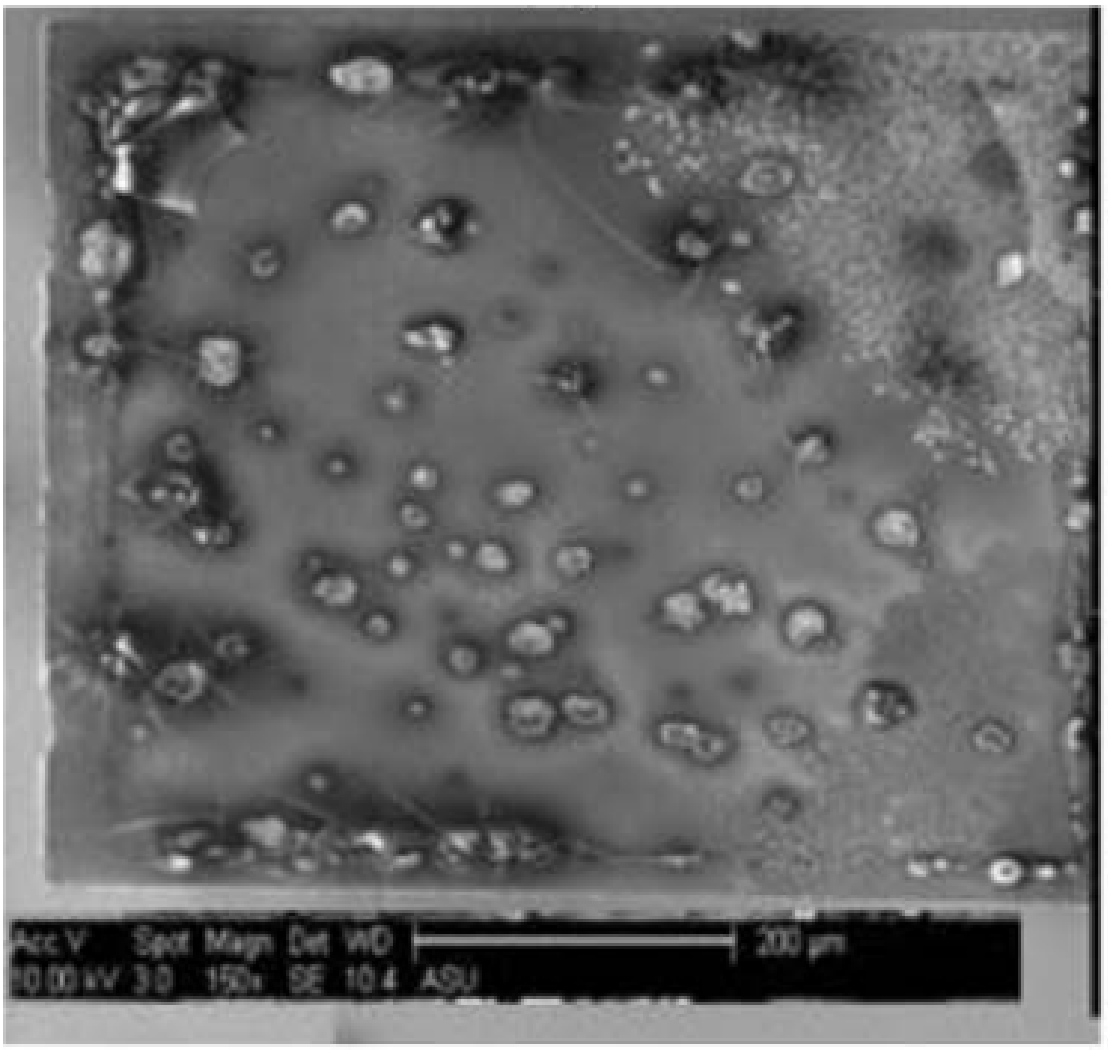


FIGURE 2.17: Scanning electron micrograph showing the observable effects of radiation on a resistive switching device. There were no electrical effects to the device at 10Mrads. Increasing the dose to 4.5MRad showed bit errors, as well as observable surface defects. [130]

performance of radiation-hardened ReRAM using a high-temperature PECVD process that was developed and shown in chapters 3 and 5.

Even with the high tolerance to Total Ionising Doses, there is a form of radiation damage that can affect ReRAM cells known as Single Event Effects. Whilst Total Ionising Dose is the effects of cumulatively generated electron-hole pairs on a device, Single Event Effects is the damage caused by a single ionising particle, for example, a neutron.

Such damage can be broken down into several different types, however, for this thesis we will only discuss Single Event Upsets (SEU). SEU occur when a single highly energetic particle causes a brief current pulse, which would have the potential to change a logic state. An example of this, would be altering a bit state from '1' to a '0' after exposure to a high energy neutron particle. This does not cause permanent damage to the

system and a reset/rewrite to the system can return the array to normal function. The radiation hardness of devices such as this is determined by its linear energy transfer threshold (LET_{th}). linear energy transfer (LET) is used to describe the action of radiation on a material and it describes the amount of energy is transferred to the material from an ionising particle per unit distance ($MeV/mg/cm^2$) [132].

Heavy ion strikes can cause SEU in ReRAM cells due to the possibility of striking the area where the filament has formed on the electrode. This has been investigated by a group at the Sandia National Labs, where microbeam irradiation were used to find the position of the conductive pathway in ReRAM cells [121]. This was done by irradiating single devices across the top electrode and measurement any changes in the resistance state. It was found that by striking specific places across the MIM structure it was possible to switch the device from a LRS to a HRS. This alteration in state was presented to be due to dissolution of the conductive bridge, due to the interaction of the high energy particle at that location. These regions were shown to mainly form at the edges of the structure, due to the higher strength of the electric field at these areas.

In simulation, it has been shown that SEU could occur via an increase in the number of redox reactions brought about by the transfer of energy from the interacting particle [133]. This would then lead to the growth of a conductive filament and could potentially alter a bit state from the HRS to the LRS, or with enough energy permanently breakdown a device. As well as altering the distance between the two electrodes, this work also shows the potential for the diameter of the filament to widen, causing the LRS and HRS values to reduce, while maintaining the same resistive ratio.

This was further investigated by looking at the effects of high energy particles on the formation of a conductive filament, through targeted radiation, which is shown by figure 2.18 [122]. This report shows that through the use of other formation techniques, outside of electroforming, it is possible to create the conductive bridge in other areas of the device. This was done by using ion beam irradiation to form the initial conductive pathway.

These investigations are the main ones concerning single resistive switching in CBRAM devices. Other investigations have been made, however, these concentrate on the use of Crosspoint structures, where the failure mechanisms are often the transistors that are used to select individual bits [124, 125, 134]. Such investigations also include utilising complex external peripheral circuitry to avoid the problems associated with 1T1R based SEU [135].

Further investigations of SEU need to be made using SiC-based devices as they have only been shown to be radiation tolerant against against Total Ionising Doses. However, these types of devices show low cyclability and would not be able to be used for this form of tests. This is because reliability is extremely important so that we can

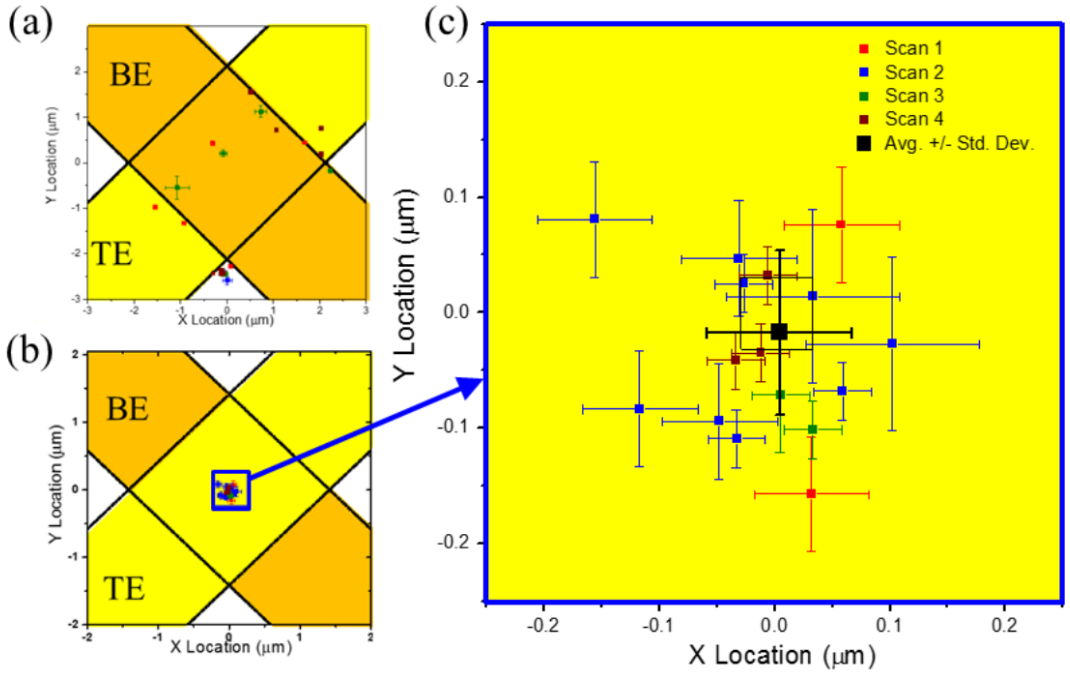


FIGURE 2.18: This figure shows the conductive filament localisation using microbeam irradiation. Image (a) shows the conductive filament of a device through electroforming, with the conductive filaments mainly at the edges of the device. Image (b) shows the creation of the conductive filament at the centre of the device after ion beam formation. Image (c) is a zoomed in view of the centre of image (b). Image taken from [122]

determine if a device has failed due to ion strike, instead of the inherent device characteristics. Therefore, using the high endurance memory cells that we have fabricated during this thesis, we can finally determine the energy required to cause a SEU. However, it should be noted due to the COVID lockdown restrictions these devices were not able to be measured under radiation conditions. Instead, there will be a chapter dedicated to a literature review of radiation harsh systems and a brief results chapter will show the device characterisation that was conducted pre-irradiation, just before the initial lockdown. After this initial lockdown, the devices had degraded beyond a point at which they could be measured and it was decided that the neuromorphic samples showed a greater opportunity to investigate, due to the lack of availability of a radiation source at the time.

2.6.2 Theory of Radiation Interaction

To understand the overall effects of TID it is first important to know the interactions between photons and matter, as well as the probabilities of interaction between the two. This is because the penetration of photons through matter is controlled by the probability per unit area that the photon will interact through several different physical processes [136]. This probability is known as the linear attenuation coefficient (μ_{att}) and is dependant on both the energy of the photon and that material being penetrated.

This explains the previously mentioned literature in which two similar materials, with different fabrication processes, show altering radiation tolerance. The slight variation in the dielectric properties, as well as energies, can have impacts on the probabilities of photon interactions.

It is important to express μ_{att} in terms of the probability per unit volume and fluency that an interaction will occur. (fluence is the number of radiant-energy particles passing through a surface in a given period, divided by the area of the surface.) This is known as the atomic cross-section ($\sigma_{"interaction process"}$) and its equation is given by 2.5 below, in which n is the number of atoms.

$$\sigma_{"interaction process"} = \frac{\mu_{att}}{n} \tag{2.5}$$

In general μ_{att} is referred to as the macroscopic cross-section and $\sigma_{"interaction process"}$ as the microscopic cross-section. For this thesis, we will focus on the microscopic cross-section to discuss photon interaction with matter.

One way in which photons can interact with matter is the ejection of electrons (e^-) through the photoelectric effect, which was previously mentioned in 3.3.2.3 which describes how X-ray photon spectroscopy works. To recount this equation 2.6 is given below, where T_{max} is the maximum kinetic energy of the electron emitted, h is plank's constant, v is the frequency and φ_0 is the minimum energy required to remove the most loosely bound electron, known as the work function.

$$T_{max} = hv - \varphi_0 \tag{2.6}$$

Another interaction that can occur is known as Compton scattering. This is when the incident photon ejects an e^- and emits a γ which has a shift in its wavelength(λ). An example of this is given in figure 2.19a, which illustrates Compton scattering. The emitted photon has a wavelength as described by equation 2.7, where θ is the angle at which the electron is ejected. The e^- that is ejected has an energy-related to equation 2.8 where T is the kinetic energy of the electron and c is the speed of light in a vacuum.

$$\Delta\lambda = \frac{h}{m_e c}(1 - cos\theta) \tag{2.7}$$

$$T = \frac{1 - cos\theta}{mc^2/hv + 1 - cos\theta} \tag{2.8}$$

Finally, another main form of interaction is known as pair production. This is the creation of an e^- and positron pair (β^+) pair that annihilates and produces two photons with energies equal to $511keV + \Delta T$. Both the γ photons emitted from Compton scattering and pair production can either be emitted out or further interact with the material.

The relative energies of the emitted pairs are shown by equation 2.9, where T_+ is the kinetic energy of the positron and T_- the electron.

$$h\nu = 2mc^2 + T_+ + T_- \tag{2.9}$$

The $\sigma_{"interaction process"}$ probabilities associated with these interactions of photoelectric effect, Compton scattering and pair production alters with the energy of the incident λ and the number of protons in the target material. This can be shown by the following equations:

$$\sigma_{photoelectric} = \frac{Z^5}{T^{\frac{7}{3}}} \text{per atom} \tag{2.10}$$

$$\sigma_{compton} = \frac{1}{\hbar\omega} \text{per electron} \tag{2.11}$$

$$\sigma_{pair production} = Z^2 ln(\frac{2\hbar\omega}{m_e c^2}) \text{per atom} \tag{2.12}$$

As we can see by these equations the probability of the photoelectric effect increases with reduced energies, while the probabilities of pair production increase with both increasing atomic number and increasing energies./ This is represented by figure 2.19b which shows the areas in which the three interactions described above dominate through varying both the atomic number (Z) and the energies of the incident photons.

It should also be noted that there is another interaction known as photo-disintegration. This is when a photon is absorbed by an atomic nucleus and knocks out a nucleon. This interaction can emit a neutron and can only occur above a threshold value, similarly to the photoelectric effect. The photon must have enough energy to overcome the binding energy of the ejected nucleon and hence has a probability of orders of magnitude smaller than the photoelectric effect, Compton scattering and pair production combined. An illustration of this process is shown in figure 2.19c.

With all of this in mind, we can say that there are two main mechanisms in which there could be some failure in resistive switching devices from photon interactions. The first method is through the ejection of electrons, causing vacancies. These vacancies could rebuild a conductive filament that has been ruptured, altering its bit state from 0 to 1. This has shown to affect valence change memory (VCM), whereby the conductive filament is formed using oxygen vacancies [137,138]. This could mean potentially cause bit errors due to ion migration, as well as the damage associated with the dielectric. The second method is through damage to the dielectric causing the electrical properties of the thin film to alter. For example, it has been shown that radiation-induced metal migration can occur through dielectrics [139]. This could potentially lead to alterations in bit states or even changes to the electrical properties of the thin films through doping.

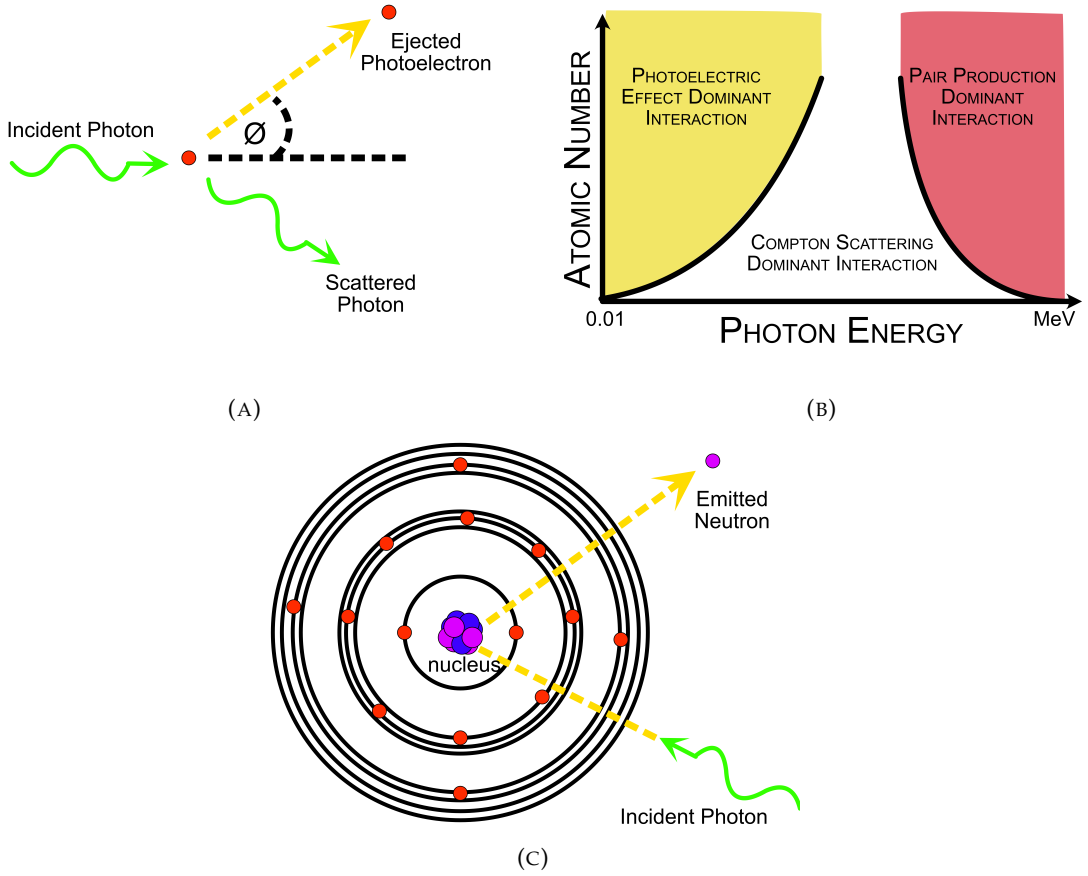


FIGURE 2.19: (A) Illustrations describing the interactions of photons with matter during the Compton Effect. (B) Graph of the dominant interactions of photons between matter while changing the atomic number and photon energy. (C) Shows photo-disintegration with a nucleon being ejected from the nucleus.

The next section will describe in-depth the literature surrounding the investigations into the tolerance of resistive memory against total ionising dose damage.

2.6.3 A Review Of Radiation Effects In Resistive Memory

It is important to understand the effects of radiation on the switching characteristics of ReRAM, due to the potential alterations that exposure could cause on the functionality of the devices. Such alterations have even been suggested to be used as a form of radiation sensor, due to the predictable nature of the dielectric breakdown [140–143].

Total ionising dose (TID) is measured through the use of a Cobalt-60 (^{60}Co) source for gamma irradiation (γ) as a standard practice for radiation effects qualification of devices for the use in harsh environments [144]. These tests often focus on the devices' ability to withstand ionisation radiation concerning its retention, cycling characteristics and its ability to switch resistance state both before and after its pristine state. In

this section we will review the literature of different materials tested against TID, however, the majority of this work is focused on chalcogenides. This is because there is a limited amount of literature surrounding Electrochemical Metallisation (ECM) ReRAM devices, as well as those about SiC-based devices. Therefore, this extended literature review will cover a range of dielectrics to provide a context of the possible radiation effects that TID can cause.

The first material that we will discuss is the TID effects of Ge_xSe_y based dielectrics, which show the general radiation hardness of resistive memory against gamma radiation. Looking initially at Ag/$Ge_{30}Se_{70}$ devices, with the Ag being utilised as the top electrode, varying levels of γ radiation was exposed to see if any changes in the HRS, LRS and the cyclability of the devices could be observed [145, 146]. Devices were irradiated progressively and differing steps up to 5.21 MRad of radiation and showed no alteration in the LRS. A small amount of deviation was shown in the HRS, however, this was concluded not to be due to the radiation dose but instead the deviation of the device to device characteristics. Additional separate devices were irradiated with 10 MRad of TID, without steps, to look at the high-intensity radiation doses without influence from previous irradiation. These devices no major alterations and there appeared to be no changes in the switching voltages or any increases in the potential failures of the endurance across 500 cycles post-irradiation. Further investigations into Ag/$Ge_{40}Se_{60}$ also showed no degradation in the switching properties and the resistive ratio keeping within 10^4 up to 10 MRad dose [147]. There is only a small noticeable change of the HRS state at 10 MRad, however, it is not enough to affect the resistive ratio within a tolerance.

Looking at another study, a comparison of annealed and non-annealed of $Ag_xGe_ySe_z$ based dielectrics were investigated to look at the differences in their characteristics to radiation exposure [148]. Before radiation, the annealed samples had a lower HRS than the non-annealed. The non-annealed samples also had a lower Set and Reset voltage, as well as a lower standard deviation. After radiation exposure of 1.06 and 2.38 MRad, the devices were cycled 500 times and the annealed samples showed an increase in resistance for both the LRS and HRS with an increase in dose. This is the first description of the LRS altering with radiation exposure. Conversely, the non-annealed samples initially showed an increase in the resistance states with 1.06 MRad, however, the resistance decreased below the original states after 2.38 MRad. For the switching voltages, it was found that the set decreased with an increasing amount of dose. The reset voltage, on the other hand, showed that it was easier to reset annealed devices and harder to reset non-annealed devices after radiation exposure.

Further TID testing of $Ge_{30}Se_{70}$ looked at the retention of these devices using γ up to 2.8 MRad [149]. No major abrupt changes in the HRS or LRS were recorded and all of the devices were able to hold their bit states throughout retention testing. Through endurance testing, it was shown that no degradation was found in 10^4 cycles whilst

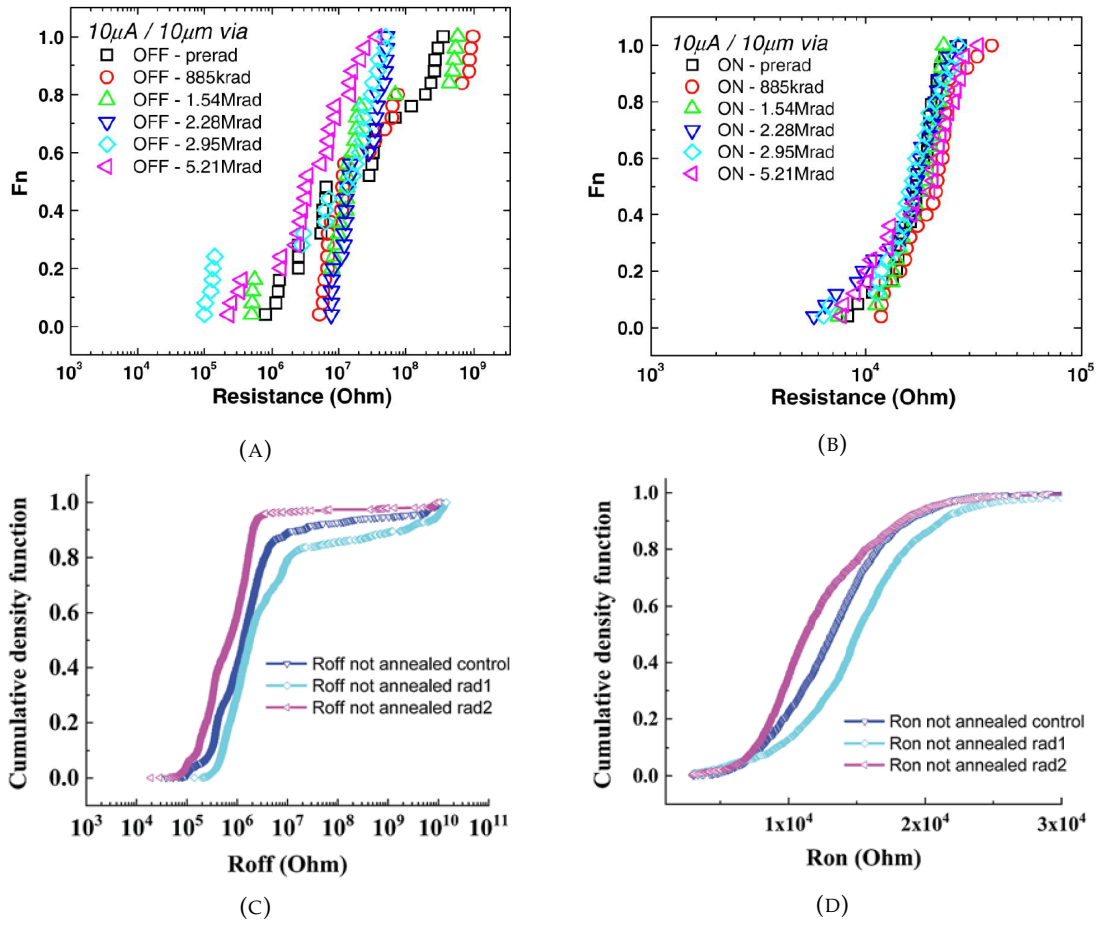


FIGURE 2.20: Cumulative density function plots of two separate studies showing the effects of radiation hardness of the type of dielectric. (A) Retention of the HRS using Ge_xSe_y up to 5Mrad (B) Retention of the LRS using Ge_xSe_y up to 5Mrad [145]. (C) Effects of the HRS on $Ag_xGe_ySe_z$ based devices up to 2MRad (D) The associated LRS retention up to a dose of 2MRad [148].

stepping the TID dose up to 4.62 Mrad. Degradation for these devices was defined as having a resistive ratio below 100. It should be noted that further testing of these samples was conducted with 100 keV electrons to assess any alterations with the type of radiation exposure. The devices were step irradiated up to 12 Mrad and the devices were still able to effectively switch even after exposure. the LRS did not seem to alter with an increase in radiation and the HRS showed minimal alterations showed only a slight reduction in resistance and standard deviation.

As well as this retention of photodoped $Ag_5Ge_{30}Se_{70}$ was tested up to 24Mrad of γ exposure and showed no abrupt changes in the resistance states across the 16hr exposure [113]. It should be noted that this paper heavily focuses on ion bombardment to compare displacement damage dose, but this will not be discussed in this chapter.

Along with the standard ReRAM device, 1s1R devices were also measured against radiation doses. 1S1R devices are built to counteract parasitic resistances when combining ReRAM into arrays, this is discussed in depth in chapter 6, $Ge_{30}Se_{70}$ based films were

stepped stressed, along with SiO_2 selectors, up to 5Mrad [150]. The resistive switching devices showed a decrease in the resistance states, which was found to be due to photodoping effects. This effect can be suppressed simply by pre-photodoping the thin film under UV light. The selector device, on the other hand, showed no signs of degradation. This further shows the improvement of. a 1s1r device over a 1t1r device.

TID using other forms of photons has also be investigated in chalcogenides. It was found that, by using X-rays, the switching characteristics of the devices would change with 24 kRad of dose, however, the composition of the dielectric greatly affected how the device deteriorated [151]. $a - Ge_xSe_{100-x}$ was investigated with altering x with 22.6, 32.4 and 44.3 atomic percentage. Each device was able to perform up to 10^5 switching cycles pre and post-irradiation of 12 and 24 kRad. The switching voltages after exposure were found not to change and any variations were found to be due to inherent device characteristics. There was, however, slight increases in the HRS with radiation exposure. It should be noted that the devices exhibited an increase in the resistive ratio with a decrease in x, before irradiation. This was mostly maintained after exposure, except for x=32.4 at 24 kRad.

Moving away from chalcogenides, Cu/SiO2 based ECM devices have also been investigated for radiation harsh experiments. These devices showed no change in the standard operation of devices from the pristine state, the On state and the overall switching voltages and endurance [152]. The HRS did reduce slightly after 1.5 Mrad of dose, however, this settled out and the overall resistance of the off-state remained within GΩ.

Cu doped HfO_2 also shows good radiation tolerance to radiation environments, however, with some alterations in its switching properties. It was found that while the On state resistances, over 1200 cycles, the Off state reduces its average resistance and standard deviation with only 350 kRads of γ [153]. As well as this, the set voltages increased from 4.17 to 5.15V, with little changes in the reset voltage.

Other HfO_2 based RRAM devices have shown good resistive switching and zero degradation of the resistive switching devices up to 22.1Mrad dose of gamma radiation [154]. As well as this, good retention up to 10^6 seconds after a total dose of 7.9MRad.

$Ag/AlO_x/Pt$ based devices have shown that with an increase in radiation, up to 1Mrad exposure, the resistance of the HRS decreases [155]. It's also shown that there is an increase in the formation voltage and a decrease in the Set voltages. The alteration in the HRS was proven to be created through electron-hole pairs in the AlO_x, through temperature dependant tests.

While the previously discussed devices have all been focused on standard logic resistive memory, there is only a handful of literature that focuses on radiation-hardened neuromorphic devices. A single discussion on the displacement damage dose shows

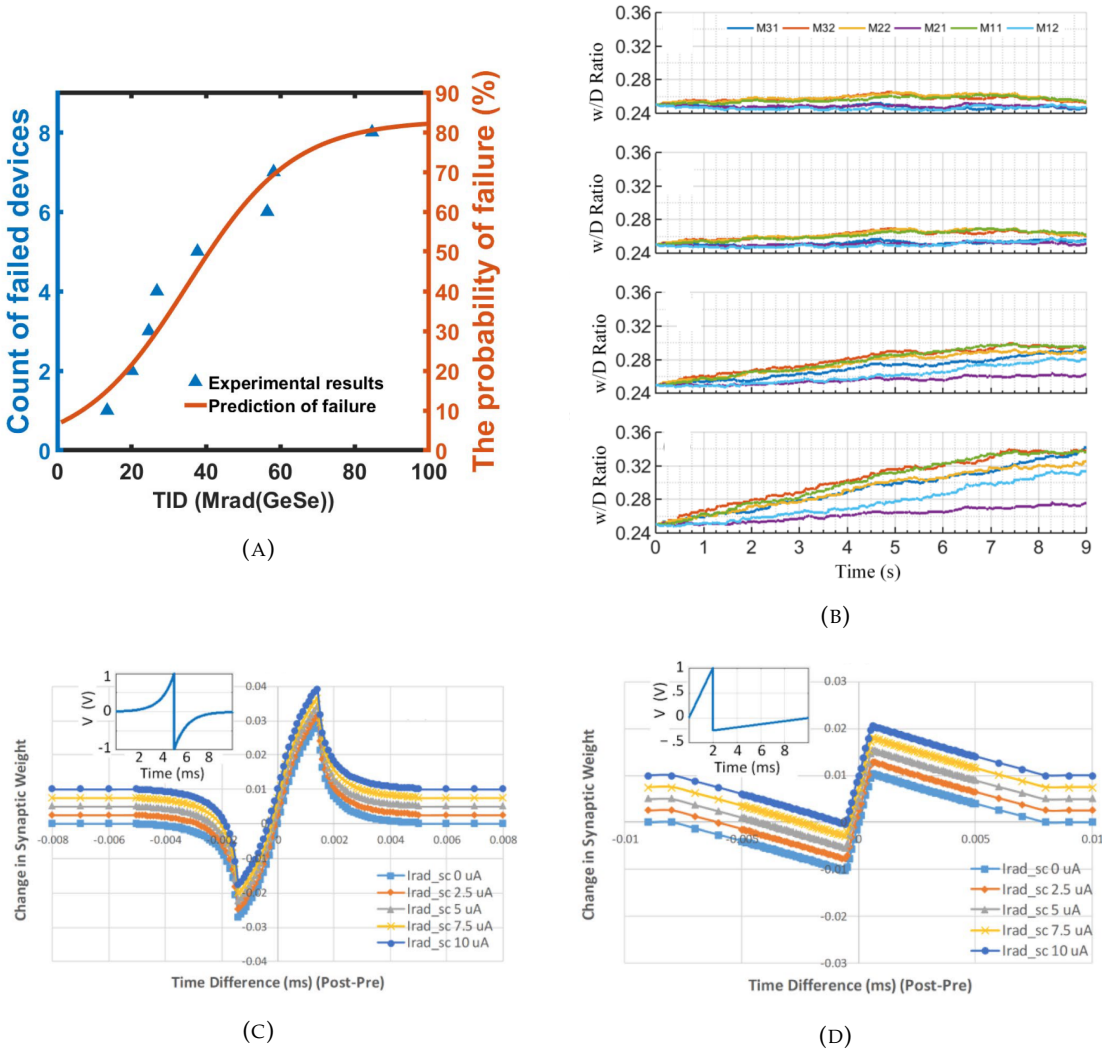


FIGURE 2.21: Simulation results from literature showing the effects of radiation on neuromorphic ReRAM devices. (A) The failures of cells above an equivalent TID of 30MRad. (B) Increase in synaptic weight with an increase in radiation dose (C) and (D) Effects of STDP simulations after a state altering radiation event using exponential and triangular bi-phasic pulses respectively. [156]

only small effects on the resistances, but not on the switching characteristics of the neural networks [157]. this data, however, does not show the effects of gamma radiation of TID.

Looking at $LiNbO_2$ based devices, proton and X-ray radiation were investigated. It was found that X-rays lowered the resistance values of the dielectric, while proton radiation increased the resistance states [158]. However, even though these devices appear to show neuromorphic analogue behaviour, no analysis was done to look at the changes in the synaptic weights. Along with this another publication focuses on the c-f response from radiation on a neuromorphic ReRAM device [159]. These devices who no alteration in the characteristics up to 1MRad, however no analysis of the short or long term potentiation were investigated

Other published work focus on the use of simulations to predict any changes in the potentiation timings and conductances of neuromorphic devices, against radiation. The first paper that we will discuss looked at simulations of both SEE and TID and compared their results to actual experimentation taken from another journal described above [113, 160]. This simulated data shows that the neural networks were resistant to SEE over 30 years of operation and only slightly susceptible to cumulative heavy ion exposure with an equivalent TID of 30Mrad. However, above this value, critical failures can occur, as shown by figure 2.21a

Further simulation analysis also shows that resistance states during TID doses do not affect the resistance states of the neuromorphic devices. However, it can alter the synaptic weight associated between the pre and postsynaptic neuron, with an increase in radiation causing an increase in the synaptic weight [156]. This is shown in figure 2.21b.

This analysis was taken further by looking at the effects of radiation on the learning behaviour of ReRAM neural networks [161]. it was found that the previous report on increasing the radiation dose on synaptic weight also brings asymmetry to the STDP, shown in figure 2.21c and 2.21d. The network destabilises and takes longer to relearn patterns, meaning the system might suppress synapses causing a different learned pattern. Overall it was found that at a lower flux the alteration in the spiking neural network was negligible, however, at a significantly higher dose can affect the learning behaviour, meaning that layer may learn slightly different functions when exposed to radiation.

2.7 Conclusions

There is a great potential for SiC-based resistive memory with its good retention capabilities, large resistive ratios, and its ability to withstand harsh environments. The methods described above mainly focus on the use of sputtering techniques for standard SiC devices. BEOL processes favour chemical vapour deposition and so the compatibility of these methods to fit within the interconnect lines is very limited. For chemical vapour deposition, the best endurance was 10^6 cycles using PECVD to deposit SiCN [56]. The work in the next chapter will show the fabrication methods for a PECVD deposited SiC thin film that can outperform its sputtered counterpart and yield the highest endurance for CBRAM memory which currently is at 10^8 cycles. This increase in endurance is also important to fully characterise the radiation hardness of these devices. The next chapter will focus on the fabrication and material characterisation of the devices measured in this thesis with the subsequent chapters detailing their electrical characterisation.

Chapter 3

Fabrication of PECVD SiC-based Resistive Memory

This chapter details the fabrication of the SiC resistive memory cell using plasma enhanced chemical vapour deposition. Numerous wafers were prepared with varying performance, but three batches had particularly good characteristics. These wafers are separated by a single characteristic, whether the wafers have a single layer or a bilayer. Four wafers were fabricated with a single layer in the same fabrication process. For this thesis these will be called the ”Single layer” wafer.

Only one wafer was fabricated with the bilayer and subsequently two more wafers were fabricated successfully to see if the bilayer was reproducible. For this thesis, the first wafer will be called the ”Bilayer” wafer and the subsquent wafers the ”2^{nd} Bilayer” wafer. Each memory cell consists of a substrate, a bottom electrode, a SiC-based dielectric layer and a top electrode.

It should be noted that the initial bilayer resistive memory utilises a shadow mask lithography step, while the subsequent bilayer and single layer wafers utilise a more complex lithography process. Figure 3.1 outlines the fabrication process for all of the PECVD resistive memory wafers. Details of the experimental techniques to characterise the fabrication process are introduced throughout this chapter at their first use.

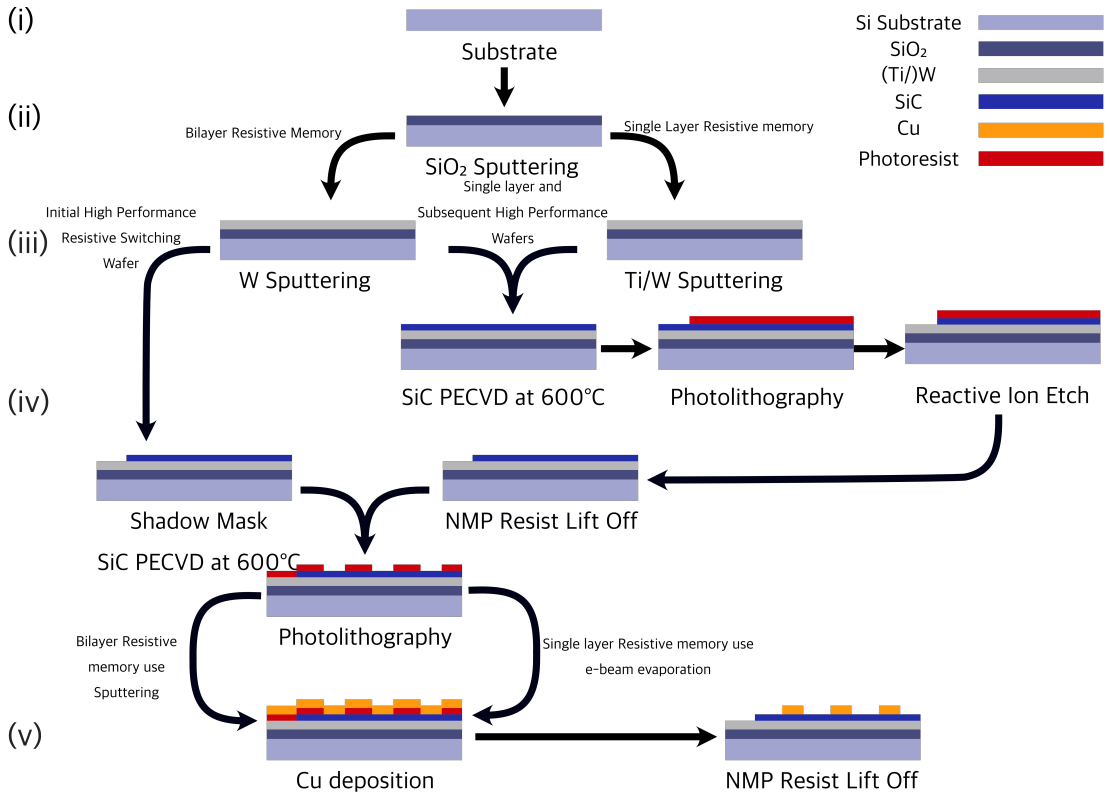


FIGURE 3.1: Process flow of the fabrication of SiC-based resistive memory using PECVD. (i) Initial Si substrate, a 4-inch substrate is required for this process(ii) 500nm of insulating SiO_2 layer was sputtered to stop any leakage currents through the substrate (iii) The W bottom electrode was sputtered, with the Single layer cells having an additional Ti adhesion layer (iv) The SiC layer was deposited using Plasma Enhanced Chemical Vapour Deposition at 600^0C. The bottom electrode was opened through either photolithography and etching or utilising a shadow mask in the SiC deposition. (v) The top electrode was deposited using 100nm of Cu

3.1 Silicon Substrate and Silicon Dioxide Insulation

Silicon wafers were purchased to act as the substrate, as they commonly used for most micro and nano-electronic fabrication processes. The cells that we describe in this thesis do not require the use of the silicon substrate and can be fabricated on any insulated surface. Therefore, there was no preference on the conductivity and type of doping of the Si substrate.

Instead, the wafer was insulated using around 500nm of SiO_2. This was done using a reactive sputterer instead of thermal oxidation as it is a slightly faster process that still allows for good uniformity as shown further in section3.1.1. Reactive sputtering is the process in which compounds are able to be deposited on top of a substrate by introducing reactive gases to a plasma which is typically formed by an inert gas, in this case Argon. This process used a silicon target with added Oxygen gas to produce the required thin film.

The process was not conducted by crystal monitor to observe the deposition thickness, instead the rate of deposition was already known and the required time was calculated. The rate of deposition for the SiO_2 recipe was 0.5nm/s. Therefore, to reach the required $500nm \pm 10\%$ isolation layer, the deposition time used was around 17 minutes. The parameters of this deposition are given by table 3.1.

TABLE 3.1: Parameters used for the SiO_2 deposition using a reactive sputterer.

Substrate Temperature (^oC)	Power (W)	O_2 (sccm)	Deposition rate (nm/s)
75	2000	22	0.5

3.1.1 Ellipsometry Measurements

The thickness of the SiO_2 thin film and its uniformity was checked using an ellipsometer. Ellipsometry is the process of measuring the change in the polarisation of light that is reflected or transmitted from the surface of a sample, which can be used to measure optical properties and the thickness of the thin films. Figure 3.2a gives an example of this setup. Light is emitted from a source and is linearly polarised before reaching the sample. The light is then reflected and is passed through a second polariser, also known as an analyser, and then is absorbed by a detector. The incident and reflected angles of the polarised light are equal and the polarised light that is parallel to the incident plane is known as the p-plane. A polarisation perpendicular to this plane is known as the S-plane.

The analysis of the incident and reflected polarised light is used to measure the complex reflectance ratio ($\rho_{complex}$) which is the ratio of the amplitudes of the s and p components after reflection (r_s and r_p respectively). Therefore, using the amplitude component (ψ) and the phase difference (Δ), between the incident and reflected waves, we can use equation 3.1 to model the thin film material.

$$\rho = \frac{r_p}{r_s} = tan(\psi).e^{i\Delta} \tag{3.1}$$

Figure 3.2b shows the data collected and modelled from the highlighted point at the centre of the wafer. This graph illustrates the measured ψ and Δ, as well as the models used to provide an accurate measurement of the thickness of the dielectric, using equation 3.1. Experimentally, this data was not manually fitted and instead standard models within the ellipsometry tool were used to determine the thickness of the thin films.

The ellipsometry data presented in figure 3.2c is taken from a 4-inch wafer and shows the achieved thickness of the SiO_2 layer is 530nm $\pm$ 3nm, compared to the aimed 500nm. The uniformity across the wafers is hence better than 0.5% and even higher

near the centre. it shows that the largest difference in thickness across a wafer using this SiO_2 recipe is around 3nm.

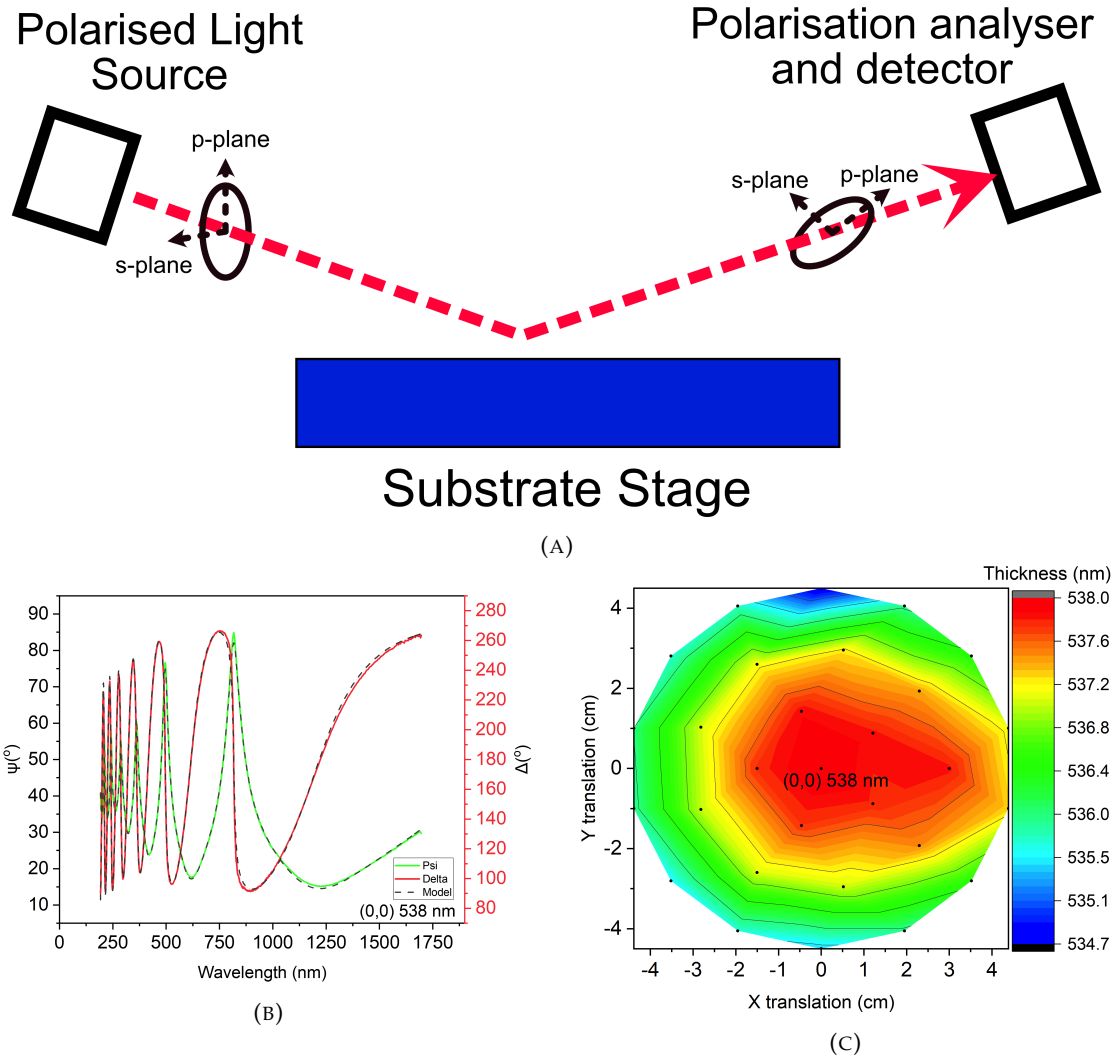


FIGURE 3.2: (A) Representation of the operation of ellipsometry. (B) ψ and Δ values measured at the centre of the wafer and the model used to fit and find the thickness (C) Ellipsometry data showing the thickness of the SiO_2 layer, that was sputtered, in relation to its position on a 4 inch substrate, with the centre data highlighted.

3.2 W Bottom electrode with and without Ti adhesion

The next fabrication step is to deposit the Tungsten (W) bottom electrode, which is done using a standard DC sputterer. The rate of deposition is set within the tool by altering the power input to the target, with the maximum RF power being 700W and the Maximum DC power being 1000W. The rate of deposition from this recipe is estimated using a crystal monitor which must be calibrated using a tooling factor. This is the correction between the thickness deposited on the crystal monitor and the substrate.

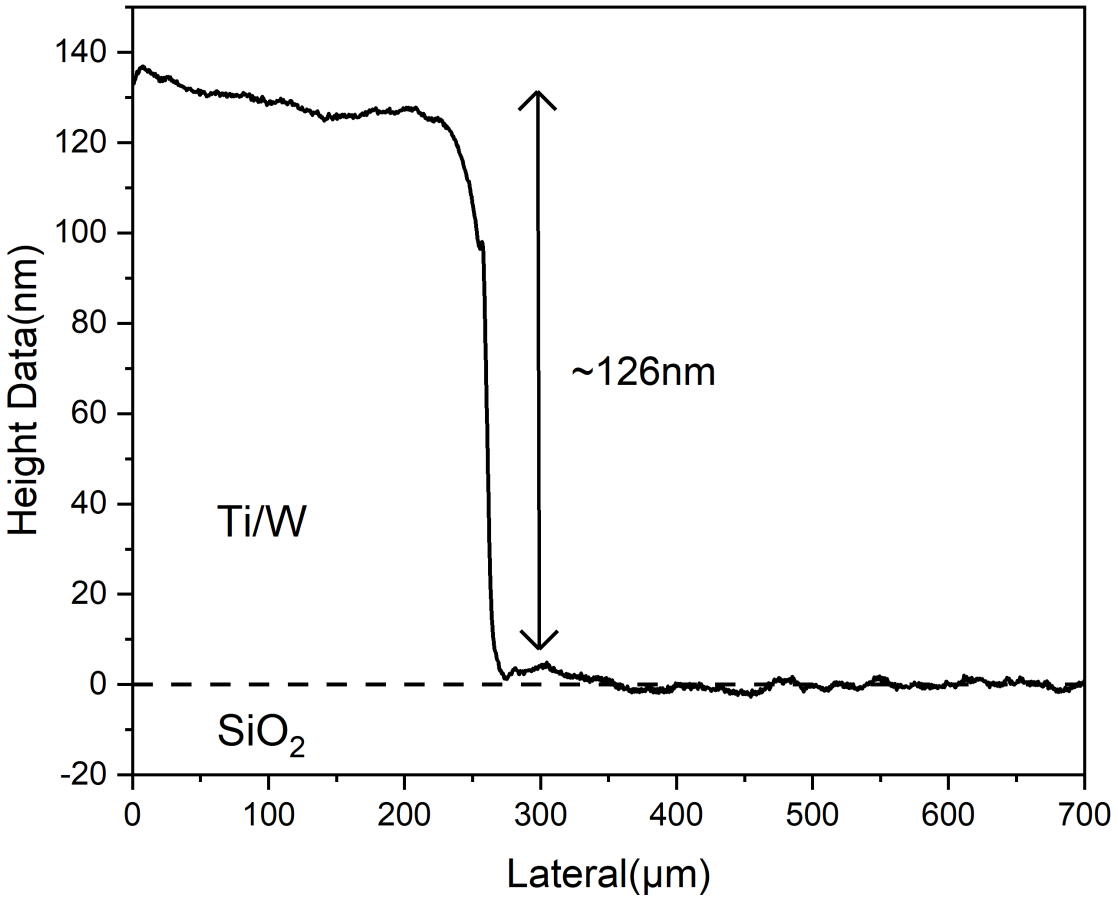


FIGURE 3.3: Height-distance graph showing the step height of the Ti/W bottom electrode on SiO_2, with a combined expected thickness of 130nm and a measured thickness of 126nm.

This tooling factor can depend on several factors including the material being deposited or the distance between the monitor and substrate. To calibrate the crystal monitor I deposited an estimated 100nm of W on a patterned substrate and measured the actual deposition across a 6-inch wafer using a profilometer. This was done using both the DC and RF targets and using equation 3.2 the tool could be correctly calibrated. The deposition conditions used in these final recipes are shown in table 3.2. The overall process pressure for both sources was around 3 mTorr and the substrates were not heated. The targets allowed for 100nm of W to be deposited within 10%. An example of this is seen in figure 3.3, which shows the step height measured using a profilometer. This sample was deposited to have around 30nm of Ti and 100nm of W, both sputtered in the same tool under vacuum and the measured thickness is around 126nm.

$$\text{New Tooling Factor} = \frac{\text{Actual deposition thickness}}{\text{Desired deposition Thickness}} \text{x Current tooling factor} \quad (3.2)$$

The substrate rotation was also investigated briefly. Depositions were conducted between 10 and 30 RPM to look at uniformity. Too high of a rotation (30RPM) would

cause bad adhesion with flakes of the W layer to fall off the substrate. The final rotation was settled to be 15 RPM which gave a uniformity of within 10% across the entire wafer, with the largest difference in thickness of a 200nm deposition being around 20nm and the average thickness being 208nm utilising the DC source. The RF source was able to achieve a uniformity of around 2.5%, however, its deposition rate is extremely low at 0.16A/s. Due to this slow rate, all wafers utilised the DC source for the cells.

TABLE 3.2: Magnetron sputtering recipe settings for the deposition of W using both the RF and DC sources

Target	Power (W)	Ar flow rate (sccm)	deposition rate(nm/s)
RF	210	20	0.016
DC	150	20	0.063

Both the Bilayer and the 2^{nd} Bilayer Wafer used just W for its back electrode. During the high-temperature SiC deposition, it was noted that stress bubbles seemed to form on the surface as shown in figure 3.4. The stress on the wafer appears to be due to the W layer, as we can see thatt the stress has also caused the W to lift off from the substrate, revealing the yellow SiO_2 below it. Therefore, to give the W layer better adhesion to the SiO_2 during the high-temperature process, a Ti layer was investigated and used in the Single layer Wafer.

Four wafers were fabricated using the Ti/W bottom electrode. Two of these wafers had 5nm of Ti and 100nm of W, while the other two had 25nm of Ti and 100nm of W. It was found that the Ti layer greatly reduced the stress bubbles caused by the high-temperature PECVD process, however, there was a slight difference between the 5nm and 25nm Ti wafers. The 5nm Ti layer wafer appeared to produce micron-sized holes in the SiC dielectric as shown in figure 3.5. While some cells still functioned normally the wafer suffered from severe shorts caused by the Cu top electrode coming into direct contact with the W bottom electrode. These shorts were measured by probing two top electrode contacts next to each other and applying a voltage sweep between $\pm 4V$. The 25nm Ti layer wafers, however, do not suffer from these shorts and produce a smooth thin film throughout the deposition. Therefore, we can say that a thick Ti layer is needed to stabilise the SiC deposition during the high-temperature process. Even with the shorts found in the 5nm process, the deposited SiC thin film was still more stable than previous depositions with the W layer remaining adhered to the substrate and no signs that any portion of it had lifted off or any surface bubbling.

Overall the inclusion of the Ti layer greatly improved the adhesion problems caused by the high-temperature PECVD process described in the next section.

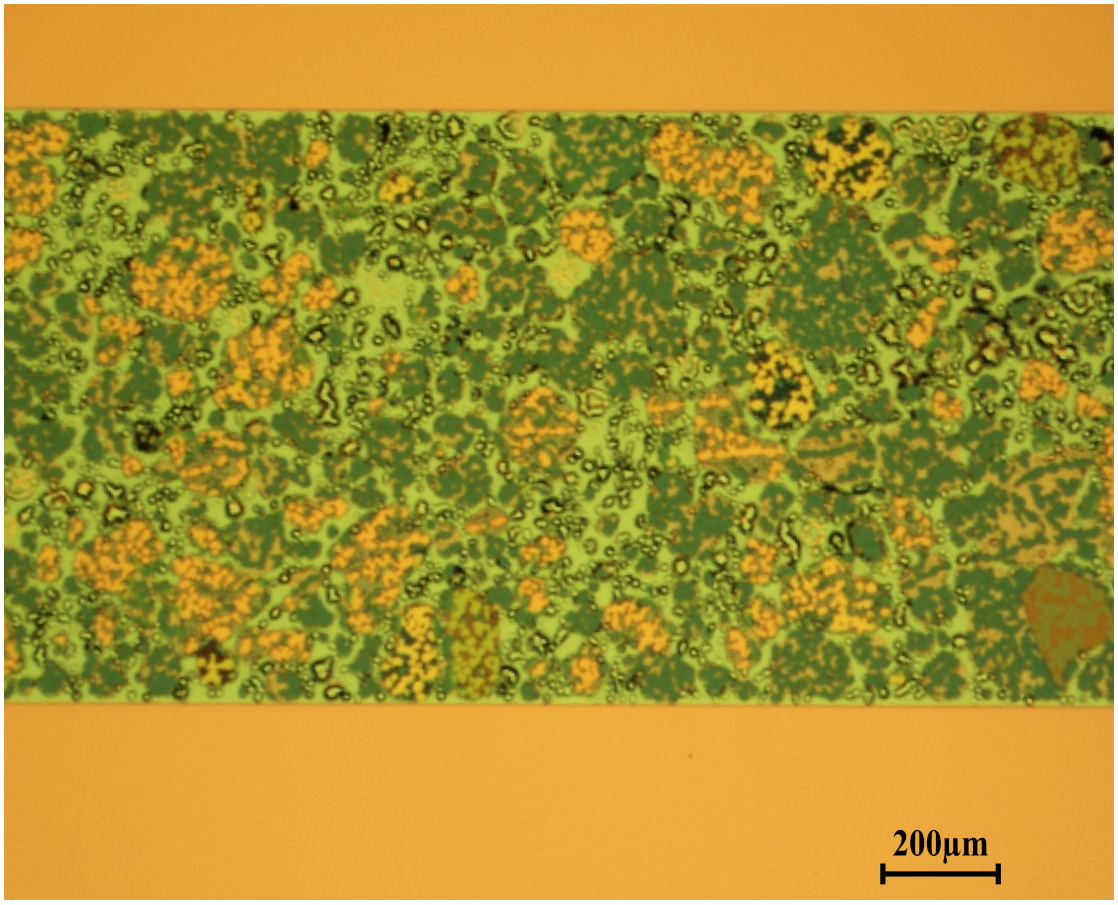
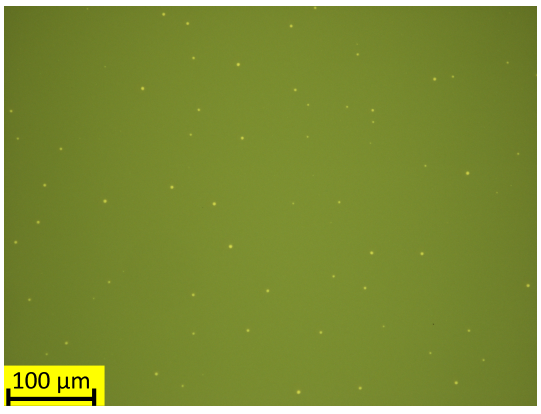
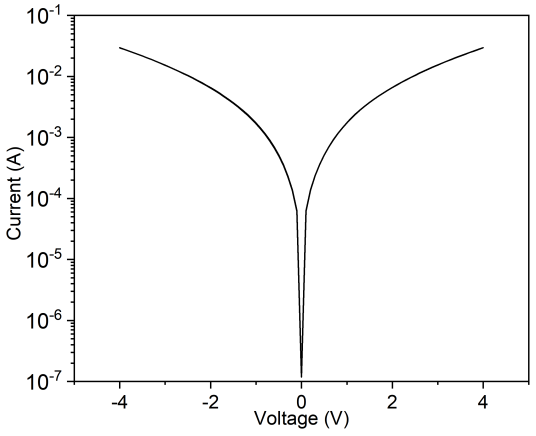


FIGURE 3.4: Optical image of a test structure after the high temperature deposition process, with SiO_2/W/Si/SiC in green and the surrounding SiO_2 in yellow. We can see stress bubbles forming on the W pad and portions of these areas lifting off with the dielectric stack, revealing the yellow SiO_2 below



(A)



(B)

FIGURE 3.5: (A) Optical micrograph of the surface of a 40nm single SiC layer on top of W/Ti, with thicknesses 100 and 5nm (green area). There are no apparent stress bubbles caused by the high temperature process, but instead micron sized holes which reveal the bottom W layer in yellow. These holes cause shorts to form within the cells. (B) I-V sweep from $\pm$4V with the probes connected to two separate 200μm top electrodes next to each other. This IV sweep shows the severe leakages caused by the micron sized holes

3.3 Amorphous Si/SiC deposition

3.3.1 Plasma Enhanced Chemical Vapour Deposition

The SiC dielectric utilised in the three different wafers were all deposited using Plasma Enhanced Chemical Vapour Deposition (PECVD). PECVD is a deposition that utilises reactant gasses that are fed between parallel electrodes, as shown in figure 3.6. The top electrode is connected to an RF source which controls the plasma and rate of deposition. The second electrode is grounded and sits below the substrate. The capacitive coupling between these electrodes causes the input gasses to form a plasma, which in turn creates a chemical reaction. This reaction is deposited on the substrate as a thin film. In general, PECVD is utilised over standard CVD techniques as it can achieve deposition at much lower temperatures ($250 - 350^oC$ instead of $600 - 800^oC$). However, for this process we maintain the high temperatures on the substrate to achieve the desired dielectric thin film. The reason for this increase in temperature is that poly-SiC has been shown to be deposited using PECVD at 600^oC and the crystallinity degree can further be improved by increasing the annealing temperature [162]. My initial goal was to investigate the resistive switching properties of SiC with different grain sizes, as it is understood that grain boundaries in poly-crystalline thin films play a vital role in switching processes [27, 163–166]. In fact it's been shown that ion migration appears to move faster in these grain boundaries than through the interior grains [167]. With this in mind, I had hoped to investigate the confinement of Cu filaments through poly-crystalline SiC, to see if they could improve the resistive switching properties. It should be noted that the PECVD tool that was used for this deposition can to around 900^oC, however, this will be discussed further in the future works section of chapter 7.

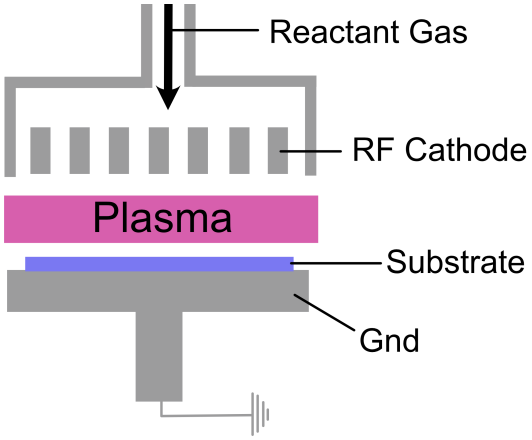


FIGURE 3.6: Diagram showing the operation of a PECVD tool to deposit thin films. Parallel plates between the substrate causes input reactant gasses to create a plasma. This plasma causes a chemical reactions that deposit materials on the surface of the substrate.

These depositions were all conducted at 600^oC, with the Bilayer Wafer deposited at 80 seconds, while the 2^{nd} Bilayer and Single layer wafer were deposited at 70 seconds. This slight change in time was due to a calibration in the deposition rate.

The chamber of the PECVD tool is always kept at 100^oC and the initial process is to ramp the tool to 600^oC after the wafer has been loaded. The ramp rate was altered between the Bilayer and 2^{nd} Bilayer wafer to see if there were any differences in the amount of stress that was caused on the Tungsten layer, however, there was no observable change. The temperature during the entire process of each wafer is shown in figure 3.7a.

The tool then undergoes a gas pre-flow stage where the initial gas conditions of the chamber are set. The deposition is then started for 80 seconds for the Bilayer wafer. However, the time was reduced to 70 seconds for the 2^{nd} Bilayer and Single layer wafers. All of the parameters during the deposition, including the gas flow rates and power are presented in figure 3.7.

The power of the RF generator, for both forward and reflected is consistent throughout the deposition, as well as the flow rates for all of the gas lines. The chamber is cooled down back to 100^oC over 2 hrs, as shown in figure 3.7a. The gas flow rates and power settings are given in table 3.3.

TABLE 3.3: Processing conditions set in the PECVD tool for the SiC deposition at 600^oC.

Gas	Flow Rate (sscm)
SiH_4	15
CH_4	100
Ar (Carrier)	285
RF Power (W)	20
Deposition Time (s)	70

With the similar processing conditions outlined above there are two small alterations between each wafer. The entire fabrication process flow, including all the variations of each wafer is outlined in table 3.4. There are two main differences when accounting for any changes during the deposition of the dielectric layer. However, we must first look at the initial deposition of the Bilayer wafer which was deposited with the chamber filled with over 2μm of nanocrystalline graphene (NCG). The deposition was also conducted on an 8-inch wafer carrier, also containing NCG. This means that the temperature of the wafer would be slightly less than the 600^oC set during the deposition.

The 2^{nd} Bilayer wafer went through a similar process, whereby the chamber had not been cleaned before the deposition. Other depositions had been conducted in the tool before this wafer was processed, so a precondition of NCG was done so that it could be similar to the conditions of the previous chamber. The main difference between the

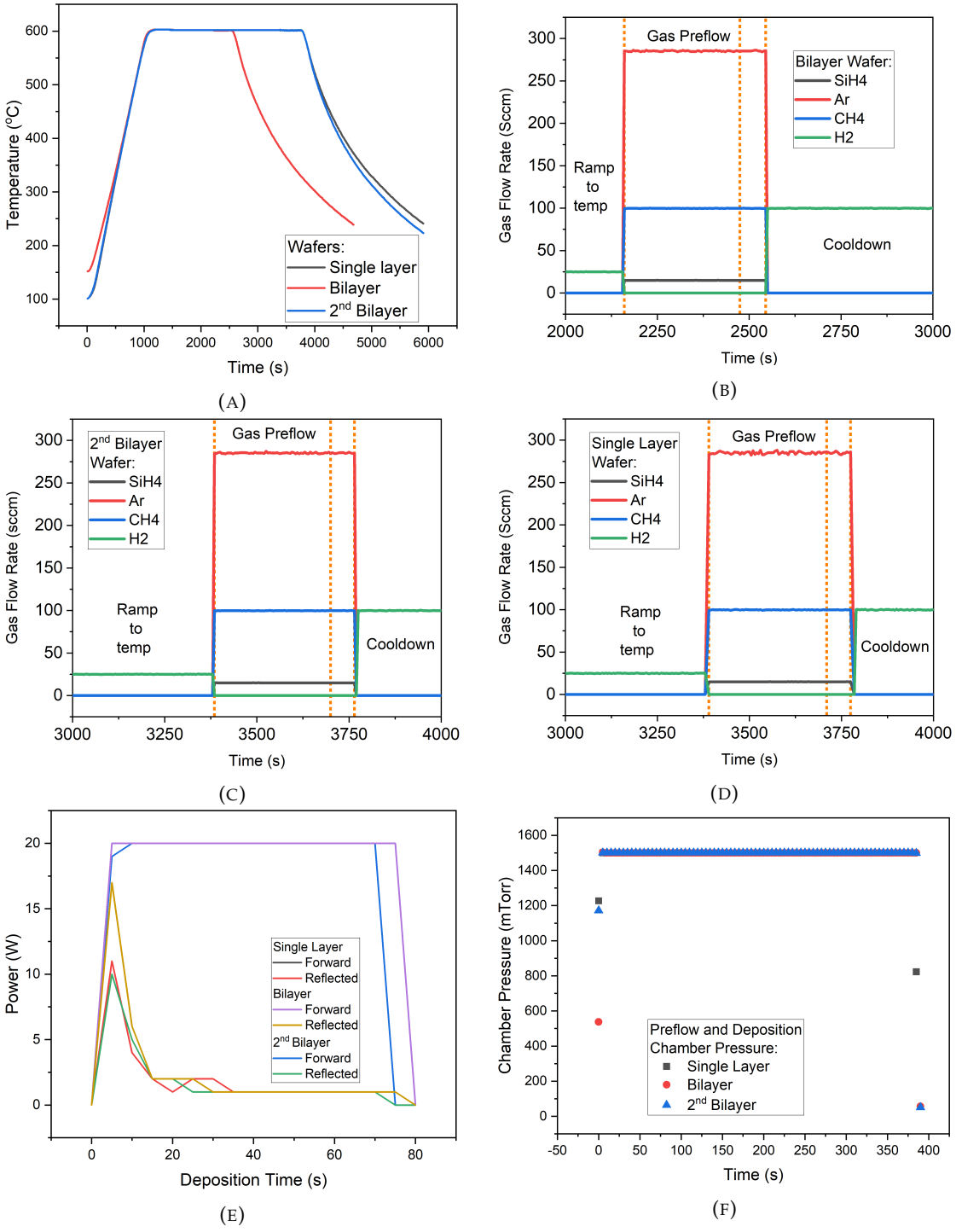


FIGURE 3.7: Conditions of the PECVD tool used during processing (A) Temperatures across all three samples during the entire process. (B) Pre-flow and Deposition of the Bilayer wafer (C) Pre-flow and Deposition of the 2^{nd} Bilayer wafer (D) Pre-flow and Deposition of the Single layer Wafer (E) Chamber pressure during all three depositions (F) Forward and reflected power of the RF generator

two depositions is that this wafer did not use a carrier wafer, but instead was directly on top of the stage at the 600^oC. The thickness of the deposited material remains the same as the Bilayer wafer.

The Single layer wafer was similar to the Bilayer in that it utilised an 8-inch wafer carrier filled with NCG. However, there were two chamber cleans that were done to the PECVD before the deposition took place. The first being before the March COVID shutdown and again in June when the building reopened. A wafer was fabricated with NCG to see if the difference between the bilayer and single layer was due to the NCG deposition. However, it was found that the addition of NCG in the PECVD did not effect the deposition of the single layer wafer. The difference in the dielectrics of the single layer and bilayer will be discussed later in this chapter and was analysed through TEM imaging, as well as EDX and XPS mapping. A discussion on the possible reasons for the difference in the deposition is also discussed later in this chapter.

TABLE 3.4: Process conditions that vary between the SiC deposition of the three wafers discussed in this section

Process Conditions	Bilayer	2^{nd} Bilayer	Single layer
Ti adhesion Layer	No	No	Yes
NCG Wafer carrier	Yes	No	Yes
Pre Chamber clean	No	No	Yes
W opening windows	Shadow Mask	Etch	Etch
Final Thickness (nm)	100	100	40

3.3.2 Material Characterisation

To look at the composition of the SiC deposited using the processes described above a sample of the Bilayer wafer was characterised using X-ray diffraction (XRD), X-ray photoelectron spectroscopy (XPS) and Raman Spectroscopy. The Bilayer, 2^{nd} Bilayer and Single layer wafers also underwent imaging using a transmission electron microscope (TEM), along with energy dispersive X-ray mapping (EDX). This section will focus on the material characterisation of the thin films using these processes.

3.3.2.1 Energy Dispersive X-ray

Energy Dispersive X-ray (EDX) is generally used alongside SEM and TEM imaging to identify compositions at specified locations. For this use we have explored EDX alongside TEM imaging techniques.

EDX works with TEM systems as the generated e-beam that is used knock electrons from the inner shell of an atom. Electrons in higher shells get attracted to the positive

hole left behind and the drop to the lower energy state. This transition release a characteristic X-ray photon and is unique to the atom. The EDX detector can analyse this and produce a map of atomic concentrations, which is overlapped with the TEM image. Figure 3.8 shows an illustration of this phenomenon for reference.

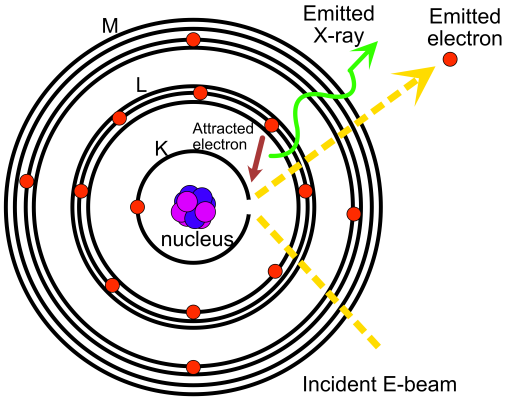


FIGURE 3.8: Illustration of how SEM/TEM e-beam can produce characteristic X-rays that are used to detect atomic percentages across a map, using an EDX detector.

Looking at the TEM and EDX mapping of figures 3.9a and 3.9c, we can that the Single layer wafers have a SiC thickness of around 40 nm. We can also see that the Ti adhesion layer is roughly 25nm. The interface between the SiC and Cu layer also appears to have a large oxidation peak. This peak is also visible between the W and SiC layer. This oxidation is not present in the 2^{nd} Bilayer wafer shown by the TEM and EDX map in figures 3.9b and 3.9d.The Single layer sample also shows that the SiC dielectric is possibly Silicon rich.

The 2^{nd} Bilayer wafer in figures 3.9b and 3.9d show that the dielectric deposited is in fact a bilayer. At the W interface there is around 50nm of silicon, followed by another 50nm of SiC. Looking at figure 3.7 we can clearly state that the processing gases, power and temperature are not that factors involved with the changes in the dielectric. One possible explanation is the use of the Ti adhesion layer in the Single layer devices. The reduction in stress caused by the Ti adhesion layer could could have caused an alteration in the surface chemistry making it more energetically favourable to first deposit Si. Unfortunately, due to limited time this could not be fully explored and so is outside the scope for this thesis.

To further analyse this process would have to go further investigations in both fabrication of dielectrics and TEM/EDX mapping. Due to the COVID pandemic it was only possible to compare the XPS data of the Single layer and Bilayer wafer. Raman and XRD analysis was only able to be conducted on the Bilayer wafer.

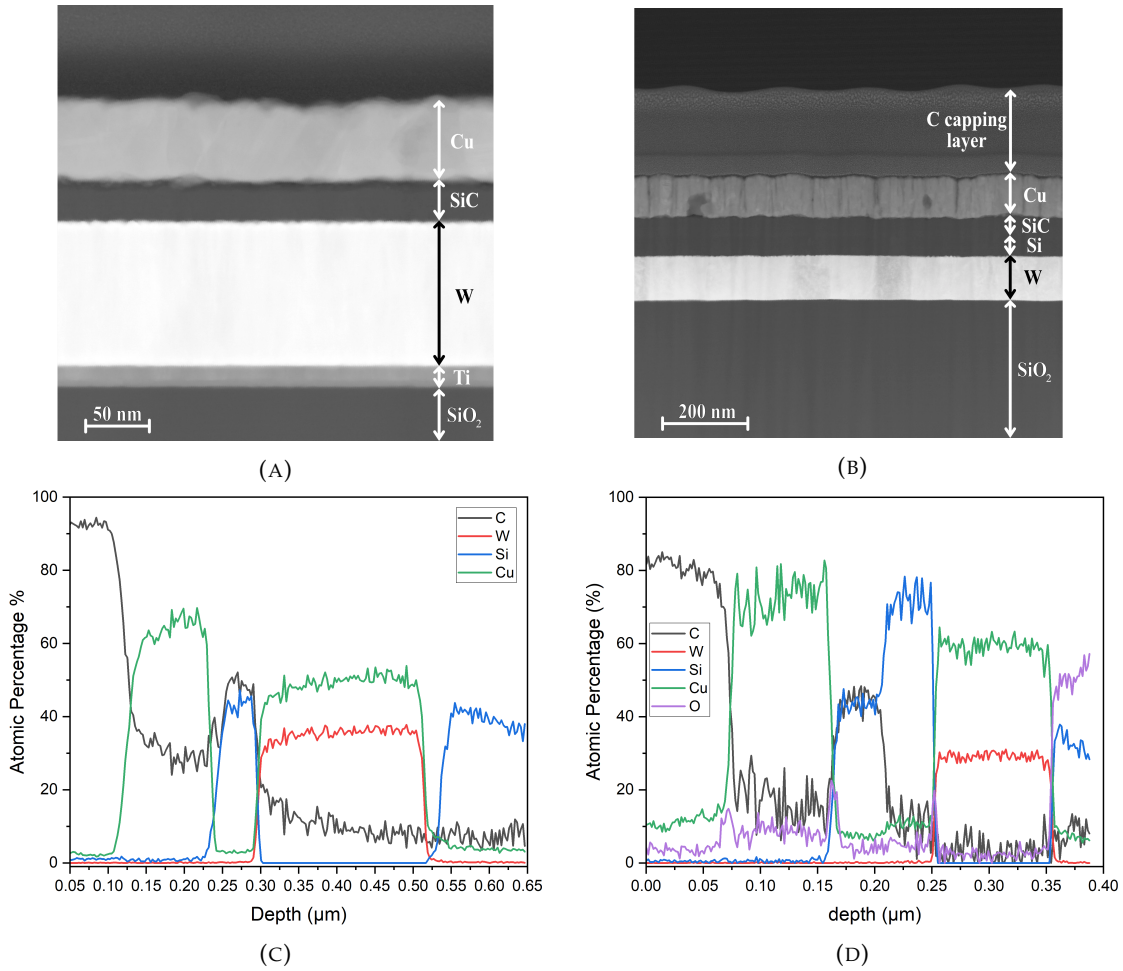


FIGURE 3.9: Transmission Electron Microscopy cross-sectional micrograph of a single cell from a (A) Single layer cell (B) Bilayer cell. Associated Electron Dispersive X-ray Cross-sectional mapping of (C) Single layer cell (D) Bilayer cell. All TEM images in this thesis have been taken by Yisong Han and Richard Beanland in the University of Warwick.

3.3.2.2 X-ray Diffraction

X-ray Diffraction (XRD) is used to identify materials through diffraction patterns and can show deviations in structure from ideal materials, due to stresses and defects.

Materials with a crystal lattice have a specific structured arrangement of atoms. Incident X-rays can interact with the electrons of the structured atoms causing elastic scattering. The majority of the scattered X-ray waves are cancelled out through destructive interference, whilst the rest constructively interfere. These constructive interferences produce a diffraction pattern that is determined by Bragg's law 3.3.

$$2dsin(\theta) = n\lambda \tag{3.3}$$

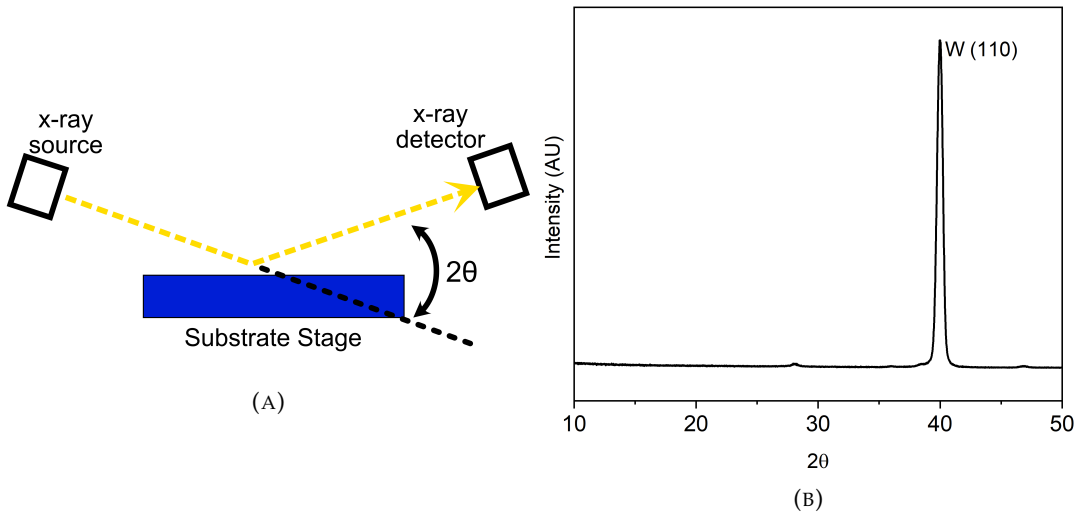


FIGURE 3.10: (A) Representation of the operation of X-ray Diffraction which measures grazing diffraction when an incident X-ray is scattered across the surface of a substrate. (B) X-ray diffraction measured on the Bilayer sample, showing that the SiC layer deposited being amorphous, with the lack of any SiC crystalline peaks. The large peak at 40^o is caused by the 110 W below the SiC layer.

Where d is the spacing between diffracting planes, θ is the incident angle, λ is the beam wavelength and n is an integer. Generally, only the primary diffraction maximum is considered in the analysis which means that n=1. The constructive interference angle alters depending upon the different crystal orientations and materials. Therefore, observing and analysing this diffraction pattern can reveal any potential crystalline material properties.

For this measurement, a grazing diffraction XRD was used, which involves using a small incident angle for the incoming x-rays and so the diffraction pattern is most sensitive to the surface level scattering. Using this technique we can determine whether the SiC thin film deposited is amorphous or crystalline.

Looking at figure 3.10b we can see that there is only a single major peak at 40^o. This is attributed to a 110 W peak, which was below the SiC layer when the measurements were conducted [168]. To confirm if the SiC is crystalline, we should be able to see peaks at 35.6^o and 41.4^o for 3C-SiC with orientations 111 and 200, respectively. Other orientations have peaks with much lower intensities at 59.9^o, 71.7^o, 75.4^o [169]. As well as this the poly-type 6H-SiC should show peaks at 34.2^o, 38.2^o, 65.8^o and 73.6^o [170]. In this figure we can see that these peaks are non-existent in this data set and so we can say that the SiC dielectric is amorphous. This is to be expected as crystalline SiC films are usually annealed at temperatures greater than 700^oC, with annealing at lower temperatures between 250 and 700^oC for up to 10hrs has shown only minor density changes [171].

3.3.2.3 X-ray Photoelectron Spectroscopy

X-ray Photoelectron Spectroscopy (XPS) utilises the photoelectric effect to identify elements and their bonds that exist within a surface material. X-rays are bombarded on the surface of the material, whereby core-level electrons can interact with the incident photons. These electrons are ejected from its orbital shell and combined with the energy from the photon, escapes the atom, as shown by figure 3.11a. This electron is now known as a photoelectron and has the energy equivalent to the energy of the incident photon minus the binding energy of the electron. The energy of the ejected photoelectrons are then measured using a detector and using the photoelectric effect equation, rearranged in eqn 3.4, we can calculate the binding energy of the electron.

$$T_{binding} = hv - T_{Kinetic} - \varphi \tag{3.4}$$

Where $T_{binding}$ is the binding energy of the electron, h is planks constant, v is the frequency of the incident photon, $T_{Kinetic}$ is the kinetic energy of the electron that is measured and φ is the work function which accounts of the energy that is given up by the photon electron as it gets emitted and absorbed by the detector. φ is a constant that does not need to be considered for this chapter.

Figure 3.11b shows the XPS survey spectra of a sample taken from the Bilayer wafer. To obtain this data 6 samples were measured and etched every 20 seconds, up to a minute, and the composition of the Si 2p, C 1 s and O 1 s peaks were observed from the survey to calculate the composition. This data is presented by table 3.5.

TABLE 3.5: X-ray photon-electron Spectroscopy data showing the average atomic composition over 6 samples that were etched 4 times to compare the surface and internal composition.

Etching time (s)	Avg Atomic Si %	Avg Atomic C %	Avg Atomic $O_2(\%)$
0	44.2	29.4	26.3
20	68.7	26.0	5.3
40	67.3	29.0	3.7
60	70.0	27.4	2.6

On the surface of the wafer there appeared to be a strong O 1s peak in the survey indicating surface contamination. Once this area had been etched the O 1s peak dropped down to below 5% as shown by figure 3.11b. As shown by this figure there are strong C1s and Si2p peaks. Looking further at the C1s peak in figure 3.11c there appear to be two main peaks. The first at around 284 can be attributed to a-carbon contamination randomly incorporated within the film [172]. This is a standard peak that is to be expected and is due to the exposure of the thin film to the atmosphere. From this separate peak we can already say that there is not a high concentration of carbon atoms, as, with an increase in the carbon in the thin film, the C1s peak should shift and become more

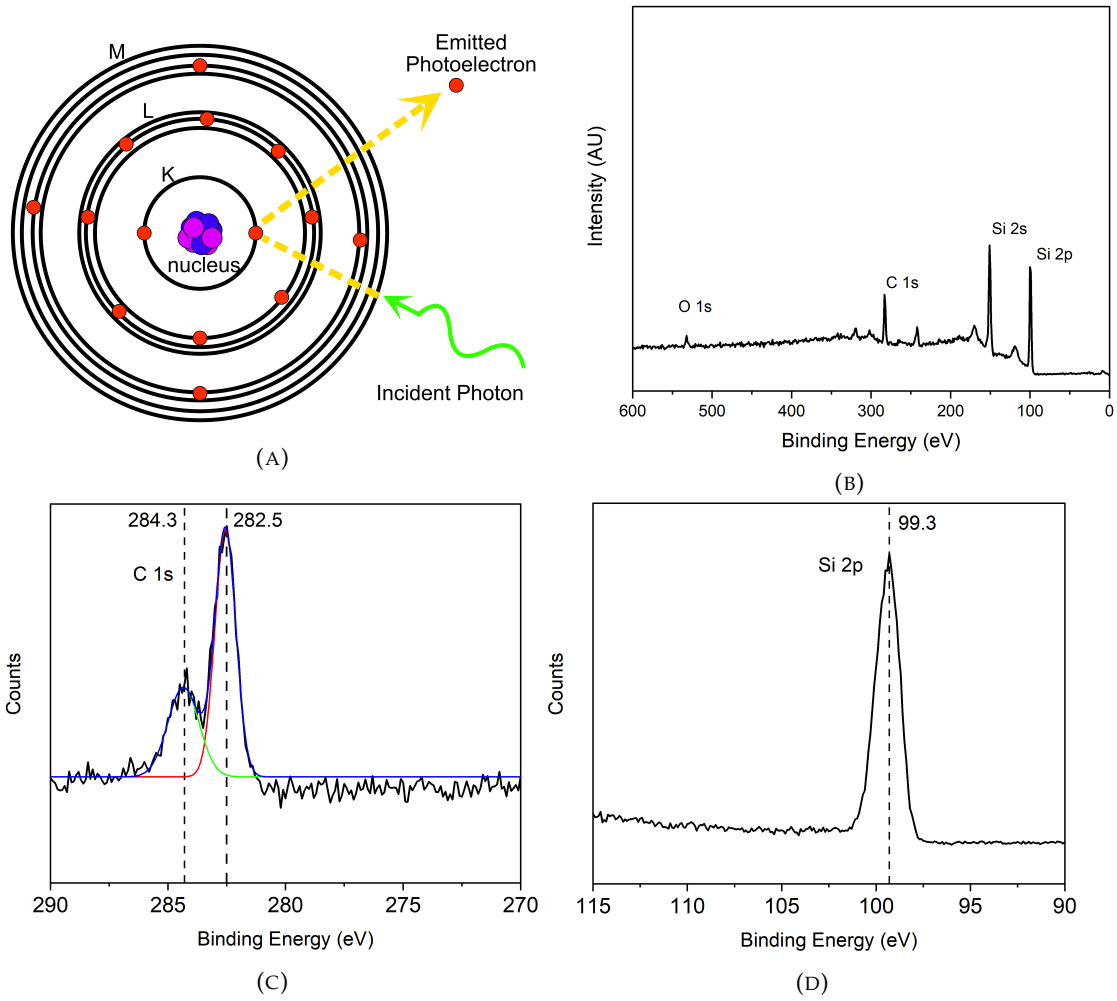


FIGURE 3.11: (A) Diagram showing the photoelectric effect with an incident photon transferring enough energy to a core electron for it to be ejected from the atom as a photoelectron. (B) Full XPS data measured on the Bilayer wafer, showing strong C 1s and Si 2p peaks, with low Oxygen contamination. (C) and (D) Zoomed XPS data of the peaks responsible for the Carbon and Silicon atoms in the material, respectively. (C) The split peaks show low Carbon concentrations (D) shows a strong a-Si:H peak that is due to the high concentrations of Si. Overall the data presents a 7:3 ratio of Silicon to Carbon

overlapped with this contamination peak. Further analysis of the graphs shows that the normal binding energy of the a-C:H is around 284.8 eV, however, with $a - Si_xC_{1-x}$ as x increases the value of shifts towards 282 eV, with a concentration of x= 0.9 being around 282.7eV. Therefore, we can say that there is a low concentration of carbon atoms.

Looking at figure 3.11d we can see a single peak at 99.3 which represents an a-Si:H peak [172]. This shows that there is a high concentration of Si atoms. If the film had a reduced amount of Si atoms, for example in a sputtered sample x =0.5, the peak would shift towards 100 eV.

With these peaks analysed we can finally look at table 3.5 which presents the atomic concentrations from the measured XPS data and figure 3.12 which shows the atomic

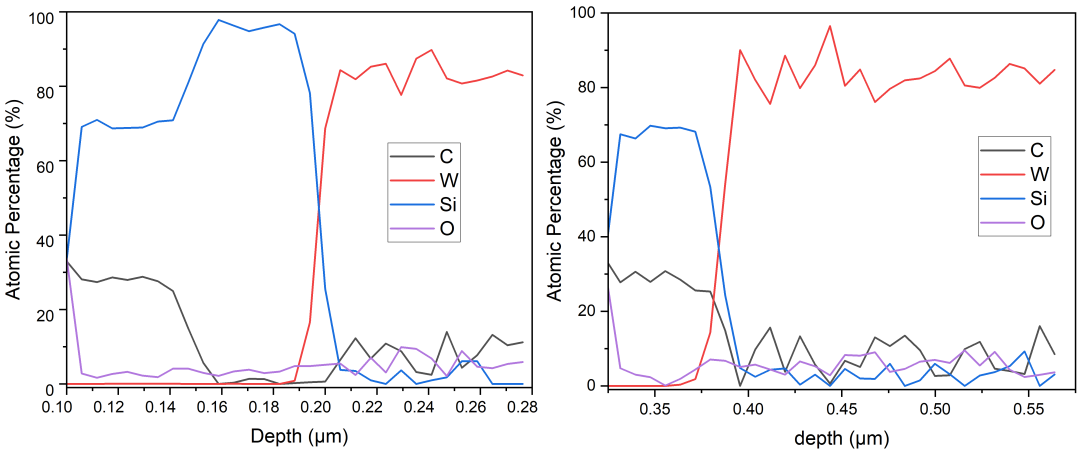


FIGURE 3.12: Atomic percentage of the dielectric thin films and W bottom electrode taken from data collected by X-ray Photoelectron Spectroscopy on a sample taken from the (A) Bilayer (B) Single layer Wafers.

percentage against depth. It was found that the Bilayer wafers had a bi-layer structure, whereas the Single layer samples only had a single thin film. The top half of the bi-layer showed a composition of Si to C at a ratio of 7:3. The thin film below this was only made up of Si. The single layer in the Single layer memory devices exhibited a similar 7:3 Si to C atomic composition. This is in keeping with literature as we used a 1.5:10 ratio of Silane to Methane and it has been shown that increasing this ratio from 1:10 to 2:10 causes the a-SiC thin film to become Si rich [173]. To further investigate the material properties and analyse the bonding structures of the thin film Raman Spectroscopy was investigated on the samples.

3.3.2.4 Raman Spectroscopy

Raman spectroscopy is used to determine the vibrational modes of molecules, providing a structural fingerprint that can be used to determine the composition and information about the bonding of the atoms. When an incident photon of light interacts with a molecule it causes the excitation of electrons to a virtual energy state. This virtual energy state is not stable and so the electron will eventually fall back down to a lower energy state and release a photon. When the energy of the scattered photon is equal to the incident photon it is known as Rayleigh scattering (or elastic scattering). If the energy is greater than or less than the incident photon this is known as Anti-Stokes and Stokes Raman scattering respectively (or inelastic scattering), figure 3.13b.

Therefore, by looking at the Raman shift, shown by equation 3.5, we can effectively look at the energy gap between the vibration levels of the molecule. Where Δv is the wavenumber Raman shift in cm^{-1}, λ_0 is the wavelength of the incident photon (nm),

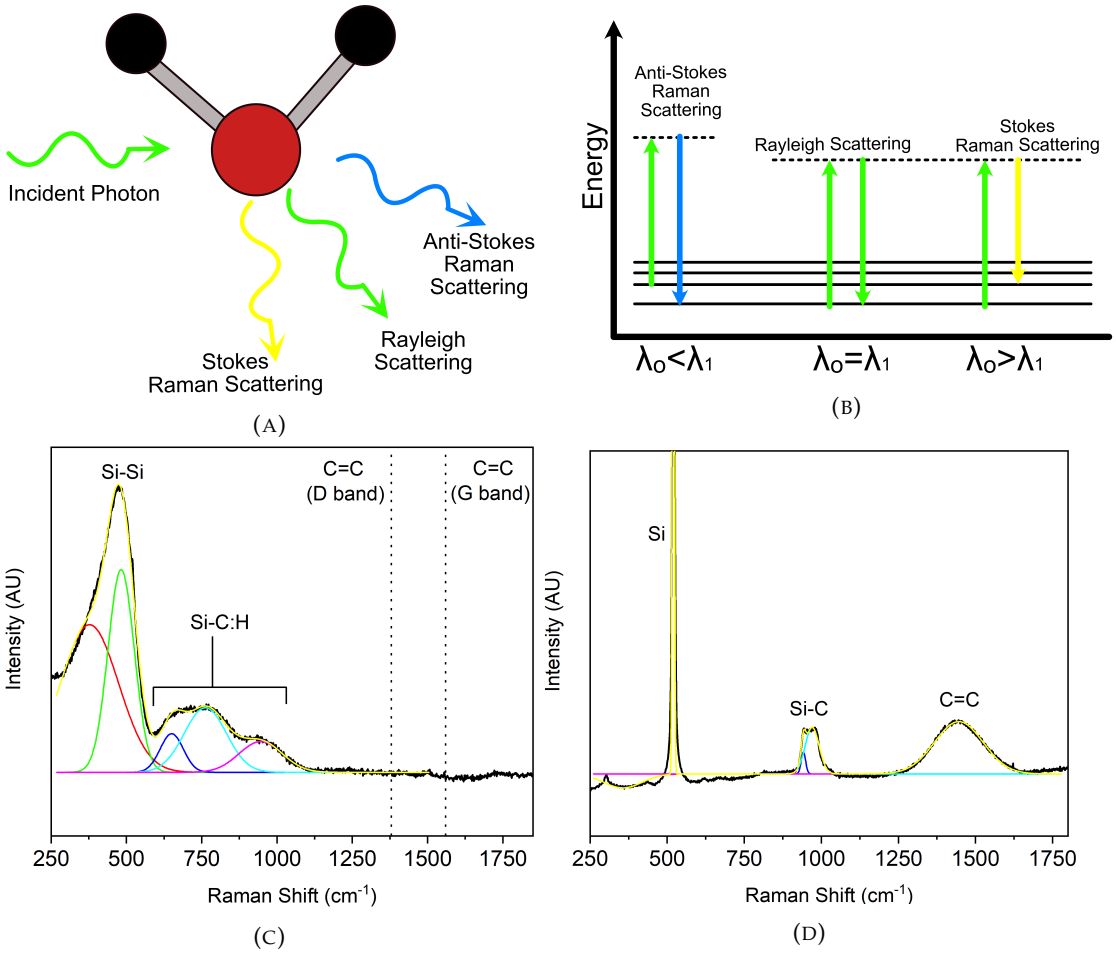


FIGURE 3.13: diagram Showing (A) an incident photon and the three possible types of scattering; Rayleigh, Anti-Stokes and Stokes Raman Scattering. (B) the excitation of the electrons, from an incident photon, and its subsequent drop in energy state releasing a photon. Depending on the type of scattering the electron will fall to an energy greater than, equal to or less than it's original energy level. (C) Raman spectroscopy of the Bilayer wafer which shows Si-Si bonds, Si-C bonds but no graphitic bonds. (D) Raman Spectroscopy of a sputtered SiC sample which shows the graphitic bonds, stronger Si-C bonds, but weaker Si-Si bonds. These alterations are due to the high concentrations of Si, relative to C, in the Bilayer wafer, whereas the sputtered sample has a ratio of 1:1, Si:C.

and λ_1 is the wavelength of the inelastic scattering (nm).

$$\Delta v = (\frac{1}{\lambda_0} - \frac{1}{\lambda_1}) \tag{3.5}$$

Figure 3.13c presents the data measured on the Bilayer wafer. Graphite D and G bands are centred around 1380 and 1560 cm^{-1} and in these samples are minimal. This is attributed to the low C concentration compared to Si [174]. The Si-C bonds are found in the wide bands centred around 800 and 970 cm^{-1}, which represents the Transverse Optical (TO) and longitudinal optical (LO) vibrations respectively. Around 970 cm^{-1}

there could also be some second-order Si-Si TO vibration modes [175]. The weak peak around 650 cm^{-1} can be seen as the Si-H wagging and the second-order Lateral Acoustic (LA) mode of the Si-Si vibration. There is also a spike at 519cm^{-1} which is attributed to the crystalline Si bonds below the SiC thin film.

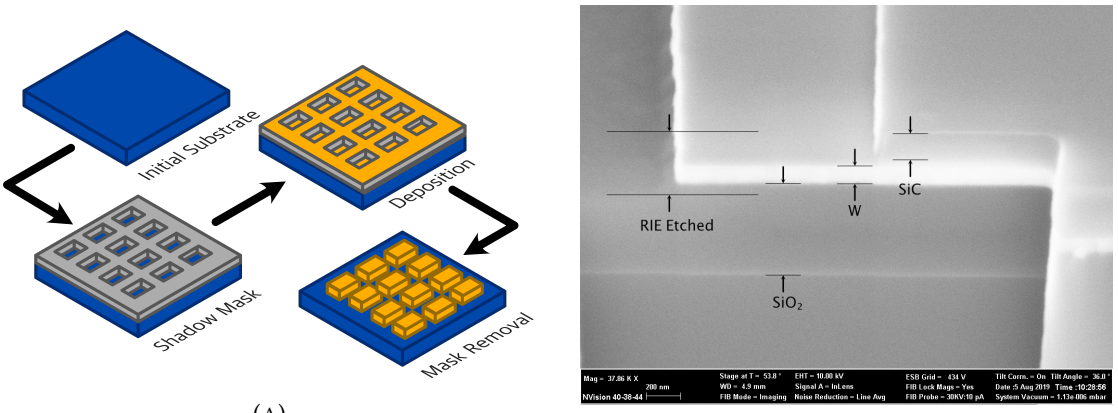
The wide-band centred around 480 cm^{-1} represents the Si-Si bonds in the amorphous state with a first-order scattering of TO modes. As the amount of Si reduces this peak should also reduce until it disappears when the amount of Si and C are equal. This is shown by figure 3.13d which shows the Raman peaks measured from a 1:1 SiC sputtered sample.

Overall the material characterisation of the PECVD thin film shows that we have an amorphous thin film for the SiC layer with a Si to C ratio of around 7:3. There is also evidence for the Si layer below this thin film, for the 100nm dielectric used in the Bilayer and 2^{nd} Bilayer wafers.

3.3.3 Patterning Bottom Electrode Windows

Once the cells have been fully fabricated there needs to access to the bottom W electrode. If at this point we were to simply apply a top electrode, the cells that we have fabricated could not be measured as there is no way to contact the bottom electrode. This is because the PECVD technique described above deposits the material across the entire wafer and due to the high temperature process it is not possible to pattern the wafer before with resist. Therefore, there needs to be a method to allow a portion of the wafer free from both the SiC dielectric and the top electrode, so that we can contact the W for electrical measurements. To pattern windows they would either have to be done using a shadow mask during deposition or patterned and etched after the deposition was done. The Bilayer wafer utilised the former while the 2^{nd} Bilayer and Single layer wafers used the latter as shown by table 3.4.

A shadow mask is a patterned material that is placed physically on top of the substrate before it is moved into the deposition chamber. It patterns the substrate below by blocking the deposition from occurring in unwanted areas which are given in figure3.14a. While this process is extremely quick, compared to standard lithography techniques, it cannot create a sharp feature and has problems with accurate alignment. As this is the first patterned layer the accuracy in where the patterns are positioned is not an issue. As well as this the patterns being created are to allow the bottom contact to be exposed and are not for features being deposited. This means that well-defined features are not a priority. However, a change in the fabrication design, so that further testing such as TEM imaging could be conducted, meant that the 2^{nd} Bilayer wafer and Single layer wafers were designed to utilise photolithography and etching. This was so



(A) (B)

FIGURE 3.14: (A)Diagram showing the lithography technique using a shadow mask, which was used for the Bilayer wafer in the high temperature PECVD process. The patterned mask is placed within the deposition chamber and blocks the unwanted areas being deposited with material (B) SEM showing the initial development of the RIE for the SiC layer, with the first recipe etching the SiC layer and 100nm of W in 5 minutes.

that the fabrication process could utilise the better alignment from photolithography to fabricate $1cm^2$ chips across the wafers.

The photolithography step utilised a positive resist and light field mask. These process conditions will be further described in the next section. This section, however, will focus on the etching process that was developed for SiC. With the help of Dr Libe Totorika, the SiC etch recipe was initially developed from a review paper looking at the review of Reactive ion etching of crystalline SiC in Fluorinated plasmas [176]. Initially, the gases flow rates presented in table 3.6 were used with a power of 100W. However, this proves to have an extremely high etch rate. This can be seen in figure 3.14b, in which a test was done using a wafer with around 270 nm of SiC, 100 nm of W and 500nm SiO_2. During a 5 minute test run the wafer was etched to the bottom SiO_2 insulating layer. This extremely fast and is thought to be since the SiC film is amorphous and not crystalline as the literature review looked at.

Due to the etch rate being partially tied to the power input of the plasma, the power was set to 50W and it was found that 100nm of the SiC could be etched in 1 minute. While this is can still be considered an extremely fast etch, it was able to be used with our process flow given that the thickness of the normal resistive switching cells was also 100nm. These final settings are given by table 3.6 below.

TABLE 3.6: Processing Conditions of the RIE etch, giving 100nm etch in 60 seconds

Process Conditions	Gas Flow Rate (sscm)
O_2	2.5
CF_4	47.5
Forward Power (W)	50
Time (s)	60

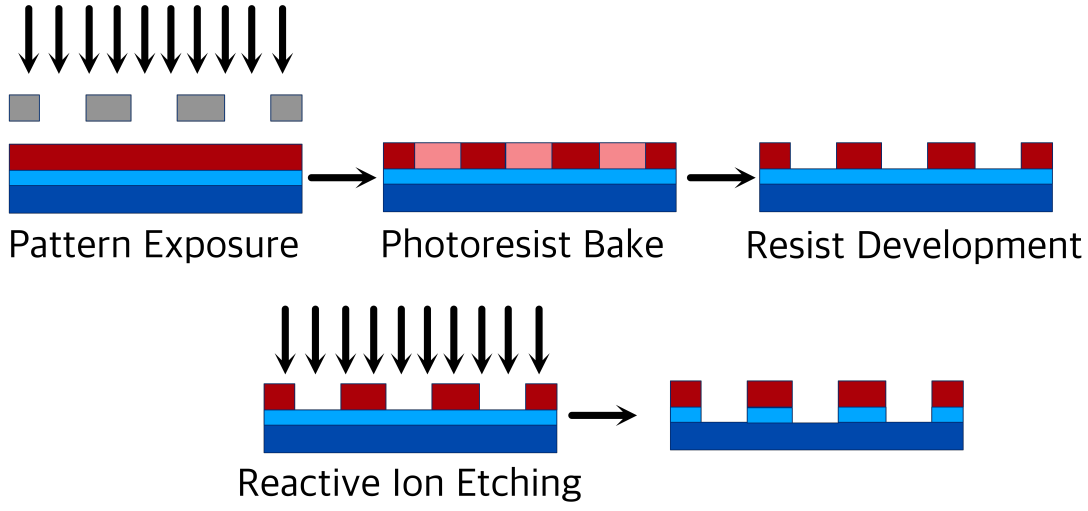
3.4 Cu top electrode

3.4.1 Photolithography layout

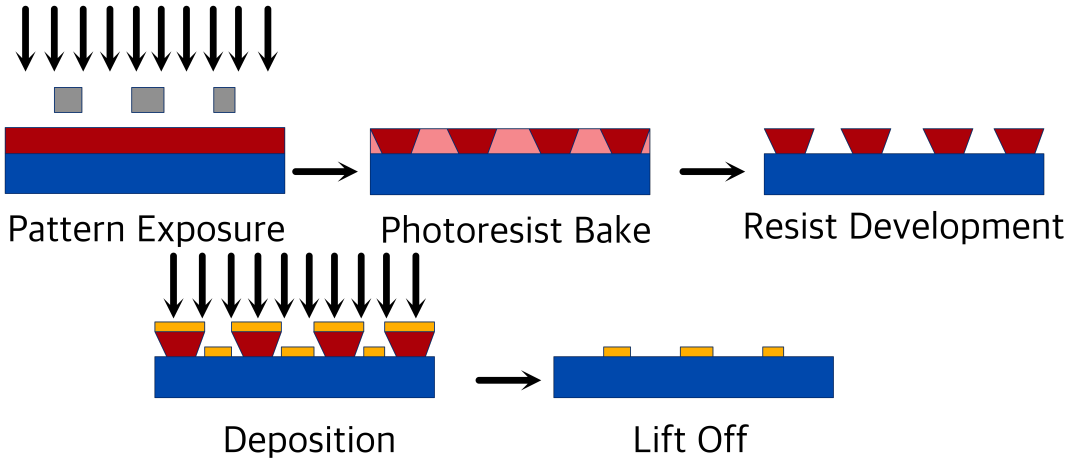
The top electrode was patterned using photolithography, which is a technique in which a pattern from a photomask is transferred on top of a substrate to a photosensitive material known as a photoresist. There are two types of photosensitive materials that can be used and are known as a positive and negative resist. Positive resist is initially insoluble material which becomes soluble in the presence of light, figure 3.15a. Negative is the exact opposite in that light causes the material to become insoluble figure 3.15b. These opposite reactions with light also affect the sidewalls of the patterned photoresist and make them suitable for different tasks. Positive resist patterns have vertical sidewalls which make them perfect for dry etching techniques for pattern transfers, which was used for the SiC etch recipes 3.15a. These sidewalls, however, are not optimal for use with deposition and lift-off processes. This is because they allow the deposition within the patterned region to still be partially connected to the layer on top of the photoresist. Therefore, when the lift-off process occurs the edges of the patterned regions can be deformed as shown by figure 3.16a which shows rounded corners on large 100μm square patterns. This is especially a problem for smaller features that can be completely lifted off from the substrate.

As the photoresist material is also insoluble in the areas that have not been pattered it can also cause re-deposition which does not allow for a clean lift-off. This can also be seen in figure 3.16a in which the patterned areas are the squares and circles, while the other shapes are redeposition of the Cu caused by using a positive resistive with a lift-off process. This image is taken from the Bilayer wafer which utilised the positive resist S1813 to pattern its top electrode. These patterns created circle and square cells ranging in diameter from 100μm to 10μm, however, the problems associated with the lift-off process meant that it was not possible to probe cells smaller than around 40μm. As well as this only the square cells were measured. An example of the photomask pattern is presented in figure 3.17a.

The 2^{nd} Bilayer and Single layer wafer moved away from this process and instead utilised a negative resist. Using negative resist the sidewalls have a sloping profile



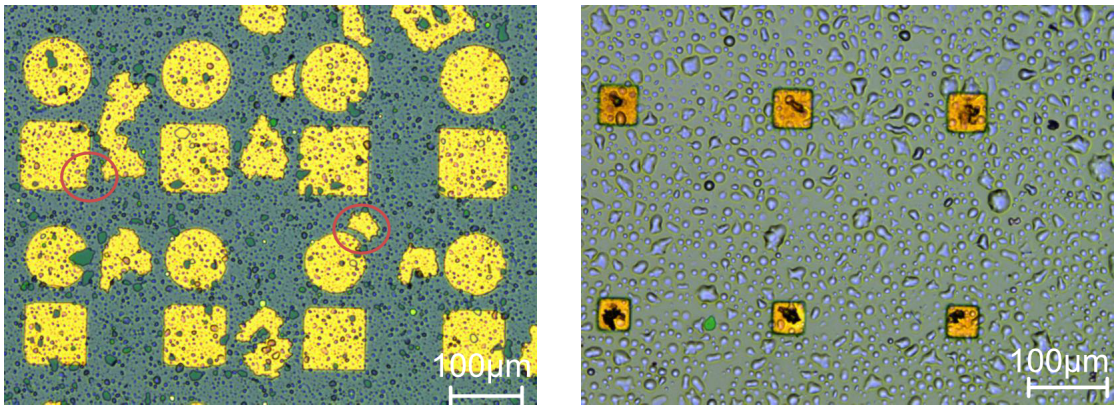
(A)



(B)

FIGURE 3.15: Process diagrams of photolithography to show the differences between positive and negative resist. (A) shows positive resist and the extremely vertical sidewalls that can efficiently pattern transfer etching processes. (B)shows negative resist and the sloping sidewalls which make deposition and lift off processes easier and without any issues that the vertical sidewalls of positive resist would cause.

as presented in figure 3.15b. This means that during the deposition there is no way for the layers to connect from the substrate to the photoresist. This allows for a clean lift-off and hard edges as shown by figure 3.16b which shows the top electrodes of the 2^{nd} Bilayer wafer. The 2^{nd} Bilayer and Single layer wafers both utilise the negative resist AZ2070 to pattern its top electrode. These patterns created square cells with diameters ranging from 200μ to 10μm. These patterns also were arranged in such a way that $1cm^2$ chips could be created and each chip was easily defined across a 4 and 6-inch wafer. The individual cells were also labelled so that each cell across an entire wafer could easily be monitored using a simple naming convention. This was done by providing each chip with a specified number depending if it was in the 4 or 6-inch area. The cells



(A) (B)

FIGURE 3.16: Optical images showing the comparison using a positive and negative resist for the lift off process of the top electrode. (A) uses the positive resist S1813 and the red circles indicate the areas of re-deposition and where the edges of the lift off have failed (B) uses a negative resist AZ2070 and shows a clean lift off process without any issues seen when using s1813. The dark areas seen on the electrodes occur once a cell has been measured

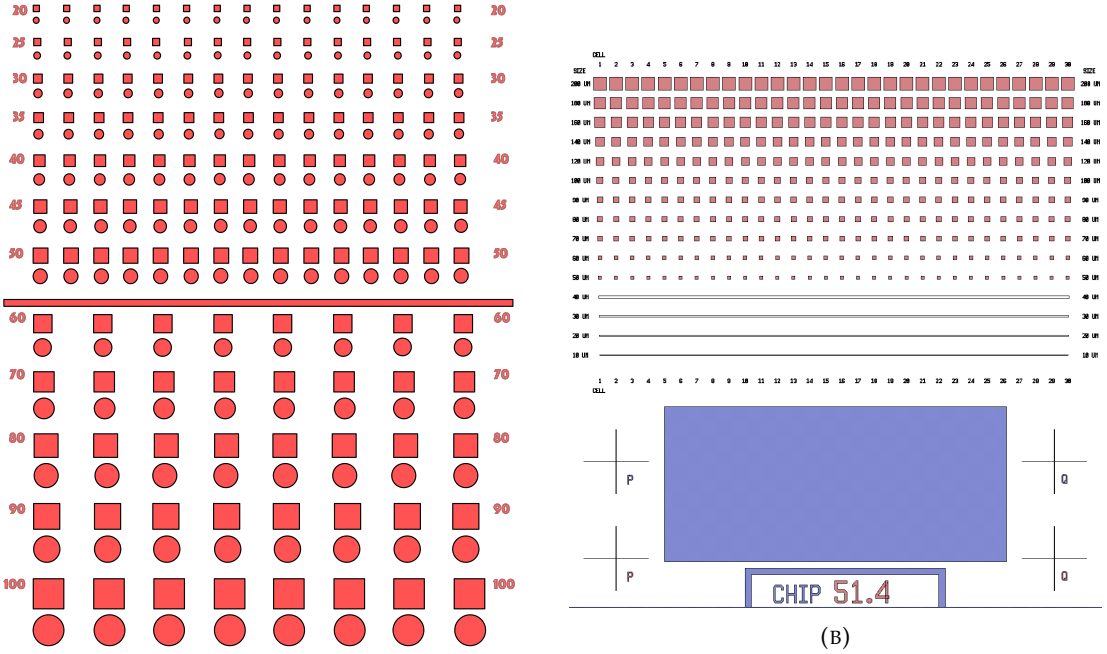
with the same sizes are kept within the same row and each column is labelled from 1 to 30. Therefore, the names of each cell are as follows: Wafer Name, Chip Number, cell Row (Size) and cell Column (number). An example of this chip is given by figure 3.17b. The processing conditions of both the S1813 and AZ2070 that was used is presented in table 3.7.

TABLE 3.7: Processing conditions used for the entire fabrication when using either positive or negative resist.

Processing Conditions	Positive Resist (S1813)	Negative Resist (AZ2070)
Spin Speed (RPM)	6000	6000
Prebake temperature/time (s)	$115^oC/60$	$110^oC/60$
Exousre time (s)	2.5	10
Post Bake	N/A	$110^oC/60$
Developer/time (s)	MF-319/45	AZ726MIF/90

With the top electrodes patterned it is first important to note that the high-performance wafer was fabricated using a 6-inch wafer. However, the sputter tool described below can only hold a 4-inch sample. Therefore, this wafer was hand-scribed to allow it to be able to fit into the tool and subsequently the 2^{nd} Bilayer and Single layer wafers were moved to 4-inch substrates. Following this final was to deposit the top 100nm Cu electrodes. The Bilayer and the 2^{nd} Bilayer Wafers utilised a Magnetron Sputtering tool. A 4 inch Cu target was purchased for this system with a purity of 99.99%. The sputterer used for the deposition requires manual operation for the entire system, unlike the previous sputtering tools used in this fabrication process. For example to start and stop the deposition process the user must manually open and close the target shutter.

3.4.2 Physical vapour deposition of Cu



(A) (B)

FIGURE 3.17: Representations of the patterns used in the photolithography masks (A) Lithography mask for the Bilayer wafer giving cells with diameters from $100 - 20\mu$m (B) Lithography masks for the 2^{nd} Bilayer and Single layer cells that give cells with diameters between $200 - 20\mu$m shown in red, and a separate mask in blue which shows the etched regions to contact the bottom W electrode.

The whole process also requires the user to time the deposition and so the initial step was to determine the deposition rate. This tool previously had a Cu target that was used and so this recipe was used on the new target. These settings are presented in table 3.8 and were run for 10 minutes at 110W to determine the rate of the deposition. After this, the thickness of the deposition was measured and found to be 149 nm. This gave a rate of 0.248 nm/s. Therefore, to deposit the required 100nm of Cu the target shutter was left open for 6 minutes and 42 seconds.

TABLE 3.8: Processing conditions of the Magnetron sputterer for the deposition of 100nm of Cu to use as the top electrode

Target	Power (W)	Ar (sccm)flow rate	Pressure (mBar)	Deposition rate (nm/s)
DC	110	5	$5x10^{-3}$	0.248

The top electrode deposited was 100nm and this method was used for both the Bilayer and 2^{nd} Bilayer wafer. However, this sputterer was located in the physics cleanroom and once the initial COVID lockdown and eased this lab did not reopen. Therefore, for the Single layer wafer, the Cu electrode could not be deposited using this method. Instead, with the help of Dr Liam Boodhoo, this wafer was deposited using an e-beam evaporator in the Integrated Photonics Cleanroom (IPC). Once this process had been

completed the positive resist was then lifted off using N-Methyl-2-pyrrolidone (NMP) leaving behind the required patterned electrodes.

3.5 Final memory cell structure

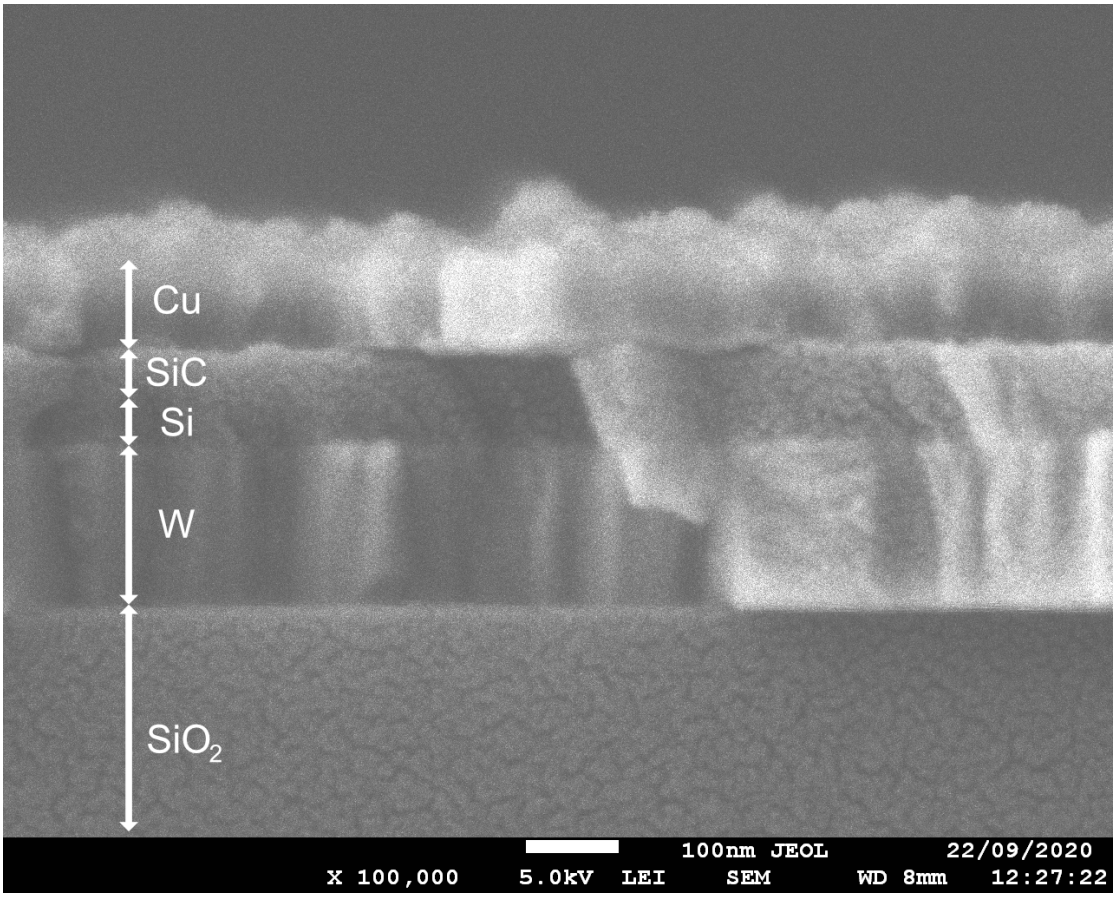


FIGURE 3.18: Scanning electron micrograph of a cross section of a single cell taken from the 2^{nd} Bilayer wafer. To achieve this high resolution image the sample was placed in an evaporator where Au was deposited on the cross sectional surface area. The bilayer is confirmed with the TEM image discussed previously in this chapter.

Two different types of memory cells have been fabricated, using a high temperature plasma enhanced chemical vapour deposition method. Using XRD, XPS, Raman spectroscopy and TEM/EDX mapping, we have shown that the Bilayer and 2^{nd} Bilayer wafers have a double stacked dielectric layer (Si/SiO_2/W/Si/SiC/Cu), whilst the Single layer wafer has a single SiC thin film (Si/SiO_2/Ti/W/SiC/Cu). The fabricated cells have a range of diameters depending upon the fabrication mask that was used. The fabrication process is discussed and detailed in this chapter, along with justifications for any changes and improvements to develop a reproducible fabrication process. The electrical properties of the Single layer devices are displayed and discussed in chapter 4. The electrical characteristics of the Bilayer wafers are discussed in Chapter 5.

Chapter 4

SiC Resistive Memory and Short-term Potentiation

This chapter will discuss the experimental data collected from the single SiC thin film deposited using high temperature plasma enhanced chemical vapour deposition (PECVD). Firstly, the DC characteristics of the fabricated devices are presented. Then short-term potentiation using pulse trains as a form of input stimuli is demonstrated and discussed. Parts of the measurements presented in this chapter were taken with the help of Mr Dongkai Guo.

4.1 Electrical Measurement Setup and DC Behaviour

This section presents the results taken from our PECVD deposited SiC thin film, with a focus on the effects of the input pulse on STP relaxation. These devices utilise the fabrication techniques outlined in Chapter 3, with the sample named Single layer Wafer. These devices were deposited with a Ti/W bottom electrode, 40nm of Si rich SiC and a Cu top electrode. This gives a final structure of Si/SiO_2/Ti/W/SiC/Cu, as shown in figure 4.1. Four wafers were fabricated and only two were measured, this was due to the micron sized pin holes in two of the wafers, caused by the Ti adhesion layer being too thin as described in Chapter 3. The two wafers that were measured showed identical performance, with 90% of the devices working across the wafer. However, a full reproducibility experiment was not conducted in this thesis as it is outside of the focus. Instead, we focus on characterising the neuromorphic properties of the memory cells.

Figure 4.2a shows the DC switching characteristics of 100 cycles, indicating consistent switching throughout. The log(I)-V graph shows that there is no need for a formation cycle and that the set process does not require a compliance current. This means that these devices do not need to depend on any external peripheral circuitry when in use.

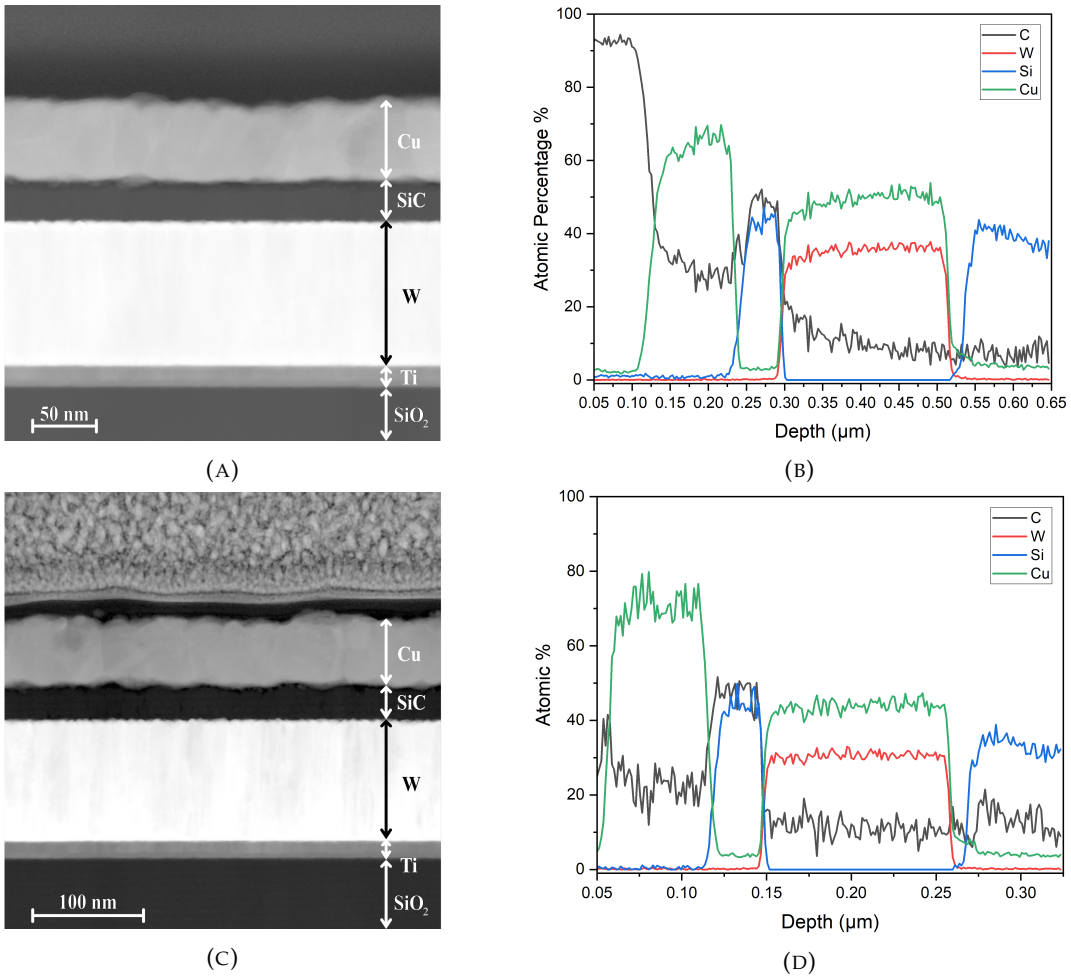


FIGURE 4.1: (A) Transmission electron micrograph cross section of a single SiC-based RRAM device from (B) Associated Electron dispersive X-ray mapping. (C) Transmission electron micrograph cross section of a second memory cell (D)Associated Electron dispersive X-ray mapping. (All TEM images in this thesis have been taken by Yisong Han and Richard Beanland in the University of Warwick.)

The switching characteristics also show an asymmetrical behaviour depending on the polarity of the applied bias, which is emphasised by figure 4.2b. This figure presents the same data as the log(I)-V graph, however the y axis has been changed to a linear scale to show the self-rectifying behaviour. This behaviour is extremely important to counteract sneakpath when combining these devices into Crosspoint structures. Sneakpath in a system can cause both read and write bit errors due to parasitic leakages. The self-rectifying behaviour would allow for selectivity between each device [177–179]. These effects will be talked about in-depth in chapter 6.

Furthermore, analysing the resistive ratio of the 100 cycles we can see that there is a difference in resistance by a factor of three, between measuring the LRS using a positive or negative bias at 0.1V. The HRS shows no difference between the two polarities. Using a positive polarity, the resistive switching ratio is around 600, however, this is not a consistent value across the DC cycles. This is because there is a shift in the LRS, with

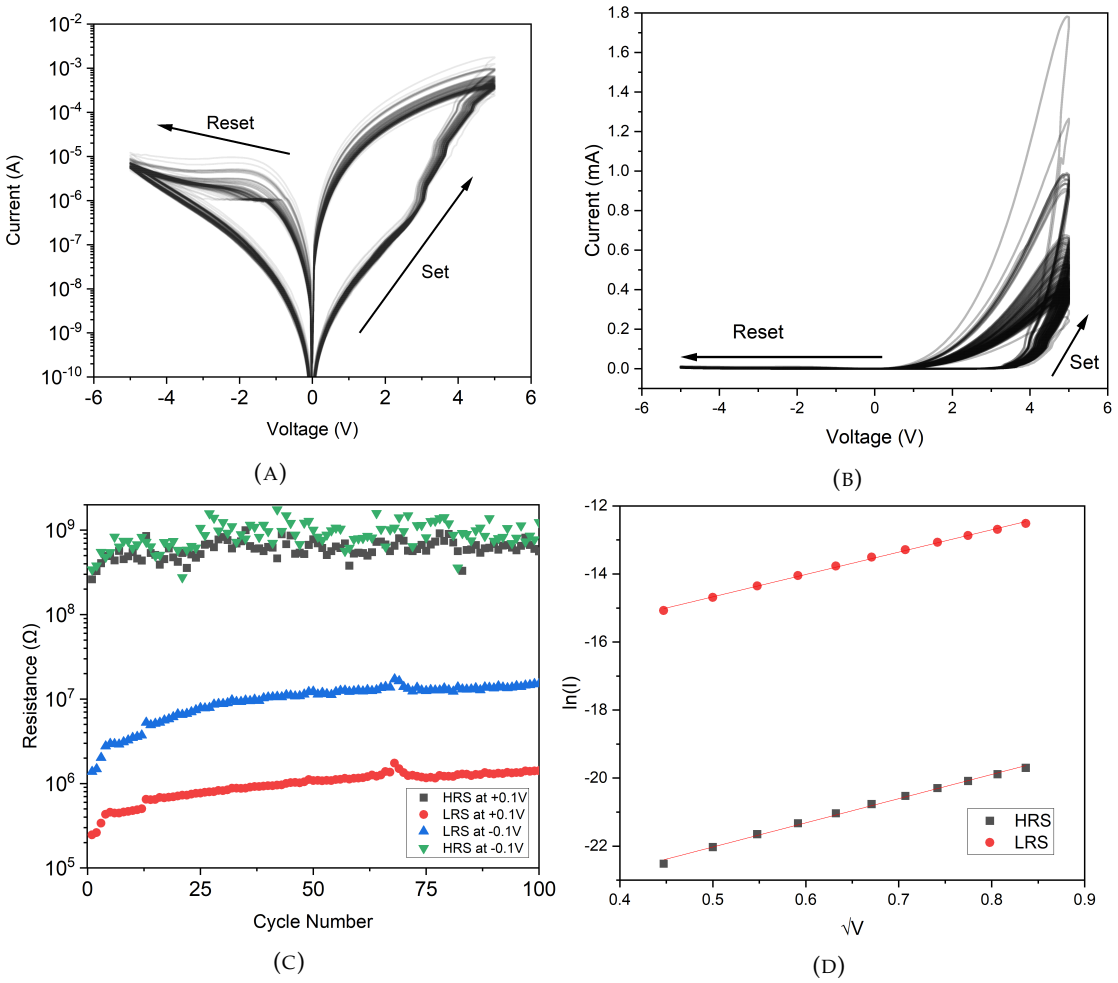
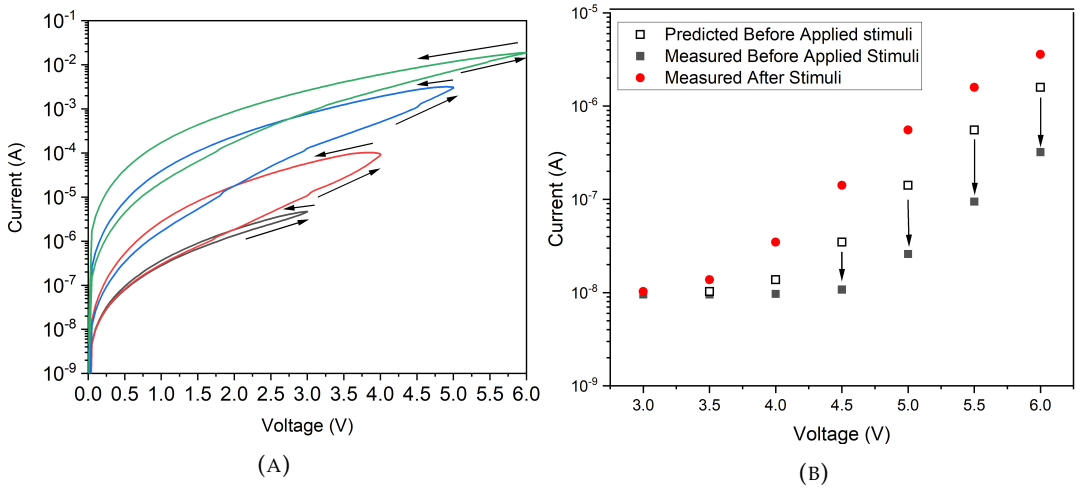


FIGURE 4.2: DC characterisation of 100 cycles using a device with a diameter of 80μm (A) log(I)-V graph showing the consistent switching between the LRS and HRS. (B) I-V graph showing the self-rectifying behaviour that could be used to suppress sneakpath. (C) Resistance states with cycle number of both using $\pm$0.1V showing that the LRS alters by an order of magnitude depending on the applied polarity, whereas there are no effects with the HRS. (D) $ln(I) - \sqrt{V}$ using the average current measured across 100 cycles. This graph shows that both the HRS and LRS is dominated by Schottky emission

the resistance slowly increasing with cycle number from a minimum of 0.25$M\Omega$ to around 1.7$M\Omega$. This overall reduces the resistive ratio from 10^3 to 10^2.

The conduction mechanisms for both the HRS and LRS appear to be dominated by Schottky emission, showing in figure 4.2d. This is surprising considering the standard LRS mechanism for SiC based resistive memory is usually dominated by Ohmic conduction. If the voltage bias applied was increased too high and the device altered to ohmic conduction, then the device would be irreparable broken. This could possibly mean that the different resistance states is due to the movement of ions through the SiC dielectric and when the two electrodes are connected, the filament is too strong to rupture.



(A) (B)

FIGURE 4.3: (A) I-V graph showing the effects of increasing the applied voltage on the current. (B) I-V graph showing the measured current at 0.1V before and after the applied voltage bias. Presented is also the expected current before the sweep, showing the partial loss of information.

To confirm this, varying DC stresses were applied to the memory cells to look at their effects on the resistance. Figure 4.3 presents the data collected when applying varying levels of DC amplitudes, without a reset applied in between. Voltages were continually applied to a cell from 3V to 6V in steps of 0.5V. After each DC sweep there is a noticeable relaxation in which the cell increases its resistance. Figure 4.3b shows this by displaying the current at 0.1V before and after each DC sweep, as well as the expected current that should be maintained between each cycle. We can see that there is a clear drift in the measured current which could be due to spontaneous diffusion of Cu ions that have not formed part of the stable filament.

Figure 4.4 shows the effects of the current when a fixed voltage is applied multiple times, without a reset. The device is reset when altering the value of the applied voltage, so that each experiment would start at the same HRS. Voltages from 3 to 5V in steps of 0.5V are used to see if it is possible to precisely tune multilevel states through increasing the number of DC sweeps and their associated amplitudes. Figure 4.5a shows that the effects of these voltages on the conductance of the device. Here conductance is mentioned instead of resistance as this is the typical form in which neuromorphic based devices are compared. We see that the change in conductance can be precisely controlled with 3.5V providing a minimal change while 5V shows a much greater change in conductance. This process shows that the devices have clear neuromorphic properties, as the amplitude and number of applied stresses will directly increase the conductance. The alterations between the initial and peak currents are presented in table 4.1

By using the Schottky equation we are able to determine how the barrier height alters while increasing the number of DC sweeps and the amplitude, shown in figure 4.4. This graph shows that the barrier height directly alters between 0.54 and 0.73 eV, depending

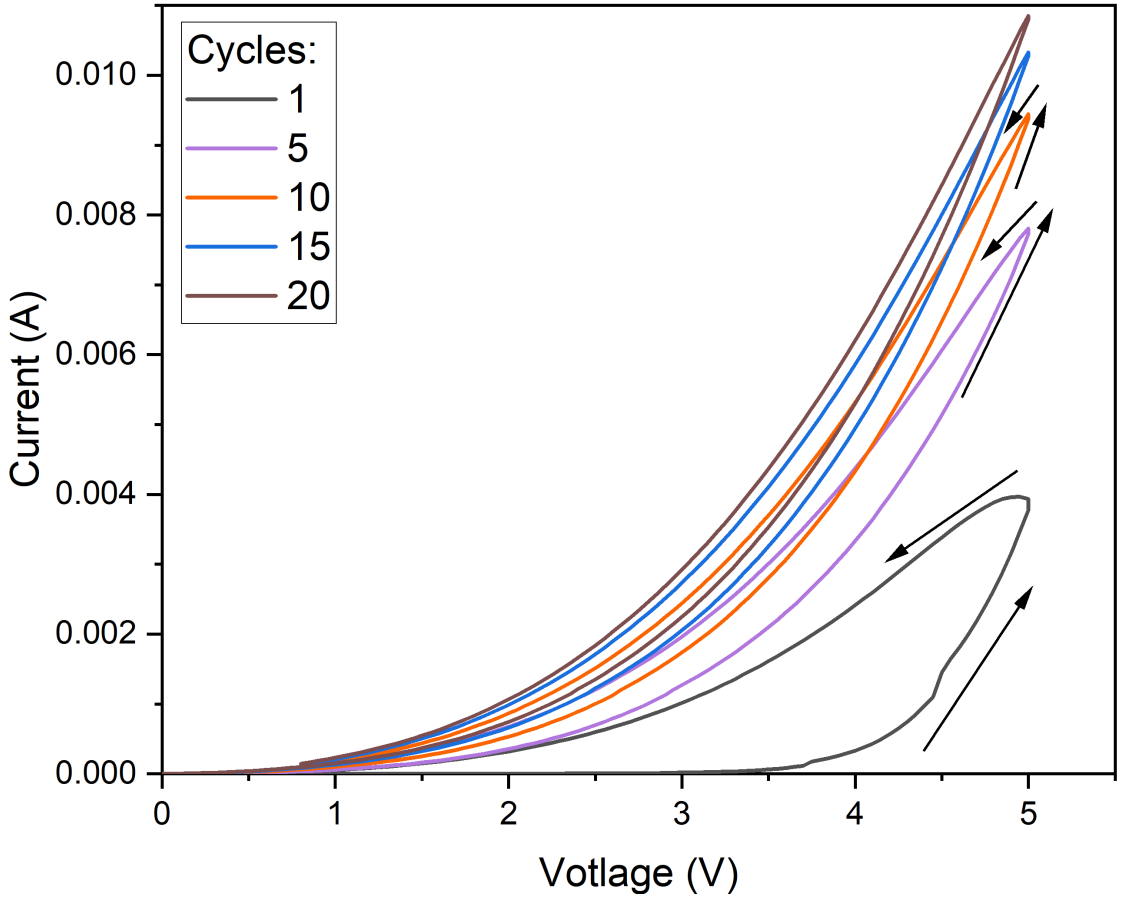


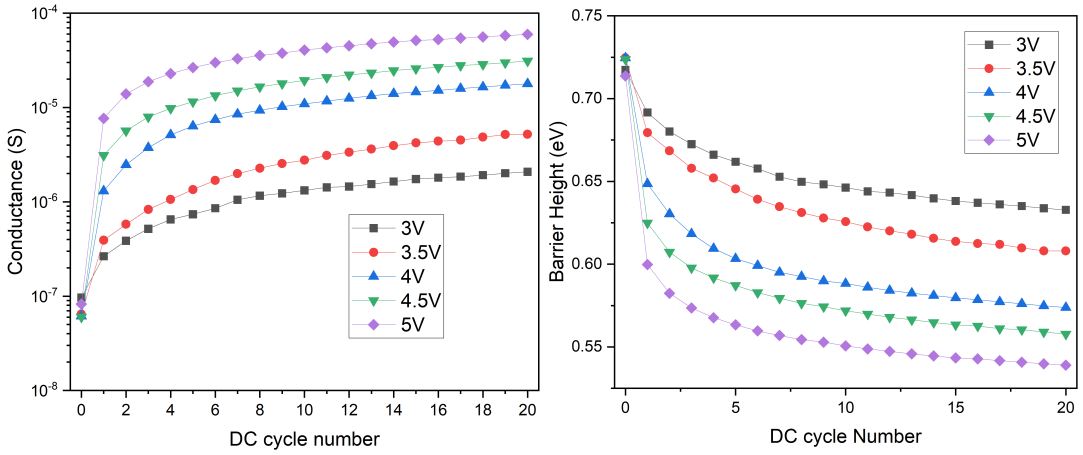
FIGURE 4.4: I-V graph showing the effects of increasing the number of DC sweeps on the current.

TABLE 4.1: Current before and after 20 set DC sweeps, with altering applied bias. This is to simulate the amount of stimuli applied across a neuron using a DC measurement

Voltage (V)	Current Before input stimuli (nA)	Current After 20 DC cycles (μA)
3	9.69	0.21
3.5	6.47	0.52
4	6.15	1.78
4.5	6.01	3.11
5	8.23	5.95

upon the applied voltage and pulse number. This could be due to a change in ion migration through the dielectric and would consequently change the Schottky barrier height.

To get a more detailed analysis of the effects of the input stimuli with relation to the conductance we must alter the measurement setup towards pulsing, so that we can precisely measure the exact times of any relaxation loss. These measurements are investigated in the next section.



(A) (B)

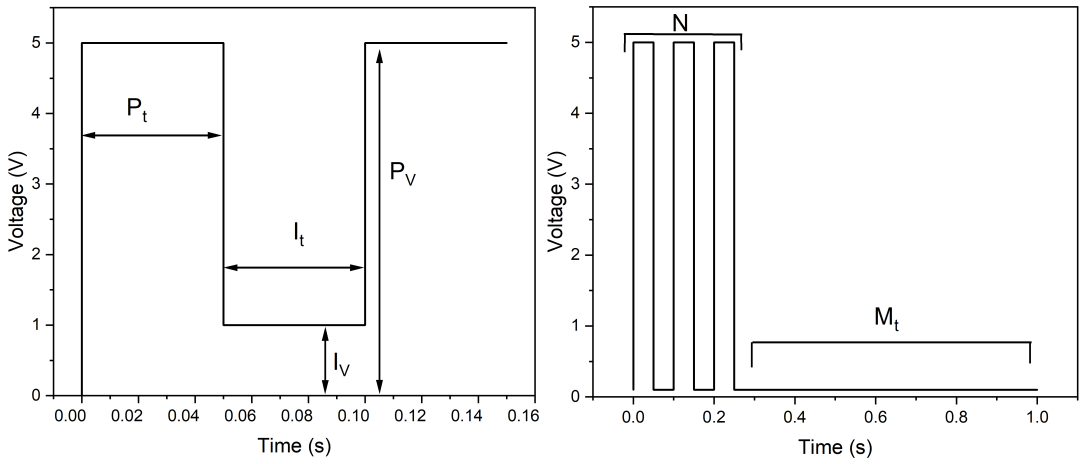
FIGURE 4.5: (A) I-V graph showing the measured conductance at 0.1V of 20 DC sweeps, using voltages between 3V and 5V. (B) The extracted barrier heights when changing both the applied DC amplitude and the number of sweeps.

4.2 Short Term Potentiation Characteristics

The memory cells were cycled before applying pulse trains to make sure that their characteristics were as expected. After each experiment the cells were cycled so that we can be sure that the HRS goes back to its original state. Varying the input pulse was done by fixing or changing the parameters shown in figure 4.6. Firstly, the duration time (P_t) is the amount of time a pulse is applied to the memory cell, with a duration voltage (P_V). In between each pulse is an interval time (I_t), with an interval voltage (I_V). For all the experiments the interval voltage is kept at 0.1V, so that the change of conductance between each pulse can be measured. After the full pulse train the device was monitored at 0.1V for a total measurement time of 60 seconds, with the measurement time being (M_t). This continuous read voltage allows for the analysis of the decay of short-term potentiation and how it varies depending on the input pulse.

For this initial measurement P_t and I_t are equal to 50ms, whilst a change in N is analysed. Figure 4.7 shows an example of this with a fixed voltage of 5V and pulse number ranging between 20-100. As expected, we can see that an increase in the number of stimuli increases the conductance in an almost linear fashion. The change in conductance is not expected to be truly linear, due to the nature of resistive switching neuromorphic devices. However, we can clearly see that it is possible to tune the required conductance by altering the number of pulses

Further measurements were taken by increasing both N and the P_V. The number ranged between 20 to 100 pulses and the voltages between 5V and 7V. Figure 4.8a shows the peak conductance after each potentiation is applied. As demonstrated previously, as the number of pulses increases the conductance also increases, in a linear fashion. Increasing the applied voltage also increases the peak conductance even further. We



(A) (B)

FIGURE 4.6: Representation of the different variables when designing the input pulse (A) Presents the duration time (P_t), duration voltage (P_V) interval time (I_t) and the interval voltage (I_V) (B) The number of pulses (N) and the subsequent continuous read (M_t) which has a voltage equal to I_V and is used to measure the decay of short-term potentiation

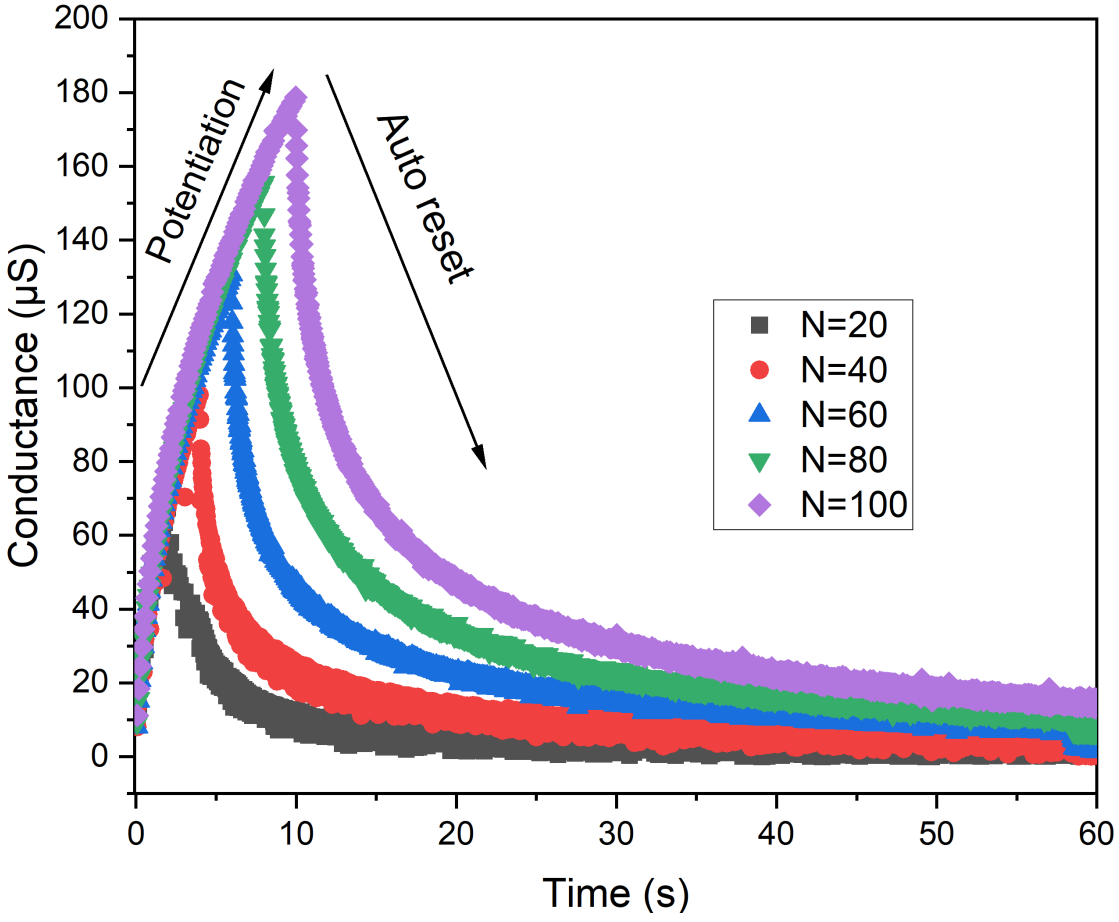


FIGURE 4.7: Conductance-Time graph showing short-term potentiation through varying the number of input pulses, whilst fixing the voltage at 5V. As N is increased the conductance increases and once taken away, the conductance decays back towards its original value

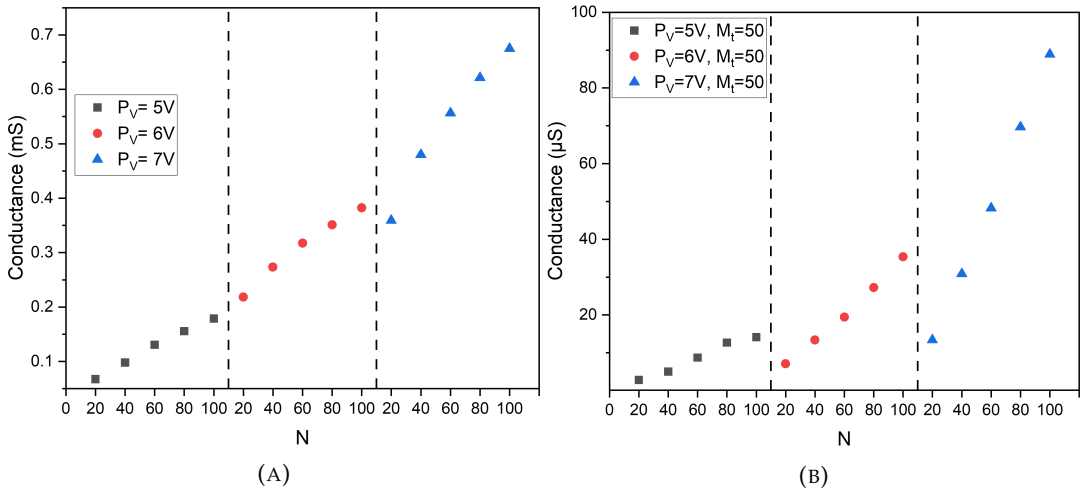
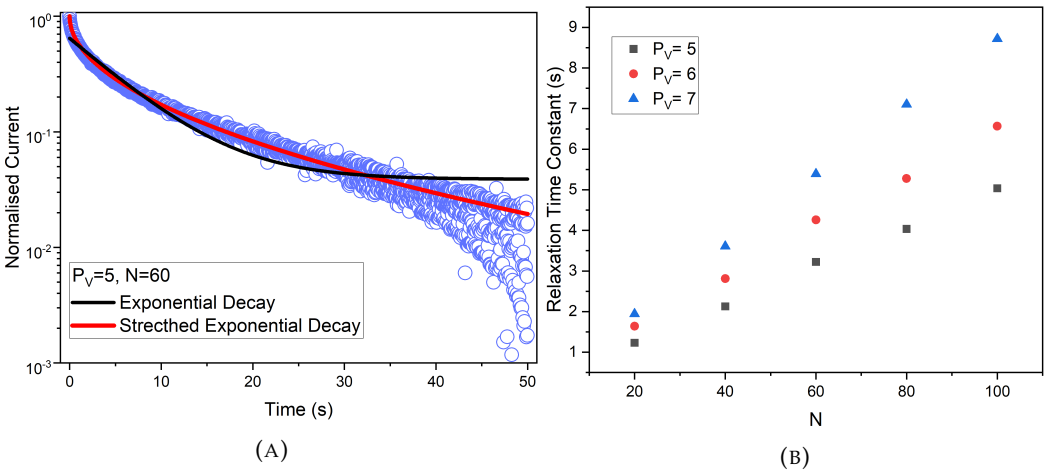


FIGURE 4.8: (A) Peak potentiation conductance while changing N and P_V (B) Conductance of the memory cell 50 seconds after the peak potentiation, showing a weight attached with the decay.

also find that by increasing the applied voltage the rate of change increases with 5, 6 and 7V giving a change of 42, 187 and 307 μS per number of pulses, respectively. This is too be expected as increasing the applied voltage will increase the amount of ion migration in the same time, which would further decrease the barrier height.

The decay of the short-term potentiation can be analysed using the data collected from the continuous 0.1V read section of the measurement (M_t). Figure4.8b This relaxation shows the conductance of the memory cells after a relaxation of 50 seconds. It shows that with in an increase in the number and intensity of the input pulse the more difficult it is to forget the associated conductance state due to the weight attached to the input stimuli.

To analyse this relaxation further we can compare the normalised decay of the memory cell after each potentiation. Figure 4.9a shows an example of this normalised decay after 60 pulses with a voltage of 5V. As we can see by this graph a standard exponential decay curve does not adequately fit the trend. Instead, we can use the Kohlrausch–Williams–Watts (KWW) function, also known as a stretched exponential decay. This is given by the equation 4.1 below, whereby ϕ_t is the relaxation function, I_0 is the initial current, t is the time, τ is the relaxation time constant and β is the stretched exponent. For these devices we have kept β as 0.5. As we are using a normalised current value, I_0 is equal to 1. Using this analysis, figure 4.9b shows the calculated relaxation time constant for the varying voltages and number of pulses used in the above experiment. The relaxation time constant increases with an increase in both the intensity and number of pulses. This could be due to the increase in ion migration across the cell, caused by the increase in both voltage and number of pulse. This increase in ion concentration would require a longer period of time for the diffusive rupture of the filament. This mimics the plasticity found in the synapses of the brain, with the changing



(A) (B)

FIGURE 4.9: (A) Normalised decay of the current over 50 seconds, after a potentiation with 60 pulses at 5V. A comparison of both an exponential and stretched exponential decay fitting is shown (B) Relaxation time constant with a change in pulse number

concentrations of the neurotransmitters.

$$\phi_t = I_0 e^{(t/\tau)^\beta} \tag{4.1}$$

Figure 4.10a shows the effects of changing I_t of each pulse on the potentiation of the memory cell. As I_t between the pulses increase the rate of change of the potentiation decreases, except for when I_t is 20ms but this was taken as an outlier measurement. This means that the the peak conductance decreases with an increasing interval as well, shown in figure 4.10b. Figure 4.10c shows the effects of changing P_t on the potentiation of the memory cell, between 50ms and 200ms. As P_t increases there is an increase in the conductance. This is also shown in figure 4.10d which shows the associated peak conductance of each duration. Both of these processes can be explained by the time allowed for the diffusive rupture and migration of ions through the SiC dielectric. By increasing the time in between the the applied pulse we allow for the diffusive rupture of the conductive filament, seen in the decay after potentiation. Therefore, the more time allowed between each pulse the larger the diffusion and the lower the overall conductance. Similarly, if we increase the duration of the applied pulse, we allow for an increase in ion migration and hence we increase the conductance further.

Figure 4.11a shows the extracted relaxation times from the decay of the experiment above. The relaxation time increases while decreasing the the interval between the pulse. Therefore, we can say that it is easier to lose information when the time between each pulse is too long.

Figure 4.11 gives the extracted relaxation time constant, from the short-term potentiation decay, when changing I_t between 5ms and 30ms, and P_t between 50ms and 200ms. As expected when the interval increases the relaxation time decreases and when the

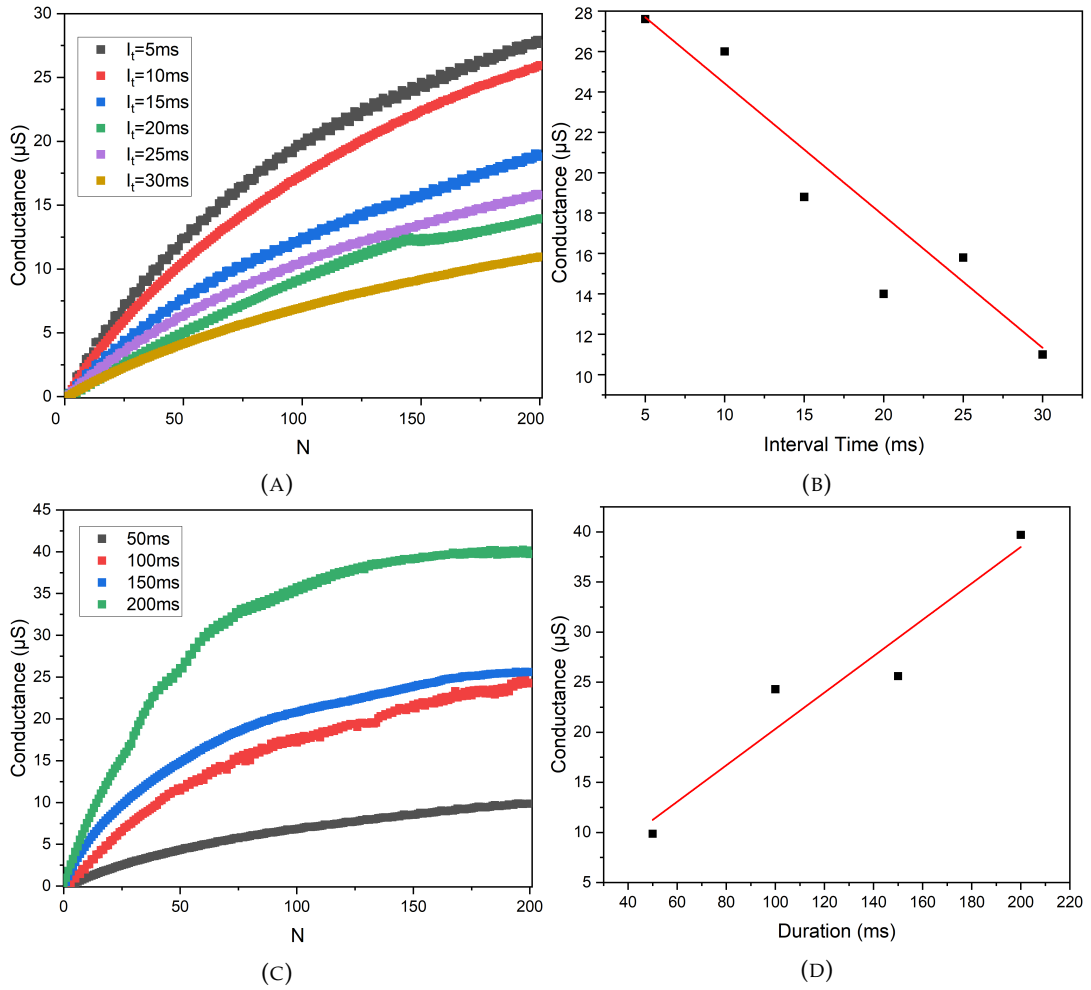


FIGURE 4.10: (A) Potentiation while varying I_t of 200 input pulses between 5ms and 30ms (B) Associated peak conductance of the potentiation, showing that the conductance decreases with an increase in I_t. (C) Potentiation while varying the P_t between 50ms to 200ms.(D) Associated peak conductance of the potentiation, with an increase in conductance with an increase in P_t

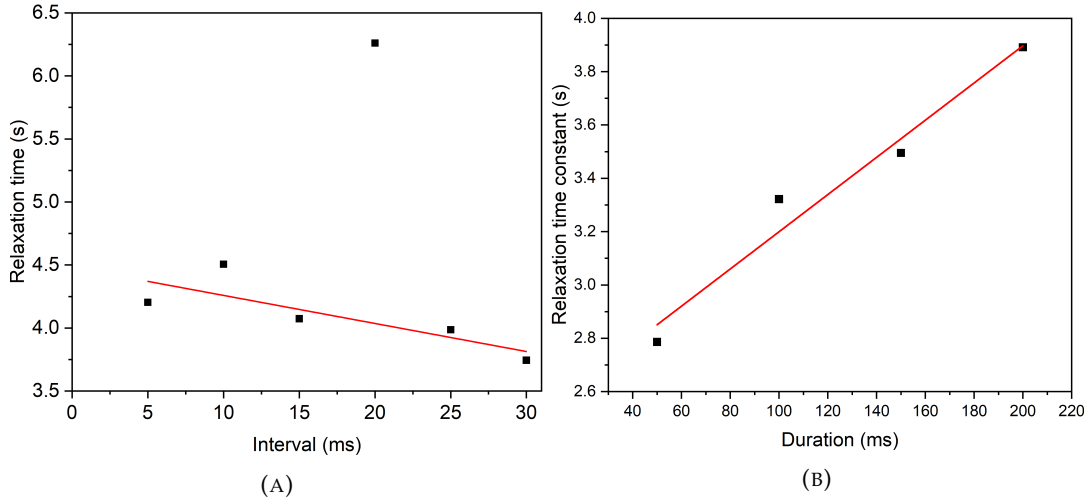
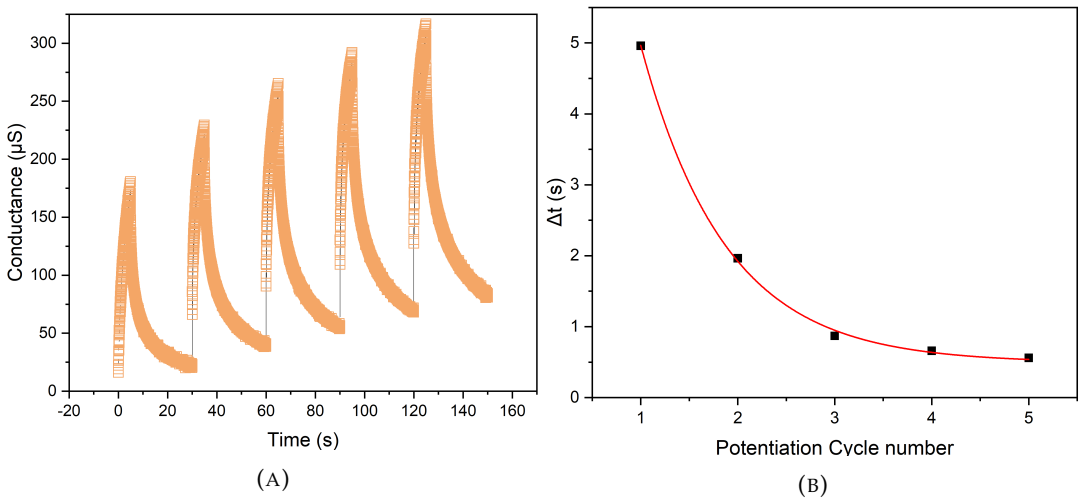


FIGURE 4.11: (A) Extracted relaxation time constant while changing interval between 5ms and 30ms. (B) Extracted relaxation time constant while changing duration of the applied pulse



(A) (B)

FIGURE 4.12: (A) Conductance-time graph showing the effects of the same short-term potentiation cycle applied multiple times.(B) Time between the initial potentiation and peak conductance from 5 STP cycles. This graph shows that the time taken to reach back to the initial 181μS peak is exponentially quicker.

duration increases the relaxation time also increases. This is because, when the interval increases the filament diffusion is higher during the pulse train. This means the filament is weaker and so it is possible to fall back to its original conductance state quicker. Conversely, when the duration of the pulse is increased ion migration also increases, making the filament significantly stronger. Therefore, it is harder for the filament to rupture and it takes longer for the conductive state to fall back to its original value. This is in keeping with the plasticity of synapses and their strength depending on input stimuli and neural activity.

Finally, figure 4.12 shows the effects of applying the same short-term potentiating cycles multiple times. In this example, P_t and I_t are set to 50ms and N is equal to 100. As the cycles are applied we can see that the initial peak conductance is reached faster with each cycle and because we are using the same time of pulse this also means we are increasing our peak conductance and each point. Figure 4.12b shows the time taken between the start of each cycle until the that potentiation reaches 181μS, which is the peak conductance of the first potentiation. As we can see the time taken to reach this value is exponentially quicker the more cycles we apply. This could be cause by the filament not fully rupturing after the initial pulse and so less time is needed to get back to the peak conductance. As we further increase the peak conductance and hence make the filament stronger, it requires a even less time to rebuild back to the conductive bridge and reach the required 181μS.

4.3 Conclusion

In this chapter we have investigated short-term potentiation switching using SiC-based RRAM devices. This work is the first detailed analysis of short-term potentiation of SiC-based memories and is the first neuromorphic SiC-based memory using PECVD as a deposition method. The memory cells exhibit asymmetrical DC switching with a drift in the LRS with cycle number. The cells can hold multi-level states that are controlled through changing the applied voltage and number of DC Set sweeps. This behaviour is thought to be caused by a changing Schottky barrier height, which is the dominant conduction mechanism in both the LRS and the HRS.

Through pulsed measurements, we have been able to study the effects of varying the input pulse parameters on the conductance during both the potentiation and the subsequent decay. Through varying the number of pulses and the applied voltage we can finely control the conductance of the memory cell between 0.07μS and 0.7μS. By further altering the duration of the pulse train we can control the conductance of the cell up to 40μS. By varying the interval between 5ms and 30ms, we can further tune the peak conductance of our resistive memory cell and show that our decay between the input stimuli is in the order of milliseconds. The control in the conductance state is thought to due to the ion migration caused by the applied pulses and the spontaneous diffusion of the conductive filament. It was also found that a applying multiple STP potentiation and decay cycles showed that the overall peak conductance increased with cycle number. Therefore, taking a single conductance point of 181μS it was found that this specified conductance state could be re-learned exponentially quicker with each cycle, which has been seen in other neuromorphic based devices.

The observed potentiation and decay time was of the order of 1 minute which is comparable to other resistive switching devices [180]. This is within the millisecond-minute range seen in real world STP functions, using purely BEOL compatible processes [96, 181, 182]. This is important to note as STP is understood to play an important role in information processing and decision making. Therefore, the memory cells must be able to decay at a steady rate such that multiple STP functions can be used for memory processing and the BEOL compatible memory cells measured in this chapter have shown to be a great candidate for embedded neuromorphic systems.

Chapter 5

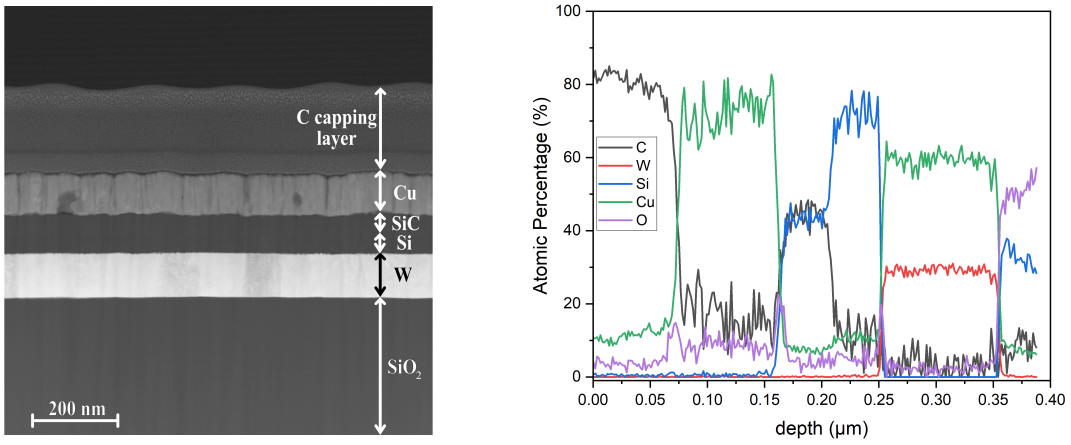
High Performance Bilayer SiC Resistive Memory

This chapter focuses on the electrical characterisation of 100nm Si/SiC RRAM wafers deposited using PECVD. The electrical characterisation setup is discussed for both DC and pulsed measurements. The switching results are displayed and analysed in detail of both the initial Bilayer wafer and the 2^{nd} Bilayer wafers that were fabricated to show reproducibility.

5.1 Electrical Measurement Setup and Current Compliance Investigation

The memory cells in the Bilayer wafer have a cross sectional structure Si/SiO_2 /W/Si/SiC/Cu, as seen in figure 5.1a. These devices utilise 180nm bottom W electrode, a 100nm Si/SiC bilayer and a 100nm Cu top electrode. The fabrication of this device is outlined in Chapter 3 and the bilayer dielectric is fabricated from a single high temperature PECVD process. Figure 5.1b shows bilayer used in the cell, which is taken from an Electron Dispersive X-ray Cross-sectional mapping of a Bilayer cell. As discussed in chapter 2 the resistive memory devices operate through the formation and rupture of a conductive bridge. To test the characteristics, as well as to confirm these results, it is important to first understand the reasoning for the measurement setup, applied voltage stresses, polarities and added circuitry.

The devices were cycled so that a Cu filament would be formed as the conductive bridge mechanism. Bipolar and Unipolar mechanisms were investigated with differing polarities used for the Set voltages. This was to look at the stability and any asymmetrical switching characteristics in the different methods.



(A) (B)

FIGURE 5.1: (A) Transmission Electron Microscopy cross-sectional micrograph of a single cell from the Bilayer wafer (B) Associated Electron Dispersive X-ray Cross-sectional mapping of the Bilayer cell.

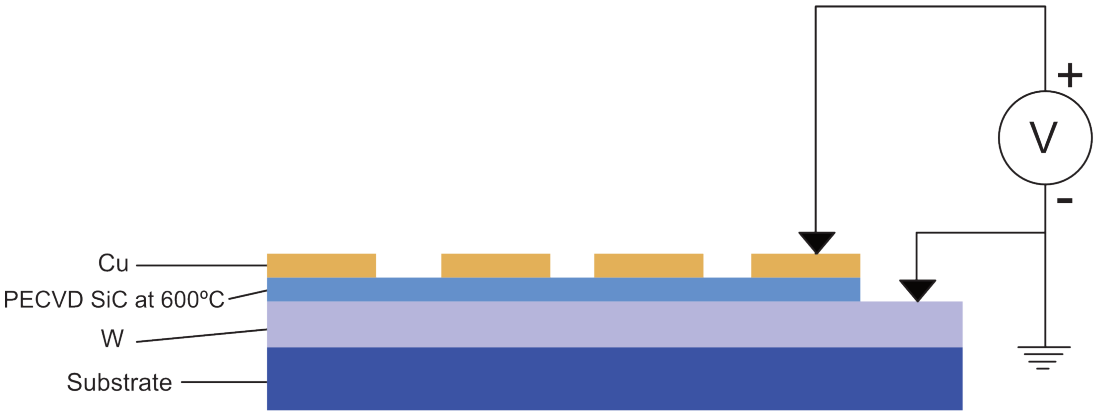


FIGURE 5.2: Representations of the DC characterisation setup utilising a positive voltage through the Cu electrode, with the W acting as ground.

Using a positive voltage for the Set operation the W thin film acts as the effective ground and the applied voltage is varied through the Cu electrode, shown by figure 5.2. This applied electric field causes Cu ion migration towards the inert electrode forming the conductive bridge. This alters the device from the HRS to the LRS. Applying a negative voltage in this setup would cause the ion migration to reverse which is used to reset the device in a bipolar mechanism discussed in Chapter 2 .

For the switching characteristics, the Set voltage is defined as the voltage at which the device reaches I_{prog} and is stable enough not to fall back to the HRS. The Reset voltage is defined by the voltage after which the last sharp change in the resistance of the log(I)-V graph occurs. More specifically the point at which the gradient between two points of the DC sweep, at 50mV steps, alters by $\frac{dI}{dV} < -0.001\text{A/V}$ for a positive reset and $\frac{dI}{dV} > 0.001\text{A/V}$ for a negative reset. An example of this is shown in figure 5.3.The reset of the memory cell is given by the back curve and the red curve shows $\frac{dI}{dV}$. As the

memory cell is Reset and a sharp change in current occurs, $\frac{dI}{dV}$ also has a sharp change from around 0 to -0.03. This drastic change in the gradient allows us to automatically find the Reset voltage, without having to manually analyse every single cycle that is taken. This is important for taking large set of cycling data, as it drastically speeds up the analysis process.

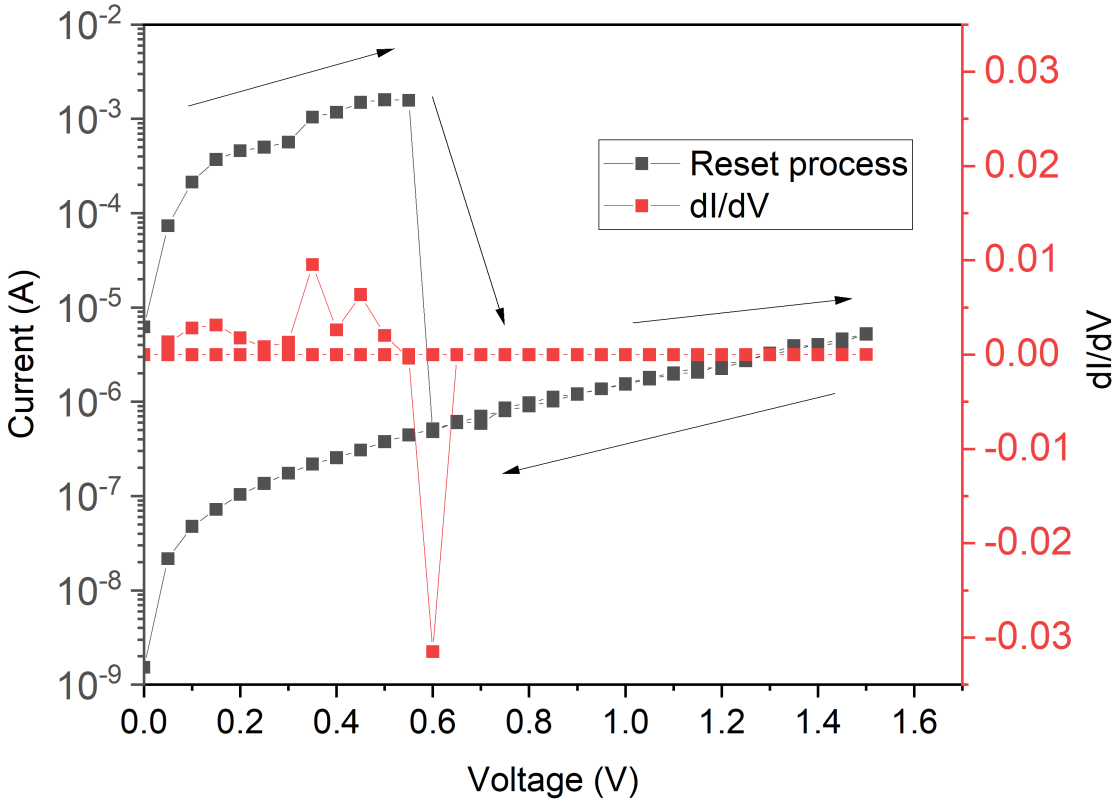


FIGURE 5.3: I-V and dI/DV-V graph showing the method in which the Reset voltage can be automatically found. The black curve shows the I-V of the memory cell during the reset process and the red curve shows dI/dV. When a sharp change in resistance occurs during the reset process, we can see a drastic change in the gradient. This change in gradient is defined as the Reset of the device.

For the pulsing measurements, a slight alteration in the measurement setup was necessary. This is because the setup used the Keysight B1530 WGFMU pulsing module which does not have any current compliance abilities. Therefore, an external compliance current circuit had to be developed so that the device could be Set and Reset.

Initially, a transistor was used with the same setup shown in 5.4a. The transistor was positioned in between the W electrode probe and the RSU which connects the WGFMU port to the probes using SMA connections. The gate was controlled using a Triax cable connected to an SMU in the B1500a. Figure 5.4b shows the IV characteristic of a standard resistive switching cycle with the I_{prog} of 1mA for the positive Set and 100mA current for the negative Reset sweep. Figure 5.4c shows a single IV of a device without the I_{prog} applied in the semiconductor analyser and instead the current compliance is controlled using a transistor. For the DC operation, the transistor works well at keeping

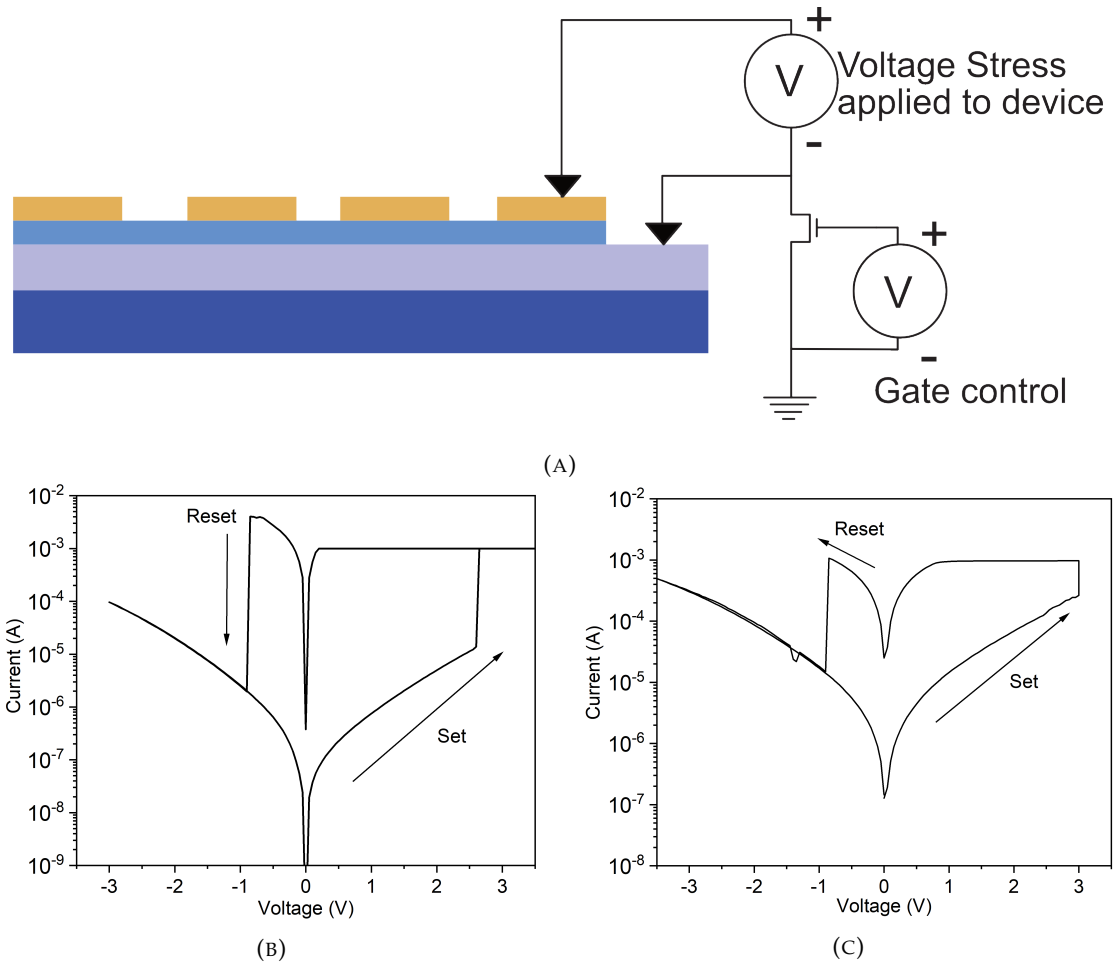


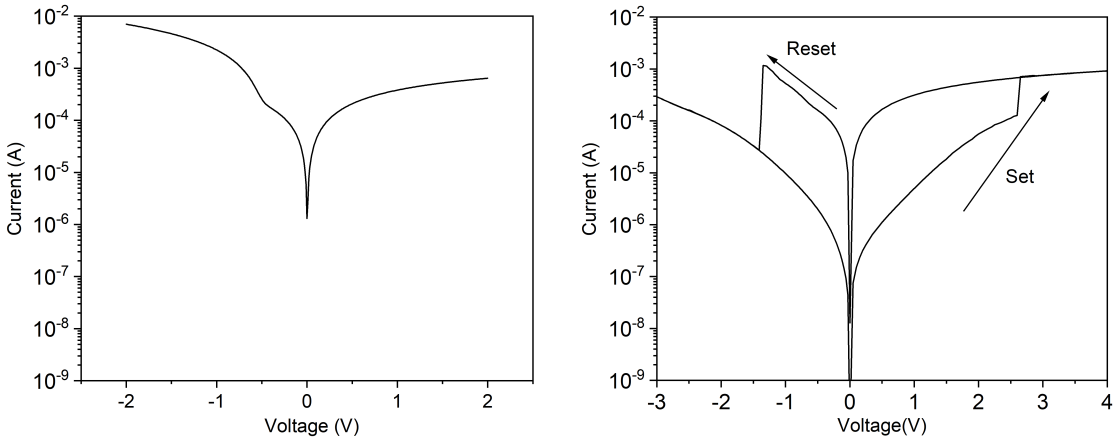
FIGURE 5.4: (A) Representation of a compliance current circuit in series with a resistive memory device under test. (B) IV characteristics of a standard RRAM sweep with a 1mA $I_{programme}$ (C) IV characteristics of a RRAM sweep using a standard transistor to control the compliance current.

the devices within their I_{prog} range. However, when operating the devices using high-speed pulses the devices could not be fully reset or would even break down. This could be due to an overshoot of the current when applying the Set voltage, caused by the charging of parasitic capacitance (C_p) between the transistor and the RRAM [15, 183]. This overshoot is given by equation 5.1:

$$I_{overshoot} = C_p * \frac{dV}{dt} \tag{5.1}$$

Keysight's manual states that the current limit device needs to be placed close to the device under test to reduce this effect for accurate current limiting [184]. This would involve the design, fabrication and characterisation of transistors on the same wafers as the RRAM devices, which is outside the scope of this project.

Therefore, further testing of differing transistors was investigated to see if this could this effect could be minimised in a way to still be able to measure the devices. Initially



(A) (B)

FIGURE 5.5: IV characteristics of a RRAM device in series with a broken down IRF540 (A) $\pm 2V$ both probes on the same metal contact showing inherent characteristics (B) DC switching of a RRAM device

the transistor IRF540 was investigated with its delay on and off switching time less than 55ns . During DC operation the device appeared to be working similarly to the previously reported transistor in 5.4c. However, when utilising a μs On/Off pulse train, the transistor's IV characteristics had altered. Without applying a gate voltage the transistor now exhibited the required 1mA set and greater than 1mA reset current. This is shown by figure 5.5a which shows the IV characteristics of the transistor in series with two probes contacting the same metal pad. This method was tested on other IRF540 transistors which all showed the same characteristics. This meant that the pulsing test conducted would no longer have to rely on the SMU connected to the gate. It should be noted that the initial pulse tests in section 5.3 used long rise times to be able to test the devices without the possibilities of large overshoots in the current compliance. However, as further testing was conducted it was found that this was unnecessary and that the current limiting circuit adequately prevented large overshoots in the current compliance.

Figure 5.5b shows the DC characteristics of a RRAM device in series with the transistor and the gate left floating it is clear that this device was the perfect candidate to use when testing the long term endurance of the RRAM devices. This current limiting device gave the ability to measure extremely long endurance testing, with the longest-running test lasting 12 days. The results from using this setup is explored in section 5.3. Before this we will first explore the DC characteristics of the devices outlined in the next section.

5.2 DC Switching Results

The DC characteristics of these devices were measured using a 50mV step voltage. The power required to form the initial conductive bridge is significantly higher than the subsequent switching power, due to the subsequent only requiring a partial reformation of the filament, figure 5.6a. Figure 5.6b shows the I-V characteristics of a formation and a subsequent switching cycle with the large variation in both the required voltage and current compliance of the Set process. The initial DC operation to change the device from a HRS to a LRS required a sweep above 8.5V with a compliance current above 10mA. However, if the device was set above 45mA a hard breakdown would occur. After this, the device could be set below 4V.

Amorphous-Silicon based RRAM devices have shown non-volatile switching being above a 100μA current compliance, during the Set operation [185]. Below the current compliance, spontaneous rupture filament cause the device to exhibit volatile threshold switching, described in Chapter 6. The Si/SiC devices measured in this chapter showed that the device exhibited non-volatile switching with a compliance current of around 100μA, figure 5.6c. However, using 100μA the devices could only be cycled around 50 times, before requiring multiple Sets to retain information. By increasing the current compliance to 1mA, the formation of the filament was strong enough to so that spontaneous filament rupture would not occur. Using a current compliance greater than 1mA would increase the possible risk of forming a filament that was too strong and could not be broken. Unlike the Set process, the Reset for both the formation and subsequent cycles are fairly similar, as we are only partially rupturing the filament within the same area.

Figure 5.8 shows the analysis of the conduction mechanisms of the HRS and LRS. The linear I-V characteristic of the LRS shows that the On state is dominated by Ohmic conduction. This is in keeping with the theory of the Cu ions migrating and connecting the two electrodes. Looking at the ln(I)-$\sqrt{V}$ graph we can see that the HRS is dominated by Schottky emission, due to its linear trend. The Richardson's constant was assumed to be 1202 mA/mm^2K^2. There is an alteration in the barrier height between the pristine and subsequent reset of the device from 0.6 to 0.57 eV. This could possibly be due to the effective doping cause by the migration of the Cu ions after the initial formation of the conductive filament. The dielectric constant of the thin film was also extracted by measuring the capacitance over area, shown in figure 5.7. The extracted dielectric constant was 26.4, showing the bi-layer as a high-K dielectric.

These devices showed non-polar switching characteristics, meaning that it can be cycled using both a unipolar and bipolar mechanism, figure 5.9. Both of these mechanisms are presented having measured 100 cycles, with a typical cycle highlighted in

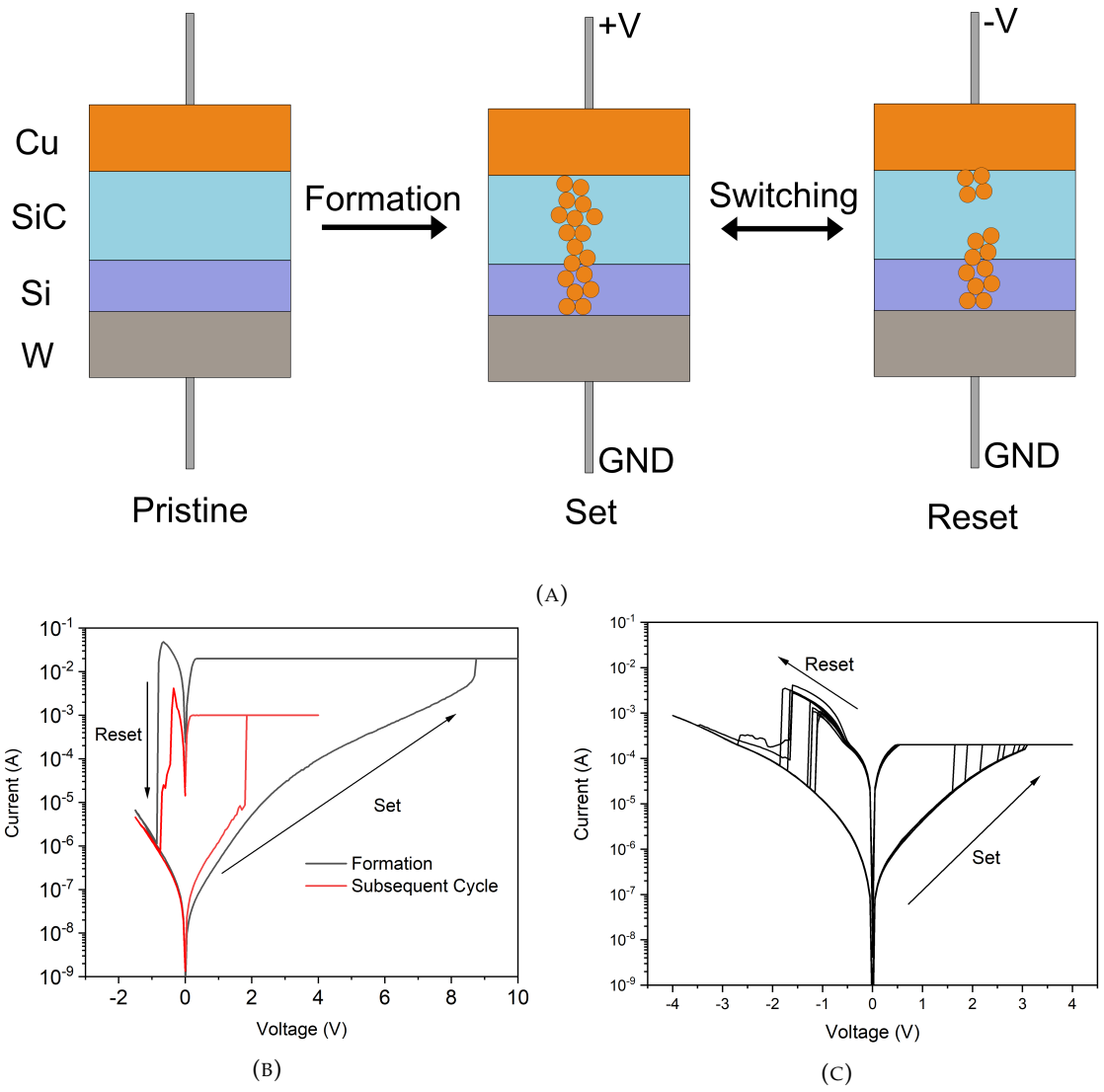


FIGURE 5.6: Formation characteristics of the Si/SiC bi-layer based devices (A) Representation of filament formation/rupture (B) I-V graph of Formation and subsequent cycle, showing alteration in the Set voltage and current compliance (C) I-V graph showing the ability to switch the device at 200μA. Below 100μA and the device cannot be switched on. 1mA is usually used for an increased in stability over cycle number.

their respective I-V graphs. Looking at these graphs we can clearly see that the switching voltages of the unipolar mechanism is lower than the bipolar, with the data presented in table 5.1. For unipolar and bipolar switching, the average switching voltage are around 1.7 and 2.1 for the Set process and 0.7 and -0.8 for the Reset process respectively.

Figures 5.9b and 5.9d show the resistance states for the LRS and HRS across 100 cycles, using both unipolar and bipolar switching. Utilising unipolar switching the average resistive ratio is around 10^2, compared with bipolar that has a ratio of around 10^3. Furthermore the standard deviation of the resistance states is higher in the unipolar than the bipolar mechanism.

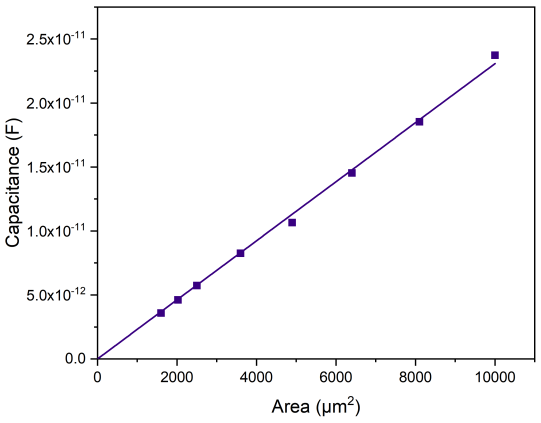
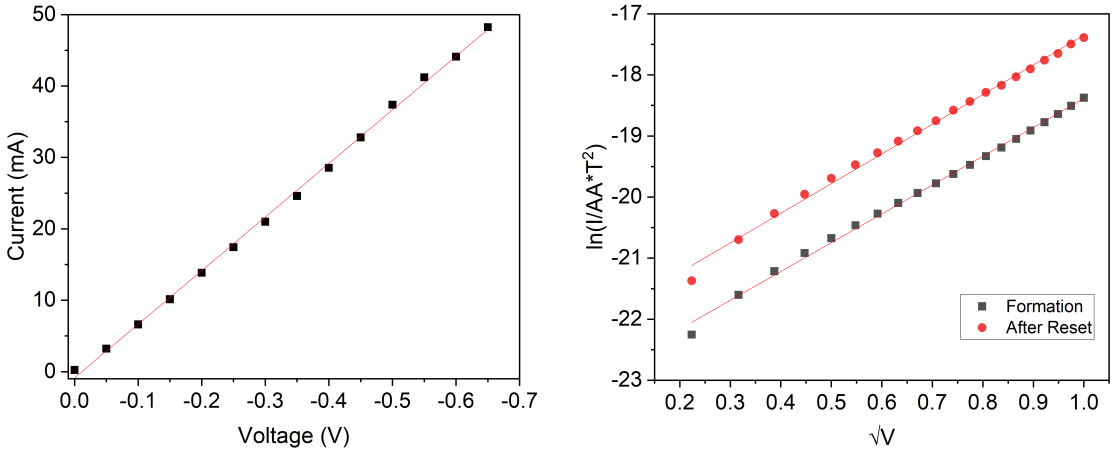


FIGURE 5.7: Capacitance-Area graph used to determine the dielectric constant, which was extracted to be 26



(A) (B)

FIGURE 5.8: Analysis of the conduction mechanisms between the two bit states.(A) I-V graph showing ohmic conduction is the dominant mechanism in the On state due to its linear nature (B)$ln(IAA * T^2) - \sqrt{V}$ graph showing the schottky emission is the dominant conduction mechanism in the HRS, with a shift in the barrier height between the pristine and subsequent HRS state

TABLE 5.1: DC characteristics for 100 cycles using Bipolar and Unipolar switching. Presented are the average switching voltages and the resistance states for both mechanisms.

	Avg Set (V)	Avg Reset (V)	Avg HRS (kΩ)	Avg LRS (Ω)
Unipolar	1.66±0.45	0.66 ± 0.18	119 ±68	250± 169
Bipolar	2.14±0.24	-0.8± 0.22	158± 29	177 ± 127

Overall, the devices have displayed a much lower resistive ratio than compared to a sputtered SiC based thin film. However, they are more in line with devices that can produce a higher endurance capabilities [4, 41, 55]. Therefore, to test this possibilities the devices would have to be pulsed as the DC measurements are too slow for high endurance measurements. With the switching characteristics in mind the long term cycling tests were conducted using only the bipolar mechanism. This is because, the

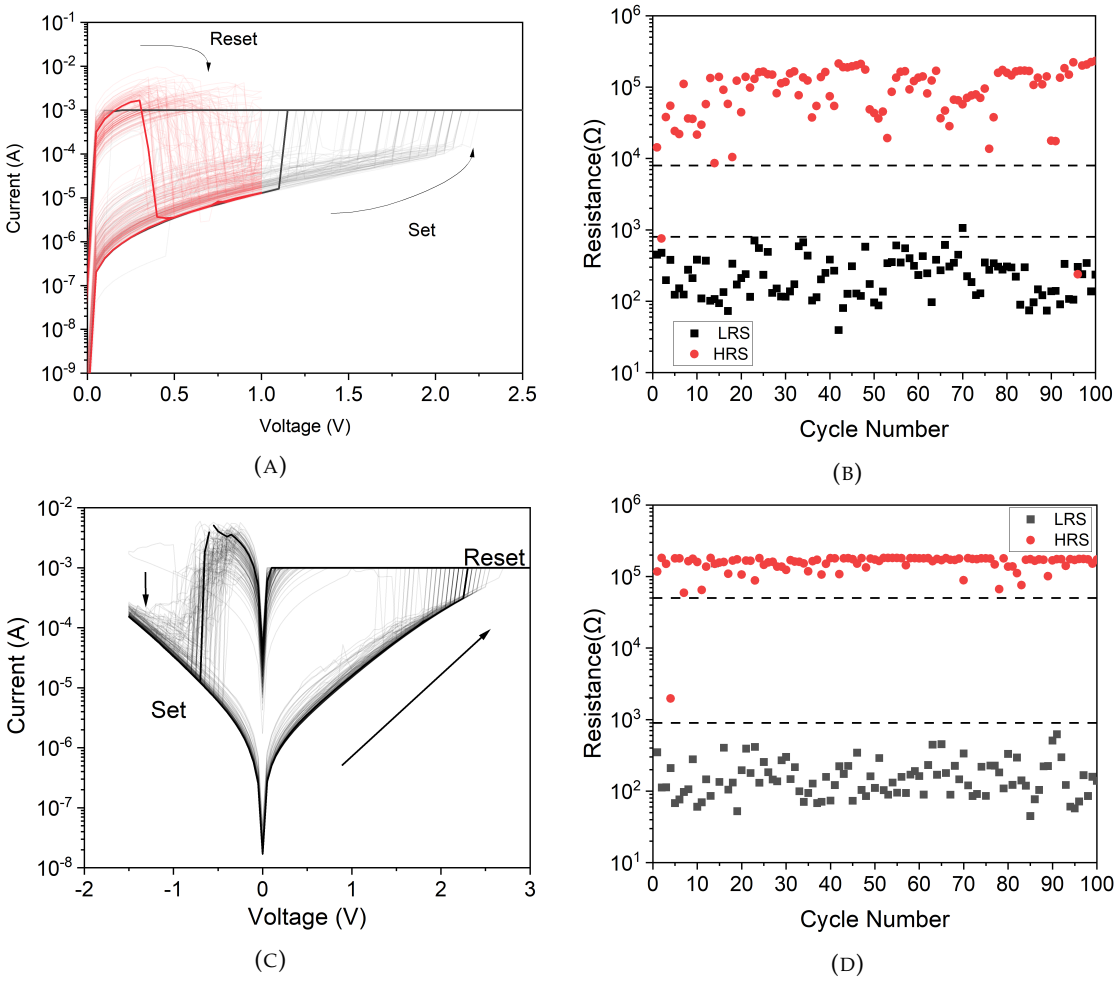
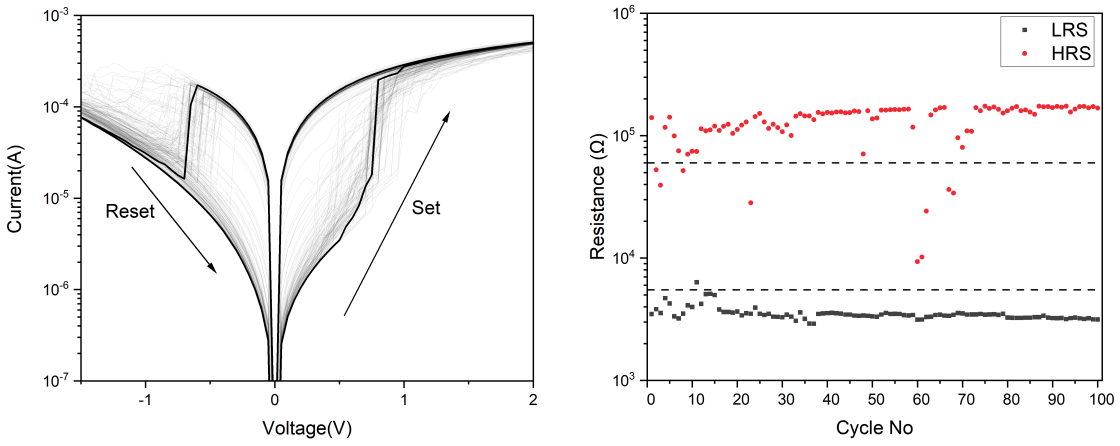


FIGURE 5.9: Characteristics through the application of a DC voltage bias measuring 100 switching cycles (A) I-V graph of unipolar switching with a typical cycle highlighted. (B) Unipolar resistance states across 100 cycles. (C) I-V graph of bipolar switching with a typical cycle highlighted. (D) Bipolar resistance states across 100 cycles.

resistance states of the bipolar scheme is more stable while also yielding a higher resistive ratio. This is important especially for radiation hardened resistive memory devices, as it requires a stable switching characteristic. For this test the semiconductor analyser used did not have internal capabilities for a current compliance when pulsing, as described above. DC cycles were measured with the current compliance circuit described in section 5.1 to determine if the setup was suitable. Figure 5.10b shows the IV characteristics of 100 cycles taken from a device with the compliance current in series. As we can see the device is able to switch between the HRS and LRS with only a few failed cycles. The LRS and HRS keeps its stability, but with a lower resistive ratio of around 10^2. This is because the effective resistance of the circuit is around $2.4k\Omega$. As with table 5.1 we can see that the usual resistance of the LRS is around 200Ω. Therefore, this decrease in the resistive ratio can be attributed to the higher drop in potential across the compliance circuit in series.

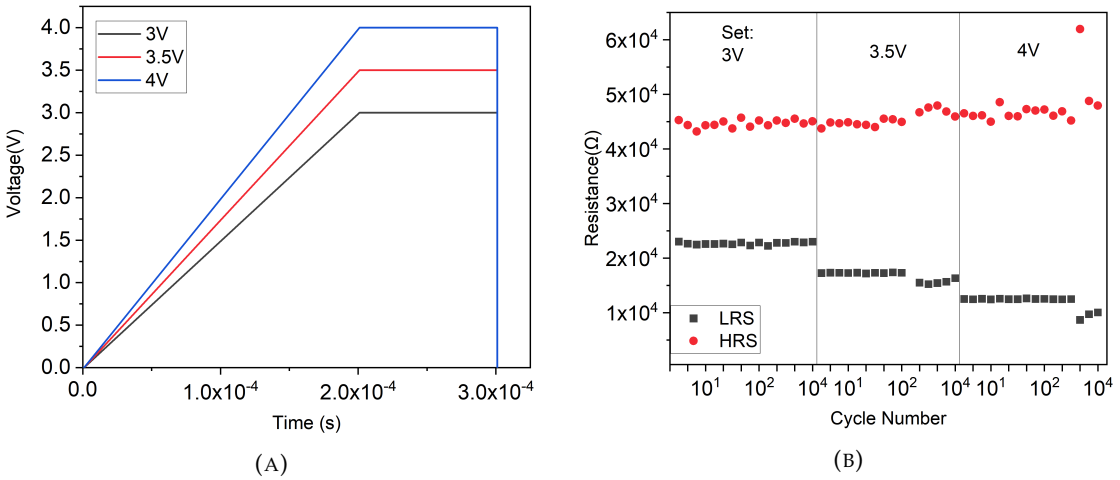


(A) (B)

FIGURE 5.10: DC characteristics using an external current compliance circuit in series with a SiC device (A) I-V graph of 100 cycles with a typical cycle highlighted (B) Resistance states across the 100 cycles

5.3 Pulsed Switching Results

Before being able to test the endurance characterisation of the devices, an adequate set and reset pulse had to be investigated. The first thing that was investigated was the effects of altering the rate of change of the set pulse. Therefore, a 300μs pulse was made with a rise time of 200μs a width of 100μs and a fall time of 500ns. This is shown by figure 5.11a. The device was then pulsed on and off 10^4 times with the resistive ratio read 4 times per decade. With a 3V and -4V set and reset pulse used it was found that a resistive ratio of 1.8 could be achieved. By increasing the amplitude, and hence rate of change, it was possible to full control the LRS showing multi-level switching, shown in figure 5.11b.



(A) (B)

FIGURE 5.11: Control of the LRS through the alterations of the input Set pulse: (A) V-t graph of the three separate Set pulses used (B) Resistance states across 10^4 cycles using the three separate input pulses on the same SiC device.

Taking this pulsing scheme, a device was testing using 10^7 and showed consistent switching with the LRS and HRS, using 3V, figure 5.12b. By increasing the set rise time to 300μs and the amplitude to 3.5V we are able to increase the resistive ratio of the device to around 100 across 10^7 cycles, figure 5.12d. This pulse train, however, requires an initially settling tin-me of 10^5 cycles before being able to give the consistent resistance switching states. This is shown in figure 5.13a. As well as this, across the 10 million cycles, the LRS appears to be breaking down by continually reducing its resistance, shown in figure 5.13b. This means that there is potentially could be a full dielectric breakdown, in which the device would eventually not be able to reset. This could be due to the increase in the amount of time that a potential is placed across the device. This would be similar to how it is considered DC cycling to be more stressful on a device than pulsing, due to the stressed caused by the measurement.

Therefore, reducing the time of the input pulse to 200μs, increasing the amplitude to 4V, and having the rise/fall time to be 500ns we can try to mitigate these effects. The reset voltage for this pulse train was also altered to 3v, as it was shown to be able to fully reset the device, without degrading the switching performance. Looking at figure 5.15b we can see that the resistive ratio remain consistent across the device, even with a reduced pulse time. As well as this, there was no need for an initial settling time and there appeared to be no apparent breakdown in either the LRS or HRS.

It is important to understand the breakdown mechanism of these RRAM devices, so that we can be be confident testing the radiation hardness of the device, without questioning if any breakdown is due to the inherent nature of the device. Therefore, an endurance test was conducted to look to see the breakdown effects of cycling using the 200μs pulse developed. However, simply using the same endurance parameters above does not provide enough information to analyse any breakdown or deviation in the resistance states across these large cycling tests. An example of this is figure 5.14, which shows a measurement taken of 100 million cycles. These memory cells clearly show high endurance capabilities, but no further information can be extracted from this graph. Therefore, a measurement scheme was developed so that the devices could be accurately testing for long term cyclability, whilst being able to compare any deviation in the resistance states over cycle number.

The measurement was broken down into two parts. The first was determining the total endurance that we would like to measure. Given that the memory requires a 200μs to cycle Set and Reset and it is clear that the device is able to cycle hundreds of millions of times, the maximum endurance that was set was 10^9. This allows enough data collection to either observe or predict degradation and cyclability of the memory cells.

If we were to simply set this and measure, we would not be able to gather any meaningful data, as we see in figure 5.14. To add to this we create a smaller endurance loops

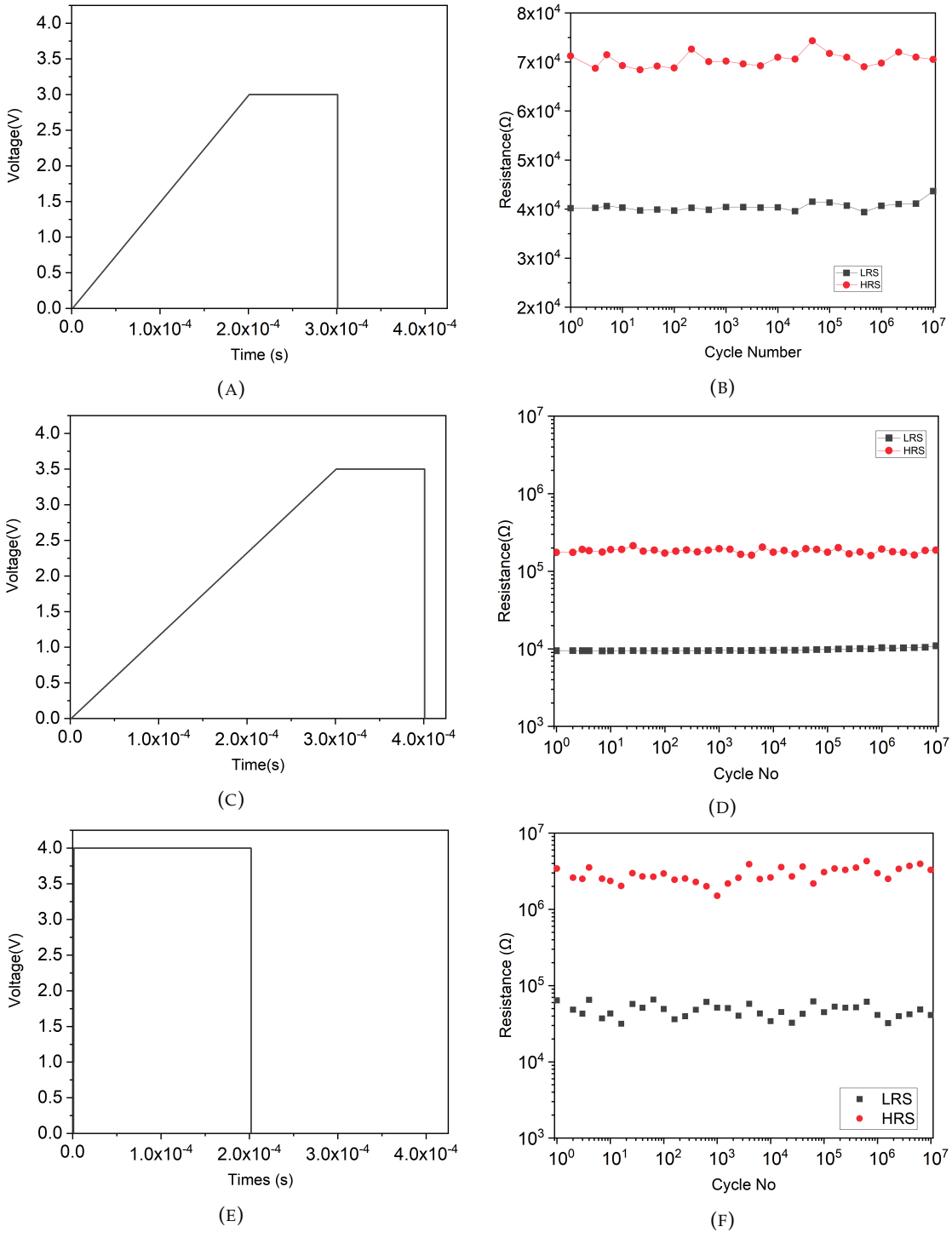


FIGURE 5.12: (A) (C) and (E) are V-t graphs that present the alterations of the rise time and pulse width of the input Set pulse to control the Resistive Ratios. (B) (D) and (F) show the Resistance states across 10^7 cycles and the effects of the resistive ratio with the input pulse: (A) presents a rise time of 200μs and a top width of 100μs. (B) shows consistent switching across 10^7 cycles with a small resistive ratio. (C) Presents an increase in the rise time to 300μs. (D) The increase in the rise time gives a large increase in the resistive ratio. (E) Presents an input pulse withe a rise time of 500ns and a top width of 200μs. (F) Shows that a fast rise time and an increase in the top width can achieve a similarly large resistive ratio.

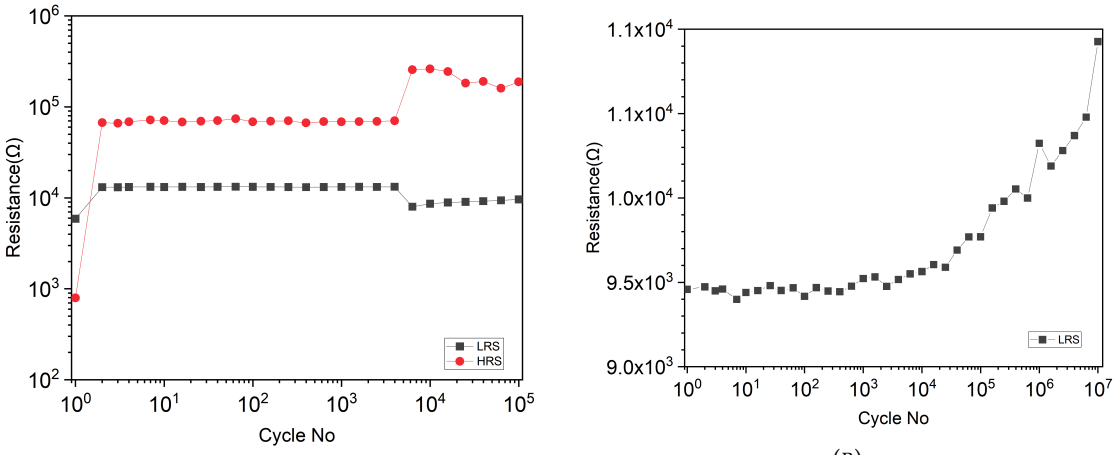


FIGURE 5.13: The potential of error states with the use of a long rise time. (A) presents the first 10^5 cycles using a rise time of 300μs, which requires an initial settling time. (B) Shows the slow breakdown of the LRS with an increase in cycle number using a rise time of 300μs.

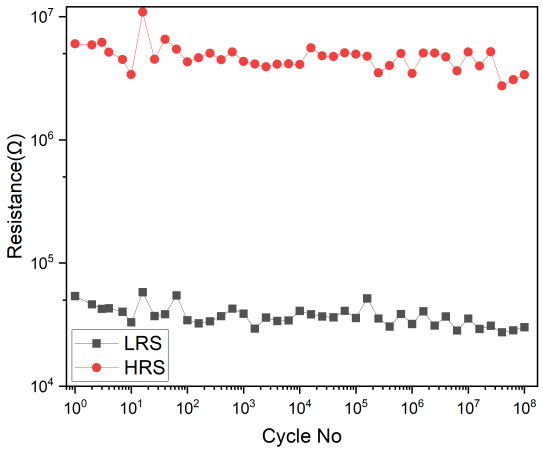


FIGURE 5.14: Endurance graph showing 100 million cycles, using a 200μs Set and Reset Pulse.

within the billion cycle, each being set to 10^7 cycles, with measurements being taken 5 times per decade. Each individual 10^7 will be noted as a Supercycle. This is not a standard system, but something that was created for this thesis. The Supercycle could then be looped 100 times to give a total of a billion cycles. Measuring the endurance using the Supercycles allows for enough data points to be measured to determine the noise level and deviation of resistance states, whilst allowing for a reasonable measurement time. The total time for this measurement setup came to be 12 days in total. Figure 5.15a shows an example of the measurement setup using 10 cycles per Supercycle, with a loop of 10, giving us 100 total cycles. Along with this figure 5.15b shows an example of the switching time of a typical set and reset pulse measured using the b1530A semiconductor analyser. As we can see in the graph the Set process is limited by the compliance current circuit to around 1mA, which we can see when the device turns on.

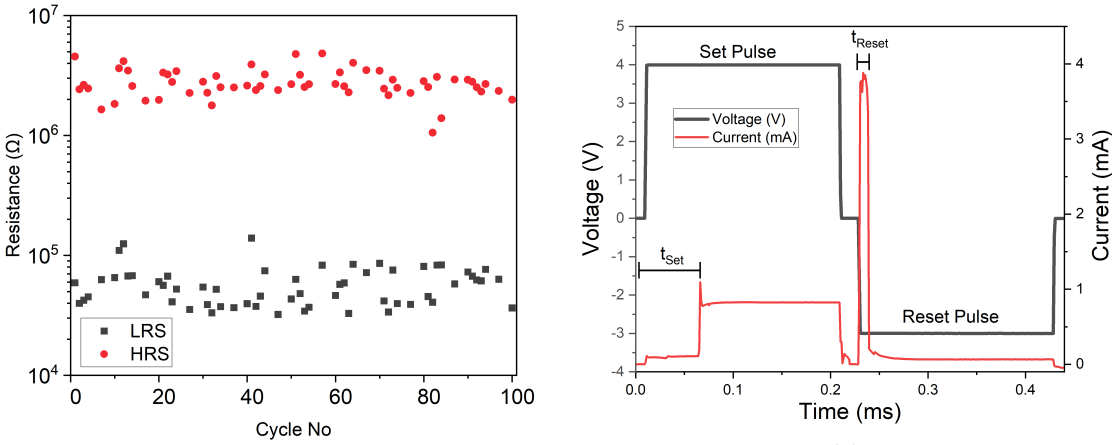


FIGURE 5.15: Initial Super Cycle looping test. (A) Resistance states of the first 100 cycles using 10 cycles per SuperCycle with the resistance measured 5 times per Super Cycle. (B) example of the Set and reset pulse with a 200μs width and a 500ns rise and fall time. The measured current was monitored every 1μs using the b1530a

This current compliance is lifted when the polarity of the voltage is switched, which is apparent when the current goes up to 4mA before the device is reset to the off state.

Utilising the Supercycle scheme described above, figure 5.16a shows the resistive states across 10^9 switching cycles. This device shows consistent cycling and is one of the highest endurance measured for a CBRAM based resistive switching cell. As well as this, there appears to be no apparent degradation in the resistive states and maintains a large resistive ratios of around 10^2. This measurement shows the potential of these types of memory cells for both radiation harsh environments and for a commercially scalable next generation memory, due to its simple fabrication process being compatible with back-end-of-line processing.

Looking at the cumulative probability graph of the 1st, 50th and 100th Supercycle in figure 5.16b it is clearly that there is a slight drift in the resistance states. A more detailed analysis in figures 5.16c and 5.16d show the cumulative probability of the LRS and HRS of the first 10 Supercycles. We can see that as the cycle number increases the Supercycles shift towards the LRS. We can also see that the deviation of the resistance states improves with the cycle number, due to the gradient of the data sets becoming steeper with each Supercycle.

By analysing the average standard deviation and resistance states of each Supercycle, we can determine the change in the standard deviation and drift towards LRS over the entire 10^9 cycles. This is extracted data is seen in figure 5.17. We can see that both the resistance states and standard deviation take around 200 million cycles for the device to settle. After this point there is no apparent degradation in the mean or deviation in resistance, states. This data shows that the fabricated resistive switching cells do not degrade, but instead improve with cycle number.

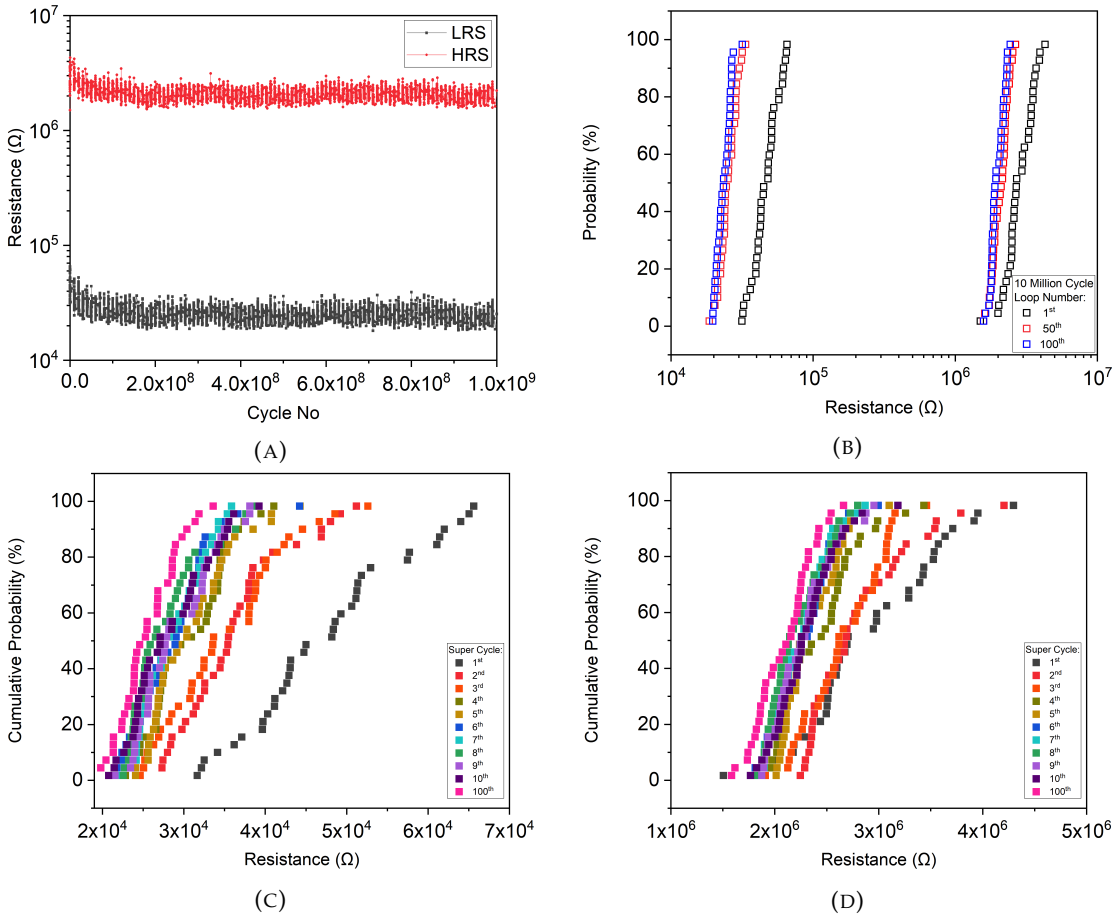


FIGURE 5.16: (A) Endurance tests using 100 Supercycles with each having 10^7 cycles and the resistance state measured 5 times per decade, giving a total of 7200 points of data. (B) The cumulative probability distribution of the 1^{st}, 50^{th} and 100^{th} Supercycle. (C) cumulative probability of the first 10 and last Supercycles in the LRS (D) cumulative probability of the first 10 and last Supercycles in the HRS.

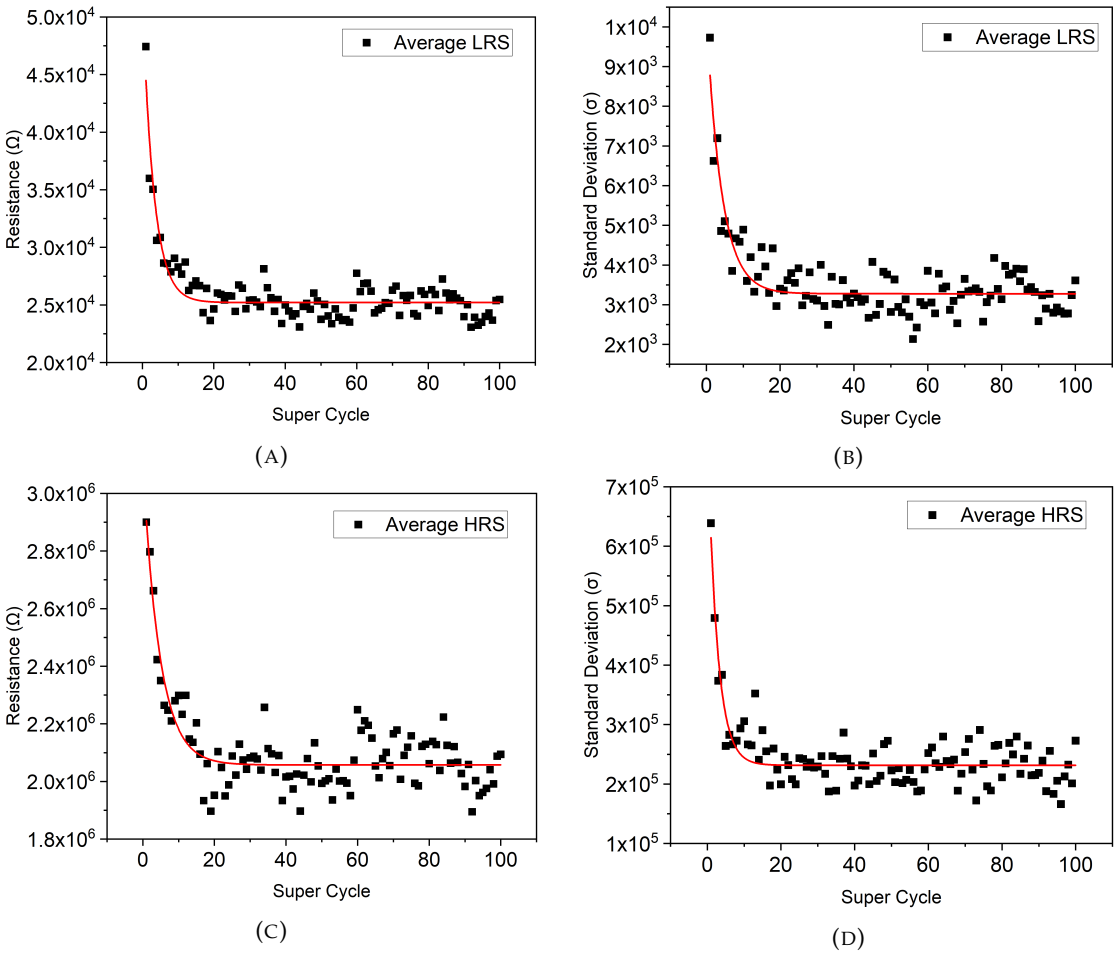


FIGURE 5.17: (A) Mean resistance of the LRS in each Supercycle across 10^9 cycles (B) Associated Standard deviation of the LRS (C) Mean resistance of the HRS in each Supercycle across 10^9 cycles (D) Associated Standard deviation of the HRS.

5.4 Wafer Reproducibility

Only a single wafer was fabricated for the initial Bilayer test. Therefore, more wafers were fabricated to look at its reproducibility. A detailed analysis of the DC operations was investigated to determine whether its switching characteristics matched that of the Bilayer wafer. Figure 5.18 shows the formation of a memory cell from it's pristine state. Like the Bilayer wafer we need a current compliance and voltage greater than 1mA and 8V to form the initial conductive bridge.

Figure 5.19a show the IV characteristics of 100 cycles. The device initially starts in the HRS and a DC voltage is applied from 0 to 4V with 50mV steps and a compliance current of 1mA. The device is then Reset using bipolar switching by applying a voltage sweep between 0 and -2V. These voltages are similar to those applied to the Bilayer devices and it shows the similarity in the switching characteristics.

Figure 5.19b shows the resistive states across 100 cycles using three devices of sizes between 30 and 50 μm, with their switching values presented in table 5.2. As we can see they are comparable to the switching characteristics of the Bilayer wafer, with the set voltages around 2.4 and reset under -1V. The resistive ratio was also around 10^3 which is also similar to the previous sample. There also appears to be a trend with the HRS shifting depending on the size of the device, increasing the resistive ratio with a decrease in size. This could be a consequence of the bilayer causing the HRS to become partially interfacial, possibly due to the rupture of the filament in the SiC layer, as discussed in Chapter 2.

TABLE 5.2: Average DC characteristics of 100 cycles using devices with diameters of 30, 40 and 50 μm

Diameter of Device (μm)	Average Set (V)	Average Reset (V)	Average Ratio
30	2.3 $\pm$ 0.43	-0.803 $\pm$ 0.23	8.6 x 10^3
40	2.6 $\pm$ 0.48	-0.821 $\pm$ 0.27	7.2 x 10^3
50	2.4 $\pm$ 0.48	-0.8735 $\pm$ 0.21	3.1 x 10^3

Looking at figure 5.20a we can see that the LRS is dominated by Ohmic conduction from the linear I-V graph of the average LRS of 100 cycles. Figure 5.20b presents a $ln(I) - \sqrt{V}$ graph of the average HRS of 100 cycles, showing that Schottky emission is the dominant mechanism. With these measurements we can say that the devices exhibit similar switching characteristics to the Bilayer wafer. Therefore, we can say that these devices attribute similar characteristics to the Bilayer wafer and could be used to determine the tolerance of extreme environments.

The first experiment to determine the device's suitability to extreme environments is a retention test. This was done using a temperature dependant probe station, with the 2x2cm chip cut and placed on a stage that was heated to 85^{o}C. In between the stage and the sample, a high temperature grease was used to improve the heat transfer

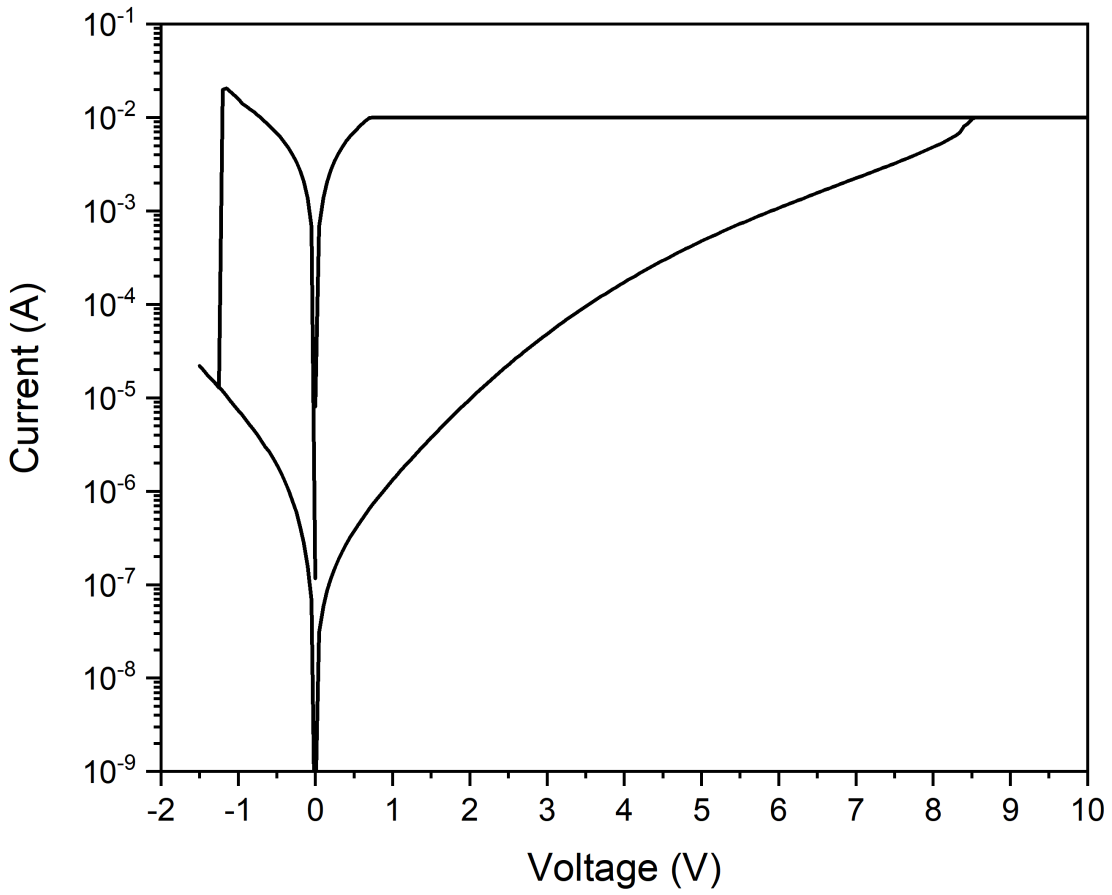
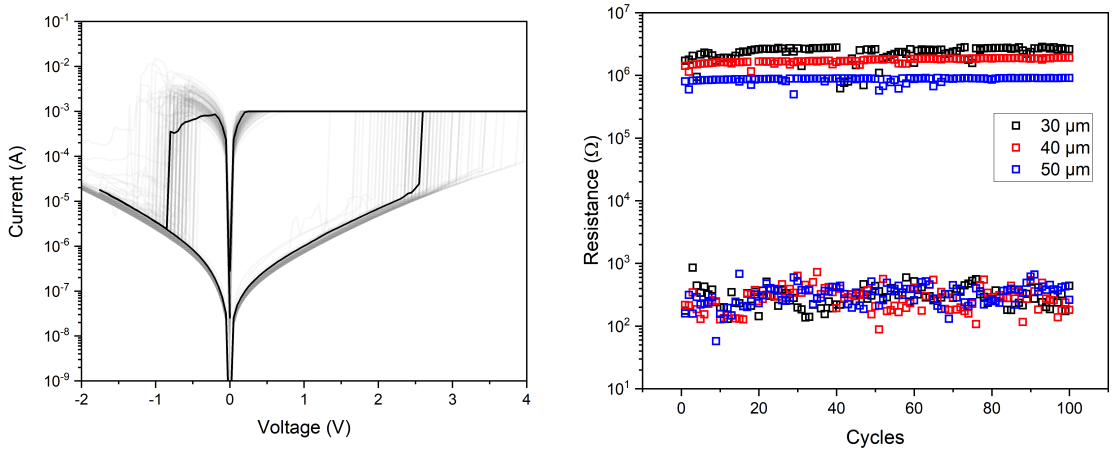
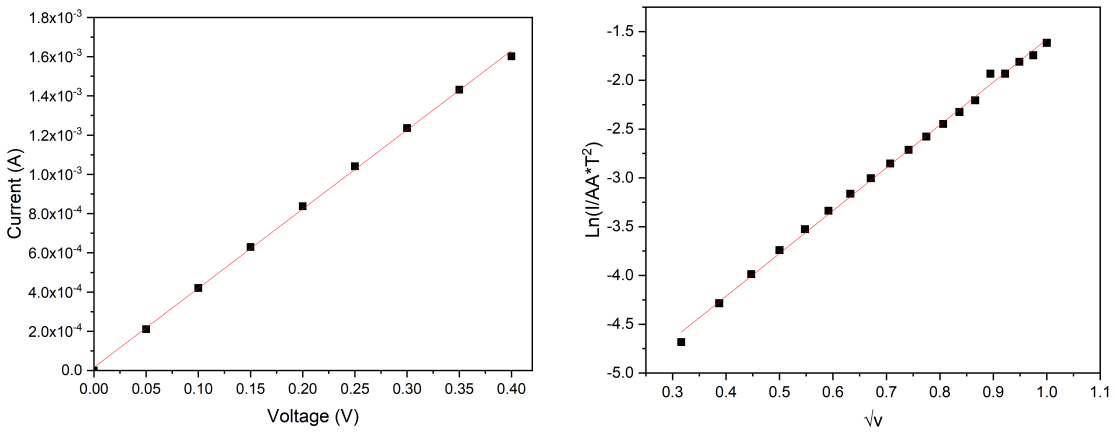


FIGURE 5.18: I-V graph from the 2nd Bilayer wafer showing the formation of the device from Pristine state



(A) (B)

FIGURE 5.19: (A)I-V graph of 100 cycles after the formation of the 2nd Bilayer wafer (B) 100 cycles of the HRS and LRS of 30, 40 and 50μm sized device showing similar stable resistive switching to the Bilayer SiC devices.



(A) (B)

FIGURE 5.20: (A) I-V graph using the average of 100 cycles in the on state between 0 and 0.4V, showing ohmic conduction is the dominate conduction mechanism in the LRS. (B) $ln(IAA * T^2) - \sqrt{V}$ graph using the average of 100 cycles, showing schottky emission is the dominate conduction mechanism in the HRS.

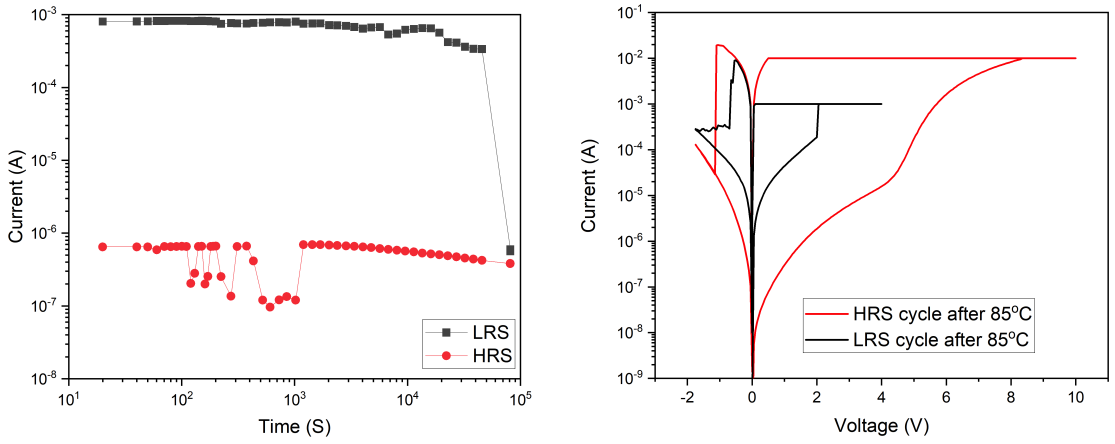
between the stage and the chip. The chip was also left to reach temperature for around 30 minutes to make sure that there was even heating across the entire sample.

Two separate devices were measured, one in the LRS and the other HRS. Each state was measured at 0.1V 10 times per decade over 10^5 seconds. This was to reduce the stress applied to the device over a long period of time, as continually reading, for example every 30 seconds, could provide enough stress to alter the bit state.

As we can see by figure 5.21a the devices were able to hold their bit states below 10^5 seconds at this high temperature. It should be noted, however, that the computer controlling this setup had froze during the final measurements, hence there are a few data points missing in the data set. However, we can see clearly that the devices are able to withstand their bit states of around 10 10^4 with a minor drift in their resistances. This drift is not large enough to cause any read errors during normal operation.

After this measurement was taken, a standard DC sweep was conducted on both samples, figure 5.21b. As we can see the device that was at the LRS (and broke down the HRS) was able to cycle normally after the retention test. The device left in the HRS, however, appeared to have to undergo a reformation of the conductive bridge. This is because its IV mimics that of the initial formation of the device, requiring a current compliance of 10mA and a voltage greater than 8V.

To further understand this mechanism devices were cycled at temperatures varying between 25 - 200^{o}C. Figure 5.22a shows the IV characteristics of DC cycling up to 125^{o}C, which shows consistent switching, with devices being able to be cycled multiple times. We can see that as the temperature increases, the HRS seems to decrease in resistance. Above this temperature the device becomes unstable and the device has to be set multiple times to be able retain it bit state, figure 5.22b. Above 175^{o}C degrees and the device



(A) (B)

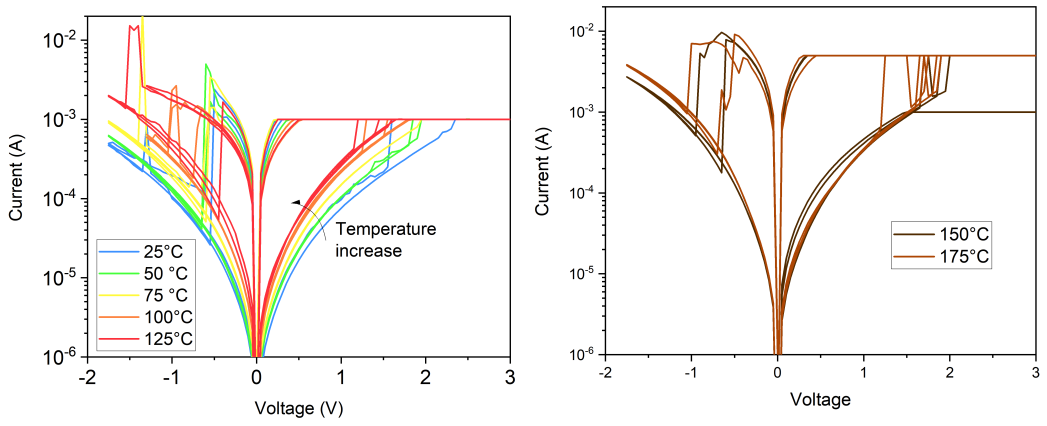
FIGURE 5.21: (A) Shows the retention measured of a 120μm device at 85^oC. The last point was measured manually as the automatic retention setup broke down before this measurement point and could be the reason for the failed LRS. (B) IV cycles after the retention measurement were taken of both the devices that were left in the HRS and LRS

is not able to be switched to the LRS, no matter how many times the Set procedure is applied. Looking at figure 5.23a we can see that the linear fit to the $ln(I) - \sqrt{V}$ plot shows that at all temperatures the HRS resistance is determined by a reversed Schottky barrier.

Both breakdown of the LRS and HRS from the retention test and the instability of the switching characteristics above 125^{o}C could be due to the high temperatures causing a thermal breakdown of the filament, in a similar mechanism to the unipolar reset mechanism described in Chapter 2. As stated in this chapter, the reset process is a thermal process and so the increase in temperature could facilitate the rupture of the filament.

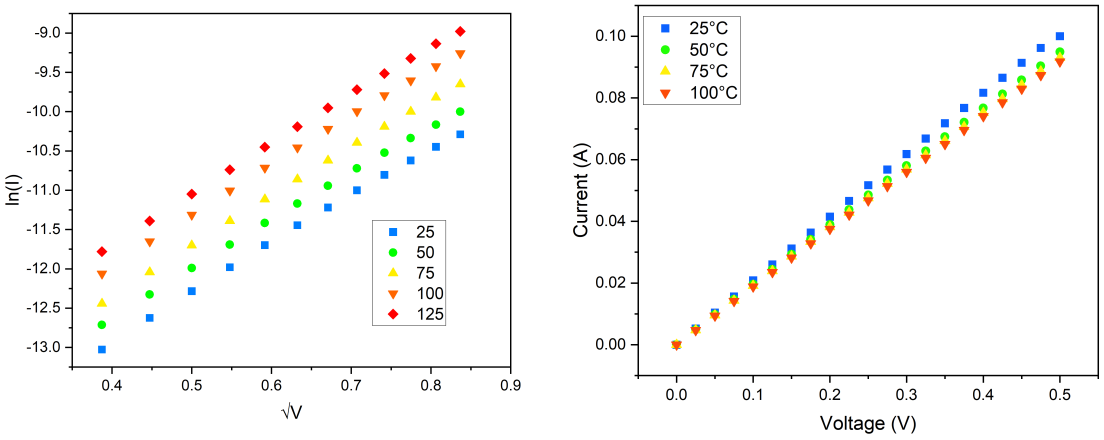
A single device was also switched on and its resistance was measured across increasing temperatures, figure 5.23b. By normalising these resistances it is possible to extract the temperature coefficient of the filament, figure 5.24. This was extracted to be 1.39 x $10^{-3}K^{-1}$, which is in agreement with the temperature coefficient of resistance of Cu nanowires [41].

The last measurement taken with these devices was to look at the endurance to see if they matched those from Bilayer wafer. Figure 5.25 shows the endurance of 10^7 cycles that were measured using the same pulses that was used for the Bilayer wafer. As we can see there is a clear drift of the HRS towards the LRS with cycle number. This could be corrected easily by increasing the time or the amplitude of the Reset pulse. However, after this measurement was taken the initial COVID-19 lockdown began. Once the initial lockdown had eased all of these devices had degraded. New samples were attempted to be fabricated, but there wasn't a chance to both make new devices and measure them with radiation dose, due to the problems associated with the pandemic.



(A) (B)

FIGURE 5.22: (A) IV characteristics of a stable switching cycle at temperatures between 20 - 125 ^oC. (B) IV characteristics showing the devices unable to switch at temperatures greater than 125^oC.



(A) (B)

FIGURE 5.23: (A) $ln(I) - \sqrt{V}$ graph showing Schottky conduction with a change in the temperature (B)I-V graphs showing Ohmic conduction with a change in the temperature.

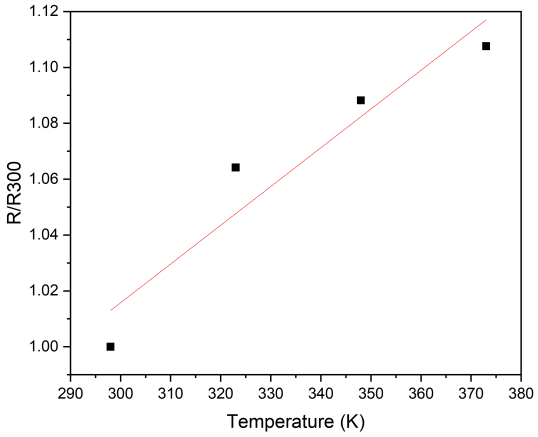


FIGURE 5.24: Normalised resistances of the LRS state at each temperature, with the extracted temperature coefficient of the filament being 1.39 x $10^{-3}K^{-1}$

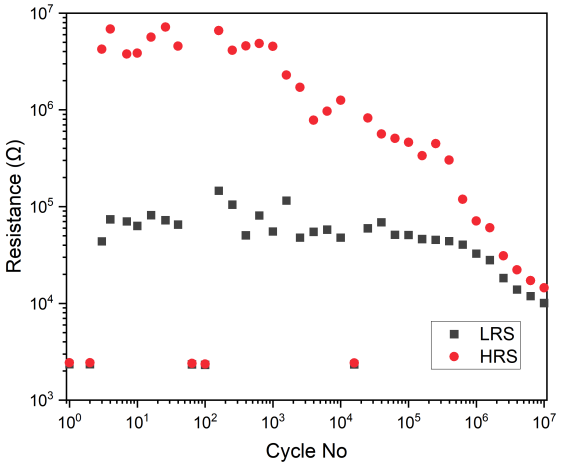


FIGURE 5.25: 10 million cycles measured 5 times per decade, showing a breakdown of operation over cycle number towards the LRS, using the same input pulse characteristics as the Bilayer wafer.

Therefore, instead of describing the radiation hardness of these devices, the next section will focus on future radiation hardened experiments that were supposed to be investigated.

5.5 Future Radiation Experiments

The first radiation experiment would be to analyse the hardness of the SiC-based memory cells against gamma radiation. This is important to compare the PECVD thin film hardness against the 2MRad dose that was applied to sputtered samples [5]. This would involve comparing the IV characteristics before and after radiation dose, using radiation doses from 1-5MRad, to see if there is any alteration in the resistance states.

As well as this, devices should be exposed to single heavy ion particles to determine any possible effects of SEE. This could also include mapping of the conductive filament, with comparisons between isolated and overlapped resistive switching devices to determine if there are any alterations with the filament formation. This is because, as discussed in chapter 2, the edges of the overlapped devices would have significantly more defects than central area, whereas the isolated devices are purely confined. Testing both of these devices to SEU could show both how the filament formation differs, but also if one form of devices structure is more resilient to ion bombardment than the other.

Another radiation harsh experiment would be to see look at the effects of altering the amount of neutrons radiation applied to the device. In the presence of a large neutron source (which is an important parameter for such nuclear defence and energy), can undergo neutron transmutation doping (NTD) of silicon [186]. This is where a neutron interacts and gets captured by a Si-30 atom and produces radioactive Si-31. This atom

then undergoes a beta decay, whereby the neutron transforms into a proton and releases an electron and an anti-neutrino. Therefore, Si-31 decays into P-31 (Phosphorus). P-31 is a well understand element that is conventionally used to dope Silicon wafers. NTD is used in some facilities offset the cost of running reactors. Knowing this known phenomenon it is important to understand the possible doping effects over-time that neutrons could pose to silicon-based resistive memory. This experiment would involve investigating potential alterations in conduction, due to radiated doping of the dielectric.

5.6 Conclusion

In this chapter we have investigated bilayer resistive switching devices with the structure W/Si/SiC/Cu. This W/Si/SiC/Cu is the first of its kind, with no other literature found on PECVD deposited Si/SiC-based devices. These memory cells exhibited consistent switching using a DC bias with a 1mA current compliance during the Set process and can be cycled over 100 times with an average Set and Reset voltage of 2.1V and -0.8V for a Bipolar mechanism and 1.7V and 0.7V for a unipolar.

Using an external compliance current circuit, a pulsed measurement scheme was implemented to analyse the long-term endurance capabilities. Using a 200μs pulse, it is possible to Set and Reset the memory cells at 4V and -3V over a billion times. Analysing the average resistance and deviation across this billion cycle range, it was found that the memory cells showed no degradation and instead improved with cycle number. The endurance and stability is one of the highest recorded endurances for CBRAM based resistive memory. Furthermore, the cells uses a lower voltage compared to Sony's Cu based resistive switching cells (with a selector in series) showing an endurance 100million cycles using 7V at 100ns, with visible degradation at 10 million cycles [187, 188]. As well as this, it also outperforms current commercially available RRAM devices that are sold specifically for their radiation harsh tolerance, which have an endurance of 10^6 cycles [118]. The high performance found in this chapter is extremely important for radiation harsh environments, as these systems are difficult to repair or alter if they fail. The large endurance, with improved performances with cycle number, and large resistive ratio show that the PECVD SiC more cells in a BEOL compatible processes can produce a highly scalable memory for embedded systems.

Furthermore, the designed was re-fabricated to look at the reproducibility of the electrical performance. The memory cells showed similar electrical characteristics to the Bilayer wafer, showing the reliability in the fabrication process developed. Temperature dependant switching showed that the devices could operate to 125^oC, with the HRS reducing its resistance with an increase in temperature.

Chapter 6

Crosspoint Structures and Investigation of Sneakpath

This chapter focuses on the initial investigation of Crosspoint structures and provides a template for the optimal fabrication methods and analysis of parasitic leakages. This can be used in future investigations to develop SiC-based Crosspoint structures for use in embedded systems and AI processing. This chapter serves as a proof of concept and the full characterisation of large Crosspoint structures is outside the scope of this project. As well as this, any development to overcome sneakpath is also outside the scope of this project.

6.1 E-beam Device Design and Fabrication

The devices that were fabricated were designed so that they could also be utilised for future investigations into Crosspoint structures. Single devices were included so that their I-V characteristics could be compared to the effects of combining ReRAM into arrays. The arrays that were added to the design included a 2x2 and 10x10 structure in the initial version of the masks. Subsequent design changes also added a 1kb (32x32) Crosspoint structure. The redesign of this mask and the reasoning is outlined in section 6.1. An example of this type of device that was fabricated is shown by figure 6.1

The first part of the design was to determine which form of Crosspoint structure to fabricate, which can be split into two varieties. These are known as layered and confined arrays and their differences are shown in figure 6.2. The layered arrays have a simple fabrication process in that they only require two lithography steps. The first lithography step is used to pattern the bottom electrode, while the second is used to pattern and deposit both the dielectric and top electrode. This causes the dielectric and top electrode to wrap around the bottom contact. This means that there is less control

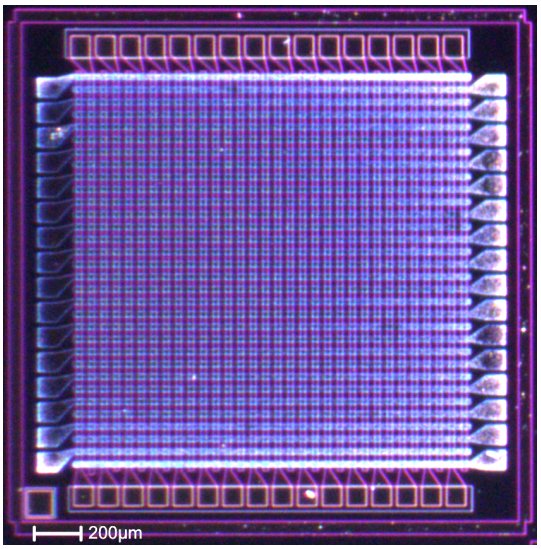


FIGURE 6.1: Optical image of a 1kb chip that I have fabricated fully using a CVD-based SiC dielectric. These cells could not be measured as a problem with etching resulted in the bottom electrode being unable to be contacted.

as to where the filament is formed in the device structure. These filaments could form at the edges and sides of the bottom contact, where the dielectric is at its thinnest. To confine the filament to specified area confined arrays can be utilised. These confined devices have extra fabrication steps to define a specified region to be able to confine the formation of the filament, which would be surrounded by an insulating layer.

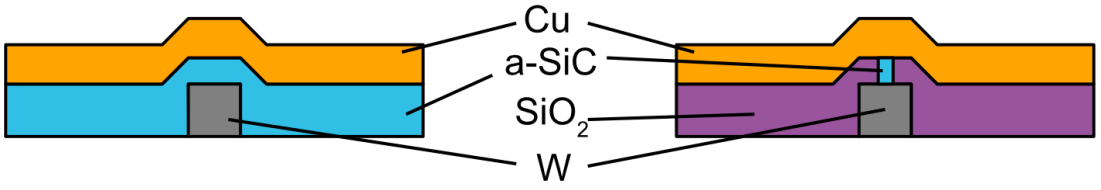
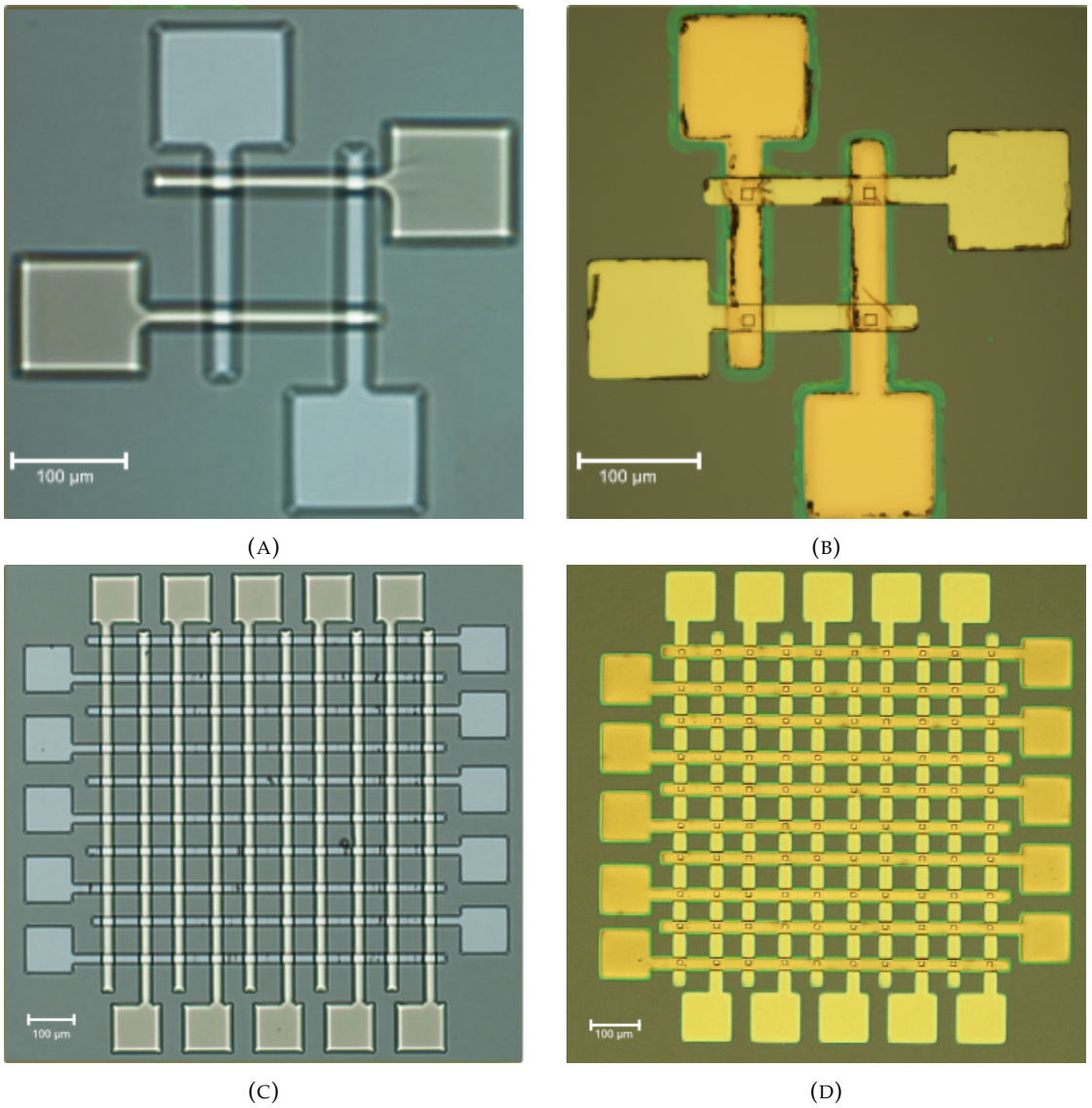


FIGURE 6.2: Representation of the cross sections of (left) a layered memory cell and (right) a confined memory cell for a Crosspoint array.

To determine if there were any benefits between the two forms of Crosspoint structures, a single layered wafer was still processed using the photolithography masks from the confined Crosspoint structures. Using this method meant that all the designs had a fixed size of a diameter of 20μm.

There were two sizes of arrays that were initially designed for the sneakpath investigations. 2x2 arrays were the main focus of this project due to it being the optimum design to study sneakpath. 10x10 arrays were designed for future investigations into a more complex analysis of sneakpath, as they require the design of peripheral circuitry to analyse all 100 devices in each chip easily.



(A) (B)

(C) (D)

FIGURE 6.3: Optical images showing fabricated arrays using both layered and isolated types. (A) 2x2 array using the layered method (B) 2x2 array using the confined method, which is evident through the square feature in between the interconnect. (C) 10x10 array using the layered method (D) 10x10 array using the confined methods.

Figure 6.3 shows an example of the fabricated designs. As we can see by the layered structures, the area of each device corresponds to the region in which the top and bottom electrode tracks intersect. The defined regions in the confined structures are the square shapes in between the intersections of the top and bottom electrodes. These squares shapes are holes that are etched into an insulating layer to allow the deposition of the SiC and Cu layers into a confined space. The fabrication of these designs is discussed in depth in the next section below.

The process flow of the fabrication for the Crossbar structures is shown by figure 6.4. All of the processing conditions for the tools and photolithography steps are the same as outlined in chapter 3, except for the SiC recipe. This is due to COVID 19 restrictions

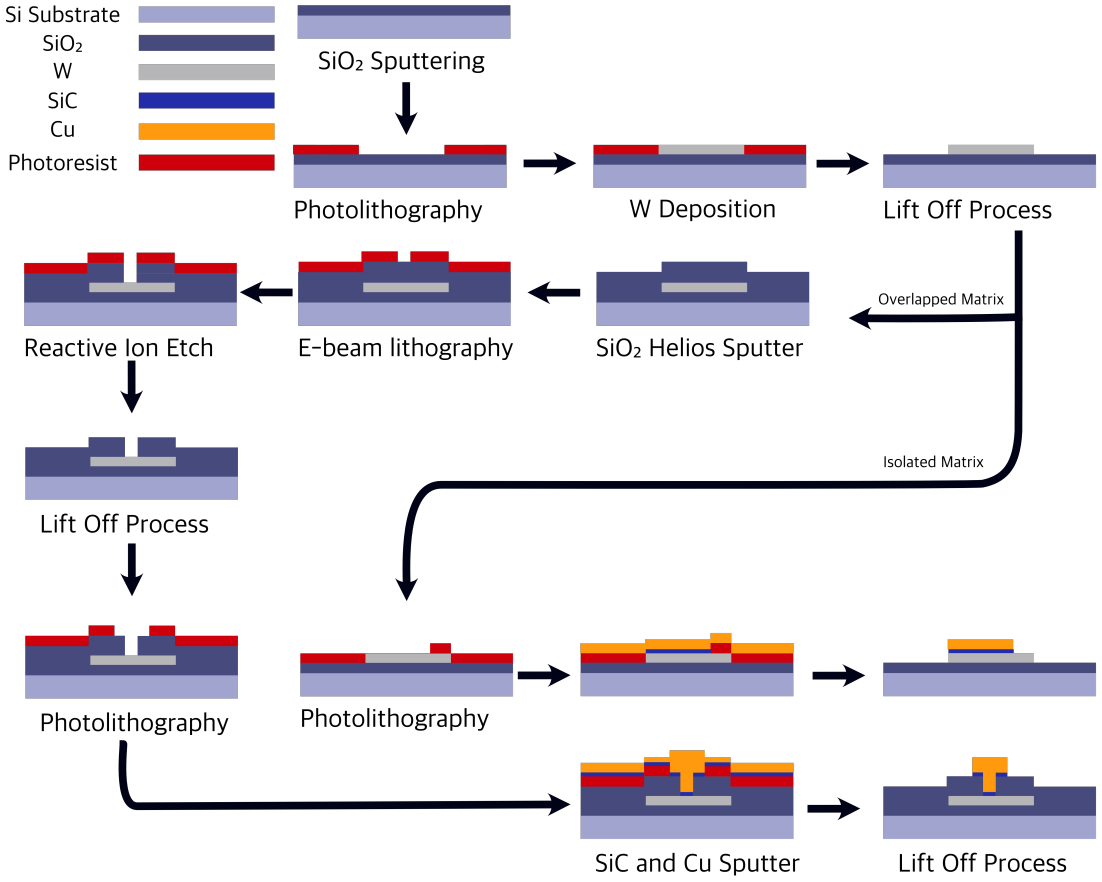
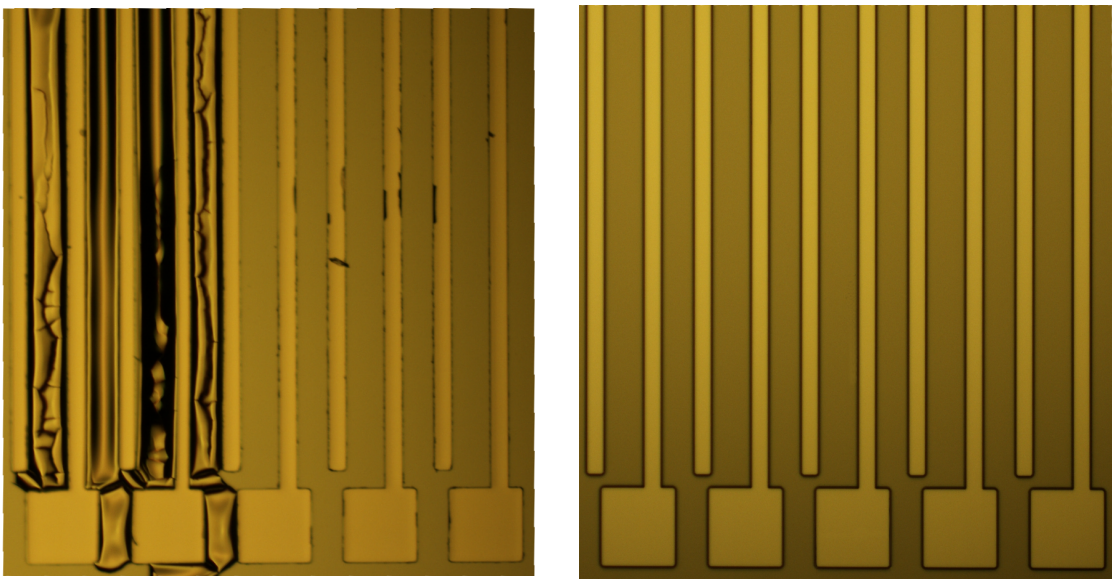


FIGURE 6.4: Process flow of the fabrication of the Crosspoint structures using both the layered and confined methods.

and so this chapter could not be completed using the high-temperature PECVD process. Instead, a sputtered SiC process had to be used.

As with the previous fabrication processes the first step was to insulate the wafer using 500nm of SiO_2, which was deposited using the Helios sputterer. The second step was to pattern and deposit the bottom electrode using AZ2070 and a lift-off technique. 100 nm of W was used for the bottom electrode and was deposited using the Angstrom Sputterer. Initially, shorts between the bottom electrode tracks appeared, due to a problem with the lift-off process. It was found that the lift-off process for the Crosspoint tracks required light ultra-sonic cleaning with the NMP solution to prevent any shorts between the lines, as shown by figure 6.5.

Once the bottom electrode had been deposited the layered devices could move to the last lithography step. The confined devices, however, still had further processing steps to be completed. This involved depositing a second layer of SiO_2, which acts as the insulation layer, so that the confined devices could be patterned. 200nm was deposited using the Helios sputterer. As there have been many reports of SiO_2 resistive switching



(A) (B)

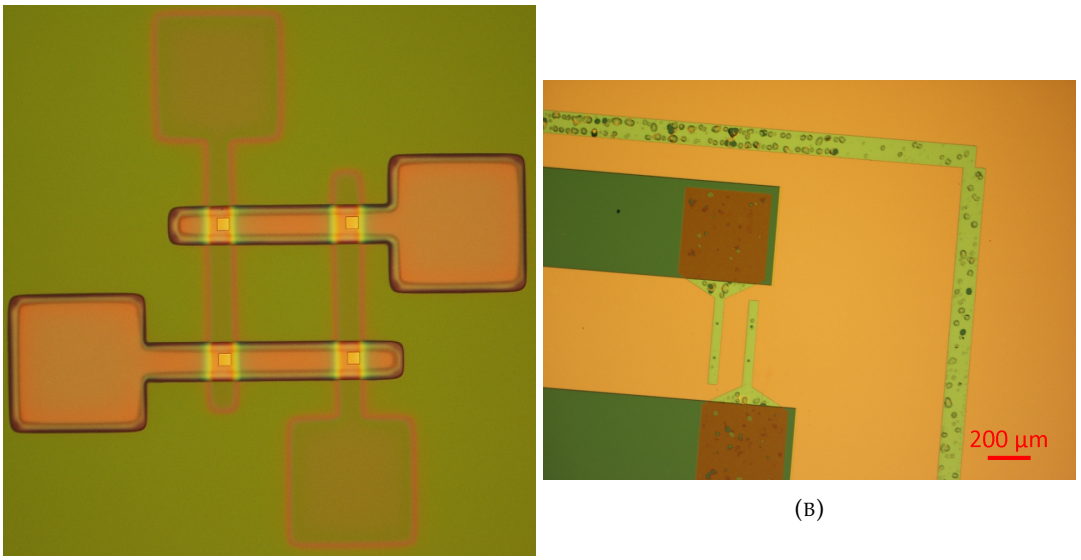
FIGURE 6.5: Lift off processes of the bottom W electrodes (A) using just NMP we can see the potential for shorts between the word and bit lines (B) using light sonication and NMP we get a clean lift off process

capabilities, the isolation had to be significantly thicker than the SiC layer [189]. This thicker layer was used to prevent any oxide-based switching from occurring.

In the initial fabrication process of the Crosspoint structures the SiO_2 was deposited on top of the wafers patterned with the same mask as the top electrode, figure 6.6a. This meant that there would be no need for any etching steps to open the bottom electrode for probing. This then required precise alignment when using the same mask for the top electrode, as the patterned lithography would have to sit exactly on top of the SiO_2 layer. To help with this process the patterning of the SiO_2 layer was underexposed, as a negative resist was used, causing the structures to widen. The top electrode was then overexposed which caused the structures to shrink. This allowed enough flexibility in the potential error to fabricated the wafers, however, the masks were redesigned to allow for a simpler alignment process.

The new design allowed the SiO_2 layer to be deposited throughout the wafer and, using S1813, windows were opened and etched to allow probing of the bottom contact. An example of this new fabricated design is shown in figure 6.6b. This method, however, was not able to be fully fabricated during the PhD due to time constraints. A wafer was attempted with the high-temperature PECVD dielectric, but a problem with the RIE etch rate caused the W layer to be etched away with the SiO_2 layer. As this fabrication takes up to 1 month to process it was not possible to re-fabricate the wafer and so in this chapter we only consider the devices that were made using version 1 of the designs.

After the insulation layer had been deposited the next step was to pattern the isolation area using e-beam lithography and ZEP as the resist. The processing conditions used



(A) (B)

FIGURE 6.6: Optical image showing two methods in patterning the SiO_2 layer and allowing access to the bottom electrodes. (A) Top electrode mask is used to pattern and deposit the isolation layer leaving the W layer open. This requires precise alignment when re-patterning the top electrode. (B) A separate mask and etch process to open windows to the bottom W electrode. This requires an easier alignment process and so gave the ability to fabricate 1kb without any shorts.

for this lithography is found in table 6.1. The devices that were fabricated had a range of diameters from 10μm to 100nm. Examples of these patterned devices are shown in figure 6.7 which presents SEM images taken of the active regions, after the full fabrication of the Crosspoint structures, of a 5μm and 500nm device.

TABLE 6.1: Process conditions for defining the confined region using e-beam lithography

Processing Conditions	Ebeam Resist (ZEP)
Spin Speed (RPM)	5000
Prebake temperature ^oC//time (s)	180/180
Beam exposure conditions	100kV at 1nA (double check)
Developer/time (s)	ZEDN50/135

Once the devices had been patterned the SiO_2 layer was etched using the RIE method and a standard SiO_2 etch recipe. The resist was then lifted off using NMP. The confined wafer was then ready to move to the final lithography step, which patterns the top electrode. AZ2070 was used with the lift-off process and the SiC and Cu were sputtered in the same chamber of a magnetron sputtering system. The processing conditions of the deposition is outlined in table 6.2. This deposition provided 40nm of SiC and 100nm of Cu. 40nm of SiC was deposited as previous research has shown that this thickness, using a 1:1 SiC sputtered target, provides adequate thickness for resistive switching devices.

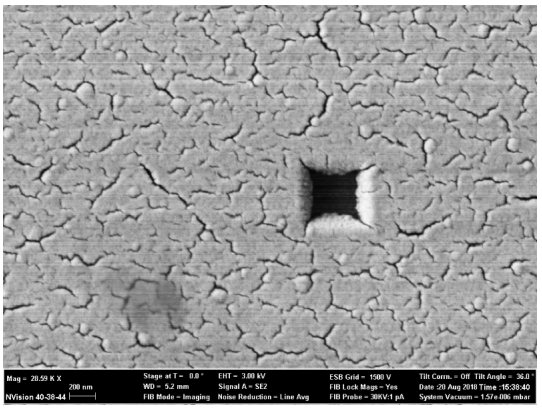


FIGURE 6.7: Scanning electron micrograph of the top surface of the top electrode of a confined cell. The Cu electrode shows cracks on its surface and black square region is the confined cell. The black colour is due to the sharp transition in depth of the 500nm cell, as the confined area has a depth of 200nm

TABLE 6.2: Process conditions used to sputter the SiC dielectric and Cu for the Crosspoint structures. 5 sccm of Ar was used as the flow rate

Target	Power (W)	Deposition rate (nm/s)
DC Source (Cu)	120	0.248
RF Source (old target SiC)	250	0.095
RF Source (new target SiC)	250	0.063

6.2 Crosspoint Memory Electrical Characteristics

The initial characterisation of the fabricated devices looked at individual cells to determine their normal operation. The comparison of the confined and layered Crosspoint structures was also investigated. This is important to determine if the increase in fabrication complexity, through the use of an isolation layer surrounding the SiC dielectric layer, benefits the overall operation of the device.

6.2.1 Single Device Characterisation

The sputtered SiC devices had a much higher resistive ratio than the devices fabricated using the high-temperature PECVD process. The ratio of the layered devices shown in figure 6.8 has a resistive ratio of around 10^6. These devices, however, were incredibly unstable with the majority of devices only being able to switch a few times before breaking down. The highest endurance measured from these devices was 12 DC cycles. Therefore, no meaningful data could be analysed. In contrast, the confined sputtered devices appeared to have a similar resistive ratio with much higher endurance, shown in figure 6.9b which presents the resistance states of 100 DC cycles from a single confined device. It should be noted that for these devices an I_{prog} of 100μA was able to be used instead of 1mA used in the PECVD devices.

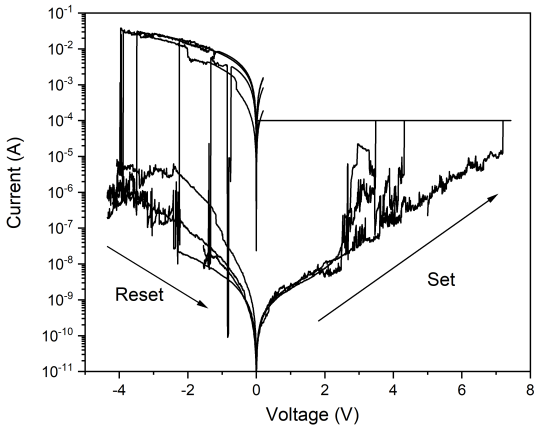
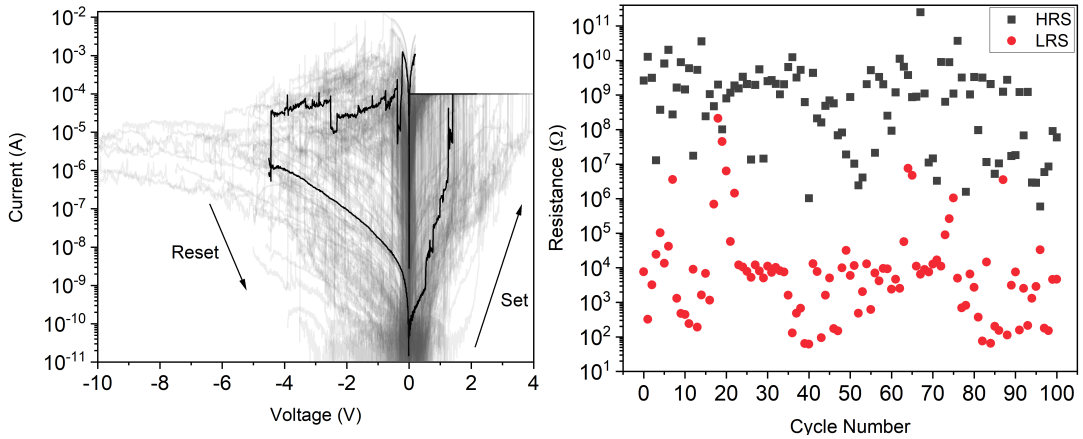


FIGURE 6.8: I-V characteristics of the layered Crosspoint structures with limited endurance.



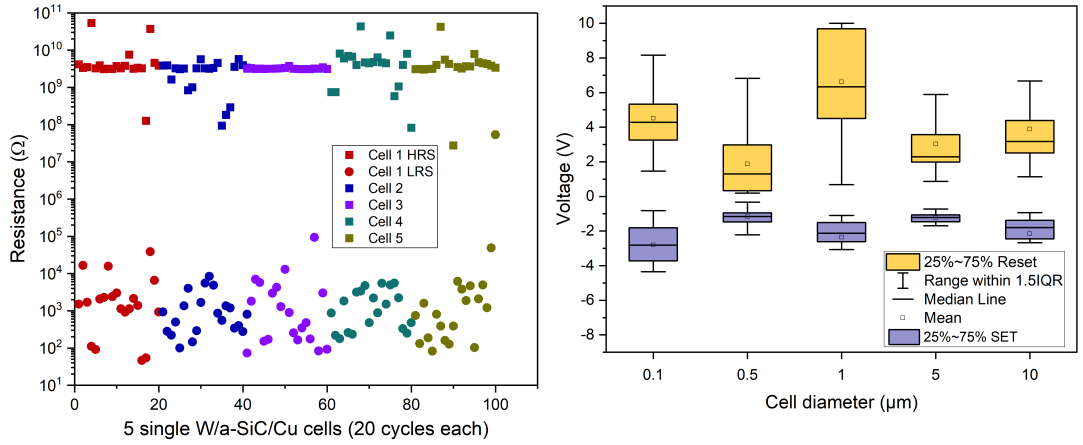
(A) (B)

FIGURE 6.9: (A) 100 I-V cycles using the confined Crosspoint structure. (B) Resistance states of the 100 DC cycles measured.

Unlike the PECVD wafer, the 100 cycles were not typical for the entire wafer. However, every device easily managed to reach over 20 cycles. A comparison of the switching characteristics between the PECVD and the sputtered SiC samples is presented in table 6.3. As well as the 100 cycles measured in a single device, 5 devices that were were cycled 20 times, not including the formation of the device, has been added with their characteristics averaged.

TABLE 6.3: Comparison of the switching characteristics of a single confined device switching 100 times, 5 confined devices switching 20 times and a high temperature PECVD device switching 100 times.

SiC Device	Set (V)	Reset (V)	LRS (Ω)	HRS (MΩ)
Sputtered confined	1.78 ± 1	-2.46 ± 1.6	572 ± 285	15.6 ± 4.7
5 Sputtered confined Averaged	1.72 ± 0.98	-2.65 ± 1.9	351 ± 246	937 ± 248
$600^{o}C$ PECVD	2.14 ± 0.24	-0.8 ± 0.22	177 ± 127	0.158 ± 0.029



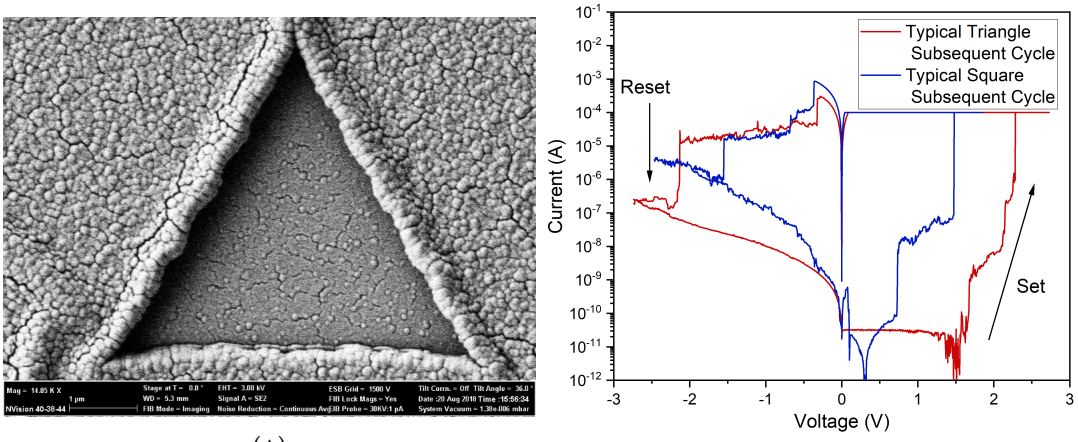
(A) (B)

FIGURE 6.10: (A) Resistance states of 5 single 10x10 μm^2 cells that have been switched 20 times each, after the initial pristine cycle.(B) The variation in the switching voltages with an change in the size from devices with diameters between 0.1 and 10 μm.

The table shows that the Set voltage is lower and the Reset voltage is higher with the sputtered SiC compared to the PECVD devices. The increase in the resistive ratio of the sputtered devices also appears to be due to the increase in resistance of the HRS. With this increase in the resistive ratio, however, the overall endurance of the sputtered devices is much smaller than the high-temperature PECVD SiC memory. Along with this, the standard deviation of the Set and Reset voltages is much higher compared to the PECVD samples. This can be emphasised with the maximum Set and Reset voltage of the confined 100 cycle endurance test being -6 and 8.41V. Comparatively the maximum Set and Reset voltage of the 100 cycles using the high-temperature PECVD SiC was -2.7 and 1.5V. Due to this extremely large deviation in the switching voltages pulsing of these devices only yielded a few switching cycles. This is because the required input pulse would have to be extremely long or have a voltage greater than 10V, which could not be carried out on the B1530A. However, as the sputtered SiC devices are just a placeholder to show the sneakpath in arrays, determining their endurance characteristics using pulsing would not be useful for this chapter.

As well as this, the initial formation of the device did not require an increase in the current compliance, as the high-temperature PECVD SiC devices did. It also was shown that the devices with a square confined region had a much lower formation voltage, with an average of -2.36V, compared to a triangular device which had an average formation of -6.32. However, due to the large standard deviation in the subsequent switching characteristics, any further analysis of the switching voltages with a change in the isolation region must be redone using the high-temperature PECVD dielectric

The large variance in the RESET voltage, using a square device, can be seen across different sized cells as shown by figure 6.10b. This data was taken from devices between 0.1 and 10 μm in diameter that was cycled 20 times, not including the pristine



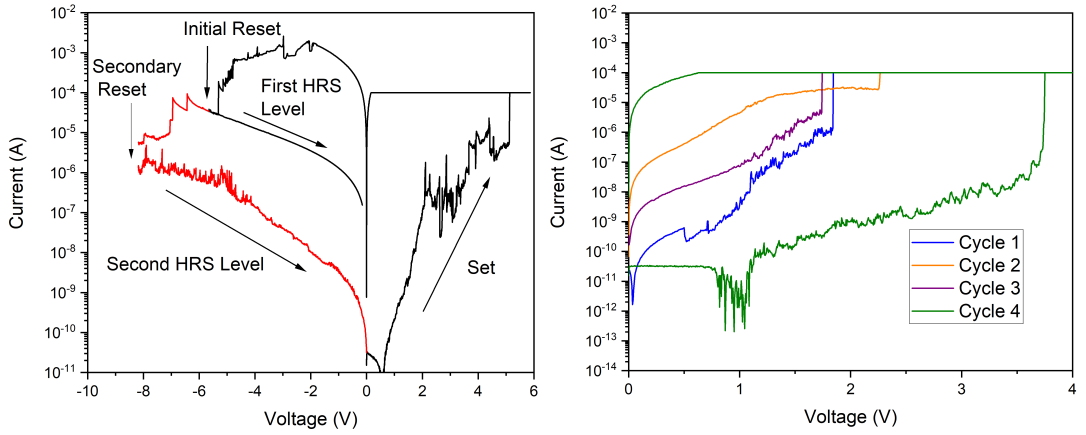
(A) (B)

FIGURE 6.11: (A) Scanning electron micrograph of an confined device with a triangular active region. (B) I-V graph comparing a typical formation from with a square and triangular confined memory cells.

state. A possible explanation of the large voltage outliers could be from the stress between the a-SiC and Cu layer. Figure 6.7 shows defects and cracks on the surface of the Cu electrode which could have been produced due to high thermal strain between the two materials. This is because the coefficient of thermal expansion (CTE) of both Cu and SiC is 17x10^{-6} $^{\circ}C^{-1}$ and 4.1x10^{-6} $^{\circ}C^{-1}$ respectively [190]. A mismatch between the CTE can cause the development of tensile stresses, which can lead to spontaneous cracking [191]. This cracking could then lead to non-uniform electric fields through the dielectric material, causing ion migration to vary through the device. The PECVD fabricated devices do no suffer from these cracked layers, however, it is unclear why, but it could indicate that the electric field that controls the filament is completely uniform, providing a lower deviation in the switching voltages. One possible explanation is that SiC thin films suffer from compressive stress. It has been shown that annealing a-SiC:H thin films can reduce overall stress and when annealed at 600 ^{o}C this stress can reduce to zero [192]. This change in stress has been shown to be caused through the change of the bonds in the lattice. Hydrogenated bonds produce a compressive film and as the annealed temperature is increased, these bond will break and the subsequent Si-C bonds produce a more tensile thin film [193]. therefore increasing the temperature will cause the thin film to move from a compressive to tensile dielectric. Stress can produce many defects and cracking in thin films and so this could be a possible explanation. However, a detailed thin film stress analysis must be investigated to prove this theory.

Whilst comparing the IV characteristics it was noted that that the cells could be switched into the HRS through two different methods. The first way is as previously described, utilising an abrupt change in the state caused by the immediate rupture of the filament. However, the second method utilises the gradual rupture of the filament as a reset voltage bias is applied. This allows multi-state switching to occur in the HRS, 6.12a. This

figure presents four different SET cycles with three distinct HRS, once the cell has been partially or fully ruptured.



(A) (B)

FIGURE 6.12: (A)I-V characteristics of multi-stage switching showing the Multi-stage mechanism based off of the RESET mechanism (B) 4 Set cycles with 3 distinct HRS.

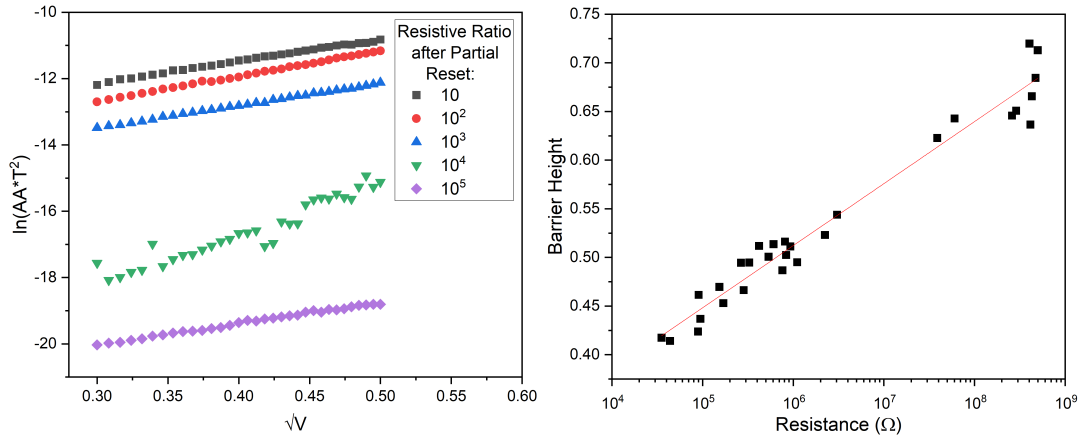
Multi-state switching has been previously reported in silicon carbide resistive cells, which are controlled by changing I_{prog} during the Set operation [18]. Controlling multi-level states through this method requires an increase n the complexity of the peripheral circuitry, compared to controlling the states using RESET voltages.

To analyse the multi-level mechanism it is important to look at how the HRS operates. As previously stated, Schottky emission is the dominant mechanism and is described by equation 6.1.

$$ln(\frac{I}{AA^*T^2}) = \frac{q\sqrt{\frac{q}{4\pi\epsilon_i d}}}{KT}\sqrt{V} - \frac{q\phi_B}{KT} \tag{6.1}$$

The multi-HRS described in this report has been observed similarly in oxide-based memories [15, 17]. It has been suggested that in oxide-based memories, due to the unchanging barrier height, the distance between the filament and electrode could be calculated. This showed that an increase in the reset voltage increases the distance between the filament and electrode. The change in distance between the filament and electrode can be calculated using the gradient of the ln(I/AA^*T^2)-$\sqrt{V}$ graph, while the barrier height can be calculated from the intercept.

When the SiC cells were measured and analysed it was shown that there was a change in both the intercept and the gradient with a change in the HRS, as shown by figure 6.13a. This could be because in the oxide-based memories there is no physical change in the dielectric, whereas, the measured cells contain a Cu conductive bridge. This conductive bridge could act as a form of doping in the dielectric layer, altering the barrier height. Therefore, it could mean that with cation migration based ReRAM, the



(A) (B)

FIGURE 6.13: (A)ln(I/AA*T^2)-$\sqrt{V}$ of 5 different resistive ratios showing Shottky emission is the dominant mechanism in all of the HRS and a change in barrier height with resistance state(B) Barrier height- resistance graph showing a linear trend between the multi-level resistance state of the HRS and the barrier height

amount of rupture of the filament would change the effective doping of the insulating material, causing an change in the barrier height. To show this possibility 30 cycles were measured whilst altering the HRS, to see if there is a trend with the barrier height and the HRS. Due to the slightly random nature of the SET and RESET voltage, the cells were determined to have changed into one of the multi-HRS when a change in the current was observed, over a magnitude of 1. Figure 6.13b presents the HRS using Ln(I/AA^*T^2) at 0.1V against the calculated barrier height, which shows a clear trend.

To calculate the distance between the filament further analysis of the capacitance between each HRS must be taken to calculate the change in the dielectric constant. This is because, currently the data shows that the distance between the electrode and the filament increases with an increase in leakage of the HRS, which is not correct. This could be due to the effective change in doping of the Cu filament causing the dielectric constant to alter, meaning that these calculations are not accurate. Therefore, further investigation is required, which is outside the scope of this work, as the mechanisms of the sputtered SiC devices is not the focus of this project.

Unlike Chapter 5 there was not an investigation in the DC characterisation with respect to device size. This is because these a single layer devices with the a Cu ion conductive filament as its switching mechanism. This means that the HRS is dictated by the change in barrier due to the distance between the filament and bottom electrode and not on the device area. Therefore, there would be no meaningful data that could be presented with this dataset and so is outside the scope of this thesis.

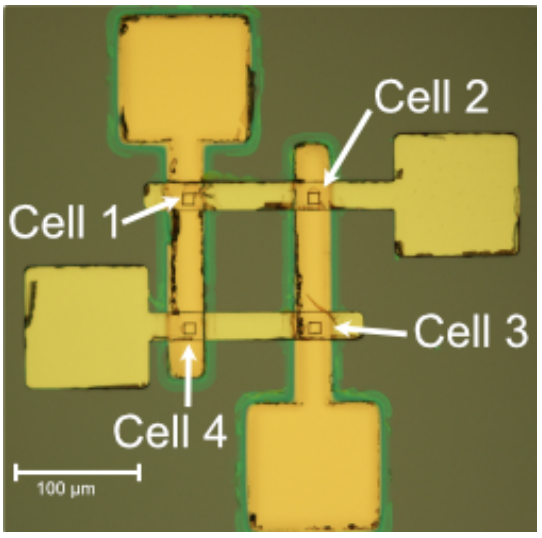


FIGURE 6.14: Optical image of a 2x2 array with each cell labelled, used to identify the effects of sneakpath

6.2.2 Sneak Path Analysis

As with the single cells, the 2x2 arrays showed good reliability in their endurance and so they could be used to test the effects of the sneakpath and their potential for bit errors. This was done by first cycling each device individually to form the initial pristine state and to confirm that they were working as expected. After this, the four cells were cycled to specific states, as shown by table 6.4, by altering one bit at a time and measuring the states of all the devices to see any possible effects that their interactions had on each other. An example of arrangement of these devices is given in figure 6.14, which shows the identification of each individual bit.

TABLE 6.4: Bit states of each device in a 2x2 array that were cycled to look at the effects of sneak path

cell 1	cell 2	cell 3	cell 4
0	0	0	0
1	0	0	0
1	1	0	0
1	1	1	0
1	1	1	1
1	0	1	1
1	0	0	1
0	0	0	1

Each device was read at -0.1V to see if their output matched the bit states. The measured states are shown in figure 6.15. The devices followed the expected values from table 6.4 until the array reached '1110'. At this point, the first order sneak path dominates the array and we record a read bit error. This is because cell 4 appears to be in the ON state when it should be in the OFF state. This device goes back to appearing in the OFF state

once the sneakpath is broken when the array is changed into '1011' state. However, he we see a read bit error with cell 4, as it appears to be in the HRS when it should be in the LRS. This change from LRS to HRS is due to the cell not being able to switch on at the '1111' state, due to the severe parasitic leakages cause by sneakpath. Therefore, we can say that the effects of sneakpath on bit errors affect both the read and write scheme in a 2x2 array.

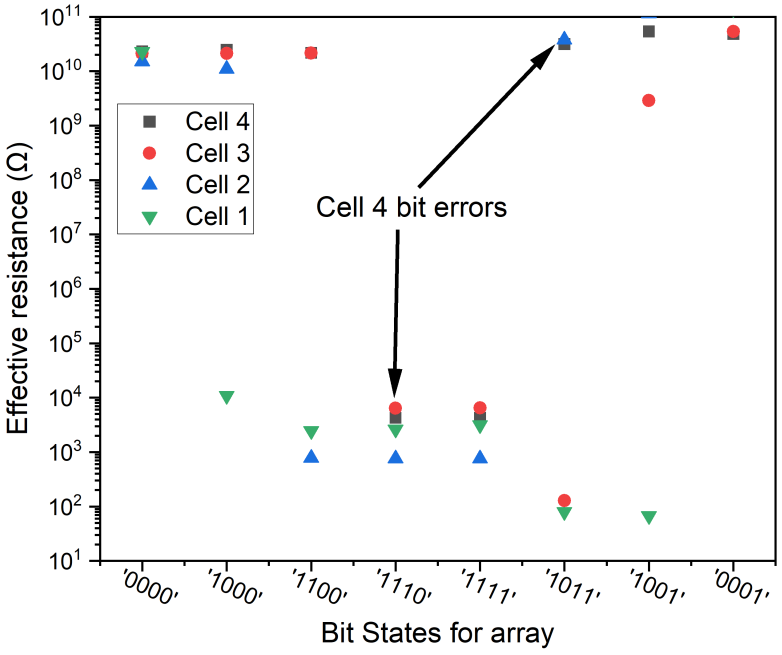


FIGURE 6.15: Measured resistance states of each cells in an array to analyse bit errors. The 4 cells are changed from a configuration of '0000' to '1111' and back to '0000'. Sneakpath is clearly seen and both a read and write bit errors have been found in a simple 2x2 array.

6.3 Conclusion

This Chapter presents the first known resistive memory Crosspoint structure using SiC-based dielectrics, as well as showing how a change in the physical structure of the Crosspoint memory can have an impact on the resistive switching characteristics. Passive sputtered SiC Crosspoint arrays have been designed and fabricated using photolithography and e-beam lithography. The use of e-beam lithography to make confined cells greatly enhanced the cyclability from 12 to over 100 cycles, compared with overlapped arrays. The IV characteristics were measured across two different active region shapes, showing instability using a triangular instead of square confined cell. However, more analysis needs to be conducted to understand why this occurs.

Multi-high resistance states were measured which were controlled through the reset process. The HRS is dominated by Schottky emission and barrier height was shown to alter with a change in multi-level resistance state. The presence of sneakpath was measured with bit errors identified in both read and write schemes in a 2x2 array. This work shows the need for a selector to counteract the possibilities of bit errors for standard logic based resistive memory seen in chapter 5. For the neuromorphic memory in chapter 4, the asymmetry between the forward and reverse current is an automatic protection against sneakpath.

Chapter 7

Conclusion and Future Work

7.1 Conclusion

Single and bilayer resistive memory (RRAM) based on a SiC dielectric have been investigated. These dielectrics were deposited using plasma enhanced chemical vapour deposition at a high temperature and the material properties were characterised using EDX and XPS mapping. The bilayer dielectrics were also analysed using XRD and Raman spectroscopy. The analysis of these materials showed that the SiC layers are Si rich with an average atomic ratio of 7:3 Si-C.

The single SiC dielectric memory cells exhibited an asymmetrical I-V characteristic, did not require a formation process, and have compliance free switching. The average resistive ratio measured was around 10^2. However, this ratio initially started with a ratio of 10^3 and during 100 DC cycles there was an observed drift in the LRS from $0.25M\Omega$ to $1.7M\Omega$. Both the LRS and HRS were dominated by Schottky emission and multi-resistance states were achieved. As the resistance of the device reduced, so did the barrier height. The control of the resistance states is thought to due to the ion migration caused by the applied stresses and the any relaxation in the bit state is thought to be dude to the spontaneous diffusion of the conductive filament.

Using a pulsed measurement system these devices were demonstrated to emulate the synapses between neurons, known as neuromorphic computing. The influence of input pulse on the effects of short-term potentiation was investigated by altering a combination of the number of pulses and the applied voltage, allowing the conductance of the memory cell to be tuned between 0.07μS and 0.7μS. By further changing the duration of the pulse train we can control the conductance of the cell up to 40μS. STP decay was analysed through the use of normalised current, which allowed to determine the change in relaxation constant. The time constant was comparable with other resistance switching devices and was maintained under 10s [91]. The decay time of around 60

seconds that was measured has also been shown in oxide based resistive switching devices [180]. This is within the millisecond-minute range seen in real world STP functions, using purely BEOL compatible processes [96, 181, 182]. This shows the potential of these devices as an easily scalable and functional neuromorphic system for embedded devices.

Bilayer memory cells with a structure of W/Si/SiC/Cu exhibited consistent cyclability using DC bias with a 1mA compliance current in the Set process. The cells were able to be switched using both unipolar and bipolar mechanisms, with the latter showing a higher resistive ratio of 10^3, with the former being 10^2. The devices switched On and Off below 4 and -2V respectively. However, these devices did require an initial formation process with a bias and current compliance above 8V and 10mA. This is thought to be due to the initial drift of Cu ions through the SiC and Si layers, with the SiC layer providing a confined space for the rupture and re-formation of the filament. This confined space could be the cause of the enhanced cyclability that was measured using 200μs pulses, which has been shown in other bilayer structures [30, 70]. An endurance of a record 1 billion cycles was measured with zero degradation in the performance. Analysis of the resistance and deviation across these billion cycles showed that the memory cell improved its performance over time. This enhanced endurance outperforms other Cu-based CBRAM cells with have shown up to 100 million cycles, with some degradation after the first 10 million cycles [187, 188]. In comparison the memory cells in this thesis seemed to drift towards a reduced resistance for both resistance states after 200 million cycles, which then levelled to a consistent range. This bilayer structure shows the potential for BEOL compatible resistive switching devices for scalable embedded memory.

In addition, the fabrication and characterisation of RRAM systems connected into Crosspoint structures was also investigated. These devices utilised a sputtered technique to deposit a single SiC thin film. These devices exhibited resistive switching characteristics with a large ratio of around 10^6, which is comparable to most resistive memory using sputtered SiC [5, 18, 60, 61]. A comparison of overlapped and isolated Crosspoint structures revealed that the isolated arrays exhibited greater endurance, showing 100 cycles whereas the overlapped cells switched under 20 times. The presence of sneakpath was also analysed, with bit errors identified in both read and write schemes in a 2x2 array. This work shows the need for a selector to counteract the possibilities of bit errors for standard logic based resistive memory seen in chapter 5. For the neuromorphic memory in chapter 4, the asymmetry between the forward and reverse current is an automatic protection against sneakpath.

Finally, it was planned to investigate the radiation hardness of the resistive switching memory deposited using the PECVD process. A wafer was fabricated using the bilayer technique and the DC characteristics were measured to ensure that the process was reproducible and exhibited similar switching results. The devices were also measured

at high temperature for an initial investigation in extreme environments. It was found that that increasing the temperature cause the HRS of the devices, during cycling, to decrease in resistance. The devices were able to be cycled up to 125^{o}C and above this value the device had to be Set multiple times to retain their bit states. At 175^{o}C the devices could no longer be set, due to spontaneous rupture of the filament. After this, the initial COVID lockdown occurred, making it impossible to measure the radiation hardness of the devices during this time. Once the COVID restrictions had eased, measuring the devices showed that they had degraded. However, the reproducibility of the fabrication process shown in the chapter shows that these experiments could still be continued in the future.

7.2 Future work

The future of this project can be split into three categories. These are presented in the list below and each contain a list of goals that could be achieved.

Characterisation of the change in temperature of plasma enhanced chemical vapour deposition (PECVD). The PECVD tool that was used for this thesis can operate between 100 and 900 ^oC. Therefore, characterising the change in switching performance across these temperatures could provide opportunities to explore further enhancements with the resistive switching devices. Furthermore, the device the emulation of synapse using single layer SiC thin films needs to be further explored and is described below:

- Characterise the effects of altering input stimuli on Long-term potentiation and depression.
- Characterise Hebbian learning mechanisms by comparing the effects of altering the time between a potentiation and depression stimuli.
- Investigate the alteration of the synapse emulation through decreasing the thin film thickness.
- Fabricate synapses in a 1kb Crosspoint Structure and compare sneakpath with these type of devices.

Analysis of selector technology using the bi-layer Si/SiC based dielectrics, for high density Crosspoint structures:

- Fabricate Selector devices using single devices described in chapter 3, for example Vanadium Dioxide (VO_2)

- Characterise the electrical properties of these devices, for example On/Off voltages, ratios and endurance.
- Integrate the selector with the bi-layer memory in a 1kb to make the first SiC based Crosspoint structure.
- Fabricate and compare the efficiencies of a selector based Crosspoint structure with a complimentary based RRAM device.

Characterisation of Radiation Hard Neuromorphic and standard logic RRAM. All the parameters described below should be investigated using the single and bi-layer devices, as well as any selector material that is investigated. This method has been described in depth in Chapter 5 Section 5.5, as the radiation experiments planned for this thesis could not be conducted, due to the COVID-19 lockdown. These experiments are outlined below:

- Characterise the effects of γ radiation above 2MRad.
- Investigation into filament formation on isolated RRAM devices in Crosspoint structures using Single Event Upsets.
- Characterise the alterations in electrical properties from neutron bombardment, and monitor the effects of neutron transmutation doping of silicon on both the HRS and LRS.
- Compare the effects of radiation on the learning and forgetting of neuromorphic devices, including any changes in inherent characteristics such as relaxation time constants.

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