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Back-End-of-Line SiC-Based Memristor for Resistive Memory and Artificial Synapse

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Two-terminal memristor has emerged as one of the most promising neuromorphic artificial electronic devices for their structural resemblance to biological synapses and ability to emulate many synaptic functions. In this work, a memristor based on the back-end-of-line (BEOL) material silicon carbide (SiC) is developed. The thin film memristors demonstrate excellent binary resistive switching with compliance-free and self-rectifying characteristics which are advantageous for the implementation of high-density 3D crossbar memory architectures. The conductance of this SiC-based memristor can be modulated gradually through the application of both DC and AC signals. This behavior is demonstrated to further emulate several vital synaptic functions including paired-pulse facilitation (PPF), post-tetanic potentiation (PTP), short-term potentiation (STP), and spike-rate-dependent plasticity (SRDP). The synaptic function of learning-forgetting-relearning processes is successfully emulated and demonstrated using a 3 × 3 artificial synapse array. This work presents an important advance in SiC-based memristor and its application in both memory and neuromorphic computing.

1. Introduction

The rapid march of information technology towards the big data era demands highly dense information bit storage and fast computing electronics.[1] This has imposed a bottleneck for the conventional Von Neumann computing architecture where the separation of the memory and central processing units has significantly limited the performance. Inspired by human brains where the data processing and storage are unified within the synapses and neurons to realize complex functions such as perception, learning, and memory, several electronic devices that could implement such biological synapse characteristics have been proposed and developed.[2] These include technologies such as ferroelectric memory,[3] phase change memory,[4] flash memory,[5] ionic transistor,[6] and memtransistor.[7] Compared with these technologies, the two-terminal memristor is widely accepted to be the most promising candidate electronic device to mimic the synapse in human brain.[8–12]

Memristor is defined as the 2-terminal resistive switching memory device where the resistance can be switched between high and low states via the application of electrical pulses.[12] The resistive switching of a memristor has been widely suggested to be associated with the repeated formation and rupture of local conductive filaments originating either from an active metal electrode (e.g., Cu, Ag) or inherent vacancies in the electrolyte layer (e.g., oxygen).[8] This unique switching mechanism has led to extensive research for the next generation of non-volatile memory with great potential for high-density integration and extremely low power consumption.[13] However, over the past decade, research has discovered more advanced switching characteristics of the memristor where the resistance can be modulated gradually through the controlling of input electrical pulses.[14] This has stimulated the application of memristor in the paradigm of synaptic electronics and neuromorphic computing.[15] Since then, several key synaptic characteristics such as paired-pulse facilitation (PPF), short-term plasticity (STP), long-term plasticity (LTP) and spike-rate-dependent plasticity (SRDP) have been emulated by the memristor based artificial synapses.[8]

A wide range of materials has since been proposed as the electrolyte medium for the memristor based artificial synapse. Noticeable candidates including chalcogenides,[16–18] metal oxides,[19–21] and perovskite materials.[22,23] Amorphous Silicon carbide (SiC) is a promising material for future CMOS interconnection dielectric and Cu diffusion barrier and has been regarded as the typical interconnection dielectric material in third-generation semiconductors due to its superior electrical properties such as large band-gap, high breakdown voltage, and good thermal conductivity.[24–26] Several investigations have been conducted into the resistive binary resistive switching behavior of SiC-based memory.[27–29] Our group has previously

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demonstrated SiC-based memory with ultra-high ON/OFF ratio up to 10^9,[30] co-existence of bipolar and unipolar modes, as well as high stability.[28] However, the multilevel switching for SiC-based memristor and its application in artificial synaptic electronics is rarely reported. One exception is the work presented by Yan et al. in which the characteristics of an artificial nociceptor is emulated by a memristor with the structure of Ag/SiC/Pt.[31] However, the SiC film reported there was deposited via a sputtering process while the chemical vapor deposition (CVD) process are normally required in the BEOL process to allow excellent wafer-scale uniformity.[32]

In this work, we present a two-terminal SiC-based memristor with a Cu/SiC/W stacking device structure developed from a CVD process. The memristor demonstrates excellent binary resistive switching with compliance-free and self-rectifying characteristics which are advantageous for its application in non-volatile memory. In addition, the resistance state of the memristor can be modulated gradually by varying the input DC and AC electrical signals. Several synaptic functions including PPF, STP, SRDP have been successfully emulated. The dynamic process of memorization and forgetting are also mimicked through a 3×3 artificial synaptic device array.

2. Results and Discussion

2.1. SiC Device Structure

Figure 1a displays the schematic of the SiC-based memristors. Top view optical microscope image of the as-fabricated memristor is shown in Figure S1a, Supporting Information. The Cu/SiC/W/Ti/SiO_2/Si stack is confirmed by the transmission electron microscopy (TEM) cross-sectional image as shown in Figure 1b. The Cu top electrode serves as the active metal layer while the W bottom electrode is used as the inert electrode. The Ti film is sputtered as an adhesion layer between the W and SiO_2. The switching electrolyte in this work is the SiC layer sandwiched between the two electrodes. It demonstrates an amorphous nature with a thickness of ≈20 nm clearly visible. The surface roughness was measured to be ≈1 nm by the atomic force microscopy (AFM) measurement (shown in Figure S1b, Supporting Information). To confirm the composition of our CVD grown SiC film, X-ray photoelectron spectroscopy (XPS) was conducted directly on the SiC layer. The depth profile in Figure 1c reveals a Si-rich layer with a Si:C ratio of 70:30 across the entire SiC film. To analyze the chemical structure of the SiC layer, the core-level XPS spectra of Si 2p and C 1s are plotted in Figure 1d. The Si 2p spectrum can be fitted by two sub-peaks at 99.4 eV and 100.3 eV, respectively. The former can be attributed to the metallic Si^0 (Si–Si bonding) while the latter is the characteristic peak for Si–C bonding.[33,34] The C 1s spectrum is characterized by a single peak at 283.0 eV. This suggests our CVD grown SiC layer is a mixture of Si and SiC which leads to the unique switching performance of the memristor.

2.2. DC Switching Behavior

DC I-V measurements were performed on the SiC memristor to investigate its switching properties. The pristine memristor

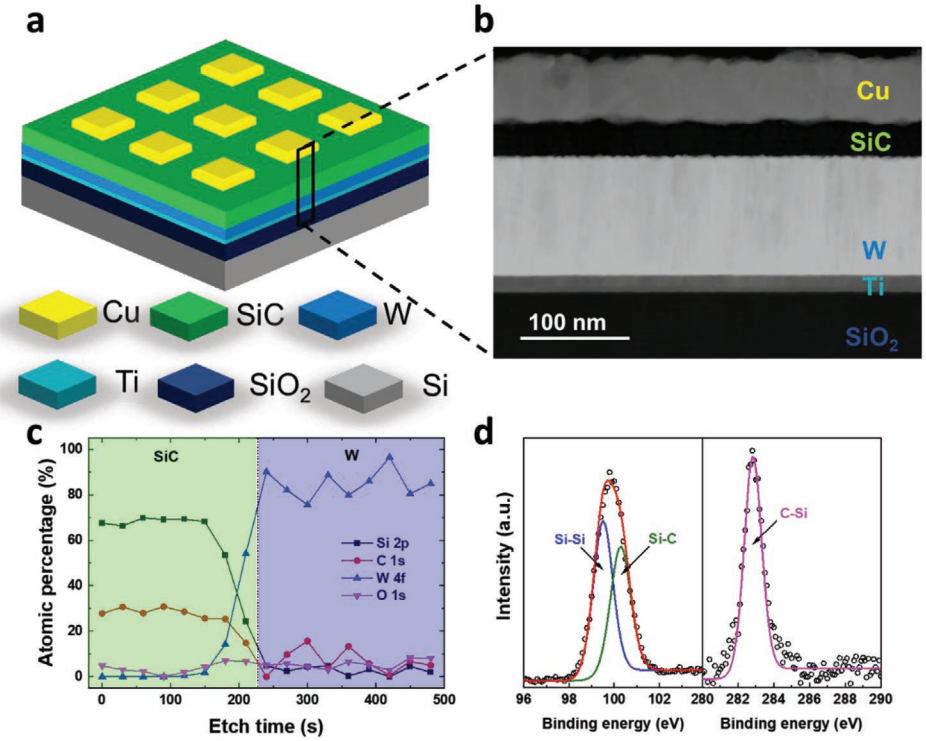

Figure 1. Characterization of the SiC film and Cu/SiC/W memristor. a) Schematic of the Cu/SiC/W memristor structure. b) Cross-sectional TEM image of the memristor. c) XPS depth profile characterization of the SiC film on W electrode. d) XPS core-level spectra of Si2p and C1s of the SiC film.

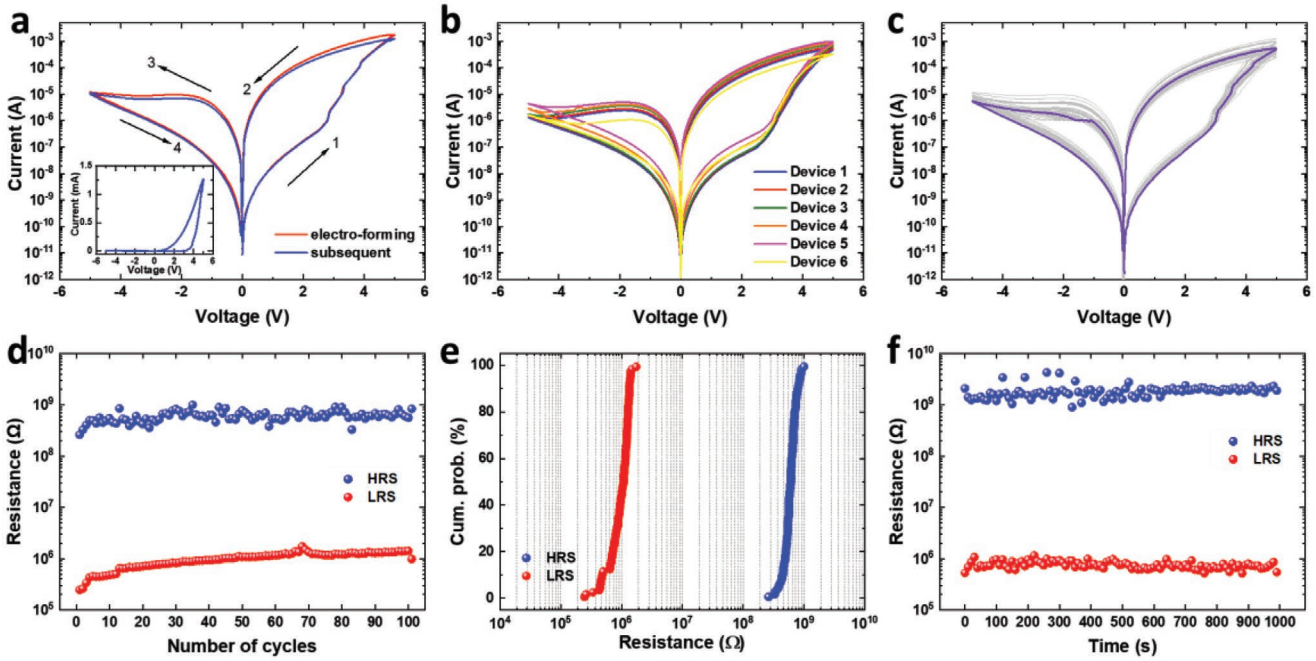

Figure 2. Electrical characterization of the SiC memristor. a) The DC-IV curves of the electro-forming and subsequent switching cycles; inset is the subsequent cycle plotting in linear scale showing a high level of self-rectification. b) Representative DC-IV cycles from six different devices. c) 100 DC-IV cycles of a device. d) DC endurance and e) the resistance states distribution of the device over 100 switching cycles. f) Retention of the SiC memristor.

is initially in a high resistance state (HRS) and can be switched to a low resistance state (LRS) by a positive DC sweep from 0 V to 5 V (shown in **Figure 2**a). A negative DC sweep (0 V to −5 V) is then required to RESET the device back to HRS. This electro-forming cycle (red in Figure 2a) is very similar to the subsequent switching cycle (blue in Figure 2a), indicating an electroforming free behavior. Both SET and RESET steps are characterized by gradual change of the current while no compliance current is required. In addition, the bipolar switching demonstrates current asymmetry where the current under negative bias is significantly suppressed, resembling the typical switching curve of one-diode-one-resistor (1D1R) memory devices (linear plot in Figure 2a inset).[35] The has normally been linked with the Schottky barrier at the electrode/electrolyte interface.[36] For example, self-rectifying behavior was also reported in a Cu/Al_2O_3/a-Si/Ta resistive memory where the non-linearity observed on the device *I–V* characteristic was ascribed to the effective Schottky barrier height at the electrode/aSi interface.[37] The self-rectifying behavior in this work could be attributed to the rectifying property of the Schottky barrier at the SiC/W interface. Figure 2b plots the representative DC switching characteristic of six different SiC memristors fabricated in this work. The high similarity of the switching properties observed suggests the high reproducibility of our device. Continuous cyclic *I–V* measurements were performed on the memristor to investigate the switching repeatability. Figure 2c plots 100 cyclic *I–V* curves which demonstrates good consistency. Over the 100 cycles, the memristor maintains an ON/OFF ratio of over 3 orders of magnitude with a highly uniform distribution of the HRS and LRS as shown in Figure 2d,e. The retention of the devices is plotted in Figure 2f where both HRS and LRS remain stable over 1000 s, confirming the non-volatile behavior under DC sweeps. It is worth mentioning that this ON/OFF ratio is smaller than our previously reported value from memristors based on sputtered stoichiometric SiC film,[38] but is still sufficient for memory applications. The observed modulation of resistance can be understood by the formation and rupture of conductive filament consisting of Cu ions within the SiC device layer. A similar mechanism has been reported previously by our group and others.[28] The current conduction at OFF state is dominated by the Schottky emission as indicated by the linear fitting in Figure S2, Supporting Information. This is consistent with the previously reported SiC resistive memory.[28]

Multiple resistance states are essential for the synaptic devices to build artificial neural networks. By applying a series of positive sweeps (i.e., stimuli) with increasing potential from 3.0 V to 6.0 V, the conductance of the memristor (measured at 0.1 V) demonstrates gradual increment, as shown in **Figure 3**a. This suggests the conductance of filament can be modulated by stimuli with different strengths. It is interesting to notice that the conductance prior to each stimulus is lower than that after the previous stimuli. This implies a spontaneous dissolution of the conductive filaments between the two stimuli. When small DC sweep voltages or short electrical pulses were applied onto the memristor, the Cu filaments formed were likely to be weak and unstable due to the high surface energy and chemical reactivity.[39] Being an active metal, it is reasonable to deduce that Cu can then chemically dissolve into the Si-rich SiC thin film without any treatment.[40] This represents a typical characteristic for STP behavior which will be investigated further in the following section. Figure 3b depicts the change of the memristor conductance under consecutive DC sweeps with the same strength (i.e., 5 V). Similarly, the conductance can

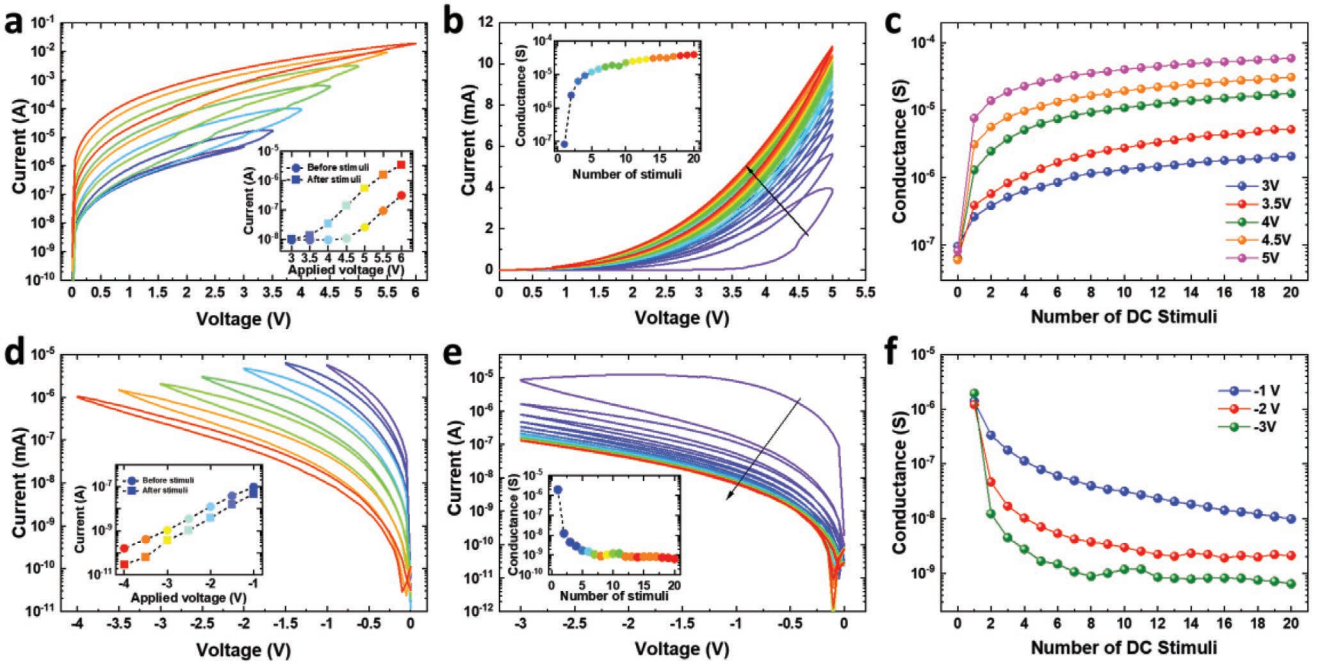

Figure 3. I-V characteristic of the SiC memristor with resistance state modulation via DC stimulation. Current as a function of continuous DC sweep with a) increasing positive voltage and b) constant voltage of 5 V. c) The gradual modulation of the memristor conductance via the different number of DC stimulation and positive voltages; Current as a function of continuous DC sweep with d) increasing negative voltage and e) constant voltage of −3 V. f) The gradual modulation of the memristor conductance via a different number of DC stimulation and negative voltages. Insets show current and conductance at 0.1 V.

be modulated by the number of identical stimulus, indicating a growth of Cu filament in the memristor. The dependence of the memristor conductance on the number stimulus at varying strength is presented in Figure 3c. This clearly suggests neuromorphic behavior of our SiC-based memristor where the multi-state resistance can be precisely controlled by the stimulus properties to realize synaptic plasticity. The gradual decrement of the memristor conductance can also be achieved by supplying a series of negative DC sweeps. After the memristor was set to ON state, a series of negative sweeps were applied (Figure 3d) where the gradual decrement of the conductance can be observed. Similarly, when consecutive identical DC negative sweeps were applied, the conductance can also be modulated gradually (Figure 3e). The magnitude of the decrement can also be modulated by applying different negative biases as shown in Figure 3f.

2.3. Synaptic Performance

A synapse can be considered as a two-terminal device whose synaptic weights can be dynamically modified and stored using voltage spikes as illustrated in **Figure 4**a. When an action voltage pulse arrives at the pre-synaptic terminal, weights in biological synapses are changed by releasing Ca^{2+} ions from the pre-neuron. This leads to the dynamic modulation of synaptic connection intensity which forms the biological basis for brain information processing.[41] This essential biological synaptic plasticity can be emulated by using the two-terminal SiC-based memristor proposed in this work. The memristor conductance can be regarded as the weight of the synapse while an increase or decrease in conductance corresponds to the enhancement or suppression of the synaptic connection. Figure 4b presents the continuous modulation of the synaptic weight of our SiC artificial synapse through a series of 50 positive voltage pulses (5 V). After each repeating pulse, the current was recorded using a read voltage of 0.1 V. The small read voltage was to minimize bias stress effects. The synaptic weight, or equivalently post-synaptic current (PSC), increases sharply under consecutive excitation but attenuates in a short time after the removal of pulses. This response characterizes a typical short-term synaptic plasticity where the intensity of synaptic connection will return to its initial value in hundreds to thousands of milliseconds after the pre-synaptic activity ceases. This short-term plasticity (STP) is thought to be critical in performing computational functions relevant to spatiotemporal information processing in biological neural systems.[2] In biological systems, the strengthening of synaptic connections is attributed to the influx of Ca^{2+} ions into the synaptic cleft. If a subsequent stimulus fires before the recovery of the Ca^{2+}, the update on the synaptic weight can be much larger than that from the first stimulus. Such pre-synaptic spiking interval-dependent behavior is a typical characteristic of STP. To emulate this behavior, we stimulated the memristor using 4 sets of pulse trains which contain pulses with identical amplitude and width (5 V and 50 ms) but different pulse intervals (5, 10, 15, 20, and 30 ms). Figure 4c presents the PSCs after each stimulation where the current increases gradually with increased pulse numbers. More importantly, the increment can be modulated by the stimulation rate, which is altered

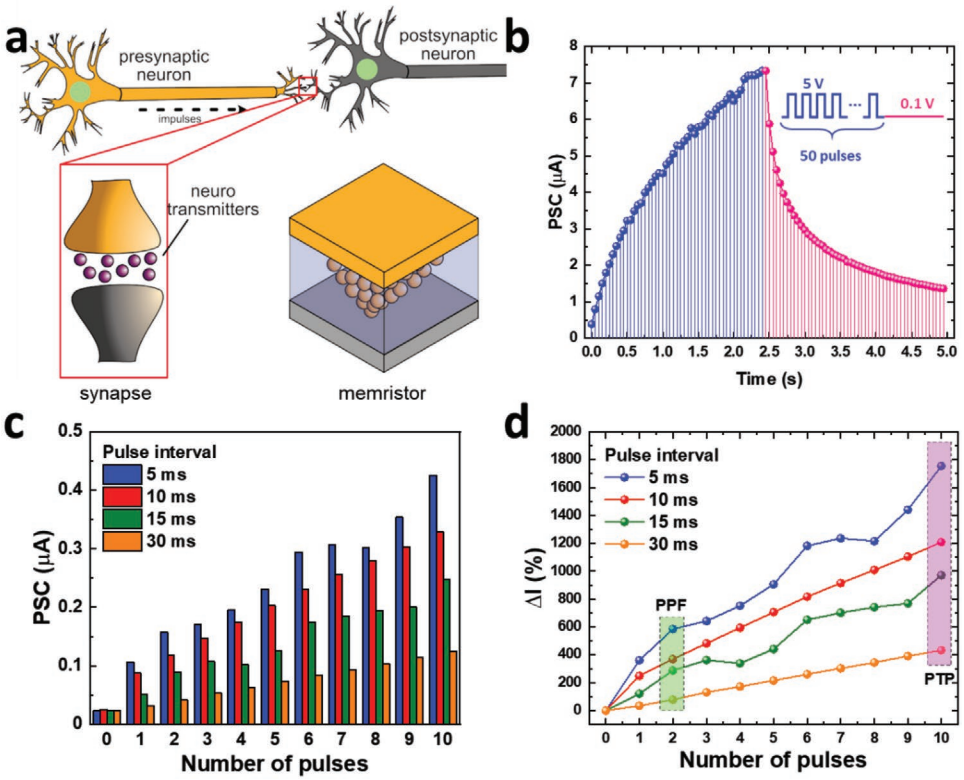

Figure 4. Synaptic behaviors of the SiC based artificial synapse under electric field regulation. a) Schematic representation of a biological neural network and a memristor device showing the correspondence between biological and electronic synapses. b) Gradual PSC change with a series of voltage pulses (+5 V) and the subsequent auto-decay showing the STP behavior. c) Current response of the device for pulses with different inter-spike intervals, emulating SRDP behavior. d) Mean changes in the current during the application of 10 pulses for pulse trains with different pulse intervals. The rectangular boxes indicate PPF and PTP behavior.

by varying the interval between each pulses. A small interval (e.g., 5 ms) leads to a more rapid increase of the PSC, while a large interval (e.g., 30 ms) demonstrates a slow modulation of the synaptic weight. The relative differences in PSC ΔI can be calculated using the equation $\Delta I = [(I_n - I_0)/I_0] \times 100\%$ and are shown in Figure 4d. Both paired-pulse facilitation (PPF) and post-tetanic potentiation (PTP) can be clearly observed to be dependent on the pulse interval. This artificial synaptic behavior is likely due to the balance between the formation and spontaneous dissolution of Cu filaments in the SiC layer under continuous pulse stimulation. This is similar to the releasing and recovery of Ca^{2+} ions in synapses. A large pulse interval leaves a long time for the spontaneous decay of the weak Cu filaments, which results in a smaller current enhancement by the following pulse.

Similar to the performance of biological synapses, the synaptic weight in our artificial memristor synapse can also be modulated by the pulse amplitude, duration, and number. The spike-voltage-dependent plasticity (SVDP) is demonstrated in **Figure 5**a where continuous pulse trains with varying voltages (5 V, 6 V, 7 V, and 8 V) were applied on our memristor. It can be observed that the PSC increases drastically as the spike amplitude increases from 5 V to 8 V. The relative differences in PSC ΔI is plotted in Figure 5b. Larger pulse voltages can trigger more Cu ions into the SiC electrolyte and result in higher device currents. Similarly, extending the duration of the pre-synaptic spike can also amplify the strength of the connection. This spike-duration-dependent plasticity (SDDP) behavior can be observed in Figure 5c,d where SDDP is strengthened with increasing pulse duration. As pulse duration increases, the number of Cu ions injected into the SiC layer is increased, leading to increased PSCs.

In addition to the modulation of synaptic weight, repeated pulse stimulation also enables control of the artificial synapse retention time. As demonstrated in Figure 4b, the SiC-based memristor experiences a spontaneous decay of synaptic weight when the external stimulation is removed. This decay rate is fast in the initial stage but gradually slows down with time. Such behavior is consistent with the "forgetting curve" of human memory in psychology. **Figure 6**a,b plot the spontaneous decay processes after applying a different number of stimulation pulses and the same pulse number but with increasing pulse interval, respectively. Here we adopt a stretched-exponential based function (SEF) to evaluate the relaxation time after each stimulation.[21,42] The memory level is modeled by an exponential equation $M(t) = M_0 e^{[-(t/\tau)^{\beta}]}$. Here $M(t)$ is the memory level at a given time t, M_0 is the memory level at $t = 0$, τ is the characteristic relaxation time, which can be used to evaluate the forgetting rate. β is the stretch index and was fitted to be 0.5 in this work. It can be observed that the modelled relaxation time τ increases from 3.5 s to 12.0 s as the number of stimulations increasing from

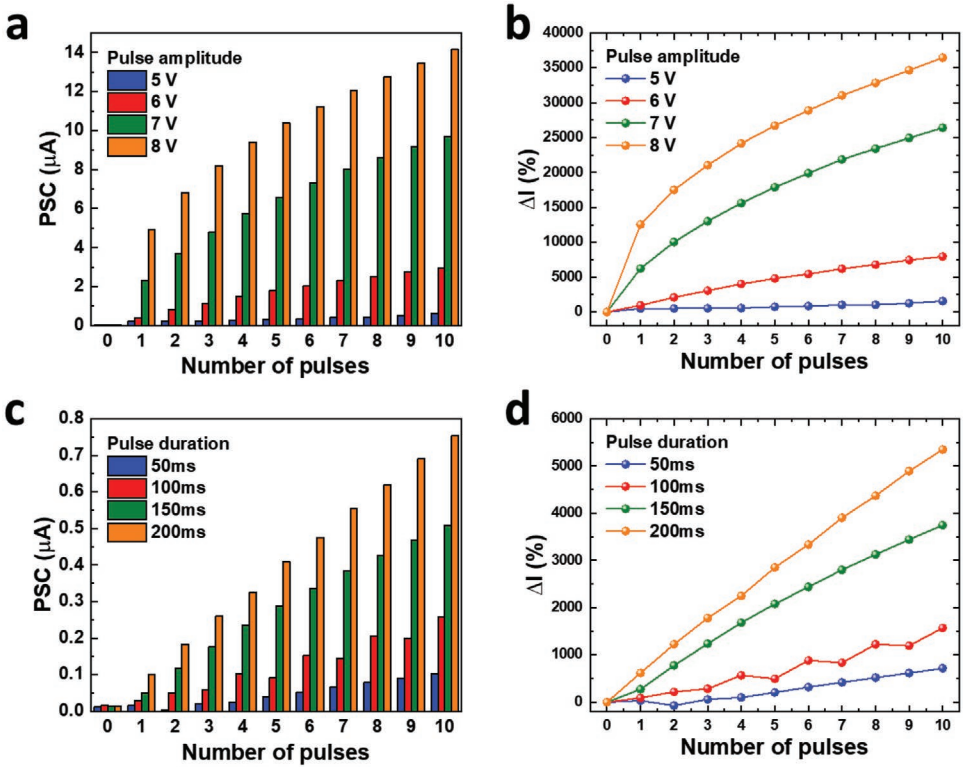

Figure 5. Experimental demonstration of the essential biological synaptic functions for neuromorphic computing. a) Current response of the device for pulses with different pulse amplitude, emulating SVDP behavior. b) Mean changes in the current during the application of 10 pulses for pulse trains with different pulse amplitudes. c) Current response of the device for pulses with different pulse duration, emulating SDDP behavior. d) Mean changes in the current during the application of 10 pulses for pulse trains with different pulse durations.

20 to 100, indicating a decreasing forgetting rate (Figure 6c). On the other hand, Figure 6d shows that the relaxation time decreases with increasing pulse intervals when the same number of pulses are applied. This suggests that forgetting happens sooner if the repetition of stimulation is less frequent, which resembles that of human memory. The impact of pulse amplitude and duration on the forgetting rate is also investigated (shown in Figure S3, Supporting Information).

A more advanced synaptic function in synaptic plasticity is the "learning-forgetting-rehearsal" process. This process is normally described by the Ebbinghaus Forgetting Curve where the memory is reinforced through repetitive learning.[43,44] This behavior is mimicked by our SiC based artificial synapse and is shown in **Figure 7**. Here the learning and rehearsal processes are represented by the application of consecutive electrical pulse trains while the absence of pulse train stands for the forgetting process. Figure 7 presents eight learning and forgetting cycles through turning the pulse trains ON and OFF. Similar to the previous observation, the PSC decays spontaneously after the first sequence of pulse trains, indicating the initially learned information will be partially forgotten over time. However, after repeating the learning process through the application of other sequences of pulse trains, the PSC increases gradually with the number of pulse train sequences, representing that rehearsing the previously memorized information can significantly strengthen the memory capability. At the end of the 8th rehearsal process, the PSC is at a level that is over four times higher than the first learning process.

Memorizing and forgetting simple images are one of the basic functions of the human brain. Based on the "learning-forgetting-rehearsal" process illustrated in this work, the dynamic processes of memorizing and forgetting two images are mimicked through a 3 × 3 synaptic device array. In **Figure 8**a, an image of the shape "□" is learned through one sequence of 10 pulse trains. The resultant memorization level is represented by the PSC of the synaptic device. It can be observed that the shape "□" can only be memorized for a short time as the pattern is fading rapidly after 20 s, indicating that a single learning process is not enough to remember the content of the image. For the shape of "+ " and " × " that are learned by repeating the sequence of 10 pulse trains 4 and 10 times (shown in Figure 8b,c) respectively, the patterns remain clear after 20 s, especially for the case of 10 cycles. This can be ascribed to the over 10 times higher memorization levels achieved after the 10 repeated learning cycles.

The successful emulation of memorizing and forgetting simple images through our SiC-based artificial synapses proves the relatively uniform and stable electrical properties of our devices. **Table 1** lists the recent reports on memristor-based synaptic devices that are made from Si compounds (e.g., SiO_x, SiN_x). Only a small number of memristor devices were deposited using CVD process and only our SiC-based memristor demonstrates both compliance-free and self-rectifying behavior.

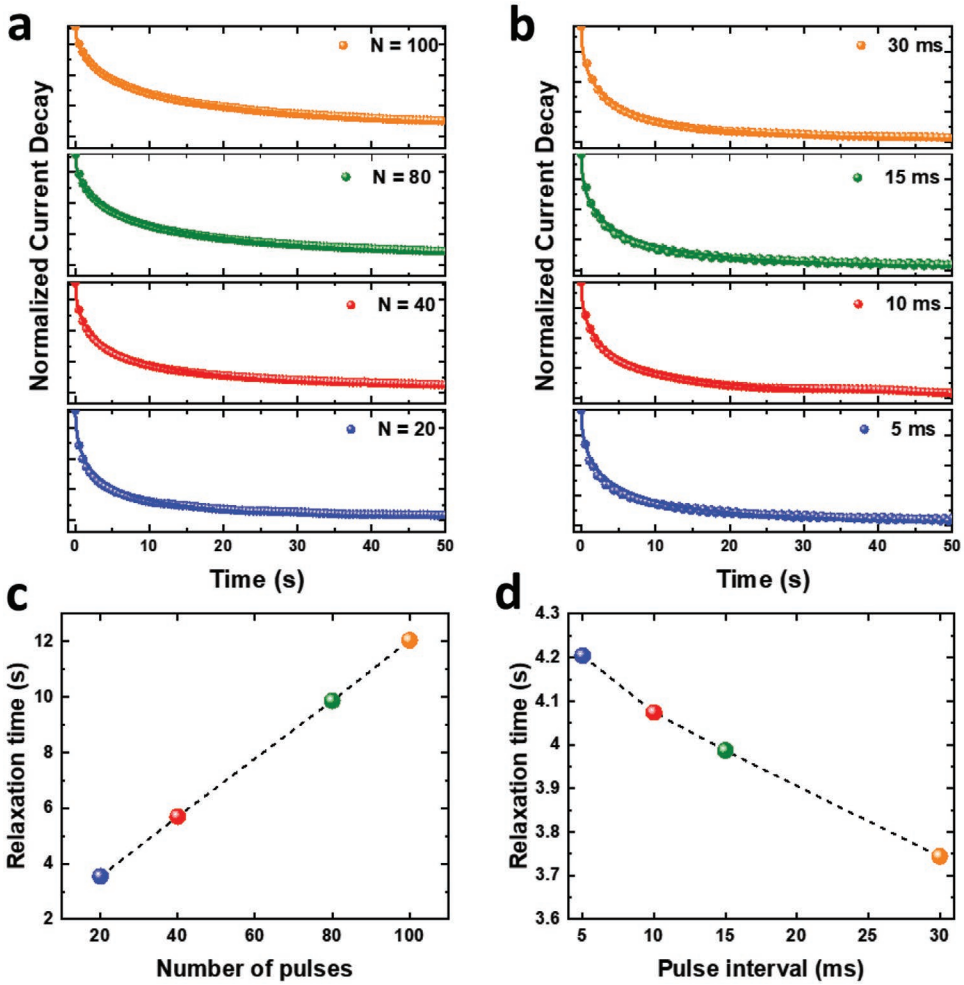

Figure 6. Memory retention data recorded (dots) after a) different numbers of identical stimuli, and b) different pulse intervals with fitted curves using the SEF (solid lines). The data are scaled by a prefactor M_0. Characteristic relaxation time (τ) was obtained as a function of c) the numbers of identical stimuli, and d) pulse interval.

This inherent self-rectifying property will be beneficial when integrating in the 3D crossbar arrays for sneak path suppression.[45] This certainly points towards the capability of our SiC-based memristor to implement more complex neuromorphic functions through advanced and high-density memristor architectures arrays.[46,47]

3. Conclusions

In summary, a memristor based on the back-end-of-line material SiC is developed. The memristor demonstrates excellent bipolar switching behaviors with unique compliance-free, self-rectifying properties that are extremely beneficial for the

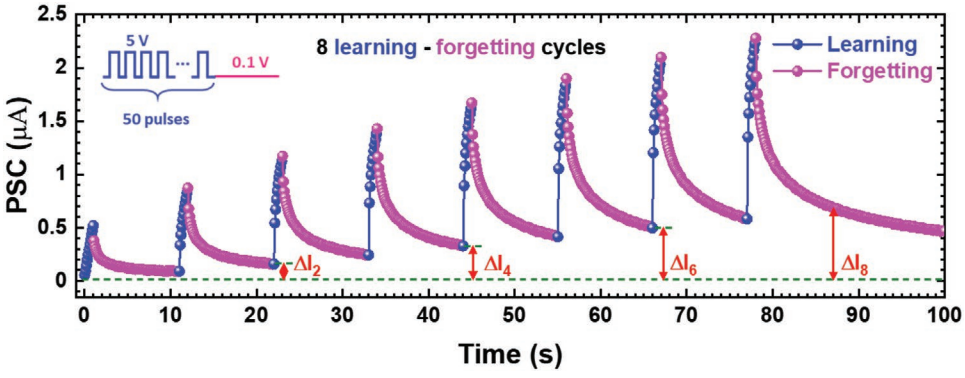

Figure 7. The "learning-forgetting-rehearsal" process of 8 cycles.

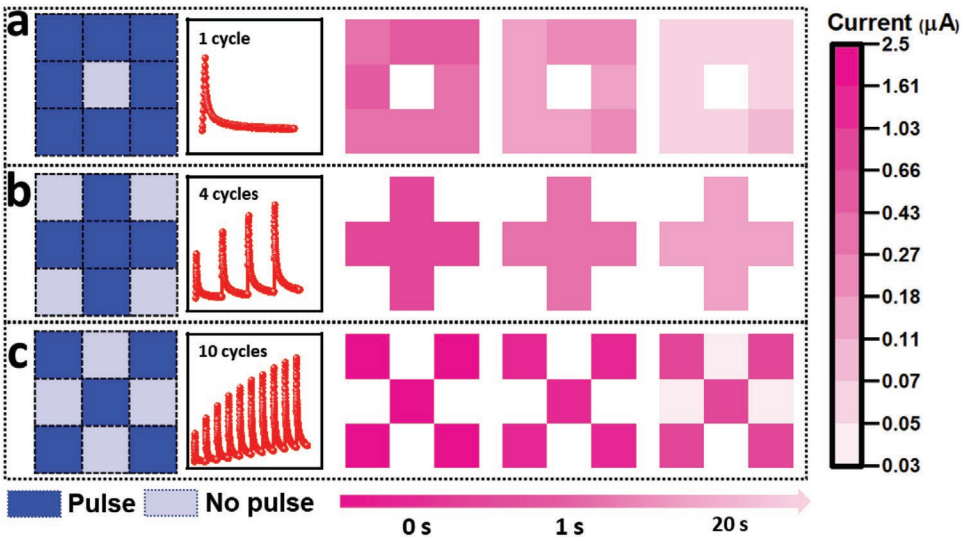

Figure 8. Emulation of "learning-forgetting-rehearsal" memory function in a 3 × 3 array. The current response image mapping of the SiC artificial synapse after a) 1, b) 4, and c) 10 learning and rehearsal cycles at different times.

application as conventional memory application. More importantly, the conductance of our SiC-based memristor can be modulated gradually through the application of both DC and AC bias which are essential for human synapse emulation. Synaptic characteristics including PPF, PTP, STP, SRDP, SDDP, and SVDP have been presented. The synaptic function of learning-forgetting-relearning processes were successfully emulated and demonstrated using a 3 × 3 artificial synapse array. This work presents an important advance in SiC-based memristor and its application in both memory and neuromorphic computing.

4. Experimental Section

Device Fabrication: The Cu/SiC/W memristor was fabricated on a Si/SiO_2 substrate. A 25nm thick Ti adhesion layer was deposited by sputtering. This was followed by the sputtering of a 100 nm thick W bottom electrode. The SiC electrolyte layer was deposited on this W layer via a plasma enhanced chemical vapor deposition (PECVD) process. Silane (SiH_4) and Methane (CH_4) were used as the reactive gas and the flow rates were kept at 15 sccm and 85 sccm, respectively. The deposition time of 70 s was used to achieve the 20 nm thick SiC layer. Finally, a top electrode of the active metal Cu with approximately 100 nm thickness was deposited via evaporation on the SiC thin films and patterned by a photolithography and lift-off process.

Characterization and Measurement: X-ray photoelectron spectroscopy (XPS) data were obtained using a ThermoScientific Theta Probe System with Al–K_α radiation (photon energy = 1486.6 eV). Transmission electron microscopy (TEM) specimens were prepared using conventional mechanical polishing followed by ion milling to electron transparency using Ar^+ at 6 keV. A final low-energy milling step was performed at 500 eV. In order to minimize surface damage, the structure and morphology of the samples were analyzed using a JEOL 2100 TEM equipped with LaB_6 and JEOL ARM200F TEM/scanning TEM (STEM) with a Schottky gun both operating at 200 kV. Atomic force microscopy data was obtained by a Park XE7 system using a non-contact mode.

DC current-voltage curves of this device were characterized by a Keysight BA1500A semiconductor analyzer while the pulse electrical properties were measured by Keysight B1530A waveform generator. During electrical testing, the stimulation signal was applied to the top Cu electrode and the bottom W electrode was grounded.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Table 1. Comparison of recent memristor-based synaptic devices.

Stack	Deposition method	Compliance-free	Self-rectifying	Gradual set	Gradual reset	Pulse scheme	Ref.
$Ag/Ag_2S/SiO_2/ITO$	Stöber solution growth	No	No	No	No	Incremental amplitude	[48]
$TiN/SiO_x/TiN$	Sputtering	No	No	No	No	Identical pulses	[49]
Ag/SiCO:H/Pt	CVD	No	No	No	No	Identical pulses	[50]
$Cu/SiO_2/W$	e-beam evaporation	No	No	Yes	Yes	Identical and Incremental amplitude	[51]
$Cu/SiN/SiO_2/p\text{-}Si$	CVD	No	No	No	no	identical pulses	[52]
$Ni/SiN_x/AlO_y/TiN$	CVD	No	No	Yes	Yes	Identical and Incremental amplitude	[32]
Ag/SiC/Pt	Sputtering	No	No	No	No	Identical and Incremental amplitude	[31]
Cu/SiC/W	CVD	Yes	Yes	Yes	Yes	Identical and Incremental amplitude	This work

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are openly available in University of Southampton repository at https://doi.org/10.5258/SOTON/D2165, reference number 2165.

Keywords

artificial synapses, memristors, neuromorphic computing, silicon carbide

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