NOISE CONSIDERATIONS IN THE DESIGN OF INTEGRATED WIDE BAND AMPLIFIERS

by

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ABSTRACT

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A general discussion on transistor circuit noise is followed by a theoretical noise analysis for the bipolar transistor long tailed pair. The results are then compared with those of the common emitter amplifier. The theory is developed for the more generalised case of differential input and output mode amplifiers. Voltage noise in all modes is shown to be double that of the common emitter, but current noise in the differential input, differential output mode is shown to be half that of the common emitter. The results are verified experimentally under a variety of conditions.

An integrated low noise amplifier suitable for use with an infrared imaging detector of low source impedance is developed. The amplifier has a frequency response of 1Hz-1MHz and uses only two external capacitors. The required noise figure with a source impedance of 50 ohms is to be less than 3dB. The voltage noise which dominates at such low source impedances is shown to be largely dependent on the base spreading resistance (r_x) of the input transistor. A structure for this transistor is developed and the measured value for r_x is 12 ohms, giving a noise figure of less than 3dB.

CONTENTS

INTRODUCTION

This thesis describes an investigation into the noise performance of integrated wide band amplifiers. The initial motivation for the work came from the need to design an integrated amplifier with the following required specifications:

Noise level:	Less than 3dB referred to 300K. Source resistance of any value between 30-50 ohms
Voltage gain:	Minimum of 46dB with provision for external adjustment of gain to 60dB
Input impedance:	Greater than 10K ohm
Output impedance:	Less than 1 ohm
Frequency response:	Flat from DC to 500kHz but with provision to externally boost to 1MHz or cut to lower frequencies
Power supply:	Conventional low voltage power rails with the total power consumption less than 10mW

This amplifier is to be used for video applications with an infrared imaging photodetector of low impedance as the source.

Unfortunately, there are several basic problems associated with the design of low noise amplifiers. The presence

of a low impedance source immediately places a demanding requirement on the noise performance. It is well known that the voltage noise contribution at the input of an amplifier increases for decreasing source impedance. This in turn makes the noise figure larger. The added problems of integration are already well known. Large values of resistance are difficult to integrate and only the smallest of capacitances can be integrated. Moreover, the NPN transistor is the basic building block since the process is centred around the fabrication of this device. The integrated circuit designer is far more restricted than the discrete designer for this reason.

The long tailed pair transistor configuration is a very useful and well accepted building block for the design of most wideband amplifiers. The circuit has many invaluable features such as the facility of both inverting and non-inverting inputs, and low DC drift to make stable operating points possible without the use of capacitors. Unfortunately, the long tailed pair suffers from two major drawbacks when compared with the common emitter stage, namely:

(a) Only half of the voltage gain is obtained, but double the power is consumed.

(b) The noise performance is poorer because the associated voltage noise is approximately doubled and this is very significant for low values of source impedance.

The thesis as a whole may be subdivided into two main parts, both of which are directly relevant to the investigation. These are:

(a) An investigation into the noise properties of the long tailed pair (a widely used input configuration for integrated wide band amplifiers).

(b) A description of the actual design of a low noise amplifier meeting the above specifications. In the design considerations, it is shown that the use of the long tailed pair as input configuration is rejected on the grounds of its higher power consumption and poorer noise performance at low source impedances.

The thesis also contains introductory chapters for the reader unfamiliar with noise. Chapter 1 contains the basic theory of circuit noise, describing the various types of noise, an appropriate model for the bipolar transistor and noise performance of amplifiers in general. Chapter 2 contains information regarding amplifier noise measuring techniques - in particular, a description of the methods used in this project. Their relative merits and accuracy are compared. Chapter 3 then goes on to discuss a theoretical analysis for noise in the long tailed pair and Chapter 4 is a description of the experiments designed to test this theory. Chapter 5 is devoted to the design of the low noise amplifier with the required specifications. The frequency response is evaluated by computer simulation and this theory is then checked against experimental measurements on an equivalent discrete circuit and on the final integrated circuit itself. Finally, the noise figure is measured. Chapter 6 contains a

brief discussion and conclusions drawn on the work carried out.

This research is an extension of part of a study into low noise transistors by B.Soerowirdjo and the reader is referred particularly to his report.

CHAPTER 1

NOISE SOURCES AND MODELS

If the gain of an amplifier is sufficiently large, an output can be observed with no applied input. (We are not referring to the possibility of oscillation due to positive feedback - we assume that the amplifier is inherently stable). The amplifier output under these conditions, when viewed on an oscilloscope with a fast sweep, is seen to consist of a sequence of sharp pulses of random height following directly on one another. This spurious output is called 'noise', and because of the progressive amplification by the successive stages of the amplifier, it clearly comes, in the main, from the first stage. We shall see that it arises both in the circuitry of the amplifier itself and in the resistor at the input of the amplifier. We will begin the discussion by considering the various types of noise associated with transistor circuits.

1.1 THERMAL NOISE

Thermal noise, or Johnson noise (after its first investigator) refers to the noise generated thermally in a resistor. We can think of the random Brownian motion of the electrons as resulting in the appearance of small fluctuating voltages across the resistor. It is obvious that the magnitude of this voltage will increase with increasing temperature. Clearly there can be no steady voltage in any one direction (that is, the average voltage $\overline{v}_n = 0$), but the mean square voltage, $\overline{v_n^2}$, need not be zero...and its value was in fact deduced by Nyquist[1] in 1928. He found that the mean square voltage developed by a resistor in any frequency interval Δf is given

by

$$\overline{v_n^2} = 4kTR.\Delta f \qquad (1)$$

The noisy resistor R can be considered as made up of a noiseless resistor R in series with a simple Thevenin noise voltage source of mean square value as given by equation(1). In terms of an equivalent Norton current source,

$$\overline{i_n^2} = 4kT\Delta f/R \qquad (2)$$

where the noisy resistor can be considered as made up of a noiseless resistor R in parallel with a simple Norton noise current source of mean square value as given by equation(2). In terms of the available power (that is, the power which will be delivered to a load resistor of similar size), this becomes

$$\overline{P_n^2} = kT\Delta f \qquad (3)$$

Equations(1), (2) and (3) are quite general and are not related to any particular type of resistor, nor do they depend on any assumptions about the fundamental nature of electricity. It was convinient to think of thermal noise as due to random motion of electrons, but in fact, the electronic charge q does not appear in the equations. The corpuscular nature of electricity, however, is obviously important in noise theory, and it is mentioned again in the next section.

1.2 SHOT NOISE

Shot noise arises from the fundamental fact that electric charge is quantized into units of magnitude q. It was first investigated by Schottky in connection with the fluctuations in

the anode current of a thermionic valve. He attributed this to the fact that the current consisted of a stream of individual charged particles. The effect is not of course confined to the anode current of a valve, but can occur in valve grid current, transistor collector or base current [2,3].

Specifically, if a PN junction is biased, then, to a first approximation, all of the minority carriers within one diffusion length of the junction will move by diffusion into the space charge region and then be attracted across it by the electric field. These carriers create a fluctuating current because each carrier has a discrete amount of charge. The current will vary with time around a statistical mean giving rise to a series of pulses superimposed upon the background DC value of the current. The Shot noise current across the junction is given by the Schottky formula:

$$\overline{i_n^2} = 2qI\Delta f \qquad (4)$$

where I is the DC value of the current through the junction. A noisy PN junction can thus be represented as a noiseless one with a noise current generator of value given by equation(4) connected across it in parallel. As was the case for thermal noise, the spectrum of shot noise is independent of frequency (ie. 'white' spectrum).

1.3 MODULATION OR 1/f NOISE

Thermal and shot noise are both referred to as 'white' noise because they extend uniformly over the frequency spectrum. In transistors, another noise source is usually present, with a frequency dependence varying approximately as 1/f. It arises from different physical mechanisms, none of which are well understood, but is thought to be mainly due to crystal imperfections

and surface effects. We can consider it as transformed into an equivalent noise source at the input (gate or base as the case might be) and write it as

$$\overline{v_n^2} = A.\Delta f/f \qquad (5)$$

where A is some constant depending on the type of transistor used, and its operating conditions. Although there is still no good explanation in general for this type of noise, it can be concluded that

(a) The surface state density is the unique parameter that determines the 1/f noise and the only way to lower the 1/f noise significantly is to decrease the surface state density in the region of the Fermi level[4,5].

(b) The 1/f noise has a dependence on DC current very much like that of shot noise. Hence, high DC operating currents tend to increase the 1/f noise effect[4,6].

For the purpose of analysis, the 1/f noise in bipolar transistors can usually be modelled by a current generator connected across the internal base-emitter junction. The value of this current generator is empirically shown to be

$$\overline{i_n^2} = KI_b(f_c/f)^{\gamma}.\Delta f \qquad (6)$$

where f_c is the break frequency of the noise power, and γ and K are constants dependent upon the transistor and its operating point.

1.4 BURST NOISE

Burst noise, like 1/f noise, is also related to surface effects[7]. It is a bistable fluctuation phenomenon and gets its name from its appearance when monitored by oscilloscope. The

random burst noise pulses are seen to be superimposed upon a shot and thermal background. Burst noise has been studied in PN junctions, transistors and operational amplifiers[6,7,8]. It is always found that although the amplitude of the noise pulses is never higher than a few tenths of a microamp, no lower limit has ever been detected[7]. Thus, without a very good amplifier indeed, it is difficult to detect burst noise pulses. There are still many wide and varied ideas on the subject but most research seems to point to

(a) Burst noise in silicon planar transistors originates at the emitter-base junction[7,9]

(b) High gain transistors have less burst noise due to the fact that there is more gettering in processing and cleaner surface treatment[8].

1.5 A NOISE MODEL FOR THE BIPOLAR TRANSISTOR

A knowledge of the various sources of circuit noise now enables us to construct a reasonable model for predicting the noise behaviour of the bipolar transistor. The hybrid-π linear incremental model[10] can be adapted as a noise model by inserting the noise sources where appropriate. For the purpose of this research, the shot and thermal sources are considered primarily, and 1/f and burst noise mechanisms will be commented upon at the end.

The hybrid-π linear model without the noise sources is shown in figure 1(a). The terms r_x and r_π represent the parasitic base spreading resistance and the input resistance respectively. C_π and C_μ represent the base-emitter capacitance and the base-collector feedback capacitance respectively. r_{cs} and r_o represent the collector-series resistance and the

output resistance respectively. The current generator $g_m V$ represents linear transistor action in the active region. The model as it stands can be simplified appreciably before the noise sources are inserted. To a very good approximation, r_{cs} can be considered a short circuit and r_o an open circuit for a reasonable transistor. Furthermore, C_π and C_μ can be considered as open circuits for midband frequency operation. Typically, these capacitances will begin to affect the performance at about 1MHz[11]. It is also fair to say that 1/f noise does not appreciably alter the noise performance above 1kHz[4]. This means that 'midband operation' allows the model to be valid for a large range of frequencies.

The relevant noise sources may now be inserted into the model where appropriate. These sources may be listed as

(a) Thermal noise generated by the base spreading resistance r_x. This may be represented by a voltage generator of magnitude $\overline{v_{nx}^2} = 4kTr_x\Delta f$ (7)

(b) Shot noise generated by the base current I_b. This may be represented by a current generator of magnitude

$$\overline{i_{nb}^2} = 2qI_b\Delta f \quad (8)$$

(c) Shot noise generated by the collector current I_c. This may be represented by a current generator of magnitude

$$\overline{i_{nc}^2} = 2qI_c\Delta f \quad (9)$$

The full noise model is shown in figure 1(b). This model will be the basis for evaluation of the noise performance of networks in the remainder of this thesis.

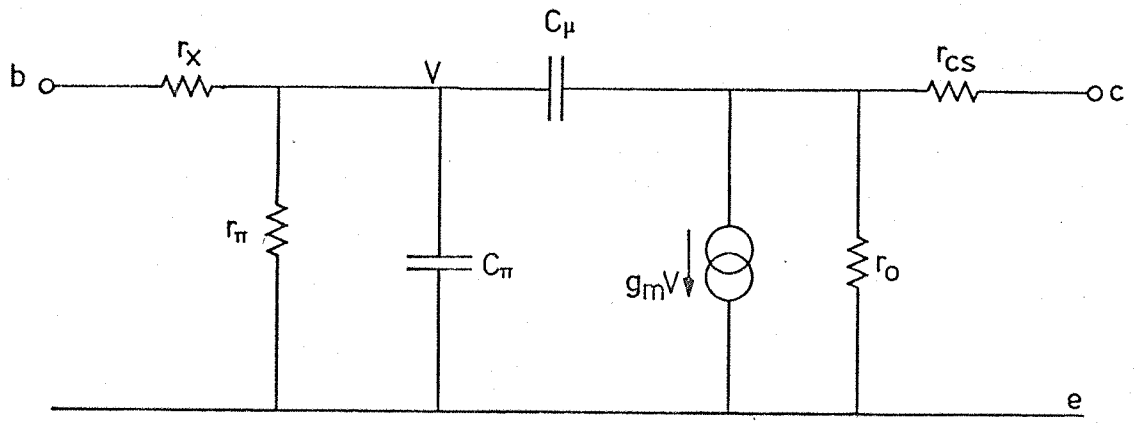


figure 1(a). Full hybrid- π model of bipolar transistor

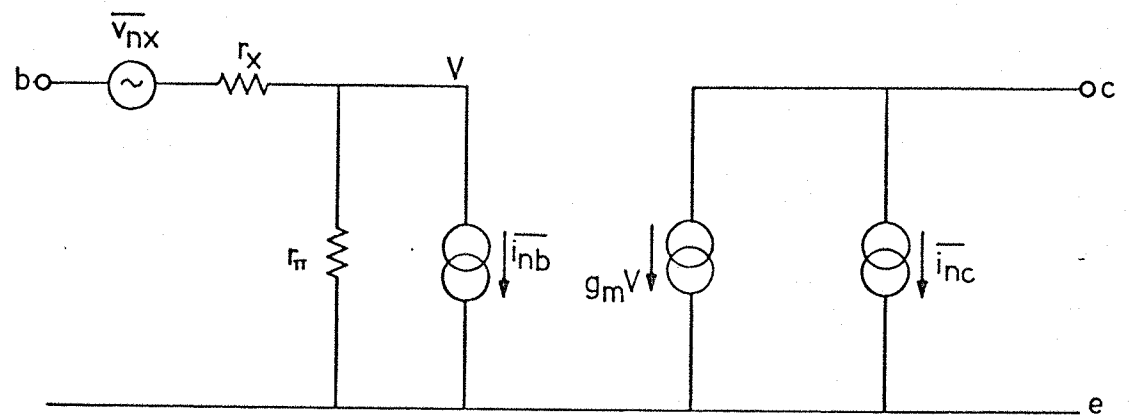


figure 1(b). Linear model including appropriate noise sources

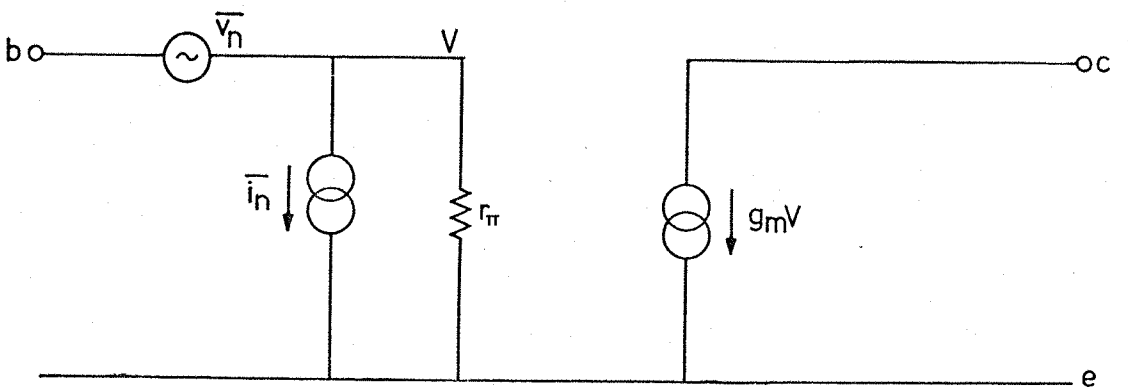


figure 1(c). Representation in terms of equivalent noise generators

1.6 REPRESENTATION OF THE NOISE MODEL IN TERMS OF EQUIVALENT NOISE GENERATORS

In the most general case, a bipolar transistor may be represented by a simple voltage controlled current source with equivalent noise voltage and noise current generators referred to the input[12]. This is shown in figure 1(c). When the input is short-circuited, the noise within the amplifier is due to $\overline{v_n}$ alone. Conversely, when the input is open circuited, the noise is due to $\overline{i_n}$ alone. In practice, with a finite value of source impedance, the noise contributed by the amplifier itself will contain components from both $\overline{v_n}$ and $\overline{i_n}$. By respectively shorting and opening the input of the noise model described in 1.5, it is straightforward to obtain $\overline{v_n}$ and $\overline{i_n}$ in terms of $\overline{v_{nx}}$, $\overline{i_{nb}}$ and $\overline{i_{nc}}$. We find that

$$\overline{v_n^2} = \frac{r_\pi^2\,\overline{v_{nx}^2}}{(r_\pi + r_x)^2} + \frac{r_\pi^2\, r_x^2\,\overline{i_{nb}^2}}{(r_\pi + r_x)^2} + \frac{\overline{i_{nc}^2}}{g_m^2} \qquad (10)$$

and that

$$\overline{i_n^2} = \frac{\overline{i_{nc}^2}}{\beta^2} + \overline{i_{nb}^2} \qquad (11)$$

This representation is particularly useful because it allows all of the noise sources within the transistor to be referred to the input in terms of one equivalent voltage generator and one equivalent current generator. We have assumed that no correlation exists between the two generators. In practice, this is a very good approximation for the bipolar transistor. It is important to realise that the model just described is identical to the model described in 1.5; it is purely the method of representation that is different.

1.7 NOISE FIGURE

There are several ways of quantifying the noise performance of amplifying devices. One way is simply to quote values for the equivalent noise generators $\overline{v_n}$ and $\overline{i_n}$ over a specified bandwidth. But perhaps a more meaningful figure of merit is the NOISE FIGURE. For an amplifier, this is defined as

$$F = \frac{\text{SIGNAL TO NOISE POWER RATIO AT SOURCE}}{\text{SIGNAL TO NOISE POWER RATIO AT OUTPUT}} \qquad (12)$$

It is obvious from this definition that $F>1$ always for a real amplifier since the amplifier can only add to the noise. An alternative definition for the noise figure may be obtained by realising that

$$N_{out} = G(N_{source} + N_{amplifier}) \qquad (13)$$

where N_{out}, N_{source} and $N_{amplifier}$ are the noise powers at the output, source and amplifier itself. Substitution of (13) into (12) and a little manipulation yields

$$F = \frac{\text{AMPLIFIER NOISE POWER AT AMPLIFIER OUTPUT}}{\text{SOURCE NOISE POWER AT AMPLIFIER OUTPUT}} \qquad (14)$$

Of course, the second term in this equation tends to zero for the perfectly noiseless amplifier.

The noise figure of the simple common emitter stage can be obtained by direct substitution of the appropriate values of noise contributions for amplifier and for source in (14). If the source is resistive, then it can be thought of as being split into a pure resistance of value R_s in series with a Thevenin equivalent noise generator $\overline{v_{ns}^2}$ of magnitude

$$\overline{v_{ns}^2} = 4kTR_s\Delta f \qquad (15)$$

This generator will manifest itself at the output by producing a noisy voltage (or current) component at the output. Similarly, the other noise generators within the amplifier itself will each separately produce noisy components at the output. Simple nodal analysis of the noise model of the amplifier (shown in figure 2(a) provides the magnitude of these components. The total noise voltage at the output $\overline{v_{no}^2}$ may then be obtained by superposition[13] of the various noise contributions in the form

$$\overline{v_{no}^2} = \overline{v_{n1}^2} + \overline{v_{n2}^2} + \overline{v_{n3}^2} + \cdots \tag{16}$$

The total noise figure of the system is now given by

$$F = 1 + \frac{\sum \text{all contributions of output noise from amplifier sources}}{\text{contribution of output noise from } R_s} \tag{17}$$

For the common emitter amplifier, these contributions, as noisy voltages, are

FROM SOURCE
$$\overline{v_{no}^2} = \left(\frac{-\beta R_L}{r_\pi + r_x + R_s}\right)^2 \overline{v_{ns}^2} \tag{18}$$

FROM BASE SPREADING RESISTANCE
$$\overline{v_{no}^2} = \left(\frac{-\beta R_L}{r_\pi + r_x + R_s}\right)^2 \overline{v_{nx}^2} \tag{19}$$

FROM SHOT NOISE OF BASE
$$\overline{v_{no}^2} = \left(\frac{-\beta R_L (r_x + R_s)}{r_\pi + r_x + R_s}\right)^2 \overline{i_{nb}^2} \tag{20}$$

FROM SHOT NOISE OF COLLECTOR
$$\overline{v_{no}^2} = R_L^2 \overline{i_{nc}^2} \tag{21}$$

It follows that the noise figure for the common emitter amplifier is given by substituting (18), (19), (20) and (21) into (17). This yields

$$F = 1 + \frac{\left[\frac{\beta R_L}{r_\pi + r_x + R_s}\right]^2 \overline{v_{nx}}^2 + \left[\frac{\beta R_L (r_x + R_s)}{r_\pi + r_x + R_s}\right]^2 \overline{i_{nb}}^2 + R_L^2 \overline{i_{nc}}^2}{\left[\frac{\beta R_L}{r_\pi + r_x + R_s}\right]^2 \overline{v_{ns}}^2} \qquad (22)$$

where the values for $\overline{v_{nx}}^2, \overline{i_{nb}}^2, \overline{i_{nc}}^2$ and $\overline{v_{ns}}^2$ are given by equations (7), (8), (9) and (15) respectively. Substitution for these values and simplification leads to

$$F = 1 + \frac{r_x}{R_s} + \frac{1}{2 g_m R_s} + \frac{g_m R_s}{2\beta} \qquad (23)$$

Only the dominant terms are shown in this equation and it is assumed that $r_\pi \gg r_x$. This of course, would not be valid for high current operation, when r_π^{-1} can approach r_x^{-1}. It is apparent from (23) that a plot of F against R_s for a certain value of operating current will have a minimum value F_{min} for an optimum source impedance $R_{s_{opt}}$. This is shown in figure 2(b). Simple differentiation shows that

$$R_{s_{opt}} = \frac{1}{g_m}\left[\beta(1 + 2 g_m r_x)\right]^{\frac{1}{2}} \qquad (24)$$

and that

$$F_{min} = 1 + \left[\frac{1 + 2 g_m r_x}{\beta}\right]^{\frac{1}{2}} \qquad (25)$$

Inspection of equation (23) also shows that a minimum value of F may be obtained by fixing R_s and varying g_m (or collector current). The variation here, however, is not so dramatic, because the second term, namely r_x/R_s is the dominant one, and remains constant.

A more informative depiction of the variation of F with respect to R_s can be obtained by plotting log(F-1) against

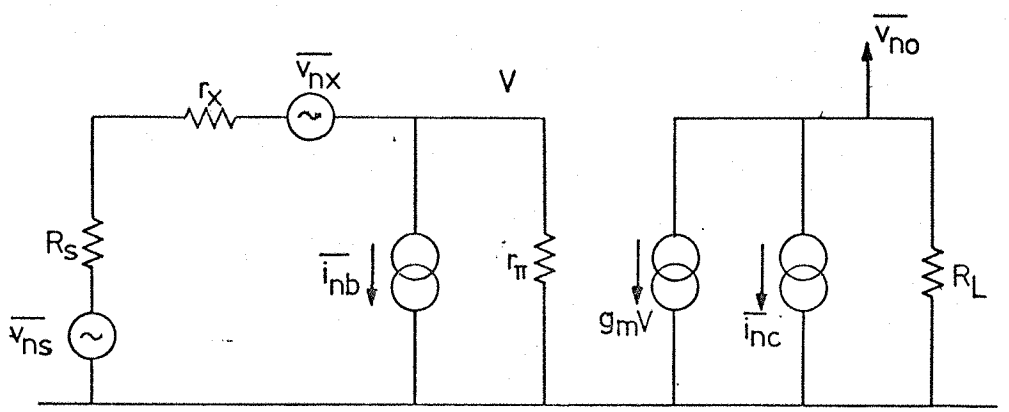


Figure 2(a). Noise equivalent circuit for the common emitter amplifier

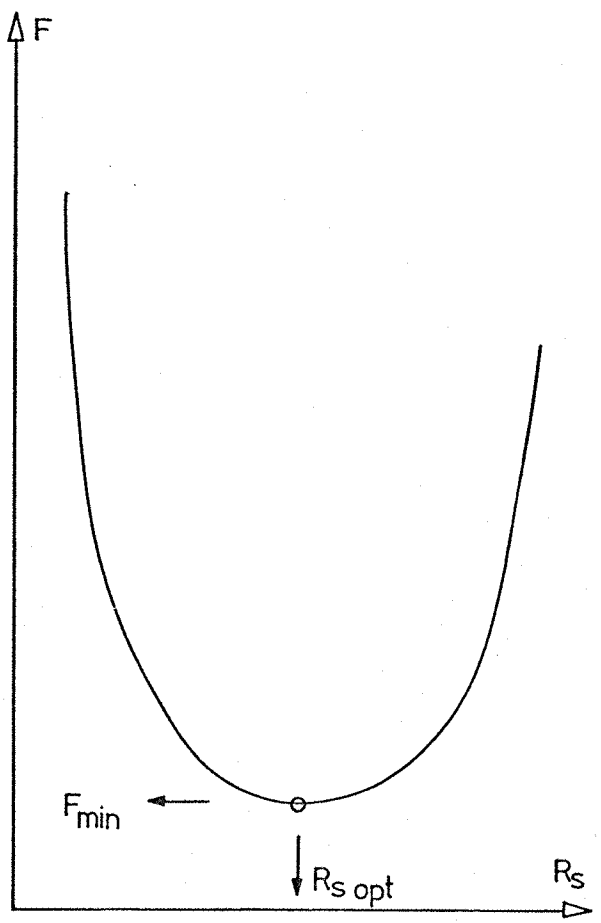


Figure 2(b). Variation of F with R_s for the general amplifier

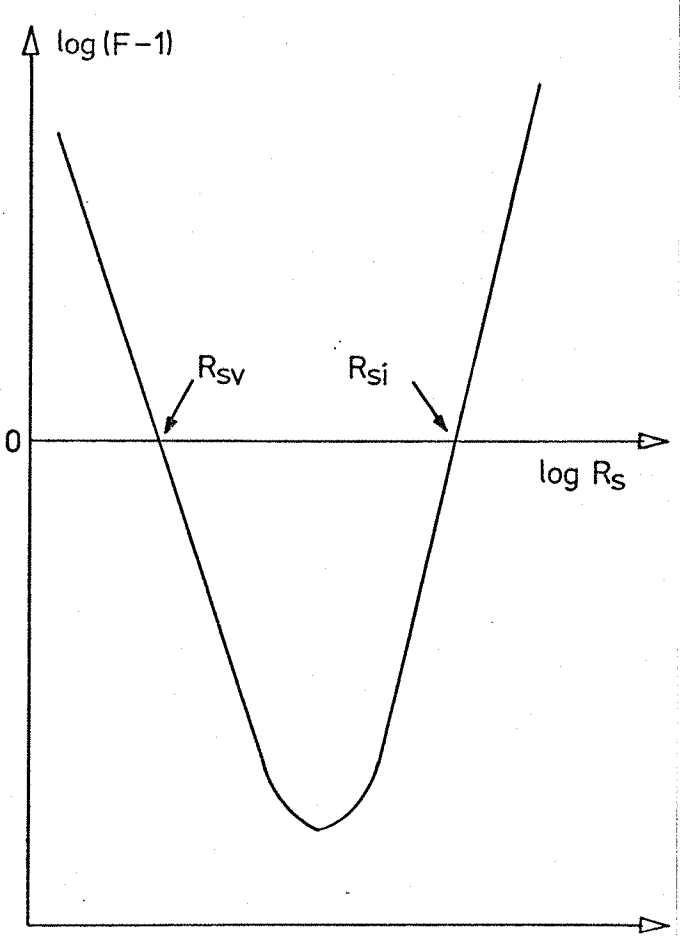


Figure 2(c). A plot of log(F−1) against log R_s

log R_S. This is shown in figure 2(c). The low source impedance asymptote may be assigned purely to voltage noise, and the high source impedance asymptote purely to current noise. Simple evaluation of equation(23) shows that the intersection of this curve with the R_S axis at R_{S_V} and R_{S_i} is given by

$$R_{S_V} = r_x + \frac{1}{2g_m} \tag{26}$$

and

$$R_{S_i} = \frac{2\beta}{g_m} \tag{27}$$

Furthermore, a comparison of the equivalent noise voltage and current generator magnitudes in equations 10) and (11) with equations(26) and (27) shows that

$$\overline{v_n^2} = 4kTR_{S_V}\Delta f \tag{28}$$

and

$$i_n^2 = \frac{4kT\Delta f}{R_{S_i}} \tag{29}$$

It is perhaps interesting to note in passing that the noise bandwidth does not enter the expression for the noise figure provided that the noise is white, and so measurements on F may be made over unspecified bandwidths.

1.8 THE EFFECT OF NEGATIVE FEEDBACK ON NOISE PERFORMANCE

Unfortunately, negative feedback does not have the same beneficial effect on noise performance as it does on bandwidth, stability and input impedance[14]. It can be shown that ideal feedback does not affect noise performance, but that in reality feedback will degrade noise performance because the thermal

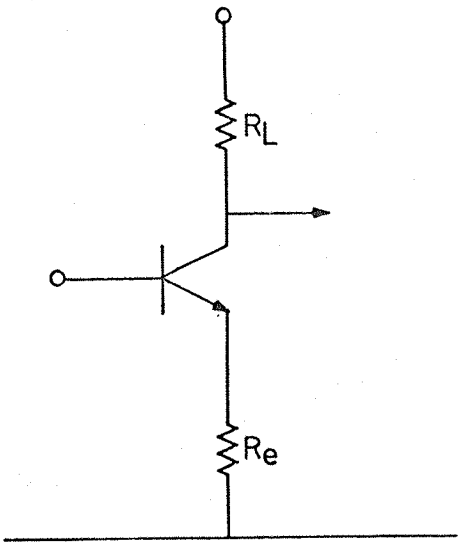


Figure 3(a). Series current feedback

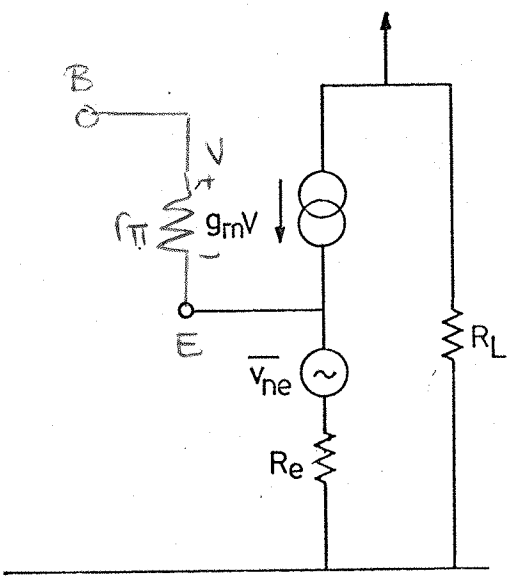


Figure 3(b). Equivalent circuit

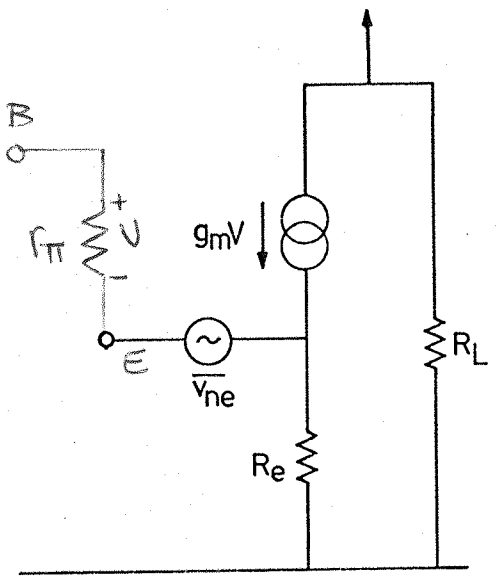


Figure 3(c). Equivalent circuit redrawn

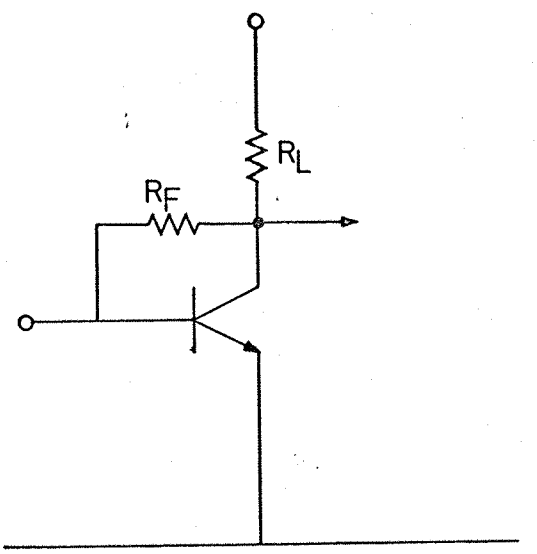


Figure 3(d). Shunt voltage feedback

noise of some extra feedback resistor is also included in the circuit. As a simple example, consider the case of series current feedback as shown in figure 3(a). The feedback resistor, R_e, in the emitter lead, can be split into a noiseless resistor in series with an associated noise generator. The equivalent circuit is shown in figure 3(b). Because the current generator $g_m V$ has infinite impedance, it might just as well be connected to the other side of $\overline{v_{ne}}^2$. This means that $\overline{v_{ne}}^2$ could just as easily have been inserted on the source side of the circuit. This is shown in figure 3(c). Of course, from the noise point of view, this is exactly equivalent to lumping the noise due to R_e with the noise due to r_x. The noise figure of this stage will thus be given by replacing r_x with $r_x + R_e$ in equation(23). The result is

$$F = 1 + \frac{r_x}{R_s} + \frac{R_e}{R_s} + \frac{1}{2g_m R_s} + \frac{g_m R_s}{2\beta}\left\{1 + \frac{r_x + R_e}{R_s}\right\}^2 \quad 30)$$

It is now apparent that by introducing Re, an extra term has been introduced into the equation for the noise figure. For good noise performance, it is essential that $R_e \ll R_s$. A similar argument can be used for the case of shunt voltage feedback using a resistor R_f as shown in figure 3(d). Here, it can be shown that we require $R_f \gg R_s$ for good noise performance.

CHAPTER 2

NOISE MEASUREMENT TECHNIQUES

Since noise voltages are frequently in the nV region, it is virtually impossible to measure noise directly at its source. We cannot put a sensitive voltmeter at the input of the amplifier and hope to measure the noise in that manner. Usually, noise generation is not physically located at the input, but is distributed throughout the system. The total noise is the sum of contributions from all noise generators. In any case, the signal to noise ratio at the output is the main concern, for that is where the meter or display is located. Noise is measured at the output port where the level is highest.

Three general techniques for noise measurement are the sine wave method[14], the noise generator method[13] and the two temperature method. We will briefly discuss each of these in turn, but it should be noted that the sine wave method was not used in this work. It is a very good method for the measurement of low frequency noise but the other two methods are favoured at higher frequencies due to their relative ease.

2.1 THE SINE WAVE METHOD

The sine wave method requires measurement of both output noise $\overline{v_{no}}^2$ and the transfer voltage gain A_v. Then the procedure for measuring equivalent input noise is

(a) Measure the transfer voltage gain A_v

(b) Measure the total output noise $\overline{v_{no}}^2$

(c) Calculate the equivalent input noise $\overline{v_{ni}}^2$ by dividing the output noise by the transfer voltage gain

The amplifier equivalent input noise voltage $\overline{v_n}^2$ and noise current $\overline{i_n}^2$ parameters are then calculated from the equivalent

input noise $\overline{v_{ni}}^2$ for two source resistance values. As previously defined in 1.6, the equivalent input noise is

$$\overline{v_{no}}^2/A_v^2 = \overline{v_{ns}}^2 + \overline{v_n}^2 + \overline{i_n}^2 R_s^2 \qquad (31)$$

if all correlation between $\overline{v_n}^2$ and $\overline{i_n}^2$ is neglected. Measurement gives the total equivalent input noise $\overline{v_{ni}}^2$. To determine each of the three quantities $\overline{v_n}^2$, $\overline{i_n}^2$ and $\overline{v_{ns}}^2$, make the relevant term dominant by choosing either a very low R_s or a very high R_s. Of course, the thermal noise of R_s should be much less than $\overline{v_n}^2$ for the low impedance measurement. It is important to note that the bandwidth of the measurement must be specified using this method. In practice, $\overline{v_n}^2$ and $\overline{i_n}^2$ are always specified in nV per root Hz or pA per root Hz respectively.

2.2 THE NOISE GENERATOR METHOD

This method was used extensively for investigating the noise properties of the long tailed pair. A block diagram of the experimental set-up is shown in figure 4(a). In practice, the measurement of the noise figure is very simple. The impedance of the noise generator is transformed to the required R_s by adding an extra compensating resistor in series or in parallel. For R_s less than the impedance of the generator, the extra R must be added in parallel. Conversely, for R_s greater than the impedance of the generator, the extra R must be added in series. The noise figure is then measured as follows:

(a) Turn down the generator to zero so that all output noise is from amplifier+source thermal Read this value of $\overline{v_{no}}^2$ on the RMS meter.

(b) Turn up the generator until the output noise is doubled. Then read the value of RMS noise being supplied by the generator. This must be exactly equal to the amplifier

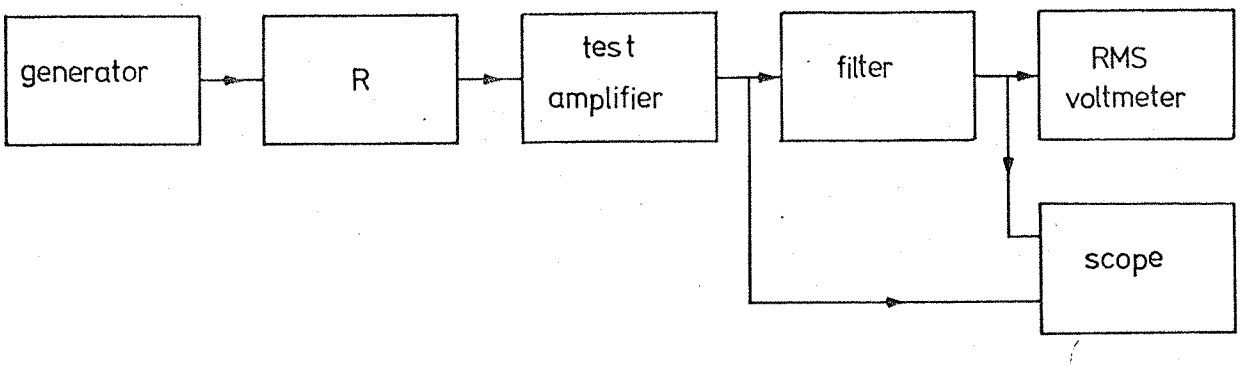
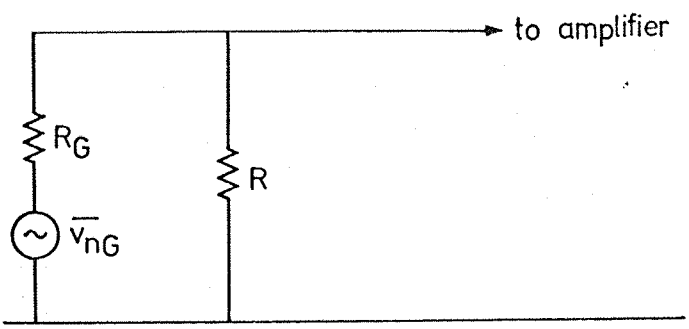
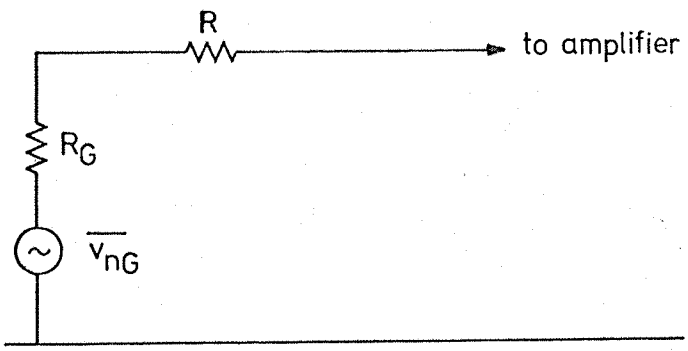


Figure 4(a). Block diagram of noise generator method



$$R_S = \frac{R.R_G}{R+R_G}$$

Figure 4(b). Parallel source combination



$$R_S = R + R_G$$

Figure 4(c). Series source combination

noise + thermal noise of source

(c) Calculate the noise generated by the source. For the parallel combination (low R_s) as shown in figure 4(b), this noise can easily be shown to be

$$\overline{v_{ns}}^2 = 4kT\Delta f. \frac{RR_G}{R+R_G} \tag{32}$$

where R_G is the internal impedance of the generator and R is the external resistor added in parallel to give the required R_s. For the series combination (high R_s) as shown in figure 4(c), the noise is

$$\overline{v_{ns}}^2 = 4kT\Delta f.(R + R_G) \tag{33}$$

(d) Now the output noise is divided by the noise from the source to give the noise figure. If $\overline{v_{no}}^2$ is the output reading on the noise generator, then the output noise for the parallel combination is

$$\overline{v_{no}}^2 \left(\frac{R}{R + R_G}\right)^2$$

and for the series combination is just $\overline{v_{no}}^2$. It follows that for the parallel source set-up, and a specified bandwidth Δf,

$$F = \frac{\overline{v_{no}}^2 \left(\frac{R}{R + R_G}\right)^2}{4kT.RR_G/(R+R_G)} = \frac{\overline{v_{no}}^2 \left(\frac{R}{R + R_G}\right)}{4kTR_G} \tag{34}$$

and for the series source set-up that

$$F = \overline{v_{no}}^2/4kT(R+R_G) \tag{35}$$

For the experiments used in this research, the source resistors

and amplifier were enclosed in earthed metal boxes with interconnecting shielded cable to minimise pickup. In a noise figure measurement, the bandwidth is irrelevant for white noise, but it is important that a flat gain portion of the bandwidth is selected by the filter. The oscilloscope is used to ensure that the filtered noise does not contain any discrete frequency components such as hum, RF pickup or even oscillation.

2.3 THE TWO TEMPERATURE METHOD

In the two temperature method, the output noise is compared for the two cases of identical source resistances, but at two different temperatures T_1 and T_2. In otherwords, this method involves taking two readings only, and simply changing a temperature. It is particularly accurate for low noise figures as we shall see and is an easy measurement to make. In practice, the lower temperature is supplied by liquid nitrogen at 77K and the higher by room temperature at about 294K. A block diagram of this method is shown in figure 5. The noise figure for a particular value of R_s may be obtained as follows. Consider the noise powers at the output for two identical sources at different temperatures. We have

$$N_{out_1} = N_{amp} + G \cdot N_{in_1} \qquad (36)$$

and

$$N_{out_2} = N_{amp} + G \cdot N_{in_2} \qquad (37)$$

Solving these two simultaneous equations gives

$$N_{amp} = G \cdot N_{in_2} \left[\frac{(N_{in_1}/N_{in_2}) - (N_{out_1}/N_{out_2})}{(N_{out_1}/N_{out_2}) - 1} \right] \qquad (38)$$

However,

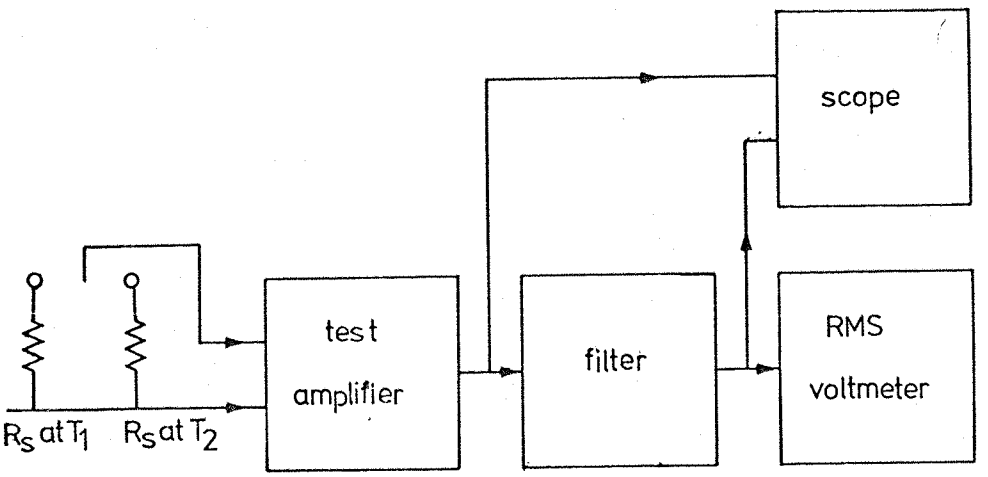


Figure 5. Block diagram of the two temperature method

$$N_{out_1} = \overline{v_{no_1}}^2/R_L \quad , \quad N_{out_2} = \overline{v_{no_2}}^2/R_L \qquad (39), (40)$$

and

$$N_{in_1} = 4kT_1R_s\Delta f \quad , \quad N_{in_2} = 4kT_2R_s\Delta f \qquad (41), (42)$$

If we now let

$$\overline{v_{no_1}}^2/\overline{v_{no_2}}^2 = \zeta \quad \text{and} \quad T_1/T_2 = n \qquad (43), (44)$$

then

$$N_{amp} = \left[\frac{n - \zeta}{\zeta - 1}\right] G \cdot N_{in_2} \qquad (45)$$

But for a real amplifier we recall

$$F = 1 + \left(\frac{N_{amp}}{G \cdot N_{in}}\right) \qquad (14)$$

Substitution of equation(45) into equation(14) now gives

$$F = 1 + \left(\frac{n - \zeta}{\zeta - 1}\right)\frac{N_{in_2}}{N_{in}} \qquad (46)$$

Now if T_1 is chosen at room temperature then $N_{in} = N_{in_1}$ and so

$$F = \left(\frac{\zeta}{\zeta - 1}\right)\left(\frac{n - 1}{n}\right) \qquad (47)$$

2.4 A COMPARISON BETWEEN METHODS

The table on the next page lists the relative advantages and disadvantages of the noise generator method compared with the two temperature method.

NOISE GENERATOR METHOD	
advantages	disadvantages
I. Accurate for high noise figures	1. One end of R_s always to be grounded 2. Innaccurate for low noise figures 3. Reliance on accuracy of generator noise meter

TWO TEMPERATURE METHOD	
advantages	disadvantages
1. No circuit parameters changed in measure-ment 2. Facility of floating source (neither end of R_s needs to be grounded) 3. Accurate for low noise figures 4. Speed of measure-ment	1. Cost of liquid nitrogen 2. Construction of a carefully matched set of resistors for two temperatures 3. Innacurate for high noise figures

A comparison of the expressions for F using either method shows that the generator method is better for high noise figures but worse for low noise figures.

Assuming that the error in reading the meter ϵ_m is 5% and that the tolerance of a given resistor ϵ_r is 5%, it is easy to show for the noise generator method that the percentage error in measuring F, ϵ_F, is 15% for the series combination and 18% for the parallel combination. This is true even for high noise figures since the error in F is independent of F for this method.

In the two temperature method however, it can be shown that the percentage error in F is given by

$$\varepsilon_F = \frac{20}{\frac{F/\left(\frac{n-1}{n}\right)}{F/\left(\frac{n-1}{n} - 1\right)} - 1} \quad \% \qquad (48)$$

and is thus dependent on the value of F. A comparison of the two methods reveals that the two temperature method is more accurate for

$$F < 1.3 \qquad (49)$$

at which point the error in F is in fact 15%.

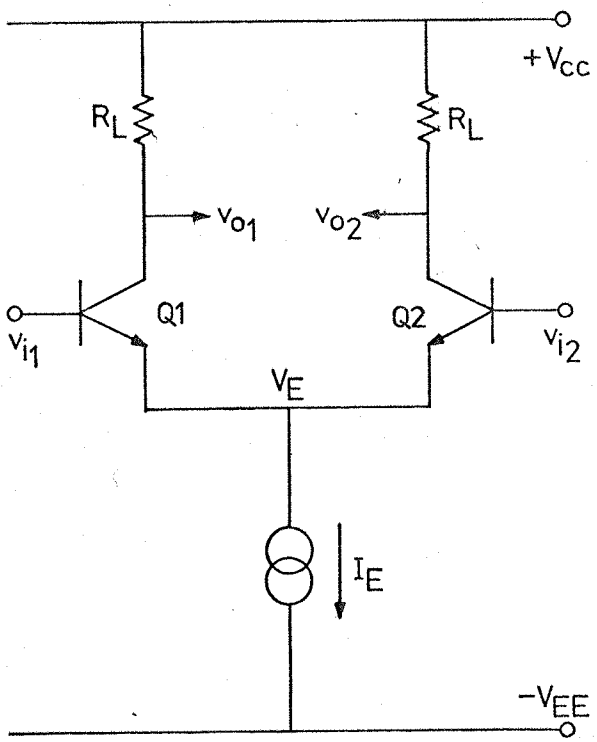
CHAPTER 3

A NOISE ANALYSIS FOR THE LONG TAILED PAIR

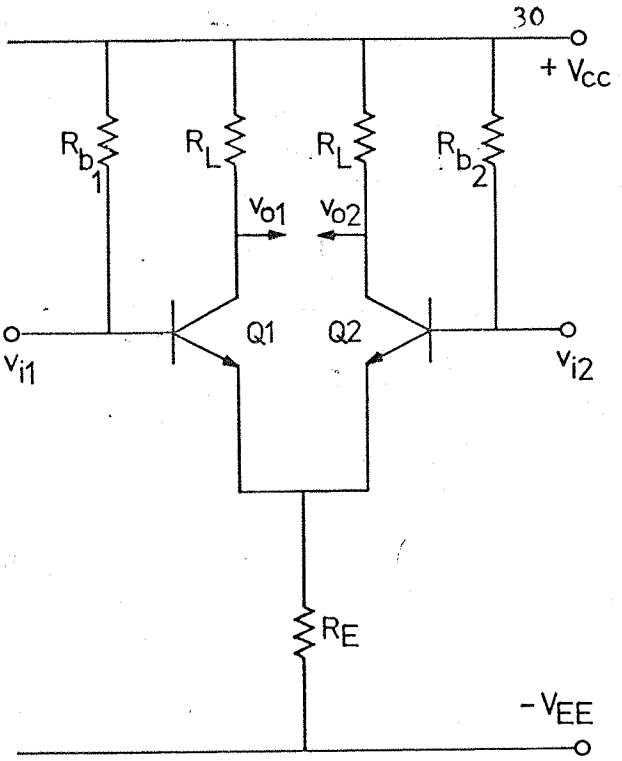
As was mentioned earlier, the long tailed pair is the standard building block for modern monolithic amplifier input design[15,16]. This chapter describes a noise analysis for the basic long tailed pair configuration in order to quantify its noise performance. The noise behaviour of the current source and differential to single sided converter are also considered as accompanying circuit configurations in state-of-the-art operational amplifiers[17,18].

3.1 COMPLETE SMALL SIGNAL NOISE ANALYSIS FOR THE SINGLE SIDED INPUT, SINGLE SIDED OUTPUT DIFFERENTIAL AMPLIFIER

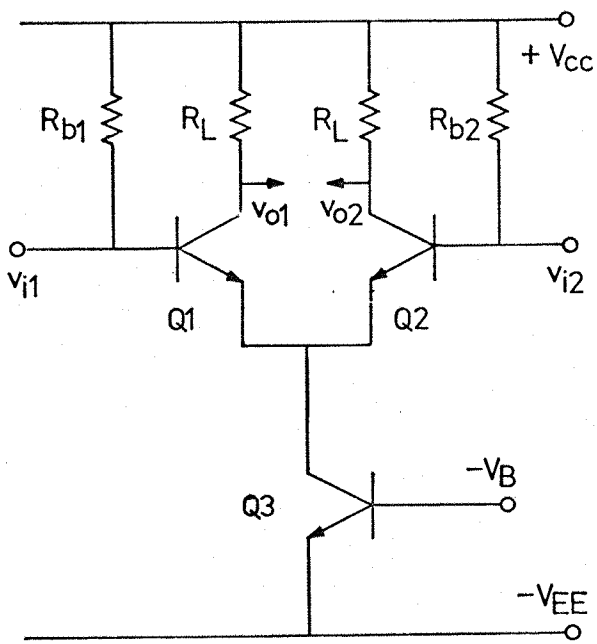
The basic circuit of the long tailed pair when used as a differential amplifier is shown in figure 6(a). In general, input signals v_{i_1} and v_{i_2} are applied to the two transistor bases and output signals v_{o_1} and v_{o_2} are obtained at the respective collectors. Ideally, the pair is supplied with a constant level of DC current, I_E, by a constant current source. If the load resistors and the two devices of the pair (Q1 and Q2) are identical, then the current through each device will be $I_E/2$. Figure 6(b) shows a more practical arrangement for the configuration; I_E is supplied by a large 'tail' resistor of value R_E and the base currents for the two devices are supplied by R_{b_1} and R_{b_2} which are normally quite large. An improved tail arrangement is achieved by using a third transistor, Q3, as the source of tail current. A large voltage drop across R_E is thus avoided, and the output impedance at the collector of Q3 approaches infinity. This is shown in figure 6(c). In modern operational amplifier design, the actual passive load resistors are replaced by



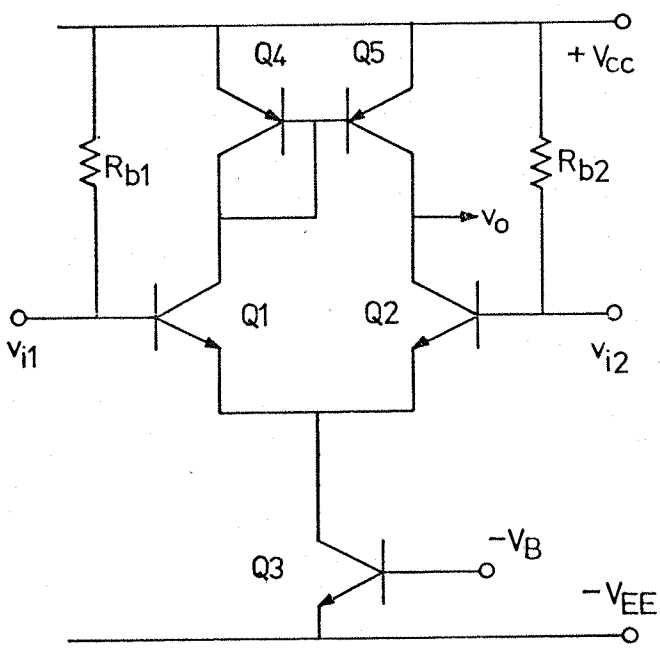
(a) Basic long tailed pair



(b) A practical arrangement



(c) Transistor as current source



(d) Arrangement with active load

Figure 6.

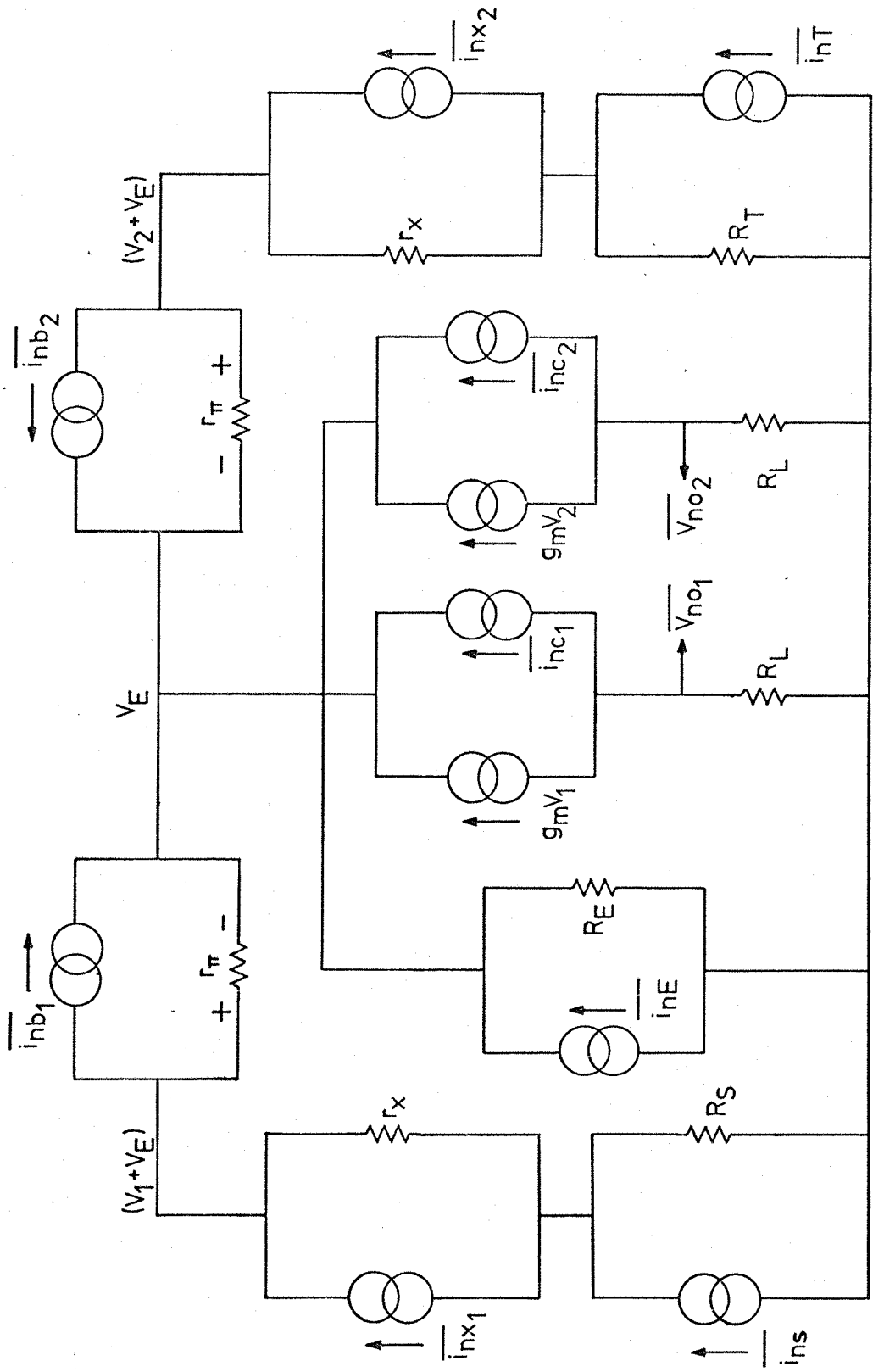


Figure 7. Noise equivalent circuit for the long tailed pair

transistors Q4, Q5 forming an active load arrangement as shown in figure 6(d). In order to simplify the analysis, we will analyse the basic long tailed pair structure shown in figure 6(b), and subsequently consider noisy contributions from the transistor current source and differential to single sided converter.

The noise equivalent circuit is shown in figure 7. A source impedance R_s is connected to the base of Q1. In practice, R_{b_1} can be lumped with R_s, but if $R_{b_1} \gg R_s$, it can be neglected. R_T is a 'balancing' resistor connected to the base of Q2 emphasising the symmetry of the arrangement. Similarly, R_{b_2} can be lumped with R_T. The thermal noise sources have been represented by Norton equivalents. In particular, the tail resistor R_E has an associated noisy current source $\overline{i_{nE}}$. It is worth noting that the small effect of the contribution from the load resistors has been neglected.

The noise contributions at the collector of Q1 from each of the sources in turn is now obtained by nodal analysis as for the common emitter in 1.7. These contributions are listed below.

FROM SOURCE
$$\overline{v_{no_1}}^2 = \frac{\overline{i_{ns}}^2(\beta R_L R_s)^2}{A^2}\left[\frac{1}{r_\pi + r_x + R_T} + \frac{1}{R_E}\right]^2 \qquad (50)$$

FROM r_x IN Q1
$$\overline{v_{no_1}}^2 = \frac{\overline{i_{nx}}^2(\beta R_L r_x)^2}{A^2}\left[\frac{1}{r_\pi + r_x + R_T} + \frac{1}{R_E}\right]^2 \qquad (51)$$

FROM BASE OF Q1
$$\overline{v_{no_1}}^2 = \frac{\overline{i_{nb_1}}^2(\beta R_L)^2}{A^2}\left[1 + \frac{r_x + R_s}{R_E} + \cdots \right.$$
$$\left. \cdots + \frac{(\beta+1)(r_x + R_s)}{r_\pi + r_x + R_T}\right]^2 \qquad (52)$$

FROM COLLECTOR OF Q1

$$\overline{v_{no_1}^2} = \frac{\overline{i_{nc_1}^2}(\beta R_L)^2}{A^2}\left[\frac{1}{\beta} + \frac{r_\pi + r_x + R_s}{\beta R_E} + \cdots \right.$$

$$\left. \cdots + \frac{(\beta+1)(r_\pi + r_x + R_s)}{\beta(r_\pi + r_x + R_T)}\right]^2 \qquad (53)$$

FROM R_T

$$\overline{v_{no_1}^2} = \frac{\overline{i_{nT}^2}(\beta R_L R_T)^2}{A^2}\left[\frac{1}{r_\pi + r_x + R_T}\right]^2 \qquad (54)$$

FROM r_x IN Q2

$$\overline{v_{no_1}^2} = \frac{\overline{i_{nx}^2}(\beta R_L r_x)}{A^2}\left[\frac{1}{r_\pi + r_x + R_T}\right]^2 \qquad (55)$$

FROM BASE OF Q2

$$\overline{v_{no_1}^2} = \frac{\overline{i_{nb_2}^2}(\beta R_L)^2}{A^2}\left[\frac{r_\pi - (r_x + R_T)}{r_\pi + r_x + R_T}\right]^2 \qquad (56)$$

FROM COLLECTOR OF Q2

$$\overline{v_{no_1}^2} = \frac{\overline{i_{nc_2}^2}(\beta R_L)^2}{A^2} \qquad (57)$$

FROM TAIL R_E

$$\overline{v_{no_1}^2} = \frac{\overline{i_{nE}^2}(\beta R_L)^2}{A^2} \qquad (58)$$

where

$$A = \beta + 1 + \frac{r_\pi + r_x + R_s}{R_E} + \frac{(\beta+1)(r_\pi + r_x + R_s)}{r_\pi + r_x + R_T} \qquad (59)$$

The noise figure of the single sided input, single sided output amplifier is now obtained by letting $\overline{v_{no_1}} = \overline{v_{no}}$ and $R_T \longrightarrow 0$ and proceeding as in 1.7. Assuming that $\beta \gg 1$ and $r_\pi \gg r_x$ (low current operation) we find

$$F = 1 + \frac{r_x}{R_s} + \frac{r_x}{R_s}\left[\frac{g_m}{g_m + g_E}\right]^2 + \frac{g_m}{2\beta R_s}\left[r_x + R_s + \frac{1}{g_m + g_E}\right]^2 + \cdots$$

$$\cdots + \frac{g_m}{2\beta R_s}\left[\frac{1 - g_m r_x}{g_m + g_E}\right]^2 + \frac{g_m}{2R_s}\left[\frac{1/\beta\,(1 + R_s/R_E + g_m(r_x + R_s)) + g_E/g_m}{g_m + g_E}\right]$$

$$+ \cdots$$

$$\cdots + \frac{g_m}{2R_s}\left(\frac{1}{g_m + g_E}\right)^2 + \frac{R_E}{R_s}\left(\frac{1}{g_m + g_E}\right)^2 \qquad (60)$$

where $g_E = 1/R_E$ (61)

Clearly, as for the common emitter noise figure, both current and voltage noise terms are present. Theoretical plots of the noise figure of the single sided input, single sided output differential amplifier are shown in figures 8(a) and 8(b). The optimum value for R_s giving the lowest F decreases with increasing collector current as in the common emitter amplifier. The tail resistor R_E can be seen to have little effect when it is large, specifically when

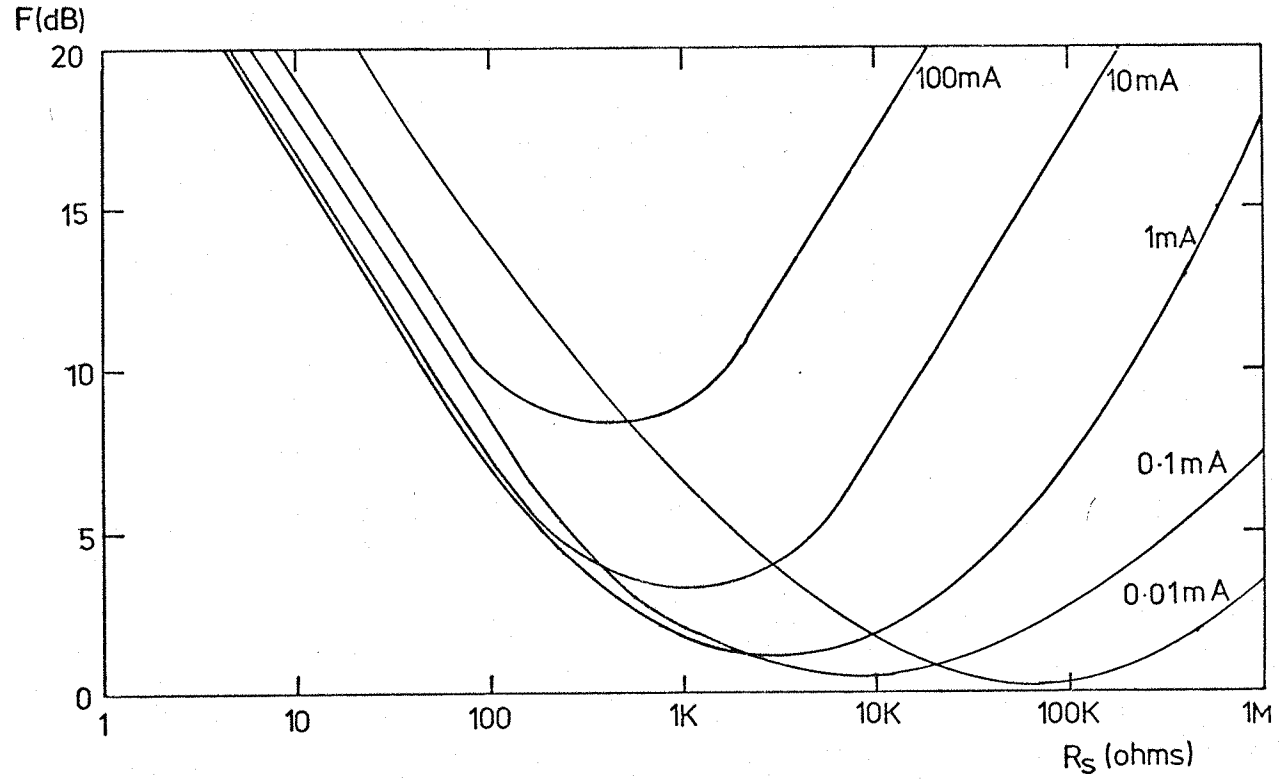
$$R_E \gg r_\pi + r_x + R_s \qquad (62)$$

In these plots, a value of $\beta = 400$ and $r_x = 200$ ohms is assumed. A striking comparison between the noise performance of this amplifier with that of the common emitter is realised by setting $R_E = \infty$. This relation should indeed be approximately satisfied for a good tail source. Equation(60) then reduces to

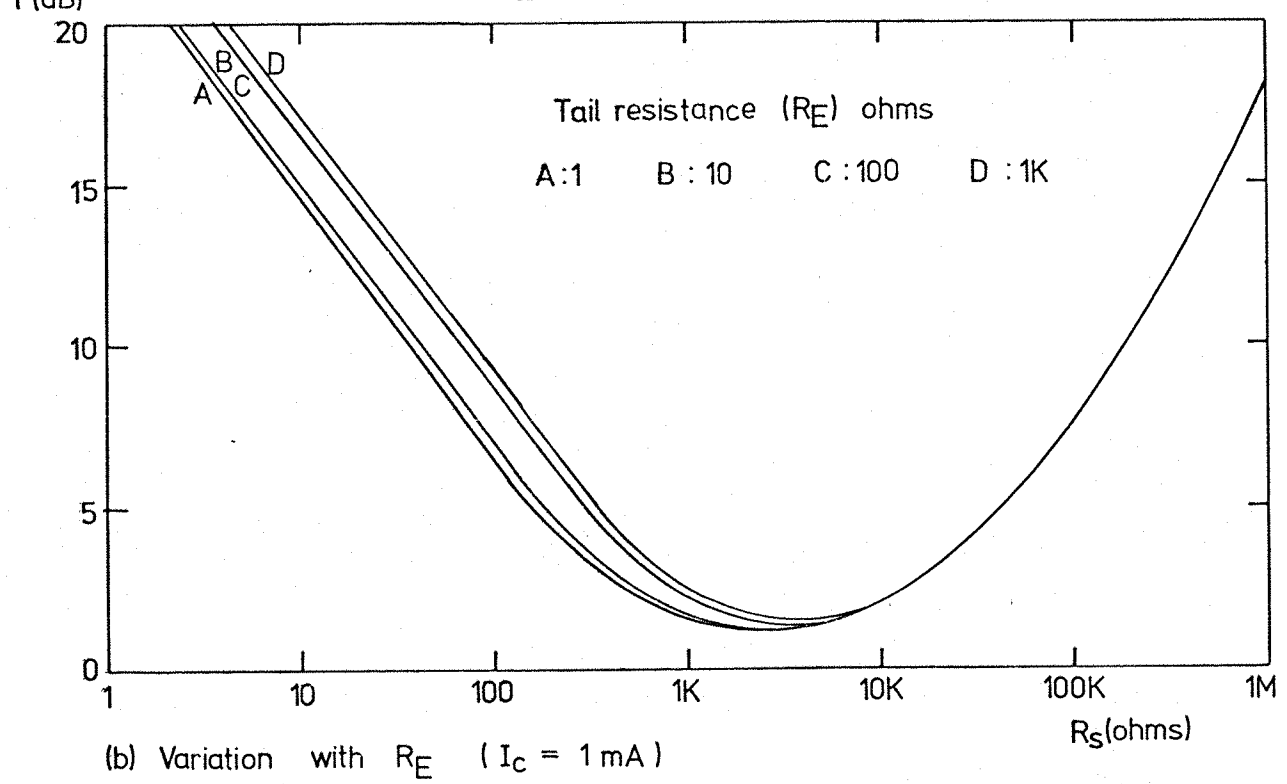
$$F = 1 + \frac{2r_x}{R_s} + \frac{1}{g_m R_s} + \frac{g_m R_s}{2\beta} \qquad (63)$$

When this is compared with the common emitter analysis in equation(23) it can be seen that the voltage noise terms are doubled, but the current noise terms remain identical.

A quantitative comparison of noise figure with the voltage and current generators is shown in the appendix.



(a) Variation with I_C (R_E = 10 K ohm)



(b) Variation with R_E (I_C = 1 mA)

Figure 8. Theoretical plots of noise figure against source impedance for the single-sided input, single-sided output differential amplifier

3.2 THE APPROXIMATE NOISE ANALYSIS

The noise analysis just described shows that the voltage noise in the single sided input, single sided output differential amplifier is twice that of the common emitter, but the current noise is the same within the limits of the approximations made. A full comparison of noise in the differential amplifier to noise in the common emitter amplifier would have to include the four possible modes of operation of the differential amplifier, namely

(a) Single sided input, single sided output (designated S-S)

(b) Single sided input, differential output (designated S-D)

(c) Differential input, single sided output (designated D-S)

(d) Differential input, differential output (designated D-D)

As will no doubt be now apparent to the reader, it would be very tedious to repeat the analysis in 3.1 for each of these four modes. A much simpler analysis is possible if some intelligent assumptions are made. Firstly, R_E is set to infinity. So the small contribution of noise from the tail resistor is neglected. Secondly, the noise from R_L is neglected as before. Thirdly, we assign a general noise model for each device Q1 and Q2 as explained in 1.6. For the sake of argument, Q1 is assigned $\overline{v_{n1}}$ and $\overline{i_{n1}}$; Q2 is assigned $\overline{v_{n2}}$ and $\overline{i_{n2}}$. Then the contribution to noise at the output from each of these four sources in turn is evaluated for a particular mode. By dividing by the appropriate voltage or current gain, the noise can be referred back to the input, expressed in terms of a single $\overline{v_n}$ and $\overline{i_n}$. Finally, a comparison of $\overline{v_n}$ with $\overline{v_{n1}}$ and $\overline{v_{n2}}$ and $\overline{i_n}$ with $\overline{i_{n1}}$ and $\overline{i_{n2}}$ can be made. It is important to note that $\overline{v_{n1}} = \overline{v_{n2}}$ and $\overline{i_{n1}} = \overline{i_{n2}}$ for a perfectly matched pair. Furthermore, the comparison just mentioned immediately compares the noise performance of the

common emitter amplifier. This analysis was carried out for each mode, and a comparison with the common emitter was obtained by dividing the appropriate parameter for a mode by the same parameter for the common emitter. The results are summarised in the table below.

RATIOS

MODE	$\frac{A_v}{A_vCE}$	$\frac{A_i}{A_iCE}$	$\frac{v_n^2}{v_n^2CE}$	$\frac{i_n^2}{i_n^2CE}$	$\frac{v_n}{v_nCE}$	$\frac{i_n}{i_nCE}$	$\frac{v_{nout}}{v_{nout}CE}$	$\frac{i_{nout}}{i_{nout}CE}$
SS	$\frac{1}{2}$	1	2	1	$\sqrt{2}$	1	$\frac{1}{\sqrt{2}}$	1
SD	1	2	2	1	$\sqrt{2}$	1	$\sqrt{2}$	2
DS	$\frac{1}{2}$	1	2	1	$\sqrt{2}$	1	$\frac{1}{\sqrt{2}}$	1
DD	1	2	2	$\frac{1}{2}$	$\sqrt{2}$	$\frac{1}{\sqrt{2}}$	$\sqrt{2}$	$\sqrt{2}$

The absolute magnitudes of v_n and i_n for the common emitter amplifier are as given in equations(10) and (11). Of course, $A_v = -g_m R_L$ and $A_i = \beta$ for the common emitter amplifier. It can be seen that the voltage noise is double in each mode, but the current noise is the same except in the case of the D-D mode amplifier where it is HALVED.

Here, the current noise is actually HALF that of the common emitter amplifier. These results are perfectly general, and would be true for MOS transistors as well as bipolars. The theory simply hinges on the fact that the devices are voltage controlled current sources.

3.3 TRANSISTOR AS CURRENT SOURCE

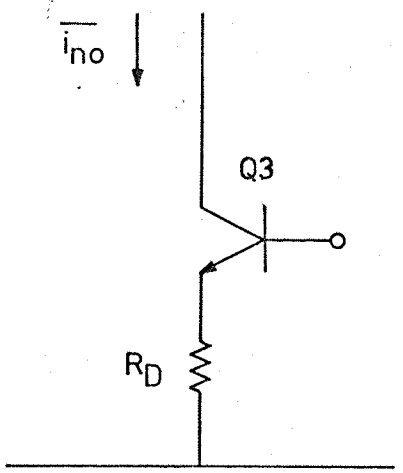
The value of having a transistor as a current source was explained in 3.1. It is also worthwhile mentioning that it is far more convinient to integrate a small NPN transistor than a large valued resistor. The full arrangement when used with the long tailed pair is shown in figure 6(c). In practice, a resistor R_D is often placed in series with the emitter in order to provide degeneration as shown in figure 9(a). We will show that this has a significant effect on the noise performance. The transistor source, Q3, together with the degeneration resistor, R_D, will deliver a noisy current i_{no} to the emitters of the pair transistors, Q1 and Q2, which will in turn produce an additional noisy voltage at the outputs $\overline{v_{o1}}$ and $\overline{v_{o2}}$. The overall noise performance of the circuit can be compared to that of the tail resistor source circuit performance by contrasting the noisy currents that each tail source delivers. The noise equivalent circuit for the current source is shown in figure 9(b). We assume that the base is fed with a noiseless DC current (ie base short circuited for signals). Nodal analysis of this model now yields

$$\overline{i_{no}^2} = \frac{\overline{v_{nx}^2}\beta^2 + \overline{i_{nD}^2}(\beta R_D)^2 + \overline{i_{nb}^2}(\beta r_x + \beta R_D)^2 + \overline{i_{nc}^2}(r_\pi + r_x + R_D)^2}{\left[(\beta+1)R_D + r_\pi + r_x\right]^2} \qquad (64)$$

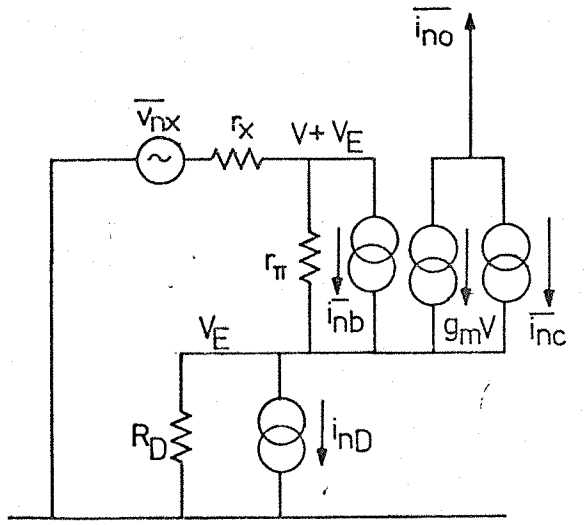
This noisy current can now be compared to that of the ordinary tail resistor, $\overline{i_{nE}^2}$. The two limiting cases are for $R_D \to 0$ (no degeneration) and for $R_D \to \infty$ (full degeneration):

(a) When $R_D \to 0$, the current source Q3 supplies the same noise as would a tail resistor of value $R_E = 2/g_m$

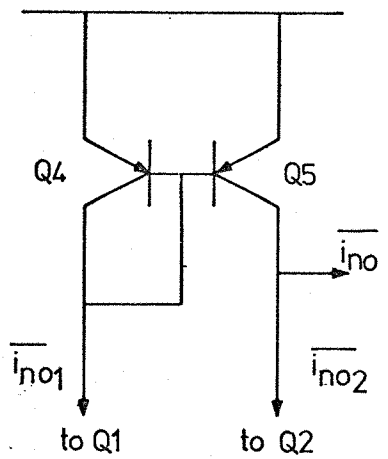
(b) When $R_D \to \infty$, the current source supplies the same noise as



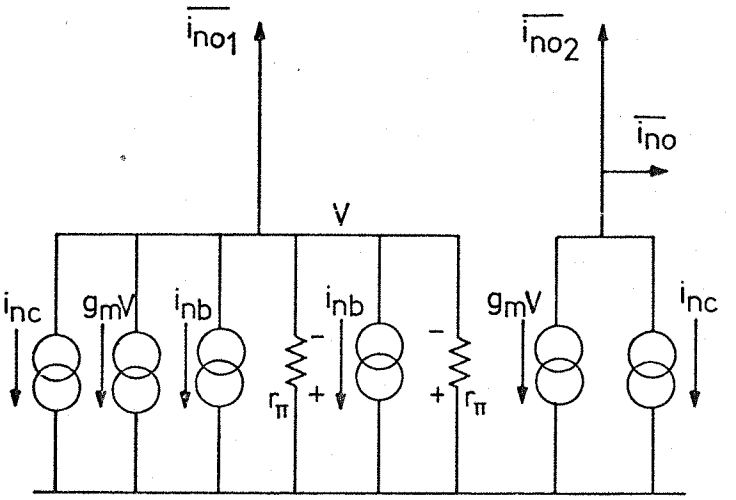
(a) Transistor as current source



(b) Equivalent circuit



(c) Active load



(d) Equivalent circuit

Figure 9.

would a tail resistor of value R_D

It is obvious from these two criteria that if some degree of degeneration is included, a larger tail current can be drawn and still give the same noise level. However, in this case, the current source will drop more DC volts due to the presence of R_D. Nevertheless, in the case of the differential output modes, the noise performance of the tail is irrelevant because two fully correlated contributions appear at either collector, and since their difference is taken, the noise cancels.

3.4 DIFFERENTIAL TO SINGLE SIDED CONVERTER

The majority of integrated circuit operational amplifier designs do not use passive load resistors at the collectors of the input differential pair, but an active differential to single sided converter[19]. The arrangement with the long tailed pair is shown in figure 6(d). The most basic form of this circuit building block is shown in figure 9(c) together with its small signal noise equivalent circuit in figure 9(d). Nodal analysis of the equivalent circuit gives the total noisy current at the output to be

$$\overline{i_{no}}^2 = \left(\frac{\beta}{\beta+2}\right)^2 \left(\overline{i_{nb_1}}^2 + \overline{i_{nb_2}}^2 + \overline{i_{nc_1}}^2\right) + \overline{i_{nc_2}}^2 + \left(\frac{\overline{i_{no_1}}^2 - \overline{i_{no_2}}^2}{\beta+2}\right)^2 \tag{65}$$

$\overline{i_{no_1}}^2$ and $\overline{i_{no_2}}^2$ can be obtained directly from equations (50-58) by summing the contributions and dividing throughout by R_L^2. The contributions at the collector of Q1 are exactly the same as those at the collector of Q2 except that R_S and R_T are interchanged throughout. In summing contributions, R_T is set to zero for the simplest case, the noise from r_x is neglected, and R_E is

assumed to be infinite. Then, after some manipulation, the total output noise is found to be

$$\overline{i_{no}^2} = \overline{i_{ns}^2}\left(\frac{2\beta R_s}{D}\right)^2 + \overline{i_{nb_1}^2}\left(\frac{(2\beta R_s)^2+D^2}{D^2}\right) + \overline{i_{nb_2}^2}\left(\frac{R_s^2+D^2}{D^2}\right) + \cdots$$

$$\cdots + \overline{i_{nc_1}^2}\left(\frac{(R_s+2r_\pi)^2+D^2}{D^2}\right) + \overline{i_{nc_2}^2}\left(\frac{(2r_\pi)^2+D^2}{D^2}\right) \qquad (66)$$

where $D = 2r_\pi + R_s$ (67)

The parts shown in heavy type (D) are from the converter itself. It can be seen from this equation that the active load arrangement adds significantly to the noise performance.

CHAPTER 4

EXPERIMENTAL MEASUREMENTS ON THE NOISE PERFORMANCE OF THE DIFFERENTIAL PAIR.

This chapter describes the experimental measurements carried out on the bipolar differential pair, and the results obtained. The experiment itself was divided into two main parts:

(a) An investigation into the behaviour of the S-S mode differential amplifier. This includes looking at the noise performance with various tail currents.

(b) A comparison of the four modes of operation of the differential amplifier with the common emitter.

In each case, the results are displayed on graphs; solid lines show the expected performance from evaluation of the theory and experimental measurements are shown as a set of data points.

4.1 NOISE PERFORMANCE OF THE S-S MODE DIFFERENTIAL AMPLIFIER

The experimental technique used for this part of the investigation was the noise generator method as described in 2.2. A circuit diagram of the amplifier is shown in figure 10 and its measured frequency response in figure 11. Q1 and Q2 form the differential pair to be examined. The base current for Q1 is supplied via DC coupling to the source resistance. The two branch currents of the pair are balanced by trimming VR1, and a new balance must be made with each new value of R_S. Voltmeters V1, V2 ensure that the currents down each branch are equal and the ammeter A measures the total tail current. C1 ensures that the base of Q2 is AC grounded for all noise signals of interest. R7, C2 and R8, C3 form decoupling networks on the power rails in an attempt to suppress power supply hum and the possibility of oscillation due to positive feedback via the

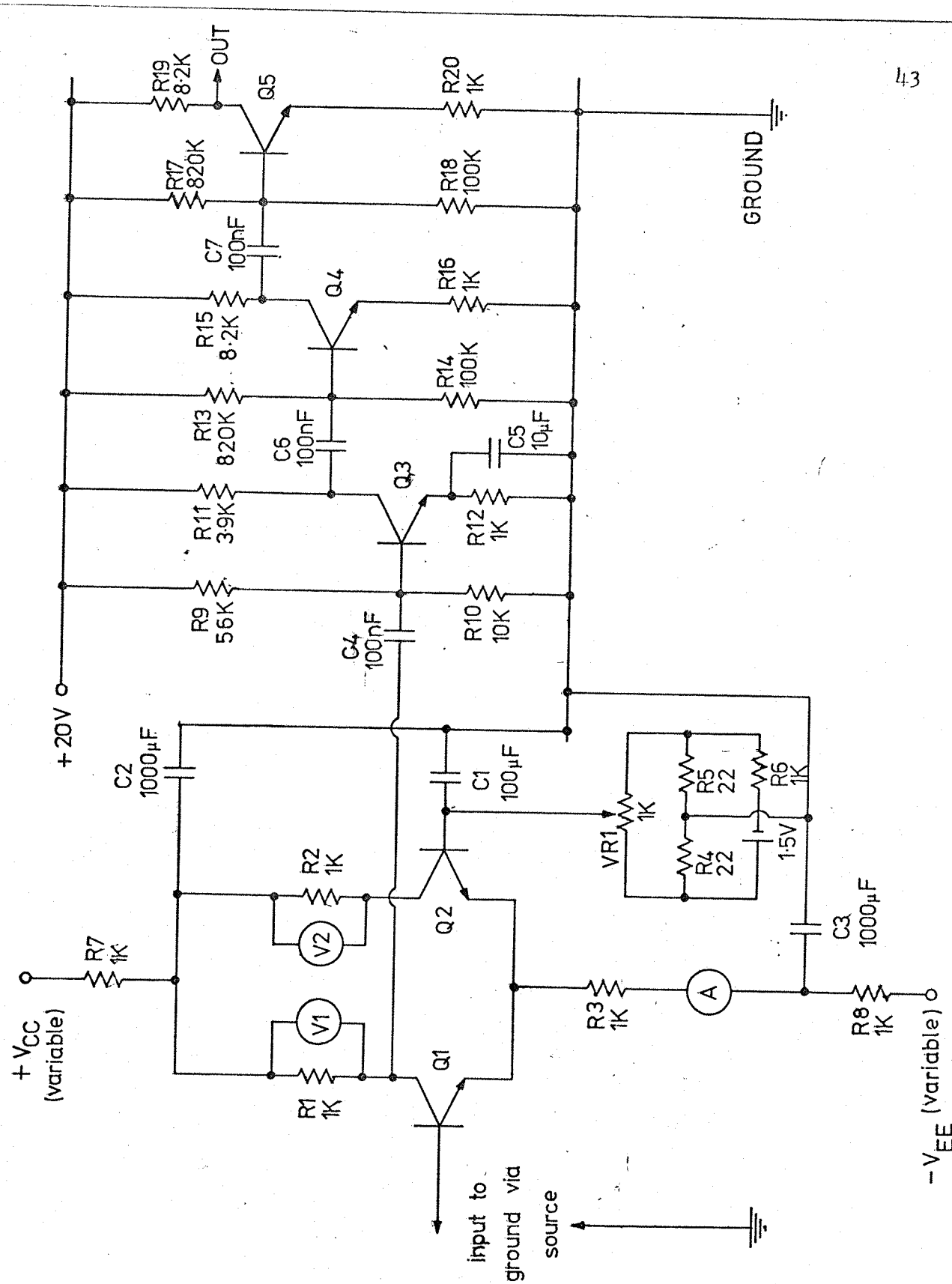


Figure 10. Experiment for S–S mode differential amplifier

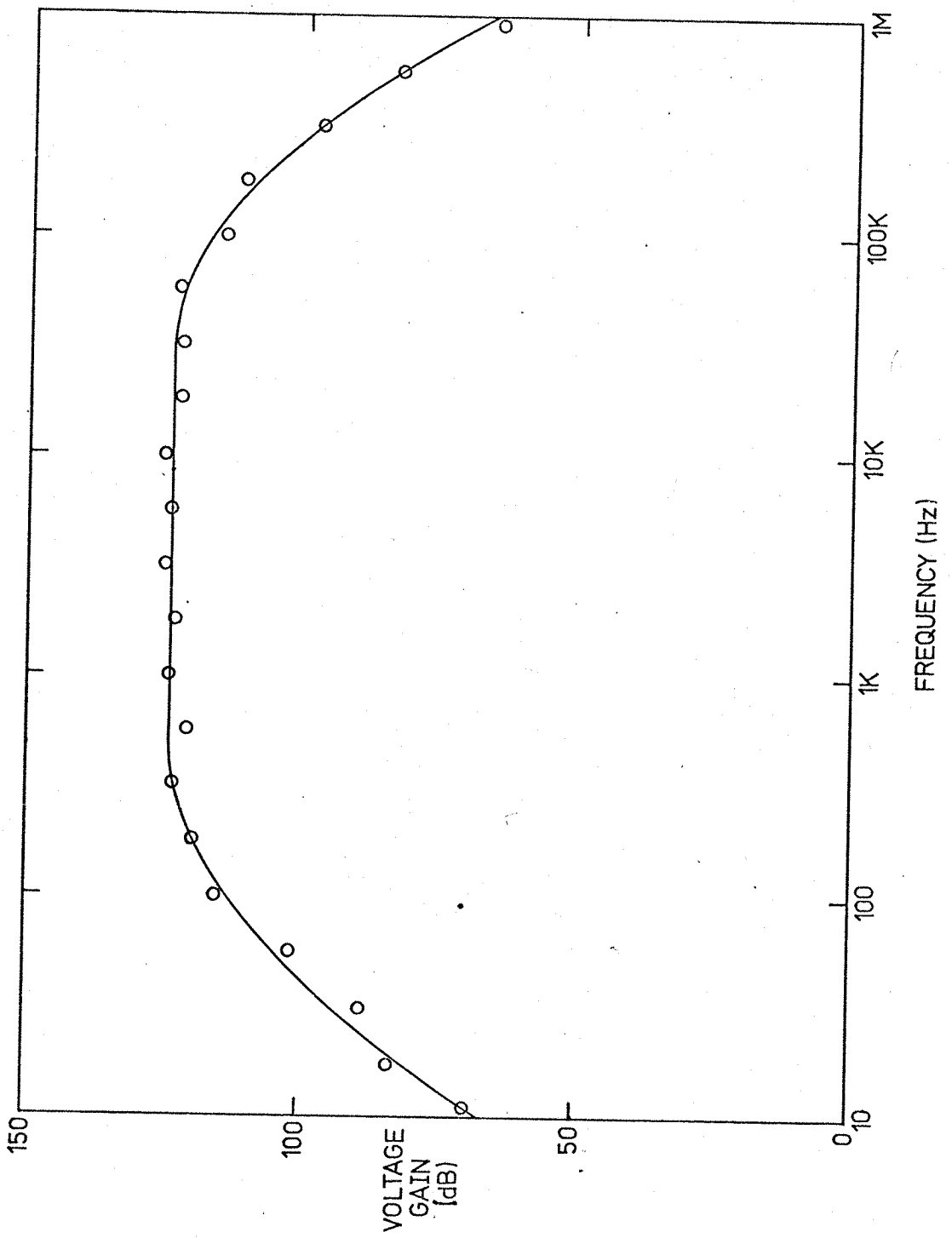


Figure 11. Measured frequency response of the long-tailed pair with noise boosting amplifier

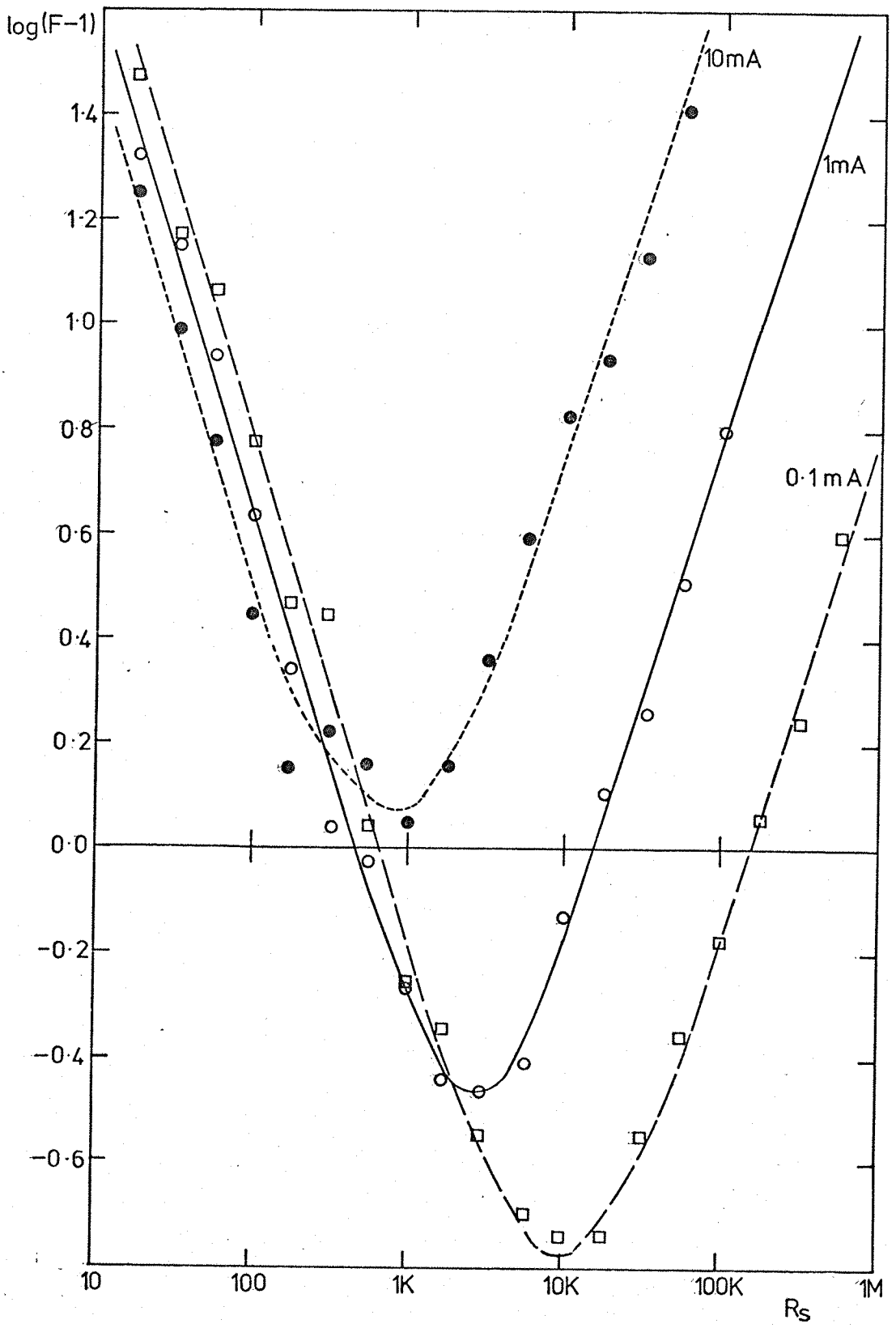


Figure 12. Experimental results for the S-S mode differential amplifier

power supplies. The noisy output of the differential pair at the collector of Q1 is fed to a cascade of amplifiers constructed from Q3, Q4 and Q5. The output then goes to the filter and RMS meter. The tail current is varied by altering $-V_{EE}$ and $+V_{cc}$ to ensure that V_{ce} remains constant. When making a noise measurement, V1 and V2 are disconnected to ensure that they do not introduce excess noise.

All of the transistors Q1-Q5 used in this experiment were silicon planar NPN's (BC182L from Texas Instruments). The measuring equipment used was as follows:

(a) Noise generator: Quan-Tech Model 420

(b) Power supplies: Farnell type E30/1

(c) Oscilloscope: Telequipment D67

(d) Filter: Rockland Analog Filter model 1200

(e) RMS meter: Hewlett Packard model 3400A

In measuring the noise figure of the amplifier, the bandwidth is selected to be relatively narrow, so that the spot noise figure rather than wide-band noise figure is measured. A bandwidth of 9kHz-11kHz was chosen to ensure that no 1/f noise was present and the frequency response was still maintained. The results of the experiment are shown in figure 12. The error bars have been omitted to avoid confusion, but a check with 2.4 will reveal that all of the experimental points lie within the allowed spread from the theory.

4.2 COMPARISON OF THE FOUR DIFFERENTIAL MODES WITH THE COMMON EMITTER AMPLIFIER

In evaluating the theory for a comparison between modes, R_E was assumed infinite. It follows that R_E will have to be very large (as required by equation(62)) if the halving effect of

the current noise for high R_s is to be seen. The noise generator method could not be used here because as was mentioned in 2.4, one end of the source impedance has to be grounded. This is not possible with a differential source. For this reason, the two temperature method was used instead. A circuit diagram of the differential pair with boosting amplifier is shown in figure 13. The circuit is essentially the same as that used for the previous experiment, but the second stage is also a long tailed pair to allow for the facility of single sided output or differential output.

There are three switches, SW1, SW2 and SW3 in the circuit. These switches allow the amplifier to be switched into one of its four possible modes. SW1 and SW2 ground the bases of Q1 and Q2 respectively from the point of view of signals. This allows either input to be single sided or differential. SW3 controls the nature of the output. In the 'ON' position, the collector of Q2 is fed to the base of Q3 via coupling capacitor C4, and the output is differential. In the 'OFF' position, the base of Q3 is grounded via R11. This means that the output is single sided, because Q3, Q4 is now acting as a balanced single sided input amplifier since R11 = R3. The table below shows the positions of the switches for each of the four modes.

MODE	SW1	SW2	SW3
SS	OFF /ON	ON/OFF	OFF
SD	OFF /ON	ON/OFF	ON
DS	OFF	OFF	OFF
DD	OFF	OFF	ON

Q5 and Q6 are straightforward common emitter amplifiers with series current feedback. These boost the noise into the 1V RMS

region. As before, R20,C7 and R21,C8 form decoupling networks on the supply rails. The ammeter A measures the total tail current which is set to 2mA (I_C= 1mA) for the whole of the experiment. Screened leads were used to connect the bases of Q1 and Q2 to the source resistances. Once again, the freq.band was selected at 9kHz-11kHz, all transistors Q1-Q6 were BC182L's and the measuring equipment was the same as for the previous experiment. The results are shown in figure 14. The theory for the common emitter has also been plotted on these diagrams so that a direct comparison may be made.

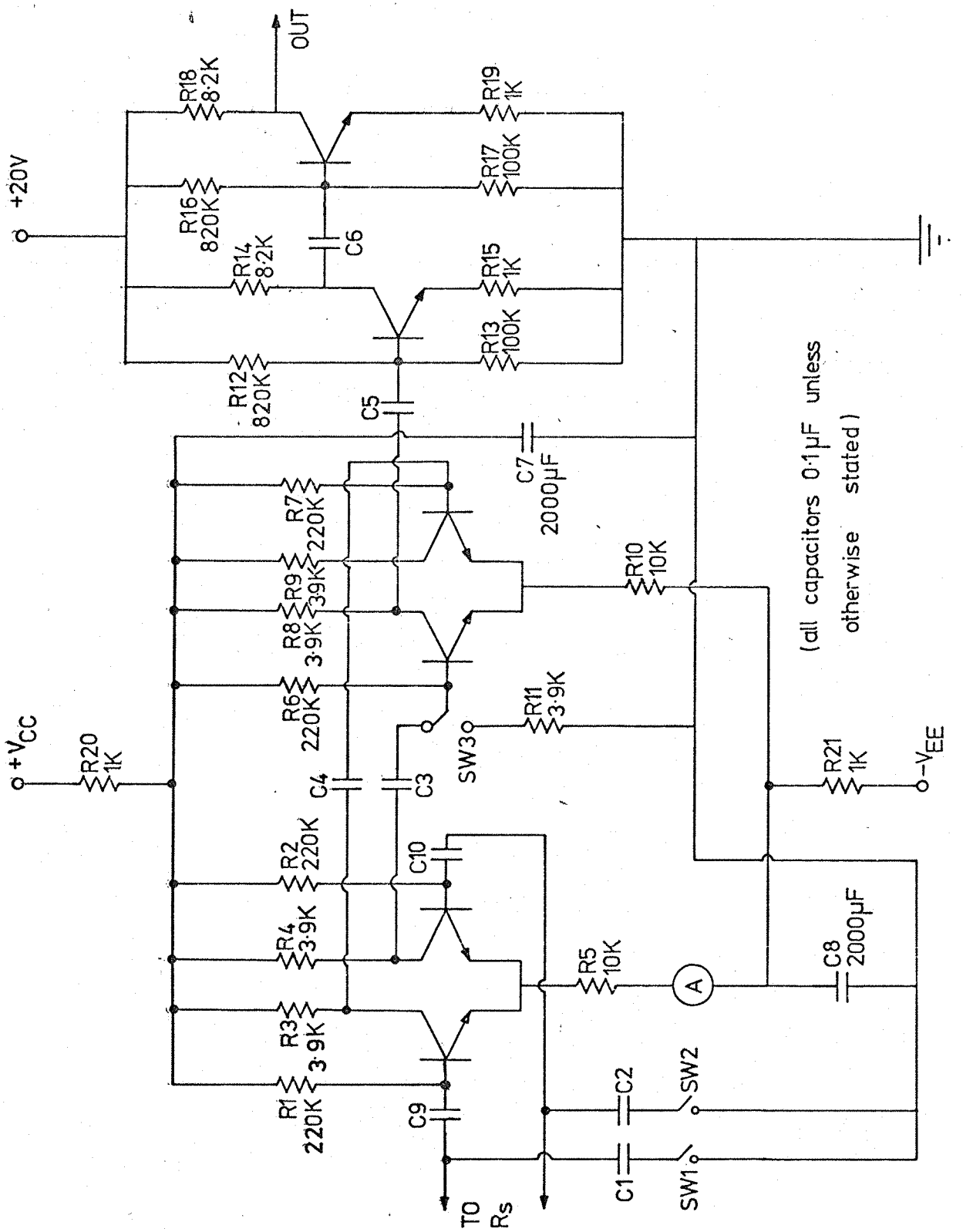


Figure 13. Circuit for comparison of differential amplifier modes

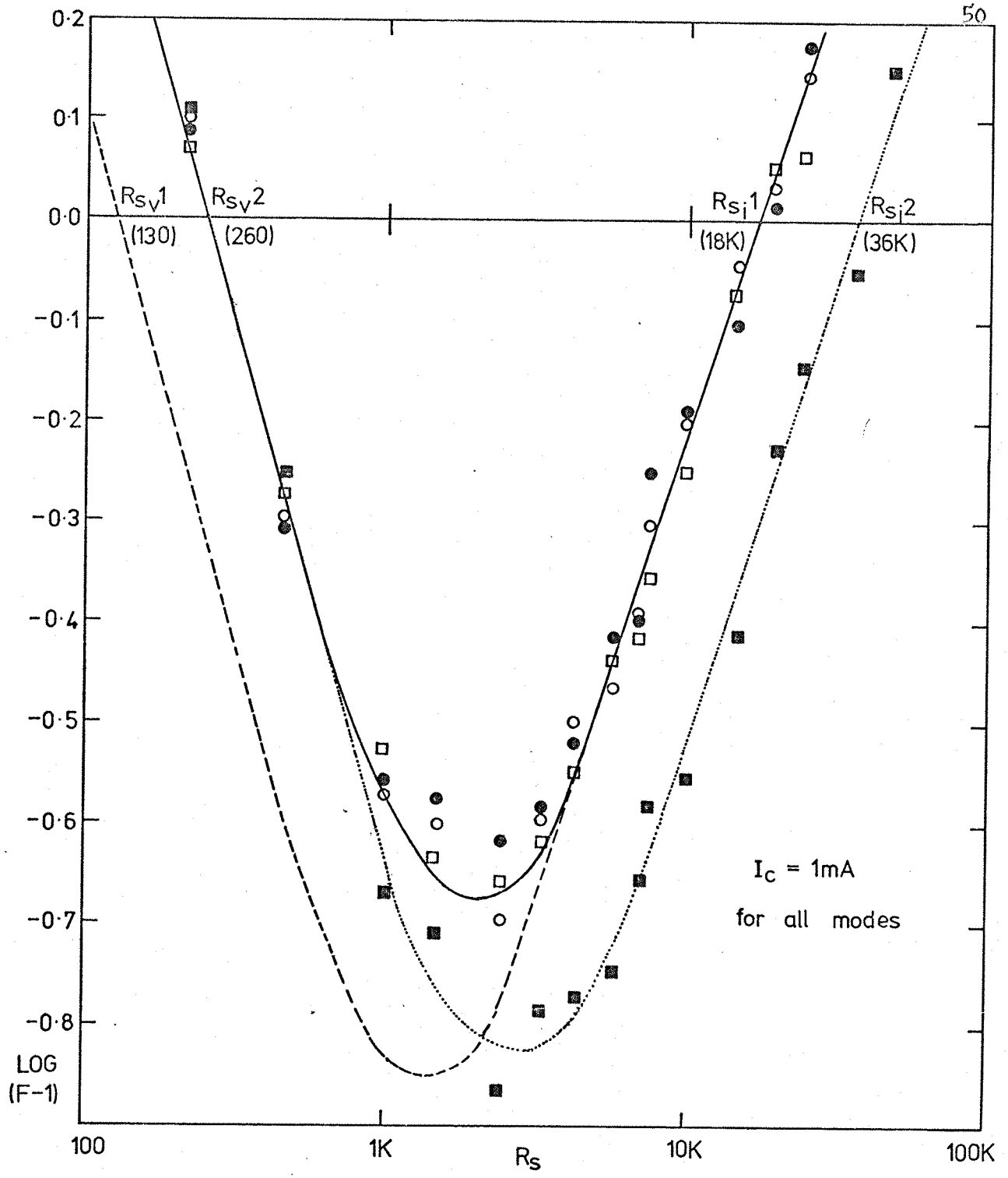


Figure 14. Experimental comparison of noise in the four differential modes with noise in the common emitter

mode	CE	SS	SD	DS	DD
experiment		o	●	□	■
theory	----	——	——	——	——

CHAPTER 5

DESIGN OF AN INTEGRATED LOW NOISE AMPLIFIER

The work described so far has been mainly concerned with the noise performance of the differential pair as compared with that of the common emitter. In particular, it has been shown that the noise performance of an amplifier is dominated by the value of the base spreading resistance when the amplifier is used with a low source impedance (ie $R_s < r_{\pi}$). This chapter describes an amplifier design procedure carried out in order to meet the specifications listed in the introduction as closely as possible. It is perhaps important to note at this point that bipolar technology was originally chosen for fabrication of the amplifier because the JFET and MOST exhibit very poor noise figures (typically in excess of 15dB) for low values of source impedance[14]. In a sense, this chapter is divided into three parts. Firstly, information regarding the device parameters in the process to be used must be obtained. Secondly, a full circuit design is proposed, and this circuit is tested by bread-boarding of discrete equivalents and by computer analysis of an integrated analogue. Finally, a layout suitable for integration is described, and the resulting integrated circuits are tested after encapsulation. The bipolar processing of these circuits was carried out in the clean room of the microelectronics department of Southampton University.

5.1 MODELLING OF THE BIPOLAR PROCESS

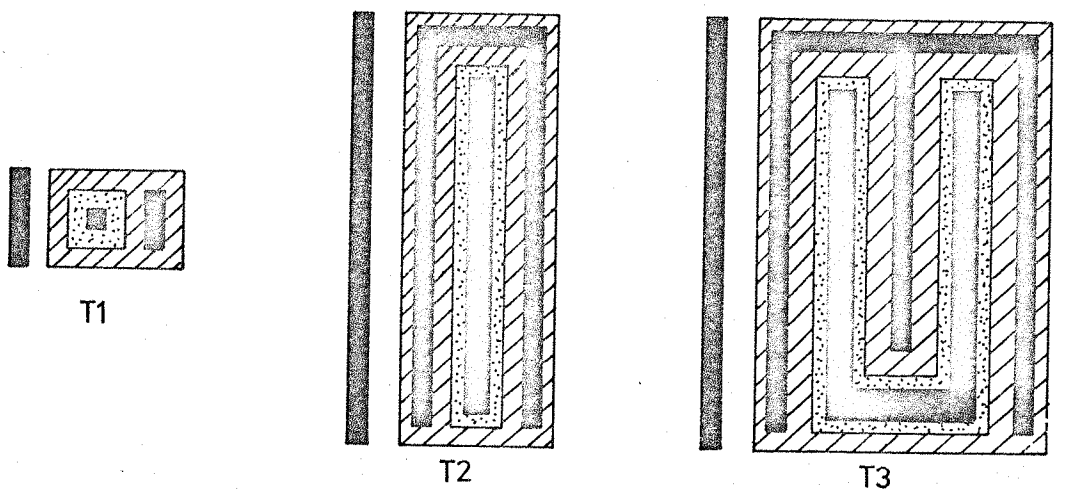
In order to design an amplifier, it is necessary to know the individual component parameters to a reasonable degree of accuracy. For the bipolar transistor (be it NPN or PNP) this involves a knowledge of the magnitudes of the elements within the full hybrid

pi model as was shown in figure 1(a). r_{cs}, r_o and β (and hence r_π) are obtained with sufficient accuracy from a curve tracer[10]. The input capacitance, C_π, and the feedback capacitance, C_μ are most easily measured using an AC impedance bridge[12]. r_x may be measured by examining the noise figure in the low source impedance region where the voltage noise due to r_x dominates. Specifically, a plot of log(F-1) against R_s gives a value for $r_x + \frac{1}{2g_m}$ where the curve cuts the R_s axis (see section 1.7). It can be shown that for an amplifier to have a noise figure of less than 2 (ie 3dB) at a source impedance of 50ohms, r_x must itself be no more than 50ohms. This in fact assumes that all current noise in the device is neglected. For this reason, several configurations of input transistor were considered in an attempt to decrease r_x. It is well known that an interdigitated structure for the base-emitter junction tends to minimise the effect of the parasitic r_x because the ratio of perimeter to surface area of the emitter region is increased[20]. Several NPN transistor layouts are shown in figure 15(a) and the measurements performed on their base spreading resistances are included in figure 16. A minimum geometry lateral PNP was also integrated on a test chip with the foresight that most integrated amplifier circuits require a PNP device at some point in their design. This is shown in figure 15(b) and its performance tabulated in figure 16.

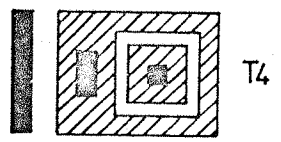
Finally, three types of resistor were tested prior to circuit design. These are

(a) Low valued diffused resistor formed by emitter (n^+) diffusion
(b) Medium valued diffused resistor formed by base (p) diffusion
(c) High valued 'pinch' resistor formed from a p channel with a superimposed n^+ diffusion.

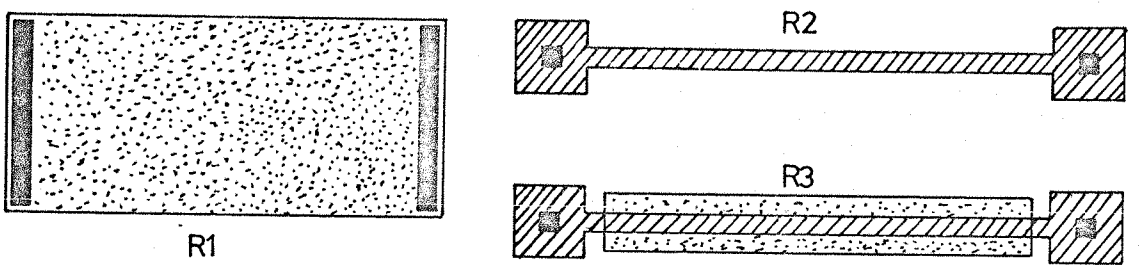
They are shown in figure 15(c), and their values in figure 16. In



(a) npn transistors
- T1 : minimum geometry
- T2 : folding base contact
- T3 : double emitter stripe



(b) T4: minimum geometry lateral pnp transistor



(c) resistors
- R1 : emitter (n^+) diffused type
- R2 : base (p) diffused type
- R3 : pinched (n^+ on p) type

contact window | base | emitter | land

Figure 15. Layout of test devices for parameterization
(scale : 1mm to 4 microns)

	T1	T2	T3	T4
BETA 0·1 mA I_C	80	75	85	10
BETA 1 mA I_C	100	90	100	7
BETA 10 mA I_C	150	170	130	0·5
r_{cs}	20	20	20	400
r_o (at I_C=1mA)	10K	10K	10K	7K
C_π (pF) (at I_C= 1mA)	340	335	339	526
C_μ (pF)	0·4	3·5	6·8	1·6
r_x	220	154	45	—

(a) transistors

	approximate value (ohms)	number of squares	approximate sheet resistivity of diffusion (ohms/square)
R1	10	2	5
R2	2·6K	24	100
R3	115K	22	—

(b) resistors

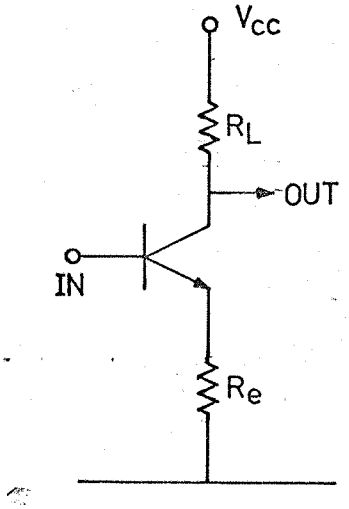
Figure 16. Typical measured values of test device parameters

measuring a diffused n^+ resistor of the type R1 as shown in figure 15, it is necessary to ensure that the surrounding silicon 'land' is p-type to avoid shorting the resistor through the land. A surrounding p-type background implies that the resistor itself will always be reverse-biased with respect to its surroundings. Similar backgrounds are not required for the other two types (R2 and R3) since the substrate is weakly n-type to begin with.

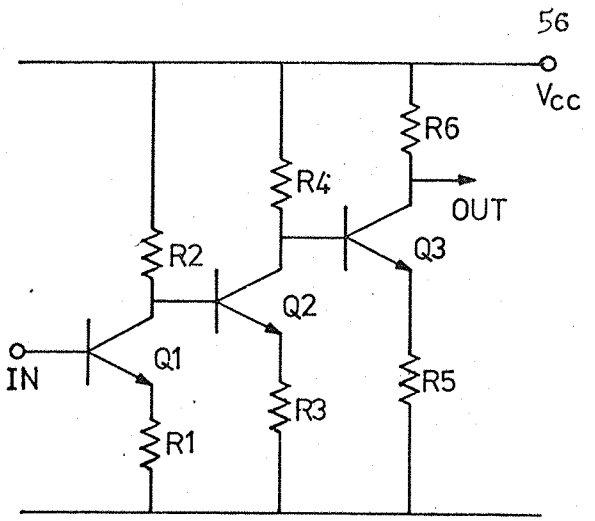
5.2 CIRCUIT DESIGN CONSIDERATIONS

Because the noise figure of an amplifier is dominated by the noise performance of the first stage, careful optimization of the first stage is essential. The choice of configuration of the input stage is largely determined by four requirements, namely low power consumption, good voltage gain, high input impedance and low noise figure. For this reason, a common emitter stage using series current feedback was decided upon. This is shown in figure 17(a). The DC response of the long tailed pair (no coupling capacitor) was sacrificed in order to meet the other requirements just mentioned. The long tailed pair has twice the power consumption, twice the input noise and half the voltage gain of the common emitter. Transistors with a base spreading resistance of 25 ohms at the very most would be required for the long tailed pair input noise requirement, but a common emitter transistor could have an r_x of less than 50 ohms and still meet the specified noise performance. If a sufficiently large transistor is used in the input stage, we can expect a base spreading resistance of somewhere in the region 10 to 50 ohms (see figure 16).

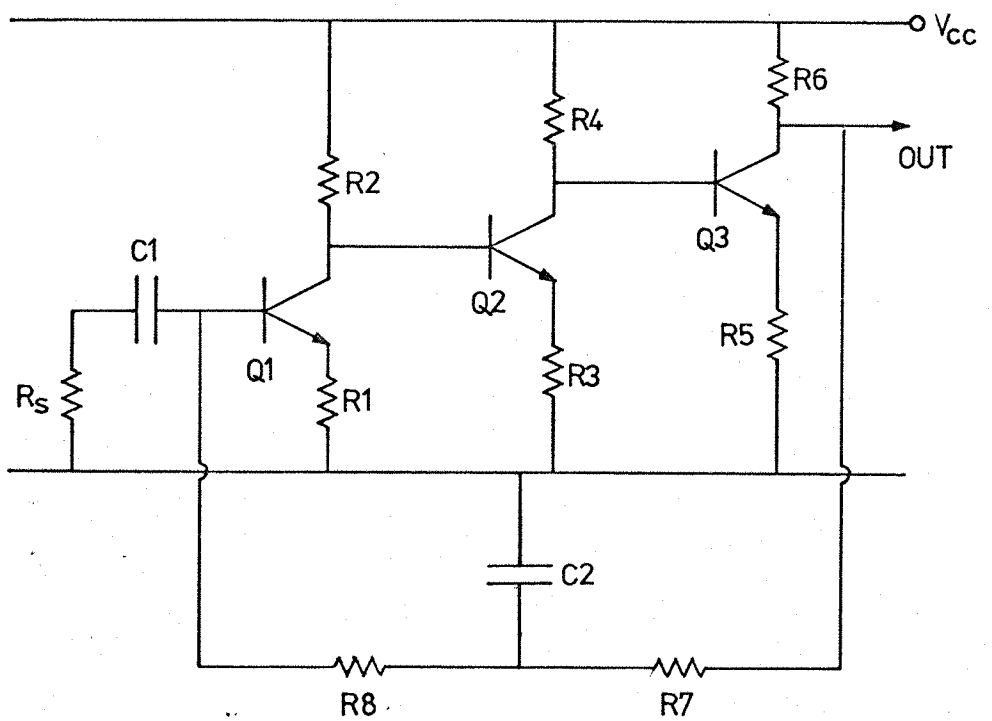
The collector current for the input transistor may now be fixed for optimum noise performance. Differentiation of



(a) series current feedback



(b) 3-stage DC coupled amplifier



(c) 3-stage DC coupled amplifier with biasing network

Figure 17. Amplifier circuit designs

equation 23 with respect to g_m yields

$$g_{m_{opt}} = \beta / R_s \tag{68}$$

from which

$$I_{c_{opt}} = kT\beta / qR_s \tag{69}$$

Assuming a source impedance of 50 ohms and a current gain of 80 we expect the noise figure to be a minimum when I_c is approximately 3mA. It is important to note, however, that this minimum is quite broad. Local series current feedback of the stage will stabilize the voltage gain and increase the input impedance. Approximating the expression for the voltage gain of such a stage obtained by nodal analysis gives

$$A_v = \frac{-R_L}{R_e + 1/g_m} \tag{70}$$

and the expression for the input impedance is

$$Z_{in} = r_\pi + \beta R_e \tag{71}$$

If the supply voltage, V_{cc}, is set to 1.5V in order to keep power consumption to a minimum, then the collector of the first transistor can be assumed to be at a potential of around 0.7V (halfway between V_{cc} and ground) in order to maximise the output AC signal swing. This means that a load resistor of approximately 330 ohms is needed to give the required collector current from the point of view of noise performance.

The value of the local feedback resistor, R_e, can now be fixed. Gain stability is improved by increasing R_e, but equation (30) shows that R_e effectively adds on to r_x when the noise figure of the stage is evaluated. Clearly, we cannot afford to make R_e

larger than about 5 ohms. When R_e is 5 ohms, the voltage gain of the stage, given by equation (70), is approximately 22, or 27dB, and the input impedance, given by equation (71), is approximately 1.5 kohm. This will of course be dramatically increased when overall feedback is applied and the amplifier is used in the closed loop mode.

It can be seen from the list of specifications that the amplifier needs to have a flat response down to DC. This requirement cannot be achieved exactly for a common emitter input because some form of AC coupling must be used at the base of the input transistor. However, careful choice of the input capacitor can fix the lower 3dB break point very close to DC. If the amplifier is to be built from a series of cascades, AC coupling with suitably large capacitors or straightforward DC coupling may be used. Obviously, the latter is to be favoured if eventual integration of the circuit is to be carried out. DC coupling is possible with bipolar transistors because in the forward active region, V_{be} is always larger than the minimum value of V_{ce} corresponding to saturation. For instance, for silicon npn's, $V_{be} \simeq 0.7V$ whereas $V_{ce(sat)} \simeq 0.2V$. This relationship is true for any bipolar because the base-emitter voltage is across a forward biased diode, whereas collector saturation voltage is the DIFFERENCE between two forward biased diode drops. For the amplifier to supply 60dB of gain, it is possible to cascade two stages each with voltage gains of 30dB, or three stages each with 20dB. The three stage amplifier has to be used because it is not possible to achieve a voltage gain of 30dB with local series current feedback in the stage[10]. Moreover, in the three stage design, there is ample gain (each load resistor could be as low as 60 ohms), and some of this can be sacrificed to increase bandwidth.

Such a three stage DC coupled amplifier (without biasing) is shown in figure 17(b).

The next important step is to fix the values of R3, R4, R5 and R6 for the second and third stage. Each stage will need to have a voltage gain similar to the first, and for this reason, the ratio of the load resistors to the emitter resistors should all be kept at approximately 66 to 1. Initially, it was decided to run stages 2 and 3 identically at a collector current of 1mA each, and to have R3 = R5 = 10 ohms and R4 = R6 = 680 ohms. The equivalent circuit was represented as a network with numbered nodes, and this was fed into a linear analysis programme and analysed by computer. The gain and phase response of the original design is shown in figure 18(a). It can be seen from this diagram that when the phase drops to zero, the magnitude of the voltage gain is 53dB at 36MHz. From the specifications, the amplifier has to be stable down to a voltage gain of 46dB. But from this plot, there will still be 7dB of gain left when the net phase shift is zero. Hence regeneration can occur and the amplifier will oscillate at 36MHz.

Nodal analysis of the network soon makes it apparent that the dominant high frequency time constants in the circuit are in the middle stage. Firstly, C_μ for the second transistor was 'artificially' increased by adding extra external capacitance across the base-collector junction. This was in an attempt to lower f_T for the second stage. C_μ was altered from its original value of 0.4pF to 20pF. The frequency response of the new configuration was evaluated by computer as before, and the result is shown in figure 18(b). Note that the open loop gain is now approximately 50dB when the net phase shift is zero. This occurs at a frequency of 26MHz. So increasing C_μ has little effect on

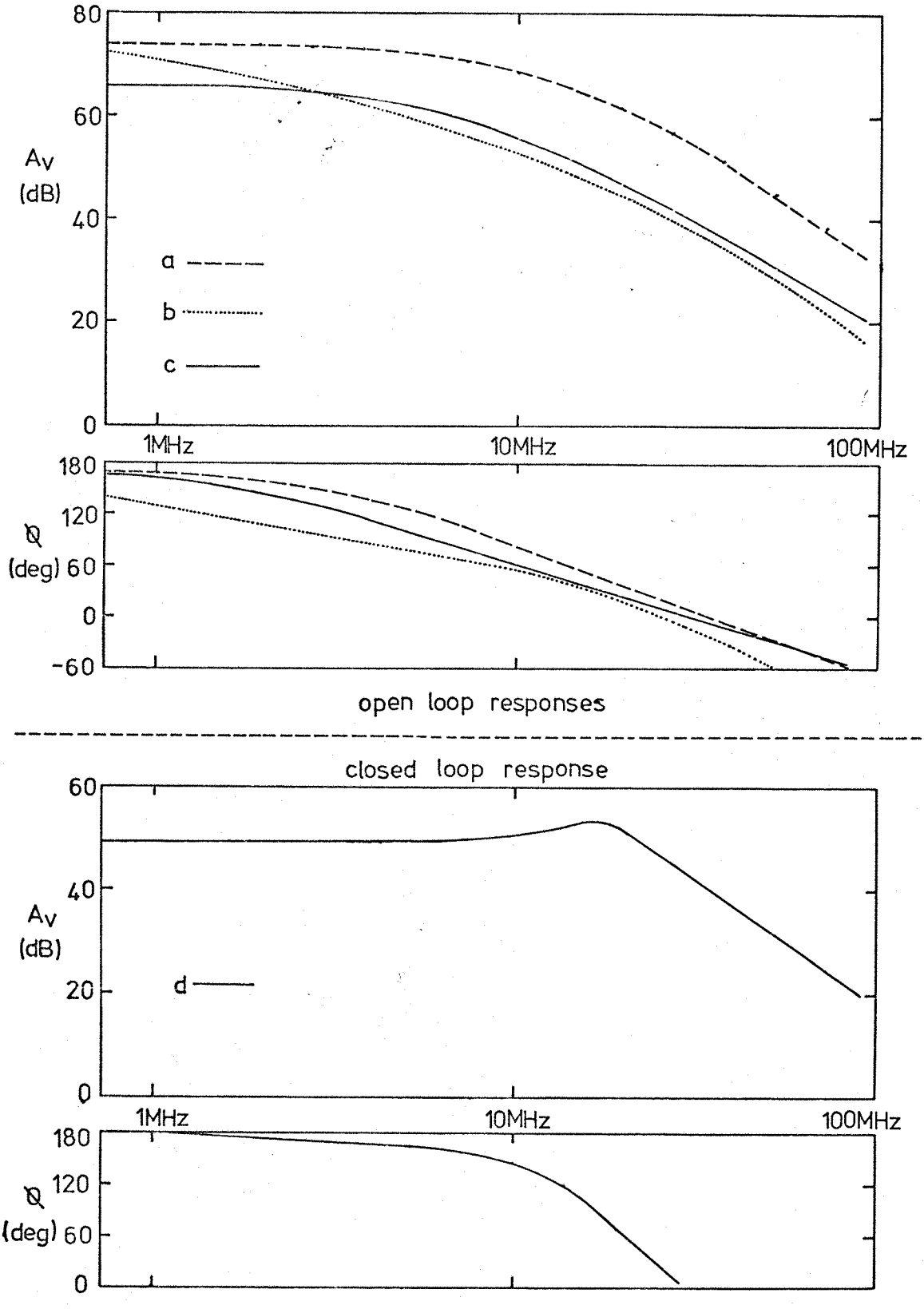


Figure 18. Bode plots of various amplifier designs

reducing the gain in the neighbourhood of $\varphi \rightarrow 0$. It has merely shifted the responses further down the frequency axis.

Stability was finally achieved by running the second stage at 0.1mA rather than 1mA. This in fact also helps to keep the power consumption down. Now R3 = 100 and R4 = 6.8K from the voltage gain requirements. The dominant time constant is now set by R4 and C_π in the third transistor. In increasing R4 by an order of magnitude, this time constant is reduced and the amplifier is stabilized. The frequency response is shown in figure 18(c). Note that the voltage gain is now 39dB (7dB down from 46dB) when the net phase shift is zero at 32MHz. This implies that signal regeneration cannot occur around the loop for any amount of negative feedback between the closed loop gains of 46dB and 60dB. Hence the amplifier is stable. When the open loop gain is in fact 46dB, the phase shift is 22°. This is quite small and causes slight peaking in the closed loop response of 46dB. This is shown in figure 18(d).

5.3 CIRCUIT BIASING

The circuit shown in figure 17(b) would not work as it stands because no base current is supplied to Q1. The standard method of supplying base current from a potential divider between V_{cc} and ground cannot be used with a high gain DC amplifier because any small DC drifts in the base voltage of Q1 are immediately amplified throughout the three stages and the output voltage at the collector of Q3 will switch to either V_{cc} or zero. Clearly, some control over the base drive of Q1 is required.

Figure 17(c) shows a way around this problem. R7 and R8 tap a portion of the current from the output of the amplifier and

feed this back negatively to Q1. Now any drifts in the base current of Q1 are immediately sensed at the output and fed back accordingly to compensate. The capacitor C2 is required to prevent signal feedback occuring around this loop and hence destroying the gain. The time constant set by R7 and C2 must be small enough to ensure that all low frequencies of interest are shorted to ground via C2 and not fed back to the input. This means that R7 and C2 need to be large. Excessively large values of R7 are not possible, however, because a large voltage drop across R7 will drive Q3 towards cutoff
(The current through R7 is the same irrespective of what value R7 takes). Also, large values of C2 are bulky and expensive.

Figure 19 shows the proposed amplifier with two modifications. The base current for Q1 is now supplied via the current mirror formed from Q5 and Q6. If the V_{be} matching of these transistors is good, then their collector currents will be equal. This means that the base current of Q1 is equal in magnitude to the collector current in Q4 which is beta times bigger than the current drawn from the output via R7. R7 can now be safely increased to 100K ohms without interfering with the collector current of Q3. The second change is that C2 is now connected to the collector of Q8 rather than to ground. Q5 and Q7 form a current mirror supplying Q8 with the same base current as Q1 so that the collector current in Q8 is almost equal to that in Q1. This stage provides Miller magnification of C2, thus improving the low frequency response further. The value of C2 will be magnified $(1 + g_m R_L)$ times. This turns out to be about 34 times.

The circuit was constructed on breadboard from discrete components using BC182L transistors for all NPN types and BC214L

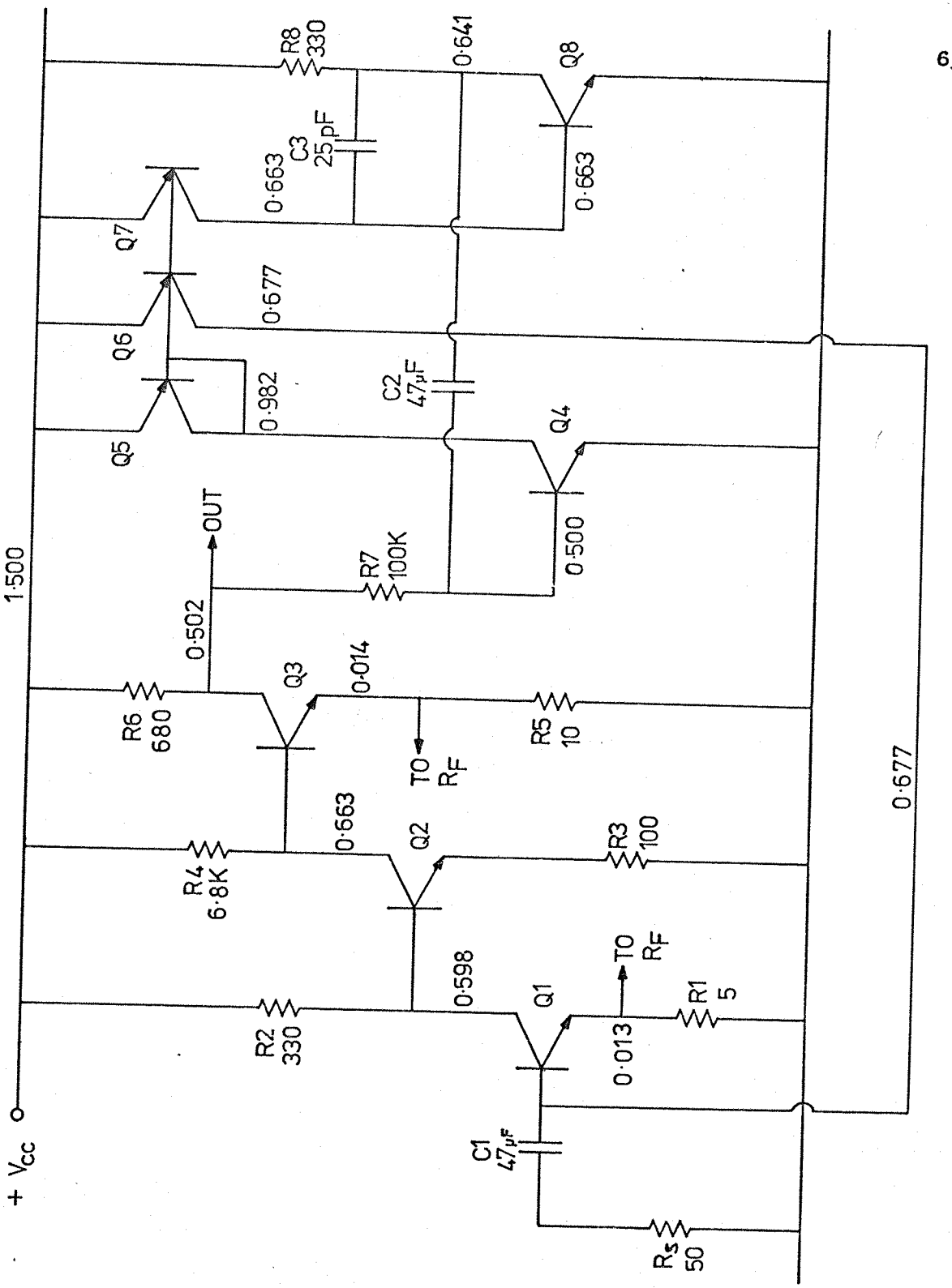


Figure 19. Complete design of low noise amplifier with DC voltages from discrete breadboard model

for all PNP types. The measured DC voltages at the nodes in the circuit are also shown in figure 19. In the experimental circuit, a small capacitor C3 had to be connected across the base-collector junction of Q8 to reduce the f_T of this transistor and avoid oscillation of the Miller stage. It was found that 25pF was adequate for this.

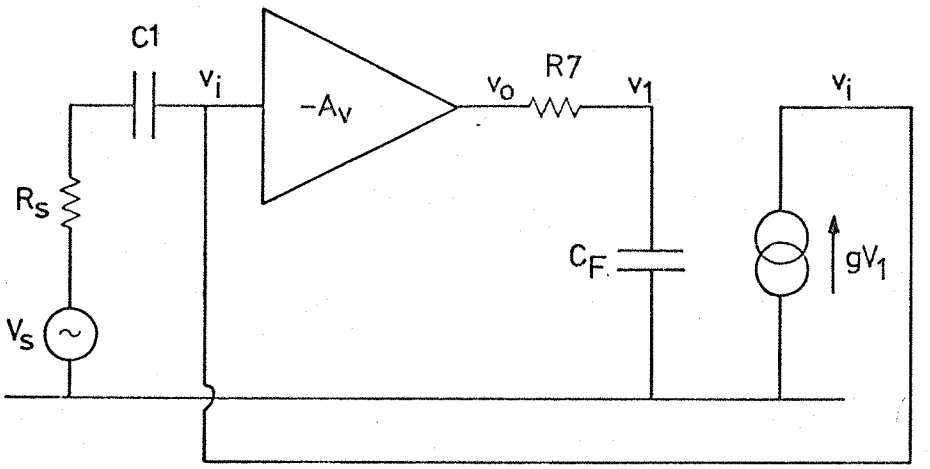
Gain control is achieved by applying overall feedback for AC signals around the three stages. A resistor is connected between the emitters of Q1 and Q3 thus providing series current feedback. In practice, a feedback resistor of value 10 ohms brings the total gain down to 46dB.

5.4 LOW FREQUENCY RESPONSE

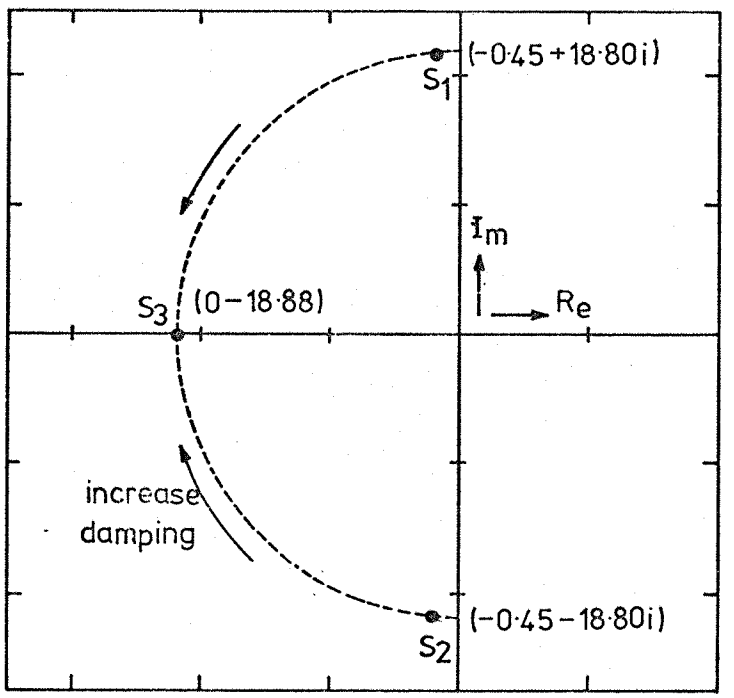
The behaviour of the low frequency response of the amplifier may be examined by evaluating a transfer function for the equivalent circuit. The relevant parts of this equivalent circuit are shown in figure 20(a). Note that C_F is the Miller magnified value of C2 and hence takes a value of approximately 1600μF. The current generator gV_1 represents all transistor action feeding current back to the base from the output through Q4, Q5 and Q6. The basic amplifier is considered to be inverting and have an infinite input impedance. In fact, at low frequencies, the phase shift through the amplifier is almost exactly 180°. By inspection of figure 20(a),

$$\frac{V_s - V_i}{R_s + 1/sC_1} = -gV_1 = -gV_o\left[\frac{1/sC_F}{R_7 + 1/sC_F}\right] \qquad (72)$$

(73)



(a) Equivalent circuit



(b) Pole representation on s-plane

Figure 20. Low frequency response

However,

$$V_i = V_o/A_v \tag{74}$$

Direct substitution of equation 74 into equation 72 leads to

$$A_v' = \frac{A_v sC_1(1+sC_FR_7)}{s^2(C_1C_FR_7)+s(C_1+A_vgC_1R_s)+A_vg} \tag{75}$$

The poles of the amplifier will then be given by setting the denominator equal to zero, and solving the resulting quadratic equation:

$$s^2(C_1C_FR_7)+s(C_1+A_vgC_1R_s)+A_vg = 0 \tag{76}$$

When the real circuit values are inserted into equation 76, the poles can be located and represented in an Argand diagram as shown by S_1 and S_2 in figure 20(b). Equation 75, giving the transfer function of the amplifier at low frequencies, can be seen to be that of a second order high pass filter. The poles of such a filter are complex conjugates and lie on a semicircle in the real-imaginary s-plane[11]. They are characteristic of damped oscillations in the frequency response, and manifest themselves by peaking the frequency response near DC, as shown in figure 21(a).

This curve was in fact obtained by the linear analysis on computer as before. In practical terms, it means that when the amplifier is switched on, the signal moves up and down for a short while at this low value of frequency (about 1Hz). The condition is commonly known as BOUNCE. Furthermore, when the amplifier is used in video applications, the picture can brighten and darken sinusoidally at the frequency peak. If these low frequency oscillations are suppressed by some method of damping, the response will be very much improved.

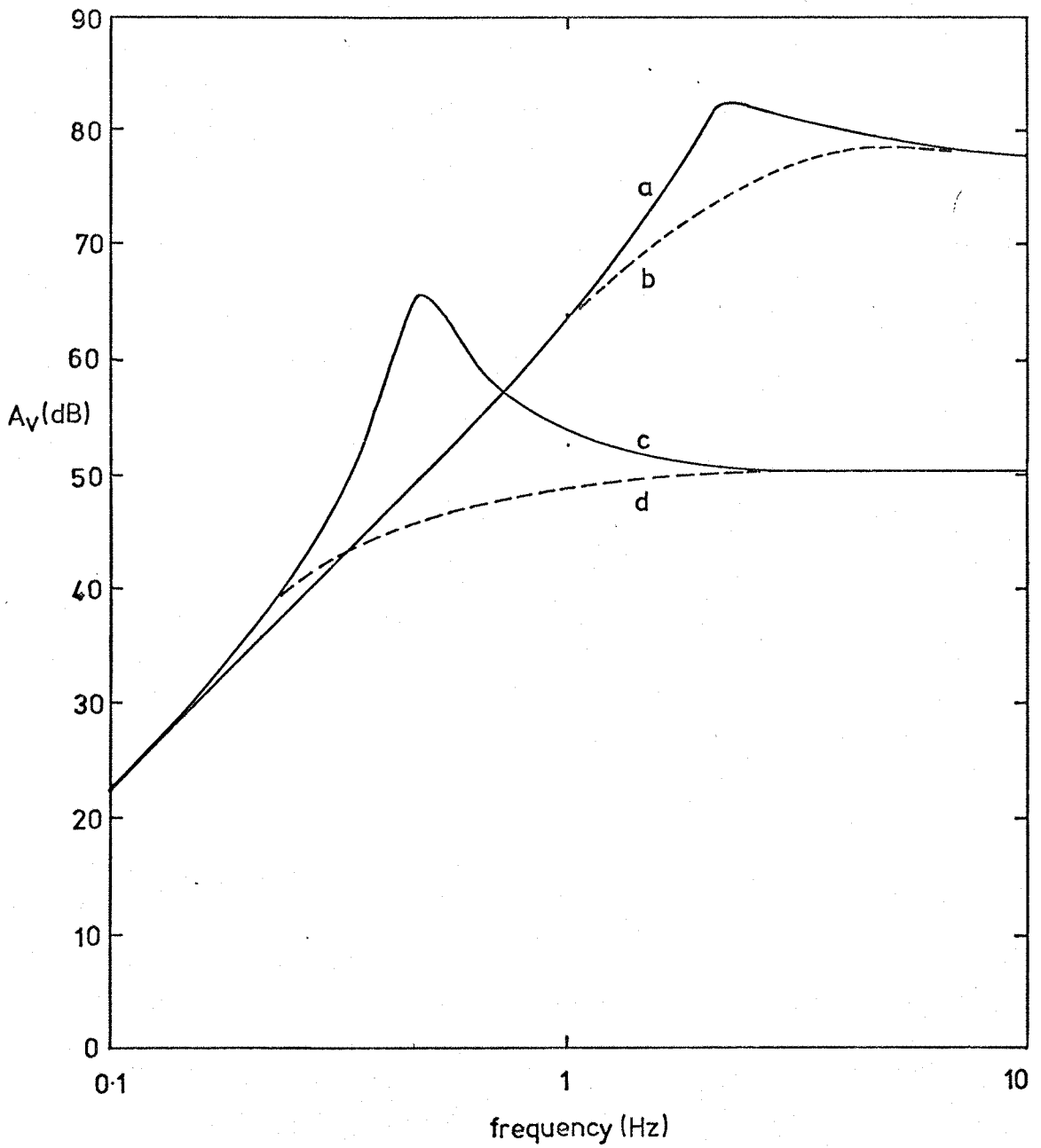


Figure 21. Low frequency response

Reducing the low frequency peaking is equivalent to moving the natural poles of the system further down the semi-circle to meet one another, because the imaginary or oscillatory component of the poles then becomes negligible. One way of acheiving this situation without altering existing component values is to introduce a damping resistor R_d in series with C_F. The expression for the gain transfer function now becomes

$$A_v' = \frac{A_v sC_1(sC_FR_7 + sC_FR_d + 1)}{s^2(C_FC_1R_7 + C_FC_1R_d + A_vgC_FC_1R_sR_d) + s(C_1 + A_vgR_sC_1 + \ldots}$$

$$\ldots + A_vgC_FR_d) + A_vg \qquad (77)$$

If the poles are to contain no imaginary component, then we require a zero square root in the solution of the denominator of equation 77. Specifically,

$$R_d^2(A_vgC_F)^2 - R_d(2A_vgC_1C_F + 2A_v^2g^2C_1C_FR_s) + \ldots$$

$$\ldots + (C_1^2 + A_v^2g^2R_s^2C_1^2 + 2A_vgR_sC_1^2 - 4A_vgC_1C_FR_7) = 0 \qquad (78)$$

This is a quadratic equation in R_d with solutions $R_d = 70.8$ or -67.7. The negative solution has no meaning. When this value is substituted back into the denominator of equation 71, the poles are found to be coincident on the negative real axis as shown by S_3 in figure 20(b). The amplifier low frequency response is now critically damped, and in practice, this can be achieved by connecting a resistor of approximate value $34 \times 71 \approx 2K$ ohms in series with C_2 because of the Miller effect. The resulting change in low frequency response as a result is shown in figure 21(b). When the amplifier is used in the closed loop mode with a gain of approximately 46dB, the peaking is found to be even more pronounced as shown in figure 21(c). In this case, it can be

shown that a resistor of approximately 9Kohms is required to critically damp the response. This is shown in figure 21(d).

5.5 CIRCUIT LAYOUT OF THE INTEGRATED AMPLIFIER

The layout of the low noise amplifier in integrated circuit form is shown in figure 22. Note that the input transistor is large and interdigitated. The base spreading resistance should be appreciably lower than that of T3 shown in figure 15(a); the perimeter to surface ratio of the base-emitter junction is almost an order of magnitude greater. R2, R4 and R6 are all p-type diffused resistors produced simultaneously with the transistor bases, and resistors R1, R3 and R5 are all emitter (n^+) diffused resistors. Ideally, the n^+ resistors should be surrounded by p-type land, but since their value is so low, the effect of the surrounding epitaxial land can be ignored. R7 is a pinch resistor formed by an n^+ diffusion on top of a p-type diffused resistor. Q2, Q3, Q4 and Q8 are all minimum geometry NPN transistors, and Q5, Q6 and Q7 are minimum geometry lateral PNP transistors with an enclosed emitter structure.

Aluminium pads are larger than the minimum geometry limit in an effort to facilitate bonding, and these allow access to V_{cc}, input, output, the emitters of Q1 and Q3 for feedback control, C2, C3 (and hence R_d) and earth. Note that C1, C2, R_d and C3 (if required) are external components. A test resistor and NPN transistor are also included on the chip. The isolation between devices is connected to earth to keep it at the most negative potential in the circuit. Similarly, resistor 'land' areas are connected to the highest potential end of the resistor to prevent forward diode action. Buried layers (not shown) are incorporated

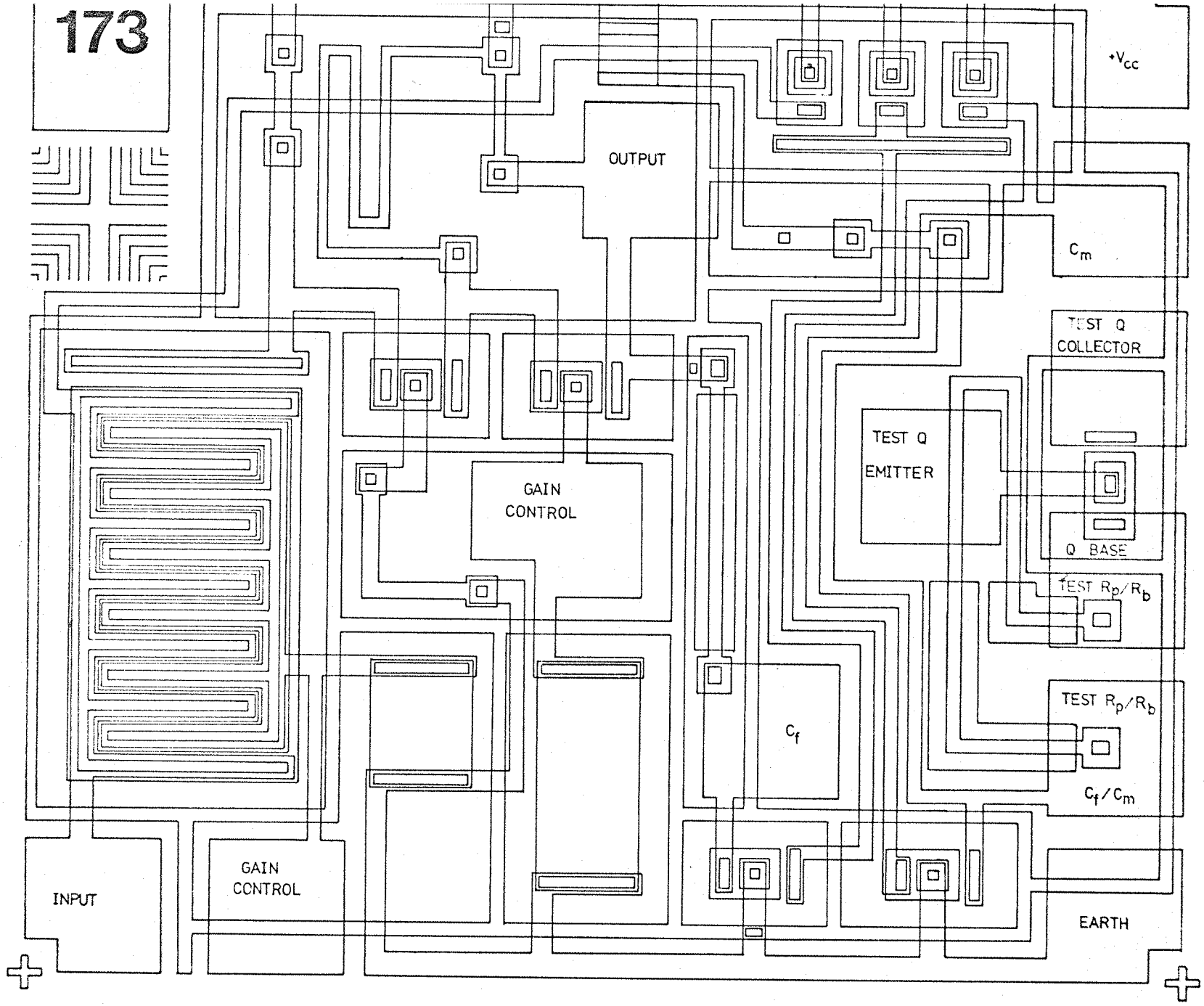


Figure 22

LOW NOISE AMPLIFIER

under all transistors to minimise collector series resistance.

5.6 EXPERIMENTAL MEASUREMENTS AND RESULTS

Experimental data were collected from a discrete breadboard construction of the circuit and from the final integrated circuit itself. The breadboard circuit was built using BC182L transistors for all NPN types and BC214L transistors for all PNP types. The frequency response and noise figure of this amplifier was then measured. In measuring the low frequency response, the usual method of signal generator with oscilloscope was not used because it is difficult to make such a measurement with any accuracy in the 1Hz region. Instead, a step voltage was applied to the input, and the resulting exponentially decaying sinusoid recorded on moving paper chart at the output. It can be shown that this output is of the form

$$f(t) = V_o \cos\omega_o t . e^{-kt} \qquad (79)$$

where ω_o is the frequency of the oscillation and k is the decay constant. This output can now be converted to the frequency domain by means of a Laplace transformation and the resulting expression for the voltage gain can be obtained in the form

$$A_V(\omega) = \frac{s(s+k)}{(s+k)^2 + \omega_o^2} \qquad (80)$$

where s is defined by equation 73. A plot of this equation using the measured values for ω_o and k then exhibits the low frequency peaking effect already mentioned.

The noise figure of the discrete amplifier was measured as a function of R_s (using the two temperature method) with various numbers of BC182L transistors wired in parallel for the input

stage. This is a well known technique for decreasing the effective r_x in the first stage[14]. In measuring the noise figure, input stages comprising of one BC182L, five BC182L and ten BC182L were considered. The freq.band f the noise measurements was 19-21kHz. The entire frequency response is shown in figure 23. Note that the solid lines show the evaluated response by computer analysis for the open and closed loop cases. Measurements are shown as a series of data points scattered around these lines. The measured noise figures are shown in figure 24. Note that the required noise performance of less than 3dB at a source impedance of 50ohms is attained when ten BC182L transistors are wired in parallel to act as the first stage.

One of the main difficulties throughout the course of this project has been the inability to reproduce a bipolar processing schedule with any accuracy. In particular, time has not allowed a slice of the low noise amplifiers to be processed exactly like the test transistors and resistors that were used for the measurement of the device parameters. The main reasons for this seem to be due to shortcomings in the epitaxial process and the emitter drive-in process. However, one slice of amplifiers was processed that had four working chips and the frequency response of these were measured using probes. The results are also shown in figure 23. Unfortunately, the four working chips were inadvertantly destroyed during bonding and so it was impossible to measure the noise figure for the integrated amplifier. Nevertheless, a great deal of knowledge of the noise behaviour can be obtained by measuring the base spreading resistance of the input transistor. The parameter was measured for several input transistors on the slice and the mean found to be 12 ohms with a small standard deviation. This figure is in fact less than the

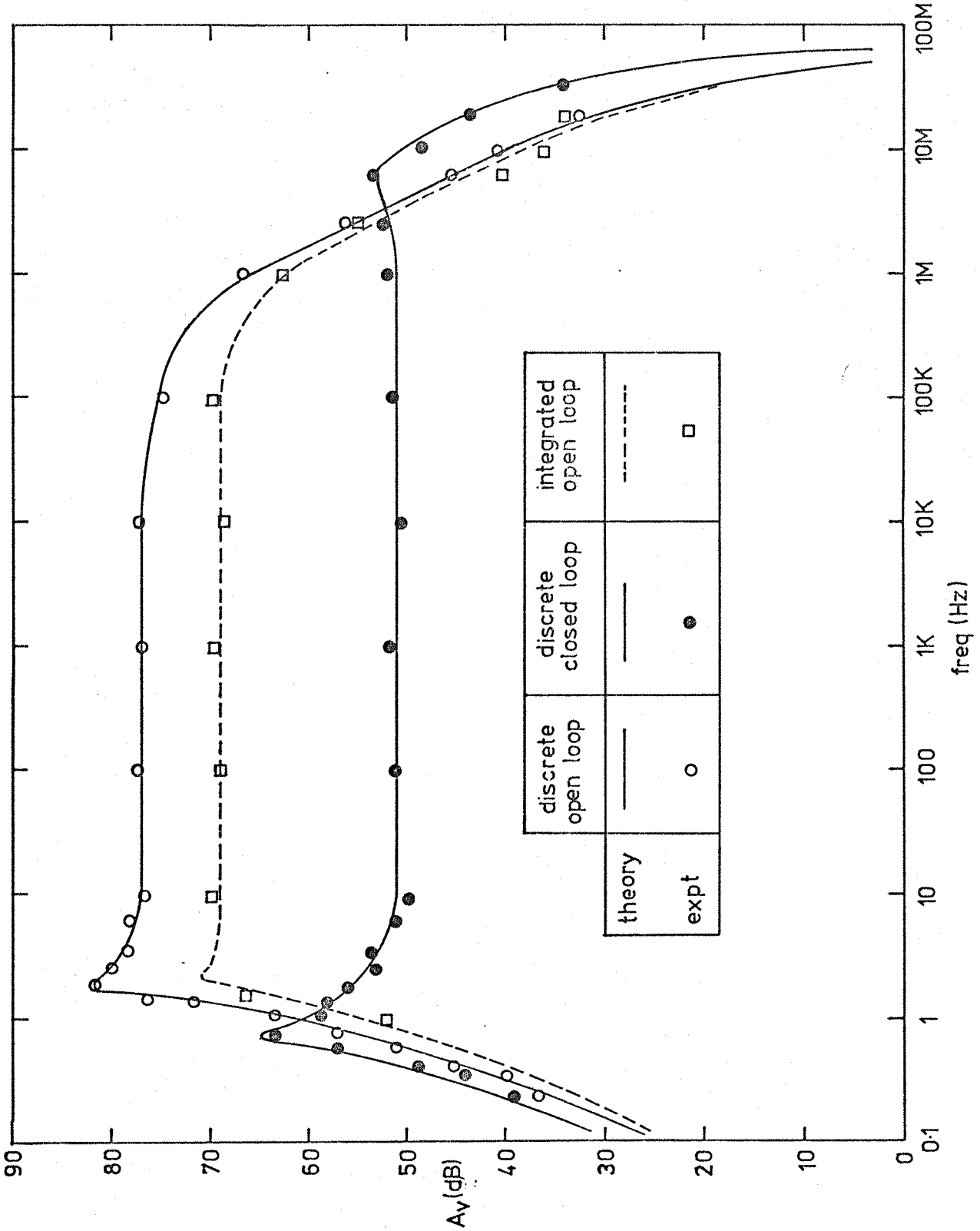


Figure 23. Experimental and theoretical frequency response of the low noise amplifier

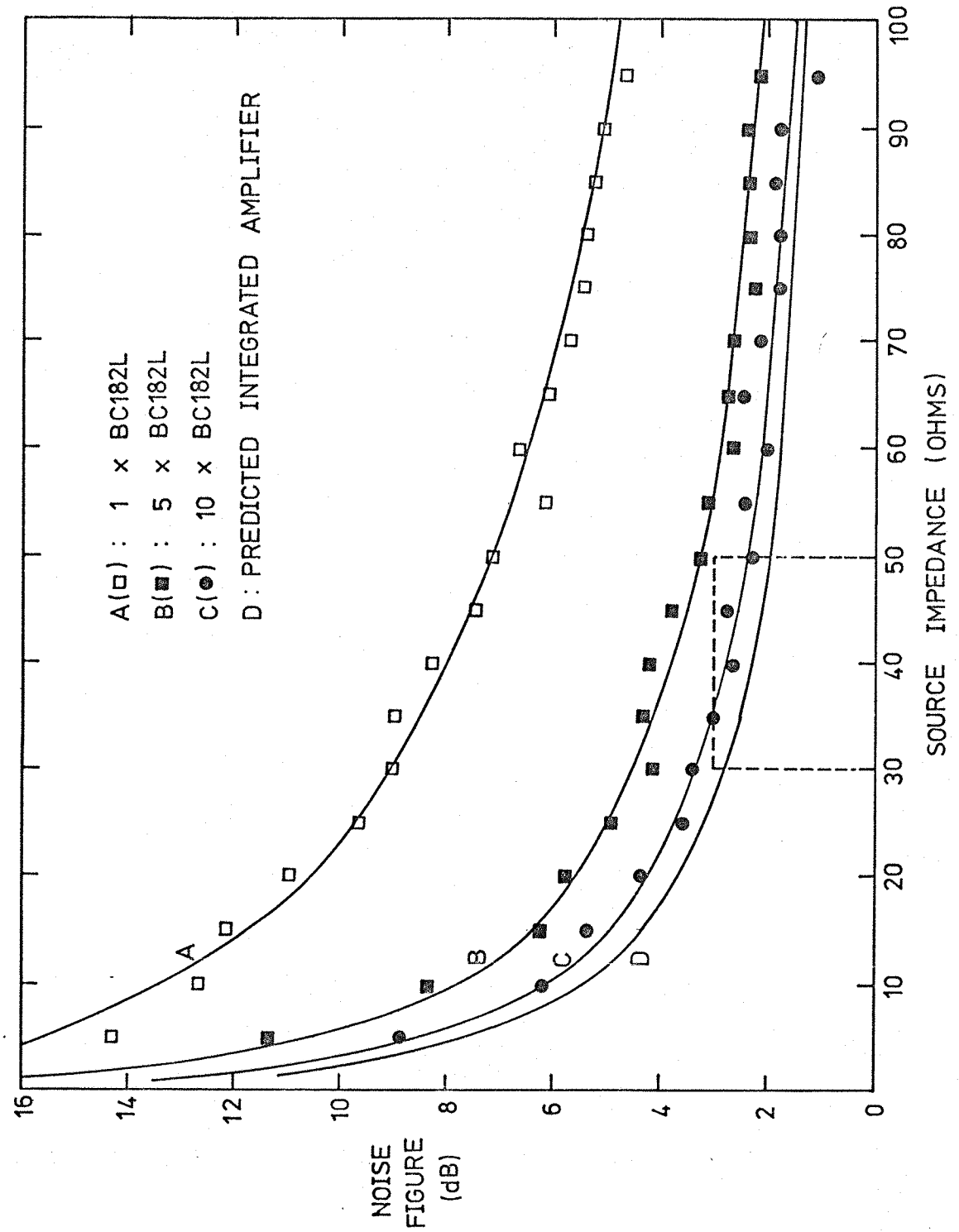


Figure 24. Measured noise figures for discrete amplifier and predicted noise figure for integrated amplifier

effective base spreading resistance for ten BC182L transistors wired in parallel, which turns out to be approximately 18ohms. For this reason, it is expected that the integrated amplifiers meet the required noise specification when processed correctly.

CHAPTER 6

DISCUSSION AND CONCLUSION

An exact expression for the noise figure of the single sided input, single sided output mode differential amplifier and approximate expressions for all four possible modes have been obtained. A comparison of the noise performance of a particular mode with that of the common emitter amplifier has shown that the voltage noise is double for all four modes (ie. noise figure is 3dB greater in low source impedance region), but the current noise is the same except in the case of the differential input, differential output mode amplifier. Here, the current noise is half that of the common emitter (ie. noise figure is 3dB less in the high source impedance region). The effect on noise figure of the differential amplifier for the case of a transistor as current source and with an active load was also considered.

A low noise amplifier was designed for specific use with values of source impedance in the 30-50 ohm range. The long tailed pair as the standard input configuration was rejected on the grounds of its higher voltage noise and lower voltage gain. When the input stage was constructed with ten BC182L transistors in parallel (each having $r_x \simeq 180$ ohms) running at a total collector current of approximately 2.5mA, the noise figure measured with a 50 ohm source resistor was 2.4dB. Measurements on an interdigitated transistor showed that this had a value of $r_x \simeq 12$ ohms and consequently, the estimated noise figure for the integrated amplifier used with a source impedance of 50 ohms is approximately 2dB.

At this stage, it is worth considering 1/f noise. The basic properties of 1/f noise have already been outlined in 1.3 but, as

yet, no mention has been made of the effects on the noise performance of the differential amplifier. For an amplifier with a good low frequency response, the effect of the noise can be very important, especially if little care is taken in the processing of the devices. A low temperature annealing stage was introduced into the standard bipolar process at Southampton University in an attempt to reduce the number of surface states. Measurements on the low frequency noise figures of NPN transistors appear to have been improved by this step.

In measuring the noise performance of the long tailed pair, narrow bandwidths centred at high frequencies were selected. This was to ensure that the measured noise arose purely from shot and thermal sources. If the noise figures had been measured at low frequencies (well below 1kHz) they would have had higher values due to the prescence of 1/f noise as shown in equation 6. However, the table of ratios in 3.2 would still be valid since only a comparison between identical transistors is drawn. Equation 6 showed that 1/f noise can be modelled like base shot noise with a frequency dependant current generator of magnitude i_{nf} connected across the input impedance, r_{π}, of the device. Hence, all of the long tailed pair theory previously described could easily be modified to accomodate 1/f noise by adding two extra contributions from i_{nf} in Q1 and i_{nf} in Q2. The actual terms would be identical to the base shot terms but with i_{nf} replacing i_{nb}.

The measurements of the noise figure of the low noise amplifier were shown in figure 24. If the noise figure of a transistor with identical base spreading resistance and a series feedback resistor in the emitter lead of 5 ohms were to be measured carefully, the result would be slightly lower than that

shown in figure 24. This is because some additional noise from the current mirror is being fed to the base of the input transistor. An exact theoretical evaluation of the noise figure of the amplifier would have to take account of this noisy output current from the mirror.

The gain of the three stage amplifier has been shown to be easily variable between 46dB and 60dB. In the computer linear analysis for the frequency response of the circuit, certain values of base-collector feedback capacitance, C_μ, were assumed. These values were taken from measurements made on our own integrated transistors. The measurements were made at a V_{ce} of 1V which means that the potential of the collector was approximately 0.3V above that of the base. The situation is slightly artificial in the sense that the quiescent points of the devices in the actual working amplifier were such that the collector voltages were just below those of the bases. This means that the collector-base diodes for each of the devices are forward biased and the associated capacitance of the junction is considerably higher. Hence more phase shift is introduced throughout the three stages and care has to be taken to ensure that the amplifier does not oscillate at a slightly higher value of closed loop gain than anticipated.

SUGGESTIONS FOR FUTURE WORK:

1. Decreasing the output impedance of the low noise amplifier. An inspection of the final stage of the amplifier will show that the output impedance is approximately that of the load resistor, namely 680 ohms. This, of course, is much higher than the demanding value of 1 ohm quoted in the original specification. One way to decrease output impedance further

is to add an emitter follower stage after the three gain stages. This will bring the output impedance down to approximately $1/g_m$ ohms where g_m is the transconductance of the emitter follower stage. For reasonable current levels, an emitter follower could be expected to decrease the output impedance to somewhere in the region of 50 ohms, and voltage feedback could be applied to lower this value even further.

2. 1/f noise properties.

   As has been already mentioned, 1/f noise could appreciably affect the noise performance of a wide-band amplifier at low frequencies. Experiments investigating the low frequency noise behaviour of our own devices would be very useful. Some further control of bipolar processing with respect to 1/f noise may be possible.

3. Temperature and power supply variation.

   With input signals at the microvolt level, small changes in power supply and ambient temperature may affect the voltage gain and hence performance to an appreciable extent. Further experimental investigation of this effect could usefully be carried out.

APPENDIX : The relation between noise figure and noise equivalent generators for an amplifier.

The equivalent circuit is shown in figure 25. Transforming the Norton current source i_n into an equivalent voltage source $i_n R_s$ leads to the equivalent circuit of figure 25(b). Summing the noise contributions at the output gives

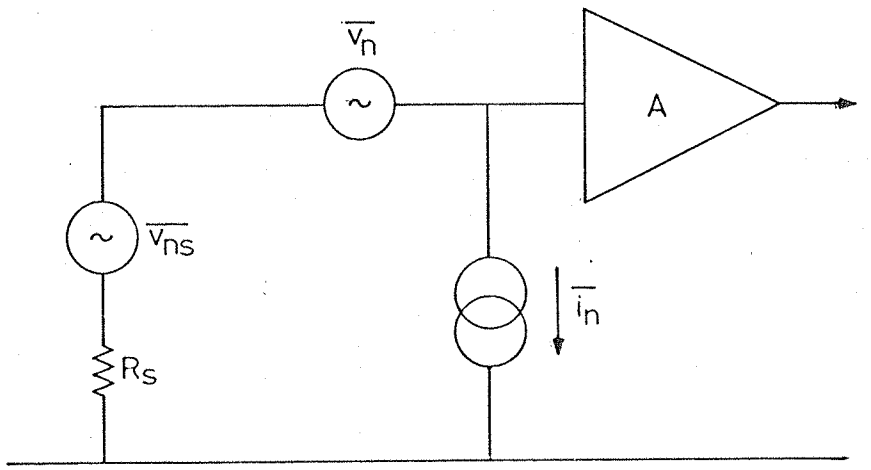
$$F = \frac{\overline{Av_{ns}^2} + \overline{Av_n^2} + \overline{Ai_n^2}R_s^2}{\overline{Av_{ns}^2}} \qquad (81)$$

which leads to

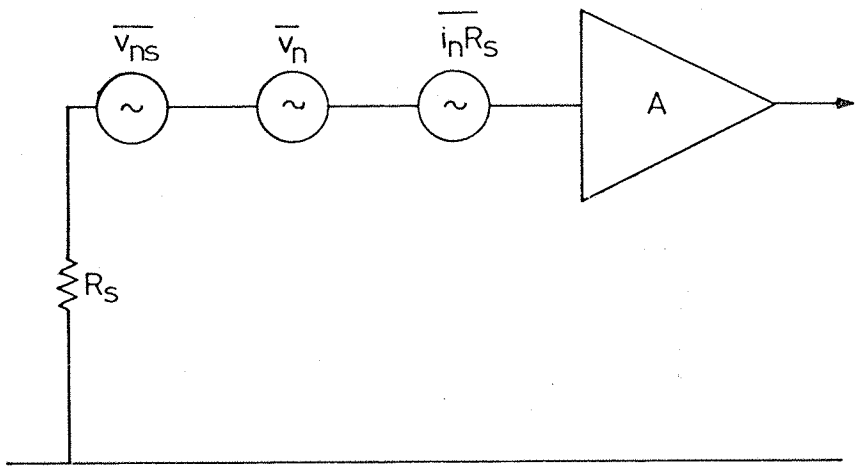
$$F = 1 + \frac{\overline{v_n^2} + \overline{i_n^2}R_s^2}{\overline{v_{ns}^2}} \qquad (82)$$

and inserting the thermal noise of the source, we have

$$F = 1 + \frac{\overline{v_n^2} + \overline{i_n^2}R_s^2}{4kTR_s\Delta f} \qquad (83)$$



(a) Equivalent circuit



(b) Thevenin equivalent

Figure 25. Relation between noise figure and equivalent noise generators.

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