University of Southampton

University of Southampton Research Repository

Copyright © and Moral Rights for this thesis and, where applicable, any accompanying data are retained by the author and/or other copyright owners. A copy can be downloaded for personal non-commercial research or study, without prior permission or charge. This thesis and the accompanying data cannot be reproduced or quoted extensively from without first obtaining permission in writing from the copyright holder/s. The content of the thesis and accompanying research data (where applicable) must not be changed in any way or sold commercially in any format or medium without the formal permission of the copyright holder/s.

When referring to this thesis and any accompanying data, full bibliographic details must be given, e.g.

Thesis: Author (Year of Submission) "Full thesis title", University of Southampton, name of the University Faculty or School or Department, PhD Thesis, pagination.

Data: Author (Year) Title. URI [dataset]

UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND APPLIED SCIENCE

ELECTRONICS DEPARTMENT

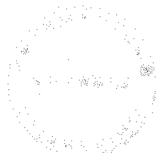
OPTICAL CHARACTERISTICS OF PN JUNCTIONS AND MOS TRANSISTORS WITH APPLICATIONS TO INTEGRATED CIRCUIT MEASUREMENTS

A thesis submitted for the degree of

Doctor of Philosophy of the University of Southampton

by

Pearson Vincent Chitanda Luhanga



- August 1981 -

SOUTHAMPTON
LIBRARY
UNIVERSITY

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING AND APPLIED SCIENCE

Doctor of Philosophy

OPTICAL CHARACTERISTICS OF PN JUNCTIONS AND MOS TRANSISTORS WITH APPLICATIONS TO INTEGRATED CIRCUIT MEASUREMENTS

by Pearson Vincent Chitanda Luhanga

The photocurrent generation characteristics of pn junctions and MOS transistors are studied with a view to applying these devices to input data optically direct into the internal circuity of integrated circuits, by a finely focussed laser beam. This permits simple testing schemes for fault detection; and can make large savings in the time taken for diagnostic testing of IC's. A review of the spectral characteristics of the photocurrents of both the diffused pn junction and the MOS (induced) pn junction are presented and compared.

It is also shown that the optical input of data can be employed to measure propagation delay times associated with each stage in an MOS dynamic shift-register circuit; which leads to a better understanding of the internal operation of the circuit.

A novel application of the MOS phototransistor is also presented. It is shown that amplification of the photocurrent generated can be produced by including a large resistance between the substrate and the source. A simple model which adequately describes the mechanisms involved is presented. Results of calculations of both the amplification factor and the response speed, based on this model show good agreement with experiment.

This configuration can be used to produce from a moderate laser beam power, the large photocurrents needed to switch some digital IC families (e.g. CMOS).

Silicon-gate devices are very suitable as MOS phototransistors because the gate electrode transmits visible radiation. This property, coupled with photocurrent amplification where necessary, makes the laser probe method of data input in conjunction with standard test equipment a useful method for testing of present day MOS integrated circuits.

ACKNOWLEDGEMENTS

I would like to thank my supervisor, Mr. J. G. Smith, for his continuing support and encouragement and other members of the Microelectronics Group, in particular Professor H. A. Kemhadjian, Dr. A. G. R. Evans and Dr. A. Brunnschweiler; and also Professor D. J. Roulston (on visit from the University of Waterloo, Ontario, Canada), for helpful discussions and comments throughout this work. It is also a pleasure to acknowledge the invaluable assistance of my colleagues Mr. D. W. Eddowes and Mr. C. M. Dyson at all levels of this work; and the help I obtained from the staff of the Microelectronics Group processing laboratory.

I am also very grateful for the financial support from the Association of Commonwealth Universities.

Finally, I would also like to thank Miss S. Makin and Miss J. Sutton for typing this thesis.

CONTENTS

		Page
CHAPTER ONE	INTRODUCTION	1
CHAPTER TWO	OPTICAL CHARACTERISTICS OF PN JUNCTION DIODES	3
CHAPTER THREE	APPLICATION OF THE PN JUNCTION PHOTODIODE IN LASER TESTING OF DIGITAL IC'S	7
3.1	Introduction	7
3.2	Optical Injection of Information	8
3.3	The Laser Probe	11
3.4	Laser Testing of a Digital Integrated Circuit	12
3.5	Conclusions	13
CHAPTER FOUR	MEASUREMENT OF DELAY TIMES ON AN MOS SHIFT REGISTER CIRCUIT	14
4.1	Introduction	14
4.2	The Design of the Test Circuit	14
4.3	Operation of the Shift Register Circuit	16
4.3.1	Inverter switching times	17
4.3.1(a)	The fall time : t'_F	20
4.3.1(b)	The rise time : t'_R	22
4.3.2	Propagation delay and maximum clock-rate	24
4.3.2(a)	Source potentials V_n, and turn-on voltages V_{Tn}, of the driver transistors	26
4.3.2(b)	Predicted delay-times for each inverter	27
4.3.2(c)	The maximum clock-rate	28
4.4	Measurement of Delay Times	29
4.4.1	Measurement of the maximum clock-rate	31
4.5	Discussion of Results	32
4.6	Conclusions	34

CHAPTER FIVE THEORY OF THE OPTICAL CHARACTERISTICS OF MOS TRANSISTORS 35

5.1 Optical Characteristics of the MOS Diode 36

5.1.1 Optical transmission through the gate layers of a polysilicon-gate MOS diode 39

5.1.2 Spectral characteristics of the photocurrent of the polysilicon gate MOS diode 40

5.2 Model of the MOS Transistor Photocurrents 41

5.3 Photocurrent Gain in MOS Transistors 43

5.4 The Dependence of the Photocurrent-Gain on the Substrate Resistance 46

5.5 Switching Speed of the Photocurrent Amplifier 47

5.6 Discussions and Conclusions 50

CHAPTER SIX MEASUREMENT OF THE OPTICAL CHARACTERISTICS OF A P-MOS TRANSISTOR 53

6.1 The Design of the MOS Phototransistor 53

6.2 Spectral Characteristics of the Photocurrents 54

6.3 Photocurrent Amplification 56

6.3.1 Dependence of the photocurrent-gain on the substrate resistance 57

6.3.2 Dependence of the photocurrent-gain on the primary photocurrent 59

6.4 Switching Speed 61

6.5 Discussion of the Results 63

6.6 Conclusions 64

CHAPTER SEVEN CONCLUDING REMARKS 65

APPENDIX 1 : MOS THEORY 68

A1.1 Theory of the Space Charge and the Electric Field at the Semiconductor Surface 68

A1.2 Theory of the MOS Transistor 73

A1.3 The Approximate MOS Transistor Theory : (The Text-book Approach) 81

APPENDIX A2 : OPTICAL TRANSMISSION THROUGH THE GATE LAYERS OF A POLYSILICON GATE MOS DIODE 85

APPENDIX A3 : OUTLINE OF THE PROCESSING OF THE MOS-PHOTOTRANSISTORS 88

REFERENCES 90

CHAPTER ONE

INTRODUCTION

The optical characteristics of pn junctions and MOS transitors are of interest in connection with the application of these structures as image sensors, solar cells, and as optically activated switches in the laser testing of integrated circuits[1.1,1.2]. In this thesis we are interested in the application of the pn junction and the MOS transistor as photodetectors for use in the testing of MOS digital IC's, using a laser to input data.

In Chapter 2 of this thesis we review the photocurrent generation characteristics of the diffused pn junction, in particular the spectral characteristic of the photocurrent and its dependence on the diffused junction depth. In Chapter 3, we introduce as an application of the pn junction photodetector: the optical injection of data into the internal circuitry of the IC, via a focussed laser beam (the laser probe), in the laser testing of an MOS digital circuit. This chapter also briefly describes the laser probe[1.1,1.2]; and also introduces a typical (diagnostic) test that can be performed on an IC in a much simpler fashion using the laser probe, than without it.

Chapter 4 presents the results of experiments performed on an MOS serial-input, serial-output, shift-register circuit, using the laser probe. The experiments were aimed at measuring the propagation delay times from each internal node to the output of the circuit. In these experiments, the photocurrents were generated by directing the laser beam onto pn junctions in the circuitry.

The beginning of Chapter 5 reviews the optical characteristics of the MOS diode (i.e. the pn junction formed between the induced

inversion layer at the surface/oxide interface and the bulk semiconductor) as used in CCD imagers and Metal Insulator Semiconductor (MIS) solar cells. In particular, we compare the spectral characteristics of the photocurrent to those of the diffused pn junction.

A novel application of the MOS transistor is introduced in this chapter. It is found that by operating the transistor as a photodetector when the substrate terminal is connected to ground via a large resistance ($\sim$ 100 kΩ), the transistor will provide photocurrent amplification. A model is developed in this chapter to explain this characteristic. The MOS transistor theory (this is presented in Appendix A1) used in the development of this model, is based on the double integral model of Pao and Sah[1.3] and the subsequent refinements by Baccarani et al[1.4] and Van de Wiele[1.5]. This transistor model includes both the drift and diffusion current components of the channel current.

Chapter 6 presents the results of experiments performed on p-MOS transistors to test the predictions of the theory developed in Chapter 5; and the results show very good agreement between the theory and the experiment.

A summary of the results is presented in Chapter 7, together with a definition of areas where it is hoped that further work would be profitable.

CHAPTER TWO

OPTICAL CHARACTERISTICS OF PN JUNCTION DIODES

The pn junction is used extensively as a photodetector (e.g. in light measuring instruments, or as a solar-cell). A knowledge of the characteristics of the diode photocurrent is therefore necessary to understand the operation of the pn junction photodetector.

The generation by illumination of a current in a pn junction has been studied by several authors; the treatment presented here follows the work of Terman[2.1].

Consider Figure 2.1(a) which is a one-dimensional representation of a pn junction under illumination. The illumination produces a photocurrent, I_{ph}, the size of which is directly proportional to the power of the incident light beam according to the formula[2.2]:

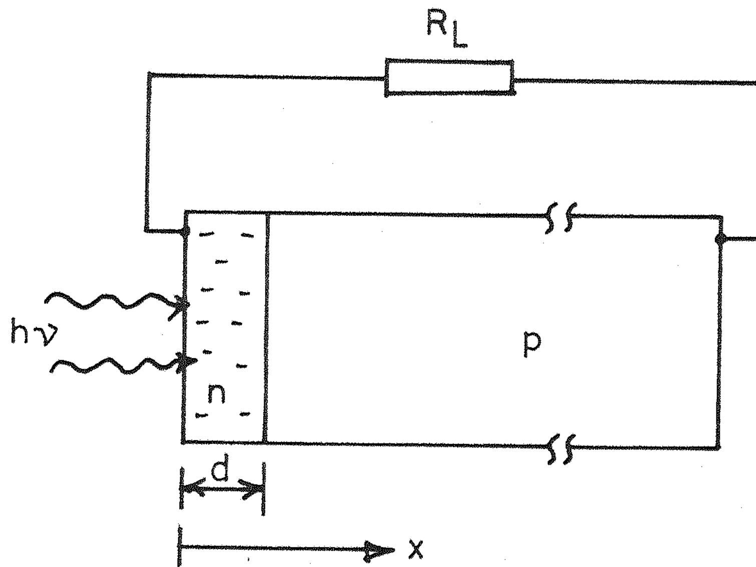
$$I_{ph} = \phi_o \cdot \eta \cdot q = \frac{P}{h\nu} \cdot \eta \cdot q \qquad (2.1)$$

where ϕ_o ($= P/h\nu$) is the incident photon flux density (photons . cm^{-2} . sec^{-1}), $h\nu$ is the photon energy, P is the incident power, and η is the quantum efficiency (i.e. the number of electron-hole pairs generated per incident photon).

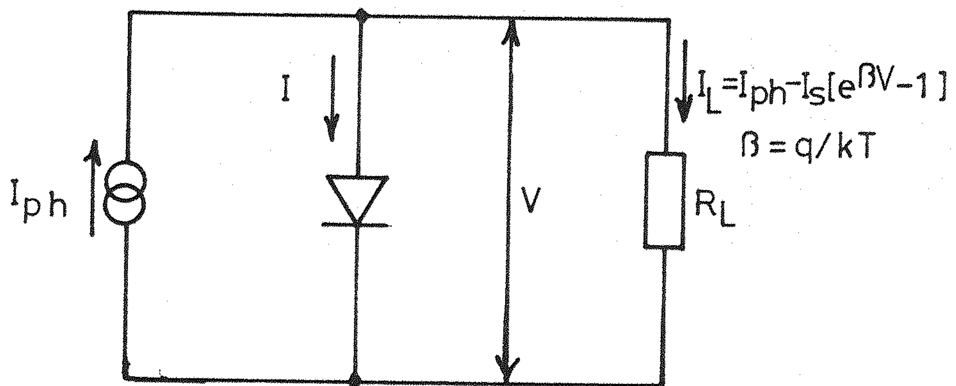
The following assumptions will be made in the analysis:

(a) the semiconductor quantum efficiency η, is unity, i.e. each incident photon of energy greater than the energy band gap of the semiconductor generates an electron-hole pair.

(b) low level injection; i.e. the increase in the concentration of majority carriers (due to illumination) is negligible in comparison to the equilibrium majority carrier concentration.



(a)



(b)

Fig. 2.1 (a) A pn junction under illumination, and (b) its equivalent circuit.

(c) the sample thickness is semi-infinite; i.e. the sample thickness is much greater than the minority carrier diffusion length in the bulk, so that recombination at the back contact can be neglected.

The generation rate (of electron-hole pairs) at a distance x in the semiconductor is given by:

$$G(x) = \alpha \phi_o e^{-\alpha x} \text{ (carriers . cm}^{-3} \text{ . sec}^{-1}\text{)} \tag{2.2}$$

where $\alpha = \alpha(\lambda)$ is the absorption coefficient of the semiconductor, λ is the wavelength of the incident illumination (considered monochromatic). Refer to Figure 2.1(a); in the n-side, the minority carriers (holes) created at a distance x will have a fraction proportional to $\exp\{-(d-x)/L_p\}$ diffuse to the junction (L_p is the minority carrier diffusion length in the n-region). The total number of minority carriers reaching the junction due to the creation of electron-hole pairs in the n-side is given by:

$$N \sim \int_o^d \alpha \phi_o \exp(-\alpha x) \,.\, \exp\{-|d-x|/L_p\} \, dx \tag{2.3}$$

$$= \frac{\alpha \phi_o L_p}{1 - \alpha L_p} \{\exp(-\alpha d) - \exp(-d/L_p)\} \tag{2.4}$$

Similarly, the number of minority carriers (electrons) reaching the junction as a result of the creation of electron-hole pairs in the p-region is given by

$$N \sim \int_d^\infty \alpha \phi_o \exp(-\alpha x) \exp[- \frac{|d-x|}{L_n}] \, dx \tag{2.4}$$

$$= \frac{\alpha \phi_o L_n}{1 + \alpha L_n} \exp (-\alpha d) \tag{2.5}$$

where L_n is the minority carrier diffusion length in the p-region.

The total number of carriers crossing the pn junction is

$$N_T \sim \phi_o \left\{ \frac{\alpha L_p}{1 - \alpha L_p} [\exp(-\alpha d) - \exp(-d/L_p)] + \frac{\alpha L_n}{1 + \alpha L_n} \exp(-\alpha d) \right\} \quad (2.6)$$

In the steady state the current through the cell is uniform everywhere, hence it is proportional to N_T. For a constant photon flux at each wavelength, the short circuit current per unit wavelength is given by:

$$I_{ph} \sim \frac{\alpha L_p}{1 - \alpha L_p} [\exp(-\alpha d) - \exp(-d/L_p)] + \frac{\alpha L_n}{1 + \alpha L_n} \exp(-\alpha d) \quad (2.7)$$

Figure 2.2 is a plot of the spectral response of the diffused pn junction as given by equation 2.7 for d = 2.0 μm, L_p = 0.5 μm and L_n = 10.0 μm (from Terman, ref. 2.1); the values of α for each wavelength were obtained from Dash and Newman[2.3].

The equivalent circuit of the illuminated pn junction is shown in Figure 2.1(b). The generated photocurrent can be used to drive an external circuit (R_L in Figure 2.1(b)); thus the pn junction diode is being used to generate electrical power from illumination (i.e. as a solar cell). The maximum voltage generated (V) can be obtained when the circuit is open-circuited (i.e. $I_L = 0$), to give V_{oc}

$$V_{oc} = \frac{1}{\beta} \ln (1 + I_{ph}/I_s) \quad (2.8)$$

where $\beta = q/kT$, q is the electronic charge, k is Boltzmann's constant, T is the absolute temperature, and I_s is the diode reverse saturation current.

Summary and Discussions

The absorption coefficient α, is a strong function of the wavelength λ[2.3]. Consequently the wavelength range in which appreciable photocurrent can be generated is limited. The long-wavelength cutoff λ_c is determined by the energy gap of the semiconductor (1.1 μm for

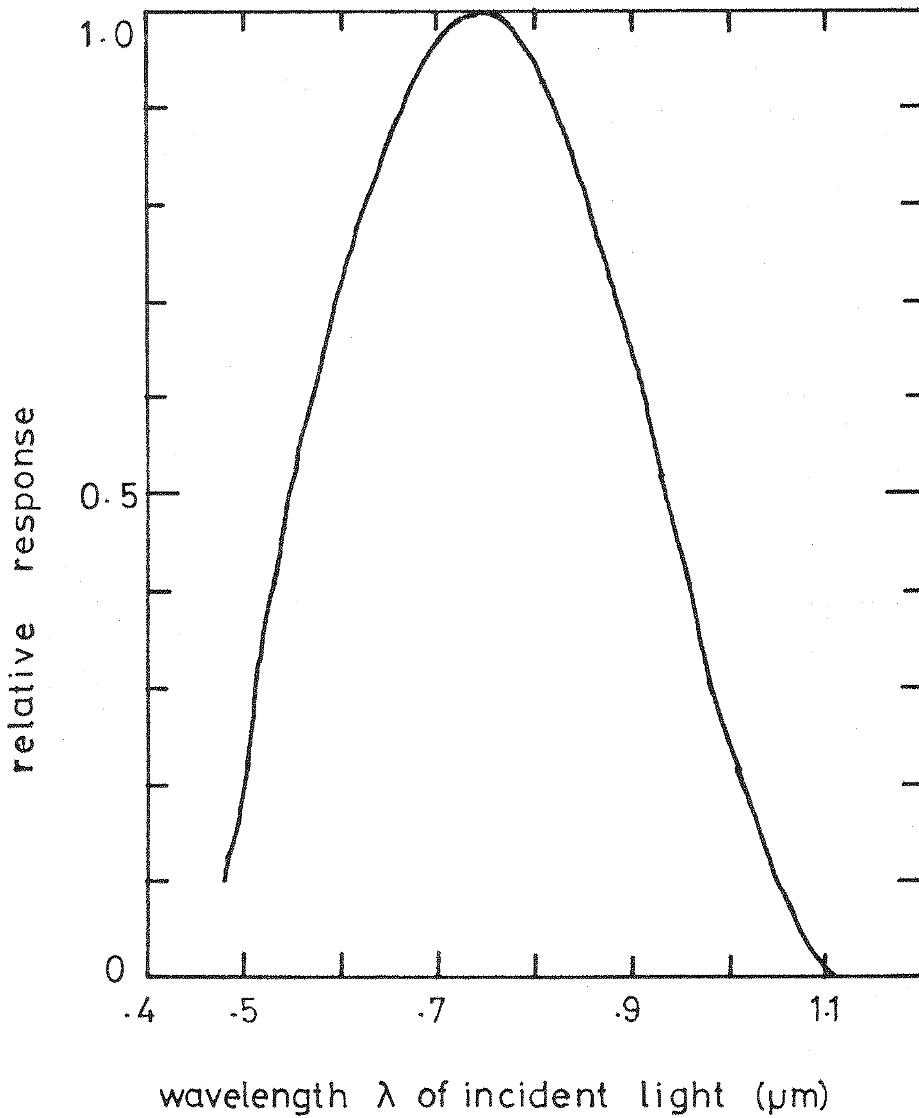


Fig. 2.2 Spectral response of a diffused pn junction photocell with d = 2.0 μm, L_p = 0.5 μm, L_n = 10.0 μm (after Terman, ref. 2.1).

Silicon). For wavelengths longer than λ_c, the values of α are too small to give appreciable absorption. The short-wavelength cutoff of the photoresponse comes about because the values of α for short wavelengths are very large ($\sim 10^5$ cm^{-1}), and therefore the radiation is absorbed very near the surface where there is very high surface-recombination. The generated carriers then recombine before they can reach the junction. The effect of surface recombination is to reduce the effective diffusion length (L_p) of the minority carriers in the n-region[2.1]. As this recombination is reduced by the processing technology (e.g. present day planar-process as opposed to the mesa-devices studied by Terman), the effective L_p increases, thereby improving the short-wavelength response of the diode.

The photon flux incident on the semiconductor surface (ϕ) is dependent on the optical properties of the surface. Normally, the pn junction is covered by a layer of SiO_2. The reflectance of the combined system (SiO_2 + semiconductor surface) determines how much of the incident photon flux actually reaches the semiconductor (lowering the sensitivity of the photodiode).

The ability of the pn junction diode to produce large magnitudes of photocurrents when illuminated can be applied to advantage in Laser testing of integrated circuits. This technique, to be described in the next chapter, uses the photocurrent generated at some pn junction to switch the state of the circuit. The requirement on the photodiode, then, is high sensitivity (production of large magnitudes of photocurrents for the incident photon flux).

CHAPTER THREE

APPLICATION OF THE PN JUNCTION PHOTODIODE IN LASER TESTING OF DIGITAL IC'S

3.1 Introduction

The complexity of modern LSI circuits means that the proportion of the circuitry which can be directly accessed by the tester from the external pins has decreased quite sharply. This leads to the requirement of long input sequences to exhaustively test the circuits for all the possible conditions that might be encountered in service, resulting in extremely long test times. With the laser testing technique developed by Oldham[3.1], information can be injected directly into the internal circuitry of the integrated circuit (IC) leading to a simplification of the testing scheme. An example of a typical test on an IC will be given in section 3.4.

The laser testing technique is a method of injecting information directly into the internal circuitry of an IC via a finely focussed, intensity-modulated laser beam. Intensity modulation is accomplished by an electro-optic modulator[3.2,3.3].

Fault diagnosis can be performed quickly and easily by using the movable laser input which is non-contacting and non-destructive. The ability of the laser probe to access the internal nodes, thereby making a reduction in the number of steps required in the test sequence, means large savings in the time required to test the IC's when the laser testing system is used in conjunction with conventional test equipment; it also provides deeper insight into the internal operation of the circuit.

In this chapter we present an outline of the laser testing technique. Section 3.2 shows how a pn junction photodiode is used to optically inject information into the required node of the circuit. In section 3.3 we look at the design of the laser probe and see how the laser beam is intensity-modulated with the signal. In section 3.4 we look at an example of laser testing of a digital IC, the example being a diagnostic test.

3.2 Optical Injection of Information

The injection of information into the required node is achieved by the generation of a photocurrent at a suitable pn junction. Consider the most basic MOS digital circuit, the MOS inverter. In an integrated MOS inverter, the two transistors used as the driver and the load, share a common substrate which is usually grounded (see Figure 3.1).

Figure 3.1 shows an NMOS inverter that is illuminated at the output node. The output node is an n-diffusion that acts both as drain terminal of the driver transistor and the source of the load transistor. This n-diffusion forms a pn junction with the p-type substrate which can be used as a photodiode as shown in this figure.

Illuminating this pn junction produces a photocurrent. The size of the photocurrent produced is directly proportional to the power of the light beam (equation 2.1 of Chapter 2).

The effect of this current upon the inverter will depend upon its state: if the driver is ON (low impedance), the photocurrent merely flows through the driver and the output stays low; the load current is only slightly altered and there is no effect upon the circuit behaviour. Conversely, if the driver is OFF (so that the inverter output is high), the photocurrent will shunt the driver and pull the output low. It is

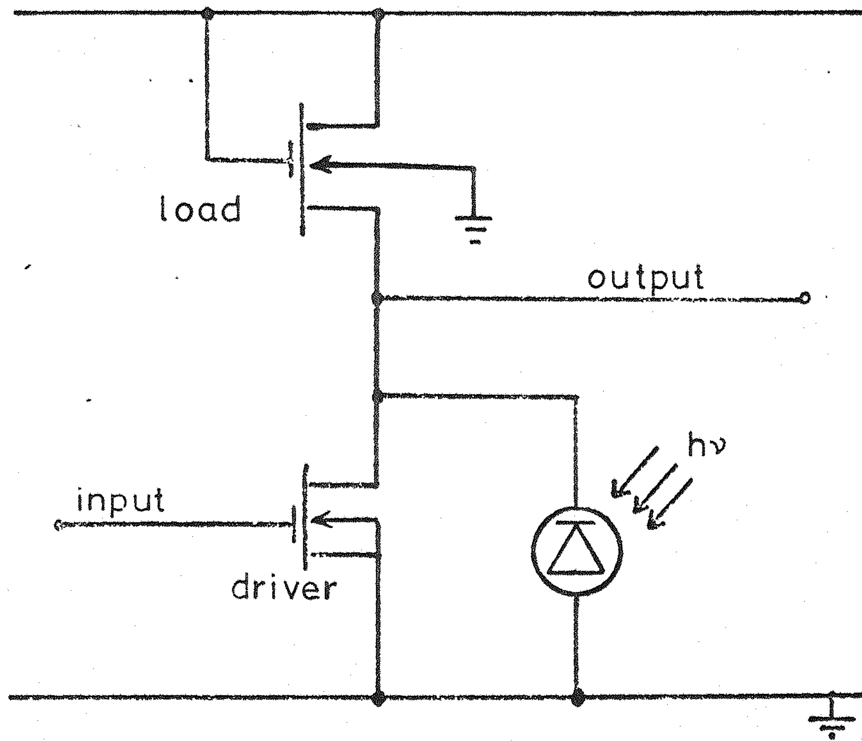


Fig. 3.1 An illuminated NMOS Inverter

necessary for the magnitude of the photocurrent to be comparable with the total current which normally flows when the inverter output is low to ensure that the output is low.

The light effectively shorts a node to ground so that it may be driven low, but cannot be driven high directly. This is not a serious drawback in practice though, because complementary nodes are often available.

Another possibility of optically generating a current to shunt the driver transistor is to direct the illumination at the gate area of the driver transistor (assuming the gate electrode is transparent). In this case as well, assuming the driver is OFF, the minority carriers generated by the light in the channel area will produce a conduction channel between the drain and source terminals, causing a drain current to flow which will shunt the driver and pull the output low.

In both cases, when the illumination is switched off, the circuit reverts to its original state. Thus by intensity-modulating the illumination with the signal, the signal can be injected into the required node.

The photocurrent generated in a circuit is proportional to the incident light power, and only slightly on the circuit type. Its influence upon the circuit action is determined by its relative magnitude to that of the currents already flowing in the circuit. Thus, different types of IC require different laser powers to inject information, see Table 3.1[3.4].

Table 3.1 : Laser Testing of Various MOS IC Logic Families[3.4]

Circuit Type	Focussed Beam Power (μW)
M.O.S. Static (Al-gate tuner)	8.0
M.O.S. Static (Si-gate 100 bit shift register)	2.4
M.O.S. Dynamic (Si-gate 256 bit shift register)	0.081
M.O.S. Dynamic (Al-gate 16 bit shift register)*	0.10
C.M.O.S. (J.K. bistable, V_{DD} = 4V)	4,200
C.M.O.S. (J.K. bistable, V_{DD} = 10V)	30,000 estimated[3.4]

* measured by the author

Both Al-gate and polysilicon gate circuits need similar light powers, but with the latter class light can reach the channel through the gate material. There is a significant difference in the laser switching power required between CMOS and the rest of the other MOS logic families.

CMOS requires surprisingly high laser powers. Figure 3.2 is a representation of an illuminated CMOS inverter. In either state, one transistor in the complementary pair is ON and can pass a large current without causing the output to switch when the OFF transistor is shunted by the photocurrent. Smith and Oldham[3.2] have calculated that a laser spot power of 30 mW would be needed to switch a bistable in the RCA CD4000 series when a supply of +10V is used. This causes a limitation on the laser testing technique to test MOS digital circuits implemented in the CMOS technology.

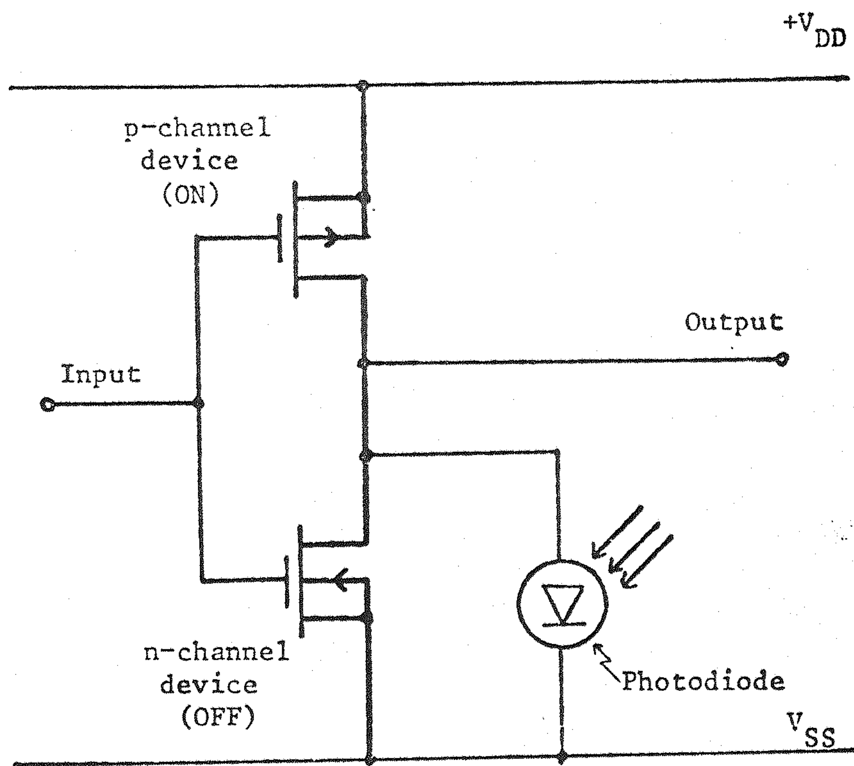


Fig. 3.2 AN ILLUMINATED C.M.O.S. INVERTER

3.3 The Laser Probe

Figure 3.3 shows in block diagram form the outline of the laser probe. The laser beam emerging from the He-Ne laser is polarised by the polariser crystal and then passed through an electro-optic modulator crystal and then through an analyser; (this combination of the polariser, modulator crystal, and the analyser, is known as a Pockel Cell[3.2,3.3]). The principle employed in the operation of this type of electro-optic modulator is the linear electro-optic effect[3.3]. This is essentially the linear change in the refractive index of the modulator crystal produced by an applied electric field. This way plane polarised light can be phase modulated to become elliptically polarised. If a crystal of this type is placed between crossed polarizers (the polariser and the analyser in Figure 3.3), it will intensity modulate the light emerging out of the analyser.

The Pockel cell has a light transfer function given by[3.2,3.3]

$$\frac{I_o}{I_{in}} = \mathrm{Sin}^2\left(\frac{\pi}{2} \cdot \frac{V}{V_*}\right) \tag{3.1}$$

where I_o is the intensity of the output beam, I_{in} the intensity of the input beam, V the applied voltage and V_* is the voltage needed to produce maximum transmission and is known as the halfwave voltage. This is the voltage required to spatially rotate plane polarised light through 90°. Figure 3.4 shows the transfer function of the Electro-optic Developments Ltd PC100 Pockel cell modulator with $V_* = 250V$. In normal operation, the operating point is shifted on this characteristic to the near-linear region in the centre of the sine^2 curve by applying a suitable d.c. bias to the cell.

LIBRARY

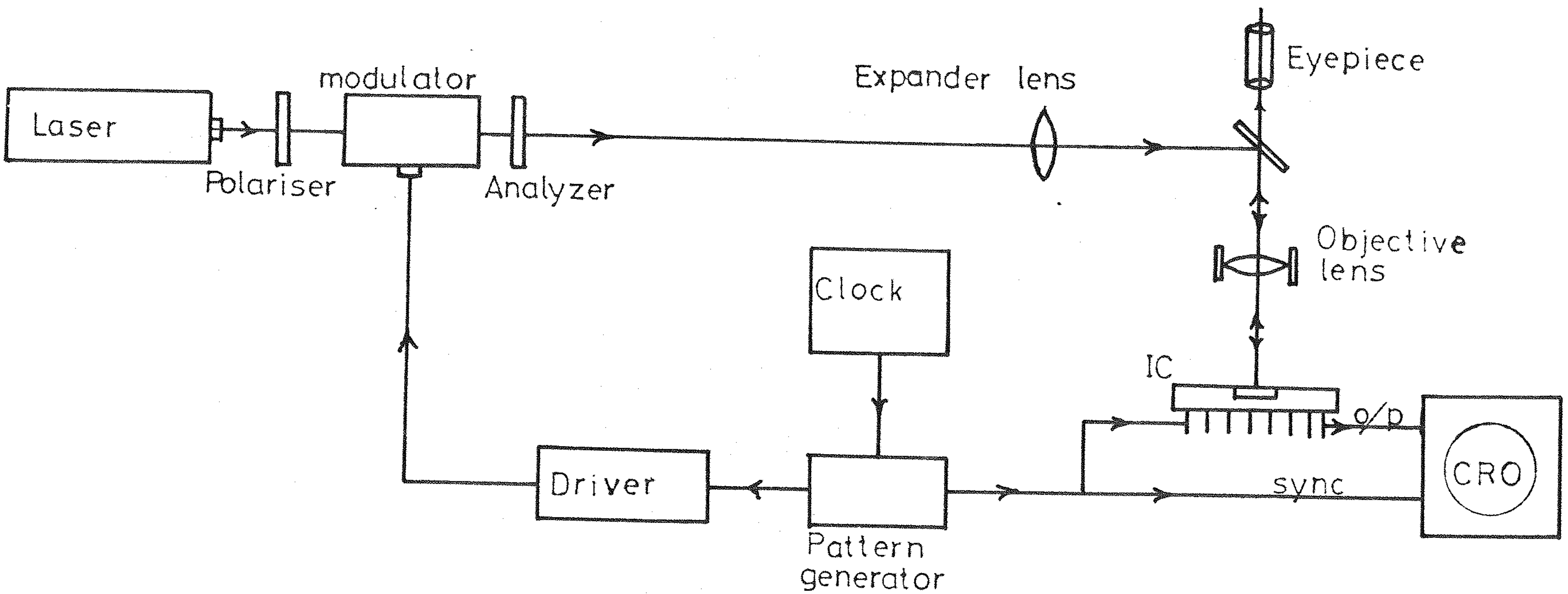


Fig. 3.3 The Laser Probe

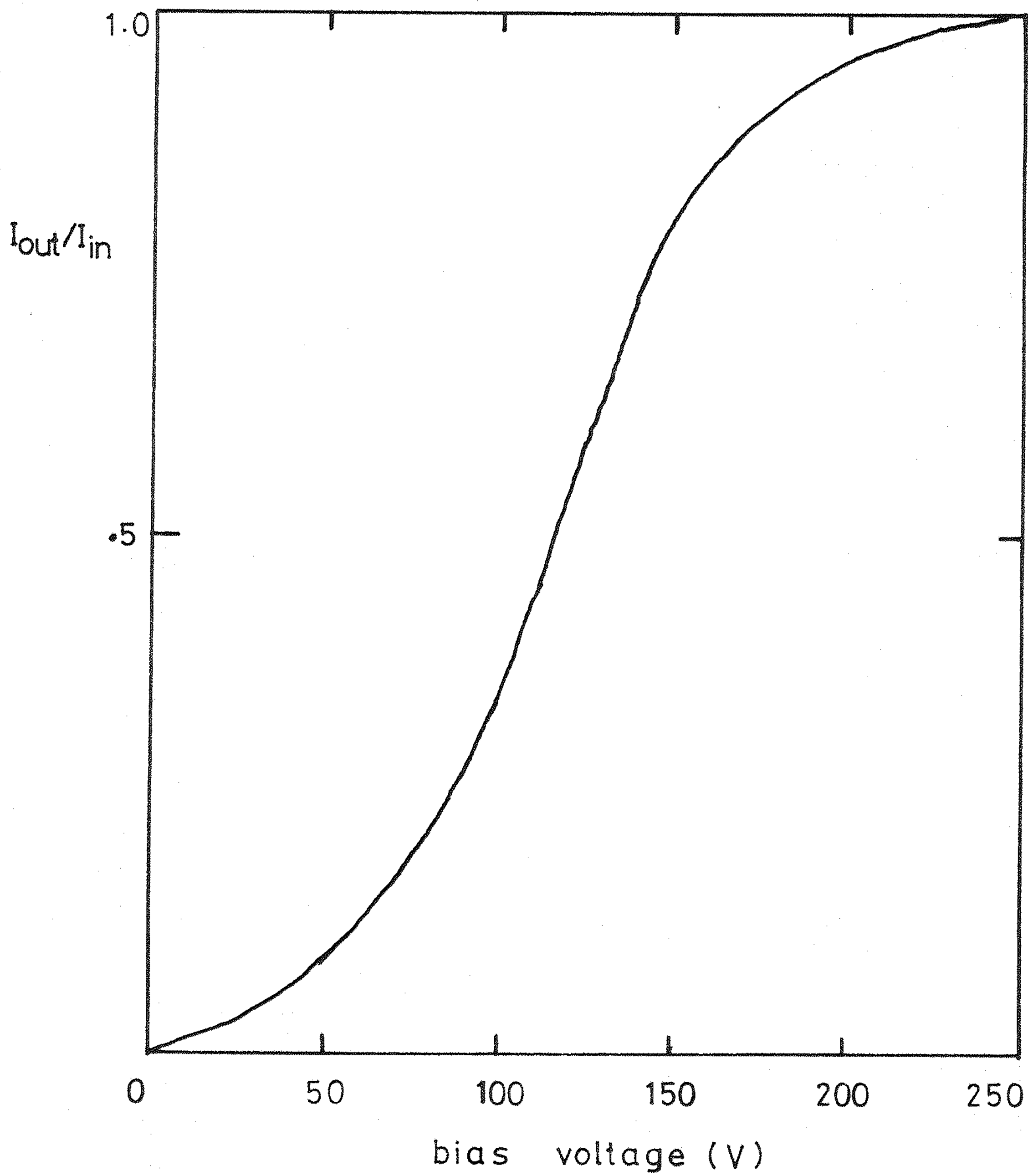


Fig. 3.4 Intensity response of the PC-100 Pockel Cell modulator as a function of the applied bias voltage (from ref. 3.3).

Focussing of the beam is accomplished by using two lenses, see Figure 3.3. The first, a low power expander lens, forms an intermediate focus which is transformed by the second lens, the objective, to form the final spot.

3.4 Laser Testing of a Digital Integrated Circuit

As an example of a typical test on an Integrated Circuit, consider a serial input Shift Register circuit. In its simplest form, a shift register circuit consists of a chain of inverter circuits each of which is 'gated' by a clock-voltage to pass the data onto the next stage. A schematic representation of a two-phase shift-register is given in Figure 3.5(a).

The operation of this circuit is straightforward. Information appearing at the input to the shift register (in) is gated to the output of inverter 1, by clock ϕ_1 rising to logic level '1'. This information, which is now the inverse of the input data, is then gated through inverter 2 to the output of the first bit, by clock ϕ_2 rising to logic level '1' while clock ϕ_1 is held at logic level '0'. By switching the clocks ON and OFF alternatively (as shown in Figure 3.5(b)) the information can propagate through the chain of inverters to the output terminal (out).

Suppose now that the shift register (SR) malfunctions because one (or more) of the inverters in the chain is (are) defective. The task for the diagnostic tester now is to locate which inverters are defective. This can be most easily achieved by partitioning the circuit.

By working backwards from the output towards the input; the last inverter in the chain is tested, and if this one works, the preceding one can be tested, and so on until the defective one is located. This

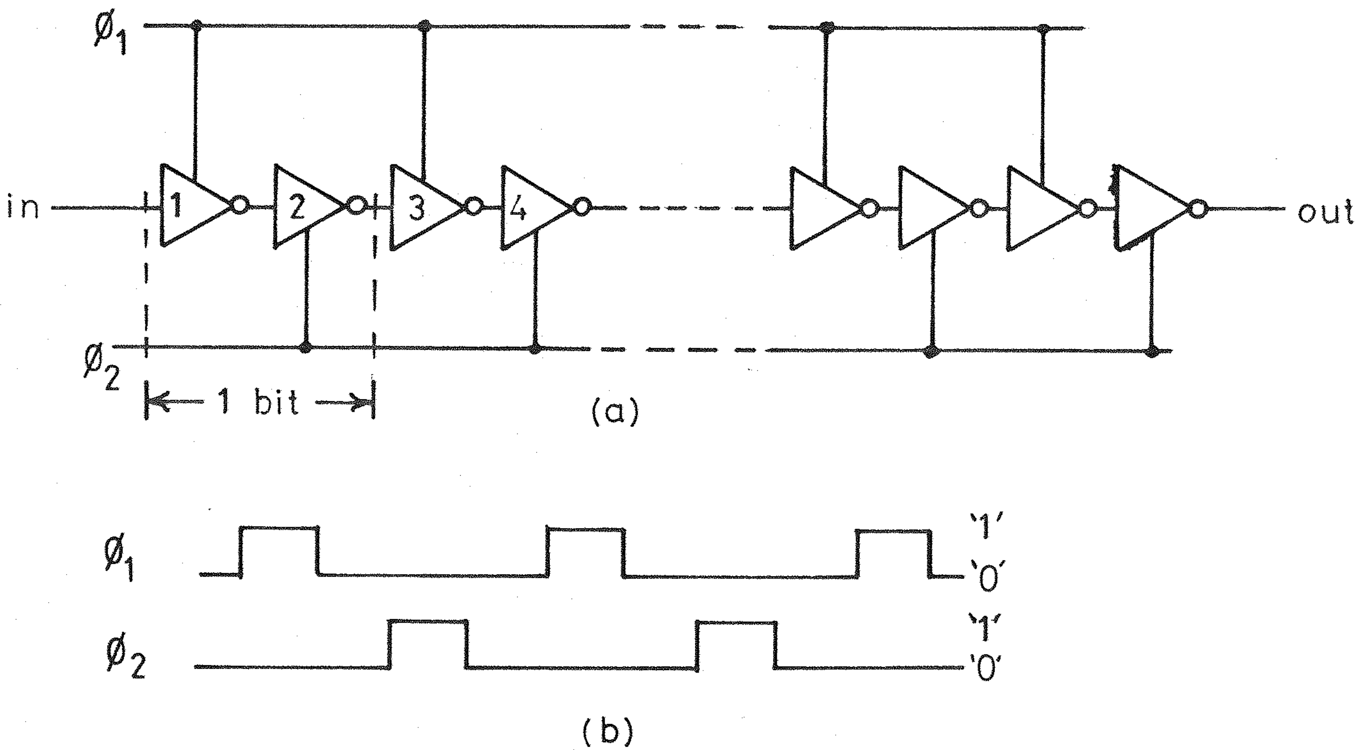


Fig. 3.5 (a) Schematic representation of a two phase shift register circuit; (b) clock timing waveforms for the operation of the circuit.

cannot be easily achieved unless each of the input nodes to the inverters is accessible to the tester. Even in as short a chain as a 16 bit shift register, for example, (which implies 32 inverters), for the tester to have access to all the nodes he would require 31 additional pins for the IC (additional to the input, the output, ϕ_1, ϕ_2, V supply, and Ground pins). This is obviously not practical, for as the complexity of the circuit increases and the number of nodes to be accessed increases, the required number of external pins would be unattainable in a reasonably sized package. Additionally each node would require a contacting pad for the external pin thereby increasing the stray capacitance at that node.

The obvious way around this problem, and probably the most practical solution to this partitioning problem, is to use an optical probe. This solution does not require any additional pins to the package, does not require any contact pads (and hence does not capacitively or resistively load the circuit nodes), and is non-destructive. The only requirement is for the nodes to be clear of any metallisation which can block the light from reaching them. The information is then injected into any required node via the optical probe.

3.5 Conclusions

The laser testing technique when used in conjunction with standard testing techniques can greatly simplify the testing procedure. This can lead to shorter testing times and a consequent reduction in the cost of development of integrated circuits.

To further investigate the potential of this testing technique, a purpose built circuit was fabricated and tested with the laser probe. The details of the circuit and the analysis of the results of the experiments are presented in the next chapter.

CHAPTER FOUR

MEASUREMENT OF DELAY TIMES ON AN MOS SHIFT REGISTER CIRCUIT

4.1 Introduction

To investigate further into the potentials of the Laser testing technique a p-MOS digital circuit was designed, fabricated and tested with the Laser probe. This chapter presents the details of the circuit, and an analysis of the results of the experiments performed.

Section 4.2 presents the design and the fabrication details, while a qualitative description of the operation of the circuit is presented in section 4.3, followed by an analysis to derive the operating speed. Section 4.4 presents the results of the experiments and compares these results with those calculated from the theoretical model.

4.2 The design of the Test Circuit

The digital circuit that was designed and fabricated for the purpose of evaluating the Laser testing technique was a 16-bit, aluminium gate, p-MOS, serial-input, serial-output, two-phase, dynamic shift-register. The important criteria for this circuit design were that:

(a) the circuit can be easily partitioned for diagnostic testing; so that parameters associated with intermediate units of the circuit could be determined,

(b) the input and output nodes of each basic unit of the shift register (i.e. the inverter circuit) be clear of metallisation so that they can be exposed to the light probe.

The four mask design was made using the $MM Mk III mask making programme[4.1], developed around a DDP516 computer in the Electronics Department of Southampton University. The fabrication of the circuit

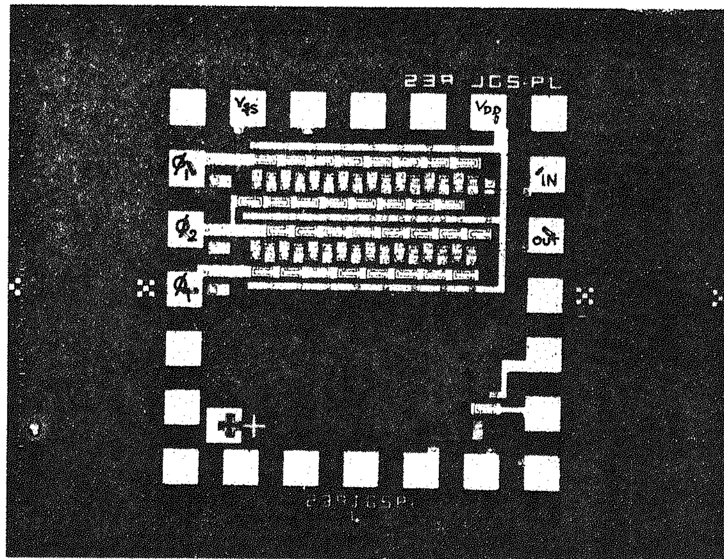
was carried out in the Micro-electronics Group processing laboratory in the same department. A photo-micrograph of the final chip is shown in Figure 4.1(a).

Basically, the shift register circuit comprises a chain of 2-transistor inverters coupled by pass transistors (the 'gate' transistors in Figure 4.2). On the chip, there are 32 inverters forming a 16-bit shift register. The layout is such that there are two chains of 16 inverters coupled by a long diffused link. This is portrayed in Figure 4.1(b). This figure also shows that the V_{SS} diffusion is grounded at one point which is approximately halfway through its length.

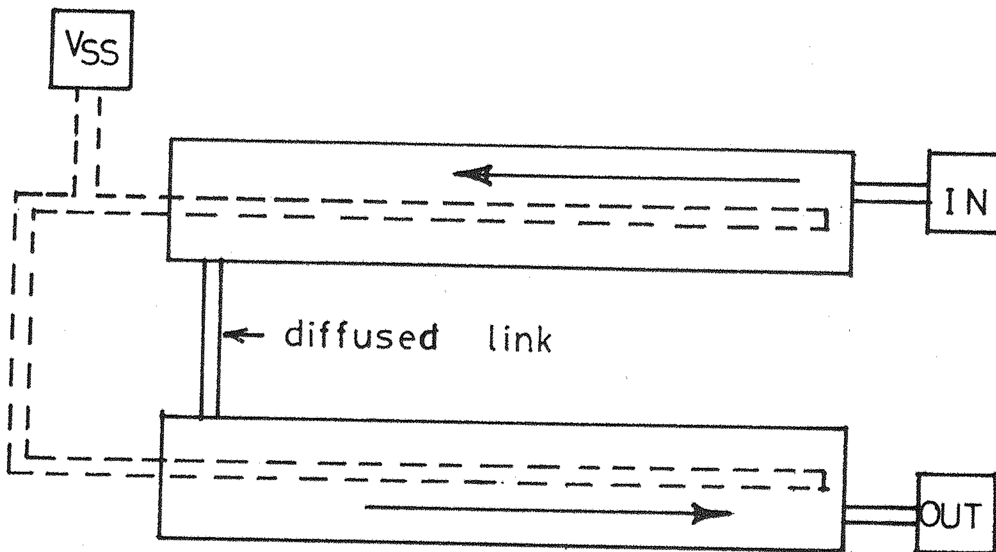
The circuit was fabricated on (Wacker) n-type silicon slices of 2.5 - 5.0 Ω.cm resistivity and <100> orientation. The dopant used for the source, drain and V_{ss} diffusions was boron. Table 4.1 summarises the processing characteristics of the device.

Table 4.1 : Characteristics of the shift register

Substrate doping concentration, N_D	10^{15} cm^{-3}
Orientation	<100>
Isolation oxide thickness	1.0 μm
Gate oxide thickness	1500 Å
Diffused regions sheet resistivity, R_S	250 Ω/□
Diffused regions junction depth, X_j	2.4 μm
Dopant for diffusions	Boron
Threshold voltage, V_T	-3.5 volts

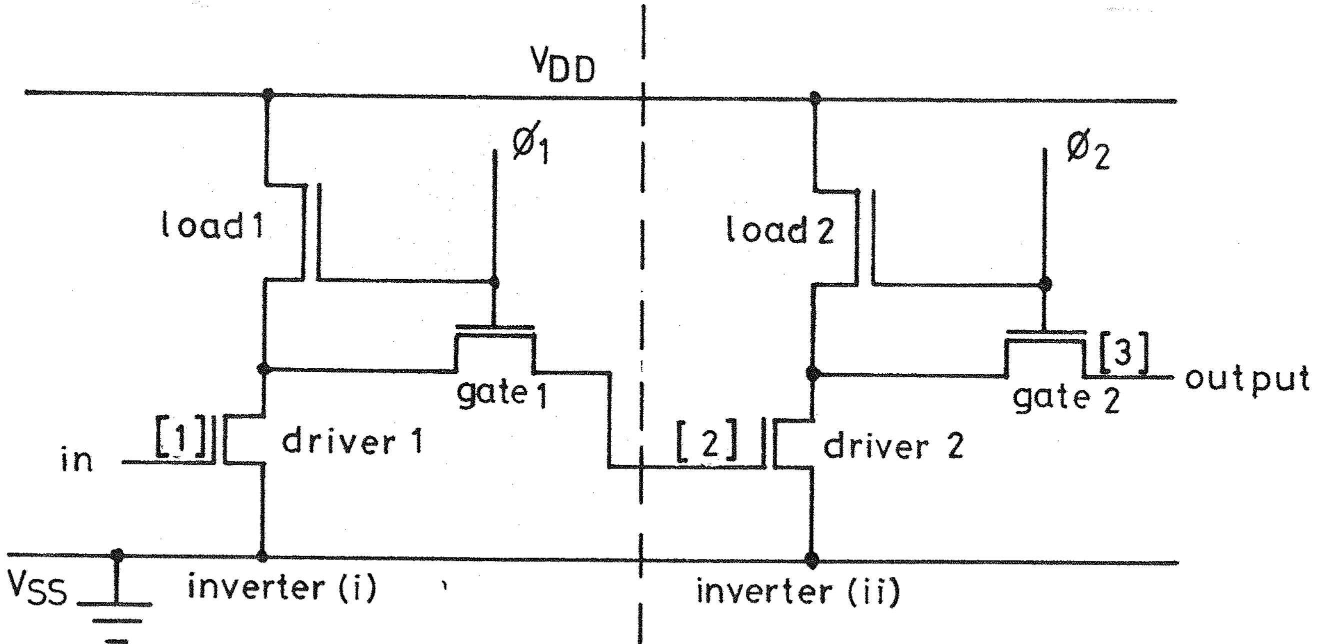


(a)

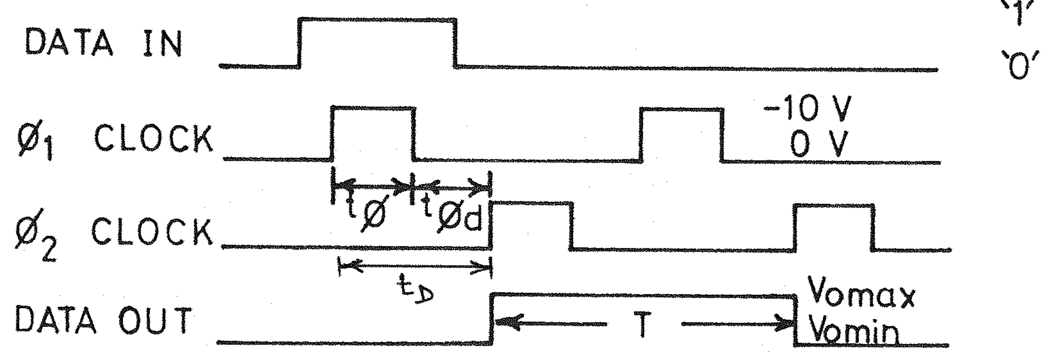


(b)

Fig. 4.1 (a) Photomicrograph of the test circuit, (b) schematic of the layout of the shift register.



(a)



(b)

Fig. 4.2 (a) Schematic of the dynamic shift register, showing one bit; (b) the timing waveforms.

4.3 Operation of the Shift Register Circuit

In this section we present a qualitative description of the operation of the MOS 2-phase dynamic shift register (SR). This is followed by a definition of the switching times of the basic unit of the SR (the inverter), and an estimate of the propagation delay times for the circuit.

Figure 4.2 shows 1 bit (i.e. two inverters) of the SR, and the timing waveforms for the operation of this circuit. When the ϕ_1 clock voltage switches from 0 V (low) to -10V (high), inverter (i) is switched ON and the data at the input (node [1]) is transferred to node [2]. The data at node [2] is the inverse of the data at node [1]. The time that it takes the data to get transferred from node [1] to node [2] after the change of the clock state is determined by the discharge or charge of the capacitance at node [2] (depending upon whether the data at the input is a logic '1' or '0', respectively). The information will be regarded as having reached node [2] when the capacitance on this node has discharged (charged) to below (above) the magnitude of the threshold voltage of driver 2, the driver transistor of inverter (ii). The next part of the cycle is to transfer the data on node [2] to node [3], the output of the 1 bit of the SR (which is also the input to the first inverter of the next bit of the SR). With ϕ_1 held at low, ϕ_2 switches from low to high, thereby switching ON inverter (ii) which passes the data to node [3]. The data appearing at node [3] will be of the same polarity as the input data at node [1], and will have been delayed by a period, t_D (Figure 4.2(b)). Again, the information will be regarded as having reached node [3] when the capacitance at this node has charged (discharged) to above (below) the threshold voltage of driver 3 (not shown in Figure 4.2). The minimum clock pulse width

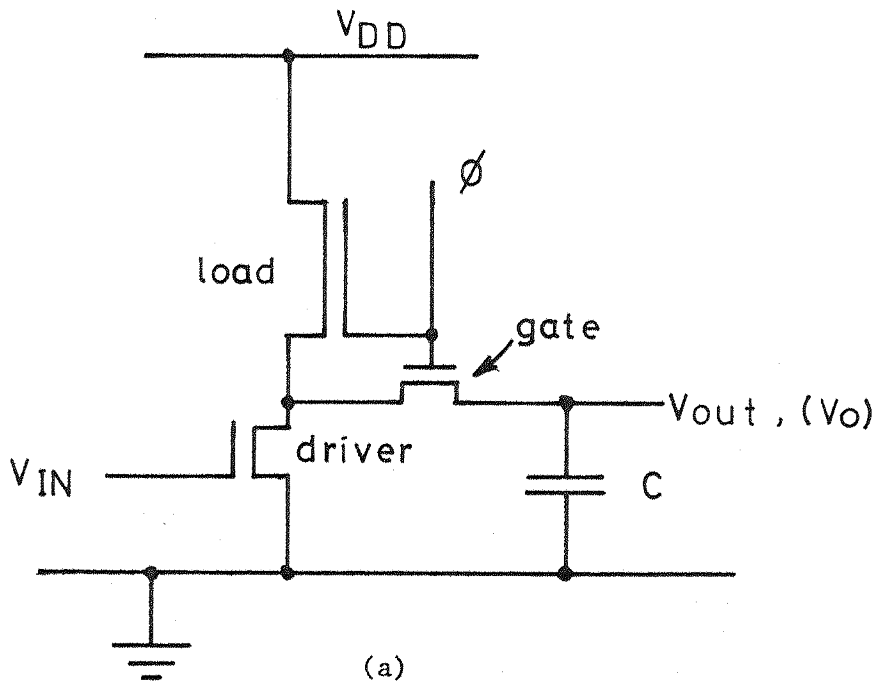
(t_ϕ in Figure 4.2(b)), and hence the maximum clock-rate, will be limited by the rates at which the capacitances at the inputs to the inverters can charge up (discharge) to the threshold voltages of the driver transistors.

4.3.1 Inverter Switching Times

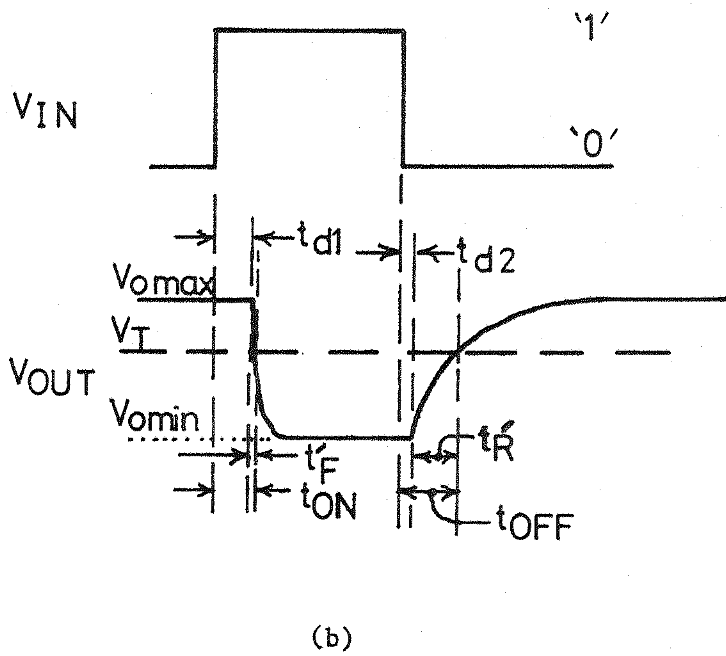
Refer to Figure 4.3 which will be used in the definition of the inverter switching times. This figure shows the basic unit of the SR as a 3-transistor inverter, it also shows the operating waveforms.

There are two modes of operation of this circuit. When the ϕ_1 and ϕ_2 lines are clocked alternately (normal SR operation mode), data is always present at the input of the inverter before the clock changes state. On the other hand, during the measurement of the propagation delay times, the clock lines ϕ_1 and ϕ_2 are connected to the same potential as V_{DD} (and are hence always in the high state); thus the data at the input of the inverter changes its logic state while the clocks are already high.

Consider first, the case when the clock lines are held high before data appears at the input of the inverter. When the input voltage (V_{IN}) changes from logic '0' to '1', it charges up the capacity at the input to the driver transistor, producing a delay (t_{d1}) between the arrival of the input data and the start of the fall of the output voltage. t_{d1} depends on how fast the input capacity can charge up to V_T of the driver transistor. At the input of the SR, where the input signal is derived from a low-impedance source, this time is negligibly short. Anywhere else within the SR, this time will be the risetime (t'_R in Figure 4.3(b)) of the preceding inverter. The time between the start of the fall in the output voltage (V_{out}) and the time that V_{out} falls to V_T of the succeeding driver transistor, will be defined as the 'effective fall-time', t'_F (see Figure 4.3(b)). The Switch-ON time (t_{ON} in



(a)



(b)

Fig. 4.3 (a) The p-MOS inverter circuit, and (b) the switching waveforms.

Figure 4.3(b)) is the sum of t_{d1} and t'_F.

When V_{IN} switches from '1' to '0', it discharges the input capacity, producing a delay time t_{d2}, between the start of the change in V_{IN} and the start of the rise of V_{out}. Again, at the input of the SR, t_{d2} would be negligible, while anywhere else within the SR t_{d2} would be due to the effective fall time (t'_F) of the preceding inverter. The time between the start of the rise in V_{out} and the time V_{out} rises to V_T of the succeeding driver transistor, will be defined as the 'effective risetime', t'_R (Figure 4.3(b)). The switch-OFF time is the sum of t_{d2} and t'_R.

During the calculation of the propagation delay times, we need to calculate both t'_F and t'_R of each inverter in order that we work out t_{ON} and t_{OFF} for any inverter; since t_{d1} and t_{d2} are given by t'_R and t'_F of the preceding inverter, respectively.

Consider next, the case when the SR operates normally (i.e. ϕ_1 and ϕ_2 clocked, alternately). In this case data is already present at the input to the inverter before the clock changes state. Consider Figure 4.3(a) and assume that the V_{IN} is at a logic '1' before ϕ switches from low to high. Since the ϕ voltage is derived from an external (low-impedance source), it switches to its high state in negligible time. Also, since V_{IN} is already at a '1' when ϕ changes state, V_{out} starts to fall at the same time as ϕ switches state, i.e. t_{d1} of Figure 4.3(b) is zero; so that t_{ON} is approximately equal to t'_F. Similarly, if V_{IN} was at a logic '0' before ϕ changed state, V_{out} would start to rise towards V_{omax} with t_{d2} equal to zero, so that t_{OFF} would be approximately equal to t'_R.

In Figure 4.3(b) t'_F is portrayed as a very much shorter time than t'_R. This will indeed be the case in practice because the load transistor

is a very low current device compared with the driver transistor. This condition is required in the design of the inverter so that when the driver is switched ON, it is capable of sinking all the current from the load device and still maintain a logic '0' at its drain terminal. When the driver transistor is OFF, the output capacitance charges up towards V_{omax} through the load transistor and the 'pass' or 'gate' transistor; while when driver is ON, this capacitance discharges through the driver transistor and the 'gate' transistor. Since the load transistor is a very much lower current device compared to the driver transistor, the output capacitance will take a longer time to charge up from V_{omin} to V_T than it will take to discharge from V_{omax} to V_T, even when $V_T - V_{omin} = V_{omax} - V_T$; so that $t'_R > t'_F$.

To analyse the operation of the inverter circuit and derive the switching times, requires a knowledge of the MOS-transistor theory. Two treatments of the MOS theory are to be found in Appendix A1. The first is a treatment based on considering both the drift and diffusion current components of the drain current and is based on the paper by Baccarani et al[4.2]. The second, which is an approximation to the fuller theory, is based on the works of Crawford[4.3] and Penny and Lau[4.4]. The fuller theory is more suited to analyses of single transistors, while the approximate theory makes the analyses of multiple transistor circuits more tractable. In the analysis of the MOS inverter to derive the transient characteristics, we (like Refs. 4.5, and 4.6) will employ the approximate theory (equations A1.47 - A1.50 of Appendix A1). This approach involves slight approximations, but it has the advantage of providing a clearer insight into the operation of the circuit.

4.3.1(a) The Fall Time : t'_F

Refer to Figure 4.4, which will be used in the derivation of the switching time. The capacitance C at the output of the inverter represents the gate-electrode capacity of the input to the next inverter plus pn-junction capacities of all diffusions connected to this gate-electrode, and the Miller-capacitance between the input and the drain of the driver transistor of the next inverter. At the output of the SR, C would also include the capacitances of the output pad and the output load circuit.

Figure 4.4(b) represents the equivalent circuit of the inverter when the driver transistor is conducting heavily. It will be assumed that $|V_{in}| >> |V_T|$; this ensures that the voltage at node [2'] reaches V_{omin} in negligible time. This condition is satisfied when the SR operates with ϕ_1 and ϕ_2 clocked (i.e. data is set at the input before the clock changes state). During the measurement of the propagation delay times though, this condition is only satisfied at the input of the SR where V_{IN} is derived from a low-impedance source. Anywhere else within the SR, V_{IN} slews between $|V_{IN}| < |V_T|$ and $|V_{IN}| > |V_T|$ with the consequence that the voltage at node [2'] ($V_{[2']}$) falls to V_{omin} in a finite time. This will introduce a slight error to the t'_F to be calculated; as the calculation assumes that $V_{[2']}$ reaches V_{omin} as soon as V_{IN} reaches V_T. This error can be minimised by making the geometrical ratio (β_R) of the load and driver transistors large (∿20)[4.6,4.7,4.8].

$$\beta_R = \left(\frac{W_{dr}}{L_{dr}} \right) / \left(\frac{W_{\ell d}}{L_{\ell d}} \right)$$

where W is the width, and L the length of the channel of the transistor; and the subscripts dr and ℓd refer to the driver and load devices, respectively. In the present design, β_R from the design geometries (see Figure 4.8) is 27.4; and when lateral diffusions are taken into account,

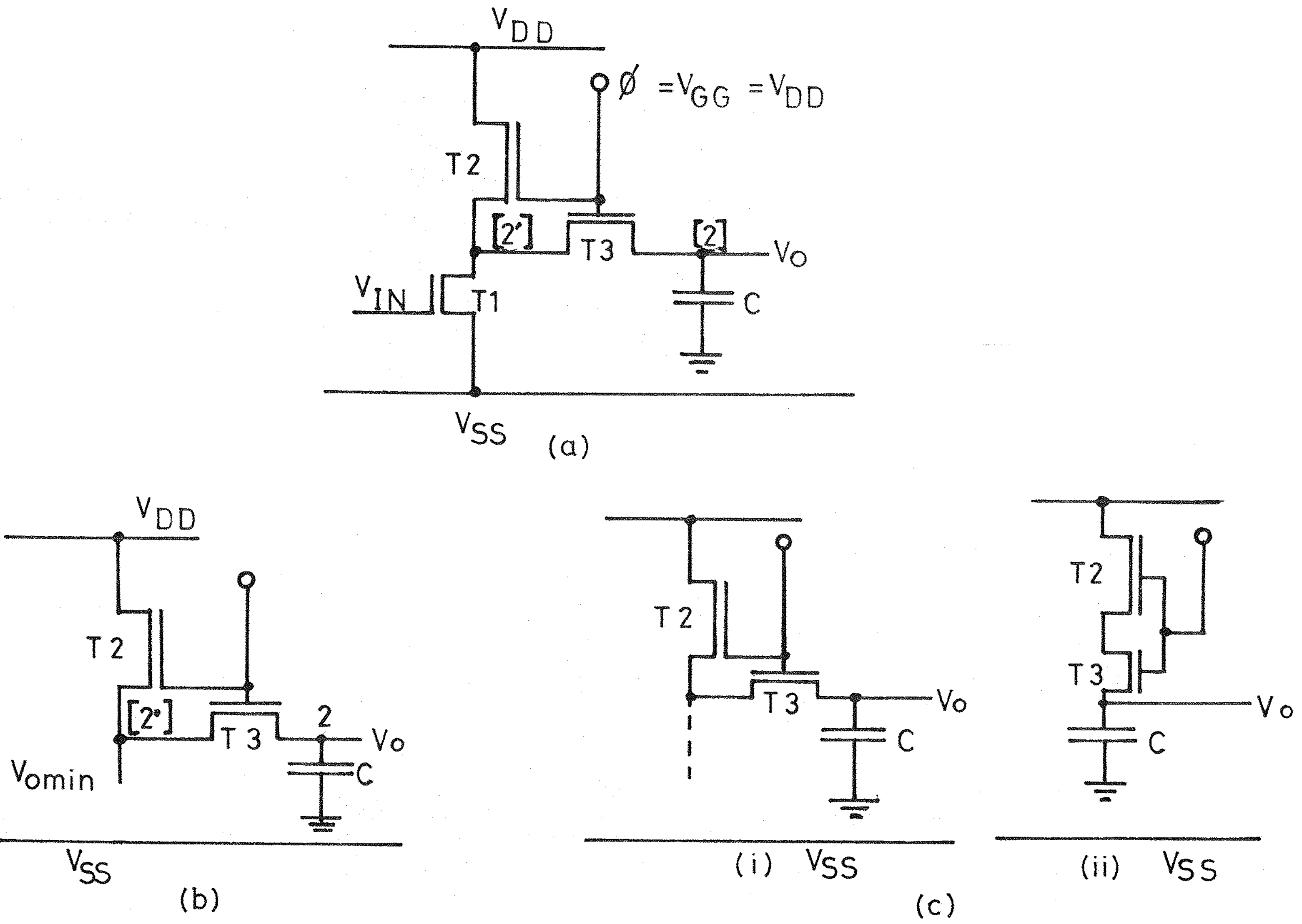


Fig. 4.4 (a) The basic inverter, (b) and (c) equivalent circuits of the inverter with the driver ON and OFF respectively.

β_R rises to above 40, reducing the error even further.

The rate of discharge of the capacitance C, is determined by the current of transistor T_3 and the resistance of the diffusion linking T_3 to C. This resistance is negligible, except for the inverter at the end of the first chain (Figure 4.1(b)). The capacitor discharge current is given by:

$$I_C = - C \frac{d V_o}{dt} \qquad (4.1)$$

with the boundary conditions that at time t = 0, the output voltage (V_o) is V_{omax}, and $V_{o(t\to\infty)} = V_{omin}$. The capacitor discharge current must equal the drain current of transistor T_3, I_{D3}. The source and drain voltages of T_3 are now V_{omin} and V_o, respectively. Since V_o is less than the gate voltage of T_3 ($V_G = \phi = V_{DD}$), this transistor operates in the triode mode, and its drain current is given by equation A1.49(a) of appendix A1, i.e:

$$I_{D3} = \beta_3 \left\{(V_G-V_T)(V_o-V_{omin}) - \tfrac{1}{2}(V_o^2 - V_{omin}^2)\right\} = -C \frac{d V_o}{dt} \qquad (4.2)$$

so that:

$$\int dt = - \frac{C}{\beta_3} \int \frac{d V_o}{\left\{(V_G-V_T)(V_o-V_{omin}) - \tfrac{1}{2}(V_o^2 - V_{omin}^2)\right\}} \qquad (4.3a)$$

where now $V_G = V_{DD}$ and V_T is dependent on V_{omin} and is given by equation A1.50 of appendix A1. Since V_{omin} is constant (and hence is V_T), equation 4.3a can be re-written as follows:

$$\int dt = - \frac{C}{\beta_3} \int \frac{d V_o}{\left\{(V_G - V_T) V_o - \tfrac{1}{2} V_o^2 - V_{omin} (V_G - V_T - \tfrac{1}{2} V_{omin})\right\}} \qquad (4.3b)$$

From the definition of the effective fall time, we have that:

$$t'_F = \frac{-C}{\beta_3} \int_{V_{omax}}^{V'_T} \frac{d V_o}{\left\{(V_G-V_T) V_o - \tfrac{1}{2} V_o^2 - V_{omin} (V_G-V_T-\tfrac{1}{2} V_{omin})\right\}} \qquad (4.4)$$

where V'_T is the turn-off voltage of the driver transistor of the succeeding inverter. This can be integrated (e.g. using integrals tables of

ref. 4.9) to give:

$$t'_F = \frac{-C_3}{\beta_3(V_G-V_T-V_{omin})} \ \ell n \left\{ \frac{\frac{1}{2}V^2_{omin}-(V_G-V_T)V_{omin}-(V_G-V_T-V_{omin})-V_o}{\frac{1}{2}V^2_{omin}-(V_G-V_T)V_{omin}+(V_G-V_T-V_{omin})-V_o} \right\} \Bigg|_{V_{omax}}^{V'_T} \quad (4.5)$$

V_{omax}, the output voltage before T_1 is switched on (see Figure 4.4) is given by:

$$V_{omax} = V_{GG} - [V_{TO}+K\{(V_{omax}+2\phi_F)^{\frac{1}{2}} - (2\phi_F^{\frac{1}{2}})\}] \quad (4.6)$$

where $K = \frac{1}{C_{ox}}\sqrt{2EsqN_A}$ ($\simeq$ 0.9 volt$^{\frac{1}{2}}$). This can be solved (on a computer) with only a few iterations to give an accurate value of V_{omax} for any given V_{GG} voltage. For V_{GG} = -10V, V_{omax} works out to be = -5.0 V.

The value of the capacitance C for all internal nodes (except for the inverter at the end of the first chain) was calculated to be equal to 0.28 pF, and the value of β_3 was calculated to be approximately 1.0 $\mu mho/V^2$. Using these values in equation 4.5 and assuming a value for V_{omin} = - 1.0 V when V_G = - 10 V gives a fall time of t'_F = 66.35 ns.

4.3.1(b) The Risetime : t'_R

Figure 4.4(c) shows a simplified equivalent circuit of the inverter once the driver transistor has been turned OFF by the input voltage. The output voltage rises towards V_{omax} by charging the capacitance C through transistors T_2 and T_3. In Figure 4.4c(ii) these two transistors are grouped together into one composite device to aid the analysis. The current that charges up C is the drain current of this composite device. Since $V_{GG} = V_{DD}$ (see Figure 4.4(a)), the composite device must be operating in the saturation mode; therefore, its drain current (which is equal to the capacitor current) is given by equation A1.52(b) of appendix A1, i.e:

$$I_D = \beta/2\ (V_{GG} - V_o - V_{TO} - \Delta V_T)^2 = C\frac{d\,V_o}{dt} \quad (4.7)$$

where ΔV_T is a function of V_o and is given by:

$$\Delta V_T = K \left\{ (V_o + 2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}} \right\} \tag{4.8}$$

Using the definition of the effective risetime, t'_R, we have from equation 4.7, that:

$$t'_R = \frac{2C}{\beta} \int_{V_{omin}}^{V_T} \frac{d\,V_o}{(V_{GG} - V_o - V_{TO} - \Delta V_T)^2} \tag{4.9}$$

where V_T is the turn-on voltage of the driver transistor of the succeeding inverter and V_{omin} is the output voltage before T_1 (see Figure 4.4(a)) is switched-off. Equation 4.9 can be used for each stage to obtain t'_R for a given pair of values of V_{omin} and V_T. A more elegant approach is to plot a general curve that relates the voltage (V) to the time (t) that the capacitor would take to charge up from 0 V to V. With such a curve, t'_R for any particular case (i.e. any pair of values of V_{omin} and V_T) can simply be read off the curve. This has been done, and the equation for this curve is given by:

$$t = \frac{2C}{\beta} \int_{0}^{V} \frac{d\,V_o}{(V_{GG} - V_o - V_{TO} - \Delta V_T)^2} \tag{4.10}$$

The relationship between the time and the voltage, given by equation 4.10, has been obtained using numerical analysis on a digital computer (ICL 2970).

Figure 4.5 shows the dependence of the output voltage, on time (t), for an output capacitance of 0.28 pF. The experimental data was obtained by connecting a known large capacitor across the output terminals of a test inverter on the chip; and dividing the results obtained by the necessary factor to arrive at an output capacitance of 0.28 pF. The calculated curve represents the best fit to the experiment using the model developed and assuming a capacitance of 0.28 pF, the fitted parameter being β of the composite device (see Figure 4.4(c)). The calculated

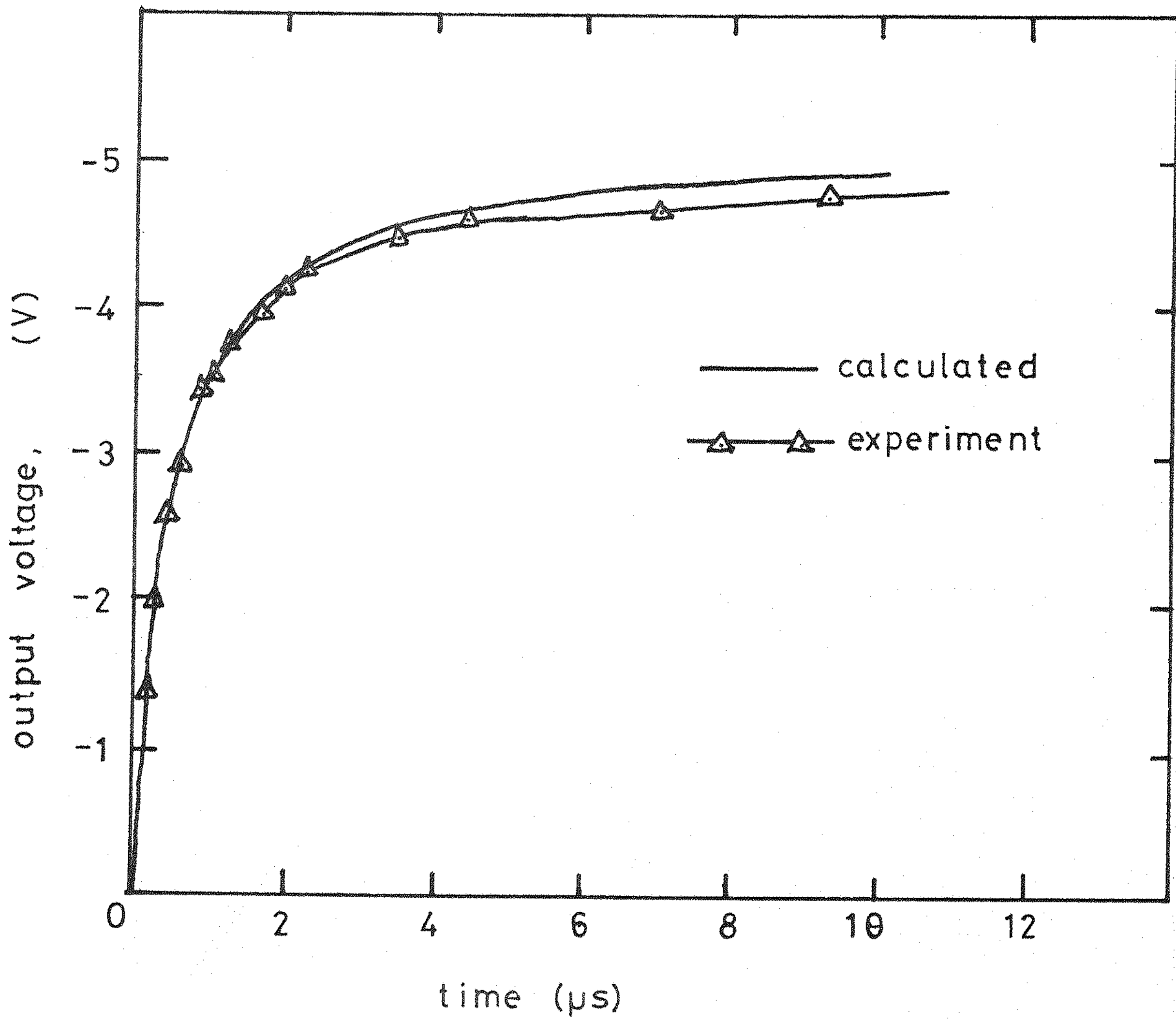


Fig. 4.5 The rise of the output voltage of the inverter as a function of time.

data was fitted to the experiment at $V_o = -3.5$ V.

These results show a reasonably good match between the theory and the experiment.

4.3.2 Propagation Delay and Maximum Clock-rate

The propagation delay time between the input and output of the SR circuit can be obtained by connecting the ϕ_1 and ϕ_2 clock lines to the V_{DD} supply, and then applying a signal to the input and noting how long it takes to arrive at the output terminal. Each inverter in the chain of 32 contributes a delay time to the total delay time, but as observed in the discussions above those inverters whose input capacitances get discharged on the arrival of the signal contribute a negligible amount (t'_F in ns) to the overall delay time. They will therefore be neglected here and the delay time will be taken as only due to the risetimes (t'_R) of those inverters whose capacitances get charged up as the signal propogates. These are alternate inverters in the chain.

Refer to Figure 4.6 which is a representation of the SR circuit, and assume that $\phi_1 = \phi_2 = V_{DD}$. The application of a step voltage at the input will switch ON inverter 1. The capacitance at the input of inverter 2, C_2, will start discharging and will drop below the V_T of the driver transistor of this inverter, thereby switching OFF inverter 2. This takes negligible time, as assumed above. Once inverter 2 has switched off, C_3, the capacitance at the input of inverter 3 starts to charge up, reaching V_T of the driver transistor of inverter 3 after a delay t_3. The driver of inverter 3 is now on, and there will be a further delay before inverter 5 turns on, and so on.

The individual delay times will depend on the values of the capacitances C_3, C_5, C_7, etc. at the inputs of the inverters and also on the turn-on voltages V_{Tn} of the respective driver transistors,

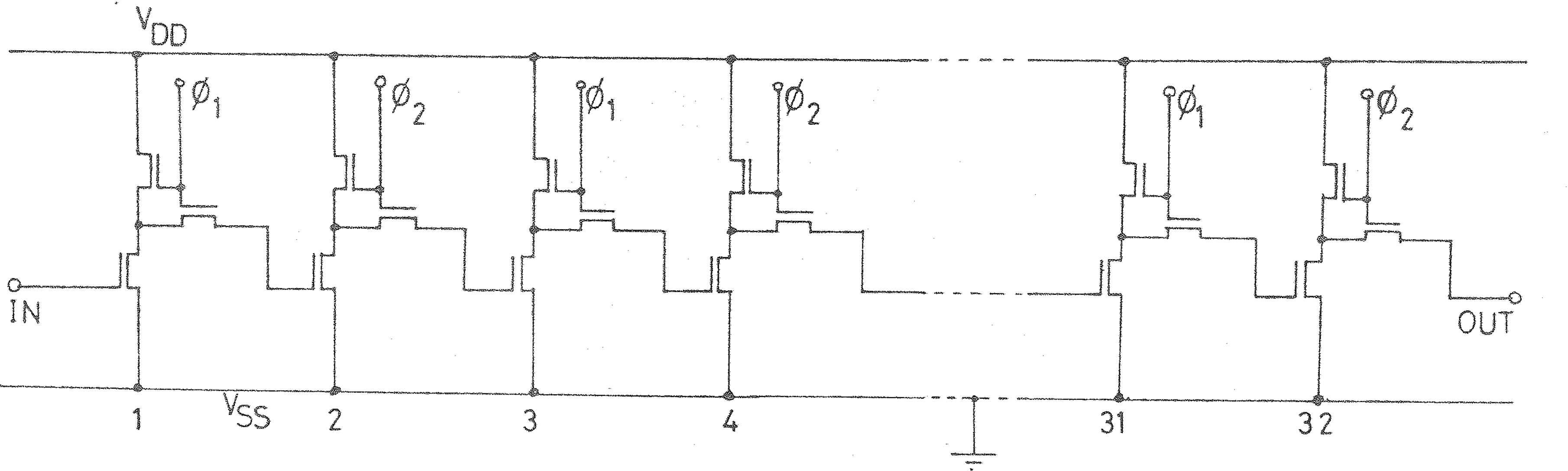


Fig. 4.6 Schematic of the shift register

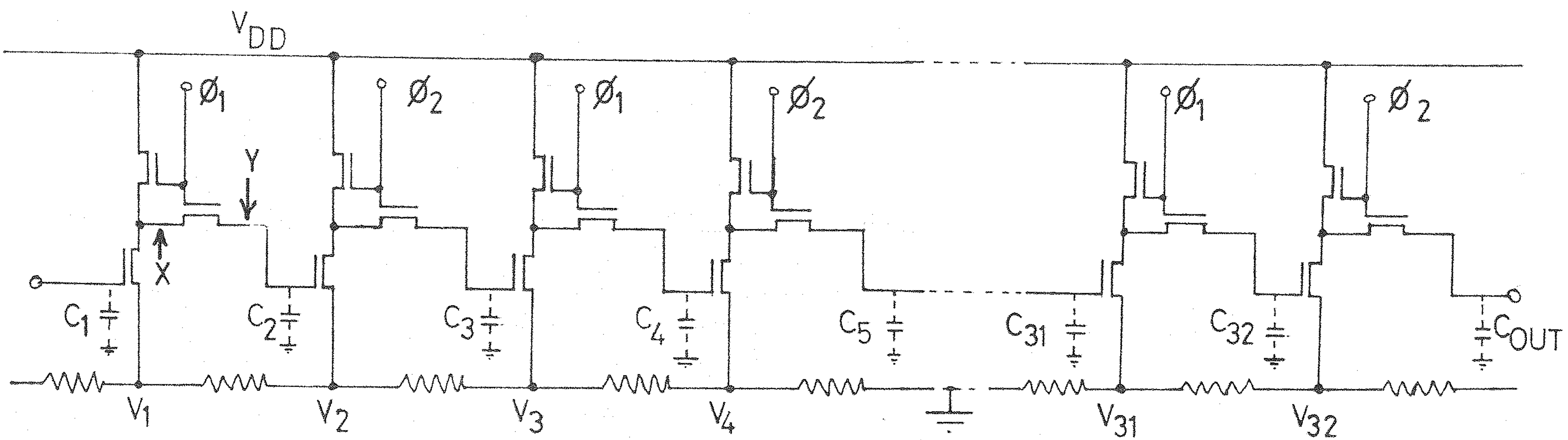


Fig. 4.7 The SR, showing the effect of the finite resistance of the V_{SS} bus

which depends upon the potentials of the sources.

Figure 4.1(b) shows the layout of the circuit and the division of the circuit into two chains of the inverters. Also, note that the grounding to the V_{SS} diffusion is applied at a point approximately halfway through its length. It will also be observed from Table 4.1 that the sheet resistance of the V_{SS} diffusion (and all other p-diffusions) is 250 $\Omega/\square$, so that the resistance of the V_{SS} diffusion is not negligible (as depicted in Figure 4.6). Figure 4.7 is an attempt at representing the effect of this finite V_{SS}-diffusion resistance on the source potentials of the driver transistors of the inverters. The currents flowing through the V_{SS}-diffusion to ground develop voltages V_n at the source terminals of the driver transistors resulting in varying turn-on voltages V_{Tn} and hence varying delay times from each inverter.

In arriving at the value of 0.28 pF for the capacitance at the input of each driver transistor (and used in section 4.3.1 to calculate t'_F and t'_R), we have added a contribution from the pn junction capacitance (at 0V bias) of the diffusion linking the 'pass' transistor (T_3 in Figure 4.4) to the gate of the driver transistor of the next inverter. The dimensions used in this calculation are common to all pass transistors, except that which links the two chains of inverters (i.e. the output of inverter 16, or the input to inverter 17), which is longer. This contributes a high junction capacitance to C_{17} (this makes C_{17} = 0.45 pF instead of 0.28 pF), which contributes an extra long delay time to the propagation delay.

4.3.2(a) Source Potentials V_n, and Turn-on voltages V_{Tn}, of the Driver Transistors

From the measured sheet resistivity of 250 Ω/□ and the design geometry, the value of the resistances associated with the V_{SS}-diffusion have been calculated. The use of the design geometries neglects the effects of lateral diffusion, which introduces an error of the order of 6% to the calculated resistance (Glaser and Subark-Sharpe; Ref. 4.10), making the value of the resistors lower than calculated.

With $\phi 1 = \phi 2 = V_{DD}$ (and V_{IN} at logic '1'), alternate inverters will be conducting and passing currents I_n through the V_{SS} diffusion resistors to the grounded point; thereby raising the magnitudes of the source potentials above ground. To find the source potentials V_n, a computer iterative technique has been used (i.e. calculating I_n's and then V_n's alternately); iterations were carried out until V_n converged to within 0.01% for each successive iteration. Having obtained the V_n's, the associated turn-on voltages V_{Tn} can be obtained by using the equation:

$$V_{Tn} = V_{TO} + V_n + K\left\{(V_n+2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}\right\} \quad (4.11)$$

Table 4.2 shows the values of V_n and V_{Tn} for the driver transistors of odd numbered inverters.

Table 4.2 : The Source Potentials and Turn-on Voltages of alternate driver transistors

Stage	$-V_n$ (V)	$-V_{Tn}$ (V)	Stage	$-V_n$ (V)	$-V_{Tn}$ (V)
1	0.682	4.45	17	0.466	4.16
3	0.667	4.43	19	0.566	4.30
5	0.638	4.39	21	0.651	4.41
7	0.593	4.33	23	0.720	4.50
9	0.533	4.25	25	0.776	4.58
11	0.457	4.15	27	0.817	4.63
13	0.365	4.02	29	0.844	4.67
15	0.255	3.87	31	0.857	4.69

4.3.2(b) Predicted delay-times for each inverter

As discussed above, the delay time from each inverter depends on the turn-on voltage V_{Tn}, and the value of the input capacitance C_n (C_n = 0.28 pF for all inverters except stage 17, where C_{17} = 0.45 pF). Using Figure 4.5 in conjunction with the values of V_{Tn} of Table 4.2, the delay time t_d (= t'_R) for each stage has been calculated, the results are tabulated in Table 4.3.

Table 4.3 : Delay-times from alternate inverter stages

Stage	$-V_{Tn}$ (V)	t_d (μs)	Stage	$-V_{Tn}$ (V)	t_d (μs)
1	4.45	0	*17	4.16	2.89
3	4.43	2.7	19	4.30	2.1
5	4.39	2.5	21	4.41	2.7
7	4.33	2.3	23	4.50	3.2
9	4.25	2.1	25	4.58	3.7
11	4.15	1.8	27	4.63	3.9
13	4.02	1.5	29	4.67	4.8
15	3.87	1.25	31	4.69	5.6
				total propagation delay	43.04

*Note the long t_{d17} due to C_{17} being 0.45 pF (instead of 0.28 pF)

From Table 4.3 it will be noticed that although at inverter 1, C_1 has to charge up to - 4.45 V, this capacitance gets charged from the low-impedance signal source and therefore contributes negligible time to the propagation delay. Another feature worth note is at stage 17, C_{17} is 0.45 pF (instead of the 0.28 pF of all the other stages), it therefore takes longer to charge up to V_{T17} (-4.16 V) than, say, C_{19} does to charge up to V_{T19} (- 4.30 V).

4.3.2(c) The Maximum Clock-rate

As stated earlier, when the SR circuit operates with the ϕ_1 and ϕ_2 lines clocked alternately, the situation is such that the data is present at the input of each inverter before the clocks change state.

Refer to Figure 4.7 and assume that the input is at logic 'O' before the ϕ_1 clock changes from low to high. Also assume that the clock stays high for a period t_{ϕ_1} before it goes to low again. When clock ϕ_1 is high, capacitance C_2 charges up to V_{T2} in a time t_{d2}. This will be true as long as $t_{\phi_1} > t_{d2}$. If, on the other hand, $t_{\phi_1} < t_{d2}$, then while ϕ_1 is high capacitance C_2 will be unable to charge up to V_{T2}. The limiting value of t_{ϕ_1} is therefore $t_{\phi_1} \geqslant t_{d2}$. If the input is at logic '1', then when ϕ_1 changes from low to high, C_2 discharges to below V_{T2} (assumed in negligible time). Next, with ϕ_1 held low, ϕ_2 changes from low to high and stays high for a period t_{ϕ_2}, allowing C_3 to charge up to V_{T3} in a time t_{d3} (assuming $t_{\phi_2} > t_{d3}$). For stage 3 then, the limiting value of t_ϕ is $t_{\phi_2} \geqslant t_{d3}$. Assuming that $t_{\phi_1} = t_{\phi_2} = t_\phi$; the limiting value for t_ϕ in the SR ($t_{\phi Lim}$) will be the inverter stage with the longest delay time ($t_{d\ell}$), i.e:

$$t_{\phi_{Lim}} = t_{d\ell} \qquad (4.12)$$

A measure of $t_{\phi_{Lim}}$ will therefore furnish one point in Table 4.3, that of the stage with the longest delay time.

4.4 Measurement of Delay Times

To obtain the delay times from each stage, the partitioning technique described in section 3.3 of Chapter 3 was used; working from the input side to the output side of the SR.

As stated earlier (section 4.3.1), for this measurement, the clock lines are connected to the same potential as the V_{DD} supply (i.e. $\phi_1 = \phi_2 = V_{DD}$). The input of the SR was grounded.

By directing the laser beam onto either the drain-diffusion of the driver transistor (point 'X' in Figure 4.7), or the diffusion linking the pass-device to the input gate of the succeeding inverter (point 'Y' in Figure 4.7), we can discharge capacitance C_2 to ground with the generated photocurrent (points 'X' and 'Y' are also shown on the layout diagram, Figure 4.8). This will switch-off inverter 2 and the data will propagate through to the output of the SR as described previously.

The delay time between the injection of the data at point X, say, and its appearance at the output is the sum of the delays of the intermediate stages. So, by measuring this delay and then repeating the measurement but with the laser beam moved along the SR by one-bit (i.e. two inverter stages), the delay of the intervening stage can be calculated.

Using this technique, the delay times for each of the stages 3, 5, ... 31 have been measured. In Figure 4.9 (which shows typical waveforms for this measurement), this is consistent with the measurement of the time t_1. The time t_2 in this figure is the result of the delay after the light is switched off, or the charging up of the even-numbered stages; hence a measurement of t_2 would furnish the delay times due to the even-numbered stages (2, 4, ... 30).

The delay times from each of the odd-numbered stages are shown in Figure 4.10. Figure 4.10(a) presents the predicted calculations, i.e.

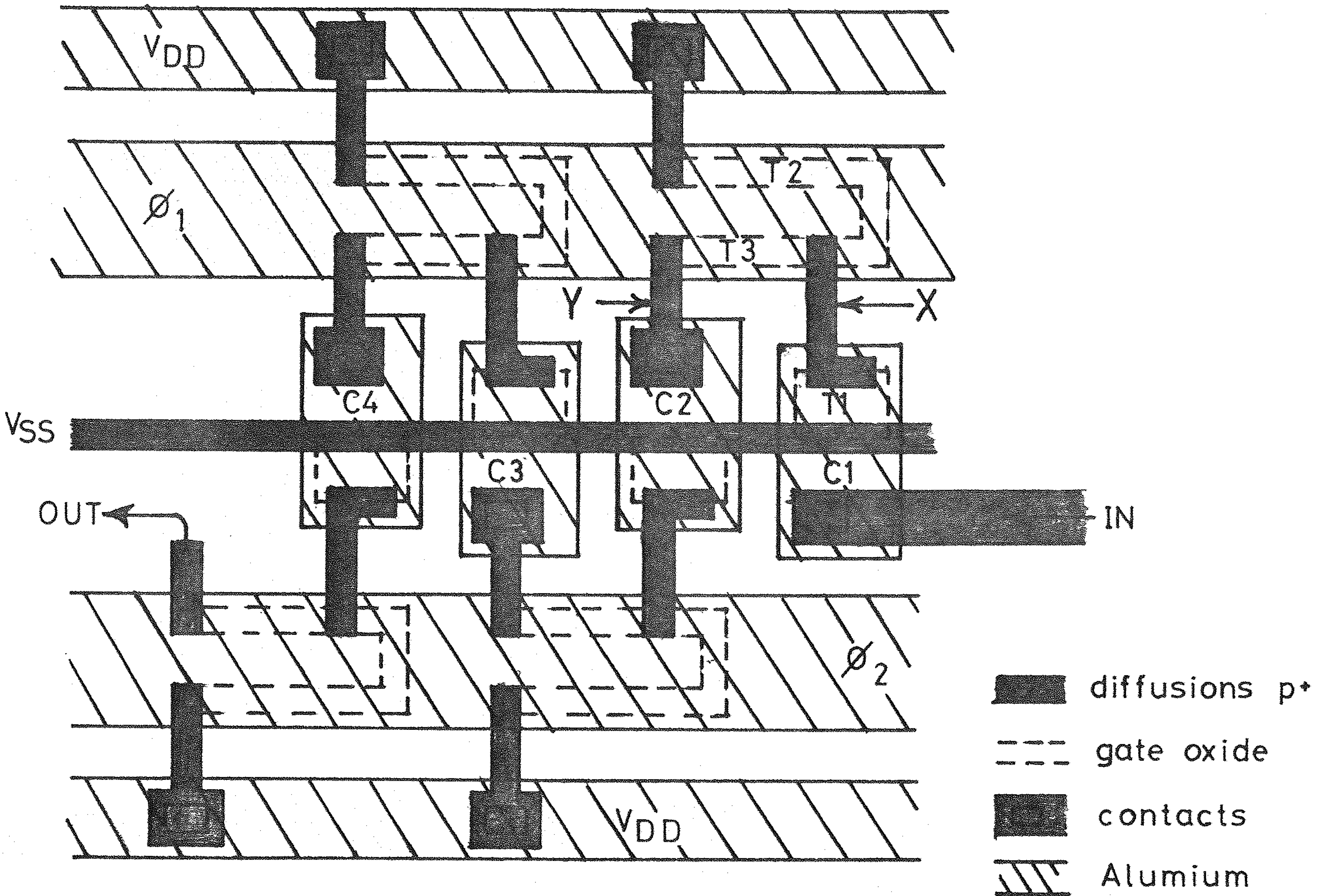


Fig. 4.8 Layout of the shift register circuit components

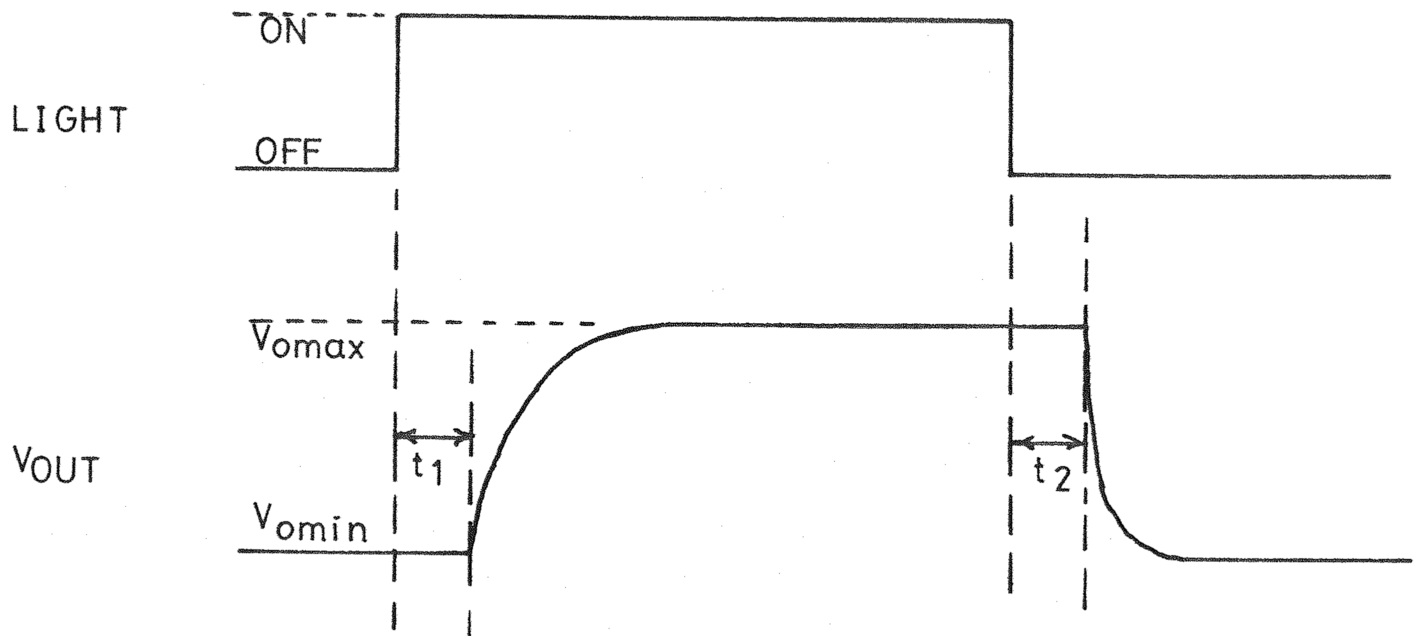
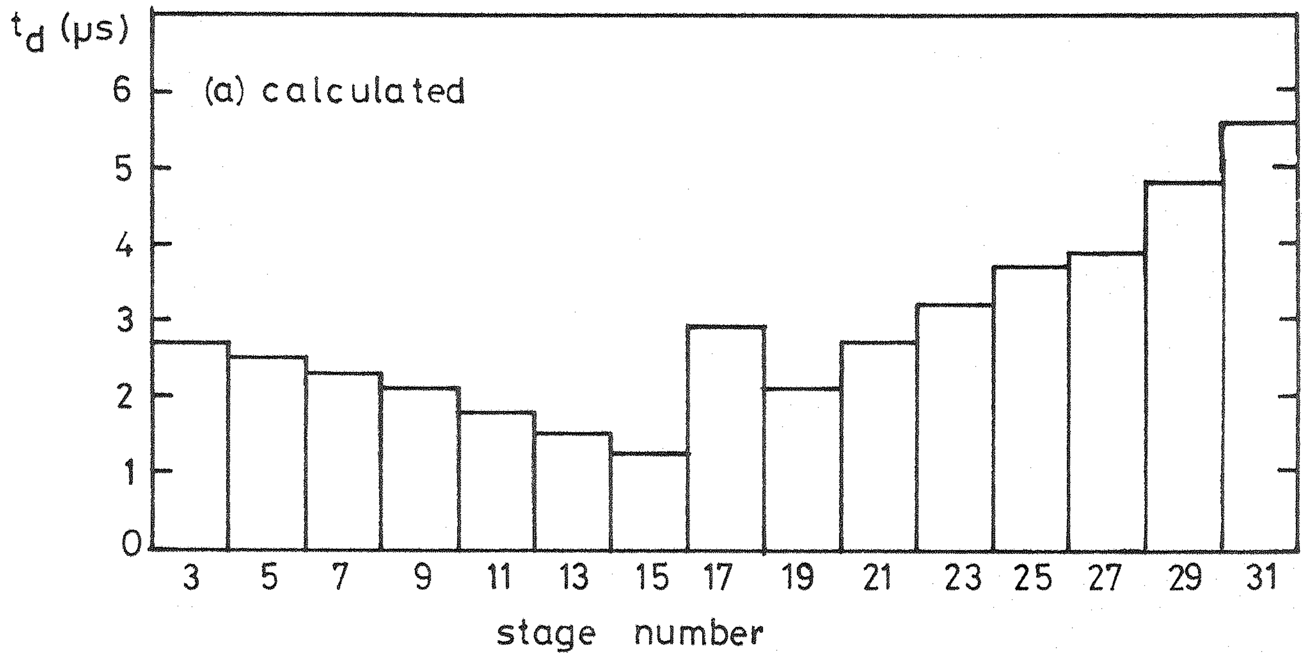


Fig. 4.9 Typical oscilloscope waveforms for the measurement of delay times.



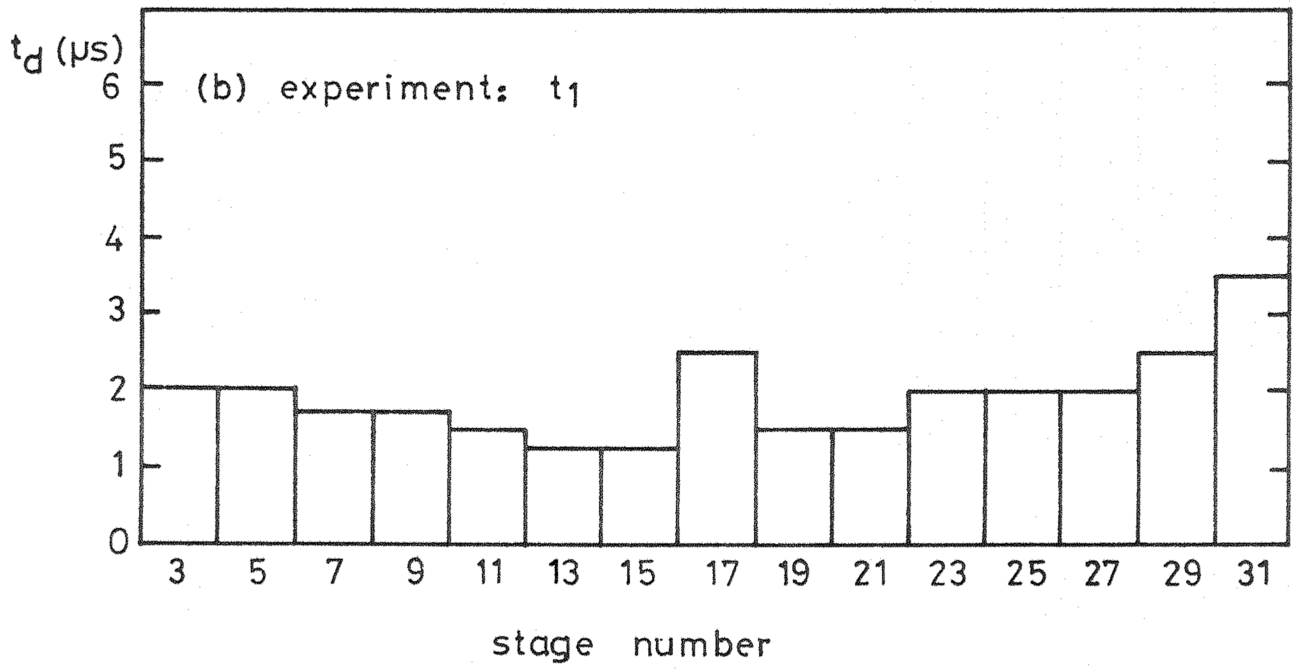


Fig. 4.10 Delay times from each (odd-numbered) inverter stage.

data of table 4.3, while Figure 4.10(b) presents the experimental results obtained by the technique described above. Two points are worth noting in this figure: (i) the magnitudes of the measured delay times are about 25% lower than the calculated ones; and (ii) while the agreement is not perfect, the overall shapes of these histograms are very similar, showing a gradual decrease from stage 3 to stage 15, the jump at stage 17 due to the large value of C_{17} (0.45 pF instead of 0.28 pF) and the gradual increase from stage 19 to stage 31.

To obtain additional information on the delay times, two more experiments were performed. In the first of these, the total propagation delay time from the input to the output of the SR was measured while data was applied electrically (and the SR chip was in darkness). This was then compared with the results obtained when the data was injected optically into position 'X' in Figure 4.7. The results thus obtained were:

$$t_{1_{electrical}} = 36.0 \ \mu s \tag{4.13a}$$

$$t_{1_{optical}} = 29.0 \ \mu s \tag{4.13b}$$

where the measured time in both experiments was t_1 of Figure 4.9. The subscripts electrical and optical, refer to the method of application of the input data. The results of the optical experiment are lower than the electrical by about 19%.

The second experiment was the measurement of the maximum clock-rate. From the discussion at the end of section 4.3.2(c) it was observed that a measurement of the maximum clock-rate will furnish the delay time of the stage with the longest delay. The experiment was performed with both types of data application (i.e. electrically, at the input with the chip in darkness; and optically, into any stage of the SR).

4.4.1 Measurement of the Maximum Clock-rate

Refer to Figure 4.11 which will be used to describe the technique used in the measurement of the maximum clock-rate. As shown in Figure 4.11(b) the input data was synchronised to the ϕ_1 clock and had a length equal to the clock period, T. During the electrical application of the data (at the input of the SR), the input signal switched from 0 V (OFF) to - 10 V (ON), thereby switching node [2'] from V_{omax} to V_{omin}. Optical injection of the data was achieved by grounding the input of the SR and directing the (intensity-modulated) laser beam into node [2'], i.e. point 'X', whence node [2'] switches from V_{omax} to 0 V.

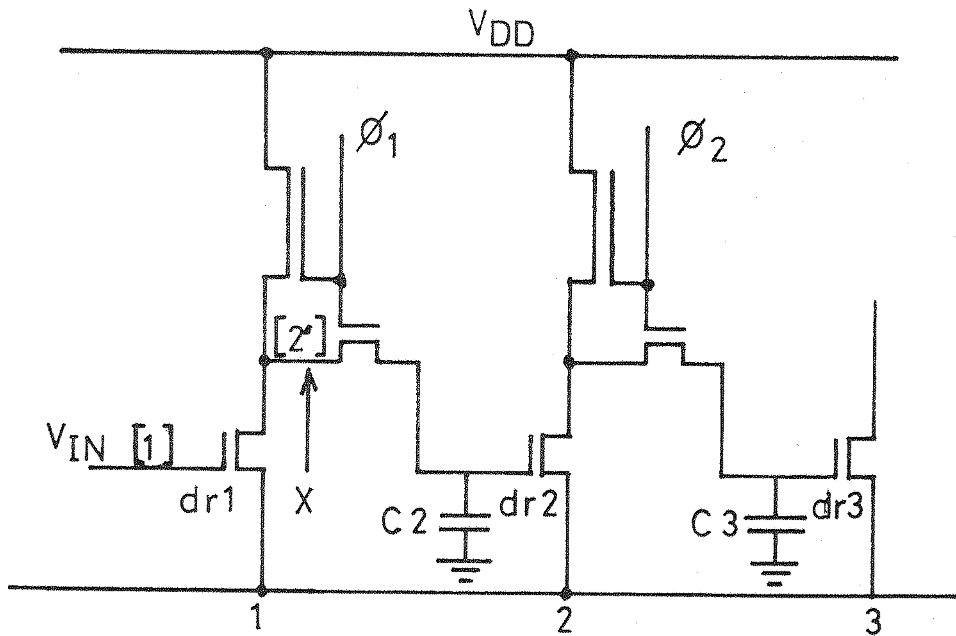
In either method of data application, when ϕ_1 is in its high state (- 10 V) for the period t_{ϕ_1}, the capacitance C_2 discharges to below V_{T2}, switching off driver transistor dr_2 (it is assumed here that $t_{\phi_1} >> t'_{F2}$ always). Next, with ϕ_1 held low, ϕ_2 changes from low to high for a period t_{ϕ_2}. This enables C_3 to charge up to V_{T3} in a time t'_{R3}. This data then gets passed on through the rest of the stages to the output of the SR by alternately clocking the ϕ_1 and ϕ_2 lines. If $t_{\phi_2} < t'_{R3}$, C_3 cannot get charged to V_{T3}, and hence the data is lost.

To obtain the limiting t_ϕ then, the clock frequency was gradually increased until the data at the output of the SR just disappeared, t_ϕ is then $t_{\phi Lim}$, and this time was measured. The results obtained for $t_{\phi Lim}$ are given below:

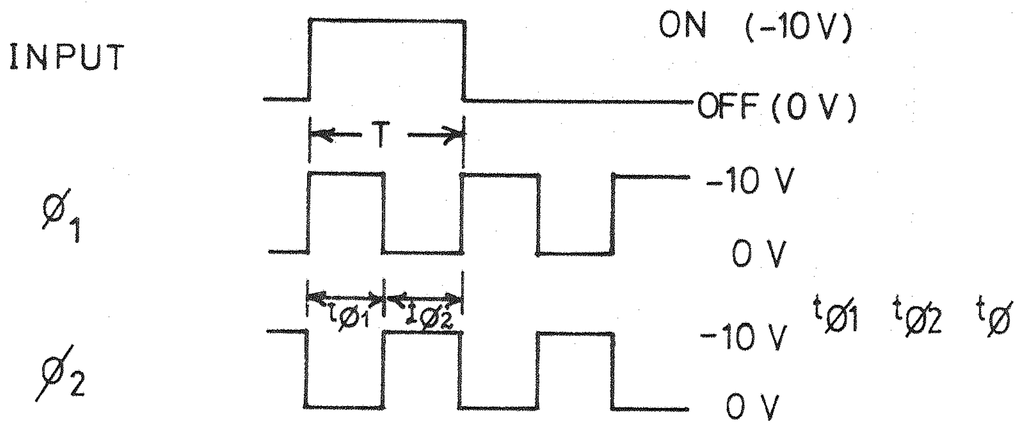
$$t_{\phi Lim(electrical)} = 5.0 \ \mu s \qquad (4.14a)$$

$$t_{\phi Lim(optical)} = 4.3 \ \mu s \qquad (4.14b)$$

where again the subscripts in brackets refer to the mode of application of the input data. In the optical case $t_{\phi Lim}$ was found to be the same for all stages.



(a)



(b)

Fig. 4.11 (a) Schematic of the SR (showing one-bit), and (b) the operating waveforms.

An attempt at explaining the differences between the electrical and optical experimental results, and also the difference between the predicted and measured delay times, has been made and will be presented in the next section, section 4.5.

4.5 Discussion of results

The results of the experiments described above show that: (i) there is a slight difference between the predicted delay times and those measured, and (ii) there also is a difference between the results of the electrical and optical experiments.

Consider first, the results of the electrical experiments and those predicted by the model. Two comparisons can be made here: (i) the total propagation delay, and (ii) the maximum clock-rate. The predicted data can be read off Table 4.3 and the measured data are given by equations 4.13a and 4.14a; these results are reproduced below.

	Predicted	Measured
Propagation delay time (μs)	43.04	36.0
$t_{\phi Lim}$ (μs)	5.6	5.0

Both these results indicate that the predicted times are longer than the actual times. Two probable sources of error in the calculated results are: (i) the effect of lateral diffusion on the value of the V_{ss} resistance, and (ii) the voltage dependence of the pn-junction capacitance contribution to the input capacity of each inverter.

The effect of the lateral diffusion is to reduce the calculated resistance by increasing the effective width of the resistor. The width is increased by about 20% of the diffusion junction depth[4.10]. In the present design, this would reduce the calculated resistance by about 6%, which would lead to a reduction in V_n and V_{Tn} (see Table 4.3)

of about 5% and 1% respectively. A reduction in V_{Tn} means reduced delay times; in particular the longest calculated t_d of 5.6 μs would reduce to about 5.2 μs, by this effect.

Although the sidewall capacitance[4.10] was taken into account in the calculation of the pn junction capacitance contribution to each inverter, this calculation was made assuming a 0 V bias to the junction. As the voltage at the inverter-input increases, this capacitance falls ($\sim 1/\sqrt{V}$), reducing the total inverter-input capacity, leading to a further reduction in t_d.

These two effects would explain the lower values of the delay times observed experimentally.

Next, let us compare the electrical and optical experimental results. Here again the electrical experiments provide only two data to be compared with the data of the optical experiments; these are reproduced below:

	Electrical	Optical
Propagation delay time (μs)	36.0	29.0
$t_{\phi Lim}$ (μs)	5.0	4.3

These results indicate that the optical results give slightly shorter times than the electrical. It has been stated earlier that the electrical measurements were obtained with the chip in darkness; this is because, during these measurements, the lid of the chip-package was closed. For the optical experiments though, the lid had to be removed so that the laser beam could reach the internal circuitry of the chip. It was assumed therefore, that the ambient light plus the scatter in the laser beam were responsible for the lower times observed in the optical

experiments. To confirm this, the electrical measurements were performed once more, but this time with the lid on the chip removed; and it was observed that indeed the propagation delay time fell from the 36.0 μs to about 30 μs and $t_{\phi Lim}$ fell from 5.0 μs to about 4.6 μs. These are considered near enough to the optical ones (t_d = 29.0 μs, $t_{\phi Lim}$ = 4.3 μs), to confirm that the ambient light was responsible for the shorter times observed in the optical experiments. The ambient light generates photocurrents at pn junctions thereby lowering the voltage on the junctions. The most pronounced effect is the generation of these photocurrents in the V_{ss} diffusion, this lowers the V_n's (and hence V_{Tn}'s) with a consequent reduction in the delay times.

4.6 Conclusions

The experiments described above show the great potential that the Laser testing technique has in testing integrated circuits. The experiments show how some of the circuit characteristics that might otherwise have been unobtainable can be very easily measured by using the laser probe; provided simple precautions are taken care of in the interpretation of the results.

The contribution to the total propagation delay from each inverter of the shift register circuit, for example, is very easily measured using the laser probe; while this might not have been as easily obtained otherwise. These results provide deeper insight into the internal operation of the integrated circuit, e.g. the characteristics at stage 17 of the SR.

The laser testing technique, coupled with conventional testing methods, should therefore make diagnostic testing of integrated circuits very much simpler. This should lead to much more efficient and hence faster testing schemes in the diagnostic testing of integrated circuits with a consequent reduction in the cost of the production of IC's.

CHAPTER FIVE

THEORY OF THE OPTICAL CHARACTERISTICS OF MOS TRANSISTORS

The optical characteristics of MOS transistors are of interest in connection with the use of the transistor as a photodetector (e.g. in laser testing of IC's, in MOS solar cells, and in CCD's as imagers). In the laser testing of IC's, the MOS transistor can be used as an optically activated switch; the switching being effected by directing the illumination at the gate region of the transistor. In MOS solar-cells and CCD imagers, the field induced pn junction of the MOS structure is used in a similar manner to the diffused pn junction. The MOS structure shows a higher sensitivity than the diffused pn junction, in the short wavelength region of the visible spectrum; this characteristic can be used to advantage in CCD imagers.

This chapter initially presents the optical characteristics of the MOS (induced pn junction) diode and compares these with those of the diffused pn junction. This is then followed in section 5.2 by a model for the MOS transistor photocurrents; the model being an extension of the MOS transistor theory to include the effects of illumination. The model also predicts that it is possible to operate the MOS-phototransistor in such a manner as to produce photocurrent amplification. This is achieved by operating the transistor with its substrate terminal connected to ground through a large resistance ($\sim$ 100 kΩ).

Section 5.3 develops the equations (based on the above model) that relate the transistor photocurrents to the rest of the parameters of the transistor. Section 5.4 considers the parameters which affect the photocurrent gain in the transistor and derives the relationships between these parameters and the gain. In section 5.5 we discuss the switching speed of the photocurrent amplifying configuration of the

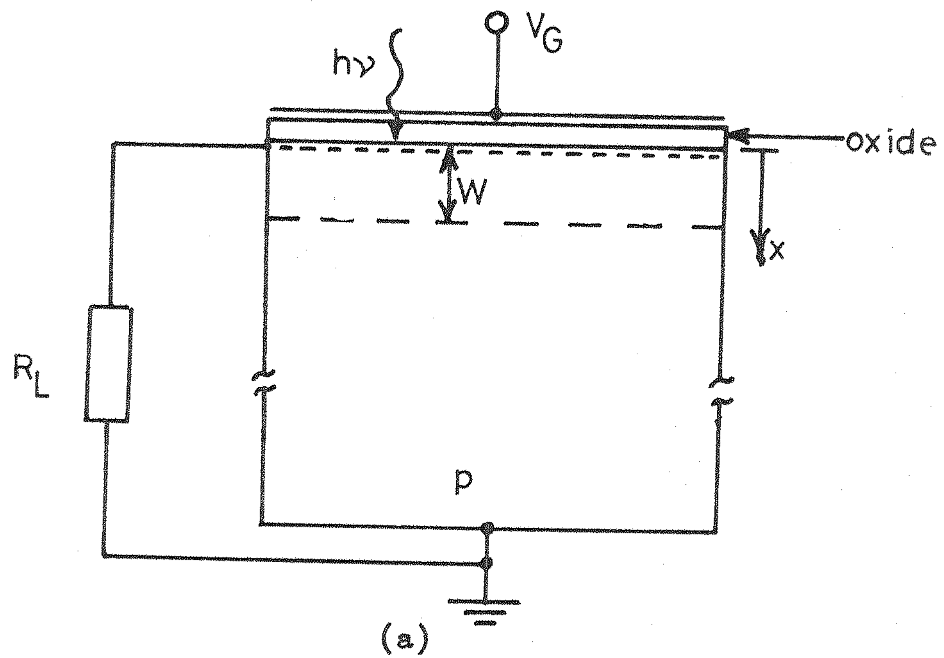
MOS transistor.

5.1 Optical Characteristics of the MOS Diode

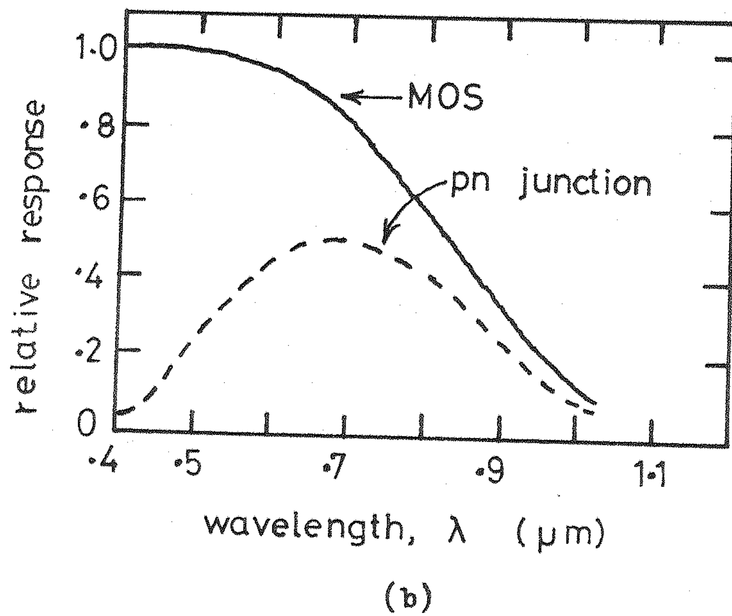
Refer to Figure 5.1(a) which is a one-dimensional representation of an MOS photocell. The positive gate voltage V_G applied to the gate metal (with respect to the grounded substrate) induces an n-inversion layer at the surface of the semiconductor and at the same time supports the space charge in the surface depletion region W. Contact can be made to the inversion layer, e.g. by diffusing a small n^+ contact region or otherwise[5.1-5.7].

Since the detector is a vertical collection device, it can be modelled as a one-dimensional structure[5.3]. The two dimensional effects caused by the inversion-layer sheet resistance can be applied as modifications to the one dimensional theory[5.3]. In developing the theory we will make use of the assumptions used in Chapter 3, in the analysis of the diffused pn junction photocell: i.e. that (a) the semi-conductor quantum efficiency is unity, (b) the sample thickness is semi-infinite and (c) we consider only low-level injection. In addition we will assume that recombination and thermal generation within the surface depletion layer (w) is negligible. We will also assume a monochromatic source of illumination. The analysis closely follows the work of W. W. Gartner[5.4].

The total photocurrent density through the depeletion layer (Jph) is the sum of the drift current density (Jdr) due to carriers generated inside the depletion layer, and the diffusion current density (Jdiff) of minority carriers generated outside the depletion layer in the bulk of the semiconductor and diffusing into the junction. The generation rate at a distance x in the semiconductor is G(x), and is given by



(a)



(b)

Fig. 5.1 (a) An MOS photocell under illumination, (b) comparison of the MOS photocell spectral characteristics with those of the pn-junction; W=2.0 um, L_n=10.0 um.

equation 2.2 of Chapter 2. The drift current density is given by:

$$Jdr = -q \int_{o}^{w} G(x)\, dx = -q\, \phi_o \,(1 - e^{-\alpha w}) \tag{5.1}$$

The electron diffusion equation in the bulk region of the semiconductor ($x > w$) can be written as:

$$D_n \frac{d^2 n}{dx^2} - \frac{n_p - n_{po}}{\tau_n} + G(x) = o \tag{5.2}$$

where D_n and τ_n are the electron diffusion coefficient and lifetime in the bulk, respectively; and are related to L_n by $L_n = \sqrt{D_n \tau_n}$. n_p is the electron concentration in the p substrate and n_{po} its equilibrium concentration. Equation 5.2 can be solved with the boundary conditions that $n_{p(\infty)} = n_{po}$, and $n_{p(w)}$ is approximately zero; to give the diffusion component of the photocurrent, Jdiff, entering the space charge layer at $x = w$, (see for example W. W. Gartner, ref. 5.4):

$$Jdiff = -q\, \phi_o \left(\frac{\alpha L_n}{1 + \alpha L_n}\right) e^{-\alpha w} - q n_{po} \frac{D_n}{L_n} \tag{5.3}$$

The total photocurrent density is given by the sum of the drift and diffusion components:

$$Jph = Jdr + Jdiff = -q\, \phi_o \left(1 - \frac{e^{-\alpha w}}{1 + \alpha L_n}\right) - q n_{po} \frac{D_n}{L_n} \tag{5.4}$$

The last term in equation 5.4 is independent of illumination, and is the diffusion current due to thermal generation in the bulk, and is negligible for appreciable levels of illumination. The spectral response

of the photocurrent, for a constant photon flux at each wavelength, is therefore given by:

$$Jph \sim \left(1 - \frac{e^{-\alpha w}}{1 + \alpha L_n}\right) \tag{5.5}$$

In Figure 5.1(b) we have plotted the spectral response of the MOS photocell as given by equation 5.5 (using the absorption coefficient data of ref. 2.3), together with the pn junction response given in Figure 2.2. To enable comparison with the pn junction response, the depletion width is set equal to the pn junction depth (2.0 μm) and L_n has been chosen to be the same (10.0 μm) as that for the pn junction diode. It will be noticed that the MOS photocell provides a better response to light in the short-wavelength region of the visible spectrum than the diffused pn junction photocell.

In a practical device, the response is modified by the optical transmission characteristics of the surface layers on the device: oxide in the case of the pn junction, and oxide + gate electrode in the case of the MOS photocell. In the case of the polysilicon-gate MOS devices (to be studied in the next chapter), the light reaching the semiconductor passes through 3 thin films: an oxide layer, polysilicon, and finally the gate oxide. In passing through these layers the light suffers attenuation due to absorption. There will also be multiple-reflection interference in these films. Because of these effects, practical results depart from the theoretical form of Figure 5.1(b) (the optical transmission characteristics ($T(\lambda)$) of the polysilicon-gate of the MOS device will be dealt with in section 5.1.1 of this chapter). At high current levels, the series resistance in the cells will reduce the magnitude of the photocurrent. This will also modify the practical response of the cells.

Gorban et al[5.5] reported the experimental results of comparing the spectral characteristics of an MOS photocell and a commercial pn junction photocell. Their MOS photocell was made on sufficiently high resistivity p-type silicon material (5-10Ω.cm) so that the built-in oxide charge was sufficient to ensure the presence of an induced inversion layer at the oxide-semiconductor interface without the need of a gate electrode. Their results are reproduced in Figure 5.2; and they show that the ultraviolet sensitivity of the MOS photocell is about an order of magnitude higher than the diffused pn junction photocell. These results have also been reported by Okamoto[5.1]. The high ultraviolet photosensitivity of the MOS photocell is due to low surface recombination losses (compared with the relatively high surface recombination in the diffused n-region of the pn junction photocell)[5.1,5.3].

5.1.1 Optical transmission through the gate layers of a polysilicon-gate MOS diode

Figure 5.3 illustrates the path of light through the gate layers of a polysilicon-gate MOS diode. The treatment of the optical transmission through these thin films has been adapted from Heavens[5.8], and is presented in Appendix A2. Only the case of normal incidence has been considered. The transmission, which is dependent on the wavelength (λ) of the illumination is given by:

$$T(\lambda) = \left|\frac{n_4}{n_o}\right| \cdot \left|t_{1234}\right|^2 \qquad (5.6)$$

where n_o and n_4 are the refractive indices of air and the semiconductor, respectively; t_{1234} is the effective Fresnel transmission coefficient of the 4 interfaces (labelled 1-4 in Figure 5.3), and is given in Appendix A2.

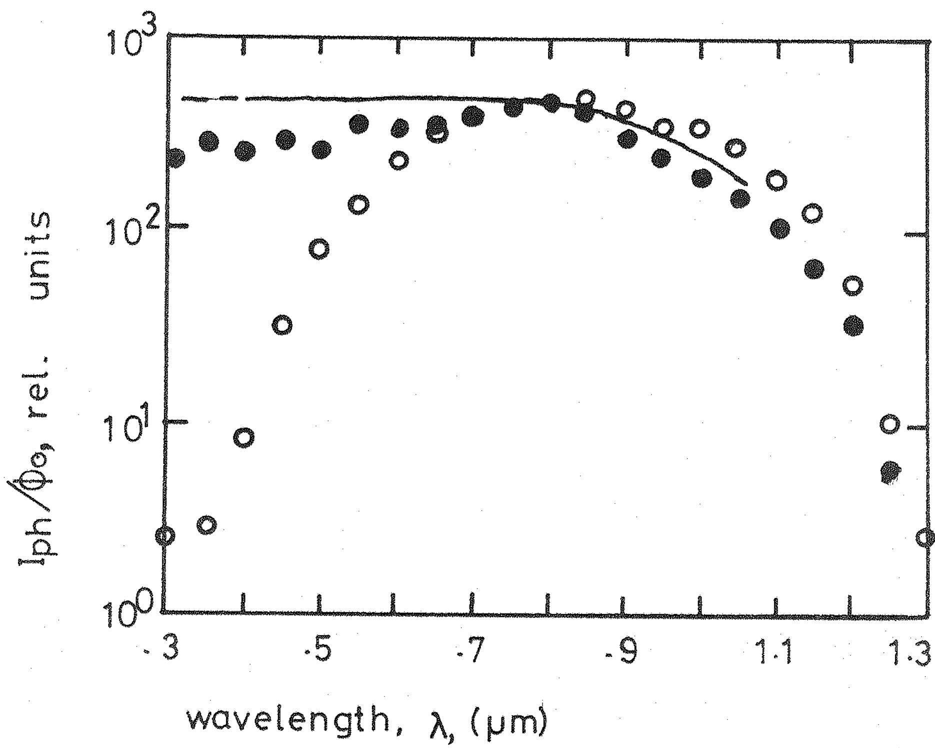


Fig. 5.2 Spectral characteristics of an MOS photocell (● ● ● ●), and an FD-7K pn junction photocell (o o o). The continuous line is the theoretical MOS photocell characteristic (after Gorban et al, ref. 5.5).

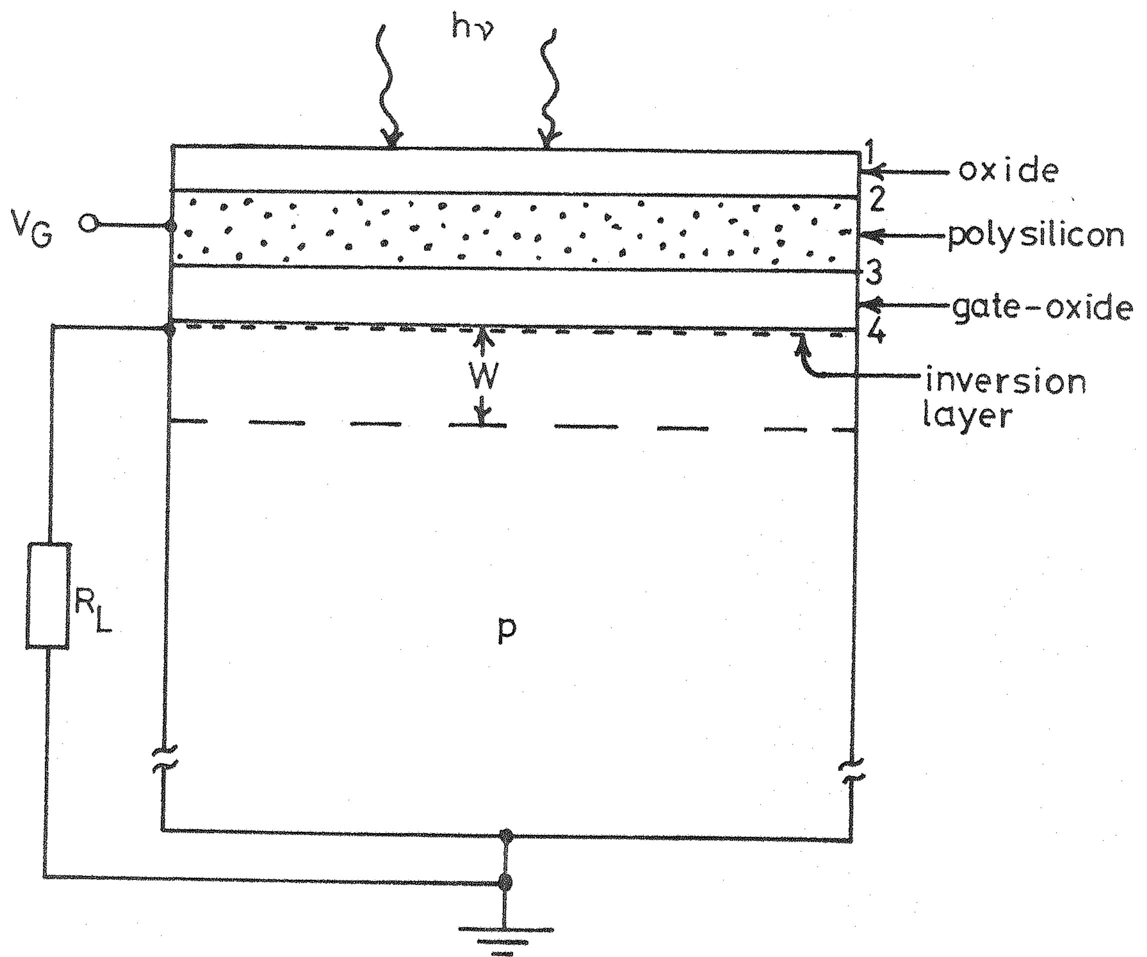


Fig. 5.3 A polysilicon-gate MOS photocell under illumination.

5.1.2 Spectral characteristics of the photocurrent of the polysilicon gate MOS diode

The photocurrent density in an MOS diode is given by equation 5.4:

$$Jph = -q\,\phi_o \left(1 - \frac{e^{-\alpha w}}{1 + \alpha L_n}\right) - q n_{po} \frac{D_n}{L_n} \qquad (5.7)$$

The photon flux density at the semiconductor surface (ϕ) is determined by the optical transmission T (= T(λ)); i.e.

$$\phi = T \cdot \phi_o \qquad (5.8)$$

In discussing the spectral response of the photocurrent, the second term in equation 5.7 can be dropped, since it is independent of ϕ. Applying this simplification the spectral characteristics of the photocurrent can be obtained by writing equation 5.7 using equations 5.6 and 5.8, i.e.:

$$Jph \cong -q \left|\frac{n_4}{n_o}\right| \cdot \left|t_{1234}\right|^2 \cdot \phi_o \left(1 - \frac{e^{-\alpha w}}{1 + \alpha L_n}\right) \qquad (5.9)$$

A normalised equation 5.9 (normalised to $q\phi_o$) is plotted in Figure 5.4 for values of d_1, d_2 and d_3 (i.e. the top oxide, the polysilicon layer, and the gate oxide thickness respectively) of 0.12 μm, 0.195 μm and 0.15 μm, respectively. The refractive indices of the materials used in the calculations have been obtained from ref. 5.7 and the absorption coefficients of the silicon layers have been obtained from references 5.9 and 5.10.

d1= .12 d2= .195 d3= .15

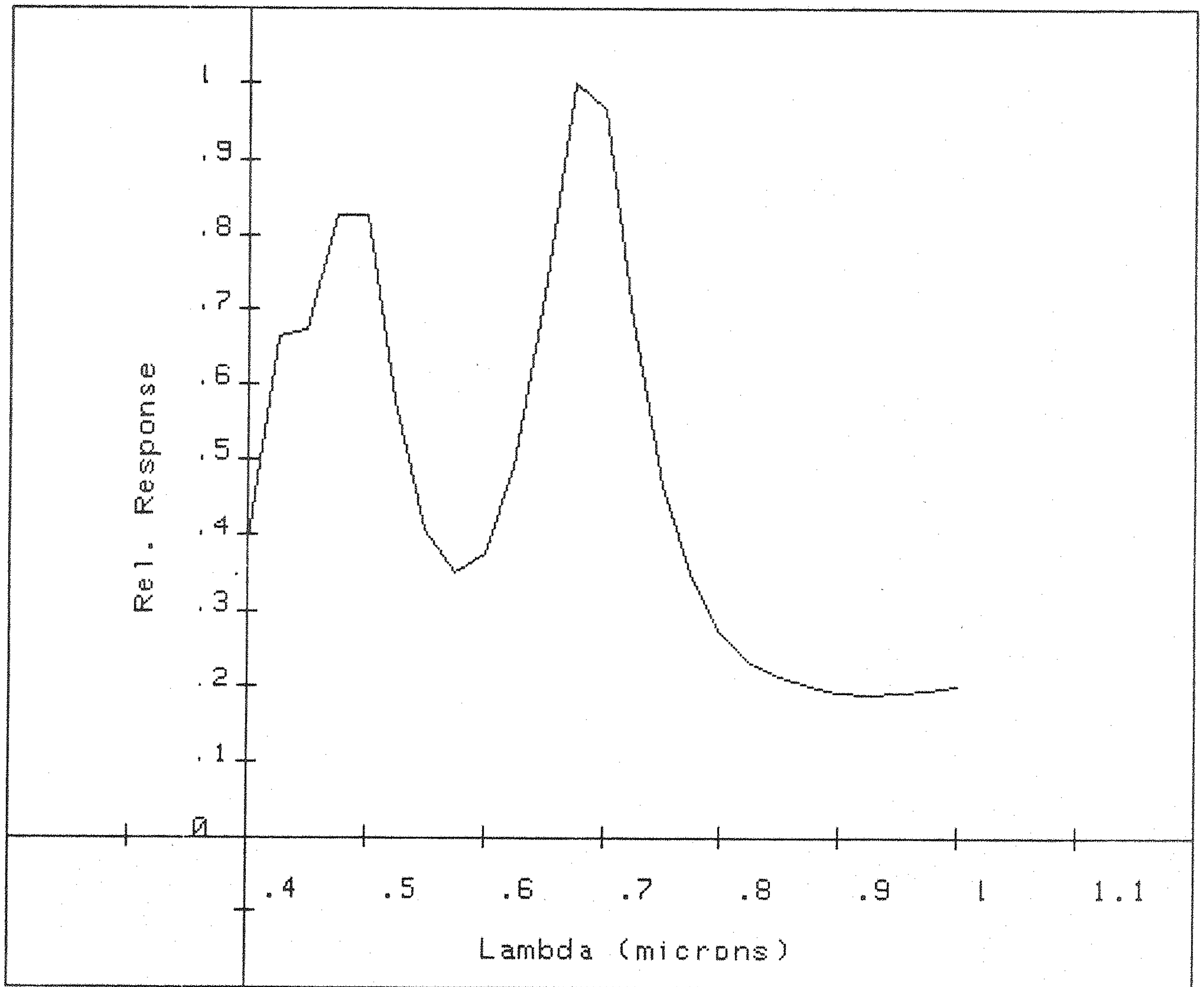


Fig. 5.4 Spectral response of a polysilicon gate MOS diode

5.2 Model of the MOS Transistor Photocurrents

In this section we consider the effect on the operation of the MOS transistor of illuminating its gate region. When considering the transistor, the vertical (x-directed, in Figure 5.5) photocurrent will be termed the Primary-photocurrent (I_{pr}), to distinguish it from the source-drain (y-directed) photocurrent, which will be termed the Drain-photocurrent (I_{dph}). The primary-photocurrent can be seen to be the same as the MOS diode-photocurrent just discussed above (in section 5.1); and this current can be measured at the substrate terminal of the transistor.

The white light response of the MOS transistor has been studied by several authors. Okamoto and Mochizuki[5.11] and Okamoto and Inoue[5.12] studied the effect of the position of a small illuminated spot through the gate, while Lam and Tong[5.13] studied the photocurrent observed when the light illuminated the entire gate electrode. In these studies the current studied was the increase in the drain current with illumination, the drain-photocurrent.

Card and Fang[5.14] and Shmyreva and Ivashchuk[5.15] were interested in the spectral response of the substrate-photocurrent (i.e. the increase in the substrate current with illumination, measured at the substrate terminal; this current is approximately equal to the primary-photocurrent). They also studied the dependence of this photocurrent on the gate, substrate, and drain biasses.

In none of the above studies did the authors compare the magnitudes of the drain-photocurrent and the substrate-photocurrent. In the present study we aim at finding this relationship between the transistor photocurrents.

Consider Figure 5.5, which is a representation of an illuminated NMOS transistor, and assume that the illumination fills the entire gate region. A photocurrent, generated in the manner described in section 5.1 for the MOS photocell, flows between the substrate (SUB) and the channel (at the surface, x=o) where it splits into two components; one component αI_{pr} flows through the drain terminal (D), and the other $(1-\alpha) I_{pr}$ through the source (S). This, the primary-photocurrent, can be measured in the substrate lead. In flowing from the channel-region to the substrate lead, I_{pr} generates a voltage (V_{ph}) in the substrate resistance (R_{sub}) (the substrate resistance referred to here is the series sum of the ohmic resistance of the bulk material, the contact-resistance of the substrate-contact, and any externally connected substrate resistance (R_{ext})). The polarity of V_{ph} is such as to forward bias the pn junction formed between the substrate p-region and the source-channel-drain n-region. This forward bias lowers the magnitude of the quasi-Fermi[5.16] potential of the minority carriers (electrons) which causes an increase in the electron concentration in the surface inversion region. This leads to a large increase in the drain current (in addition to αI_{pr} which also flows through the drain). The sum of the drain photocurrent that is due to V_{ph} ($F(V_{ph})$) and αI_{pr}, is the drain-photocurrent, I_{dph}. The ratio of the drain-photocurrent to the primary-photocurrent is here termed the 'Photocurrent-Gain' ($G_{ph} = I_{dph}/I_{pr}$). For a given value of I_{pr}, the magnitude of V_{ph} (and hence the drain-photocurrent due to V_{ph}), and G_{ph}, will depend upon the substrate resistance. The magnitudes of I_{dph} and G_{ph} are also dependent on the soure-drain voltage.

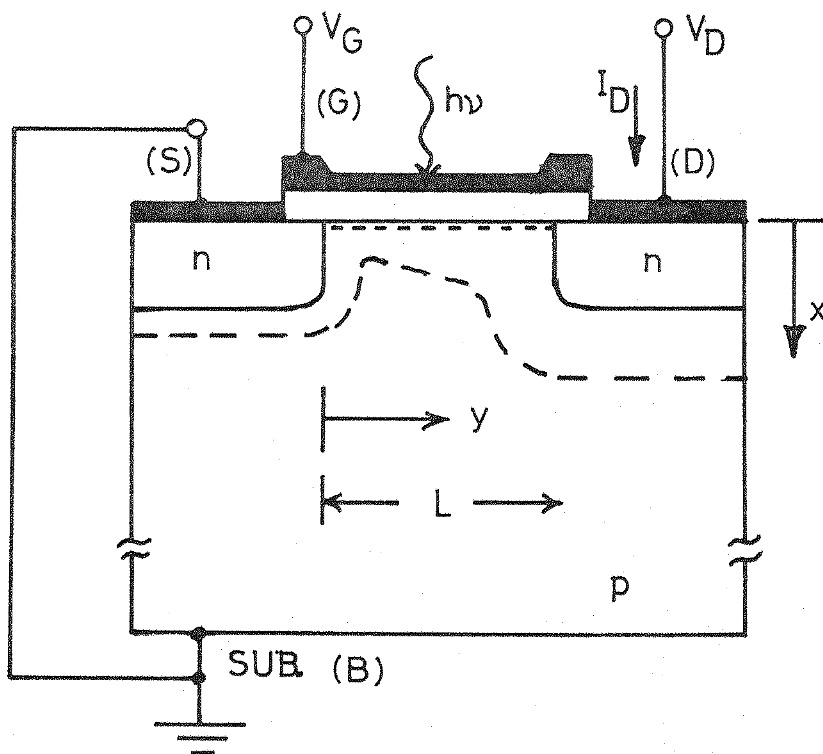


Fig. 5.5 An illuminated MOS transistor

5.3 Photocurrent Gain in MOS Transistors

The drain-photocurrent of an MOS transistor can be deduced by combining the theory of the MOS photodetector of section 5.1 with the theory of the MOS transistor, and the model described above. The theory of the MOS transistor has been treated in Appendix A1. The theory to be presented in this section is an extension of the theory in Appendix A1 to include the effects of illumination. An explanation of the terms to be used here can be found in this Appendix.

As depicted in Figure 5.6, the photovoltage (V_{ph}) generated by the primary photocurrent in the substrate resistance, lowers the quasi-Fermi level of the minority carriers from the no-illumination value of $U_F + \xi (\xi = \beta V_y)$ to a new value of $U_F + \xi'$ ($\xi' = \beta(V_y - V_{ph})$). This leads to new values for the surface potential ($U_s \rightarrow U_s'$), and the space charge density at the surface of the semiconductor.

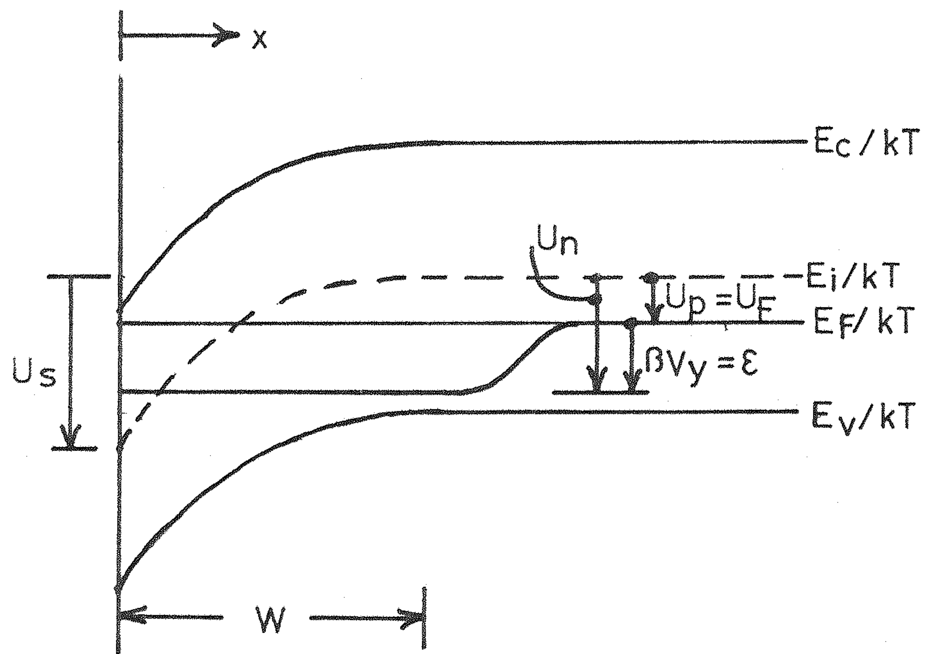
$$U_s' = 2U_F + (\xi - U_{ph}) + \ln \{\delta^2 (U_G - U_s')^2 - (U_s' - 1)\} \qquad (5.10)$$

$$Q_s' = \frac{-\varepsilon_s \sqrt{e^{U_F}}}{\beta L_i} \{e^{-U_s'} + U_s' - 1 + e^{-(2U_F + \xi - U_{ph})} (e^{U_s'} - 1)\}^{\frac{1}{2}}$$

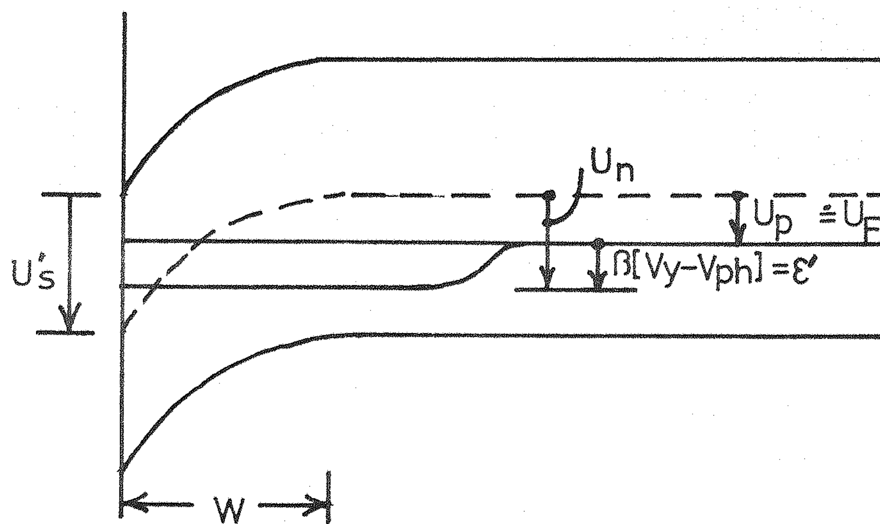
(5.11)

where $U_{ph} = \beta V_{ph}$. In these expressions we have implicitly used the assumption of low level injection (i.e. $U_p \simeq U_F$). Equation 5.10 shows that the surface potential gets reduced below the no-illumination value. We can now write expressions for Q_b and Q_n in terms of the new value of U_s given by equation 5.10

$$Q_b' \cong \frac{-\varepsilon_s \sqrt{e^{U_F}}}{\beta L_i} \{U_s' - 1\}^{\frac{1}{2}} \qquad (5.12)$$



(a) without illumination



(b) with illumination

Fig. 5.6 Potential variation at the semiconductor surface; (a) without illumination and (b) with illumination

$$-Q_n' \cong \frac{C_{ox}}{\beta}(U_G - U_s') - \frac{\varepsilon_s \sqrt{\ } e^{U_F}}{\beta L_i}(U_s' - 1)^{\frac{1}{2}} \tag{5.13}$$

From equation 5.13 we note that since now the value of U_s is lower than its no-illumination value, $|Q_n|$ has increased above its value without illumination, as expected. This increase in the channel charge $|Q_n|$ will increase the drain current for the same drain-source voltage.

From Appendix A1 (equations A1.28 and A1.29) we note that the drain current can be deduced from the following expressions:

$$J_n = -q\,\mu_n \left| -n\ (\partial\phi/\partial y + \frac{1}{\beta}\ (\partial n/\partial y)\right| \tag{5.14}$$

and

$$I_D = -Z\mu_n\ Q_n\ (\partial V/\partial y) \tag{5.15}$$

which show that the drain current is the sum of a drift-component and a diffusion-component. These expressions show that as Q_n increases (for a fixed drain-source voltage, or dV/dy), the drain current increases, and also that as the drain-source voltage (V_{DS}) increases, so will the drain current. A particular case as an example, is when the V_{DS} is greater than V_{Dsat} (the saturation drain-source voltage); with this condition Q_n at the drain end will be approximately zero, at the source end though, $|Q_n|$ will increase quite appreciably with illumination. This leads to a large increase in dn/dy, causing a large increase in the diffusion-current component of the drain current (see equation 5.14), in addition to the drift-current component.

Following the analysis of section A1.2 of Appendix A1 we can derive the expressions for the drain current that flows due to V_{ph}

when the transistor is illuminated; by re-writing equations A1.26, A1.32 and A1.33 in terms of U_s' and ε' $(\varepsilon' = \varepsilon - U_{ph})$.

$$U_s' = 2U_F + \varepsilon' + \ell n \; \{\delta^2 \, (U_G - U_S')^2 - (U_s' - 1)\} \tag{5.16}$$

$$I_D' = - \int_{U_S'(o)}^{U_S'(L)} Q_n(U_G, U_S') \cdot \frac{d\varepsilon'}{dU_s'} \cdot dU_s' \tag{5.17}$$

$$\frac{d\varepsilon'}{dU_s'} = \{1 + \frac{2\delta^2 (U_G - U_S') + 1}{\delta^2 (U_G - U_S')^2 - (U_S' - 1)}\} \tag{5.18}$$

Finally the expression for the drain current is obtained by integrating equation 5.17:

$$I_D' = \frac{C_{ox}}{\beta} \{(U_G + 2)\, U_s' - \frac{1}{2} U_s'^2 - \frac{2}{3\delta} (U_s' - 1)^{\frac{3}{2}} + \frac{4}{\delta} (U_s' - 1)^{\frac{1}{2}}$$

$$- \frac{1}{\delta} (2k - \frac{1}{\delta}) \; \ell n \left| k + (U_s' - 1)^{\frac{1}{2}} - \frac{1}{2\delta} \right|$$

$$+ \frac{1}{\delta} (2k + \frac{1}{\delta}) \; \ell n \left| k - (U_s' - 1)^{\frac{1}{2}} + \frac{1}{2\delta} \right| \} \Bigg|_{U_s'(o)}^{U_s'(L)} \tag{5.19}$$

The difference between the drain current given by equation 5.19 and that given by equation A1.39 of Appendix A1 (i.e. the drain current flowing in the absence of illumination) is the drain-photocurrent resulting from V_{ph}, i.e.

$$F(V_{ph}) = I_D' - I_D \tag{5.20}$$

The total drain-photocurrent is:

$$I_{dph} = F \; (V_{ph}) + \alpha I_{pr} \tag{5.21}$$

and the photocurrent-gain is:

$$G_{ph} = \{F(V_{ph}) + \alpha I_{pr}\}/I_{pr} \tag{5.22}$$

Figure 5.7 presents the calculated dependence, on I_{pr}, of (i) the drain-photocurrent (α assumed 0.5) and (ii) the photocurrent-gain, for a substrate resistance of 250 kΩ, a V_{DS} of 0.5V and a gate-source voltage (V_{GS}) of 1.0V. The values of the parameters for the transistor used in these calculations are typical of the transistors that have actually been made.

5.4 The Dependence of the Photocurrent-Gain on the Substrate Resistance

The inset to Figure 5.8 is a simplified equivalent circuit of an illuminated MOS transistor. The diode represents the pn junction formed between the p-substrate and the source-channel-drain n-region. The current source represents the primary photocurrent (flowing between the channel and the substrate). The photovoltage (V_{ph}) can be obtained by equating I_{pr} to the sum of the diode current and the current through the resistance (R_{sub}). The diode current is given by

$$I_D = I_s \left| \exp\left(\frac{\beta V_{ph}}{n} - 1 \right) \right| \tag{5.23}$$

where n is known as the diode quality factor and can have values between 1 and 2[5.17]. Therefore:

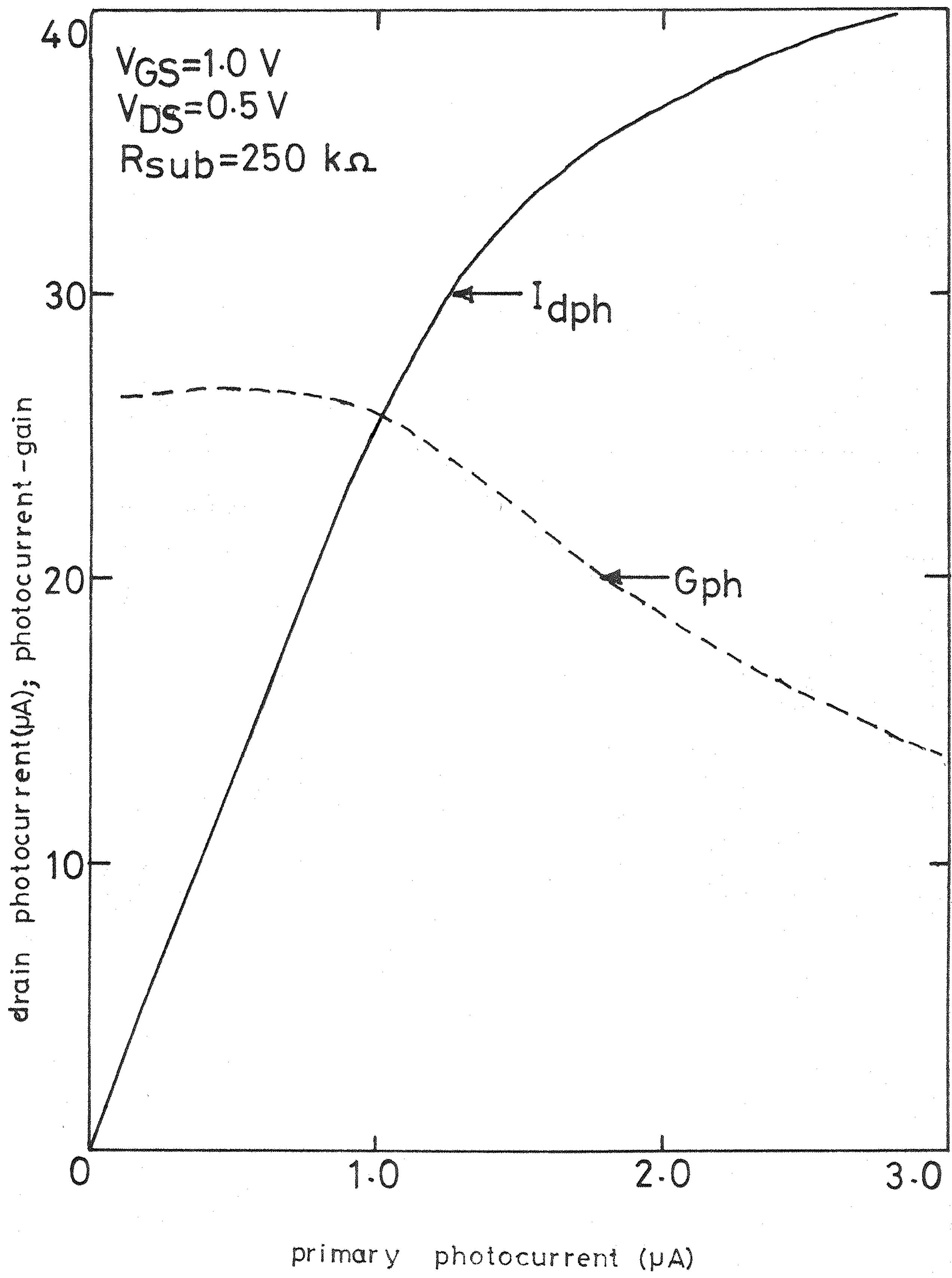


Fig. 5.7 The dependence of the drain photocurrent (————), and the photocurrent-gain (— — —), on the primary photocurrent; N_A = 3.0×10^{14} cm^{-3}, t_{ox} = 1500 Å, Z/L = 30.

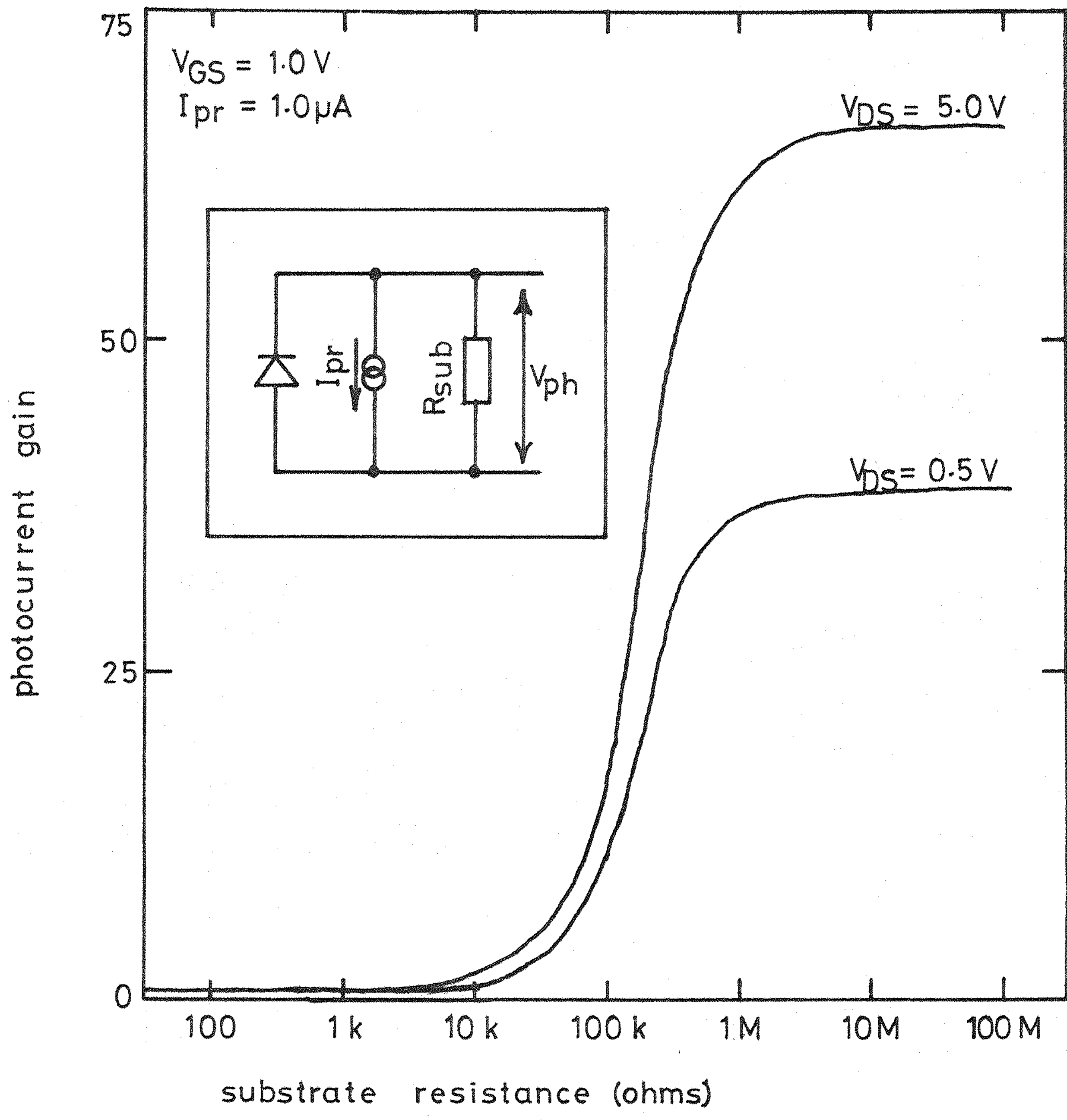


Fig. 5.8 The dependence of the photocurrent-gain on the substrate resistance, and the drain-source voltage

$$\frac{V_{ph}}{R_{sub}} + I_s \left| \exp\left(\frac{\beta V_{ph}}{n} - 1\right) \right| = I_{pr} \qquad (5.24)$$

or;

$$V_{ph} = I_{pr} R_{sub} - R_{sub} \cdot I_s \left| \exp\left(\frac{\beta V_{ph}}{n}\right) - 1 \right| \qquad (5.25)$$

This equation requires only a few computer iterations to give an accurate value of V_{ph}. Having obtained V_{ph}, equations 5.10 and 5.19 - 5.22 can be applied to obtain the drain-photocurrent and the photocurrent-gain.

The dependence of G_{ph} on R_{sub} has been calculated this way, for a value of the I_{pr} of 1.0 μA; and for two values of V_{DS} (0.5V and 5.0V), and the results are presented in Figure 5.8. The value chosen for the diode quality factor (n) and used in these calculations was 1.5; this value being typical of illuminated MOS structures[5.6,5.18,5.19]. The value of the diode reverse-saturation current (I_s) used in these calculations was 100 pA.

5.5 Switching Speed of the Photocurrent Amplifier

It has been postulated in this chapter that to obtain a large photocurrent amplification, the MOS transistor must be operated with a large resistance in the substrate lead. Figure 5.9 is a representation of the circuit that results when the transistor is operated in this manner. As shown in this circuit, when the substrate (terminal B in this diagram) is grounded, the source-substrate capacitance (C_{SB}) and the back contact-to-ground capacitance (C_{BCG}) are shorted out and therefore do not contribute to the switching speed of the transistor. Connecting a large valued resistor between the substrate and the ground results in an increase in the stray capacitance (i.e. capacitance

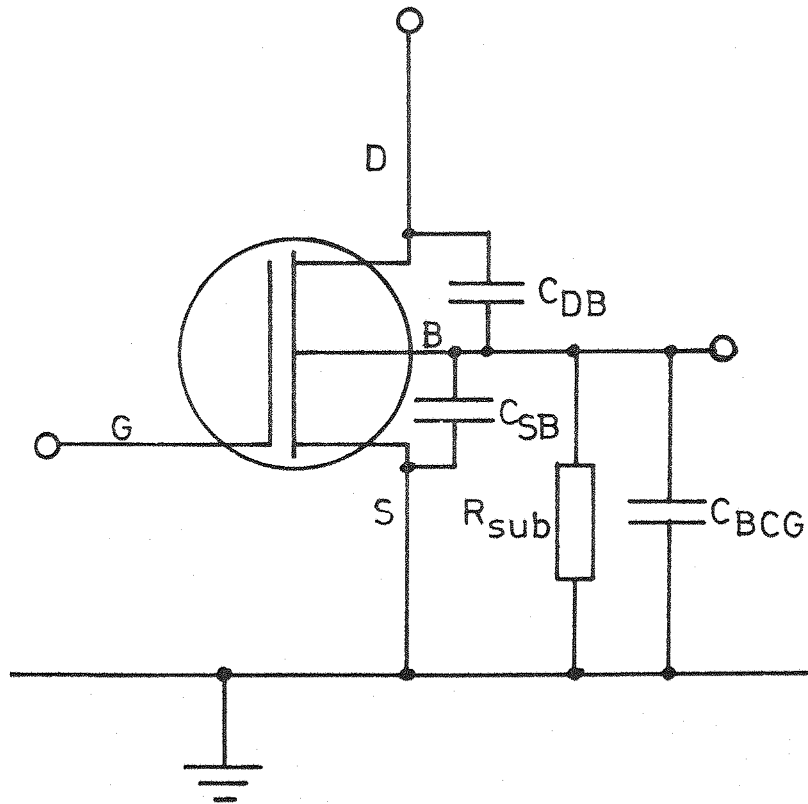


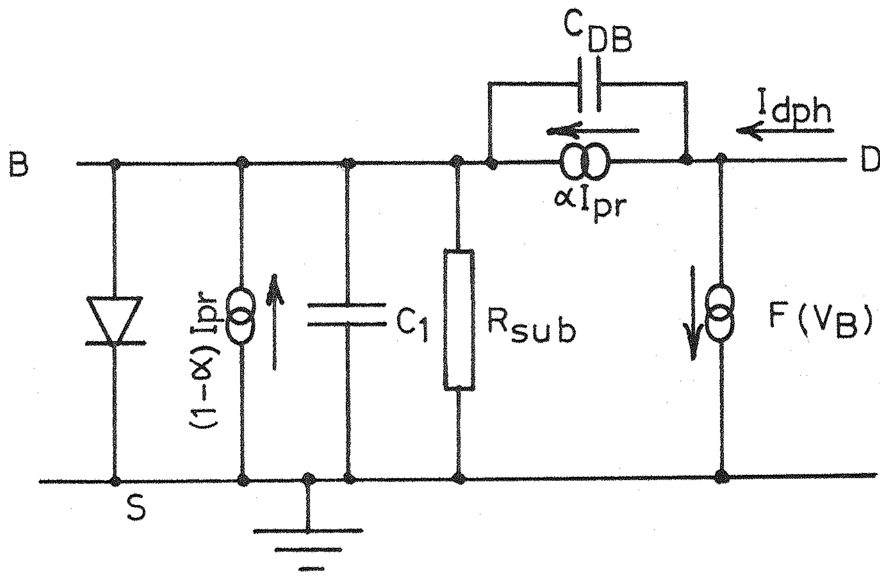
Fig. 5.9 An MOS transistor operated with a large valued substrate resistance

unnecessary for actual device operation) which degrades the switching speed; C_{SB} and C_{BCG} now contribute to the switching speed. Also, the effect of C_{DB} is increased by the Miller-effect.

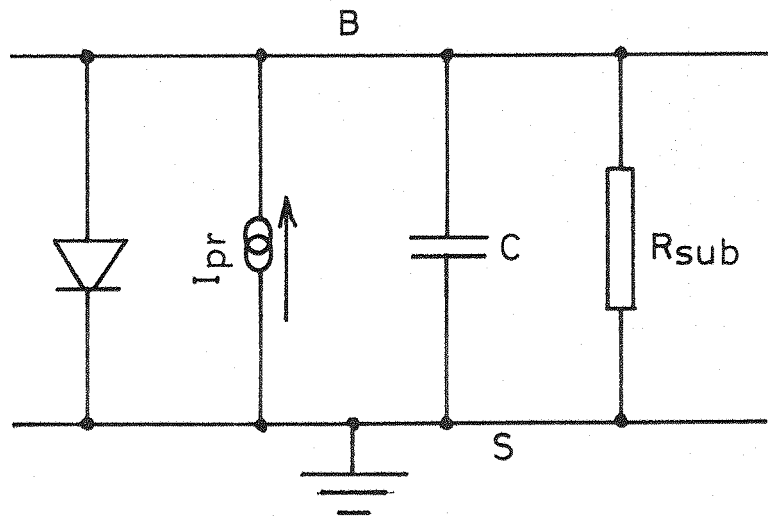
In the analysis of the switching speed of the photocurrent amplifying circuit we will assume that the switching speed of the intrinsic device (shown enclosed in a circle in Figure 5.9) is much much faster than the circuit external to the device, so that the overall switching speed is limited by the external circuit. The input signal of the photocurrent-amplifier is the primary-photocurrent, which develops a voltage in the substrate (B); the substrate voltage (V_B) produces the drain current $F(V_B)$, which adds to a fraction of the primary-photocurrent (αI_{pr}) to make the drain-photocurrent. Figure 5.10(a) is a representation of this effect. Isolating the input process, which is the generation of the voltage V_B by I_{pr}, results in Figure 5.10(b); where the capacitance C represents the sum of C_{SB}, C_{BCG} and $(1 + A_V)C_{DB}$ (the Miller-capacitance of C_{DB}), and A_V is the voltage gain from the substrate to the drain of the transistor. As this figure shows, the input circuit determines the overall switching speed of the amplifier. We will therefore restrict our analysis to the input circuit, Figure 5.10(b).

The voltage V_B is a function of I_{pr}; how fast V_B reaches its final value depends on how fast the capacitance C charges up. The rate at which C charges up depends on its value, the value of R_{sub}, and the current-voltage characteristics of the diode. The capacitor charging current is given by:

$$I_c = I_{pr} - (I_d + I_R) = C \frac{dV_B}{dt} \tag{5.26}$$



(a)



(b)

Fig. 5.10 (a) Equivalent circuit of the Photocurrent-amplifier showing the photocurrents, and (b) the equivalent of the input circuit: $C1 = C_{SB} + C_{BCG}$, and $C = C1 + (1+A_V)C_{DB}$

where I_d is the diode current (= I_s $|\exp \beta V_B/n - 1|$) and I_R is the current through R_{sub} (V_B/F_{sub}). The time taken for C to charge up to V is given by:

$$t = c \int_{o}^{V} \frac{dV_B}{I_{pr} - I_d - I_R} \qquad (5.27)$$

The risetime (t_r) will be defined as the time it takes C to charge up from 0.1 V_f to 0.9 V_f (where V_f is the final value of V_B). The final value of V_B can be obtained by setting C=o; $I_{pr} = I_d + I_R$ and solving for V (see equation 5.25).

t_r has been calculated for various values of R_{sub} at a primary photocurrent of 1.0 μA and C = 1.0 pF, and, as in section 5.4, the diode characteristics used in these calculations were n = 1.5 and I_s = 100 pA. The results are presented in Figure 5.11. This figure shows that for very low values of the substrate resistance, the risetime is very short; this is because when R_{sub} is small, the risetime (which approaches the value 2.2 x RC) becomes small. As R_{sub} increases, so does the risetime, linearly at first (= 2.2 R x C) until it reaches a peak at about 350 kΩ, after which it falls to an asymptotic value with further increases in Rsub. The value of R_{sub} where the peak in the risetime falls is dependent on the magnitude of I_{pr}; being lower than 350 kΩ for I_{pr} > 1.0 μA and higher than 350 kΩ for I_{pr} < 1.0 μA.

A qualitative explanation for the shape of the risetime curve can be obtained by using a simplified picture of the process. Refer to Figure 5.12 which is a simplified pictorial representation of the process; and assume an ideal diode that switches on at a voltage V_d. For all resistances for which the final voltage (I_{pr} x R) is less than V_d, the

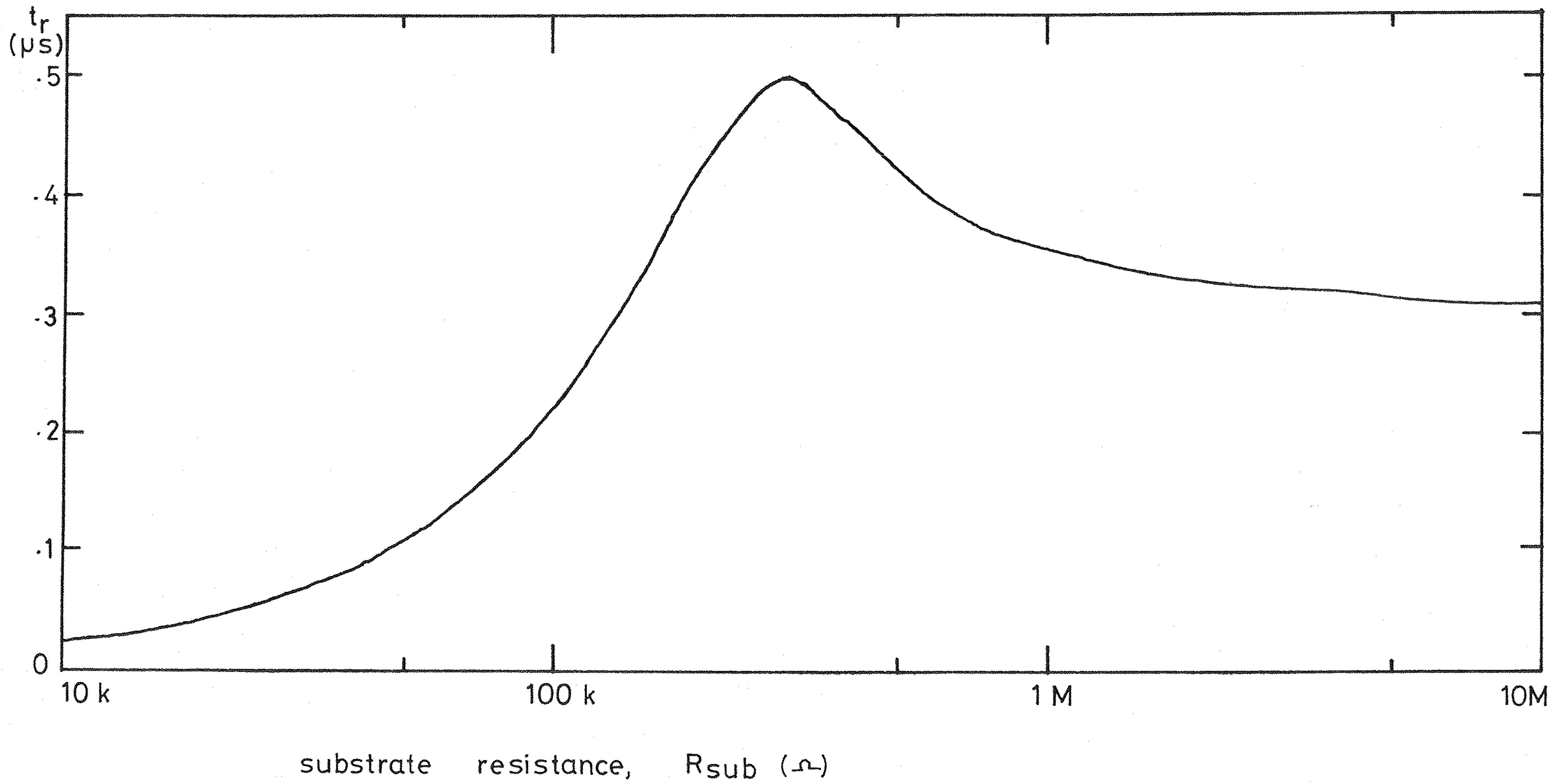


Fig. 5.11 The risetime (for 1.0 pF capacitance) of the substrate voltage of the photocurrent amplifier as a function of the substrate resistance.

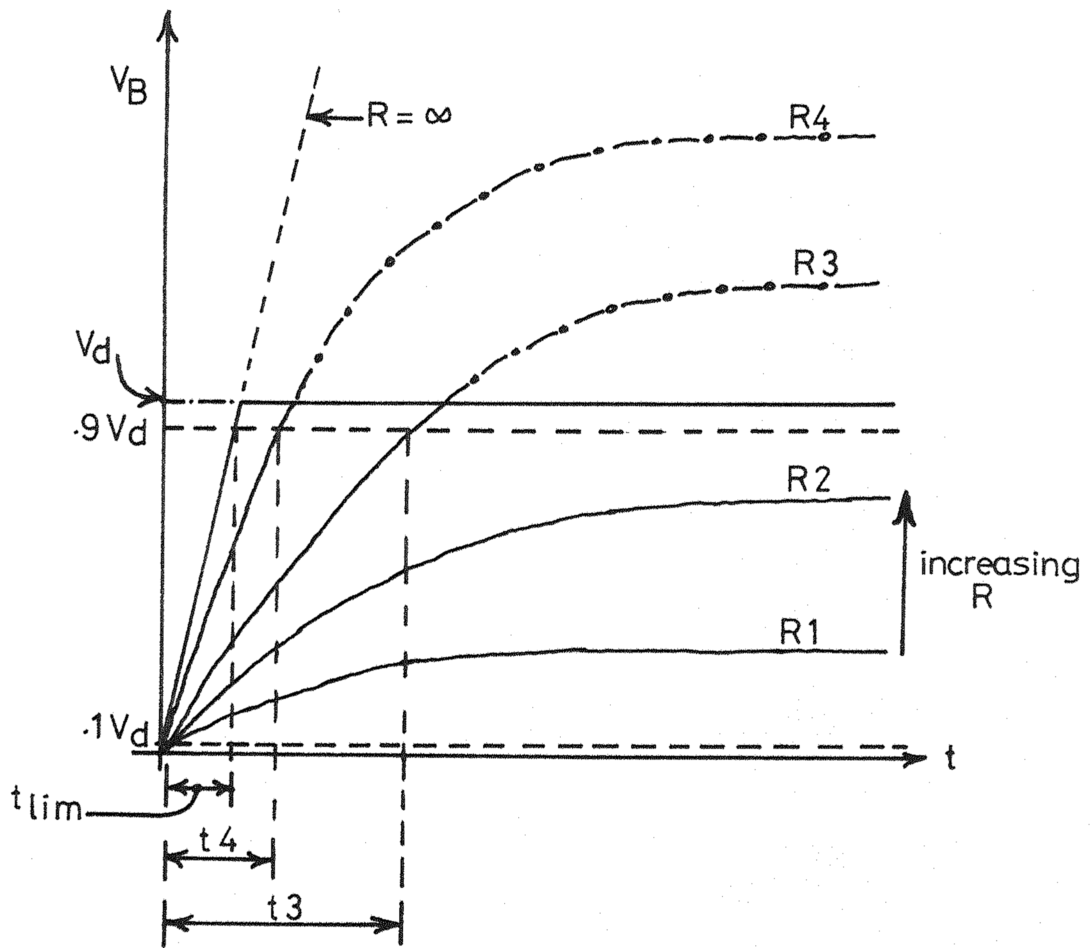


Fig. 5.12 Pictorial representation of the dependence of the risetime of the substrate voltage on the substrate resistance

risetime will be ≃ 2.2 x RC, and will therefore increase linearly with resistance (e.g. R_1 and R_2 in Figure 5.12). For resistances for which the product I_{pr} x R would be greater than V_d (e.g. R_3 and R_4) the risetime will be less than 2.2 x RC. For such resistors, the voltage would rise exponentially until it reached V_d where it would be clamped to this value. As depicted in Figure 5.12, as R increased, the risetime would fall to a limiting value t_{lim} (t_{lim} as shown would be given by 0.8 V_d x C/I_{pr}).

In the real situation, the diode starts conducting before the voltage reaches V_d reducing the capacitor charging current and therefore increasing the risetime.

The peak risetime of approximately 0.5 μs (for C = 1 pF) shown in Figure 5.11 is very much longer than the times associated with the intrinsic MOS transistor[5.20]; therefore the overall switching speed of the photocurrent amplifier is limited by these characteristics. The large capacitance between the substrate and ground will make this risetime very long leading to a degradation of the switching speed.

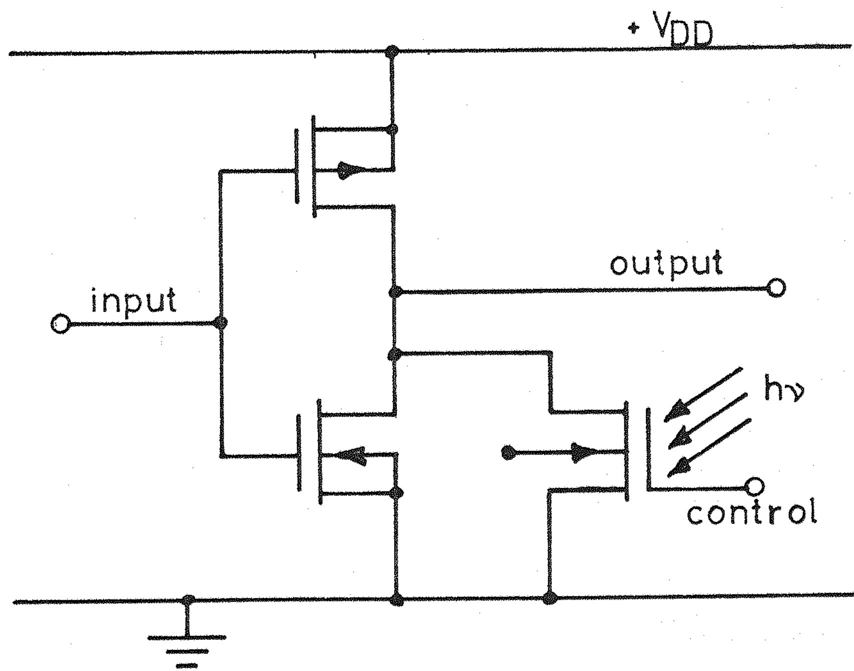
5.6 Discussions and Conclusions

It has been shown in this chapter that an MOS photodetector can provide a much better photosensitivity than a diffused pn junction in the visible spectrum; provided absorption and destructive-multiple reflection interference can be minimised, by a suitable choice of the gate materials. It has also been predicted that by operating an MOS transistor as a photodetector with its substrate connected to the source via a large resistance (∿ 100 kΩ), the transistor can provide photocurrent amplification (albeit at the expense of the transistor switching speed).

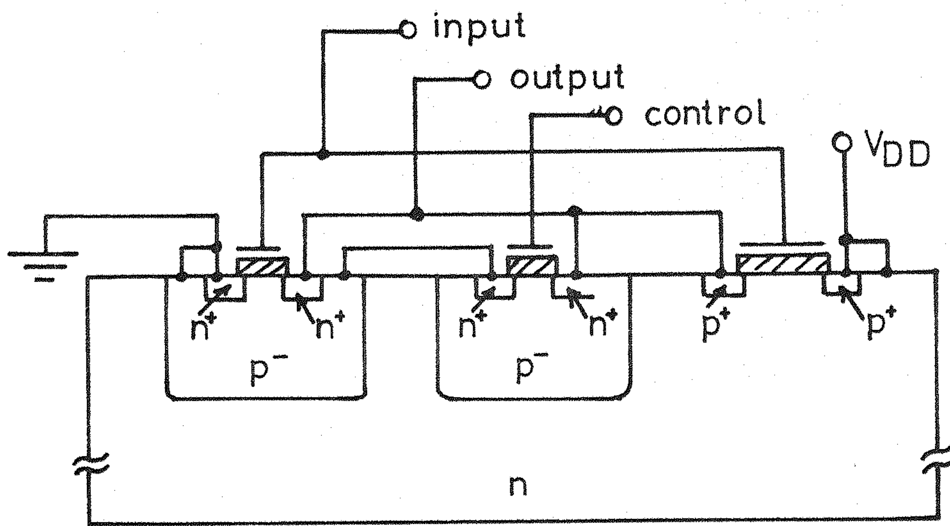
The photocurrent amplifying properties of the MOS transistor could be employed advantageously in the laser testing of integrated circuits. In section 3.2 of Chapter 3 we observed how CMOS digital circuits can be extremely difficult to test with a laser beam; this is because the laser beam power required to generate sufficient photocurrents to switch their logic states are very high. A photocurrent amplifying device like the one discussed above could be employed in a suitable position to provide large magnitudes of photocurrents for moderate laser beam powers, thereby reducing the laser power required to switch the circuit logic states. In the example of the CMOS digital circuit of Figure 3.2 (the inverter), this photocurrent amplifying device could replace the photodiode, see Figure 5.13(a). This structure can be integrated in the circuit very easily, as Figure 5.13(b) shows. In this circuit, the transistor being used as the photodetector has its substrate floating (i.e. R_{sub} is at its maximum), which means that its G_{ph} will be at its maximum, to its advantage in this application.

The ability of the MOS transistor to amplify photocurrents could also be a great disadvantage; especially if it appears in applications where it was not intended. This will indeed be the case where the substrate resistance is relatively high; either because the resistivity of the bulk material is high or because the method employed for making electrical contact to the substrate results in high contact resistance. Such a situation can lead to gross errors in the interpretation of results of optical experiments performed on such devices, if the effect is not fully appreciated.

We have observed in this chapter that the optical properties of an MOS transistor are very dependent on the actual design of the transistor.



(a)



(b)

Fig. 5.13 (a) Example of an application of an MOS phototransistor; (b) the circuit implemented in an integrated form.

An experimental device was designed and fabricated and used to test the theory presented in this chapter. The design and the optical characteristics of this device are presented in the next chapter.

CHAPTER SIX

MEASUREMENT OF THE OPTICAL CHARACTERISTICS OF A P-MOS TRANSISTOR

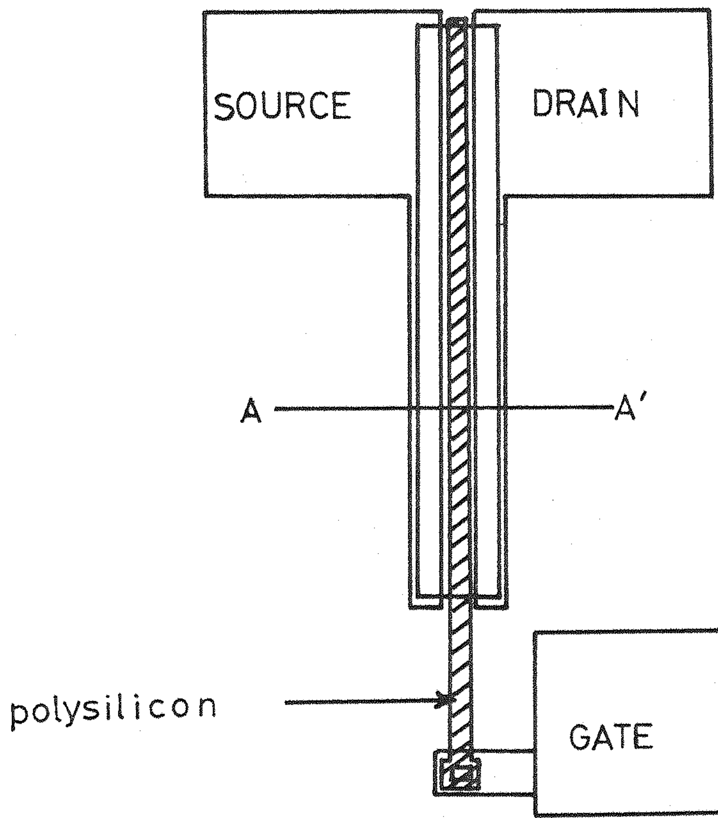
A p-MOS transistor was designed and fabricated to test the theory developed in Chapter 5. The device was an enhancement type, with polysilicon as the gate electrode. The gate electrode was made of polysilicon, so that the gate region of the transistor could be 'semi-transparent' to the incident illumination.

Section 6.1 presents the design and the processing parameters of the device, while section 6.2 presents the spectral characteristics of its photocurrents. In section 6.3 we present the photocurrent amplification properties of the device, followed by the measured switching speed in section 6.4. This is then followed by a discussion in section 6.5.

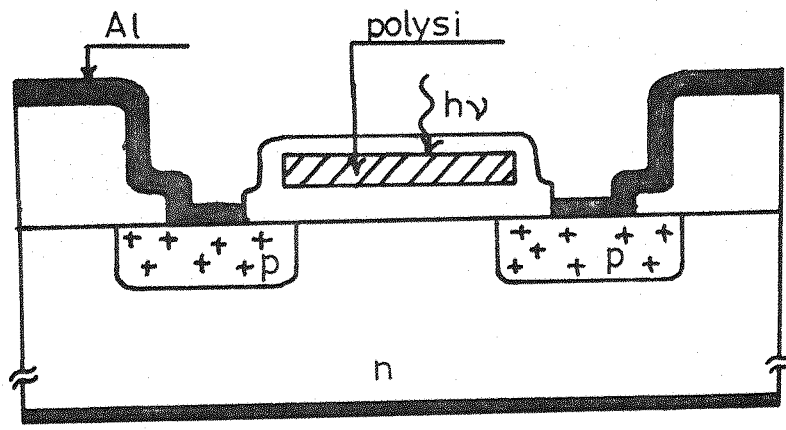
6.1 The Design of the MOS Phototransistor

In operating the MOS structure as a photodetector (e.g. in MOS solar cells and CCD image sensors), the illumination is directed at the gate region of the device. The incident light must penetrate the gate layers of the device to reach the semiconductor. This implies that the gate electrode must be made transparent. One way of achieving this requirement, without grossly modifying the standard processing sequence in the fabrication of the device, is to use polycrystalline silicon (polysilicon) as the gate electrode; hence the present device.

Figure 6.1 shows the outline of the polysilicon gate transistor that was designed and fabricated for the optical experiments. Figure 6.1(b) shows a sectional view of the transistor. This figure shows how the light focussed onto the gate area reaches the underlying semiconductor; by passing through an oxide layer, then through the polysilicon



(a)



(b)

Fig. 6.1 (a) Outline of the MOS phototransistor, (b) cross-sectional view; section through AA'

film, and finally through the gate-oxide layer. The transistor was fabricated using four basic masks shown in Figure 6.2. As shown in the photograph of the final chip (Figure 6.3) in addition to this transistor (shown as 'F' in the photo), the chip included several other test structures.

The devices were fabricated on Wacker n-type slice of <100> orientation, 8-16 Ωcm resistivity, and approximately 330 μm thickness. The processing sequence used in the fabrication of the devices is given in Appendix A3. Table 6.1 presents a summary of the processing parameters of the devices.

Table 6.1 : Characteristics of the Phototransistor

Substrate doping concentration, N_d	3×10^{14} cm^{-3}
Orientation	<100>
Isolation oxide thickness	0.60 μm
Gate-oxide thickness	1500 Å
Final polysilicon layer thickness	1950 Å
Diffused regions junction depth	1.5 μm
Dopant	Boron

6.2 Spectral Characteristics of the Photocurrents

The spectral characteristics of the MOS transistor photocurrents were measured using a Higler-Watts Monochromator with a tungsten filament lamp source. The incident light spectral characteristics were calibrated at the exit port of the monochromator using a United Detector Technology (UDT) Opto-meter model 40X which uses a 1 cm^2 PIN silicon photodiode as the basic sensor with a subtractive radiometric filter to

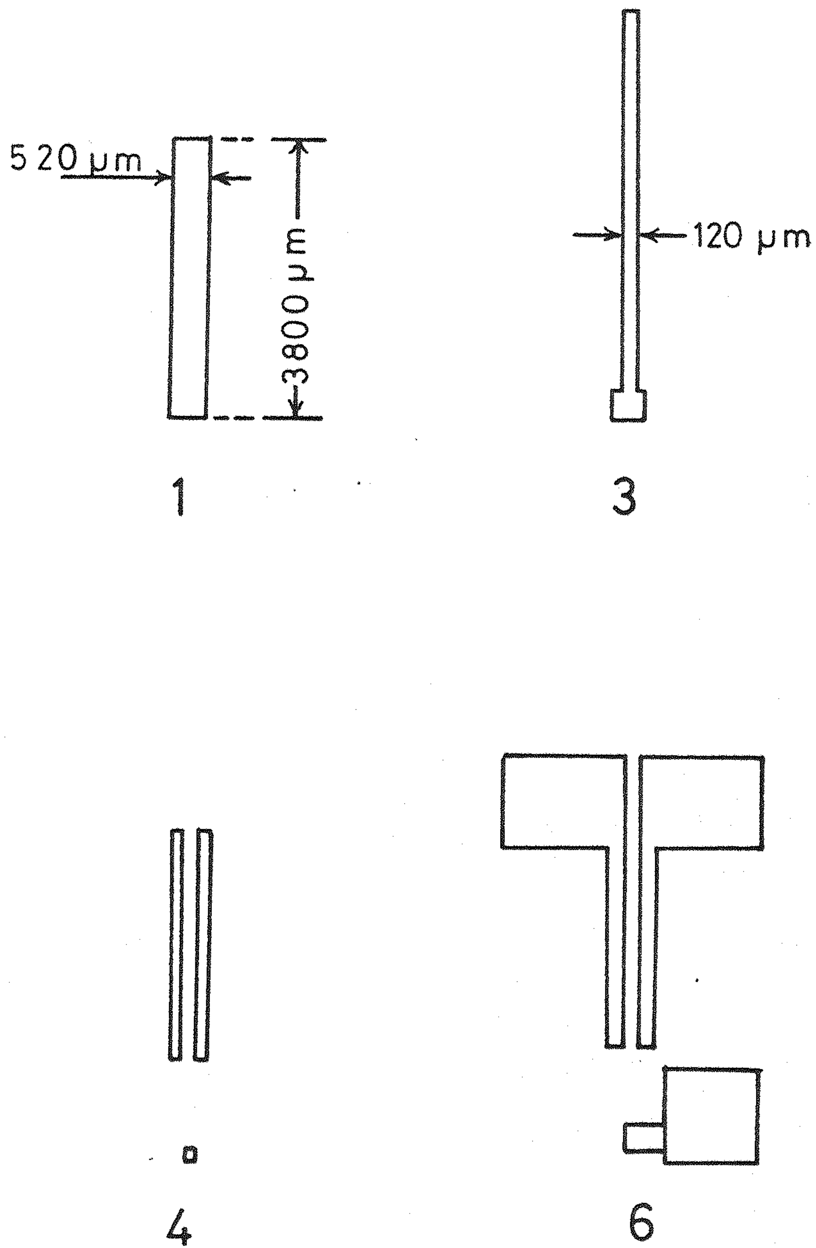


Fig. 6.2 The 4 masks used in the fabrication of the MOS transistor

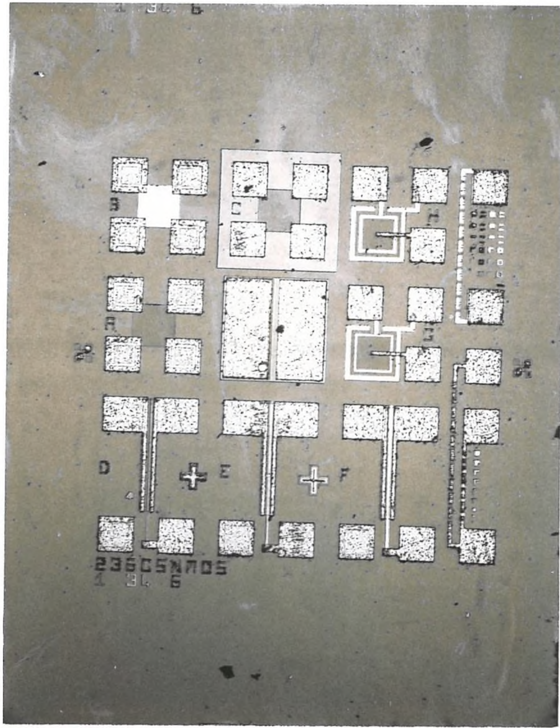


Fig. 6.3 Photomicrograph of the chip

provide a flat spectral response in the range .45 μm to .95 μm. The substrate photocurrent ($\approx I_{pr}$) was measured using the usual phase-sensitive detection techniques using the Brookdeal 9400 series apparatus. Figure 6.4 shows diagramatically, the arrangement for this experiment.

The output signal at each wavelength was then normalised to the incident power and the wavelength, to produce the relative spectral response. Figure 6.5 shows typical results of these experiments (open circles) together with the results of the calculation (equation 5.9 of Chapter 5). The thickness of the gate layers, as measured by a Tencor Alpha-step model 10, were as follows:

top oxide (d_1) : 1200 Å, polysilicon (d_2) : 1950 Å, and gate-oxide (d_3) : 1500 Å.

In attempting to fit the theory to the experiment, it was found that the calculated response was very sensitive to the thicknesses d_1, d_2 and d_3. The calculated curve shown in Figure 6.5(b) represents the best fit to the experimental data that could be obtained, and shows that the thickness of the polysilicon layer had to be slightly adjusted to get this match (d_2 = 1865 Å). This sensitivity of the response to the layer thickness means that any uncertainty in these values or any variation of these values over the surface would affect the agreement between the calculated and experimental results. Additionally, the polysilicon gate was modelled optically as a uniform film. However, polysilicon layers are known to have a microcrystalline structure, in which the diameters of the crystalline regions are of the same order of dimension as the layer thickness. This limits the validity of the assumption of a uniform layer of well-defined thickness; leading to a variation of the thickness of the polysilicon layer.

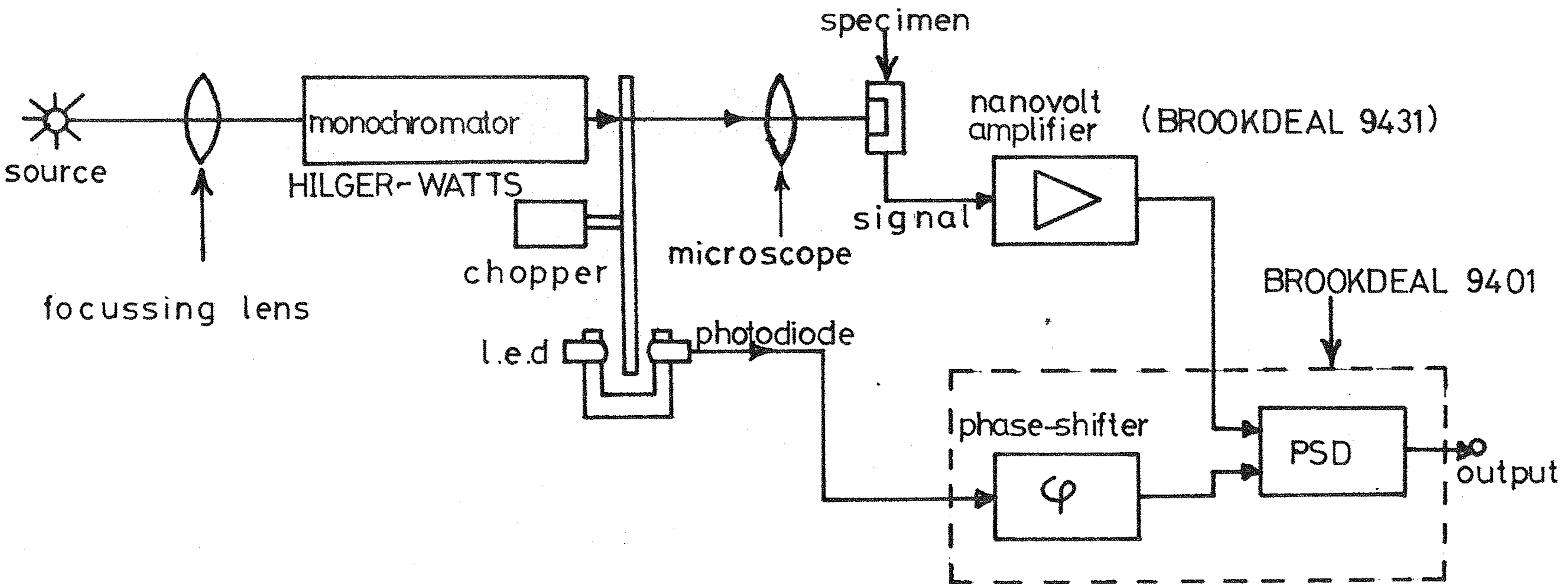


Fig. 6.4 Schematic of the set-up for measuring the spectral characteristics of the MOS transistor photocurrents.

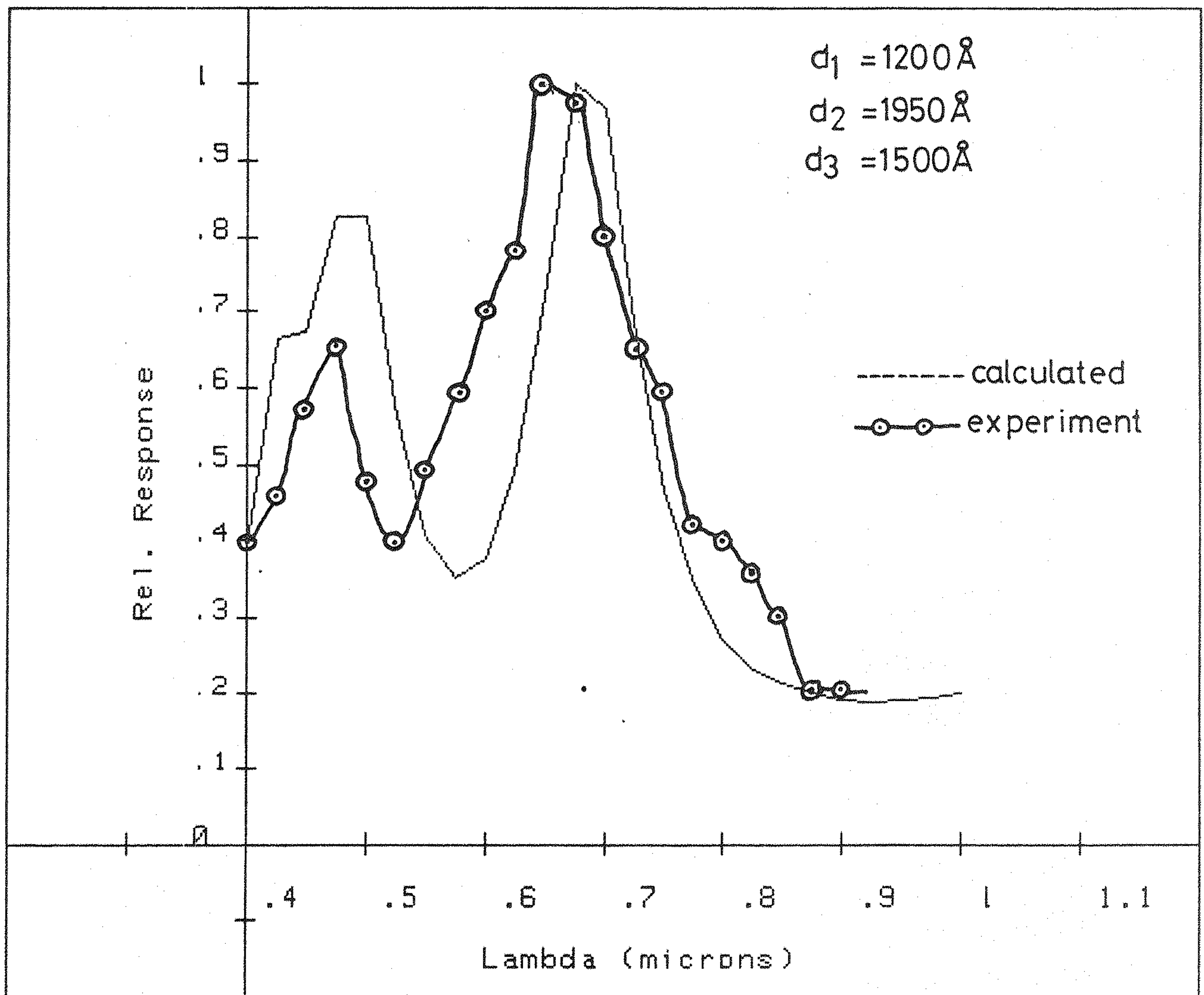


Fig. 6.5 (a) Spectral characteristics of the substrate photocurrent (-o—o-) measured, (--------) calculated; for d1= 0.12 um, d2= 0.195 um, and d3= 0.15 um.

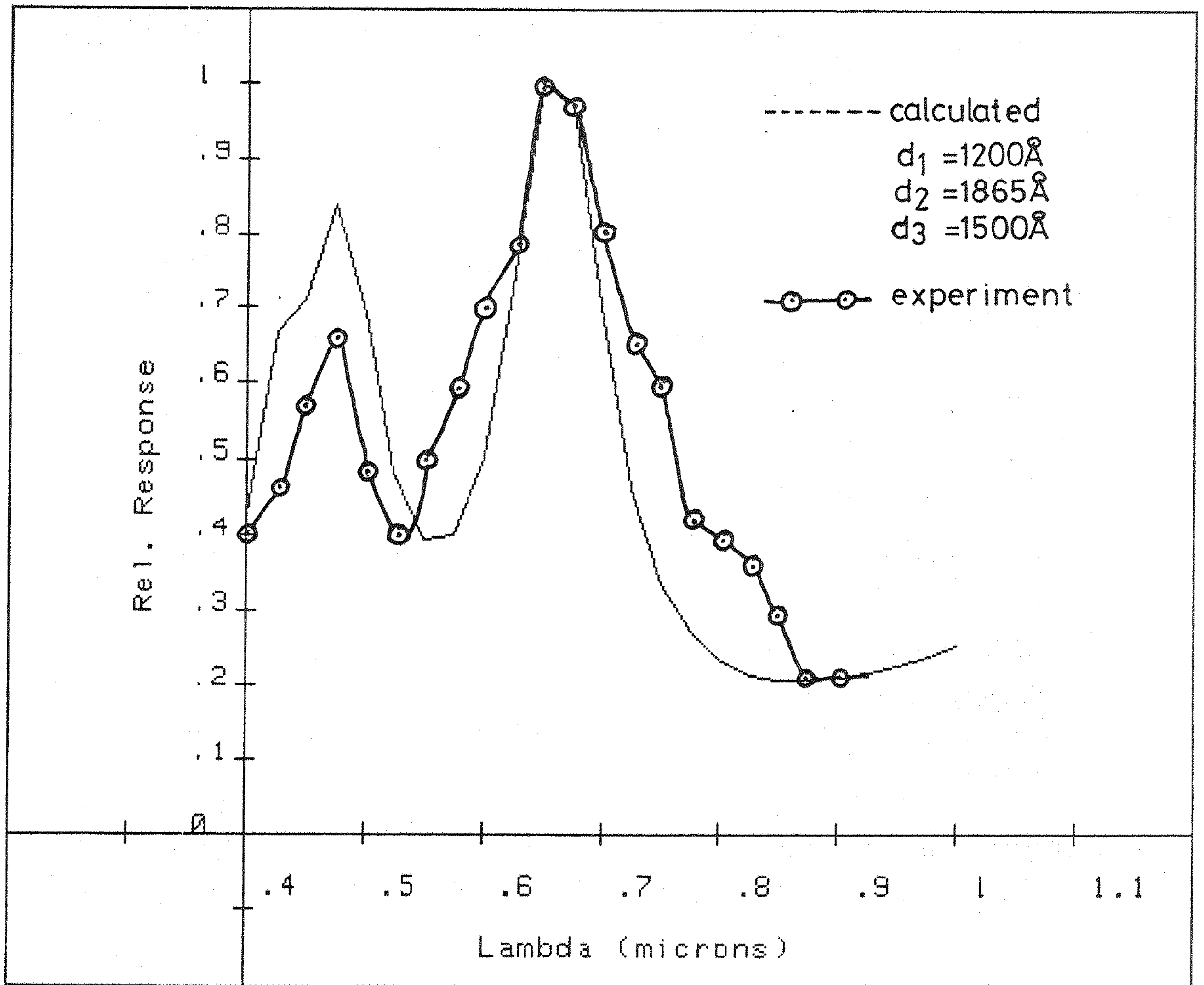


Fig. 6.5 (b) Spectral characteristic of the substrate photocurrent (—o——o—) measured, (------) calculated with d2 adjusted.

Although the agreement between the calculated and experimental results in Figure 6.5(b) is not excellent, the shapes of the major peaks (at 0.475 μm and 0.65 μm) more closely resemble the corresponding peaks in the measured response. The structure appearing in the measured response at 0.8 μm may be due to interface-state absorption as claimed by Okamoto[6.1] and Card and Fang[6.2].

The spectral shape of the drain-photocurrent spectral characteristic was found to be similar to that of the substrate photocurrent, with the major peaks appearing at the same wavelengths.

6.3 Photocurrent Amplification

To be able to use the theory developed in Chapter 5 to calculate the photocurrent amplification properties of the transistor, it is necessary to measure the current-voltage characteristics of the pn junction diode formed between the source-channel-drain p-region and the n-type substrate. These characteristics will furnish the parameters n and I_s of the diode (see equation 5.23 of Chapter 5). Figure 6.6 is a representation of the experimental set-up used to make these measurements. A large negative voltage (- 10.0 V) was applied to the gate (w.r.t. the substrate) to ensure the presence of an inversion layer at the surface. A variable positive voltage was then applied to the source + drain terminal to forward bias the diode. The current was monitored by a Digital Multimeter (Solartron model 7045), and the voltage across the diode was monitored by a Keithley Electrometer (Model 610C).

Two sets of experiments were performed. In the first, the sample was in darkness, while in the second experiment the sample was illuminated, the illumination produced a short-circuit current (I_{sc}) of 1.005 μA. These I-V characteristics of the diode are presented in Figure 6.7(a); the open-circles represent data obtained with the sample in the dark (i.e. I_{sc} = 0) and the triangles represent data for the illuminated case.

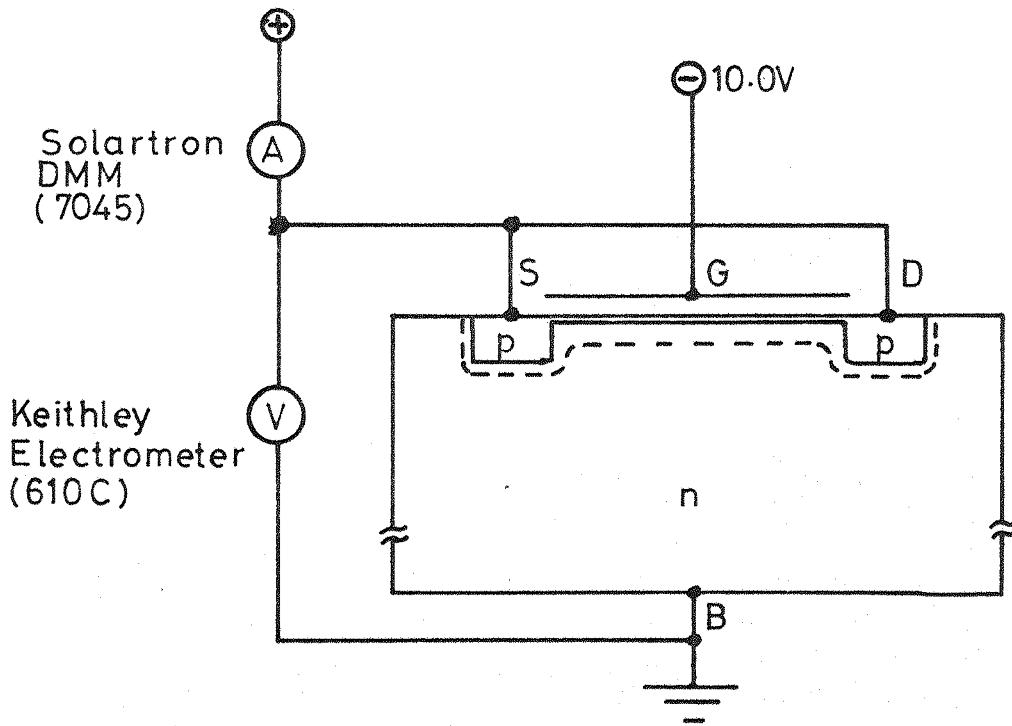
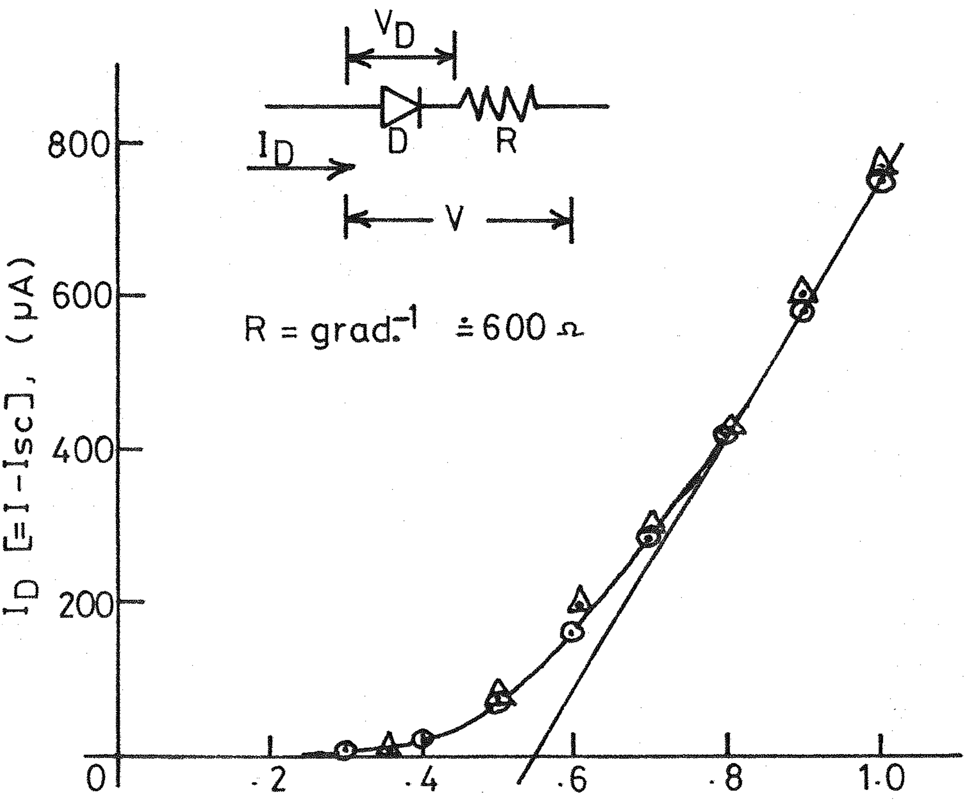


Fig. 6.6 Schematic of the technique used to measure the forward I-V characteristics of the MOS diode.



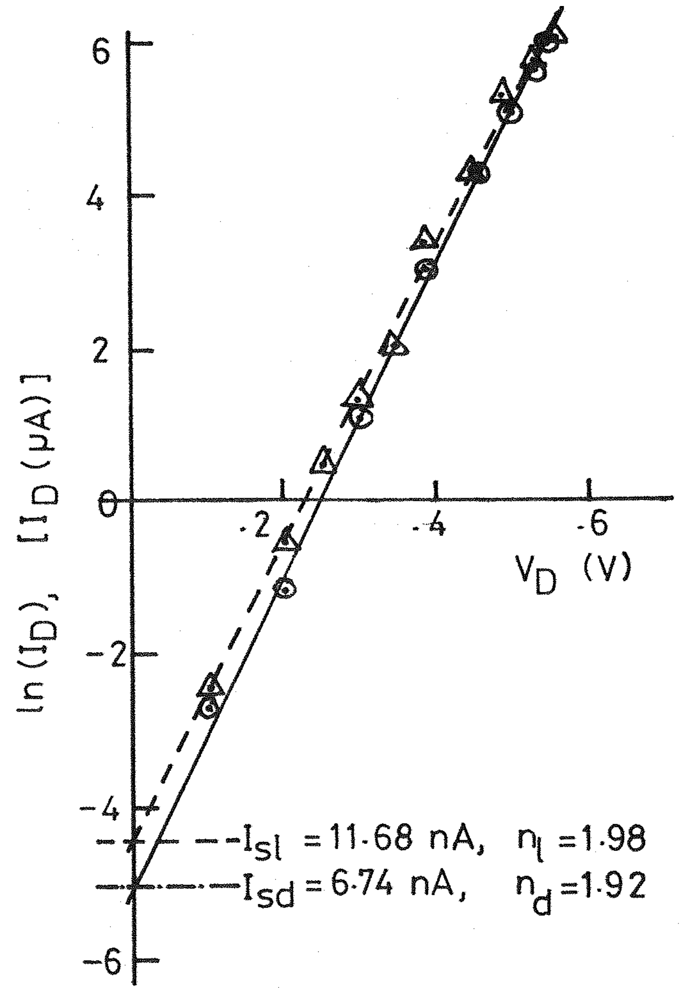


Fig. 6.7 (a) Typical forward I-V characteristics of the diode, inset: simplified equivalent circuit, (b) log/lin plot of the modified diode I-V characteristics; (⊙ ⊙ ⊙) in darkness, (Δ Δ Δ) with light.

This diagram also includes a simplified equivalent circuit (the diode + the substrate resistance R). The value of the resistance, as obtained from the gradient of the linear portion of the characteristics, was about 600 Ω (600 Ω in the dark, and 582 Ω illuminated).

From the equivalent circuit (inset to Figure 6.7(a)), the voltage across the diode (V_D) can be obtained for each measured diode current (I_D); since:

$$V_D = V - I_D R \tag{6.1}$$

Using the data presented in Figure 6.7(a) and this modification, a new set of I-V data for the diode alone have been obtained. These modified characteristics have been plotted on a log/lin scale in Figure 6.7(b). The gradient of this curve furnishes 'n' for the diode, and the (extrapolated) intercept on the y-axis furnishes the diode-reverse saturation current (I_s). Both diode parameters were found to increase with illumination. I_s increased from the 'dark' value (I_{sd}) of 6.74 nA to the illuminated value($I_{s\ell}$) of 11.68 nA; and n increased from (n_d)1.92 to (n_ℓ) 1.98 with illumination. This is in fair agreement with the results obtained by several authors working on Metal-Insulator-Semiconductor (MIS) solar cells; notably: Panayotatos, Card and Yang[6.3], Panayotatos and Card[6.4], Pulfrey[6.5], and Salter and Thomas[6.6]. These state that the illumination enhances depletion-region recombination, with a consequent increase in the values of n and I_s for the diode from those measured with the diode in darkness.

6.3.1 Dependence of the Photocurrent-gain on the substrate resistance

It will be recalled from the theory in Chapter 5, that the drain-photocurrent is a function of: (i) the primary photocurrent, and (ii) the voltage (V_{ph}) developed by this current in the substrate

resistance; i.e:

$$I_{dph} = \alpha I_{pr} + F(V_{ph}) \qquad (6.2)$$

and

$$G_{ph} (\equiv I_{dph}/I_{pr}) = \alpha + F(V_{ph})/I_{pr} \qquad (6.3)$$

where αI_{pr} is the fraction of I_{pr} flowing through the drain; and the magnitude of V_{ph} (for a fixed I_{pr}) depends on R_{sub}. For very low R_{sub}, V_{ph} will be very low, so that $F(V_{ph})$ will be much lower than αI_{pr}; hence a plot of I_{dph} versus I_{pr} will produce a straight line, the gradient of which will furnish α.

The variation of the drain photocurrent as a function of the substrate photocurrent has been measured with the substrate grounded. The substrate photocurrent was varied by altering the illumination intensity, and was measured at the substrate using a Solartron Digital Multimeter (Model 7045). It will be observed from the preceding section that when the substrate is grounded, R_{sub} is approximately 600 Ω; this is considered low enough for the above condition to be satisfied for the range of values of I_{pr} used in the present experiment. The results of this experiment are presented in Figure 6.8 (open-circles) together with the calculated results, calculated using R_{sub} = 600 Ω; and n = 1.98 and I_s = 11.68 nA for the diode parameters. The calculated curve represents the best fit to the experimental data, fitted by adjusting the value of α. The best fit was obtained with α = 0.528.

In the next experiment, a constant level of illumination was used (the substrate photocurrent was monitored to be 1 μA); a range of resistors (R_{ext}) (between 1 kΩ and 30 MΩ) were then inserted between the substrate and ground, and the resulting drain-photocurrent was then monitored for each R_{ext}. The results of this experiment are presented

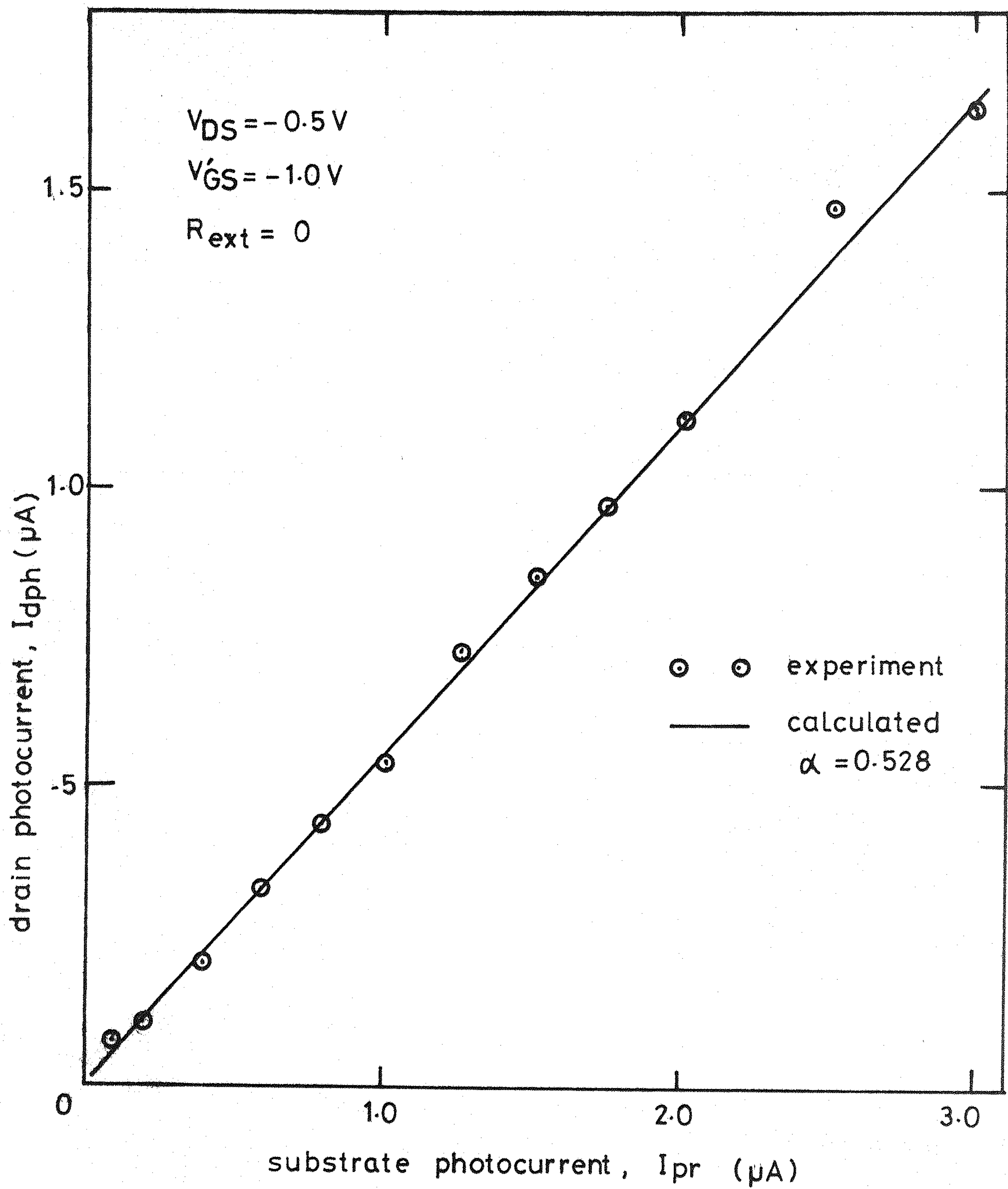


Fig. 6.8 Dependence of the drain-photocurrent on the substrate-photocurrent for $R_{ext} = 0$.

in Figure 6.9 (open circles), together with the results of the calculation which assumes $R_{sub-int} = 600\ \Omega$, $\alpha = 0.528$; and $n = 1.98$ and $I_s = 11.68$ nA for the diode. Since $I_{pr} = 1\ \mu A$, the same curves represent the photocurrent-gain.

This figure shows a fairly good agreement between the theory and experiment, within the experimental error.

6.3.2 Dependence of the Photocurrent-gain on the primary photocurrent

Figure 6.10 shows the dependence of the drain-photocurrent and the photocurrent-gain on the primary photocurrent for an external substrate resistance of 300 kΩ. The open-circles and triangles represent the measured data, I_{dph} and G_{ph}, respectively; while the continuous and dashed lines represent the calculated results. For the calculated data, the values of $R_{sub-int} = 600\ \Omega$, and $\alpha = 0.528$, and the diode parameters for $I_{pr} = I\ \mu A$ (i.e. $n = 1.98$ and $I_s = 11.68$ nA), have again been used here. The difference between the experiment and the theory needs further investigation. An attempt at explaining this difference is presented below. In this discussion, we will restrict our attention to I_{dph} versus I_{pr}; this can be extended to G_{ph} very easily since $G_{ph} = I_{dph}/I_{pr}$.

This figure shows that for $I_{pr} < 1.6\ \mu A$ the calculated results are lower than the measured while for $I_{pr} > 1.6\ \mu A$, the calculations are higher than measured. This is here attributed to the use of constant values for the diode parameters n and I_s, over the whole range of I_{pr}'s. It was noted earlier (beginning of section 6.3), that these parameters vary with illumination (see Figure 6.7(b)); being lower at low levels of illumination (e.g. in darkness). To see how these parameters affect I_{dph}, consider that R_{ext} is sufficiently high, so that V_{ph} for

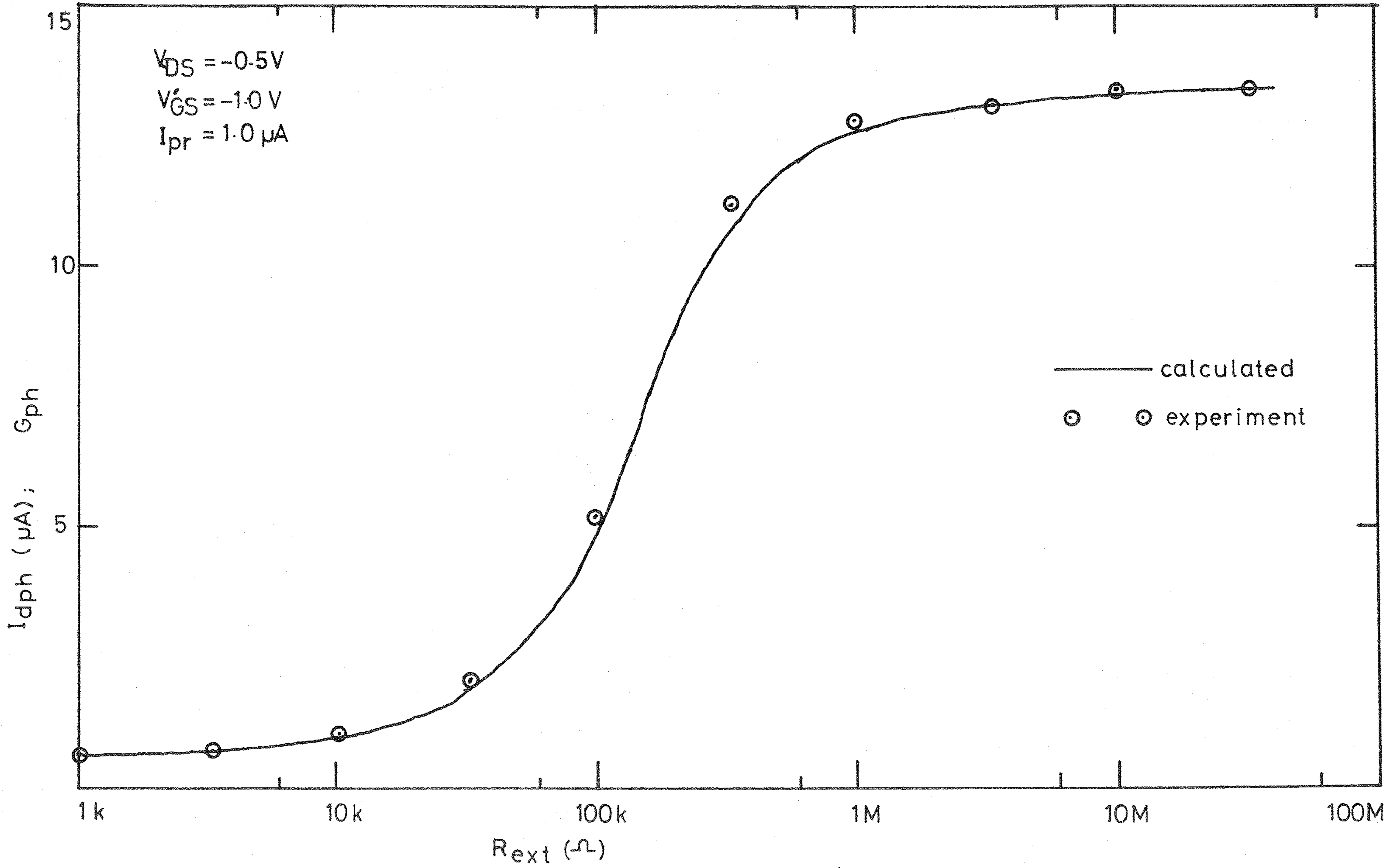


Fig. 6.9 Dependence of the drain-photocurrent and the Photocurrent-gain on the substrate resistance.

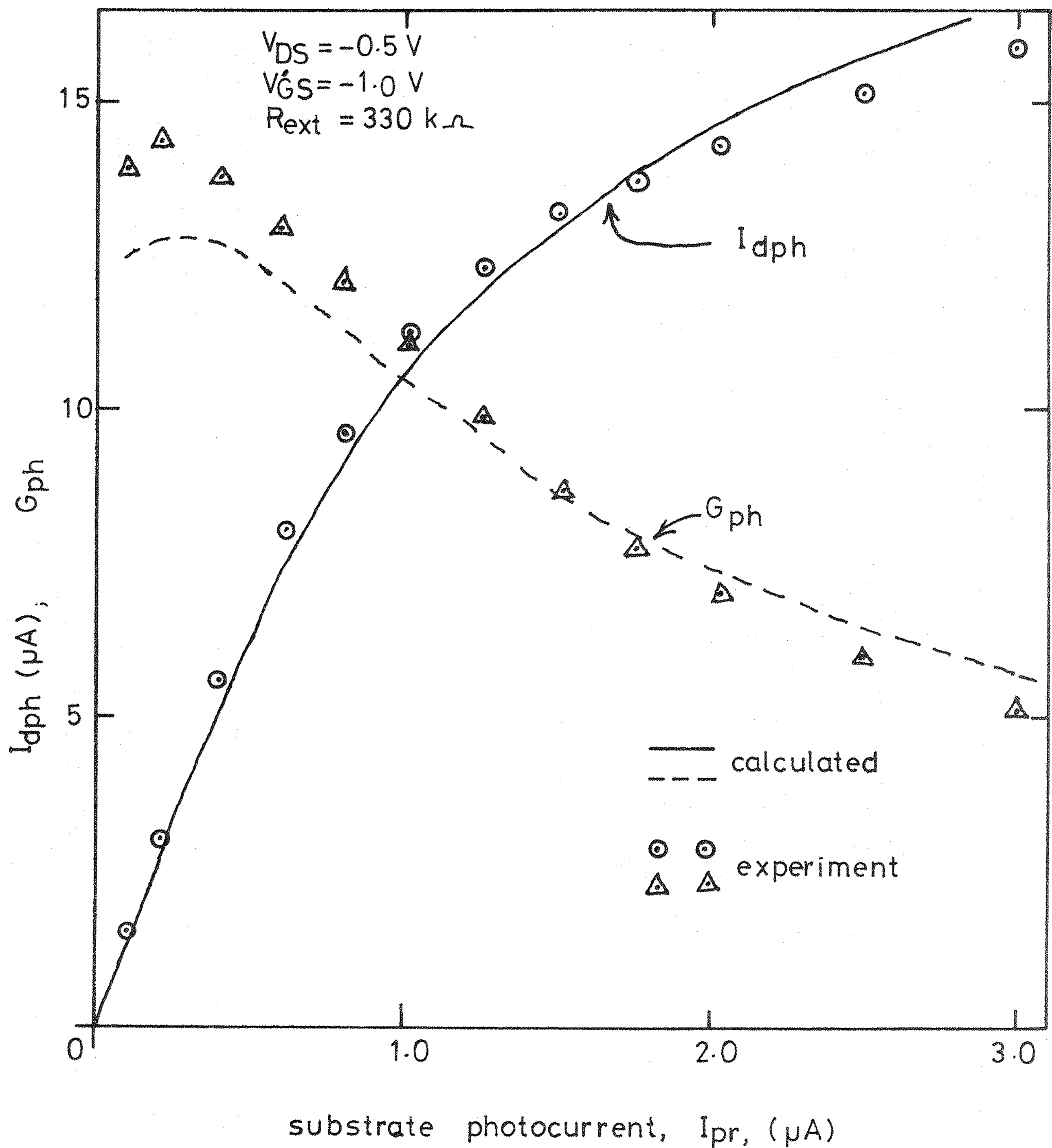


Fig. 6.10 Dependence of the drain-photocurrent and the photocurrent-gain on the primary-photocurrent for R_{ext} = 330 k-ohms.

any I_{pr} is given approximately by the diode open-circuit voltage, i.e:

$$V_{ph} \approx \frac{n}{\beta} \ell n \left(1 + \frac{I_{pr}}{I_s}\right) \qquad (6.4)$$

obtained from equation 5.23 of Chapter 5, by setting $I_D = I_{pr}$ (since $R_{ext} \to \infty$), and re-arranging the terms. We also note from equation 6.2 that:

$$I_{dph} = F(V_{ph}) + \alpha I_{pr}$$

and therefore for a fixed I_{pr} and α, the higher V_{ph} is, the higher will be I_{dph}. It will be observed from equation 6.4 that V_{ph} will increase (for a fixed I_{pr}) if I_s is lower or n is higher. As noted in Figure 6.7(b), while the change in n with illumination is only of the order of 3%, the change in I_s is quite appreciable (being about 70% in Figure 6.7(b)). This means that although n is lowered as I_{pr} falls, the fall in I_s will make V_{ph} higher than that calculated using n = 1.98 and I_s = 11.68 nA. As an example, consider that when I_{pr} = 0.2 μA, the actual diode parameters are the dark ones (n_d = 1.92, I_{sd} = 6.74 nA): using the diode parameters at I_{pr} = 1 μA gives V_{ph} = 0.148 V, while the 'dark' parameters give V_{ph} = 0.170 V. This will make the measured I_{dph} higher than that calculated for I_{pr} = 0.2 μA, and this will be the case for all I_{pr} < 1.0 μA. Conversely, at very high values of I_{pr}, I_s will be much greater than 11.68 nA, making V_{ph} lower than that calculated, thereby making the measured I_{dph} lower than that calculated.

The above discussion qualitatively explains the differences between the experiment and the theory, shown in Figure 6.10. It will also be observed in both Figures 6.9 and 6.10 that with R_{ext} = 330 kΩ and I_{pr} = 1.0 μA, the theory and experiment do not coincide; this error is attributed to the experimental error in extracting n and I_s from the diode I-V characteristics of Figure 6.7(b).

6.4 Switching Speed

Refer to Figure 6.11 which shows schematically, the set-up that was used to measure the switching speed of the MOS transistor while it operates as a photocurrent amplifier. The Laser probe described in section 3.3 of Chapter 3 was used as the source of the illumination falling on the gate of the transistor. The modulating signal was a square wave of 200 Hz pulse repetition frequency. The substrate resistance R_{sub} represents the series sum of the internal resistance and the externally connected resistor R_{ext}. The capacitor C represents all the stray capacitance associated with the substrate terminal; i.e. source-substrate capacitance (C_{SB}), Miller effect of the drain-substrate capacitance [$(1 + A_v)\ C_{DB}$], and the back-contact to ground capacitance (C_{BCG}).

The gate voltage was adjusted so that the transistor was slightly conducting ($I_D \sim 0.5\ \mu A$) in the quiescent state. The risetime of the output voltage(i.e. 10% to 90% of the final voltage) was monitored using an oscilloscope. The results obtained for various values of external substrate resistance are represented by open-circles in Figure 6.12. On the same graph are presented the calculated results (dashed-line curve). The theoretical results were obtained by applying the theory of section 5.5 of Chapter 5, and using the diode parameters n = 1.98 and I_S = 11.68 nA; the results obtained for C = 1.0 pF were then multiplied by a constant factor to match the peak in the measured response (i.e. 450 μs at 250 kΩ R_{ext}).

The shapes of these two curves are very similar, showing a fairly good agreement between the experiment and the model. The discrepancies at the extreme ends of these curves need further investigation; these are here attributed to the non-linear value of the capacitance C associated with the substrate.

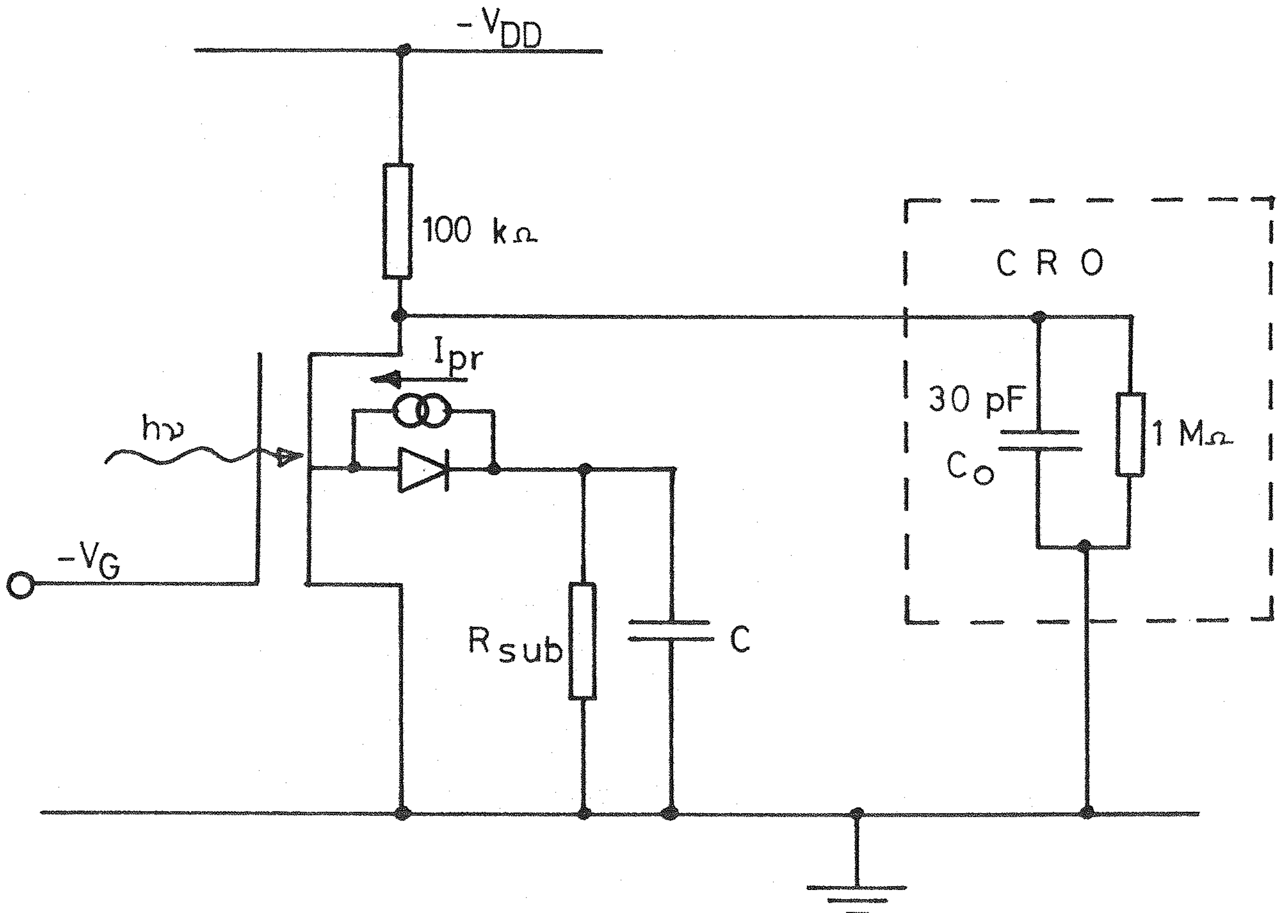


Fig. 6.11 Schematic of the experimental set-up for the measurement of the switching speed of the photocurrent amplifier.

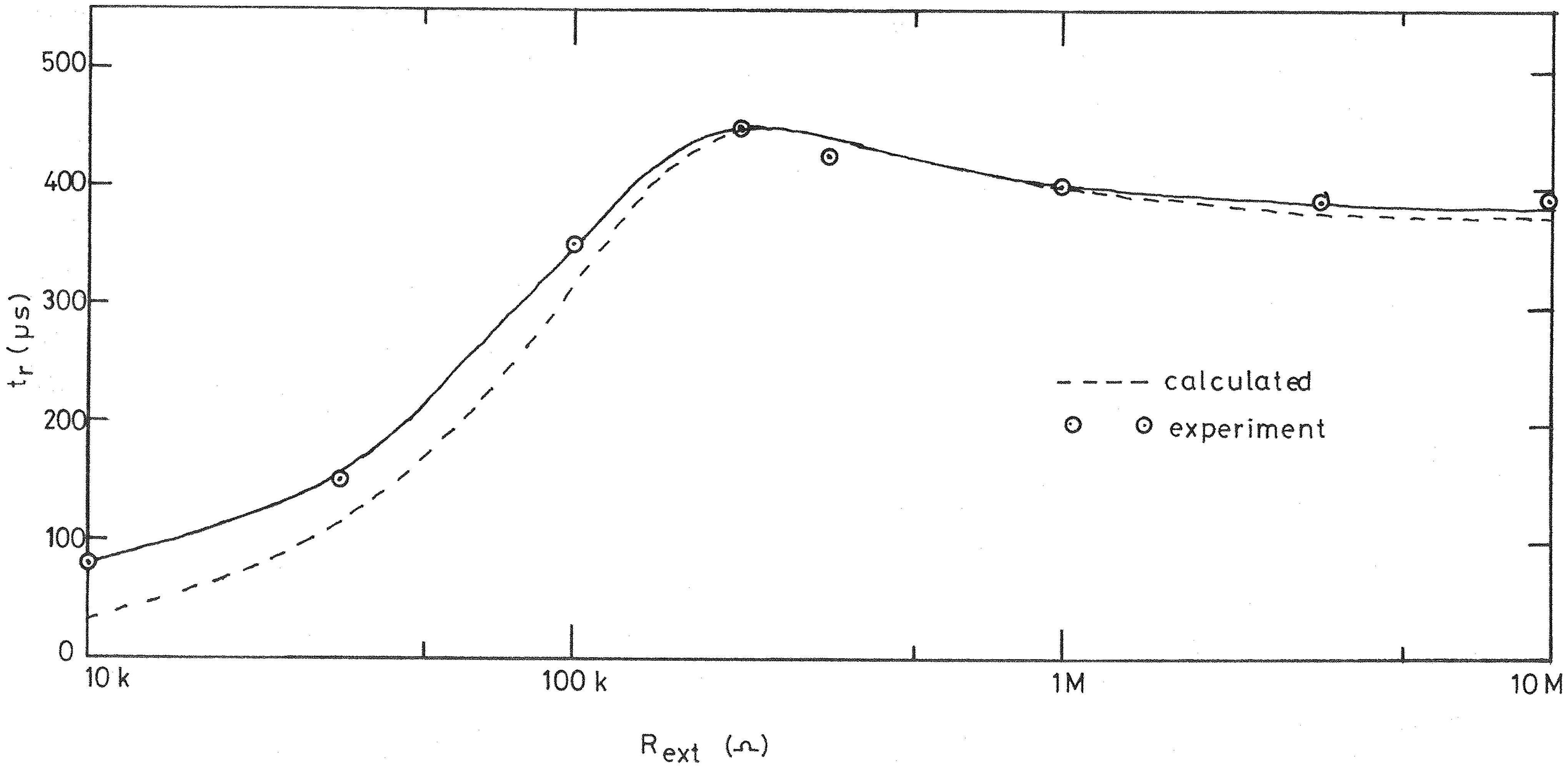


Fig. 6.12 Risetime of the output voltage as a function of the external substrate resistance.

In obtaining the theoretical results, we have used a constant value of C (matched to the value of C when R_{ext} = 250 k). C is actually very non-linear; in particular the largest component of C (that due to the Miller-effect on C_{DB}) changes quite appreciably with the voltage gain (A_V) between the substrate (the input) and the drain (the output). It will be recalled (from equation 6.2, say) that the drain photocurrent is given by

$$I_{dph} = \alpha I_{pr} + F(V_{ph})$$

where V_{ph} is the substrate voltage developed by the primary photocurrent in R_{sub}. From Figure 6.11 we note that the output voltage (V_{out}) is given by $I_{dph} \times R_L$ (where R_L = the load resistor, and is 100 kΩ). The voltage gain between the substrate and the drain is given by:

$$A_V = V_{out}/V_{ph} = 100\ k\Omega \times I_{dph} / V_{ph} \qquad (6.5)$$

since the theory gives both I_{dph} and V_{ph} for each R_{sub}, the voltage gain for R_L = 100 kΩ can be calculated very easily. Figure 6.13 shows the calculated voltage gain as a function of R_{ext}, using the measured parameters of the device (α = 0.528, n = 1.98 and I_S = 11.68 nA). This curve shows that the voltage gain is a non-linear function of the substrate resistance; and in particular that for R_{sub} < 30 kΩ, A_V is higher than its asymptotic value of 5.8.

Since the Miller-effect contribution of C_{DB} to the substrate capacitance is $(1+A_V)\ C_{DB}$, and since the value of A_V used (implicitly) in the calculation of the theoretical curve of Figure 6.12 was assumed constant (A_V used was for R_{ext} = 250 kΩ); this will introduce an error in the calculated results. As an example, consider the situation for R_{ext} = 10 kΩ. In this case A_V is about 1.8 times higher than A_V at 250 kΩ; making $(1+A_V)\ C_{DB}$ about 1.5 times higher at 10 kΩ than it is at 250 kΩ. This will result in higher measured times at 10 kΩ than those calculated using A_V at 250 kΩ, if we assume that this Miller-

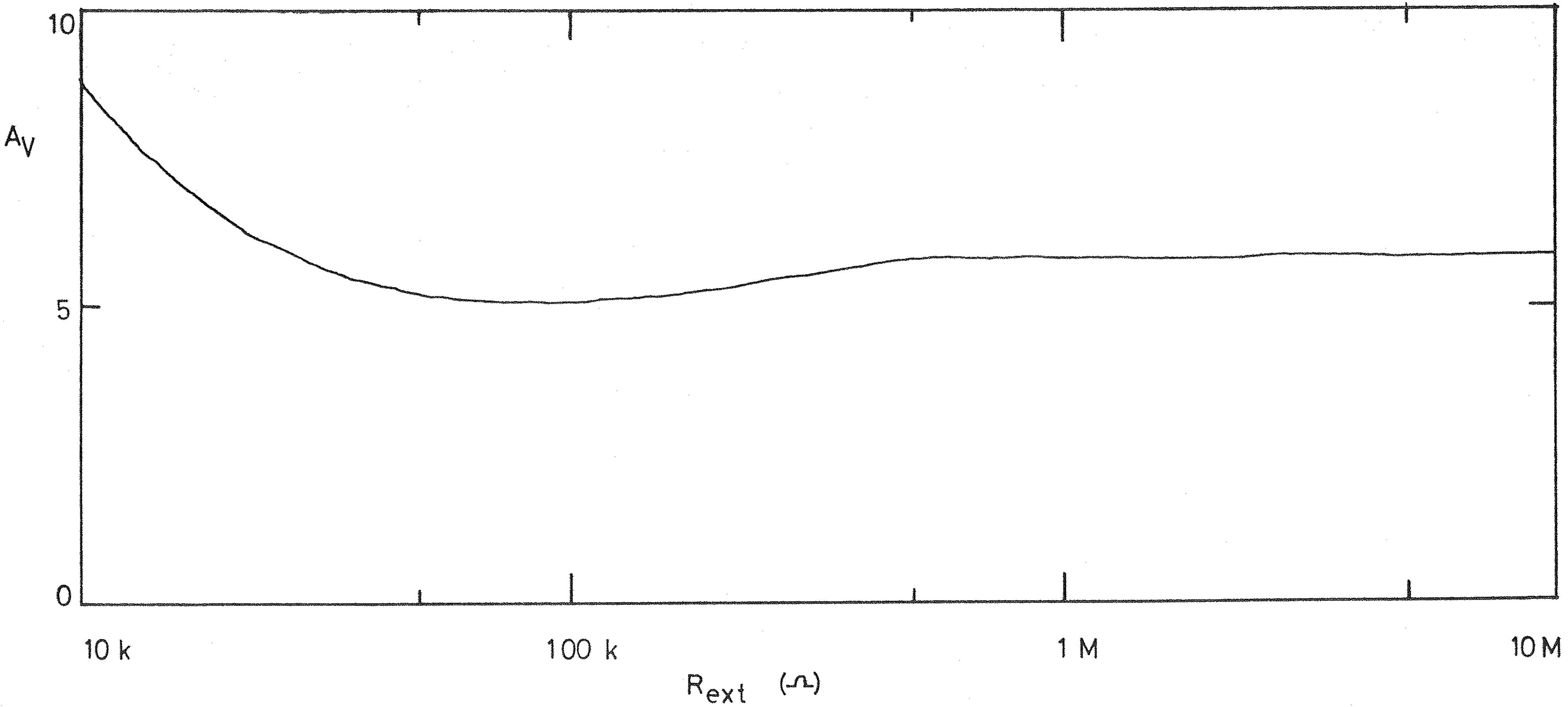


Fig. 6.13 The voltage gain between the substrate and the drain as a function of the external substrate resistance.

capacitance dominates the C at the substrate. By the same token, the higher A_V for $R_{ext} > 1$ MΩ (compared with $R_{ext} = 250$ kΩ) will make the measured t_r higher than calculated for these resistors. This effect is expected to qualitatively explain the discrepancies between the theory and experiment in Figure 6.12.

6.5 Discussion of the results

The photocurrent-gain and switching speed characteristics of the MOS transistor have been shown to be very dependent on the values of the substrate resistance and the substrate capacitance. The capacitance is dependent quite appreciably on the surface area of the sample. Reducing this area 100 fold, say, (e.g. by a 10X photographic reduction in the size of the masks) would reduce C by about 100 times, which would lead to a reduction of about 100 times in the switching times.

If we assume that the shift register circuit discussed in Chapter 4 was implemented in CMOS, then the limitation imposed on the laser testing technique by the CMOS technology (in attempting to measure the delay times due to each unit of the SR circuit), could be overcome by implementing this photocurrent amplifying structure in the manner described in section 5.6 of Chapter 5. The poor switching speed characteristic of this device would not be a severe limitation in this particular experiment as long as its risetime was not much longer than the SR speed. This can be achieved by a reduction in the surface area of the device to reduce C, as stated above. A reduction of about 300 times in the area of the present device, would make the dimensions of the structure comparable to those of the SR circuit. Such a reduction in the area of the device would make the longest risetime of the transistor about 1.5 μs (450 μs/300), which is comparable with the delay times of the SR circuit; and should therefore not severely limit the measurement of the Delay times of the SR.

6.6 Conclusions

It has been shown in this chapter that, as predicted by the model of Chapter 5, an MOS phototransistor when operated with a large valued substrate resistance ($\sim$ 100 kΩ), can provide photocurrent amplification (albeit at the expense of the switching speed of the transistor). The transistor amplifies the primary photocurrent that flows between the channel region and the substrate, the amplified photocurrent flows between its source and drain terminals.

This property of the MOS phototransistor could be employed to overcome the limitation of the Laser Testing Technique in testing CMOS types of digital integrated circuits by integrating the device into an appropriate position in the circuit.

Although the switching speed of this configuration of the transistor is poor, it could still be used successfully to determine the delay times of a shift register circuit, where this circuit was implemented in CMOS technology.

The advantages of this arrangement over amplifying the photocurrent of a pn junction with a subsequent MOS transistor are the saving in the chip area by using one device instead of two (a separate pn junction to generate the photocurrent, followed by a separate MOS transistor to amplify the photocurrent).

CHAPTER SEVEN

CONCLUDING REMARKS

We have established that the new method of integrated circuit testing, which employs the laser probe, can be used to measure propagation delay times in an MOS digital circuit in a very simple manner. This should ease and improve the resolution of diagnostic testing, and should therefore reduce the time taken for the development of new designs of IC's.

The laser produces a current within the i.c., the magnitude of which determines the testability of the circuit when using the laser testing technique. The target for the laser probe in the integrated circuit interior has so far been a pn-junction. The magnitude of the photocurrent generated at the junction is a function of the wavelength of the illumination and the junction depth (the peak response for a 2.0 μm junction depth, for example, being at a wavelength of approximately 0.75 μm). This tends to limit the choice of suitable monochromatic light sources for use in the testing of the i.c.'s using an optical beam probe.

The laser power requirements for testing different kinds of MOS integrated circuit technologies depend on the relative magnitude of the generated photocurrent to that of the currents which normally flow in the circuits. Thus different types of IC technologies require different laser powers to inject information; in particular CMOS i.c.'s require extremely large photocurrents ($\sim$ 1-3 mA) to input data optically. This would require very high laser beam powers ($\sim$ 30 mW) when the pn junction is employed for the generation of the photocurrent. By directing the laser beam onto the gate region of the transistor, the photocurrent

generation characteristics are modified from those of the pn junction; the new characteristics could be used advantageously in the laser testing of MOS digital IC's.

In this thesis we have introduced a novel application of the MOS transistor, which could overcome some of the problems encountered in attempting to test MOS digital i.c.'s using the laser probe. It has been shown that by operating the MOS transistor as a photodetector when the substrate terminal is connected to ground via a large resistance ($\sim$ 100 kΩ), the transistor will provide photocurrent amplification. This configuration could be employed in an appropriate position in CMOS integrated circuits to overcome the requirement of high laser beam powers to inject data optically; by providing amplification of the photocurrent generated by moderate laser probe beam powers. Also, by making a suitable choice of materials for the gate electrode (to reduce absorption and/or reflection in the gate), the short wavelength response of the MOS transistor photodetector can be greatly improved beyond that of a pn junction; thus widening the range of monochromatic light sources suitable for use as optical probes to test MOS i.c.'s.

A model has been developed to predict the MOS transistor response to illumination under different bias conditions. Calculations based on this model have been compared with experimental data obtained from measurements on p-MOS transistors; the results show good agreement between the simple model and the experiment. It has also been shown that the photocurrent amplification in the transistor is obtained at the expense of the switching speed; and therefore a suitable compromise must always be sought for a particular application of this structure.

Suggestions for Future Work

1. Refinement of the model for photocurrent amplification:

It was noted in section 6.3.2 of Chapter 6 that the diode parameters n and I_s vary with illumination falling on the diode. Therefore an improvement can be obtained in the theoretical model by determining these diode parameters for each level of illumination; the simple technique used to obtain these (described in section 6.3) can be used for each value of the primary photocurrent.

In section 6.4, we observed that the voltage gain between the substrate and the drain (A_v) (which is a non-linear function of the substrate resistance) plays a very important role in determining the switching speed of the circuit. An improvement in the theoretical model can also be obtained by explicitly including this variation in A_v with R_{sub} in the model. This will require a knowledge of the ratio of the drain-substrate capacitance (C_{DB}) to the rest of the components of the substrate capacitance (i.e. C_{SB} and C_{BCG}); which can be estimated from the device geometry.

2. Depletion mode transistor structure:

The device studied in Chapter 6 of this thesis was a pMOS enhancement mode transistor, necessitating a gate electrode bias for proper operation. The gate electrode could be dispensed with by fabricating a depletion mode device. The absence of the gate electrode would improve the spectral response of the photocurrent, by removing the absorption associated with it; with a consequent improvement in the photosensitivity of the device.

APPENDIX 1 : MOS THEORY

This appendix presents the theory required for the understanding of the behaviour of MOS devices under the application of external electric fields. The analysis is based on the works of Kingston and Neustadter[A1.1], Garrett and Brattain[A1.2], and Sze[A1.3]. This relates the total space charge in the semiconductor Q_s, to the potential difference ϕ_s, between the semiconductor surface and the bulk of the semiconductor. ϕ_s is also known as the surface potential and is the amount of band bending on the energy band diagram representing the semiconductor surface, Figure A1.1.

The relationship between Q_s and ϕ_s can be extended to the MOS transistor, to obtain expressions relating the transistor currents to the applied voltages.

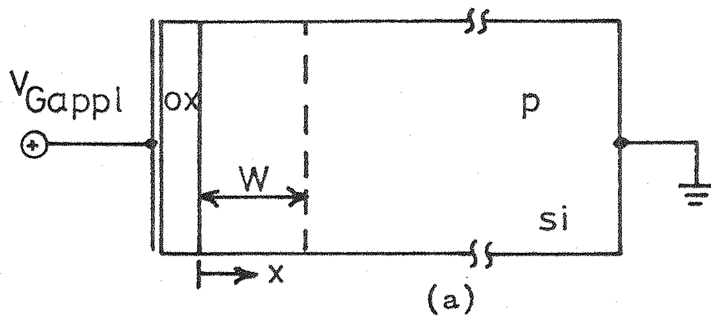
A1.1 Theory of the Space Charge and the Electric Field at the Semiconductor Surface

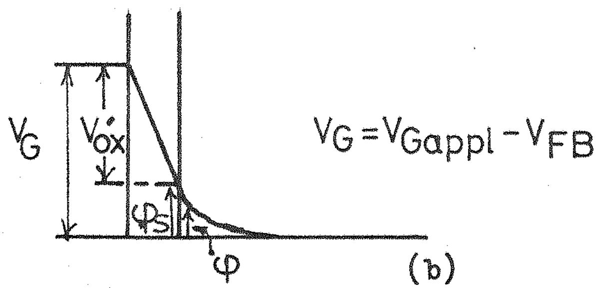
Taking the surface plane as x=o and positive values of x as towards the bulk of the semiconductor, the space charge density ρ at a point x is related to the electric potential ϕ at that point by Poisson's equation:

$$\frac{\partial^2 \phi}{\partial x^2} = -\frac{\rho}{\varepsilon_s} \qquad (A1.1)$$

where ε_s is the permittivity of the silicon semiconductor (1×10^{-12} F/cm). The space charge density ρ is given by:

$$\rho = q(N_D^+ - N_A^- + p-n) \qquad (A1.2)$$





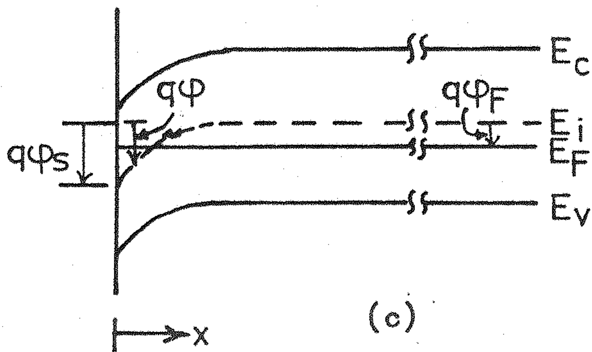


Fig. A1.1 (a) An MOS device with a positive voltage applied to the gate terminal; (b) potential distribution; (c) energy band diagram (from Sze, ref. A1.3).

where N_D^+ and N_A^- are the ionised donor and acceptor impurity concentrations and p and n are the mobile hole and electron densities; q is the electronic charge (1.6×10^{-19} coulomb). Here we have assumed complete ionisation of the impurity atoms. This treatment also assumes thermal equilibrium; that the semiconductor is non-degenerate; that the generation and recombination within the space charge layer, and the time rates of change of local carrier concentrations are negligible. The treatment will be restricted to an MOS device having a p-type substrate, but the discussion is equally applicable to a device with an n-type substrate provided appropriate changes in the signs of the parameters and applied voltages are made.

In a p-type substrate, the donor concentration N_D is assumed negligible so that the space charge density can be approximated to:

$$\rho = q(p_p - N_A^- - n_p) \quad \text{(A1.3)}$$

where:

$$N_A^- = p_{po} = n_i \exp(\beta\phi_F) = n_i \exp(U_F) \quad \text{(A1.4a)}$$

$$p_p = p_{po} \exp(-\beta\phi) = n_i \exp(U_F - U) \quad \text{(A1.4b)}$$

$$n_p = n_{po} \exp(\beta\phi) = n_i \exp(U - U_F) \quad \text{(A1.4c)}$$

and $\beta = q/kT$; k is the Boltzmann's constant (1.38×10^{-23} joule/^{o}K), T the absolute temperature and $U = \beta\phi$. p_p and n_p are the hole and electron concentrations in the p-type substrate, respectively; the subscript (o) designates the equilibrium concentrations. n_i is the

intrinsic carrier concentration. The space charge density can now be re-written as:

$$\rho = qn_i e^{U_F} \left| e^{-u} - 1 - e^{u-2U_F} \right| \tag{A1.6}$$

and Poisson's equation becomes

$$\frac{\partial^2 U}{\partial x^2} = - \frac{\beta q n_i e^{U_F}}{\varepsilon_s} \left| e^{-u} - 1 - e^{u-2U_F} \right| \tag{A1.7}$$

Integrating (A1.7) leads to[A1.2]:

$$\frac{\partial U}{\partial x} = \frac{\sqrt{\ } e^{U_F}}{L_i} \left| e^{-u} + U - 1 + e^{-2U_F} (e^{u}-1) \right|^{\frac{1}{2}} \tag{A1.8}$$

where $L_i = (kT\varepsilon_s/2q^2 n_i)^{\frac{1}{2}}$, is the intrinsic Debye length.

The electric field inside the semiconductor is given by:

$$E = - \frac{\partial \phi}{\partial x} = - \frac{1}{\beta} \frac{\partial u}{\partial x} \tag{A1.9}$$

The electric field at the semiconductor surface E_s is given by setting $\phi = \phi_s$.

The charge per unit area required to produce this field is given by Gauss' law:

$$Q_s = - \varepsilon_s E_s = \frac{\varepsilon_s}{\beta} \frac{\partial u}{\partial x} \tag{A1.10}$$

i.e.

$$Q_s = - \frac{\varepsilon_s}{\beta L_i} \sqrt{e^{U_F}} \left| e^{-U_s} + U_s - 1 + e^{-2U_F} (e^{U_s} - 1) \right|^{\frac{1}{2}} \tag{A1.11}$$

Equation (A1.11) relates the charge in the semiconductor to the normalised surface potential U_s and is plotted in Figure A1.2.

Figure A1.1(b) shows the relationship between the applied external voltage and ϕ_s in an MOS device.

$$V_{Gapplied} = V_{ox} + \phi_s + \phi_{ms} \tag{A1.12}$$

where ϕ_{ms} is the work function difference between the gate metal and the semiconductor. By considering the charge neutrality of the MOS device we must have:

$$Q_G + Q_{ss} + Q_s = 0 \tag{A1.13}$$

where Q_G is the charge on the gate, Q_s the semiconductor space charge and Q_{ss} the effective charge at the oxide-silicon interface.

The fixed oxide charge is known to be residing very close to the interface (within about 200Å of the interface)[A1.4]. Here we have lumped it into the Q_{ss} term and assumed that the whole of it is actually at the interface. Any charge Q_{ox} that is at a distance x_o from the interface can be taken into account by an equivalent Q'_{ox}, at the interface, where Q'_{ox} is given by[A1.5]:

$$Q'_{ox} = Q_{ox} \left(\frac{t_{ox} - x_o}{t_{ox}} \right) \tag{A1.14}$$

where t_{ox} is the oxide thickness. Thus we now have an essentially charge-free oxide so that the voltage across it can be obtained by treating the oxide as a capacitor of capacitance per unit area, C_{ox} $(= \varepsilon_{ox}/t_{ox})$;

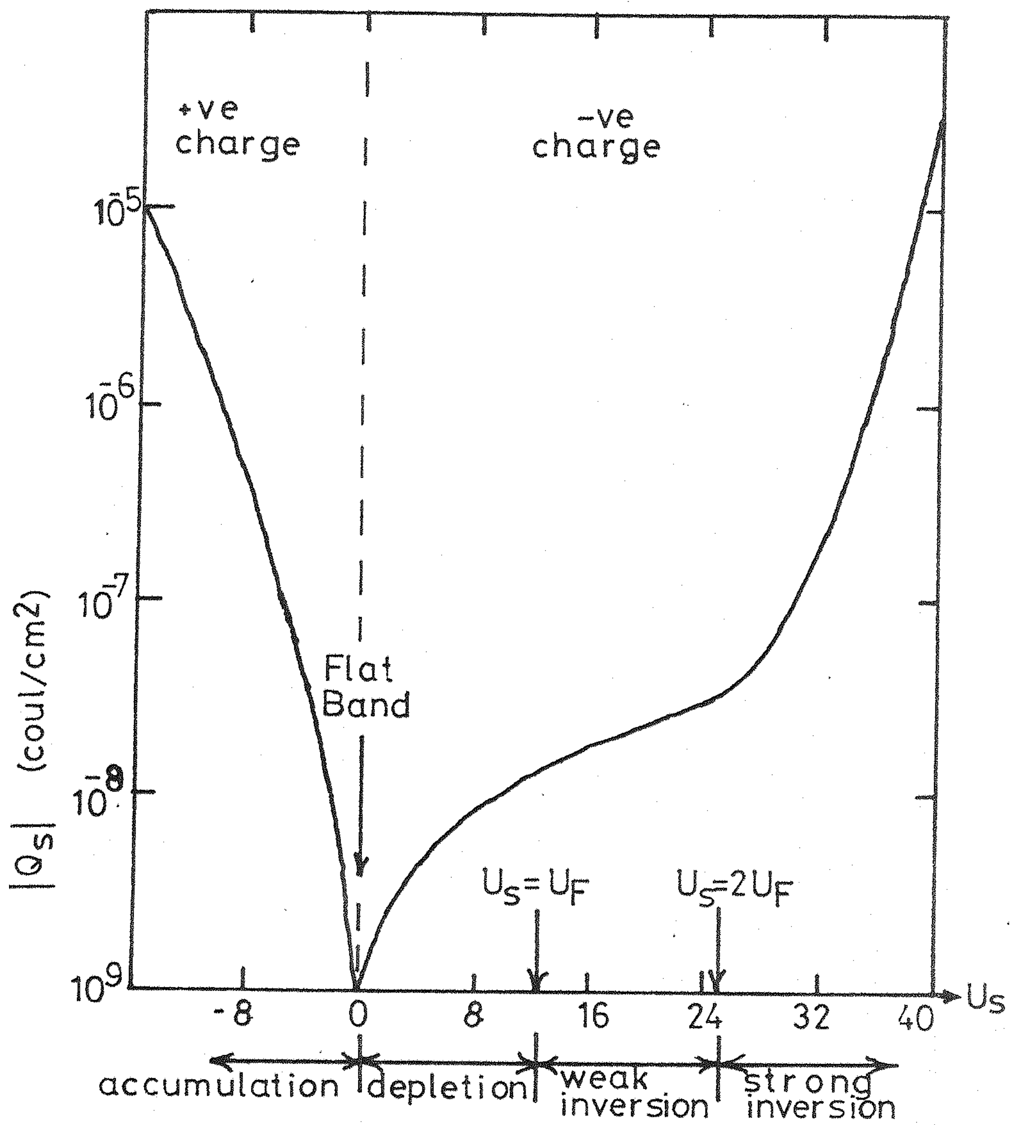


Fig. A1.2 Variation of the semiconductor space charge with the surface potential (U_s); p-type silicon at 300°K, $N_A = 4.0x10^{15}$ cm^{-3}, (from Sze, ref. A1.3).

ε_{ox} being the permittivity of the oxide $(\frac{1}{3}\varepsilon_s)$.

$$V_{ox} = \frac{Q_G}{C_{ox}} = -\frac{Q_{ss}}{C_{ox}} - \frac{Q_s}{C_{ox}} \qquad \text{(A1.15)}$$

so that now:

$$V_{Gapplied} = -\frac{Q_{ss}}{C_{ox}} - \frac{Q_s}{C_{ox}} + \phi_s + \phi_{ms} \qquad \text{(A1.16a)}$$

$$(V_{Gapplied} - V_{FB}) \equiv V_G = \phi_s + V'_{ox} \qquad \text{(A1.16b)}$$

where:

$$V_{FB} = \phi_{ms} - \frac{Q_{ss}}{C_{ox}} \qquad \text{(A1.17a)}$$

$$V'_{ox} = -\frac{Q_s}{C_{ox}} \qquad \text{(A1.17b)}$$

Equation A1.16 essentially says that the Flat Band Voltage (V_{FB}) has the effect of reducing the effectiveness of the applied gate voltage to V_G, where $V_G = \phi_s - Q_s/C_{ox}$. Using equations (A1.16b) and (A1.11) we have:

$$(V_G - \phi_s) = -\frac{Q_s}{C_{ox}} \qquad \text{(A1.18a)}$$

or that

$$(U_G - U_s) = \frac{\varepsilon_s \sqrt{} e^{U_F}}{C_{ox} L_i} \left| e^{-U_s} + U_s - 1 + e^{-2U_F} (e^{U_s} - 1) \right|^{\frac{1}{2}} \qquad \text{(A1.18b)}$$

Equation (A1.18) relates the gate voltage to the semiconductor space charge Q_s.

A1.2 Theory of the MOS Transistor

The principle of the MOS Field Effect Transistor was first demonstrated by Lilienfield[A1.7a] and Heil[A1.7b]. It was subsequently studied by Shockley and Pearson[A1.8]. Kahng and Attala[A1.9] proposed and fabricated the first MOSFET using a thermally oxidised structure. The basic device characteristics have subsequently been studied by several authors.

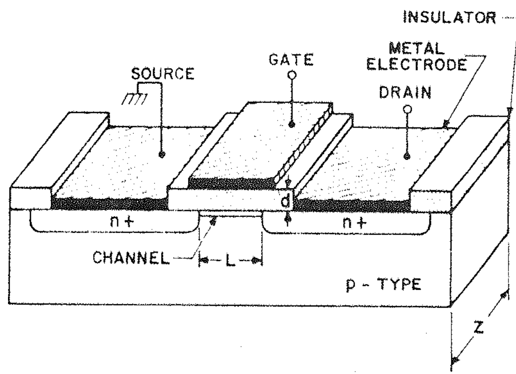
The theory presented here, which is based on a gradual-channel approximation, and includes drift and diffusion channel current components is based on the double integral model of Pao and Sah[A1.10]. This theory has subsequently been reviewed by Baccarani et al[A1.11] and Van de Wiele[A1.12] to present it in an analytical form suitable for computer aided design applications; their approaches will be closely adhered to here.

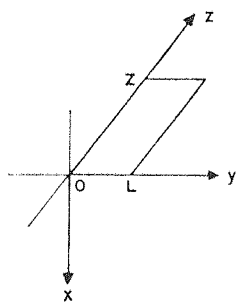
Figure A1.3 shows the structure of an n-channel MOSFET, and Figure A1.4 shows both the semiconductor charge distribution, and the band bending for the equilibrium, and non-equilibrium (the transistor with V_D applied) cases. These diagrams use the depletion approximation of Grove and Fitzgerald[A1.6].

To obtain the space charge characteristics under the non-equilibrium conditions we use the assumptions of quasi-equilibrium[A1.6]. Using these assumptions we can write that the space charge density is given by:

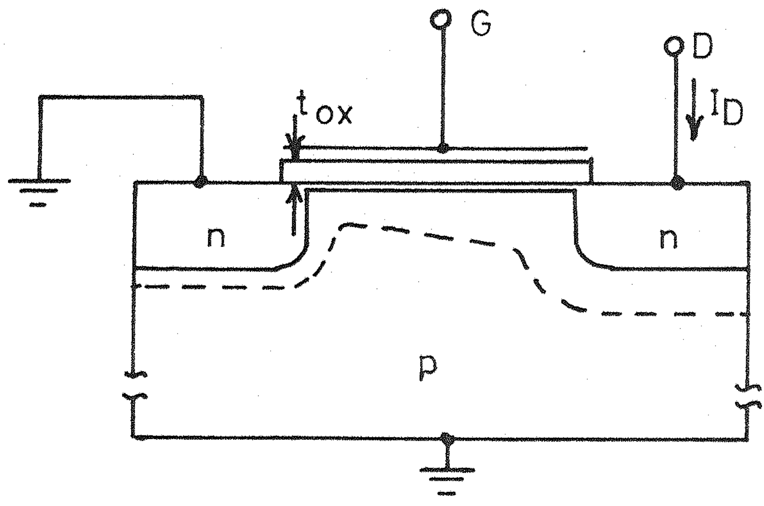
$$\rho = qni \left| e^{U_p} (e^{-U} - 1) - e^{-U_n} (e^{U} - 1) \right| \qquad (A1.19)$$

where U_p ($= \beta\phi_p$) and U_n ($= \beta\phi_n$) are the quasi-Fermi[A1.6] potentials for holes and electrons respectively. These potentials are measured relative to the intrinsic Fermi potential in the bulk of the substrate. Two assumptions are made to simplify the calculations:





(a) Schematic diagram of an insulated-gate field-effect transistor. The important parameters are the channel length (L), the channel width (Z), and the insulator thickness (d). (After Kahng and Atalla, Ref. A1.9).



(b) Cross-sectional view of the transistor

Fig. A1.3

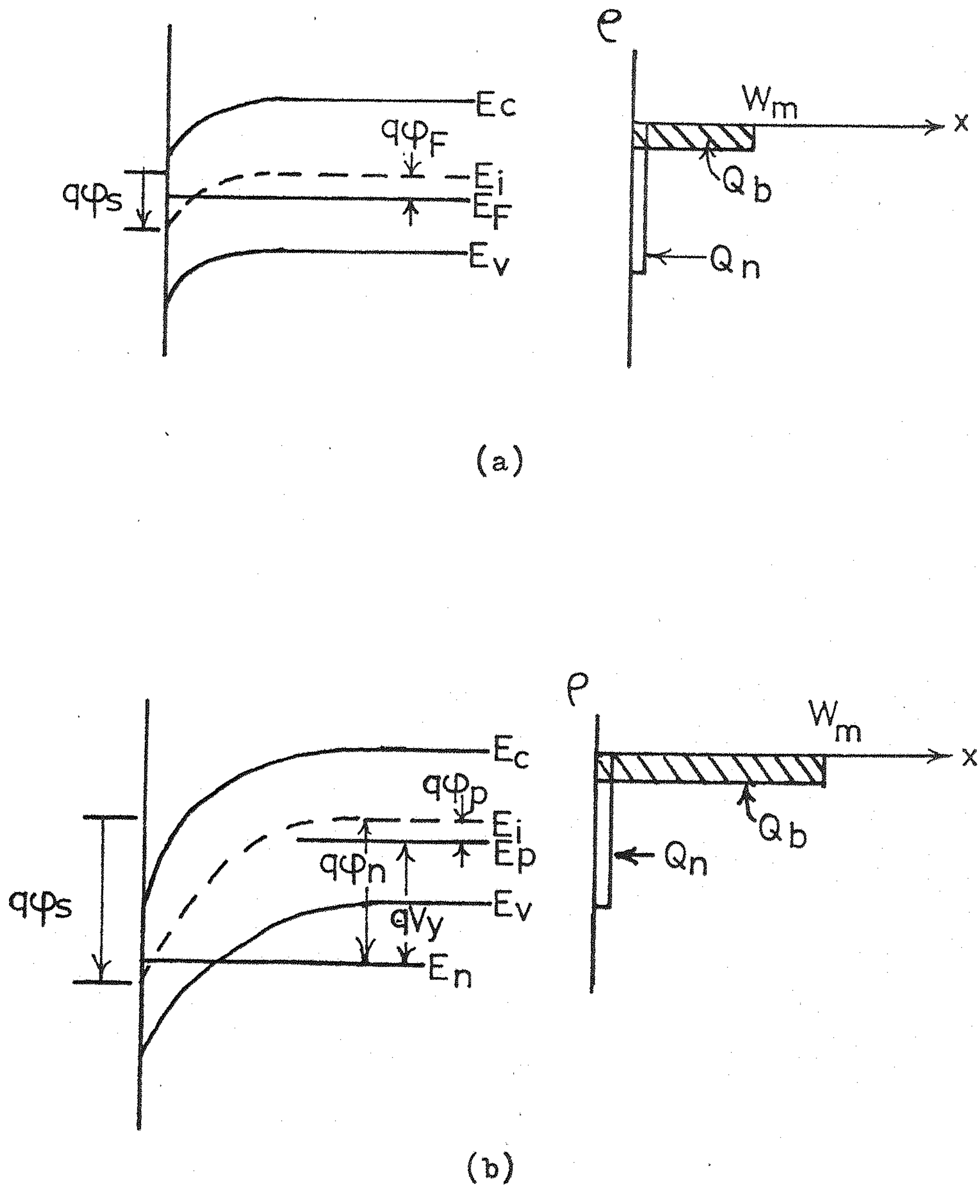


Fig. A1.4 Comparison of the charge distribution and energy band variation of an inverted region for: (a) the equilibrium case, and (b) the non-equilibrium case (After Grove and Fitzgerald, ref. A1.6).

(i) The quasi-Fermi level for the majority carriers (holes, in this case) does not vary with distance from the bulk to the surface. When the surface is either depleted or inverted, this assumption introduces little error since the majority carriers are then only a negligible part of the surface space charge.

(ii) The quasi-Fermi level for the minority carriers (electrons) at a point y in the channel, is separated from the quasi-Fermi level for majority carriers by the applied potential along the channel, V_y[A1.12], i.e.:

$$U_n = U_p + \xi = U_F + \xi \tag{A1.20}$$

where $\xi = \beta V_y$; and use has been made of assumption (i). Poisson's equation in quasi-equilibrium can therefore be written as:

$$\frac{\partial^2 U}{\partial x^2} = -\frac{\beta q n_i e^{U_F}}{\varepsilon_s} \left| e^{-U} - 1 - e^{U-(U_F+U_n)} \right| \tag{A1.21}$$

Integration of equation (A1.21) leads to:

$$\frac{\partial U}{\partial x} = \frac{\surd\, e^{U_F}}{L_i} \left| e^{-U} + U - 1 + e^{-(U_F+U_n)} \left(e^{U}-1\right) \right|^{\frac{1}{2}} \tag{A1.22}$$

and therefore

$$Q_s = -\frac{\varepsilon_s \surd\, e^{U_F}}{L_i} \left| e^{-U_s} + U_s - 1 + e^{-(2U_F+\xi)} \left(e^{U_s}-1\right) \right|^{\frac{1}{2}} \tag{A1.23}$$

and therefore the relationship between the applied voltages and the semiconductor space charge becomes:

$$(U_G - U_s) = -\frac{\varepsilon_s \surd\, e^{U_F}}{C_{ox} L_i} \left| e^{-U_s} + U_s - 1 + e^{-(2U_F+\xi)} \, (e^{U_s} - 1) \right|^{\frac{1}{2}} \qquad \text{(A1.24)}$$

For large positive values of the surface potential equation (A1.24) can be approximated by:

$$(U_G - U_s) = -\frac{\varepsilon_s \surd\, e^{U_F}}{C_{ox} L_i} \left| (U_s - 1) + e^{U_s - 2U_F - \xi} \right|^{\frac{1}{2}} \qquad \text{(A1.25)}$$

valid for all regions of interest in a conducting transistor, i.e. regions of weak and strong inversion. This leads to an expression of the surface potential in terms of V_G and V_y:

$$U_s = 2U_F + \xi + \ln \{\delta^2 (U_G - U_s)^2 - (U_s - 1)\} \qquad \text{(A1.26)}$$

where $\delta = C_{ox} L_i / (\varepsilon_s \exp(U_F/2))$. Only a few iterations are necessary to obtain an accurate value of U_s from equation (A1.26). Clearly the usual expression

$$U_s = 2U_F + \xi, \text{ equivalent to}$$

$$\phi_s = 2\phi_F + V_y \qquad \text{(A1.27)}$$

is only a first order approximation of equation (A1.26). Equation (A1.26) (and (A1.27)) is plotted in Figure A1.5 for various values of U_G and ξ; and shows the saturation behaviour of U_s for large ξ, corresponding to the subthreshold condition[A1.11].

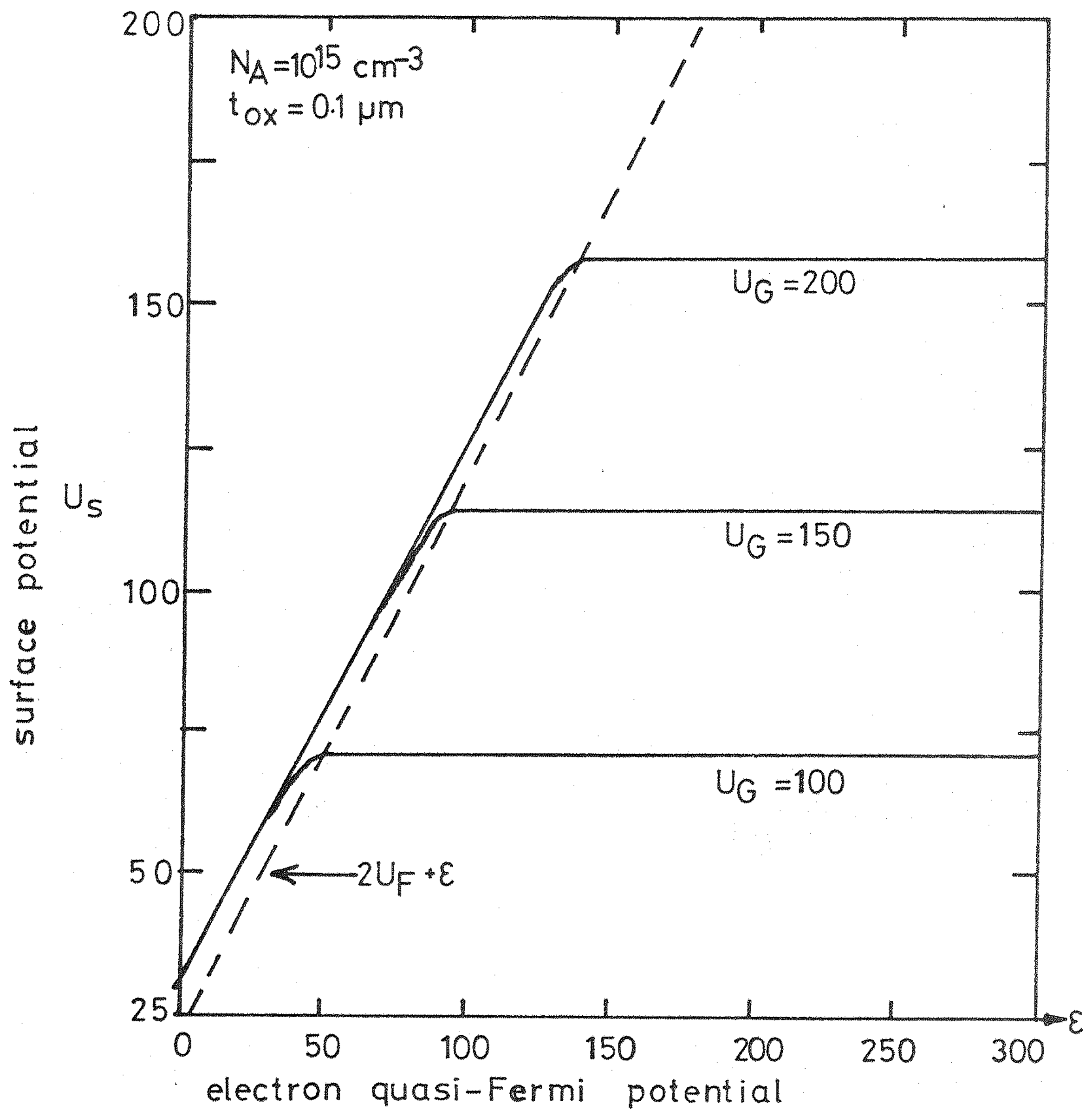


Fig. A1.5 Surface potential (Us) against quasi-Fermi potential (ε) for various gate voltages (U_G); (————) equation A1.26, (— — —) equation A1.27 (after Baccarani et al, ref. A1.11).

The Drain Current, I_D

The electron current density in the y-direction is given by[A1.12]:

$$J_{n(y)} = -q\mu_n \left| -n(\partial\phi/\partial y) + \frac{1}{\beta}(\partial n/\partial y) \right| \quad \text{(A1.28a)}$$

i.e. the sum of the drift and the diffusion current components; μ_n is the electron mobility in the channel. This expression leads to:

$$J_{n(y)} = + q\mu_n\, n(dV/dy) \quad \text{(A1.28b)}$$

Integrating over the entire cross-sectional area of the channel, we obtain the drain current as:

$$I_D = -Z\, \mu_n\, Q_n\, (dV/dy) \quad \text{(A1.29)}$$

where $Q_n = \int qn\, dx$ is the total inversion charge per unit area at a point y along the channel, Z is the channel width. Another integration along the length of the channel L, yields:

$$I_D \int_o^L \frac{dy}{\mu_n} = -Z \int_{V(o)}^{V(L)} Q_n\, dV \quad \text{(A1.30a)}$$

$$I_D = -\frac{Z}{L}\,\mu_n{}^* \int_{V(o)}^{V(L)} Qn\, dV \quad \text{(A1.30b)}$$

where for simplicity we introduce an effective mobility $\mu_n{}^*$ (constant throughout the length of the channel), this being the effective or mean mobility along the channel.

In our normalised terms, equation (A1.30b) can be re-written as follows:

$$I_D \left(\frac{\beta L}{Z\mu_n^*}\right) \equiv I_D' = -\int_{U_{n(o)}}^{U_{n(L)}} Q_{n(y)}\, dU_n = -\int_{\xi_{(o)}+U_F}^{\xi_{(L)}+U_F} Q_{n(y)}\, d\xi \tag{A1.31}$$

To evaluate this integral, it is necessary to change the integration variable. We have that:

$$I_D' = -\int_{U_{s(o)}}^{U_{s(L)}} Q_n(U_G,U_s)\,\frac{d\xi}{dU_s}\cdot dU_s \tag{A1.32}$$

and using equation (A1.26) we can find $d\xi/dU_s$ to be:

$$\frac{d\varepsilon}{dU_s} = 1 + \frac{2\delta^2(U_G-U_s)+1}{\delta^2(U_G-U_s)^2-(U_s-1)} \tag{A1.33}$$

To complete the integration, all that remains now is to obtain $Q_{n(y)}$ in terms of U_G and U_s. Q_n can be expressed as:

$$Q_n = Q_s - Q_b \tag{A1.34}$$

where Q_s is the total semiconductor space charge and Q_b is the bulk fixed charge component of the space charge. Q_b can be approximated by the following expression:

$$Q_b = -\frac{\varepsilon_s\sqrt{\ } e^{U_F}}{L_i}\left|U_s-1\right|^{\frac{1}{2}} \tag{A1.35}$$

derived from Poisson's equation by neglecting the minority carriers[A1.11].
Using equation (A1.18) we can relate Q_n to U_G and U_s:

$$(U_G - U_s) = -\frac{\beta}{C_{ox}} Q_s = -\frac{\beta}{C_{ox}} (Q_b + Q_n) \tag{A1.36}$$

so that

$$-Q_n = \frac{C_{ox}}{\beta} (U_G - U_s) + Q_b$$

$$-Q_n = \frac{C_{ox}}{\beta} (U_G - U_s) - \frac{\varepsilon_s \surd\, e^{U_F}}{\beta L_i} (U_s - 1)^{\frac{1}{2}} \tag{A1.37}$$

This equation can now be used in conjunction with equations (A1.32) and (A1.33) to derive an expression for the drain current:

$$I_D' = \int_{U_{s(o)}}^{U_{s(L)}} \left| \frac{C_{ox}}{\beta} (U_G - U_s) - \frac{\varepsilon_s \surd\, e^{U_F}}{\beta L_i} (U_s - 1)^{\frac{1}{2}} \right| \times$$

$$\left| 1 + \frac{2\delta^2 (U_G - U_s) + 1}{\delta^2 (U_G - U_s)^2 - (U_s - 1)} \right| dU_s \tag{A1.38}$$

On integrating this expression, we get that the drain current is given by:

$$I_D' = \frac{C_{ox}}{\beta} \{ (U_G + 2) U_s - \tfrac{1}{2} U_s^2 - \frac{2}{3\delta} (U_s - 1)^{\frac{3}{2}} + \frac{4}{\delta} (U_s - 1)^{\frac{1}{2}}$$

$$- \frac{1}{\delta} (2k - \frac{1}{\delta}) \ln \left| k + (U_s - 1)^{\frac{1}{2}} - \frac{1}{2\delta} \right|$$

$$+ \frac{1}{\delta} (2k + \frac{1}{\delta}) \ln \left| k - (U_s - 1)^{\frac{1}{2}} + \frac{1}{2\delta} \right| \} \Bigg|_{U_{s(o)}}^{U_{s(L)}} \tag{A1.39}$$

where $k = \sqrt{U_G - 1 + 1/4\delta^2}$. The surface potential is evaluated at the source (o) and drain (L) edges of the channel using equation (A1.26). Equation (A1.39) is plotted in Figure A1.6 for various values of U_G.

The Threshold Voltage, V_T

The threshold voltage is defined as the gate potential required to achieve strong inversion at the semiconductor surface, i.e. the gate potential that will make $\phi_s = 2\phi_F$ for $V_s = o$, or $\phi_s = 2\phi_F + V_s$ for $V_s \neq o$.

From equation (A1.26), the above requirement means that the following equality must hold at the source terminal:

$$U_s = 2U_F + \xi_{(s)} + \ell n \{\delta^2 (U_G - U_s)^2 - (U_s - 1)\} = 2U_F + \xi_{(s)} \quad \text{(A1.40)}$$

or, that the argument of the log term be unity. This means that when $U_G = U_T^*$:

$$\delta^2 (U_T^* - U_s)^2 - (U_s - 1) = 1 \quad \text{(A1.41a)}$$

and

$$U_s = 2U_F + \xi_{(s)} \quad \text{(A1.41b)}$$

Equation A.141a solves to give that:

$$U_T^* = U_s + \frac{1}{\delta} \sqrt{U_s} \quad \text{(A1.42a)}$$

or that

$$V_T^* = \phi_s + \frac{1}{C_{ox}} \sqrt{2\varepsilon_s q N_A (\phi_s)} \quad \text{(A1.42b)}$$

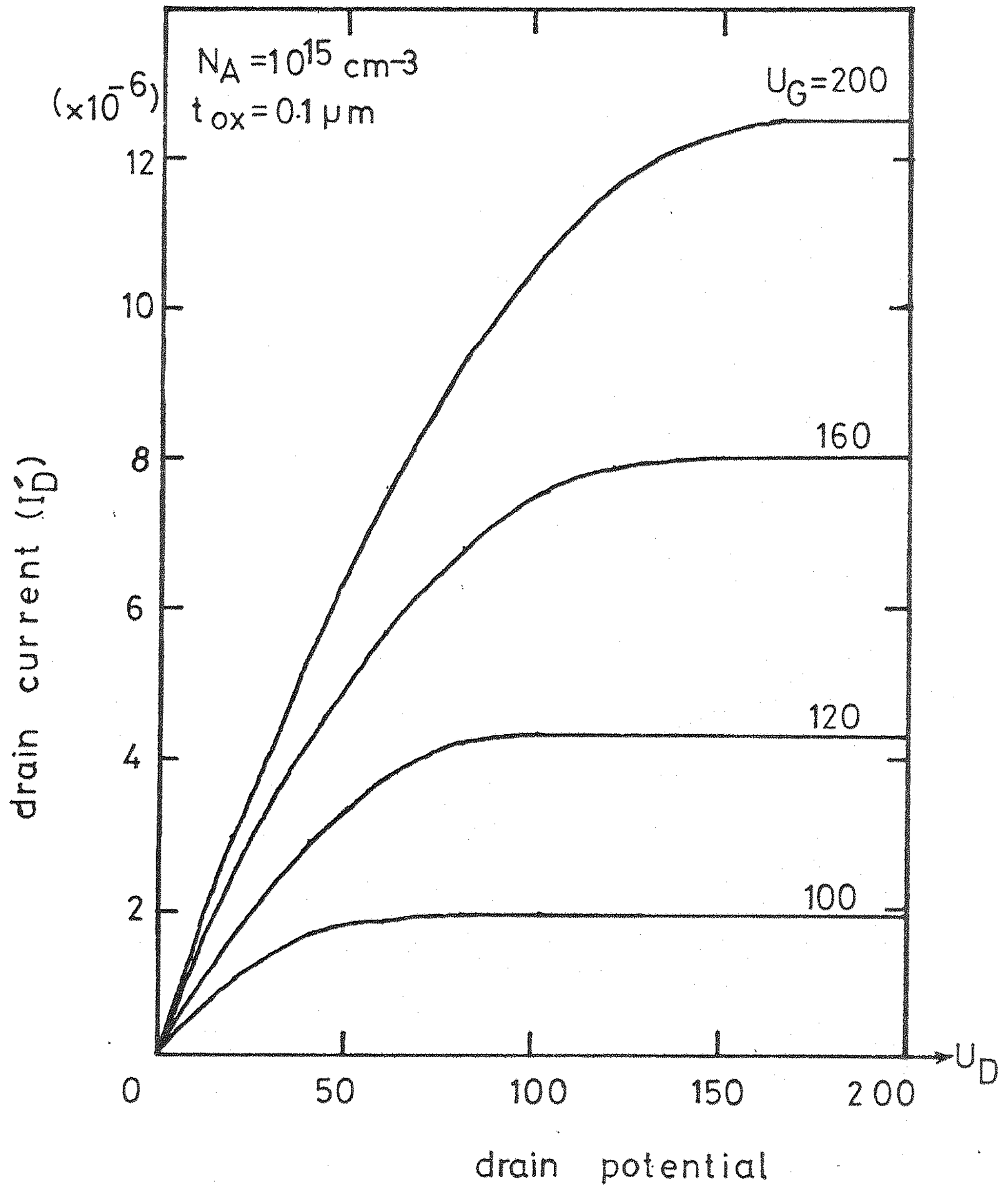


Fig. A1.6 Drain current (I_D) against drain potential (U_D) for various gate potentials (U_G); equation A1.39

where $\phi_s = 2\phi_F + V_s$ (equation A1.41b). The threshold voltage is therefore given by the sum of V_T* and V_{FB}, i.e.:

$$V_T = V_{FB} + 2\phi_F + V_s + \frac{1}{C_{ox}} \sqrt{2\varepsilon_s q N_A (V_s + 2\phi_F)} \quad \text{(A1.43a)}$$

when the threshold voltage is referenced to the source (i.e. the V_{GS} at $\phi_s = V_s + 2\phi_F$), then V_T is given by V_{TS}:

$$V_{TS} = V_{FB} + 2\phi_F + \frac{1}{C_{ox}} \sqrt{2\varepsilon_s q N_A (V_s + 2\phi_F)} \quad \text{(A1.43b)}$$

when $V_s = o$, $V_T = V_{TS} \equiv V_{TO}$, and is given by:

$$V_{TO} = V_{FB} + 2\phi_F + \frac{1}{C_{ox}} \sqrt{2\varepsilon_s q N_A (2\phi_F)} \quad \text{(A1.43c)}$$

The MOS transistor theory presented this far in this appendix is suited to the analysis of single transistors and will be used in the analysis of the photo-response of the MOS transistor.

For the analysis of multi-transistor circuits, this theory is not very suitable as it requires quite a large number of parameters to be accurately specified for each transistor and also involves several iterations to obtain a solution. This analysis would take very long times to complete even when the numerical analyses were performed by a computer. An approximate theory must therefore be sought.

The approximate MOS transistor theory (to be found in most textbooks), will now be derived. This theory neglects the diffusion-current component of the drain current.

A1.3 The Approximate MOS Transistor Theory: (The Text-book Approach)

The MOS transistor theory presented above takes into account both the drift and diffusion components of the drain current. This leads to the correct $U_s = U_s(U_G, \xi)$ relationship. The approximate MOS theory, to be found in text-books (e.g. refs A1.14-A1.17), neglects the diffusion component of the drain current (valid for most of the Triode region of operation, where a uniform inversion channel is assumed to exist between the source and drain terminals of the transistor). This leads to the following relationships for the surface potential[A1.11]:

$$U_s = 2U_F + \xi \tag{A1.44a}$$

and

$$dU_s = d\xi \tag{A1.44b}$$

These expressions lead to the following result for the drain current:

$$I_D' = \int_{2U_F+\xi_S}^{2U_F+\xi_D} \frac{C_{ox}}{\beta}(U_G - U_s) - \frac{\varepsilon_s \sqrt{e^{U_F}}}{\beta L_i}(U_s - 1)^{\frac{1}{2}} \quad dU_s \tag{A1.45}$$

Integrating this expression and applying the limits, we get the following equation for the drain current:

$$I_D' = \frac{C_{ox}}{\beta} \quad (U_G - 2U_F)(\xi_D - \xi_S) - (\xi_D{}^2 - \xi_S{}^2)$$

$$- \frac{2}{3\delta}\left|(2U_F + \xi_D - 1)^{\frac{3}{2}} - (2U_F + \xi_S - 1)^{\frac{3}{2}}\right| \tag{A1.46}$$

This relationship can be further simplified if it is assumed that the substrate resistivity is high so that the magnitude of δ is high[A1.17]. For low values of drain to source voltages, this leads to:

$$I_D' = \frac{C_{ox}}{\beta} \quad (U_G-2U_F)(\xi_D-\xi_s) - \tfrac{1}{2}(\xi_D{}^2-\xi_s{}^2) \qquad \text{(A1.47a)}$$

and if $V_s = o$, we have that:

$$I_D' = \frac{C_{ox}}{\beta} \quad (U_G-2U_F)\xi_D - \tfrac{1}{2}\xi_D{}^2 \qquad \text{(A1.47b)}$$

and re-writing this expression in terms of V_{TO}, we get:

$$I_D = \frac{Z}{L} C_{ox} \mu_n{}^* \{(V_{GS}-V_{TO})V_{DS} - \tfrac{1}{2} V_{DS}{}^2\} \qquad \text{(A1.47c)}$$

When the transistor is in saturation, this equation breaks down due to the incorrect relationships in equation (A1.44). The saturation characteristics are then obtained by assuming that after saturation, the drain current remains at its maximum value. Its value can be obtained by differentiating equation (A1.47) with respect to V_D, setting the differential equal to zero and solving for V_{DS} $(= V_{Dsat})$. This value of V_{Dsat} is then used in equation (A1.47) to obtain the saturation drain current, I_{Dsat}; for V_s=o this gives:

$$I_{Dsat} = \frac{Z}{L} \cdot \frac{C_{ox} \cdot \mu_n{}^*}{2} (V_{GS} - V_{TO})^2 \qquad \text{(A1.48)}$$

To include the effect of a source voltage (and hence the 'back-gate bias effect', represented by equation (A1.43a)) in these simplified

expressions for I_D, we can modify equations (A1.47c) and (A1.48) by using equation (A1.43a); i.e.:

$$I_D = \beta_i \{(V_G-V_T)(V_D-V_s) - \tfrac{1}{2}(V_D{}^2-V_s{}^2)\} \qquad (A1.49a)$$

and

$$I_{Dsat} = \frac{\beta_i}{2}(V_G-V_T)^2 \qquad (A1.49b)$$

where $\beta_i = Z\, C_{ox}\, \mu_n^*/L$ and V_T is given by equation (A1.43a). Equation (A1.43a) can be written in terms of V_{TO}, by noting that V_T can be written thus:

$$V_T = V_{FB} + 2\phi_F + V_s + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A}\,\{(2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}} + (V_s+2\phi_F)^{\frac{1}{2}}\}$$

(A1.50)

or that

$$V_T = V_{TO} + V_s + \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A}\,\{(V_s+2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}\} \qquad (A1.51a)$$

$$V_T = V_{TO} + V_s + K\,\{(V_s+2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}\} \qquad (A1.51b)$$

$$V_T = V_{TO} + V_s + \Delta V_T \qquad (A1.51c)$$

where $K = \frac{1}{C_{ox}}\sqrt{2\varepsilon_s q N_A}$ and is known as the substrate body factor and $\Delta V_T = k\{(V_s+2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}\}$. Using this new notation we can re-write the drain current as:

$$I_D = \beta_i\{(V_G-V_s-V_{TO}-\Delta V_T)(V_D-V_s) - \tfrac{1}{2}(V_D{}^2-V_s{}^2)\}$$

$$= \beta_i\{(V_{GS}-V_{TS})(V_D-V_s) - \tfrac{1}{2}(V_D{}^2-V_s{}^2)\} \qquad \text{(A1.52a)}$$

and

$$I_{Dsat} = \frac{\beta_i}{2}\{V_G-V_s-V_{TO}-\Delta V_T\}^2$$

$$= \frac{\beta_i}{2}(V_{GS}-V_{TS})^2 \qquad \text{(A1.52b)}$$

where V_{TS} is now defined as the threshold voltage (referenced to the source):

$$V_{TS} = V_{TO} + K\{(V_s+2\phi_F)^{\frac{1}{2}} - (2\phi_F)^{\frac{1}{2}}\} \qquad \text{(A1.53)}$$

This approach involves some slight approximations, but provides more tractable expressions suitable for analysing circuits of more than one transistor, and have been used successfully by several authors, e.g. Ref. A1.16.

APPENDIX A2 : OPTICAL TRANSMISSION THROUGH THE GATE LAYERS OF A POLYSILICON GATE MOS DIODE

The treatment of the optical transmission through thin films is adapted from Heavens[5.8]. Only the case of normal incidence will be considered. Figure A2.1 illustrates the path of light through the films. The transmitted electric field vectors in each medium are shown as $E^{+}_{(x)}$ and the reflected as $E^{-}_{(x)}$, the media from air to the substrate are numbered 0 to 4.

At an interface between non-absorbing materials with refractive indices n_o and n_1 (Figure A2.2(a)), the reflected and transmitted electric field amplitudes are related to the incident electric field amplitude (E^{+}_{o}) by the Fresnel Coefficients of reflection (r) and transmission (t). For normal incidence, these are given by[5.8]:

$$r = \frac{E^{-}_{o}}{E^{+}_{o}} = \frac{n_o - n_1}{n_o + n_1} \qquad \text{(A2.1a)}$$

$$t = \frac{E^{+}_{1}}{E^{-}_{o}} = \frac{2\, n_o}{n_o + n_1} \qquad \text{(A2.1b)}$$

Figure A2.2 represents light of normal incidence, but the rays are shown at an angle for clarity.

The reflected and transmitted intensities are related to the incident intensity by[5.8]:

$$R = \left| \frac{E^{-}_{0}}{E^{+}_{0}} \right|^2 = r.r^* \qquad \text{(A2.2a)}$$

$$T = \frac{|n_1|}{|n_0|} . \left| \frac{E^{+}_{1}}{E^{+}_{0}} \right|^2 = \left| \frac{n_1}{n_0} \right| . \; tt^* \qquad \text{(A2.2b)}$$

The effect of an absorbing medium can be included in the above relations by writing the complex refractive index of that medium[5.7,5.8]:

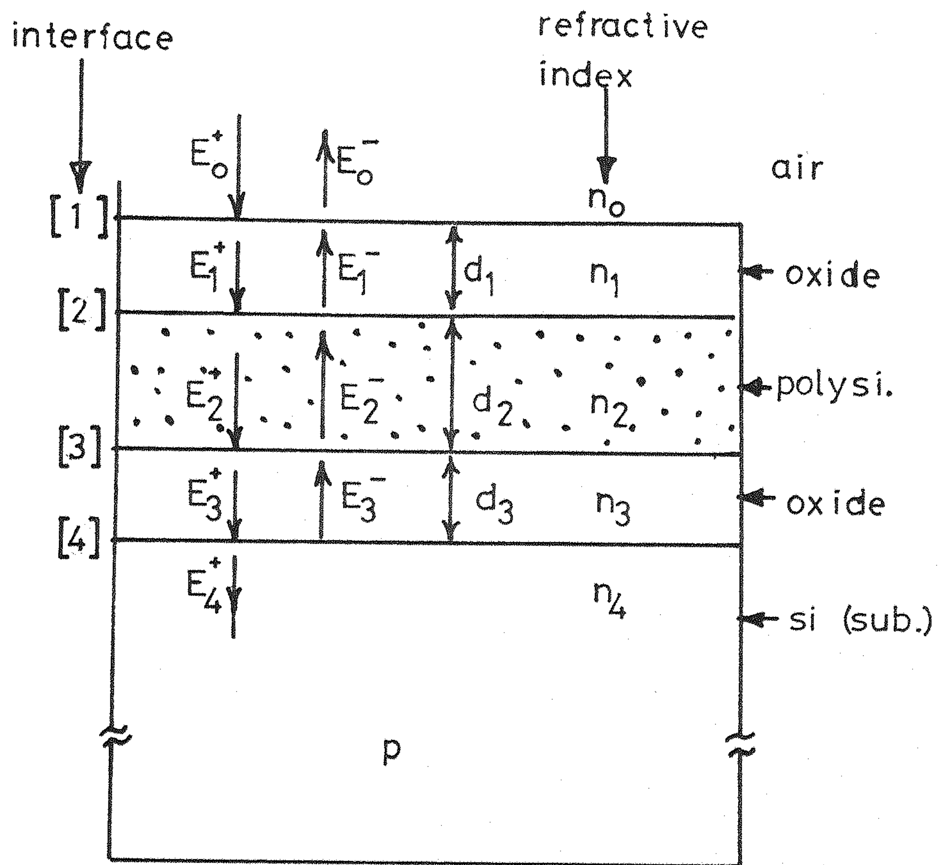
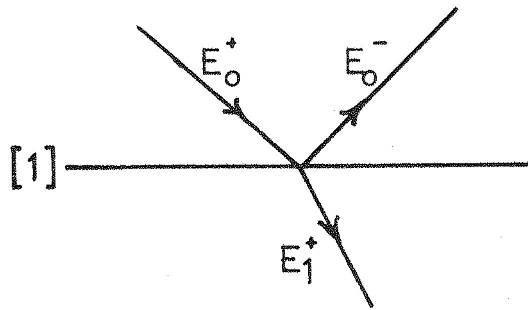


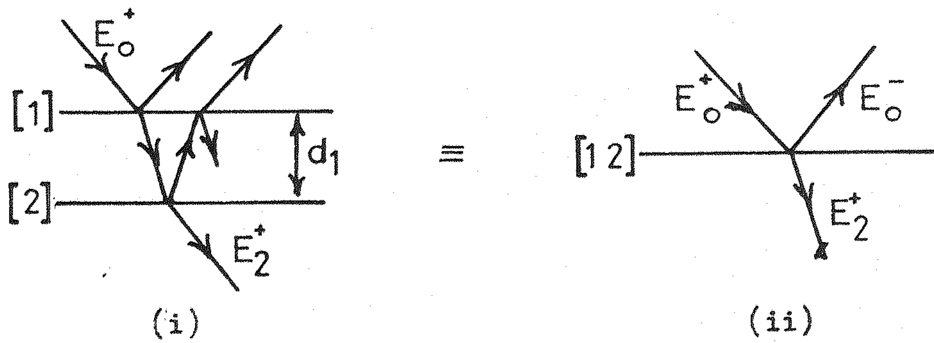
Fig. A2.1 Light path through the gate layers of the polysilicon-gate MOS transistor.



$$r_1 = \frac{E_o^-}{E_o^+} = \frac{n_o - n_1}{n_o + n_1} \quad ; \qquad R = r\,r^*$$

$$t_1 = \frac{E_1^+}{E_o^+} = \frac{2\,n_o}{n_o + n_1} \quad ; \qquad T = \frac{|n_1|}{|n_o|}\,t\,t^*$$

(a)



(i) (ii)

$$r_{12} = \frac{r_1 + r_2\,e^{-2j\delta_1}}{1 + r_1 r_2\,e^{-2j\delta_1}} \qquad t_{12} = \frac{t_1\,t_2\,e^{-j\delta_1}}{1 + r_1 r_2\,e^{-2j\delta_1}}$$

(b)

Fig. A2.2 (a) Definition of Fresnel Coefficients and (b) Fresnel coefficients for a 'sandwich'; for normal incidence (from ref. 5.8).

$$\tilde{n} = n - j\frac{\alpha\lambda}{2\pi} \tag{A2.3}$$

where α is the absorption coefficient and λ is the wavelength of the illumination.

Figure A2.2(b) shows a layer of thickness d_1 sandwiched between media 0 and 2. The Fresnel coefficients for such a system can be derived[5.8] to give:

$$r = \frac{r_1 + r_2\, e^{-2j\delta_1}}{1 + r_1 r_2\, e^{-2j\delta_1}} \tag{A2.4a}$$

$$t = \frac{t_1 t_2\, e^{-j\delta_1}}{1 + r_1 r_2\, e^{-2j\delta_1}} \tag{A2.4b}$$

where $\delta_1 = 2\pi\, n_1\, d_1/\lambda$; and r_1, t_1 and r_2, t_2 are the Fresnel coefficients of interfaces [1] and [2] as given by equation A2.1, respectively. As shown in Figure A2.2(b)(ii), this combination of layers can be treated as a single interface [12]. Using this reduction technique step by step, the layers of Figure A2.1 can be analysed to obtain the effective Fresnel coefficients for the whole system. These coefficients can be used with equation A2.2 to obtain the overall transmission ($T(\lambda)$) and reflection ($R(\lambda)$) characteristics of the gate layers of the MOS diode.

Consider first, layer 3 on layer 4; the Fresnel coefficients are given by:

$$r_{34} = \frac{r_3 + r_4\, e^{-2j\delta_3}}{1 + r_3 r_4\, e^{-2j\delta_3}} \tag{A2.5a}$$

$$t_{34} = \frac{t_3 t_4\, e^{-j\delta_3}}{1 + r_3 r_4\, e^{-2j\delta_3}} \tag{A2.5b}$$

Next, consider layer 2 on layer (34); the Fresnel coefficients are now given by:

$$r_{234} = \frac{r_2 + r_{34}\, e^{-2j\delta_2}}{1 + r_2 . r_{34}\, e^{-2j\delta_2}} \tag{A2.6a}$$

$$t_{234} = \frac{t_2\ t_{34}\ e^{-j\delta_2}}{1 + r_2.r_{34}\ e^{-2j\delta_2}} \qquad \text{(A2.6b)}$$

and finally for layer 1 on layer (234); we have for the Fresnel coefficients:

$$r = r_{1234} = \frac{r_1 + r_{234}e^{-2j\delta_1}}{1 + r_1.r_{234}e^{-2j\delta_1}} \qquad \text{(A2.7a)}$$

$$t = t_{1234} = \frac{t_1\ t_{234}\ e^{-j\delta_1}}{1 + r_1.r_{234}\ e^{-2j\delta_1}} \qquad \text{(A2.7b)}$$

where

$$r_{(x)} = \frac{n_{(x-1)} - n_{(x)}}{n_{(x-1)} + n_{(x)}} \qquad \text{(A2.8a)}$$

$$t_{(x)} = \frac{2.n_{(x-1)}}{n_{(x-1)} + n_{(x)}} \qquad \text{(A2.8b)}$$

$$\delta_{(x)} = \frac{2\pi\ n_{(x)}\ d_{(x)}}{\lambda} \qquad \text{(A2.8c)}$$

We are now in a position to obtain the required transmission characteristics $T_{(\lambda)}$:

$$T_{(\lambda)} = \left|\frac{n_4}{n_0}\right| . \left|t_{1234}\right|^2 \qquad \text{(A2.9)}$$

The transmission, which is dependent on the wavelength of the illumination, determines the spectral characteristic of the photocurrent of the polysilicon gate MOS diode.

APPENDIX A3 : OUTLINE OF THE PROCESSING OF THE MOS-PHOTOTRANSISTORS

This Appendix presents an outline of the processing steps used in the fabrication of the polysilicon gate p-MOS transistors, used in the optical experiments.

1. RCA clean.

2. Initial oxide : temp. 1100°C

   Gas 1 : 1 litre/min O_2 in steam, for 120 minutes.

   Gas 2 : 1 litre/min dry O_2, for 5 minutes.

3. Negative Photomech. (Active Areas) : Mask [1]

4. Gate Oxide : temp. 1100°C

   Gas 1 : 2 litre/min dry O_2 + 30 cc/min HCℓ, for 45 minutes.

   Gas 2 : 1 litre/min N_2, for 15 minutes.

5. Polysilicon deposition (CVD) : temp. 600°C

   Gas : Silane at 0.5 torr.

6. Polysilicon Oxidation : temp. 1100°C

   Gas 1 : 1 litre/min dry O_2, for 25 minutes.

   Gas 2 : 1 litre/min N_2, for 5 minutes.

7. Positive Photomech. (Gate Areas) : Mask [2]

8. Boron deposition (Boron Nitride Slices) : temp. 900°C

   Gas 1 : 3 litre/min N_2, for 30 minutes.

9. Boron drive-in : temp. 1100°C

   Gas 1 : 1 litre/min N_2, for 30 minutes.

   Gas 2 : 1 litre/min O_2, for 20 minutes.

10. Negative Photomech. (Contract windows) : Mask [4]

11. Aluminium Deposition on front surface (∿ 0.5 μm)

12. Positive Photomech. (Al. Pattern) : Mask [6]

13. Aluminium Deposition on back of slices (∿ 0.5 μm)

14. Alloying and Annealing

Gas 1 : 1 litre/min N_2 at 500°C for 10 minutes.

Gas 2 : 1 litre/min H_2/N_2 (60/40%) at 420°C for 30 minutes.

The polysilicon film is doped p-type with boron at the same time as the source and drain.

REFERENCES

1.1 J. G. Smith and H. E. Oldham; IEEE JSSC-12, 247 (1977).

1.2 H. E. Oldham; Ph.D. Thesis, Southampton University (1978).

1.3 Pao and Sah; S.S. Electron. 9, 927 (1966).

1.4 Baccarani et al; S.S. Electron. Dev. 2, 62 (1978).

1.5 F. Van de Wiele; S.S. Electron. 22, 991 (1979).

2.1 L. M. Terman; S.S. Electron. 2, 1 (1961).

2.2 R. A. Smith; Semiconductors, Cambridge University, 1959, Ch. 8.

2.3 W. C. Dash and R. Newman; Phys. Rev. 99, 1151 (1955).

3.1 H. E. Oldham; Ph.D. Thesis, Southampton University, 1978.

3.2 J. M. Ley; Proc. IEE 117, 1057 (1970).

3.3 Electro-optic Developments Ltd., Sales publication, 1973.

3.4 J. G. Smith and H. E. Oldham; IEEE JSSC-12, 247 (1977).

4.1 A. D. Brown, $MM Mk III, Electronics Dept., Southampton University, 1978.

4.2 G. Baccarani et al; S.S. Electron. Dev. 2, 62 (1978).

4.3 R. H. Crawford; MOSFET in Circuit Design, McGraw-Hill, 1967, Chapter 2.

4.4 Penny and Lau; MOS Integrated Circuits, Van Nostrand Reinhold, 1967, Chapter 2.

4.5 R. H. Crawford; MOSFET in Circuit Design, McGraw-Hill, 1967, Chapter 4.

4.6 Penny and Lau; MOS Integrated Circuits, Van Nostrand Reinhold, 1967, Chapter 4.

4.7 R. H. Crawford; MOSFET in Circuit Design, McGraw-Hill, 1967, Chapter 5.

4.8 Carr and Mize; MOS/LSI Design and Applications, McGraw-Hill, 1972, Chapter 4.

4.9 M. R. Spiegel; Mathematical Handbook, McGraw-Hill, 1968.

4.10 Glaser & Subak-Sharpe; Integrated Circuit Tengineering, Addison Wesley, 1977, Chapter 4.

5.1 K. Okamoto; S.S. Electron. 17, 1155 (1974).

5.2 Tong and Lam; S.S. Electron. 19, 422 (1976).

5.3 Norman and Thomas; IEEE Tr-ED - 27, 731 (1980).

5.4 W. W. Gartner; Phys. Rev. 116, 84 (1959).

5.5 Gorban et al; Sov. Phys. Semicond. 11, 824 (1977).

5.6 Salter and Thomas; S.S. Electron. 20, 95 (1977).

5.7 Brown and Chamberlain; Phys. Stat. Sol. (a) 20, 675 (1973).

5.8 O. S. Heavens; Optical Properties of Thin Solid Films, Butterworth (1955).

5.9 S. M. Sze; Physics of Semiconductor Devices, Wiley (1969), p.661.

5.10 Dash and Newman; Phys. Rev. 99, 1151 (1955).

5.11 Okamoto and Mochizuki; Proc. IEEE 59, 1351 (1971).

5.12 Okamoto and Inoue; S.S. Electron. 16, 657 (1973).

5.13 Lam and Tong; El. Lett. 12, 13 (1976).

5.14 Card and Fang; J. Appl. Phys. 48, 2481 (1977).

5.15 Shmyreva and Ivashchuk; Sov. Phys. Semicond. 13, 1067 (1979).

5.16 Grove and Fitzgerald; S.S. Electron. 9, 783 (1966).

5.17 S. M. Sze, Physics of Semiconductor Devices, Wiley (1969).

5.18 Panayotatos and Card; S.S. Electron. 23, 41 (1980).

5.19 D. L. Pulfrey; S.S. Electron. 20, 255 (1977).

5.20 C. T. Sah; IEEE Tr. ED-11, 324 (1964).

6.1 K. Okamoto; S.S. Electron. 17, 1155 (1974).

6.2 H. C. Card and F. F. Fang; J. Appl. Phys. 48, 2481 (1977).

6.3 P. Panayotatos et al; Proc. IEEE 65, 1213 (1977).

6.4 P. Panayotatos and H. C. Card; S.S. Electron. 23, 41 (1980).

6.5 D. L. Pulfrey; S.S. Electron. 20, 455 (1977).

6.6 G. C. Salter and R. E. Thomas; S.S. Electron. 20, 95 (1977).

A1.1 Kingston and Neustadter; J. Appl. Phys. 26, 718 (1955).

A1.2 Garrett and Brattain; Phys. Rev. 99, 376 (1955).

A1.3 S. M. Sze; Physics of Semiconductor Devices, Ch. 9, Wiley, 1969.

A1.4 B. E. Deal et al; J. Electrochem. Soc. 114, 266 (1967).

A1.5 Badcock and Lamb; Int. J. Electron. 24, 1, (1968).

A1.6 Grove and Fitzgerald; S.S. Electron. 9, 783 (1966).

A1.7a J. E. Lilienfeld; U.S. Patent no. 1745175 (1930).

A1.7b O. Heil; British Patent no. 439457 (1935).

A1.8 Shockley and Pearson; Phys. Rev. 74, 232 (1948)

A1.9 Kahng and Attalla; IRE Solid-State Device Research Conf. Carnegie Inst. of Tech., Pittsburgh, Penn. (1960).

A1.10 Pao and Sah; S.S. Electron. 9, 927 (1966).

A1.11 Baccarani et al; S.S. Electron. Dev. 2, 62 (1978).

A1.12 F. Van de Wiele; S.S. Electron. 22, 991 (1979).

A1.13 Merckel et al; IEEE Tr. Electron. Dev. ED-19, 681 (1972).

A1.14 A. S. Grove; Physics and Technology of Semiconductor Devices, Wiley, 1967.

A1.15 S. M. Sze; Physics of Semiconductor Devices, Wiley, 1969.

A1.16 R. H. Crawford; MOSFET in Circuit Design, McGraw-Hill, 1967.

A1.17 Penny and Lau; MOS Integrated Circuits, Van Nostrand, Reinhold, 1967.