AN INVESTIGATION OF LEAKAGE CURRENTS AND CHARGE PUMPING CURRENTS IN Si-DIODES

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UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF SCIENCE

ELECTRONICS

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AN INVESTIGATION OF LEAKAGE CURRENTS AND CHARGE PUMPING CURRENTS IN Si-DIODES

by Zambia J. Dalierakis

A study of leakage current in silicon p-n gated diodes with HCl gate oxidation and 'TCE' gate oxidation is presented. The investigation was concerned with the relative importance of the different HCl concentration in the process which were used, and the variants of processing of the devices. A study was made using an alternative oxidation technique using Trichloroethylyne performed by G.J. Decklerk of the Katholieke Universiteit Leuven, Belgium. It is concluded that there was an overriding controlling factor in the processing schedules used here, which resulted in the improvements in the values of bulk lifetime and surface recombination velocity.

A new method is described for determining the surface state density at the $Si-SiO_2$ interface in the channel of a p^+n gated diode from the charge pumped current flowing to the substrate when gate pulses of constant amplitude are applied. A theoretical analysis of this method is described which suggests that from a simple measurement of the pumped current the energy distribution of surface state density may be obtained. Representative results obtained on a set of gated diodes and a CCD show an increase in the surface state density near the middle of the band-gap. However, further work must be done to confirm the reliability of the data in order to apply the technique for general purpose surface state density measurements.

1. INTRODUCTION

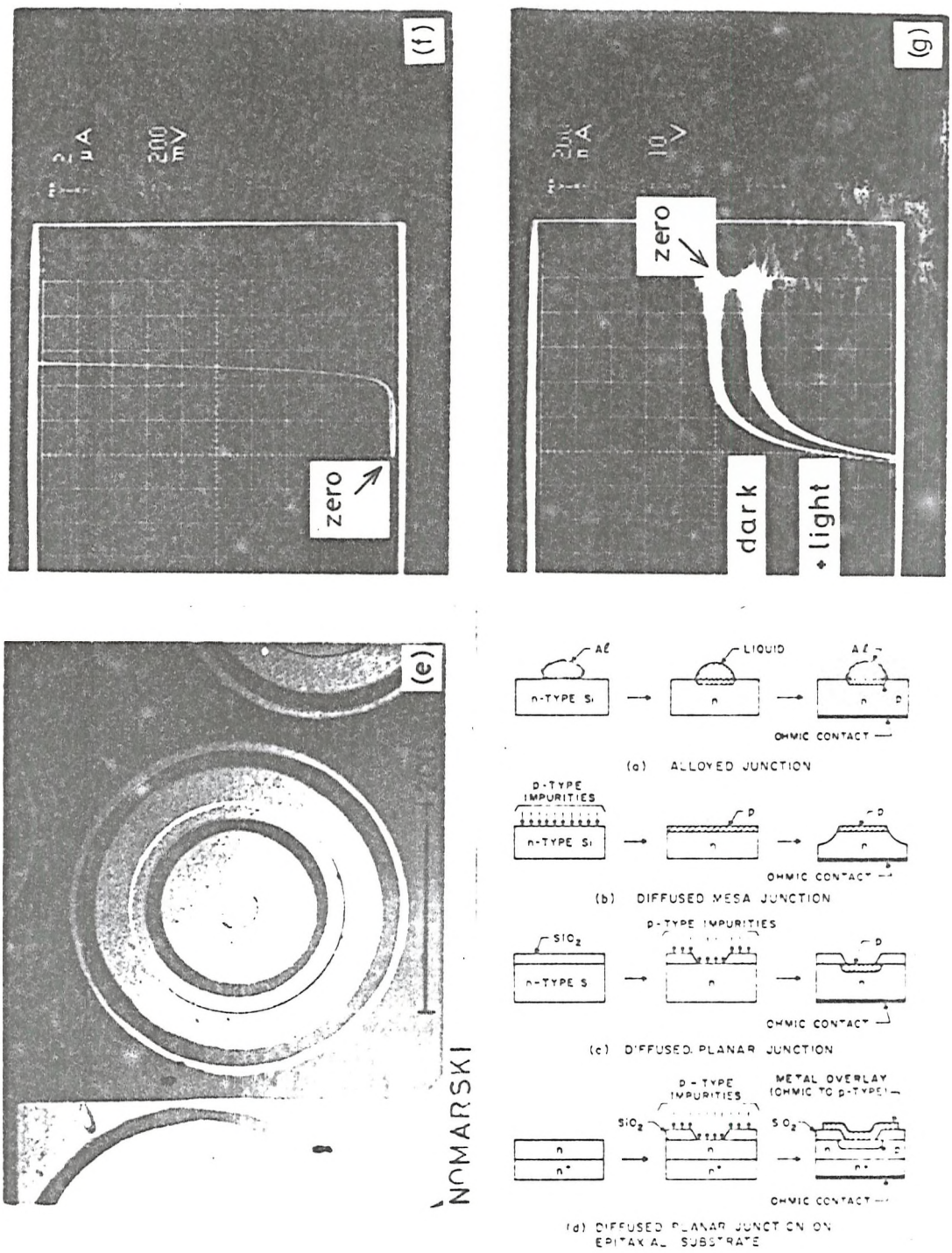
1a Leakage Current

One of the most important requirements of the microelectronics industry is the fabrication of suitable p-n junctions in semiconducting crystals. Silicon, for many reasons, has evolved as the most suitable material in which to form the devices required for complex electronic systems. Planar processing of silicon has been developed in the last decade into a highly sophisticated method of fabrication since the pioneering work of Shockley in the 1940's (1). Rectifying p-n junctions are manufactured in silicon by doping, through a 'mask', selected regions with elements from group III or V of the Period Table in a silicon substrate which is already lightly doped with group V or III elements respectively. The 'mask' is a thin film of silicon oxide thermally grown on the substrate. The junction thus formed will pass high currents for a forward bias of only about 1 volt and a relatively very small current at reverse biases of many volts (Fig. 1.1). The magnitude of this reverse current is usually called 'leakage current' and is dependent on the physical structure of the junctions as will be shown in Chapter 2.

Usually, the leakage current is insignificant. However, for some applications, extremely low leakage is required, e.g., opto-electronic imagers, charge coupled devices (surface and buried channel), self addressed diode arrays high gain, low current, bipolar transistors.

In Chapter 2 and 4 of this thesis we are interested in the leakage current in gated diodes and charge coupled devices. Surface channel charge coupled devices (SCCD) consist of closely spaced MOS capacitors that are pulsed into deep depletion sequentially for times much shorter than that required to form an inversion layer of minority carriers by thermal generation. This causes potential wells to be formed at the $Si-SiO_2$ interface which are then used to store and transfer minority carriers representing the sampled analogue signal, as shown in Fig. 1.2. In the buried-channel charge coupled device (BCCD) the potential wells are formed at some distance below the oxide-semiconductor interface and are used to store and transfer majority carriers, as shown in Fig. 1.3.

For image sensing purposes, the potential well pattern is held constant for a certain time known as the 'intergration time'



(a) - (d) junction fabrication methods.

(e) planar diode (two metal electrodes on oxide) (+one central anode contact)

(f), (g) forward & reverse bias characteristics of (e).

Fig. 1·1

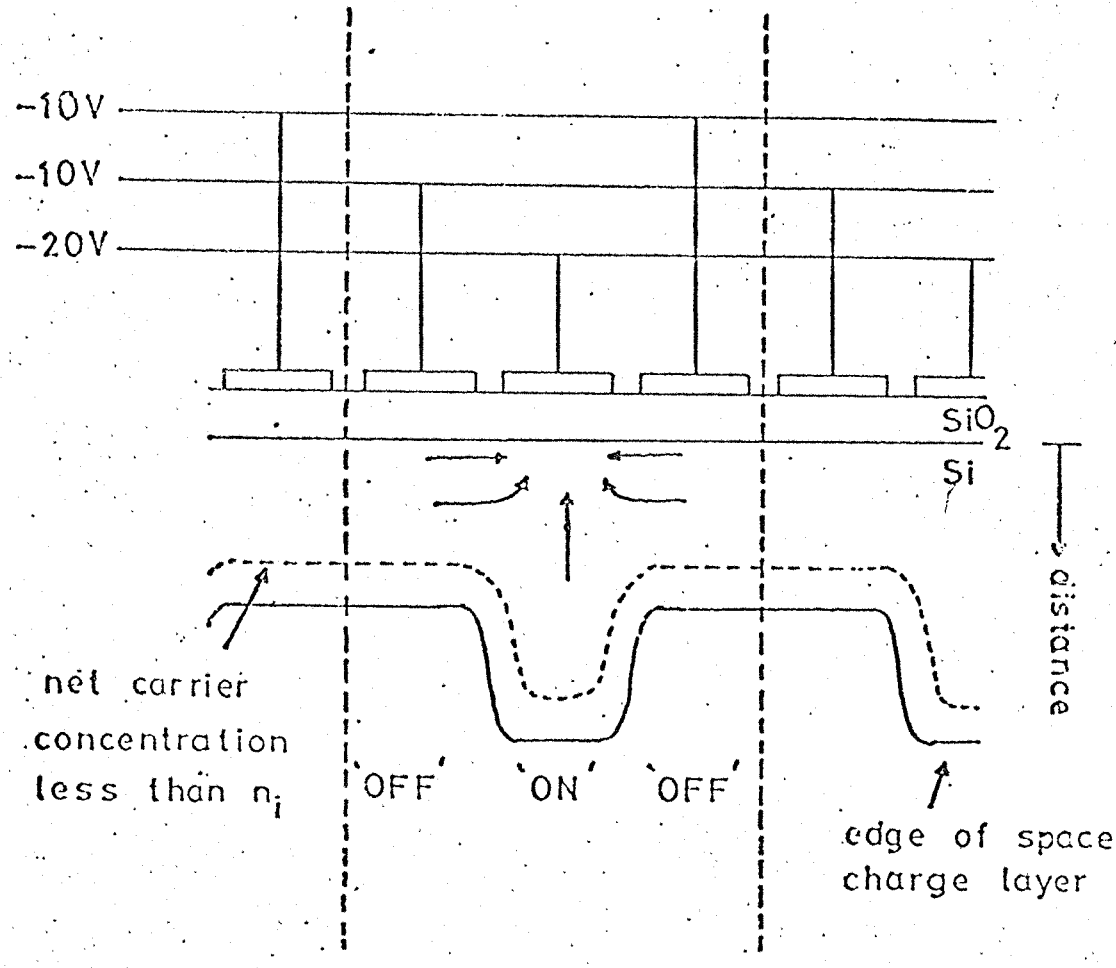


Fig. 1.2 A surface channel CCD

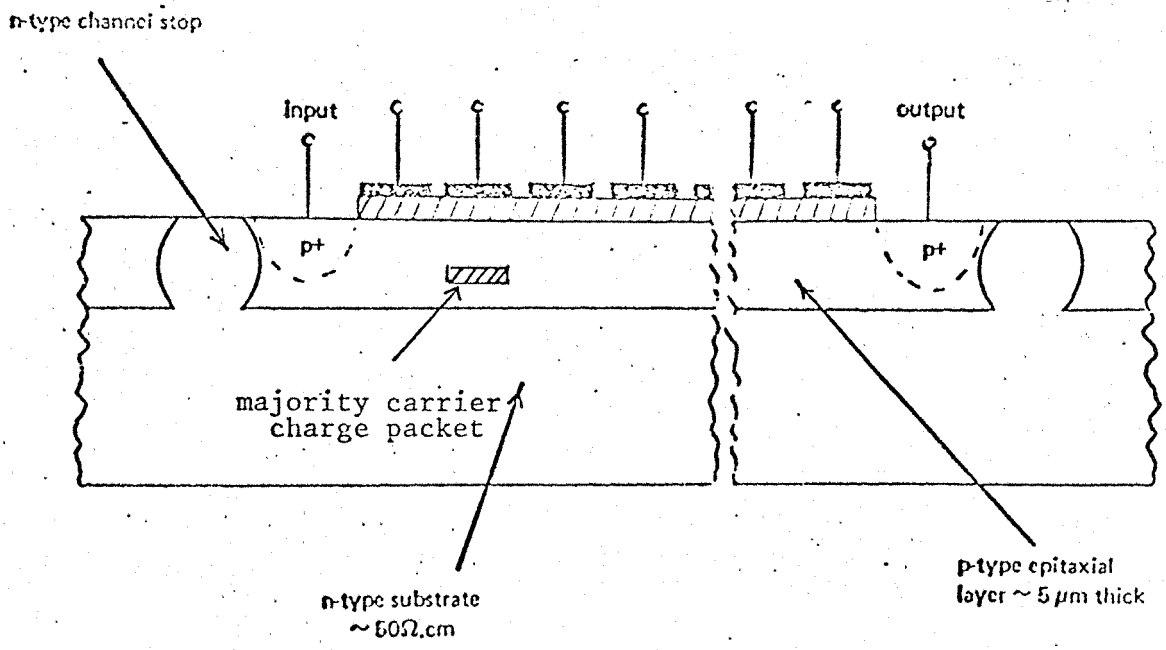


Fig. 1.3 A Buried channel CCD

(typically tens of msecs) whence a spatial distribution of optically generated minority carriers under the CCD elements is obtained representing the image. These charges are then transferred and collected by a quick succession of clock pulses for further processing and display. For low light level imaging applications the integration time needs to be as long as possible but the limit is set by the thermal generation of carriers in the substrate.

In the low frequency operation of the CCD's the same thermal generation again sets the limit. In this case, the potential pattern sweeps all of the gates at a constant rate and hence the contribution of thermally generated carriers to each of the output pulses will be roughly the same. If the generation current under each gate is assumed uniform and equal to J (in one electrode area A_s), and t_c is the clock period and equal to $1/f_c$ where f_c is clock frequency, and if there are n electrodes in all, then the total contribution of thermally generated carriers to each output pulse will be:

$$Q_\ell = q(nt_c)JA_s = q(\frac{n}{f_c})JA_s \quad [C] \qquad 1a.1$$

So this noise limits the size of the signal that can be transferred with a reasonable signal to noise ratio.

In plate 1 is shown the output voltage pulses from a CCD 134DRLMPS which is an 8 bit three-phase, p-channel, Aluminium-gate device operated in 'Interrupted Clock' integration mode. This device was manufactured in the Microelectronics laboratory of the Department of Electronics at Southampton University using the same process as is used for the devices extensively measured in this work with the addition of an n^+ 'guard'-ring diffusion step at the beginning of the process. In plate 2 the complete CCD is shown.

There are three major components of thermal generation current, J:

a) Surface generation.

b) Generation in the depleted space-charge region in the bulk.

c) Generation in the neutral bulk within a diffusion length of the depletion region.

Usually at room temperature in Silicon the contribution of the last one is nebligible compared to that of the first two.

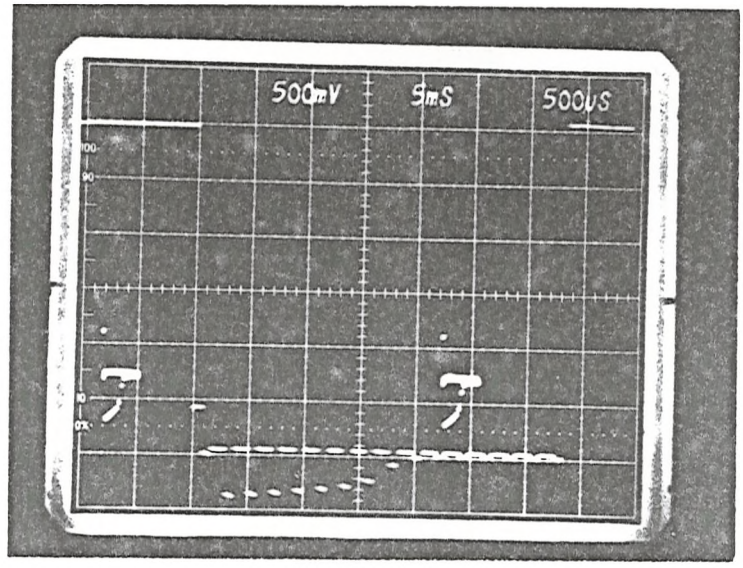


Plate 1. The split time-base display showing the output pulses for an integration time of 30 msec with a clock readout frequency of 5kHz.

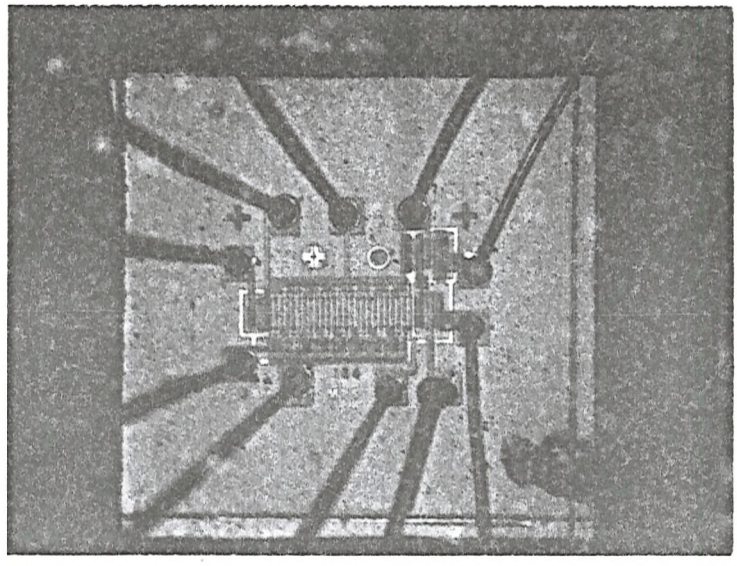


Plate 2. The topography of the 134 DRLMPS 3-phase surface channel CCD used to obtain plate 1.

1b Interface State Measurements

Another aspect of CCD performance is that of transfer inefficiency. In surface channel devices the two most important charge loss mechanisms which limit the charge transfer efficiency of the device are backward flow loss and interface state loss (2).

However, the backward flow loss is a function of the clock driving voltages and by suitable choice of the clocking, waveforms the backward flow loss can be made significantly less than the interface state loss except at high frequencies. So in practice at all but the highest operating frequencies the charge transfer efficiency of the device is expected to be limited by the interface state trapping mechanism.

This loss occurs by the interface states at the $Si-SiO_2$ interface trapping some of the signal charge carriers and not re-emitting all of them within the time allowed for the free charge transfer. It was first thought that the use of Fat Zeroes (i.e. the continuous circulation of a non-zero background charge) would tend to keep the interface states filled and dramatically reduce the loss since this loss occurs because of the unsymmetrical filling and emptying of the interface states. However, it has subsequently become apparent that this technique is only partially successful due to the so called "Edge Effect" which is associated with the edge regions of the transfer gases where the interface states are not refilled by the Fat Zero charge (3,4). This then means that the only really effective way of reducing the interface state loss is to reduce the interface state density. This is achieved in practice by using (100) orientation substrates and including in the processing steps both high temperature ($1050^{\circ}C, N_2$) and low temperature ($420^{\circ}C, H_2/N_2$) annealing treatments. In the best devices to date the value of interface state density is of the order of $10^9/cm^2eV$ and reasonably uniform over the band gap (5). Conventional methods of measuring interface state density are, with the exception of the conductance technique (6), unable to obtain sufficient precision to measure these low values of interface state density.

The conductance technique, though, is a very laborious and time consuming method and it would be highly desirable to develop an alternative, simpler, technique for measuring a finished CCD.

In Chapter 3 an investigation of the technique of 'charge

pumping' is presented which was first suggested by Brugler and Jespers (7) and subsequently by Elliot (8). This is a measuring technique for low surface state densities in packaged commercial devices. The technique involves only a knowledge of the active area of the gate region, the doping level of the substrate and the oxide thickness in the gate regions together with measurements of current flowing to the substrate, in order to calculate the interface state density. The magnitude of the current is of the order of nA depending of the interface state density and the rate of pumping. For very low interface state densities it is merely necessary to increase the rate of pumping charge through the interface states to obtain easily measured currents. The only serious limitation to the method is the presence of gate protection diodes internally connected to the gate to be measured, since it is necessary in some cases to pulse either side of zero volts.

In Chapter 4 the leakage current and charge pumping currents are measured in gated diodes that are fabricated using TCE (trichloroethylene) instead of HCl in the gate oxidation process.

Finally, conclusions and comparisons of the different processing steps are included in the last chapter of this work together with a discussion of the usefulness of the measurement technique.

2. LEAKAGE CURRENT INVESTIGATION

2a Theory of Leakage Current

It is known that under equilibrium conditions electron holes pairs thermally generated everywhere within a p-n junction diode, on average all recombine and no current flow results in the absence of an applied voltage.

However, if a negative voltage is applied to the p-region of a diode with respect to the n-region (reverse bias) the electron-hole paris after generation will be separated and their probability of recombination is thereby diminished. Thus the reverse currents observed in p-n junction diodes are due to electron-hole pairs generated some-place in the semiconductor (Shockley-Read-Hall, 9). At room temperature the reverse current of a silicon p-n junction is due to electron-hole paris generated predominantly (through the action of recombination-generation centres) within the depletion region where the net carrier concentration is below the intrinsic carrier concentration n_i and is called the generation current. At higher temperatures it is also necessary to consider the current due to electron-hole pairs generated in the neutral regions of the p-n junction which is called the diffusion current. This can be seen from the expressions for diffusion and generation currents. Thus for n-type material and $|V_R| >> \frac{kT}{q}$ (Shockley) we have,

$$I_{diff,p} = q \frac{P_{no}}{\tau_p} L_p A_{MJ} = qD_p \frac{n_i^2}{N_D L_p} A_{MJ} \qquad 2a.1$$

where P_{no} is the minority carrier density in equilibrium

τ_p is the minority carrier lifetime in the neutral region

A_{MJ} is the cross-sectional area of the junction

$L_p = \sqrt{D_p \tau_p}$ is the diffusion length of holes in the neutral n-region.

Thus the diffusion current is independent of bias but has a temperature dependence proportional to n_i^2 ($n_i^2 \alpha e^{-Eg/KT}$).

The magnitude of the generation current (current due to generation within the depletion region as explained above) is given by: (Grove, 10).

$$I_{gen} = q|U|WA_{MJ} = \tfrac{1}{2}q\frac{n_i}{\tau_o} WA_{MJ} \qquad 2a.2$$

where τ_o is the effective lifetime within a reversed bias depletion region and is given by:

$$\tau_o = \frac{\sigma_n e^{(E_t-E_i)/KT} + \sigma_p e^{-(E_t-E_i)/KT}}{2\sigma_p \sigma_n \upsilon_{th} N_t} \qquad 2a.3$$

U is the rate of generation of electron-hole pairs in the depletion region.

W is the width of depletion region.

For the simple case of $E_t=E_i$ we can see that the generation current component has the same temperature dependence as n_i that is

$$I_{gen} \propto e^{-Eg/2KT}$$

All the experiments that will be described here are done at room temperature so the current that we measure is almost all generation current from the depletion region.

So far we have considered only generation of electron-hole pairs at centres that are distributed uniformly within the semiconductor bulk. However, at the surface of a semiconductor the generation of electron-hole pairs is associated with a possibly different concentration of centres and their spatial distribution is usually not known. In this case a recombination velocity of the surface, S_o, is defined which is related to the surface generation rate U_s per unit area as will be shown later and is defined as

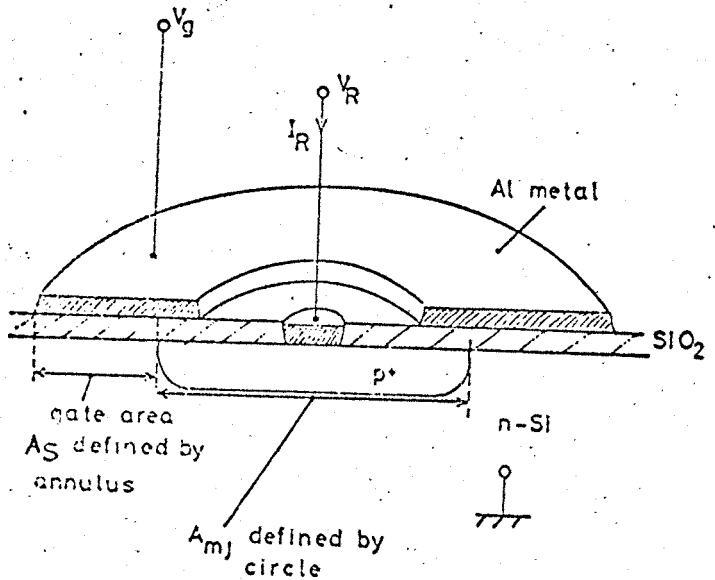
$$S_o = \sigma_s \upsilon_{th} N_{st}$$

where σ_s is the mean cross section for holes and electrons,

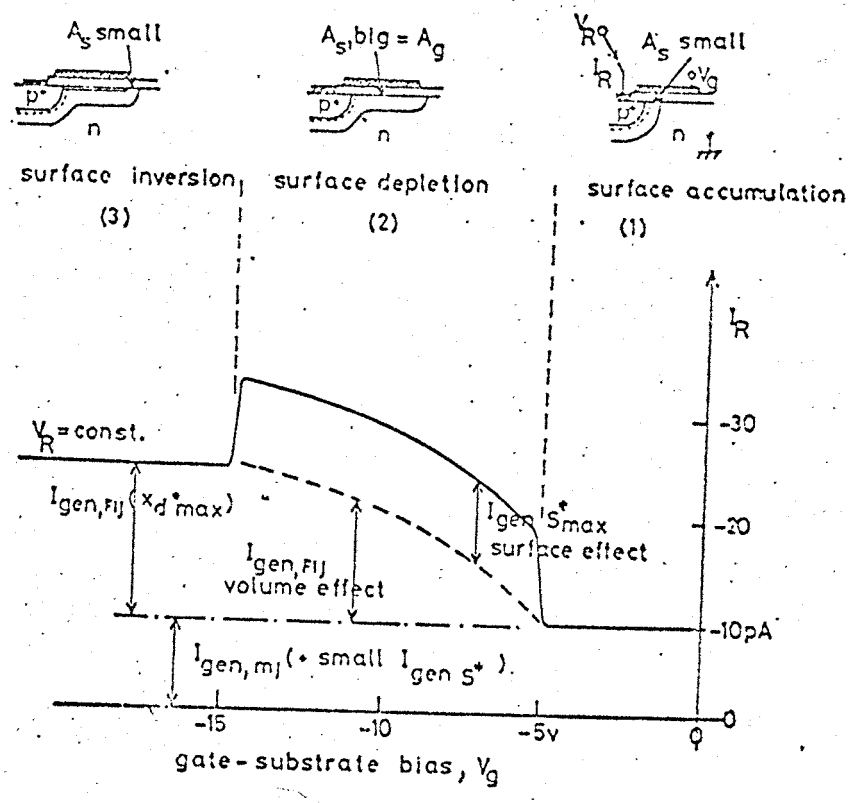
υ_{th} is the thermal velocity,

N_{st} is the density of the centres per unit surface area.

In order to distinguish between the surface generation current and the generation current in the rest of the depletion region a gated diode structure, as was introduced by Grove (10) is used. This structure is shown in Fig. 2.1. The introduction of a gate electrode over the surface as shown, enables the geometry of the depletion region at the surface to be modified in a controlled manner. In particular, this enables us to change the active


V_g
V_R
I_R
Al metal
SiO_2
p+
n-Si
gate area
A_S defined by
annulus
A_{mJ} defined by
circle

F . 2.1


A_S small
A_S big = A_g
A_S small
V_R
I_R
V_g
p+
n
surface inversion
(3)
surface depletion
(2)
surface accumulation
(1)
I_R
V_R = const.
-30
-20
-10pA
$I_{gen,FIJ}$ (x_d max)
$I_{gen,FIJ}$
volume effect
I_{gen} S_{max}
surface effect
$I_{gen,mJ}$ (+ small $I_{gen\ S^*}$).
-15
-10
-5v
0
gate-substrate bias, V_g

F . 2.2

surface area, A_s, by altering the gate voltage. Thus we are able to measure an increased surface generation component from which we can determine the value of the surface recombination velocity S_o as will be shown later in this chapter. Let us now consider the reverse current versus gate voltage characteristic at a fixed reverse voltage of a gate controlled p^+n junction depicted in Fig. 2.2. An analogous characteristic holds for n^+p with the appropriate changes in sign for voltages and currents . At zero gate voltage it is usually found that (for n-type substrate) the semiconductor surface is in accumulation (11). In this case only those centers which are within the depletion region of the metallurgical junction contribute to the leakage current. This is shown in the case (1) of Fig. 2.2. As the gate is biased more negatively, a voltage is reached at which the surface under the gate changes from being accumulated to being depleted. This is shown in case (2) of Fig. 2.2. At this point we observe an increase in leakage current. This increase is due to the changed surface area of the depletion region and also to the changed surface generation rate, U_s, which is dependent on the concentration of free carriers at the surface. The gate voltage at which this occurs is such that the surface potential, ψ_s, is sufficient to deplete the surface of majority carriers n_s. This surface generation current depends on the product $A_s U_s$. But U_s depends on the surface recombination velocity S and on the value of the supression of the carrier concentration at the surface Δp, which for a reverse bias $|V_R| >> \frac{KT}{q}$ is usually constant and equal to the minority carriers concentration at equilibrium, $-p_{no}$.

So we have

$$U_s = S\Delta p \qquad 2a.4$$

Therefore

$$U_{s,max} = -S_{max}p_{no} = -S_o \frac{n_{no}}{2n_i} p_{no} \qquad 2a.5$$

since $n_{no}p_{no} = n_i^2$, $U_{s,max} = -S_o \frac{n_i}{2}$ 2a.6

Where the conventional approximations

$\sigma_{ns} = \sigma_{ps} = \sigma_s$ and $E_{ts} = E_{is}$ have been made. Therefore while the surface is depleted, we have a total surface generation component,

$$I_{gen,s} = qU_{s,max} \quad A_s = \tfrac{1}{2}qn_i S_o A_s \qquad 2a.7$$

The surface area A_s, in this region is defined by the entire area of the gate electrode covering the undiffused substrate as shown in Fig. 2.1. This current is independent of the reverse voltage and remains constant with changes in the gate voltage as long as the surface is in depletion but reduces again when the surface becomes inverted with sufficient carriers to reduce the surface generation rate U_s.

In the second case as well as the surface current, we have a generation component from the depletion region below the surface, the field induced junction,

$$I_{gen,FIJ} = qUx_d A_s = q\left(\frac{x_d}{2\tau_{oFIJ}}\right) A_s \qquad 2a.8$$

This component, however, increases as V_G is made more negative, because x_d increases and takes the maximum x_{dmax} when inversion is reached. It is evident from this equation that $I_{gen,FIJ}$ depends on the magnitude of reverse bias through x_d, and in fact increases with V_R since $x_d \propto V_R^{\frac{1}{2}}$ for an abrupt one-sided junction. This current reaches a limit at inversion of the interface, as shown in Fig. 2.2(b). At some more negative gate voltage depending on the value of reverse junction bias, the substrate surface becomes inverted. The surface is no longer included in the depletion region and therefore the extra surface generation current is reduced almost to zero leaving only the field induced depletion region below the surface and the metallurgical junction as significant sources of electron-hole pairs. In this case the width of the field induced depletion region reaches its maximum value x_{dmax}. So during inversion the total current reduces to some value depending on the volume of the Field Induced depletion region and the Metallurgical Junction depletion region and the lifetimes τ_{oFIJ}, τ_{oMJ} respectively, and remains at this value for further negatively increased gate voltages as is shown in case (3) of Fig. 2.2.
Summarising, for all three cases we have
For accumulation:

$$I_1 = I_{gen,MJ} = \tfrac{1}{2}q\,\frac{n_i}{\tau_{oMJ}}\,WA_{MJ} \qquad 2a.9$$

For depletion:

$$I_2 = I_{gen,MJ} + I_{gen,FIJ} + I_{gen,s}$$

$$= \tfrac{1}{2}q \frac{n_i}{\tau_{oMJ}} WA_{MJ} + \tfrac{1}{2}q \frac{n_i}{\tau_{oFIJ}} x_d A_s + \tfrac{1}{2}qn_i S_o A_s \qquad 2a.10$$

For inversion:

$$I_3 = I_{gen,MJ} + I_{gen,FIJ}$$

$$= \tfrac{1}{2}q \frac{n_i}{\tau_{oMJ}} WA_{MJ} + \tfrac{1}{2}q \frac{n_i}{\tau_{oFIJ}} x_{dmax} A_s \qquad 2a.11$$

The currents I_1, I_2, I_3 are measured experimentally and the difference between I_2 amd I_3 gives the surface generation current from which S_o can be calculated. The difference between I_3 and I_1 gives the field induced junction current from which τ_{oFIJ} can then be calculated. A_s may be measured by photography and geometric calculations as will be shown later in this chapter while x_{dmax} may be calculated from the measured doping concentration using the relationship:

$$x_{dmax} = \frac{2\varepsilon_o K_s \psi_s (inv)}{qN_D} \qquad 2a.12$$

as shown by Roberts (15),

where ε_o = permitivity of free space

K_s = relative permitivity of silicon

N_D = donor concentration

ψ_s (inv) = surface potential at inversion where $p_s = N_D$

$\simeq (V_R + 2\psi_B)$

V_R = reverse bias applied to the diode

$\psi_B = \frac{KT}{q} \cdot \ell n \frac{N_D}{n_i}$ = bulk Fermi potential

In the above analysis the assumption that the generation rate U is constant over all the space-charge layer was used, but Calzolari and Graffi (13) suggested that this is not true. They have shown that the active generating volume is the region bounded by the two points where the Quasi-Fermi levels cross the intrinsic Fermi level (Fig. 2.3). Thus U is only constant over a certain interval W_i and drops rapidly to negligible values outside this but W_i is by no means

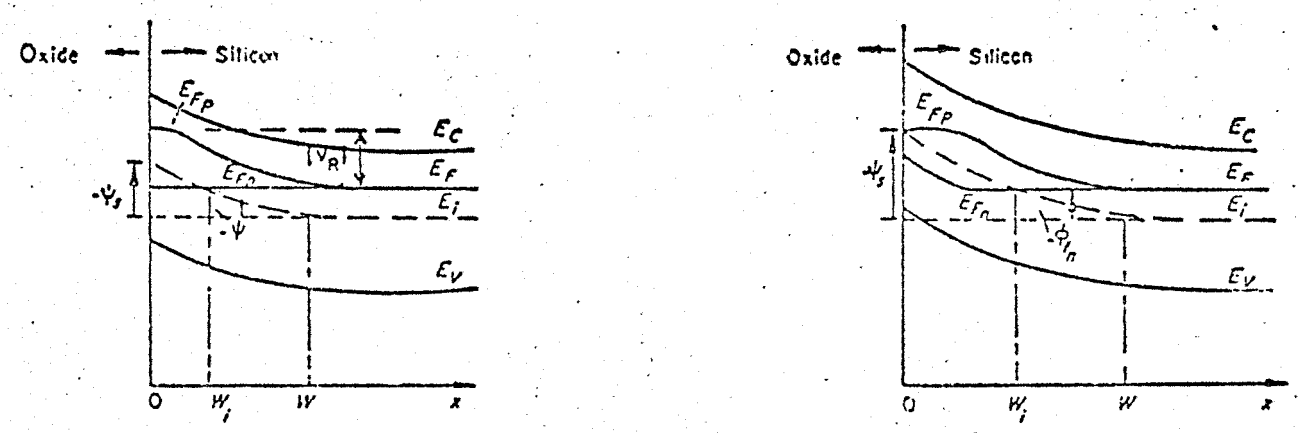


Fig. 2,3 Energy band diagrams showing active generation width W_i in relation to the depletion width W for the two cases,

(i) $|\psi_s| < |V_R| + |\phi_{fn}|$ and (ii) $|\psi_s| = |V_R| + |\phi_{fn}|$

(Roberts and Beynon[14])

equal to W. On the contrary, it remains much smaller than W up to voltages so high that the multiplication current is no longer negligible. Thus the generation current from the metallurgical junction becomes:

$$I_{gen,MJ} = \tfrac{1}{2}q \frac{n_i}{\tau_{oMJ}} W_i A_{MJ} = \tfrac{1}{2}q \frac{n_i}{\tau_{oMJ}} W\left(\frac{W_i}{W}\right) A_{MJ} \qquad 2a.13$$

where $\frac{W_i}{W}$ versus $\frac{qV_R}{KT}$ is shown in Fig. 2.4 (13).

Roberts and Beynon (14) used the same criterion as Calzolari for the field induced junction depletion region of the gated diode structure. The Field induced space-charge region closely resembles the structure of an abrupt p-n junction when the silicon immediately under the oxide is inverted.

In this case U_{FIJ} is constant over a width W_i that is less than x_{dmax} given by (14):

$$\frac{W_i}{x_{dmax}} = 1 - \frac{\phi_{Fn}}{\psi_s(inv)} = 1 - \frac{\phi_{Fn}}{|V_R| + |\phi_{Fn}|} \qquad 2a.14$$

Thus the $I_{gen,FIJ}$ at inversion becomes

$$I_{gen,FIJ} = \tfrac{1}{2}q \frac{n_i}{\tau_{oFIJ}} W_i A_s = \tfrac{1}{2}q \frac{n_i}{\tau_{oFIJ}} x_{dmax}\left(\frac{W_i}{x_{dmax}}\right) A_s \qquad 2a.15$$

In the above analysis the non-equilibrium MOS theory was employed in the study of recombination generation processes within the space-charge region of gate controlled p-n junction diodes. In particular it was shown that the surface recombination velocity S_o and the minority carrier lifetime in the surface space-charge region τ_{oFIJ} of an oxidized silicon surface can be determined by measuring the reverse bias current as a function of gate voltage.

In the next section of this chapter the fabrication of gated diodes using different processing is described, together with the measurement technique.

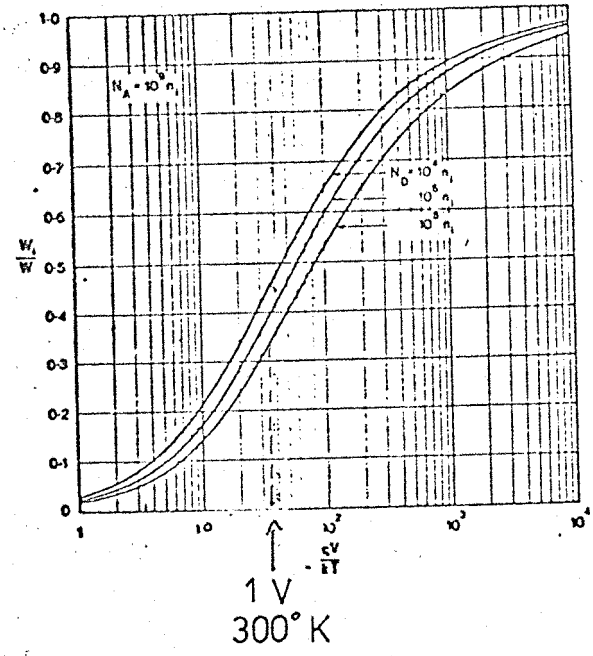

1·0
0·9
0·8
0·7
0·6
0·5
0·4
0·3
0·2
0·1
0
$\frac{W_i}{W}$
$N_A = 10^{18} n_i$
$N_D = 10^{18} n_i$
$10^{16} n_i$
$10^{14} n_i$
1
10
10^2
10^3
10^4
$\frac{qV}{kT}$
1 V
300° K

Fig. 2.4.

2b. Gated diode fabrication using HCl oxidation

The process for producing gate-controlled p^+n diodes that was used for the present work was chosen to be the same as the CCD fabrication schedule. The only difference between the gated diode structure and the CCD structure for the p-channel Alluminium-gate shadow-gap devices is the absence of the n^+ diffused guard ring. Three types of gated diodes were manufactured with a variation in the process described below

1. No gettering step apart from the HCl oxidation
2. A gettering step listed as stage 7 below performed before the HCl oxidation for the gate oxide.
3. A gettering step again listed as 7 below, performed without alteration of the complete process.

The complete process is described below with the omission of the n^+ phosphorus guard ring which is not necessary for the gated diode operation. This allowed a more rapid manufacture of the slices thereby permitting quicker evaluation and a large number of repeat processes for estimating the reliability of the data obtained. The material that was used was n-type (111) orientation with 3-6 Ω cm resistivity. The diameter of the whole slice is 2" and they were cut before processing in half since the furnace tubes in use at the time in the laboratory were only $1\frac{1}{2}$" diameter.

Gated diode process schedule:

1. Cleaning - The slices are boiled in a quartz beaker with concentrated HNO_3 (Analar grade) for 5 mins. Then a thorough wash in double distilled water (DDH_2O) followed by a 20 sec dip each in buffered HF (6:1 of NH_4F:HF) in a Teflon plastic beaker and again a thorough wash in DDH_2O. This is to degrease the slice and remove any particular residue from the surface. This is followed by another boil in concentrated HNO_3 for 15 mins in the quartz beaker followed in turn by a thorough wash in DD-H_2O. The slices are then spun dry on a PTFE coated plastic spinner. They are then presented to the furnace for the first heat treatment.
2. Initial Oxidation - The slices are put in the initial oxidation furnace at 1200°C for 50 mins at a flow rate of 1000cc/min in an ambient of oxygen bubbled through distilled H_2O which is maintained at 80°C. Then the oxygen flow is diverted from the bubbler giving a dry oxidation for a further 5 mins to prepare the slices for the first photomechanical stage.

3. Photomechanical stage - With this stage the diffusion windows are defined. After the photomech the slices are etched in buffered HF at room temperature and washed with H_2O. Then the resist is stripped off by washing the slices with $1H_2SO_4$:$1H_2O_2$ mixture. The slices then are thoroughly washed in DDH_2O and spun dry to prepare them for the next stage.

4. Boron deposition - The slices are put in the Boron deposition furnace at 960°C in a nitrogen ambient for 10 min. The sheet resistance of Boron diffusion was then 100 /D. This produces a shallow diffusion of Boron in the silicon from the doped glass on the surface. The slices are washed in DDH_2O and spun dry. Then the cleaned slices are put in the Boron drive in furnace at 1200°C in an ambient of dry O_2 for 40 min. The slices then are ready to be prepared for the reoxidation.

5. Oxide strip and re-oxidation - The oxide of the gate regions of the slices is stripped off with HF and cleaned. The slices are next put in the gate oxide double walled furnace at 1150°C for 30 mins in an ambient of O_2 in which a trace amount of HCl gas was added. Different volume ratios of HCl-gas were used. These ratios used were 0.5%, 1.5%, 3.7% and 6%. After the oxidation period the O_2 is switched off and nitrogen is switched on and the slices are pulled to the mouth of the furnace in the nitrogen ambient. The furnace is cooled down to 1050°C then the slices are again pushed into the furnace for 30 min. This is the high temperature annealing treatment in a nitrogen ambient which has been found to produce a minimum in the interface N_{ss} (Lamb Badcock, 20).

6. The slices are prepared for the gettering process for this resist is spun on the front of the slice, then they are exposed fully to UV, they are then baked for 5 mins at 150°C and then the oxide from the back of the slices is etched off. The slices then are cleaned with $1H_2SO_4$:$1H_2O_2$ mixture, washed with DDH_2O and spun dry.

7. Phosphorus gettering - The slices are put in the phosphorus gettering furnace at 1050°C for 10 min in an ambient of 1000 cc/min nitrogen plus 10cc/min O_2 and 200cc/min. N_2 bubbled through $POCl_3$ at melting-ice temperature. After 10 min the oxygen and $POCl_3$ vapor are switched off and the slices are exposed to a 1000 cc/min nitrogen ambient for a further 30 min at 1050°C. During this step the slices are supported on pimples to give an n^+ diffusion in back.

8. Photomechanical stage - With this photomech the contact windows in the slices are defined. Then the slices are etched, washed and spun dry.

9. Low temperature anneal - The slices are then put in the low temperature anneal furnace at 400°C for 40 min in an ambient of 60% H_2 and 40% N_2.

10. Metallization 1 - The slices then are put in a vacumn chamber which is pumped down to about 10^{-5} torr and Aluminium in a tungsten filament in evaporated onto the front of the slice to about 0.5μm. thickness.

11. Photomechanical stage - With this step the gate, p^+n contact and metal guard ring are defined. The rest of the Aluminium is then etched off.

12. Metallization II - This step is the same as no. 9 step except that the Aluminium is deposited on the back of the slice so as to ensure a good ohmic contact to the back of the wafer.

The processing steps are shown schematically in Fig. 2.5. It was mentioned earlier that three types of gated diodes were manufactured. For the first type, gated-diodes without gettering the no. 7 step is omitted from the process described above. For the second type, gated diodes with phosphorus gettering before oxidation, the no. 7 step comes before no. 5 step and no. 6 is omitted. For the last type the processing was as described above without alteration.

The three types of gated diodes are now tested as described in the next section of this chapter.

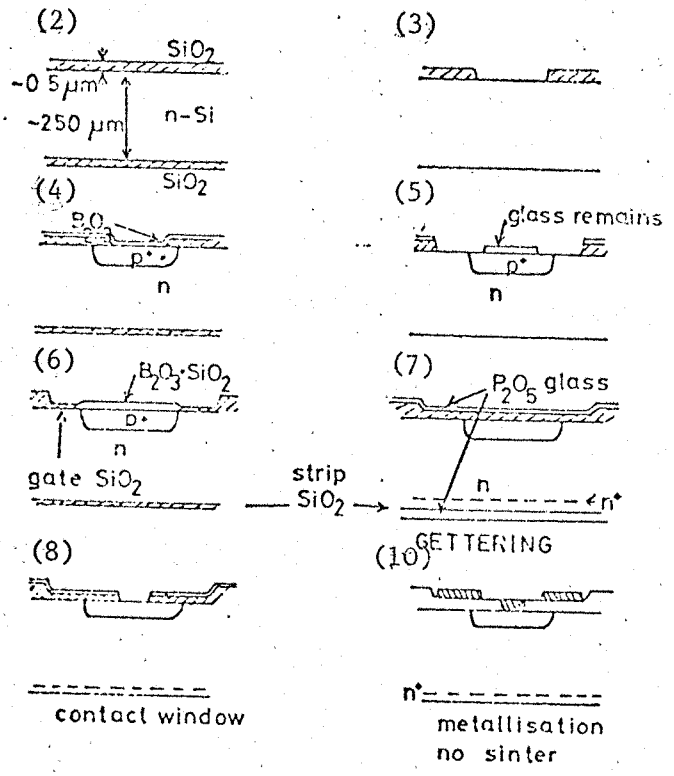


Fig. 2.5 Stages of process - type 3 with getter after oxidation.

2c. Leakage Current Measurements on HCl gate diodes.

The leakage currents that we have to measure are expected to be as low as 10^{-13} amps at -1V bias. So it is necessary for the environment of the devices to be at least one order of magnitude lower leakage. That is the parallel resistance due to the measuring jig must be in excess of 10^{14} Ωhms. It is convenient to probe directly on to the diode since defective devices can be quickly detected and there is no need to dice the slice into individual chips with possible damage.

A light tight metal box was therefore constructed with a metal platform supported at three points by PTFE pillars about 1" long and $\frac{1}{4}$" diameter. The area of the platform 6" x 8" is large enough to accommodate three PTFE insulated microphone assemblies. This gives a total of four probes with each probe of 5μm tip radius.

Bias inputs to the box internally are via self supporting coiled wires to each of the four probes and from the platform out via a PTFE loaded VHF plug and socket rigidly connected to the electrometer. This arrangement gives a total insulation of 5×10^{14} Ωhms at D.C. with about 10% to 30% relative humidity. To measure the currents a Kiethley instruments electrometer type 610C was used. This instrument incorporates a feedback loop in the current measuring circuit as shown in Fig. 2.6., which causes the input of the instrument to be a 'virtual earth' at a maximum of 100μV away from earth potential. The accuracy claimed by the manufacturer is 4% of full scale on 0.001×10^{-11} range with an input impedance of 10^{14}Ω shunted by 22pF without feedback. Drift after one hour warm up is less than 200 V/^{o}C in any hour which implies on the most sensitive current range a drift of less than 1×10^{-15} amps. The input offset of the 610C is 5×10^{-15} amps.

There is a recorder output from the instrument (0-3V, 1kΩ) with a noise of less than 3%RMS of full scale at maximum sensitivity.

The output was measured by a Hewllet Packard x-y recorder type 7035B which has a linearity of better than 0.1% of full scale with repeatability of better than 0.2% of full scale. The Kiethley output was displayed in y-axis and the x-axis used as a voltmeter to display gate volts.

The value of the anode volts measured by a Solartron Digital voltmeter type LM1420.2 to ±1 part in 9999.0. The lowest leakage devices measured had settline times of the order of a second or so

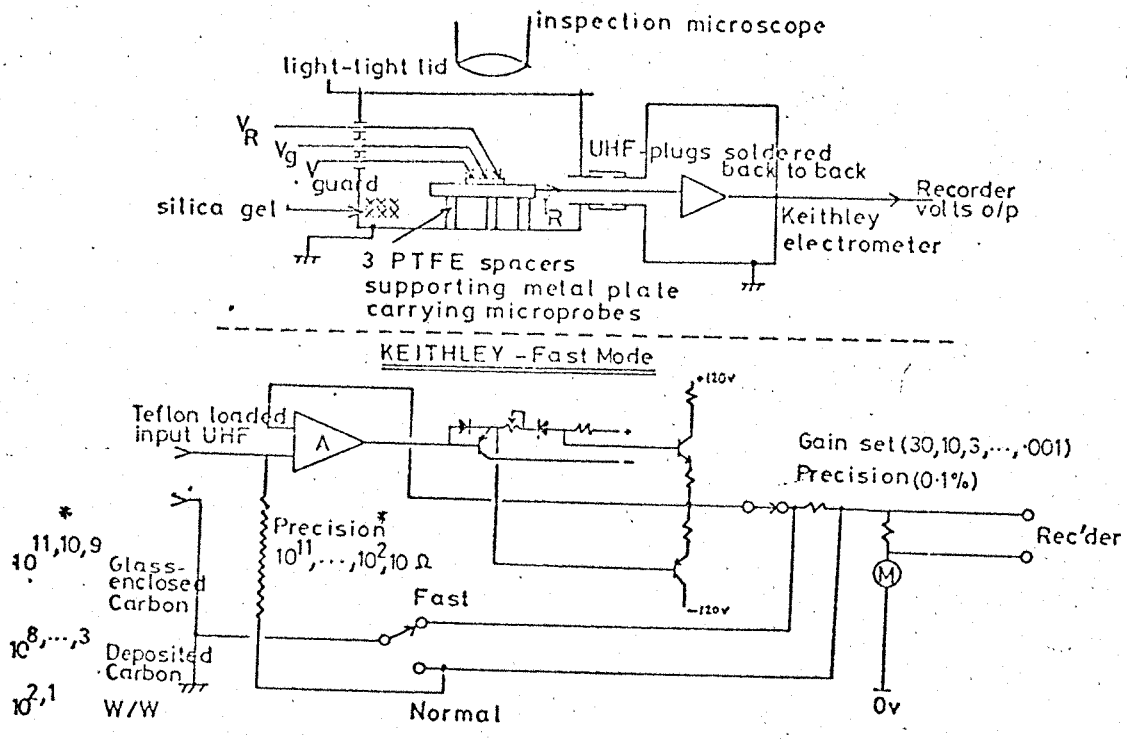

inspection microscope
light-tight lid
V_R
V_g
V_{guard}
silica gel
UHF-plugs soldered back to back
Recorder volts o/p
Keithley electrometer
3 PTFE spacers supporting metal plate carrying microprobes
KEITHLEY - Fast Mode
Teflon loaded input UHF
A
+120v
-120v
Gain set (30,10,3,...,·001)
Precision (0·1%)
Rec'der
Precision $10^{11},\ldots,10^{2}$ Ω
$10^{11,10,9}$
Glass-enclosed Carbon
$10^{8},\ldots,3$
Deposited Carbon
$10^{2,1}$
W/W
Fast
Normal
0v

Fig. 2.6

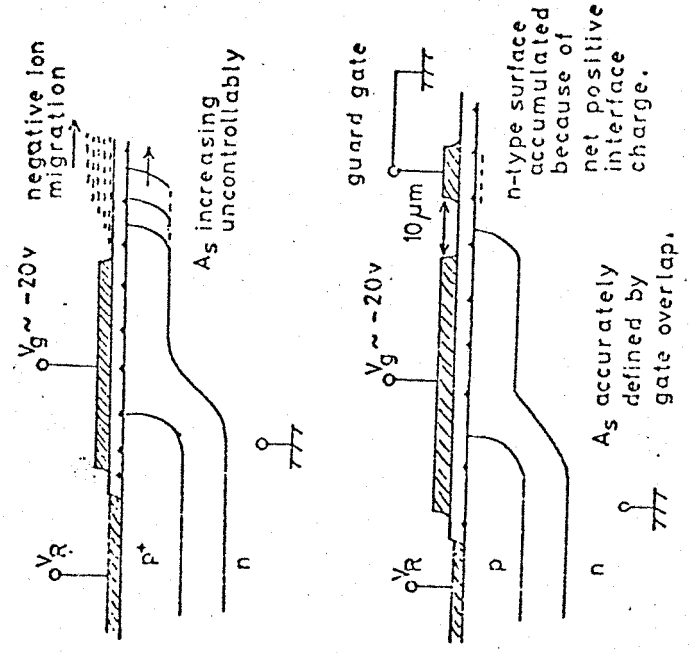
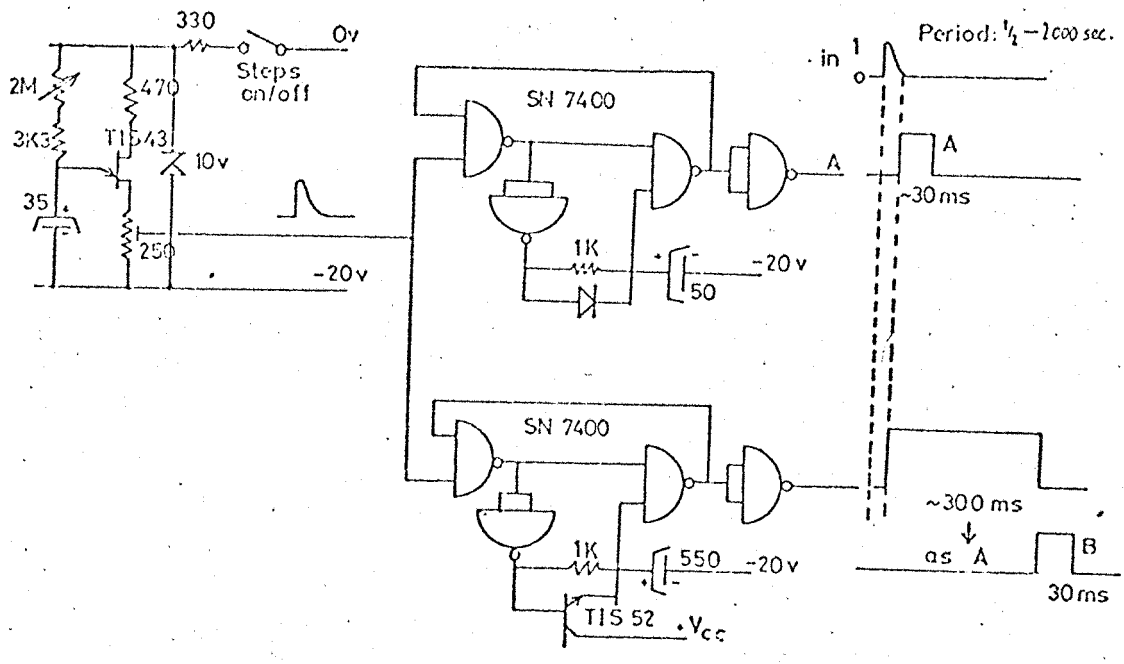
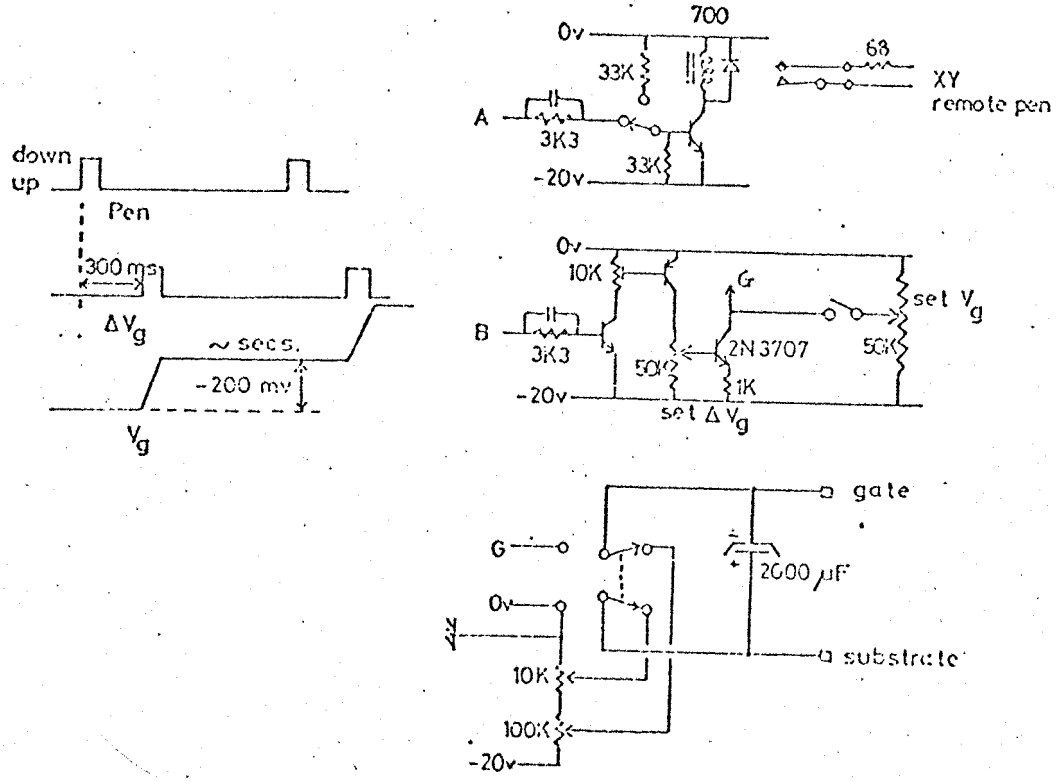

negative ion migration
$V_g \sim -20v$
A_S increasing uncontrollably
V_R
p^+
n
guard gate
10μm
n-type surface accumulated because of net positive interface charge.
$V_g \sim -20v$
A_S accurately defined by gate overlap.
V_R
p
n

Fig. 2.7



(a) Logic control cct



(b) Data-logging drives

Fig. 2.8

because of the gate capacitance - leakage resistance time constant.

It was found difficult to make measurements by 'hand' and so a semi-automatic control box was used (15) (Fig. 2.8). With this control box the pen of the x-y recorder is brought down only after an interval of say 4 seconds has elapsed since the gate voltage was last stepped. This method enables rapid measurements of transfer characteristics (I_R, V_G at constant V_R) without incurring capacitive current component.

Using the apparatus described above transfer characteristics similar to those shown in Fig. 2.9 were obtained.

In the Fig. 2.9 transfer characteristics of several devices have been plotted on the same axis to enable an estimate of the spread of values of leakage currents in the three regions. The devices were chosen from a single line of the array of the devices selecting only those which did not exhibit gross defects such as leaking gate to substrate poor diffusion leakage or short circuits gate to diffusion. This procedure permitted a reasonable estimate to be made with a minimum of devices measured.

From these transfer characteristics the values for I_{MJ}, I_{FIJ}, I_s were obtained. The value of I_{MJ} current is the leakage current in the accumulation regime which is a direct measurement. The value of I_{FIJ} current is the value obtained by substracting the value I_{MJ} from the leakage current in the inversion regime. And finally the surface current I_s is obtained by estimating first of all the value of bulk current in the depletion regime, using a straight line approximation. The straight line joins the leakage current at the up-turn of the transfer characteristic to the leakage current at the bottom part of the down-turn of the transfer characteristic. This value of bulk current is substracted from the leakage current in the depletion regime of the transfer characteristic to give the value of surface leakage current I_s. The values thus obtained are averaged and a value of standard deviation was calculated using the formula:

$$S_x = \frac{\Sigma x^2 - \frac{(\Sigma x)^2}{n}}{n - 1}$$

The average values of current densities are shown plotted in Figs. 2.10 through 2.18, with the standard deviation shown by an error bar, as a function of HCl percentage by volume for the three

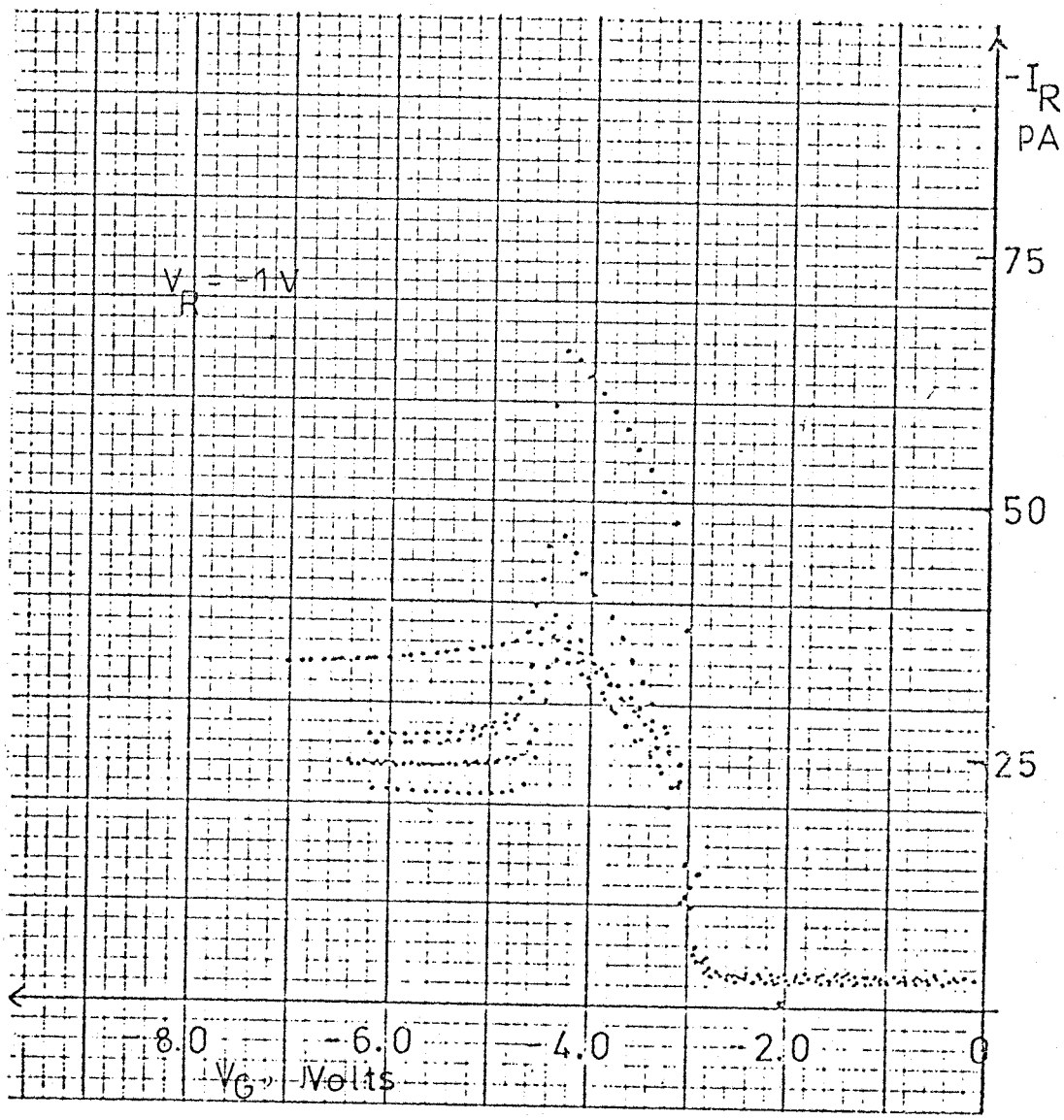


Fig. 2.9

processing types.

Fig. 2.10 shows I_{MJ} current density obtained by measuring a 200μm diffusion diameter diode and dividing the value of the leakage current by the diffusion cross sectional area A_{MJ} ignoring any side-wall components. The area A_{MJ} for the devices that we measure here is equal to $3.0 \times 10^{-4} cm^2 \pm 5\%$. The processing conditions were type 1 where no phosphorous gettering treatment is purposely introduced. No devices of this type were manufactured with 0% HCl since previous work (16) has shown that in general much higher leakage currents are obtained when no gettering is included.

As can be seen from the Fig. 2.10 there is no definite trend of I_{MJ} with changes in HCl concentration for this process.

The values of lifetime are shown on the same graph and have been calculated using the relationship:

$$\tau_{oMJ} = q \frac{n_i}{2J_{MJ}} W_i \qquad 2c.1$$

Where q is the electronic charge and equal to 1.6×10^{-19} coulomb n_i the intrinsic concentration and is equal 1.45×10^{10} cm^{-3} and W_i the depletion width which is equal to

$$\left(\frac{W_i}{W}\right) W = (0.45) \times 1.5\ 10^{-4} cm = 0.675 \times 10^{-4} cm$$

Fig. 2.11 shows the J_{FIJ} current density obtained by measuring the same 200μm diffusion diameter diode as before and taking the difference in leakage current as explained above and dividing by the value of the gate area A_s. In the devices that were used here for the whole work a second 'guard' gate electrode separated by 10μm from the 'active' gate was incorporated to enable the gate area A_s to be clearly defined by biasing the 'guard' gate so as to accumulate the semiconductor surface under this electrode as shown in Fig. 2.7. The device is photographed and the area A_s is calculated by measuring the diameter. It is found that A_s is

$$\frac{\pi(d_1^2 - d_2^2)}{4}$$ and is equal to $8.65 \times 10^{-4} cm^2 \pm 5\%$

Again it can be seen that there is no definite trend of J_{FIJ} with changes in HCl concentration. The values of lifetime τ_{oFIJ} are shown in the same graph and have been calculating using the relationship.

$$\tau_{oFIJ} = q \frac{n_i}{2J_{FIJ}} W_i' \qquad 2c.2$$

where W_i' is equal to $\left(\frac{W_i'}{x_{dmax}}\right) x_{dmax} = (0.51) \times 1.43\ 10^{-4}\text{cm} = 0.78\ 10^{-4}\text{cm}$

Fig. 2.12 shows the J_s current density obtained again by measuring the same 200μm diffusion diode as before and dividing the I_s leakage current (which is obtained as explained above) by the same gate area A_s as before. Again it can be seen that there is no definited trend of I_s with changes in HCl concentration.

The values of surface recombination velocity are shown in the same graph and have been calculated using the relationship:

$$S_o = \frac{2J_s}{qn_i} \qquad 2c.3$$

The graphs in the Fig. 2.13, 2.14, 2.15 show the analogous current densities, lifetimes and surface recombination velocities but for devices which were type 2, that is with phosphorous gettering before HCl oxidation. The rest of the graphs in Fig. 2.16, 2.17, 2.18 were obtained from measuring type 3 devices that is with phosphorous gettering after HCl oxidation.

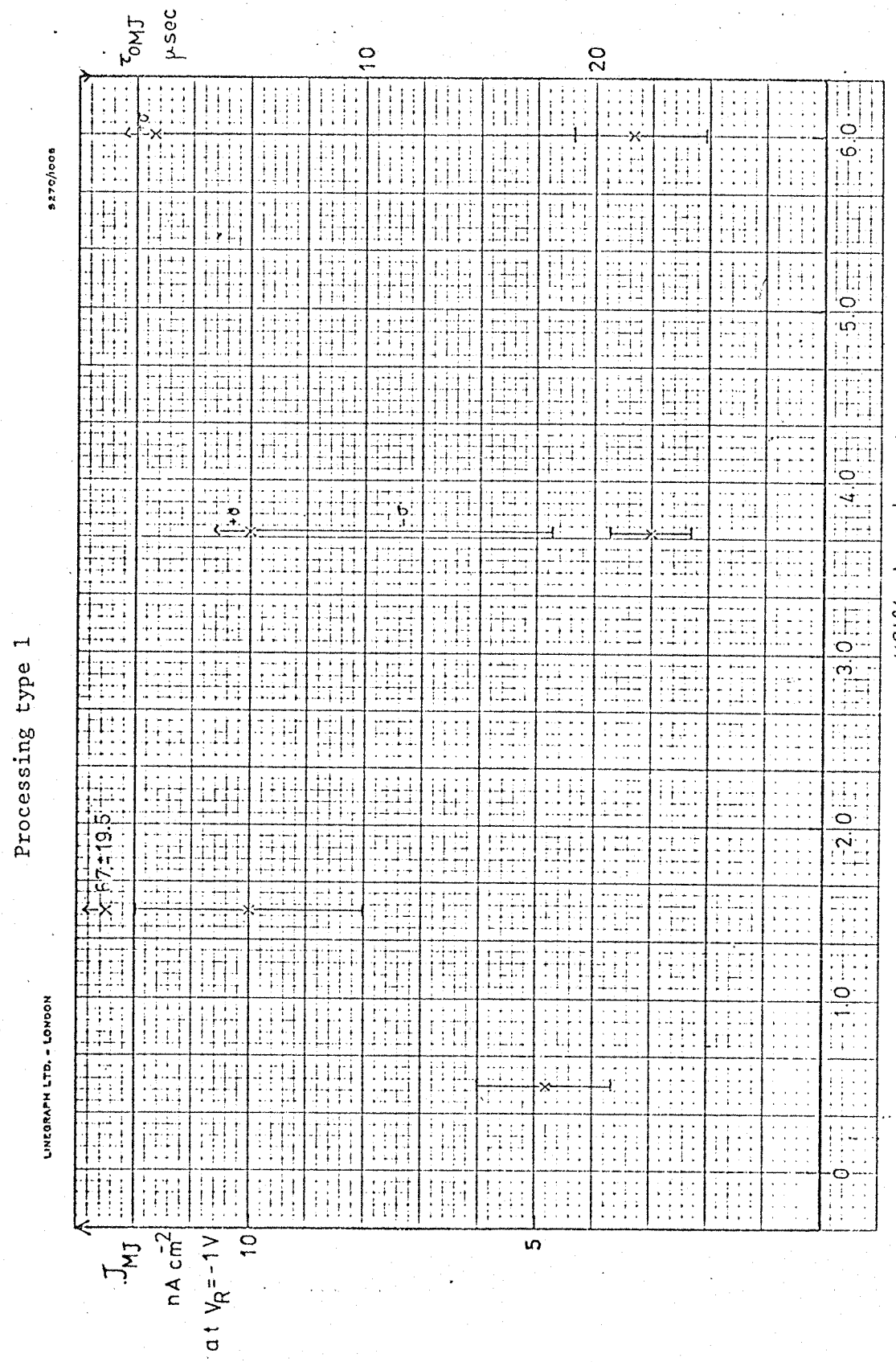

Processing type 1
LINEGRAPH LTD. - LONDON
5270/1008
τ_{OMJ} μsec
10
20
J_{MJ} nA cm^{-2} at V_R = -1V
10
5
67±19.5
+σ
-σ
HCl% by volume
0
1.0
2.0
3.0
4.0
5.0
6.0

Fig. 2.10

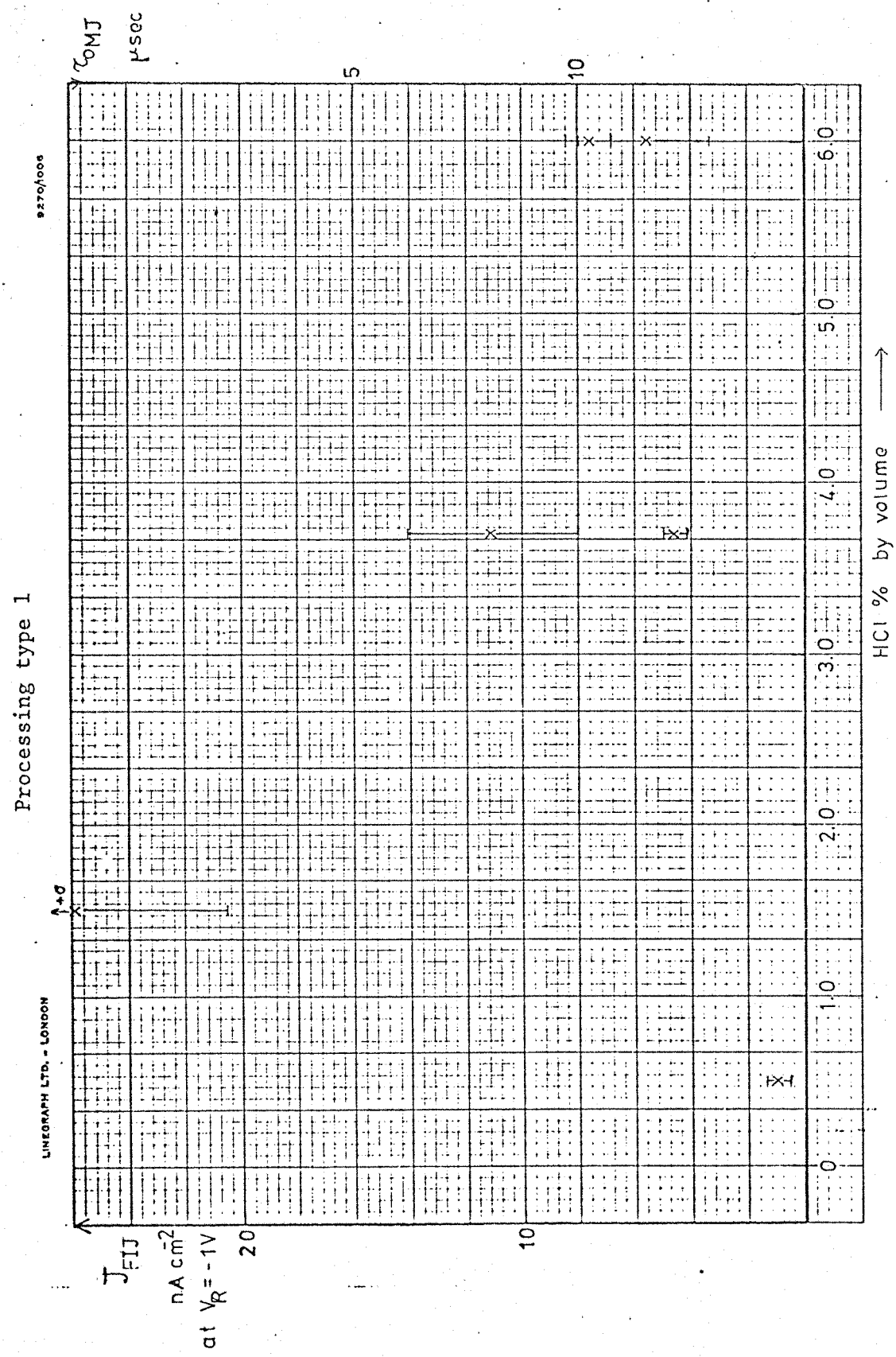

Processing type 1
τ_{OMJ} μsec
5
10
6.0
5.0
4.0
3.0
2.0
1.0
0
HCl % by volume ⟶
J_{FIJ} nA cm^{-2} at V_R = -1V
20
10
±σ
LINEGRAPH LTD. - LONDON
9270/008

Fig. 2.11

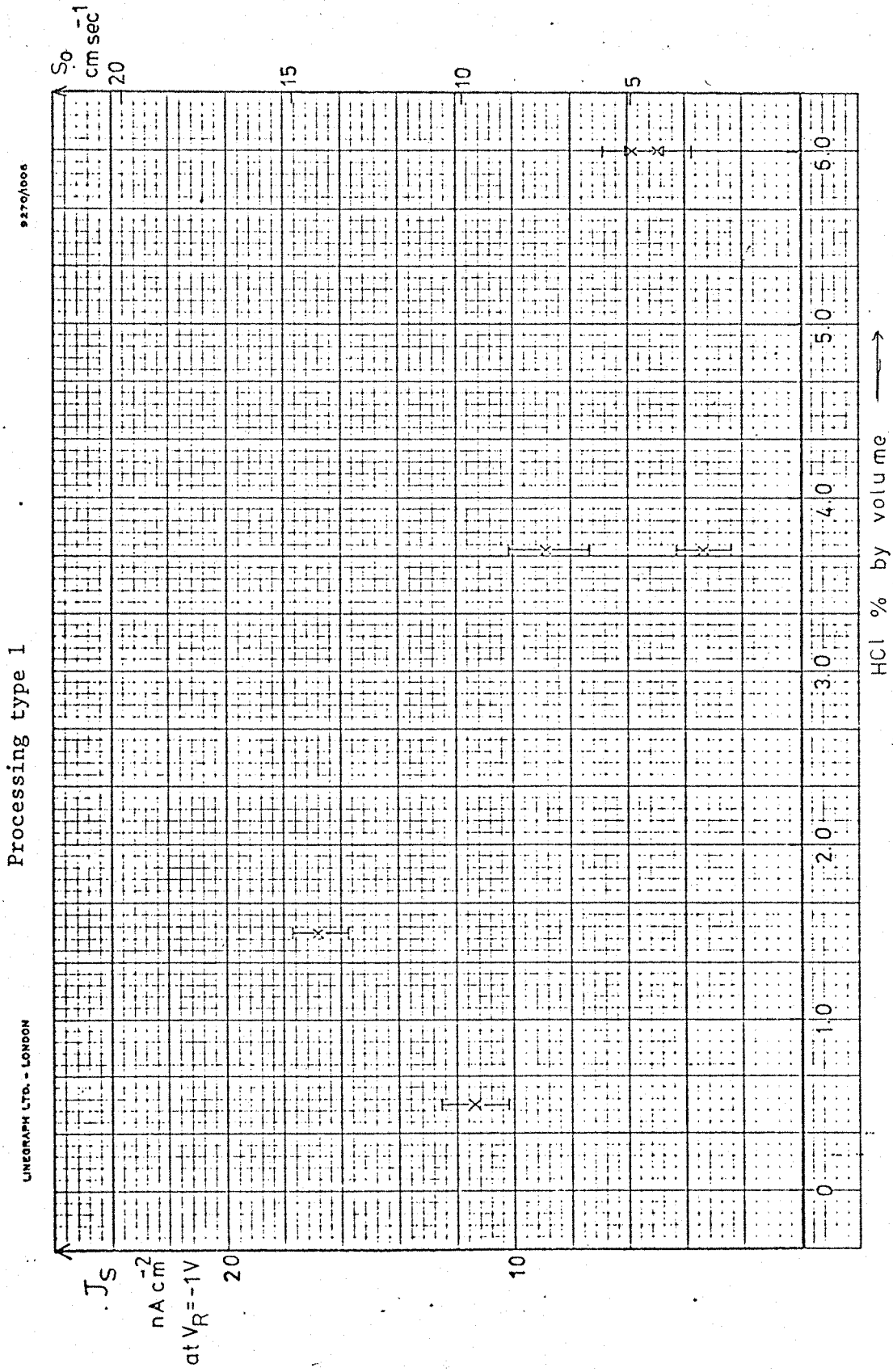

Processing type 1
LINEGRAPH LTD. - LONDON
9270/1006
S_o cm sec^{-1}
20
15
10
5
J_S nA cm^{-2} at V_R = -1V
20
10
0
1.0
2.0
3.0
4.0
5.0
6.0
HCl % by volume

Fig. 2.12

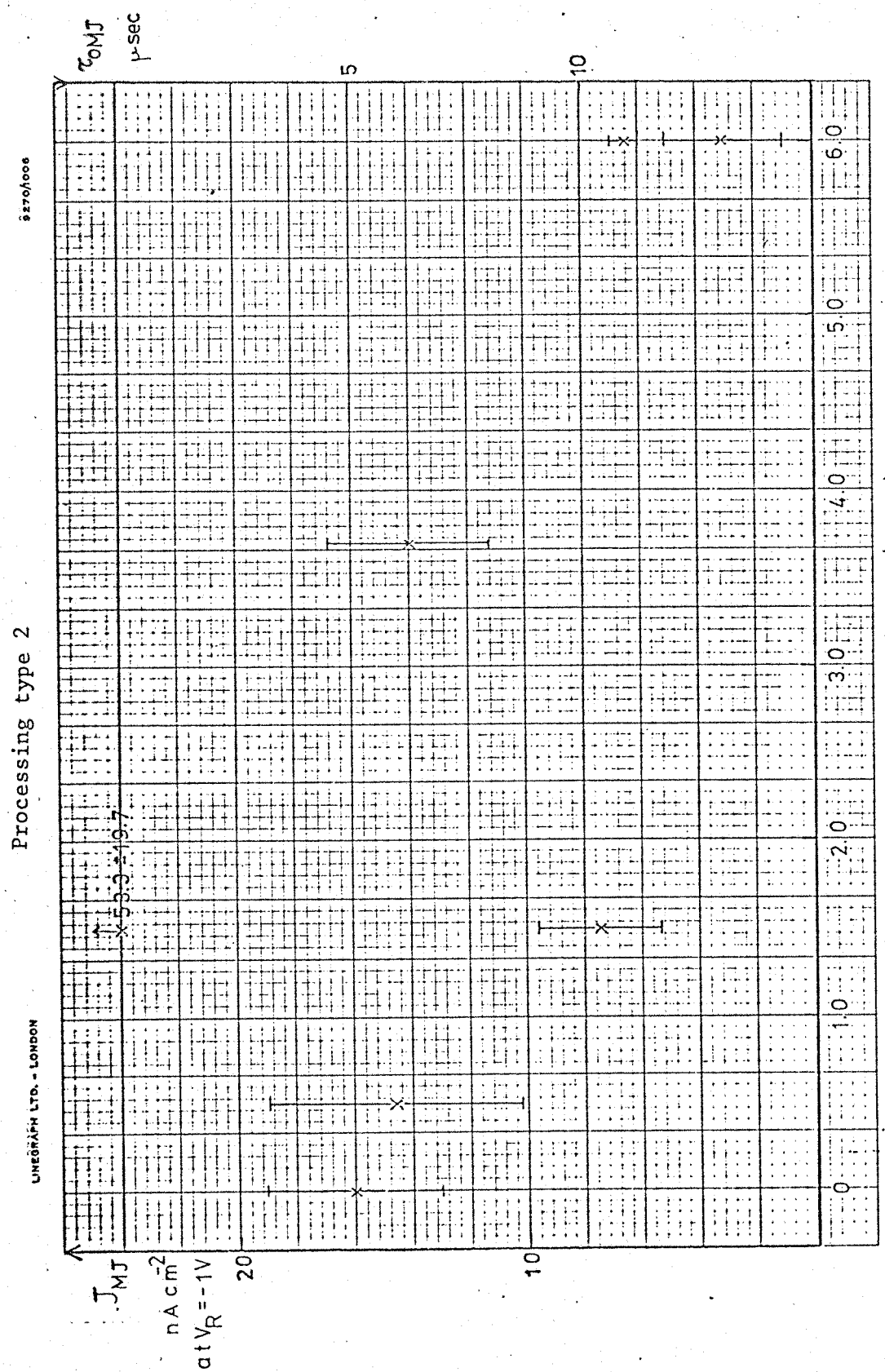

Processing type 2
τ_{OMJ} μsec
J_{MJ} nA cm^{-2} at V_R = -1V
HCl % by volume
LINEGRAPH LTD. - LONDON
5
10
20
0
1.0
2.0
3.0
4.0
5.0
6.0

Fig. 2.13

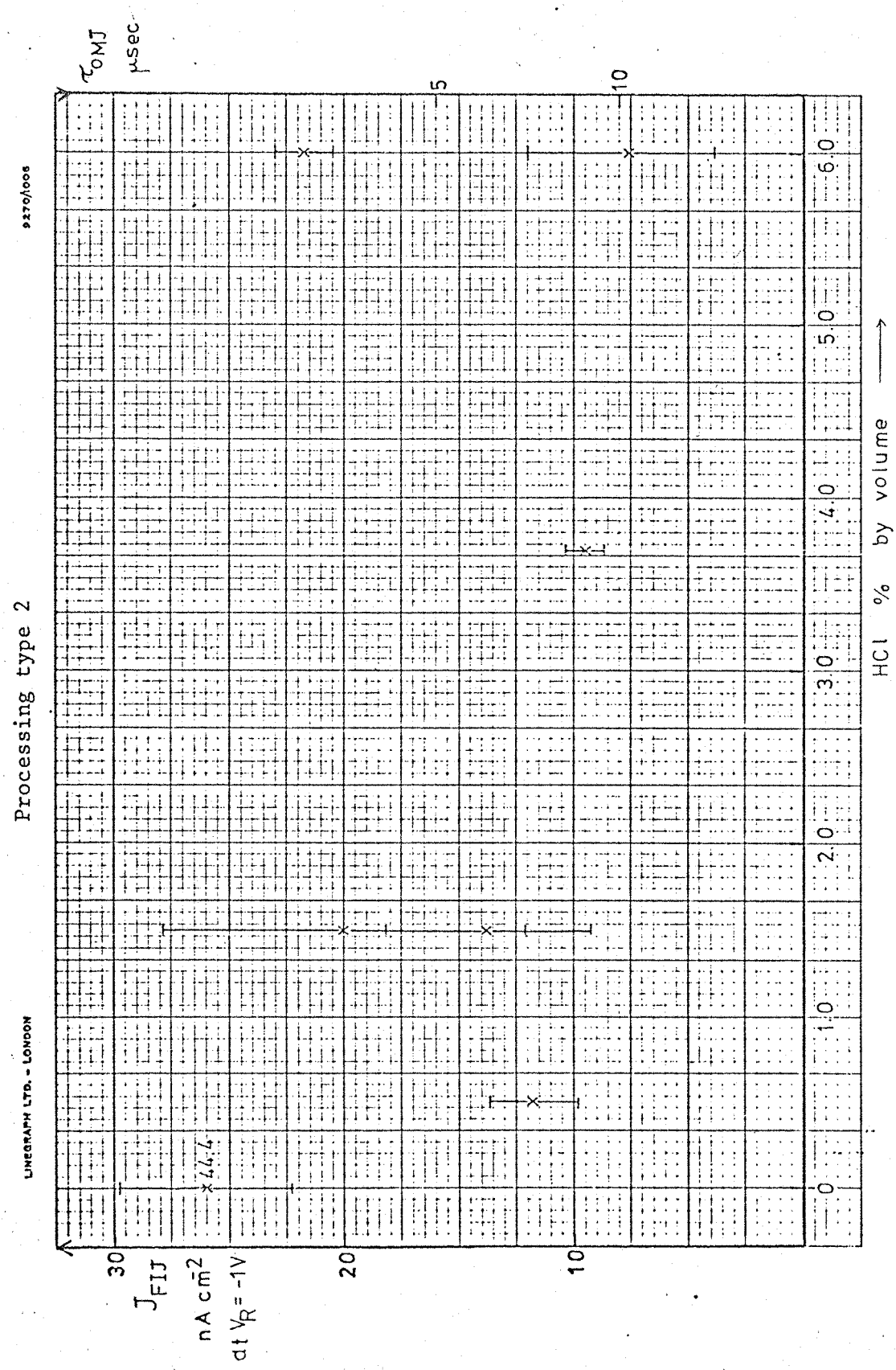

Processing type 2
9270/1008
LINEGRAPH LTD. - LONDON
τ_{OMJ} μsec
5
10
J_{FIJ} nA cm^{-2} at V_R = -1V
30
20
10
444
0
1.0
2.0
3.0
4.0
5.0
6.0
HCl % by volume

Fig. 2.14

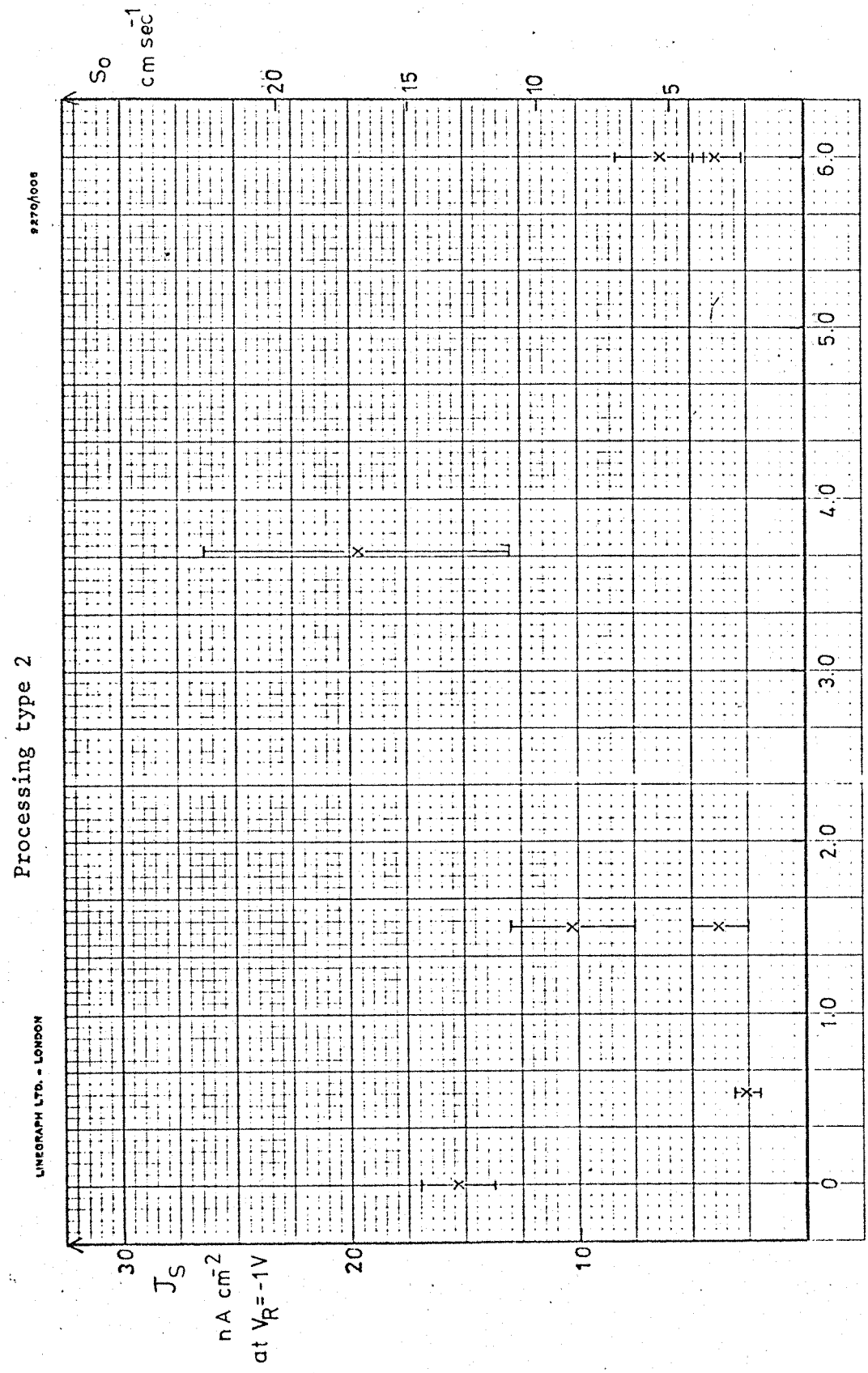

Processing type 2
LINEGRAPH LTD. - LONDON
9270/1008
S_o cm sec^{-1}
20
15
10
5
J_S nA cm^{-2} at V_R=-1V
30
20
10
0
1.0
2.0
3.0
4.0
5.0
6.0
HCl % by volume

Fig. 2.15

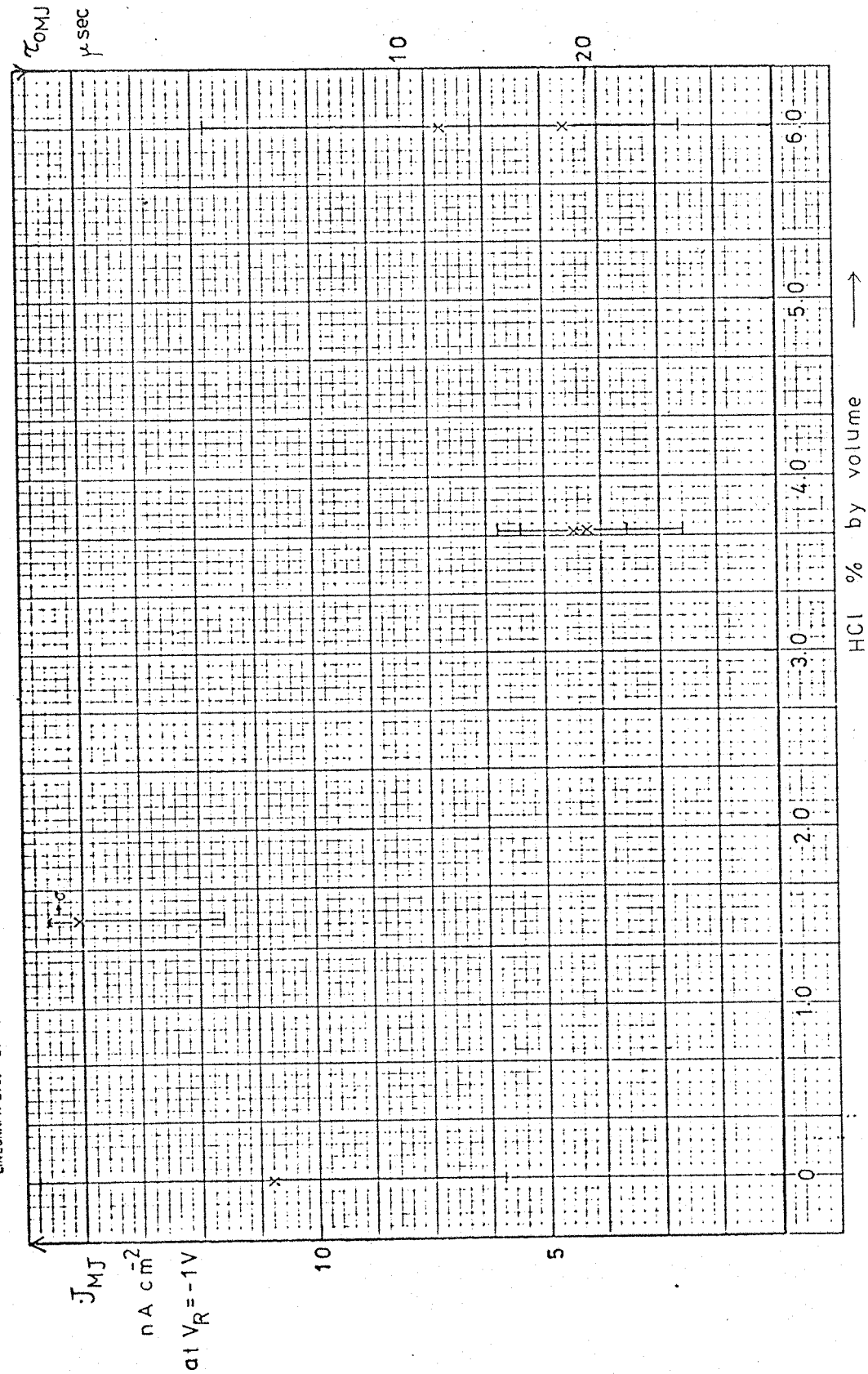

τ_{OMJ} μsec
10
20
J_{MJ} nA cm^{-2} at V_R = -1V
10
5
0
1.0
2.0
3.0
4.0
5.0
6.0
HCl % by volume
Processing type 3
9270/1008
LINEGRAPH LTD. - LONDON

Fig. 2.16

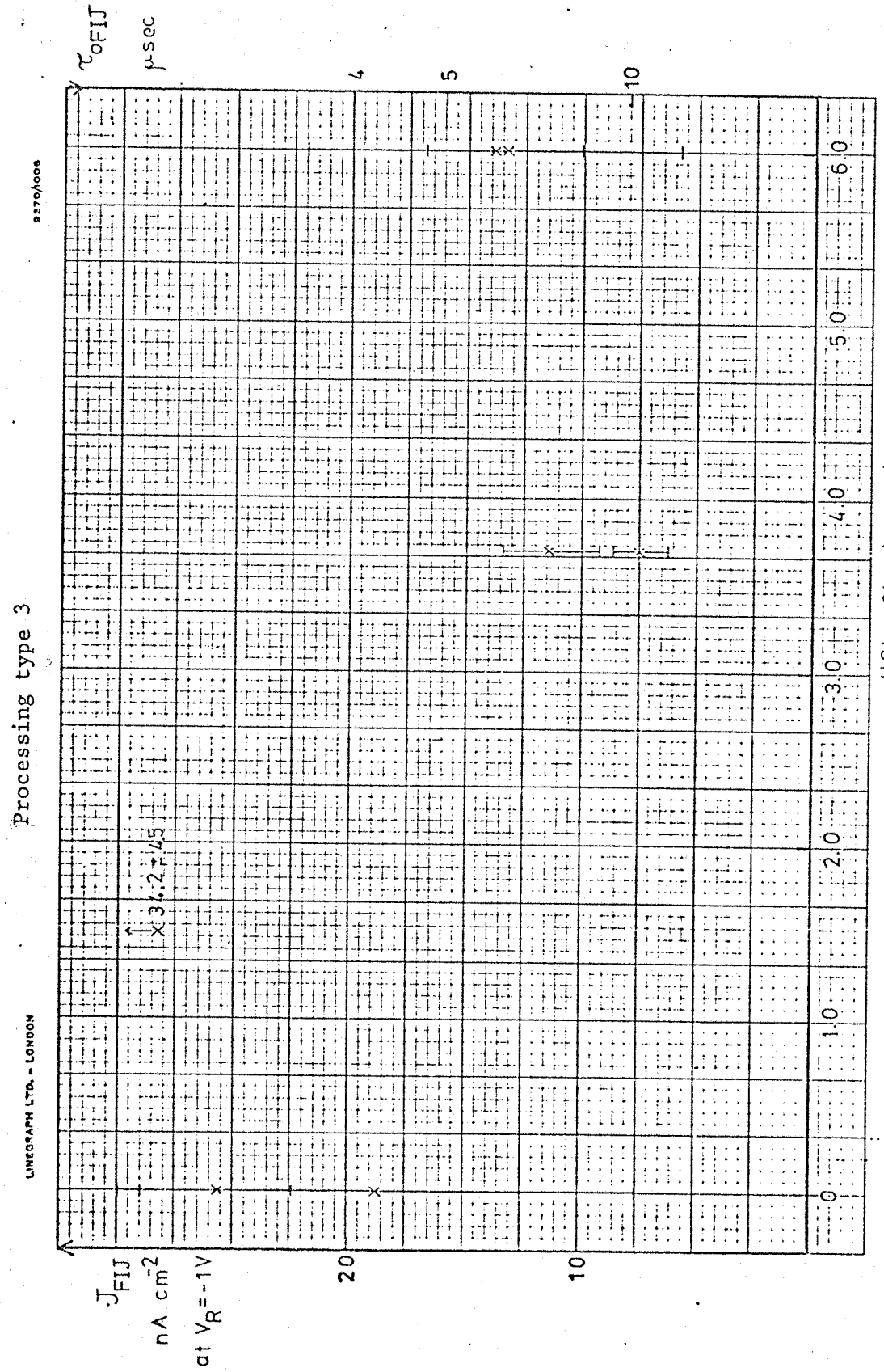

Processing type 3
LINEGRAPH LTD. - LONDON
τ_{OFIJ} μsec
J_{FIJ} nA cm^{-2} at V_R = -1V
HCl % by volume
34.2 ± 4.5
0
1.0
2.0
3.0
4.0
5.0
6.0
4
5
10
20
10

Fig. 2.17

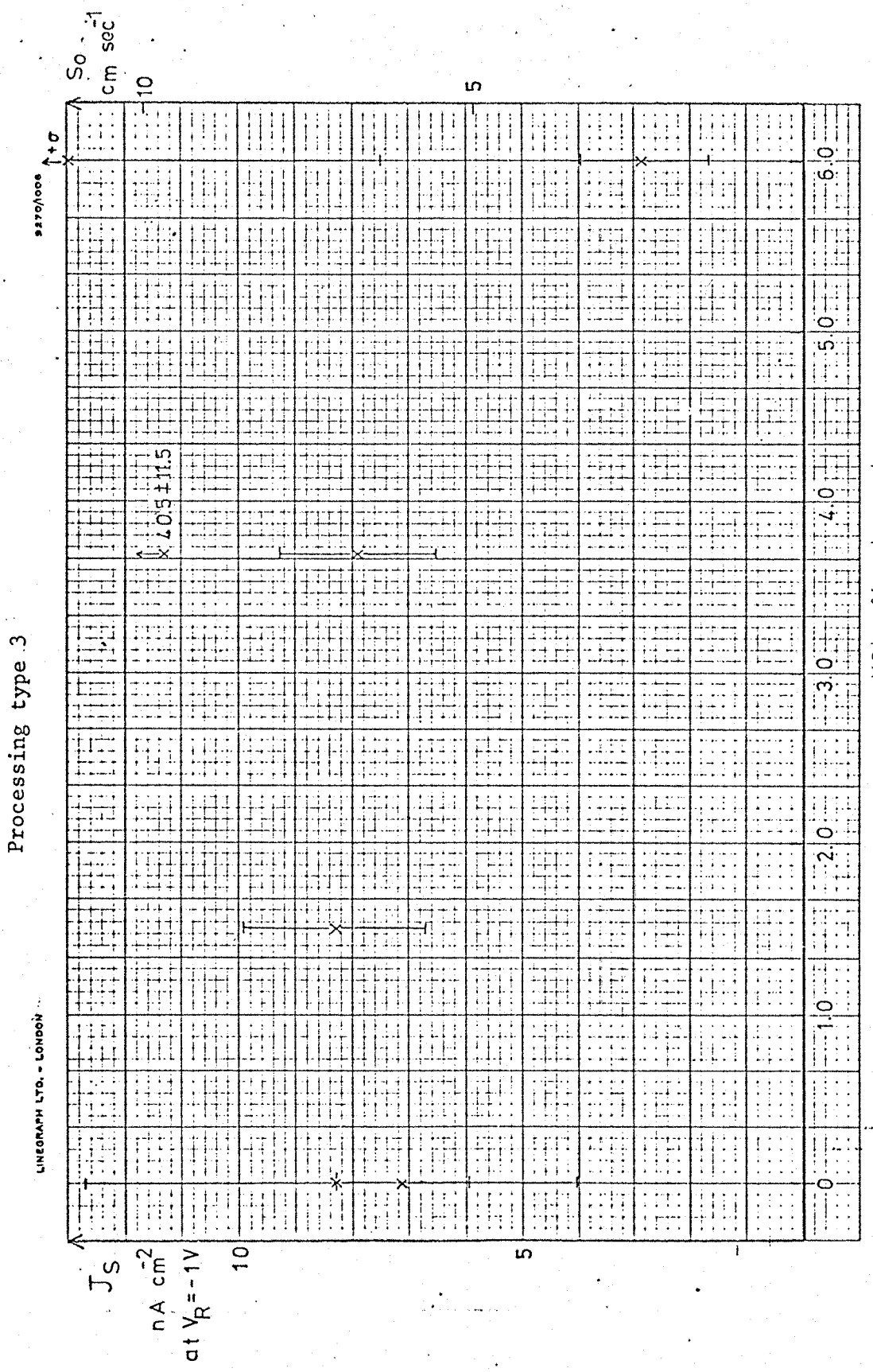

Processing type 3
S_o - $cm\ sec^{-1}$
10
5
+σ
5270/1008
405 ± 11.5
J_S
$nA\ cm^{-2}$
at $V_R = -1V$
10
5
1
0
1.0
2.0
3.0
4.0
5.0
6.0
HCl % by volume
LINEGRAPH LTD. - LONDON

Fig. 2.18

2d Leakage Current Measurements on CCD's

Leakage current measurements were made in a 134, 8-bit, three-phase, aluminium gate, CCD (sample 1) fabricated on a (111) orientation substrate, (p-channel) which was manufactured at the Microelectronics Lab. at the University of Southampton. The measurement technique applied was the same as described in section 2c for gated diodes. These measurements were made on the input circuit that is the input diode and input gate of the CCD. The photograph of this CCD is shown in Fig. 2.19. In Fig. 2.20 both the forward bias and reverse bias transfer characteristics are shown. The diffusion area A_{MJ} was measured from the photograph of the Fig. 2.19 and is equal to $0.47\times10^{-4}cm^2$. The gate area A_s was also measured and is equal to $0.18\times10^{-4}cm^2$. From the reverse bias transfer characteristic in Fig. 2.20 the metallurgical junction current I_{MJ} was measured and it was found to be equal to 3.2pA. Also the field induced current I_{FIJ} and surface generation current I_s were measured from this curve as was explained in section 2c of this chapter and were found to be 4pA and 0.4pA respectively.

Thus using equation 2a.9 we have for the metallurgical junction a lifetime,

$$\tau_{oMJ} = \tfrac{1}{2}q \frac{n_i}{I_{MJ}} W_i A_{MJ} \qquad 2d.1$$

From this equation for $n_i = 1.45\times10^{10} cm^{-3}$, $W_i = 0.675\times10^{-4}$cm, $A_{MJ} = 0.47\times10^{-4}cm^2$ and $I_{MJ} = 3.2$pA we have a value,

$$\tau_{oMJ} = 1.15\mu sec$$

For the field induced junction we have a current,

$$I_{FIJ} = \tfrac{1}{2}q \frac{n_i}{\tau_{oFIJ}} W_i' A_s ,$$

or a lifetime,

$$\tau_{oFIJ} = \tfrac{1}{2}q \frac{n_i}{I_{FIJ}} W_i' A_s .$$

For $W_i' = 0.78\times10^{-4}$cm, $A_s = 0.18\times10^{-4}cm^2$ and $I_{FIJ} = 4\times10^{-12}$A, we have a value.

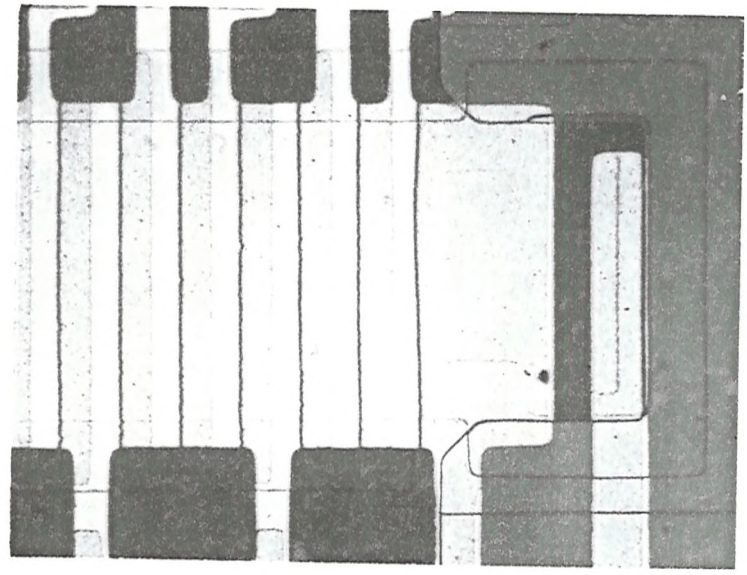


Fig. 2.19 Input structure of a 134 DRL MPS CCD. The channel width is 100μm, the phase gate length is 20μm.

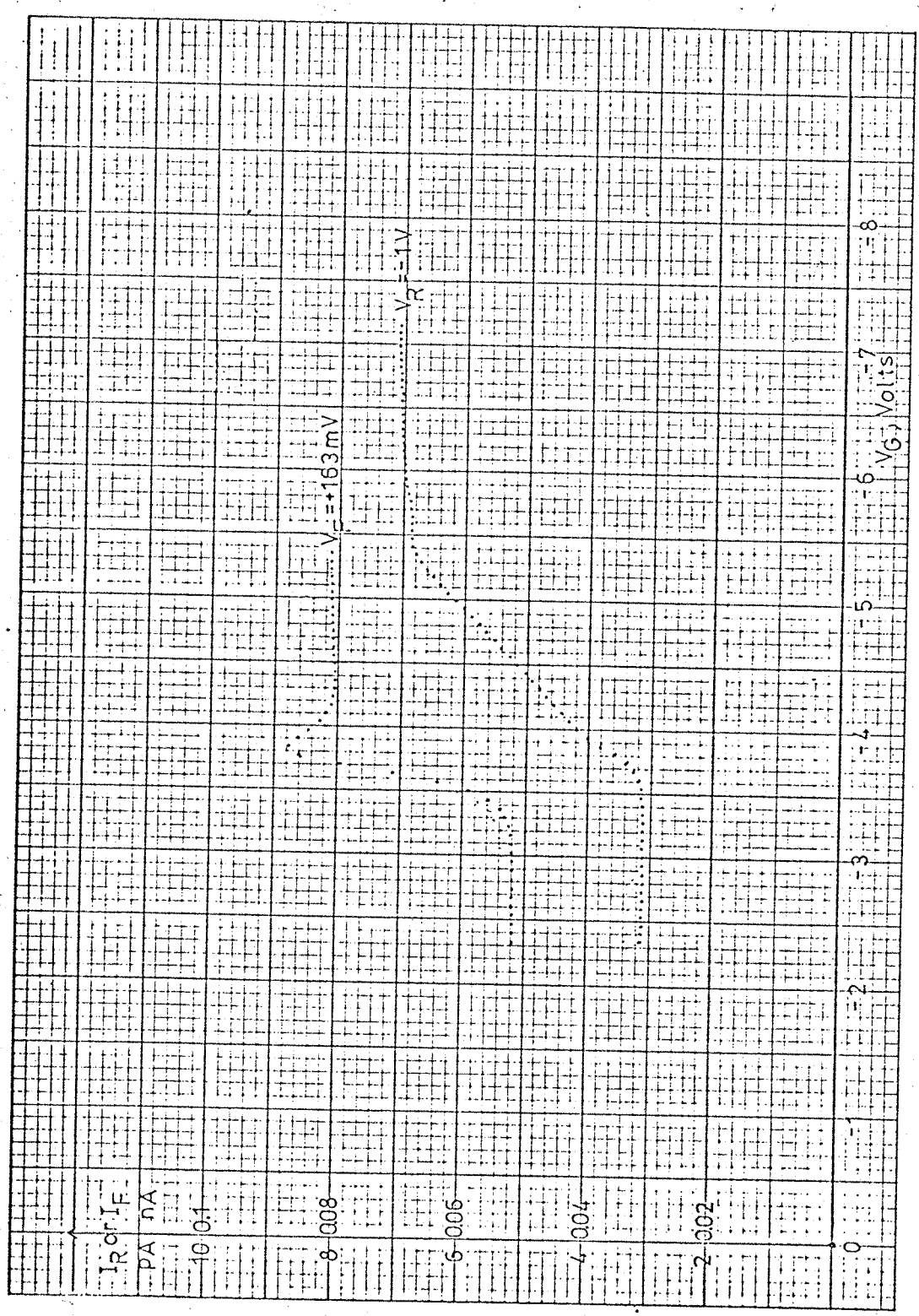

I_R or I_F
pA nA
10 0.1
8 008
6 006
4 004
2 002
0
-1 -2 -3 -4 -5 -6 -7 -8
V_G Volts
V_F = +163 mV
V_R = -1V
LINEGRAPH LTD. - LONDON
9270/1006

Fig. 2.20

$\tau_{oFIJ} = 380\times10^{-9}$ sec = 380nsec

For the surface area in depletion we have a current,

$$I_s = \tfrac{1}{2} q n_i S_o A_s$$

or a recombination velocity

$$S_o = \frac{2I_s}{q n_i A_s} = 19 \text{ cm/sec}$$

This particular device was also measured in the 'Interrupted Clock' mode using three-level clock voltages (21). The voltages on the gates were $\phi_1 = -5V$, $\phi_2 = -.25V$ and $\phi_3 = -15V$ for integration times up to 18ms at room temperature. The results over a range of integration times, from about 8msec to 18msec, shows a straight line of collected charge versus integration time as in Fig. 2.21. From the slope of this line the total generation current I_{gen} can be obtained. Two limiting cases for the partitioning of this current can be assumed. Firstly, it can be assumed that the current is exclusively from the depleted surface under the two phase gates adjacent to the storage gate. With this assumption the value of surface recombination velocity can be obtained using eq. 2a.7 as follows:

$$S_o = \frac{2I_{gen}}{q n_i 2A_s} = \frac{2 \times 85\ 10^{-12} A}{1.6\times10^{-19} C\ 1.45\times10^{10} cm^{-3} 2x0.2\ 10^{-4} cm^2}$$

$$= 1831 \text{ cm/sec}$$

where A_s is the area of each of the non-storage gates.

Alternatively, it can be assumed that the bulk current dominates the total response and furthermore that the depletion regions do not reduce significantly during the integration period. With an estimated value of $V_{FB} = -3.5V$ from the input circuit measurements, the surface potential ψ_s under each gate region can be calculated using eq. 3b.23. From these values of ψ_s the depletion widths x_d can be calculated using eq. 2a.12 as well as the fraction of the depletion width $\frac{W_i'}{x_d}$ under the three gates using eq. 2a.14.

The average value of τ_{oFIJ} can be calculated as follows:

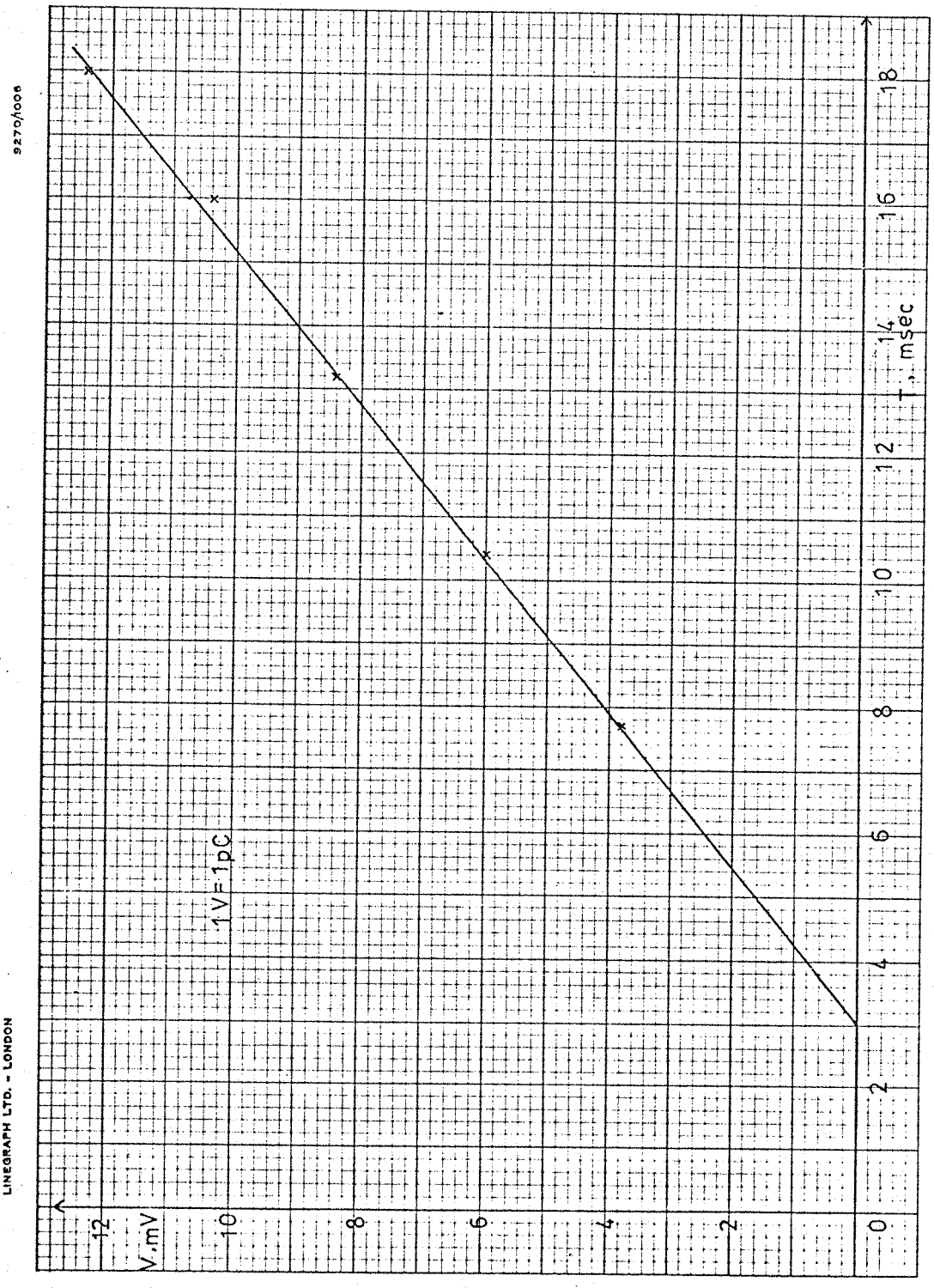

9270/1006
LINEGRAPH LTD. - LONDON
V, mV
1 V=1pC
T, msec
0
2
4
6
8
10
12
14
16
18

Fig. 2.21

$$\overline{\tau}_{oFIJ} = \tfrac{1}{2} \frac{qn_i}{I_{gen}} \left[x_{d1}\left(\frac{W_{i1}'}{x_{d1}}\right) + x_{d2}\left(\frac{W_{i2}'}{x_{d2}}\right) + x_{d3}\left(\frac{W_{i3}'}{x_{d3}}\right) \right] A_s$$

$$= 183\text{nsec}$$

Comparing this average value of τ_{oFIJ} with the value obtained from the input circuit measurements it can be seen that there is only about a factor of 2 discrepancy. The value from the 'Interrupted Clock' CCD measurements is an average over the whole device where we have assumed a uniform distribution of bulk leakage current and a uniform value of Flat-band voltage. Under these assumptions the comparison is reasonably close.

However, the values of surface recombination velocity S_o do not agree at all. The conclusion is therefore that the leakage current is bulk current almost exclusively.

Thus it seems reasonable to use the input structure of the CCD for making gated diode measurements and using the values of τ_{oFIJ} and S_o for the whole structure in small CCD's. This will not be true for CCD's with a large number of bits because of random variations in generation rate in large structures. For these structures we may predict the leakage current to a reasonable degree of precision using the values τ_{oFIJ} and S_o measured from the input structure.

3. CHARGE PUMPED CURRENT INVESTIGATION

3a Charge Pumping Method

This method was first developed by Brugler and Jespers (7), and it is useful in obtaining a quick estimation of the total surface state density from a complete device. They show that repetitive gate pulses of magnitude sufficient to turn-on, (ie. to change the conductivity type of the surface under the gate), an MOS transistor, can stimulate a net flow of majority carriers from the source and drain to the substrate via the interface states. In the following description of the charge pumping phenomenon a gate-controlled diode as was described earlier is considered, with n-type substrate. The set up is shown schematically in Fig. 3.1. For simplicity the p-type region is assumed to be much more heavily doped than the substrate. The junction is reverse biased with an applied voltage V_R (non-equilibrium condition). The gate is connected to the pulse generator with respect to the substrate. In the absence of any gate pulse the silicon surface would be in accumulation and the ammeter simply indicates the junction negative reverse leakage current.

If a pulse is applied to the gate such that $V_G < V_T(V_R)$ where $V_T(V_R)$ is the turn-on voltage, then the surface is only depleted. In this case the band bending is insufficient to bring the conduction band near enough to the quasi-Fermi level for holes (minority carriers) to cause inversion, and the diode is not switched on so the current that the ammeter registers is very small, being only the leakage current.

If the pulse applied to the gate is such that $V_G > V_T$ then the diode is switched on and holes from the p^+ region flow into the n region under the gate. Thus an inversion surface layer is formed as is seen in Fig. 3.2a.

Some of the holes that flow into the n region under the gate are trapped by the surface states and the rest are present as mobile carriers in the inversion layer. When the voltage on the gate is turned off the mobile minority carriers (holes) flow back to the p+ region under the influence of the reverse bias and leave behind the trapped holes in the interface states as shown in Fig. 3.2b. During the period that the pulse is off, electrons from the n-type substrate recombine with the trapped holes from the surface states thus giving rise to a

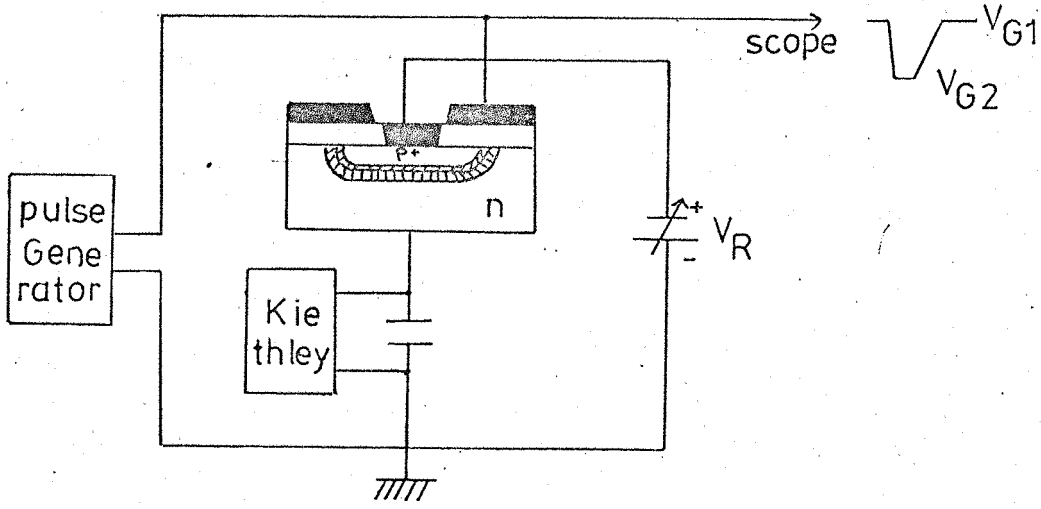


Fig. 3.1 Block diagram of Charge Pumping measurement circuitry

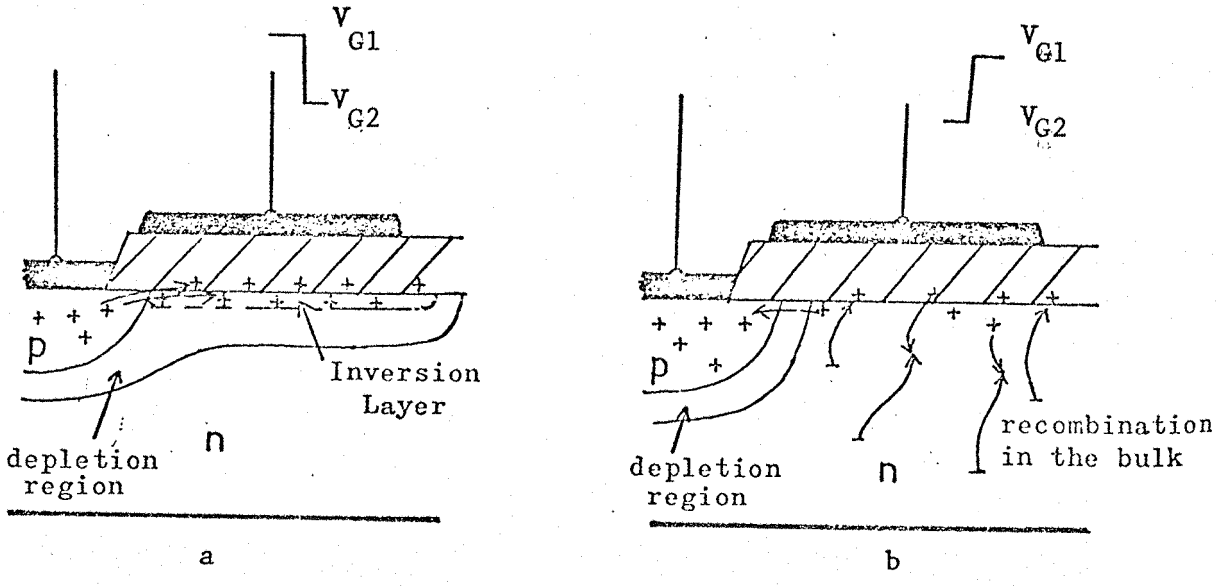


Fig. 3.2 Physical mechanism for the origin of pumped current

net flow of positive charge into the substrate. A repetitive application of the negative gate pulse results in a unidirectional current of majority carriers from the p+ region to the substrate through the interface states. This current is called 'charge pumping' current. If the gate area is large and the turn-off time of the pulse is too small some of the mobile carriers will not be able to flow back to the p+ region fast enough so they too recombine with the substrate electrons thus contributing to the pumped current. The net pumped charge density per gate pulse may therefore be expressed as follows:

$$Q_T = aQ_p + qN_{st}, \left[C\ cm^{-2}\right] \qquad 3a.1$$

where

a = fraction of mobile carriers under the gate that recombine in the bulk,

q = electronic charge $[C]$,

N_{st} = total fast surface-state density contributing to the effect with energy levels which are swept through the Fermi level when the pulse is applied $\left[cm^{-2}\right]$,

Q_p = mobile minority charge (holes) density in the inverted n-region $[Ccm^{-2}]$, which from the MOS theory (18) is:

$$Q_p \simeq 0 \qquad |V_G| < |V_T|$$

$$Q_p = C_{ox}|(V_G - V_T)| + N_D X_{inv} \qquad |V_G| \gtrsim |V_T|$$

Where C_{ox} is the oxide capacitance per unit area $[C\ cm^{-2}]$ and x_{inv} is the effective inversion layer thickness for a rectangular distribution. The pumped current is simply Q_T multiplied by the gate area A_g and gate pulse frequency f.

So for $|V_G| \gtrsim |V_T|$ the pumped current is:

$$I_{cp} = AgfQ_T = Agf\{a\left[C_{ox}\ (V_G - V_T) + N_D X_{inv}\right] + qN_{st}\} \qquad 3a.2$$

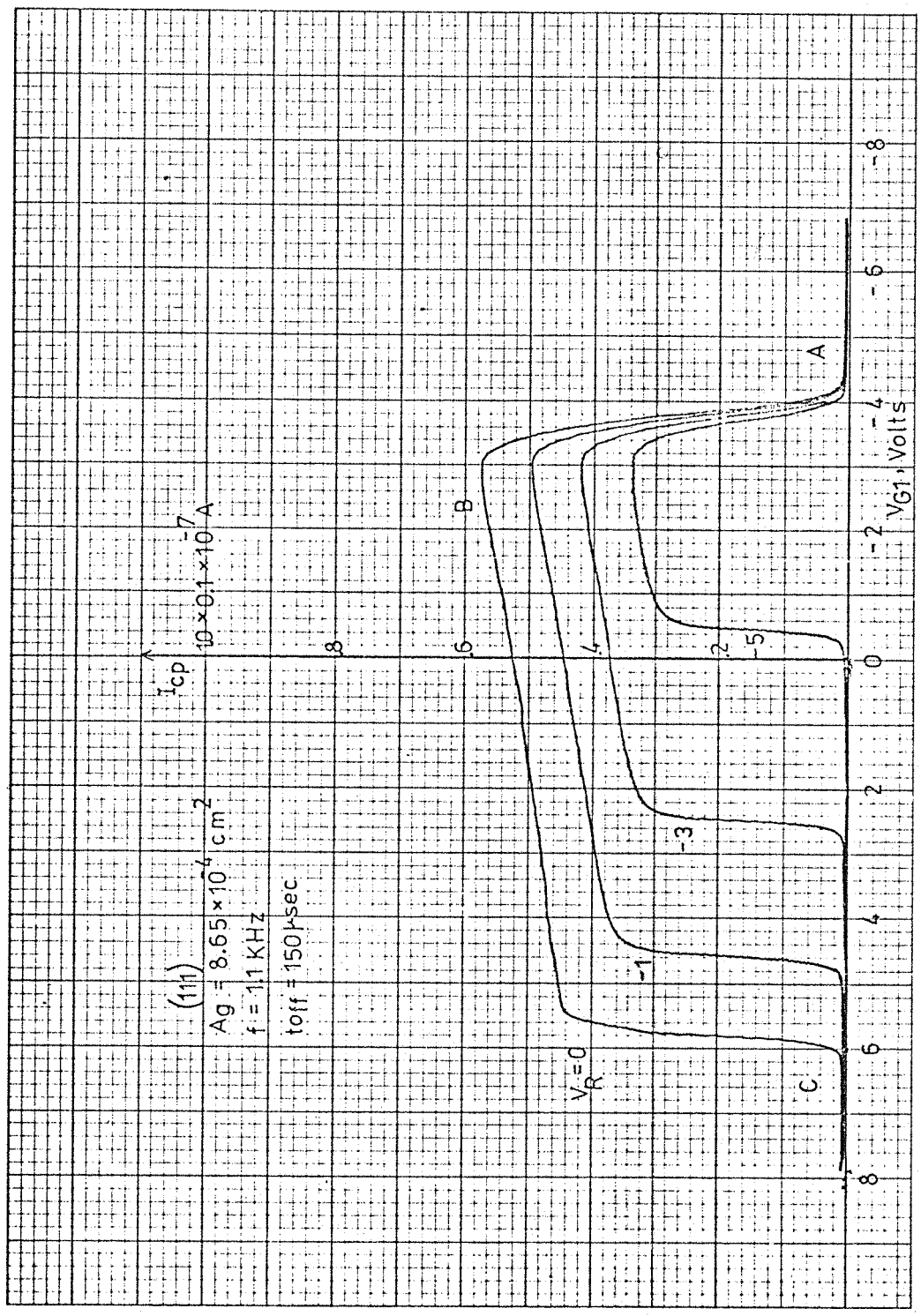
For a small gate length, a sufficiently long turn-off time (i.e., $\sim$ 100μsec) and a sufficiently large V_R the term in square brackets in the above equation 3a.2 of charge pumping the geometric components can be made negligible so that the charge pumping current will be only due to the surface state density, that is:

$$I_{cp} = A_g f q N_{st} \qquad 3a.3$$

Thus a simple way of determining to total density of surface states with energy levels which are swept through by the Fermi level when a gate pulse is applied is to measure the substrate current when a small reverse bias is applied to the junction. One volt is usually adequate to eliminate the 'geometric component' as will be shown later.

Equation (3a.3) due to Brugler (7) gives only a total number of interface states since no value is required for the actual quasi-Fermi level excursion. In CCD operation it is very important to have a low density of interface states throughout the part of the band gap scanned by the quasi-Fermi level.

Elliot (8) used an alternative approach which does enable the surface state energy distribution to be examined across most of the forbidden band gap. This is achieved by measuring the charge pumping current as a function of the pulse base level, while keeping the pulse amplitude constant. Characteristics of this type are shown in Fig. 3.3 where a gate pulse of constant amplitude equal to -10V has a base level which is scanned from +8V to -8V. Consider first region A. Here, the gate voltage goes from -6V to -16V. Both these values are above the device turn-on voltage thus the interface states are filled but are never allowed to empty and the pumped current is consequently very small. As the base level is shifted towards zero volts the pumped current increases to a maximum value because the base level is now below the turn-on voltage but the pulse level is above it. This is shown in region B. If the base level is then shifted to positive values, eventually the gate pulse is insufficient to turn the channel on at all. In this case the interface states are never filled with holes and the current is again small in region C. Thus the current level in region B corresponds to the saturation level in Fig. 3.3 and is the value required to obtain the total interface state density N_{st}. The current is a function of the reverse bias voltage since the turn-on voltage is a function of the reverse bias voltage. These characteristics were taken from a 200μm diffusion diameter gated diode (14/S, 168, 3.7% HCl) fabricated on a (111) orientation substrate. The circuit used to obtain these measurements is shown in Fig. 3.4. In the photograph of the complete test fixture in Fig. 3.5 the central box with the oscilloscope probe attached contains the circuit shown in Fig. 3.4.


(111)
Ag = 8.65×10⁻⁴ cm²
f = 11 KHz
toff = 150 μsec
Icp
10×0.1×10⁻⁷ A
A
B
C
VR=0
-1
-3
-5
VG1, Volts
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9270/1008

Fig. 3.3

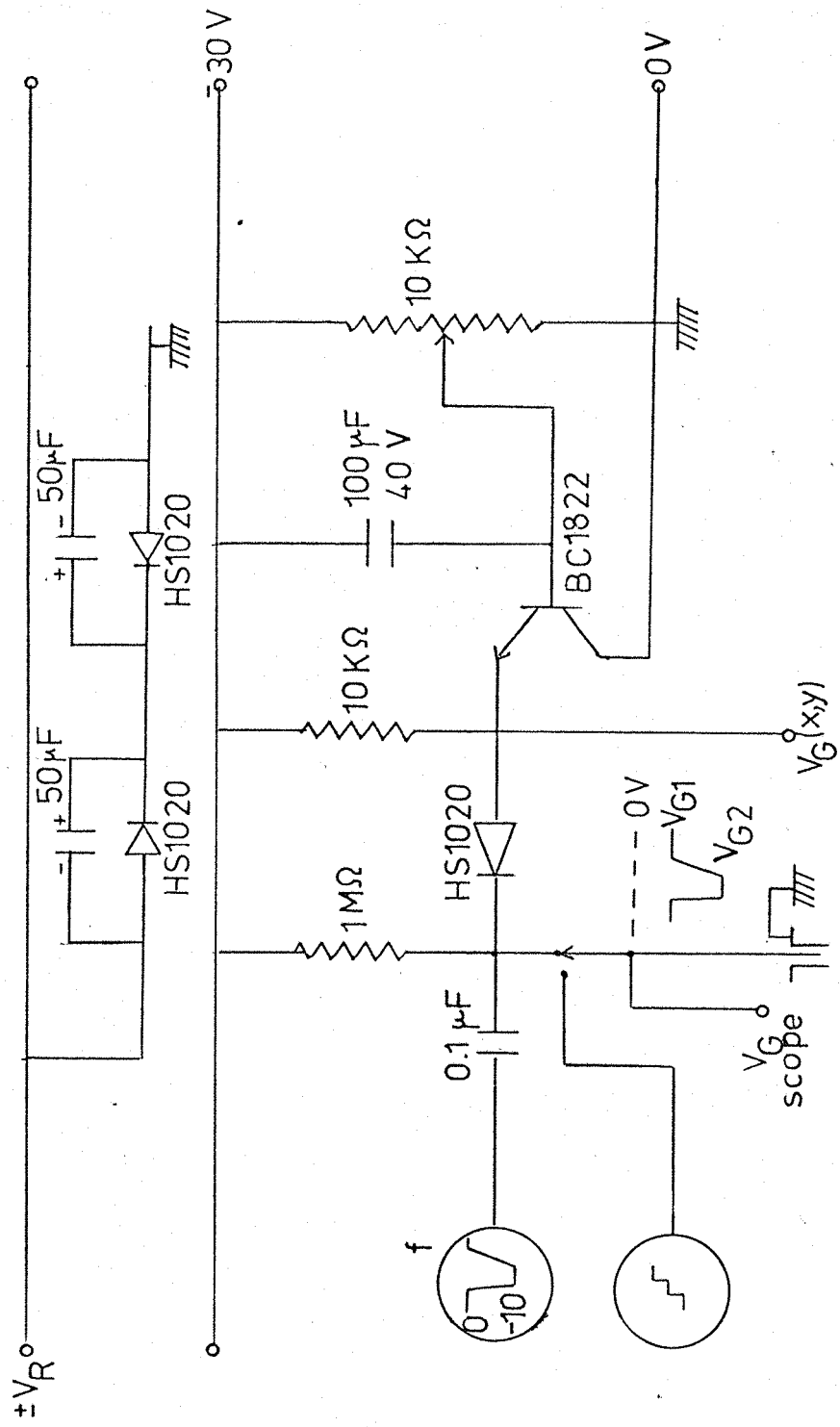


Fig. 3.4 Circuit to produce -10V amplitude pulses with +ve or -ve base level.

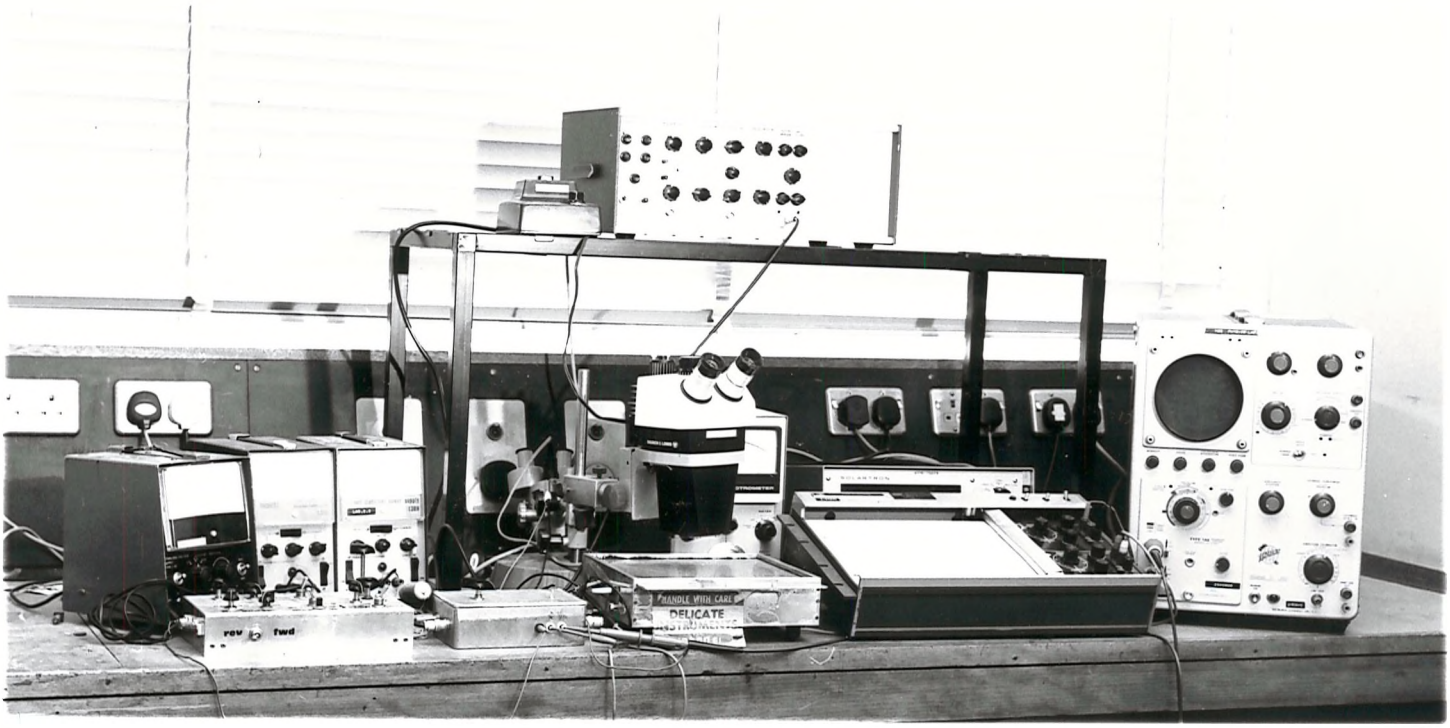


Fig. 3.5 The complete test fixture showing the centrally placed light-tight low leakage box

A simple interpretation of how the surface states are able to act as a charge coupling medium can be given by reference to the energy band diagrams in Fig. 3.6 which are drawn for a direction normal to the n-type substrate surface. The equilibrium case is first considered, that is V_R = 0V, and it is assumed that only donor states are present at the interface but the situation is not significantly different if acceptor states also exist. The energy band diagrams are not intended to be accurate they simply indicate the form of the band bending near the surface in order to simplify the description of the processes which give rise to the zero bias voltage characteristic in Fig. 3.3. In (a) the gate pulse goes from -3V to -13V and the surface potential is close to $2\phi_{Fn}$ level at both values of the gate voltage so there is little change in the occupancy of the surface states and consequently the contribution of surface states to the pumped current is small.

In (b) where the gate pulse goes from 0 to -10V some of the surface donor states which have been filled with holes during the previous pulse are below the Fermi level when the pulse is off and therefore trapped holes will be emitted and recombine subsequently with electrons from the n-type substrate giving rise to a significant charge pumping current.

In (c) where the gate pulse goes from +11V to -1V the pulse level becomes more positive and the gate voltage is below the threshold voltage even when the pulse is on and the surface states can no longer be filled by holes from the p+ region. This leads to a rapid decrease of the charge pumping current.

In all the above cases the net injected charge is proportional to the uniform trap density N_{ss} times the peak-to-peak band bending $(\psi_{s1} - \psi_{s2})$. Therefore:

$$Q_T = qN_{ss}\,(\psi_{s1} - \psi_{s2}) = qN_{ss}\Delta\psi_s = qN_{st}, \left[Ccm^{-2}\right] \qquad 3a.4$$

Thus the current will be:

$$I_{cp} = A_g f q N_{ss} \Delta\psi_s = A_g f q N_{st} \qquad 3a.5$$

When a reverse bias is applied to the junction the gate voltage at which an inversion layer forms is changed to a more negative value. This should give only a change in the voltage axis as shown in Fig. 3.3. However, there is a reduction in the overall current

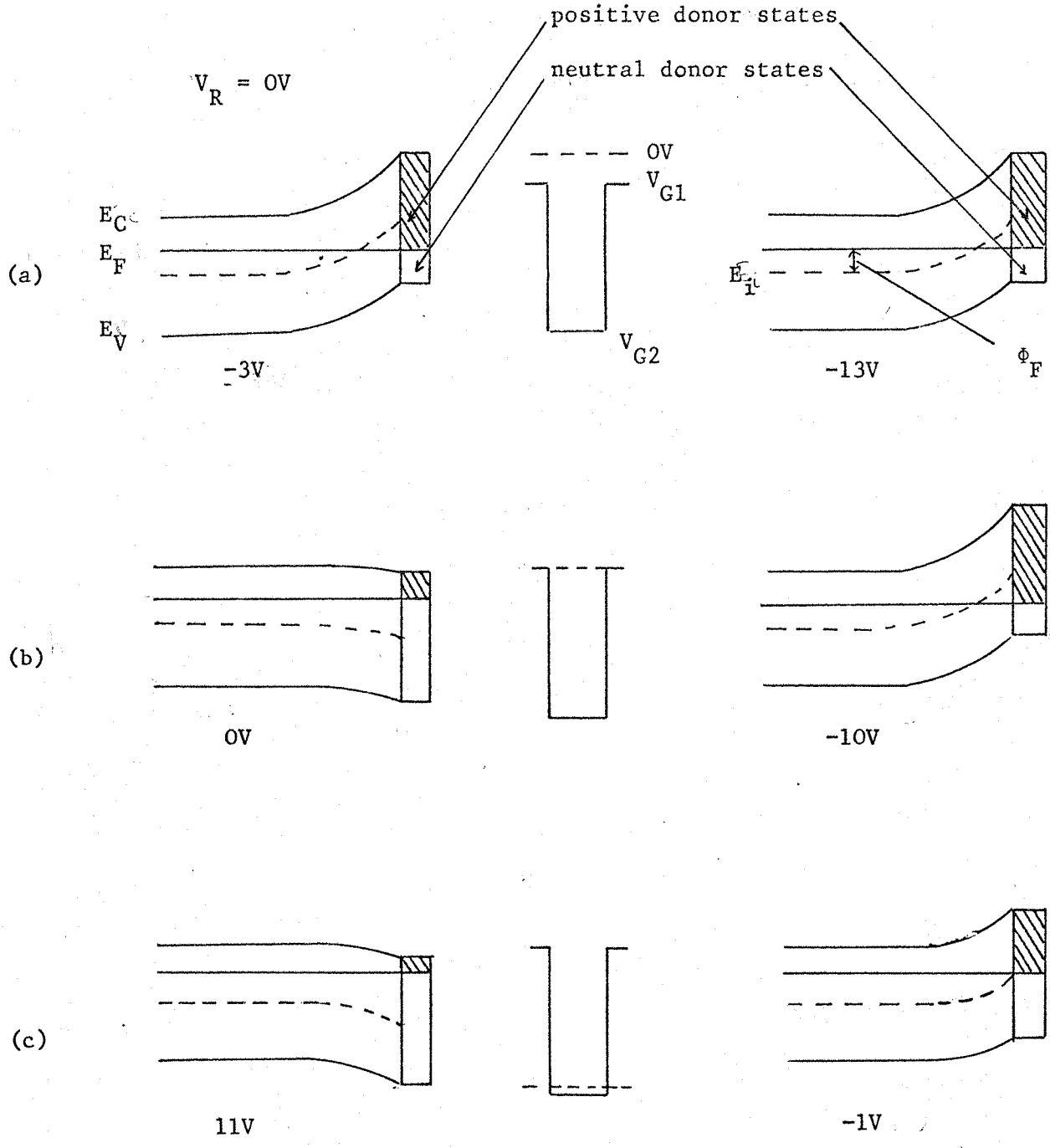


Fig. 3.6 Energy band diagrams in the device channel normal to the surface.

level because the time taken for the gate voltage to change from the new turn-on voltage to the flat band voltage is longer and allows some of the faster interface states to empty their holes which are then re-collected by the p+ region. The gate voltage at which we have the transition from region A to B is not affected by the reverse bias because the base level gate voltage here is insufficient to cause depletion of the surface at any value of reverse bias therefore we always collect those holes which were trapped during the previous turn-on period if any. This is shown schematically in Fig. 3.7 for two values of reverse bias.

The rising edge in Fig. 3.3 from A to B clearly contains information on the energy distribution of surface states and the method used to determine this distribution is explained in the next section.

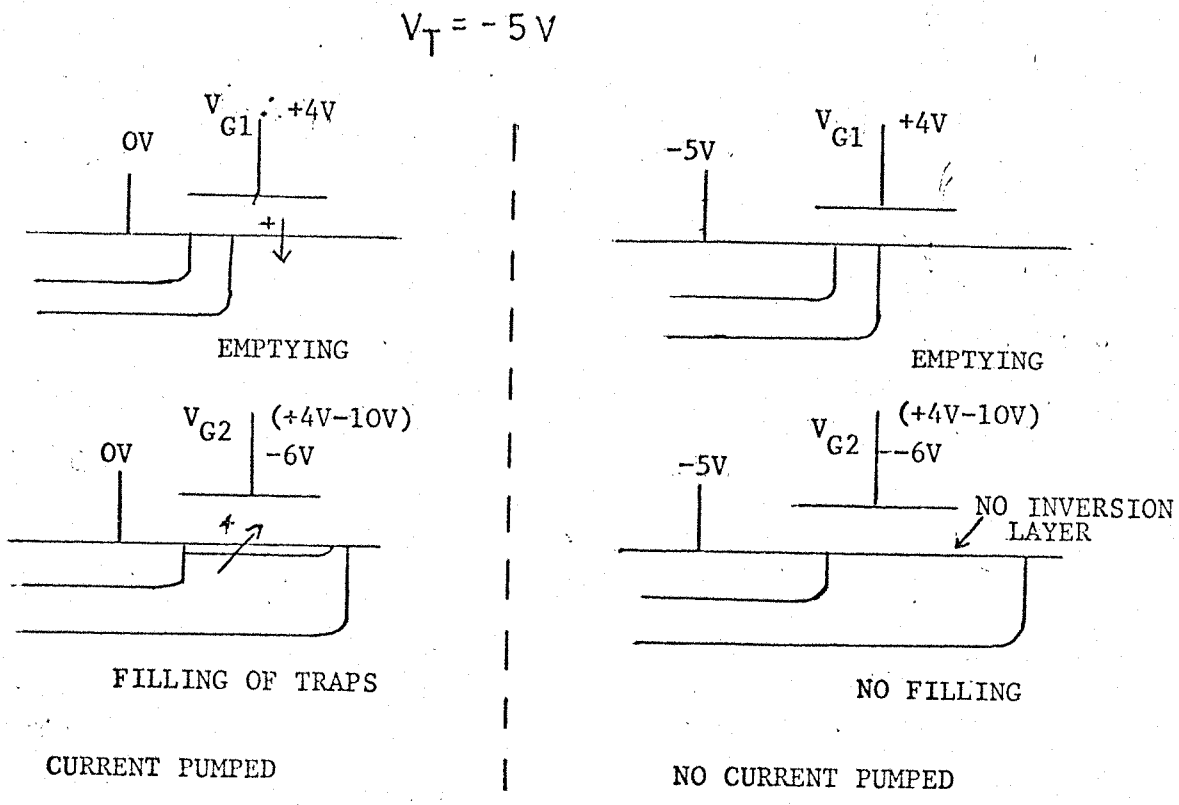

$V_T = -5V$
V_{G1}
+4V
0V
EMPTYING
V_{G2}
(+4V-10V)
-6V
0V
FILLING OF TRAPS
CURRENT PUMPED
-5V
V_{G1}
+4V
EMPTYING
V_{G2}
(+4V-10V)
-6V
-5V
NO INVERSION LAYER
NO FILLING
NO CURRENT PUMPED

Fig. 3.7

3b Theoretical Calculation of the Surface State Density as a Function of Energy from Charge Pumping current measurements

In Section 3a it was shown that the charge pumping current must be proportional to the excursion of surface potential $\Delta\psi_s$ caused by the gate voltage pulse. From the theory of the gated diode the relation between V_G and ψ_s in non-equilibrium case can be obtained (17). From this relation the graph of ΔV_G versus $\Delta\psi_s$ can be calculated. This graph, with the assumption that N_{ss} is constant as a function of ψ_s, should have the same shape as the I_{cp} versus V_G. We shall see later that in fact the theoretical graph $\Delta\psi_s$ versus V_G has almost the same shape as the experimentally measured curves of I_{cp} versus V_G, thus the agreement between the theory and experiment seems to be quite good. Let us now consider the case of an ideal gated diode with an n-type substrate in the non-equilibrium condition.

For an ideal gated diode we define the following conditions:

1. At zero applied gate voltage V_G there is no energy difference between the metal work function ϕ_m and the semiconductor work function ϕ_s is zero as is shown in Fig. 3.8 (17), therefore,

$$\phi_{ms} = \phi_m - (x + \frac{Eg}{2q} - \psi_B) = 0,$$

where x is the semiconductor electron affinity,

Eg the band gap of the semiconductor and

ψ_B the potential difference between the Fermi level E_F and intrinsic Fermi level E_i

In other words, the bands are flat (Flat-band condition) when there is no applied voltage.

2. The only charges which can exist in the structure under the condition $V_G \neq 0$ are those in the semiconductor with equal but opposite sign to the change on the metal surface adjacent to the SiO_2

3. The resistivity of the insulator is infinite.

For non-equilibrium situations the relation between the gate voltage and surface potential ψ_s in an ideal diode can be derived as follows The gate voltage V_G will appear partly across the oxide and partly across the silicon that is,

$$V_G = V_{ox} + \psi_s \qquad 3b.1$$

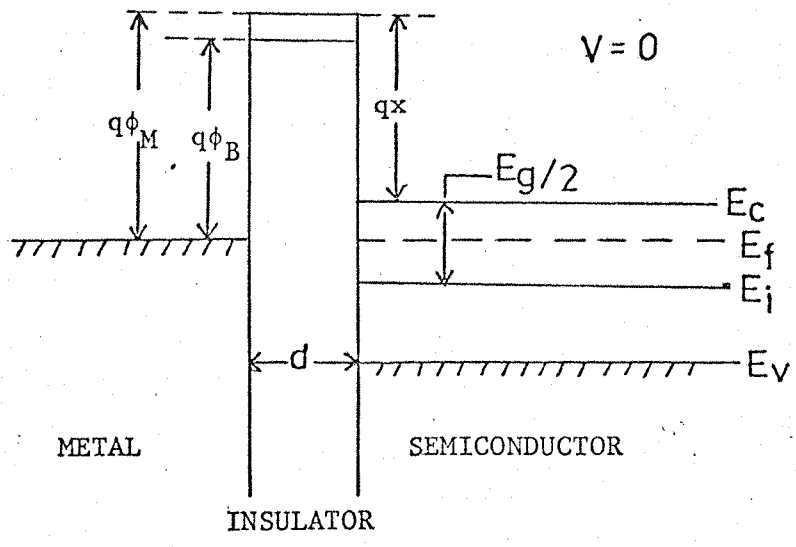


Fig. 3.8 Ideal MIS diode (n-type semiconductor)

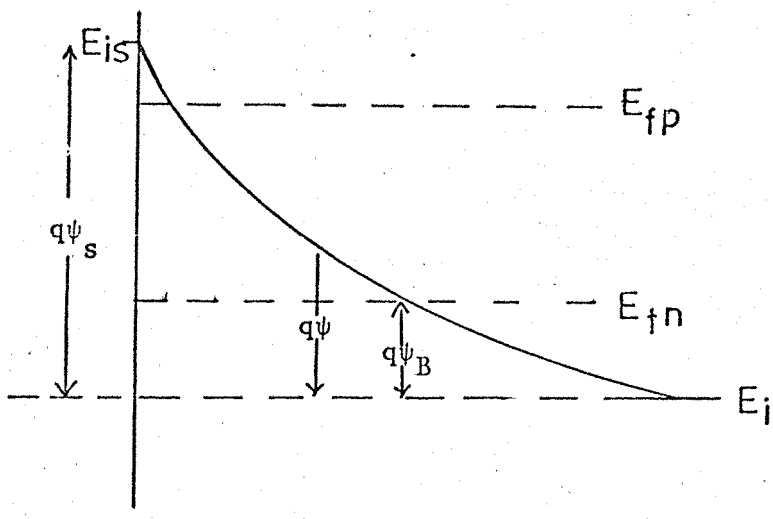


Fig. 3.9 Energy diagram near the surface in non-equilibrium for n-type diode.

By Gauss'law the electric displacement must be continuous across the oxide-silicon interface in the absence of charge at the interface. Therefore

$$\varepsilon_{ox}\mathcal{E}_{ox} = \varepsilon_{si}\mathcal{E}_{si} \qquad 3b.2$$

Since we deal with ideal diode $\mathcal{E}_{ox}$ must be uniform i.e.,

$$\mathcal{E}_{ox} = -\frac{V_{ox}}{X_{ox}} \qquad 3b.3$$

where V_{ox} is the voltage across the oxide and X_{ox} the oxide thickness.

At the Si surface by Gauss'theorem we have

$$\mathcal{E}_{si} = -\frac{Q_s}{\varepsilon_{si}} \qquad 3b.4$$

where Q_s is the total charge in the silicon and ε_{si} the permitivity of the silicon.

Combining 3b.2, 3b.3, 3b.4 we have

$$V_G = -\frac{X_{ox}}{\varepsilon_{ox}} Q_s + \psi_s = -\frac{Q_s}{C_{ox}} + \psi_s \qquad 3b.5$$

where $C_{ox} = \frac{\varepsilon_{ox}}{X_{ox}}$

Q_s is also a function of surface potential and in this case of non-equilibrium, it is a function of the reverse bias-voltage, V_R.

Thus we write,

$$V_G = -\frac{Q_s(\psi_s, V_R)}{C_{ox}} + \psi_s \qquad 3b.6$$

The analytical function of Q_s can be derived as follows.

The one dimensional Poisson equation for the potential ψ is:

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_{si}} \qquad 3b.7$$

where $\rho(x)$ is the total space charge density given by:

$$\rho(x) = q(N_D^+ - N_A^- + p_n - n_n) \qquad 3b.8$$

where N_D^+, N_A^- are the densities of the ionized donors and

acceptors respectively and p_n, n_n the minority and majority carriers in the space charge region of the diode.

Fig. 3.9 shows the energy diagram near the surface for a n-type gate diode from which the expressions for p_n, n_n can be derived, for non-equilibrium . Therefore,

$$n_n = n_i e^{(E_{Fn} - E_i + q\psi)/KT} = n_i e^{(E_{Fn} - E_i)/K_T} e^{q\psi/KT}$$
$$= n_{no} e^{q\psi/KT} = n_{no} e^{\beta\psi} \qquad 3b.9$$

where n_{no} is the majority carrier density in the bulk of the semiconductor and $\beta = q/KT$ (K = Boltzmann's constant).

For p_n we have, as seen from the Fig. 3.9.

$$p_n = n_i e^{-(E_{Fp} - E_i + q\psi)/KT}$$
$$= n_i e^{-(E_{Fn} - qV_R - E_i + q\psi)/KT}$$
$$= n_i e^{-(E_{Fn} - E_i)} e^{(qV_R - q\psi)/KT}$$
$$= p_{no} e^{(qV_R - q\psi)/KT} = p_{no} e^{(-\beta\psi + \beta V_R)} \qquad 3b.10$$

where p_{no} is the equilibrium minority carrier density in the bulk of the semiconductor.

At the surface we have, for p_n, n_n:

$$n_{ns} = n_{no} e^{\beta\psi s} \qquad 3b.11$$

$$p_{ns} = p_{no} e^{(-\beta\psi_s + \beta V_R)} \qquad 3b.12$$

Combining equations 3b.7 and 3b.8 we have

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\varepsilon_{si}} (N_D^+ - N_A^- + p_n - n_n) \qquad 3b.13$$

Substituting equations 3b.9 and 3b.10 into 3b.13 we have

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\varepsilon_{si}} (N_D^+ - N_A^- + P_{no} e^{(-\beta\psi + \beta V_R)} - n_{no} e^{\beta\psi}) \qquad 3b.14$$

In the bulk of the semiconductor far from the surface, charge neutrality must exist. Therefore $\rho(\infty) = 0$ and $\psi(\infty) = 0$. Thus in the bulk we have,

$$N_D^+ - N_A^- + p_{no} - n_{no} = 0, \text{or } N_D^+ - N_A^- = n_{no} - p_{no}$$

The resultant Poisson equation to be solved is therefore:

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\varepsilon_{si}}\left(n_{no} - p_{no} + p_{no}e^{(-\beta\psi+\beta V_R)} - n_{no}e^{\beta\psi}\right) \qquad 3b.15$$

or

$$\frac{\partial^2\psi}{\partial x^2} = -\frac{q}{\varepsilon_{si}}\left(p_{no}(e^{(-\beta\psi+\beta V_R)}-1) - n_{no}(e^{\beta\psi}-1)\right) \qquad 3b.16$$

Integration of Equation 3b.16 from the bulk towards the surface (19) gives,

$$\int_0^{\partial\psi/\partial x} \frac{\partial\psi}{\partial x}\, d\left(\frac{\partial\psi}{\partial x}\right) = -\frac{q}{\varepsilon_{si}} \int_0^{\psi}\left[p_{no}(e^{(-\beta\psi+\beta V_R)}-1) - n_{no}(e^{\beta\psi}-1)\right] d\psi \qquad 3b.17$$

which gives the relation between the electric field $\mathcal{E}$ $\left(\equiv \frac{\partial\psi}{\partial x}\right)$ and the potential ψ as

$$\mathcal{E} = \left(\frac{2kT}{q}\right)^2 \left(\frac{qn_{no}}{2\varepsilon_{si}}\right)\left[\frac{p_{no}}{n_{no}}\left(e^{(-\beta\psi+\beta V_R)} + \beta\psi - e^{\beta V_R}\right) - \left(\beta\psi - e^{\beta\psi} + 1\right)\right] \qquad 3b.18$$

We shall introduce the following abbreviations:

$$L_D = \sqrt{\frac{2KT\varepsilon_s}{n_{no}q^2}} = \sqrt{\frac{2\varepsilon_{si}}{2n_{no}\beta}}$$

and

$$F(\beta\psi, V_R, \frac{p_{no}}{n_{no}}) = \left[\frac{p_{no}}{n_{no}}\left(e^{(-\beta\psi+\beta V_R)} + \beta\psi - e^{\beta V_R}\right) - \left(\beta\psi - e^{\beta\psi} + 1\right)\right]^{\frac{1}{2}} \gtrless 0$$

where L_D is called the extrinsic Debye length for electrons. Thus the electric field becomes

$$\mathcal{E} = -\frac{\partial\psi}{\partial x} = \pm \frac{2KT}{qL_D} F(\beta\psi, V_R, \frac{p_{no}}{n_{no}}) \qquad 3b.19$$

with the positive sign for $\psi>o$ and the negative sign for $\psi<o$. To determine the electric field at the surface, we let $\psi = \psi_s$, so that

$$\mathcal{E}_s = \pm \frac{2KT}{qL_D} F(\beta\psi_s, V_R, \frac{p_{no}}{n_{no}}) \qquad 3b.20$$

Similarly, by Gauss'law the space charge per unit area required to produce this field is

$$Q_s = -\varepsilon_{si}\mathcal{E}_s = \mp \frac{2KT\varepsilon_{si}}{qL_D} F(\beta\psi_s, V_R, \frac{p_{no}}{n_{no}}) .$$

Thus equation 3b.6 becomes:

$$V_G = -\frac{Q_s}{C_{ox}} + \psi_s = \pm \frac{2KT\varepsilon_{si}}{qL_D C_{ox}} F(\beta\psi_s, V_R, \frac{p_{no}}{n_{no}}) + \psi_s \qquad 3b.21$$

or

$$V_G = \pm \frac{2KTX_{ox}\varepsilon_{si}}{qL_D\varepsilon_{ox}} \left[\frac{p_{no}}{n_{no}} (e^{(-\beta\psi_s + \beta V_R)} + \beta\psi_s - e^{\beta V_R}) + (e^{\beta\psi} - \beta\psi_s - 1)\right]^{\frac{1}{2}}$$

$$+ \psi_s \qquad 3b.22$$

or

$$V_G = \pm \frac{2KTX_{ox}\varepsilon_{si}}{qL_D\varepsilon_{ox}} \left[\frac{p_{no}}{n_{no}} e^{\beta V_R} (e^{(-\beta\psi_s)} + \beta\psi_s e^{(-\beta V_R)} - 1)\right.$$

$$\left. + (e^{\beta\psi_s} - \beta\psi_s - 1)\right]^{\frac{1}{2}} + \psi_s \qquad 3b.23$$

where again the signs are for $\psi_s > o$ and $\psi_2 < o$ respectively.
We are interested here in the values of $V_G > V_T$ (V_R) that is the case for strong inversion.
ψ_s is then given by,

$$\psi_s \simeq V_R + 2\psi_B \qquad 3b.24$$

Where ψ_B the potential in the bulk equal to $E_i - E_{Fn}$ as shown in Fig. 3.9 and V_T is the turn-on voltage.
Thus we obtain,

$$V_T = -\frac{Q_s(V_R)}{C_{ox}} + V_R + 2\psi_B . \qquad 3b.25$$

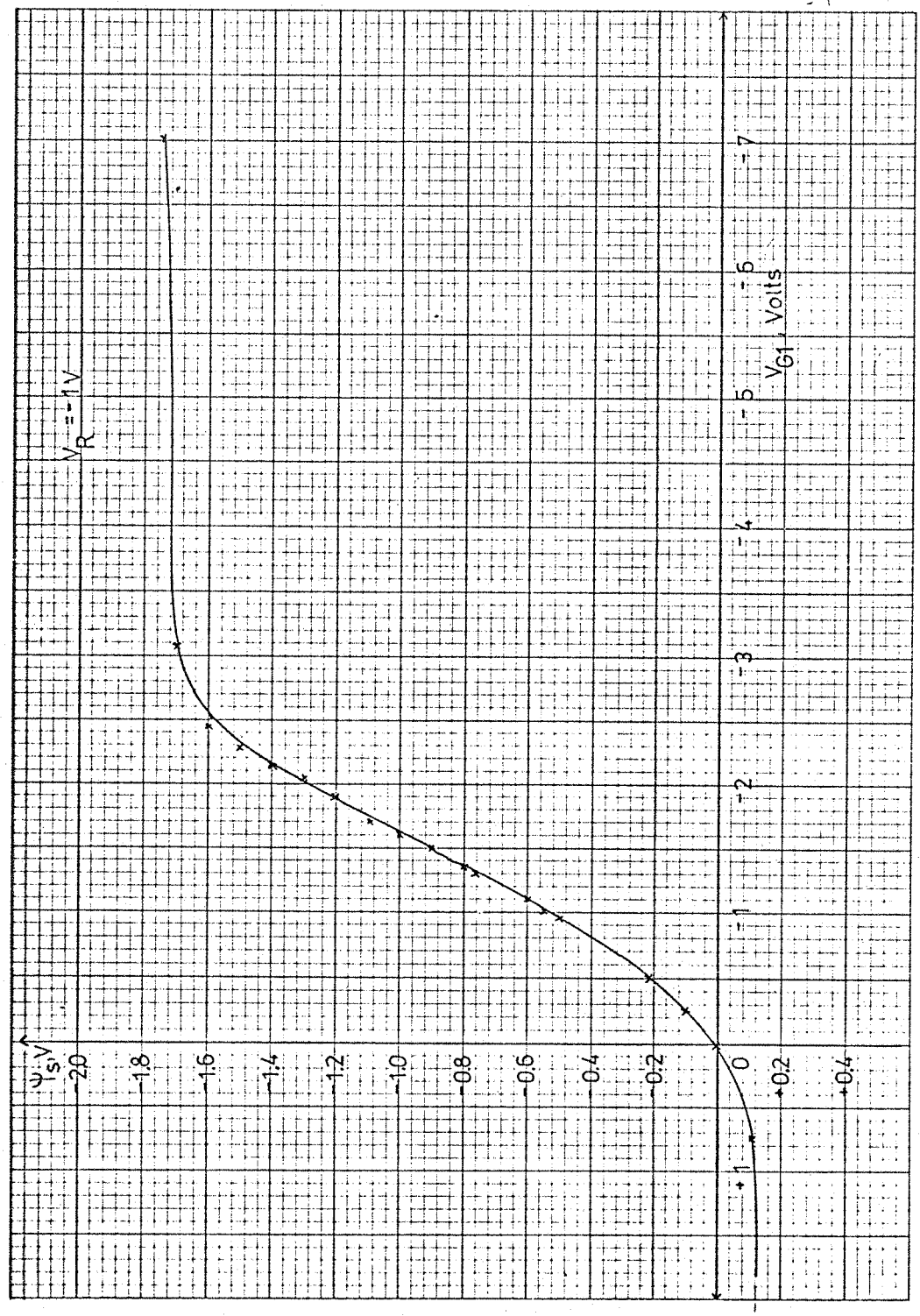
For $V_R = -1V$, $X_{ox} = 1.2\times10^{-5}cm$, $n_{no} = 10^{15}cm^{-3}$, $P_{no} = 2.1\times10^{5}cm^{-3}$.

we can get values of V_G from equ. 3b.23 which shows the changes of V_G with ψ_s. These are listed in table 1.

Table 1

ψ_s	V_{G1}
-1.9	-54.597
-1.8	- 9.486
-1.7	- 3.080
-1.6	- 2.426
-1.5	- 2.284
-1.4	- 2.159
-1.3	- 2.029
-1.2	- 1.900
-1.1	- 1.769
-1.0	- 1.630
-0.9	- 1.504
-0.8	- 1.364
-0.5	- 0.944
-0.1	- 0.275
0.0	0.000
+0.1	+ 0.776
+0.3	+34.310
+0.6	+8239.600

These data are plotted in Fig. 3.10.
From this graph we can obtain approximate values of $\Delta\psi_s$ versus V_{G1}, (where V_G switches between the two values V_{G1}, and V_{G2}) the difference being 10 volts and the values are shown in table 2 and subsequently plotted in Fig. 3.11.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ψ_s, V
V_R = -1V
V_{G1}, Volts
-2.0
-1.8
-1.6
-1.4
-1.2
-1.0
-0.8
-0.6
-0.4
-0.2
0
+0.2
+0.4
+1
-1
-2
-3
-4
-5
-6
-7

Fig. 3.10

Table 2

V_{G1} (volts)	V_{G2} (volts)	$\Delta\psi_s$ (volts)
-8.0	-18	0.06
-7.0	-17	0.06
-6.0	-16	0.07
-5.0	-15	0.07
-4.0	-14	0.08
-3.0	-13	0.15
-2.5	-12.5	0.22
-2.3	-12.3	0.32
-2.0	-12.0	0.52
-1.8	-11.8	0.63
-1.6	-11.6	0.82
-1.4	-11.4	0.92
-1.2	-11.2	1.11
-1.0	-11.0	1.30
-0.5	-10.5	1.59
-0.3	-10.3	1.70
0.0	-10.0	1.81
+0.3	-9.7	1.89
+0.5	-9.5	1.90
+0.8	-9.8	1.91
+1.0	-9.0	1.93
+2.0	-8.0	1.96
+3.0	-9.0	1.97
+4.0	-6.0	1.97
+5.0	-5.0	1.97
+6.0	-4.0	1.95
+7.0	-3.0	1.90
+8.0	-2.0	1.50
+9.0	-1.0	0.70
+10.0	0.0	0.20

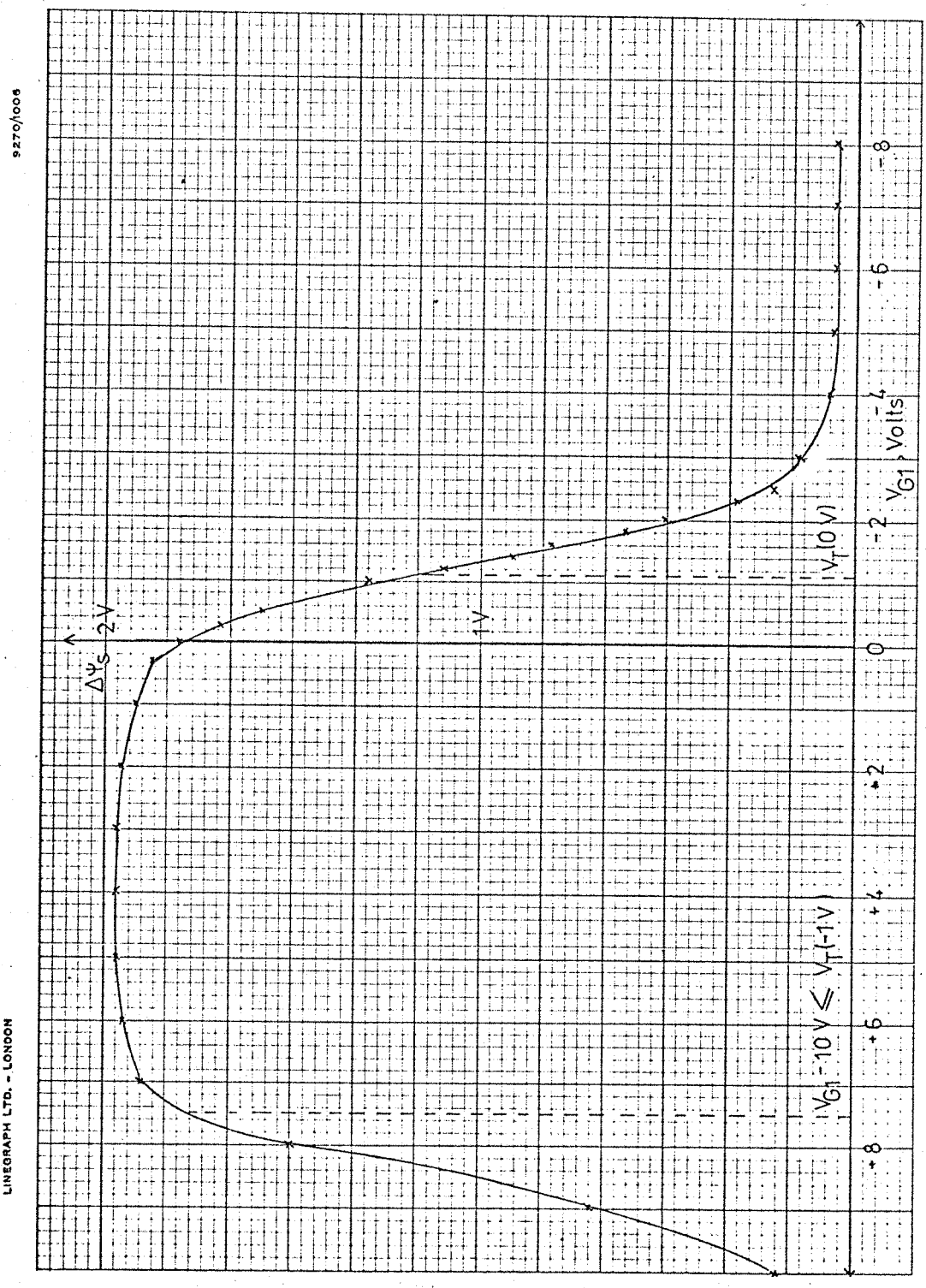

9270/1006
LINEGRAPH LTD. - LONDON
$\Delta\psi_s$ 2V
1V
V_T (10 V)
V_{G1}, Volts
0
-2
-4
-6
-8
+2
+4
+6
+8
V_{G1} -10 V ≤ V_T-1 V

Fig. 3.11

Indicated on the graph of Fig. 3.11 are the two extremes of V_{G1} between which an inversion layer is created by the pulse, together with a return of the gate voltage to a value such that the surface is approximately at the Flat-band condition. These two conditions are necessary and sufficient to obtain the charge pumped current.

The charge pumped current is the result of a scan of surface potential between ψ_{s1} and ψ_{s2} corresponding to V_{G1} and V_{G2}. This leads immediately to the following expression for the pumped current

$$I_{cp} = qfA_g \left[-\int_{\psi_{s1}}^{\psi_{s2}} N_{ss} d\psi_s \right] . \qquad 3b.26$$

In order to obtain a scan of the value of the distribution of N_{ss}, that is the value of N_{ss} at each ψ_{s1} it is necessary to form the derived function of I_{cp} with respect to ψ_{s1}.

Therefore, using the calculus method we have:

$$I_{cp} + \delta I_{cp} = qfA_g \left[-\int_{\psi_{s1}+\delta\psi_{s1}}^{\psi_{s2}+\delta\psi_{s2}} N_{ss} d\psi_s \right] \qquad 3b.27$$

or

$$I_{cp}+\delta I_{cp} = qfA_g \left[-\left(\int_{\psi_{s1}}^{\psi_{s2}} N_{ss} d\psi_s + \int_{\psi_{s2}}^{\psi_{s2}+\delta\psi_{s2}} N_{ss} d\psi_s + \int_{\psi_{s1}+\delta\psi_{s1}}^{\psi_{s1}} N_{ss} d\psi_s \right) \right] \qquad 3b.28$$

or

$$I_{cp}+\delta I_{cp} = qfA_g \left[-\int_{\psi_{s1}}^{\psi_{s2}} N_{ss} d\psi_s \right] - qfA_g \left[\int_{\psi_{s2}}^{\psi_{s2}+\delta\psi_{s2}} N_{ss} d\psi_s + \int_{\psi_{s1}+\delta\psi_{s1}}^{\psi_{s1}} N_{ss} d\psi_s \right] \qquad 3b.29$$

or

$$\delta I_{cp} = -qfA_g\left[\int_{\psi_{s2}}^{\psi_{s2}+\delta\psi_{s2}} N_{ss}d\psi_s + \int_{\psi_{s1}+\delta\psi_{s1}}^{\psi_{s1}} N_{ss}d\psi_s\right] \qquad 3b.30$$

hence (19)

$$\delta I_{cp} = -qfA_g\ \delta\psi_{s2}N_{ss}(\psi_{s2}+\partial\delta\psi_{s2}) + \delta\psi_{s1}N_{ss}(\psi_{s1}+\beta\delta\psi_{s1}) \qquad 3b.31$$

where ∂ and β have some value between 0 and 1.

Dividing equation 3b.31 by $\delta\psi_{s1}$ we have

$$\frac{\delta I_{cp}}{\delta\psi_{s1}} = -qfA_g\ \frac{\delta\psi_{s2}}{\delta\psi_{s1}}\ N_{ss}(\psi_{s2}+\partial\delta\psi_{s2}) + qfA_gN_{ss}(\psi_{s1}+\beta\delta\psi_{s1}) \qquad 3b.32$$

On proceeding to the limit $\delta\psi_{s1} \to 0$ (also $\delta\psi_{s2} \to 0$) we have

$$\frac{dI_{cp}}{d\psi_{s1}} = -qfA_g\ \frac{d\psi_{s2}}{d\psi_{s1}}\ N_{ss}(\Psi_{s2}) + qfA_gN_{ss}(\Psi_{s1}) \qquad 3b.33$$

or

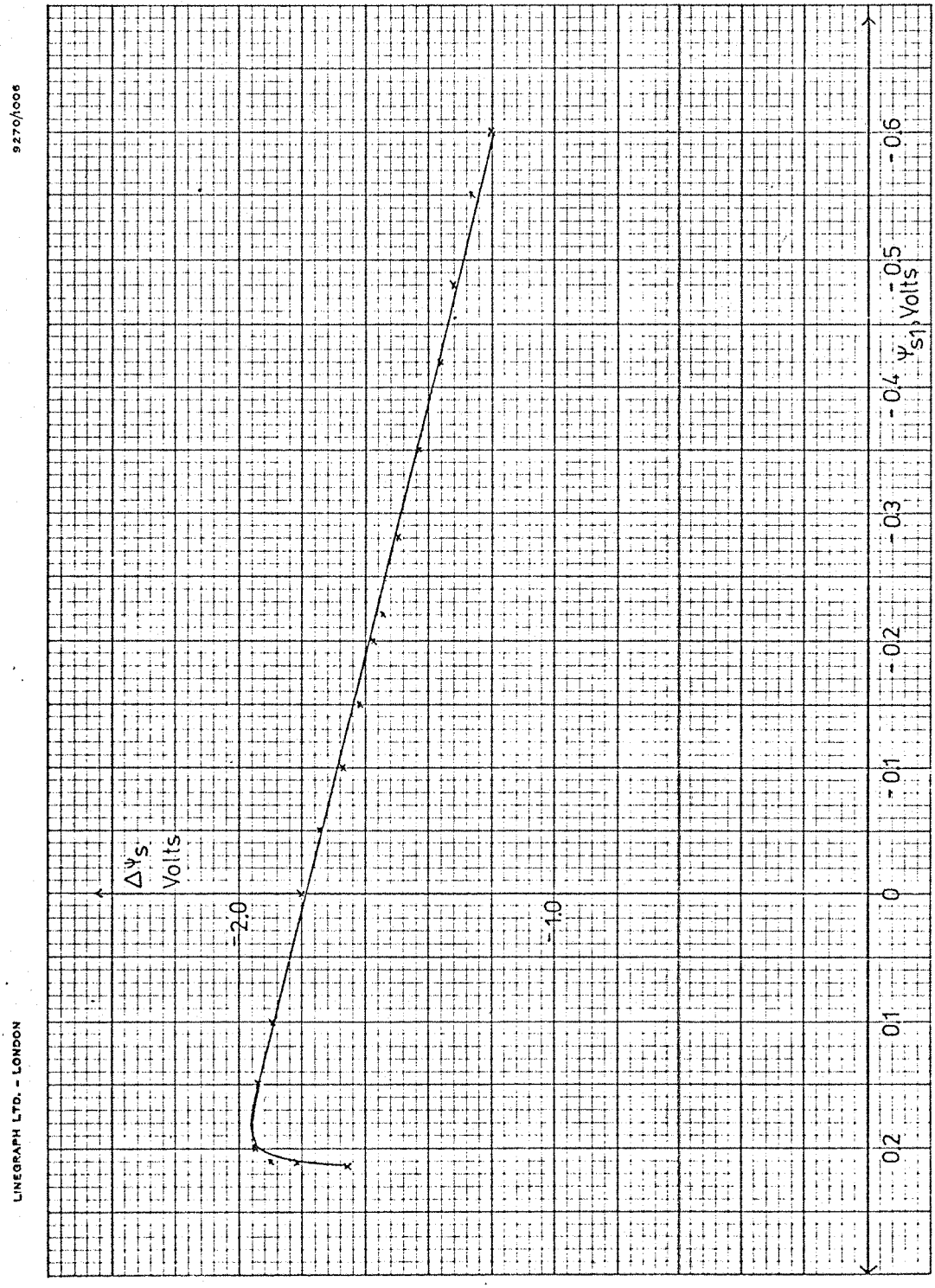
$$\frac{dI_{cp}}{d\psi_{s1}} = qfA_gN_{ss}(\psi_{s1}) - qfA_g\ \frac{d\psi_{s2}}{d\psi_{s1}}\ N_{ss}(\psi_{s2}) \qquad 3b.34$$

But $$\frac{dI_{cp}}{d\psi_{s1}} = \frac{dI_{cp}}{dV_{G1}} \cdot \frac{dV_{G1}}{d\psi_{s1}} \qquad 3b.35$$

so we have,

$$\frac{dI_{cp}}{dV_{G1}} \cdot \frac{dV_{G1}}{d\psi_{s1}} = qfA_gN_{ss}(\psi_{s1}) - qfA_g\ \frac{d\psi_{s2}}{d\psi_{21}}\ N_{ss}(\psi_{s2}) \qquad 3b.36$$

However, $\frac{d\psi_{s2}}{d\psi_{s1}}$ can be found from a graphical plot of $\Delta\psi_s$ versus ψ_{s1} as shown in Fig. 3.12. The slope of the graph is equal to $1 - \frac{d\psi_{s2}}{d\psi_{s1}}$ and in the range of interest we find that the


$\Delta\psi_s$ Volts
-2.0
-1.0
0.2
0.1
0
-0.1
-0.2
-0.3
-0.4
-0.5
-0.6
ψ_{s1}, Volts
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9270/1006

Fig. 3.12

value of $\frac{d\psi_{s2}}{d\psi_{s1}}$ is << 1. Consequently we may write:

$$\frac{dI_{cp}}{dV_{G1}} \frac{dV_{G1}}{d\psi_{s1}} \simeq qfAgN_{ss}(\psi_{s1}) \qquad 3b.37$$

From this equation we can obtain the value of N_{ss} at each ψ_{s1} since we have a measurement of I_{cp} versus V_{G1} and a calculated graph of V_{G1} versus ψ_{s1}, as will be shown in the next section.

3c Change Pumping current measurements on gated diodes

In this section, the charge pumping current measurements were made on the gated diodes that were used for the leakage current measurements described in Chapter 2.

In fact all these measurements were made on gated diodes from the same slice with characteristics

14/S 3.7% HCl type 1

The apparatus used for these measurements was described in section 3a of this present chapter. For all the following measurements the pulse which is applied to the gate has a constant amplitude of 10V and is shown in Fig. 3.13.

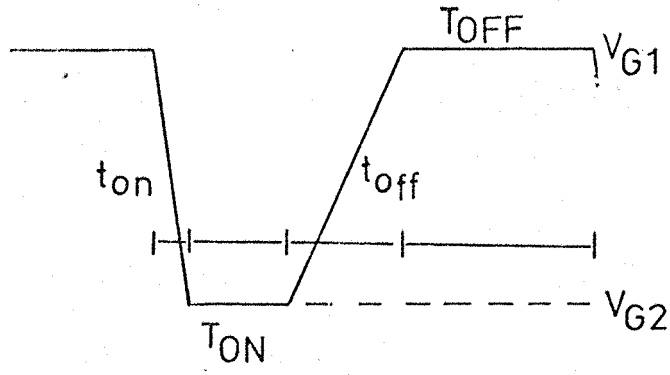
The following measurements were made so as to check the validity of equation 3b.26 .

At first we want to find the proper turn-off time, t_{off}, of the applied pulse for which the 'geometric component' of the charge pumped current is eliminated.

In Fig. 3.14 the charge pumped current versus the gate pulse testing voltage V_{G1} is shown for a particular gated diode with a gate area of 8.65×10^{-4} cm^2 and width of gate annulus, L, equal to 100μm. The pulse applied to the gate had a frequency of about 2kHz, and the resting level, V_{G1}, of this pulse was scanned from -8 to +8 volt. The diode was reversed biased to a value of V_R equal to -1V. The turn-off time of the pulse (defined in Fig. 3.13) was different for each scan and the range was from 2μsec to 180μsec.

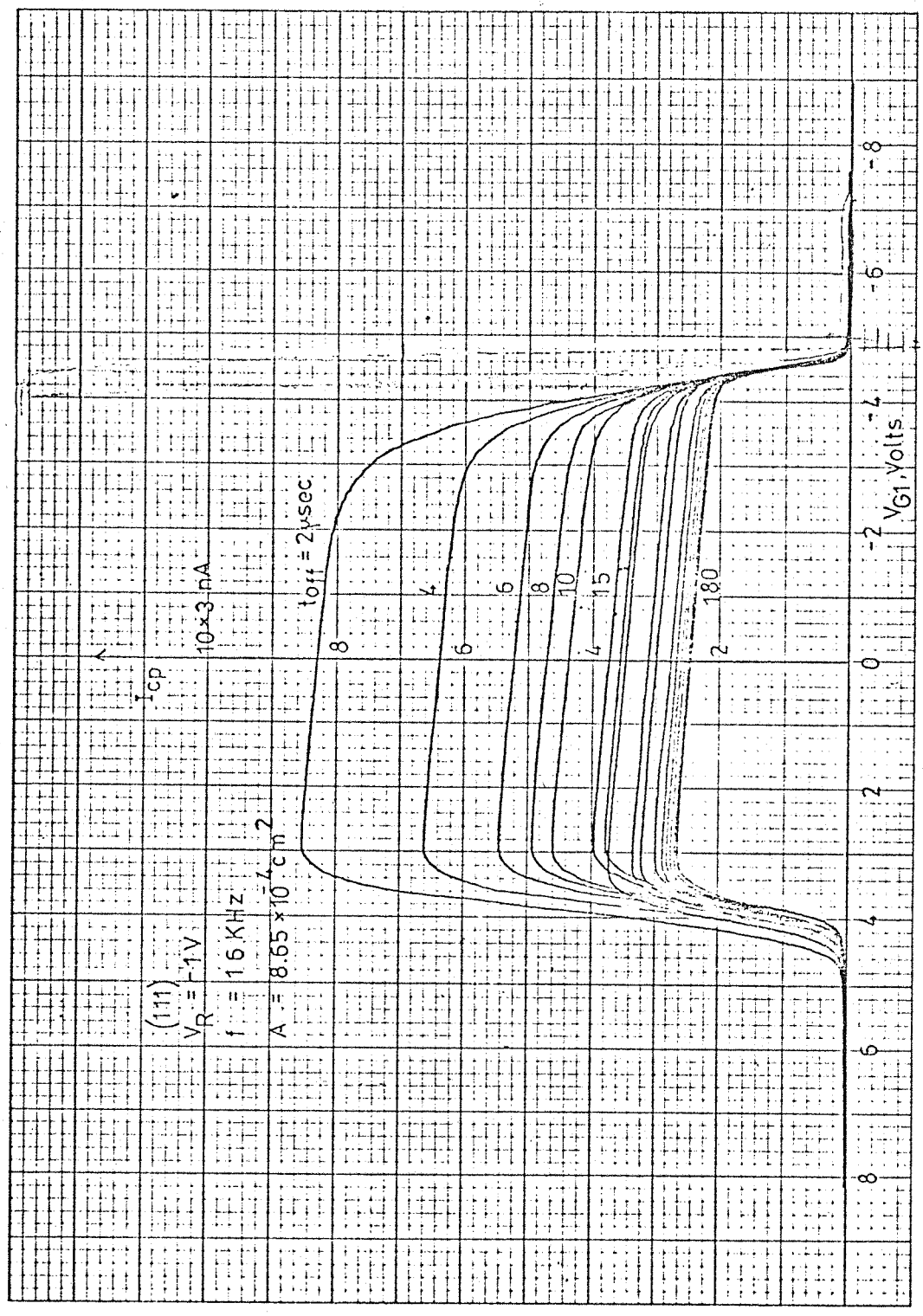
From these experimental curves the graph of charge pumped current versus t_{off} of the gate pulse, at a constant V_{G1} was obtained. This is shown in graph A of Fig. 3.15. The rest of the graphs in this Fig. were taken from repeating the experiment using other diodes with a different gate area as indicated. On each graph the value of the time constant $\frac{5L^2}{D_p}$ is indicated where D_p is the diffusion coefficient for holes in the inversion layer and is taken to be equal to $10cm^2 sec^{-1}$(22).

This time constant is the criterion for mobile carriers to escape and not give rise to a 'geometric component' of charge pumped current.



$$V_{G1} - V_{G2} = 10\ V$$

Fig. 3.13


(111)
V_R = -1V
f = 1.6 KHz
A = 8.65 x 10^{-4} cm^2
t_{off} = 2μsec
I_{cp}
10x3 nA
8
6
4
2
0
-2
-4
-6
-8
V_{G1}, Volts
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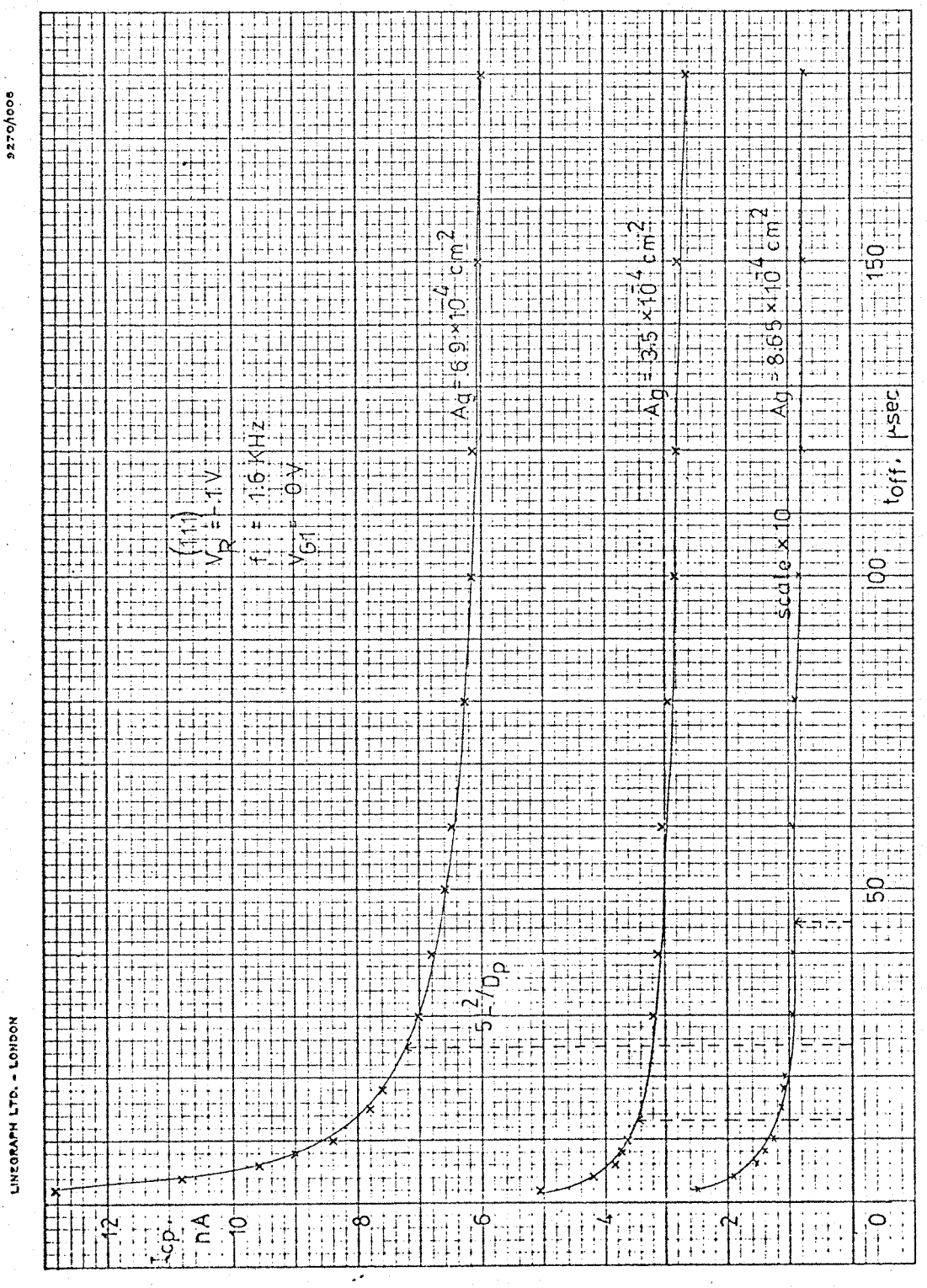
9270/1006

Fig. 3.14


(111)
V_R = -1V
f = 1.6 kHz
V_{G1} = 0V
Ag = 6.9 × 10⁻⁴ cm²
Ag = 3.5 × 10⁻⁴ cm²
Ag = 8.65 × 10⁻⁴ cm²
scale × 10
$S = 2/D_p$
Icp. nA
toff. μsec
0
2
4
6
8
10
12
50
100
150
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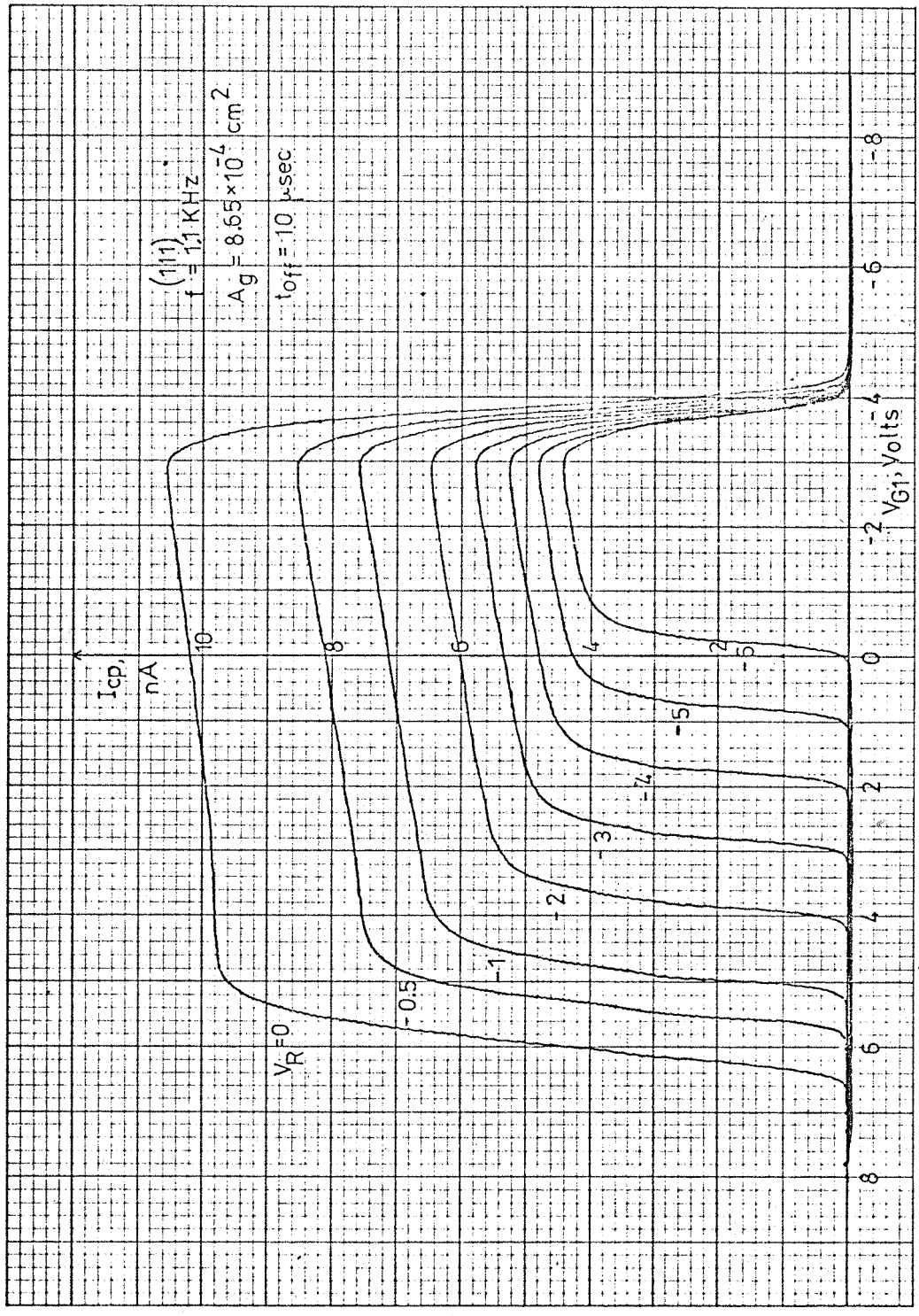
9270/1008

Fig. 3.15

Thus for values of t_{off} larger than $5L^2/D_p$ the 'geometric component' (explained in section 3a) should be eliminated. This can be seen from the graphs in Fig. 3.14 where for $t_{off} < 5L^2/D_p$ the I_{cp} rises rapidly and for $t \gg 5L^2/D_p$ there is little change since in this range the I_{cp} is due predominantly to trapped charge pumping.

Another factor affecting the 'geometric component' is the value of reverse bias V_R on the 'p^+n' junction. Thus experiments were performed on the same gated diode as before using a pulse with a value of t_{off} of 150μsec and f of 1.1KHz. The reverse bias on the diode was different for each experiment with a range of 0 to -6 volt These experimental curves are shown in Fig. 3.16. From these experiments the values of charge pumped current versus V_R were obtained for two values of V_{G1}, 0 and -2V, as shown in Fig. 3.17 and 3.18 respectively. From these figures it can be seen that for V_{G1} equal to 0V and V_R more negative than -6V the pulse base level is always above the turn on voltage V_T (V_R). The device therefore is never turned-on, consequently the charge pumped current is always zero, for these values of V_R and V_{G1}. But for V_{G1} equal to -2V and V_R equal to -6V the pulse base level is below the turn-on voltage and the charge pumped current is not zero. Also from these two sets of graphs it can be seen that when the reverse bias is more positive than -1V a 'geometric component' contributes to the charge pumped current. Since we are interested in the charge pumped current due to the trapped charge via the surface states the diode must be reversed biased to about -1V.

Using the results of these two experiments a further measurement was performed on gated diodes of different gate areas so as to check the relationship of charge pumped current first with gate area and second with frequency of the gate pulse. The reverse bias on the diode was -1V and the turn-off time of the gate pulse was 150μsec so that no 'geometric component' contributed to the charge pumped current. Two different frequencies of the gate pulse were used and the results are shown in Fig. 3.19. The gated diodes with different gate areas used for making these measurements were in the same chip so that the differences in the Icp are due to differences in gate area alone since the


Icp, nA
(111)
f = 1.1 KHz
Ag = 8.65×10⁻⁴ cm²
toff = 10 μsec
VR=0
0.5
1
2
3
4
5
6
8
10
VG1, Volts
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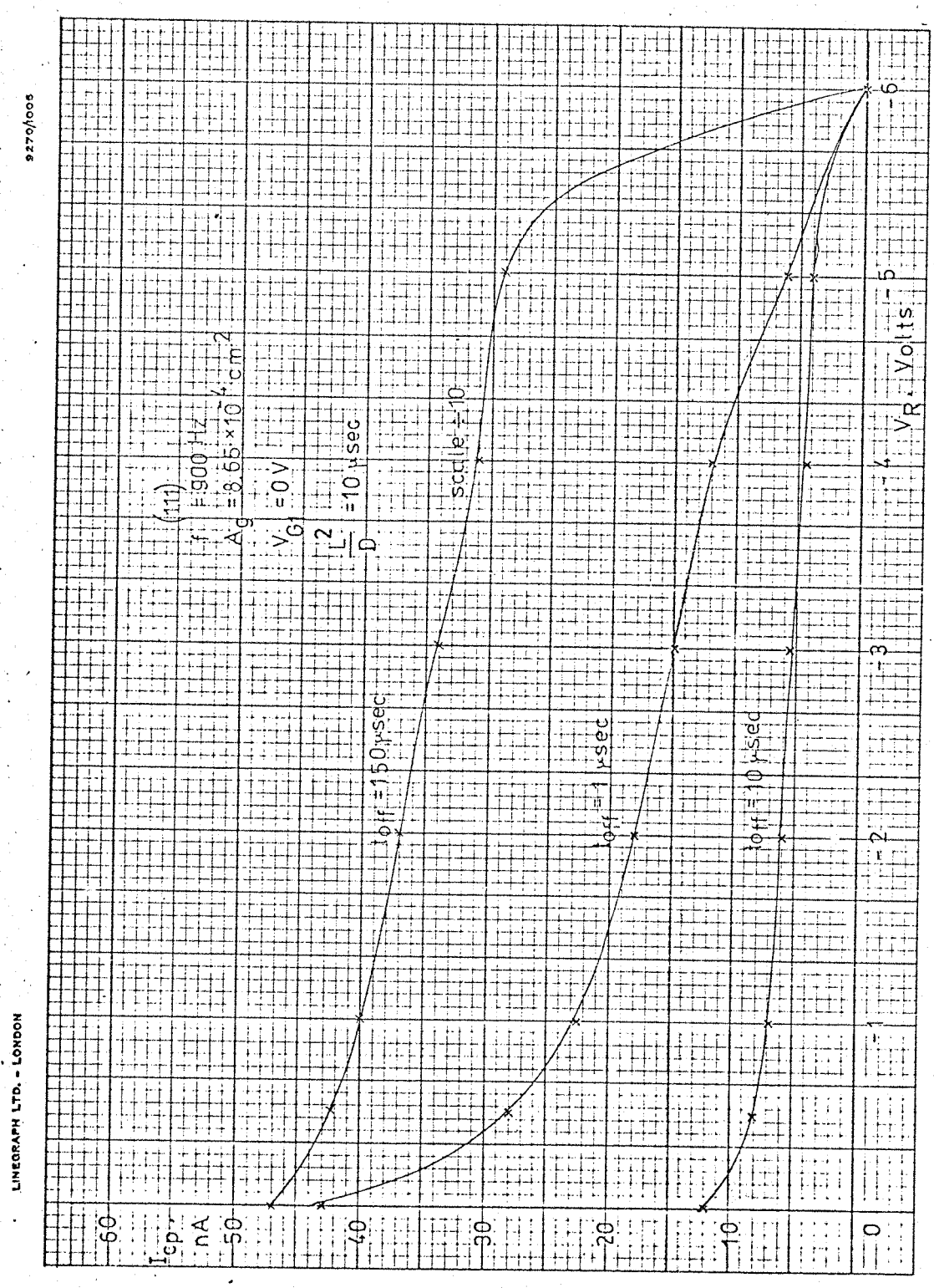
9270/1006

Fig. 3.16


9270/005
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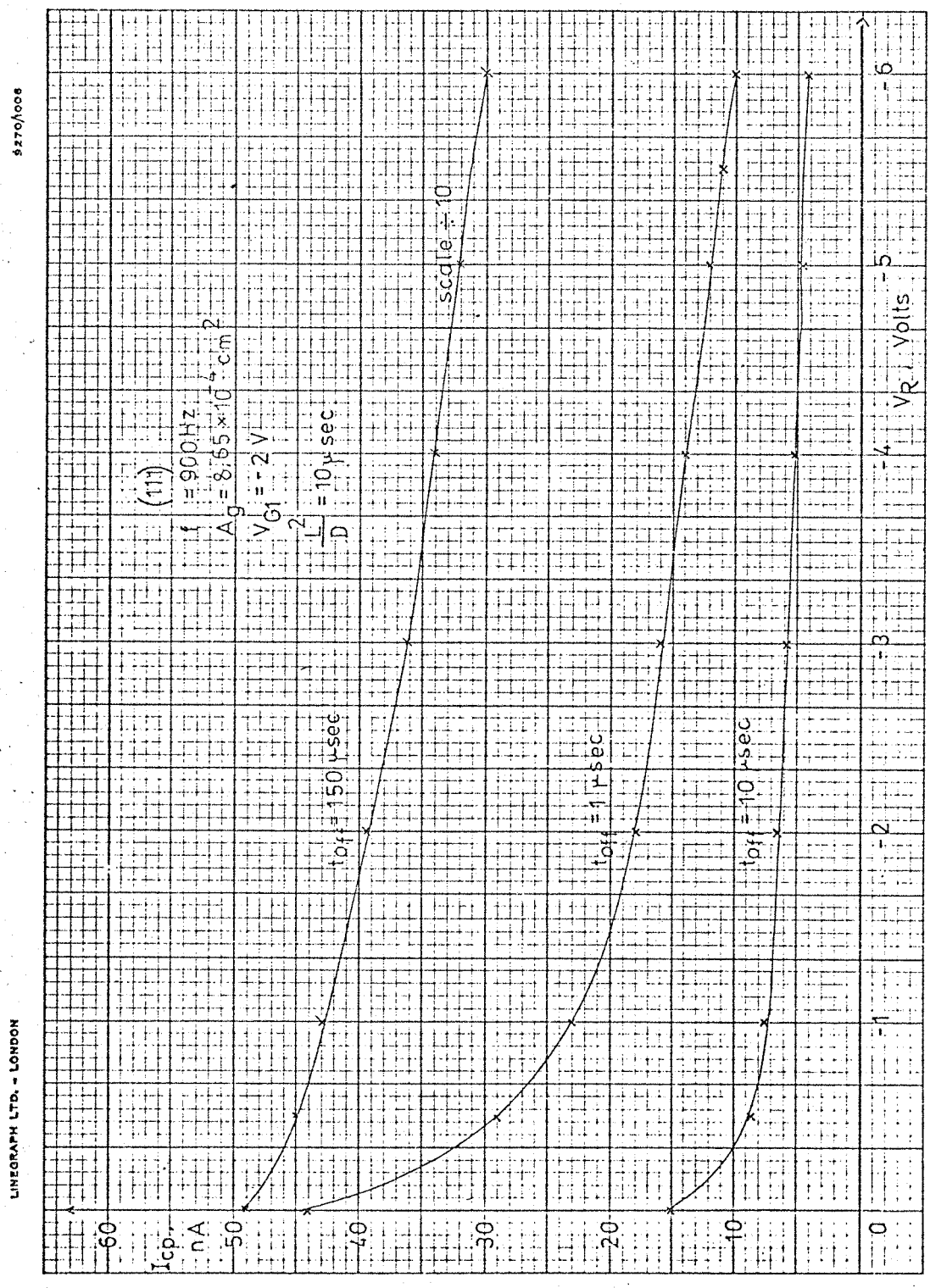
I_{cp} nA
60
50
40
30
20
10
0
-1
-2
-3
-4
-5
-6
V_R Volts
(111)
f = 900 Hz
A_g = 8.65×10⁻⁴ cm²
V_{G1} = 0 V
$\frac{L^2}{D}$ = 10 μsec
scale ÷ 10
t_{off} = 150 μsec
t_{off} = 1 μsec
t_{off} = 10 μsec

Fig. 3.18


(111)
f = 900Hz
A_g = 8.65 × 10⁻⁴ cm²
V_{G1} = - 2 V
$\frac{L^2}{D}$ = 10 μsec
scale ÷ 10
t_{off} = 150 μsec
t_{off} = 1 μsec
t_{off} = 10 μsec
I_{cp} nA
60
50
40
30
20
10
0
-1
-2
-3
-4
-5
-6
V_R Volts
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S270/1008

Fig. 3.18

value of N_{ss} should be closely matched. The value of each gate area was measured from photomicrographs as shown in plate 3. From Fig. 3.19 it can be seen that the charge pumped current is in fact directly proportional to the gate area.

To check the relationship between charge pumped current and the frequency of the gate pulse,measurements were made with the following conditions. The values of V_R, V_{G1}, t_{off} T_{OFF} and t_{on} were fixed at -1V, 0V, 150μsec, 60μsec and 15μsec respectively. The frequency was varied over the range shown in Fig. 3.20. As can be seen from the figure the value of Icp is not quite linearly dependent on pumping frequency at the higher end of the range for either of the two values of gate length shown. This experiment was therefore changed to the following conditions. The values of V_R, V_{G1}, t_{on}, T_{ON} and t_{off} were fixed at -1V, 0V, 15μsec, 60μsec and 150μsec respectively. For these conditions measurements over the range of frequencies shown in Fig. 3.21 gave an exactly linear dependence of Icp on pumping frequency. However, at the lower frequency end of the graphs for gate length the linear dependence fails. This was due to the gate pulse not being well defined at the low frequencies, by the pulse shaping circuit described before and shown in Fig. 3.4. For frequencies below about 100Hz the decay in the pulse shape was sufficient to bring the gate voltage V_{G1}, down to a negative value close to the value of the turn-on voltage at a V_R equal to -1V. Under this condition we would expect to lose the charge pumped current as already shown in 3.17 and 3.18. The value of the charge pumped current at the lower frequency end of Fig. 3.20 and 3.21 is close to the value of the leakage current due to generation in the depletion regions. Adding the value of the leakage current at 'zero' frequency to the values of Icp at the lower frequency range gave a good fit to the extrapolated values of Icp using the linear relationship. The difference between these last two graphs is that for Fig.3.20 3.20 it is the time for filling of the interface states which is varying with frequency . and for 3.21 the time for emptying is varying with frequency. These results confirm that the relationship expressed as equ. 3b.26 is valid for the appropriate condition

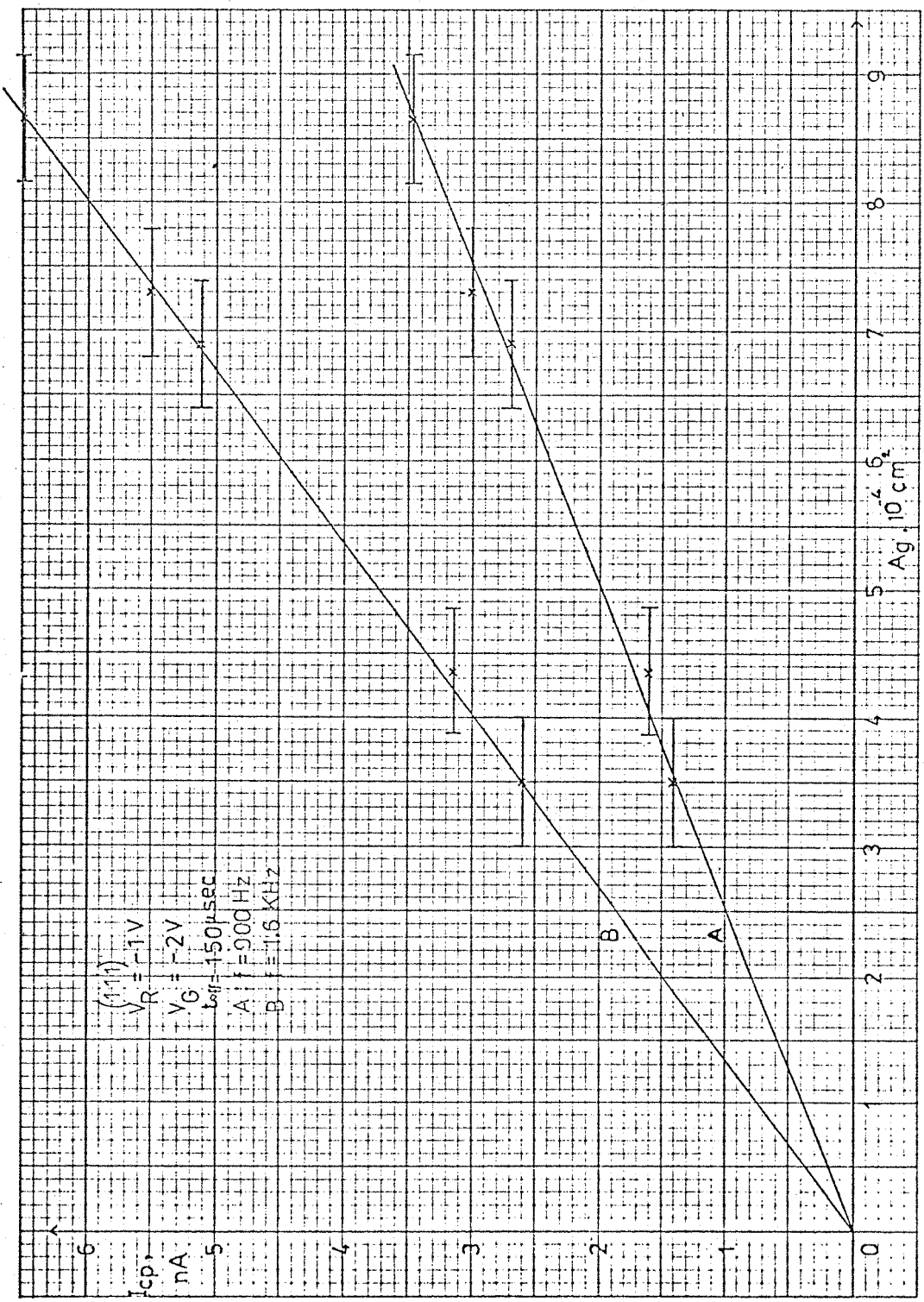
9270/1006
LINEGRAPH LTD. - LONDON
(111)
V_R = -1 V
V_G = -2 V
t_{off} = 150 μsec
A f = 900 Hz
B f = 1.6 KHz
Icp, nA
Ag, 10 cm
A
B

Fig. 3.19

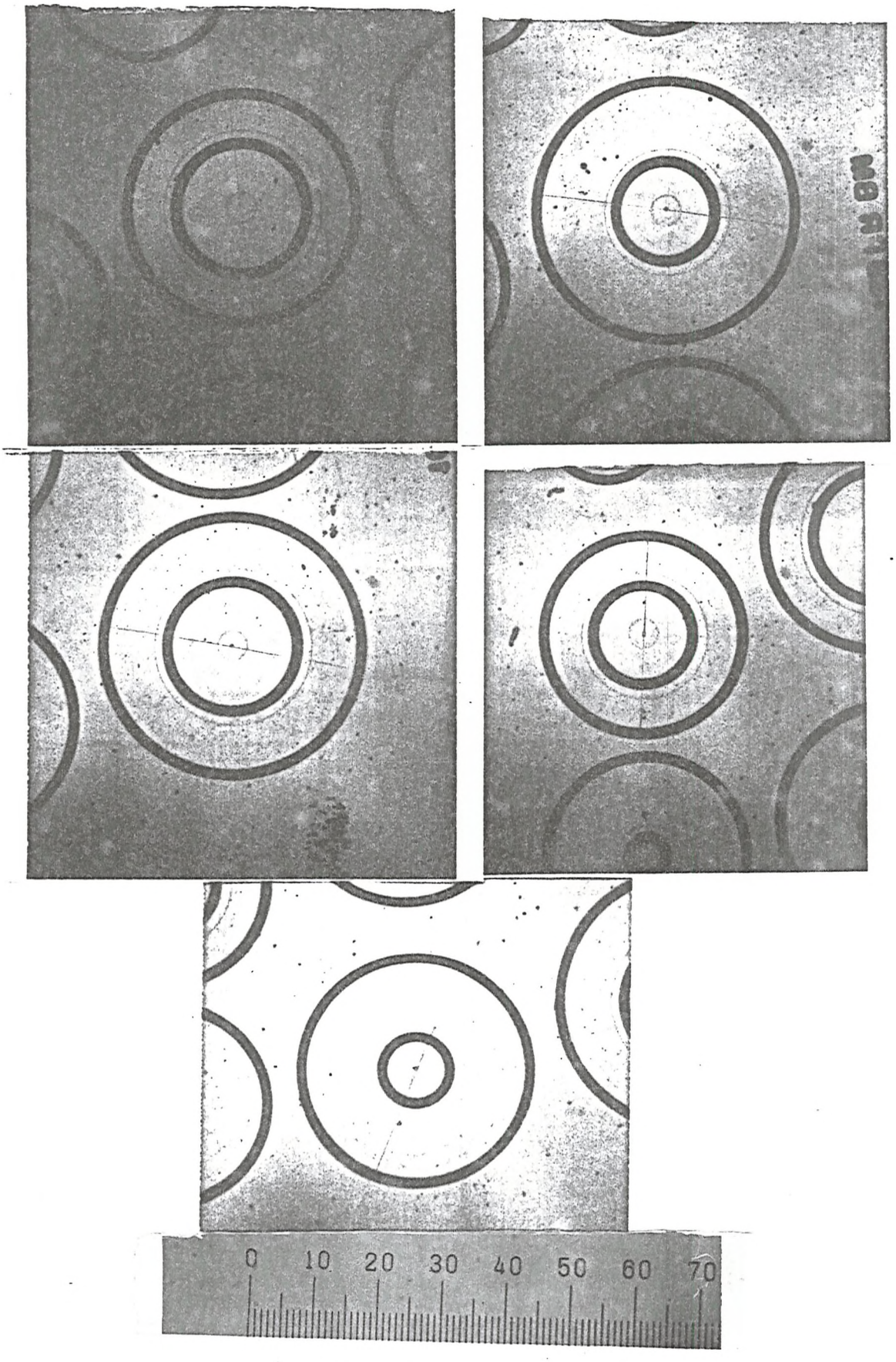

Plate 3

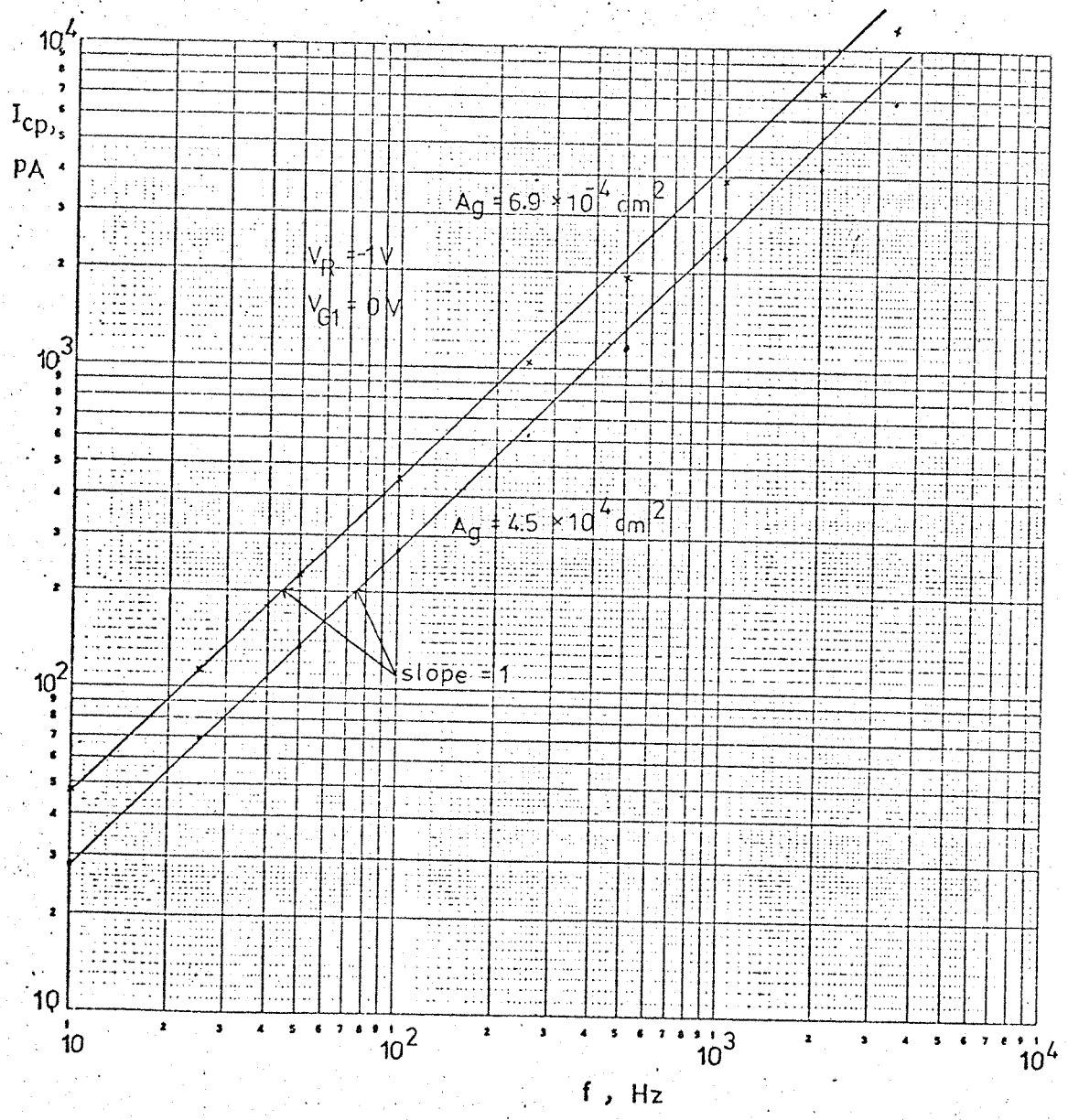
I_{cp}, pA
10^4
10^3
10^2
10
$A_g = 6.9 \times 10^{-4}$ dm^2
$V_{P2} = -1$ V
$V_{G1} = 0$ V
$A_g = 4.5 \times 10^{-4}$ dm^2
slope = 1
10
10^2
10^3
10^4
f , Hz

Fig. 3.20

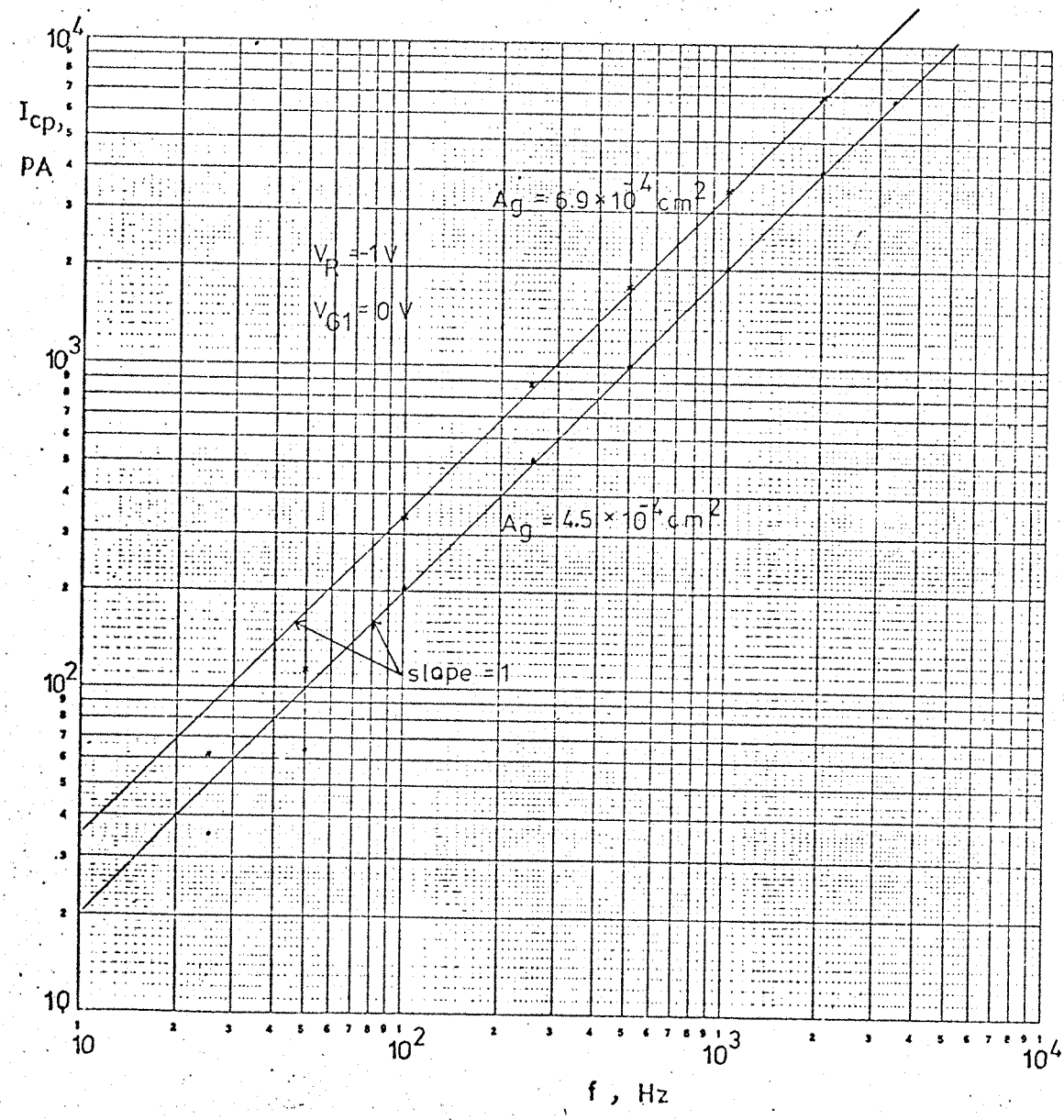
$I_{cp,s}$
PA
10^4
10^3
10^2
10
$A_g = 6.9 \times 10^{-4}$ cm^2
V_R = -1 V
V_{G1} = 0 V
$A_g = 4.5 \times 10^{-4}$ cm^2
slope = 1
10
10^2
10^3
10^4
f , Hz

Fig. 3.21

of measurements of I_{cp}.

A measurement of a gated diode was now made using the following conditions. The values of V_R, t_{off}, f, L, and gate area are -1V, 150μsec, 1.1kHz, 100μm and 8.65×15^4 cm^2 respectively. The graph of I_{cp} versus V_{G1} is shown in Fig. 3.22. An analysis of this graph was then performed to obtain a value for the energy distribution of N_{ss}. Firstly, the values of $\frac{dI_{cp}}{dV_{G1}}$ were obtained over the range of V_{G1} from (-1.3)V to (-0.2)V. This covers the range of interest as indicated by the theory and is more negative than the value of the flat-band voltage, V_{FB}. To find the flat band voltage a simple approximation was used as follows. The theoretical values for V_T (V_R) at V_R equals 0V and V_R equals -1V were computed using eq .3b.25 . The measured curves at the top of the rising portion for V_{G1} of positive value and the bottom of the falling portion for V_{G1} of negative value were compared with the theoretical value for V_T (V_R) enabling an estimate of the true value of V_{FB} to be made consistent with both ends of the graph, i.e.,

$$V_T\ (-1V) = (+4.5 - 10)V$$
$$= -5.5V \text{ , from the graph;}$$
$$V_T\ (0V) = -4.3V \text{ , from the graph}$$

Theory gives values for these turn-on voltages of

$$V_T\ (-1V) = -2.4V$$

and $V_T\ (0V) = -1.1V$, using equ. 3b.23.

Thus we estimate:

$$V_{FB} = (-4.3 + 1.1)V \text{ or } (-5.5 + 2.4)V$$
$$= -3.2V \text{ or } -3.1V$$

So, $V_{FB} \simeq -3.15V$

Values for $\frac{dV_{G1}}{d\psi_{s1}}$ were obtained from the theoretical plot of ψ_s versus V_G shown in Fig. 3.11 . Multiplying the values obtained for $\frac{dI_{cp}}{dV_{G1}}$ by the values for $\frac{dV_{G1}}{d\psi_{s1}}$ gives a set of values for

$$q\ Ag\ f\ N_{ss}(\psi_{s1}) .$$

The values for $N_{ss}\ (\psi_{s1})$ obtained in this manner are shown plotted as a function of energy in Fig. 3.23. The scan of energy is between

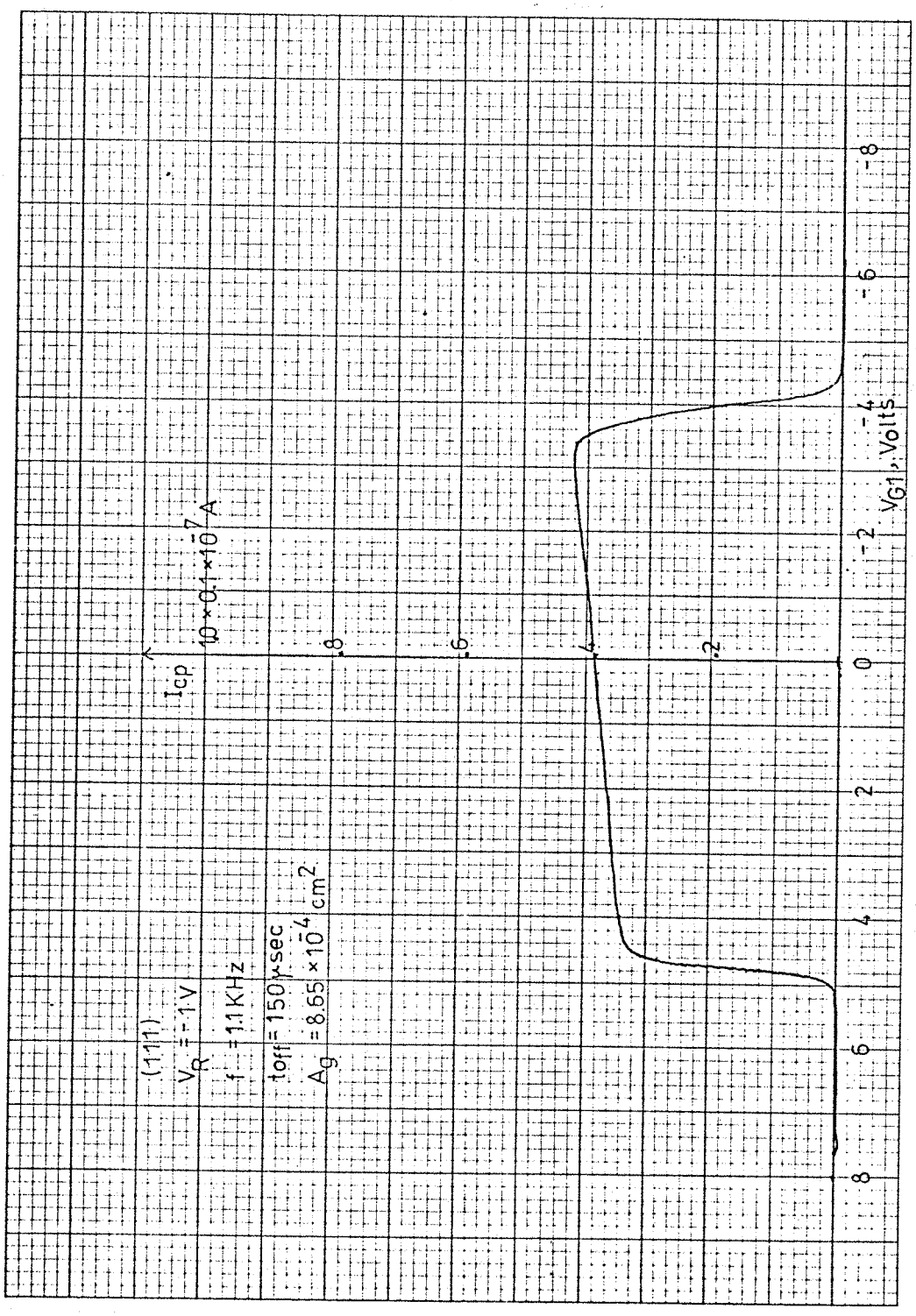
(111)
V_R = -1V
f = 1.1KHz
t_{off} = 150μsec
A_g = 8.65×10^{-4} cm^2
Icp
$10 \times 0.1 \times 10^{-7}$ A
.8
.6
.4
.2
0
-2
-4
-6
-8
2
4
6
8
V_{G1}, Volts
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Fig. 3.22

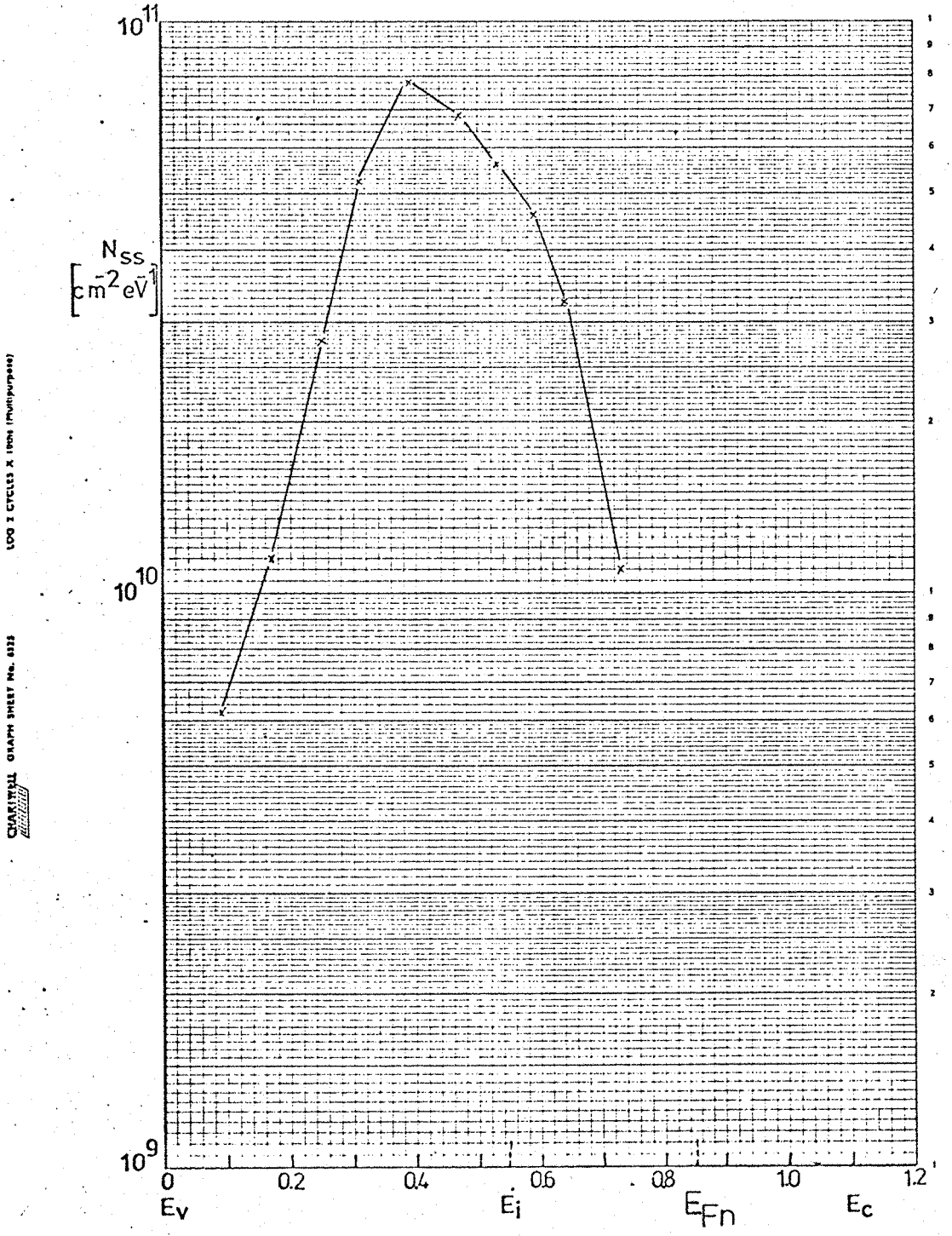
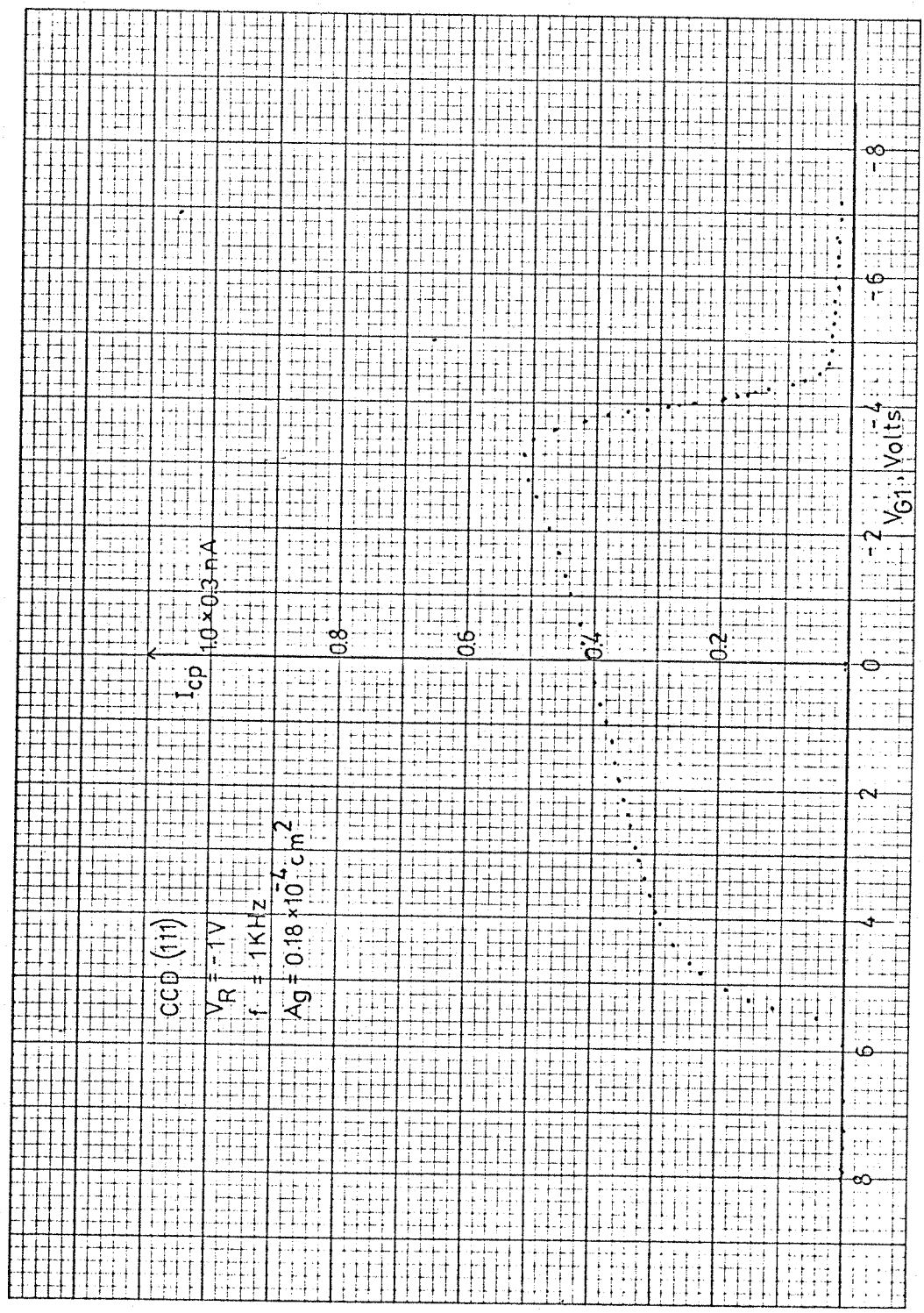


Fig. 3.23

E_{Fn} to E_V and this represents the total information which may be obtained rapidly by this technique. These interface states are the same ones responsible for the transfer inefficiency mechanism called Trapping Inefficiency in normal SCCD operation. The values of N_{ss} obtained from these charge pumped current measurements are in the range $1 \times 10^{10} cm^{-2} ev^{-1}$ to $10 \times 10^{10} cm^{-2} ev^{-1}$. The values of transfer inefficiency obtained on similar oxides used to fabricate CCD's on 111 material by Roberts, Singh and Lamb (23) in 1975 was, $\varepsilon \sim 10^{-2}$. Their estimate of the corresponding value of N_{ss} for those CCD's was $1 \times 10^{11} cm^{-2} ev^{-1}$. Evidently their estimate and these measurements are in close agreement. Measurements of a CCD of the same type used by Roberts et al, for transfer inefficiency meausrements on(111) orientation material, will be presented in Section 3d.

3d Charge Pumping Current Measurements on CCD's

These measurements were made using the same circuit as was described in Chapter 3, section 3c. The input gate and input diode of the CCD can be isolated from the main channel of the phase gates with respect to the substrate. The leakage current from the phase gates to the input structure is negligible for this example but may not be negligible in all cases. The phase gates ϕ_1, ϕ_2 and ϕ_3 were all connected directly to the substrate contact using the leads from the TO-5 package directly. Everything else was as before for the gated diode measurements. The CCD that was measured had a substate surface orientation in the (111) plane and 3-6Ω cm n-type resistivity. A measurement of charge pumped current versus gate voltage resting level was made. The rising edge of the response curve containing the information for the N_{ss} energy distribution as was explained in section 3a of chapter 3. This CCD input gate response is shown in Fig. 3.24. The Flat-band voltage was found by the same method as for the gated diodes described in section 3c and was equal to -3.6V. Equation 3b.37 was used for the analysis. Fig. 3.25 shows the surface state density N_{ss} energy distribution for this particular CCD.


CCD (111)
V_R = -1V
f = 1KHz
A_g = 0.18×10^{-4} cm^2
I_{cp}
1.0 x 0.3 nA
0.8
0.6
0.4
0.2
0
-2
-4
-6
-8
V_{G1}, Volts
8
6
4
2
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9270/1008

Fig. 3.24

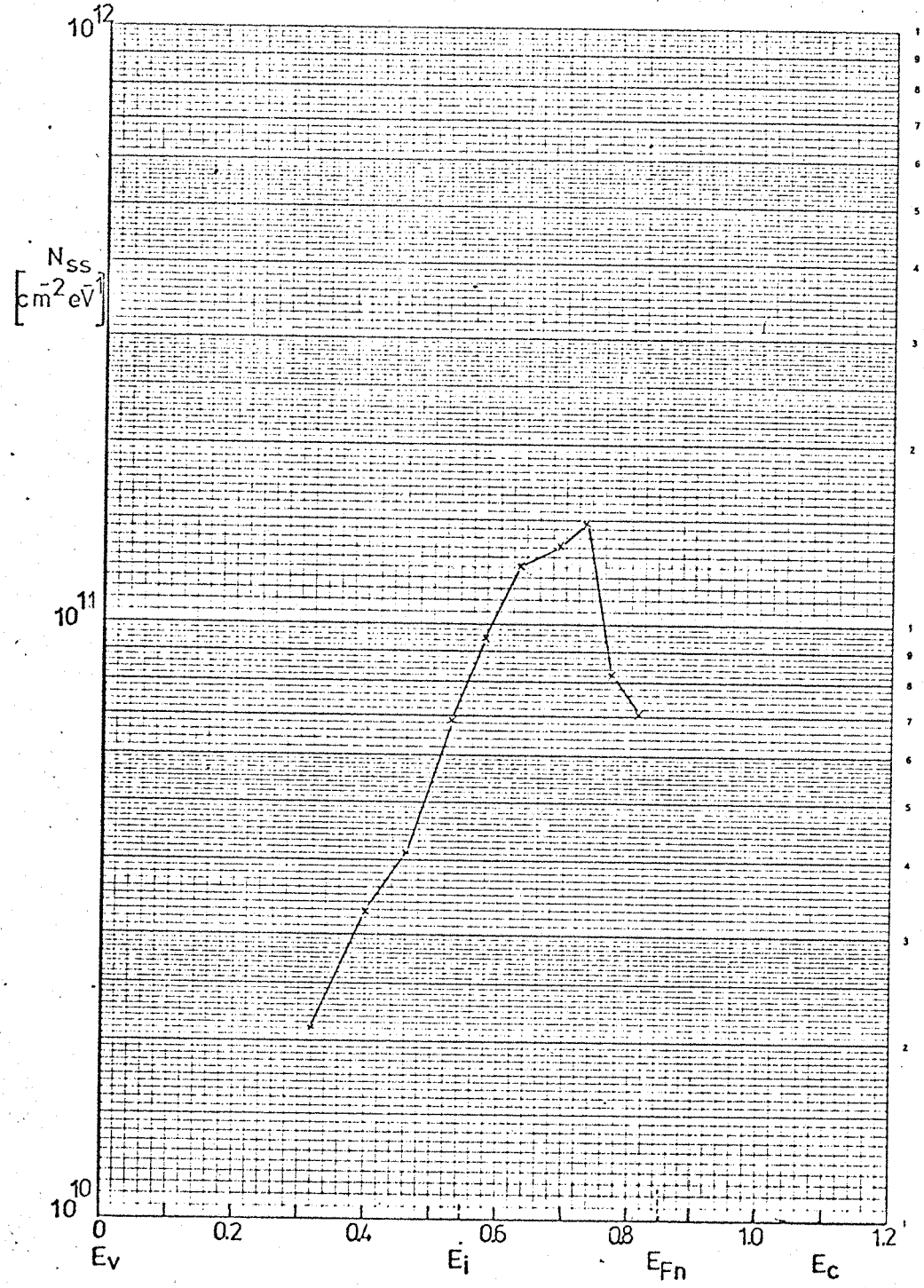


Fig. 3.25

4. LEAKAGE CURRENT AND CHARGE PUMPING CURRENT MEASUREMENTS ON DEVICES WITH TCE OXIDATION

4a Gated Diode Fabrication using TCE Oxidation

The process for producing gated p^+n diodes with TCE oxidation includes all the steps that were extensively described in section 2b of chapter 2 except for the gate oxidation stage. Instead the devices were subjected to TCE gate oxidation. There were two sets of slices, produced with exactly the same processing steps but on different days. Each set contains three types of gated diode with a variation in the process described below.

1. No gettering step apart from the TCE oxidation.
2. A gettering step (as described in stage 7 in section 2b) performed before the TCE oxidation for the gate oxide.
3. A gettering step (as above) performed after the TCE oxidation for the gate oxide.

The slices were first prepared for the oxidation step at the Microelectronics Lab. at the University of Southampton. Then they were sent to the Katholieke Universiteit Leuven, Belgium were the TCE gate oxidation was performed by G.J.Decklerk at the Lab. Fysicaen Electronica van de Halfgeleiders, of that University. This step is shown in Fig. 4.1. The slices were then returned for completion in the Microelectronics Lab at the University of Southampton where subsequently they were tested. The material that was used was again n-type substrate (111) orientation with 3-6Ωcm resistivity. The "RCA clean" was used for these devices (see Fig. 4.2).

4b. Leakage Current Measurements on TCE Gated Diodes

These measurements were made using the same apparatus described in section 2c of Chapter 2. Transfer characteristics similar to those shown in Fig. 4.3 were obtained, taken from several devices from the same slice. These transfer characteristics have been plotted on the same axis to enable an estimate of the spread of values of leakage currents in the three regions (depletion accumulation and inversion). From these transfer characteristics the values for I_{MJ}, I_{FIJ}, I_s were obtained with the same method as was described in section 2c. Using equation 2c.1, 2c.2, 2c.3 the values for τ_{OMJ}, τ_{oFIJ} and S_o were obtained. These values for the two sets of slices are shown in table 1a for the first set and table 1b for the second set.

TCE GATE OXIDE

Slices cleaned by "RCA clean" (see Fig. 4.2),
Oxidised at 1050^{0}C in dry oxygen with TCE equivalent to 0.6% Molar ratio of HCl for 100 mins.
This is followed by an anneal in dry nitrogen at 1050^{0}C (i.e., in the same furnace) for 20 mins.

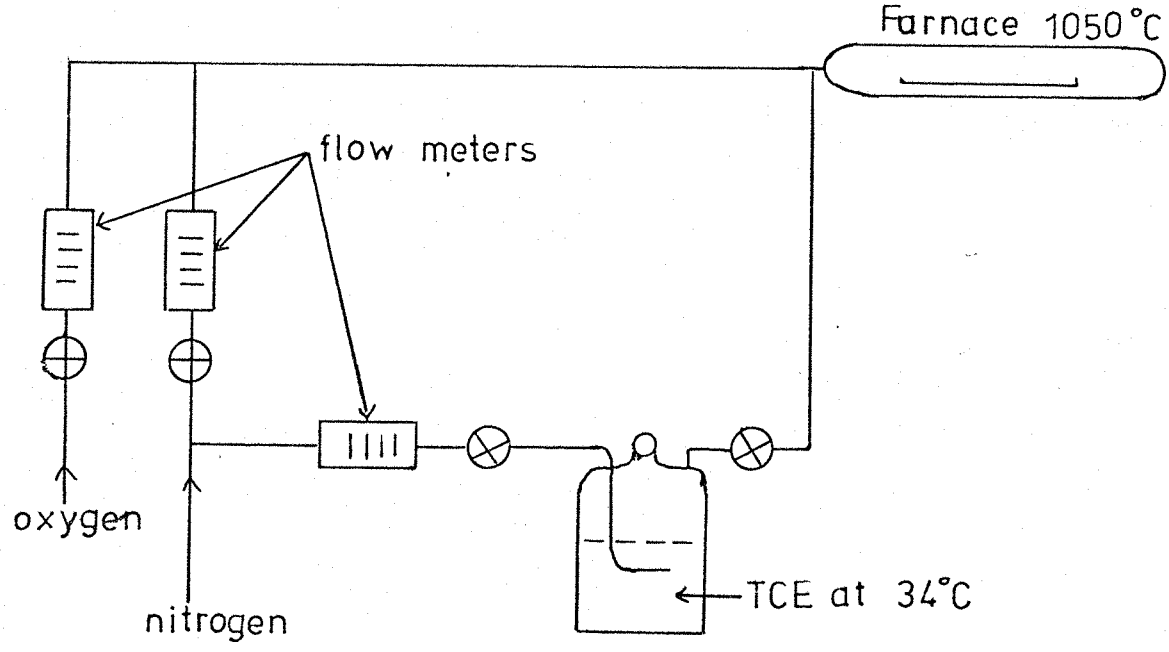


Fig. 4.1

R.C.A. Clean (12)

(i) Initial Clean

Plastic beakers will be provided with markings on them which indicate the amounts of the chemicals to be mixed up for each clean. The blue markings refer to the first solution and the red markings refer to the second solution.

N.B. The clean specifies boiling for 10 minutes. This 10 minute period is in addition to the time necessary for the solution to reach boiling point.

A rinse is defined as filling the beaker completely with double distilled water (d.d. water) and then emptying it all out. Care must be taken not to allow anything other than d.d. water to contact the slice (i.e., the tap, tap water, etc.).

A wash is defined as at least 15 minutes washing in the recirculating deionized water system (ρ >2 MΩcm).

1. Inspect slices visually (in laminar flow cabinet) for chips and scratches - reject slice if there are any major imperfections.
2. Place slices into a quartz holders and beaker and rinse two or three times to remove surface dust.
3. Make up first cleaning solution: d.d. water + ammonia solution + hydrogen peroxide in volume ratios 5:1:1 (blue markings).
4. Pour solution onto slices and boil for 10 minutes.
5. Rinse slices carefully 10 times.
6. Dip-etch the slices in buffered HF until hydrophobic (ie. until liquid runs off surface - about 5 seconds).
7. Rinse slices carefully 10 times.
8. Make up second cleaning solution: d.d. water + hydrochloric acid + hydrogen peroxide in volume ratios 6:1:1 (red markings).
9. Pour onto slices and boil for 10 minutes.
10. Rinse slices carefully 5 times.
11. Wash in recirculating deionized water for at least 15 minutes (and until ρ>2MΩ.cm).
12. Spin slices dry and transfer to furnace immediately in a Fluoroware tray.

(ii) Clean after stripping resist

Resist should be stripped in the normal way (fuming nitric etc.) and the cleaning procedure described above should be carried out excluding steps 6 and 7.

1. All handling during processing to be done on the edges of slices only and with plastic tweezers only. (The only exception is handling during photomech., stages).
2. The slices must always be transported in covered Fluoroware trays. The covers should only be removed from the Fluoroware trays in laminar flow cabinets or when the slices are being loaded into or removed from a furnace.
3. After cleaning a slice prior to a furnace treatment, the delay between spinning dry and loading into the furnace should be as short as possible. If a delay between cleaning and furnacing is necessary, the slices should be stored in the recirculating deoinized water system rather than in a Fluoroware tray.
4. Only quartz slice holders and beakers to be used.

Fig. 4.2

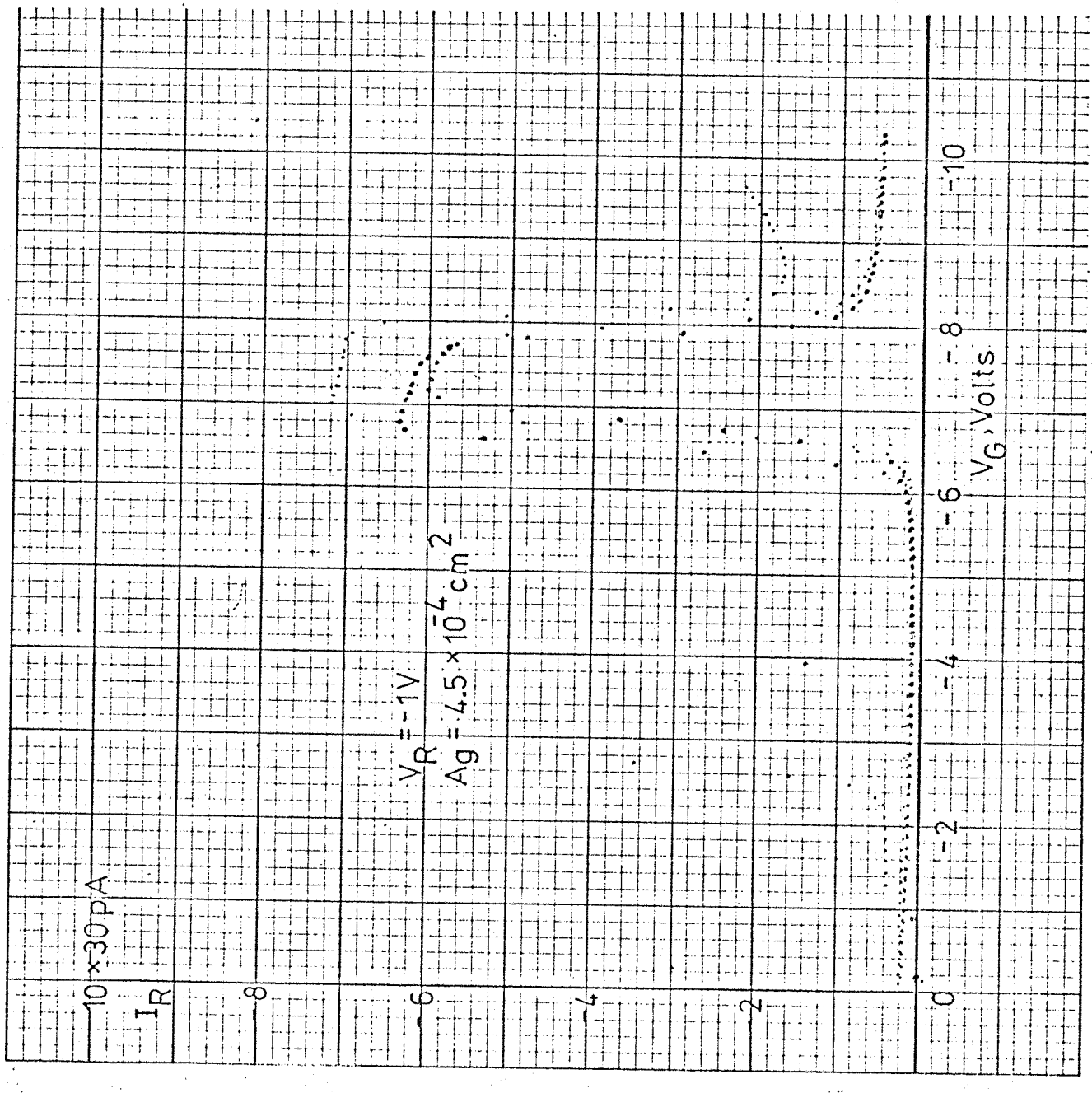


Fig. 4.3

TABLE 1

(a)

	Gate Oxide with TCE		
	Process 1 only TCE-oxidation	Process 2 Phosphorous gettered before TCE-oxidation	Process 3 Phosphorous gettered after TCE-oxidation
Bulk lifetime in depleted volume of the p-n junction τ_{oMJ}	11.8 μsec	11.8 μsec	17.6 μsec
Bulk lifetime in depleted volume under the gate τ_{oFIJ}	2.6 μsec	9.2 μsec	2.16 μsec
Surface recombination velocity in depleted surface S_o	340 $\frac{cm}{sec}$	40.2 μsec	39.5 μsec

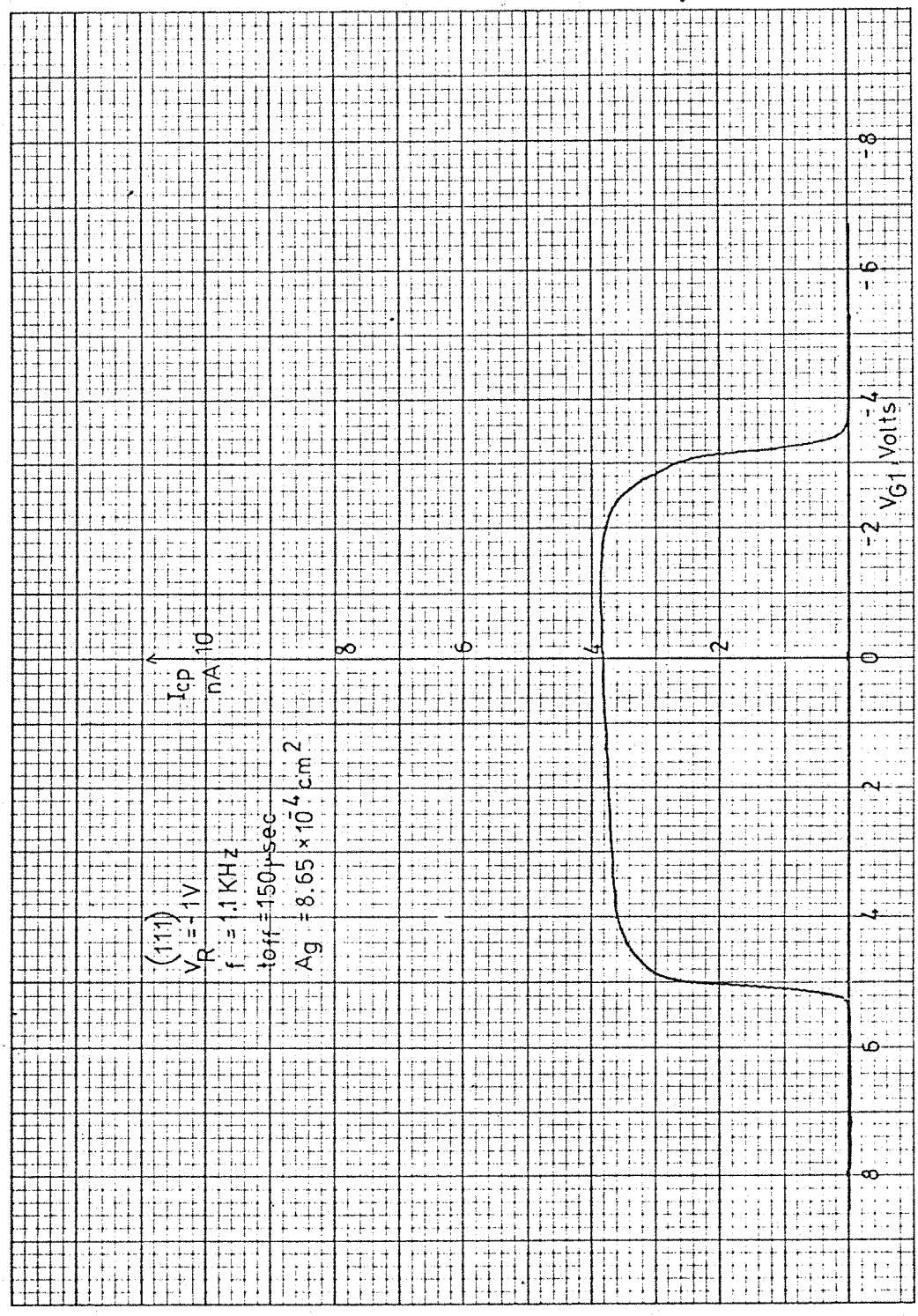
(b)

	Gate Oxide with TCE		
	Process 1 only TCE-oxidation	Process 2 Phosphorous gettered before TCE-oxidation	Process 3 Phosphorous gettered after TCE-oxidation
Bulk lifetime in depleted volume of the p-n junction τ_{oMJ}	3.5 μsec	8.8 μsec	35.2 μsec
Bulk lifetime in depleted volume under the gate τ_{oFIJ}	0.4 μsec	2.46 μsec	12.3 μsec
Surface recombination velocity in depleted surface S_o	454 $\frac{cm}{sec}$	2.27 μsec	7.9 μsec

4c Charge Pumped Current Measurements on'TCE' gated diodes

Using the apparatus described in section 3b the charge pumped current, Icp, versus gate voltage resting level was obtained from a gated diode with a TCE gate oxide. The obtained response is shown in Fig. 4.4. From this current the Flat-band voltage was calculated in the same way as for the 'HCl' gated diodes described in section 3d of Chapter 3 and it was found to be -2.5 volts. The rising edge of the response was then analysed to find the energy distribution of N_{ss} for this particular device, in a range of energy over the band-gap.

The analysis was done using equation 3b.27 in the same way as for the CCD and 'HCl' gated diodes. The result of this analysis is shown in Fig. 4.5.


(111)
V_R = -1V
f = 1.1 KHz
toff = 150 μsec
Ag = 8.65 × 10⁻⁴ cm²
I_{cp} nA
10
8
6
4
2
0
-2
-4
-6
-8
V_{G1} Volts
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9270/1006

Fig. 4.4

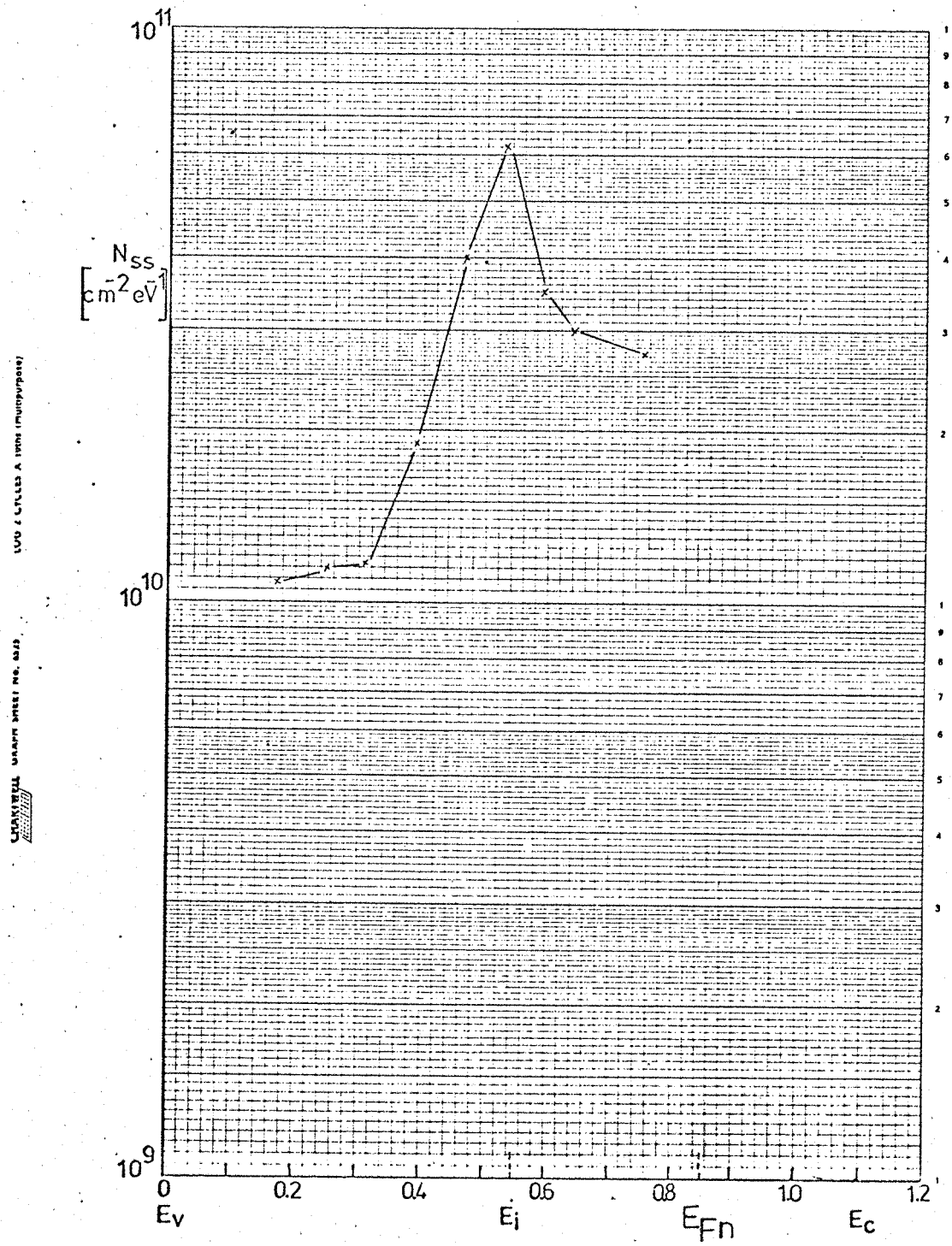

Fig. 45

4d Comparison of results of 'TCE' devices with results on 'HCl' devices

The values of generation lifetime of the carriers, from the metallurgical junction depletion region are in the range of 5 to 40μsec for the three types of gated diodes with HCl oxidation. A range of 3 to 35μsec was obtained for the same types of gated diodes with TCE gate oxidation.

The values of generation lifetime of the carriers in the field induced junction depletion region are in the range 4 to 20μsec for the three types of gated diodes with 'HCl' gate oxidation. For the same three types of gated diodes with TCE oxidation the range is 0.5μsec to 13μsec. So the values of τ_{oFIJ} for 'TCE' devices are slightly worse than those for the 'HCl' devices.

The values of surface recombination velocity for those gated diodes with HCl oxidation are in the range 3 to 11 cm/sec. For TCE oxidation (very high values) the values of surface recombination velocity are in the range 8 to 450 cm/sec. These latter values are much higher than those for the HCl oxides.

As an overall comparison it seems that TCE oxide treatment is if anything slightly worse than the HCl oxide treatment for these particular devices.

This result shows that there is another riding controlling factor in the processing schedule which results in moderate to poor values of bulk lifetime and surface recombination velocity. Work is proceeding by T.F. Unter (12) in the microelectronics group which shows that the initial oxidation process used for our devices usually produces severe extrinsic stacking fault crystallographic damage at the surface region of the device.

This we believe is the mechanism controlling the values of τ_{oFIJ}, τ_{oMJ}, S_o found in the measurements presented in this present work.

5. CONCLUSIONS

5a Comparison of the effects of different processing schedules

The values of bulk lifetimes and surface recombination velocities of n-type gated diodes with different HCl % (by volume) in the gate oxidation and different ways of processing were presented in section 2b of Chapter 2. Also the same values for gated diodes with TCE gate oxidation were presented. The results show improvement with these different processes. There must be another overriding factor and that is probably the way the initial oxidation was performed. This initial oxidation produces many shocking faults which can be the dominant cause of the leakage current. Recent experiments have shown lifetime measured by the pulsed capacitance technique on MOS structures is dominated by oxidation induced stacking faults. It is probably that the results presented here are similarly dominated by stacking faults introduced during the initial oxidation and gate oxidation processes. The same experiments must be repeated using a better initial oxidation process.

5b Usefulness of the Charge Pumping measurement technique as related to packaged CCD's.

An attempt has been made in Chapter 3 to establish a technique to obtain the surface state density energy distribution in gated diodes. With this method the only experimental data necessary is the charge pumped current versus gate voltage resting level. It is also necessary to know the gate oxide thickness, gate area, gate length and substrate doping level (assumed to be uniform) of the measured device. From the results obtained we conclude that the peak in the curve of N_{ss} versus energy is not at the present thought to be reliable since this has not been observed by any of the other techniques. These other techniques suggest the opposite behaviour for N_{ss}. The final assumption for the differential form of the charge pumped current equation, may be inaccurate. However, it was demonstrated here that the current has the correct dependence on the parameter of the simple form of the charge pumping equation. So the result for a spot measurement of Icp at values of V_{G1}, V_{G2} and V_R is useful in obtaining an estimate of the average value of N_{ss}. This

measurement technique can now be applied to automatic data logging systems to obtain, rapidly, a picture of the distribution of N_{ss} over an entire wafer of CCD's. Therefore an on-line technique has been established for predicting the performance of CCD's, without the need to measure the actual performance.

In order, though, to obtain an accurate N_{ss} distribution over an energy interval appropriate to CCD transfer inefficiency measurements, more theoretical analysis of the problem must be done. Also there seems to be a possibility of obtaining some further information on the capture cross-section from the transient behaviour of charge pumped current but this requires further work to establish the method. Leakage current data might give a correlation through the value of surface recombination velocity and therefore give another estimate of the cross-section of the mid-band interface states.

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