AN INVESTIGATION OF GROUP IV ALLOYS AND THEIR APPLICATIONS IN BIPOLAR TRANSISTORS

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ABSTRACT

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This thesis investigates the use of carbon in group IV alloys and their potential uses in bipolar transistors. The first part of the thesis investigates the ability of carbon to suppress transient enhanced diffusion in SiGe heterojunction bipolar transistors, whilst the second part deals with the impact of carbon incorporation on the electrical properties of polycrystalline silicon and silicon-germanium films.

A background doping concentration ($10^{20}cm^{-3}$) of C has been introduced into the base of SiGe HBTs with the aim of studying the effects of C on TED of B from the base. An electrical method is used to extract the bandgap narrowing in the base of SiGe and SiGe:C HBTs through measurements of the temperature dependence of I_c at different C/B reverse biases. The method is very sensitive to small amounts of dopant out-diffusion from the base and hence is ideal for determining the effect of C on TED. Extracted BGN values of 115meV and 173meV were obtained for the SiGe and SiGe:C HBTs respectively, for a C/B reverse bias of 0V. Increasing the C/B reverse bias to 1V increased the extracted BGN of the SiGe HBT to 145meV, but left the SiGe:C value unchanged. This demonstrates that no parasitic energy barrier exists in the SiGe:C HBT and that TED has been suppressed.

The effect of carbon position and concentration has been studied by introducing a peak C concentration of $10^{20}cm^{-3}$ in the collector and $1.1 \times 10^{19}cm^{-3}$ or $1.5 \times 10^{19}cm^{-3}$ C in the base. From these measurements it has been shown that TED is only suppressed in the device with $1.5 \times 10^{19}cm^{-3}$ C in the base, indicating that a C concentration of $1.5 \times 10^{19}cm^{-3}$ is needed to suppress TED and that the C needs to be co-located with the B profile.

The effects of carbon on the electrical properties of polycrystalline Si and SiGe films have been investigated. The resistivity, Hall mobility (μ_H) and effective carrier concentration (N_{EFF}) of n- and p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers have been measured for carbon contents between 0% and 8%. For the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the addition of small amounts of C ($\leq 0.9\%$) was found to severely increase the resistivity of the layers, caused by a drop in N_{EFF} and μ_H. In contrast, for the p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the effect of C on the resistivity was much less dramatic for C concentrations up to 7.8%. Measurements of the grain boundary energy barriers for the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, extracted from the temperature dependence of the resistivity, showed that there was a square law dependence on carbon content. This is consistent with carbon increasing the grain boundary trap density. In contrast, the grain boundary energy barriers in the p-type poly$Si_{1-y}C_y$ layers exhibited a linear dependence on carbon content. This behaviour of C in p-type layers has been attributed to a shift in the dominant trap energy level towards the valence band at high C concentrations.

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List of Acronyms

at.%	-	atomic percent
BGN	-	bandgap narrowing
BHF	-	buffered Hydrofluoric acid
BJT	-	bipolar junction transistor
C/B	-	collector-base
CB	-	Carbon in the base
CC	-	Carbon in the collector
CMOS	-	complimentary metal oxide semiconductor
CVD	-	chemical vapour deposition
DLTS	-	deep level transient spectroscopy
DOS	-	density of states
E/B	-	emitter-base
FHWM	-	full-half width maximum
FTIR	-	Fourier transform infra-red
HBT	-	heterojunction bipolar transistor
HCB	-	High Carbon in the base
HF	-	Hydrofluoric acid
IHP	-	Institut fur Halbleiterphysik
LDE	-	low doped emitter
LPCVD	-	low pressure chemical vapour deposition
LTO	-	low temperature oxide
MBE	-	molecular beam epitaxy
MEMS	-	microelectro - mechanical systems
MFC	-	mass flow controller
MOS	-	metal oxide semiconductor
NC	-	No Carbon
PL	-	photoluminescence
polySi	-	polycrystalline silicon
poly$Si_{1-x}Ge_x$	-	polycrystalline silicon-germanium

poly$Si_{1-y}C_y$	-	polycrystalline silicon-carbon
poly$Si_{1-x-y}Ge_xC_y$	-	polycrystalline silicon-germanium-carbon
RBS	-	Rutherford back scattering
RTA	-	rapid thermal annealing
RTCVD	-	rapid thermal chemical vapour deposition
sccm	-	standard cubic centimetre per minute
SEM	-	scanning electron microscopy
SIMS	-	secondary ion mass spectroscopy
SIS	-	semiconductor-insulator-semiconductor
SPC	-	solid phase recrystallisation
SPE	-	solid phase epitaxy
SUMEC	-	Southampton University Micro-electronics Centre
TED	-	transient enhanced diffusion
TEM	-	transmission electron microscopy
TFT	-	thin film transistor
UHV/CVD	-	ultra high vacuum chemical vapour deposition
uv	-	ultraviolet
VLSI	-	very large scale integration
XTEM	-	x-ray transmission electron microscopy

List of Symbols

a_C	-	Lattice parameter of carbon
a_{Ge}	-	Lattice parameter of germanium
a_{Si}	-	Lattice parameter of silicon
a_{SiGe}	-	Lattice parameter of silicon-germanium
a_{SiGeC}	-	Lattice parameter of silicon-germanium-carbon
A	-	Area of device
B	-	Magnetic field applied to van der Pauw structures
C	-	Constant taking into account differences in Si and SiGe density of states and minority mobilities
C_a	-	Number of atoms per unit volume
C_g	-	Reactant species in the gas stream
$D_{nb(SiGe)}$	-	Electron diffusion coefficient in the silicon-germanium base
D_{pe}	-	Hole diffusion coefficient in the emitter
E_a	-	PolySi resistivity activation energy
E_B	-	Grain boundary energy barrier
E_C	-	Conduction band energy
E_F	-	Fermi level
E_{Fn}	-	Fermi level in n-type polySi
E_{Fp}	-	Fermi level in p-type polySi
E_H	-	Hall electric field
E_i	-	Intrinsic Fermi level
E_V	-	Valence band energy
$E_{g(Si)}$	-	Silicon bandgap
$E_{g(Si)}(T)$	-	Silicon bandgap, as a function of temperature
$E_{g(SiGe)}$	-	Silicon-germanium bandgap
E_T	-	PolySi grain boundary trap energy
f_T	-	Unity gain frequency
F	-	Steady state flux
F_1	-	Flux arriving at the semiconductor interface

F_2	-	Flux consumed at the semiconductor interface
$F_{\frac{1}{2}}$	-	Fermi-Dirac integral
G_B	-	Base Gummel number
h	-	Planck's constant
h_g	-	Vapour phase mass transfer coefficient
I	-	Applied current to van der Pauw structures
I_B	-	Base current
$I_C]$	-	Collector current
$I_{B(Si)}$	-	Base current of a silicon bipolar transistor
$I_{C(Si)}$	-	Collector current of a silicon bipolar transistor
$I_{C(SiGe)}$	-	Collector current of a silicon-germanuium bipolar transistor
I_{rg}	-	Depletion region recombination current
J	-	PolySi current density
J_C	-	Collector current density
$J_{C(Si)}(T)$	-	Collector current density in a silicon BJT, as a function of temperature
$J_{C(SiGe)}(T)$	-	Collector current density in a silicon-germanium HBT, as a function of temperature
$J_0(T)$	-	Silicon BJT saturation current density, as a function of temperature
$J_{0(ideal)}(T)$	-	Silicon BJT saturation current density assuming ideality of 1, as a function of temperature
$J_{0(non-ideal)}(T)$	-	Silicon BJT saturation current density assuming ideality is not 1, as a function of temperature
J_{oc}	-	Collector saturation current density
k	-	Boltzmann's constant
k_s	-	Surface reaction rate constant
L	-	PolySi grain size
L_{nb}	-	Electron diffusion length in the base
L_{pe}	-	Hole diffusion length in the emitter
m_n	-	Effective mass of an electron
m_o	-	Rest mass of a free electron
m_p	-	Effective mass of a hole
n	-	Electron concentration
n_c	-	Ideality factor
$n_i(x)$	-	Position dependent intrinsic carrier concentration
n_{io}	-	Equilibrium intrinsic carrier concentration
n_{ibo}	-	Equilibrium intrinsic carrier concentration in the base
$n_{ibo(Si)}(T)$	-	Equilibrium intrinsic carrier concentration in a silicon base,

		as a function of temperature
$n_{ibo(SiGe)}$	-	Equilibrium intrinsic carrier concentration in a SiGe base
$n_{ibo(SiGe)}(T)$	-	Equilibrium intrinsic carrier concentration in a SiGe base, as a function of temperature
n_{ieff}	-	Effectice intrinsic carrier concentration due to heavy doping
$n_{ieff}(T)$	-	Effectice intrinsic carrier concentration due to heavy doping, as a function of temperature
n_{ieo}	-	Equilibrium intrinsic carrier concentration in the emitter
N	-	PolySi doping level
N^*	-	PolySi critical dopant concentration
N_a	-	Doping level in the semiconductor for Klaassen BGN eq.
N_{ab}	-	Acceptor concentration in the base
$N_{ab}(T)$	-	Acceptor concentration in the base, as a function of temperature
$N_{ab}(x)$	-	Position dependent acceptor concentration
$(N_C N_V)_{Si}$	-	Density of states product for silicon
$(N_C N_V)_{Si}(T)$	-	Density of states product for silicon, as a function of temperature
$(N_C N_V)_{SiGe}$	-	Density of states product for silicon-germanium
$(N_C N_V)_{SiGe}(T)$	-	Density of states product for silicon-germanium, as a function of temperature
N_{de}	-	Donor concentration in the emitter
N_T	-	PolySi grain boundary trap density
$N_{T(Si_{1-y}C_y)}$	-	PolySi$_{1-y}$C$_y$ grain boundary trap density
$N_{T(Si_{0.82-y}Ge_{0.18}C_y)}$	-	PolySi$_{0.82-y}$Ge$_{0.18}$C$_y$ grain boundary trap density
p	-	Hole concentration
q	-	Charge on an electron
r	-	Growth rate
$R_B(T)$	-	Base sheet resistance
R_H	-	Hall coefficient
T	-	Temperature
v_c	-	Collection velocity
V	-	Measured voltage on van der Pauw structures
V_B	-	Grain boundary potential barrier
V_{BE}	-	Base-emitter bias voltage
V_G	-	Applied voltage across a single grain in polySi
W_B	-	Width of the base
$W_B(T)$	-	Width of the base, as a function of temperature
W_E	-	Wwidth of the emitter

x	-	Germanium mole fraction
x_d	-	Grain boundary depletion region
y	-	Carbon mole fraction
β_{MAX}	-	Maximum forward current gain
ΔE^*	-	Parasitic energy barrier height
ΔE^{FD}	-	Fermi-Dirac correction to heavy doping bandgap narrowing
ΔE_C	-	Bandgap discontinuity in the conduction band
ΔE_G	-	Bandgap narrowing due to germanium
ΔE_{GB}	-	Bandgap narrowing due to heavy doping effects
ΔE_{GB}^{app}	-	Apparent bandgap narrowing due to heavy doping effects
$\Delta E_{gGe}(0)$	-	Ge bandgap narrowing at the emitter junction
$\Delta E_{gGE}(Grade)$	-	Germanium grading within the base, difference between the Ge bandgap narrowing at the emitter and collector junctions
ΔE_V	-	Bandgap discontinuity in the valence band
ΔW	-	Parasitic energy barrier width
ϵ	-	PolySi relative permitivity
γ	-	Mole fraction of reactant species
μ	-	PolySi effective mobility
μ_H	-	Hall mobility
$\mu_{nb(Si)}(T)$	-	Minority electron mobility in the silicon base, as a function of temperature
$\mu_{nb(SiGe)}(T)$	-	Minority electron mobility in the silicon-germanium base, as a function of temperature
$\mu_{pb(Si)}(T)$	-	Majority hole mobility in the silicon base, as a function of temperature
$\mu_{pb(SiGe)}(T)$	-	Majority hole mobility in the silicon-germanium base, as a function of temperature
Ψ	-	Fermi level temperature shift correction
ρ	-	PolySi resistivity

Chapter 1

Introduction

The last decade has seen major research into group IV-IV heterojunction bipolar transistors (HBTs). This increased interest is driven by the desire to create devices with improved performance whilst still maintaining the VLSI mass production capability associated with the standard silicon technology. The $Si_{1-x}Ge_x/Si$ binary alloy and its device applications have been extensively studied, making the production of high performance and high yield devices possible, and has culminated in the production of large scale circuits such as high performance digital to analogue converters [1]. The physical and electronic structure have also been thoroughly investigated and documented [2–5] allowing the fabrication of structures with mathematically predictable behaviour.

Until 1993 most of the high performance HBTs reported were either grown by UHV/CVD or by Molecular Beam Epitaxy (MBE). However Hong *et al.* [6] reported high performance devices produced in a commercial Low Pressure CVD reactor (LPCVD), thus breaking away from the reliance on reactor technology which had historically been the major factor of process costs. The SiGe bases were grown at 700°C using a Dichlorosilane (DCS) process, and produced devices with a reasonable forward current gain (β_{max}) of 51 and a peak f_T of 31 GHz. Since then several authors have also reported growth of high quality SiGe layers, suitable for use as the base layer in SiGe HBTs, using LPCVD reactors [7–9]. More recently, active research has been undertaken to form the $Si_{1-x}Ge_x$ base layer by germanium implantation [10]. Although this does not produce the ultimate high performance device there is still a noticeable improvement over a conventional all silicon transistor. Typical devices had a basewidth of approximately 60nm and a peak germanium concentration of 8 at.% at the collector-base junction. Gummel plots of collector

and base currents of the HBT and a silicon control device, which was processed identically apart from the germanium implantation, showed that there was approximately a factor of 2 improvement in the collector current of the HBT.

The $Si_{1-x}Ge_x$ HBT has three key advantages [11] over the traditional silicon bipolar transistor. Firstly the base transit time is reduced which implies a higher f_T and f_{max}. Secondly the collector current density (J_c) is increased for a given base current which directly translates to an increase in the current gain, which can then be traded for higher base doping and lower base resistance. Finally the Early voltage (V_A) is increased for a given cutoff frequency. These key advantages have allowed the fabrication of devices with record cut-off and maximum oscillation frequencies of 130GHz [12] and 160GHz [13] respectively.

A major concern in the fabrication of SiGe HBTs is the realisation of the thin, highly doped SiGe base layer. If the metallurgical junctions lie outside of the SiGe layer, due to the base dopant out-diffusing into the lighter doped emitter and collector, the formation of parasitic energy barriers in the conduction band occurs, severely degrading device performance [14, 15]. This problem is further compounded by the phenomenon of transient enhanced diffusion which occurs during the annealing of implantation damage [16–24]. Ion implantation is particularly useful in forming the p^+ extrinsic base contacts, which are necessary to reduce the extrinsic base resistance and so optimise the transistors for high speed performance. Transient enhanced diffusion is the term given to the anomalous diffusion of dopant during the first few seconds of an anneal and has become increasingly noticeable during rapid thermal anneals since the anneal times are so short.

One method of minimising the impact of transient enhanced diffusion has been to include undoped silicon-germanium spacer layers at the emitter-base and collector-base junctions, in order to keep the base dopant within the SiGe alloy [15]. However this requires making the SiGe base layer thicker than required, which can cause problems at high Ge concentrations since such layers are prone to relax, especially during high temperature anneal cycles [7, 25]. This relaxation not only reduces the strain enhanced bandgap narrowing in the base, thereby reducing the current gain enhancement associated with the heterojunction, but can also increase the neutral base recombination component of the base current, reducing the forward current gain of the device.

In order to avoid the problems of both TED and strain relaxation, active research has been performed on the substitutional incorporation of carbon into SiGe to form

the ternary alloy $Si_{1-x-y}Ge_xC_y$. The incorporation of carbon has been shown to both reduce strain within the epitaxial layer [25–31] and suppress transient enhanced diffusion [32–41]. The research is still underway, but early results seem promising. The original growth methods were centred around MBE and SPE, however with recent advances in CVD technology and suitable organosilicon carbon precursors the emphasis has shifted to RTCVD and LPCVD. One problem with this ternary heterojunction system, is that the growth of such materials is hindered by two conflicting conditions, a higher growth temperature to ensure the precursor decomposes, and a lower growth temperature to avoid the formation of silicon carbide precipitates [41–43]. This often results in a small process window.

Since 1996, several authors have reported successful fabrication of SiGeC HBTs [44–47] and have demonstrated that enhanced boron diffusion, due to emitter and extrinsic base implants, is reduced by carbon incorporation. Room temperature collector current measurements, as a function of collector/base reverse bias, have been used to determine whether parasitic energy barriers are present and hence indicate whether TED has occurred [46]. This method is useful for easy detection of larger potential energy barriers at the collector/base junction but is not sensitive enough to accurately determine the presence of small energy barriers. Since the impact of the energy barrier increases with decreasing temperature, low temperature measurements are a better way of determining the presence of parasitic energy barriers. In this thesis, parasitic energy barriers are characterised using a novel electrical method [48] which involves the measurement of the temperature dependence of the collector current at various collector/base reverse biases. The presence of a parasitic energy barrier is detected by a decrease in the slope of an Arrhenius plot and confirmed by a change in the slope with C/B reverse bias. This method is extremely sensitive to small amounts of boron out-diffusion from the base and allows a more accurate determination of the presence of parasitic energy barriers, since the collector current is measured over a wide range of temperatures. The sensitivity of the method in determining the presence of parasitic energy barriers will also allow an investigation of how the carbon concentration and position in the transistor affect the TED suppression. This will allow the carbon profile to be optimised for maximum TED suppression.

For many years, polycrystalline silicon has been a major contributor to the success of silicon technology. This incredibly useful material has found many applications in both CMOS and bipolar devices, where it is used as a gate electrode for a MOS transistor [49], and as an emitter for a bipolar transistor [50]. Polysilicon has also found additional uses in more specialised silicon technologies, such as substrates

for the fabrication of thin film transistors (TFT) [51, 52] and in Micro-Electro-Mechanical Systems (MEMS) [53].

More recently, considerable interest has been shown in polycrystalline SiGe films [54–62] because of their increased dopant activation [63–65]and lower thermal growth budget. In MOS transistors, polySiGe gates could be used to reduce gate depletion and to tailor the work function by varying the Ge content, allowing more freedom in the setting of threshold voltages. Furthermore, these films can be realised using a process that is fully compatible with existing silicon-based technologies.

The effects of adding germanium to polysilicon films differ depending on the type of dopant used. In p-type polycrystalline SiGe, the resistivity decreases with increasing Ge content, which has been attributed to increases in both hole mobility and dopant activation with increasing Ge incorporation [64, 66]. In contrast, it has been shown [64] that for n-type films containing less than 25% Ge, the Hall mobility increases, but the effective carrier concentration steadily decreases, with increasing Ge content. The net effect is a slight decrease in the resistivity at low Ge concentrations. For layers with Ge concentrations above 25%, a large drop in phosphorus activation combined with a drop in the Hall mobility is observed [54, 64], causing a large increase in resistivity. This was attributed to increased phosphorus segregation to the grain boundaries with increasing Ge content.

As stated earlier, considerable interest has been shown in single-crystal SiGeC for use in heterojunction bipolar transistors to suppress transient enhanced diffusion. Polycrystalline $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ are also of interest because they offer the prospect of increased bandgaps [30, 31] and hence give an additional degree of freedom for bandgap engineering not offered by poly$Si_{1-x}Ge_x$ alone. Although there is a large body of work on single-crystal SiGeC films, little, if any, has been published on the properties of polycrystalline SiGeC films. In this thesis the electrical properties of in-situ doped n- and p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers are studied. The resistivity, Hall mobility and effective carrier concentration have been measured for a range of carbon contents, allowing a thorough investigation of the effects of carbon incorporation. In addition, the temperature dependence of the resistivity has also been measured, allowing the extraction of the grain boundary energy barrier, to show whether carbon is influencing the electrical properties of the layers via the grain boundary. From these results a hypothesis is presented, which attempts to explain the role of carbon in the n- and p-type layers, at both low and high C concentrations.

The structure of the thesis is organised as follows; Chapter 2 gives details of the theory pertaining to the growth, characterisation and device physics of the $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ alloy system. Chapter 3 gives a brief overview of the LPCVD epitaxial reactor and outlines details of the experimental procedures used in this work. Chapters 4 and 5 present results of investigations into the TED suppression capability of carbon in $Si_{1-x-y}Ge_xC_y$ HBTs. Chapters 6 and 7 present results of investigations into the effects of carbon on the electrical properties of $Si_{1-y}C_y$ and $Si_{0.82-y}Ge_{0.18}C_y$ layers. Finally in chapter 8, some conclusions are drawn and future work discussed.

Chapter 2

Theory: Growth, Characterisation and Physics of $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ Alloys

2.1 Introduction

The epitaxial growth of a $Si_{1-x}Ge_x$ layer is an important step in producing a silicon heterojunction device. In order to maximise the full benefits associated with the incorporation of a heterojunction, the fundamentals of the growth phenomena have to be understood, allowing both precise process control and easier exploration of new applications. In addition, an accurate knowledge of current mechanisms within the heterojunction allows further optimisation of transistor design since parasitic elements, such as emitter-base recombination, can be identified and minimised.

In this chapter the growth and characterisation techniques for both $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$ alloys will be discussed. Section 2.2 briefly discusses models used to describe the growth kinetics of epitaxial growth [67–72]. Reactor technology and process constraints on the growth of pseudomorphic SiGe and SiGeC films will be examined in sections 2.3 and 2.4. These determine both the composition and quality of the deposited films. In section 2.5, the band alignment in the SiGe/Si and SiGeC/Si heterojunction system is considered, whilst in section 2.6 analytical expressions for the current enhancements within the heterojunction will be presented.

Section 2.7 discusses advanced issues that affect device performance, such as parasitic energy barriers. Section 2.8 outlines details of a novel electrical method [48,73] that allows the bandgap narrowing in the base to be extracted from the temperature dependence of the collector current. This allows the presence and approximate magnitude of parasitic energy barriers to be determined. Finally in section 2.9, expressions describing conduction mechanisms in polycrystalline silicon are presented, whilst in section 2.10, expressions allowing the effective carrier concentration and Hall mobility to be extracted from van der Pauw measurements are also presented.

2.2 Kinetics of epitaxial growth

2.2.1 A simple model describing the epitaxial growth process

A simple model can be used to describe the kinetics of epitaxial growth [67], and is shown schematically in figure 2.1. It is assumed that the bulk concentration of the reactant species in the gas stream can be described by a constant C_g, which drops to a surface concentration C_s at the interface. This assumption allows two fluxes to be defined. F_1 represents the fiux of the reactant species arriving at the semiconductor interface, whilst F_2 represents the flux corresponding to the amount of reactant species consumed at the surface. Using a linear approximation, F_1 and F_2 can be described by :

$$F_1 = h_g(C_g - C_s) \tag{2.1}$$

and

$$F_2 = k_sC_s \tag{2.2}$$

where h_g and k_s are the vapour phase mass transfer coefficient and the surface reaction rate constant respectively [67]. In the steady state, F_1=F_2=F, allowing the surface concentration to be given by :

$$C_s = \frac{C_g}{1 + \frac{k_s}{h_g}} \tag{2.3}$$

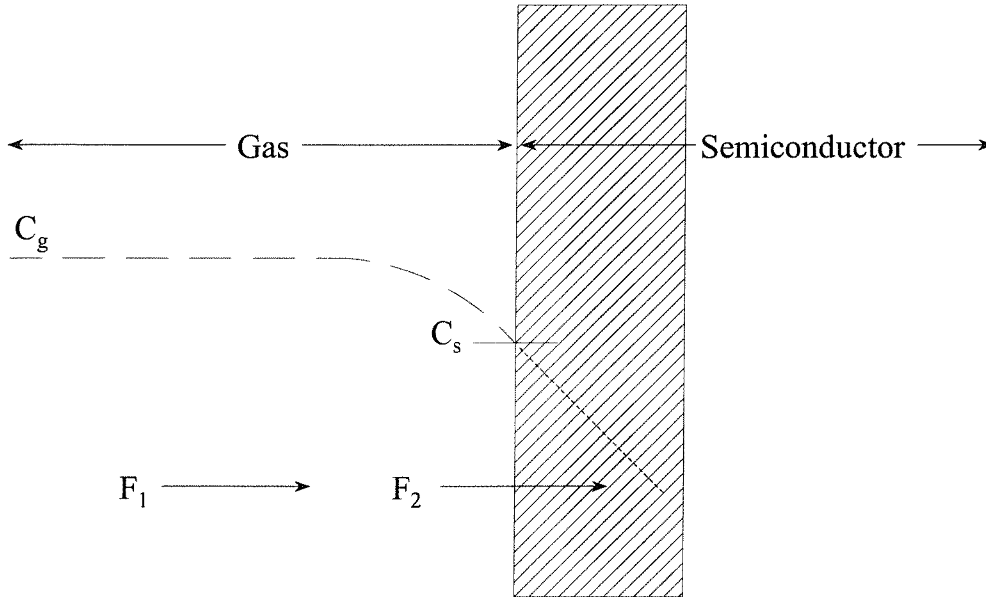


Figure 2.1: Simple schematic model for the epitaxial growth process. After Sze [67]

The growth rate of the layer (r) is given by the steady state flux F divided by the number of atoms per unit volume (C_a) in the deposited semiconductor layer, which in the case of silicon is 5×10^{22}cm^{-3}. Using this relationship and substituting equation 2.3 into 2.2, the growth rate r is given by :

$$r = \frac{F}{C_a} = \frac{k_s h_g}{k_s + h_g} \frac{C_g}{C_a} \tag{2.4}$$

Finally, the bulk gas concentration C_g is proportional to the product of the mole fraction (γ) of the reactant species to the total number of atoms in the gas (C_t). Therefore equation 2.4 can be rewritten as :

$$r = \gamma \frac{k_s h_g}{k_s + h_g} \frac{C_t}{C_a} \tag{2.5}$$

From equation 2.5 it can be seen that for a given mole fraction, the growth rate will be determined by the relative magnitudes of k_s and h_g, with two limiting cases of :

$$r \simeq \gamma k_s \frac{C_t}{C_a} \qquad k_s \ll h_g \tag{2.6}$$

and

$$r \simeq \gamma h_g \frac{C_t}{C_a} \qquad h_g \ll k_s \tag{2.7}$$

Equation 2.6 shows that the growth rate will be limited by how fast the surface reaction can take place, and is hence termed surface reaction controlled. In contrast equation 2.7 shows that the rate will be limited by how fast the reactant species can be transported to the wafer surface. This is referred to as mass transfer controlled. Figure 2.2 shows the temperature dependence of the growth rate of silicon using silane as the source gas. It can be seen that at low temperatures (T $\leq$ 850°C), the growth rate follows an exponential temperature dependence, whilst above this temperature, the growth rate is fairly temperature invariant. From this behaviour, the low temperature region is characterised as surface reaction controlled since chemical reactions generally follow an exponential temperature dependence. In contrast, the mass transfer process is relatively independent of temperature, indicating that the high temperature region is therefore mass transfer controlled. The growth of in-situ doped amorphous Si, SiGe and SiGeC layers, described later in this work, will be performed at a temperature of 540°C. From figure 2.2 it can be seen that this means that the growths are surface reaction rate controlled and are therefore sensitive to deposition temperature.

2.3 $\mathrm{Si_{1-x}Ge_x}$ Epitaxial Growth and Film Properties

A major feature of the group IV-IV heterojunction system is that the lattice mismatch (4.2%) between silicon and germanium means that devices have to be fabricated by strained layer epitaxy. As the germanium content in the pseudomorphic layer is increased the lattice parameter approaches the value of pure germanium, since from Vegard's Law :

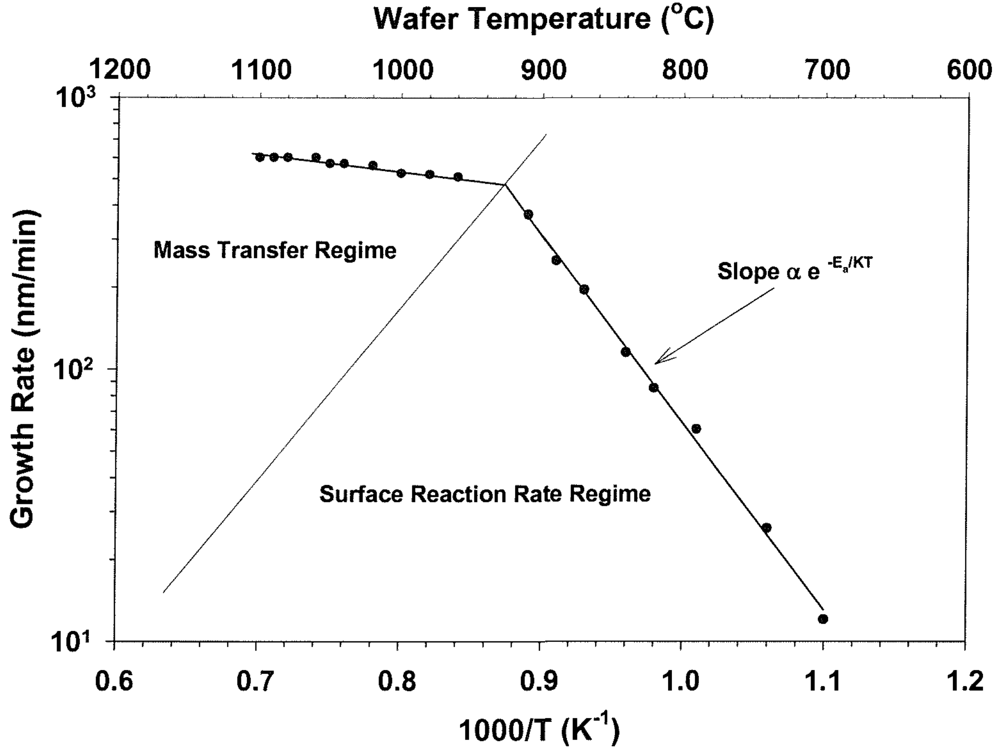


Figure 2.2: The temperature dependence of the growth rate using silane as the source gas. After Eversteyn [74].

$$a_{SiGe} = a_{Si} + x(a_{Ge} - a_{Si}) \tag{2.8}$$

where a_{Si} (5.43Å) and a_{Ge} (5.65Å) are the lattice parameters of Silicon and Germanium respectively

The dependence of the lattice parameter on germanium content severely limits the thickness of layer that can be grown whilst still remaining fully strained and completely stable. This upper limit is termed the *critical thickness.* If layers are grown which exceed this thickness they may be metastable or fully relaxed. The relaxation causes misfit dislocations within the lattice which are efficient recombination centres and hence have a deleterious effect on the transistor performance. The term metastable is used to define a layer that is stable when grown but will relax if subjected to subsequent high temperature processing. Figure 2.3 shows the growth modes of a SiGe layer as a function of germanium content.

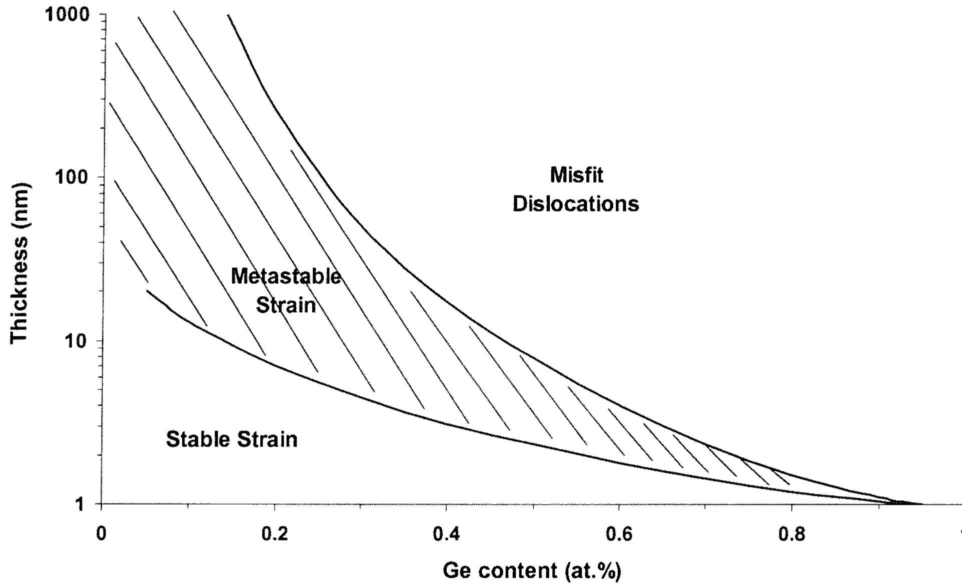


Figure 2.3: SiGe thickness as a function of Ge content for the three growth modes. After Mi. Phd Thesis 1995 [25]

2.4 $\mathrm{Si_{1-x-y}Ge_xC_y}$ Epitaxial Growth and Film Properties

As stated earlier the growth of high quality $Si_{1-x}Ge_x$ films is limited by the lattice mismatch between the grown alloy and the underlying silicon substrate and can only be achieved by strained layer epitaxy, where the alloy is forced to adopt the substrate lattice dimensions at the interface between the two materials.

To overcome this limitation active research has been performed where carbon is substitutionally incorporated into the $Si_{1-x}Ge_x$ to form the ternary alloy $Si_{1-x-y}Ge_xC_y$. Since Si, Ge and C are all group IV elements they are isostructural and can, in theory, be intermixed to give alloys with a larger bandgap than that of $Si_{1-x}Ge_x$ [42]. In addition the smaller lattice parameter of carbon (3.546Å) will compensate for the larger one of germanium (5.646Å), reducing the net lattice mismatch between the alloy and silicon substrate (5.431Å) and hence decreasing the strain within the layer. Assuming that Vegard's law applies the lattice parameter of $Si_{1-x-y}Ge_xC_y$ can be given by [27]:

$$a_{SiGeC} = a_{Si} + x(a_{Ge} - a_{Si}) + y(a_C - a_{Si}) \tag{2.9}$$

where a_{Si} (5.43Å), a_{Ge} (5.65Å) and a_C (3.57Å) are the lattice parameters of silicon, germanium and carbon respectively.

Obviously the third term is negative and so it is possible to get complete cancellation between the second and third terms. i.e. the alloy has lattice dimensions equivalent to the bulk silicon substrate. If these two terms are equated then it is found that complete compensation is achieved by a germanium to carbon ratio of 9:1. However the incorporation of carbon into the alloy is hindered by several problems :

1. The solid solubility of carbon in silicon is very low, less than 2×10^{-3} at.%, making it very difficult to fabricate alloys with a wide composition range.
2. The growth temperature has to be carefully selected to minimise the thermodynamically favourable tendency to form silicon carbide precipitates instead of substitutionally incorporating the carbon. These precipitates severely reduce the epitaxial quality.
3. There is a limited number of suitable carbon precursors that give good carbon incorporation efficiency at the required low growth temperatures.

2.5 Band Alignment in the SiGe/Si and SiGeC/Si Heterojunction System

In addition to understanding the growth kinetics of $Si_{1-x}Ge_x$ and $Si_{1-x-y}Ge_xC_y$, an accurate knowledge of band alignment is required to make devices with known electrical characteristics. To a large extent the conduction and valence band discontinuities, ΔE_C and ΔE_V, determine the electrical properties of the heterojunction. Walle *et al* [75] have performed theoretical calculations which predict that most of the bandgap narrowing in the $Si_{1-x}Ge_x$ alloy is in the valence band, i.e. $\Delta E_V \approx \Delta E_g$. Chock *et al* [76] have used a Semiconductor-Insulator-Semiconductor (SIS) heterostructure in order to measure the valence band discontinuity for low germanium concentrations (x $\leq$ 20%), which had been used previously to determine the band alignments in the GaAs/AlGaAs heterojunction system. The SIS heterostructure consists of an undoped wide bandgap material sandwiched between

two doped narrow bandgap layers. Under equilibrium conditions the heterostructure has a symmetric square shaped potential barrier which easily lends itself to mathematical analysis and hence accurate extraction of band discontinuities. From their data a best line fit of $\Delta E_V = 6.4$x meV (where x is the Ge percentage) was obtained for the top interface and $0 \leq x \leq 17.5\%$. Also, apart from the 10% case, the lower interface had a consistently lower band discontinuity, of between 10 and 20 meV, and is attributed to surface roughening due to germanium segregation at the interface during growth.

Experiments on SiGeC layers to determine band alignment have shown that the valence band offset, which is the dominant offset in SiGe layers, remains largely unaffected [77]. In contrast, similar experiments on SiC layers showed that there is almost no valence band offset, with nearly all of the band gap difference being taken up in the conduction band. Eberl *et al* [31] have performed photoluminescence measurements on $Si_{0.84}Ge_{0.16}$ and $Si_{0.82}Ge_{0.16}C_{0.02}$ films to investigate the affect of carbon on bandgap. From their results an increase of approximately 24meV/%C was observed. In this work, much lower concentrations of carbon are used, $\approx 10^{20}$cm^{-3} or 0.2% , resulting in a bandgap increase of approximately 5meV compared to an identical SiGe layer without carbon. Since the band differences between the SiGe and SiGeC systems appear to differ in the conduction band, and that the amount of carbon used in this work is small, it is assumed that equations describing the electrical characteristics of SiGe HBTs still apply to SiGe:C HBTs. Therefore, the analysis method described in section 2.8, for the extraction of the bandgap in SiGe HBTs, can be equally applied to the SiGe:C devices and a correction added to the extracted value for the incorporated carbon.

2.6 Collector and Base Currents in a Heterojunction Transistor

A heterojunction transistor is created when the emitter and base are constructed of materials with a different bandgap. Originally early research was limited to group III-V compound semiconductors such as AlGaAs/GaAs, since growth methods only allowed materials with similar lattice constants to be epitaxially grown on top of each other. However with advances in chemical vapour deposition systems it is now possible to perform strained layer epitaxy, where an alloy is forced to adopt the lattice dimensions of the underlying substrate. This has made group IV-IV

semiconductors, such as $Si_{1-x}Ge_x$, a viable alternative, with the added advantage of being potentially integrable with present silicon technologies.

If small and large bandgap materials are brought into intimate contact, as is the case in a SiGe HBT, the bands align in such a way that discontinuities, ΔE_c and ΔE_v, are formed in the conduction and valence bands respectively. This is shown in figure 2.4.

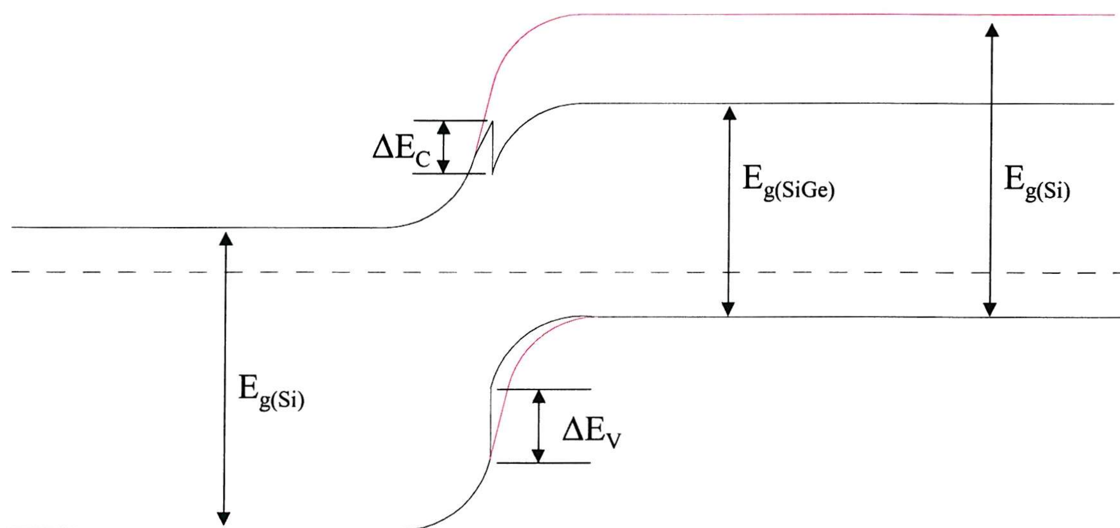


Figure 2.4: Band line up at the emitter-base junction of a SiGe heterojunction bipolar transistor

The discontinuities form since the Fermi level is constant either side of the junction, at thermal equilibrium, and the energy bands must remain parallel. In SiGe, the bandgap difference between the two materials divides unevenly between the conduction and valence bands, with the majority appearing as an offset at the valence band. From figure 2.4 it can be seen that the barrier in the valence band for the Si/Si homojunction and Si/SiGe heterojunction is the same. This means to a first approximation that the base currents of both devices are equivalent. However the conduction band barrier in the heterojunction is reduced by ΔE_c which leads to a greater electron injection efficiency. This increased efficiency leads to improved collector current, for a given base-emitter voltage, and hence higher current gain, which can then be traded for reduced base resistance by increased base doping.

In order to derive the current equations for a SiGe HBT it is easiest to start with the equations for a Si BJT, since both devices are similar in nature. The equations for the base and collector current in a Si BJT with uniform doping are given by [78] :

$$I_B = -\frac{qAD_{pe}n_{ieo}^2}{W_E N_{de}} exp \frac{qV_{BE}}{kT} \tag{2.10}$$

and

$$I_C = -\frac{qAD_{nb}n_{ibo}^2}{W_B N_{ab}} exp \frac{qV_{BE}}{kT} \tag{2.11}$$

where n_{ieo} and n_{ibo} are the intrinsic carrier concentrations in the emitter and base. N_{de} and N_{ab} are the emitter and base doping levels, D_{pe} and D_{nb} are the minority carrier diffusivities and W_E and W_B are the neutral emitter and base widths respectively. Equations 2.10 and 2.11 assume that the emitter and base are both transparent, i.e. $L_{pe} \ll W_E$ and $L_{nb} \ll W_B$, where L_{pe} is the hole diffusion length in the emitter and L_{nb} is the electron diffusion length in the base.

For the silicon BJT the intrinsic carrier concentrations in the base and emitter are equivalent and are given by :

$$n_{ieo}^2 = n_{ibo}^2 = (N_C N_V)_{(Si)} exp \frac{-E_{G(Si)}}{kT} \tag{2.12}$$

where N_C and N_V are the effective density of states and $E_{G(Si)}$ in the bandgap of silicon. It can be seen from equation 2.12 that the intrinsic carrier concentration is bandgap dependent and increases with bandgap reduction. Therefore it follows that in a heterojunction transistor the intrinsic carrier concentrations are no longer equal, and so $n_{ibo(Si)}$ must be replaced by $n_{ibo(SiGe)}$, which is given by :

$$n_{ibo(SiGe)}^2 = (N_C N_V)_{(SiGe)} exp \frac{-E_{G(SiGe)}}{kT} = (N_C N_V)_{(SiGe)} exp \frac{-E_{G(Si)} + \Delta E_G}{kT} \tag{2.13}$$

where ΔE_G is the bandgap difference between the silicon emitter and the SiGe base. This means equation 2.11 must be rewritten as :

$$I_{C(SiGe)} = -\frac{qAD_{nb(SiGe)}n^2_{ibo(SiGe)}}{W_BN_{ab}}exp\frac{qV_{BE}}{kT} \quad (2.14)$$

By combining equations 2.11, 2.12, 2.13 and 2.14 the collector current enhancement, and hence current gain enhancement, can be given by :

$$Enhancement = \frac{I_{C(SiGe)}}{I_{C(Si)}} = \frac{(D_{nb}N_CN_V)_{(SiGe)}}{(D_{nb}N_CN_V)_{(Si)}}exp\frac{\Delta E_G}{kT} \quad (2.15)$$

From equation 2.15 a substantial current gain enhancement can be expected for an HBT over an equivalent silicon BJT even for small bandgap differences. For example a bandgap difference of 74meV, which equates to approximately 10% germanium, gives a theoretical gain enhancement factor of 50 at room temperature (assuming no difference in the density of states of silicon and silicon-germanium). It should be noted that equation 2.15 is an idealised case where emitter-base recombination and conduction band spikes [79] are not considered.

As mentioned earlier the gain enhancement was calculated assuming equal density of states and diffusivities in Si and SiGe. However research has shown [2,4] that strain and germanium content reduce the N_CN_V product significantly, for example a Ge concentration of 12% at a doping level of $5 \times 10^{18}cm^{-3}$ leads to a N_CN_V product which is only 20% of that in Si [80]. This implies the gain enhancement could be a value less than predicted by the simplified case.

An additional modification to the equations is the incorporation of heavy doping effects. When a semiconductor is heavily doped the discrete impurity level splits forming an impurity band [78]. In addition the large concentration of dopant atoms disrupts the periodicity of the lattice causing band tails to form in the conduction and valence bands. The combination of these effects causes a further reduction in the bandgap, which has the effect of further increasing the intrinsic carrier concentration.

There has been a significant amount of research and theoretical investigation into heavy doping bandgap narrowing (BGN) with mixed results [81–84]. A major discrepancy is the difference in values of BGN obtained from optical absorption

and electrical measurements. From the mass action law, theory predicts that the minority carrier concentration is suppressed by the same factor by which the majority concentration is enhanced upon doping the crystal. However, in heavily doped semiconductors Fermi Dirac statistics predict a rapid rise of the Fermi level into the majority band which has the effect of suppressing the minority carrier concentration by a larger than expected amount. This has the net effect of suppressing the BGN enhancement factor of the intrinsic carrier concentration [81]. To model these effects the mass action law must be modified to :

$$pn = n_{io}^2 exp\frac{\Delta E_{GB}}{kT} exp\frac{-E_F}{kT} F_{1/2}\left(\frac{E_F}{kT}\right) \tag{2.16}$$

where n_{io} is the intrinsic carrier concentration in lightly doped material, ΔE_{GB} is the heavy doping induced BGN, E_F the Fermi level and $F_{1/2}$ is the Fermi-Dirac integral. Equation 2.16 can be rewritten in the more familiar form of [81]:

$$pn = n_{ieff}^2 = n_{io}^2 exp\frac{\Delta E_{GB}^{app}}{kT} \tag{2.17}$$

ΔE_{GB}^{app} is the apparent bandgap narrowing and is given by :

$$\Delta E_{GB}^{app} = \Delta E_{GB} + \Delta E^{FD} \tag{2.18}$$

where ΔE^{FD} is the Fermi-Dirac correction to the heavy doping BGN. This correction is always negative, making the apparent bandgap narrowing smaller than the actual BGN. This is attributed as the source of the discrepancies between optical absorption and electrical measurements since the former measures the actual BGN whilst the latter measures the apparent BGN. Apparent BGN is more convenient for use in current models and so an empirical fit, valid for both n and p-type semiconductors, has been calculated by Klaassen *et al* [85] and is shown in equation 2.19

$$\Delta E_{GB} = 6.92 \left[ln\left(\frac{N_a}{1.3\times 10^{17}}\right) + \sqrt{\left[ln\left(\frac{N_a}{1.3\times 10^{17}}\right)\right]^2 + 0.5}\right] meV \qquad (2.19)$$

where N_a is the doping level in the semiconductor. The empirical fit is valid for doping levels up to $10^{20} cm^{-3}$ and germanium concentrations of $x \leq 0.3$.

2.6.1 Graded Germanium Profiles

As stated earlier some authors [11, 86] favour a graded profile to improve base transit times and hence increase f_T. However the graded profile is highly sensitive to the bias conditions used [86]. A box profile HBT has an identical gain-bias dependency to that of a standard BJT and so the movement of the edge of the depletion layer in the base has little effect on the collector current. This effect is magnified for a triangular Ge profile in the base since the collector saturation current (J_{oc}) is now position dependent and is determined by an exponential factor related to the germanium content at that point. i.e. from [86]

$$J_{oc} \approx \frac{qD_{nb}{n_{io}}^2}{N_{ab}W_b}\frac{\Delta E_{gGe}(Grade)}{kT}\exp\left(\frac{\Delta E_{gGe}(0)}{kT}\right) \qquad (2.20)$$

where $\Delta E_{gGe}(0)$ is the bandgap narrowing due to the Ge content at the emitter-base depletion layer edge and $\Delta E_{gGe}(Grade)$ is the germanium grading within the base. i.e. the difference between the Ge bandgap narrowing at the collector and emitter junctions. From equation 2.20 and Figure 2.5, it can be seen that an increase in V_{BE} shrinks the depletion layer causing a significant reduction in J_{oc}. This is a problem since it will reduce the collector current ideality and cause a roll-off in the forward current gain. From equation 2.20 it can be expected that this effect will be much more pronounced at lower temperatures due to the ratio of $\Delta E_{gGe}(0)$ and kT.

In order to investigate how much the collector current ideality will be affected by the dependence of J_{oc} on applied V_{BE}, a simple uniformally doped transistor with a 10% Ge graded profile was considered. This is shown schematically in figure 2.6.

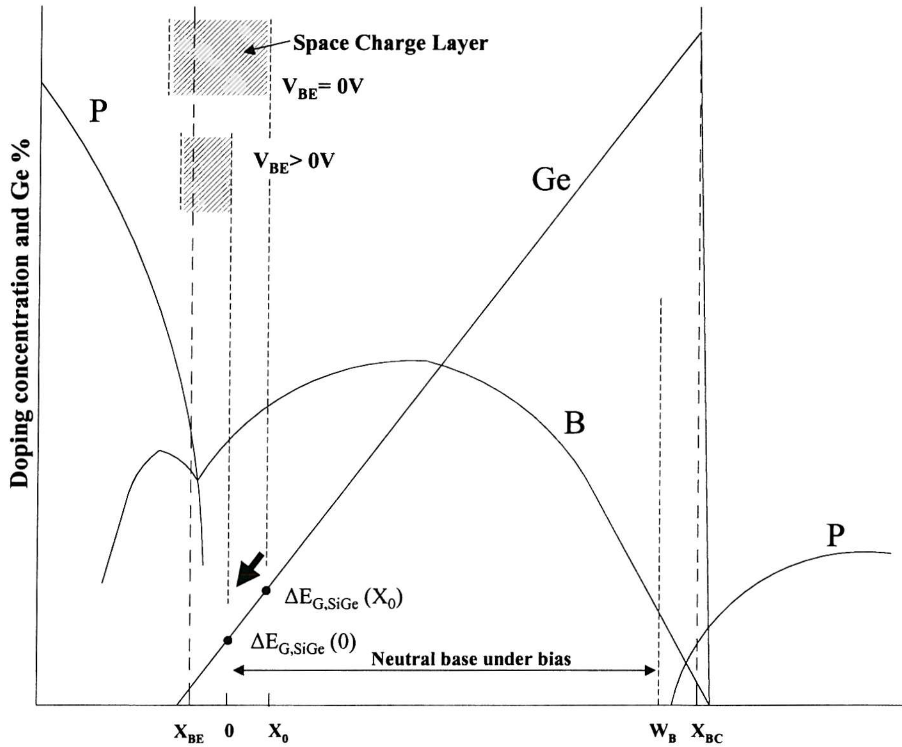


Figure 2.5: Diagram showing how bias conditions vary the bandgap narrowing (BGN) at the emitter-base depletion region edge. The exponential dependence of collector current on this BGN means that a small change has significant effects. After Crabbe *et al* [86] IEEE Electron Dev. Lett. 1993

To this structure, the effect of applying forward base-emitter bias, in the range of 0V to 0.7V, was calculated. At each bias point, the neutral basewidth, the penetration of the E-B depletion region into the base and the corresponding value of $\Delta E_g(0)$ was calculated. These values were then inserted into equation 2.20 to give a value for the collector saturation current density at that bias point. In addition, the calculations were carried out at three different temperatures (100K, 200K and 300K) to study the temperature effects on bias dependency. Figure 2.7 shows plots of the collector saturation current density, normalised against the zero bias value, calculated at temperatures of 100K, 200K and 300K. From figure 2.7 it can be seen that as the applied bias, V_{BE}, is increased, the collector saturation current density decreases due to the reduction in the bandgap narrowing at the emitter side of the neutral base, i.e. $\Delta E_g(0)$. In addition, it can be seen that as the temperature is reduced the effects of bias are dramatically increased, with J_{OC} having a normalised value of 0.64 at 300K dropping to 0.33 at 100K, for a base-emitter bias of 0.7V. To investigate the affects of the reduction of J_{OC} with applied bias on collector current ideality, the collector current density was calculated using the standard expression given in equation 2.21, the results of which are shown in figure 2.8 for temperatures

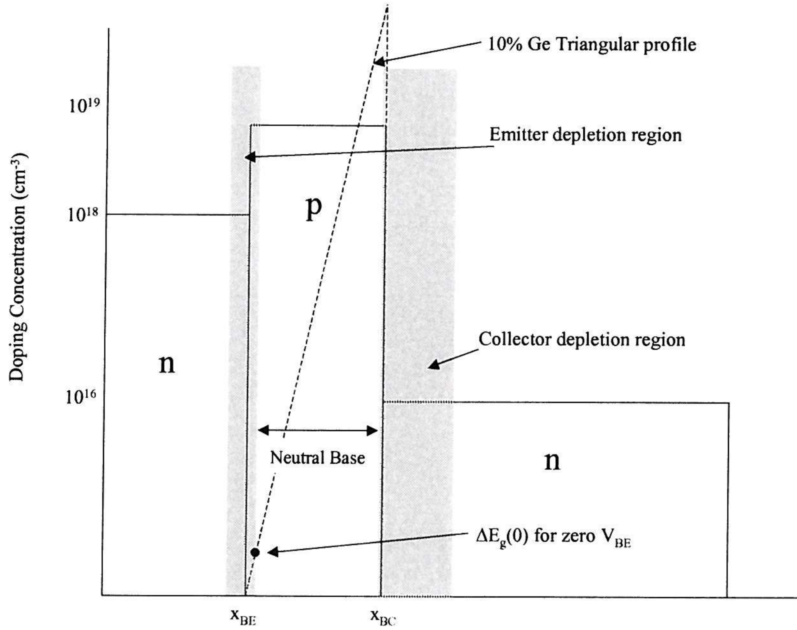


Figure 2.6: Simple uniformally doped transistor with a 10% Ge graded profile.

of 100K and 300K.

$$J_C = J_{OC}\ exp\frac{qV_{BE}}{kT} \tag{2.21}$$

Also plotted in figure 2.8 is the collector current expected with a non varying saturation current density, giving an ideal collector current ($n_c = 1$) . From figure 2.8 it can be seen that the collector current of the transistor with the triangular Ge profile deviates from the ideal case, due to the reduced J_{OC}, indicating an increase in the non-ideality. Calculated values for the ideality factor were 1.014 and 1.017 for the investigated temperatures of 100K and 300K respectively. These results show that the collector current ideality is significantly influenced by the bias dependency of the collector saturation current density. For an arbitrary shaped germanium profile, the effects on the collector saturation current density can be described by [87]:

$$J_{oc} = qD_{nb}\left(\int_0^{W_B}\frac{N_{ab}(x)}{{n_i}^2(x)}dx\right)^{-1} \tag{2.22}$$

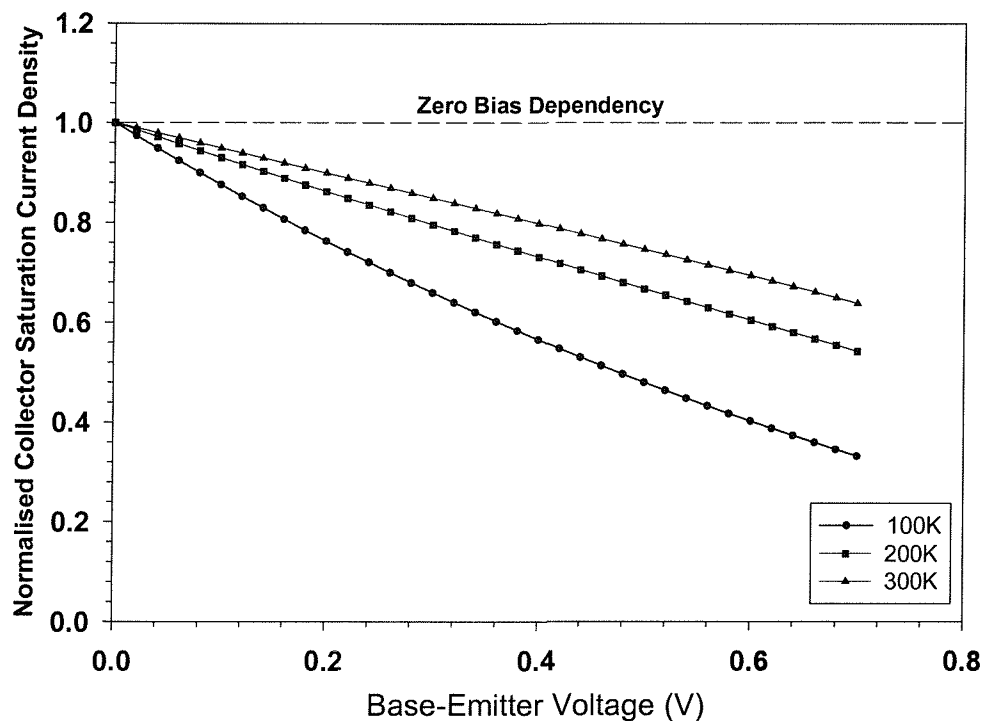


Figure 2.7: Plot of the collector saturation current density, normalised against the zero bias value, calculated at temperatures of 100K, 200K and 300K.

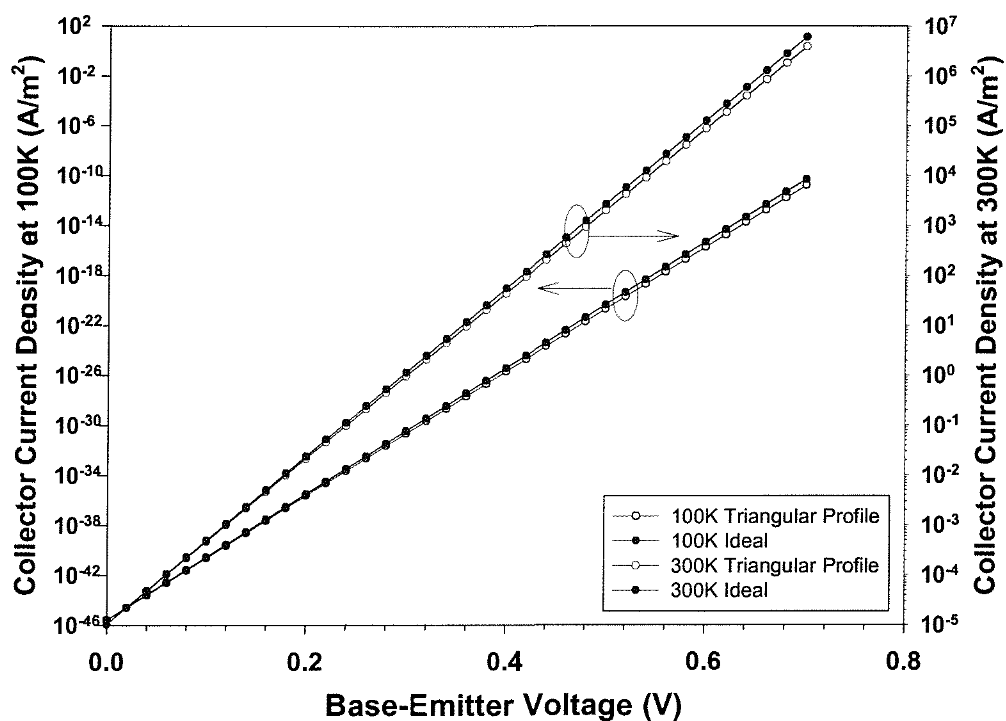


Figure 2.8: Calculated collector current densities showing how the dependence of the saturation current density on applied bias affects the collector current ideality n.

where $n_i^2(x)$ represents the position dependent intrinsic carrier concentration, which is a function of the Germanium content at that point.

2.7 Parasitic energy barriers in SiGe and SiGeC HBTs

Another problem, inherent to HBTs, is the formation of parasitic barriers, shown schematically in figure 2.9, when the germanium profile does not reach the metallurgical junctions within the device [14, 15]. This is generally due to the outdiffusion of the boron dopant into the lighter doped emitter and collector and has the effect of strongly reducing the collector current for a given bias. This effect can be explained by considering equation 2.22, where the term in brackets represents the effective base Gummel number (G_B), which is the integral of the base dopant weighted by a bandgap dependent intrinsic carrier concentration. Therefore if some

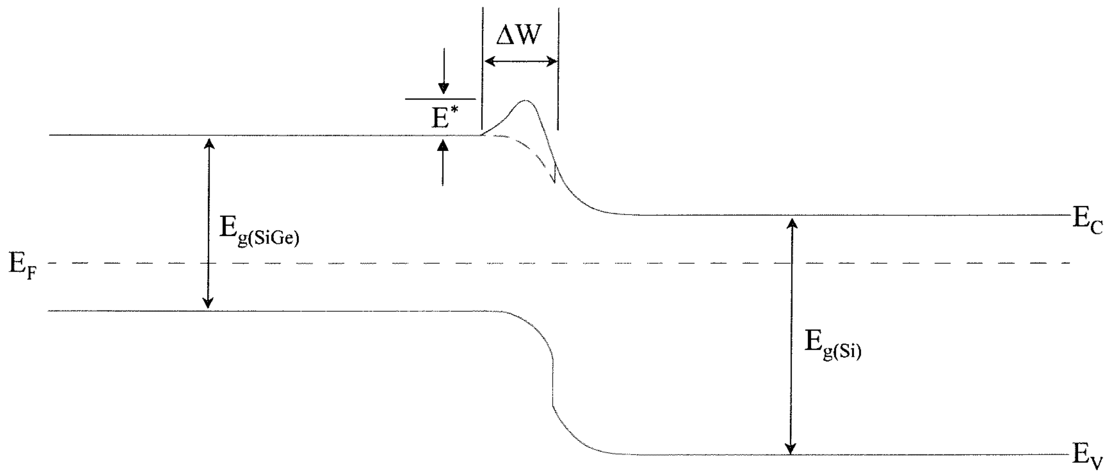


Figure 2.9: Schematic diagram showing a parasitic energy barrier at the collector/base junction.

dopant lies outside the germanium profile the n_i^2 term is much lower for this part of the base and leads to a reduction in J_{oc}. More significantly the barrier reduces the slope of the collector current enhancement vs. inverse temperature and standard equations describing this enhancement can no longer be used [15], thus making

it essential to develop models which fully account for this phenomena. A mathematical expression for the collector current of an HBT that accounts for a parasitic energy barrier at the collector-base junction has been reported by Slotboom *et al.* [14] and is shown in equation 2.23.

$$J_C = \frac{qD_{nb}n_{ib}^2(SiGe)}{N_{ab}W_B} \frac{\exp\left(\frac{qV_{EB}}{kT}\right)}{1 - \frac{\Delta W}{W_B} + \frac{\Delta W}{W_B}\exp\left(\frac{\Delta E^*}{KT}\right)} \tag{2.23}$$

where $n_{ib}(SiGe)$ is the intrinsic carrier concentration in the SiGe base, W_B is the base width between the metallurgical junctions, ΔW is the distance between the Ge profile and the base collector junction and ΔE^* is the parasitic energy barrier height at the C/B junction. It should also be noted that the barrier effect is further compounded by the modulation of the space charge layers within the base.

2.8 Extraction of the bandgap narrowing in the base of $\mathrm{Si_{1-x}Ge_x}$ and $\mathrm{Si_{1-x}Ge_x:C}$ HBTs

This section describes an electrical method [73] that allows the bandgap narrowing in the base of bipolar transistors to be determined using the temperature dependence of the collector current. For SiGe HBTs, the extracted bandgap narrowing value represents the total bandgap narrowing due to the combined effects of heavy doping and germanium incorporation. In addition, the method is also extremely sensitive to small amounts of boron out-diffusion from the base, and hence allows accurate determination of the presence of parasitic energy barriers. It should be noted that the following analysis assumes uniform doping levels within the base, a reasonable assumption for epitaxially grown films.

2.8.1 Temperature Dependence of $\mathrm{I_C}$

Equation 2.11 can be rewritten to describe the temperature dependence of the collector current density for a silicon BJT as :

$$J_{C(Si)}(T) = \frac{qD_{nb}(T)n_{ibeff(Si)}^2(T)}{N_{ab}(T)W_B(T)} exp\frac{qV_{BE}}{kT} \tag{2.24}$$

where $n_{ibeff(Si)}$ in the effective intrinsic carrier concentration due to heavy doping.

The temperature dependence of the diffusion coefficient can be described by :

$$D_{nb}(T) = \frac{\mu_{nb}(T)kT}{q} \tag{2.25}$$

where $\mu_{nb(Si)}(T)$ is the minority carrier electron mobility within the silicon base. The base doping concentration $N_{ab}(T)$ can decrease with cooling as a result of freeze-out effects [73]. This causes the intrinsic base sheet resistance to increase at low temperatures, as can be seen from the following equation :

$$R_B(T) = \frac{1}{q\mu_{pb(Si)}(T)N_{ab}(T)W_B(T)} \tag{2.26}$$

where $\mu_{pb(Si)}(T)$ is the majority carrier hole mobility within the silicon base. Equation 2.26 allows the calculation of the number of free carriers per unit area, $N_{ab}(T)W_B(T)$, and the mean ionized doping level within the base.

Combining equations 2.17, 2.24, 2.25 and 2.26, an expression for the temperature dependence of the collector current density in a Si BJT is obtained.

$$J_C(T) = qkT\mu_{nb(Si)}(T)\mu_{pb(Si)}(T)R_B(T)n_{ibo(Si)}(T)exp\frac{qV_{BE}}{kT}exp\frac{\Delta E_{GB}^{app}}{kT} \tag{2.27}$$

where ΔE_{GB}^{app} is the apparent doping induced BGN. A similar equation for SiGe HBTs can be used as follows :

$$J_{C(SiGe)}(T) = qkT\mu_{n(SiGe)}(T)\mu_{p(SiGe)}(T)R_B(T)n_{ibo(SiGe)}(T)exp\frac{qV_{BE}}{kT}exp\frac{\Delta E_{GB}^{app}}{kT} \tag{2.28}$$

2.8.2 Parameter Models for Bandgap Extraction

From equations 2.27 and 2.28 it can be seen that the temperature dependence of several parameters are required, namely the intrinsic carrier concentration $n_{ibo}(T)$, the majority carrier mobility $\mu_n(T)$ and the minority carrier mobility $\mu_p(T)$.

The temperature dependence of the intrinsic carrier concentration can be described by equation 2.12, using the substitution for the density of states product given by [88], and is as follows :

$$n_{ibo(Si)}^2(T) = 4\left(\frac{2\pi kT}{h^2}\right)^3 (m_n m_p)^{1.5} exp\frac{-E_{G(Si)}(T)}{kT} \quad (2.29)$$

where h is Planck's constant, m_n and m_p are the electron and hole effective masses and $E_{G(Si)}(T)$ is the undoped silicon bandgap, which varies with temperature. The effective masses used in this analysis were chosen as $1.258m_o$ for holes and m_o for electrons, consistent with the values used in the Klaassen unified mobility model [89, 90].

The temperature dependence of the undoped silicon bandgap can be described by the Thurmond model [91], given by:

$$E_{G(Si)}(T) = 1.17 - \frac{4.73 \times 10^{-4}T^2}{T + 636}eV \quad (2.30)$$

Similarly, from equations 2.12 and 2.13 the temperature dependence of the intrinsic carrier concentration in SiGe can be expressed as :

$$n_{ibo(SiGe)}^2 = \frac{(N_C N_V)_{SiGe}(T)}{(N_C N_V)_{Si}(T)} n_{ibo(Si)}^2(T) exp\frac{\Delta E_G}{kT} \quad (2.31)$$

Now that all of the temperature dependencies have been described, the expression for the collector current density for an HBT can be expressed as :

$$J_{C(SiGe)}(T) = J_{C(Si)}(T)\frac{(N_CN_V)_{SiGe}(T)}{(N_CN_V)_{Si}(T)}\frac{\mu_{nb(SiGe)}(T)}{\mu_{nb(Si)}(T)}exp\frac{\Delta E_G}{kT} \tag{2.32}$$

which can be rewritten as

$$J_{C(SiGe)}(T) = \frac{(N_CN_V)_{SiGe}(T)}{(N_CN_V)_{Si}(T)}\frac{\mu_{nb(SiGe)}(T)}{\mu_{nb(Si)}(T)}J_0(T)exp\frac{\Delta E_{GB}^{app}}{kT}exp\frac{\Delta E_G}{kT} \tag{2.33}$$

where

$$J_0(T) = 4q\left(\frac{2\pi}{h^2}\right)^3 (m_nm_p)^{1.5}\mu_{nb(Si)}(T)\mu_{pb(Si)}(T)R_B(T)exp\frac{qV_{BE} - E_{G(Si)}(T)}{kT} \tag{2.34}$$

The pre-exponential term $\frac{(N_CN_V)_{SiGe}(T)}{(N_CN_V)_{Si}(T)}$ represents the ratio of the density of states (DOS) between SiGe and Si. The data of Poortmans *et al* [2] at 300K is used to calculate the DOS and minority mobility ratios for $Si_{0.8}Ge_{0.2}$. Values of 0.17 and 1.3, for the DOS ratio and $\mu_{nB(SiGe)} : \mu_{nB(Si)}$ ratio respectively, have been extracted from the authors [2] experimental data. The majority carrier mobility ratios are assumed equal, since no experimental data exists to the contrary.

The value of bandgap narrowing in the SiGe base can now be found from the slope of the graph of

$$ln\left(\frac{J_{C(SiGe)}(T)}{CJ_0(T)}\right) vs\frac{1}{T} \tag{2.35}$$

where

$$C = \frac{(N_CN_V)_{SiGe}(T)}{(N_CN_V)_{Si}}\frac{\mu_{n(SiGe)}(T)}{\mu_{n(Si)}(T)} \tag{2.36}$$

The factor C does not to vary strongly with temperature and so is assumed constant in the analysis. It should be noted that the plot should intercept the vertical axis at unity, any deviation from which implies either inaccuracies in the model parameters or the existence of parasitic energy barriers. The latter effect will be apparent from

a reduction in the slope of the graph signifying a reduction in the collector current enhancement.

It has been shown in section 2.6.1 that the introduction of a non-uniform Ge profile can result in a non-ideal collector current. In order to ascertain whether this could introduce significant errors in the value of the extracted bandgap narrowing, the effects of incorporating the non-ideality factor have been calculated. By comparing the saturation current density for the ideal case ($J_O(T)$), as shown in equation 2.34, with the non-ideal case, the error introduced by assuming an ideal collector current can be calculated. This corresponds to :

$$\frac{J_{O(non-ideal)}(T)}{J_{O(ideal)}(T)} = exp\left(\frac{qV_{BE}}{kT}\frac{1-n_c}{n_c}\right) \tag{2.37}$$

From equation 2.37, it can be seen that assuming an ideal collector current will result in an overestimation of the extracted bandgap narrowing value. In addition it can be seen that the overestimation will be at its worst at the lowest measurement temperature. Figure 2.10 shows the expected error in the extracted bandgap narrowing value, as a function of ideality factor, for measurement temperatures of 200K and 300K . It can be seen that the errors introduced are not significant until the ideality factor is well above 1.1, and is only about 0.5meV for an ideality of 1.02. Since transistors exhibiting ideality factors in excess of 1.02 would be excluded from the analysis, it can be concluded that the extraction method is still valid for arbitrary shaped Ge profiles and that any non-linearities in the collector current resulting from these profiles can be ignored.

2.9 Conduction Mechanisms in Polycrystalline Silicon

In order to ascertain how carbon is influencing the electrical properties of poly$Si_{1-y}C_y$ and poly$Si_{1-x-y}Ge_xC_y$ layers grown in this work, the conduction mechanisms of polySi must first be considered. Investigations by several authors [92–95], have shown that the electrical properties of polySi are markedly different from those of single-crystal silicon. At low dopant concentrations, the resistivity of polySi is

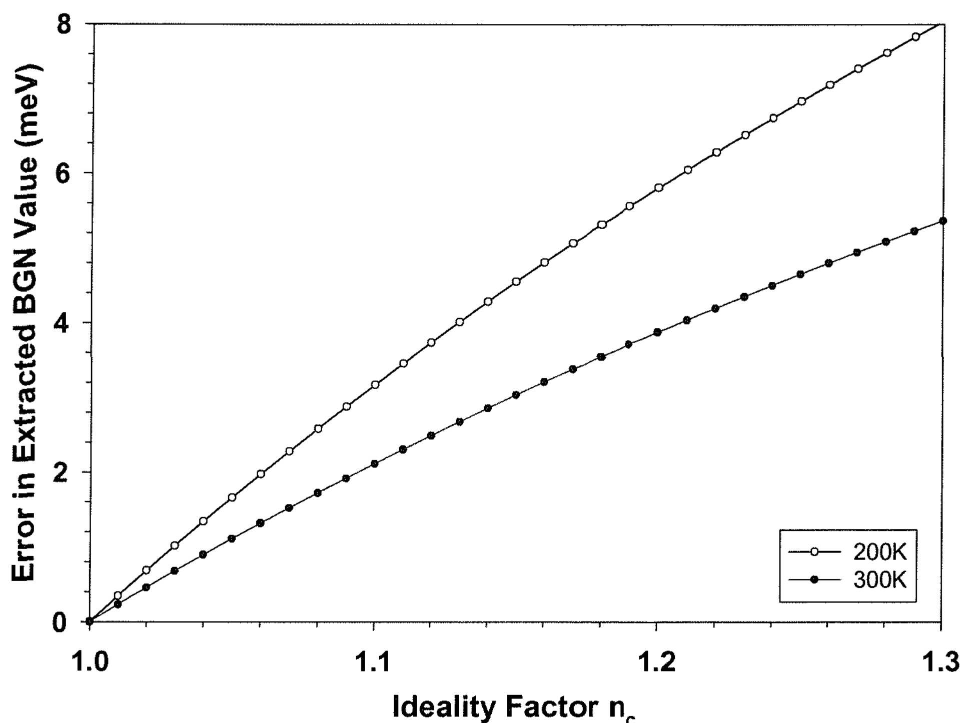


Figure 2.10: Graph of expected error in the extracted bandgap narrowing plot assuming an ideal collector current vs the actual ideality factor.

several orders of magnitude higher and insensitive to dopant concentration. At medium doping concentrations, a small increase in doping concentration leads to a significant decrease in the resistivity, whilst at high dopant concentrations, the resistivity approaches that of single-crystal silicon, but remains slightly higher. This behaviour is shown in figure 2.11 [96].

Polysilicon is composed of small, randomly orientated, single-crystal crystallites joined together by grain boundaries (figure 2.12). The grain boundary is a complex structure of disordered atoms that represents the transitional region between the different orientations of neighbouring crystals [94]. Traditionally, two models have been proposed for the variation of resistivity with dopant concentration. The first model, the dopant segregation model [97,98], hypothesises that the conductivity of the polySi layer is controlled by segregation of dopant atoms to the grain boundary. Once segregated, the dopant atoms become trapped and electrically inactive. The variation in resistivity is therefore explained by the fact that at low dopant concentrations, most of the dopant atoms segregate leaving fewer to contribute to conduction, whilst at higher dopant concentrations, more dopant remains in the crystallite leading to a sharp drop in the resistivity.

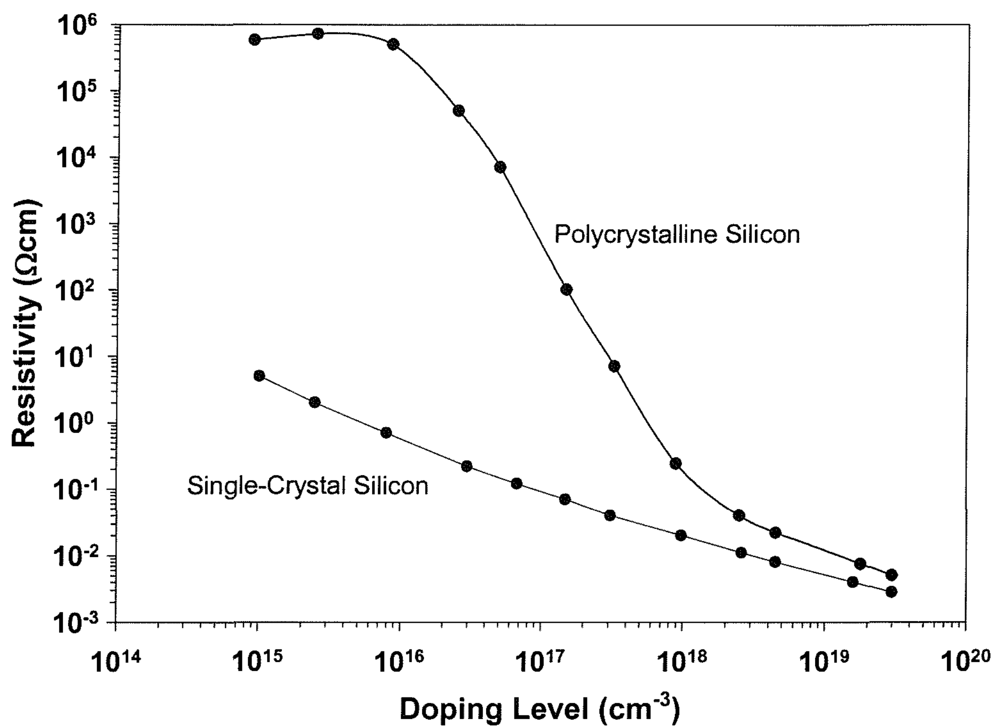


Figure 2.11: Graph of resistivity vs doping for single-crystal and polycrystalline silicon. After Kamins [96].

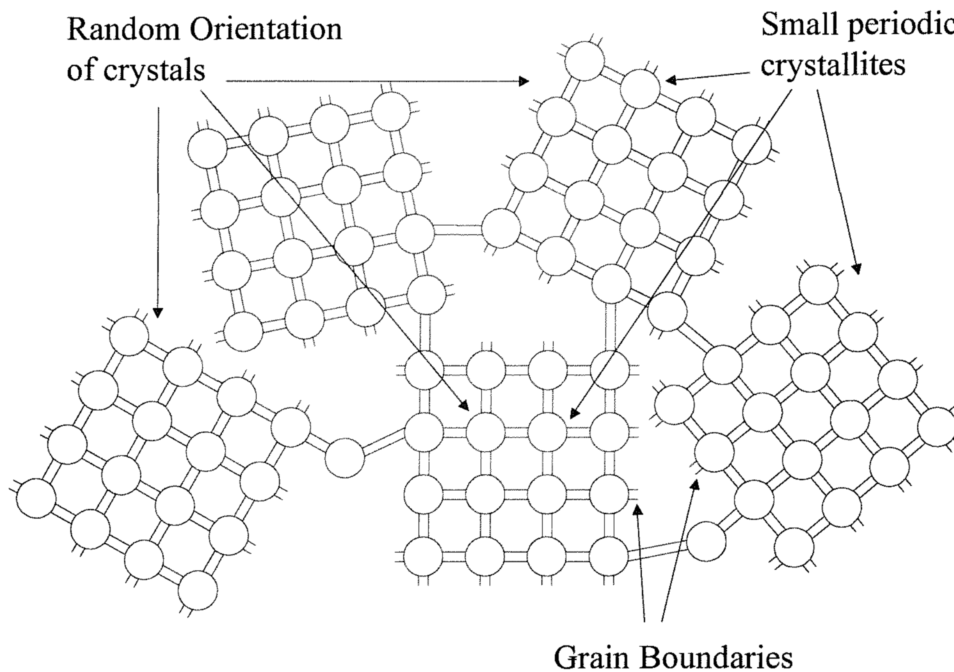


Figure 2.12: Schematic diagram of the structure of polycrystalline silicon, showing small periodic crystallites that are randomly orientated.

The second model, the carrier trapping model [93–95], hypothesises that the dopant atoms are uniformly distributed throughout the material and that the conductivity is limited by carrier trapping at the grain boundaries, caused by the large number of defects in the disordered region between the crystallites. This trapping of free carriers causes the formation of potential energy barriers at the grain boundaries, thereby impeding the flow of carriers from one crystallite to another.

Each model has tried to explain the electrical properties of polySi whilst completely neglecting the other, and both have been successful at modeling the variation of resistivity with total dopant concentration. However, the carrier trapping model has become more generally accepted since the dopant segregation model cannot explain the temperature dependence of the resistivity and the minimum in the Hall mobility observed at intermediate dopant concentrations [94]. Nevertheless, segregation has been observed by several research groups, particularly in n-type polysilicon. Its influence on conduction in polysilicon cannot therefore be entirely neglected.

2.9.1 Grain Boundary Carrier Trapping

As discussed earlier, the carrier trapping model hypothesises that defects at the grain boundaries trap free carriers causing the formation of a potential barrier at the grain boundary, thereby impeding the flow of carriers from one grain to another. The simplest carrier trapping model uses the assumption that a discrete energy level exists at the grain boundary and that the Fermi level is pinned close to this level until all of the traps are filled by the addition of more dopant. In addition, the similar behaviour of n- and p-type polysilicon layers indicates that either type of majority carrier can be trapped at the grain boundary, suggesting that the grain boundary traps are located near mid-gap (figure 2.13). However, investigations have shown that for p-type layers the resistivity and its activation energy decreases monotonically with doping concentration [99]. In contrast, for n-type layers, the resistivity and its activation energy first increase as dopant is added, and then decreases for higher concentrations. This suggests that the dominant trap level is actually located below mid-gap, and has been found to be approximately 0.62eV below the conduction band edge [100].

The grain boundary potential energy barrier arises because of the need to maintain charge neutrality, leading to compensation of the trapped charge by the formation of depletion regions around the grain boundaries. The height of the energy barrier

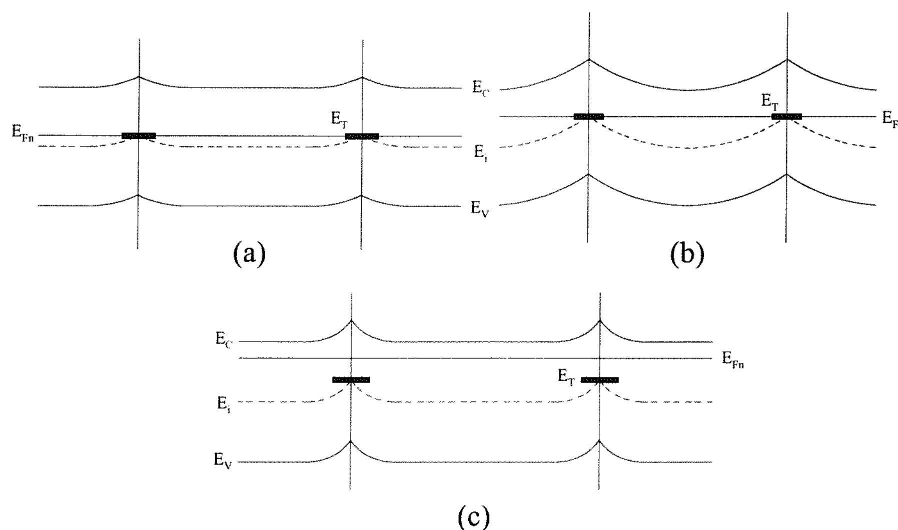


Figure 2.13: Schematic diagram of the energy band structure in n-type polysilicon for (a) a low doping level ($N \leq N^*$), (b) an intermediate doping level ($N \approx N^*$) and (c) a high doping level ($N \geq N^*$). In each case a single dominant trap level, located in the middle of the energy gap, has been assumed.

V_B can be expressed in terms of the dopant concentration N and the depletion region width x_d using the one dimensional case of Poisson's equation [96]:

$$\frac{d^2V}{dx^2} = \frac{qN}{\epsilon} \tag{2.38}$$

Solving for V_B gives

$$V_B = \frac{qN}{2\epsilon}{x_d}^2 \tag{2.39}$$

which can be alternatively expressed as

$$E_B = \frac{q^2N}{2\epsilon}{x_d}^2 \tag{2.40}$$

From equation 2.40 it can be seen that the energy barrier height is strongly dependent on the dopant concentration within the layer and the grain boundary trap density, since the grain boundary depletion region width is a function of trap density. For polysilicon layers containing low dopant concentrations, the total number of free carriers per unit area NL, in a grain of length L, is much less than the number of traps N_T per unit area. Therefore, provided that the energy of the defects is low enough, nearly all of the free carriers are trapped at the grain boundary, leaving very few available for conduction [96]. Because the dopant concentration is low, the grain boundary depletion regions extend throughout the whole grain and no neutral region exists. In addition, the low dopant concentration also means that the energy bands within the grain have little curvature, resulting in only a small energy barrier (figure 2.13(a)). This small barrier and low free carrier density result in a polysilicon layer whose resistivity approaches that of intrinsic silicon [96]. The height of the energy barrier in this case is found by putting the depletion region width x_d equal to half the grain size L/2 i.e. the depletion region associated with the grain boundary extends halfway across the grain from each side. This gives E_B as

$$E_B = \frac{q^2N}{2\epsilon}\left(\frac{L}{2}\right)^2 = \frac{q^2NL^2}{8\epsilon} \tag{2.41}$$

As the dopant concentration increases, more free carriers are trapped at the grain boundaries, and both the curvature of the energy bands and the potential energy barrier increase (figure 2.13(b)), thereby compensating the effect of the additional carriers and keeping the resistivity high. In the simplest case, it is assumed that the energy of the traps is low enough that they are completely filled before a neutral region forms [94]. Using this assumption a critical dopant concentration can be defined at which the neutral region begins to form and is given by equation 2.42.

$$N^* = \frac{N_T}{L} \tag{2.42}$$

Above this critical doping concentration, the number of trapped carriers per unit area saturates at a level N_T, allowing the additional free carriers begin to form neutral regions within the grains (figure 2.13(c)). Since charge neutrality must be maintained, the width of the depletion regions decreases according to the relation

$$x_d = \frac{N_T}{2N} \tag{2.43}$$

Substituting equation 2.43 into equation 2.40 gives

$$E_B = \frac{q^2 N}{2\epsilon}\left(\frac{N_T}{2N}\right)^2 = \frac{q^2 {N_T}^2}{8\epsilon N} \tag{2.44}$$

which is the energy barrier height for dopant concentrations above N*. Therefore, from equations 2.41 and 2.44, it can be seen that the grain boundary potential energy barrier first increases, reaches a maximum when the dopant concentration N equals N*, and then decreases rapidly as more dopant is added. This is shown schematically in figure 2.14.

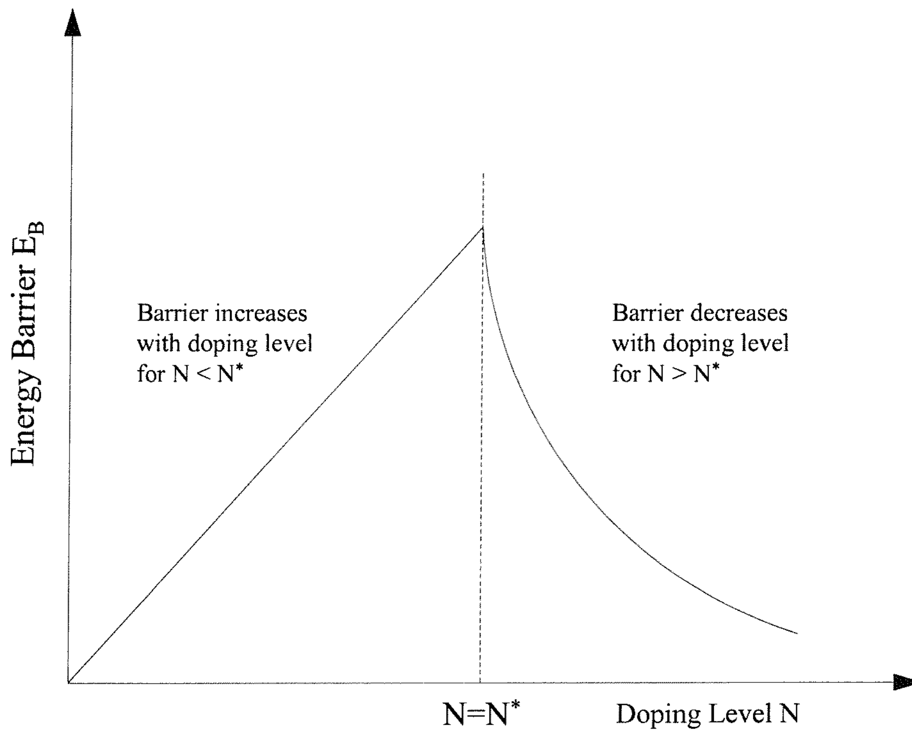


Figure 2.14: The barrier height increases with doping concentration until the critical doping concentration N* is reached. Above this level neutral regions form in the grain and the barrier decreases.

2.9.2 Effects of Carrier Trapping on Resistivity

In order to consider the effects of grain boundary barrier trapping on the resistivity of the layer, an expression describing the relationship between current flow and applied voltage must be derived. As stated earlier, at low dopant concentrations the polysilicon grains are fully depleted since the depletion regions extend halfway across the grain from each side. As the dopant concentration is increased, neutral regions begin to form and the depletion regions reduce in width. However, using equation 2.43, a depletion region width of 50nm can be calculated for a dopant concentration and trap density of 10^{17}cm^{-3} and 10^{12}cm^{-2} respectively. For barriers of this width, the free carriers travel from one grain to another by thermionic emission over the barrier [96]. When thermionic emission dominates, the current flow in the polysilicon layer is given by

$$J = \frac{q^2 n v_c V_G}{kT} exp\left(-\frac{qV_B}{kT}\right) \tag{2.45}$$

which gives a linear relationship between current and applied voltage. The derivation of equation 2.45 is shown in appendix B. The average resistivity of the layer can now be found by dividing the electric field across the grain (V_G/L) by the current density, giving

$$\rho = \frac{kT}{q^2 n v_c L} exp\left(\frac{qV_B}{kT}\right) \tag{2.46}$$

From equation 2.46 it can be seen that the resistivity is thermally activated with an activation energy equal to the energy barrier height, which is itself a function of dopant concentration and grain size. At low dopant concentrations, the grain boundary traps are not fully filled so the free carrier concentration is low, resulting in a high resistivity. As more dopant is added, the barrier height increases due to increased trapped charge, thereby compensating the additional free carriers associated with the increased dopant concentration. Therefore the resistivity remains high. As the dopant concentration exceeds the critical doping concentration N^*, the grain boundary traps are saturated and the additional free carriers can form neutral regions in the grains, thereby lowering the grain boundary barriers and causing a

dramatic decrease in the resistivity. Also from equation 2.46 it can be seen that plotting the natural log of the resistivity as a function of temperature will give an Arnhenius plot whose activation energy will be related to the grain boundary energy barrier height. Lee *et al* [101] have shown that due to the shift in the Fermi level with temperature, the relationship between the activation energy and the energy barrier height is given by

$$E_a = qV_B(1 + \Psi T) \tag{2.47}$$

where $\Psi \approx 1.5 \times 10^{-3}/K$ [102]. For low dopant concentrations, below the critical dopant concentration, the grains are fully depleted and the activation energy of the resistivity will be approximately half the bandgap for polysilicon. This arises since the Fermi level is pinned near mid-gap due to the unfilled grain boundary traps. At dopant concentrations above the critical dopant concentration, the formation of the neutral region in the grain means that the free carrier concentration n in equation 2.46 is approximately equal to the dopant concentration N, and the resistivity becomes proportional to

$$\rho \;\alpha\; \frac{1}{N} exp\left(\frac{q^2 {N_T}^2}{8\epsilon kTN}\right) \tag{2.48}$$

Therefore, for doping levels above N*, it can be seen that the resistivity and activation energy both decrease with doping concentration (figure 2.15) until other conduction mechanisms, such as impurity scattering, limit the conduction process at very high dopant concentrations. At these levels, the conduction process is no longer thermally activated and equation 2.46 is not valid.

2.9.3 Effects of Carrier Trapping on Mobility

The effects of carrier trapping on the mobility can be modeled by considering an effective mobility that allows the resistivity to be expressed in the more usual form:

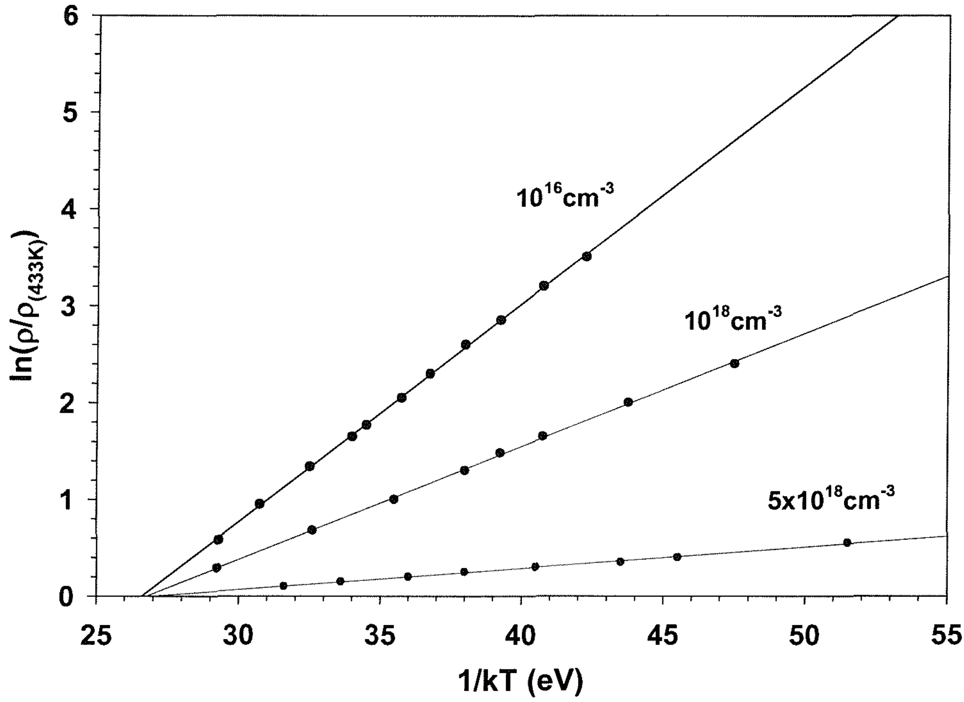


Figure 2.15: Logarithm of the normalised resistivity as a function of reciprocal temperature for polysilicon layers doped at 10^{16}cm^{-3}, 10^{18}cm^{-3} and 5×10^{18}cm^{-3}. After Seto [94].

$$\rho = \frac{1}{qn\mu} \tag{2.49}$$

Comparing equations 2.46 and 2.49, it can be seen that this would give an effective mobility that can be defined as

$$\mu = \frac{qv_cL}{kT} exp\left(-\frac{qV_B}{kT}\right) \tag{2.50}$$

In this case the effective mobility no longer describes the traditional mobility used for single-crystal semiconductors, but rather how easily carriers can move between grains. It can be seen from equation 2.50 that the mobility is strongly dependent on the energy barrier at the grain boundary, which is itself dependent on the boundary trap density and the doping level within the layer. As dopant is added to undoped polysilicon, the energy barrier increases due to increased trapped charge at the grain

boundary. This causes a corresponding decrease in the mobility until the dopant level reaches the critical concentration N*. Above this level, the grain boundary energy barrier decreases with increasing dopant level due to formation of a neutral region within the grain. This reduction in the energy barrier causes a corresponding increase in the mobility. Therefore it can be seen that equation 2.50 describes a mobility that first decreases with increasing doping level, has a minimum value around the critical dopant concentration N*, and then increases as more dopant is added. This is fully consistent with the observed experimental results of Seto [94], shown in figure 2.16. It should be noted however, that at very high dopant

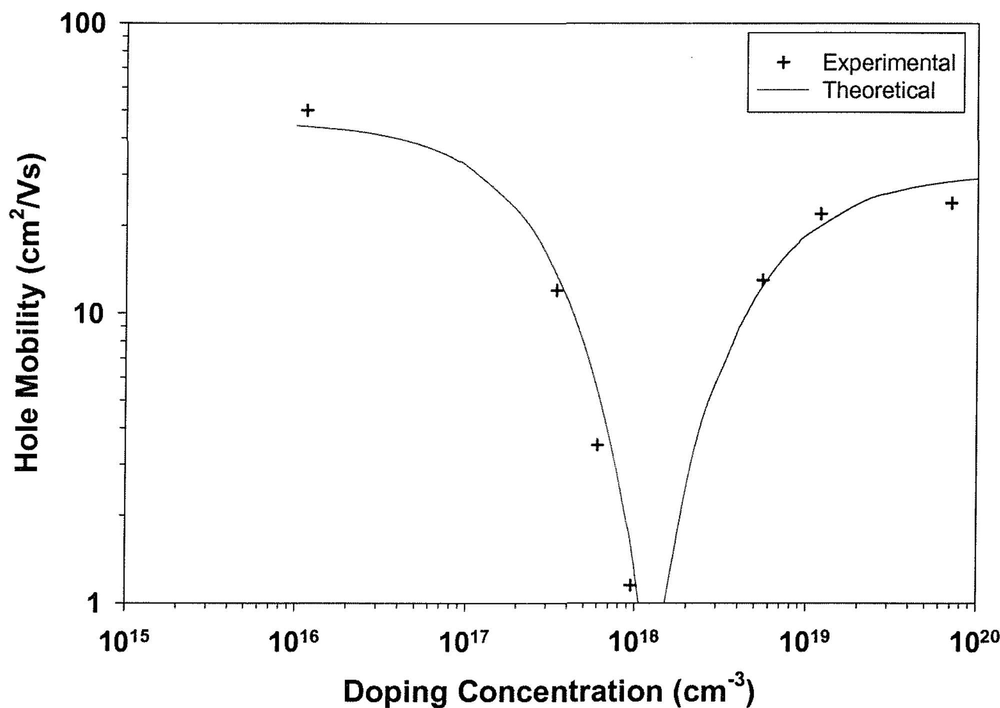


Figure 2.16: Plot of Hole mobility vs doping concentration showing a clear minimum at a doping level of around 10^{18}cm^{-3}. After Seto [94].

concentrations the energy barrier is so small that it no longer limits the mobility. In this regime, the mobility is now dominated by mechanisms traditionally associated with single-crystal silicon, such as ionised impurity scattering, resulting in a decrease in the mobility with increasing doping level. This leads to similar trends in the mobilities of polysilicon and single-crystal silicon at high doping concentrations, with the magnitude of the former being about a factor of two lower due to additional scattering from the additional defects in the material.

2.10 Hall mobility and effective carrier concentrations

In this section, the calculation of the Hall mobility and effective carrier concentration from van der Pauw measurements will be discussed. The extraction of Hall mobility and effective carrier concentration from deposited poly-Si and poly-SiGe films, discussed in chapter 5, will allow full electrical analysis of the layers, giving insight as to whether any differences in resistivity are due to increased mobility and/or dopant activation. Figures 2.17 and 2.18 show schematic diagrams of the setup for measurement of the resistivity and Hall voltage. For a symmetrical structure, the resistivity is given by equation 2.51 [103]

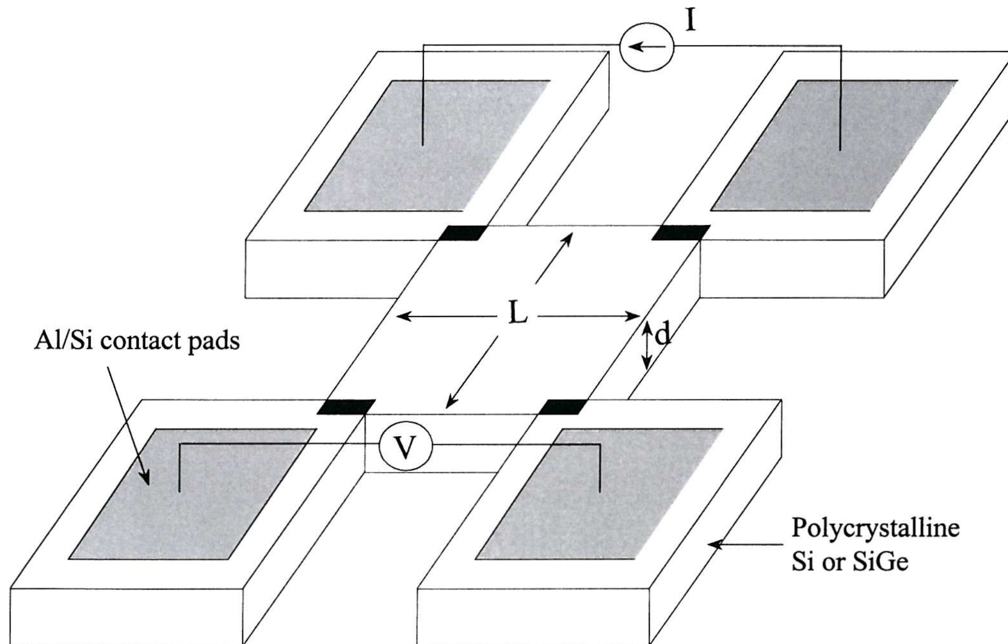


Figure 2.17: Schematic diagram of the van der Pauw structure used to measure the resistivity of in-situ doped polySi and polySiGe layers.

$$\rho = \frac{\pi d}{ln2} \frac{V}{I} \tag{2.51}$$

where d is the layer thickness and V is the measured voltage across two terminals for a current injected through the opposite two.

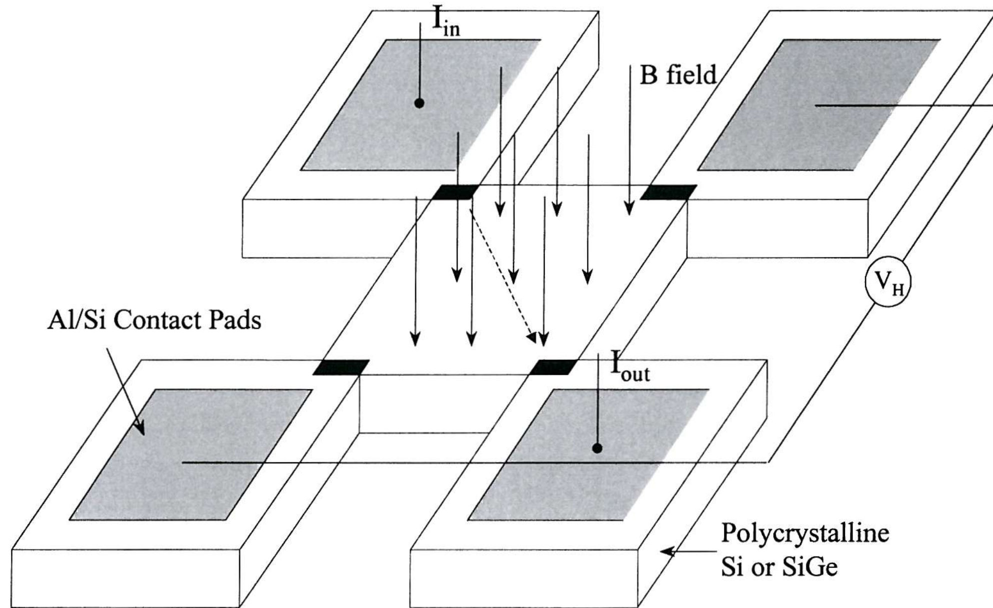


Figure 2.18: Schematic diagram of the van der Pauw structure used to measure the Hall voltage of in-situ doped polySi and polySiGe layers

The Hall voltage arises from the effect of the magnetic field on the current passing through the layer, pushing the carriers, electrons in the case of an n-type layer, towards the back of the semiconductor. As the carriers are pushed to the back of the layer, the front becomes depleted of carriers and the semiconductor loses neutrality. In the case of an n-type semiconductor, this will cause the front of the layer to become more positive with respect to the back, giving rise to a measurable voltage, termed the Hall voltage. The magnitude of this voltage is determined by the balance reached between the electric field E_H and the magnetic field B, such that the forces exerted on the carriers are equal and opposite. For a magnetic field normal to the current density, this can be expressed as :

$$JB + nqE_H = 0 \tag{2.52}$$

where

$$E_H = -\frac{JB}{nq} \tag{2.53}$$

A Hall coefficient, R_H, can be defined as :

$$R_H = \frac{E_H}{JB} = -\frac{1}{nq} \tag{2.54}$$

for n-type semiconductors. The Hall mobility can now be calculated using the Hall coefficient in the standard expression for resistivity i.e.

$$\rho = \frac{1}{nq\mu_n} = \frac{R_H}{\mu} \tag{2.55}$$

giving the Hall mobility as

$$\mu_H = \frac{|R_H|}{\rho} \tag{2.56}$$

Chapter 3

Experimental Procedure

3.1 Introduction

In this chapter the experimental procedures used to study the effect of carbon on the temperature dependence of the collector current of a SiGe heterojunction bipolar transistor are described. In addition details of the LPCVD system used in the study of in-situ doped amorphous Si, SiGe and SiGe:C layers are given. Section 3.2 describes the methods used to measure the temperature dependence of the collector current and base sheet resistance. Sections 3.3 and 3.4 briefly describe the extraction techniques used to determine the metallurgical basewidth and the emitter, collector and base doping levels. Section 3.5 gives details of the low pressure CVD reactor and growth procedures used to produce in-situ phosphorus doped amorphous layers. Finally some conclusions are drawn in section 3.6.

3.2 Electrical Measurements at Low Temperatures

In this work the temperature dependence of the collector current, base current and intrinsic base sheet resistance are measured. The current measurements were taken in common emitter mode, with the base and collector grounded and a negative potential applied to the emitter. The sheet resistance measurements were made in two ways depending on the transistors being tested. For the devices fabricated completely by the Institut fur Halbleiterphysik (IHP), the intrinsic base sheet resistance

was measured using a transistor with two base contacts. A small current, 1-10μA, was injected through the base layer of the transistor, with known dimensions of 150μm × 100μm, and the voltage drop across it measured. This is shown schematically in figure 3.1. Alternatively, for the devices fabricated at the Southampton University Microelectronics Centre (SUMEC), measurements of the base sheet resistance were made using van der Pauw structures with an area of 120μm by 120μm. For this method, a slightly larger current (20-100μA) was injected through a pair of terminals and the voltage drop measured across another pair. The measurement was repeated another three times by rotating the probes clockwise around the structure. An average value was then taken for the four different probe positions. A schematic diagram of the pad connections for the van der Pauw measurement is shown in figure 3.2. In all cases the measurement temperature was varied between 160K and 400K, at 20K intervals, in order to study any effects on the electrical characteristics of the devices under test.

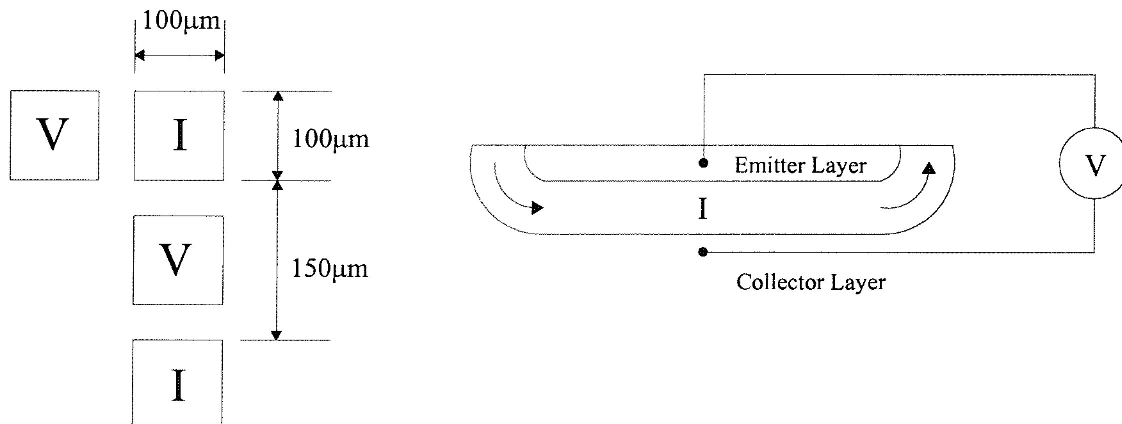


Figure 3.1: Schematic diagram showing the measurement of the resistance under the emitter for the devices fabricated at the Institut fur Halbleiterphysik.

3.2.1 The low temperature measurement setup

The low temperature measurement setup is shown in figure 3.3. The device was mounted on the cryostat cold finger, using heatsink compound to obtain good thermal contact, and the chamber evacuated to a pressure of approximately 50mTorr. The evacuation of the chamber is an important step to remove residual contaminants, such as water vapour, and to minimise heat loss from the sample and thermal fluctuations within the chamber.

The temperature is controlled by a closed loop feedback system that maintains the set point temperature by either varying the flow of liquid nitrogen to the chamber or

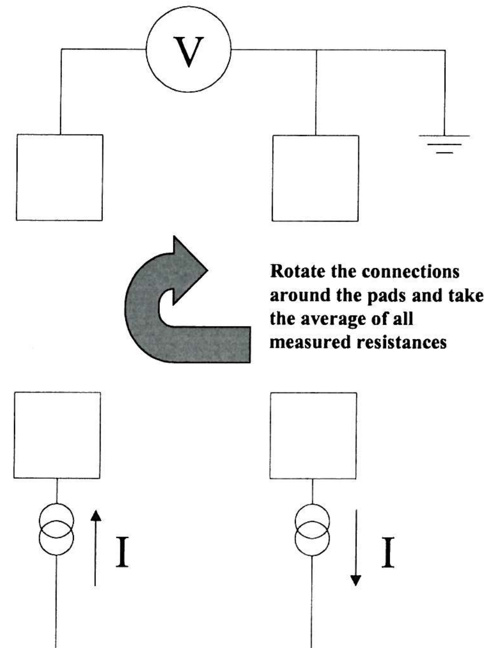


Figure 3.2: Schematic diagram showing the pad connections for the van der Pauw measurements to extract the base sheet resistance.

by heating the sample via a small built in heater within the cold finger. The feedback in the system is provided by a 100Ω platinum resistance thermometer within the cryostat chamber, located approximately 5mm from the sample. The required set point temperature is determined by thumb-wheel switches mounted on the DLTS temperature controller, with two modes available. The first mode is the RESET mode which uses a single set point to determine the sample temperature. This method was found to be unsatisfactory since a constant temperature could not be maintained for long enough periods to allow the electrical measurements to be taken. The second mode, the CYCLE mode, uses a start and stop set point which the controller cycles between. By setting both set points to the same temperature it was found that the fluctuations observed when using the RESET mode were significantly minimised, allowing more accurate measurements to be made. Therefore in this work the CYCLE mode was used throughout.

3.2.2 Sample preparation

Before the temperature dependence measurements could be performed, some sample preparation was required. This entailed sawing the finished wafers into small

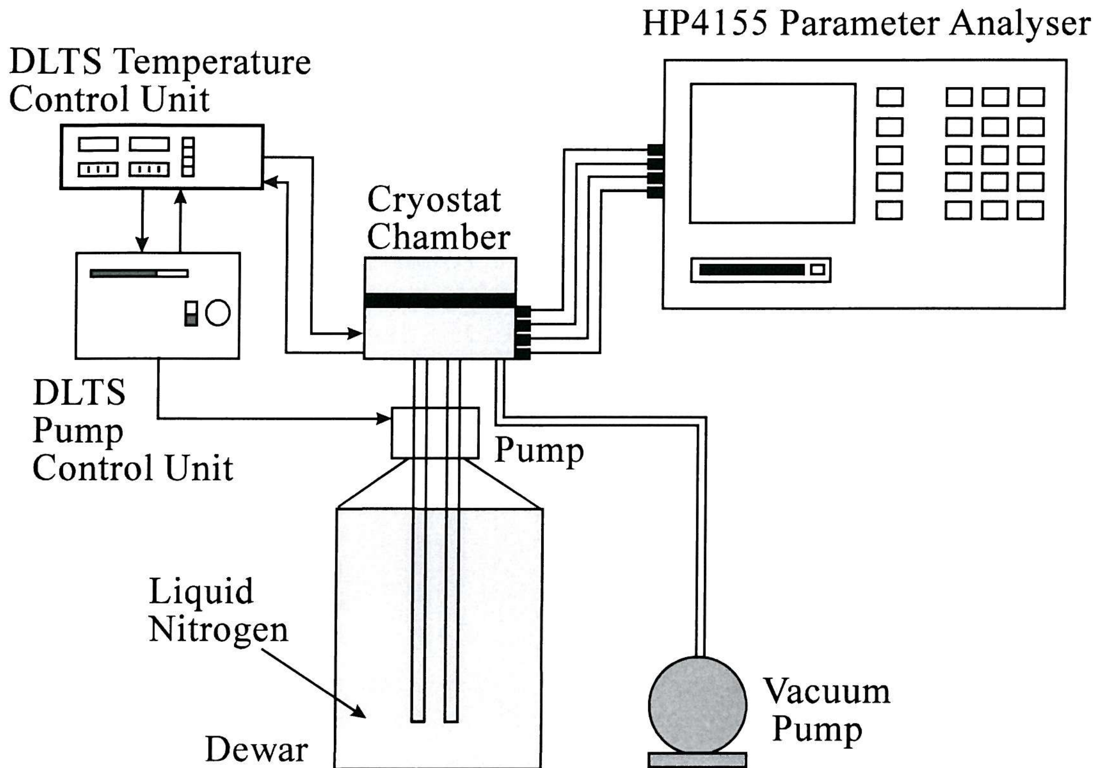


Figure 3.3: Experimental setup used in the low temperature measurements.

individual chips and then mounting the required chips onto a high thermal conductivity ceramic substrate. Connections to the chip were provided by bonding gold filament wires between the device contact pads and external gold pads on the ceramic substrate. Both the transistor and base sheet resistance structure were bonded out to the gold contact pads, allowing two measurements to be performed without disturbing the sample. This ensures that any temperature deviations from the set point temperature, due to thermal contact between the sample and the cryostat cold finger, are identical for the collector current measurement and sheet resistance measurement. The sample preparation is shown schematically in figure 3.4.

Once sample preparation was complete, the substrate was firmly mounted on the cryostat cold finger, using a heat conducting paste to obtain good thermal contact. Probes were then brought into contact with the gold pads and room temperature measurements of the collector current and base sheet resistance performed to ensure sufficient contact had been made. The chamber was then evacuated and cooled to the minimum temperature of 160K, at a cooling rate of approximately 0.5K/sec. The coolest temperature was chosen first for two reasons. Firstly, the seal on the dewar was not sufficient to stop the liquid nitrogen escaping into the atmosphere,

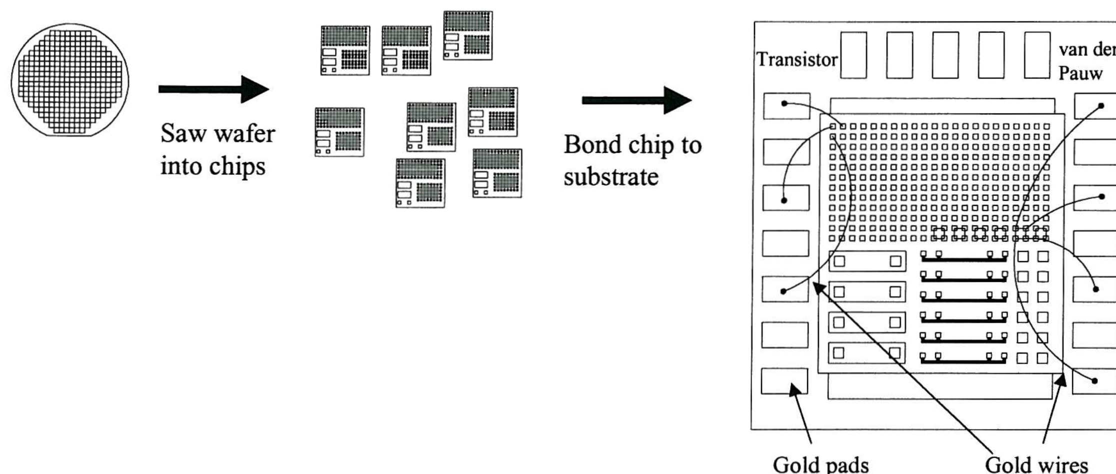


Figure 3.4: Schematic diagram showing sample preparation to allow temperature dependence measurements to be made.

giving a finite usage time of approximately two complete temperature sweeps. Since the lowest set point requires the most liquid nitrogen flow, it is sensible to perform these measurements first to ensure two complete runs can be performed without interruption. Secondly, the DLTS temperature controller appeared to be able to reach the required set point much faster when heating from a lower temperature, with much less overshoot. This reduces the settling time and hence speeds up the measurement process. During the cooling process, quick measurements were made continuously using the repeat feature of the HP4155 parameter analyser. No data was stored during this period, but this provided a quick visual check that good contact between the probes and the gold contact pads had been maintained.

As stated earlier, the measurements were taken in the range of 160K to 400K, in 20K intervals. At each measurement temperature, the sample was left at the set point for two minutes to allow thermal equilibrium to be achieved, before any measurements were taken. Once this time had elapsed, Gummel and base sheet resistance measurements were performed. For the Gummel measurements, the base and collector were grounded and a negative potential applied to the emitter, from -0.2V to -1V in -0.01V steps. In cases where increased collector-base reverse bias was required, the ground connection to the collector was replaced by a positive potential of between 1 and 2V, depending on the device. The sheet resistance measurements were performed as discussed earlier in section 3.2. In all cases the

measured data was stored in ASCII data files which could then by formatted and processed accordingly.

3.2.3 Temperature measurement

As stated in section 3.2.1 the temperature within the cryostat was measured by a 100Ω platinum resistance thermometer, located approximately 5 mm from the sample. This distance introduces a thermal lag between the sample and the measured point which would cause significant errors in the bandgap narrowing extraction. To avoid these possible errors, the sample temperature was calculated from the linear region of the measured collector current, using equation 3.1, and is shown in figure 3.5.

$$T = \frac{q}{n_c k} \frac{V_{BE1} - V_{BE2}}{ln(I_{C1}) - ln(I_{C2})} \tag{3.1}$$

where V_{BE1}, V_{BE2}, I_{C1}, and I_{C2} are pairs of base-emitter biases and corresponding collector currents respectively. In calculating the temperature the ideality factor, n_c, was assumed to be unity. This assumption has been validated by previous experimentation [80] and was shown not to introduce any significant error (± 0.2K) into the temperature data.

In order to minimise the error in the calculated temperature, the calculation was made over the entire linear region of the collector current, resulting in an almost constant value, as can be seen from figure 3.5. In addition small bias steps, 10mV, were used to give an increased number of calculation points.

Previous work [80] has shown that the low temperature analysis is sensitive to noise, thus making the correct choice of data acquisition essential. Room temperature measurements of collector current were taken using the HP4145 and HP4155 parameter analysers and the temperatures calculated using equation 3.1. These results showed that at low bias voltages, 0.35-0.5V, the noise level in the calculated temperature for the HP4155 was approximately ±0.5K as opposed to ±1.5K for the HP4145 [80]. In addition the noise figure is also affected by the choice of *sweeping mode.* The HP4155 allows three modes, short, medium and long. The short mode

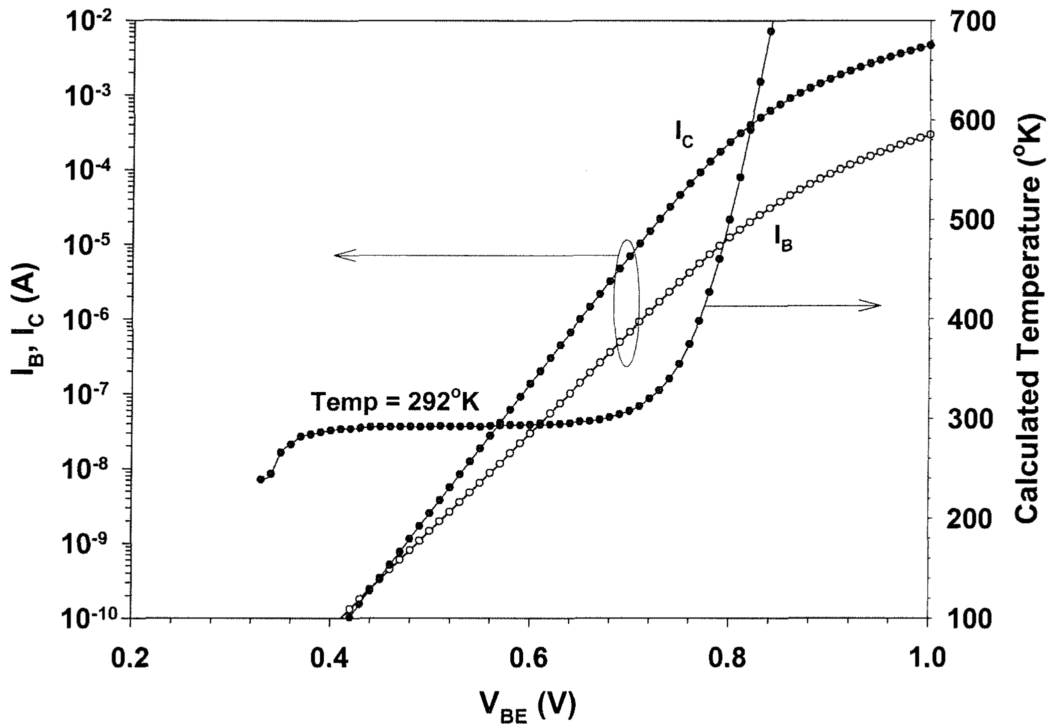


Figure 3.5: Sample temperature determination from the measured collector current using equation 3.1.

takes the value of the measurand over a single sweep, medium mode takes the average of 16 runs per bias point and the long mode takes the average of 256 runs per bias point. Obviously medium or long modes are preferential since an average of a number of runs should minimise the noise error. Therefore throughout this work all electrical measurements were made using an HP4155 parameter analyser running in long mode.

Finally, the collector current at a particular bias, V_{BE}=0.6V, is used to extract bandgap narrowing data by applying the analysis described in chapter 2. However at high and low temperatures this particular bias point is outside the linear region, the former due to collector series resistance and the latter due to measurement limitations of the HP4155. In these cases the collector current is measured at an alternative bias point, within the linear region, and a new value extrapolated, assuming an ideality factor of unity, for the desired bias point of $V_{BE} = 0.6$V.

3.3 SIMS analysis

In order to apply the electrical analysis described in section 2.8, a knowledge of the doping profiles within the device is needed. These profiles are required to allow the calculation of the neutral basewidth, and hence the mean base doping, and to allow comparisons between extracted and theoretical bandgap narrowing values. Secondary ion mass spectroscopy (SIMS), performed by Loughbrough Surface Analysis Ltd, was the primary tool used to provide the doping profile information, using a special SIMS bar located down one side of each chip. The SIMS bar was subjected to the same fabrication process as the devices, and its close proximity to the actual test device should ensure that the SIMS data is representative of the actual device profiles.

The analysis was initially performed using 10keV 0_2^+ primary ion bombardment and positive secondary ion detection to optimise the sensitivity to boron. Optimum sensitivity to C and As was achieved using 10keV Cs^+ primary ion bombardment and negative secondary ion detection. The SIMS data was quantified using implanted reference materials, whilst the depth scales were determined by measuring the sputtered crater depths by interference microscopy. The determination of the actual Ge content is more complicated than the other measured species since the measured secondary ions of Si_{30} and Ge_{74} bear no direct relationship to the actual layer composition [104]. Therefore in order to calculate the Ge content, a reference sample containing 20% Ge is analysed, using identical bombardment conditions, and the Si:Ge ratio of this layer is compared to the Si:Ge ratio of the devices. The Ge content can then be extracted using equation 3.2:

$$Ge\% = 20\% \times \frac{Si : Ge\ ratio\ of\ device}{Si : Ge\ ratio\ of\ reference} \tag{3.2}$$

The emitter/base metallurgical junction could not be found directly from the SIMS data since an artifact is introduced into the measurement when attempting to detect As in the presence of Ge. This occurs because interference occurs from $Ge_{74}H$, which has the same signal mass of 75 required to detect arsenic. Therefore the data for the As profile is truncated prior to the Ge profile and the metallurgical junction estimated by linear interpolation of the slope down to the intersection with the boron profile. This is shown in figure 3.6.

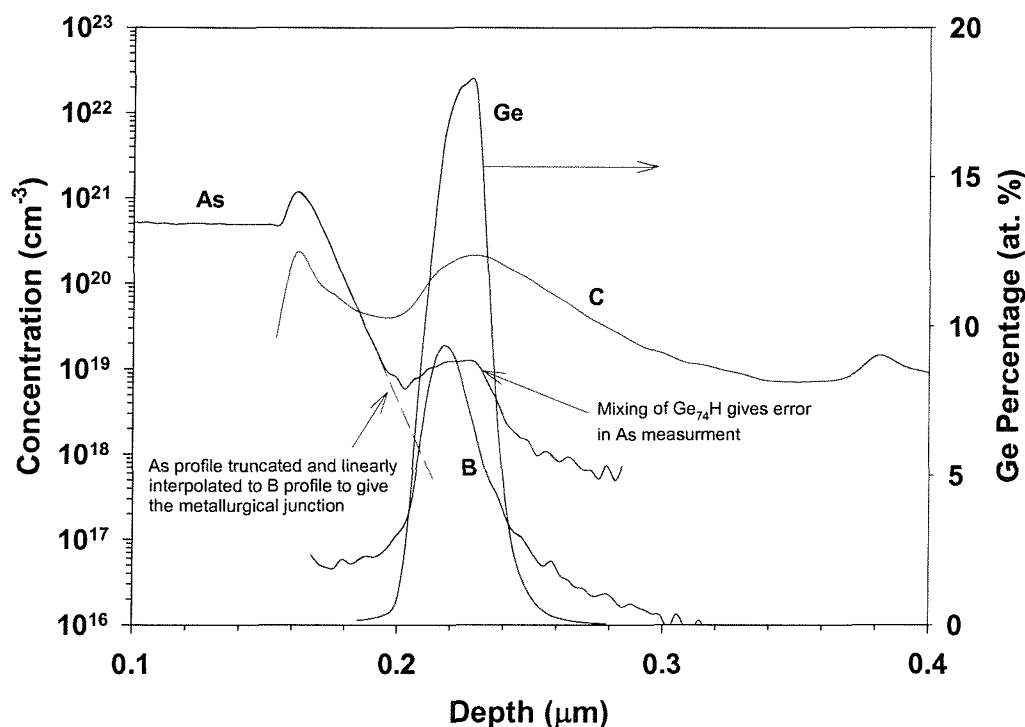


Figure 3.6: Example of SIMS profiles for an SiGe HBT showing how the E/B metallurgical junction is determined.

3.4 Mean base doping

The mean base doping for the SiGe and SiGe:C HBTs was calculated, using equation 2.26, from the intrinsic base sheet resistance, measured at a temperature of 300K. The calculation was performed using a specially designed C program that iteratively alters the doping level until the measured and calculated sheet resistances are equal. At each new doping concentration, the penetration of the emitter/base and collector/base depletion regions into the base, and the hole mobility are recalculated to ensure maximum accuracy. The hole mobility was calculated using the full Klaassen unified mobility model [89,90], taking into account lattice scattering, impact ionisation, majority and minority carrier scattering and temperature effects. The metallurgical basewidth was determined from the SIMS analysis of the devices, and the junctions taken at the point where the boron profile in the base coincides with a doping level of $1 \times 10^{16}\text{cm}^{-3}$ in the collector and $1 \times 10^{18}\text{cm}^{-3}$ in the emitter. This figure was then corrected using the calculated depletion region penetrations to give the neutral basewidth in the base.

This technique has the advantage that only the electrically active dopant level is extracted, as opposed to other techniques, such as integrating the SIMS profile

which gives the mean base doping level due to both active and inactive dopant.

3.5 The LPCVD reactor and wafer preparation

3.5.1 The LPCVD reactor

The LPCVD reactor used in this work uses a UHV compatible, stainless steel, cold wall chamber with a typical working pressure of 1mTorr, shown schematically in figure 3.7. The wafer is heated by a 10kW carbon two zone graphite heater, which is closed loop controlled via an Eurotherm temperature controller and a K-type thermocouple located above the heater. The positioning of the thermocouple means that the measured heater temperature will not coincide with the wafer temperature, requiring calibration runs to be performed. This was carried out using an infra-red pyrometer over a wide range of set point temperatures, creating a lookup table that relates the controller temperature to the wafer temperature. This is shown in table 3.5.1.

Table 3.1: Temperature calibration lookup table relating controller set point temperatures to wafer temperatures.

Wafer Temperature °C	Inner Set Point °C	Outer Set Point °C
514	500	480
549	550	530
586	600	580
623	650	630
664	700	680
706	750	720
749	800	770
792	850	820
836	900	870
880	950	920
925	1000	970
970	1050	1020

To minimise contaminants in the growth chamber, the wafer is first loaded into a loadlock chamber, which is then evacuated to the same base pressure (1mTorr)

as the growth chamber. Vacuum pumping is provided by an Edwards dry pump, common to both the loadlock and the growth chamber, which is interlocked to prevent both the growth chamber and loadlock being pumped simultaneously. The use of the dry pump minimises contamination of the loadlock and growth chamber by hydrocarbons from pump oil backstreaming. In addition, by using a loadlock chamber, the growth vessel can be maintained at vacuum, circumventing the problem of water vapour contamination associated with venting a chamber to atmosphere.

The system is a single deposition chamber reactor with the capability to grow both doped and undoped silicon, silicon-germanium and silicon-germanium-carbon epitaxial layers. The silicon source gases are silane (100%) and disilane (100%), whilst the germanium and carbon sources are provided by germane (10% in H_2) and methylsilane (100%) respectively. Both n and p-type layers can be grown in the chamber, with phosphine (1000 volumes per million in Ar) and diborane (1000 volumes per million in Ar) providing the n and p-type dopant respectively. In addition to these growth gases, hydrogen and nitrogen are also available on the machine, not only allowing the growth gases in the chamber to be diluted to give closer growth control, but more importantly, in the case of hydrogen, to allow in-situ wafer cleaning. This is an important step to achieve high quality epitaxy and will be discussed in section 3.5.2. All of the gases on the machine are controlled by 100sccm mass flow controllers (MFCs), which feed into a central manifold system so that the growth gases are intermixed before entering the growth vessel. As the layer is deposited, the species within the growth ambient will be depleted, giving potentially non-uniform growth as the gas flows across the wafer. To minimise this effect, the wafer is rotated during the growth cycle to ensure that no part of the wafer is continually subjected to the depleted gas stream.

3.5.2 Wafer preparation

An important step in the growth of high quality epitaxial layers is wafer preparation. A clean surface is required to ensure that the layers are deposited with minimal defects and a high crystalline quality. Any contaminants on the surface will result in stacking faults propagating through the layer, giving a lower quality epitaxial layer that can have deleterious effects on device performance. Since silicon oxidises easily at room temperature, it is necessary to remove this layer before epitaxy can begin, and is generally performed by wet chemical cleaning. Two popular ex-situ cleans are the RCA clean [105] and the HF-last treatment [106]. The former

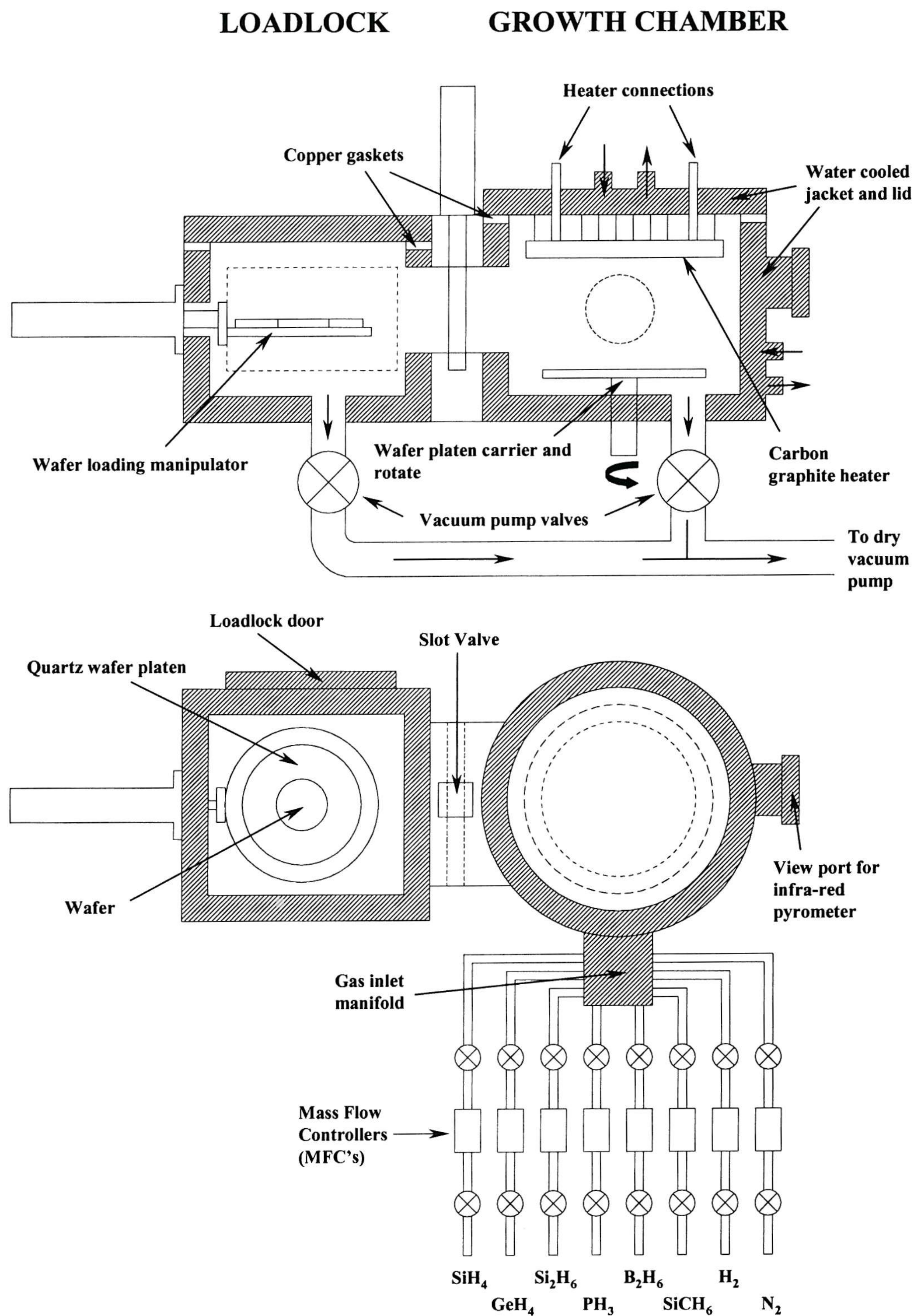
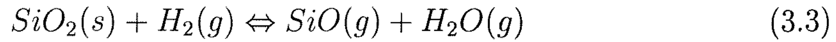
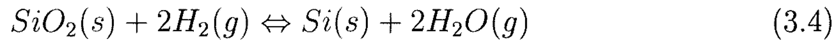


Figure 3.7: Schematic diagram of the LPCVD growth system used in this work.

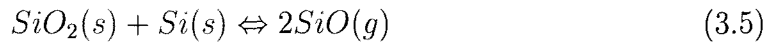
is a two stage process often referred to as RCA-1 and RCA-2. The wafers are first immersed in a solution of $NH_4OH : H_2O_2 : H_2O$, 1:1:5, at 72°C for 10 minutes (RCA1), followed by immersion in a solution of $HCl : H_2O_2 : H_2O$, 1:1:6, for 10 minutes at 72°C (RCA-2). The wafers are then rinsed in de-ionised (DI) water and spun dry in a warm nitrogen ambient. The first stage is used to remove particulate contamination and the native oxide that forms on silicon at room temperature. The second stage is then used to remove metallic contaminants and to grow a very thin chemical oxide approximately 14Å thick [105]. This RCA oxide prevents further particulate contamination of the wafer surface, and can be desorbed in-situ, just prior to epitaxial growth, with a high temperature prebake in hydrogen. The basic chemical reactions for SiO_2 reduction under prebake conditions are [107] :



$$SiO_2(s) + H_2(g) \Leftrightarrow SiO(g) + H_2O(g) \tag{3.3}$$



$$SiO_2(s) + 2H_2(g) \Leftrightarrow Si(s) + 2H_2O(g) \tag{3.4}$$



$$SiO_2(s) + Si(s) \Leftrightarrow 2SiO(g) \tag{3.5}$$

where s and g denote solid and gaseous species respectively. Equations 3.3 and 3.4 are relatively insignificant at lower prebake temperatures, leaving equation 3.5 as the dominant mechanism for the oxide removal.

Goulding [108] has shown that for high temperature hydrogen prebakes, undercutting of oxide windows can occur, causing problems if epitaxy is to be grown on patterned wafers. The undercutting can be reduced by decreasing the bake temperature, and can even be eliminated at a bake temeperature of 850°C. However, this low temperature is ineffective in completely removing the RCA chemical oxide, even if thinning in HF is performed [108]. Therefore in this work, a compromise has been chosen, and consists of thinning the RCA oxide using 100:1 BHF, followed by a hydrogen prebake at 950°C, 1T for 5 minutes.

An alternative to the RCA clean is the HF-last treatment, which uses hydrofluoric acid diluted in purified water. This clean is extremely simple and quick, without the need for complex solutions and heated baths. In addition, since no chemical oxide is grown, the need for a high temperature prebake is eliminated. The silicon atoms at the surface bond with hydrogen atoms, passivating the surface [109] long enough to load into the loadlock. This hydrogen termination is easily desorbed, at approximately 500°C, and is therefore ideal for growths where a high temperature prebake is not appropriate. This was used for the deposition of amorphous Si and SiGe films discussed later in this work. However, HF cleaned wafers can easily collect surface contaminants degrading the quality of subsequent epitaxial growth. When hydrogen passivated (hydrophobic) wafers are inserted into a liquid from air, particles present on the liquid surface will be deposited on the wafer surface, while oxide terminated wafers (hydrophilic) passing through this interface will shed particles [7]. To minimise the surface contamination of the HF cleaned wafers, nitrogen is bubbled through the DI rinse tanks in order to break up any particulate layer on the liquid surface. In addition, the wafer is immediately loaded into the reactor loadloack after cleaning and brought under vacuum to further minimise potential wafer contamination.

3.5.3 Wafer loading and the growth cycle

Once ex-situ wafer cleaning has been performed, a typical growth process is as follows. The wafer is loaded into the loadlock on a quartz platen, and the loadlock pumped down to its base pressure of 1mTorr. Once the pressures in the loadlock and growth chamber are equalised, the slot valve between the two can be opened and the wafer loaded into the chamber. To further minimise possible contamination of the growth chamber, the loadlock pump valve is kept open during loading, thus keeping the pressure differential in favour of the loadlock and preventing contaminants from entering the chamber. After loading is complete, the slot valve is closed and the vacuum pump switched from the loadlock to the growth chamber. Before growth begins, a purge cycle is initiated, which consists of pumping the chamber to 1Torr, with 100sccm of hydrogen flowing for 3 minutes, followed by pumping the chamber to base pressure for a further 3 minutes. This cycle is repeated 3 times to ensure that any contaminants entering the chamber during the loading cycle are minimal.

After the purge is completed, the in-situ clean, if required, is then initiated. After the production of a clean silicon surface, epitaxial growth can begin. The wafer is

heated, or allowed to cool, to the appropriate growth temperature, under a steady flow of hydrogen (100sccm) at a pressure of 1Torr. Once the required setpoint has been achieved, and the temperature allowed to settle, the growth gases are switched in and the growth pressure set on the pressure control valve. During the growth, the temperature, pressure and gas flows are all monitored to ensure no fluctuations occur. In addition, the current and voltage readings are taken for each growth, to allow any changes in the heater characteristics to be easily identified. Finally, after the growth is complete, another hydrogen purge cycle is performed prior to unloading the wafer. This is a safety precaution to remove any unused growth gases before the wafer is unloaded and the loadlock vented to atmosphere.

3.5.4 Quality assessment of deposited layers

An integral part of optimising growth conditions for high quality epitaxial layers is quality assessment. Several tools are used to evaluate the layers' surface morphology, composition and crystallinity, and are primarily chosen for ease of sample preparation and turn around time. The first assessment of the as grown layer is by the human eye, where an appreciation of the layer quality can be gained. Good quality epitaxial layers should have a mirror-like surface, with any cloudyness or fogging indicating degradation in the epitaxy.

After this initial inspection, the surface morphology, a good indicator of crystalline quality, can be assessed using Nomarski contrast optical microscopy and the SEM. The Normaski contrast inspection uses surface interference to highlight imperfections in the epitaxial layer. In addition, this method is very useful when used in conjunction with a defect etch, such as the Sirtl etch [110], allowing defect types to be identified and an assessment of defect density per unit area to be made. The SEM can be used to examine the surface morphology at higher magnifications than the optical microscope, allowing the presence of etch pits and/or degraded epitaxy to be determined.

If the deposition is carried out on a half mask wafer, by cleaving the wafer, the SEM can be used to obtain layer thickness information. The oxide layer will have a different contrast to the silicon areas, and since the bottom of the oxide will be on the same level as the silicon substrate, it can be used as a marker to measure the epitaxial thickness. In addition, the thickness of the polysilicon on top of the oxide can be measured, giving some idea of the incubation time (the time elapsed before Si nucleation on the oxide begins) which is extremely useful for selective growth [7].

For the growth of amorphous and poly-silicon silicon-germanium layers, the crystalline properties were characterised by ultra-violet (u.v.) reflectance measurements. It has been shown [111, 112] that silicon exhibits a strong reflectance peak at a wavelength of 280nm, the height of which can be used to determine whether the layer is crystalline, polycrystalline or even amorphous. The height of the peak is expressed as a percentage of the total reflectance figure, with values of 16-18%, 11-14% and ≈5% denoting crystalline, polycrystalline and amorphous layers respectively. A typical reflectance curve for a polycrystalline layer is shown in figure 3.8. Finally, the material composition is determined by SIMS analysis, which gives information about dopant and matrix element concentration and position, as discussed in section 3.3.

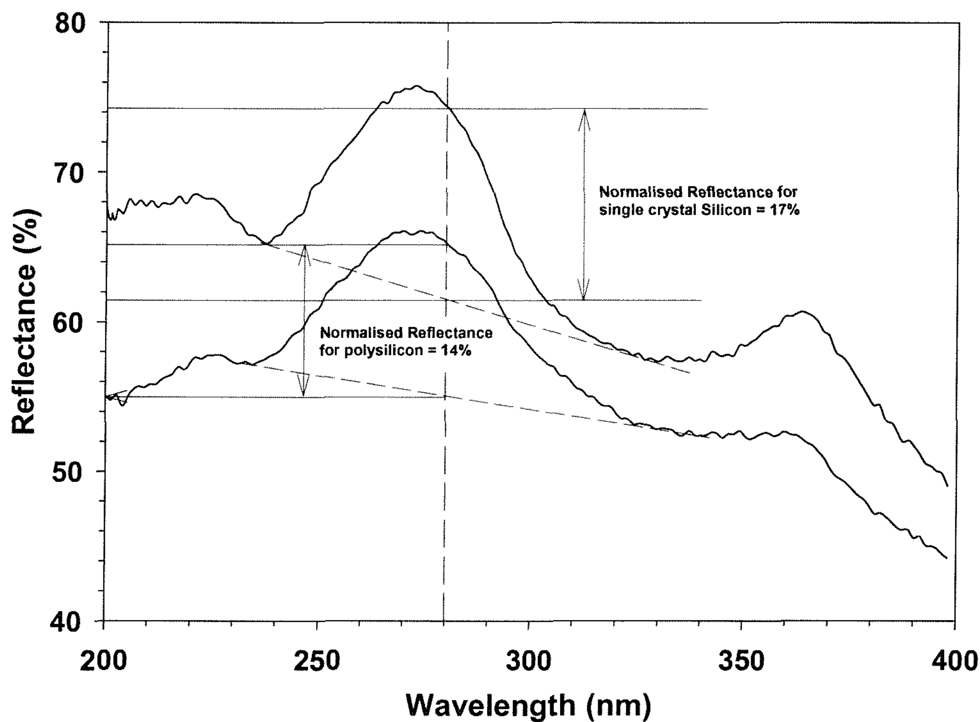


Figure 3.8: Typical u.v. reflectance curve for silicon and polysilicon layers.

3.6 Conclusions

In this chapter, the experimental procedure for the measurement of the temperature dependence of the collector current has been described. Details of sample preparation and temperature calculation have been given, and it has been shown that the most accurate method is from the measured collector current.

Material composition via the use of SIMS analysis has been discussed, showing how the base composition and width can be determined. These profiles in conjunction with the measured base sheet resistance are important to calculate the mean base doping and hence the carrier mobility.

Finally the LPCVD growth system used for the deposition of epitaxial, polycrystalline and amorphous Si, SiGe and SiGe:C layers has also been described. Two contrasting wafer preparation methods have been described, which will allow the growth of high quality layers to be achieved. A brief overview of typical growth cycles and layer assessment techniques has also been given.

Chapter 4

Preliminary investigations into $Si_{1-x-y}Ge_xC_y$ HBTs

4.1 Introduction

In this chapter the results of measurements of the electrical characteristics, as a function of temperature, of SiGe and SiGe:C heterojunction bipolar transistors are presented. The objective of this experiment is to examine whether the incorporation of a background level of carbon ($10^{20}cm^{-3}$) into the SiGe base layer can be effective in suppressing enhanced boron out-diffusion. The presence of parasitic energy barriers, and hence boron out-diffusion from the SiGe base, can be determined by extracting the bandgap narrowing in the base from the temperature dependence of the collector current, as described in 2.8.

Section 4.2 describes the details of the devices used in the experiment. Section 4.3 presents SIMS results and measurements of the collector current, base current and base sheet resistance, measured in the temperature range of 160K to 400K. From these measurements the bandgap narrowing within the base layer can be extracted. Section 4.4 examines the effect of applying an increased reverse bias to the collector-base junction, showing whether parasitic energy barriers are present, and attempts to estimate the dimensions of any barriers present. Finally, in section 4.5, conclusions are drawn from the experimental results.

The mean base doping concentrations within the device, shown in table 4.1, were determined by applying the iterative method, described in section 3.4, to the measured room temperature base sheet resistance. The neutral basewidth, W_B, was calculated from SIMS profiles, discussed in section 4.3.1, by measuring the metallurgical basewidth and then applying a correction for the penetration of the space charge layers at the emitter/base and collector/base junctions. From table 4.1 it can be seen that the neutral basewidths of the two devices are significantly different, the SiGe device being 20nm wider, possibly indicating differences in diffusion behaviour, since both devices were subjected to the same processing. The wafer to wafer repeatability of the MBE system should ensure the as grown base profiles are similar, so this is unlikely to be the cause for the differences in basewidth.

Table 4.1: Experimental details of the devices studied in the low temperature analysis.

Wafer Type	Ge (%)	Mean Doping Concentration (cm^{-3})	Basewidth W_B (nm)	Sheet Resistance (300K) R_B(kΩ/sq)
SiGe	18	1.62×10^{18}	49	6.65 ± 0.1
SiGe:C	18	4.67×10^{18}	29	4.15 ± 0.1

4.3 Experimental Results and Discussion

4.3.1 SIMS Analysis

Figure 4.2 shows the SIMS profiles for the SiGe HBT. From figure 4.2 it can be seen that the boron doping level in the base layer peaks at a value of $7 \times 10^{18}cm^{-3}$, and has a fairly broad profile. The full half width maximum (FHWM) value is approximately 20nm. In addition, it can be seen that the C level in the device drops dramatically from a value of 1.5×10^{20} at the polysilicon/silicon interface to a level of $2 \times 10^{18}cm^{-3}$ in the SiGe base layer. Several authors have shown that a C level around $10^{18}cm^{-3}$ is insufficient to suppress TED [39, 47, 113]. Therefore it is expected that these devices will remain unaffected by this background C contamination level. Finally the Ge concentration in the base peaks at a value of 18%.

Figure 4.3 shows the SIMS profiles for the SiGe:C HBT. In contrast to the SiGe device, the boron profile in the SiGe:C HBT is much narrower, the FHWM value

has decreased to 12nm, with a much higher peak value of $1.9 \times 10^{19}\text{cm}^{-3}$. The C profile in the base is $2 \times 10^{20}\text{cm}^{-3}$, very close to the desired value of 10^{20}cm^{-3}. As before, the Ge content in the base layer peaks at 18% indicating that the Ge incorporation is unaffected by the addition of carbon.

The mean base doping levels, obtained from integrating the boron SIMS profile, of $1.73 \times 10^{18}\text{cm}^{-3}$ and $5.5 \times 10^{18}\text{cm}^{-3}$, for the SiGe and SiGe:C devices respectively, are slightly higher than the values shown in table 4.1. This can probably be attributed to the fact that SIMS analysis measures the total dopant concentration in the layer, both electrically active and inactive. In contrast, the iterative method, using the measured base sheet resistance, only gives the mean base doping level due to electrically active dopants.

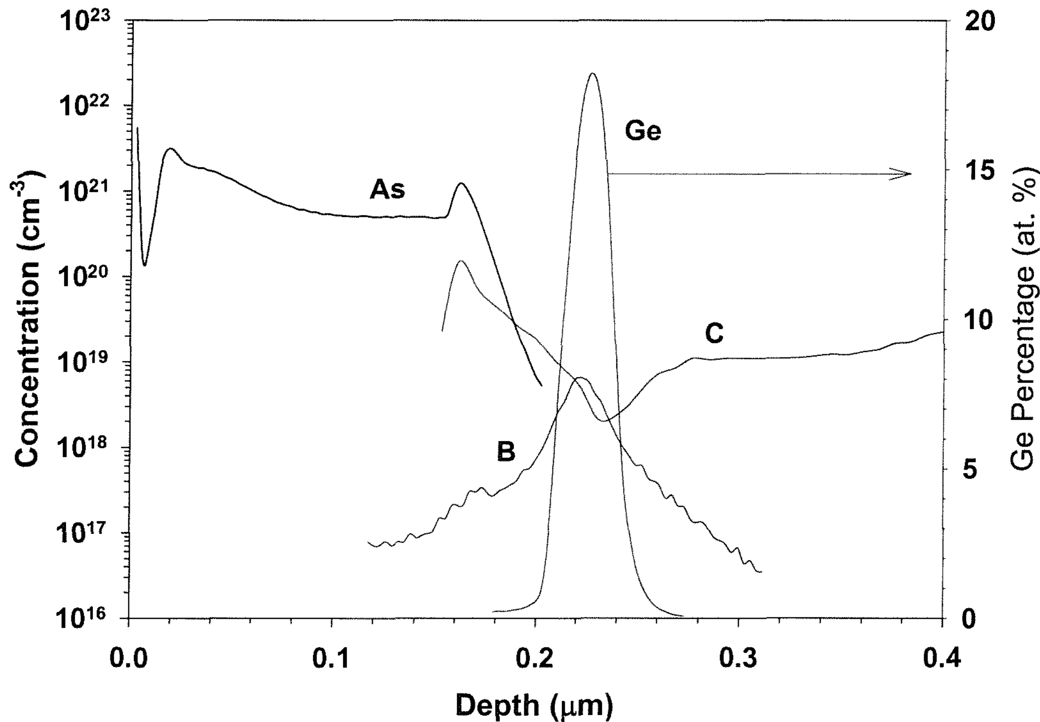


Figure 4.2: SIMS profiles for the $Si_{0.82}Ge_{0.18}$ HBT with a mean base doping level of $1.62 \times 10^{18}\text{cm}^{-3}$.

4.3.2 Base Sheet Resistance

Figure 4.4 shows how the intrinsic base sheet resistance varies with temperature for the two devices in this study. From figure 4.4 it can be seen that the base sheet resistance of the SiGe device is larger than its carbon-containing counterpart. In addition the resistance increases slightly with decreasing temperature, rising from

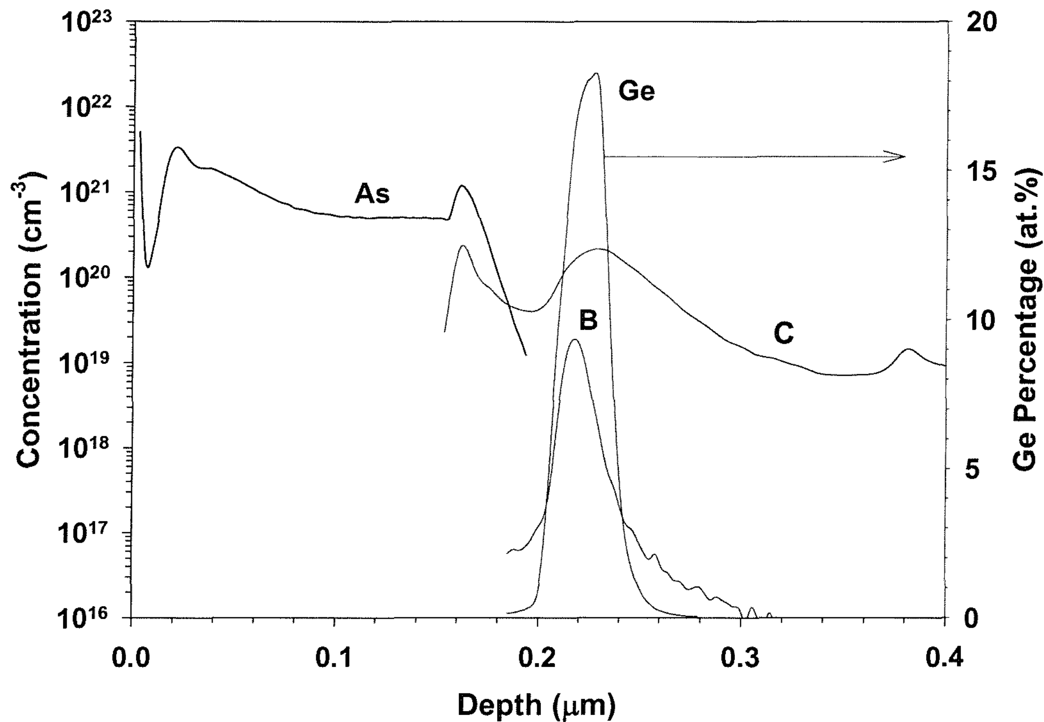


Figure 4.3: SIMS profiles for the $Si_{0.818}Ge_{0.18}C_{0.002}$ HBT with a mean base doping level of $4.67 \times 10^{18}cm^{-3}$.

a value of 6.6kΩ/sq. at room temperature to a value of 7.1kΩ/sq. at a temperature of 200K, suggesting that freeze-out of dopant may be occurring. This behaviour can be explained from the boron doping profile of the SiGe HBT, shown in figure 4.2 which exhibits long doping tails, with the majority of the profile below the Mott transition level of $1.68 \times 10^{18}cm^{-3}$ [114]. It has been shown that for doping levels below this value, dopant becomes electrically inactive as the temperature is reduced, giving a corresponding rise in the sheet resistance

In contrast the sheet resistance of the devices containing carbon decreases from 4.15kΩ/sq. to 3.82kΩ/sq. as the temperature is reduced from 300K to 200K. This relative temperature invariance implies that freeze-out of dopant atoms is not occurring to any significant extent, and that the base layer is highly doped with abrupt doping profiles. This is clearly evident from figure 4.3, where it can be seen that the boron profile is narrower, with much less of the profile being below the Mott transition level.

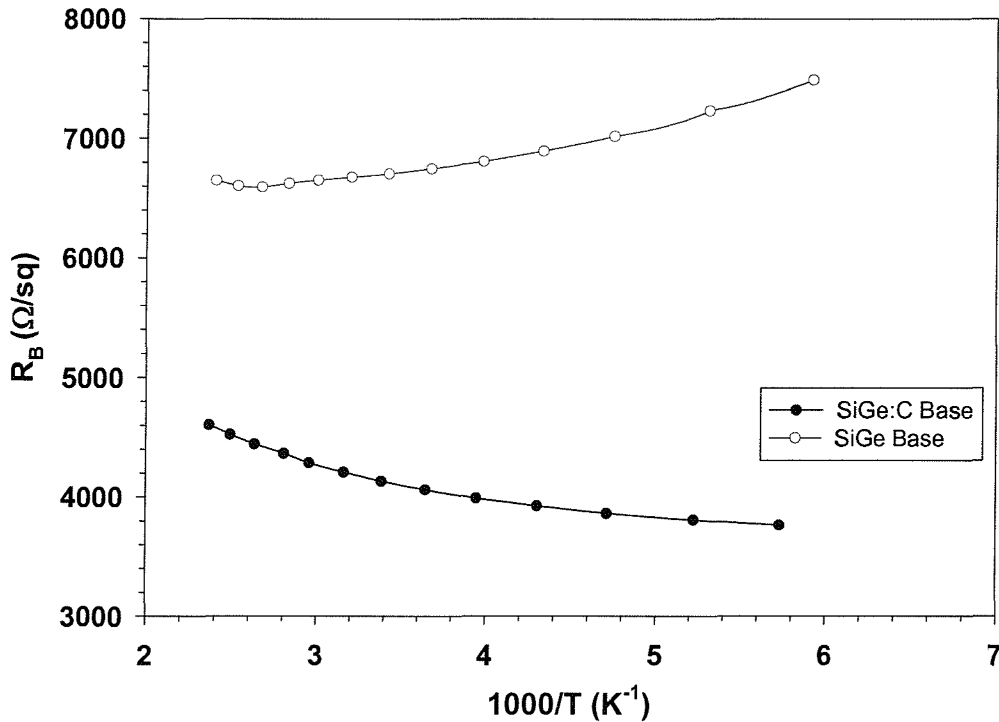


Figure 4.4: Intrinsic base sheet resistances as a function of reciprocal temperature for the SiGe and SiGe:C devices.

4.3.3 The temperature dependence of the collector and base currents

Figure 4.5 shows Gummel plots for the $Si_{0.82}Ge_{0.18}$ device, measured at 209K and 292K. Two points are readily observable. Firstly the collector current at both temperatures is near-ideal over several orders of magnitude, with an ideality factor of 1.02, and can therefore be reliably used to extract the bandgap narrowing in the base. Secondly the base current is non-ideal (1.37), especially at low V_{BE}. This non-ideality could be due to the base layer partially relaxing due to the high germanium content. The critical thickness for 18% germanium is approximately 21nm, which means that the 30nm base layer is metastable and is therefore prone to relaxation. If the thermal budget of subsequent processing is to high, the strain in the SiGe layer is relieved by plastic flow, thus causing the generation of misfit dislocations which are efficient trapping centres. Any dislocations in the E/B depletion region will increase the contribution of depletion region recombination (I_{rg}) to the base current, becoming the dominant factor at low V_{BE}. In addition from figure 4.5, it can be seen that, as the temperature is reduced, the base current ideality deteriorates, changing from 1.37 to 1.51 at low V_{BE}. A possible cause of this behaviour has been explained by Gonzalez-Bris *et al* [115], whose research has shown that the

temperature dependence of the non-ideal part of the base current can be attributed to metallic microprecipitates at the junction assisting the recombination process as the temperature is reduced. The maximum forward current gain (β_{MAX}) of 16 at 292K, dropping to 10 at 209K, is extremely low considering the expected heterojunction effect associated with the incorporation of 18% germanium, and can probably be attributed to the excessive base current caused by depletion region recombination.

Figure 4.6 shows 208K and 292K gummel plots for the $Si_{0.818}Ge_{0.18}C_{0.002}$ device, measured at a collector-base reverse bias of 0V. The plots show an ideal collector current ($n_c = 1.01$), over 6 orders of magnitude. The collector current of the SiGe:C device is a factor of 6 higher than that of the SiGe HBT at 292K, dropping to a factor of 3 at 208K. Using the data from table 4.1, the room temperature base gummel numbers (G_B) of the SiGe and SiGe:C devices can be calculated, giving values of 1.01×10^{12} and 2.16×10^{12}s/cm^4 respectively, assuming a uniform doping profile. Since I_C is inversely proportional to G_B, it would be expected that the SiGe device would have a higher collector current than the SiGe:C device, assuming both devices have equivalent Ge concentrations and that the small amount of carbon has little effect of the bandgap narrowing of the base. This shows that the improvement in the collector current in the SiGe:C device cannot be attributed to base gummel characteristics, and that some other mechanism, such as parasitic energy barrier formation, is responsible. The higher collector current in the SiGe:C devices is reflected in the values of β_{MAX}, which are 66 at 292K, rising to 140 at 208K. The rise in forward current gain with reducing temperature follows the expected trend, unlike the SiGe device, due to the thermally activated bandgap narrowing of germanium in silicon.

In addition from figure 4.6, it can be seen that the base current ideality (1.31), extracted at 292K, for the SiGe:C device is comparable to the value of 1.37 obtained for the SiGe device. As the temperature is reduced to 208K, the base current ideality deteriorates to a value of 1.47, again similar to the value obtained for the SiGe device, showing that the addition of a low level of carbon is not affecting the base current. The similar base current idealities can be explained since the carbon content is only 0.2% and hence the base layers are still metastable and prone to relaxation. This is because a much higher Ge:C ratio ($\approx 9:1$) is required to achieve complete strain compensation within the SiGe layer [27], indicating that the strain compensation achieved with the introduction of only 0.2% carbon, which equates

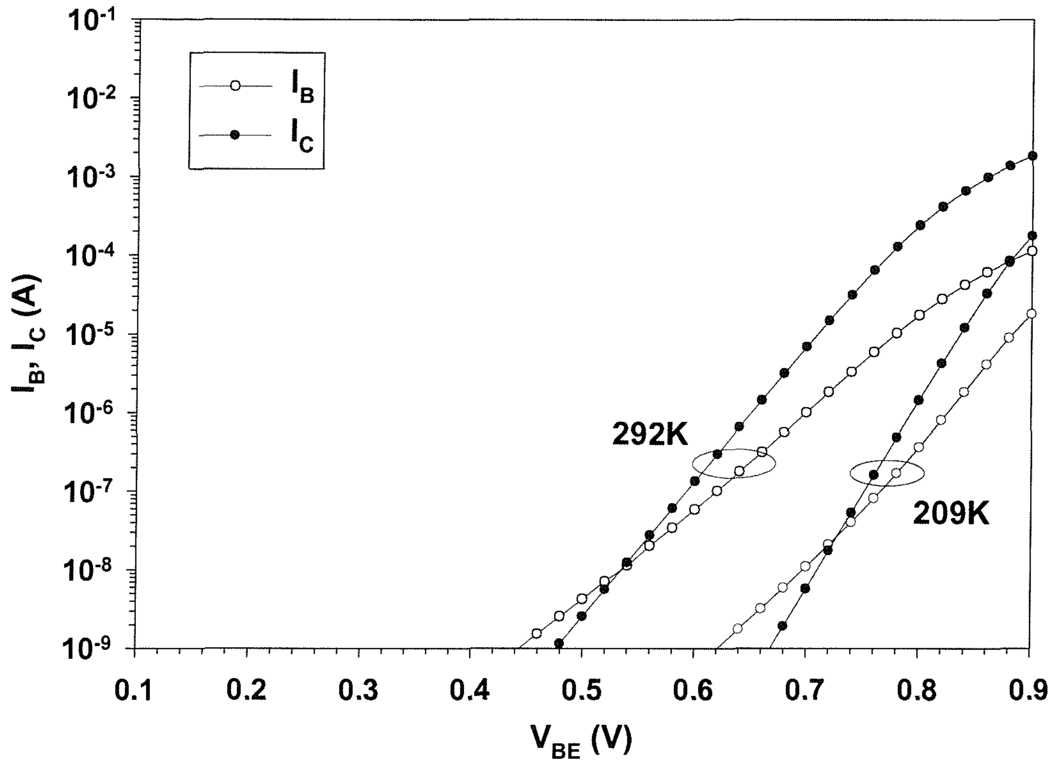


Figure 4.5: Gummel Plot for the $Si_{0.82}Ge_{0.18}$ HBT with a mean base doping level of $1.62 \times 10^{18}cm^{-3}$. Measured at 209K and 292K with $V_{CB} = 0V$.

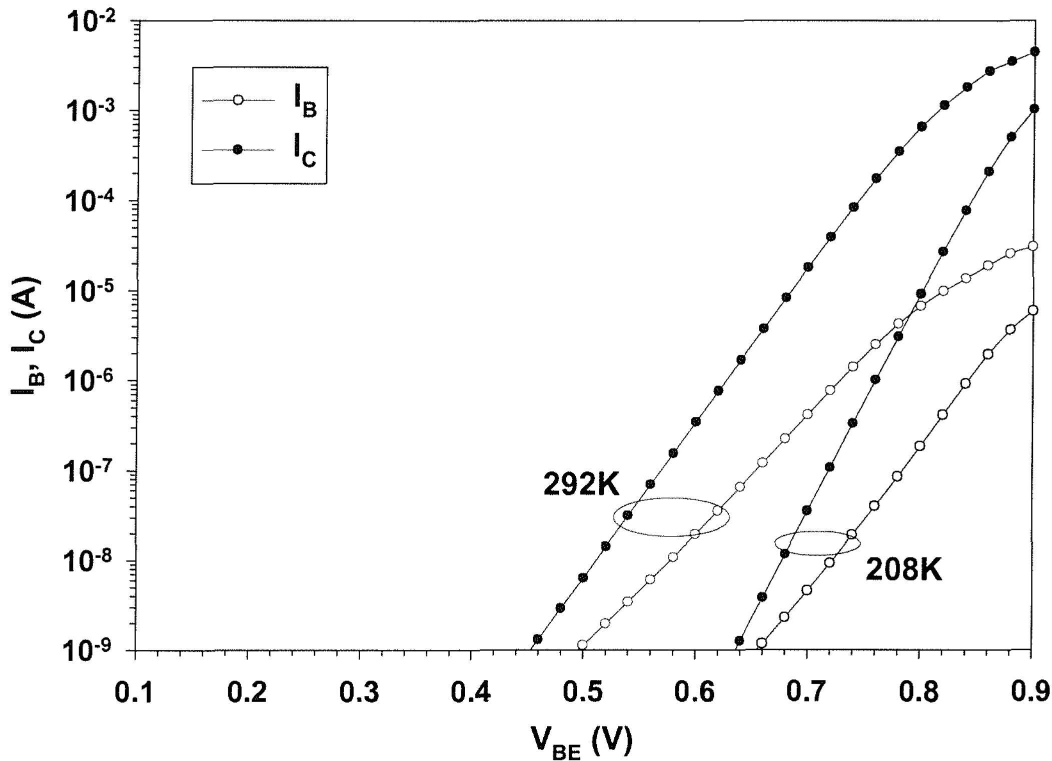


Figure 4.6: Gummel Plot for the $Si_{0.818}Ge_{0.18}C_{0.002}$ HBT with a mean base doping level of $4.67 \times 10^{18}cm^{-3}$. Measured at 208K and 292K with $V_{CB} = 0V$.

to a Ge:C ratio of 90:1, is minimal. Therefore the recombination current mechanisms due to the generation of misfit dislocations generated by strain relaxation, as discussed for the SiGe device, still apply.

4.3.4 Extraction of the bandgap narrowing in the base

Figure 4.7 shows the calculated bandgap narrowing plots for the SiGe and SiGe:C devices respectively, obtained by applying the electrical analysis, described in section 2.8, to the measured collector currents at each measurement temperature. Several points are readily apparent. Firstly the values of $J_C(T)/J_O(T)$ form a reasonably straight line, even at low temperatures, with a closer fit being observed for the SiGe:C device. The slopes were obtained from a least squares fit, using all of the measured data points, and represent the bandgap narrowing (BGN) in the base of the transistors due to germanium and heavy doping effects. Secondly, the extracted BGN values of 101meV and 155meV, for the SiGe and SiGe:C devices respectively, are significantly different. The BGN extraction for SiGe HBTs is not straightforward due to the possible presence of parasitic energy barriers, caused by boron out-diffusion [14]. As discussed in section 2.7, these barriers reduce the collector current for a given bias, thus reducing the slope of the BGN plot. Therefore the 54meV discrepancy between the identically processed devices, apart from the presence of carbon, could be due to the electrical characteristics of the SiGe device being strongly influenced by energy barrier formation. However, from these preliminary measurements it is impossible to tell whether energy barrier formation has still occurred in the SiGe:C device, but to a lesser extent. Finally the intercepts of the two plots with the vertical axis are also significantly different, with values of 9.8 and 3.1 for the SiGe and SiGe:C devices respectively. As discussed in section 2.8 the intercept should equal unity. Any deviation from unity is either due to problems with the temperature dependences in the models or to the presence of parasitic energy barriers.

Le Tron *et al* [48] have shown that the presence of a parasitic energy barrier at the collector-base junction can be determined by operating the devices with increased C/B reverse bias. The reverse bias widens the C/B depletion layer, thus suppressing any barrier present. This will give a corresponding rise in the measured collector current that will be reflected in a change of slope of the BGN plot. Therefore by comparing the slopes of the BGN plots measured at zero and non-zero C/B reverse bias, the presence of a barrier at the C/B junction can be determined since

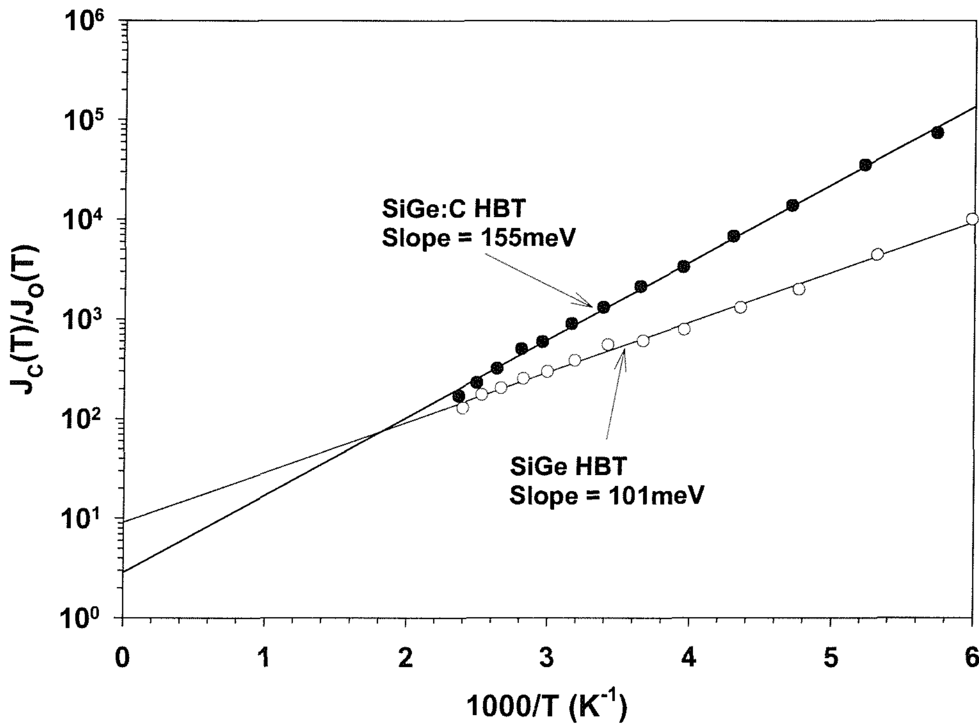


Figure 4.7: Bandgap narrowing plots for the $Si_{0.82}Ge_{0.18}$ and $Si_{0.818}Ge_{0.18}C_{0.002}$ HBTs, measured with a collector/base reverse bias of zero volts. The slope of the graph denotes the total bandgap narrowing in the base, due to the presence of germanium and heavy doping effects.

a change in slope would indicate that the barrier has been suppressed. In addition the change in slope with reverse bias will also alter the intercept with the vertical axis. This will show whether the temperature dependence models used are valid and that the intercept deviation from unity is due to parasitic energy barrier formation. Therefore in order to determine whether the carbon has fully suppressed TED, the devices were operated at increased collector-base reverse bias and the analysis re-applied. This is discussed in section 4.4.

Another possible cause for a reduction in the slope of the BGN plot is the effect of doping tails within the base. Chantre and Nouailhat [116] have shown that doping tails within the base profile increasingly dominate the base gummel number as the temperature is reduced. This causes a non-linear behaviour in the bandgap narrowing plot that results in the slope of the graph being larger at higher temperatures. Ashburn *et al* [73] have shown that the high temperature ($1000/T < 3.5K^{-1}$) slope of the bandgap narrowing plots gives reasonable bandgap narrowing values, even for extreme doping tails. In order to determine whether such non-linear behaviour was present in the devices studied in this work, the affect of splitting the data at

1000/T = $3.5K^{-1}$ on the slope of the graph was investigated. This is shown in figure 4.8.

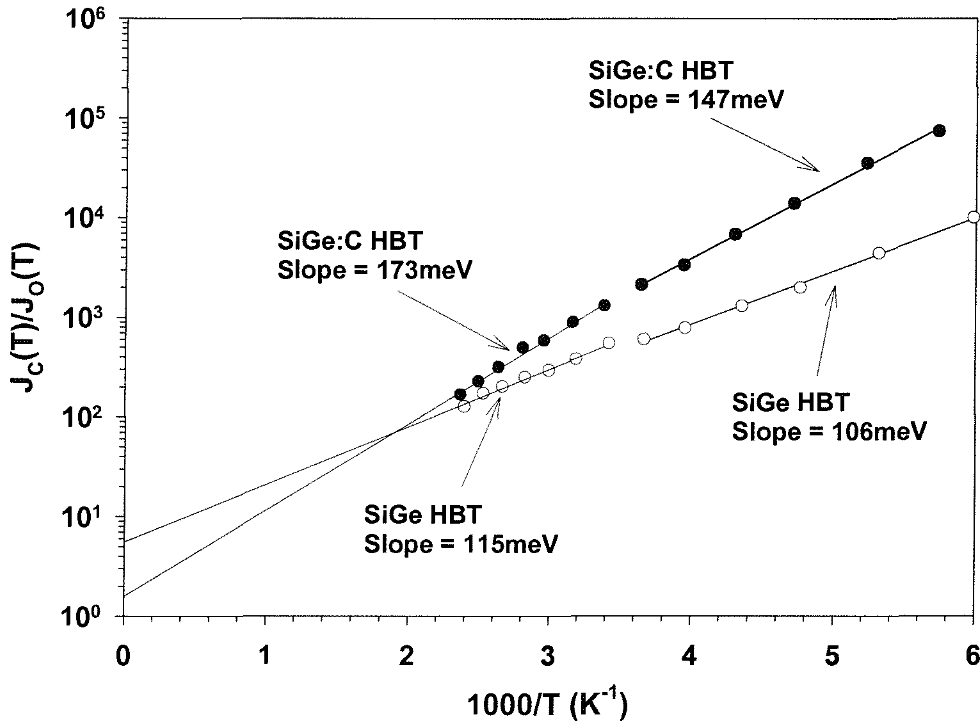


Figure 4.8: Bandgap narrowing plots for the $Si_{0.82}Ge_{0.18}$ and $Si_{0.818}Ge_{0.18}C_{0.002}$ HBTs, measured with a collector/base reverse bias of zero volts. The data is split at 1000/T = $3.5K^{-1}$ to examine the non-linear behaviour of the Gummel plot .

It can be seen from figure 4.8, that when the high temperature data (1000/T < $3.5K^{-1}$) for the SiGe:C device is taken separately, the extracted bandgap narrowing within the base increases by 18meV to a value of 173meV and the intercept reduces to 1.5, very close to the desired value of unity. In contrast, the slope for the low temperature data (1000/T > $3.5K^{-1}$) is only 8meV below the value obtained when all of the data is considered. This result shows that the low temperature effects on the base gummel number can have a significant effect on the extracted bandgap narrowing, and therefore for accurate bandgap narrowing extraction only the high temperature values should be considered.

However, from figure 4.8, for the SiGe device, splitting the data into high and low temperature components has actually caused both slopes to increase from the value of 101meV, when all of the data is considered, to values of 115meV and 106meV for the high and low temperature data respectively. The increase in slope for the low temperature data is an unexpected result and is most likely attributed to errors in the measurement of the collector current and temperature. The apparent

discontinuity in the BGN plots at the break point ($1000/T = 3.5K^{-1}$) is coincidental since all temperature measurements were taken identically, and in one sweep over the temperature range, to minimize measurement inaccuracies from thermal fluctuations.

4.4 Effects of increased Collector/Base reverse bias

4.4.1 Effect of C/B reverse bias on collector and base currents

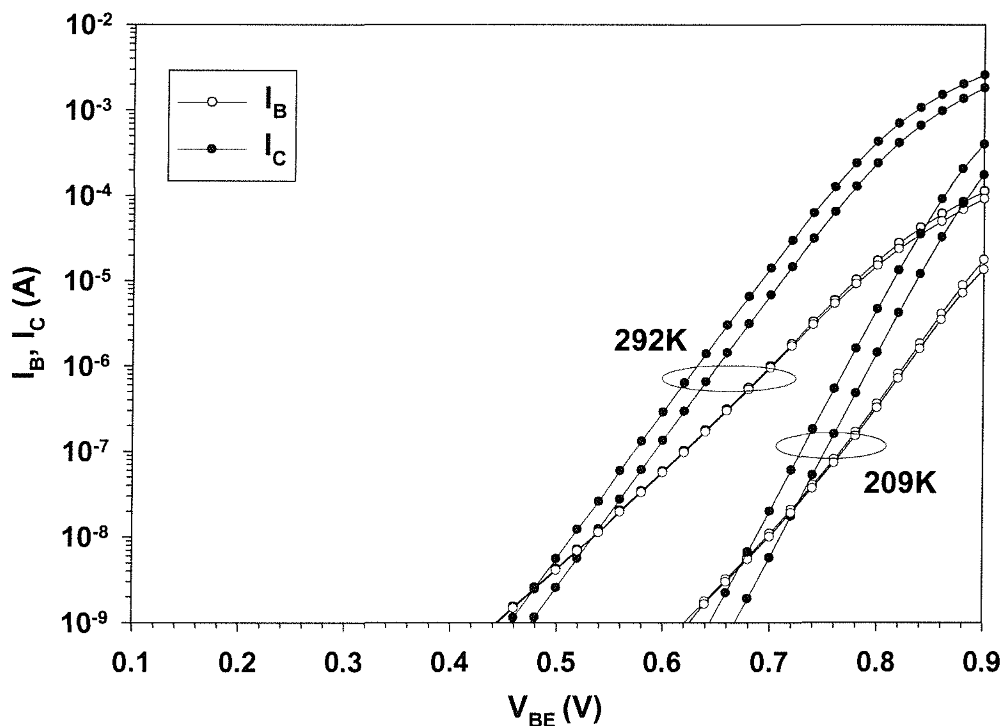


Figure 4.9: Gummel plots for the $Si_{0.82}Ge_{0.18}$ HBT measured at 209K and 292K with collector-base reverse biases of 0 and 1V. Applying the reverse bias gives a significant increase in collector current at both temperatures.

In this section the effect of increased collector-base reverse bias on the electrical characteristics of the SiGe and SiGe:C HBTs is discussed. A C/B reverse bias of 1V is applied to the devices, and the collector and base currents measured in the temperature range of 200K to 400K. Figure 4.9 shows the effects of applying the collector-base reverse bias on the electrical characteristics of the SiGe device, for the

measurement temperatures of 209K and 292K. It is readily apparent that there is a significant increase in collector current over the zero bias characteristic, confirming that a parasitic energy barrier at the collector-base junction is present. The increase in collector current is a factor of 2 higher at 292K, rising to a factor of 4 higher at 209K. Also from figure 4.9, it can be seen that applying the collector-base reverse bias has no significant effect on the base current.

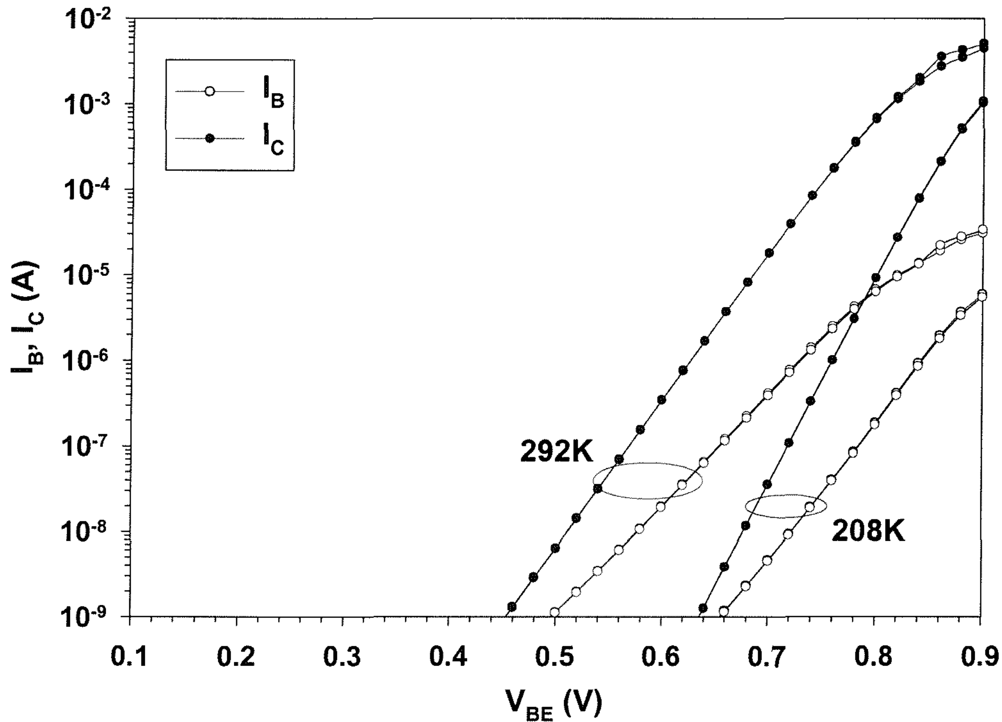


Figure 4.10: Gummel plots for the $Si_{0.818}Ge_{0.18}C_{0.002}$ HBT measured at 208K and 292K with collector-base reverse biases of 0 and 1V. Applying the reverse bias has no effect on the collector current at either measurement temperature.

In contrast figure 4.10 shows that applying a 1V collector-base reverse bias to the SiGe:C device has no effect on the collector current, the two sets of characteristics being so close as to be indistinguishable from each other, at both 208K and 292K. This shows that no parasitic energy barrier is present at the C/B junction since there is no obvious collector current dependence on C/B bias. Once again, the base current also does not show any C/B bias dependence.

4.4.2 Effect of C/B reverse bias on bandgap narrowing extraction

Figures 4.11 to 4.14 show the results of applying the electrical analysis to devices operating at a C/B reverse bias of 1V. It can be seen from figure 4.11 that applying the reverse bias to the SiGe HBT causes the slope of the graph to increase from 101meV, for a collector-base bias of 0V, to 137meV. In addition the intercept with the vertical axis has been reduced from a value of 9.8 at zero C/B bias, to a value of 4.2 with applied bias. The increase in slope, by 36meV, and the reduction in vertical intercept both confirm that a parasitic energy barrier at the collector-base junction exists, since the collector current is strongly dependent on C/B reverse bias. Figure 4.12 shows the effect of considering the high and low temperature data separately on the BGN extraction for the SiGe device. It can be seen that the slopes of both the high and low temperature plots increase to a value of 145meV. The increase in the high temperature plot by 8meV demonstrates again the effect of doping tails on the extracted bandgap narrowing value, as discussed in the previous section.

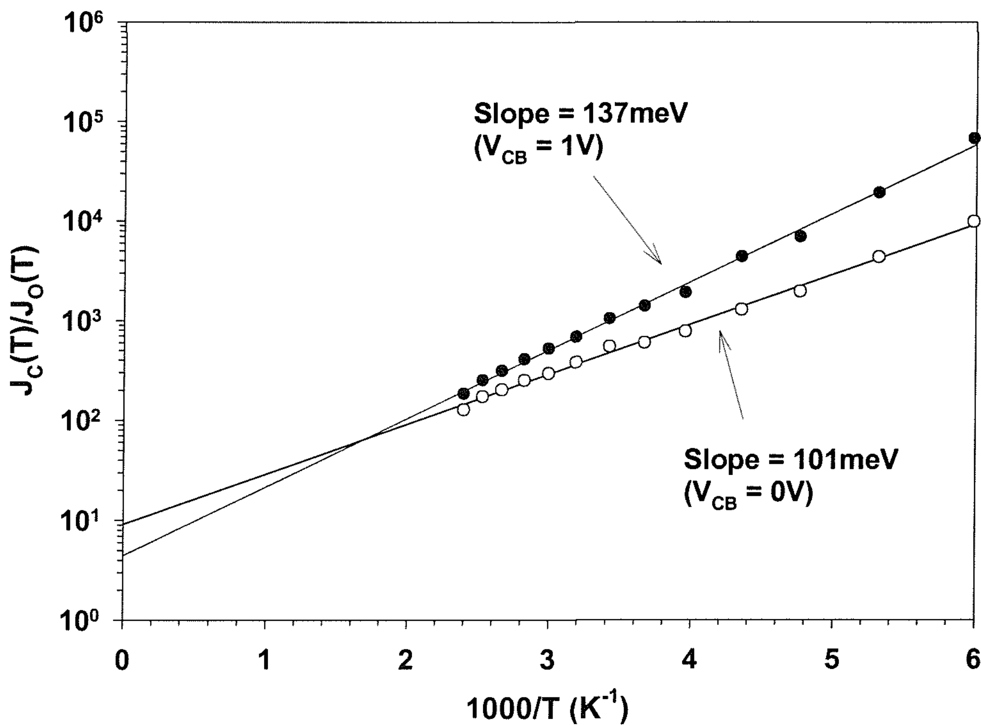


Figure 4.11: Bandgap narrowing plot for the $Si_{0.82}Ge_{0.18}$ HBT, showing the effect of applying a 1V C/B reverse bias. The change in slope with applied bias confirms the presence of a parasitic energy barrier at the C/B junction.

In contrast, figure 4.13 shows that applying the C/B reverse bias to the SiGe:C device has no observable affect on the bandgap narrowing plot, with both curves being

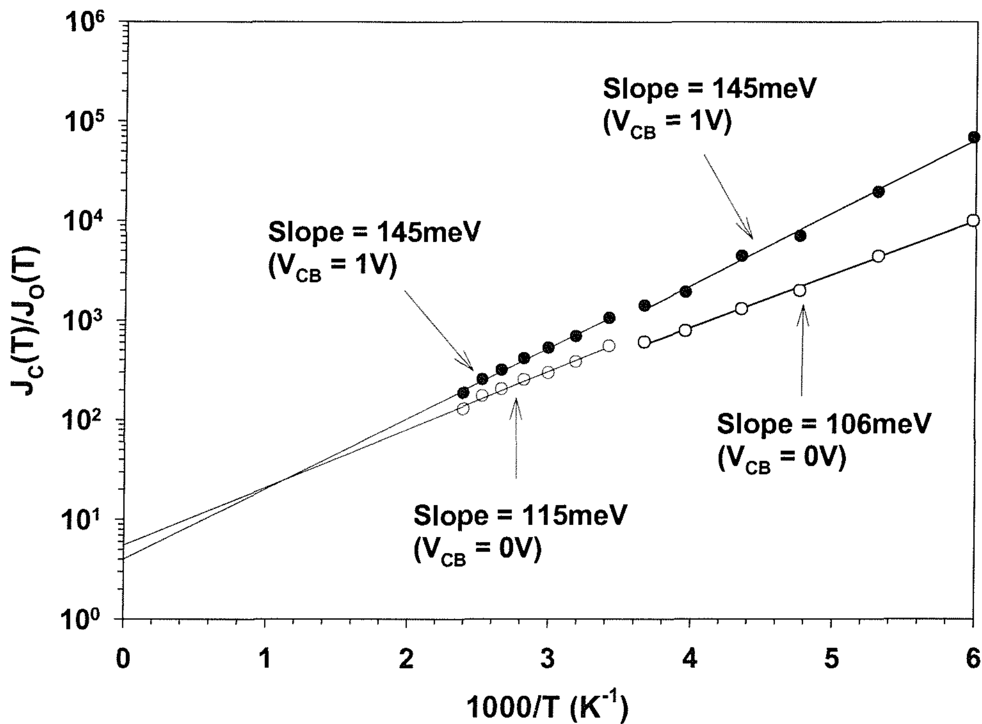


Figure 4.12: Bandgap narrowing plots for the $Si_{0.82}Ge_{0.18}$ HBT, showing the effect of taking the high temperature data separately.

virtually indistinguishable from one another, having an identical slope of 155meV. The vertical intercepts remain the same with a value of 3.1. Figure 4.12 shows the corresponding BGN plot considering the high and low temperature data separately. Once again, as was seen in figure 4.8, the slope of the high temperature data increases from 155meV to 173meV in both cases. Figures 4.13 and 4.14 both indicate that no parasitic energy barrier exists at the collector-base junction, implying boron out-diffusion has not occurred. Since both devices were identically processed, apart from the incorporation of carbon into the SiGe base layer, this suggests that carbon can be effectively used to eliminate anomalous boron diffusion due to implantation damage.

In addition the intercept value of 1.5 in figure 4.14 suggests that there are only minor discrepancies in the temperature dependences of the models used in the electrical analysis. Furthermore the results of figure 4.14 suggest that the properties of the SiGe layer are not significantly affected by the presence of such a small amount of carbon (0.2%) since both the SiGe and SiGe:C devices were treated identically in the analysis, and any affects of carbon on the density of states product, or carrier mobility were ignored.

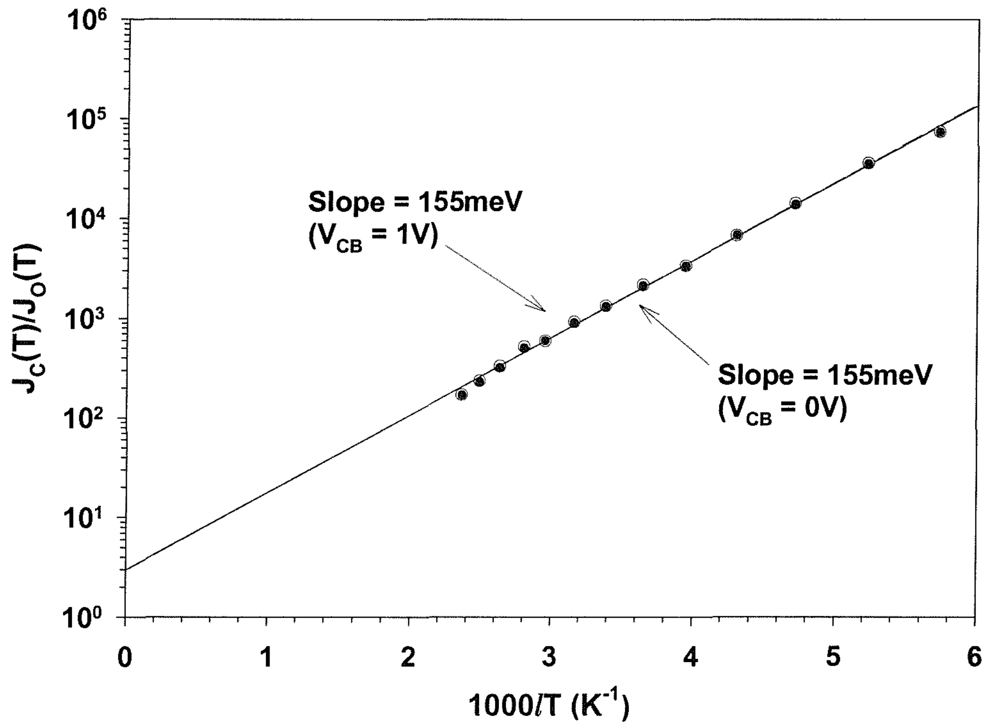


Figure 4.13: Bandgap narrowing plot for the $Si_{0.818}Ge_{0.18}C_{0.002}$ HBT, showing the effect of applying a 1V C/B reverse bias. The slopes of the graph remain unchanged, at a value of 155meV, with applied bias confirming that no parasitic energy barrier exists at the C/B junction.

Figure 4.15 shows theoretical plots of predicted total bandgap narrowing versus Ge content, for a mean base doping level of $4.6 \times 10^{18}cm^{-3}$, using two different methods. The first method assumes that heavy doping bandgap narrowing in SiGe is identical to that found in silicon, and therefore allows the empirical model of Klaassen *et al* [85] to be used to calculate the bandgap narrowing due to heavy doping effects. This gives a value of 70meV for a doping level of $4.67 \times 10^{18}cm^{-3}$. The bandgap narrowing due to Ge incorporation is calculated separately using the empirical model of Iyer *et al* [117]. The two values are then added to give the total bandgap narrowing in the layer, resulting in the top curve of figure 4.15. An alternative approach, as described by Jain *et al* [4], assumes that heavy doping effects are not identical in SiGe and Si, and therefore takes into account the effect of Ge on heavy doping bandgap narrowing. The total bandgap narrowing is calculated directly and results in the lower curve of figure 4.15.

For comparison, the experimental BGN value obtained for the SiGe:C HBT is also plotted in figure 4.15. The measured value of total bandgap narrowing value of 173meV is closer to the theoretical line of Jain *et al* [4], than that of Iyer *et al* [117] and Slotboom *et al* [118]. For the model of Jain *et al* the discrepancy with the

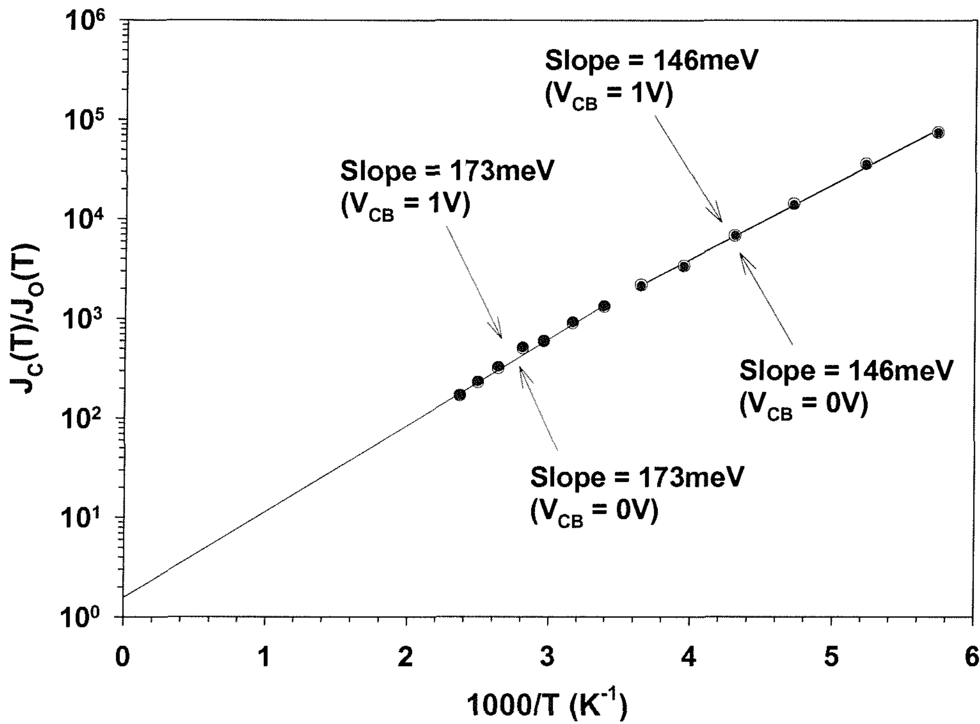


Figure 4.14: Bandgap narrowing plots for the $Si_{0.818}Ge_{0.18}C_{0.002}$ HBT, showing the effect of taking the high temperature data separately.

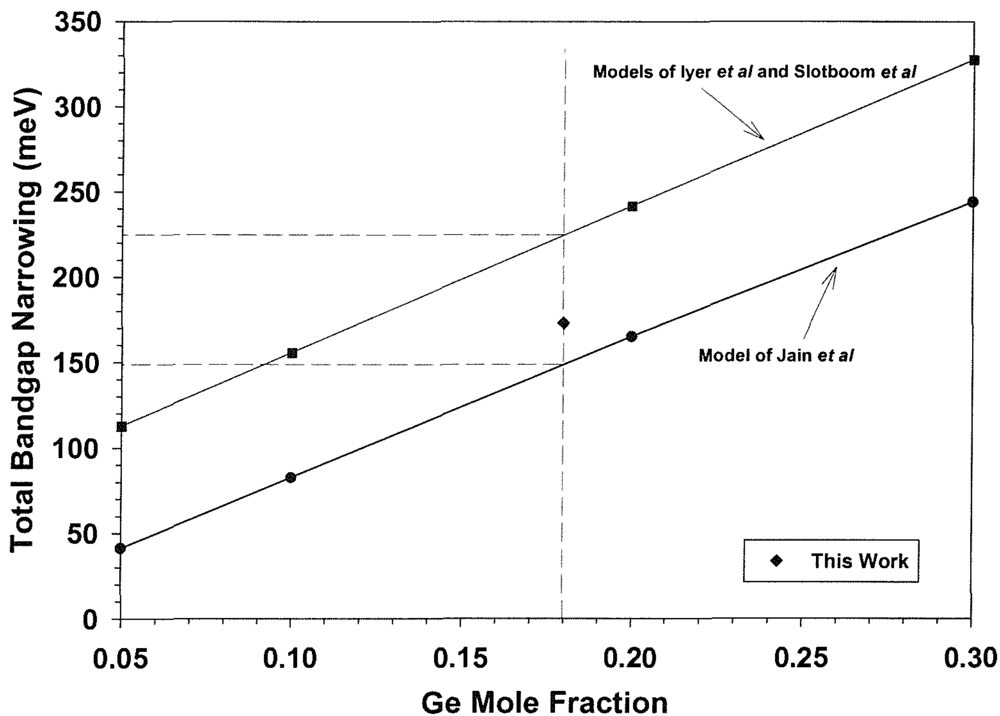


Figure 4.15: Comparison of predicted total bandgap narrowing, due to heavy doping and Ge incorporation, given by the models of Slotboom *et al* [118] and Iyer *et al* [117], and the model of Jain *et al* [4].

measured value is 23meV. This is in reasonable agreement considering the uncertainties involved in extracting the Ge concentration from SIMS data. For example an increase in the Ge content from 18% to 20%, which would correspond to an extraction error from the SIMS data of approximately 10%, would result in an increase in the value predicted by the Jain model to 168meV, only 5meV less than the measured value. It should also be noted that the BGN values predicted by the model of Jain *et al*, shown in figure 4.15, were calculated at a mean base doping level of $7 \times 10^{18}\text{cm}^{-3}$, somewhat higher than the value of $4.67 \times 10^{18}\text{cm}^{-3}$, used to extract the BGN for the SiGe:C HBT. However, it has been shown [4] that for doping concentrations below $7 \times 10^{18}\text{cm}^{-3}$, the bandgap narrowing within the layer is not significantly affected by doping level, becoming almost indistinguishable from the curve shown in figure 4.15. In addition the small amount of carbon in the base of the SiGe:C HBT (0.2% or 10^{20}cm^{-3}) is unlikely to significantly alter the bandgap narrowing from that expected for SiGe [31]. Therefore these results suggest that the experimentally extracted value of 173meV is in reasonable agreement with the model of Jain *et al* [4], considering all of the uncertainties in the measured and modeled data.

It should be noted that a possible contribution to the differences in the collector currents of the SiGe and SiGe:C transistors could be due to strain compensation associated with the incorporation of carbon. However, the good agreement of the extracted BGN in the base of the SiGe:C HBT with the model of Jain *et al* suggests that any strain relaxation is not significant. Since the expected strain compensation due to the incorporation of 0.2% carbon is minimal, it can be expected that the SiGe layer also remains strained and therefore differences in the BGN values obtained from the temperature dependence of the collector current can be attributed to parasitic energy barrier formation. In the next chapter, devices are fabricated with much lower Ge concentrations so that the base layers are fully stable, thereby removing any possible ambiguity related to strain relaxation.

4.4.3 Estimation of the energy barrier dimensions

The Slotboom parasitic energy barrier model [14] can be adapted to obtain an expression for the collector current density as a function of the barrier dimensions [48]. For a barrier width ΔW and height ΔE^*, the exponential term $\exp(qV_{BE}/kT)$ is replaced by :

$$\frac{exp[\frac{qV_{BE}}{kT}]}{1+\frac{\Delta W}{W_B}[exp\frac{\Delta E*}{kT}-1]} \tag{4.1}$$

For a large energy barrier ($\Delta E^* \gg kT$) equation 4.1 simplifies to :

$$\frac{W_B}{\Delta W}exp[\frac{qV_{BE}-\Delta E^*}{kT}] \tag{4.2}$$

If the analysis is re-applied using equation 4.2, the normalized collector current density, $J_C(T)/J_O(T)$, can be approximated by :

$$\frac{J_C(T)}{J_O(T)} \approx \frac{W_B}{\Delta W}exp[\frac{\Delta E_G+\Delta E_{GB}^{app}-\Delta E^*}{kT}] \tag{4.3}$$

In this case the slope of the graph of $\ln(J_C(T)/J_O(T))$ versus reciprocal temperature gives the value of $\Delta E_G + \Delta E_{GB}^{app} - \Delta E^*$, and the intercept gives $W_B/\Delta W$. Therefore an estimation of the barrier height in the SiGe device can be obtained using the extracted data from the SiGe:C device to give a value for $\Delta E_G + \Delta E_{GB}^{app}$. Similarly the barrier width can be estimated from the vertical intercept and the neutral basewidth for the SiGe:C device, given in table 4.1. It should be noted that this method is only valid for zero collector/base reverse bias because the simplified model of the Slotboom parasitic energy barrier model, equation 4.2, does not take into account the effects of reverse bias on the parasitic energy barrier width. Therefore, for non zero collector/base reverse bias, only the barrier height may be extracted. From figure 4.12 the bandgap narrowing value of 115meV is obtained for a collector-base reverse bias of 0V. Subtracting this value from the SiGe:C figure of 173meV gives a barrier height of 58meV. The intercept with the vertical axis $W_B/\Delta W$ has a value of 8.7, giving a barrier width of 5.6nm for a basewidth of 49nm. In addition it can be seen that applying a 1V reverse bias to the collector-base junction reduces the barrier height to 28meV, explaining the enhanced collector currents seen in figure 4.9. The estimated values are realistic, considering the barrier height should be less than the total bandgap difference between the SiGe base and the silicon collector (131meV).

4.5 Conclusions

In this chapter the effect of the addition of a background carbon concentration ($\approx 10^{20}\text{cm}^{-3}$) on boron diffusion in SiGe HBTs has been investigated. Two sets of devices have been fabricated, with and without the background carbon concentration, and were processed identically to allow direct comparisons of SIMS analysis and electrical performance. The temperature dependence of the collector current has been measured for the SiGe and SiGe:C HBTs, allowing the analysis method, described in section 2.8, to be applied. Bandgap narrowing values of 115meV and 173meV have been extracted for the SiGe and SiGe:C HBTs respectively, for a C/B reverse bias of 0V.

The effect of applying a 1V collector/base reverse bias to the devices has been investigated. The collector current was again measured as a function of temperature and the BGN analysis re-applied. Bandgap narrowing values of 145meV and 173meV were obtained for the SiGe and SiGe:C HBTs respectively. This shows that applying a 1V C/B bias to the SiGe HBT causes the extracted BGN to increase by 30meV, confirming the presence of a parasitic energy barrier. In contrast, the extracted value of 173meV remains unchanged for the SiGe:C HBT, indicating that no barrier exists. These results show that carbon is completely effective in suppressing the transient enhanced diffusion of the base dopant, due to the generation of excess interstitials created by the low doped collector and emitter implants. The extracted value of 173meV for the SiGe:C HBT is in reasonable agreement with the theoretical value of 150meV, given by the model of Jain *et al* [4], considering all of the uncertainties in the measured and modeled data.

Chapter 5

Effect of carbon position in the base for the elimination of parasitic energy barriers in SiGe:C HBTs

5.1 Introduction

In chapter 4 it was shown that a C concentration of approximately 10^{20}cm^{-3} was completely effective in suppressing transient enhanced diffusion in SiGe HBTs. In this chapter, a study is made of how the position and concentration of C within the base affects boron TED and the resulting parasitic energy barriers. Section 5.2 describes the device fabrication, giving details of carbon concentrations and positions within the SiGe base layer. Section 5.3 presents SIMS results, collector current, base current and base sheet resistance, measured in the temperature range 200K to 400K. As described in chapter 4, this allows the extraction of the bandgap narrowing in the SiGe base layer. Section 5.4 examines the effect of applying an increased collector/base reverse bias, showing whether parasitic energy barriers are present. Finally in section 5.5 some conclusions are drawn.

Table 5.1: SiGe:C HBT layer structure showing Ge content,carbon position and peak concentration.

Transistor Description	Ge Content (at.%)	Carbon Position	Peak C Conc. (cm^{-3})
NC	8.1	None	$\approx 5 \times 10^{18}$
CC	8.8	Collector	1.45×10^{20}
CB	11.6	Base	1.1×10^{19}
HCB	9.5	Base	1.5×10^{19}

5.2 Device Fabrication

The SiGe:C base layers were grown at IHP, Frankfurt(Oder), by solid source molecular beam epitaxy on (100) n-type Si substrates. Following the growth of a 30nm silicon buffer layer, a 20nm SiGe base, doped at 10^{19}cm^{-3}, with 5nm nominally undoped spacer layers on either side was grown. Finally a 60nm undoped silicon capping layer was grown which would later serve as the low doped emitter (LDE). The germanium content was targeted at 12%, however due to fluctuations in the silicon flux during growth the actual Ge content varied between 8 and 11.5%. In addition to the SiGe control wafer, 3 wafers were grown with different C profiles located in the transistor structure, keeping the boron doping level constant. Table 5.1 shows the compositions of the different devices and the position of the carbon in the transistor, where NC denotes the SiGe HBT without intentional C incorporation, CC denotes the SiGe:C HBT with carbon in the collector, CB denotes the SiGe:C HBT with the low carbon concentration in the base and HCB denotes the SiGe:C HBT with the high carbon concentration in the base. The other table entries denote the actual Ge content and peak C concentration within the transistor, measured by X-ray diffraction and SIMS respectively.

Transistors were fabricated from the as-grown wafers using a simple single mesa isolation process. The emitter was formed by CVD deposition of an amorphous silicon layer followed by arsenic implantation (10^{16}cm^{-2}, 45keV). Following emitter structuring, the extrinsic base contacts were formed by a high dose (2×10^{15}cm^{-2}, 35keV) BF_2 implant. Device fabrication was completed by a rapid thermal anneal cycle of 1000°C for 30 seconds to activate the implanted dopant and to diffuse-in the LDE using the polysilicon emitter as a diffusion source. A schematic cross section of the finished device is shown in figure 5.1.

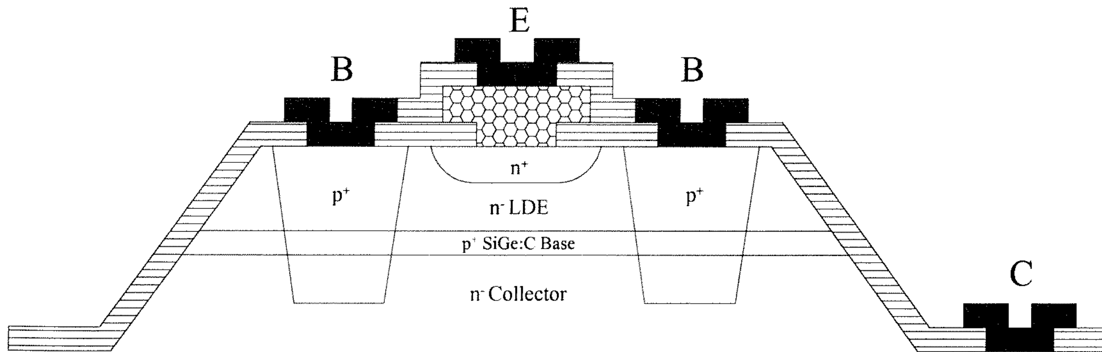


Figure 5.1: Schematic cross sectional diagram of the single mesa SiGe:C HBT used in this study.

5.3 Experimental Results and Discussion

5.3.1 SIMS Analysis

Figure 5.2 shows SIMS profiles for the SiGe HBT, transistor NC, without intentional carbon incorporation, where it can be seen that the peak boron concentration is $2.5 \times 10^{18}\text{cm}^{-3}$ and has a fairly broad profile. The full half width maximum (FHWM) value is approximately 31nm. The carbon concentration in the SiGe base is approximately constant, varying between $5.1 \times 10^{18}\text{cm}^{-3}$ and $5.2 \times 10^{18}\text{cm}^{-3}$. Finally, the polysilicon/silicon emitter interface is clearly delineated by the peaks in the arsenic and carbon profiles.

Figure 5.3 shows SIMS profiles for the SiGe:C HBT with carbon incorporated in the collector, transistor CC, where it can be seen that the C concentration steadily increases from a value of $1.8 \times 10^{18}\text{cm}^{-3}$ at the emitter/base junction, peaking at a value of $1.45 \times 10^{20}\text{cm}^{-3}$ at the collector/base junction and then decreases with depth into the collector. Once again, the boron profile is fairly broad with peak and FHWM values of $2.9 \times 10^{18}\text{cm}^{-3}$ and 30nm respectively. These values are almost identical to those of the SiGe HBT with carbon, suggesting that placing C in the collector has little effect on boron diffusion in the base.

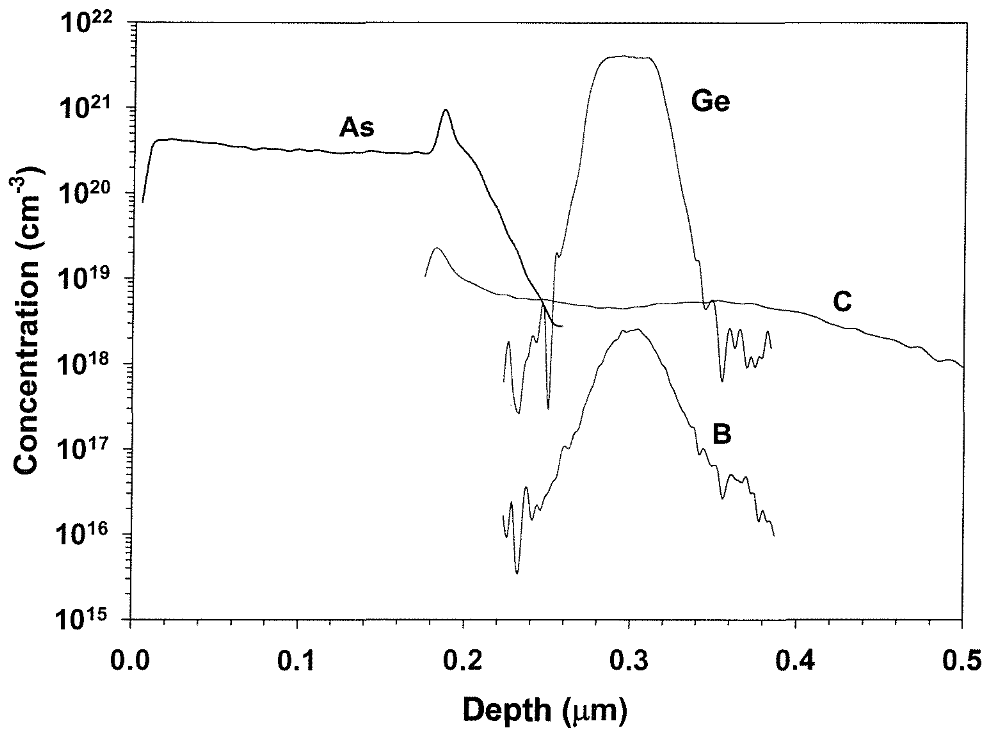


Figure 5.2: SIMS profiles of the SiGe HBT without intentional C incorporation, transistor NC.

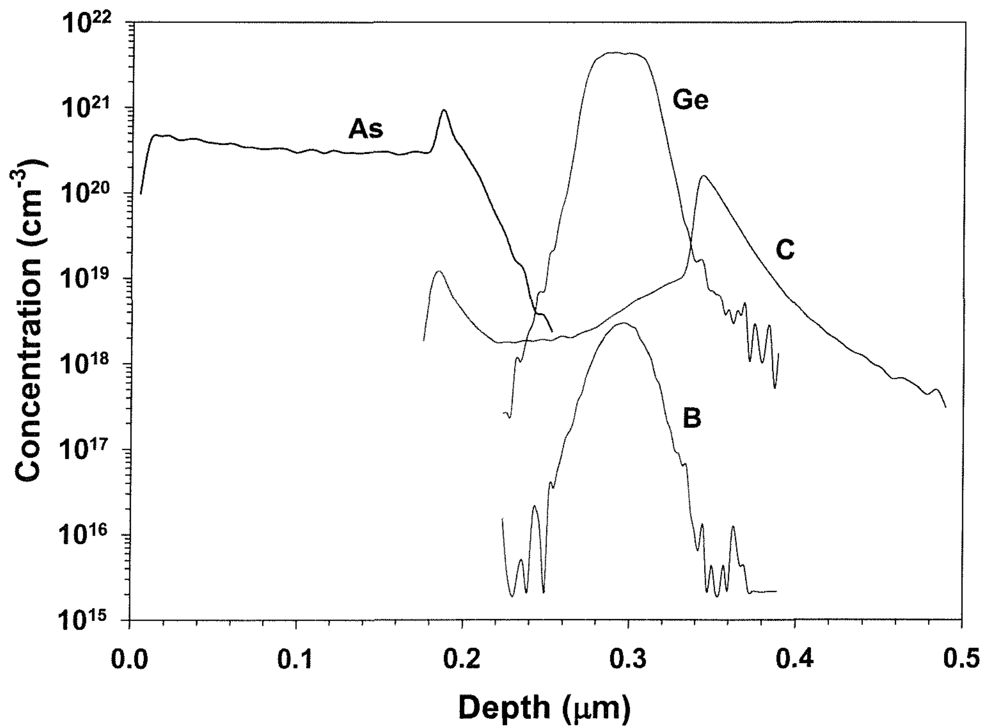


Figure 5.3: SIMS profiles of the SiGe:C HBT with C incorporated into the collector, transistor CC.

Figure 5.4 shows SIMS profiles for the SiGe:C HBT, transistor CB, with the lower C concentration incorporated in the base. From figure 5.4 it can be seen that the peak C concentration in the base is approximately $1.1 \times 10^{19}\text{cm}^{-3}$, dropping to values of $8 \times 10^{18}\text{cm}^{-3}$ at the emitter/base junction and $5 \times 10^{18}\text{cm}^{-3}$ at the collector/base junction. The peak value is nearly an order of magnitude lower than the desired value of 10^{20}cm^{-3} and can probably be attributed to the growth problems caused by the silicon flux fluctuations described earlier. In contrast to the two devices shown in figures 5.2 and 5.3, the boron profile in figure 5.4 is slightly narrower, with a FHWM value of approximately 23nm, and has a higher peak value of $5.3 \times 10^{18}\text{cm}^{-3}$.

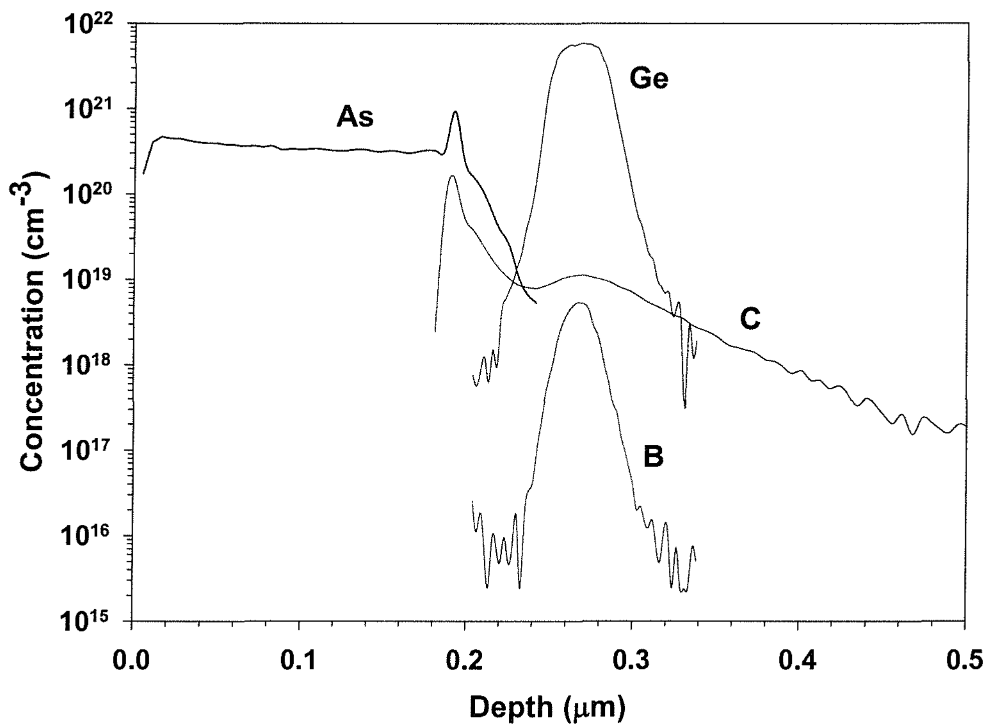


Figure 5.4: SIMS profiles of the SiGe:C HBT with the low C concentration in the base, transistor CB.

Finally, figure 5.5 shows SIMS profiles for the SiGe:C HBT, transistor HCB, with the higher carbon concentration incorporated in the base, where it can be seen that the C profile is very similar to that shown in figure 5.4. The peak C concentration in the base is slightly higher, with a value of $1.5 \times 10^{19}\text{cm}^{-3}$, but is virtually identical at the emitter/base and collector/base junctions.The peak boron concentration in the base is slightly lower than that of the SiGe:C HBT shown in figure 5.4, with a value of $4.1 \times 10^{18}\text{cm}^{-3}$, but has a very similar FHWM value of 24nm.

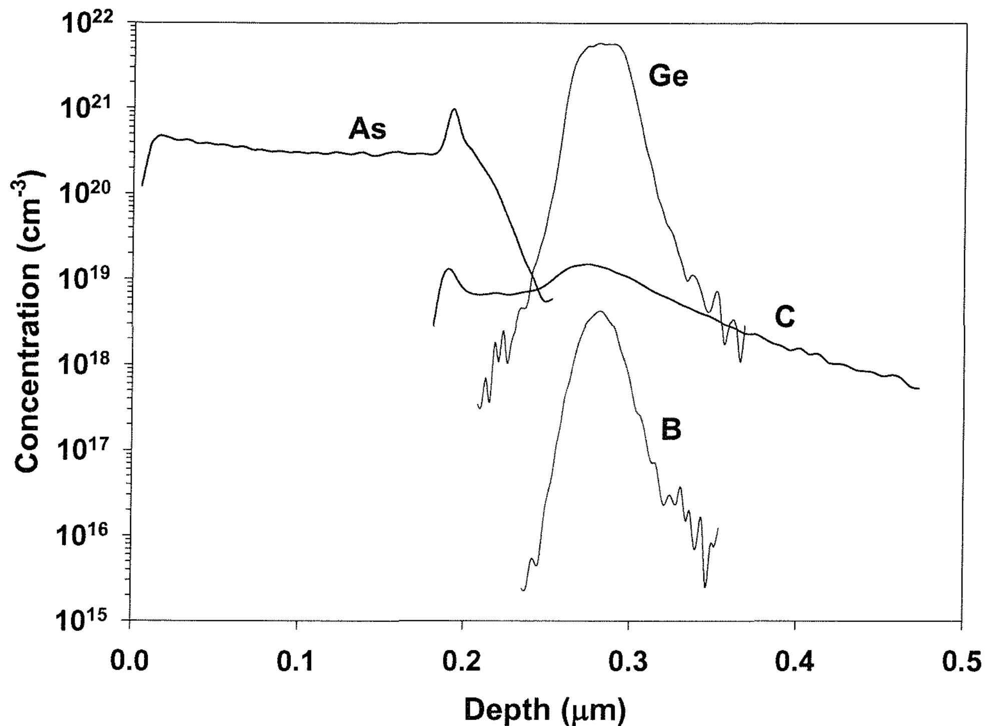


Figure 5.5: SIMS profiles of the SiGe:C HBT with the high C concentration in the base, transistor HCB.

5.3.2 Base Sheet Resistance

Figure 5.6 shows how the base sheet resistances for the four types of device vary with temperature, while table 5.2 shows calculated boron dose levels and measured base sheet resistances at 300K. From table 5.2 it can be seen that transistors NC, CC and CB have very similar boron dose levels, allowing direct comparisons between the base sheet resistance values to be made. The boron dose in transistor HCB, approximately a factor of 1.5 higher, will prevent direct comparison of this device with the other three.

Table 5.2: Boron dose levels and Base sheet resistance values measured at 300K for the SiGe and SiGe:C HBTs.

Transistor Description	Min/Max C in Base (cm^{-3})	Boron Dose 300K (cm^{-2})	300K Base Sheet Resistance (Ω/sq)
NC	$5 \times 10^{18}/5 \times 10^{18}$	1.24×10^{13}	4893
CC	$2 \times 10^{18}/1.8 \times 10^{19}$	1.33×10^{13}	5447
CB	$5 \times 10^{18}/1.1 \times 10^{19}$	1.24×10^{13}	6422
HCB	$5 \times 10^{18}/1.5 \times 10^{19}$	1.93×10^{13}	5690

Comparing the base sheet resistances of transistors NC, CC and CB in figure 5.6 it can be seen that transistor NC, with no intentional C incorporation, has the lowest base sheet resistance of the three devices. Transistor CB, with an identical boron dose has a substantially higher base sheet resistance, by approximately 25%, than transistor NC. A possible explanation for the difference between the sheet resistance values is C deactivation of dopant. Stolk *et al* [39] have shown that the introduction of $\approx 10^{19}\text{cm}^{-3}$ carbon reduces the boron activation to 80% for a layer annealed at 950°C, very similar to the C levels and anneal conditions used in this work. Transistor CC, with a similar boron dose has a consistently higher base sheet resistance, by approximately 19%, than transistor NC. The C concentration in the base of transistor CC is non-uniform, increasing from $2 \times 10^{18}\text{cm}^{-3}$ at the emitter, to $1.8 \times 10^{19}\text{cm}^{-3}$ at the collector. This could conceivably cause non-uniform boron deactivation across the base layer, giving a smaller increase in resistivity than a comparably doped layer with a more uniform C concentration (transistor CB).

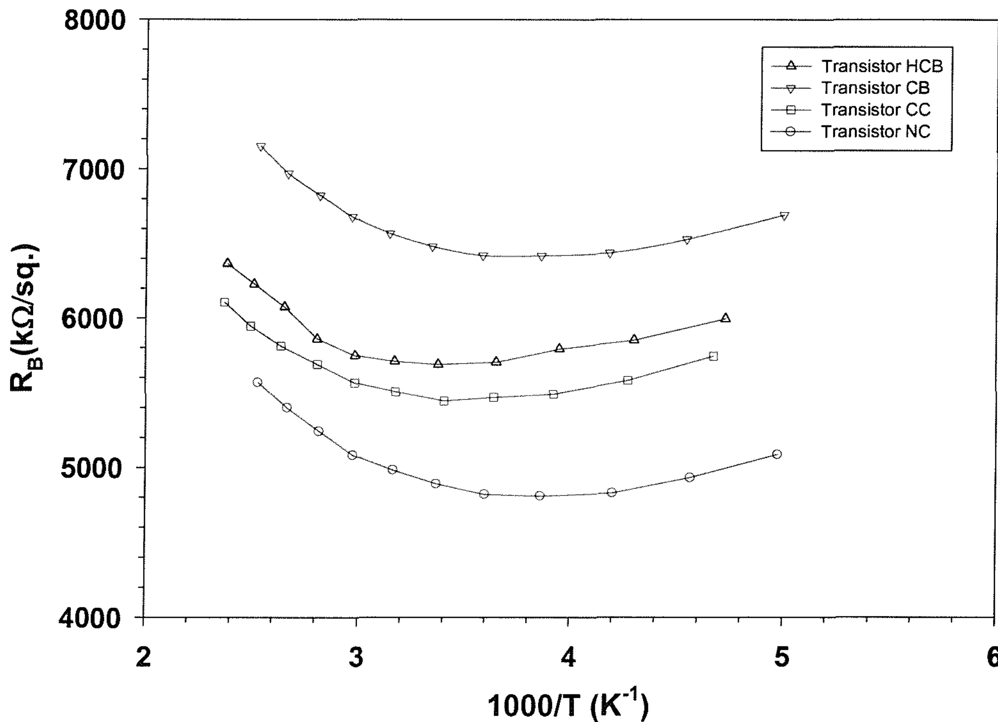


Figure 5.6: Intrinsic base sheet resistance as a function of reciprocal temperature for the SiGe and SiGe:C HBTs.

5.3.3 Collector and Base current measurements

Figures 5.7 and 5.8 shows Gummel plots for the four types of devices, measured at temperatures of 230K and 315K. Two points are readily observable. Firstly the

collector currents at both measurement temperatures for all four devices are near ideal over several orders of magnitude, with a typical value of 1.014 irrespective of carbon position. This means that the extraction method described in chapter 2 can be reliably used to find the bandgap narrowing in the SiGe base. Secondly, the base currents of all the devices are extremely non-ideal, with typical ideality factors of 1.89 and 1.81 at 230K and 315K respectively. Since the basewidths of all the devices used in this study are well within the critical thicknesses determined by their respective Ge contents, the non-ideality of the base current is unlikely to be due to misfit dislocations caused by strain relaxation. Other possible causes for the poor base current ideality are defects introduced during the growth of the base layers, metal contaminants from the MBE system, surface recombination or interstitial carbon introducing deep levels in the bandgap [119]. Since this study is primarily interested in the collector current, no further investigation into the causes of the base current non-ideality was carried out.

Figures 5.7 and 5.8 also show that the collector currents of transistors NC and CC are consistently lower than those of CB and HCB. This difference in collector currents, approximately a factor of 3 at 315K, rising to a factor of 4 at 230K, could be attributable to differences in base Gummel number or Ge content and hence prevents any conclusions about the presence of parasitic energy barriers to be drawn at this point.

5.3.4 Extraction of the bandgap narrowing in the base

Figure 5.9 shows bandgap narrowing plots for the four devices used in this study, obtained by applying the electrical analysis described in chapter 2. As discussed in chapter 4, only the high temperature data ($kT \leq 3.5K^{-1}$) is used to avoid doping tails in the base profile dominating the slope of the BGN plot. Several points are readily apparent. Firstly, all of the values of $J_C(T)/J_O(T)$ form a reasonably straight line allowing an accurate least squares fit to be obtained. Secondly, the intercepts with the vertical axis are all near unity, with the worst case value of 1.6 belonging to transistor CB. Since deviations of the intercept away from unity can signify problems with the temperature models and/or the presence of parasitic energy barriers, this result suggests that the models are reasonable and the amount of B out-diffusion from the base is small. Finally, there is a large variation in extracted slopes for the four devices, with transistor NC having the lowest value of 78meV, and transistor CB having the highest value of 126meV. However, this

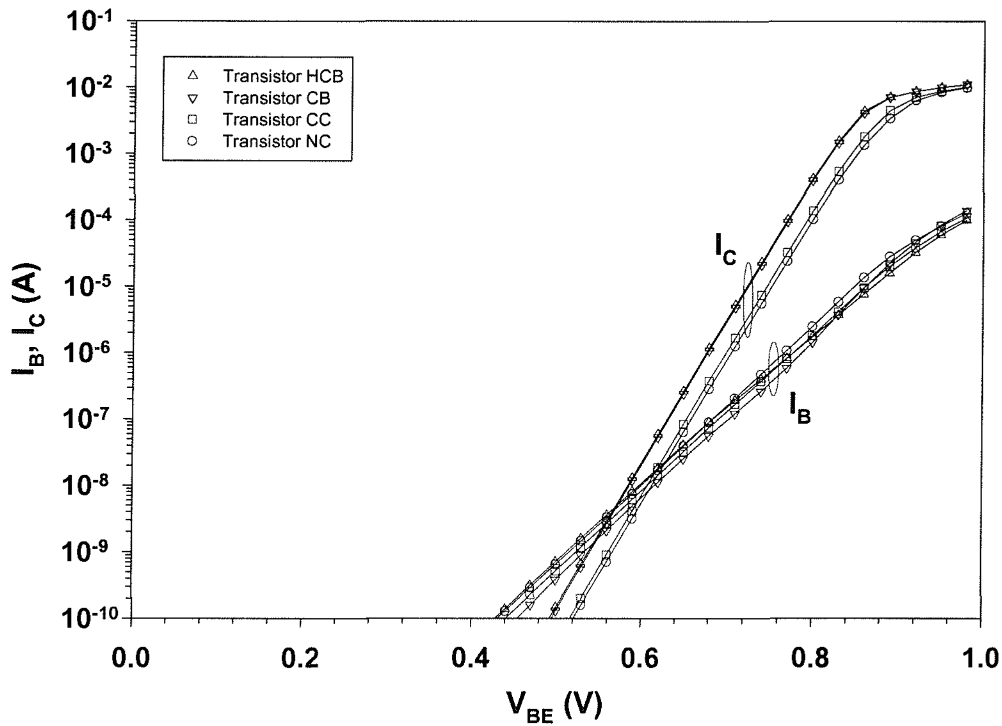


Figure 5.7: Gummel plots for transistors NC, CC, CB and HCB, measured at 230K with $V_{CB} = 0V$.

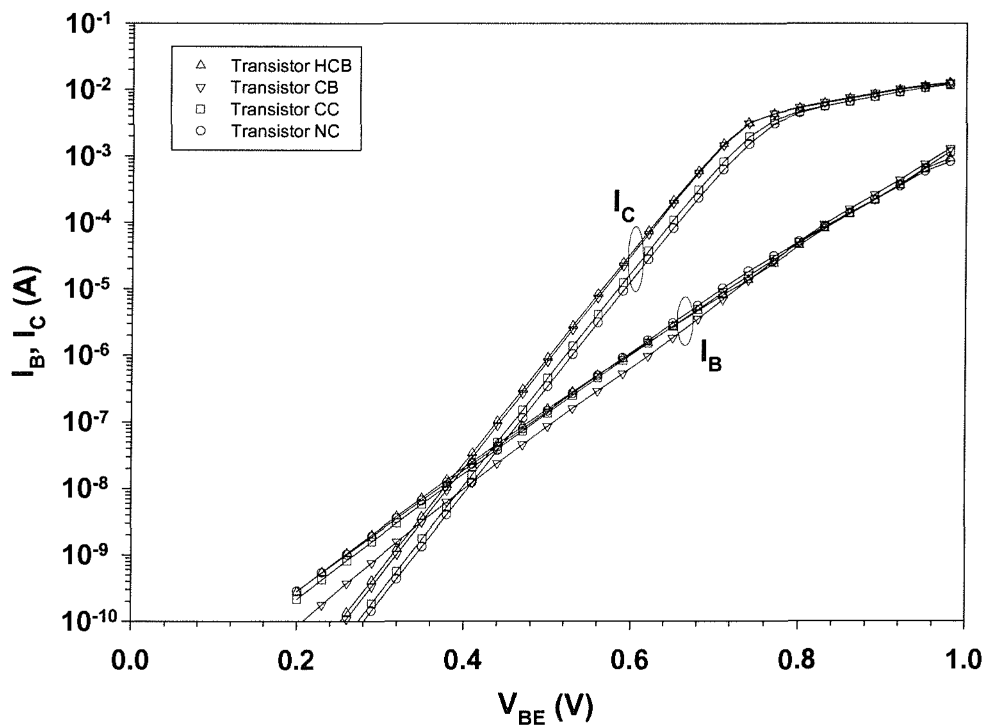


Figure 5.8: Gummel plots for NC, CC, CB and HCB, measured at 315K with $V_{CB} = 0V$.

is unsurprising since these two devices have the lowest and highest Ge contents respectively. Furthermore, the other two devices, transistors CC and HCB, also follow the trend of increased BGN with increasing Ge content, as expected. A more informative comparison would be to compare the extracted BGN values with theoretical values obtained using the model of Jain *et al* [4] and the models of Iyer *et al* [117] and Klaassen *et al* [85]. This is shown in table 5.3

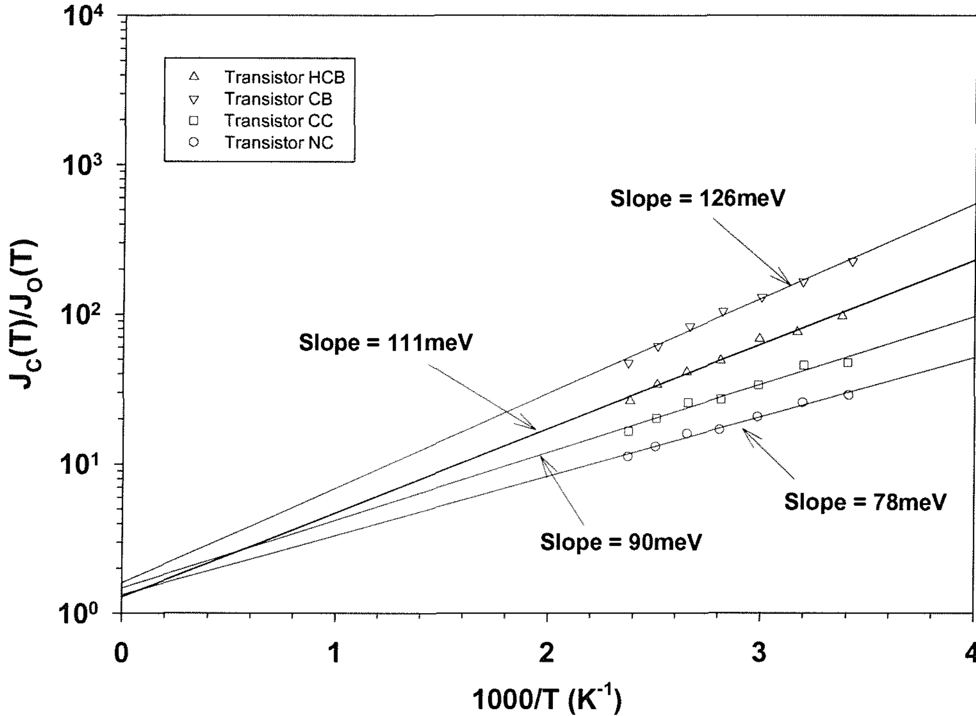


Figure 5.9: Bandgap narrowing plots for transistors NC, CC, CB and HCB, with a collector/base reverse bias of 0V.

Comparing the theoretical and extracted BGN values in table 5.3 it can be seen that the combined models of Klaassen *et al* [85] and Iyer *et al* [117] consistently predict a higher total BGN value than obtained from our electrical measurements. In contrast, it can be seen that the predicted BGN value using the model of Jain *et al* [4] gets steadily closer to the extracted value as more carbon is added, dropping from a difference of 20meV for transistor NC, to just 2meV for transistor HCB. Using the results of chapter 4, it is expected that the latter device will not suffer from parasitic energy barrier formation, suggesting that the Jain model gives a fairly accurate prediction of the total bandgap narrowing. The larger discrepancy in predicted values for transistors NC, CC and CB may therefore be attributable to parasitic energy barrier formation suppressing the slope of the BGN extraction plot. This will be examined in the next section where the devices are operated with an increased collector/base reverse bias of 2V.

Table 5.3: Comparison of theoretical and extracted total BGN in the SiGe and SiGe:C HBTs.

Transistor Description	Mean Base Doping ($\times 10^{18} cm^{-3}$)	Predicted Heavy Doping BGN [85] (meV)	Predicted Ge Induced BGN [117](meV)	Total Predicted BGN [85] + [117] (meV)	Total Predicted BGN [4] (meV)	Measured BGN (meV)
NC	1.55	35	69.9	104.9	98	78
CC	2.06	38.9	75.8	114.7	104	90
CB	2.66	42.3	99.6	141.9	116	126
HCB	3.06	44.3	81.6	125.9	109	111

5.4 Effects of Increased V_{CB} on bandgap narrowing extraction

Figures 5.10 to 5.13 show plots of the normalised collector current at collector/base reverse biases of 0 and 2V for transistors NC (figure 5.10), CC (figure 5.11), CB (figure 5.12) and HCB (figure 5.13). For transistor NC in figure 5.10, the slope of the graph is 78meV for a C/B reverse bias of 0V and 86meV for a reverse bias of 2V. This change in activation energy indicates the presence of a parasitic energy barrier at the C/B junction. For transistor CC (figure 5.11), the slope of the graph is 90meV for a C/B bias of 0V and 95meV for a reverse bias of 2V. The change in activation energy is smaller than observed in figure 5.10 (5meV compared with 8meV), but still indicates the presence of a parasitic energy barrier.

A similar result is obtained in figure 5.12 for transistor CB. However, for transistor HCB (figure 5.13), it can be seen that applying the C/B reverse bias has little effect. The slope of the characteristic is 111meV for a C/B bias of 0V and remains unchanged for a bias of 2V. This lack of sensitivity of the activation energy to the C/B reverse bias indicates that there are no parasitic energy barriers in this device. Table 5.4 summarises the extracted BGN data for all of the devices.

Table 5.4: Summary of extracted BGN values for C/B reverse biases of 0 and 2V.

Transistor Description	Carbon Position	Peak C Concentration (cm^{-3})	BGN ($V_{CB} = 0V$) (meV)	BGN ($V_{CB} = 2V$) (meV)
NC	None	$\approx 5 \times 10^{18}$	78	86
CC	Collector	1.5×10^{20}	90	95
CB	Base	1.1×10^{19}	126	131
HCB	Base	1.5×10^{19}	111	111

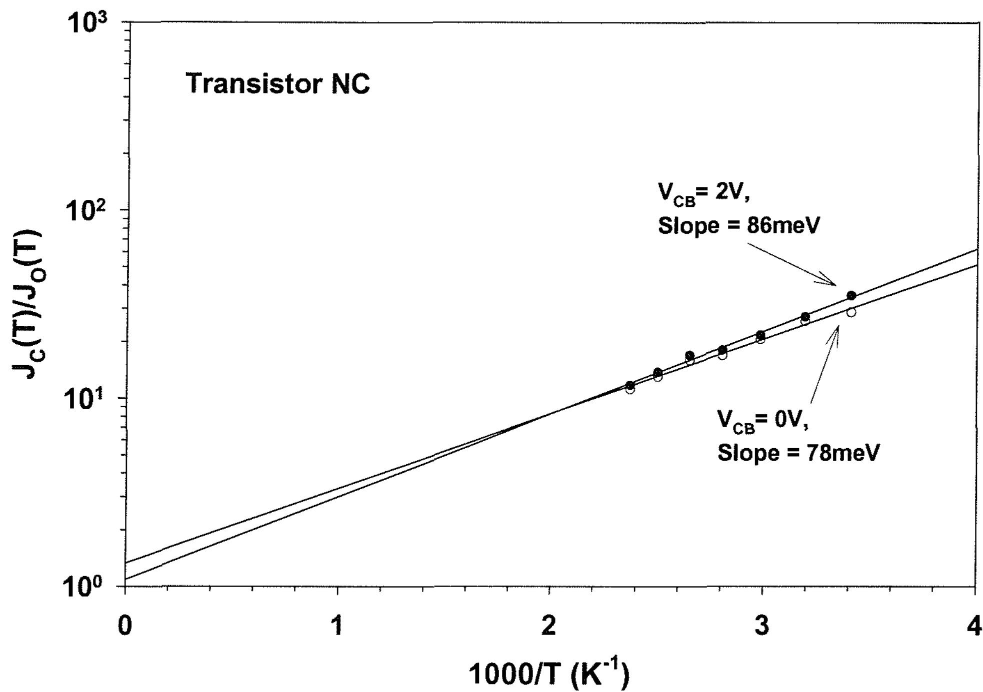


Figure 5.10: Bandgap narrowing plots for the SiGe HBT, transistor NC, with a collector/base reverse bias of 0 and 2V.

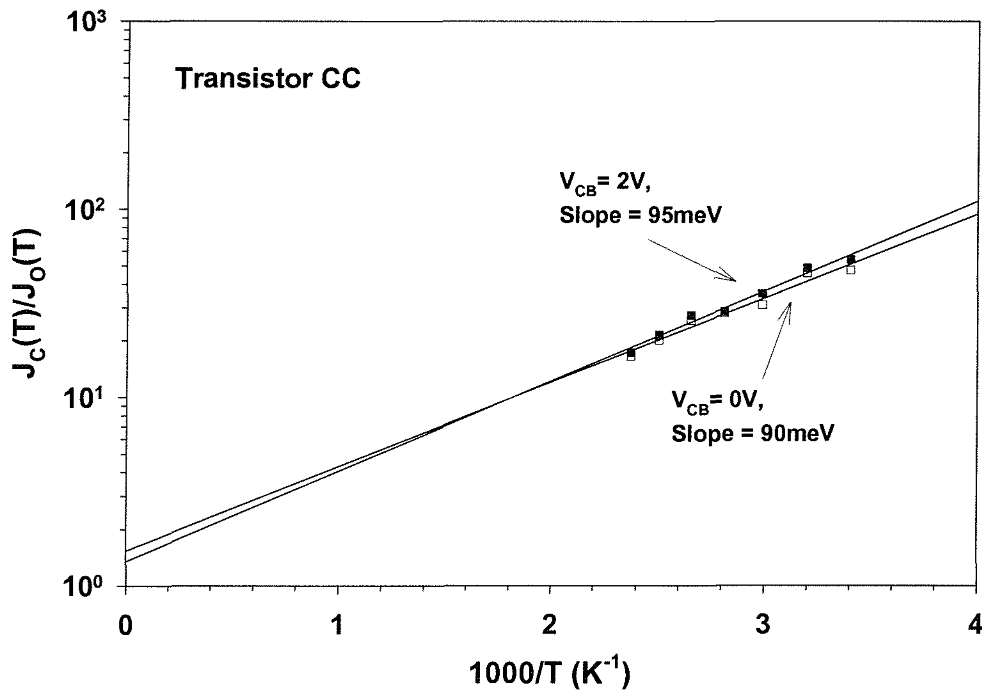


Figure 5.11: Bandgap narrowing plots for the SiGe:C HBT with carbon in the collector,transistor CC, with a collector/base reverse bias of 0 and 2V.

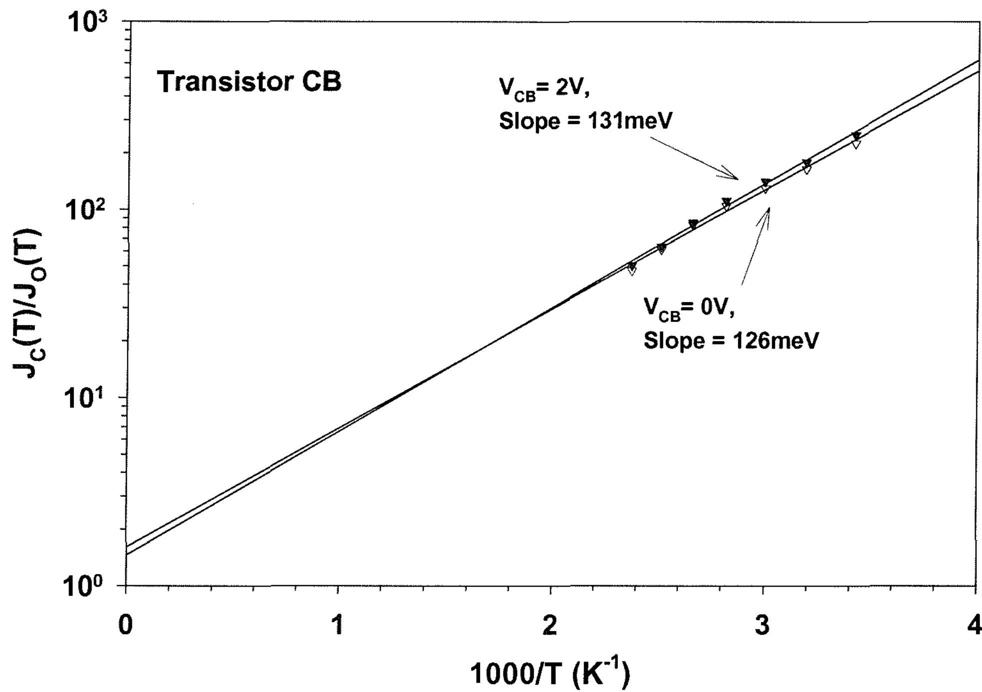


Figure 5.12: Bandgap narrowing plots for the SiGe:C HBT with the low C concentration in the base (transistor CB), with a collector/base reverse bias of 0 and 2V.

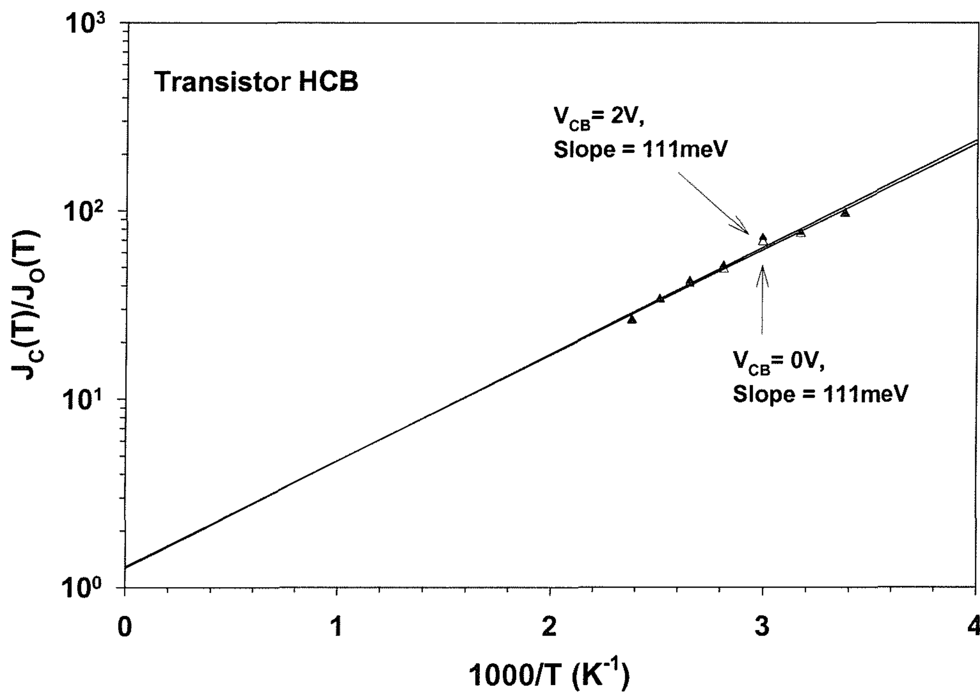


Figure 5.13: Bandgap narrowing plots for the SiGe:C HBT with the high carbon concentration in the base (transistor HCB), with a collector/base reverse bias of 0 and 2V.

These results show that the suppression of TED by the carbon is a localised phenomenon, since out-diffusion was only suppressed when the carbon was present in both the base and the spacers. This indicates that if the excess interstitials diffuse beyond the carbon rich region, TED will persist. This is consistent with the results of Stolk *et al* [40], who demonstrated that the interstitial population is only perturbed in the local vicinity of the carbon profile, thus only a localised reduction of the interstitial concentration can be expected. The localised suppression of TED by carbon is attributed to a continuous interaction of C atoms and silicon interstitials to form highly mobile C-I pairs. This interaction reduces the number of interstitials available to pair with substitutional boron atoms, thereby lowering the effective boron diffusivity, without fully suppressing the interstitial population. However the interstitials that are paired with the carbon atoms will be liberated when the C-I complex diffuses beyond the carbon profile, thus allowing TED to persist outside this region.

5.5 Conclusions

In this chapter the effect of carbon position and concentration on enhanced boron diffusion in SiGe HBTs has been investigated. Three sets of SiGe:C HBT were fabricated, one with the carbon placed in the collector (transistor CC) and two with C incorporated in the base at different concentrations (transistors CB and HCB). A SiGe HBT was also fabricated without intentional carbon incorporation to serve as a control device. All four types of HBT were processed identically to allow direct comparisons of SIMS profiles and electrical performance.

Bandgap narrowing values of 78meV, 90meV, 126meV and 111meV were obtained for transistors NC, CC, CB and HCB respectively, at a collector base reverse bias of 0V. Increasing the collector/base reverse bias to 2V resulted in corresponding BGN values of 86meV, 95meV, 131meV and 111meV. This shows that parasitic energy barriers are present in all of the devices except transistor HCB.

These results show that the lower C concentration of transistor CB, with a peak value, $1.1 \times 10^{19}\text{cm}^{-3}$, is insufficient to prevent TED. In contrast, raising the peak C concentration to a value of $1.5 \times 10^{19}\text{cm}^{-3}$, as in transistor HCB, completely suppressed the enhanced boron diffusion. This is in broad agreement with the work of Stolk *et al* [40] who have shown that a minimum concentration of 10^{19}cm^{-3}, substitutionally located, is required to prevent boron TED.

Finally results of transistor CC, with C in the collector, directly show that C located in this position is ineffective in stopping C/B parasitic energy barriers and that TED suppression by C incorporation is only a localised effect. This is in complete agreement with results of Stolk *et al* [40], who showed that boron profiles located below a carbon profile still exhibited enhanced diffusion, whilst those inside the C profile did not.

Chapter 6

Electrical Properties of in-situ doped n- and p-type Polycrystalline Si, $Si_{1-x}Ge_x$, $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ layers

6.1 Introduction

As discussed in chapter 1, there is considerable interest in the literature on single-crystal SiGeC for application in heterojunction bipolar transistors [45–47]. Eberl *et al* [31] have examined the effects of carbon incorporation in single crystal Si and SiGe layers using photoluminescence (PL) measurements on $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ quantum well structures. From an extrapolation of the PL results, it was found that for small C concentrations ($\leq 7\%$) the bandgap in the $Si_{1-y}C_y$ layer was reduced by 65meV/%C, with most of the offset occurring in the conduction band. In contrast, an increase of 24meV/%C was achieved in the $Si_{1-x-y}Ge_xC_y$ layer. Amour *et al* [30] have examined the effect of carbon on both unstrained and strained SiGeC single crystal layers and have found very different behaviours. In the strained pseudo-morhpic layers, the bandgap was found to increase by approximately 24meV/%C, in complete agreement with Eberl *et al*, whereas for the unstrained layers, the bandgap actually reduced by 10-20meV/%C for small C concentrations. Therefore it can be seen that the addition of carbon to Si and SiGe gives yet another degree of freedom in bandgap engineering. Although there is a large body of work on

single crystal SiGeC, relatively little, if any, has been published on the properties of polycrystalline SiGeC.

In this chapter the growth and electrical characterisation of heavily doped n- and p-type polycrystalline Si, $Si_{1-x}Ge_x$, $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ layers are presented. Section 6.2 describes the growth conditions used to obtain the polycrystalline films, showing how the introduction of germane and/or methylsilane affects growth rate and film composition. Section 6.3 presents results of sheet resistivity, effective carrier concentration and Hall mobility versus film composition, obtained from Hall measurements on van der Pauw structures, showing the effects of germanium and carbon incorporation on the polycrystalline layers. Finally in section 6.4 some conclusions are drawn from the experimental results.

6.2 Experimental Procedure

6.2.1 Growth Details

In-situ doped p- and n-type amorphous Si, $Si_{1-x}Ge_x$, $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ layers were deposited by low pressure chemical vapour deposition (LPCVD) using the cold-wall UHV compatible epitaxial reactor described in chapter 3. The growths were performed at 500°C for the p-type layers, and 540°C for the n-type layers, on oxide covered (600nm LTO), p-type, (100) silicon wafers. The deposition gases were Si_2H_6, GeH_4 and $SiCH_6$ for the silicon, germanium and carbon sources respectively. The in-situ dopant was introduced during growth using PH_3 for the n-type source and B_2H_6 for the p-type source. The difference in growth temperatures was necessary since it was found that addition of Diborane to the growth ambient at 540°C was sufficient to move the deposition from the amorphous to the polycrystalline regime. In all cases, the growth pressure was maintained at 4 Torr. For the $Si_{1-x}Ge_x$ layers, the germane flow was varied between 0sccm to 75sccm, keeping all other gas flows constant, giving a compositional range of 0 to 18%. To study the effects of carbon incorporation on the electrical characteristics of poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the carbon concentration in successive layers was varied by adjusting the methylsilane flow rate from 0 sccm to 10 sccm, whilst keeping the other gas flows constant. Following deposition, the layers were capped with 200nm of LTO and then annealed at 1000°C for 30 seconds in a rapid thermal processor, in order to regrow the amorphous layers into polycrystalline material. The oxide

cap was then removed and the van der Pauw structures defined using a SF_6 dry etch process. Fabrication was completed by contact metallisation, using 1000nm of Al/Si (1%), and alloy anneal at 350°C in an H_2/N_2 ambient. A schematic cross section of the van der Pauw structure is shown in figure 6.1

In addition to the amorphous depositions, in-situ doped p-type polycrystalline $Si_{1-x}Ge_x$ ($0 \leq x \leq 0.18$) layers were deposited at 625°C to investigate if the deposition temperature has any effect on electrical properties. Apart from the increased deposition temperature, all other growth parameters were kept the same as above. After deposition, the wafers were diced into small pieces and annealed at 800, 900 and 1000°C for 30 seconds. The resistivities of the as-grown and annealed samples were then measured using the standard four point probe technique. These polySiGe layers were used as control samples to check that layers without C had reasonable resistivity values comparable to those previously reported in the literature. This will allow any observed effects on the electrical properties of the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ to be attributable to the influence of the carbon alone.

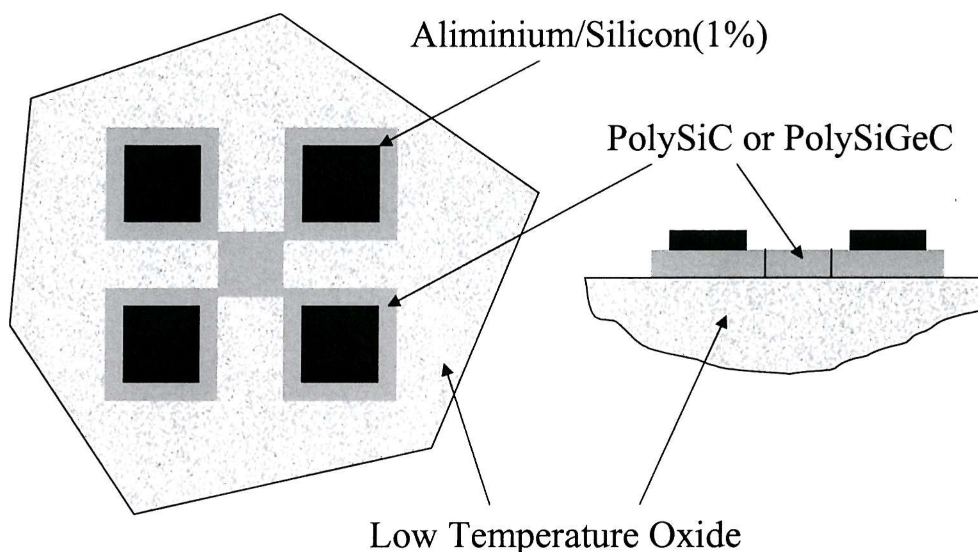


Figure 6.1: Schematic cross sectional diagram of the van der Pauw structures used to test the effect of carbon on polySi and polySiGe layers.

Figure 6.2 shows the normalised growth rates for the n- and p-type poly$Si_{1-x}Ge_x$ layers, deposited at 540°C and 500°C respectively, as a function of germane flow. For the n-type layers, it can be seen that the growth rate increases with increasing germane flow, rising to a value of 1.48 at a flow of 75sccm. The p-type layers show a much smaller increase in growth rate with germane flow, only rising to 1.13 for the

75sccm case. This can probably be attributed to the lower growth temperatures used for the p-type layers since Kulkarni *et al* [72] have shown that for growths using disilane, the surface hydrogen desorption is much slower at wafer temperatures $\leq 500^oC$. Since deposition requires the chemisorption of disilane and subsequent desorption of surface silicon hydrides, this reduction in hydrogen desorption would explain the smaller increase in growth rate for the p-type layers.

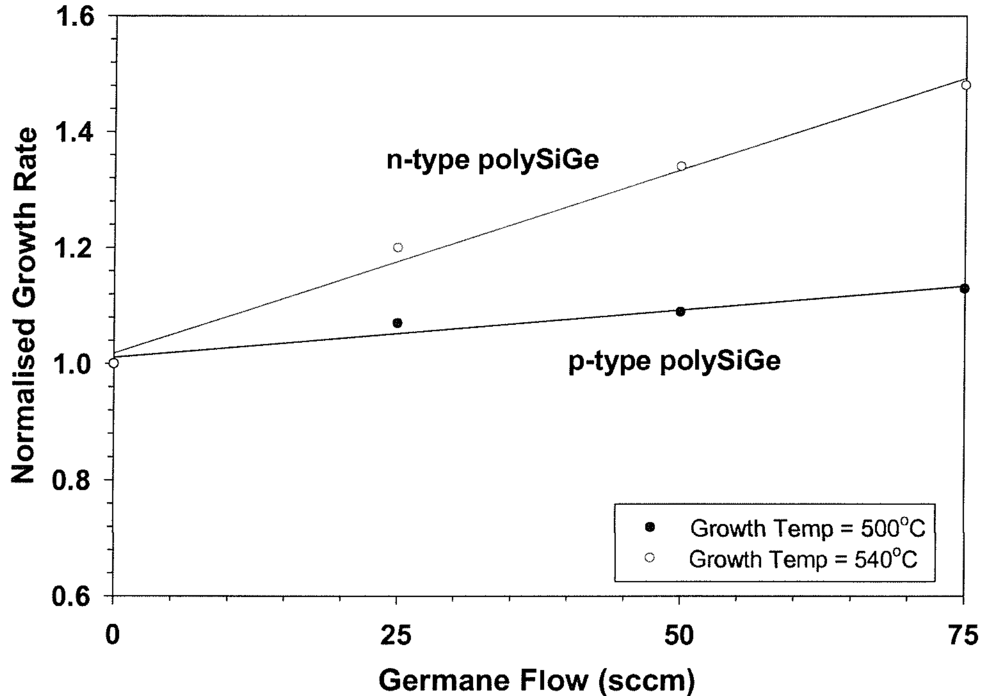


Figure 6.2: Graph showing the growth rate of poly$Si_{1-x}Ge_x$ versus germane flow rate, normalised against the polySi growth rate.

Figures 6.3 and 6.4 show the normalised growth rates of the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers versus methylsilane flow rate, where it can be seen that for the n-type layers the addition of $SiCH_6$ to the growth ambient has no significant effect on the growth rate of either the poly$Si_{1-y}C_y$ or poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. In contrast, for the p-type layers, figures 6.3 and 6.4 show a significant decrease in the normalised growth rate with increasing $SiCH_6$ flow, dropping to values of 0.48 and 0.6 for the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ cases respectively. Once again, these differences can probably be attributed to the difference in growth temperature and subsequent effects on surface hydrogen desorption.

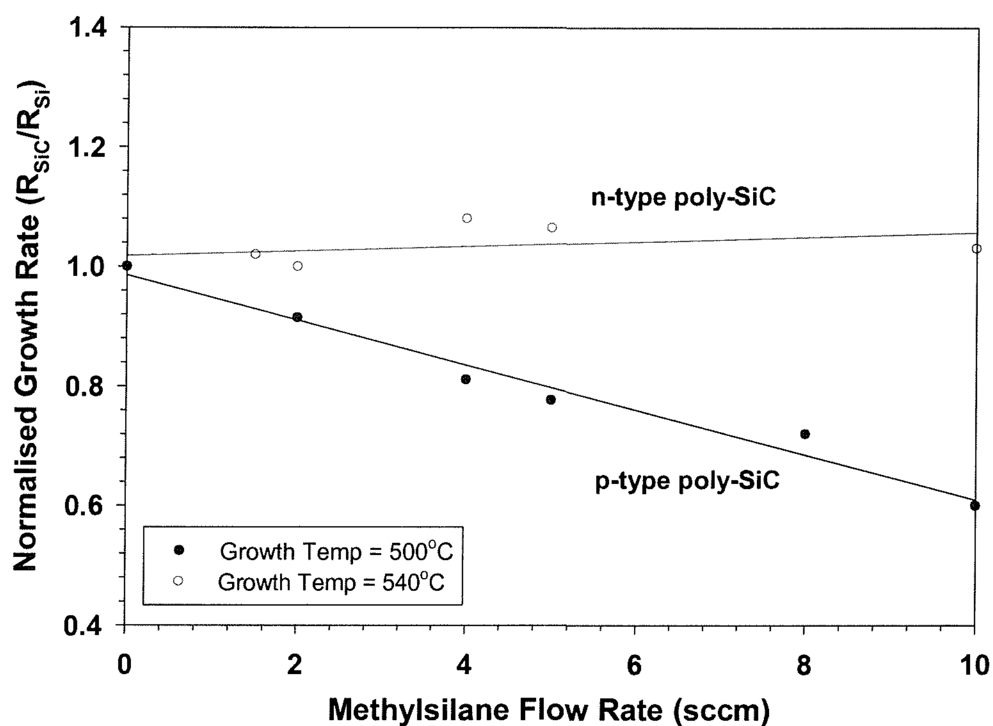


Figure 6.3: Graph showing the growth rate of poly$Si_{1-y}C_y$ versus methylsilane flow rate, normalised against the polySi growth rate.

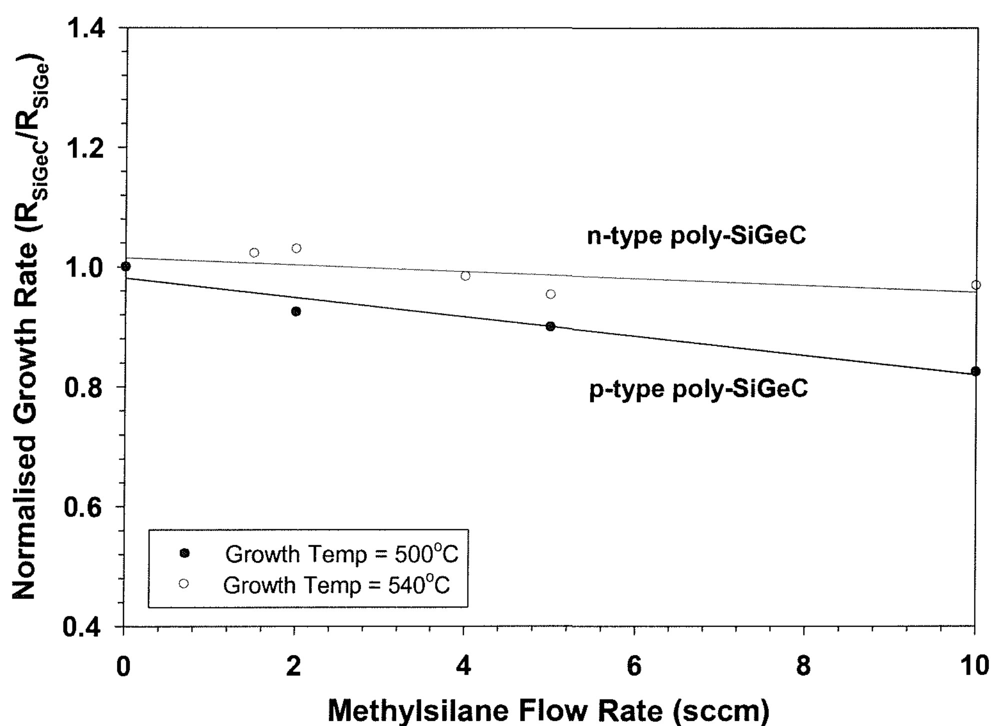


Figure 6.4: Graph showing the growth rate of poly$Si_{0.82-y}Ge_{0.18}C_y$ versus methylsilane flow rate, normalised against the polySiGe growth rate.

6.3 Results

6.3.1 SIMS Analysis

Figures 6.5 and 6.6 show SIMS profiles for the p- and n-type polycrystalline $Si_{1-x}Ge_x$ layers grown with a germane flow rate of 25sccm. For the p-type layer, it can be seen that the boron and germanium concentrations are approximately uniform throughout the layer. The boron concentration at the surface is approximately $1.7 \times 10^{20}cm^{-3}$, rising to a value of $1.85 \times 10^{20}cm^{-3}$ adjacent to the interface. The corresponding germanium concentrations are $5.1 \times 10^{21}cm^{-3}$ and $5.8 \times 10^{21}cm^{-3}$ respectively. This corresponds to a germanium content of approximately 10.8%. For the n-type polycrystalline $Si_{1-x}Ge_x$ layer, the phosphorus and germanium profiles are again nearly constant throughout the layer. The phosphorus concentrations near the surface and adjacent to the interface are $4 \times 10^{19}cm^{-3}$ and $3.75 \times 10^{19}cm^{-3}$. The corresponding Ge concentrations are $5.3 \times 10^{21}cm^{-3}$ and $5.7 \times 10^{21}cm^{-3}$, giving an average content of 11%. In both cases, the interface with the polycrystalline layer and the underlying silicon dioxide is delineated by peaks in the doping profiles.

Figures 6.7 and 6.8 show SIMS profiles for the p- and n-type polycrystalline $Si_{1-y}C_y$ layers grown with a methylsilane flow rate of 2sccm. Once again, for the p-type layer, it can be seen that the boron and carbon concentrations are approximately uniform throughout the layer. The carbon concentration at the surface is approximately $9.2 \times 10^{20}cm^{-3}$ rising to a value of $1.3 \times 10^{21}cm^{-3}$ adjacent to the interface. The corresponding boron concentrations are $6 \times 10^{20}cm^{-3}$ and $8.3 \times 10^{20}cm^{-3}$ respectively. The position of the interface between the polycrystalline $Si_{1-y}C_y$ and the underlying silicon dioxide is delineated by peaks in the boron and carbon profiles. For the n-type polycrystalline $Si_{1-y}C_y$ layer, the phosphorus and carbon profiles are again approximately constant throughout the layer. The carbon concentrations at the surface and adjacent to the interface are $3 \times 10^{20}cm^{-3}$ and $1.9 \times 10^{20}cm^{-3}$, and the corresponding phosphorus concentrations are $1.2 \times 10^{19}cm^{-3}$ and $1.18 \times 10^{19}cm^{-3}$ respectively.

Figures 6.9 and 6.10 show SIMS profiles of the p- and n-type SiGeC layers grown with a methylsilane flow rate of 2sccm. For the p-type layer in figure 6.9 it can be seen that the carbon and boron profiles are also nearly constant throughout the layer. The carbon concentration at the surface is $\approx 2 \times 10^{20}cm^{-3}$ and adjacent to the interface is $\approx 1.2 \times 10^{20}cm^{-3}$, while the corresponding boron concentrations are $\approx 2.1 \times 10^{20}cm^{-3}$ and $\approx 1.6 \times 10^{20}cm^{-3}$ respectively. As in the poly$Si_{1-y}C_y$

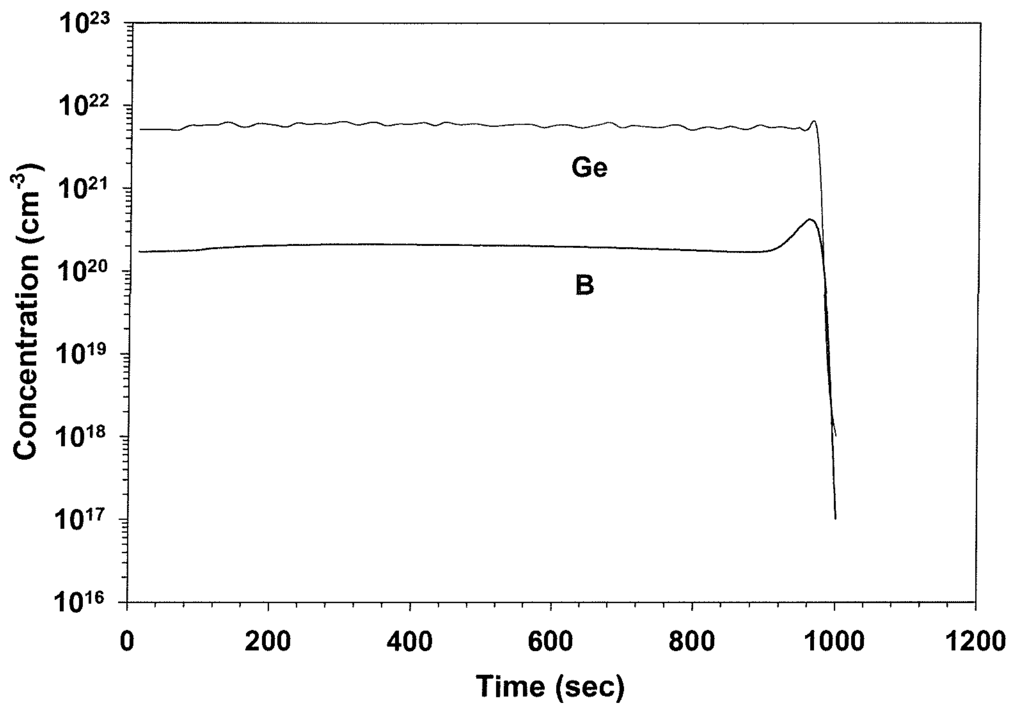


Figure 6.5: SIMS analysis results of the p-type poly$Si_{1-x}Ge_x$ layer for a germane flow of 25sccm, showing boron and germanium profiles.

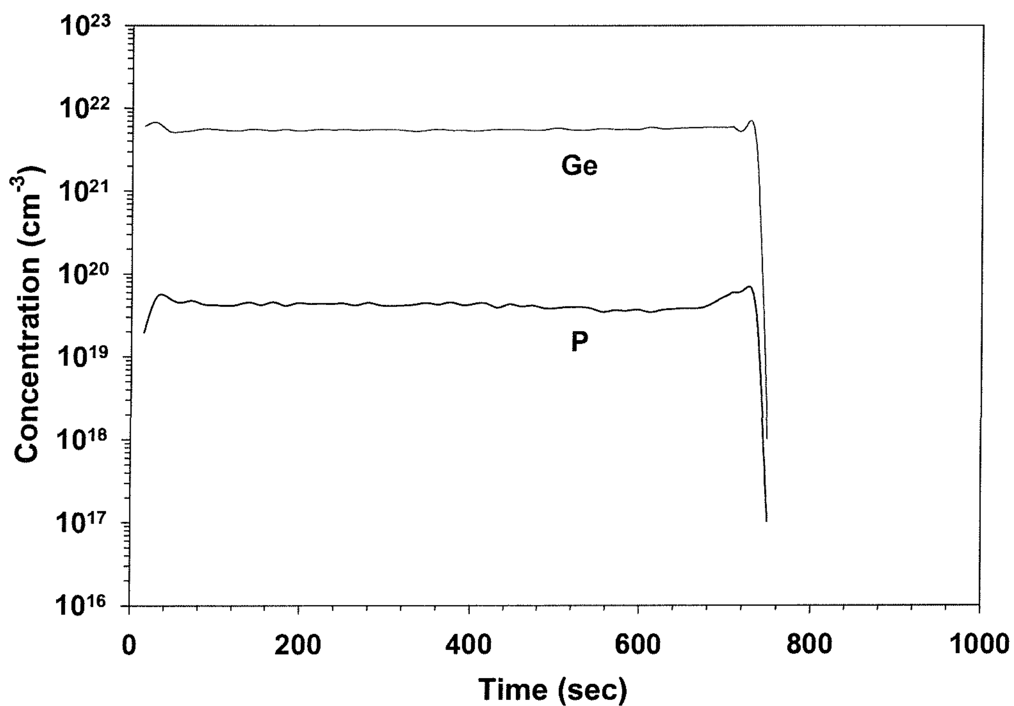


Figure 6.6: SIMS analysis results of the n-type poly$Si_{1-x}Ge_x$ layer for a germane flow of 25sccm, showing phosphorus and germanium profiles.

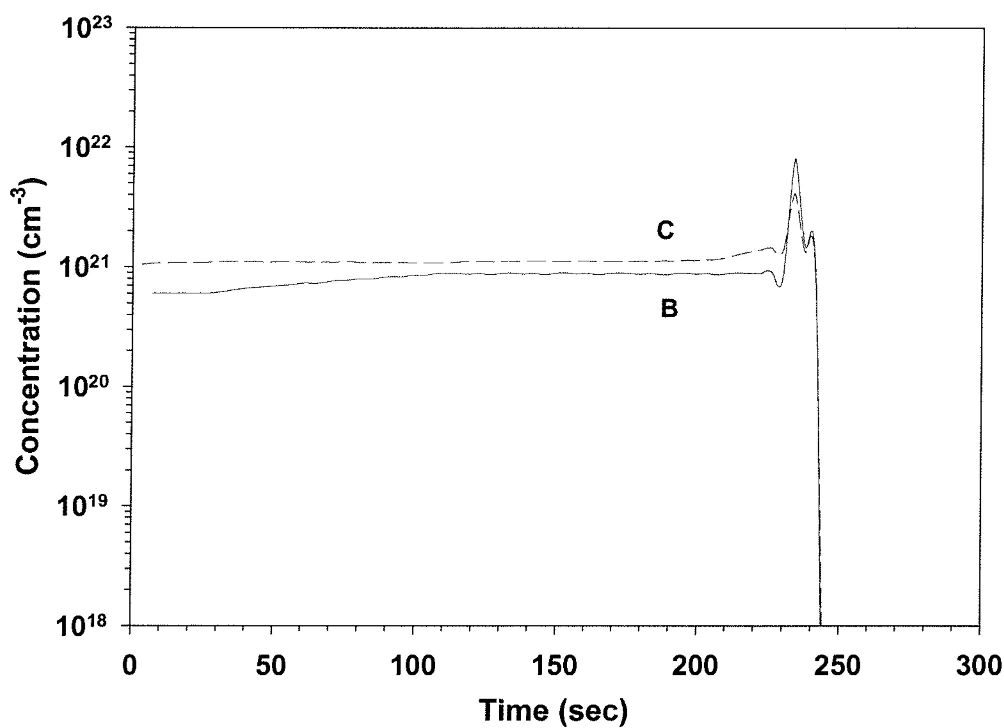


Figure 6.7: SIMS analysis results of the p-type poly$Si_{1-y}C_y$ layer for a methylsilane flow of 2sccm, showing boron and carbon profiles.

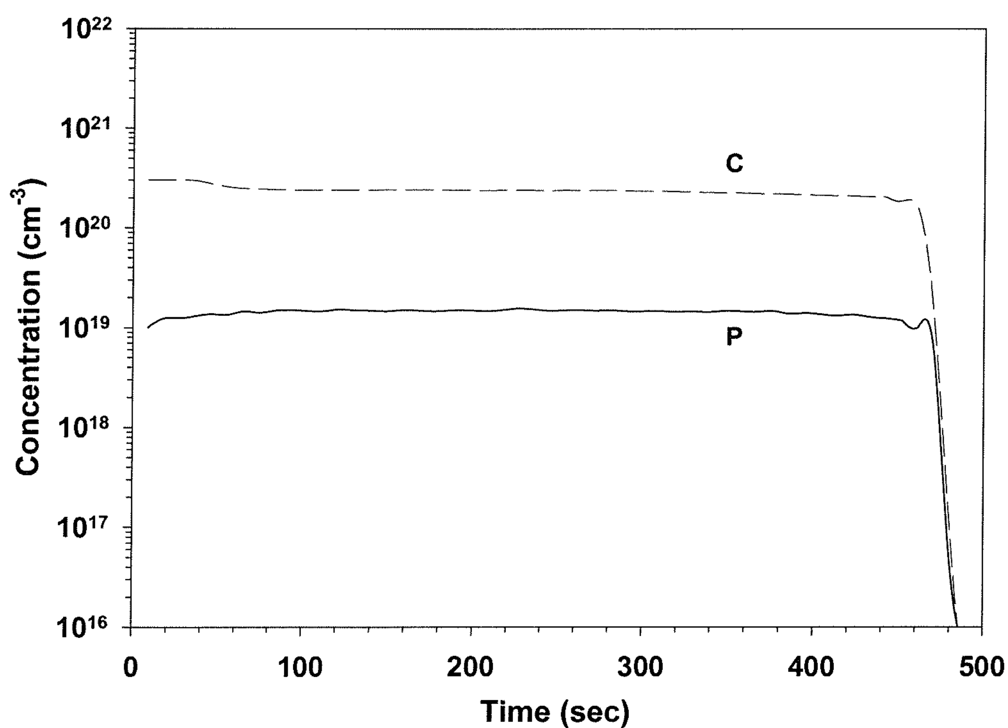


Figure 6.8: SIMS analysis results of the n-type poly$Si_{1-y}C_y$ layer for a methylsilane flow of 2sccm, showing phosphorus and carbon profiles.

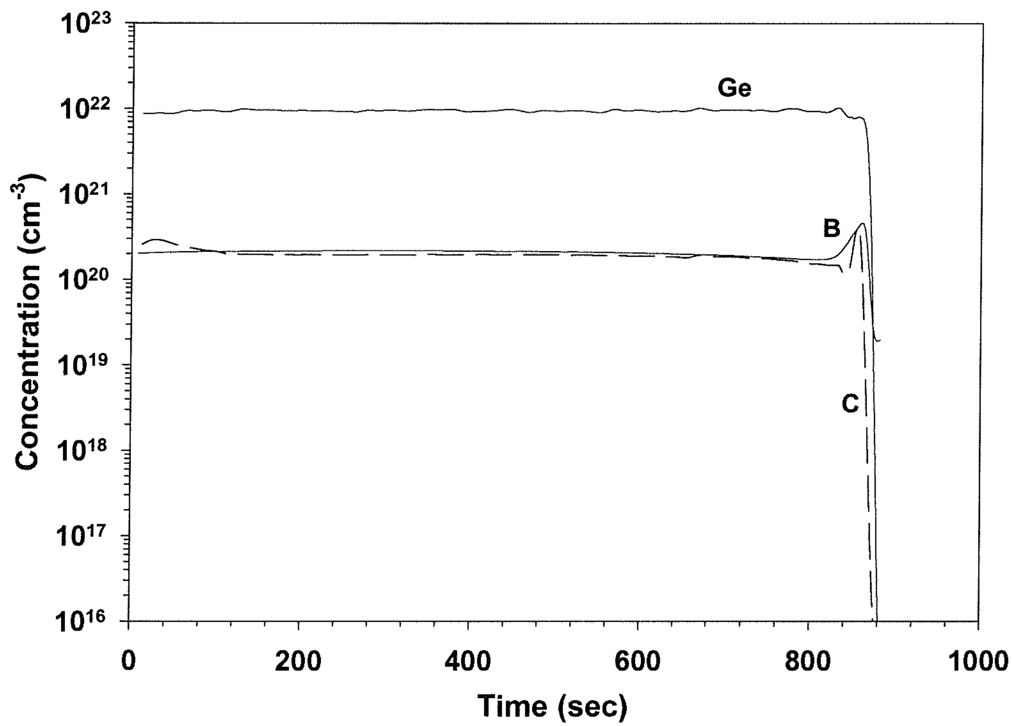


Figure 6.9: SIMS analysis results of the p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layer for a methylsilane flow of 2sccm, showing boron, carbon and germanium profiles.

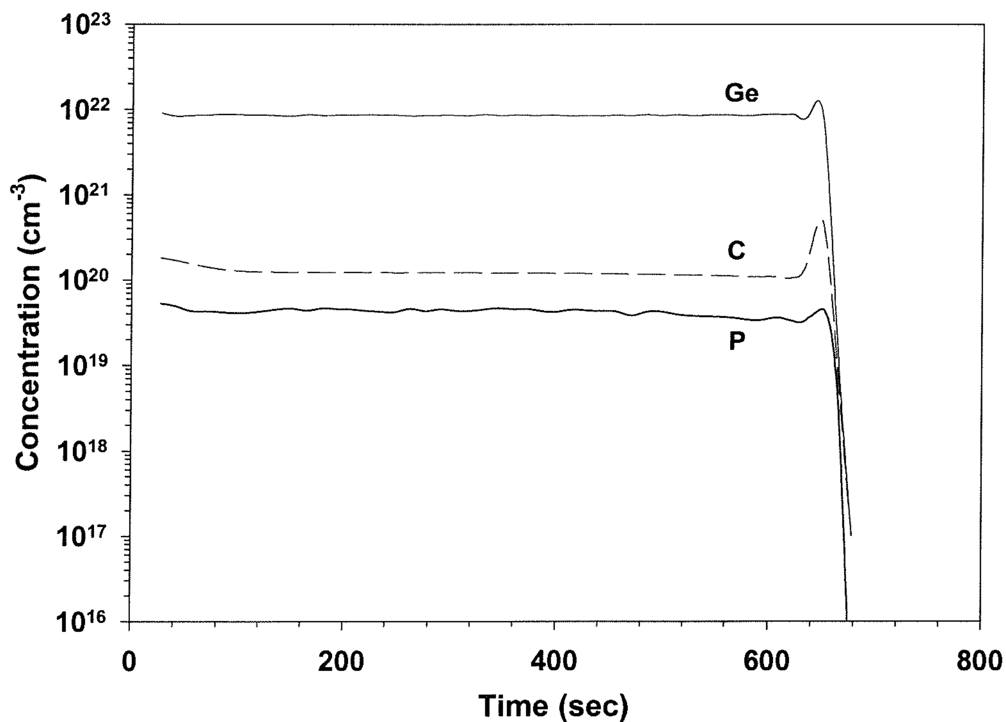


Figure 6.10: SIMS analysis results of the n-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layer for a methylsilane flow of 2sccm, showing phosphorus, carbon and germanium profiles.

case, the poly/oxide interface is delineated by the small peaks in the boron and carbon profiles. For the n-type polycrystalline SiGeC film, figure 6.10, it can be seen that the carbon concentrations at the surface and adjacent to the interface are $\approx 1.2 \times 10^{20}\text{cm}^{-3}$ and $\approx 1 \times 10^{20}\text{cm}^{-3}$, whilst the corresponding phosphorus concentrations are $\approx 4 \times 10^{19}\text{cm}^{-3}$ and $\approx 3 \times 10^{19}\text{cm}^{-3}$ respectively.

Comparing figures 6.7, 6.8, 6.9 and 6.10, several observations are readily apparent. Firstly, for the p-type layers, it can be seen that the boron concentration in the poly$Si_{1-y}C_y$ layer is over a factor of 3 higher than that found in the corresponding poly$Si_{0.82-y}Ge_{0.18}C_y$ layer. In contrast, for the n-type layers, the phosphorus concentration in the poly$Si_{1-y}C_y$ layer is actually a factor of 2 lower than its poly$Si_{1-x-y}Ge_xC_y$ counterpart. Finally, it can be seen that for both the p- and n-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the SIMS profiles show a constant Ge content of approximately 18%, with no evidence of segregation at the poly/oxide interface.

A graph of carbon concentration versus methylsilane flow rate is shown in figure 6.11, where it can be seen that at higher $SiCH_6$ flows there is a significant difference in the amount of carbon incorporated in the n- and p-type layers. At a flow of 10sccm $SiCH_6$, the amount of carbon in the p-type poly$Si_{1-y}C_y$ layer is approximately 4 times that found in the corresponding n-type layer. This falls to just over a factor of 2 for the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. A possible explanation for these differences is that phosphine has been shown to be very effective at blocking surface sites for silane chemisorption, thus inhibiting growth [120, 121]. In contrast, diborane was found not to block the surface sites, allowing easier chemisorption of SiH_4 and better growth rates. Since the chemisorption of $SiCH_6$ is likely to be similar to that of silane, the reduced number of available surface sites could lead to a reduction in the amount of carbon incorporated into the layer. It should be noted that the carbon content was calculated from the SIMS data using an implanted standard. Since the implanted sample was not calibrated to a known carbon concentration,the absolute values are likely to be inaccurate ($\pm 20\%$). However, since the SIMS analysis was performed on the layers in successive runs, using the same conditions each time, the relative concentrations between the layers should be reliable.

Figure 6.11 also shows that the C concentrations found in the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers are broadly similar, differing by a maximum of 0.3% at the highest methylsilane flow, whereas the corresponding C concentrations in the p-type layers differ by a factor of 2. The difference between the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers can probably be attributed to the fact that although the methylsilane flows were the same, the addition of germane to the growth ambient

actually reduces the methylsilane partial pressure, hence reducing the amount of carbon incorporated in the layer. However, for the p-type layers, the factor of 2 difference in C concentration is too large to be attributable to a reduction in the partial pressure and means that some other mechanism must be involved. This needs further investigation to fully understand the growth kinetics involved.

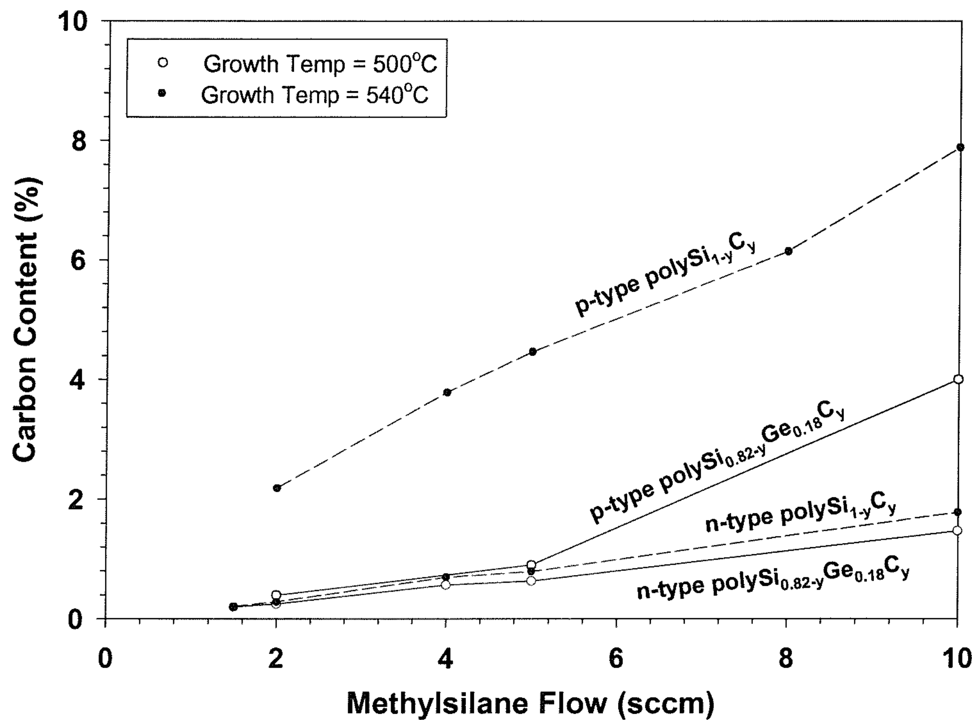


Figure 6.11: Plot of carbon concentration versus Methylsilane flow for the n- and p-type $polySi_{1-y}C_y$ and $polySi_{0.82-y}Ge_{0.18}C_y$ layers.

6.3.2 Sheet Resistivity of PolySi Layers

Table 6.1 summarises measured resistivities of n- and p-type polysilicon layers and compares the layers grown in this work with previously reported values. For the n-type polySi films, it can be seen that the layers grown by Grahn *et al* [122] offer the closest comparison in terms of doping level and anneal schedule to those in this work. The layers were deposited at temperatures in the range of 415°C to 560°C at a pressure of 0.3 Torr, using disilane (100%) and phosphine (1% diluted in H_2) as the silicon and phosphorus source gases respectively. Following deposition, the layers were annealed at 1050°C for 10 seconds and then patterned into clover leaf van der Pauw structures for resistivity and Hall measurements. The resistivity value obtained was approximately 100mΩcm for a doping level of $3 \times 10^{19}cm^{-3}$. This compares to a resistivity value of 44mΩcm for a doping level of $1.2 \times 10^{19}cm^{-3}$ for

the layers in this work. Therefore it can be seen that the resistivity of the layers grown by Grahn *et al* have a resistivity which is over a factor of 2 greater than the layers in this work, even though they have a higher doping level. This suggests that the grain size in the layers grown by Grahn *et al* is smaller than that of the layers in this work.

Table 6.1: Comparison of reported resistivity values for n- and p-type polysilicon.

Reference	Layer Type	Resistivity (mΩcm)	Doping Concentration (cm^{-3})	Anneal Schedule (°C)
This work	n-type	44	1.2×10^{19}	1000, 30sec
Grahn [122]	n-type	100	3×10^{19}	1050, 10sec
Salm [66]	n-type	30	1.7×10^{20}	950, 30min
Tsai [62]	n-type	5	1×10^{20}	600, 30hrs
This work	p-type	1.35	7×10^{20}	1000, 30sec
Salm [66]	p-type	10	1×10^{20}	950, 30min
Tsai [62]	p-type	22	1×10^{20}	600, 3hrs

Tsai *et al* [62] have also examined the electrical properties of n-type implanted polysilicon layers and have reported resistivity values as low as 5mΩcm for a doping level of approximately $10^{20}cm^{-3}$. This is almost an order of magnitude lower than the resistivity of the n-type layer reported in this work. However, the doping concentration in the n-type layer of Tsai *et al* is approximately an order of magnitude higher than the layers in this work. In addition, the layers were grown at 600°C in a commercial LPCVD system and then underwent solid phase recrystallisation (SPC) at 600°C in nitrogen for 65 hours. Following SPC, the undoped layers were implanted with P^+ at a dose of $2 \times 10^{15}cm^{-2}$ and then annealed again at 600°C for a further 30 hours. It is clear therefore that the annealing schedules used by Tsai *et al* are completely different than those used in the present work, and hence a direct comparison is difficult. Nevertheless, considering the differences in anneal schedules and doping levels, the measured resistivities of the two layers are still consistent. Similarly doped p-type layers, grown under identical conditions, were also measured. These layers were implanted with $1 \times 10^{15}cm^{-3}$ B^+ after SPC and then annealed for 3 hours at 600°C, giving a doping level of approximately $10^{20}cm^{-3}$. The measured resistivity was 22mΩcm, approximately a factor of 16 times greater than the layers measured in this work. This large discrepancy can be partially attributed to the fact that the p-type layers in this work have a factor of 7 higher doping level than those used by Tsai *et al.* The remaining discrepancy could possibly by explained by a larger grain size in the layers grown in this work.

Salm *et al* [66] have grown undoped polysilicon layers in a LPCVD cluster tool at 620°C. Following deposition, the films were implanted with $5x10^{15}cm^{-2}$ As^+ or $5x10^{15}cm^{-2}$ B^+ and then furnace annealed at 950°C for 30 minutes and 5 minutes for the n-type and p-type layers respectively. Resistivity values of 30mΩcm and 10mΩcm were obtained for the Arsenic and Boron doped layers respectively. The n-type resistivity obtained in this work is 44mΩcm, which is approximately a factor of 1.5 higher than that of Salm *et al.* However from table 6.1, it can be seen that the doping level in this work is almost an order of magnitude lower. The disparity between the differences in the doping levels and the differences in the resistivities can probably be explained by differences in the growth conditions, the doping methods (in-situ doping vs ion implantation) and the annealing schedules. The layers grown in this work were deposited as amorphous films and then recrystallised into polysilicon layers, thereby giving a larger grain size than would be obtained by depositing the layer as polycrystalline silicon [96]. In contrast, Salm *et al* [66] deposited the films as a undoped polysilicon layer which was implanted and then annealed to activate the dopant. This is likely to result in a polysilicon film which has a smaller grain size than that achieved in this work. The p-type layers in this work are approximately a factor of 7 higher doped than the layers grown by Salm *et al*, again probably explaining the factor of 7.5 lower resistivity obtained in our p-type layers. The remaining discrepancy is again consistent with a larger grain size in our layers.

6.3.3 Sheet Resistivity of $PolySi_{1-x}Ge_x$ Layers

Figure 6.12 shows the measured resistivities of the n- and p-type $polySi_{1-x}Ge_x$ films deposited at temperatures in the range of 500°C to 540°C, as a function of germanium content. From figure 6.12 it can be seen that the addition of germanium to the n-type films causes a steady decrease in the resistivity, falling from a value of 44mΩcm with no Ge, to 10mΩcm with 18% Ge. For the p-type layers, the effect of Ge is different depending on the deposition temperature. For the layer deposited at 625°C, an increase in the Ge content causes a corresponding reduction in the resistivity, falling from 2mΩcm with no Ge, to 1.5mΩcm with 18% Ge. This is fully consistent with previously reported p-type polySiGe films, where it was found that the resistivity decreased with increasing Ge content [54,56,57,64]. In contrast, the layer deposited at 500°C shows the opposite trend of increasing resistivity with increasing Ge content, rising from 1.35mΩcm with no Ge to a peak value of 2.8mΩcm with 14% Ge. Increasing the germanium content to 18% causes a slight reduction

in the resistivity to 2.6mΩcm. A possible explanation for this behaviour is that the larger grain size associated with the recrystallisation of the amorphous layer (T_G = 500°C) is sufficient enough, at this high doping level, to reduce the grain boundary energy barrier such that it no longer plays a significant role in the mobility of the free carriers from one grain to another. In this case, the mobility would be limited by ionised impurity scattering [96], as is the case in single crystal silicon, causing a decrease in the mobility with increasing dopant concentration. Since the incorporation of Ge increases dopant activation, it can be seen that this would cause the mobility to reduce with increasing Ge content, thereby explaining the increase in the resistivity observed in the p-type layers deposited at 500°C in this work.

Also shown on figure 6.12, and summarised in table 6.2, are previously reported resistivities for n- and p-type polySi and polySiGe films for comparison.

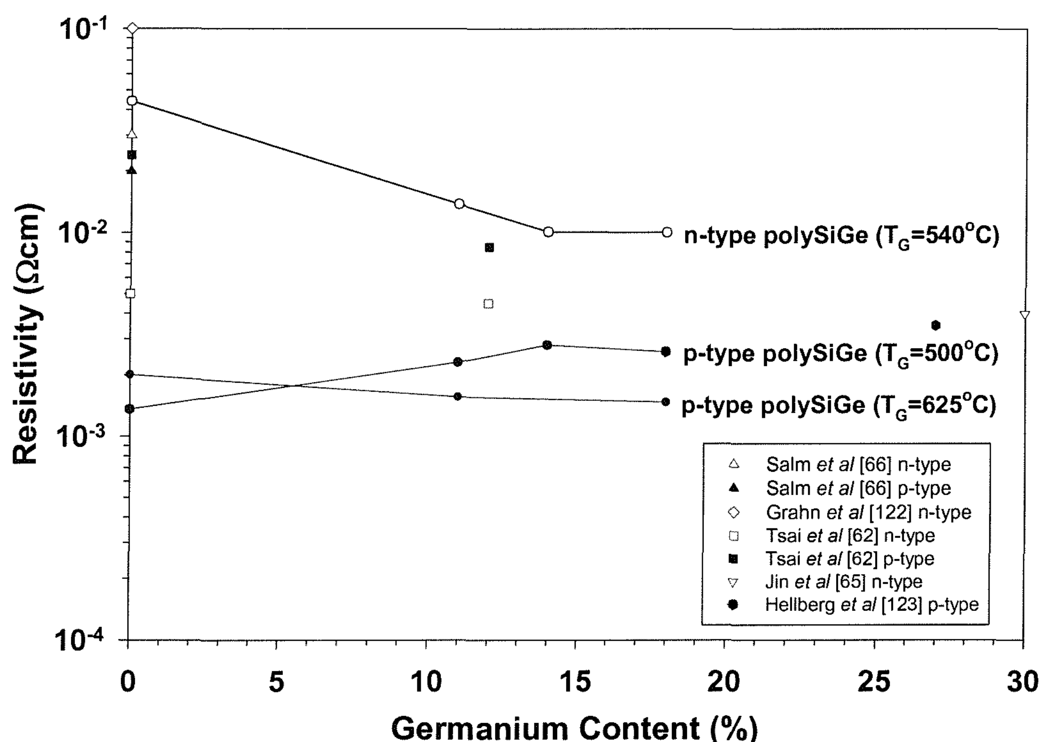


Figure 6.12: Graph of sheet resistivity of n- and p-type poly$Si_{1-x}Ge_x$ films versus germanium content. The n-type layers were deposited at 540°C and the p-type layers at either 500°C or 625°C.

From table 6.2, it can be seen that Tsai *et al* [62] have reported a resistivity value of 4mΩcm for a $Si_{0.88}Ge_{0.12}$ layer that was grown using the same deposition and

Table 6.2: Comparison of reported resistivity values for n- and p-type polySiGe.

Reference	Layer Type	Deposition Temp (°C)	Ge Content (%)	Resistivity (mΩcm)	Doping Conc. (cm^{-3})	Anneal Sched. (°C)
This work	n-type	540	18	10	4×10^{19}	1000, 30sec
Tsai [62]	n-type	600	12	4	1×10^{20}	600, 30hrs
Jin [65]	n-type	500	30	30	7×10^{19}	600, 2hrs
This work	p-type	500	18	2.6	2.1×10^{20}	1000, 30sec
This work	p-type	625	18	1.5	2.1×10^{20}	1000, 30sec
Tsai [62]	p-type	600	12	8	1×10^{20}	600, 3hrs
Hellberg [123]	p-type	500	27	5	1.4×10^{20}	900, 1hr

annealing conditions as their polysilicon layer shown in table 6.1. This compares to a resistivity value of 10mΩcm obtained in this work for a Ge concentration of 18%, a factor of 2.5 higher. The differences in resistivity values can probably be explained by the differences in the Ge content and doping level since the phosphorus doping level in the layer of Tsai *et al* is a factor of 2.5 higher than the corresponding layer in this work. The corresponding p-type layer with the same Ge content had a resistivity value of 8mΩcm, a decrease of 14mΩcm from the polysilicon case. This compares to values of 2.6mΩcm and 1.5mΩcm for the p-type $Si_{0.82}Ge_{0.18}$ layers, grown in this work at 500°C and 625°C respectively. Again the differences in resistivity values can be attributed to differences in doping level and Ge content, since the doping level and Ge content are both higher in our layers.

Jin *et al* [65] have reported a resistivity value of 30mΩcm for an n-type layer containing 30% Ge. The layer was deposited at 500°C at a pressure of 0.3 Torr and then crystallised by annealing at 550°C for 7 hours in nitrogen. Following recrystallisation, the layer was then dual implanted with P^+ at 80keV, $2 \times 10^{15}cm^{-2}$ followed by 40keV, $2 \times 10^{15}cm^{-2}$ with the same ion. and then annealed at 600°C for 2 hours to activate the dopant. The resistivity value obtained is a factor of 3 higher than that obtained in this work, even though it has a factor of 1.75 times higher doping level. However, the higher Ge content of 30% used in the layers of Jin *et al* is very close to the value of 25%, where a large reduction in phosphorus activation and a drop in Hall mobility is expected. In contrast, the much lower Ge content of 18% used in this work should not exhibit such strong dopant deactivation, and will therefore benefit from the slight increase in Hall mobility, resulting in a net decrease in resistivity. As in the case of Tsai *et al*, although the layers of Jin *et al* and this work appear comparable, the anneal schedule is significantly different, 600°C for 2 hours, as opposed to 1000°C for 30 seconds used in this work, making direct comparison difficult. However, considering the differences in Ge content and anneal temperature, the resistivity values obtained are still reasonably consistent.

Finally, Hellberg *et al* [123] have also examined the electrical properties of p-type polySiGe layers containing 27% Ge. The layers were deposited in a hot wall LPCVD reactor at 500°C at a pressure of 0.15 Torr, using silane and germane for the silicon and germanium sources respectively. Following deposition, the layers were implanted with BF_2 to a level of $1.4 \times 10^{20}cm^{-3}$ and then annealed in an Ar ambient at 900°C for 1 hour, giving a final resistivity value of approximately 5mΩcm. This compares to resistivity values of 2.6mΩcm ($T_G = 500°C$) and 1.5mΩcm ($T_G = 625°C$) obtained for the polySi$_{0.82}$Ge$_{0.18}$ layers in this work, which is 2-3 times lower than that obtained by Hellberg *et al.* The difference in resistivity values can probably be explained by the fact that the doping level in this work is a factor of 1.5 higher, thereby offsetting some of the reduction in resistivity expected with the higher Ge content used by Hellberg *et al.* In addition, the use of disilane (this work) as the silicon precursor is expected to give a larger grain size, and hence reduced resistivity, than a comparable layer grown using silane (Hellberg *et al*) [122].

In summary, values of polycrystalline Si and SiGe resistivity taken from the literature indicate that the resistivities achieved in this work are broadly comparable. Where discrepancies occur, the layers in this work tend to have a lower resistivity, suggesting a larger grain size has been achieved.

6.3.4 Sheet Resistivity of PolySi$_{1-y}$C$_y$ and PolySi$_{1-x-y}$Ge$_x$C$_y$ Layers

The resistivities of the n- and p-type polycrystalline SiC films as a function of carbon content are shown in figure 6.13. For the n-type film, it can be seen that there is a dramatic increase in the resistivity, from a value of 44mΩcm with no carbon added, to 451Ωcm for a C concentration of 0.8% . Not shown in figure 6.13 is the n-type layer grown with a C concentration of 1.7%, since no current flow was measurable for applied voltages in excess of 70V. The p-type sample shows a much less severe increase in resistivity with carbon content, with values of 1.35mΩcm and 939mΩcm for the zero and 8% cases respectively. Also shown in figure 6.13 are the resistivities of two n-type films grown with a C concentration of 0.3%, one of which was deposited in a hydrogen rich growth ambient, and the other subjected to a higher temperature anneal of 1100°C. It can be seen that depositing the n-type layer in a hydrogen rich ambient causes a decrease in the resistivity from a value of 920mΩcm to a value of 280mΩcm, approximately a factor of 3 improvement. Furthermore, annealing the sample at 1100°C leads to an even bigger decrease in the resistivity to a value

of 110mΩcm. This corresponds to over a factor of 8 reduction in the resistivity. These two results could suggest that the carbon is affecting the resistivity in the layers via interaction at the grain boundaries. It is well known that hydrogen [96] can be used to improve conduction in polysilicon films by passivating the dangling silicon bonds at the grain boundaries, thus reducing the trap density and improving conduction. In addition, raising the anneal temperature will result in a larger grain size throughout the polycrystalline layer, again improving conduction.

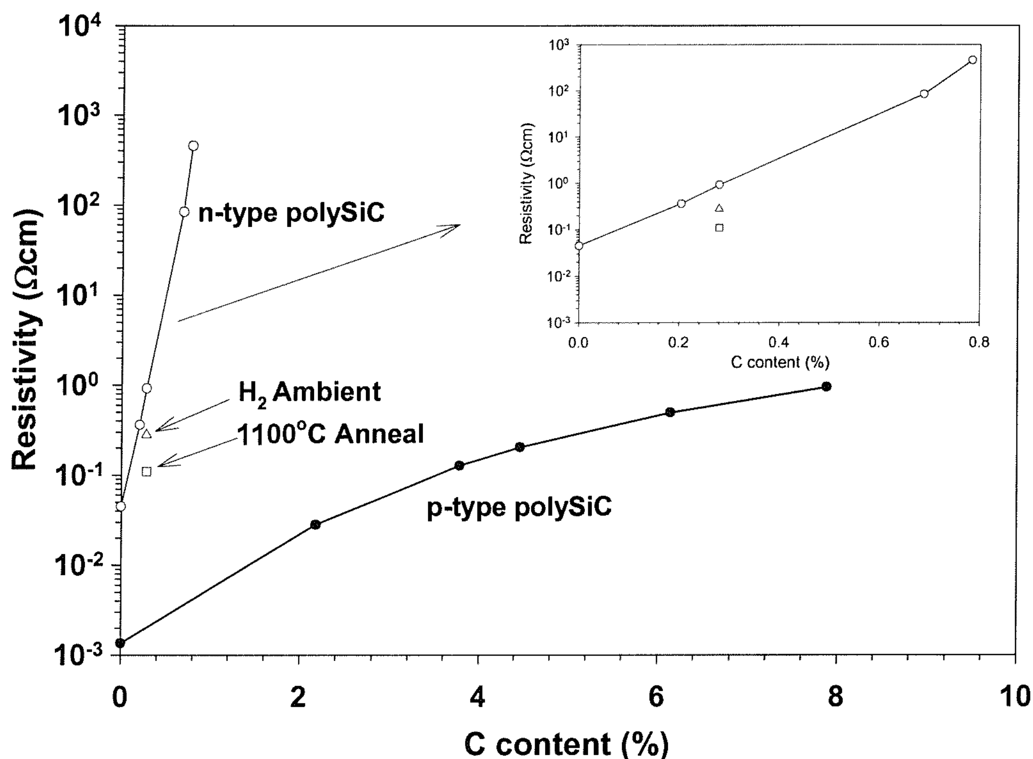


Figure 6.13: Graph of sheet resistivity of n- and p-type poly$Si_{1-y}C_y$ films versus carbon content.

The resistivities of the n- and p-type polycrystalline $Si_{1-x-y}Ge_xC_y$ films, as a function of carbon concentration are shown in figure 6.14, where it can be seen that the effect of carbon on the two sets of films is once again significantly different. The n-type sample exhibits a dramatic increase in resistivity with carbon concentration, rising from a value of 10mΩcm with no carbon added to 2.4Ωcm when 0.6% C is present. As in the SiC case, raising the carbon concentration to 1.4% resulted in a layer that was non conductive even though the layer is highly doped. In contrast, the p-type sample shows only a moderate increase in resistivity, rising from a value of 2.6mΩcm for no carbon to 14.7mΩcm for a C concentration of 4%.

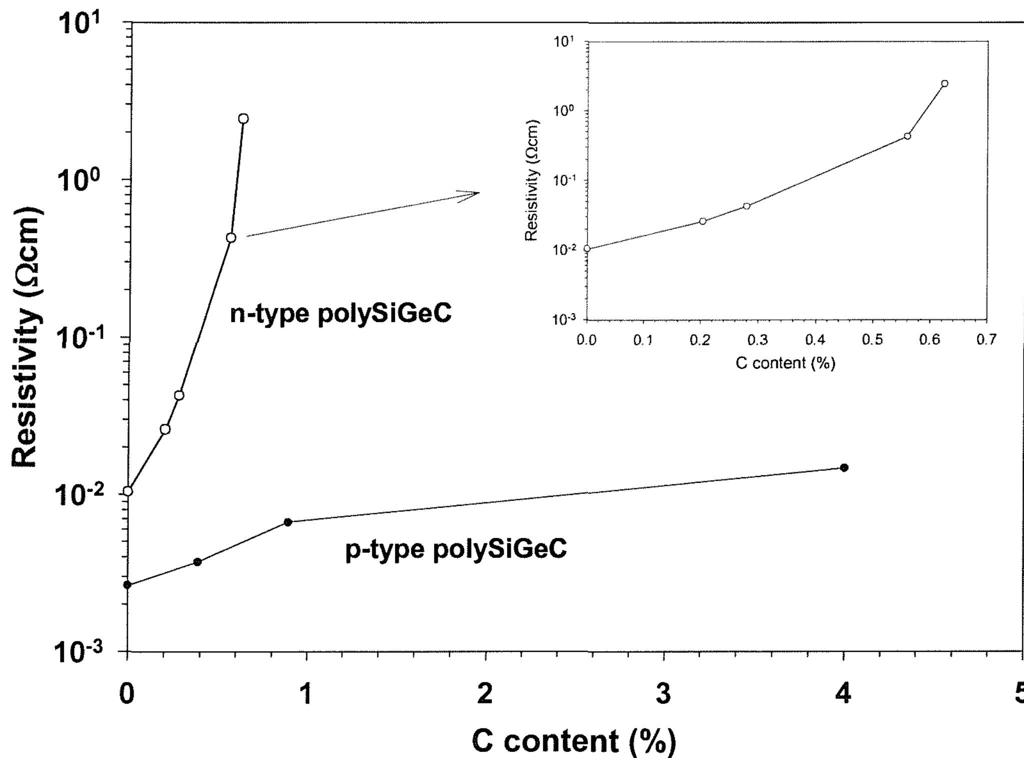


Figure 6.14: Graph of sheet resistivity of n- and p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ films versus carbon content.

6.3.5 Effect of C on the Effective Carrier Concentration

Figures 6.15 and 6.16 show plots of effective carrier concentration for the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers versus carbon content. From figure 6.15 it can be seen that the effective carrier concentration in the n-type poly$Si_{1-y}C_y$ layer decreases rapidly with C concentration, falling from a value of $7.8 \times 10^{18}cm^{-3}$ with no carbon added to $2.48 \times 10^{18}cm^{-3}$ with the addition of 0.28% C. No meaningful value was obtainable for the other n-type layers with $\geq$ 0.68%C due to their high resistivity. In contrast, for the p-type layers, the effect of C incorporation is much less severe. The effective carrier concentration is $2.8 \times 10^{20}cm^{-3}$ with no C, and falls by an order of magnitude with the addition of 8% C.

Figure 6.16 shows a similar trend in the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. The n-type layer also exhibits a dramatic decrease in effective carrier concentration with increasing carbon content, falling from a value of $2.9 \times 10^{19}cm^{-3}$ with no C, to $7.4 \times 10^{18}cm^{-3}$ with 0.56%C. As in the poly$Si_{1-y}C_y$ case, increasing the C content

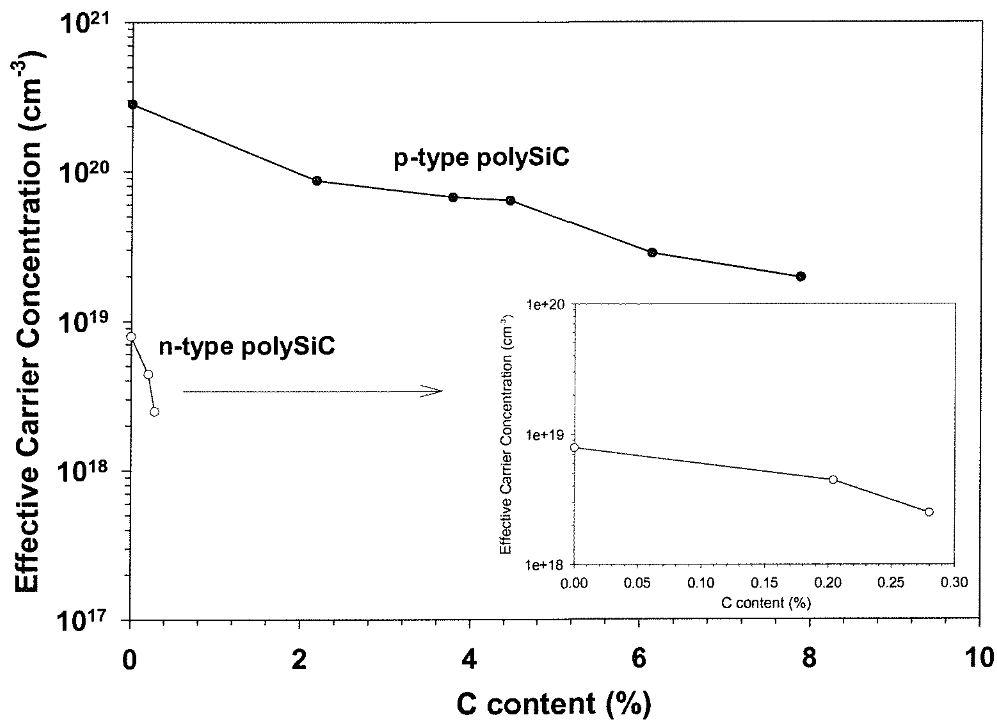


Figure 6.15: Graph of effective carrier concentration for the n- and p-type poly$Si_{1-y}C_y$ films versus carbon content.

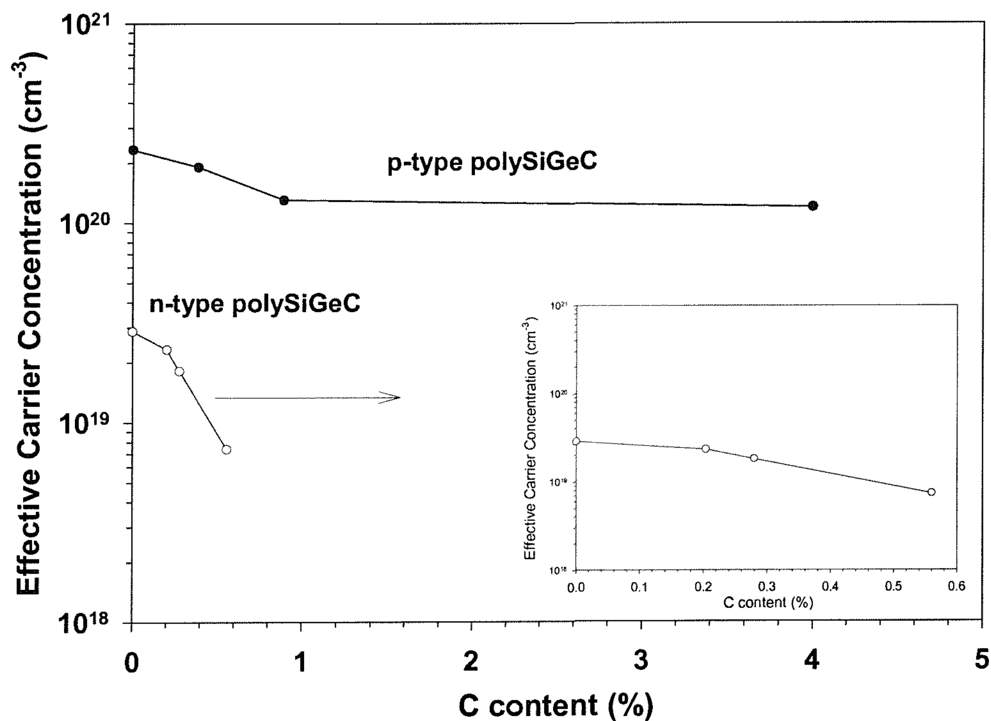
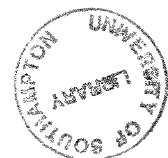


Figure 6.16: Graph of effective carrier concentration for the n- and p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ films versus carbon content.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in the n-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layer above 0.6%C resulted in a high resistivity layer thereby preventing meaningful extraction of the effective carrier concentration. It should also be noted that the trends in the effective carrier concentrations in the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers are almost identical, with only the magnitudes differing. Comparing figures 6.15 and 6.16, it can be seen that more dopant is electrically active in the n-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layers than the poly$Si_{1-y}C_y$ layers for a given C content. This could suggest that the mechanisms involved in the decreasing effective carrier concentration are identical in the two types of layers, and that the Ge incorporation counteracts the effects of carbon, thereby allowing more dopant to become electrically active.

Once again, from figure 6.16, it can be seen the effect of C on the p-type layers is much less severe than their n-type counterparts. The effective carrier concentration decreases from a value of $2.3 \times 10^{20}cm^{-3}$ with no C to a value of $1.2 \times 10^{20}cm^{-3}$ with 4%C. As for the n-type poly$Si_{0.82-y}Ge_{0.18}C_y$, the decrease in the effective carrier concentration in the p-type $Si_{0.82-y}Ge_{0.18}C_y$ layer is less severe than its poly$Si_{1-y}C_y$ counterpart, further indicating that Ge counteracts the detrimental effects of C in some way. This will be discussed in more detail in chapter 7. In addition, from figure 6.16, it can be seen that the rate of decrease in the effective carrier concentration is much higher for C contents below 0.9%, suggesting that C influences the electrical properties of p-type layers in two ways, depending on how much C is present. Again, this will be discussed in detail in chapter 7.

6.3.6 Effect of C on the Hall Mobility

Figures 6.17 and 6.18 show plots of the extracted Hall mobility for the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers respectively. From figure 6.17, it can be seen that the Hall mobility in the n-type layers dramatically decreases with C content, dropping from a value of $18cm^2/Vs$ with no carbon, to a value of $3cm^2/Vs$ with 0.3%C. As was observed for the effective carrier concentration, the n-type layers with higher C contents were too highly resistive to allow meaningful extraction of the Hall mobility. For the p-type layers, the Hall mobility drops approximately linearly with C content up to $\approx 4.5\%$C, dropping from $16.5cm^2/Vs$ to $0.5cm^2/Vs$, and then decreases much more slowly for higher C concentrations.

The poly$Si_{0.82-y}Ge_{0.18}C_y$ layers presented in figure 6.18 show a similar trend. For the n-type layers, the mobility drops from a value of $21cm^2/Vs$ with no C, to a

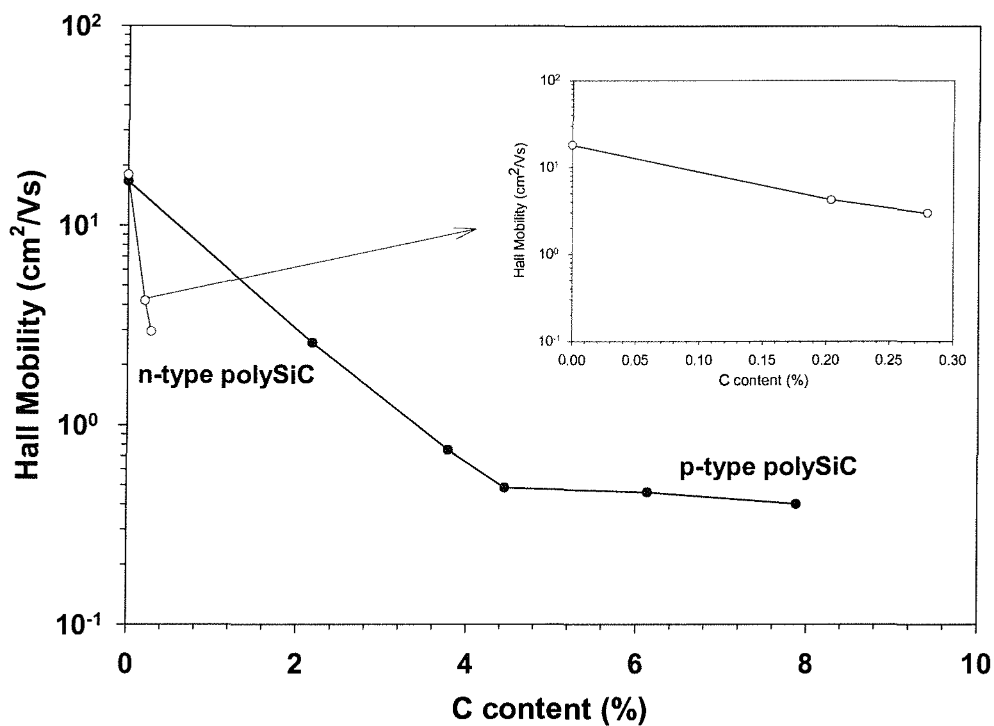

Figure 6.17: Graph of Hall mobility for the n- and p-type polySi$_{1-y}$C$_y$ films versus carbon content.

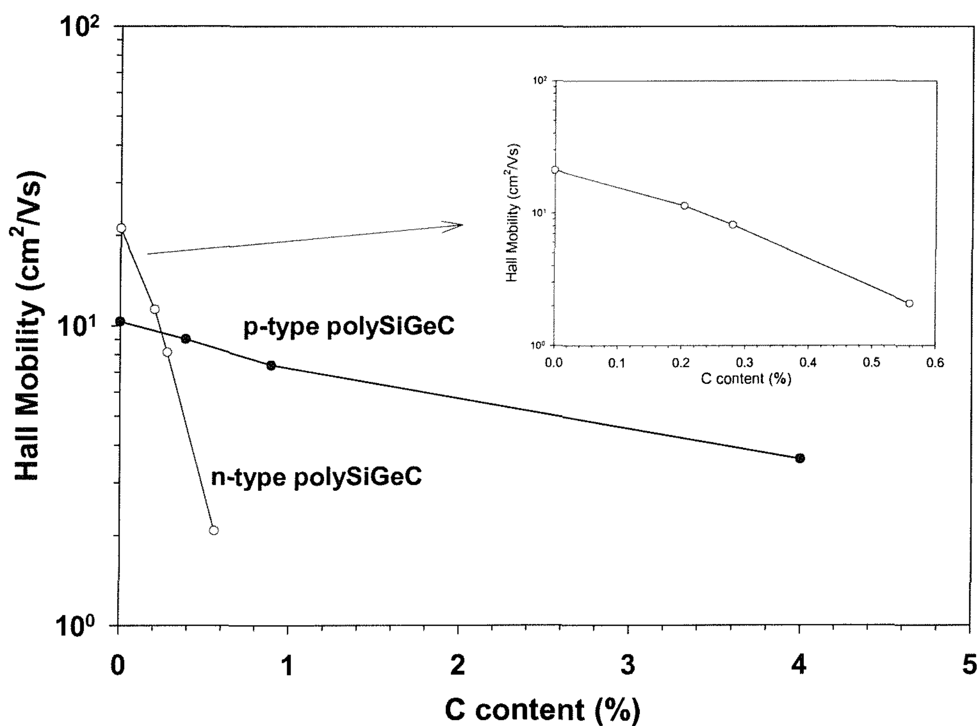

Figure 6.18: Graph of Hall mobility for the n- and p-type polySi$_{0.82-y}$Ge$_{0.18}$C$_y$ films versus carbon content.

value of 2cm^2/Vs with 0.56%C. Once again, the n-type layers containing more than 0.6%C were too highly resistive to allow meaningful extraction of the Hall mobility. In contrast, the Hall mobility decreases much more slowly with C content in the p-type layers, dropping from 10cm^2/Vs with no C, to 2cm^2/Vs with the addition of 4%C.

6.4 Conclusions

The effect of Ge content on the resistivity of in-situ doped n- and p-type polySiGe layers has been investigated. For n-type films deposited at 540°C , it has been found that the addition of up to 18% Ge causes a decrease in the resistivity, in agreement with the trend in the literature [64]. For p-type layers deposited at 625°C, it was found that the resistivity decreased with increasing Ge content. This is fully consistent with the literature, where several authors have demonstrated reduced resistivity with the addition of Ge [54, 56, 57, 64, 66]. This behaviour has been attributed to increases in both the Hall mobility and dopant activation with increasing Ge content. In contrast, the p-type layers grown at 500°C have shown a completely different trend of increasing resistivity with Ge content. A possible explanation for the behaviour of the p-type layers grown at 500°C is that the larger grain size reduces the grain boundary energy barrier sufficiently such that the mobility within the layer is now limited by dopant impurity scattering. Since the incorporation of Ge increases dopant activation, it is therefore likely that increasing the Ge content in these layers will reduce the mobility and hence increase the resistivity, therefore explaining the observed trend of increased resistivity with increasing Ge content. As in the n-type case, comparisons with previously reported p-type polySi and polySiGe layers showed that the p-type layers in this work, grown at 500°C and 625°C, had comparable resistivity values.

The electrical properties of n- and p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers as a function of C content have been investigated, with the measurement of sheet resistivity, effective carrier concentration and Hall mobility. For the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the addition of small amounts of C ($\leq$ 0.9%) severely increases the resistivity of the layers, with a corresponding drop in the effective carrier concentration and Hall mobility. Layers containing higher C concentrations were non-conductive even though highly doped. In addition, it was found that the poly$Si_{0.82-y}Ge_{0.18}C_y$ had a higher electrically active dopant level than the poly$Si_{1-y}C_y$, for a given C content, suggesting that the presence

of Ge is compensating the effects of C in some way. In contrast, for the p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the effect of C on the resistivity is much less dramatic, with the impact on the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers being small up to C concentrations of 4%. Furthermore, for the p-type poly$Si_{1-y}C_y$ layers, it was found that the Hall mobility decreases much more rapidly for C contents below 4.5%, suggesting that the influence of C on the layer is different depending on the amount of C present. A similar trend was observed in the p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ for the effective carrier concentration, where a larger reduction was observed for C contents below 0.9%. Increasing the C content to 4% resulted in only a minimal reduction, by approximately a factor of 0.92, in the effective carrier concentration. Possible explanations for the observed trends in the n- and p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers will be presented in detail in chapter 7.

Chapter 7

The role of Carbon in n- and p-type Polycrystalline $Si_{1-y}C_y$ and $Si_{1-x-y}Ge_xC_y$ layers

7.1 Introduction

In chapter 6, the effect of C on the electrical properties of n- and p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers was investigated. It was shown that for both the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ n-type layers, the addition of a small amount of C, less than 0.9%, caused a dramatic increase in the resistivity. This was associated with a corresponding drop in the effective carrier concentration and Hall mobility. For the p-type layers, the effect of C was much less severe, particularly for the poly$Si_{0.82-y}Ge_{0.18}C_y$ layer, where the addition of 4%C resulted in only a minimal increase in the resistivity. Hall effect measurements on the p-type layers showed that the decrease in effective carrier concentration and Hall mobility were significantly smaller than their n-type counterparts.

In this chapter, an explanation for the effects of carbon on the electrical properties of the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers is sought. Section 7.2 presents measurement results of the temperature dependence of the sheet resistance for the n- and p-type polySi, poly$Si_{1-x}Ge_x$, poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers grown in this work. This allows the grain boundary energy barrier to be extracted as a function of C content indicating whether C is controlling electrical conduction

via the grain boundary. Section 7.3 presents possible explanations of how C is affecting the polycrystalline layers based on the experimental results. Finally in section 7.4 some conclusions are drawn.

7.2 Extraction of Grain Boundary Energy Barriers

7.2.1 Polycrystalline Silicon Films

Figure 7.1 shows a plot of the logarithm of the normalised sheet resistance versus inverse temperature for the n-type polySi layer, in-situ doped with phosphorus to a level of $1.2 \times 10^{19}\text{cm}^{-3}$, grown in this work. Also shown on the graph is data for a polysilicon layer grown by Salm *et al* [66] which was doped by arsenic implantation to a level of $1.7 \times 10^{19}\text{cm}^{-3}$. From the graph it can be seen that the sheet resistances of the layers of Salm *et al* and this work have very similar activation energies, with values of 43meV and 46meV respectively. This close agreement between the extracted activation energies shows that the n-type polysilicon layers grown in this work are comparable with those reported in the literature. Any change in the activation energy of the resistivity in the poly$Si_{1-y}C_y$ layers can therefore be solely attributed to the influence of carbon.

Figure 7.2 shows a plot of the logarithm of the normalised sheet resistance versus reciprocal temperature for the p-type polySi layers in-situ doped with boron to a level of $7 \times 10^{20}\text{cm}^{-3}$ grown in this work. It can be seen that the resistivity varies little with temperature preventing the extraction of a meaningful activation energy. The extraction of the activation energy from the temperature dependence of the resistivity is only valid if the dominant limiting mechanism in the conduction process is the grain boundary energy barrier. Therefore, it can be seen that a boron doping level of $\approx 7 \times 10^{20}\text{cm}^{-3}$ in the p-type layer is sufficient to suppress the grain boundary energy barrier such that it no longer limits the conduction process, allowing other mechanisms, such as impurity scattering, to dominate. In this regime, the conduction process is no longer thermally activated, thereby explaining the plot shown in figure 7.2. To check whether the differences in behaviour between the n- and p-type polySi layers can be attributed to differences in doping level, the extracted activation energy from the n-type layer was corrected for the

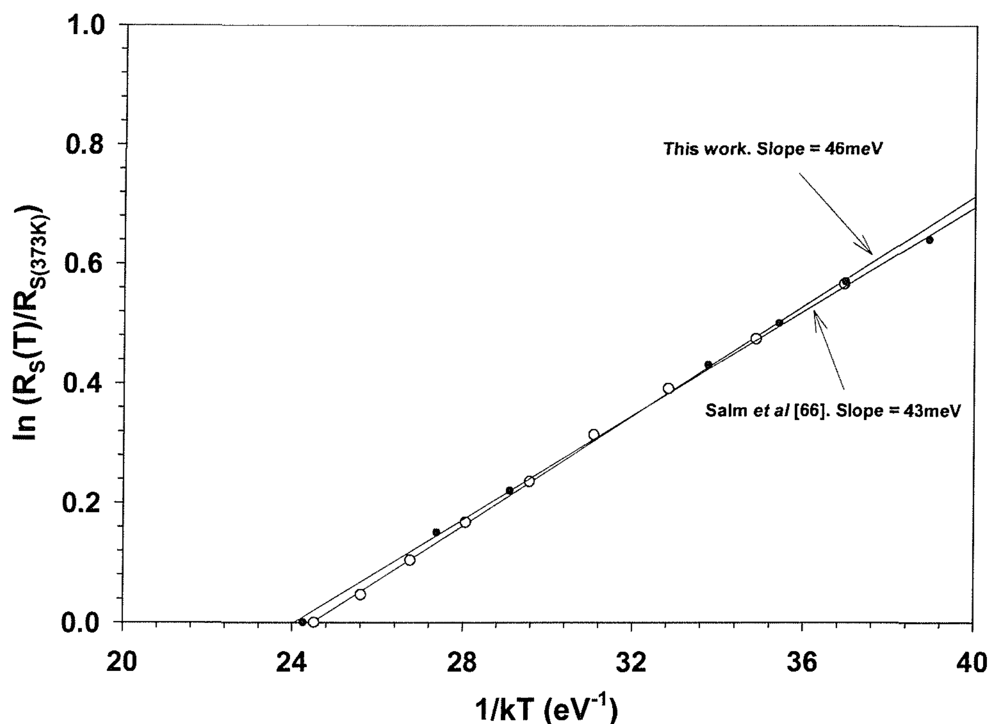

Figure 7.1: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the n-type polySi layer. Also shown for comparison is a polySi layer grown by Salm *et al* [66].

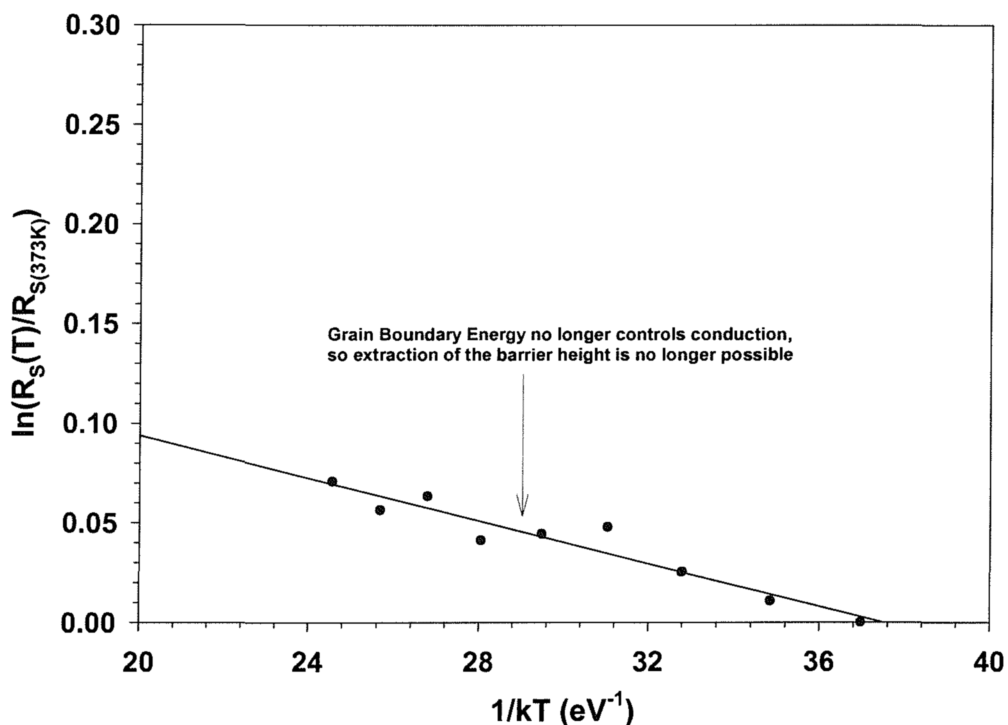

Figure 7.2: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the p-type polySi layer.

increased doping level in the p-type layer using equation 2.44, assuming an identical trap density N_T. This gave an expected energy barrier of less than 1meV. In addition, equation 2.44 assumes that the dominant trap energy is located in the middle of the energy gap. However experiments have shown that the dominant trap level is actually located at an energy of $E_C - 0.62eV$, approximately 35meV below midgap [100]. This would have the effect of making the grain boundary energy barrier even smaller for the p-type layers in this work. Therefore it can be seen that the difference in behaviour between the n- and p-type polysilicon layers is fully consistent with the higher doping concentration in the p-type layer.

7.2.2 Polycrystalline $Si_{1-x}Ge_x$ Films

Figure 7.3 shows plots of the normalised sheet resistance versus reciprocal temperature for the n-type $polySi_{0.82}Ge_{0.18}$ layer, doped to a level of $4 \times 10^{19}cm^{-3}$, grown in this work and for an n-type $polySi_{0.65}Ge_{0.35}$ layer, arsenic doped by ion implantation to a level of $1.7 \times 10^{19}cm^{-3}$, grown by Salm *et al* [66]. Also shown on the graph is

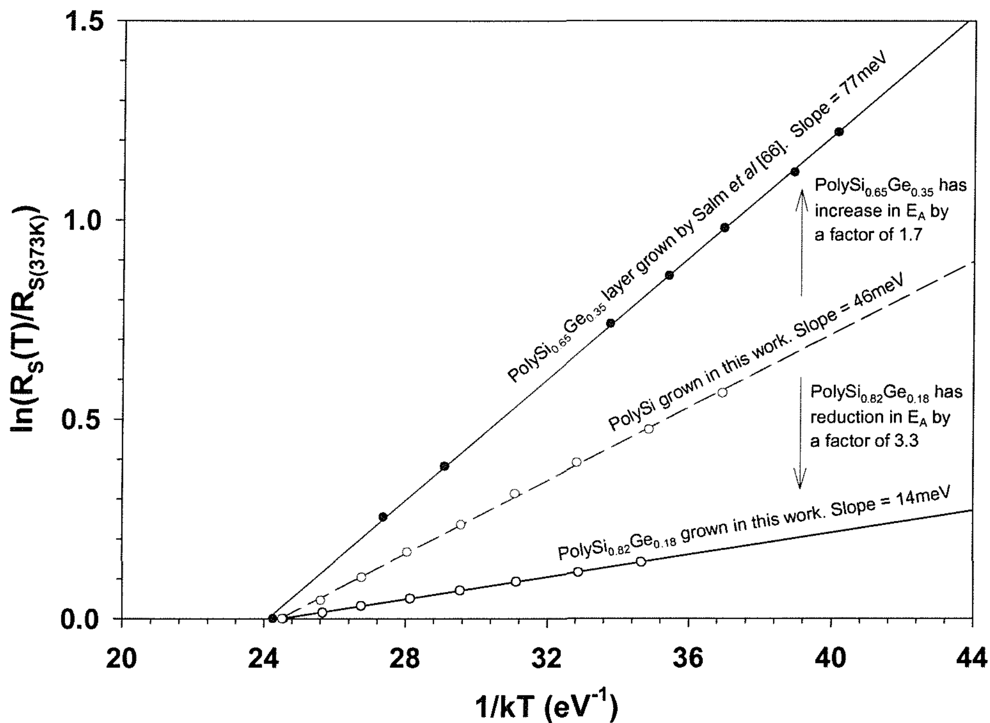

Figure 7.3: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the n-type $polySi_{0.82}Ge_{0.18}$ layer. Also shown for comparison is a $polySi_{0.65}Ge_{0.35}$ layer grown by Salm *et al* [66].

a plot of the temperature dependence of the polysilicon layer grown in this work for

Table 7.1: Comparison of extracted resistivity activation energies for the n-type polySi and $polySi_{0.82}Ge_{0.18}$ layers show the effects of the addition of Ge.

Reference	Layer Type	Doping Concentration (cm^{-3})	Activation Energy E_A (meV)	Change in E_A	Difference in in Doping Level
This work	PolySi	1.2×10^{19}	46	-	-
This work	$PolySi_{0.82}Ge_{0.18}$	4×10^{19}	14	$\div$ 3.3	$\times$ 3.3
Salm [66]	PolySi	1.7×10^{19}	43	-	-
Salm [66]	$PolySi_{0.65}Ge_{0.35}$	1.7×10^{19}	77	$\times$ 1.75	0

comparison. From the graph it can be seen that the activation energy of the layer grown in this work is significantly smaller than the activation energy of the polySiGe layer grown by Salm *et al*, with corresponding values of 14meV and 77meV respectively. In addition, comparing the activation energies of the $polySi_{1-x}Ge_x$ layers and the polySi layers grown in this work, it can be seen that the effects of adding Ge differ significantly depending on the amount incorporated. For the $polySi_{0.82}Ge_{0.18}$ layers grown in this work, the reduction in the activation energy compared with polySi can probably be attributed to differences in doping level between the polySi and $polySi_{0.82}Ge_{0.18}$ films, and not the presence of the germanium. The doping level in the $polySi_{0.82}Ge_{0.18}$ layer is approximately a factor of 3.3 higher (table 7.1) than that in the corresponding polySi layer. Using equation 2.44 to apply a correction to the activation energy of the polySi layer to account for the difference in the doping levels, a predicted activation energy of 13.8meV is obtained. This is almost identical to the extracted value of 14meV for the $polySi_{0.82}Ge_{0.18}$, showing that the reduction in the activation energy is actually due to the increased doping level and not the addition of 18% Ge.

Figure 7.4 shows plots of resistivity vs Ge content taken from the literature and this work. It should be noted that the resistivity value of the polysilicon layer grown in this work has been corrected to a doping level of $4 \times 10^{19}cm^{-3}$, equivalent to that of the $polySi_{0.82}Ge_{0.18}$ layer. From figure 7.4 it can be seen that for Ge concentrations below 25%, the addition of Ge does not significantly affect the resistivity of the layer. For example, Tsai *et al* [62] have measured the resistivities of n-type polySi and $polySi_{0.88}Ge_{0.12}$ layers and found that the resistivity only decreased from 5mΩcm with no Ge to 4.5mΩcm with the addition of 12%Ge. However for higher Ge concentrations ($x \geq 25\%$), a signficant increase in the resistivity is observed with increasing Ge content. This was attributed to increased phosphorus segregation and a decrease in the carrier mobility, showing that high Ge concentrations actually have

a detrimental effect on the electrical properties of n-type layers. These results show that the n-type layers in this work are behaving as expected, thereby allowing any differences observed in the activation energy of the polySi$_{0.82-y}$Ge$_{0.18}$C$_y$ layers to be attributed to the influence of carbon.

As in the polySi case, the activation energy of the p-type polySi$_{0.82}$Ge$_{0.18}$ layers could not be reliably extracted due to the high doping level suppressing the energy barrier such that it no longer limits conduction. Comparing with the n-type polySiGe samples, the extracted grain boundary energy barrier was 9.6meV for a doping a level of 4×10^{19}cm^{-3}. If this value is corrected for a doping level of 2.1×10^{20}cm^{-3} in the p-type layer, using equation 2.44, a grain boundary energy barrier of 1.8meV is obtained. Once again, as discussed for the polySi case, the dominant trap energy is located slightly below the midgap level ($E_C - 0.62$eV), further reducing the energy barrier in the p-type polySi$_{0.82}$Ge$_{0.18}$ layer, thereby confirming that at a doping level of 2.1×10^{20}cm^{-3} the grain boundary energy barrier is completely suppressed. This result shows that the p-type polySi$_{0.82}$Ge$_{0.18}$ layers are behaving as expected with any differences in behaviour between the n- and p-type layers being explainable by differences in their doping levels. Several authors have reported improvements in the electrical properties of p-type polySi$_{1-x}$Ge$_x$ layers [64, 66, 123] with increasing Ge content, as shown in figure 7.5. Even for layers containing less than 25% Ge, there is a significant improvement in the resistivity of p-type layers. For example, Tsai *et al* [62] have shown that the resistivity of a p-type polySi layer drops from 22mΩcm to a value of 10mΩcm with the addition of 12% Ge. This represents a factor of 2 decrease. In addition, there was no degradation in the resistivity of p-type polySi$_{1-x}$Ge$_x$ layers at high Ge concentrations as was observed for n-type layers.

7.2.3 Polycrystalline Si$_{1-y}$C$_y$ Films

Figures 7.6 and 7.7 show plots of the log of the sheet resistance versus reciprocal temperature for the n- and p-type polySi$_{1-y}$C$_y$ layers respectively, for different C contents. For the n-type layers, it can be seen that the addition of C causes a significant increase in the activation energy of the sheet resistance, from a value of 46meV with no carbon, to a value of 390meV with the addition of 0.78% C. In contrast, for the p-type layers, it can be seen that the increase in activation energy E_a with C content is much smaller, even though the C content is significantly larger. The activation energy rises from a value of 16meV with 2.2% C to 75meV with 7.9%

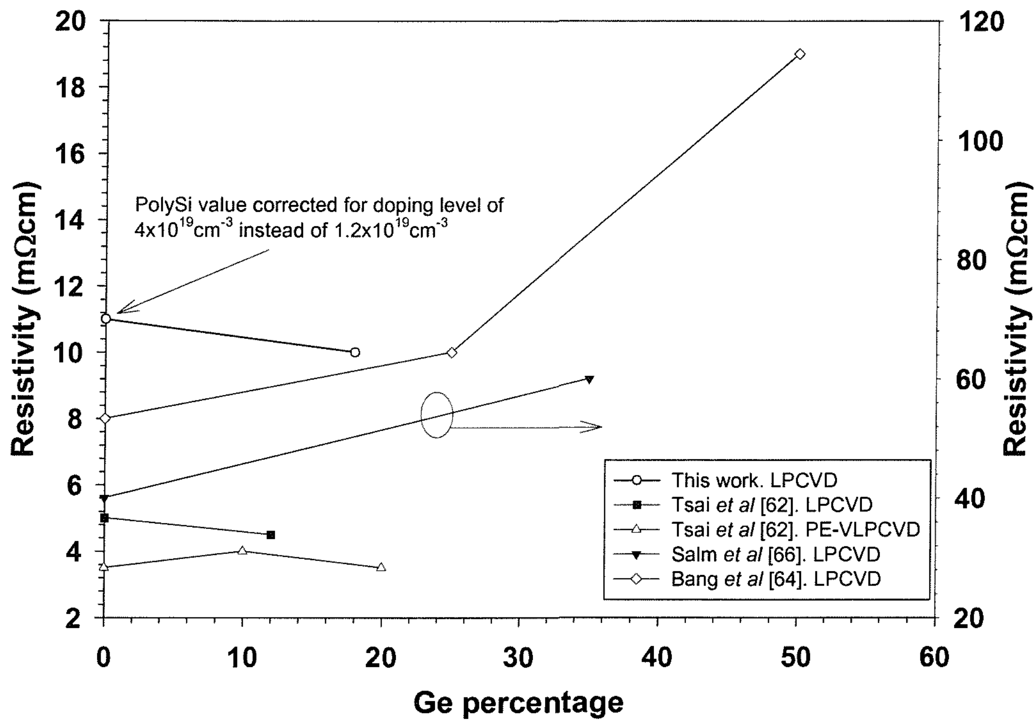

Figure 7.4: Comparison of resistivity values of n-type poly$Si_{1-x}Ge_x$ for different Ge percentages showing how the amount of Ge present significantly affects the resistivity.

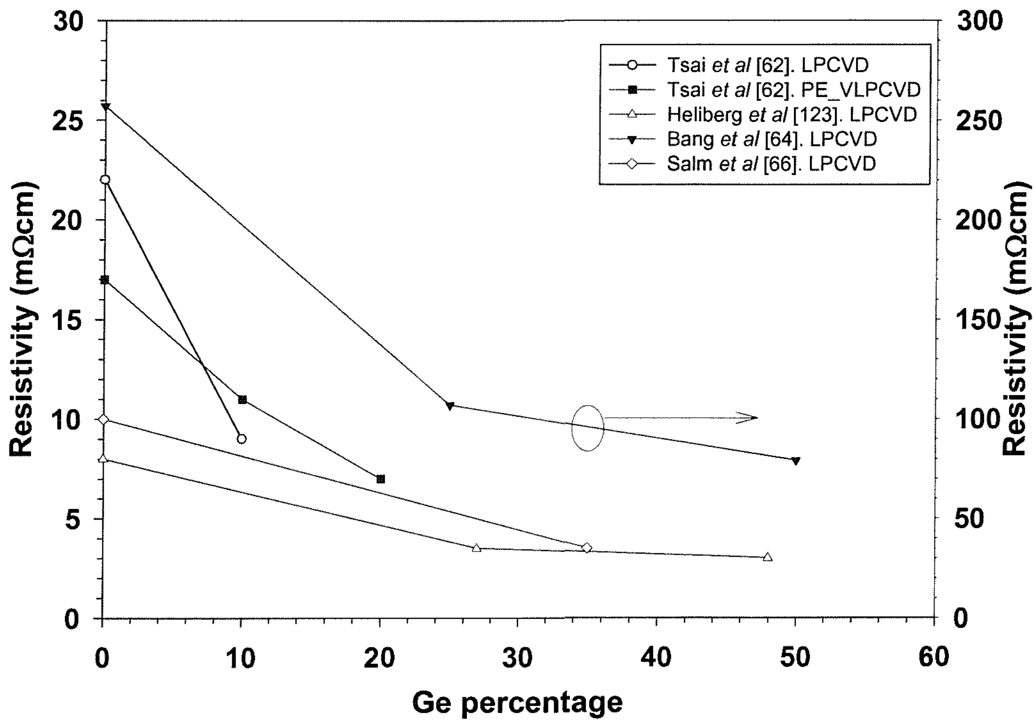

Figure 7.5: Comparison of resistivity values of p-type poly$Si_{1-x}Ge_x$ for different Ge percentages showing how the amount of Ge present affects the resistivity.

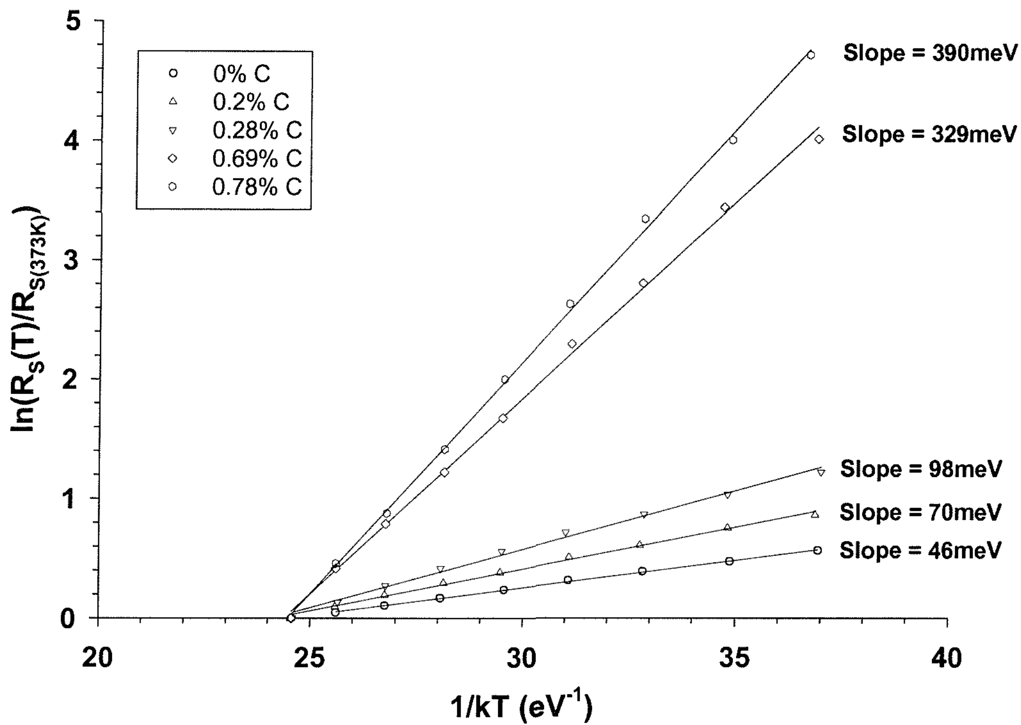

Figure 7.6: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the n-type poly$Si_{1-y}C_y$ layers.

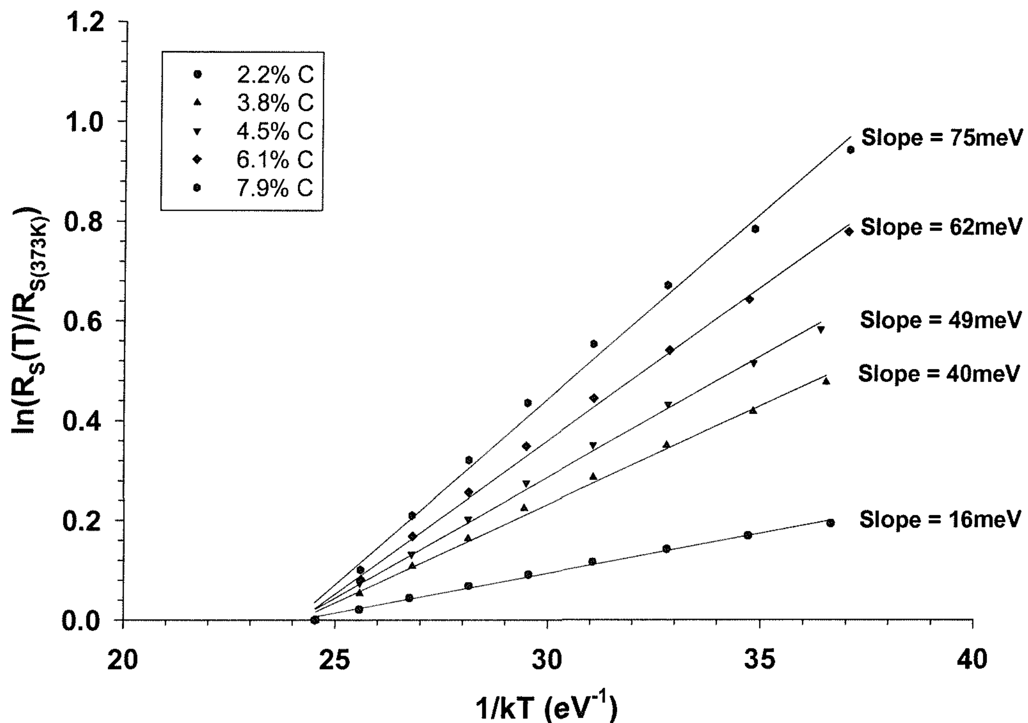

Figure 7.7: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the p-type poly$Si_{1-y}C_y$ layers.

C. As stated earlier, the activation energy for the p-type layer containing no carbon could not be extracted since the grain boundary energy barrier was too small.

Comparing figures 7.6 and 7.7, it can be seen that the relationship between the activation energy E_a and the C content for the n- and p-type layers is significantly different. The n-type layers exhibit a steady increase in E_a with carbon at low concentrations, then a dramatic increase at higher C contents. In contrast, the p-type layers exhibit a steady increase in E_a with C content at both low and high concentrations. This effect is illustrated in figures 7.8 and 7.9 which show plots of the grain boundary energy barrier at 300K, calculated by applying the correction given in equation 2.47 to the extracted activation energy, versus carbon content for the n- and p-type layers respectively. For the n-type $\mathrm{polySi_{1-y}C_y}$ layer, the grain boundary energy barrier E_B can be fitted by an empirical square law dependence of the form :

$$E_B = 4135y^2 + 0.032\ eV \tag{7.1}$$

where y is the carbon mole fraction. This empirical fit is consistent with equation 2.44 where the energy barrier is related to the square of the trap density N_T and therefore suggests that carbon is increasing the trap density at the grain boundary for the n-type layers. In contrast, for the p-type $\mathrm{polySi_{1-y}C_y}$ layers, the relationship between the grain boundary energy barrier and C content can be reasonably approximated by a simple linear equation of the form

$$E_B = 0.7y - 0.001eV \tag{7.2}$$

where once again y is the carbon mole fraction. This deviation away from the square dependence suggests that an additional mechanism needs to be considered at the high C concentrations used in the p-type layers. This will be discussed in more detail is section 7.3.

The difference in the relationship between the grain boundary energy barrier and C content seen in the n- and p-type samples is also consistent with the markedly different electrical characteristics observed for the n- and p-type layers. From equations

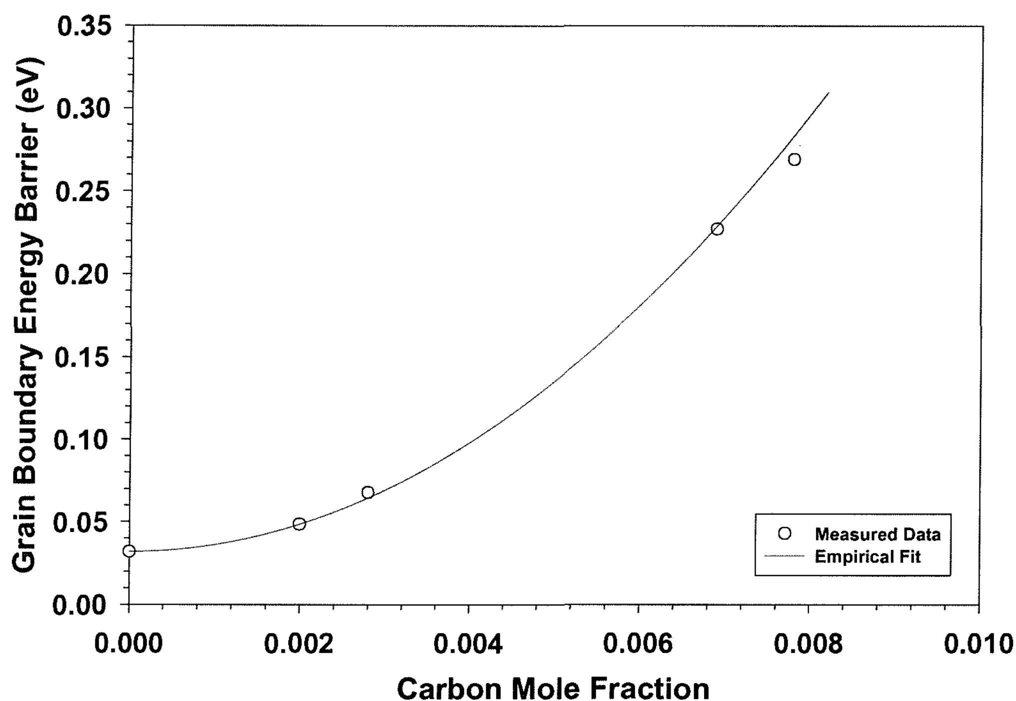

Figure 7.8: Plot of the grain boundary energy barrier versus C content for the n-type poly$Si_{1-y}C_y$ layers.

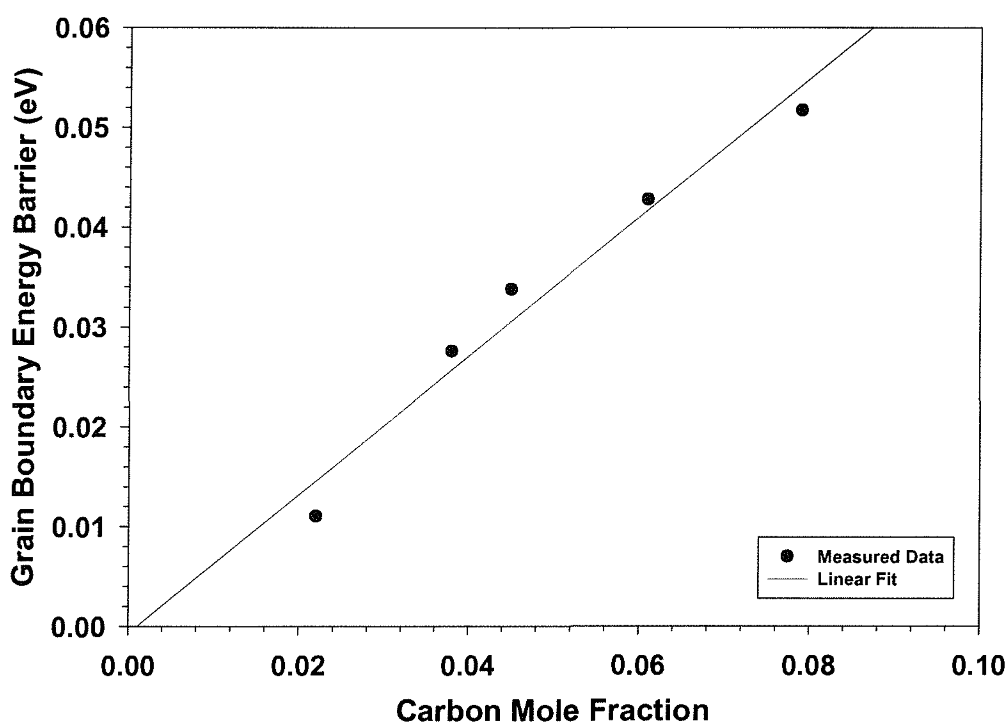

Figure 7.9: Plot of the grain boundary energy barrier versus C content for the p-type poly$Si_{1-y}C_y$ layers.

2.46 and 2.50, it can be seen that the strong dependence of the energy barrier on C content in the n-type layers will cause both a dramatic increase in the resistivity and a corresponding decrease in the mobility. However, for the p-type layers the much weaker dependence of the grain boundary energy barrier on C content results in a significantly smaller detrimental effect on the resistivity and Hall mobility, even at much higher C concentrations. This will be discussed in more detail in section 7.3.

7.2.4 Polycrystalline $Si_{0.82-y}Ge_{0.18}C_y$ Films

Figures 7.10 and 7.11 show plots of the log of the sheet resistance for the n- and p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layers respectively. For the n-type layers, it can be seen that a similar trend to that observed for the poly$Si_{1-y}C_y$ is evident, with the activation energy rising from a value of 14meV with no C added to 114meV with the addition of 0.62% C. For the p-type layers, it can be seen that the resistivity activation energy could only be extracted for the layer containing 4% C, indicating that for the other layers the resistivity is not thermally activated and hence not limited by the grain boundary energy barrier. Even at this high C content, the extracted activation energy is only 5meV, compared to a value of 45meV for the poly$Si_{1-y}C_y$ layer with a similar C content and a factor of 3.3 higher doping level.

Figure 7.12 shows a plot of the grain boundary energy barrier at 300K, calculated by applying the correction to the extracted activation energy as before, versus C content. From figure 7.12 it can be seen that the grain boundary energy barrier can be empirically fitted by a square law relationship of the form:

$$E_B = 1550y^2 + 0.01\ eV \tag{7.3}$$

Also shown on figure 7.12 is the measured data for the n-type poly$Si_{1-y}C_y$ layer and a plot of the corrected data compensating for the differences in doping level. From figure 7.12 it can be seen that the corrected data for the n-type poly$Si_{1-y}C_y$ layers almost coincides with the measured data for the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, showing that the C is having the same effect on both layers, with any discrepancies between the measured energy barriers being directly attributable to differences in the doping levels. Furthermore, this result shows that Ge in the n-type poly$Si_{0.82-y}Ge_{0.18}C_y$

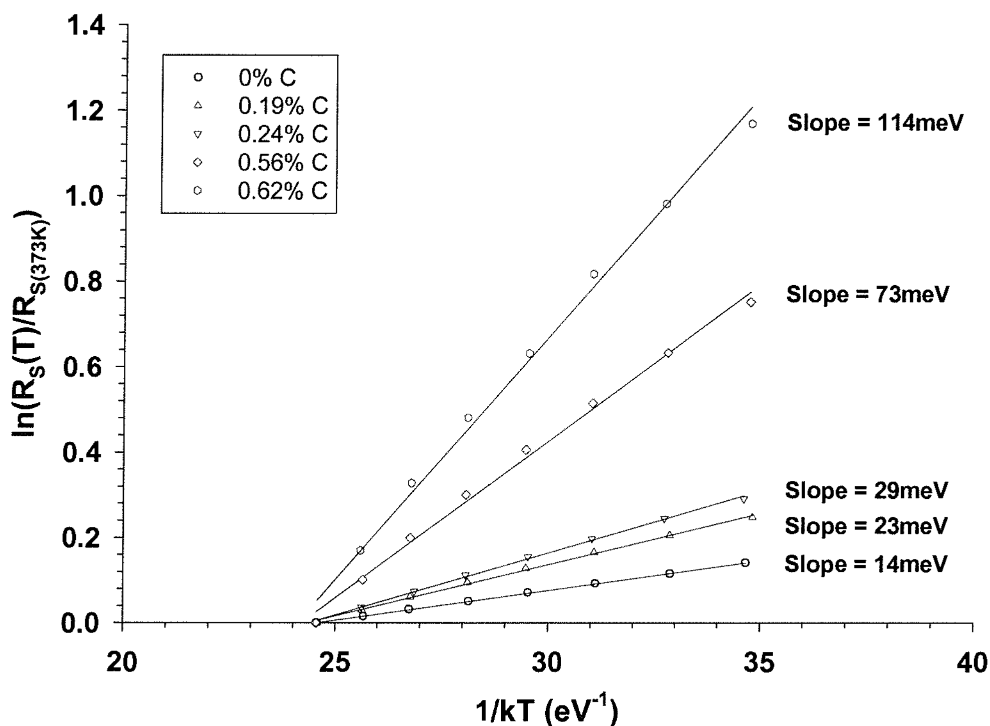

Figure 7.10: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the n-type polySi$_{0.82-y}$Ge$_{0.18}$C$_y$ layers.

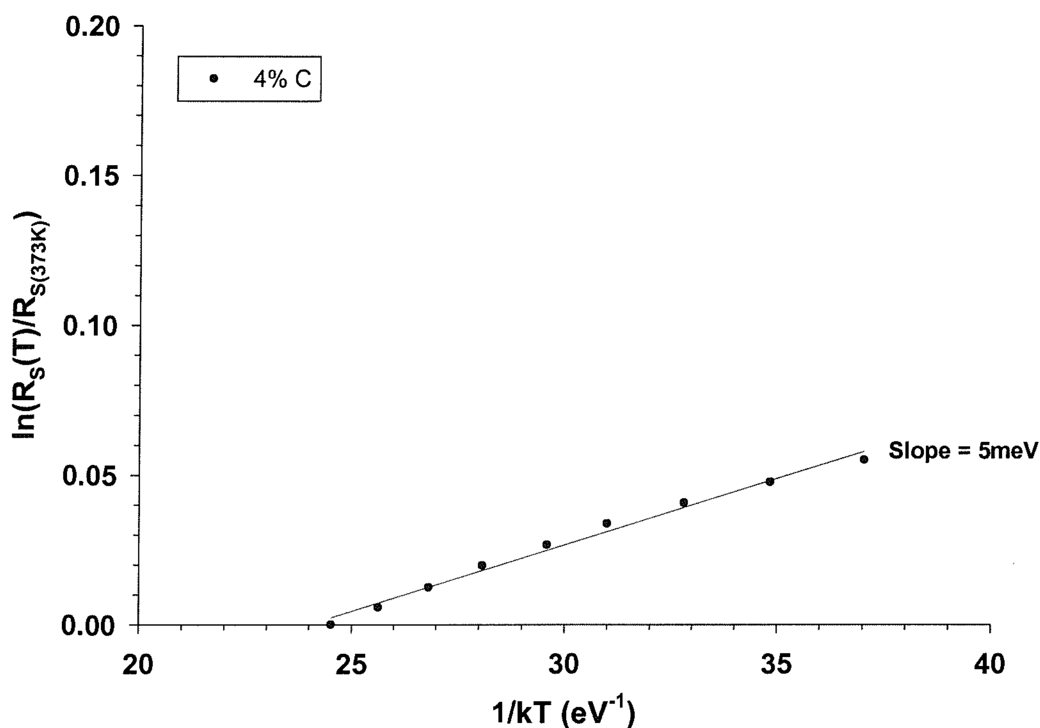

Figure 7.11: Logarithm of the normalised sheet resistance as a function of reciprocal temperature for the p-type polySi$_{0.82-y}$Ge$_{0.18}$C$_y$ layers.

layers has a negligible effect on the resistivity of the layer. In contrast, for the p-type layers, the extracted activation energy of 5meV is a factor of 9 lower than the corresponding activation energy of the $polySi_{1-y}C_y$ layer with a similar C content, even though it has a factor of 3.5 lower boron doping level. This lower doping level would be expected to give an increase in the activation energy and therefore indicates that for p-type layers, the incorporation of 18% Ge has a counteracting influence on the effects of carbon. This will be discussed in more detail in the next section.

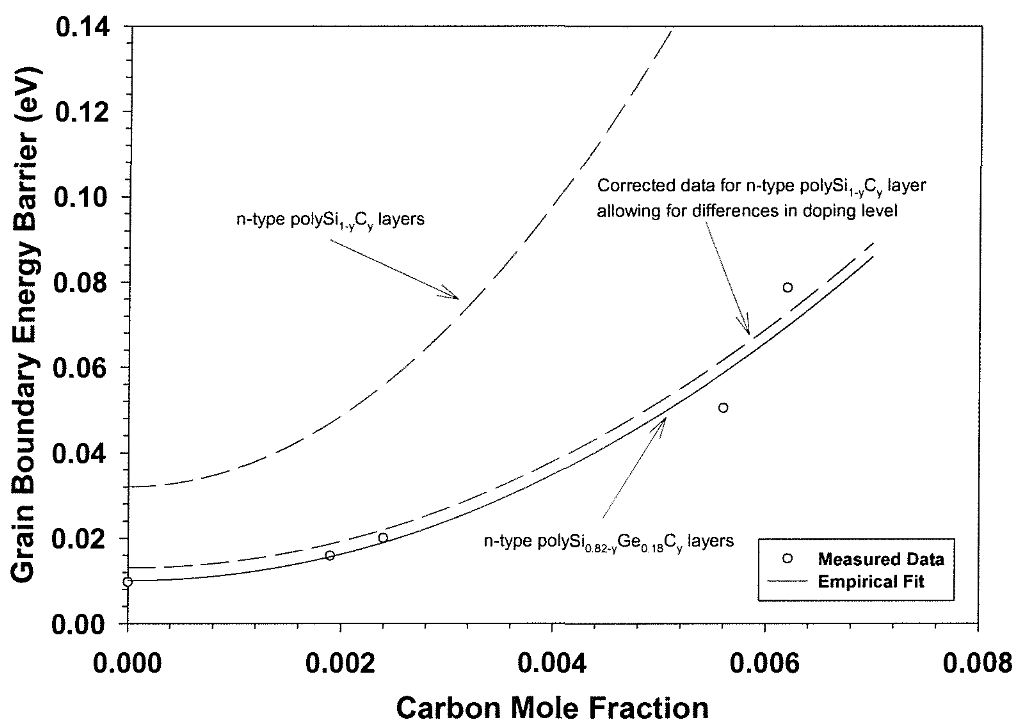

Figure 7.12: Plot of the grain boundary energy barrier versus C content for the n-type $polySi_{0.82-y}Ge_{0.18}C_y$ layers. Also shown is the empirical fit for the $polySi_{1-y}C_y$ layers for comparison.

7.3 Discussion

7.3.1 Effects of C on resistivity and the grain boundary

In chapter 6 it was shown that for n-type $polySi_{1-y}$ and $polySi_{0.82-y}Ge_{0.18}C_y$ layers the addition of a small amount of carbon gave rise to a dramatic increase in the resistivity, with the former being much more severe. This increase in the resistivity

was associated with a corresponding drop in the Hall mobility and effective carrier concentration. In order to ascertain whether the carbon was affecting the layers via the grain boundary, the temperature dependence of the resistivity was measured to allow the extraction of the grain boundary energy barrier. This showed that for both the poly$Si_{1-y}C_y$ and the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the grain boundary energy barrier was related to the square of the carbon content. From equation 2.44, it can be seen that this square law dependence is fully consistent with carbon increasing the trap density at the grain boundary, hence trapping more free carriers and explaining the increase in resistivity. In addition, when the grain boundary energy barriers of the poly$Si_{1-y}C_y$ layers were corrected for a doping level of $4 \times 10^{19}cm^{-3}$, it was found that the expected energy barriers were almost identical to those obtained for the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. This result suggests that for n-type layers the addition of 18% Ge does not have any significant effect on the electrical properties of the layer

In contrast, for the p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the increase in the resistivity was much less severe. Extraction of the grain boundary energy barriers for the poly$Si_{1-y}C_y$ layers showed that relationship between the grain boundary energy barrier and carbon content could not be described by a square law dependence. This means that the increase in the grain boundary energy barrier cannot be attributed to an increase in the trap density alone and that some other mechanism must be involved. The difference in the dependence on the energy barrier on C content between the n-type and p-type poly$Si_{1-y}C_y$ layers explains the markedly different behaviours of the resistivity.

For the p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ case, an additional effect is observed. The grain boundary energy barrier could only be extracted for the layer containing 4% C, with a value of 3.5meV, indicating that for the lower concentrations no energy barrier exists and that conduction is limited by other mechanisms such as ionised impurity scattering. This value compares to a grain boundary energy barrier of 31meV for the poly$Si_{0.955}C_{0.045}$ layer with a similar C content, almost a factor of 9 lower, even though the poly$Si_{0.955}C_{0.045}$ layer is much higher doped ($\times 3.3$). Correcting for this difference in doping gives an expected grain boundary energy barrier in the poly$Si_{0.78}Ge_{0.18}C_0$.04 layer of 149meV. Clearly this indicates that in the p-type layers, the presence of 18% Ge is counteracting the influence of the C in some way. This will be discussed in section 7.3.3.

7.3.2 Trap Density and Energy Effects

Figures 7.13 and 7.14 show plots of the grain boundary trap density, as a function of carbon content, for the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers respectively. The trap density was calculated by rearranging equation 2.44 to give:

$$N_T = \sqrt{\frac{8\epsilon N}{q^2} E_B} \tag{7.4}$$

where E_B is the grain boundary energy barrier, measured from the temperature dependence of the resistivity, and the other symbols have their usual meaning. For the poly$Si_{1-y}C_y$ layers (figure 7.13) it can be seen that the relationship between the grain boundary trap density and the carbon concentration can be reasonably approximated by a simple linear equation of the form:

$$N_{T(Si_{1-y}C_y)} = 1.16 \times 10^{16} y + 3.73 \times 10^{13}\ cm^{-2} \tag{7.5}$$

where y is the carbon mole fraction. Similarly, from figure 7.14, the grain boundary trap density of the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers is given by

$$N_{T(Si_{0.82-y}Ge_{0.18}C_y)} = 1.35 \times 10^{16} y + 3.72 \times 10^{13}\ cm^{-2} \tag{7.6}$$

Comparing equations 7.5 and 7.6 it can be seen that the linear fits for the two types of layers are very similar. This close correlation indicates that the addition of 18% Ge in the n-type layers leaves the grain boundary trap density largely unaffected, further explaining the results shown in figure 7.12. In addition, the reasonably good fit of the straight line approximation to both sets of experimental data confirms the assumption that for these low carbon concentrations, equation 2.44 is still valid. Furthermore this implies that at low carbon concentrations the effect of carbon is to increase the trap density without significantly affecting the grain boundary trap energy level.

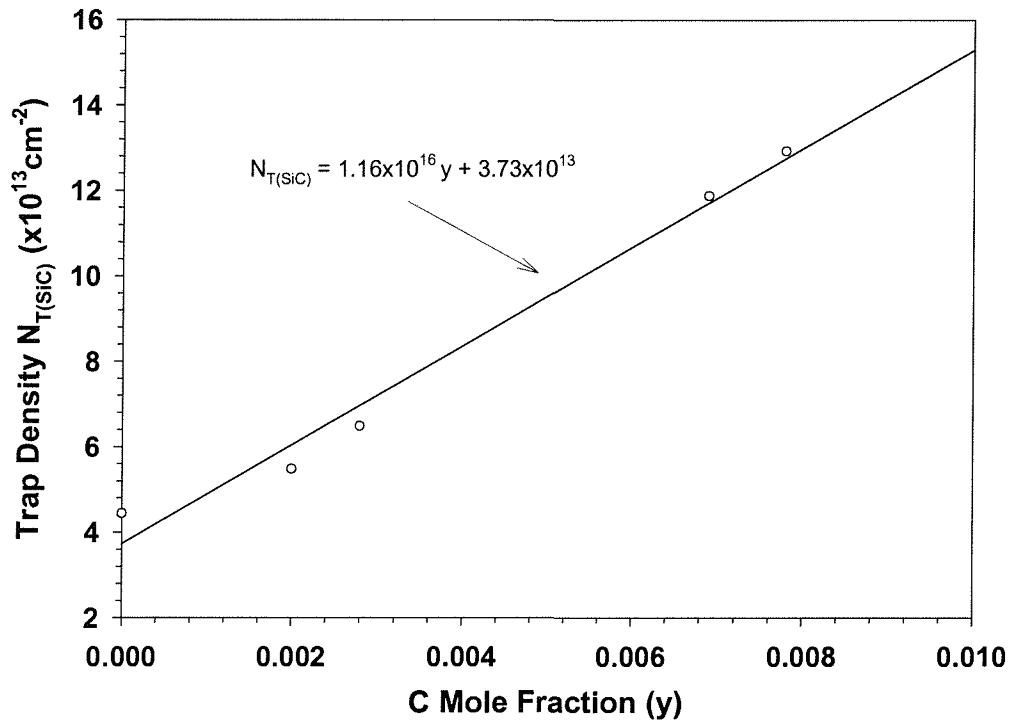

Figure 7.13: Plot of the trap density N_T versus C content for the n-type polySi$_{1-y}$C$_y$ layers, calculated using equation 2.44.

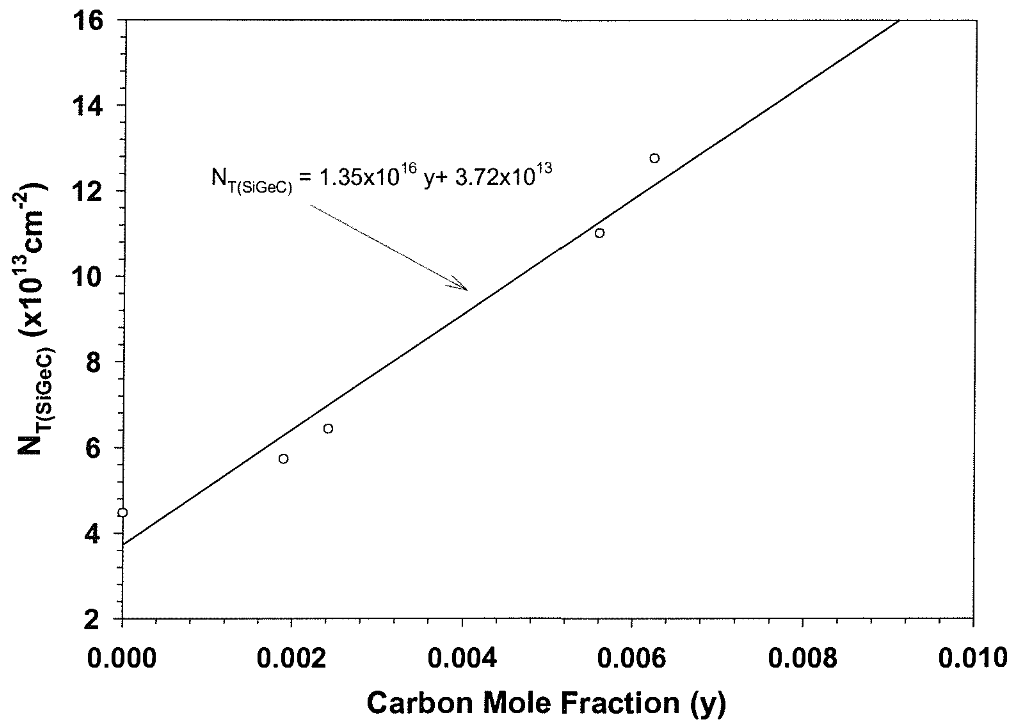

Figure 7.14: Plot of the trap density N_T versus C content for the n-type polySi$_{0.82-y}$Ge$_{0.18}$C$_y$ layers, calculated using equation 2.44.

Table 7.2: Summary of the predicted (from equation 2.44) and measured grain boundary energy barriers in the p-type poly$Si_{1-y}C_y$ layers. The predicted values were calculated assuming the barrier is solely determined by the grain boundary trap density.

Carbon Content (at.%)	Trap Density ($\times 10^{14}cm^{-2}$)	Predicted E_B (meV)	Measured E_B (meV)
0	0.373	0	0
2.2	2.93	24	11
3.8	4.78	63	28
4.5	5.59	86	34
6.1	7.45	153	43
7.9	9.54	251	52

To examine whether the p-type poly$Si_{1-y}C_y$ layers containing low C concentrations behave in the same way as their n-type counterparts, at equivalent doping concentrations, the measured grain boundary energy barriers for the n-type layers have been corrected, using equation 2.44, for a doping concentration of $7 \times 10^{20}cm^{-3}$. The results are shown in the inset of figure 7.15. From this comparison, it can be seen that the linear fit obtained for the p-type layers and the corrected n-type data are in close agreement, suggesting that at these low C concentrations ($\leq 1\%$), the effect of C on the p-type layers will be to increase the grain boundary trap density without affecting the dominant trap energy. Therefore, for C concentrations up to 1%, it can be expected that both the n- and p-type poly$Si_{1-y}C_y$ layers will demonstrate a similar electrical dependence on C content

To investigate whether this assumption is also valid for the higher carbon concentrations found in the p-type poly$Si_{1-y}C_y$ layers, the grain boundary energy barriers have been calculated, assuming that the barrier height is determined solely by the grain boundary trap density (equations 7.5 and 2.44), and then compared to the values obtained from the temperature dependence measurements. The results of these calculations are shown in figure 7.15 and are also summarised in table 7.2. From figure 7.15 it can be seen that the predicted and measured grain boundary energy barriers are significantly different for the higher C concentrations found in the p-type layers. The predicted value of 251meV, for the p-type layer containing $\approx 8\%$ C, is nearly 200meV greater than the measured value of 52meV, which represents an overestimation by a factor of 5. This result clearly shows that for high C concentrations, equation 2.44, which assumes a dominant trap energy level close to the middle of the energy gap, is no longer valid. Furthermore, figure 7.15 shows

that the effect of high carbon concentrations on the p-type layers cannot be solely explained by an increase in the grain boundary trap density, and that some other mechanism must be involved.

An extension to the simple carrier trapping model has been made by Baccarani *et al* [95], given in section 2.9, to consider the effects of the trap energy levels on the grain boundary energy barrier. If the effect of increasing the density of the traps (N_T) per unit area, located at a discrete energy level E_T is considered, the equation for charge neutrality in the grain becomes [95] :

$$2Nx_d = \frac{N_T}{1 + \frac{1}{2}exp\left[\frac{E_T+E_B-E_F}{kT}\right]} \tag{7.7}$$

As in the simple model, there is a critical dopant concentration N^* below which the grain is fully depleted. This is found by substituting equation 2.40 into equation 7.7 and putting $x_d = L/2$ i.e. half the grain size. This gives N^* as:

$$N^* = \frac{8\epsilon}{q^2L^2}\left[E_F - E_T + kTln\left[2\frac{N_T}{N^*L} - 2\right]\right] \tag{7.8}$$

which is solved iteratively. For highly doped layers, such as in this work, where $N \geq N^*$ the energy barrier E_B is given by [95]:

$$E_B = E_F - E_T + kTln\left[\frac{2qN_T}{\sqrt{(8\epsilon N E_B)}} - 2\right] \tag{7.9}$$

which can again be solved iteratively for a given N_T, E_T and N. However for the p-type layers in this work, since the grain boundary energy barrier has been measured, equation 7.9 can be used in conjunction with equation 7.5 to give values of $E_F - E_T$ as a function of C content. Figure 7.16 shows a plot of the calculated shift in $E_F - E_T$ for the p-type polySi$_{1-y}$C$_y$ layers relative to the polySi layer without C incorporation. This clearly shows that the resistivity results in the p-type polySi$_{1-y}$C$_y$ layers could be explained if high concentrations of carbon affected not

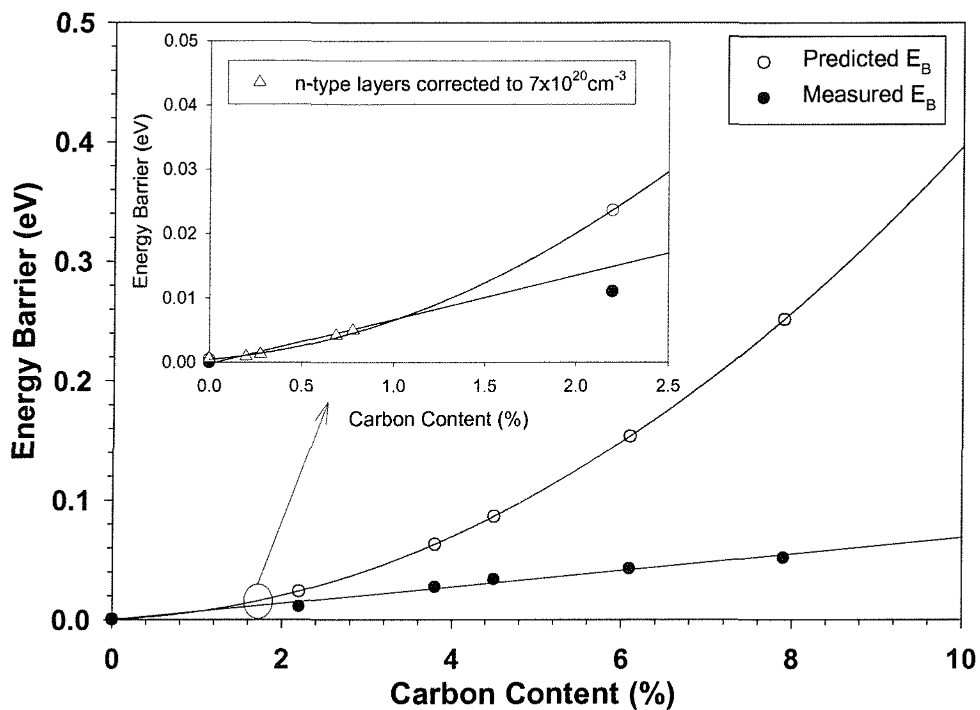

Figure 7.15: Comparison between the predicted and measured E_B for the p-type polySi$_{1-y}$C$_y$ layers. The predicted energy barriers were calculated using the trap density/C content relationship in the n-type layers. In the calculations it is assumed that the energy barrier is solely determined by the grain boundary trap density.

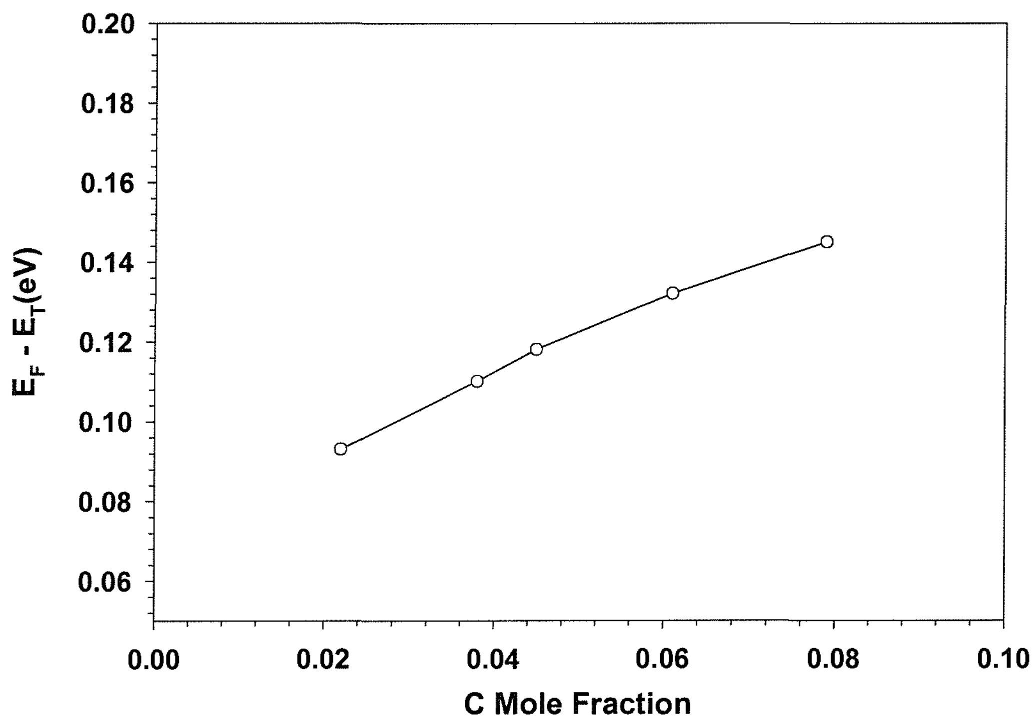

Figure 7.16: Graph of $E_F - E_T$ versus carbon content for the p-type polySi$_{1-y}$C$_y$ layers, showing how the trap energy level shifts away from the grain boundary Fermi level towards the valence band.

only the grain boundary trap density, but also shifted the trap energy level towards the valence band. Support for this hypothesis can be found in the work of Londos [119] who showed, by deep level transient spectroscopy, that interstitial carbon introduces a deep level donor defect into the bandgap (E_V + 0.28eV) of single-crystal silicon. It is therefore likely that carbon trapped at the grain boundaries could introduce such a defect level in the energy gap. At low carbon concentrations, such as in the n-type layers, the results are consistent with equation 2.44, indicating that the addition of low concentrations of carbon gives rise to an increase in the grain boundary trap density, and hence a corresponding increase in the energy barrier. This is highlighted by the square law dependence of the grain boundary energy barrier on C concentration in the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. However, at these low C concentrations, there is no evidence that the carbon significantly influences the dominant trap energy level. Since the dominant trap energy is largely unaffected at these low C concentrations, it is likely that p-type layers containing similar low C contents would also exhibit an increase in the grain boundary energy barrier according to equation 2.44. This is shown schematically in figure 7.17(a). However, as more carbon is added, the number of traps located at or near E_V + 0.28eV increases and begins to influence the dominant trap energy in the grain boundary, shifting it towards the valence band (figure 7.17(b)). At these C levels, the grain boundary energy barrier is no longer determined by the trap density alone, but also by the position of the trap energy E_T with respect to the grain boundary Fermi level. For p-type layers in this work, the shift in the dominant trap energy towards the valence band would reduce the grain boundary energy barrier, thereby compensating the increase in E_B associated with the increase in N_T introduced by C. This would explain the large difference between the predicted and measured grain boundary energy barriers shown in figure 7.15. In contrast, it can be expected that for n-type layers with high C contents, the shift in E_T would increase the energy barrier and therefore add to the increase associated with the increased defect density.

Other mechanisms that may also influence the resistivity are carbon precipitation and carbon located in the grains (substitutional and interstitial). However, for C precipitation to explain the different behaviour in the n- and p-type $Si_{1-y}C_y$ and $Si_{0.82-y}Ge_{0.18}C_y$ layers it would be necessary for the precipitates to be doping dependent, with higher precipitation evident in the presence of n-type doping. To our knowledge there is no evidence in the literature for this effect. The effect of substitutional carbon located in the crystalline grains would be to influence the mobility due to alloy scattering. However, this should be a small effect and would be expected to be worse in the high C content p-type layers than in their low C

content n-type counterparts. Bandgap measurements should allow the assessment of the amount of substitutional C in the layers, showing whether this is a significant effect.

This behaviour is analogous to the differences in behaviour seen in n- and p-type $\text{polySi}_{1-x}\text{Ge}_x$ layers ($x \geq 0.25$), where it has been shown that the addition of Ge causes a significant increase in resistivity of n-type layers, and a corresponding decrease in p-type layers [64, 66]. In polySi, the dominant trap energy is close to the middle of the bandgap, so that the effects of the carrier trapping are similar in both n- and p-type layers. In polyGe, the dominant trap energy is strongly p-type, so that grain boundary energy barriers only appear in n-type material [96]. It is therefore believed [66], that the addition of Ge to form $\text{polySi}_{1-x}\text{Ge}_x$ causes a progressive shift in the dominant trap energy towards the valence band. At high Ge concentrations ($x \geq 0.25$) the shift in trap energy will result in a lowering of the potential barrier for p-type layers and an increase for n-type, thereby explaining the corresponding decrease and increase in the resistivities of the layers. This is very similar to the behaviour exhibited by the carbon containing layers further strengthening the hypothesis presented above.

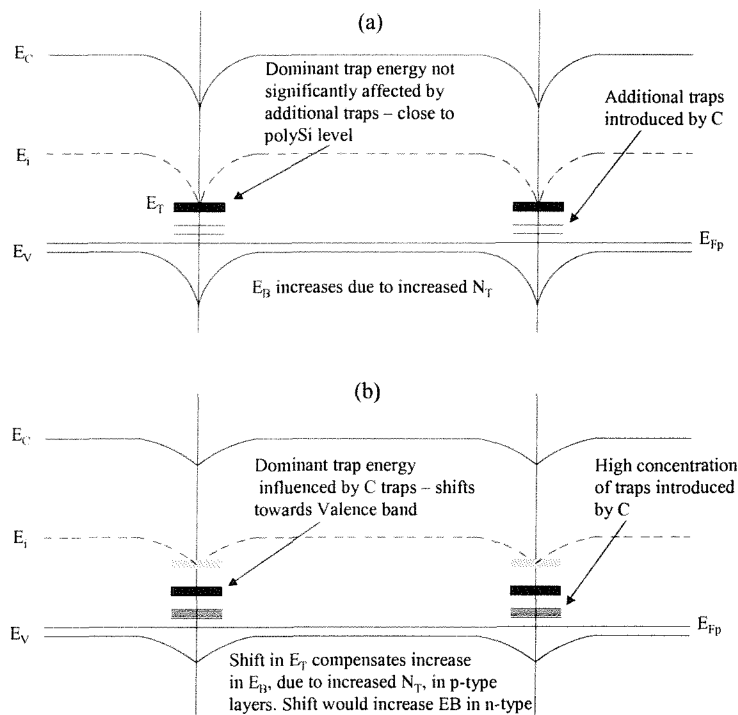

Figure 7.17: Schematic diagram of the energy bands in p-type $\text{polySi}_{1-y}\text{C}_y$ showing how the shift in $E_F - E_T$, relative to the polySi case, reduces the grain boundary energy barrier for a given N_T.

In summary, it has been demonstrated that for low C concentrations, an increase in the grain boundary energy barrier is obtained due to the increased trap density at the grain boundary. This is clearly shown in table 7.3 where the grain boundary energy barrier increases due to an increase in N_T. This behaviour has been observed for n-type layers, but similar behaviour would be expected for p-type layers at low C concentrations. For high C concentrations, the increased trap density located at or around $E_V + 0.28$eV shifts the dominant trap energy towards the valence band. For p-type layers, this shift compensates the increase in E_B due to the increase in N_T, thereby giving a lower increase in the grain boundary energy barrier. This is again clearly shown in table 7.3, where it can be seen that even though the trap density is substantially increased, the effect on the grain boundary energy barrier is much less severe. However, for n-type layers at high C concentrations, the shift towards the valence band would add to the increase in E_B associated with the increase in N_T, giving an even larger energy barrier.

Table 7.3: Summary of the grain boundary trap densities, trap energy levels and barriers for the n- and p-type poly$Si_{1-y}C_y$ layers.

Layer Type	Carbon Content (at.%)	Trap Density (N_T) ($\times 10^{14}$cm^{-2})	E_T Shift w.r.t. Grain Boundary E_F $E_F - E_T$ (meV)	Grain Boundary Energy Barrier (meV)
n-type	0	0.444	0	32
n-type	0.22	0.547	0	48
n-type	0.28	0.648	0	68
n-type	0.69	1.19	0	227
n-type	0.78	1.29	0	269
p-type	0	0.373	0	0
p-type	2.2	2.93	93	11
p-type	3.8	4.78	110	28
p-type	4.5	5.59	118	34
p-type	6.1	7.45	132	43
p-type	7.9	9.54	145	52

7.3.3 Germanium Effects

In section 7.2.2 it was shown that incorporation of 18% Ge into the polySi layers in this work has different effects on the n- and p-type layers. For the n-type layers, the incorporation of this amount of Ge has little effect on the resistivity

or its activation energy, since it has been shown that any differences between the measured values of the polySi and poly$Si_{1-x}Ge_x$ layers can be solely attributed to differences in the doping level. In addition, comparisons of the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers have shown that the addition of 18% Ge does not significantly affect the influence of carbon on the grain boundary. Extraction of the relationship between the grain boundary trap density N_T and C content has shown very similar trends for both the poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. In contrast, for the p-type layers, even this relatively low amount of Ge is shown to influence the effect of carbon on the grain boundary. Poly$Si_{0.82-y}Ge_{0.18}C_y$ layers containing up to 4% C showed no evidence of a grain boundary energy barrier, compared to a measurable energy barrier of 11meV in the poly$Si_{1-y}C_y$ layer containing just 2.2% C. This demonstrates that in the p-type layers the presence of 18% Ge introduces an additional mechanism which partially counteracts the influence of C, thereby lowering the grain boundary energy barrier for a given C content.

There is little, if any, work in the literature on the properties of polycrystalline $Si_{1-x-y}Ge_xC_y$ layers, but several authors [54, 55, 58, 64, 66] have reported that the incorporation of Ge into p-type layers decreases the resistivity with increasing Ge content. This has been attributed to increases in the grain size, Hall mobility and dopant activation with Ge content, and is shown in figure 7.18. In contrast, for n-type layers, the addition of Ge is more complicated. At low Ge concentrations ($x \leq 25\%$), the addition of Ge does not significantly affect the resistivity of the layer, since the larger grain size associated with the addition of Ge is offset by increased phosphorus segregation to the grain boundaries [64]. This was demonstrated in figure 7.4 where n-type layers grown in this work and taken from the literature only exhibited a minor decrease in resistivity over their polySi counterparts. As the Ge content is increased above 25%, the resistivity of the n-type layers has been shown to dramatically increase [58,64,66], leading to layers that actually have a higher resistivity than their polysilicon counterparts. This behaviour has been attributed to a combination of a reduction in the effective carrier concentration, due to enhanced segregation of phosphorus to the grain boundaries, and a reduction in the Hall mobility (figure 7.18).

A possible explanation for the difference in the effects of Ge in the n- and p-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layers is that in the p-type layers, the incorporation of Ge leads to an increase in both the grain size and dopant activation. This will have the net result of reducing both the trap density N_T and the critical doping concentration N^*, which directly translates to a reduction in the grain boundary energy barrier. This reduction in the grain boundary energy barrier will partially compensate the

effects of C in the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, reducing the detrimental effects on the resistivity of the layer. In contrast, for the n-type poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the compensating effects of enhanced phosphorus segregation to the grain boundaries and larger grain size discussed earlier, gives rise to layers that have very similar electrical properties to that of standard n-type polysilicon. Therefore it can be expected that the effects of carbon in the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers will be very similar in nature to those exhibited by the poly$Si_{1-y}C_y$ layers. This was highlighted in figures 7.12, 7.13 and 7.14 where it was shown that the grain boundary energy barrier and trap density dependence on carbon content was almost identical for the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers. However, from our limited results it is difficult to form a conclusive argument for the explanation of the compensating effects of Ge in poly$Si_{1-x-y}Ge_xC_y$ layers. Further work is required in which the Ge and C content are systematically varied over a wide range of compositions to allow a more thorough investigation. In addition, the doping level in the layers, especially the p-type, should be lowered to allow the effects on the grain boundary energy barrier to be studied over the entire compositional range.

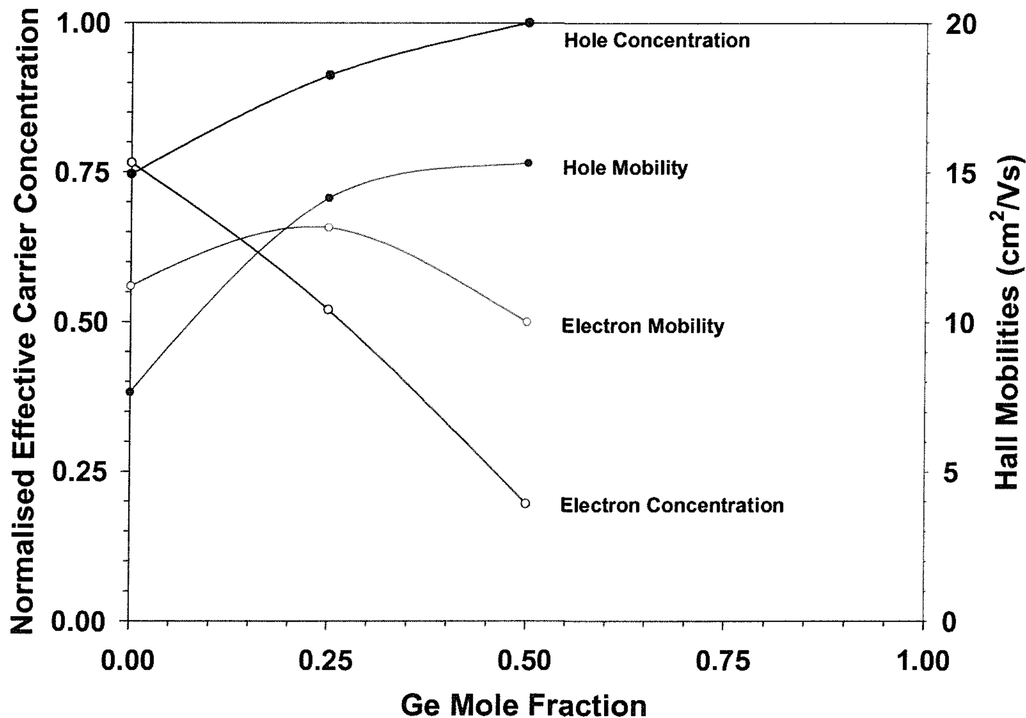

Figure 7.18: Normalised active carrier concentration and Hall mobility of n- and p-type poly$Si_{1-x}Ge_x$ layers showing the effect of Ge. After Bang *et al* [64].

7.4 Conclusions

Extraction of the grain boundary energy barriers of n- and p-type $polySi_{1-y}C_y$ layers showed significantly different behaviour. For the n-type layers, a dramatic increase in the energy barrier was observed for C concentrations above 0.28%. A plot of the relationship between the grain boundary energy barrier and carbon concentration showed that the energy barrier was proportional to the square of the carbon content. This indicates that the carbon is increasing the trapping density at the grain boundaries. Above this level, the n-type layers were non conductive, thereby preventing extraction of the grain boundary energy barrier. In contrast, the p-type layers showed a significantly smaller dependence of grain boundary energy barrier on C content, with the largest measured value being 52meV for 7.8% C. This is 217meV lower than the highest measured n-type barrier, even though it has a factor of 10 higher carbon content.

Extraction of the grain boundary energy barriers of the n-type $polySi_{0.82-y}Ge_{0.18}C_y$ layers showed that the relationship between energy barrier height and carbon content was similar to that in $polySi_{1-y}C_y$, but the magnitude was smaller. This reduction in the grain boundary energy barrier was fully attributable to differences in doping levels, indicating that the incorporation of 18% Ge has no effect on the resistivity of the n-type layers. In contrast, the extracted energy barriers in the p-type $polySi_{0.82-y}Ge_{0.18}C_y$ layers were consistently smaller than their $polySi_{1-y}C_y$ counterparts with similar C concentrations, even though the boron doping level was over a factor of three lower. This indicates that in p-type layers, the Ge partially counteracts the effects of the C at the grain boundaries.

The difference in behaviour between n- and p-type $polySi_{1-y}C_y$ and $polySi_{0.82-y}Ge_{0.18}C_y$ layers has been explained by a shift in the dominant trap energy level towards the valence band at high C concentrations. In p-type layers, the shift towards the valence band reduces the energy barrier, therefore compensating the effect of the increasing grain boundary trap density. This explains the significantly smaller dependence of the grain boundary on C content in the p-type layers. For n-type layers, the shift in the trap energy at high C concentrations would cause a corresponding increase in the grain boundary energy barrier, adding to the increase associated with the increased trap density.

Chapter 8

Conclusions and Future Work

A comprehensive study of the ability of carbon to suppress transient enhanced diffusion in SiGe:C heterojunction bipolar transistors has been performed. Using the temperature dependence of the collector current, the total bandgap narrowing in the base has been extracted for HBTs with and without a background (10^{20}cm^{-3}) carbon concentration. This method is extremely sensitive to small amounts of out-diffusion of the base profile and is therefore ideally suited to determine the existence of parasitic energy barriers. Total bandgap narrowing values of 115meV and 173meV have been extracted for the SiGe and SiGe:C HBTs respectively, for a collector/base reverse bias of 0V. Increasing the collector/base reverse bias to 1V increased the extracted bandgap narrowing in the base of the SiGe HBT to a value of 145meV, but left the SiGe:C HBT value unchanged. This increase in the base bandgap narrowing value of the SiGe HBT confirms the presence of parasitic energy barriers, which in turn shows that transient enhanced diffusion has occurred. In contrast, the unchanged bandgap narrowing of the SiGe:C HBT demonstrates that no barrier exists and hence the carbon containing device, processed identically apart from the addition of carbon to the base layer, has not suffered from transient enhanced diffusion. In addition, the bandgap narrowing value of 173meV is in reasonable agreement with the data of Jain *et al* [4] who predict a total bandgap narrowing of 150meV for a SiGe layer containing the same doping level and Ge content. The discrepancy between the predicted and actual bandgap narrowing values is approximately 15%, and can probably be explained by discrepancies in the temperature models used in the analysis and the effect of substitutional carbon on the bandgap of the SiGe base layer

The effect of carbon position and concentration on enhanced boron diffusion has also been studied. The bandgap narrowing extraction technique was applied to three sets of SiGe:C HBTs, one with carbon located in the collector (transistor CC), one with a low C concentration in the base (transistor CB) and one with a high carbon concentration in the base (transistor HCB). In addition a SiGe control device was also fabricated (transistor NC). Bandgap narrowing values of 78meV, 90meV, 126meV and 111meV were obtained for transistors NC, CC, CB and HCB respectively, for a collector/base reverse bias of 0V. Increasing the collector/base reverse bias to 2V increased the extracted bandgap narrowing values of transistors NC, CC and CB to values of 86meV, 95meV and 131meV respectively, but left the value of transistor HCB unchanged. The increase in the extracted bandgap narrowing values of transistors NC, CC and CB confirms the presence of parasitic energy barriers in these devices, indicating that transient enhanced diffusion has occurred. However, the unchanged value of transistor HCB shows that no parasitic energy barriers exists, indicating that transient enhanced diffusion has been suppressed. These results show that the carbon concentration of $1.1 \times 10^{19}cm^{-3}$, obtained from SIMS analysis, in transistor CB is insufficient to suppress TED of the base profiles. However increasing the carbon concentration to a value of $1.5 \times 10^{19}cm^{-3}$ (transistor HCB) is sufficient to completely suppress the enhanced boron diffusion, thereby preventing parasitic energy barrier formation. This is in broad agreement with the data of Stolk *et al* [40], who showed that a minimum carbon concentration of $10^{19}cm^{-3}$, substitutionally located, was required to suppress transient enhanced diffusion. Finally the results of transistor CC show that carbon located in the collector is ineffective at suppressing transient enhance diffusion of the base dopant, indicating that the carbon suppression capability is only a localised effect. This is in complete agreement with the literature [40], where it was shown that boron profiles located below a carbon rich region still suffered from transient enhanced diffusion, whilst those inside did not.

A potential problem with the incorporation of carbon into the base of a SiGe HBT is that interstitial carbon, either introduced during growth of the base layer or generated by the suppression of transient enhanced diffusion, introduces a deep level defect into the bandgap [119]. This defect could give rise to an increase in the recombination component of the base current, thereby reducing the current gain of the device. Unfortunately, both the SiGe:C devices and the SiGe control devices studied in this work had extremely poor base currents, preventing an assessment of the impact of carbon on the base current. Therefore future work should be directed towards investigating the causes behind the poor base currents of the devices studied, allowing the fabrication process to be optimised for SiGe and SiGe:C HBTs

with decent base current idealities. These devices can then be used to study the impact of carbon on the base current and suggest possible solutions to any problems found.

In addition to the study of carbon for TED suppression of SiGe:C HBTs, the effects of carbon on the electrical properties of in-situ doped, n- and p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers has also been investigated. Measurements of the resistivity, Hall mobility and effective carrier concentration, as a function of carbon content, has allowed an assessment of the effects of carbon on polycrystalline layers, showing whether there is any dependence on dopant type and/or the presence of Ge. PolySi and poly$Si_{0.82}Ge_{0.18}$ layers were grown without intentional carbon incorporation and their resistivities compared to reported resisitivities of similar layers in the literature [62, 64, 66, 123]. These comparisons showed that the layers grown in this work were in broad agreement with those in the literature, with any discrepancies being attributable to differences in doping levels, grain size and/or Ge content. This allows any differences in the electrical properties of the carbon containing layers to be directly attributable to the influence of carbon. Poly$Si_{1-y}C_y$ and Poly$Si_{0.82-y}Ge_{0.18}C_y$ layers were grown with the carbon content being varied by adjusting the Methylsilane flow between 0 and 10sccm. All other gas flows were kept constant to allow direct comparisons between successive growth runs. SIMS analysis was used to quantify the composition of the layers and showed that carbon contents in the p-type layers were consistently higher than in their n-type counterparts. Maximum carbon contents of 7.9% and 4% were obtained for the p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers respectively, whilst the corresponding contents obtained for the n-type layers, for the same Methylsilane gas flow, were only 1.8% and 1.5%. A possible explanation for the differences in the carbon content is that phosphine has been shown to be very effective at blocking surface sites for silane chemisorption, thus inhibiting growth [120, 121]. In contrast, diborane was found not to block the surface sites, allowing easier chemisorption of SiH_4 and better growth rates. Since the chemisorption of $SiCH_6$ is likely to be similar to that of silane, the reduced number of available surface sites could lead to a reduction in the amount of carbon incorporated into the layer. Future work should be directed towards fully understanding why there is a large difference in the carbon concentrations of the n- and p-type layers. Growth and characterisation of several new layers needs to be performed so that the growth process is thoroughly examined. A suitable start would be to grow undoped and low doped layers to show if the carbon incorporation is dopant level dependent, hence showing whether the carbon concentration is affected by the choice of dopant precursor.

For the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the addition of small amounts of C ($\leq 0.9\%$) was found to severely increase the resistivity of the layers, accompanied by a corresponding drop in the effective carrier concentration and Hall mobility. Layers containing higher C concentrations (up to 1.4%) were non-conductive even though highly doped. In contrast, for the p-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the effect of C on the resistivity was much less dramatic, with the impact on the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers being minimal for C concentrations up to 4%. Measurements of the grain boundary energy barriers for the n-type poly$Si_{1-y}C_y$ and poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, extracted from the temperature dependence of the resistivity, showed that there was a square law dependence on carbon content. This is consistent with carbon increasing the grain boundary trap density. In contrast, the grain boundary energy barriers in the p-type poly$Si_{1-y}C_y$ layers exhibited a linear dependence on carbon content, indicating some other mechanism is involved. For the poly$Si_{0.82-y}Ge_{0.18}C_y$ layers, the high doping level and Ge content are sufficient to suppress the grain boundary energy barriers up to a C concentration of 4%. Therefore no dependence on carbon content could be extracted.

From the results of this preliminary investigation into the effects of carbon on the electrical properties of poly$Si_{1-y}C_y$ and poly$Si_{1-x-y}Ge_xC_y$ layers, several future research topics have arisen. Firstly, an explanation of the role of carbon on the electrical properties has been presented. For the low carbon concentrations in the n-type layers, the addition of carbon to the layers causes an increase in the grain boundary trap density and hence the grain boundary energy barrier. Since the resistivity of the layer is exponentially dependent on this energy barrier, this increase due to small amounts carbon explains the dramatic increase observed in the n-type layers. In contrast, the p-type layers exhibited a much less severe dependence on carbon content, even for much higher carbon concentrations. At these higher concentrations, the electrical behaviour could not be solely explained by carbon increasing the grain boundary trap density, as in the case of the n-type layers, indicating some other mechanism was involved. Therefore an hypothesis has been presented in chapter 7 which attempts to explain the differences observed in the n- and p-type layers, at both high and low concentrations. At low concentrations, the introduction of carbon increases the trap density at the grain boundary without affecting the dominant trap energy. Therefore there is a corresponding rise in the grain boundary energy barrier and hence an increase in the resistivity. Since the dominant trap density is unaffected, the presence of carbon should affect n- and p-type layers similarly, according the the square law dependence of equation 2.44. In contrast at high C concentrations, the increased trap density due to the presence of carbon is accompanied by a shift in the dominant trap energy level towards the

valence band. In p-type layers, the shift towards the valence band reduces the energy barrier, therefore compensating the effect of the increasing grain boundary trap density. This explains the significantly smaller dependence of the grain boundary on C content in the p-type layers. For n-type layers, the shift in the trap energy at high C concentrations would cause a corresponding increase in the grain boundary energy barrier, adding to the increase associated with the increased trap density. However, from the limited set of results obtained from the preliminary work so far, it is difficult to draw firm conclusions on the validity of this hypothesis. Therefore further growths are required in which the carbon concentration in the p-type layers is reduced to a level that is comparable to that found in the n-type layers of this work, allowing a direct comparison of the effects of carbon to be made. In addition, as stated earlier, the doping level in the p-type layers should also be reduced so that the effects of carbon on the grain boundary energy barrier are more easily studied. It should be noted that increasing the carbon content of future n-type layers to the level found in the p-type layers of this work is not practically viable since is was found that layers containing just 1.4% carbon were non-conductive even though highly doped.

Secondly, it has been shown that the inclusion of 18% Ge has no effect on the influence of the carbon in n-type layers, whereas in p-type layers, the presence of Ge has reduced the impact of carbon on the resistivity. A possible explanation for this behaviour was presented in chapter 7, however from the limited results it is difficult to present a conclusive hypothesis on the effects of Ge in poly$Si_{1-x-y}Ge_xC_y$ layers. Therefore further work is required in which the Ge and C content are systematically varied over a wide range of compositions to allow a more thorough investigation. In addition, the doping level in the layers, especially the p-type, should be lowered to allow the effects on the grain boundary energy barrier to be studied over the entire compositional range.

Finally, attempts should be made to measure the bandgaps of the polycrystalline layers to see if carbon incorporation has any effect. A possible method may be to use a polycrystalline p-i-n structure to measure the photoconductivity of the layer as a function of excitation wavelength. The bandgap can then be extracted from an extrapolation of the data. This has been successfully applied to single-crystal layers [124, 125], but little, if any, work has been reported on polycrystalline layers. Therefore it is not known how the grain boundaries will affect the photoconductivity and bandgap extraction process, indicating that substantial investigative work on the optical properties of polysilicon will be required first.

Appendix A

Publications arising from this work

I. M. Anteney, G. Lippert, P. Ashburn, H. J. Osten, B. Heinemann and G. J. Parker. "*Electrical determination of bandgap narrowing and parasitic energy barriers in SiGe and SiGeC heterojunction bipolar transistors*", EDMO'97, pp 55-60

I. M. Anteney, P. Ashburn, G. J. Parker, G. Lippert and H. J. Osten. "*Effect of the Carbon position in the base for the elimination of parasitic energy barriers in SiGe:C HBTs*", ESSDERC 98, pp 132-135

I. M. Anteney, G. Lippert, P Ashburn, H. J. Osten, B. Heinemann, G. J. Parker and D. Knoll. "*Characterisation of the effectiveness of Carbon incorporation in SiGe for the elimination of parasitic energy barriers in SiGe HBTs*", IEEE Electron Device Letters Vol 20 No 3 pp 116-118

J.S. Hamel, G.R. Leach and I.M. Anteney. "*Direct extraction of intrinsic excess phase shift time constants in SiGe HBTs*", ESSDERC'99, pp456-459

I.M. Anteney, G.J. Parker, P. Ashburn and H.A. Kemhadjian. "*Electrical properties of in-situ phosphorus and boron doped polycrystalline* $Si_{0.82-y}Ge_{0.18}C_y$ *films*", accepted for publication in Applied Physics Letters.

I.M. Anteney, G.J. Parker, P. Ashburn and H.A. Kemhadjian. "*Electrical properties of in-situ phosphorus and boron doped polycrystalline* $Si_{1-y}C_y$ *films*", accepted for presentation at Materials for Microelectronics Conference - Dublin, October 2000.

I.M. Anteney, G.J. Parker, P. Ashburn and H.A. Kemhadjian. "*The role of carbon on the electrical properties of polycrystalline* $Si_{1-y}C_y$ *and* $Si_{1-x-y}Ge_xC_y$ *films*", submitted to the Journal of Applied Physics

I.M. Anteney, G.J. Parker, P. Ashburn and H.A. Kemhadjian. "*Deposition temperature effects on the resistivity of highly doped p-type polycrystalline* $Si_{1-x}Ge_x$ *layers*", to be submitted to Applied Physics Letters.

Appendix B

Derivation of a Current-Voltage Relationship for Polysilicon

When thermionic emission dominates, the current flow in the polysilicon layer can be found by finding the net current flow from the forward and reverse thermionic current densities i.e.

$$J = J_F - J_R \tag{B.1}$$

where J_F and J_R are the forward and reverse thermionic current densities respectively. The thermionic current density as a function of applied bias can be given by

$$J_i = qnv_c exp\left[-\frac{q}{kT}(V_B - V)\right] \tag{B.2}$$

where i is the current direction, n is the free carrier concentration, V_B the energy barrier height with no applied bias, V the applied voltage across the depletion region and v_c is the collection velocity given by

$$v_c = \sqrt{\frac{kT}{2\pi m^*}} \tag{B.3}$$

With no applied bias, the barriers to carrier transport are equal and so the forward current J_F emitted over the barrier is equal to the reverse current J_R, hence no net current flow. When a bias voltage is applied, the barrier to carrier transport in one direction decreases while increasing in the other direction. For an applied voltage V_{app}, the voltage across one grain V_G will be approximately V_{app} divided by the number of grains in the polycrystalline layer. For small biases it can be assumed that V_G divides equally across each depletion region without introducing significant errors [96]. Therefore the barrier in the forward direction will be decreased by $V \approx V_G/2$, whilst the barrier in the reverse direction will be increased by $V_G/2$. This is shown schematically in figure B.1. Equation B.2 can therefore be rewritten as

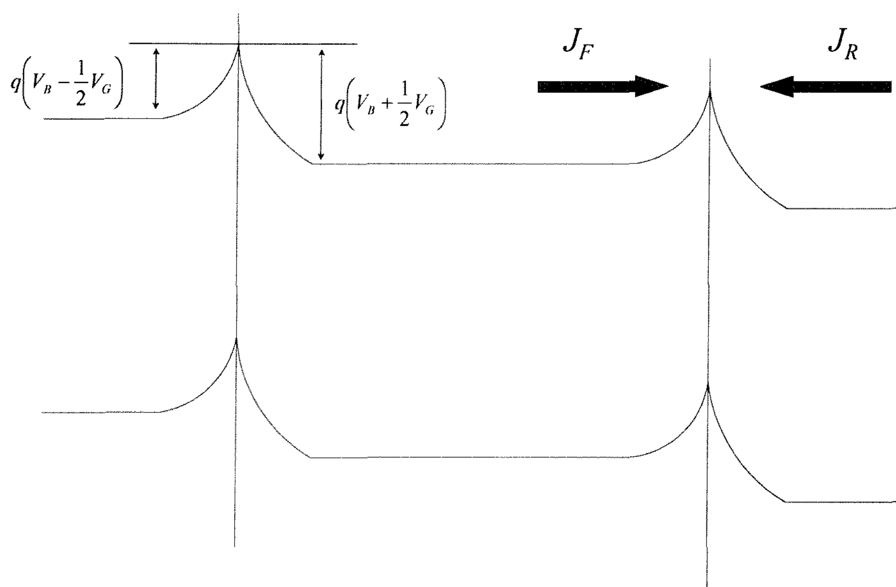

Figure B.1: Schematic diagram showing how the application of bias decreases the barrier height in the forward direction and increases it in the reverse.

$$J_F = qnv_c exp\left[-\frac{q}{kT}\left(V_B - \frac{1}{2}V_G\right)\right] \tag{B.4}$$

and

$$J_R = qnv_c exp\left[-\frac{q}{kT}\left(V_B + \frac{1}{2}V_G\right)\right] \tag{B.5}$$

for the forward and reverse thermionic currents respectively. The net current flow is then given by

$$J = qnv_c exp\left(-\frac{qV_B}{kT}\right)\left[exp\left(\frac{qV_G}{2kT}\right) - exp\left(-\frac{qV_G}{2kT}\right)\right] \tag{B.6}$$

Using the relationships $e^x - e^{-x} = 2\sinh(x)$ and $\sinh(x) \approx x$ for small x, valid for $V_G << kT/q$, equation B.6 can be rewritten in the form of

$$J = \frac{q^2 nv_c V_G}{kT} exp\left(-\frac{qV_B}{kT}\right) \tag{B.7}$$

which gives a linear relationship between current and applied voltage.

Appendix C

Process Listing for the $Si_{1-x}Ge_x$ HBT Batch

1. Deposition of SiGe and SiGe:C HBT base and emitter layers at IHP Frankfurt(Oder), Germany.
2. Photolith BA mask, dark field, $2\mu m$ resist. All Wafers.
3. Hardbake for dry etch. All Wafers.
4. Descum in SRS Barrel Asher. All Wafers.
5. See process engineer. Check etch profile on first wafer
6. Mesa Dry etch. 500nm with 45° sloping sides. All Wafers.
7. Resist strip in Barrel Asher. All Wafers.
8. RCA clean. All Wafers.
9. Low temperature oxide deposition. 150nm at $400^oC.SiH_4andO_2$. All Wafers.
10. Photolith NI mask, Dark Field. All Wafers.
11. Hardbake for wet etch. All Wafers.
12. Descum in Barrel Asher. All Wafers.
13. See process engineer. Check etching of first wafer.
14. Wet etch oxide. 7:1 BHF.
15. Resist strip in Barrel Asher. All Wafers.
16. See process engineer. Critical timing of interface treatment - LTO not densified.
17. RCA clean. All Wafers.
18. HF dip, 20:1 BHF. All Wafers.
19. Amorphous Si deposition, 200nm at 560^oC. All Wafers.
20. Poly implant. Arsenic, $1 \times 10^{16} cm^{-2}$, 45keV. All Wafers.

21. Photolith P Mask, light field. All Wafers.
22. Dry Etch PolySi. All Wafers.
23. Resist strip in Barrel Asher. All Wafers.
24. Fuming Nitric Clean - 2nd pot only. All Wafers.
25. Photolith PD mask, dark field. All Wafers.
26. Hardbake - Deep UV for implant. All Wafers.
27. Implant $B^+ 2 \times 10^{15}cm^{-2}$, 70keV. Wafer 11.
28. Implant $BF_2{}^+ 2 \times 10^{15}cm^{-2}$, 35keV. All Wafers.
29. Resist strip. All Wafers.
30. RCA Clean. All Wafers.
31. LTO deposition. 600nm at 400°C. All Wafers.
32. Frontspin resist. All Wafers.
33. Hardbake for dry etch. All Wafers.
34. Dry Etch backs of wafers for SiO_2 and PolySi removal. All Wafers.
35. See process engineer. Check all oxide and polySi has been removed from back of wafers. All Wafers.
36. Resist strip in Barrel Asher. All Wafers.
37. Rapid Thermal Anneal. 1000°C 30s in N_2. Wafers 1,3,5,7,9,11.
38. Rapid Thermal Anneal. 900°C 30s in N_2. Wafers 2,4,6,8,10.
39. Photolith CW mask, dark field. All Wafers
40. Hardbake for wet etch. All Wafers.
41. Descum in Barrel Asher. All Wafers.
42. Wet etch oxide, 7:1 BHF. All Wafers.
43. Resist strip in Barrel Asher. All Wafers.
44. Pre-metal dip etch, 20:1 BHF. All Wafers.
45. Sputter Ti 100nm + Al/Si(1%) 1000nm. All Wafers.
46. Photolith M mask, light field. All Wafers.
47. Inspect wafers for resist in windows after development. All Wafers.
48. Hardbake for dry etch. All Wafers.
49. Dry etch Al/Si and Ti. All Wafers.
50. Resist strip in Barrel Asher. All Wafers.
51. See process engineer. Preliminary electrical test before alloy. All Wafers.
52. Alloy/Anneal, $H_2/N_2, 300^oC$, 15min. All Wafers.

Appendix D

Program to calculate the mean base doping and the total bandgap narrowing in the base of a SiGe HBT

```
#include "stdio.h"
#include "math.h"
#include "stdlib.h"
#include "numeric.h"
#include "string.h"

/*Klaassen B data for majority hole mobility*/
#define mumaxh 470.5
#define muminh 49.9
#define muoneh 29
#define Nref1h 2.23e17
#define Nref2h 6.1e20
#define alpha1h 0.719
#define thetah 2.247

/*Klaassen P data for minority electron mobility */
#define mumaxe 1417
#define mumine 68.5
```

```
#define muonee 52.2
#define Nref1e 9.68e16
#define Nref2e 3.41e20
#define alpha1e 0.68
#define thetae 2.285

/* Electron and hole masses */
#define m0 9.108e-31
#define m1 1.258
#define me 9.108e-31
#define mp 1.146e-30

#define q 1.6021892e-19
#define maxerror 3

#define Nc 1e16                /* Collector Doping */
#define Ne 1e18                /* Emitter Doping */
#define alphath 4.73e-4        /* Thurmond model parameters */
#define betath 636             /* Thurmond model parameters */
#define planckh 6.626e-34      /* Plancks constant */
#define boltk 1.38e-23         /* Boltzmanns constant */
#define eV 1.602e-19           /* Electron volt */
#define micron 1e-6            /* Microns */
#define Vbe 0.6                /* Base emitter voltage */

long double temp;              /* Measurement temp */
long double Rmeas;             /* Measured Base Sheet Resistance */
long double Pp;                /* Hole Doping Concentration */
long double Wm;                /* Basewidth nm */
long double Wmcm;              /* Basewdith cm */
long double Er;                /* Relative Permitivity */
long double Ge;                /* Ge percentage */
long double Ni;                /* Intrinsic carrier concentration */
long double Wn;                /* Neutral basewidth */
long double holemob;
long double elecmob;
long double Rcalc;
long double Ic1,Ic2;
long double Jc1,Jc2;
```

```
long double Jc1divJo, Jc2divJo;
long double Sibandgap;
long double Jo;
long double C;
long double emittwidth;
long double emittlen;
long double relperm()
{
long double Esige;
Esige=(0.041*Ge)+11.9;
return(Esige);
}

long double intrinsic()
{
long double ni;
ni = 3.88e16*powl(temp,1.5)*exp(-7000/temp);
return(ni);
}

long double neutral (long double Ni)
{
long double VoCB;        /* Built in voltage at CB junc*/
long double VoEB;        /* Built in voltage at EB junc*/
long double Wbc;         /* Depletion Width at CB junc */
long double Wbe;         /* Depletion Width at EB junc */
long double Xbc;         /* Penetration into base at collector */
long double Xbe;         /* Penetration into base at emitter */
long double totpen;      /* Total penetration into base */


VoCB = 8.671346815e-5*temp*log((Pp*Nc)/(Ni*Ni));
VoEB = 8.671346815e-5*temp*log((Pp*Ne)/(Ni*Ni));


Wbc = sqrt(1104738.442*Er*VoCB*((1/Pp)+(1/Nc)));
Wbe = sqrt(1104738.442*Er*VoEB*((1/Pp)+(1/Ne)));
```

```
Xbc = (long double)(Wbc*Nc)/(Nc+Pp);
Xbe = (long double)(Wbe*Ne)/(Ne+Pp);


totpen = Xbc+Xbe;


return (totpen);
}

long double klassB(long double Pp)
{
long double Zh,Nhsc,Nhsceff,mulat;
long double Gh1,Gh2,Gh,Ph1,Ph2,Ph;
long double Fh, muhn,muin,muic,muh;
long double Nd = 10,n = 10;


muin=(powl(mumaxh,2)/(mumaxh-muminh))*powl(temp/300,((3*alpha1h)-1.5));
muic=((mumaxh*muminh)/(mumaxh-muminh))*powl(300/temp,0.5);


Zh = 1+(1/(0.5+powl((7.2e20/Pp),2)));
Nhsc = Nd + Pp + n;

mulat = mumaxh*powl((300/temp),thetah);


Ph1 = 2.459/(3.97e13*powl(((1/(powl(Zh,3)*Nhsc))*
        (powl(temp/300,3))),0.6666667));

Ph2 = 3.828/((1.36e20/(Pp+n))*(mp/m0)*powl(temp/300,2));
Ph = powl(Ph1+Ph2,-1);

Gh1 = 0.89233/powl(0.41372+powl((m0/mp)*(temp/300),0.28227)*Ph,0.19778);
Gh2 = 0.005978/powl(Ph*powl((mp/m0)*(300/temp),0.72169),1.80618);

Gh = 1 - (Gh1 + Gh2);
Fh = (0.7643*powl(Ph,0.6478)+2.2999+6.5502*m1)/
      (powl(Ph,0.6478)+2.3670-(m1*0.8552));
```

```
Nhsceff = Pp + Gh*Nd + (n/Fh);
muhn=muin*(Nhsc/Nhsceff)*powl(Nref1h/Nhsc,alpha1h)+muic*((n+Pp)/Nhsceff);

muh = powl(powl(mulat,-1)+powl(muhn,-1),-1);

return (muh);
}

long double klassP(long double Pp)
{
long double Ze,Nesc,Nesceff,mulate;
long double Ge1,Ge2,Ge,Pe1,Pe2,Pe;
long double Fe, muhe,muine,muice,mue;
long double Nd = 10,n = 10;


muine=(powl(mumaxe,2)/(mumaxe-mumine))*powl(temp/300,((3*alpha1e)-1.5));
muice=((mumaxe*mumine)/(mumaxe-mumine))*powl(300/temp,0.5);

Ze = 1+(1/(0.21+powl((4e20/Nd),2)));
Nesc = Nd + Pp + Pp;

mulate = mumaxe*powl((300/temp),thetae);


Pe1 = 2.459/(3.97e13*powl(((1/(powl(Ze,3)*Nesc))*
      (powl(temp/300,3))),0.6666667));

Pe2 = 3.828/((1.36e20/(Pp+n))*(me/m0)*powl(temp/300,2));
Pe = powl(Pe1+Pe2,-1);

Ge1 =0.89233/powl(0.41372+powl((m0/me)*(temp/300),0.28227)*Pe,0.19778);
Ge2 = 0.005978/powl(Pe*powl((me/m0)*(300/temp),0.72169),1.80618);

Ge = 1 - (Ge1 + Ge2);


Fe = (0.7643*powl(Pe,0.6478)+2.2999+6.5502*m1)/
     (powl(Pe,0.6478)+2.3670-(m1*0.8552));
```

```
Nesceff = Nd + (Ge*Pp) + (Pp/Fe);
muhe=muine*(Nesc/Nesceff)*powl(Nref1e/Nesc,alpha1e)+muice*((n+Pp)/Nesceff);

mue = powl(powl(mulate,-1)+powl(muhe,-1),-1);

return (mue);
}

long double Bsheet(long double Wn,long double holemob,long double Pp)
{
return(1/(q*Wn*holemob*Pp));
}

long double error(long double inputPp)
{
Pp=inputPp;
Wn = Wmcm - neutral(Ni);
holemob=klassB(Pp);
elecmob=klassP(Pp);
Rcalc = Bsheet(Wn,holemob,Pp);
printf("Pp=%Le, res=%Le, rmeas=%Le/n",Pp,Rcalc,Rmeas);
return(Rcalc-Rmeas);
}

long double collsat (void)
{


return (C*4*q*powl(2*3.14159/(planckh*planckh),3)* powl(me*mp,1.5)*
        powl(boltk*temp,4)*holemob*elecmob*1e-8*Rmeas*expl(((q*Vbe)
        -Sibandgap)/(boltk*temp)));

}

int main (void)
{


char ipfile[11]=" ",opfile[11]=" ",infiledir[30] ="c:/users/ima96r/";
char outdir1[30] = "c:/users/ima96r/";
```

```
char outdir2[30] = "c:/users/ima96r/";
FILE *infile, *outfile1, *outfile2;

printf("Enter Basewidth (nm) : ");
scanf("%Lf",&Wm);
printf("Enter Ge content (%) : ");
scanf("%Lf",&Ge);
printf("Enter constant C (Effective DOS ratio x Majority Mobility ratio):");
scanf("%Lf",&C);
printf("Enter emitter width (microns):");
scanf("%Lf",&emittwidth);
printf("Enter emitter length (microns):");
scanf("%Lf",&emittlen);
printf("Enter Input Filename : ");
scanf("%s",ipfile); strcat(infiledir,ipfile);
strcat(infiledir,".txt");
strcat(outdir1,ipfile);
strcat(outdir2,ipfile);
strcat(outdir1,".mob");
strcat(outdir2,".bgn");
infile = fopen(infiledir, "r");
outfile1 = fopen(outdir1, "w");
outfile2 = fopen(outdir2, "w");


if (infile == NULL)
{
printf("Cannot open desired input file. Check filename.");
exit(1);
}
else if ((outfile1 == NULL) —— (outfile2 == NULL))
{
printf("Cannot open desired output file.");
exit(1);
}
else
{
fprintf(outfile1, " T hmob emob Av Na /n");
fprintf(outfile2," 1000/T Jc1/Jo Jc2/Jo /n");
```

```
printf(" T hmob emob Av Na 1000/T Jc1/Jo Jc2/Jo/n");
do {
if(fscanf(infile,"%Lf %Lf %Lf %Lf",&temp, &Rmeas, &Ic1, &Ic2)!=EOF)
{
Er = relperm();
Wmcm=Wm*1e-7;
Ni = intrinsic();
Pp=1e18;
Pp=sucapprox(1E20,1E18,error,1);



fprintf(outfile1,"%.3Lf %.3Lf %.3Lf %.3Lf %.3Le/n",
        temp,Rmeas,holemob,elecmob,Pp);
Sibandgap=1.17*eV-((alphath*eV*temp*temp)/(temp+betath));
Jo = collsat();
Jc1 = Ic1/(emittwidth*emittlen*(micron*micron));
Jc2 = Ic2/(emittwidth*emittlen*(micron*micron));
Jc1divJo=Jc1/Jo;
Jc2divJo=Jc2/Jo;
fprintf(outfile2,"%.3Lf %.3Lf %.3Lf/n",(1000/temp),Jc1divJo,Jc2divJo);
printf("%.3Lf %.3Lf %.3Lf %.3Le %.3Lf %.3Lf %.3Lf/n",
       temp,holemob,elecmob,Pp,(1000/temp),Jc1divJo,Jc2divJo);

}
}while (!feof(infile));
fclose(infile);
fclose(outfile1);
fclose(outfile2);
}
return(0);
}
```

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