Modelling and Characterisation of Silicon-On-Insulator Lateral Double Diffused MOSFETs for Analogue Circuit Simulation

by Nele D'Halleweyn

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UNIVERSITY OF SOUTHAMPTON
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ABSTRACT

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As the scaling down of smart power ICs is gaining in importance, SOI technology is becoming more attractive. The LDMOS transistor is one of the key devices in HV ICs, and a good model is indispensable in order to perform accurate circuit design. Some subcircuit models for bulk and SOI LDMOS devices are available, but, when certain special aspects of device characteristics become critical, they are not always sufficient, and the need for an accurate, robust compact model is apparent. Particular emphasis has been placed on the behaviour and circuit level modelling issues related to high side drive applications, and on the self- and mutual heating. For the N-type LDMOS, high side operation increases the on-resistance and demands specific modelling effort.

In this thesis a circuit simulator model is developed, based on a detailed study of device physics of the LDMOS. First, the subcircuit modelling approach was followed, resulting in a 'quick-fix' LDMOS model. The drawbacks of this modelling approach are the complexity of the circuit, and convergence problems.

To overcome these disadvantages a compact model is presented. The model has only one internal node, situated in the channel at the transition point from thin gate oxide into field oxide. Both currents are carefully derived, to keep the model as physical as possible. The current under the thin gate oxide is described in terms of the surface potentials, whilst taking into account the lateral doping gradient and the overlap of the gate over the N^- drift region. The impact of the thickness of the depletion layer at the buried oxide on the current under the field oxide is studied rigorously, leading to a good prediction of the unique high-side behaviour. Next, the complete SOI LDMOS charge model is set out, presenting a promising new approach to deal with the unusual charge partitioning in the LDMOS.

DC simulations with the compact model match the measured characteristics well for a wide range of geometries, with self-heating and high-side effects being accounted for. The simulated and measured capacitance characteristics for a range of geometries show excellent qualitative behaviour, and demonstrate the soundness of the new charge model.

The model has been implemented in the SPICE circuit simulator and careful formulation and coding has led to a very robust SOI LDMOS model, which converges easily without the need for node setting. The model is evaluated thoroughly, using a set of simulations based on the SEMATECH tests. Finally, two special analogue circuits were designed and fabricated to allow circuit level evaluation of the accuracy and robustness of our model. The model predicts the measurement results well for circuits containing LV and MV transistors, and also gives a reasonable prediction of the HV circuits. We can conclude that, with further optimisation, our compact SOI LDMOS model can provide a practical and reliable simulation tool for commercial design use.

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List of Symbols

Symbol Conventions:

V_{XY}	Voltage drop between nodes X and Y [V]
C_{xy}	(Trans)capacitance of node X with respect to node Y [F]
$^{\mathrm{dr}}$	subscript referring to the drift region
$^{\mathrm{f}}$	subscript referring to the front gate
$^{\mathrm{b}}$	subscript referring to the back gate

α	Normalised pinch-off region length (second CLM model) [-]
α_θ	Scattering coefficient [cm/V]
β	Inversion layer gain factor [$\mathrm{A/V^2}$]
β_{acce}	Effective drift region accumulation layer gain factor [$\mathrm{A/V^2}$]
β_{acc}	Drift region accumulation layer gain factor [$\mathrm{A/V^2}$]
β_{e}	Effective inversion layer gain factor [$\mathrm{A/V^2}$]
χ	Temperature coefficient for the threshold voltage [V/K]
ΔL	Threshold roll-off with channel length [m]
ΔL	Threshold roll-up with channel width [m]
ΔT	Device temperature rise [K]
ϵ_0	Permittivity of vacuum [$8.854 \cdot 10^{-12}\mathrm{F/m}$]
ϵ_{ox}	Permittivity of silicon-dioxide [$3.9 \cdot 8.854 \cdot 10^{-12}\mathrm{F/m}$]
ϵ_{si}	Permittivity of silicon [$11.7 \cdot 8.854 \cdot 10^{-12}\mathrm{F/m}$]
η_{s}	Fast surface states coefficient [-]
γ	Local front gate body factor [$\sqrt{\mathrm{V}}$]
γ^{bdr}	Back gate body factor in the drift region [$\sqrt{\mathrm{V}}$]
γ^{b}	Back gate body factor in the body [$\sqrt{\mathrm{V}}$]
γ^{fdr}	Front gate body factor in the drift region [$\sqrt{\mathrm{V}}$]
γ_0	Front gate body factor in the body [$\sqrt{\mathrm{V}}$]
γ_{e1}	Mean value of γ for $L_{\mathrm{min}} < y < L_{\mathrm{i}}$[$\sqrt{\mathrm{V}}$]
γ_{e2}	Mean value of γ for $L_{\mathrm{i}} < y < L_{\mathrm{eff}}$[$\sqrt{\mathrm{V}}$]

γ_{m}	Mean value for the front gate body factor in the body [$\sqrt{\mathrm{V}}$]
γ_{oo}	Electrical drain induced barrier lowering factor [-]
κ_{ox}	Thermal conductivity of SiO_2 [W/(m·K)]
λ	Electrical CLM factor [1/V]
λ_{r}	CLM factor [m/V]
$\mu_{0\mathrm{n}}$	Low field carrier mobility for electrons [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
$\mu_{0\mathrm{p}}$	Low field carrier mobility for holes [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_0	Low field carrier mobility [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{acc}	Zero field accumulation surface mobility [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{dreff}	Effective drift region mobility [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{dr}	Zero field drift region mobility [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{eff}	High field effective mobility [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{s}	Zero field inversion surface mobility [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{xeff}	Effective mobility accounting for vertical mobility degradation [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
μ_{yeff}	Effective mobility accounting for carrier velocity saturation [$\mathrm{cm}^2/(\mathrm{V{\cdot}s})$]
ϕ_{bid}	Built-in potential for the D-B diode [V]
ϕ_{bis}	Built-in potential for the S-B diode [V]
ϕ_{Fdr}	Fermi-potential for the drift region [V]
ϕ_{F}	Fermi-potential for the body region [V]
ϕ_{t}	Thermal voltage [V]
ψ	Local channel potential [V]
ψ_{Di}	Channel potential at the internal drain [V]
ψ_{D}	Channel potential at the drain [V]
ψ_{i}	Channel potential where inversion at the buried oxide stops [V]
ψ_{s0}	Surface potential at the source end of the channel ($y = 0$) [V]
ψ_{sdi}	Surface potential at the drain end of the channel ($y = L_{\mathrm{drov}} + L_{\mathrm{eff}}$) [V]
ψ_{si0}	Strong inversion surface potential at the source end of the channel ($y = 0$) [V]
ψ_{siLinv}	Charge model expression for the strong inversion surface potential at the left side of the body-drain junction ($y = L_{\mathrm{eff}}^{-}$) [V]
ψ_{siL}	Strong inversion surface potential at the body-drain junction ($y = L_{\mathrm{eff}}$) [V]
ψ_{si}	Strong inversion surface potential in the channel [V]
$\psi_{\mathrm{si}}^{\mathrm{dr}}$	Strong inversion surface potential in the drift region under the front gate [V]
ψ_{sLacc}	Surface potential at the right side of the body-drain junction ($y = L_{\mathrm{eff}}^{+}$) [V]
ψ_{sLmin}	Surface potential at $y = L_{\mathrm{min}}$) [V]
ψ_{sLsatf}	Combined expression for the subthreshold and saturation surface potential [V]
ψ_{sLsat}	Saturation surface potential [V]
ψ_{sL}	Surface potential at the body-drain junction ($y = L_{\mathrm{eff}}$) [V]
ψ_{ss0}	Subthreshold surface potential at the source end of the channel ($y = 0$) [V]

ψ_{ssL}	Subthreshold surface potential at the body-drain junction ($y = L_{\mathrm{eff}}$) [V]
ψ_{ss}	Subthreshold surface potential in the channel [V]
$\psi_{\mathrm{ss}}^{\mathrm{dr}}$	Subthreshold surface potential in the drift region under the front gate [V]
ψ_{st0}	Surface potential at the source end of the channel, not including high-field effects [V]
ψ_{s}	Surface potential in the channel [V]
$\psi_{\mathrm{s}}^{\mathrm{dr}}$	Surface potential in the drift region under the front gate [V]
σ	Drain induced barrier lowering factor [m]
τ	Carrier life time [s]
θ	Vertical field inversion mobility degradation factor [V^{-1}]
θ_{3dr}	Velocity saturation drift mobility degradation factor [V^{-1}]
θ_{acc}	Vertical field accumulation mobility degradation factor [V^{-1}]
ξ_{c}	Critical electric field [V/cm]
ξ_{xeff}	Effective transverse electric field [V/cm]
ξ_{x}	Transverse electric field [V/cm]
ζ_{x}	Empirical parameter used in the formula for ξ_{x} [-]
C_{gbbo}	Back gate-body overlap capacitance [F]
C_{gbdo}	Back gate-drain overlap capacitance [F]
C_{gbso}	Back gate-source overlap capacitance [F]
C_{gfs}	Transcapacitance of the front gate node with respect to the body node [F]
C_{gfbo}	Front gate-body overlap capacitance [F]
C_{gfd}	Transcapacitance of the front gate node with respect to the drain node [F]
C_{gfdo}	Front gate-drain overlap capacitance [F]
C_{gfgf}	Capacitance of the gate [F]
C_{gfs}	Transcapacitance of the front gate node with respect to the source node [F]
$C_{\mathrm{gfs*}}$	Transcapacitance of the front gate node with respect to the source and body nodes tied together [F]
C_{gfso}	Front gate-source overlap capacitance [F]
C_{dd}	Capacitance of the drain node [F]
C_{dgf}	Transcapacitance of the drain node with respect to the front gate node [F]
C_{ds}	Transcapacitance of the drain node with respect to the source node [F]
$C_{\mathrm{ds*}}$	Transcapacitance of the drain node with respect to the source and body nodes tied together [F]
C_{sd}	Transcapacitance of the source node with respect to the drain node [F]
C_{sgf}	Transcapacitance of the source node with respect to the front gate node [F]
C_{ss}	Capacitance of the source node [F]
$C_{\mathrm{s*d}}$	Transcapacitance of the source and body nodes tied together with respect to the drain node [F]

C_{s*gf}	Transcapacitance of the source and body nodes tied together with respect to the front gate node [F]
C_{s*s*}	Capacitance of the source and body nodes tied together [F]
C_{ij}	(Trans)capacitance between nodes i and j [F]
C_{ob}	Back gate oxide capacitance per unit area [F/m^2]
C_{of}	Front gate oxide capacitance per unit area [F/m^2]
C_T	Thermal capacitance [J/K]
D	Diffusion constant [cm^2/s]
d	Local depletion layer thickness extending from the buried oxide in the drift region [m]
d_{dep}	Expression for d with inversion at the buried oxide [m]
d_{inv}	Expression for d without inversion at the buried oxide [m]
D_{itb}	Back fast surface state density [cm^{-2}eV^{-1}]
D_{itf}	Front fast surface state density [cm^{-2}eV^{-1}]
E_g	Band gap [eV]
f_v	Factor to account for the partially vertical current flow [-]
I_{acc}	Simplified expression for the current in the accumulation layer under the thin gate oxide [A]
I_{CH0}	Current under the thin gate oxide, without CLM and DIBL [A]
I_{chi}	Current in the inversion layer under the thin gate oxide [A]
I_{CHsat}	Saturation current under the thin gate oxide [A]
I_{CH}	Current under the thin gate oxide [A]
I_{DR0}	Drift region current under the field oxide without velocity saturation [A]
I_{drg}	Current in the drift region under the thin gate oxide [A]
I_{DR}	Drift region current under the field oxide [A]
I_{dr}	Simplified expression for the current in the drift region under the field oxide [A]
I_{DS}	Drain-Source Current [A]
I_D	Drain Current [A]
I_{inv}	Simplified expression for the current in the inversion layer under the thin gate oxide [A]
k	Temperature exponent for μ_s [-]
k_{acc}	Temperature exponent for μ_{acc} [-]
k_{dr}	Temperature exponent for μ_{dr} [-]
k_{N_A}	Doping gradient in the body [-]
L	Under-diffusion of the body-well [m]
L_{drov}	Overlap of the front gate over the drift region [m]
L_{dr}	Length of the drift region under the field oxide [m]
L_D	Under-diffusion of the source [m]

l_{d}	Reduction in effective channel length due to CLM [m]
L_{eff}	Effective channel length [m]
L_{i}	Mean value of L_{min} and L_{eff} [m]
L_{min0}	Expression for L_{min} when inversion charge is present at the drain end) [m]
L_{minL}	Expression for L_{min} when no inversion charge is present at the drain end [m]
L_{min}	y position for which inversion in the channel starts) [m]
L_{tot}	Total channel length ($= L_{\mathrm{drov}} + L_{\mathrm{eff}}$) [m]
l_{x}	Effective pinch-off region length (second CLM model) [m]
m	Smoothing factor [-]
M_{exp}	Maximum argument allowable in an exponential function [-]
n	Mobile carrier density [cm^{-3}]
N_{Ad}	Body doping concentration at the drain end [cm^{-3}]
N_{As}	Body doping concentration at the source end [cm^{-3}]
N_{A}	Body doping concentration [cm^{-3}]
N_{b}	Bottom doping concentration in an SOI PMOS [cm^{-3}]
N_{D}	Drift region doping concentration [cm^{-3}]
n_{i}	Intrinsic carrier concentration of silicon [cm^{-3}]
N_{QFB}	Back fixed charge density [cm^{-2}]
N_{QFF}	Front fixed charge density [cm^{-2}]
P	Dissipated device power [W]
q_0	Inversion channel charge density at the source end of the channel ($y = 0$) [$\mathrm{C/m}^2$]
Q_{Bdep}	Body depletion charge under front gate oxide [C]
Q_{Binv}	Drift region inversion charge under front gate oxide [C]
Q_{B}	Total body charge [C]
q_{b}	Body depletion charge density under the front gate [$\mathrm{C/m}^2$]
$q_{\mathrm{b}}^{\mathrm{dr}}$	Free bulk charge density in the drift region [$\mathrm{C/m}^2$]
q_{cacclim}	Expression for limited q_{cacc} used in Q_{Swdlim} [$\mathrm{C/m}^2$]
q_{cacc}	Drift region accumulation channel charge density [$\mathrm{C/m}^2$]
Q_{CHacc}	Total accumulation channel charge [C]
Q_{CHinv}	Total inversion channel charge [C]
Q_{CH}	Total channel charge [C]
q_{cinvlim}	Expression for limited q_{cinv} used in Q_{Swdlim} [$\mathrm{C/m}^2$]
q_{cinv}	Inversion channel charge density [$\mathrm{C/m}^2$]
$q_{\mathrm{cinv}}^{\mathrm{dr}}$	Drift region inversion charge density under the front gate [$\mathrm{C/m}^2$]
Q_{Ddep}	Drift depletion charge under front gate oxide [C]
$q_{\mathrm{depdi}}^{\mathrm{dr}}$	$q_{\mathrm{dep}}^{\mathrm{dr}}$ at $y = L_{\mathrm{tot}}$ [$\mathrm{C/m}^2$]
$q_{\mathrm{depL}}^{\mathrm{dr}}$	$q_{\mathrm{dep}}^{\mathrm{dr}}$ at $y = L_{\mathrm{eff}}^{+}$ [$\mathrm{C/m}^2$]

$q_{\rm dep}^{\rm dr}$	Drift depletion charge density under the front gate [C/m^2]
$Q_{\rm Diwd}$	$Q_{\rm Di}$ as predicted by the Ward and Dutton partitioning scheme [C]
$Q_{\rm Di}$	Total internal drain charge[C]
$q_{\rm di}$	Accumulation Channel charge density at the internal drain ($y = L_{\rm tot}$) [C/m^2]
$Q_{\rm Dwd}^{\rm MOS}$	Drain charge as predicted by the Ward and Dutton partitioning scheme in a MOSFET [C]
$Q_{\rm Gf}$	Total front gate charge [C]
$q_{\rm Lacc}$	Accumulation Channel charge density at $y = L_{\rm eff}^{+}$ [C/m^2]
$q_{\rm Llim}$	Expression for limited $q_{\rm L}$ used in $Q_{\rm Swdlim}$ [C/m^2]
$q_{\rm Lmin}$	Inversion Channel charge density at $y = L_{\rm min}$ [C/m^2]
$q_{\rm L}$	Inversion Channel charge density at the body-drain junction ($y = L_{\rm eff}$) [C/m^2]
$Q_{\rm Swdlim}$	Extra charge added to $Q_{\rm Dwd}$ ($Q_{\rm D} = Q_{\rm Dwd} + Q_{\rm Swdlim}$ [C]
$Q_{\rm Swd}$	$Q_{\rm S}$ as predicted by the Ward and Dutton partitioning scheme [C]
$Q_{\rm Swd}^{\rm MOS}$	Source charge as predicted by the Ward and Dutton partitioning scheme in a MOSFET [C]
$Q_{\rm S}$	Total source charge [C]
$R_{\rm D}$	Drain series resistance [Ω]
$R_{\rm ON}$	ON resistance in the drift region under the thin gate oxide [Ω/square]
$R_{\rm ON}^{\rm dr}$	ON resistance in the drift region under the field oxide [Ω/square]
$R_{\rm shdr}$	Sheet resistance in the drift region under the field oxide [Ω/square]
$R_{\rm S}$	Source series resistance [Ω]
$R_{\rm T}$	Thermal resistance [K/W]
$T_{\rm amb}$	Ambient temperature [^{o}C]
$t_{\rm bdr}$	Silicon film thickness in the drift region (under LOCOS) [m]
$t_{\rm b}$	Silicon film thickness [m]
$T_{\rm nom}$	Parameter measurement temperature [^{o}C]
$t_{\rm ob}$	Buried oxide thickness [m]
$t_{\rm of}$	Front gate oxide thickness [m]
$V_{\rm BS}$	Body bias with respect to the source [V]
$V_{\rm b}$	Breakdown voltage [V]
$V_{\rm DBst}$	Drain bias with respect to the body limited to $V_{\rm Psat}$ [V]
$V_{\rm DBs}$	Drain bias with respect to the body including pinch-off and velocity saturation in the drift region [V]
$V_{\rm DB}$	Drain bias with respect to the body [V]
$V_{\rm DDi}$	Drain bias with respect to the internal drain [V]
$V_{\rm DiBs}$	Internal drain bias with respect to the body limited to $V_{\rm Psat}$ [V]
$V_{\rm DiB}$	Internal drain bias with respect to the body [V]
$V_{\rm DiSn}$	Internal drain bias with respect to the source limited to $V_{\rm dsat}$ [V]

V_{DiS}	Internal drain bias with respect to the source [V]
V_{dsat}	Internal drain-source saturation voltage [V]
V_{DS}	Drain bias with respect to the source [V]
$V_{\mathrm{FB}}^{\mathrm{bdr}}$	Flat band voltage between the substrate and the drift region [V]
$V_{\mathrm{FB}}^{\mathrm{b}}$	Flat band voltage between the substrate and the body [V]
$V_{\mathrm{FB}}^{\mathrm{fdr}}$	Flat band voltage between the poly silicon gate and the drift region [V]
$V_{\mathrm{FB}}^{\mathrm{f}}$	Flat band voltage between the poly silicon gate and the body [V]
V_{GbB}	Back gate bias with respect to the body [V]
V_{GbS}	Back gate bias with respect to the source [V]
V_{GfB}	Front gate bias with respect to the body [V]
V_{GfS}	Front gate bias with respect to the source [V]
V_{Pdep}	Drift region pinch-off voltage under zero bias conditions [V]
V_{Psat}	Drift region pinch-off voltage [V]
V_{P}	Fitting parameter (second CLM model) [V]
V_{satdep}	Expression for V_{Psat} without inversion at the buried oxide [V]
v_{satdr}	Drift region saturation velocity [cm/s]
V_{satinv}	Expression for V_{Psat} with inversion at the buried oxide [V]
v_{sat}	Saturation velocity [cm/s]
V_{sat}^{*}	Drain-body saturation voltage due to velocity saturation in the drift region [V]
V_{th0}	Front gate threshold voltage at the source end of the body [V]
$V_{\mathrm{th0}}^{\mathrm{bdr}}$	Back gate threshold voltage for the drift region [V]
$V_{\mathrm{th0}}^{\mathrm{b}}$	Back gate threshold voltage for the body [V]
$V_{\mathrm{th0}}^{\mathrm{fdr}}$	Front gate threshold voltage for the drift region [V]
V_{thL}	Front gate threshold voltage at the drain end of the body [V]
W	Transistor width [m]
W_{D}	Drain width [m]
W_{S}	Source width [m]
X_{ddb}	Depletion layer width at the body side of the drain-body junction [m]
X_{ddd}	Depletion layer width at the drain side of the drain-body junction [m]
X_{gbdr}	Depletion layer width at the buried oxide in the drift region [m]
X_{gfb}	Depletion layer width under the front gate in the body [m]
X_{gfdr}	Depletion layer width under the front gate in the drift region [m]
X_{sd}	Depletion layer width under the source [m]

List of Acronyms

BESOI	Bond and Etch-back Silicon-On-Insulator
BJT	Bipolar Junction Transistor
CLM	Channel Length Modulation
CMOS	Complementary Metal–Oxide–Semiconductor (technology)
COMFET	Conductivity Modulated Field Effect Transistor
DIBL	Drain Induced Barrier Lowering
DMOS	Double Diffused MOS
DUT	Device Under Test
FD	Fully Depleted
FET	Field Effect Transistor
GIDL	Gate Induced Drain Leakage
HPIB	Hewlett Packard Interface Bus
HV	High Voltage
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
JFET	Junction Field Effect Transistor
JUNCAP	PHILIPS junction model
LDMOS	Lateral Double Diffused MOS
LOCOS	Local Oxidation of Silicon
LPCVD	Low Pressure Chemical Vapour Deposition
LV	Low Voltage
MCT	MOS Controlled Thyristor
M30.02	PHILIPS Depletion mode MOSFET
MM9.02	MOS Model 9.02 (recent Philips MOS model)
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MV	Medium Voltage
PD	Partially Depleted
PIC	Power Integrated Circuit
PSTAR	PHILIPS circuit simulator
RESURF	REduced SURFace field
SIMOX	Separation by Implanted Oxygen
SOI	Silicon-On-Insulator
SOS	Silicon-On-Sapphire
SMU	Stimulus–Measurement Unit
STAG	Southampton Thermal AnaloGue (SOI MOSFET SPICE model)
TEM	Transmission Electron Microscope
VDMOS	Vertical Double Diffused MOS
VLSI	Very Large Scale Integration
VMOS	V-groove DMOS

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Chapter 1

Introduction

1.1 History of Power Devices

In the late 1940s, research developments made the first steps towards what is today's semiconductor industry [1], [2]. In 1954, the first commercially available silicon bipolar transistors were announced, but it was not until the 1960s that their application to high power devices began. We find the real beginning of the power transistor business with the introduction of the planar process, and the application of photo-lithography to wafer processing [3]. The main advantages of the bipolar technology were the simple manufacturing process (complete double diffusion technology with high yield and low cost) and the low on-resistance due to minority carrier current. The main drawbacks were the low switching speed, the need for a high base current to control the device, and the secondary breakdown [4]. Nowadays bipolar devices with current handling capabilities of several hundred amperes, and blocking voltages of the order of kV's are fabricated.

In the late 1970s, as MOS-IC technology became more mature [5], the first power MOS transistors appeared, and, since then development has accelerated, moving away from the bipolar transistor. The primary feature of the power MOSFET is a high input impedance, which greatly simplifies the gate drive circuitry and reduces the cost of the power electronics. They can withstand the simultaneous application of high voltage and high current without showing any secondary breakdown.

In addition to the new discrete devices, monolithic high voltage ICs (HVIC) which have a high supply voltage but a low output current, and combine power and control circuitry on the same chip, have come onto the scene. This has allowed cost efficiency in the power industry for the first time. Applications have been found in the areas of telecommunications, power supplies, high voltage displays, etc. More recently power ICs (PIC), which use both high voltage and high current circuitry, have been developed.

Smart PICs, where different power device functions are combined with logic functions on the same chip, is a fast growing branch in industry for applications in television, automobiles, aircraft, motors, lighting, audio equipment, switching devices, etc [6]. They offer substantial improvements in performance, and the cost price is lower than the price

of the separate packages connected together.

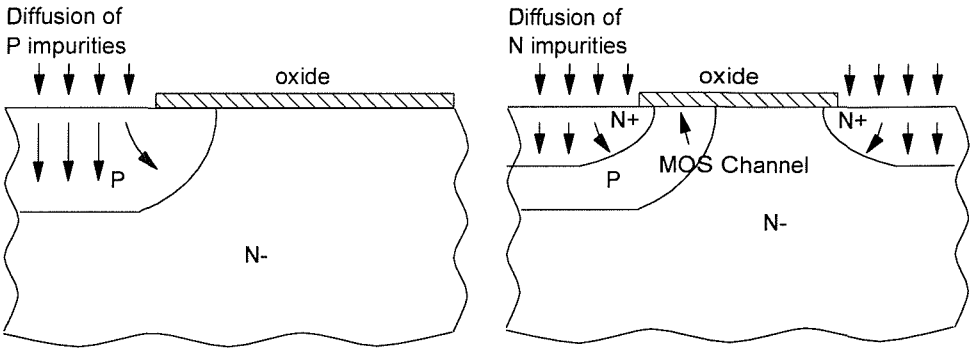

Figure 1.1: The Double Diffused MOS process

The rapid growth of the PIC industry was made possible by the arrival of the DMOS transistor [7–10] (double diffused transistor). The channel of the device is created by the sequential diffusion of two different doping impurities under the gate, as illustrated in Fig. 1.1. The P-base is driven in deeper than the N^+ source, and the difference in the lateral diffusion between the P-base and the N^+ source regions defines the surface channel region. When these double diffusion techniques were developed in the 1970s, they were used to obtain what at the time were very short channel lengths (1-3 μm).

A major change compared with the basic MOSFET structure has been the incorporation of a lightly doped drift region between the channel and the heavily doped drain [11]. The main advantages of the DMOS include the absence of secondary breakdown, negligible steady-state input current, and fast switching. The main drawback compared with the bipolar range is the increased on-resistance with increasing blocking capability.

At present, a whole range of different DMOS structures exist, but we can split them into three main categories, which are illustrated in Fig. 1.2: the VDMOS (Vertical DMOS),the LDMOS (Lateral DMOS) and the VMOS (V-groove DMOS).

The VDMOS and the LDMOS depend upon lateral diffusion profiles and sequential diffusions under the same oxide to achieve the channel region, while the channel of the VMOS derives from the vertical diffusion profile. The choice of a $< 100 >$ material for the LDMOS and VDMOS increases the electron inversion layer mobility and scattering-limited velocity, in contrast to the VMOS, which has its channel along an etched $< 111 >$ surface. The initial focus on VMOS transistors was based on the belief that they had a lower resistance than VDMOS devices. However, research pointed out that the existence

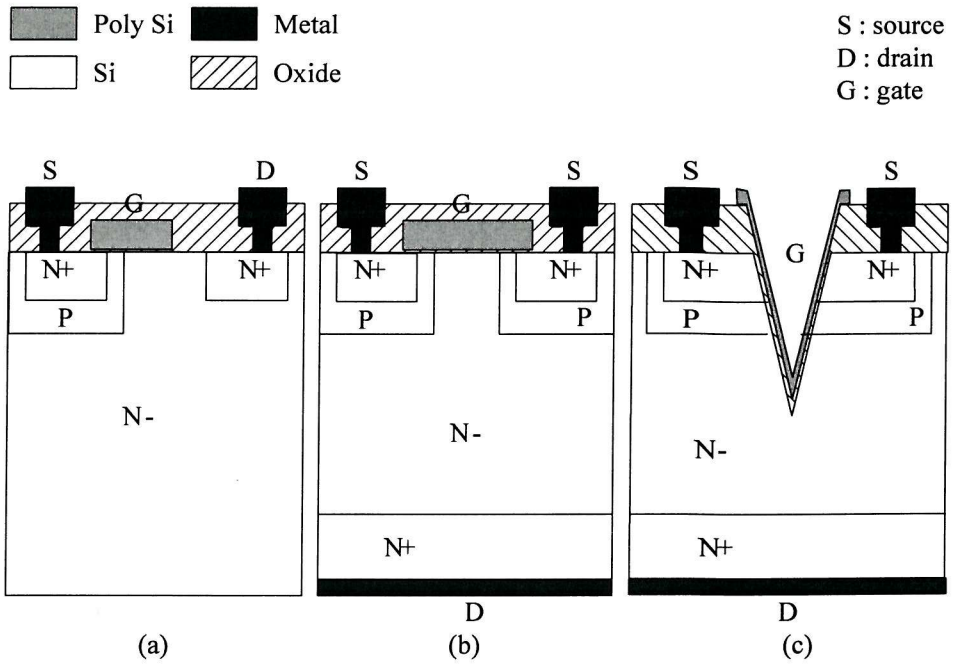

Figure 1.2: (a) LDMOS; (b) VDMOS; (c) VMOS.

of a high electric field at the bottom of the V-groves results in a significant reduction of the breakdown voltage, and the VMOS idea became less popular.

The VDMOS has its drain contact at the bottom of the silicon substrate, which limits its integration capability with other components, but allows a higher packing density. The LDMOS is a lateral device and is therefore a lot better suited for integrating high voltage, moderate current switches with low voltage control circuits. Due to lower parasitic capacitances, and hence faster switching, the LDMOS is more attractive than the VDMOS [12].

The LDMOS devices have significant advantages compared to their bipolar and GaAs counterparts for all applications in the 1GHz range, where linearity and efficiency are required. This makes them suitable for wireless communication applications like GSM [13, 14].

The IGBT (Insulated Gate Bipolar Transistor), also called COMFET (Conductivity Modulated Field-Effect Transistor), and the MOS gated thyristor combine the advantages of MOS with the minority carrier enhanced current capability of bipolar devices, thus also giving low on-resistance. The switching speed will be degraded in such devices [4, 15, 16], although it can be adjusted by lifetime control processes [17].

One of the major aspects of smart power ICs is the isolation problem; smart power development started with junction isolated techniques. However, these suffer from several problems such as latch-up and high leakage current. Dielectric insulation is a much better solution. We can distinguish three methods:

- V groove etching, polysilicon filling, lapping of the crystalline silicon [6].

- wafer bonding, lapping and etch-back.
- SIMOX (Silicon Isolated by iMplanted OXygen)

These last two techniques both give rise to SOI structures. This technology will be explained in more detail in Sec 1.2.

Another very important consideration is the heat generation in PICs. Not only do many power ICs have to function in a high temperature environment, but, due to the large currents and high biasing, a lot of heat is generated within the devices themselves, which decreases the performance of the devices and needs accurate modelling.

Recently new high voltage devices suitable for PICs, based on a partial isolation SOI technique, have been proposed. The advantage of a partial isolation is an enhanced breakdown capability and a better heat dissipation [18] compared with normal SOI.

In this thesis we will study and model the LDMOS and its associated low voltage control components. The transistors are made in an HV (High Voltage) SOI (Silicon-on-Insulator) technology, which will be explained in Sec. 1.2. The reason why this technology is preferred to an ordinary bulk technology for smart power applications will be discussed in Section 1.3.

1.2 Silicon-On-Insulator Technology

In MOS transistors produced in a bulk technology, only the upper part of the silicon substrate is useful; the rest only causes parasitic effects and degrades the operation of the transistor. Hence the idea to separate the substrate from the active part by an oxide layer, and so the SOI-transistor appeared [19]. The two main technologies to produce SOI structures are SIMOX and BESOI (Bonded and Etch-back SOI).

The SIMOX technique realises the buried oxide by an implantation of oxygen ions. This step is followed by thermal annealing to repair the crystalline quality of the silicon layer and to eliminate the defects and precipitates that coexist on the Si/SiO_2 interfaces. During the implant, dislocations, which are not eliminated by thermal annealing, are created. To avoid these anomalies, a series of implants with reduced dose are performed, each of them followed by annealing. This technique is mostly used for radiation-hard and VLSI applications where it is important to have a thin film silicon layer.

The BESOI technique involves growing an oxide on silicon wafers, then two such wafers are bonded together (by the Van der Waals forces) and annealed to strengthen the bonding. One of the wafers is etched or polished down to a thickness suitable for the application considered, and the other wafer serves as a mechanical substrate. This is the most common technique for producing smart power, power, HV and bipolar devices. These applications require partially depleted devices and do not need a very thin silicon film thickness.

Recently, a new interesting method similar to BESOI (as far as the bonding is concerned) has been developed to make thin film SOI wafers. The process is called Smart Cut and was invented at LETI, Grenoble, France [20]. Hydrogen ions are implanted into the

body of a mono-crystalline silicon wafer. Because all the ions have similar energy, they stop at the same distance below the surface. The implantation results in the formation of micro-bubbles, which creates a plane of weakness. The wafer is bonded to another wafer (just as for the BESOI technique), and put into a furnace, which causes cleaving of the first wafer along the weakened plane. With this process film thicknesses as small as 200 nm can be realised.

1.3 SOI versus Bulk for High Voltage and Power IC Applications

The foremost difficulty in the realisation of smart power devices is the need to isolate circuit sections working at very different voltage levels. SOI offers a far better isolation scheme compared with bulk [21], as is clearly visible in Fig. 1.3, where the same typical PIC structure is shown for bulk and SOI. The buried oxide provides perfect horizontal isolation, but one also needs a method of isolating each device laterally. A thin SOI film can simply be etched of (mesa etch) or consumed by LOCOS (Local Oxidation of Silicon). However, for thick films deep narrow trenches are used; these are made by plasma etching, followed by oxide and polysilicon deposition [4].

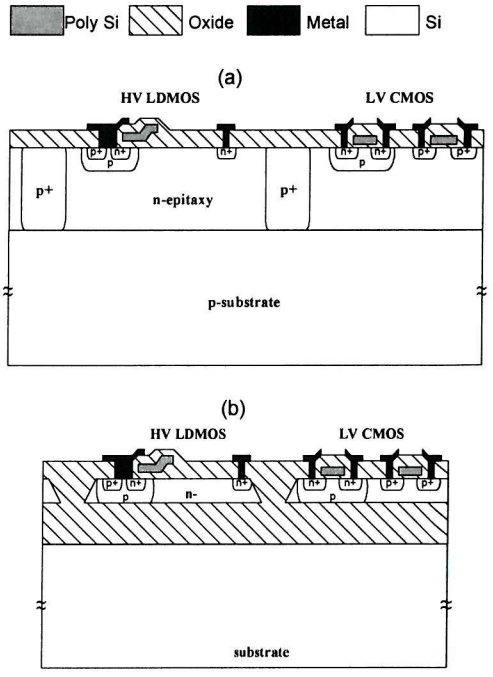

Figure 1.3: High voltage LDMOS and low voltage CMOS in bulk (A) and SOI (B) technology

SOI LDMOS devices will exhibit significantly lower on-resistance for source-high conditions than their bulk counterparts [22]. This will be explained in more detail in the next chapter. We also find diode structures [23], IGBT [19] and LDMOS-IGBT devices [16] that make use of the advantages of SOI.

Apart from this main advantage of SOI, we should notice as well the decrease in parasitic capacitances and the smaller interaction between circuit components, which lead to finer design rules and faster devices.

These benefits have lead to advanced SOI medium voltage ($\cong$ 60 V) and high voltage ($\cong$ 600 V) processes for various applications [24, 25].

1.4 The LDMOS

In this section we describe the typical fabrication process for an LDMOS. Next we look at the characteristics of the LDMOS, as we would expect them based on the analytical solution of the semiconductor equations. The example used is based on the PHILIPS HV SOI process, in which the devices studied and measured in this thesis are fabricated.

1.4.1 The Fabrication Process

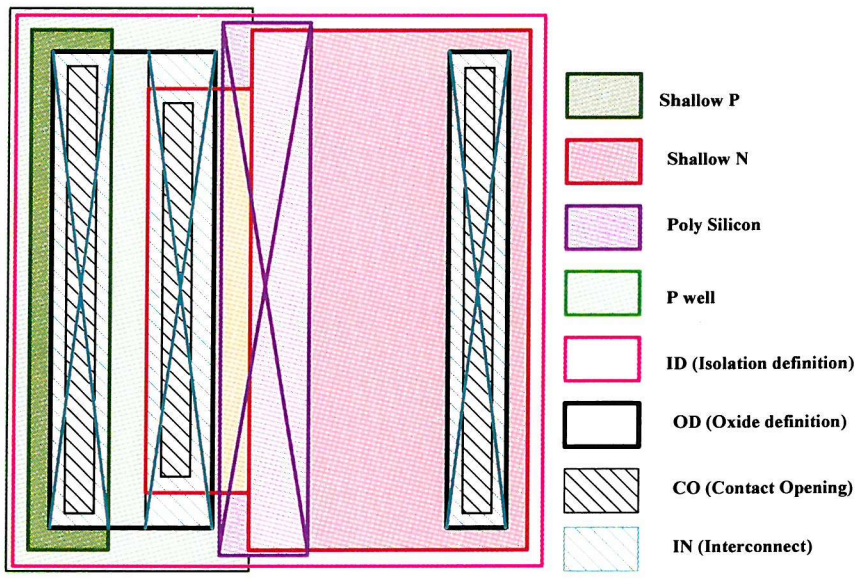

Figure 1.4: The different masks of the LDMOS layout.

The base wafer is a BESOI wafer (see Section 1.2), with a 1.5 μm thick silicon film, on top of a 3 μm thick buried oxide, with an N^+ substrate underneath. The N^- doping concentration of the silicon film is of the order of 10^{16} /cm^3. First an oxide is grown on the wafer, and next it is coated with silicon nitride. The first mask is the active mask (ID mask in Fig. 1.4), which defines the area where the transistor is formed. After the nitride is etched, the wafer is oxidized to produce the *thick LOCOS* (Local Oxidation of Silicon) areas outside the devices. This thick LOCOS oxide touches the buried oxide. Next this oxide is etched until an oxide layer of approximately 1 μm is left on top of the buried oxide. Removing the remaining nitride reveals the active area, in which the transistor will be created.

Now a second *LOCOS* oxidation masked by the OD mask (Oxide definition, see Fig. 1.4) is performed; a second oxide (typically 1 μm) is grown on top of the drift region (between the gate and the drain), to reduce the fringing fields at the edge of the polysilicon for high drain bias. In this thesis, we will use the name LOCOS for this oxide, and thick LOCOS for the oxide which defines the active area.

The following steps are similar to the standard nMOS process: first a thin oxide is grown, then the polysilicon is deposited and etched, masked by the PS-mask (see Fig. 1.4) to form the gate. The gate is typically 5 μm wide, of which typically 2 μm are on top of the LOCOS oxide. Next a lightly doped P-implantation is done in the areas defined by the thick LOCOS edges and the polysilicon gate (P-well mask in Fig. 1.4) and followed by thermal annealing. The P-well diffuses 1.5 μm under the gate and forms the MOS channel region of the LDMOS. The resulting P-well doping concentration is of the order of 10^{17} /cm^3. Now the source and drain N^+ areas (shallow N mask in Fig. 1.4) are implanted, self-aligned on respectively the gate and the LOCOS edge. The lateral diffusion of the source under the gate is typically 0.3 μm. Finally the P^+ area for the body contact is implanted, masked by the shallow P mask.

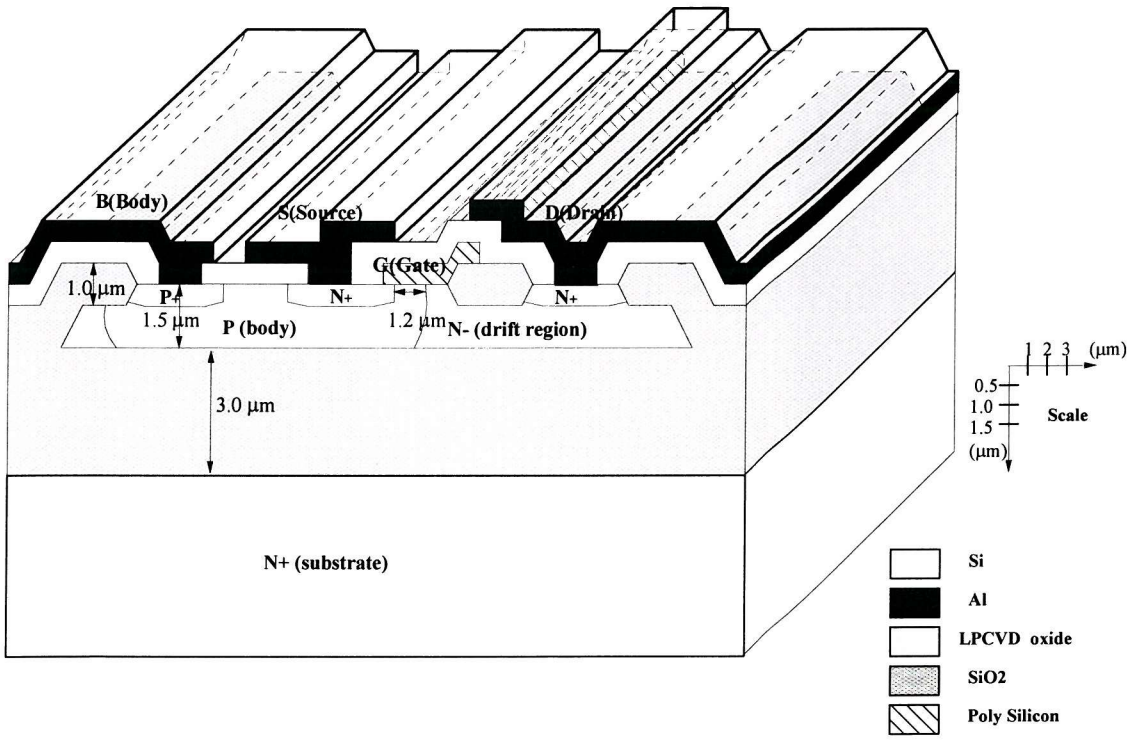

Figure 1.5: Three-dimensional view of the LDMOS.

Now the wafer is covered with a new oxide layer, deposited by an LPCVD (Low Pressure Chemical Vapour Deposition) step. This layer is typically 0.5 μm thick. The

Name	Description	value
N_A	P doping concentration under thin front gate oxide	10^{17} /cm^3
N_D	N^- doping concentration in the drift region	10^{16} /cm^3
R_{shdr}	Sheet resistance of the drift region under the LOCOS oxide	4 kΩ/square

Table 1.1: *The process parameters*

Name	Description	value
L_{dr}	Length of the drift region under LOCOS	3 μm
L_{eff}	Length of the MOS channel under thin front gate oxide	1.2 μm
L_{drov}	Length of the drift region under thin front gate oxide	1.5 μm
t_{of}	Front gate oxide thickness	60 nm
t_{ob}	Back gate (buried) oxide thickness	3 μm

Table 1.2: *The geometry parameters*

CO (Contact) mask (see Fig. 1.4) is then used to define the contact holes in this layer. Following this, the metal is deposited by means of sputtering. The METAL mask (IN mask in Fig. 1.4) defines the pattern in the aluminium layer.

As a final step the wafer is covered with a passivation layer to protect the integrated circuit from external influences. The complete three-dimensional structure is represented in Fig. 1.5.

1.4.2 The LDMOS Characteristics

This section describes qualitatively the LDMOS behaviour. As an introduction to how this device functions, how the current flows, and how the charges are distributed under different operating conditions, we perform a simplified analysis based on fundamental semiconductor physics equations.

Tables 1.1, 1.2 and 1.3 respectively list typical values for process, geometry and derived parameters [26], which are used for the analysis below:

- For the bias arrangement where all the terminals are at ground potential ($V_{DB} = V_{SB} = V_{GfB} = V_{GbB} = 0$ V), the situation illustrated in Fig. 1.6(a) is obtained. The width of the depletion layer X_{sd} under the source can be approximated (assuming an abrupt junction) by

$$X_{sd} = \sqrt{\frac{2\,\epsilon_{si}}{q\,N_A}(\phi_{bis} - V_{BS})} \tag{1.1}$$

  For $V_{SB} = 0$ V this width is equal to 0.1 μm.

  The width of the depletion layer X_{ddb} at the P-side of the P-N^- junction can be

Name	Description	value
ϕ_{F}	Fermi-potential for P-type Si, $\frac{kT}{q}ln(\frac{N_{\mathrm{A}}}{n_i})$	0.408 V
ϕ_{Fdr}	Fermi-potential for N-type Si, $\frac{kT}{q}ln(\frac{N_{\mathrm{D}}}{n_i})$	0.34 V
$V_{\mathrm{FB}}^{\mathrm{f}}$	Flatband voltage, N-type poly Si on P-type Si $-0.56\ V - \phi_{\mathrm{F}}$	-0.996 V
$V_{\mathrm{FB}}^{\mathrm{fdr}}$	Flatband voltage, N-type poly Si on N-type Si $-0.56\ V + \phi_{\mathrm{Fdr}}$	-0.212 V
$V_{\mathrm{FB}}^{\mathrm{b}}$	Flatband voltage, N^+ substrate, P-type Si $-0.45\ V - \phi_{\mathrm{F}}$	-0.858 V
$V_{\mathrm{FB}}^{\mathrm{bdr}}$	Flatband voltage, N^+ substrate, N-type Si $-0.45\ V + \phi_{\mathrm{Fdr}}$	-0.11 V
γ_0	Front gate body factor in P-well, $\frac{\sqrt{2q\epsilon_{\mathrm{si}}N_{\mathrm{A}}}}{C_{\mathrm{of}}}$	3.2 $\sqrt{\mathrm{V}}$
γ^{b}	Back gate body factor in P-well, $\frac{\sqrt{2q\epsilon_{\mathrm{si}}N_{\mathrm{A}}}}{C_{\mathrm{ob}}}$	159.6 $\sqrt{\mathrm{V}}$
γ^{fdr}	Front gate body factor in N-well, $\frac{\sqrt{2q\epsilon_{\mathrm{si}}N_{\mathrm{D}}}}{C_{\mathrm{of}}}$	1.01 $\sqrt{\mathrm{V}}$
γ^{bdr}	Back gate body factor in N-well, $\frac{\sqrt{2q\epsilon_{\mathrm{si}}N_{\mathrm{D}}}}{C_{\mathrm{ob}}}$	50.48 $\sqrt{\mathrm{V}}$
V_{th0}	Front gate threshold voltage in P-well $V_{\mathrm{FB}}^{\mathrm{f}} + 2\phi_{\mathrm{F}} + \gamma_0\sqrt{2\phi_{\mathrm{F}}}$	2.73 V
$V_{\mathrm{th0}}^{\mathrm{b}}$	Back gate threshold voltage in P-well $V_{\mathrm{FB}}^{\mathrm{b}} + 2\phi_{\mathrm{F}} + \gamma^{\mathrm{b}}\sqrt{2\phi_{\mathrm{F}}}$	144 V
$V_{\mathrm{th0}}^{\mathrm{fdr}}$	Front gate threshold voltage in N-well $V_{\mathrm{FB}}^{\mathrm{f}} - 2\phi_{\mathrm{Fdr}} - \gamma^{\mathrm{fdr}}\sqrt{2\phi_{\mathrm{Fdr}}}$	-1.75 V
$V_{\mathrm{th0}}^{\mathrm{bdr}}$	Back gate threshold voltage in N-well $V_{\mathrm{FB}}^{\mathrm{b}} - 2\phi_{\mathrm{Fdr}} - \gamma^{\mathrm{bdr}}\sqrt{2\phi_{\mathrm{Fdr}}}$	-42.99 V
ϕ_{bis}	Build-in potential for S-B diode, $\frac{kT}{q}ln(\frac{N_{\mathrm{A}}N^+}{n_i^2})$	0.875 V
ϕ_{bid}	Build-in potential for D-B diode, $\frac{kT}{q}ln(\frac{N_{\mathrm{A}}N_{\mathrm{D}}}{n_i^2})$	0.756 V
C_{of}	Front gate oxide capacitance per unit area, $C_{\mathrm{of}} = \frac{\epsilon_{ox}}{t_{\mathrm{of}}}$	0.575 fF/μm^2
C_{ob}	Back gate oxide capacitance per unit area, $C_{\mathrm{ob}} = \frac{\epsilon_{ox}}{t_{\mathrm{ob}}}$	0.0115 fF/μm^2

Table 1.3: *The derived parameters*

expressed by

$$X_{\mathrm{ddb}} = \sqrt{\frac{2\epsilon_{\mathrm{si}}N_{\mathrm{D}}}{qN_{\mathrm{A}}(N_{\mathrm{A}}+N_{\mathrm{D}})}(\phi_{\mathrm{bid}} + V_{\mathrm{DB}})} \tag{1.2}$$

This width is negligible for $V_{\mathrm{DB}} = 0$ V (0.03 μm) since N_{A} is an order of magnitude larger than N_{D}. The width of the depletion layer X_{ddd} at the N-side of the P-N^- junction can be expressed by

$$X_{\mathrm{ddd}} = \sqrt{\frac{2\ \epsilon_{\mathrm{si}}\ N_{\mathrm{A}}}{q\ N_{\mathrm{D}}(N_{\mathrm{A}}+N_{\mathrm{D}})}(\phi_{\mathrm{bid}} + V_{\mathrm{DB}})} \tag{1.3}$$

This gives a value of 0.3 μm for $V_{\mathrm{DB}} = 0$ V.

Because $V_{\mathrm{GfB}} = 0\ \mathrm{V} > V_{\mathrm{FB}}^{\mathrm{f}}$, we have a depletion layer in the P-body under the front gate oxide (region 1 in Fig. 1.6(a)). And since $V_{\mathrm{GfS}} = 0\ \mathrm{V} < V_{\mathrm{th0}}$, the Si-$SiO_2$ surface

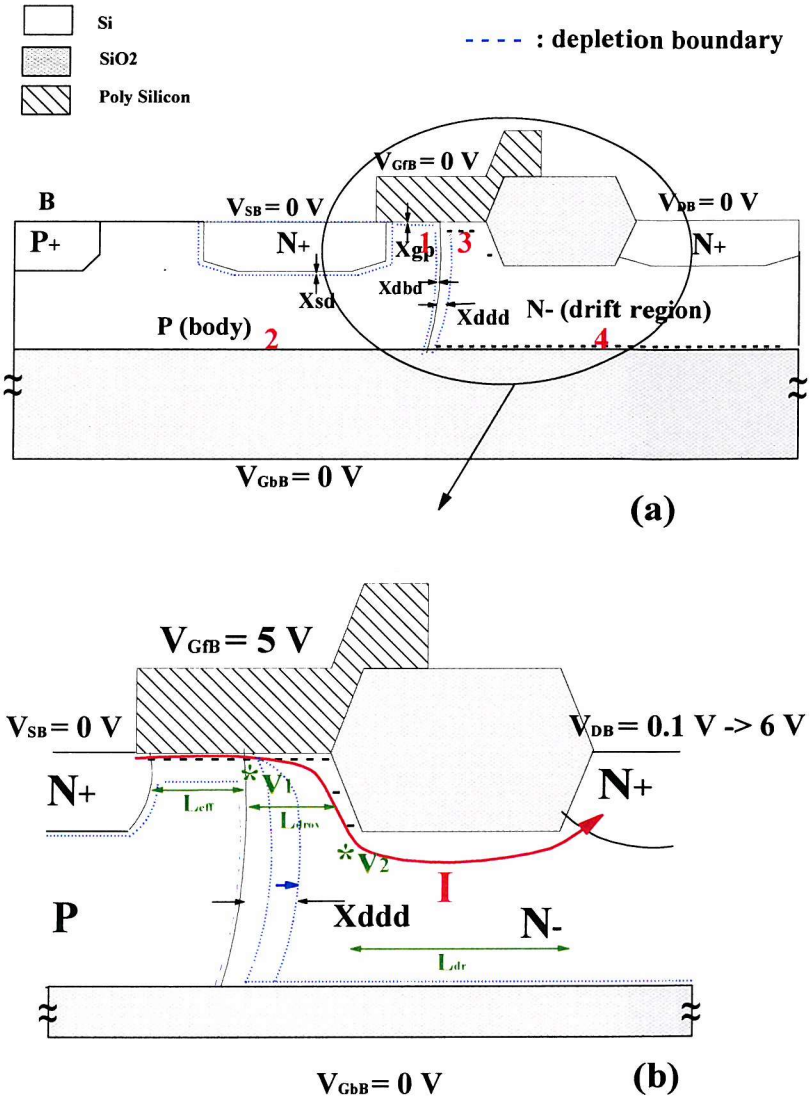

Figure 1.6: (a) Depletion layers and accumulation in the LDMOS when $V_{\mathrm{DB}} = V_{\mathrm{SB}} = V_{\mathrm{GfB}} = V_{\mathrm{GbB}} = 0$ V; (b) current flow and depletion, accumulation and inversion layer when $V_{\mathrm{DB}} = 0.1$ V $->$ 6 V, $V_{\mathrm{GfB}} = 5$ V, $V_{\mathrm{SB}} = 0$ V, $V_{\mathrm{GbB}} = 0$ V.

is not yet inverted. The width of the depletion layer, which we will call X_{gfb}, can be approximated before inversion by

$$X_{\mathrm{gfb}} = \frac{C_{\mathrm{of}}}{q\, N_{\mathrm{A}}}(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}}) \tag{1.4}$$

For $V_{\mathrm{GfB}} = 0$ V this value is very small (0.035 μm). A similar reasoning is valid for the depletion layer at the buried oxide interface in the P-body (region 2 in Fig. 1.6(a)), but this value will be even smaller because C_{ob}, the buried oxide capacitance per unit area, is 50 times smaller than C_{of}.

Let us now take a closer look at the conditions under the gate oxide in the drift

region (region 3 in Fig. 1.6(a)). We have an oxide on an N^- region (cf. a PMOS device), so we have to invert the signs, compared to the nMOS case; $-V_{\mathrm{GfD}} = 0$ V $< -V_{\mathrm{FB}}^{\mathrm{fdr}}$, and hence electrons will be accumulated at the N^- silicon surface under the gate. A similar analysis can be done for the back gate, and we will also have an accumulation layer at the silicon surface above the buried oxide.

- Applying a positive gate bias (higher than the threshold voltage given by V_{th0}) will invert the P-surface under the front gate and accumulate more electrons in the drift region under the front gate. This is illustrated in Fig. 1.6(b), where the situation when $V_{\mathrm{GfS}} = 5$ V is shown. If the drain voltage is also increased, current starts to flow; it passes from the source into the inversion layer, then primarily into the accumulation layer, and finally into the drain via the N^- region under the LOCOS oxide. First we will assume that V_{DS} is very small, for example 0.1 V. In this case we can write the following simplified equations for respectively the current in the inversion layer, in the accumulation layer and in the drift region:

$$I_{\mathrm{inv}} = \frac{W}{L_{\mathrm{eff}}} \mu_{\mathrm{s}} C_{\mathrm{of}} \cdot (V_{\mathrm{GfS}} - V_{\mathrm{th0}} - \frac{V_1}{2}) V_1 \tag{1.5}$$

$$\cong \frac{W}{L_{\mathrm{eff}}} \mu_{\mathrm{s}} C_{\mathrm{of}} \cdot (V_{\mathrm{GfS}} - V_{\mathrm{th0}}) V_1 \qquad \text{for } V_{\mathrm{DS}} \text{ very small,} \tag{1.6}$$

$$I_{\mathrm{acc}} = \frac{W}{L_{\mathrm{drov}}} \mu_{\mathrm{s}} C_{\mathrm{of}} \cdot (V_{\mathrm{GfS}} - V_{\mathrm{FB}}^{\mathrm{fdr}} - \frac{V_1 + V_2}{2}) \cdot (V_2 - V_1) \tag{1.7}$$

$$\cong \frac{W}{L_{\mathrm{drov}}} \mu_{\mathrm{s}} C_{\mathrm{of}} \cdot (V_{\mathrm{GfS}} - V_{\mathrm{FB}}^{\mathrm{fdr}}) \cdot (V_2 - V_1) \qquad \text{for } V_{\mathrm{DS}} \text{ very small,} \tag{1.8}$$

$$I_{\mathrm{dr}} = \frac{W \cdot (V_{\mathrm{DB}} - V_2)}{R_{\mathrm{shdr}} L_{\mathrm{dr}}} . \tag{1.9}$$

I_{inv} is simply the expression of the MOSFET current in the linear region and V_1 is the potential at the end of the inversion layer (of length L_{eff}) with respect to the source (see Fig. 1.6(b)). I_{acc} represents the current in an accumulation layer (of length L_{drov}), which is the current of a depletion type MOSFET. In this case V_2 is the potential at the end of the accumulation layer with respect to the source (cf. Fig. 1.6(b)). For simplification, we have assumed that the entire current flows through the inversion layer into the accumulation layer, while in reality part of it will flow in the bulk underneath the accumulation layer. In Eqs. 1.5, 1.7 and 1.9 the surface layer mobility for electrons is given by μ_{s}. I_{dr} is the current through a resistor with sheet resistance R_{shdr} and length L_{dr}.

The above equations for the current are simplified, excluding high field and other second order effects, because the aim of this section is to gain an intuitive approximation to the LDMOS behaviour, rather than finding the exact solution for the current flow and charge distribution. Since $I_{\mathrm{inv}} = I_{\mathrm{acc}} = I_{\mathrm{dr}} = I$, we have three equations in three unknowns, which we can solve for V_1, V_2 and I. With the parameters from Tables 1.1, 1.2, and 1.3, we obtain $V_1 = 0.4 \cdot V_{\mathrm{DB}}$ and $V_2 = 0.6 \cdot V_{\mathrm{DB}}$.

Increasing V_{DS} raises the current until the saturation region is reached. In the case of a low V_{GfB} (in our example 5 V), saturation is caused by pinch-off of the inversion channel, which happens at $V_1 \cong V_{GfS} - V_{th0} = 2.3$ V; the saturation current is given by

$$I_{invsat} = \frac{W}{2\,L_{eff}} \mu_s C_{of} (V_{GfS} - V_{th0})^2 \tag{1.10}$$

and for $V_{GfS} = 5$ V the current will be approximately 0.1 mA/μm. This means that $V_2 \cong V_{DS} - (L_{dr}\ R_{shdr}) \cdot 0.1$ mA/μm $= V_{DS} - 1.2$ V. For $V_1 = V_{GfS} - V_{th0} = 2.3$ V, Eqs. 1.5 and 1.7 yield $V_2 \cong 3.7$ V. This is lower than $V_{GfS} - V_{FB}^{fdr}$, and hence an accumulation layer is still present over the whole length of L_{drov}.

When $(V_{DS} - 1.2$ V) is larger than $(V_{GfB} - V_{FB}^{fdr})$, the surface in the N^- drift region under the front gate will no longer be completely accumulated, but will become partially depleted. This transition from accumulation to depletion is illustrated in Fig. 1.7. Setting $V_{DB} = 7$ V, V_2 is approximately 5.8 V and the depth of the depletion layer at this place becomes equal to

$$X_{gfdr} = \frac{C_{of}}{qN_D}(-V_{GfB} + V_2 + V_{FB}^{fdr}) = 0.28\ \mu m \tag{1.11}$$

As is obvious from Eq. 1.3, further increasing V_{DS} widens the depletion layer at the P-N^- junction, X_{ddd}. For $V_{DS} = 7$ V we have $V_2 \cong 5.8$ V and $X_{ddd} = 0.9$ μm. At a certain drain bias this depletion layer and the depletion layer under the front gate in the drift region are going to touch. Saturation is now dominated by two phenomena: pinch-off of the inversion MOS channel and pinch-off of the drift region.

For even higher drain biases, the boundary of the depletion layer in the drift region shifts increasingly close to the drain, and the lateral electrical field becomes important. The current is now also limited by velocity saturation of the carriers.

Finally we have a look at the depletion layer width at the buried oxide in the drift region:

$$X_{gbdr} = \frac{C_{ob}}{qN_D}(-V_{GbB} + \psi + V_{FB}^{bdr}) \tag{1.12}$$

where ψ is the potential at position y in the drift region. The quantity ψ is at a maximum at the drain $(= V_{DiB})$, and consequently the thickness of the depletion layer is also a maximum at this point. For $V_{DB} = 40$ V, which is approximately the maximum drain voltage for a device with our selected dimensions, we have $X_{gbdr} = 0.3$ μm.

- Now we consider the case of a high positive gate bias, i.e. $V_{GfB} = 16$ V, which in our example is the maximum allowed gate bias for oxide breakdown. This time the inversion layer will not pinch off. Assuming that V_1 became higher than $V_{GfS} - V_{th0} = 13.27$ V, then the current would have to equal the saturation current of 3.2 mA/μm for $V_{GfB} = 16$ V. This would mean that, for the maximum allowed drain

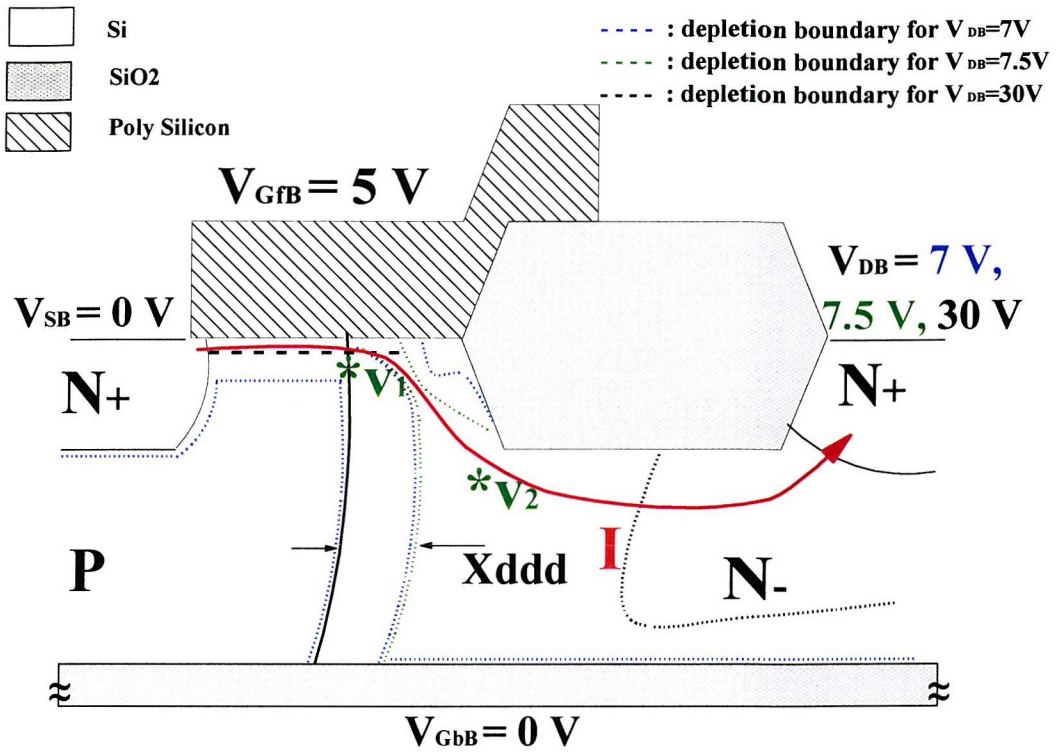

Figure 1.7: Depletion layers and current flow in the LDMOS when $V_{\mathrm{DB}} = 7$ V, 7.5 V, 30 V, $V_{\mathrm{GfB}} = 5$ V, $V_{\mathrm{SB}} = 0$ V, $V_{\mathrm{GbB}} = 0$ V.

bias $V_{\mathrm{DS}} = 40$ V , $V_2 = 40$ V $-3.2 \cdot 4 \cdot 3$ V $= 2$ V, which is lower than V_1, and hence impossible. The accumulation layer will not disappear either; for $V_2 > 16$ V $- V_{\mathrm{FB}}^{\mathrm{fdr}}$, Eqs. 1.5 and 1.7 do not provide a valid solution for V_1, and hence V_2 has to be lower than 16 V $- V_{\mathrm{FB}}^{\mathrm{fdr}}$.

For this situation, the current will be limited by velocity saturation in the drift region when the drain bias is increased.

- When an LDMOS is used in high side switching applications, high voltages can appear across the back oxide. This leads to an increased resistance of the N^- region under the LOCOS. The source-high condition with grounded back gate is equivalent to a negative back gate voltage and a grounded source. Fig. 1.8 illustrates the effect of a negative back gate voltage. As V_{GbS} is made increasingly negative, the depletion layer at the buried oxide in the drift region grows, causing an increase in the drift region resistance. This effect continues until the Si/SiO_2 surface at the buried oxide becomes inverted. The threshold for inversion at a certain point in the channel depends on the local channel potential ψ, and is given by

$$V_{\mathrm{th0}}^{\mathrm{bdr}} = V_{\mathrm{FB}}^{\mathrm{b}} - 2\phi_{\mathrm{F}} - \gamma^{\mathrm{bdr}}\sqrt{2\phi_{\mathrm{F}} + \psi} \tag{1.13}$$

At the drain end of the channel, we obtain $V_{\mathrm{th0}}^{\mathrm{bdr}} = -166$ V for $V_{\mathrm{DB}} = 10$ V. Decreasing the back gate bias below $V_{\mathrm{th0}}^{\mathrm{bdr}}$ only increases the inversion layer charge, but

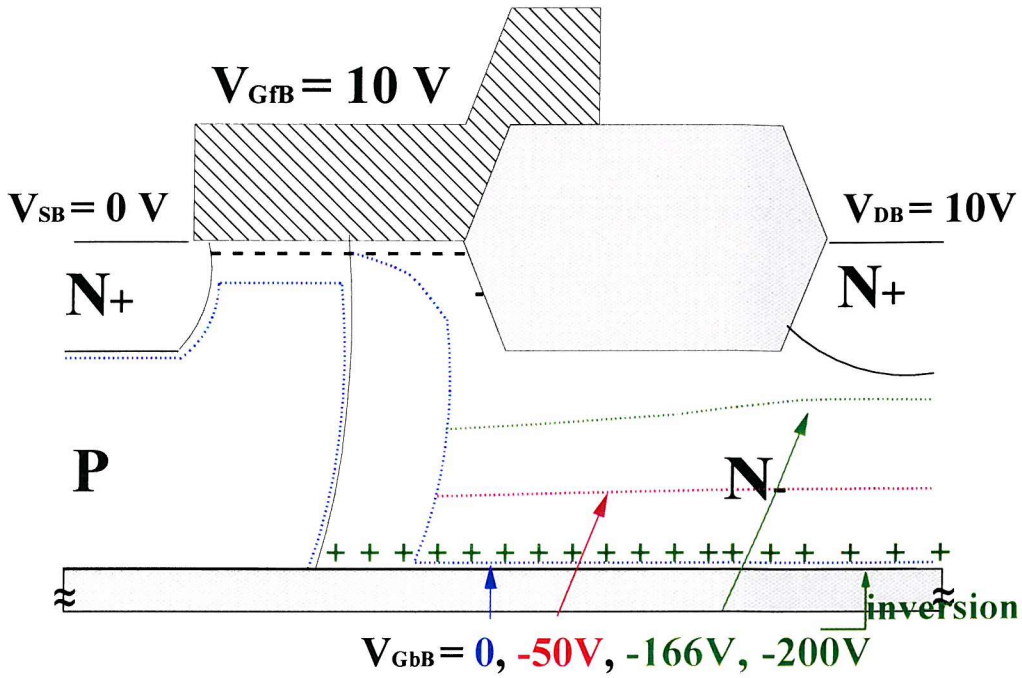

Figure 1.8: Effects of a negative substrate bias.

does not affect the depleted area. The resistance of the drift region is now constant, since the width of the depletion layer is fixed at $\sqrt{\frac{2\epsilon_{si}}{qN_D}(2\phi_F + \psi)}$. At the drain end, for $V_{DB} = 10$ V, this depletion layer width is 1.2 μm.

These different operation modes show the complexity of the device and the necessity of a thorough physical study of the LDMOS transistor before any modelling is begun. This will be done in Chapter 2.

1.5 Overview of Power Semiconductor Device Modelling for Circuit Simulation

1.5.1 Introduction

The know-how of power device modelling for circuit simulation is rapidly developing towards increasing professionalism and applicability for practical use. New model concepts have been explored to serve the needs of the designers for more efficient models. The challenge in the development of such models is the achievement of the optimal trade-off between the necessary accuracy, the required simulation speed, and the feasibility of parameter extraction.

A variety of commercial circuit simulation programs exist on the market, such as SPICE [27], SABER [28] or ELDO [29]. In addition, a number of proprietary industrial

circuit simulation programs exist, including the PHILIPS circuit simulator, PSTAR [30]. Since SPICE is used world wide, and is informally accepted as the industry standard, the compact LDMOS model reported in this thesis has been implemented in this simulation program. However, in the near future the model will also be available in the PSTAR simulator, as a PHILIPS implementation team is currently working on the transition from the SPICE code to the PSTAR code.

1.5.2 Model Implementation

According to a recent literature overview [31] the following modelling concepts can be distinguished:

- The functional model or "black box" model: the externally observed behaviour is described without considering any of the physics of the device. The application of the resulting model will, however, be rather the complete system simulation and not circuit simulation.

- The approximate solution: the exact physical equations (which are usually very complex) are replaced by an approximate solution in order to limit computation time. This technique is the most promising for future research as it enables practical employment for the design of power electronic circuits with a medium number of components. We explore this technique in Chapters 4 and 5.

- The transformation solution: the Laplace transform or the Green's function is applied and the result is an approximated solution obtained through the truncation of infinite series. However, this technique still suffers from the inability to treat moving boundaries, which are necessary to describe conductivity modulation correctly, for example.

- The lumped model: the charge storing region is subdivided into subsections, each with a node, and the derivative of the charge is replaced by the difference in charge; this approach is useful when describing bipolar effects, where charge storage phenomena are very important. The main application field would be the simulation of power electronic circuits with a large number of components [32–35].

- The numerical solution: this method clearly gives the highest accuracy, but the computational effort will also be the highest. These models will only be used for circuits with a small number of components.

We can distinguish two main methods to implement a model into a circuit simulation program [36]. Firstly there is the *subcircuit method*; a combination of existing fixed functional elements from the library of a certain circuit simulator is used to describe the behaviour of the device. Unfortunately, if accurate modelling is desired, the subcircuit can become very complex (and hence require a lot of computational power). This is because

we have to describe the complex physical equations of the power device, using predefined, possibly inappropriate elements. The great advantage though is that the resulting model can be implemented in nearly every circuit simulator, and that the model can be made within a relatively short time. This modelling approach has been followed in Chapter 3. We have developed an LDMOS model, using existing components of the PSTAR library. The result is indeed quite complex, which not only increases computation time, but can also create convergence problems when the number of components in the circuit becomes very large. On the other hand, this model demanded only modest programming skills and could be made within a relatively short time, which is very useful if designers urgently need a model.

Secondly there is the *mathematical method*, where the possibility of describing the equations in a special description language or program is made available by the circuit simulator. The modelling is usually more accurate, because we have the ability to describe the device physics with whatever equations we find appropriate. But, the use of the model will be restricted to the chosen circuit simulator. In Chapters 4 and 5 the physical equations for the SOI LDMOS are described. They have been implemented in SPICE. The compact modelling approach also offers the possibility to have a smaller computation time and an improved robustness. Ideally, the model should always converge, even without initial guesses made by the designer for the node voltages in the circuit under simulation.

1.5.3 Parameter Extraction

The accuracy of a model also depends on the quality of its parameters and the availability of a systematic extraction procedure. We can distinguish five different parameter classes:

- *technological parameters*, in general available from the device manufacturer,
- *physical parameters* determined by the semiconductor physics,
- *electrical parameters* which can usually be extracted from electrical measurements,
- *thermal parameters*, and
- *fitting parameters* to improve the fit of the model to the measurement.

To extract the parameters from measured device characteristics, we can consider two systematic methods. The first one fits the model to the measurements by changing the parameters. This method, called *parameter optimisation* works in general only for small groups of variable parameters, and it is useful to have a good idea of the initial values of the parameters to be optimised. This procedure is applied in Chapter 3 where we perform an optimisation of a part of the parameter set within ICCAP [37], a software package which is part of HP's EEsof high frequency electronic design automation solutions. ICCAP is used to measure semiconductor device and circuit modelling characteristics, and to analyse the results. We have divided the parameter set into smaller groups, and performed separate optimisations on the appropriate measurements.

The second method is called *Parameter isolation*; each parameter is extracted separately from a chosen characteristic. This method often requires a strong simplification of the model equations.

1.5.4 Existing LDMOS Models

Whilst the modelling of bulk LDMOS devices has received much attention to date, little research work has been done on the particular problems posed by SOI devices. There is a need for a good compact SOI LDMOS model, which includes high-side behaviour, the lateral doping gradient in the channel, the overlap of the gate over the drift region, heating effects and has an accurate, physical charge model.

For a model to be useful, it must be implemented in a circuit simulator, and so in this section we deal only with models which have been published and implemented. The compact models described are all for bulk power devices, since a compact SOI LDMOS model has not been developed before. The main difference with the bulk model is the drift region. For SOI we have a low-doped region on top of a thick oxide, instead of a thick low-doped region on top of a P-type substrate. However, the modelling of the MOS channel part is similar for both technologies.

Many subcircuit models for vertical and lateral bulk DMOS devices have been published, where one or more JFETs are used to describe the drift region [38–40]. Sometimes extra non-linear capacitances are added to describe the overlap of the gate over the lightly doped drift region [41].

The University of Florida has done a lot of research on compact physical modelling of vertical and lateral DMOS devices for IC CAD. Their models take into account the lateral doping gradient (but not in all the equations, see Chapter 4) , the parasitic bipolar action [42], and the JFET action and velocity saturation in the drift region [43]. Both their bulk VDMOS [44] and LDMOS models [45] have been refined (especially the charge model) and implemented in SPICE2g.6.

MOTOROLA also has a physically-based model for the bulk LDMOS [46], which is implemented in their internal simulator MCSPICE. The doping gradient can be accounted for by partitioning the channel into regions of constant doping, which is accurate but increases considerable the computation time. The drift region, and the overlap of the gate over this region are physically modelled, introducing two extra current sources and hence two internal nodes. This approach is likely to lead to larger simulation times.

1.6 Objective of this Work

The objective of this thesis is concerned with the detailed characterisation and modelling of the LDMOS devices in a HV SOI technology. Particular emphasis is placed on the behaviour and circuit level modelling issues related to the high side drive applications, and on the self- and mutual device heating for high voltage linear applications. High side

operation for CMOS implies very large bias values across the back oxide, leading to inversion of the back interface, with consequent leakage and unaccounted charges in switching and class D circuit stages. For the N-type LDMOS, high side operation increases the on-resistance and needs accurate modelling. Self- and coupled heating are also significant, particularly in small signal applications (such as video amplifiers). Other aspects, such as the influence on the charges of the lateral doping gradient in the channel, and the overlap of the gate over the lightly doped drift region, are studied and modelled.

Modelling work is aimed at improving the CAD capability for designers with better dynamic accuracy in a consistent and robust simulation model system. A closed form or compact model has the advantage of simplicity, and aims to predict as accurately as possible the device behaviour with simple mathematics, making it possible to use the formulations in a circuit simulator. Our model is based on a simplified analysis of device physics, so that the parameters have a physical meaning, which benefits the parameter extraction strategy.

The compact modelling approach is compared with the subcircuit approach, which uses a combination of existing components. The latter suffers from a very large parameter set and non-convergence problems; problems which can be overcome by the use of a compact model. On the other hand, putting together a subcircuit model is a lot faster and goes some way to meeting the urgent needs of IC designers for an SOI LDMOS model.

My modelling philosophy is strongly influenced by the compact model for the partially depleted SOI MOSFET, written by M. S. L. Lee [47]. This model, called the STAG model (Southampton Thermal AnaloGue model) includes floating body effects and self-heating effects in both static and dynamic domains. The LDMOS heating effects have been implemented in a similar way to the STAG model, and the SOI LDMOS model is also charge-conserving and surface potential based. It has one internal node, and uses two current expressions, which are both smooth and continuous for all regions of operations. The first current expression describes the LV LDMOS part, including the drift region under the thin oxide, and the second one models the drift region under the field oxide. These two current equations have been matched consistently with the help of limiting procedures and an accurate prediction of the internal node voltage.

One of the main difficulties is the realisation of a good charge model, which has to provide smooth and continuous capacitances and trans-capacitances in all operation regions. The lateral doping gradient and the drift region introduce a very different charge behaviour compared to a standard MOSFET, and we have developed a new unique charge model for the LDMOS.

The results are evaluated by comparison between circuit and device measurements, and simulation data. The model has been implemented in the SPICE3f5 simulator and provides a reliable design path for analogue circuits using a HV SOI DMOS technology.

1.7 Structure of Thesis

Modelling of a transistor demands a full comprehension of the physics of the device. In Chapter 2, we address the particular properties of the LDMOS fabricated in a HV SOI process. The typical structures of these devices are described, and the consequential electrical and thermal behaviour is studied; the unique effects, when the components are used under high side conditions (as in a typical half-bridge configuration, for example) are explained in detail. The P-body of the LDMOS is formed by under-diffusion of a P-well under the gate and hence the doping at the source side will be higher than at the drain side of the MOSFET channel. A new characterisation method for the lateral body doping gradient coefficient is developed. Finally, we discuss the important parameters for thermal behaviour.

Based on the knowledge obtained from the detailed study of the LDMOS in Chapter 2, we can now commence the modelling work. In Chapter 3, a subcircuit model for the LV and MV LDMOS has been developed to meet the needs of PHILIPS' circuit designers engaged in smart power IC design. We use a combination of elements provided by the PSTAR library. The PSTAR library contains different MOS models and JFET models from which we chose the most appropriate ones to describe the behaviour of the LDMOS. The subcircuit modelling approach yielded a "quick-fix" LDMOS model, which can be used in the PSTAR simulator. The model gives good DC agreement with measurements, and reasonable transient and AC results, but has the drawback of complexity and increased computation time. In addition, the doping gradient in the MOSFET channel is not taken into account.

In Chapters 4 and 5 respectively, we develop the DC and AC parts of the compact model to overcome the difficulties of the subcircuit approach. Our model accounts for the most important unique features of the SOI LDMOS; we use two current equations, both of which are smooth and continuous in all regions of operation. The first current expression describes the LV LDMOS part, including the lateral channel doping-density gradient and the overlap of the gate over the drift region. The second expression models the drift region under the field oxide, and includes high side behaviour.

One of the main concerns of a circuit model, especially for a device used in HV circuits, is its robustness, to ensure good convergence for all analysis modes. To make a model robust, smooth and continuous equations are required, and the smoothing functions have to be chosen with great care. The finite representation accuracy of numbers can lead to numerical overflow or underflow, resulting in floating point exceptions. These have to be avoided in all circumstances, and this demands a thorough check of all the equations, and the introduction of contingency measures where needed. Furthermore, the internal node connecting the two current sources has to be predicted accurately at every iteration step. These implementation considerations are treated in Chapter 6.

The model has been tested extensively, both in single device configuration and with circuits. In Chapter 7 we show the results of the single device SEMATECH tests [48],

used as a standard for MOSFET testing. Additional tests, which were found useful in testing convergence, are also presented. Furthermore, some analogue circuits, which caused convergence problems with the subcircuit model, have been successfully simulated with the compact model. These circuits were fabricated in the PHILIPS HV SOI process, and measurements are compared with simulations in this chapter.

The final chapter contains a summary of the achievements of this thesis. A main conclusion is drawn, and advice for possible further work is presented.

App. A shows ATLAS simulation results for the LV and MV LDMOS. App. B lists the parameters of the PHILIPS models used in the LDMOS subcircuit model developed in Chapter 3. App. C gives a complete description of our compact SPICE LDMOS model, including element card, full parameter set and all model equations. Apps. D and E provide detailed mathematical derivation for formulas respectively used in Chapters 4 and 5. In App. F a description of the full set of SEMATECH tests is listed, and the results for different parameter sets are shown. Finally App. G lists the extracted parameter sets used to simulate the circuits of Chapter 7.

1.8 Extent of Originality

Although the main body of the work described in this thesis is original, some parts could not have been done without the help of others. The subcircuit model (see Chapter 3) has been developed at PHILIPS Nijmegen, and the modelling ideas are partly inspired by the many interesting discussions I had with the people of the characterisation group of PHILIPS, Consumer Systems, Nijmegen, The Netherlands. In particular I would like to mention Maarten Swanenberg, Hans van Zwol, Michiel Stoutjesdijk and Peter Rommers. For the development of the compact LDMOS model, I would like to mention Jim Benson, who is currently refining the Southampton STAG model, Annemarie Aarts, who is at present implementing the compact LDMOS model in PSTAR, and Luuk Tiemeijer, for his help with the S-parameter measurements.

The circuits and devices used for evaluation were laid out by me and fabricated in PHILIPS Nijmegen. The driver circuit in Chapter 7 was originally laid out by Wim-Jan Brummelman and adapted by me for testing. The class AB amplifier circuit was based on a suggestion of Jan Dikken.

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Chapter 2

LDMOST in a SOI HV Process: Overview of Device Physics for Modelling

2.1 Introduction

The distinguishing feature of an LDMOST compared with an ordinary MOST is the drift region, which contributes an additional resistance in series with the active channel (in the ON-state). Depending on the length, the doping profile, and other process and geometry parameters of the drift region, the device will be able to withstand a certain voltage on the drain. In the PHILIPS high voltage process three different LDMOS structures can be distinguished: they are referred to as the LV (Low Voltage), MV (Medium Voltage) and HV (High Voltage) LDMOS structures. These devices are discussed in detail in the following paragraphs. In this thesis we have concentrated on LV and MV LDMOS modelling. However, for completeness, the HV LDMOS structure and some of the key issues which have to be taken into consideration when designing this device, are briefly described in Sec. 2.4.

The most significant characteristics of an LDMOS are the OFF-state breakdown voltage, the ON-state specific resistance, the thermal dissipation and the packing density. Device engineers have optimised the geometry parameters and the doping levels to obtain the right trade-off between these different variables.

When developing a model for a circuit simulator, it is very important to have a physical understanding of the current flow and the charge distribution in the device. In Secs. 2.2 and 2.3 the device simulations for the LV and MV LDMOS are performed, which illustrate the behaviour of the device. The main points of interest are the influence of the lateral doping gradient in the active channel and the FET action (due to front and back gate) in the drift region.

Due to the high thermal resistance of the buried oxide, the device can heat up significantly when conducting under high drain voltage conditions. Hence, it is important to

model the temperature dependent parameters very carefully. The thermal behaviour of the LDMOS is studied in Sec. 2.6.

The use of an SOI substrate results in an extra drain-substrate capacitance. Its impact on the switching behaviour of SOI LDMOST is discussed in Sec. 2.7.

In a HV circuit, it is common that the SOI CMOS or LDMOST are used under *high side conditions*, which implies a very high voltage across the back oxide. For an SOI PMOS, this leads to inversion along the back interface, which can cause leakage and unaccounted charges in switching and class D stages. An SOI LDMOS, used under high side conditions, exhibits an increased on-resistance. This particular operation mode requires careful device design, which is discussed in Sec. 2.8.

2.2 The Low Voltage LDMOS

2.2.1 Device Structure

The LV SOI LDMOST is the simplest of the three LDMOS structures. The fabrication process is identical to the process described in Sec. 1.4.1, with the exception that the LOCOS growth for the field oxide is omitted, because only a relatively low breakdown voltage (typically $\cong$ 15 V) is aimed at for the LV LDMOS, and the thin gate oxide (60 nm) can handle a voltage drop of 15 V. Hence the only differences with the layout in Sec. 1.4.1 are one OD mask instead of two, and a drain contact placed right next to the polysilicon gate. This results in the layout of Fig. 2.2. The simplified cross section of the LV SOI LDMOS is shown in Fig. 2.1.

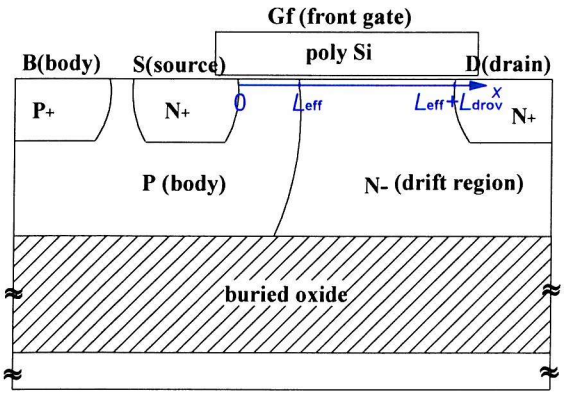

Figure 2.1: Simplified cross section of the LV LDMOS.

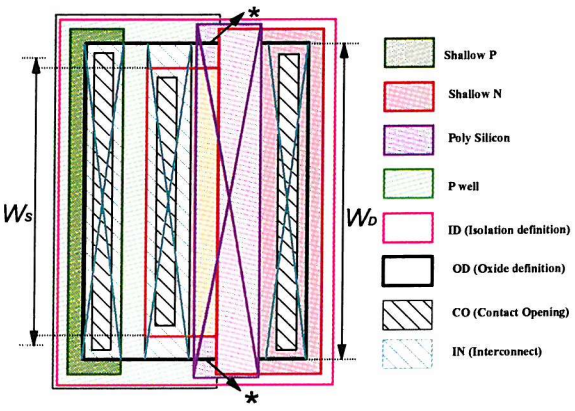

Figure 2.2: Layout of the LV LDMOS.

The N^- doping concentration of the drift region is equal to the doping density of the epitaxial layer of the SOI film, which was chosen to be quite low (typically $1{\cdot}10^{16}$ /cm^3) to obtain high breakdown values. The front gate extends all the way over the drift region on top of the thin gate oxide. This causes accumulation under the thin gate oxide in the drift region, which improves the conductance.

The P-body is formed by a lightly doped P-implementation, followed by thermal annealing (see Secs. 1.4.1 and 1.1). The result is a P-well, which extends vertically up to the buried oxide and laterally approximately 1.5 μm under the front gate. The P-body doping concentration decreases moving from the source ($x = 0$, see Fig. 2.1) to the drain ($x = L_{\text{eff}}$) and the profile is determined by various implantation and annealing processes.

The electrical channel length (L_{eff}) is equal to the lateral diffusion of the P-well, minus the lateral diffusion of the source junction under the gate.

The width of the source area W_{S} is defined by the width of the Shallow N mask, plus two times the length of the lateral diffusion of the N^+ source implant (see Fig. 2.1). This width is smaller than the width at the drain side, W_{D}, which is defined by the width of the OD mask (see Fig. 2.1). The reason behind this particular layout is the following: looking along the width of the P-well, a lower doping concentration is observed at the edges of the LOCOS (stars in Fig. 2.2), resulting in a lower threshold voltage compared with the middle of the device. The cause for this decreased density is the segregation coefficient between silicon oxide and P-type silicon, which is smaller than one [1]. Hence the oxide has the tendency to take up impurities. If the source junction were to be extended all the way until the side LOCOS edges, the two different threshold voltages would cause undesired kinks in the linear characteristics. Using a less wide source area, introducing a small area of P-type material in-between the source area and the LOCOS edges prevents current from flowing in the area with the lower threshold voltage. Therefore the smaller source width removes the kinks in the linear characteristics.

2.2.2 The Current Flow

From the analytical study of the LDMOS derived in Sec. 1.4.2, it is clear that the current flow is a two-dimensional phenomenon, unlike in standard MOSFETs, where the current flow can be considered to a good approximation to be one-dimensional. To verify our conclusions from the analytical calculations, and to have an exact solution for the current flow and for the boundaries of the depletion layers, device simulations were performed with Silvaco's device simulator, ATLAS [2].

Typical values for the geometry and dopant parameters were used: $t_{\text{of}} = 60$ nm (thin gate oxide thickness), $t_{\text{ob}} = 3$ μm (buried oxide thickness), $t_{\text{b}} = 1.5$ μm (silicon film thickness), and $N_{\text{As}} = 10^{17}$ /cm^3 (this is the maximum of a Gaussian doping profile used to describe the under-diffused P-well). The total gate length is 3 μm. The lateral diffusions of the source junction and the P-well are 0.3 μm and 1.25 μm respectively.

The lateral grid spacing of the mesh is chosen to be very fine at the front oxide - silicon interface (0.005 μm), and expands towards the bottom (0.5 μm) and the top (0.02 μm). The horizontal grid spacing is uniform and equal to 0.1 μm. For better accuracy, a "re-grid" operation was performed, based on the doping profiles in the structure. This refines the grid where the doping concentration varies strongly.

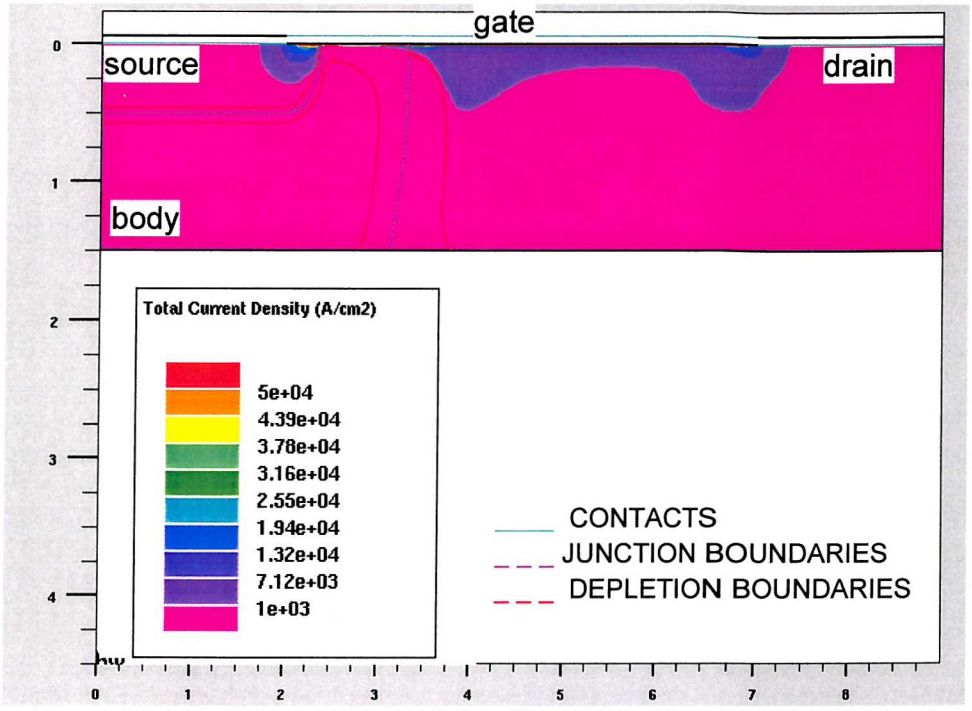

Figure 2.3: The current density in the LV SOI LDMOS for $V_{\mathrm{DS}} = 1$ V and $V_{\mathrm{GfS}} = 4$ V.

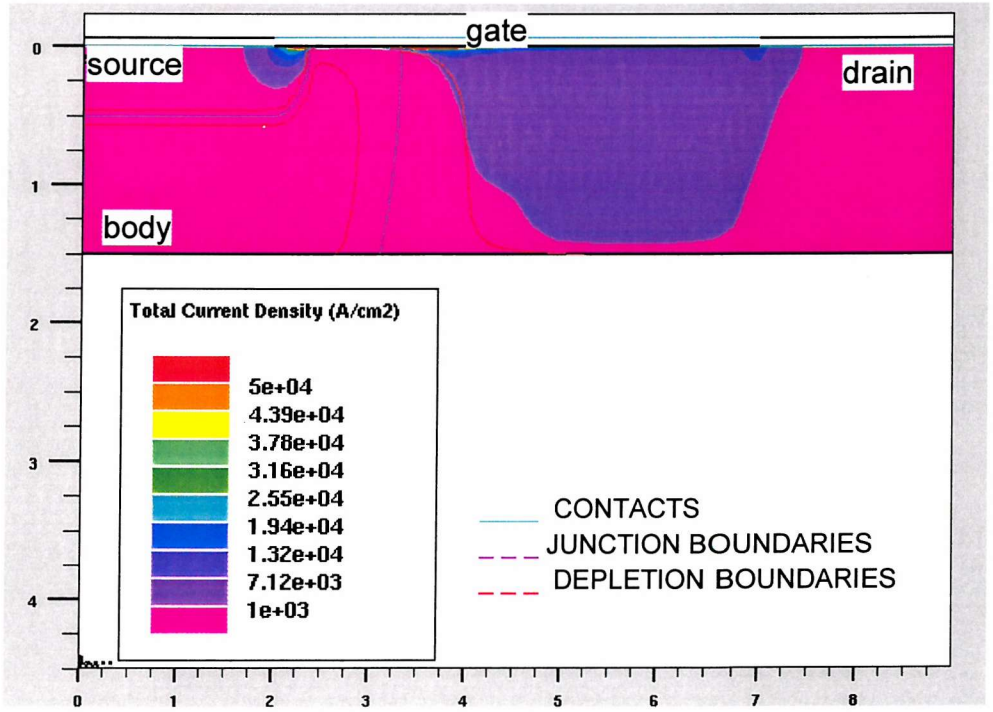

Figure 2.4: The current density in the LV SOI LDMOS for $V_{\mathrm{DS}} = 4$ V and $V_{\mathrm{GfS}} = 4$ V.

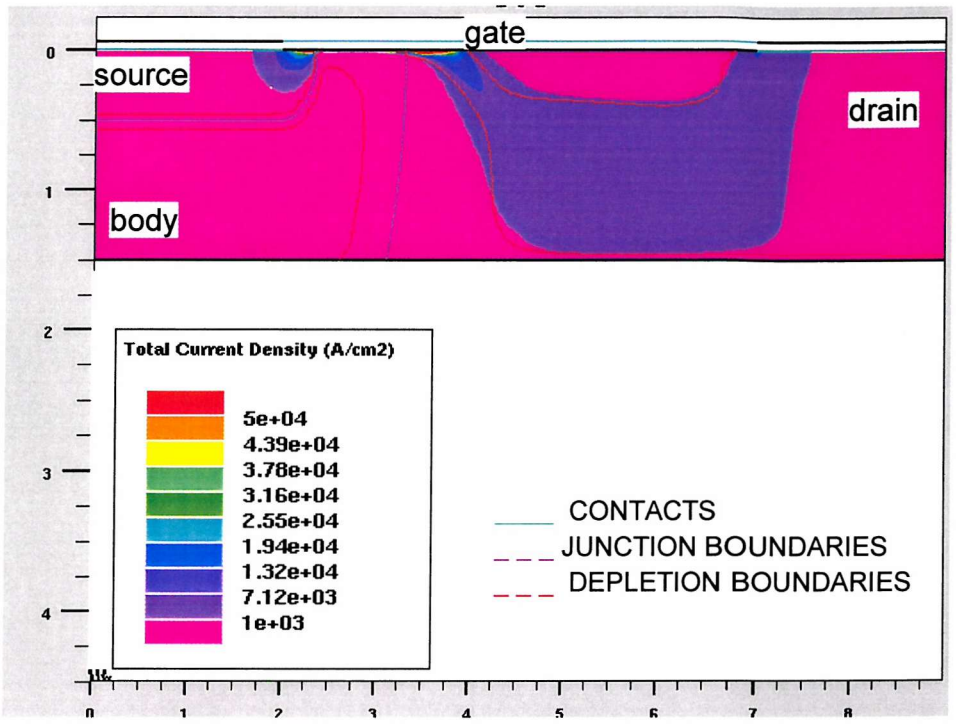

Figure 2.5: The current density in the LV SOI LDMOS for $V_{\mathrm{DS}} = 6$ V and $V_{\mathrm{GfS}} = 4$ V.

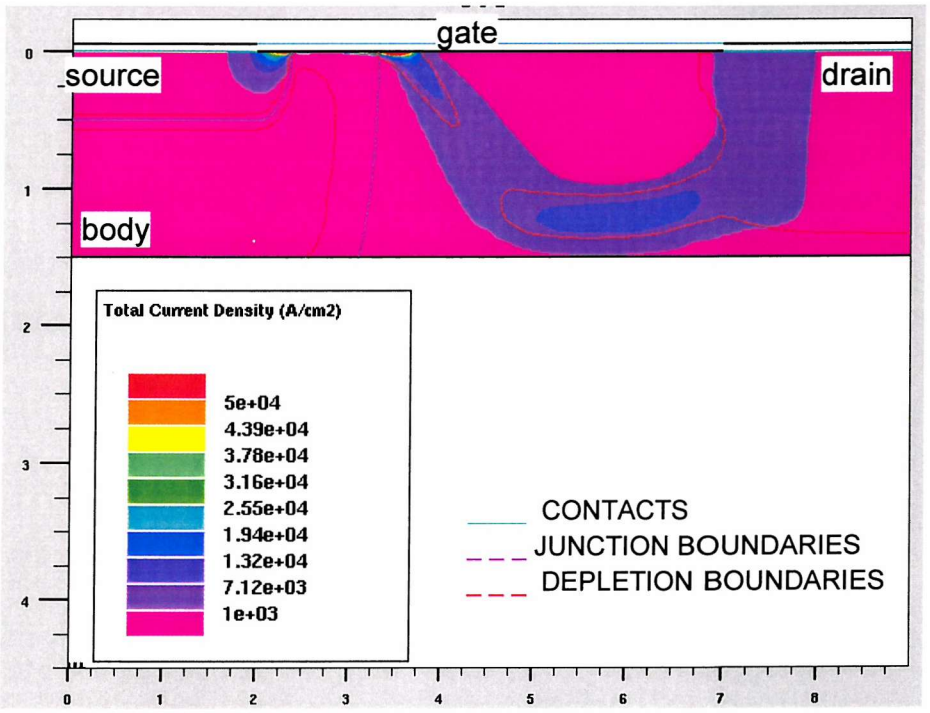

Figure 2.6: The current density in the LV SOI LDMOS for $V_{\mathrm{DS}} = 15$ V and $V_{\mathrm{GfS}} = 4$ V.

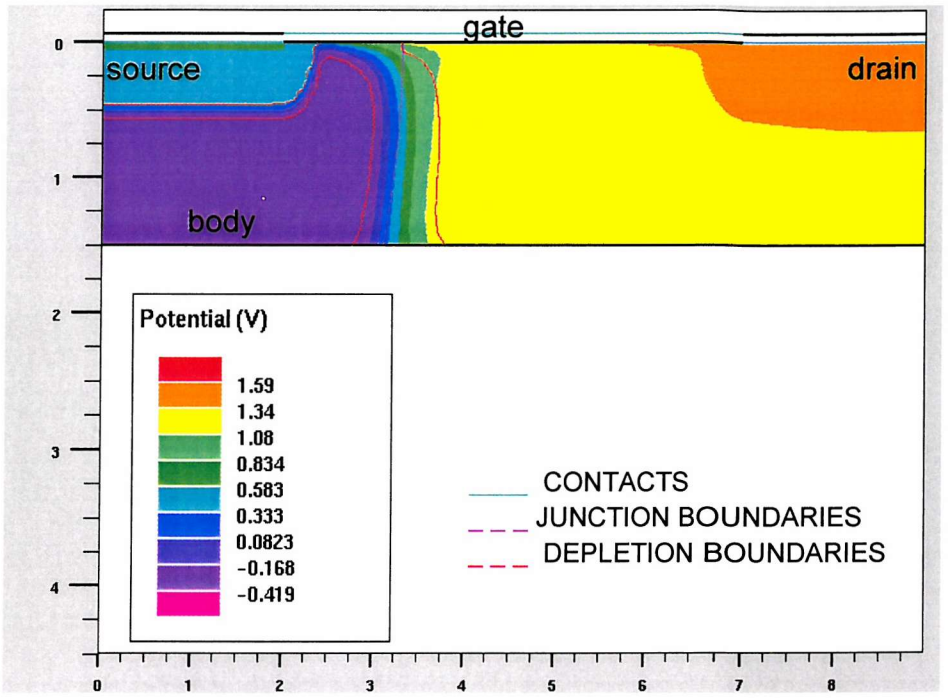

Figure 2.7: The potential in the LV SOI LDMOS for $V_{\mathrm{DS}} = 1$ V and $V_{\mathrm{GfS}} = 4$ V.

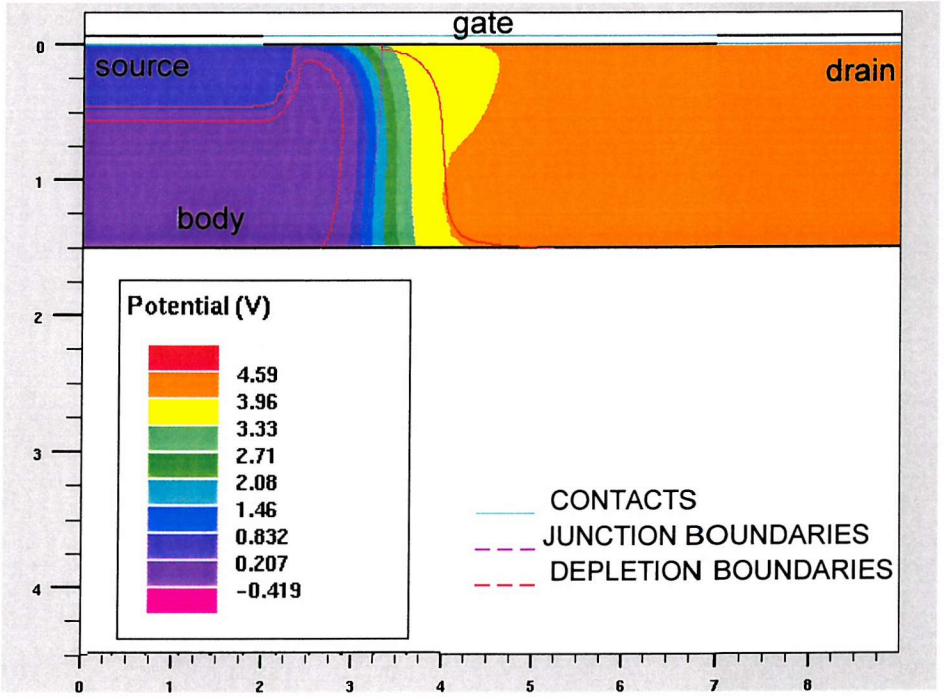

Figure 2.8: The potential in the LV SOI LDMOS for $V_{\mathrm{DS}} = 4$ V and $V_{\mathrm{GfS}} = 4$ V.

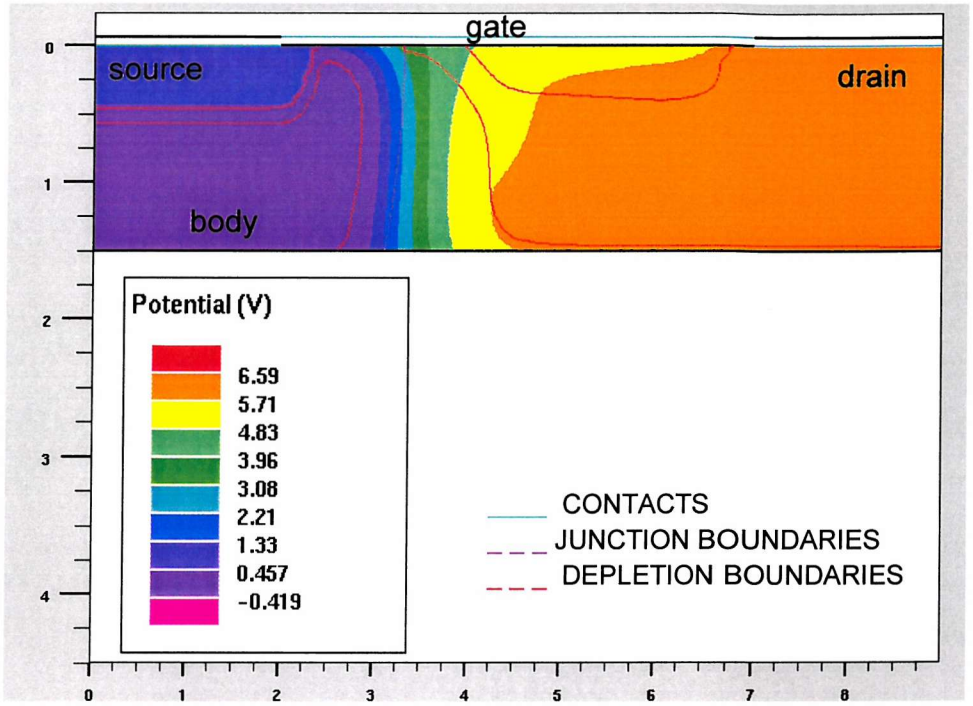

Figure 2.9: The potential in the LV SOI LDMOS for $V_{\mathrm{DS}} = 6$ V and $V_{\mathrm{GfS}} = 4$ V.

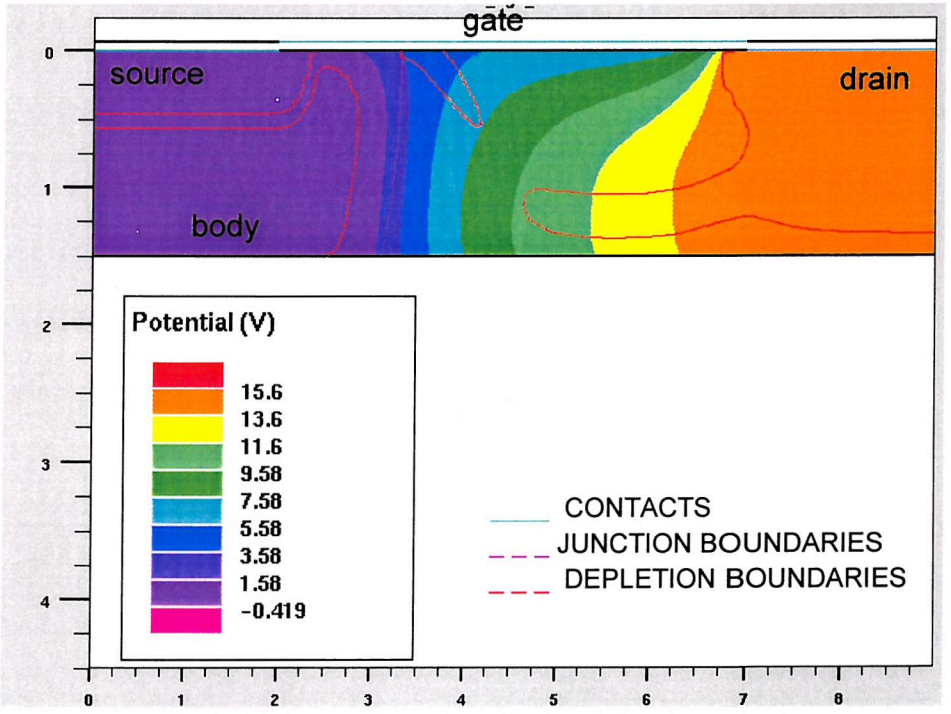

Figure 2.10: The potential in the LV SOI LDMOS for $V_{\mathrm{DS}} = 15$ V and $V_{\mathrm{GfS}} = 4$ V.

The current flow for different bias conditions is illustrated in Figs. 2.3 to 2.6. Two bias regions can be distinguished for the current flow when the transistor is in the ON-state:

- Low V_{DS} ($< V_{GfS} - V_{FB}^{fdr}$) : the Si-SiO_2 interface in the drift region is accumulated over the whole length and the current flows from the inversion layer, mainly into the accumulation layer and then into the drain (see Fig. 2.3). For $V_{DS} = 1$ V, the resistance of the drift region and the inversion channel are roughly the same and we observe a voltage drop of roughly 0.5 V over each of the regions (see Fig. 2.7). When the drain voltage approaches the gate voltage, the conductivity of the accumulation layer decreases and now a bigger part of the current flows in the bulk of the drift region (see Fig. 2.4).

- High V_{DS} ($> V_{GfS} - V_{FB}^{fdr}$): a depletion layer is growing at the drain end of the drift region at the top Si-SiO_2 interface. At the other end of the drift region the accumulation layer is still present. The current flow is now strongly two-dimensional, flowing downwards from the accumulation layer at the P-N^- junction towards the middle of the drift region and then back upwards in the drain (see Fig. 2.5). For $V_{DS} \gg V_{GfS} - V_{FB}^{fdr}$, the two depletion layers (from the front gate and from the junction) touch and the electrons flow at saturation velocity speed through the depleted region (see Fig. 2.6).

In Figs. 2.8 to 2.10 the potential distribution is plotted for three increasing values of V_{DS}, all larger than $V_{GfS} - V_{FB}^{fdr}$. Hence the current in the inversion layer has saturated. The potential at the P-N^- junction stays almost constant : 2.6 V $\pm$ 0.1 V. A further increase in drain voltage only causes a redistribution of the potential in the drift region until the breakdown voltage is reached.

Figs. A.1 to A.6 of App. A show the distribution of the current density and the potential for a high gate voltage ($V_{GfS} = 8$ V): the above discussion is valid, with the difference that accumulation disappears later, and a smaller region will be depleted under the thin gate oxide at the drain side for $V_{DS} = 15$ V. For $V_{GfS} = 8$ V the two depletion layers from the P-N^- junction and from the front gate in the drift region never reach each other and current saturation originates in the inversion channel.

2.2.3 Lateral Doping gradient in the P-body under the Thin Gate Oxide

The double diffused NMOS has a non-uniformly doped channel region defined by the compensations of the P-implant and the N^+-source lateral diffusions. Thus, the doping concentration along the channel, $N_A(x)$ has a maximum near the source ($N_A(0) = N_{As}$) and decreases sharply towards the drain ($N_A(L_{eff}) = N_{Ad}$).

From diffusion theory [1] it is known that the doping concentration after diffusion as a function of the distance normal to the surface is given by a complementary error-function type of distribution. The doping profile parallel to the surface from the edge of the opening deviates slightly from the error-function type distribution.

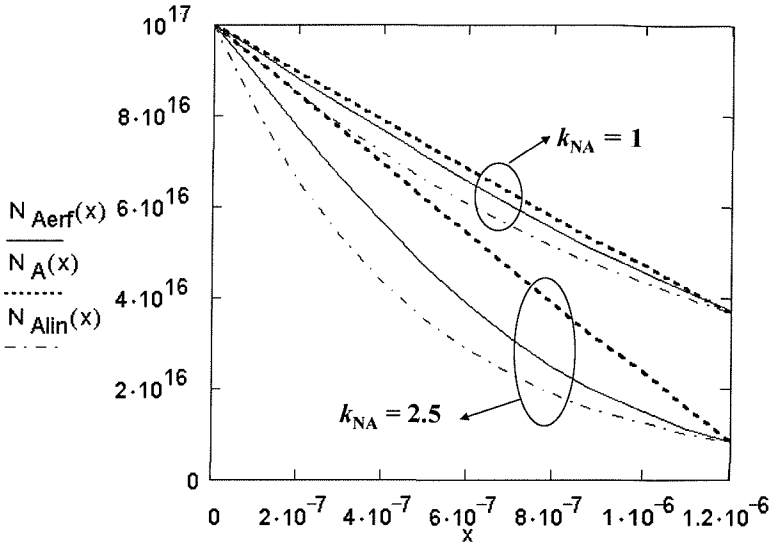

Figure 2.11: Comparison of the error-type with the exponential and linear distribution for the doping concentration in the channel.

In the following of this thesis, it is assumed that the lateral non-uniform channel (P) doping can be approximated by an exponential function [3,4],

$$N_{\mathrm{A}}(x) = N_{\mathrm{As}} \exp(-\frac{k_{\mathrm{N_A}}\, x}{L}) \tag{2.1}$$

where x is the distance along the channel, L the channel length, N_{As} the doping concentration at the source side and $k_{\mathrm{N_A}}$ the lateral body doping gradient coefficient. In Fig. 2.11 the exponential distribution is compared with the error-function type distribution,

$$N_{\mathrm{Aerf}}(x) = N_{\mathrm{As}}\, \mathrm{erfc}(\frac{x}{L_{\mathrm{diff}}}) \tag{2.2}$$

with L_{diff} the diffusion length. We have also added a linear distribution

$$N_{\mathrm{Alin}}(x) = N_{\mathrm{As}} + (N_{\mathrm{Ad}} - N_{\mathrm{As}})\, \frac{x}{L} \tag{2.3}$$

Depending on the channel length and the lateral doping gradient (or in other terms depending on the diffusion length) the linear or the exponential function will be a better approximation of the error-type distribution, but for typical LDMOS processes both provide a good approximation of the doping profile. In Fig. 2.11 the comparison is made for a typical value of the doping gradient ($k_{\mathrm{N_A}} = 1$) and for an extremely high value ($k_{\mathrm{N_A}} = 2.5$). For the high value the exponential distribution is the better choice as an approximation of the doping profile.

Extraction Technique for k_{N_A} Based on Threshold Voltage Measurements

In [5] an extraction method for the lateral channel doping profile is developed. This technique is based on C-V characterisation, and extracts the threshold voltage at the drain end of the channel from the gate-drain capacitance. The disadvantage of this technique is that one needs to know the exact curve for the accumulation capacitance originating from the overlap of the gate over the drift region.

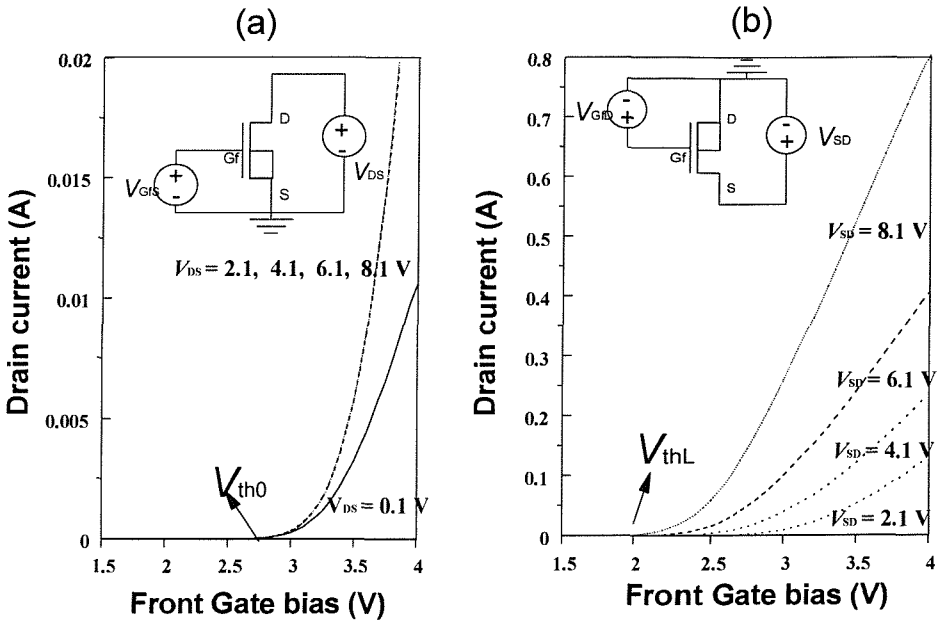

Figure 2.12: (a) The drain current versus the gate voltage for V_{DS} = 0.1 V, 2.1 V, 4.1 V, 6.1 V, 8.1 V; (b) the source current versus the gate voltage for V_{SD} = 0.1 V, 2.1 V, 4.1 V, 6.1 V, 8.1 V (source and drain are reversed compared to normal biasing).

To obtain the doping concentrations at the drain and at the source ends of the channel, a new characterisation method will now be formulated. This technique is based on the measurement of the current as a function of the gate voltage, when the LDMOS is reverse biased with a high source bias. In those operating conditions, the channel is strongly pinched at the source side (instead of at the drain, which is the case for an LDMOS biased in normal saturation conditions), and the threshold voltage will be determined by the doping concentration at the drain side of the channel.

The drain current was measured as a function of the gate voltage for normal and reverse biasing (Fig. 2.12). For the normal biasing, the drain current increases with the drain bias until the saturation regime is reached. This is clearly visible in Fig. 2.12(a), where the curves for V_{DS} = 2.1 V, 4.1 V, 6.1 V and 8.1 V all overlap each other.

For the reverse biased situation, it is observed that the threshold voltage decreases with increasing V_{SD}. This can be explained with the help of Fig. 2.13. If the channel pinches at the source side, the threshold voltage is lower than the value at the source (V_{th0}) and the doping concentration at the pinch-off point of the channel (see * in Fig. 2.13) determines

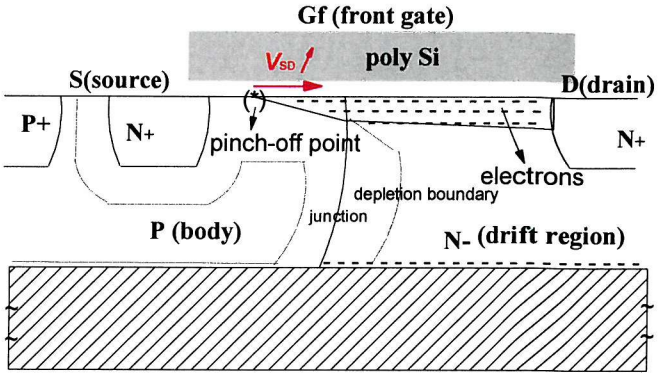

Figure 2.13: Illustration of saturation by pinch-off in the LDMOS under reverse bias operation conditions.

the actual threshold voltage. For very deep saturation the threshold voltage converges to the threshold voltage calculated from the doping concentration at the drain side of the channel, V_{thL}.

Looking closely at Fig. 2.12, one notes that the current increase in the reverse biased case cannot only be due to the threshold voltage decrease. There is another parasitic effect which causes this large increase in current as V_{SD} is increased. This could be explained by the fact that as V_{SD} is increased, the depletion layer under the source grows (for V_{SD} =8 V, it is of the order of 0.4 μm), and the body resistance increases. When holes are generated due to impact ionisation the potential in the body increases, and can switch on the parasitic bipolar.

From V_{th0} and V_{thL}, the corresponding doping concentrations, N_{As} and N_{Ad} can be calculated. In our example $V_{\mathrm{th0}} = 2.6$ V and $V_{\mathrm{thL}} = 1.5$ V. The corresponding doping concentrations are: $N_{\mathrm{As}} = 0.93 \cdot 10^{17}$ /cm^3 and $N_{\mathrm{Ad}} = 0.37 \cdot 10^{17}$ /cm^3. Knowing the doping concentrations, the lateral body doping gradient coefficient which describes the exponential doping profile can be calculated and this yields $k_{\mathrm{N_A}} = 1$.

Influence of $k_{\mathrm{N_A}}$ on the Charge Distribution in the Channel

The non-uniform doping concentration in the channel causes a substantially different charge distribution compared with the uniform case. This effect manifests itself mainly in the capacitance behaviour, which will be treated in Chapter 5. Here we want to have a look at the electron concentration along the channel for different gate biasing conditions.

The electron density in the LV LDMOS was simulated with ATLAS, for zero drain and source voltage. The gate voltage was stepped from 0.5 V to 2.5 V in steps of 0.5 V. The threshold voltage of the simulated device (V_{th0}) is 2.5 V, which corresponds to the appearance of inversion charge at the source end of the channel.

In Fig. 2.14 the electron density in the inversion channel of the LV LDMOS is shown

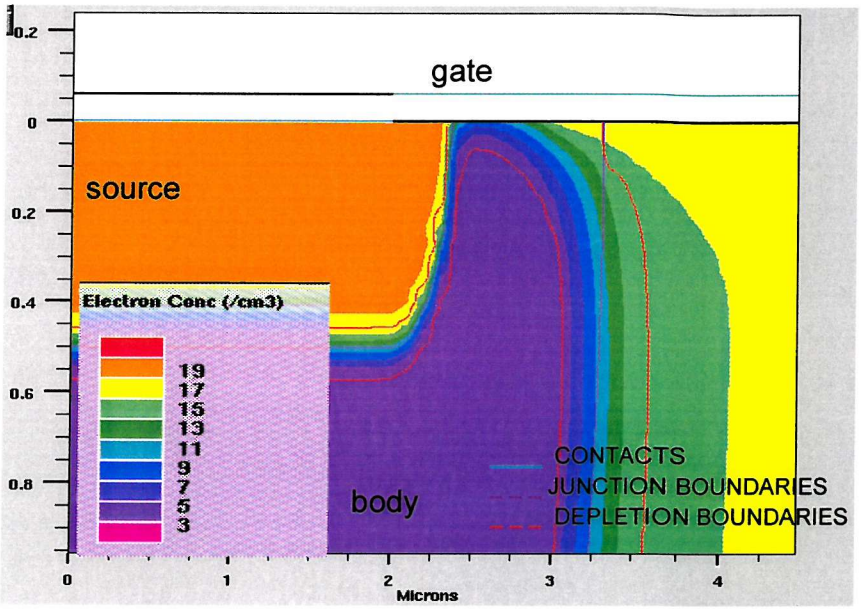

Figure 2.14: The electron density in the inversion channel of the LV LDMOS for $V_{\mathrm{GfB}} = 1$ V and $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V.

for $V_{\mathrm{GfS}} = 1$ V. The Si-SiO_2 interface in the drift region is accumulated, and inversion charge is present at the P-N^- junction spreading about half way into the P-well, but the source side of the channel is not yet inverted.

Increasing the gate voltage shifts the starting point of inversion towards the left, and when V_{GfB} exceeds the threshold voltage, the source end becomes inverted. This gradual decrease of the inversion charge from drain to source is illustrated in Fig. 2.15, where the electron concentration is plotted as a function of the position in the channel.

In a standard MOSFET device the gate-channel capacitance increases rapidly from 0 to its maximum value as the gate voltage passes the threshold voltage. The lateral doping

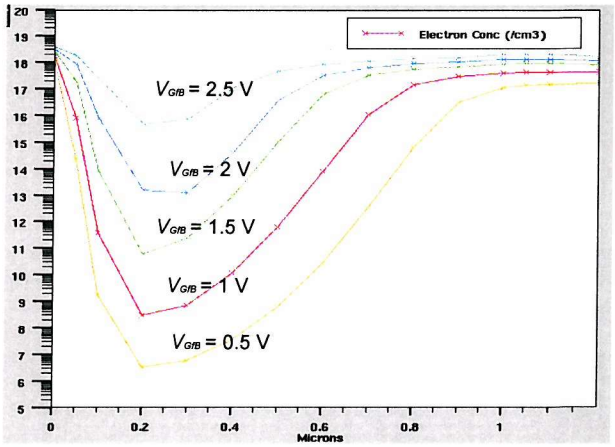

Figure 2.15: The electron density along the channel for $V_{\mathrm{GfB}} = 0.5$ V till $V_{\mathrm{GfB}} = 2.5$ V, and $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V.

profile in the channel of the LDMOS causes the gate-channel capacitance to increase more gradually starting at $V_{\mathrm{GfS}} = V_{\mathrm{thL}}$ and reaching its maximum value at $V_{\mathrm{GfS}} = V_{\mathrm{th0}}$.

2.2.4 Impact Ionisation and Avalanche Current

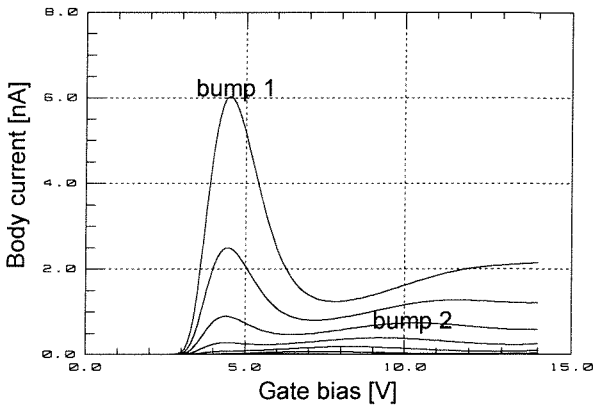

Figure 2.16: The avalanche current in function of the gate voltage for different drain voltages for an LV LDMOS with $W_{\mathrm{S}} = 20$ μm.

The high electric field that exists across depletion layers is responsible for sweeping out any holes and electrons that enter this region. When this field reaches a critical value, these carriers have sufficient energy to generate electron-hole pairs. This phenomenon, called impact ionisation, is multiplicative. When the rate of impact ionisation reaches infinity the device undergoes avalanche breakdown.

To look at the avalanche current, it is common to measure the body current as a function of the gate voltage for different drain biases (Fig. 2.16).

For gate voltages just above the threshold and a low drain bias, avalanche takes place at the P-N^- junction, just as for standard NMOS [6]; increasing the drain bias gives rise to a second impact ionisation area in the depleted region close to the N^+ drain area (see Fig. 2.17). This explains the first bump in the characteristic: the impact current first increases with increasing gate voltage due to the increase of the drain current. Then it reaches a maximum and decreases as the triode region is entered and the channel is no longer pinched. Furthermore the depleted area at the drain end reduces as the gate bias is increased. This can be seen in Fig. 2.18, where the impact generation rate is plotted for $V_{\mathrm{GfS}} = 8$ V. The total impact generation is considerably smaller than in Fig. 2.17, where $V_{\mathrm{GfS}} = 4$ V.

The second bump can be explained by the fact that the current flows partly at the two extremes of the channel (along the LOCOS edges). The current flowing from the source extremes to the drain (see arrows in Fig. 2.21) has to follow a longer current path and hence the density is lower. In this area avalanche will be maximum for a higher gate voltage. The height of the second bump is independent of the device width because the difference between the width at the source side and at the drain side is independent of the

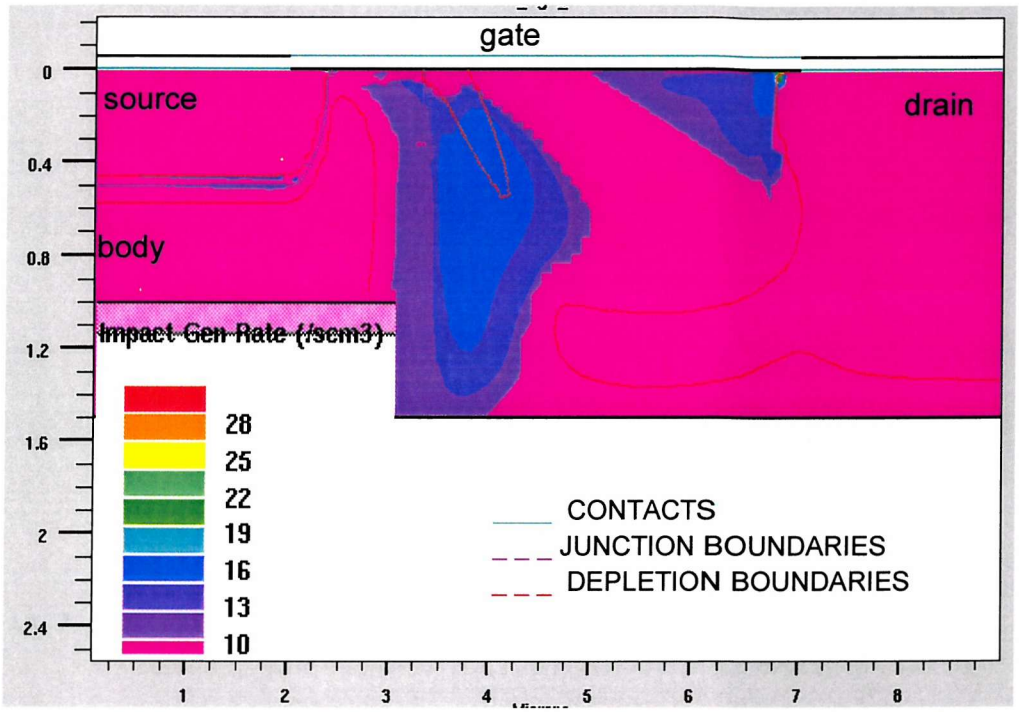

Figure 2.17: The impact generation rate in the LV LDMOS for $V_{\mathrm{GfS}} = 4$ V and $V_{\mathrm{DS}} = 15$ V.

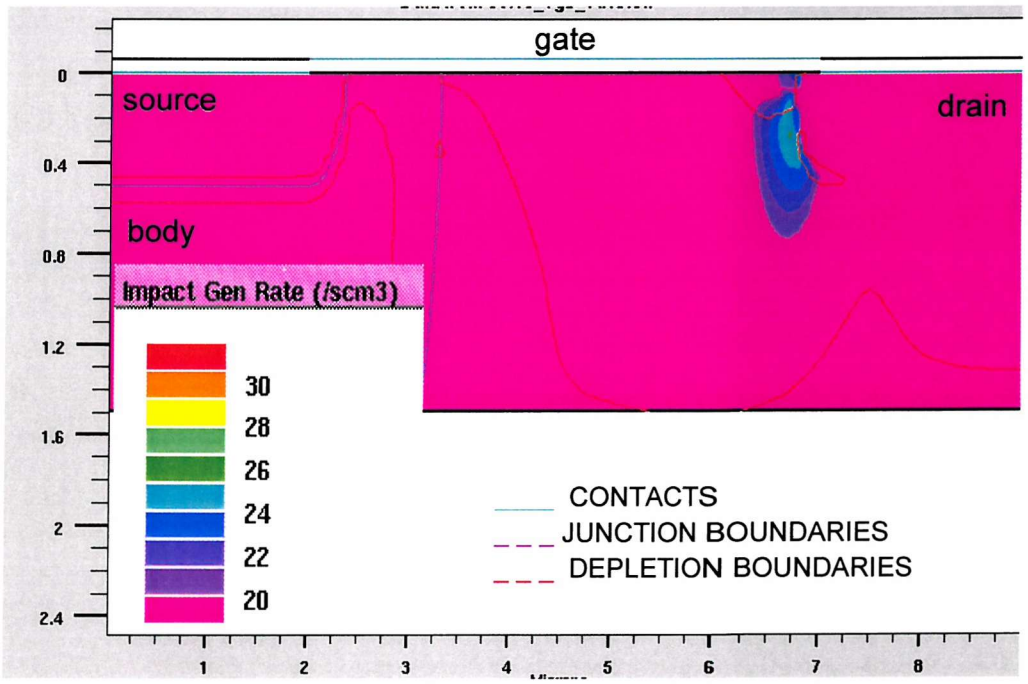

Figure 2.18: The impact generation rate in the LV LDMOS for $V_{\mathrm{GfS}} = 8$ V and $V_{\mathrm{DS}} = 15$ V.

device width.

For very high currents (hence very high V_{GfS}) more avalanche takes place at the N^--N^+ interface in the drift region. This explains the tail in the body current curves of Fig. 2.16.

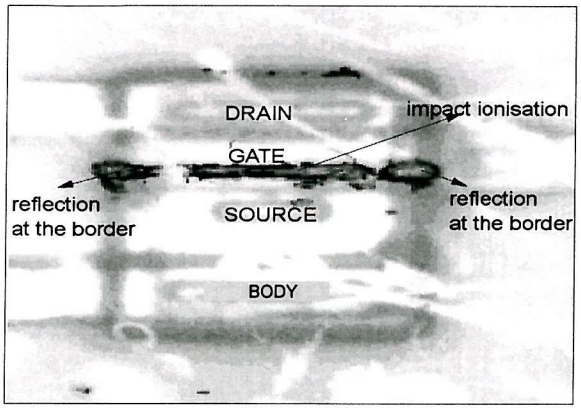

Figure 2.19: Emission micrographs of the LDMOS for the following biases: $V_{GfS} = 4$ V and $V_{DS} = 10$ V.

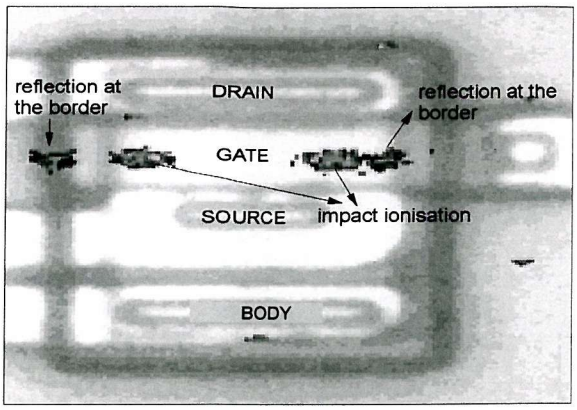

Figure 2.20: Emission micrographs of the LDMOS for the following biases: $V_{GfS} = 10$ V and $V_{DS} = 10$ V.

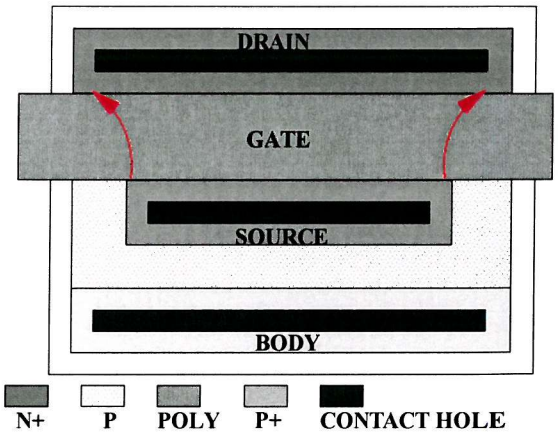

Figure 2.21: Top View of the LV LDMOS.

To verify the above explanations, photo emission measurements were performed at the bias conditions for which the two maxima in the body current are visible ($V_{GfB} = 4$ V and $V_{GfB} = 10$ V). A high drain voltage ($V_{DS} = 10$ V) was chosen to make the impact ionisation effect clearly visible.

Emission microscopy is an effective technique for reliability physics, design verification and failure analysis of industrial semiconductors. It has numerous applications like detection of the location of avalanche breakdown in reversed biased P-N^- junctions, detection of impact ionisation, analysis of the different leakage current mechanisms, etc. [7]. When carriers are generated by impact ionisation, this is accompanied by the emission of high-

energy photons, and hence light emission due to avalanche currents can be observed [8].

The photographs of the photon emission in the LV LDMOS are shown in Figs. 2.19 and 2.20. For clearness the top view of the LV LDMOS is added in Fig. 2.21. The emission at the thick LOCOS edges (ID mask) on the first photograph is merely the reflection and is not relevant. The first picture shows that impact ionisation happens in an area defined by the source width (W_S), and not over the whole width defined by the OD mask (W_D, see Sec. 2.2.1), as expected for low V_{GfS}.

On the second picture we observe the impact ionisation at the two sides of the channel where the current density is lower, and hence impact ionisation happens for higher V_{GfS}. This second maximum can of course not be simulated, because the study was limited to 2 dimensional simulations.

2.3 The Medium Voltage LDMOS

2.3.1 Device Structure

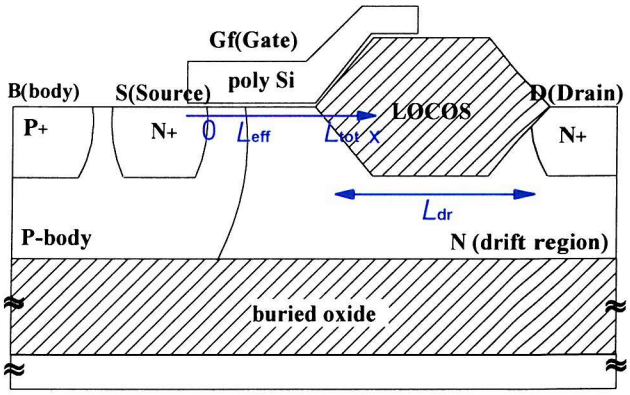

Figure 2.22: Cross section of the MV LDMOS.

The medium voltage (40V) LDMOS is schematically shown in Fig. 2.22. The structure of the MV LDMOS is very similar to the LV structure with the difference that a thicker oxide above the drift region is needed to prevent early breakdown of the thin gate oxide. The complete fabrication process was already described in Sec. 1.4.1. The gate electrode extends a little over the drift region on top of a thicker oxide, helping to shape the surface fields in the structure. This part of the gate has the function of a field plate and will bend back the equipotential lines to reduce the lateral electric fields. The thick oxide also helps to reduce the fringing fields at the edge of the polysilicon gate.

The electrical gate length (L_{eff}) is equal to the lateral diffusion of the P-body well, minus the lateral diffusion of the source junction. The length of the drift region under the field oxide (L_{dr}) depends on the desired breakdown voltage, but this structure is not very efficient for very high (> 100 V) drain voltages, because in that case it is more worthwhile

to use a graded doping profile in the drift region, and hence have more homogeneous field lines (see Sec. 2.4).

2.3.2 Depletion regions and the current flow lines

Just as for the LV LDMOS, we are going to undertake a detailed physical study of the two dimensional behaviour of the MV LDMOS with the help of Silvaco's device simulator. Typical values for the geometry and doping parameters were used: $t_{of} = 60$ nm (thin gate oxide thickness), $t_{ob} = 3$ μm (buried oxide thickness), $t_b = 1.5$ μm (silicon film thickness), $t_{bdr} = 1.0$ μm (silicon film thickness under the field oxide), and $N_{As} = 10^{17}$ /cm^3 (this is the maximum of a Gaussian doping profile used to describe the under-diffused P-well). The total gate length is 3 μm. The lateral diffusions of the source junction and the P-well are respectively 0.3 μm and 1.25 μm. Because it is only possible to specify rectangular shapes in the ATLAS simulator the shape of the field oxide has been approximated by a step profile.

The lateral grid spacing of the mesh is chosen to be very fine at the front oxide - silicon interface (0.02 μm), and is then expanded towards the bottom (0.5 μm) and the top (0.05 μm). The horizontal grid spacing reduces from 0.1 μm at the source end to 0.05 μm at the drain end. Just like for the LV LDMOS, a "re-grid" operation was performed, based on the doping profiles in the structure.

Two different situations can be distinguished for the current flow lines:

- Low V_{DS}: the Si-SiO_2 interface under the thin gate oxide in the drift region is accumulated over the whole length. The current flows from the inversion layer, mainly into the accumulation layer, and via the bulk of the drift region to the drain (see Fig. 2.23). The corresponding potential distribution is shown in Fig. 2.24.

- High V_{DS}: the Si-SiO_2 interface under the thin gate oxide is only partly accumulated starting at the P-N^- junction. The current flows from the inversion layer, into the leftover of the accumulation layer, and then flows almost vertically, guided by the two depletion layers (from the front gate and from the junction). This channel can become very narrow, and at the pinch-off voltage (when the two depletion layers touch) the current flows through the depleted area at drift saturation velocity (see Fig. 2.25). However, since the current will have already saturated due to saturation by pinch-off of the MOSFET channel at a lower drain bias, this second saturation effect cannot be seen in the output characteristic of the current. The corresponding potential distribution in Fig. 2.26 illustrates the higher voltage drop (and hence higher fields) in the saturated areas.

2.3.3 Avalanche current

While the field oxide in the MV LDMOS shifts the presence of high electrical fields to higher drain voltages compared with the LV LDMOS, the behaviour of the avalanche current is

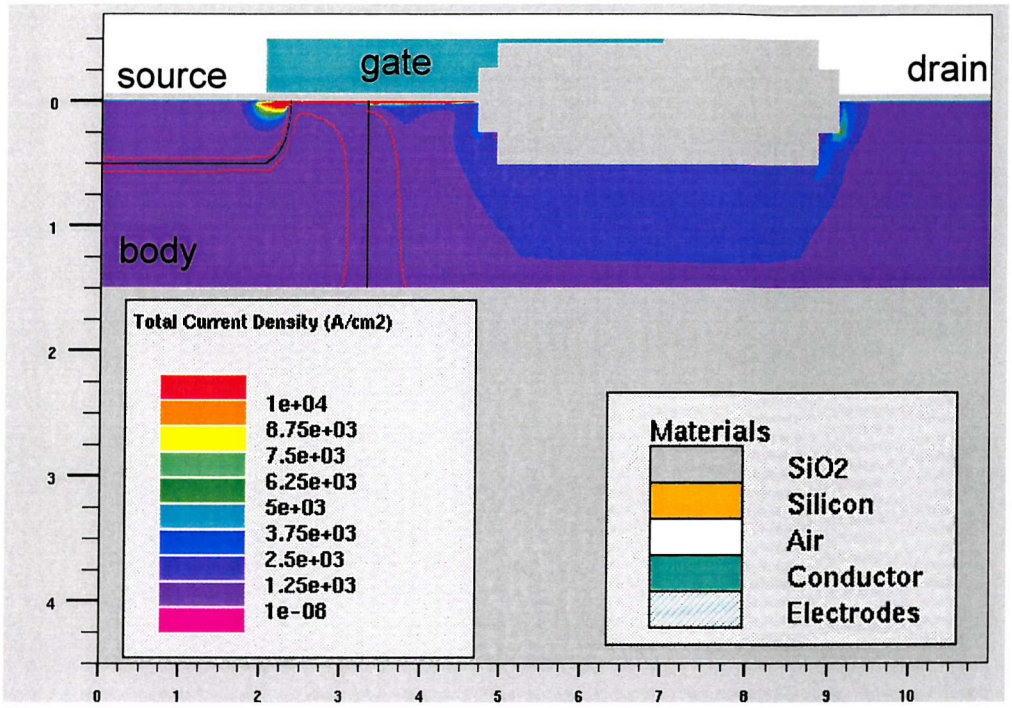

Figure 2.23: The current density in the MV SOI LDMOS for $V_{\mathrm{DS}} = 1$ V and $V_{\mathrm{GfS}} = 4$ V.

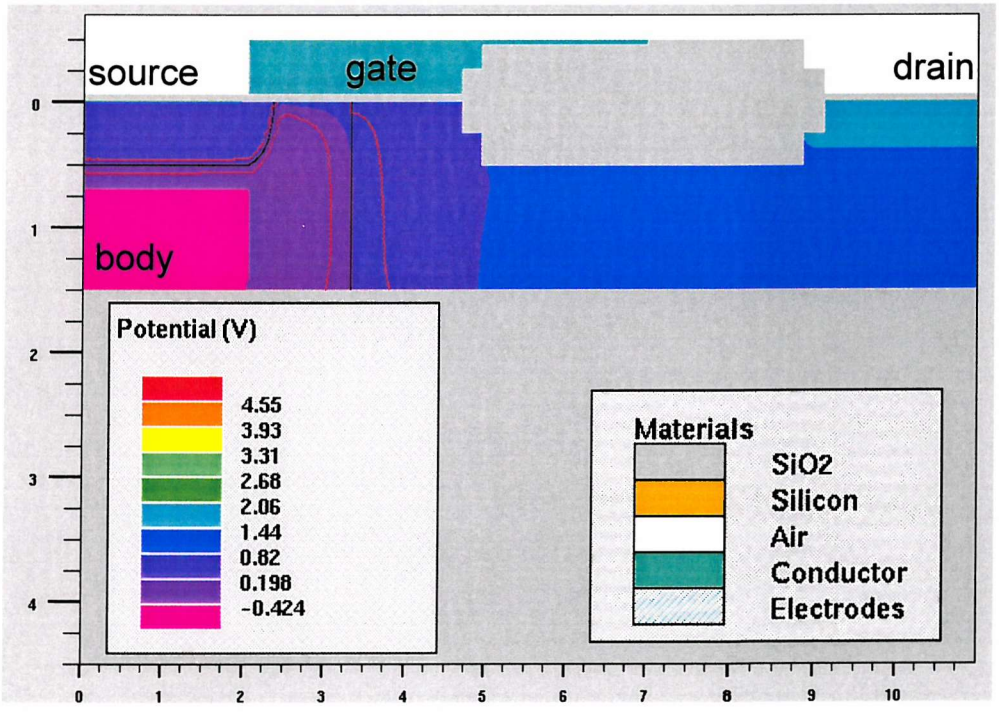

Figure 2.24: The potential in the MV SOI LDMOS for $V_{\mathrm{DS}} = 1$ V and $V_{\mathrm{GfS}} = 4$ V.

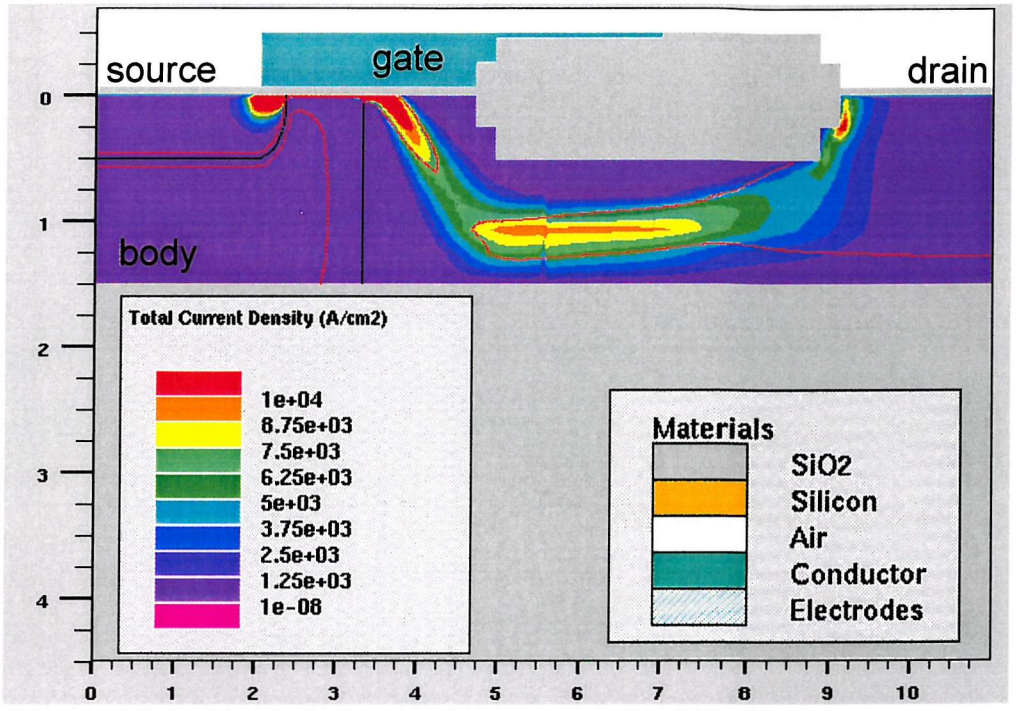

Figure 2.25: The current density in the MV SOI LDMOS for $V_{\mathrm{DS}} = 20$ V and $V_{\mathrm{GfS}} = 4$ V.

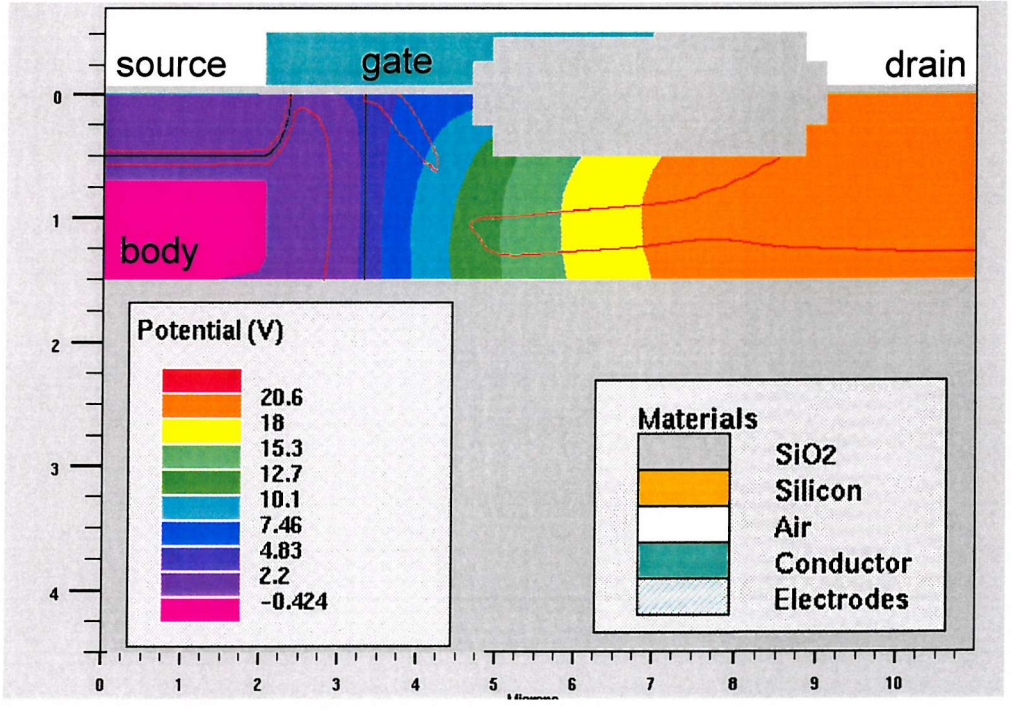

Figure 2.26: The potential in the MV SOI LDMOS for $V_{\mathrm{DS}} = 20$ V and $V_{\mathrm{GfS}} = 4$ V.

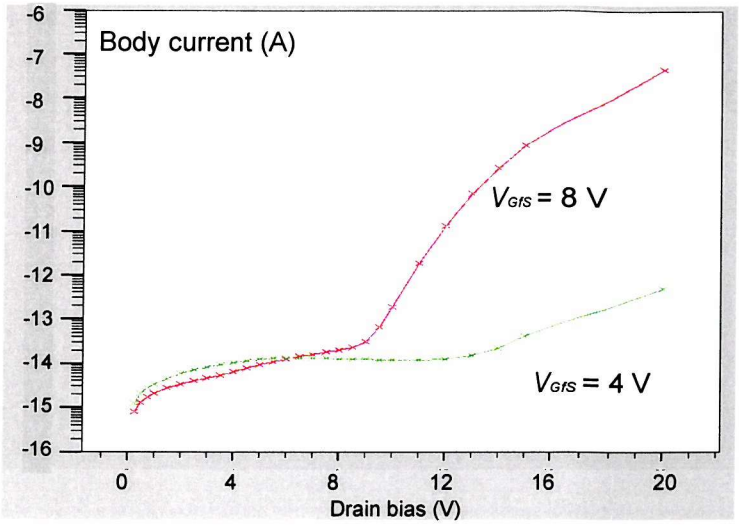

Figure 2.27: The impact ionisation current in terms of V_{DS} in the MV SOI LDMOS; $V_{GfS} = 4$ V and $V_{GfS} = 8$ V.

very similar. In Fig. 2.27 the simulated impact ionisation current is plotted as a function of the drain voltage for two different gate biases. The body avalanche current increases with increasing electrical fields and drain current. For $V_{GfS} = 4$ V the drain current is too low to cause considerable impact ionisation. For a higher gate bias ($V_{GfS} = 8$ V), and hence more drain current, impact ionisation becomes significant above the critical value for the electrical field.

To analyse the sources of the impact ionisation current, the impact ionisation rate was simulated in the cross section of the MV LDMOS. For a low gate voltage (Fig. 2.28) it takes mainly place at the P-N^- junction, where the electrical field is highest. In this situation the current in the drift region is very small and the voltage drop over the drift region under the field oxide is only a minor part of the total drain voltage.

For a higher gate voltage (see Fig. 2.29) the current is higher, and a larger part of the drain voltage drops over the drift region. A high field is created near the drain, where the current flows at drift saturation velocity. This region has now become the main source for impact ionisation.

High side bias conditions also influence the avalanche current in the MV LDMOS, but this will be discussed in Sec. 2.8.1

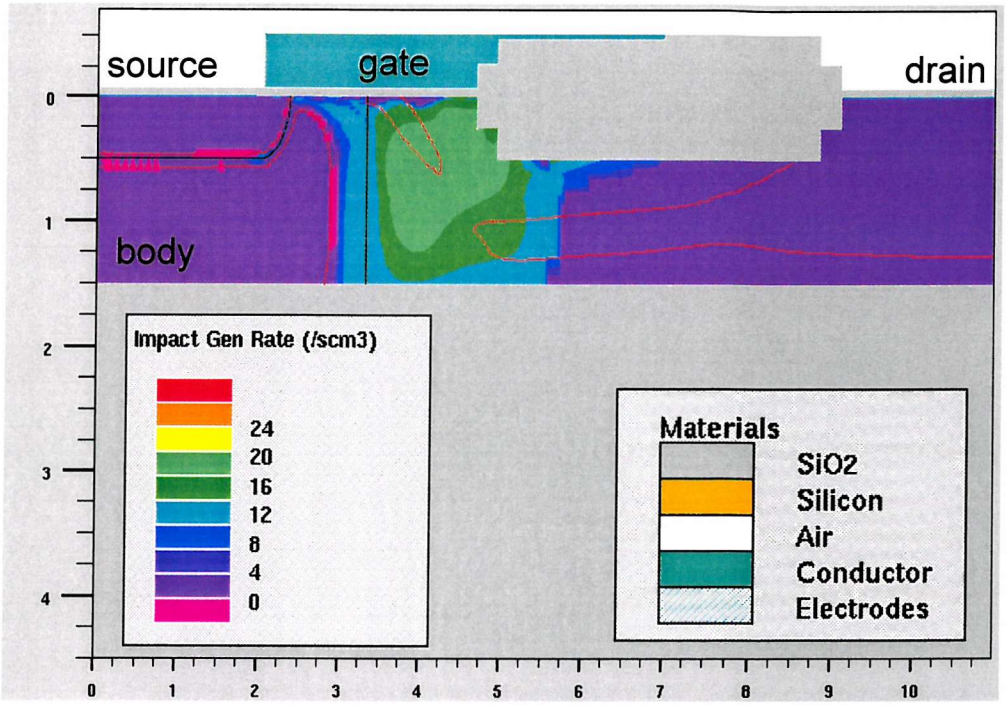

Figure 2.28: The impact generation rate in the MV SOI LDMOS for $V_{\mathrm{DS}} = 20$ V and $V_{\mathrm{GfS}} = 4$ V.

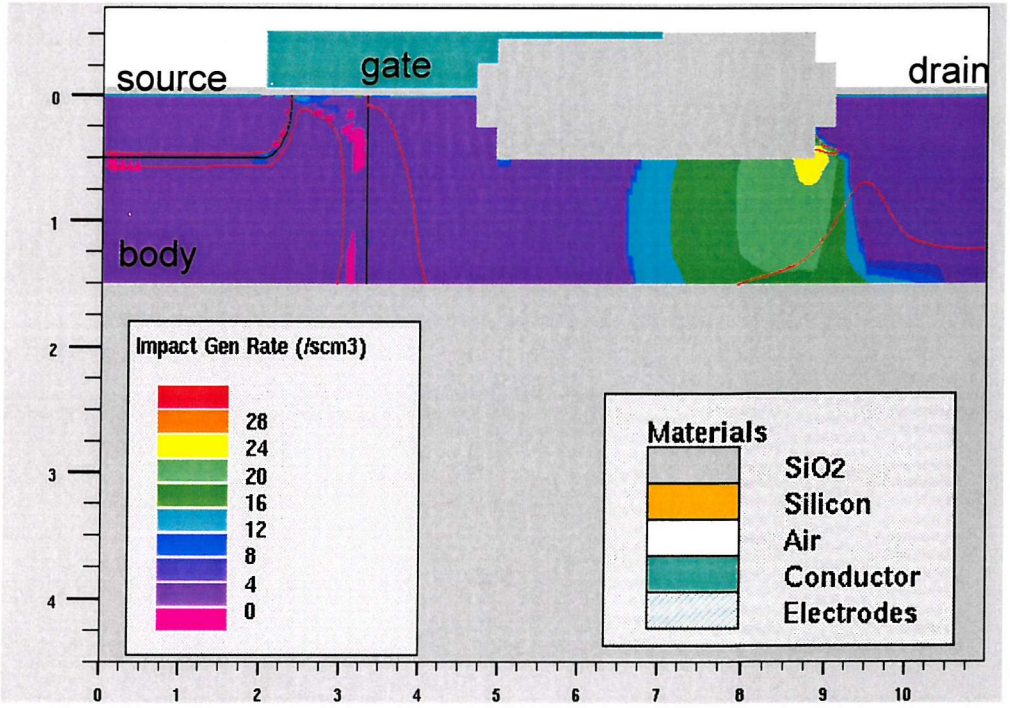

Figure 2.29: The impact generation rate in the MV SOI LDMOS for $V_{\mathrm{DS}} = 20$ V and $V_{\mathrm{GfS}} = 8$ V.

2.4 The High Voltage LDMOS

To achieve optimal on-resistance and breakdown voltage, the doping concentration in the drift region can be made to have a decreasing profile from the drain end towards the source end. This is especially worthwhile for high voltage devices (> 100 V) because then the devices can be made a lot smaller. In this thesis, these devices will be referred to as HV LDMOS transistors. This doping profile is not included in our compact model, which concentrates instead on the modelling of the LV and the MV LDMOS, but an effective avarage value for the drift doping concentration can be used if desired.

2.4.1 Breakdown Voltage versus On-Resistance

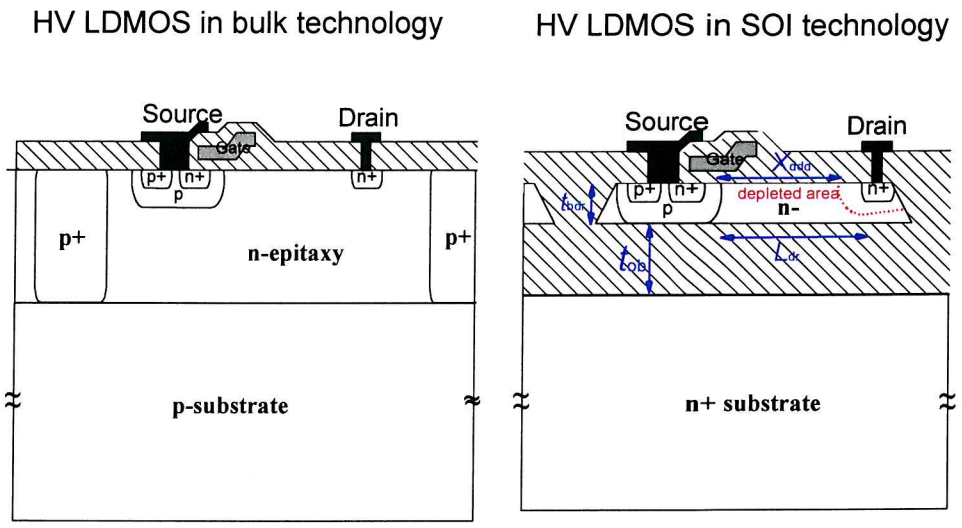

Figure 2.30: The HV LDMOS in bulk technolgy and in SOI technology.

The basic challenge for the designer of an HV LDMOS device is to minimise the on-resistance for a specific breakdown voltage. In the OFF-state of the device, the drain is biased positively and the body is grounded by the body contact, so that the P-N^- junction between the drift region and the body is reverse biased. To approach the breakdown voltage of an ideal P-N junction we have to ensure that the drift region becomes completely depleted in the OFF-state, or in other words, a uniform potential distribution in the OFF-state is needed. Therefore the doping concentration in the drift region has to be optimised. This is known as the RESURF (REduced SURFace field) effect and was discovered by J.A. Appels and H.M.J. Vaes [9]. The principle is well known for bulk LDMOS [10–12] and has been extended for SOI structures [13, 14].

In bulk (see Fig. 2.30), the two-dimensional structure is composed of a lateral P^+-N diode and a vertical P^--N diode. In the OFF-state the depletion region extends into the

P^- substrate and all the way through the epitaxial N layer for a certain doping concentration and thickness. Hence the surface depletion width is increased and the horizontal component of the electric field is reduced, compared with the case with only the lateral diode. In other words, the surface field is reduced, and thus the breakdown voltage is increased.

In an SOI technology (see Fig. 2.30) the lateral P^+-N diode is again present, but the vertical diode is replaced by a buried oxide and N^+ substrate. In the OFF-state the electric field applied across the buried oxide induces a depletion region along the surface of the buried oxide, which allows a large surface depletion width and hence a low horizontal component of the electric field.

Let us now have a closer look at the charge and field distribution in the HV LDMOS, with a mind to optimising the RESURF effect. To achieve the highest possible avalanche breakdown, the horizontal component of the electric field in the depletion region has to be uniform. It can be proven that the doping distribution necessary to obtain this uniformity is given by [13]:

$$N(x) = \frac{\epsilon_{\mathrm{si}}\, V}{q\, X_{\mathrm{ddd}}\, t\, t_{\mathrm{bdr}}} x \tag{2.4}$$

where V is the total potential drop along the depletion region, X_{ddd} the length of the surface depletion width, t_{bdr} the thickness of the silicon film in the drift region and $t = \frac{\epsilon_{\mathrm{si}}}{\epsilon_{\mathrm{ox}}} t_{\mathrm{ob}} + \frac{t_{\mathrm{bdr}}}{2}$.

This linear lateral doping profile can be achieved using a sequence of small slit openings for masking the impurity implantation. These slits become increasingly small towards the P-N^- junction (junction between the channel and the drift region), so that a linear graded drift region is obtained.

The ideal breakdown voltage (V_{b}) for a RESURF device is given by [15]:

$$V_{\mathrm{b}} = \frac{B\, L_{\mathrm{dr}}}{\ln(A\, L_{\mathrm{dr}})} \tag{2.5}$$

where L_{dr} is the length of the drift region, $A = 7.03\ 10^5\ \mathrm{cm}^{-1}$, and $B = 1.47\ 10^6\ \mathrm{V{\cdot}cm}^{-1}$.

The design of a RESURF device should be based on equation 2.5 to calculate the length of the drift region for the desired breakdown voltage, and on equation 2.4 to find the graded doping profile. However these formulas will only be valid with the assumptions of a thin film and a thick oxide.

When the silicon film thickness is too large, or the buried oxide too thin, the vertical ionisation integral dominates, leading to vertical breakdown and causing the breakdown voltage to fall below its ideal value. Preliminary horizontal breakdown can occur when non-optimum drift charge causes crowding of the horizontal electric field near the gate electrode and drain electrode.

The HV LDMOS transistors are typically used in integrated bridge circuits. In these applications the source follower high side transistor has to float above the ground potential,

creating a voltage drop across the buried oxide since the substrate is connected to the ground potential. This causes parasitic effects, called high side (HS) effects. For the N-channel LDMOS, the drift region will become partially depleted at the back oxide leading to an increase in the on-resistance or even pinch-off of the drift region. However, once inversion is established along the buried oxide, both the width of the depletion layer and the on-resistance stay constant. Thus, pinch-off can be avoided, if the SOI film thickness is significantly larger than the depletion layer thickness at inversion.

This is not the case for the LDMOS in bulk technology, where the depletion layer width keeps increasing with increasing source potential, and hence the on-resistance will continue to increase as well. For this reason, the source-follower configuration becomes more difficult to realise in very high breakdown bulk devices [16, 17]. A reasonable on-resistance in bulk technology would necessitate an increase in the device area and make it less suitable for PICs.

2.5 Linear and saturation regions for the LDMOS

For a simple NMOS two operation regions can be considered when the transistor is in the ON-state: the linear region and the saturation region. For an LDMOS, both the MOS part and the JFET-like drift part can be in the linear region or in the saturation region. It is important to know for which bias conditions these different situations happen, because this determines the different measurement set-ups for parameter extraction and optimisation which are performed in the next chapter. Based on the previous sections in this chapter, 4 different situations can be considered:

- $V_{\mathrm{GfS}} \gg V_{\mathrm{DS}}$: MOS part in linear region and JFET-like drift region in linear region
- $V_{\mathrm{DS}} \gg V_{\mathrm{GfS}}$ and $V_{\mathrm{DS}} < V_{\mathrm{Psat}}$, the pinch-off voltage of the drift region: MOS in saturation region and JFET-like drift region in linear region.
- $V_{\mathrm{DS}} \gg V_{\mathrm{GfS}}$ and $V_{\mathrm{DS}} > V_{\mathrm{Psat}}$: MOS in saturation region and JFET-like drift region in saturation region.
- $V_{\mathrm{GfS}} - V_{\mathrm{thL}} > V(L_{\mathrm{eff}})$ and $V_{\mathrm{DS}} > V_{\mathrm{Psat}}$, with V_{thL} being the threshold voltage of the drain end of the MOS part, and $V(L_{\mathrm{eff}})$ the voltage at the drain end of the MOS channel: MOS in linear region and JFET-like drift region in saturation region. Note that this situation is not always possible; with very short lengths of the drift region it is usually impossible to have pinch-off in the drift region without having pinch-off in the inversion channel as well.

Depending on the bias conditions certain model parameters have more influence than others. If for example the MOS part is in the linear region and the drift region is in saturation, only the parameters which characterize this particular behaviour will be optimised.

2.6 Thermal behaviour of the LDMOS

Numerous applications for PICs which require high temperature operation are emerging, such as automotive and aircraft control. This temperature rise can seriously degrade device performance and reliability. Also, the self-heating effect plays a major role for DC, AC and transient characteristics of SOI power devices, since the buried oxide creates a high thermal resistance layer. The self-heating effects increase with increasing buried oxide thickness and decreasing silicon thickness [18, 19]. In ultra-thin RESURF SOI structures the heat generation in the drift region will have a spatial distribution (with a maximum at the side of the P-N^- junction where the doping concentration is lowest), but it will be quite uniform in thicker devices [17, 20].

In the compact model developed in Chapters 4 and 5, a thermal node is included, so that all self- and coupled heating effects can be simulated. Details about the implementation of the thermal node can be found in Sec. 4.4.

Here we have a closer look at the key temperature dependent parameters. The saturation velocity, the mobility and the threshold voltage all strongly influence the linear and saturation current characteristics. Other important temperature dependent parameters are the leakage current and the breakdown voltage.

2.6.1 Saturation velocity and mobility

The thermal dependence of the low-field carrier mobility is given by

$$\mu_0(T) = \mu_0(T_{\text{amb}}) \cdot \left(\frac{T}{T_{\text{amb}}}\right)^{-k} \tag{2.6}$$

with T being the absolute temperature and T_{amb} the ambient temperature in degrees Kelvin. The values of $\mu_0(T_{\text{amb}})$ and k depend strongly on the doping concentration of the silicon [1]. At low doping concentrations ($N_{\text{D}} < 10^{15}$ /cm^3) lattice scattering dominates the mobility behaviour. In the region of interest for the operation of the devices under study here, we have, for electrons [22]:

$$\mu_{0\text{n}}(T) = 1360 \text{ cm}^2/(\text{V} \cdot \text{s}) \cdot \left(\frac{T}{300}\right)^{-2.42} \tag{2.7}$$

and for holes [23]:

$$\mu_{0\text{p}}(T) = 495 \text{ cm}^2/(\text{V} \cdot s) \cdot \left(\frac{T}{300}\right)^{-2.2} \tag{2.8}$$

For higher doping concentrations the effect of ionised impurities or Coulomb scattering of the free carriers reduces the mobility. However, the ionised impurity scattering exhibits a positive temperature coefficient, which decreases the temperature coefficient of the mobility, k. In the LV and MV devices from PHILIPS, k is found to be 2.2 for $\mu_{\text{dr}} = 1450$ cm^2/(V·s), the mobility of the N^- drift region.

[1] For the interested reader, the electron and hole mobility are plotted as a function of the temperature and the doping concentration in [21] on page 7.

The mobility of carriers in an inversion or accumulation layer are limited by several additional scattering processes: surface phonon scattering due to lattice vibration, additional Coulomb scattering due to a fixed oxide charge and interface states, and surface roughness scattering. The last of these causes the surface mobility to decrease with increasing electrical field and is predominant under strong inversion conditions. The maximum effective mobility in surface layers decreases with increasing substrate doping [21]. This is not due to enhanced ionised impurity scattering, but arises from the higher electric field necessary to create an inversion layer.

The carriers in an accumulation layer are distributed further from the surface than in the case of inversion layers. Therefore surface mobility in accumulation layers is expected to be higher than in inversion layers, because the surface roughness scattering is less severe.

The thermal dependence of the maximum surface carrier mobility is given by:

$$\mu_{\mathrm{s}}(T) = \mu_{\mathrm{s}}(T_{\mathrm{amb}}) \cdot \left(\frac{T}{T_{\mathrm{amb}}}\right)^{-k} \tag{2.9}$$

The parameter k is usually assumed to be 1.5 for CMOS, while for DMOS it is observed to be 2.5 [24] which is significantly higher. In CMOS the slower temperature variation of the carrier mobility is due to the variation of the Fermi level, which determines, for a given surface field, a different electron distribution, and therefore a different shape of the vertical component of the electric field [25]. In the double diffused channel of a DMOS, due to the higher peak doping concentration and graded doping profile, both the variation of the relaxation time and of the Fermi level are important [24]. The relaxation time varies with the temperature as $T^{-2.5}$, according to experimental data on electron bulk mobility [26], and hence explains the higher value of k for LDMOS transistors. In the LV and MV devices from PHILIPS k is found to be 1.7 for the inversion layer mobility ($\mu_{\mathrm{s}}(300) = 750\ \mathrm{cm^2/(V{\cdot}s)}$), and 2.0 for the accumulation layer mobility ($\mu_{\mathrm{acc}}(300) = 750\ \mathrm{cm^2/(V{\cdot}s)}$).

When the lateral electric field strength is small, the carrier velocity will increase linearly in proportion to the electric field. Under higher lateral electric fields (10^4-10^5 V/cm in silicon) the velocity saturates. The saturation velocity is an important parameter that is required for the description of the behaviour of LDMOS devices operating in the presence of very high fields. The temperature dependence of the saturation velocity for electrons can be modelled as [26]

$$v_{\mathrm{sat}} = \frac{2.4 \cdot 10^7 \mathrm{cm/s}}{1 + 0.8 \cdot \exp\left(\frac{T}{600\ \mathrm{K}}\right)} \tag{2.10}$$

2.6.2 Threshold voltage

The threshold voltage for an LDMOS transistor is (just as for CMOS) given by

$$V_{\mathrm{th0}} = V_{\mathrm{FB}}^{\mathrm{f}} + 2\ \phi_{\mathrm{F}} + \gamma_0\ \sqrt{2\phi_{\mathrm{F}} - V_{\mathrm{BS}}} \tag{2.11}$$

where both the flat band voltage, $V_{\mathrm{FB}}^{\mathrm{f}}$ and the Fermi potential, ϕ_{F} are dependent on the temperature. For the LDMOS, we use N_{As}, the maximum doping concentration in the channel near the source, to calculate ϕ_{F}, $V_{\mathrm{FB}}^{\mathrm{f}}$, and γ_0. For applications above 50 K it has been found that the threshold voltage can be modelled very accurately as a linear function of temperature [27]:

$$V_{\mathrm{th0}}(T) = V_{\mathrm{th0}}(T_{\mathrm{amb}}) + \chi\, \Delta T \tag{2.12}$$

where χ is a temperature coefficient which can be easily extracted from threshold voltage measurements at different temperatures. A value of -3.3·10^{-3} V/K was found for χ, which is a quite high value compared with a normal SOI NMOS, where χ varies between -1·10^{-3} and -3·10^{-3} V/K [28]. This is expected because $\frac{dV_{\mathrm{th0}}}{dT}$ increases with the doping concentration [26], and the doping at the source side for an N-LDMOS is higher than the doping in the channel of most common NMOS transistors. The main doping dependent term in the Eq. 2.11 is $\gamma_0\sqrt{2\phi_{\mathrm{F}} - V_{\mathrm{BS}}}$, and hence the main doping dependent term in $\frac{dV_{\mathrm{th0}}}{dT}$ is

$$\frac{dV_{\mathrm{th0}}}{dT} \sim \gamma_0\, \frac{d\phi_{\mathrm{F}}}{dT}\, \frac{1}{\sqrt{2\phi_{\mathrm{F}} - V_{\mathrm{BS}}}} \tag{2.13}$$

with $\gamma_0 = \frac{\sqrt{2\epsilon_{\mathrm{si}} q N_{\mathrm{As}}}}{C_{\mathrm{of}}}$. Thus, the threshold voltage will not only vary at a higher rate with the temperature for higher substrate doping levels, but also for thicker gate oxides. Indeed, the γ_0 factor contains the factor t_{of} in the denominator via C_{of}. In the HV SOI technology the front oxide is usually quite thick compared with the more advanced CMOS processes, which also explains the higher value of χ.

2.6.3 Drain current

Current saturation is mainly caused by velocity saturation [29]. When the device temperature is increased the saturation velocity and mobility are strongly reduced, which reduces the saturation current. On the other hand, the threshold voltage decreases with increased temperature, but this effect is less pronounced. Hence, as a consequence of the large self-heating in SOI LDMOS transistors, the slope of the drain current versus drain voltage characteristic can become negative in saturation.

2.6.4 Leakage current

The leakage current to the body consists of a generation and a diffusion component of the reverse biased $P - N^-$ junction and can be written as [26]

$$I_{\mathrm{rd}} = q\, A \sqrt{\frac{D}{\tau}}\, \frac{n_{\mathrm{i}}^2}{N_{\mathrm{D}}} + \frac{q\, A\, n_{\mathrm{i}}\, W}{\tau} \tag{2.14}$$

where the first term is the diffusion current and the second term the generation current. D is the diffusion constant and τ the space charge generation lifetime. For an SOI LDMOS, A is the area of the P-N^- body junction and the leakage will be rather small compared with a bulk structure, where A is dominated by the area of the N(drift)-P(substrate)

junction. It can be shown [26] that the generation term increases as $\exp(-E_g/2kt)$ with temperature, and the diffusion term with $\exp(-E_g/kt)$.

2.7 Switching behaviour

Considering high-speed applications at more than 1 MHz, LDMOS transistors on SOI substrates are more attractive than the SOI-IGBTs because of the better high-frequency switching performance.

Thin film SOI power MOSFETS have smaller parasitic capacitances than power MOSFETs fabricated on a conventional bulk substrate. However, some care must be taken in designing these transistors because an additional drain-substrate capacitance results from the use of an SOI substrate [30, 31].

Compared with a conventional MOSFET on SOI, the SOI-LDMOS has an additional drain-substrate capacitance associated with the area of the drift region and will give rise to an additional contribution to the output capacitance. This will increase the turn-off time of the transistor since this output capacitance has to be discharged through the rather large load resistance. This drain to substrate capacitance becomes smaller when the transistor is used under high side conditions; as the source goes high, an inversion layer is formed along the surface of the buried oxide interface in the drift region which increases the capacitance between the body and the substrate but decreases the capacitance between the drain and the substrate.

To limit this capacitance L_{dr} and t_{bdr} have to be as small as possible and t_{ob} has to be increased, but of course for the HV LDMOS these parameters still have to satisfy the RESURF conditions. An expression for this capacitance is given by

$$C_{dsub} = \epsilon_{ox} \frac{(L_{dr} - X_{ddd})\, W}{t_{ob} + d} \tag{2.15}$$

with X_{ddd} the depletion width from the P-N junction in the drift region, W the width of the transistor, and d the thickness of the depletion layer formed at the buried oxide.

2.8 Influence of High Side Behaviour

2.8.1 Influence of High Side Behaviour on LDMOST

When an LDMOS is used in high side switching applications, high voltages can appear across the back oxide. This leads to an increased resistance of the N^- region under LOCOS. The source-high condition with grounded back gate is equivalent to a negative back gate voltage and a grounded source. To analyse the high side behaviour the effect of a negative back gate voltage was simulated with ATLAS.

As V_{GbB} is made increasingly negative, the depletion layer at the buried oxide in the drift region grows, and at a certain voltage, the surface at the buried oxide becomes inverted, starting at the left side of the drift region where the channel potential is lowest.

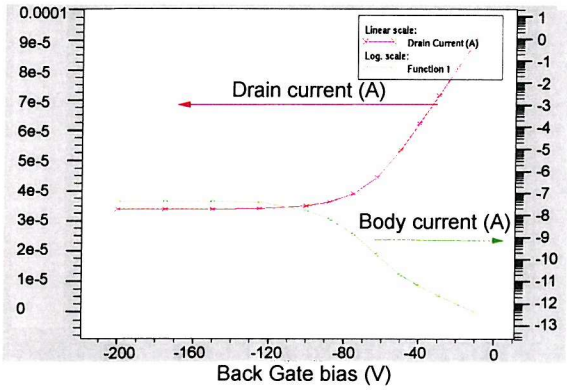

Figure 2.31: The drain and body current in terms of V_{GbB} in the MV SOI LDMOS for $V_{\mathrm{DS}} = 10$ V and $V_{\mathrm{GfS}} = 8$ V.

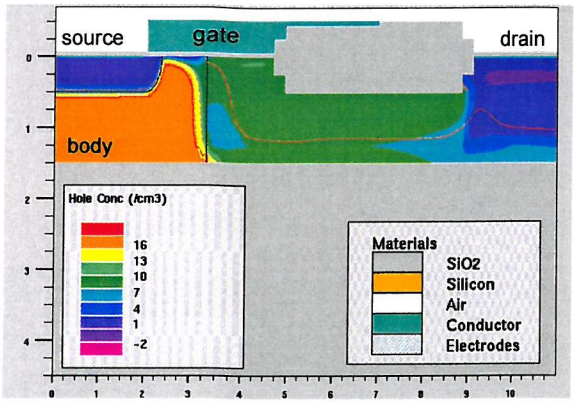

Figure 2.32: The hole concentration in the MV SOI LDMOS for $V_{\mathrm{GbB}} = -30$ V, $V_{\mathrm{DS}} = 10$ V and $V_{\mathrm{GfS}} = 8$ V.

This is illustrated in Figs. 2.32 to 2.34. For $V_{\mathrm{GbB}} = -30$ V, the hole concentration at the buried oxide interface is negligible. For $V_{\mathrm{GbB}} = -100$ V (Fig. 2.33) the surface is partly inverted and for $V_{\mathrm{GbB}} = -200$ V (Fig. 2.34) the inversion layer at the buried oxide reaches the drain end of the channel. This is what one could have expected, because threshold for inversion at the buried oxide at a point in the channel depends on the local channel potential ψ_{ch}, and is given by

$$V_{\mathrm{th0}}^{\mathrm{bdr}} = V_{\mathrm{FB}}^{b} - 2\,\phi_{\mathrm{F}} - \gamma^{\mathrm{bdr}}\,\sqrt{2\phi_{\mathrm{F}} + \psi_{\mathrm{ch}}} \tag{2.16}$$

At the drain end of the channel, $V_{\mathrm{th0}}^{\mathrm{bdr}} = -166$ V for $V_{\mathrm{DB}} = 10$ V. Decreasing the back gate bias below this value only increases the inversion layer charge and causes no more changes to the depleted area. The resistance of the drift region is now a constant, since the width of the depletion layer is fixed.

In Fig. 2.31 the simulated drain and body current are plotted as a function of the back gate voltage. The drain current first decreases with increasingly negative back gate voltage, but once inversion is established the current stabilises. Another interesting characteristic is the body current due to impact ionisation. It can be seen that the body current increases with decreasing back gate bias, and saturates when inversion is established along the buried oxide. An increased thickness of the depletion layer at the buried oxide interface confines the channel and increases the electric field at the drain, causing more impact generation. Furthermore, the inverted hole layer forms a current path for the holes generated by impact ionisation, which can now reach the body more easily through this path. These two factors explain the increase in body current with increasingly negative back gate bias until an inversion layer is present along the whole length of the buried oxide. This increased hole current will raise the body potential, and if the body resistance is quite high, this effect can turn on the parasitic bipolar transistor leading to early breakdown.

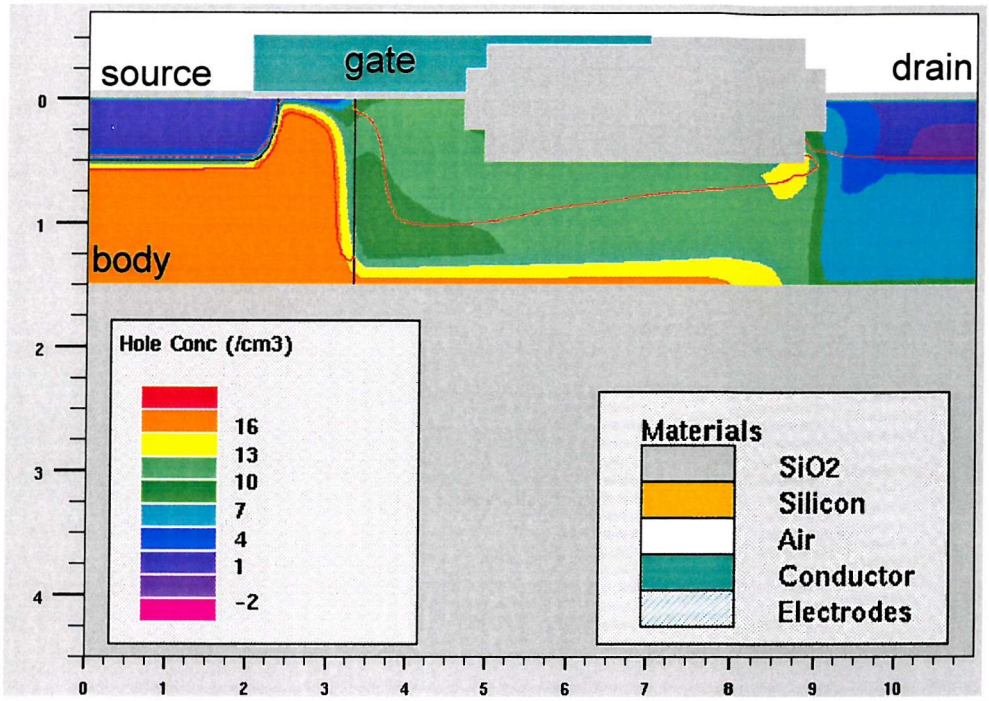

Figure 2.33: The hole concentration in the MV SOI LDMOS for $V_{\mathrm{GbB}} = -100$ V, $V_{\mathrm{DS}} = 10$ V and $V_{\mathrm{GfS}} = 8$ V.

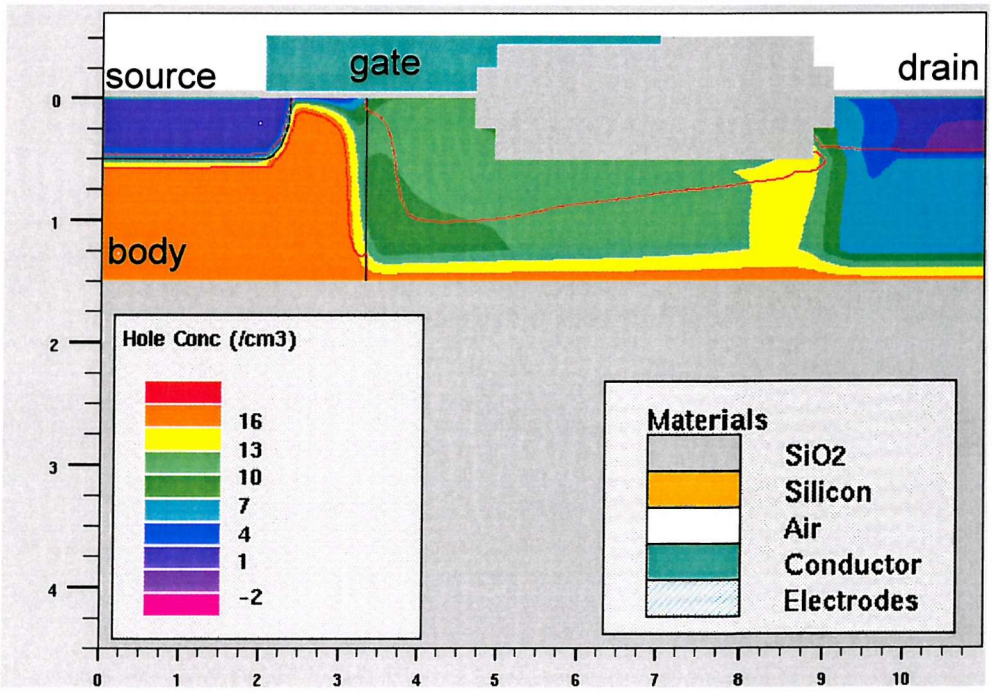

Figure 2.34: The hole concentration in the MV SOI LDMOS for $V_{\mathrm{GbB}} = -200$ V, $V_{\mathrm{DS}} = 10$ V and $V_{\mathrm{GfS}} = 8$ V.

2.8.2 Influence of High Side Behaviour on SOI CMOS

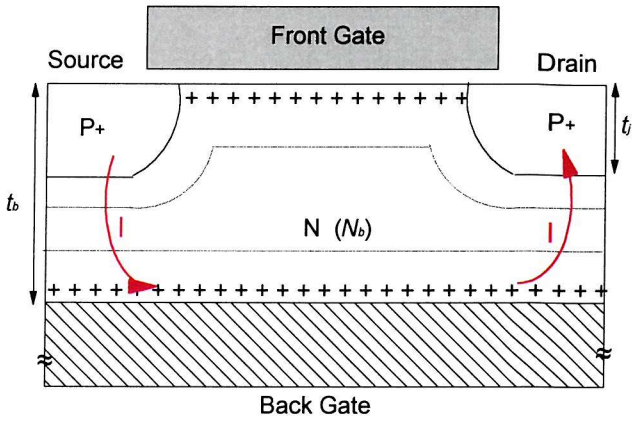

Figure 2.35: Simplified cross section of the PMOS used under high side conditions.

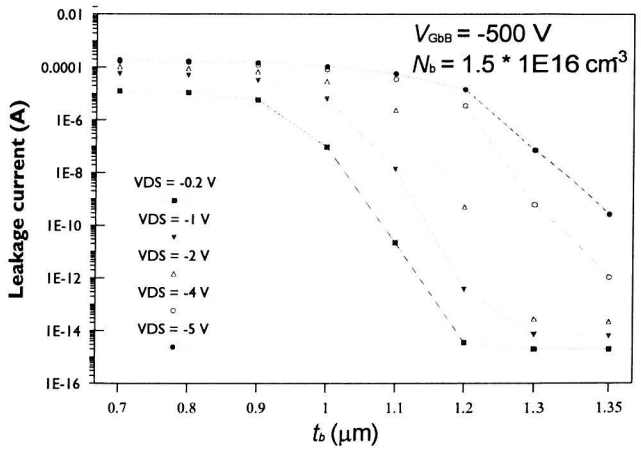

Figure 2.36: Simulated leakage current in terms of t_b for a PMOS with $N_b = 1.5 \cdot 10^{16}$ /cm^3, $V_{GfB} = 0$ V and $V_{GbB} = -500$ V.

The HS working conditions will also cause parasitic effects on the CMOS circuits controlling the source follower. For the SOI NMOS this will have no major effects; the back gate will become accumulated but this will not influence the electrical behaviour of the NMOS.

For PMOS, on the other hand, the hole inversion layer formed at the back oxide can cause serious leakage and charge displacement currents. To study these effects the leakage current of the SOI PMOS (see Fig. 2.35) was simulated with the device simulator Atlas [2]. The results are shown in Figs. 2.36 to 2.38. The drain leakage will increase drastically with substrate voltage if the doping concentration along the bottom (N_b) is low, and if the distance between the junctions and the back gate is small; under these conditions a back channel inversion layer can be formed and a current path exists between the S and D regions. Hence the on-characteristic of the transistor will depend on the substrate voltage.

Parameters that strongly influence this effect are the silicon thickness t_b minus the junction depth t_j, and the bottom doping concentration N_b. Above a critical value for the

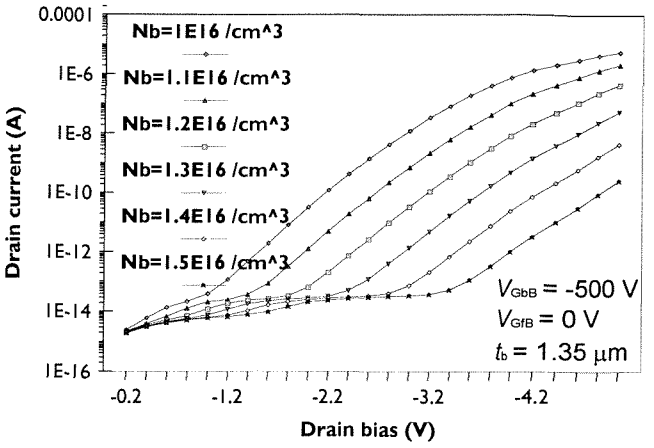

Figure 2.37: Simulated leakage current in terms of N_b for a PMOS with $t_b = 1.35$ μm, $V_{GfB} = 0$ V and $V_{GbB} = -500$ V.

drain bias the leakage becomes significant. This critical bias depends on

- the distance between the junction and the buried oxide: this is illustrated in Fig. 2.36; for $N_b = 1.5 \cdot 10^{16}$ /cm^3 the minimum silicon thickness required to avoid leakage is 1.35 μm; and
- the bottom doping concentration: this is illustrated in Fig. 2.37; for $t_b = 1.35$ μm, N_b has to be higher than $N_b = 1.4 \cdot 10^{16}$ /cm^3.

In Fig. 2.38 the leakage current is plotted in terms of the drain voltage for different values of N_b and t_b. From Fig. 2.38 (a) it can be seen that the leakage current can be very important if too small a value for the silicon thickness is chosen. For values closer to the critical N_b and t_b, serious leakage only occurs for higher drain biases (see Figs. 2.38 (b) to (d)). This leakage current needs either to be avoided by changing the process parameters, or else it needs to be modelled accurately, so that circuit designers can take account of it.

For the P-channel LDMOS [32, 33] the same problems are encountered as for the P-channel CMOS but this device is normally not used for high side and this problem is not treated here.

2.9 Summary

Modelling of a transistor demands a full comprehension of the physics of the device. In this chapter, we have given an overview of the typical structures for LV, MV and HV LDMOS transistors and have described the special electrical and thermal behaviour. The P-body of the LDMOS is formed by under-diffusion of a P-well under the gate and hence the doping at the source side is higher than at the drain side of the MOSFET channel. A new characterisation method for this lateral body doping gradient coefficient was developed and the consequences of this gradient on the charge behaviour have been described. The impact

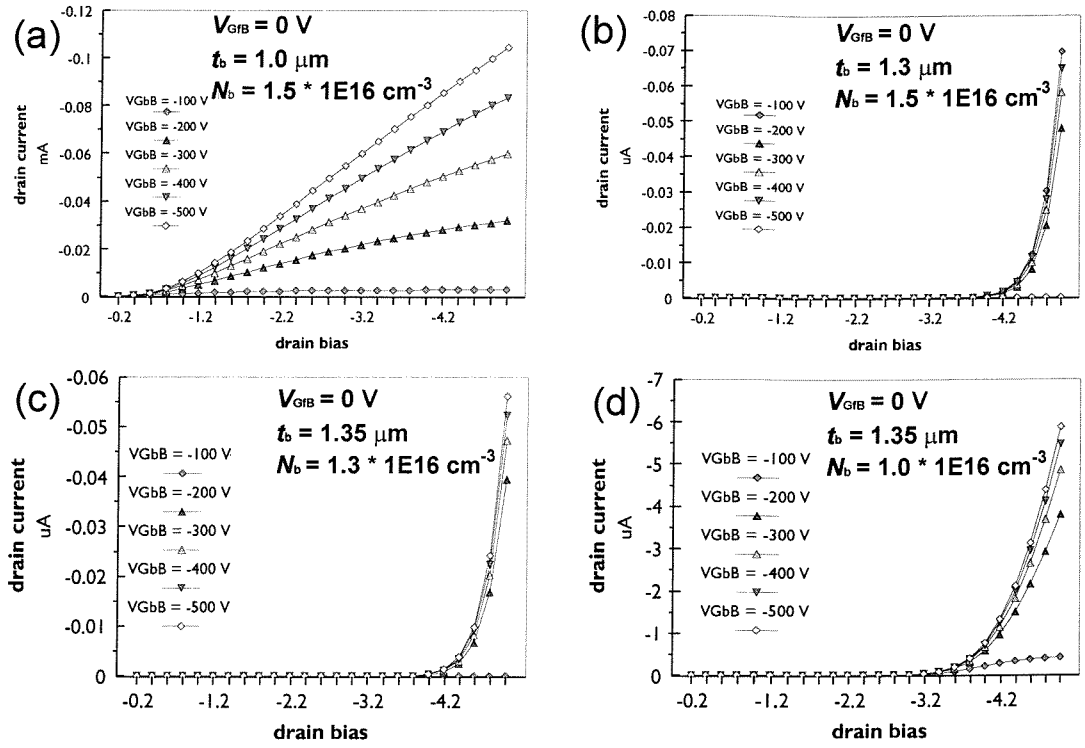

Figure 2.38: Simulated leakage current in terms of V_{DB} for a PMOS with $V_{GfB} = 0$ V and $V_{GbB} = -500$ V; (a) $N_b = 1.5 \cdot 10^{16}$ /cm^3, $t_b = 1.0$ μm; (b) $N_b = 1.5 \cdot 10^{16}$ /cm^3, $t_b = 1.3$ μm; (c) $N_b = 1.3 \cdot 10^{16}$ /cm^3, $t_b = 1.35$ μm; (d) $N_b = 1.0 \cdot 10^{16}$ /cm^3, $t_b = 1.0$ μm.

ionisation phenomenon has been fully explained for both the LV and MV LDMOS. The important parameters for thermal and switching behaviour have been discussed. Finally, the unique effects on the LDMOS and the CMOS transistors , when these components are used under high side conditions, as in a typical half-bridge configuration, have been explained in detail.

With this knowledge about the device physics of the LDMOS, the development of a circuit simulator model can commence and this is our goal in the following chapters.

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Chapter 3

A Subcircuit Model for the LDMOS

3.1 Introduction

A subcircuit model for the LV and MV LDMOS is being developed in this chapter to meet the urgent needs of the circuit designers for smart power IC design. The main advantages of the subcircuit modelling approach are that the model can be implemented in nearly every circuit simulator, that it can be built in a relatively short time, and that it requires relatively little programming skill. The drawbacks are a higher degree of complexity, compared with a compact model, and hence an increase in computation time and a more complex parameter extraction procedure. Since the device models used in the subcircuit model are not specifically designed to be combined in this way, the description of the device physics is less accurate.

The model consists of two parts: the pre-processing part where all the model parameters are calculated from the physical and extracted parameters and where the geometry scaling is done; and a second part containing the actual description of the subcircuit model.

To build the sub-circuit model, we will use a combination of elements provided by the PSTAR [1] simulator of PHILIPS. The PSTAR library contains different MOSFET models and JFET models from which we chose the most appropriate ones to describe the behaviour of the LDMOS [2]. The choices made are based on the physical study done in the previous chapter.

Finally, the parameter extraction and optimisation procedure are described and DC simulations are compared with the real-world.

3.2 The LV N-LDMOS Model

A detailed description of the models used in the subcircuit model for the LV LDMOS can be found in [3]. In this section, a short description of the employed models is given. The reasons behind the choice of these components are discussed, and we explain what the

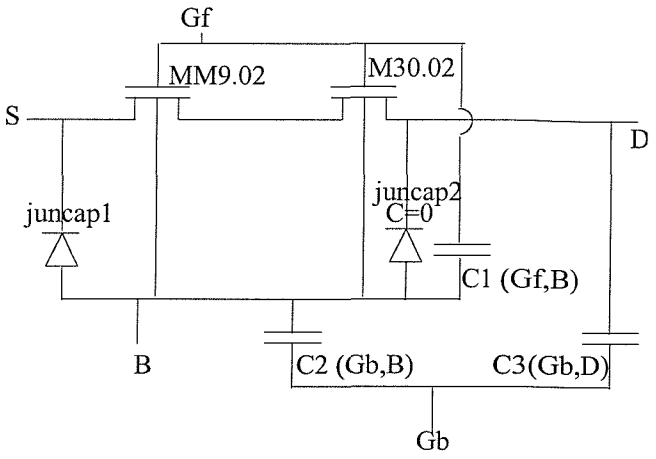

Figure 3.1: The Pstar model for the LV LDMOS.

meaning of their parameters becomes when they are used to model an LV LDMOS. The subcircuit model for the LV LDMOS consists of a MOS Model 9.02 (the normal PHILIPS MOST model) [4] in series with a MOS Model 30.02 [5] (a depletion type MOSFET) [6], two JUNCAP [7] models to describe the source to body and drain to body junctions, and a couple of voltage dependent capacitances that will be described below. The capacitance of the drain to body junction has to be set to zero because it is already included in the MOS3.002 model as will be explained below.

3.2.1 MOS Model 9.02

MOS Model 9.02 (MM9.02) is the name for a recent version of the PHILIPS MOST model. This model is of the *regional* type (also called a *threshold voltage based* model), which means that the MOSFET behaviour is divided into a weak and strong inversion region. Another approach to model a MOSFET is referred to as the *single-piece* or *surface potential based* type [8].

The equations modelling the device are based on the gradual channel approximation. The model is charge conserving and includes channel length modulation, short-channel effects, floating body effects, impact ionisation and DIBL. For a full description refer to the MM9 report [9] and to [10]. In App. B we give a list of the parameters for an individual transistor at a certain temperature; there, the length, width and temperature scaling is performed in the pre-processing phase.

In an LDMOS device the MOSFET action takes place in the P-region under the front gate, and this is where MM9.02 is used. As explained in the previous chapter, the doping in the P-region of an LDMOS decreases from the source side towards the internal node (the P-N^- junction). MM9.02 assumes a homogeneous doping along the surface, but can still lead to a good approximation of the DC current, provided the doping concentration at the source side is used to calculate the threshold voltage. The body factor uses an effective value for the doping concentration. As we shall see in Chapter 4, the influence of

the doping gradient on the output characteristic is almost negligible for high gate voltages, though quite important for gate voltages around the threshold and in the linear region. Furthermore, it plays a very important role in the charge behaviour of the LDMOS as will become clear in Chapter 5.

3.2.2 JUNCAP model

The JUNCAP model is intended to describe the behaviour of the diodes that are formed by the source/drain-to-bulk junctions in MOS devices. The model is limited to the case of reverse biasing of these junctions. Both the diffusion and the generation currents are treated in the model, each with its own temperature and voltage dependence. For a detailed description of the equations, refer to [7].

3.2.3 The Depletion Mode MOSFET for the Drift Region Modelling (M30.02)

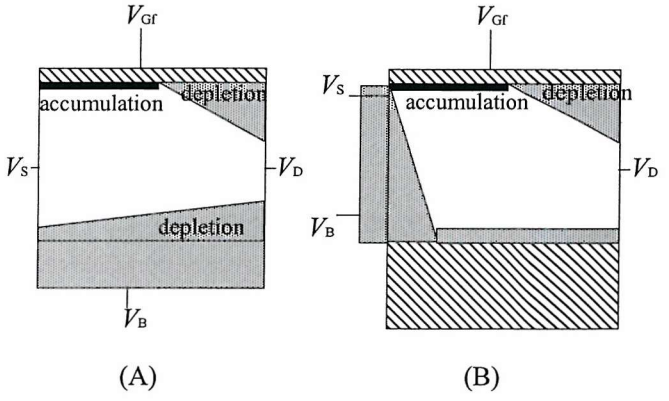

Figure 3.2: Representation of (a) M30.02. (b) M30.02 used to model the drift region of the LDMOS.

M30.02 is the name for a depletion type MOSFET model [5], which is used to describe the drift region. The depletion mode MOSFET is a semiconductor device whose operation is achieved by depleting an already existing channel via a gate controlled surface depletion, or via a voltage controlled buried P-N junction. The model assumes a device cross section as shown in Fig. 3.2(a). At the surface the channel is terminated by a MOS capacitor with an oxide thickness t_{of}. At the bottom the channel is terminated by a reverse-biased P-N diode, which is assumed to have an abrupt bias profile. In M30.02, first the ohmic current flow is calculated. This current reaches a maximum value when the drain voltage is equal to the so-called pinch-off voltage (V_P). At this voltage the depletion regions of the substrate and the gate touch at the drain side and the net charge in the channel at the drain end is zero. If the drain voltage is higher than V_P the current saturates [1].

[1] This is not velocity saturation, but saturation by pinch-off

The effect of velocity saturation is accounted for by means of three parameters: V_{SAT}, the critical drain-source voltage for hot carriers, R_{SAT}, the space charge resistance at zero bias and P_{SAT}, a coefficient to make the transition between the ohmic and saturation region smoother.

In summary, M30.02 includes accumulation at the surface, depletion from the surface and from the bulk, pinch-off mode, velocity saturation, a gate charge model, and a substrate charge model. Two major drawbacks are that the model does not include inversion for negative gate biases and does not account for any impact ionisation current. A list of the parameters is given in App. B.

In the case of the LDMOS, this model is used to describe the cross section shown in Fig. 3.2(b): the body-substrate junction is rotated through 90 degrees and hence the shape of the channel differs from the cross section of the normal depletion MOS (Fig. 3.2(a)). The consequence is that some parameters need to be calculated in a somewhat different way, and some cannot be calculated using a simple analytical formula. This is the case for the following parameters:

- In the normal M30.02, the on-resistance for zero gate and body bias (R_{ON}, App. B), is given by

$$R_{\mathrm{ON,M30.02}} = \frac{L_{\mathrm{drov}}}{W\ \mu_{\mathrm{dr}}\ q\ N_{\mathrm{D}} \cdot \left(t_{\mathrm{b}} - d(V_{\mathrm{GfB}} = V_{\mathrm{SB}} = V_{\mathrm{DB}} = V_{\mathrm{GbB}} = 0)\right)} \tag{3.1}$$

  with L_{drov} the length of the drift region under the thin gate oxide, W the width of the drift region, μ_{dr} the mobility, N_{D} the doping concentration in the drift region, t_{b} the silicon thickness and $d(V_{\mathrm{GfB}} = V_{\mathrm{SB}} = V_{\mathrm{DB}} = V_{\mathrm{GbB}} = 0)$ the thickness of the non-depleted channel under zero bias conditions.

  For the LDMOS, we have used the expression:

$$R_{\mathrm{ON,LVLDMOS}} = \frac{L_{\mathrm{drov}} + k_{\mathrm{RON}}\ t_{\mathrm{b}}}{W\ \mu_{\mathrm{dr}}\ q\ N_{\mathrm{D}}\ t} \tag{3.2}$$

  In the drift region of an LDMOS the length of the current path also depends on the silicon thickness, since the current is flowing vertically. For this reason the term $k_{\mathrm{RON}}\ t_{\mathrm{b}}$ is added to the length of the drift region. The factor $k_{\mathrm{RON}} < 1$ needs to be determined by extraction. The thickness of the non-depleted channel t is much smaller than t_{b} and rather difficult to estimate as it is not a constant for the current path: t is very small at the source side and equal to t_{b} at the drain side. Therefore an effective value needs to be determined by extraction.

- For the structure of Fig. 3.2(a), the pinch-off voltage (V_{P}) at zero gate and body voltage can easily be calculated from an analytical expression (see [10]), but for the LDMOS the calculation is not straightforward. The device simulations in Secs. 2.2.2 and 2.3.2 provide an idea of the value V_{P} for the LV and MV LDMOS, but the final exact value has to be determined by extraction.

- The critical drain source voltage for velocity saturation, V_{SAT}, for the normal structure of Fig. 3.2(b), is given by

$$V_{\mathrm{SAT,M30.02}} = \xi_{\mathrm{c}}\, L_{\mathrm{drov}} \tag{3.3}$$

with ξ_{c} the critical electrical field. For the LDMOS we have adapted the equation to

$$V_{\mathrm{SAT,LVLDMOS}} = \xi_{\mathrm{c}} \cdot (L_{\mathrm{drov}} + k_{\mathrm{VSAT}}\, t_{\mathrm{b}}) \tag{3.4}$$

with $(L_{\mathrm{drov}} + k_{\mathrm{VSAT}}\, t_{\mathrm{b}})$ the length of the current path and k_{VSAT} a factor to account for the vertical current flow.

3.2.4 Modelling of the Capacitances

MM9.02 and M30.02 describe the charge behaviour along the front oxide, but inversion at the surface of the M30.02 is not included. Also MM9.02 and M30.02 do not account for the charge behaviour at the buried oxide interface. In this section three extra expressions are derived to account for these extra charges and their corresponding capacitances.

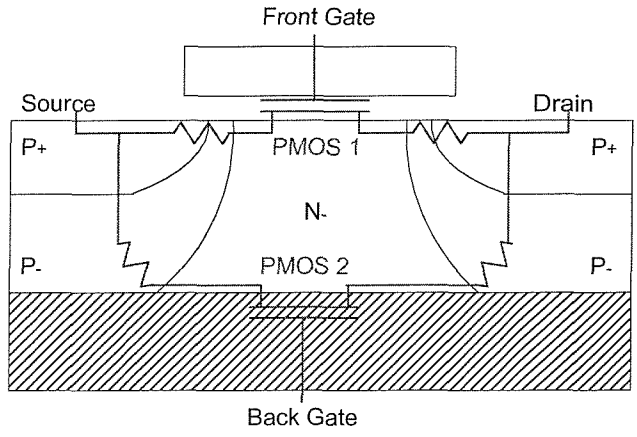

Figure 3.3: Structure of a PMOS device in the HV SOI process, and their corresponding subcircuit model.

Applying a gate voltage lower than the negative threshold voltage of the N^- drift region ($V_{\mathrm{th}}^{\mathrm{fdr}}$) inverts the surface under the front gate in the drift region. An extra gate-body capacitor is included to account for the resulting coupled increase in capacitance between the gate and the body. The threshold voltage of the channel through the N^- region depends on the drain voltage, which acts as the body voltage of the N^- region. The threshold voltage of the drift region is given by:

$$V_{\mathrm{th}}^{\mathrm{fdr}} = V_{\mathrm{th0}}^{\mathrm{fdr}} - \gamma^{\mathrm{fdr}} \cdot (\sqrt{V_{\mathrm{DB}} + 2\phi_{\mathrm{Fdr}}} - \sqrt{2\phi_{\mathrm{Fdr}}}) \tag{3.5}$$

where $V_{\mathrm{th0}}^{\mathrm{fdr}}$ and γ^{fdr} can be found from the threshold voltage and body factor respectively of a PMOS with the same N^- channel region (see PMOS 1 in Fig. 3.3).

The extra charge coupled between the gate and the body is given by

$$Q_1(Gf,B) = -C_{\rm of}\ W\ L_{\rm drov}\ \phi_{\rm t}\ \ln\left(1+\exp(-\frac{V_{\rm GfB}-V_{\rm th}^{\rm fdr}}{\phi_{\rm t}})\right) \tag{3.6}$$

with $L_{\rm drov}$ the length of the drift region under the thin front gate. Here the body voltage plays the role of "source" for the inverted "PMOS" hole layer along the surface of the thin gate oxide in the drift region; for this reason the gate bias in the above equation is referred to the body ($V_{\rm GfB}$). Hence we write

$$C_1(Gf,B) \;=\; \begin{cases} -C_{\rm of}\ W\ L_{\rm drov} & \text{for } -V_{\rm GfB} \gg -V_{\rm th}^{\rm fdr} \\ 0 & \text{for } -V_{\rm GfB} \ll -V_{\rm th}^{\rm fdr} \end{cases} \tag{3.7}$$

The capacitors between the body and the back gate and between the drain and the back gate are also included. They depend on the drain voltage in a similar way as $C_1(Gf,B)$ depends on $V_{\rm DB}$. The threshold voltage of the drift region at the buried oxide is given by:

$$V_{\rm th}^{\rm bdr} = V_{\rm th0}^{\rm bdr} - \gamma^{\rm bdr}\cdot(\sqrt{V_{\rm DB}+2\phi_{\rm Fdr}}-\sqrt{2\phi_{\rm Fdr}}) \tag{3.8}$$

where $V_{\rm th0}^{\rm bdr}$ and $\gamma^{\rm bdr}$ can be copied from the threshold voltage and the body factor of the buried PMOS transistor (PMOS 2) in a PMOS device with the same N^- channel region, as shown in Fig. 3.3.

The extra back gate-body charge is given by

$$Q_2(Gb,B) = C_{\rm ob}\ W_{\rm bob}\ L_{\rm bob}\ V_{\rm GbB} + C_{\rm ob}\ W_{\rm dob}\ L_{\rm dob}\ \phi_{\rm t}\ \ln(1+\exp(-\frac{V_{\rm GbB}-V_{\rm th}^{\rm bdr}}{\phi_{\rm t}})) \tag{3.9}$$

with $W_{\rm bob}$ and $L_{\rm bob}$ the width and the length of the P-body region at the buried oxide, and $W_{\rm dob}$ and $L_{\rm dob}$ the width and the length of the drift region at the buried oxide interface. The first term represents the capacitance between the P-region and the back gate. Because $V_{\rm GbB} \le 0$ in normal bias conditions, the surface in the P-region at the buried oxide interface is always in or close to accumulation, and so the first term in the above equation gives a good approximation for this charge. The second term represents the charge coupled between the back gate and the buried oxide surface in the N^- region. Hence

$$C_2(Gb,B) \;=\; \begin{cases} C_{\rm ob}\cdot(W_{\rm bob}\ L_{\rm bob}+W_{\rm dob}\ L_{\rm dob}) & \text{for } -V_{\rm GbB} \gg -V_{\rm th}^{\rm bdr} \\ C_{\rm ob}\ W_{\rm bob}\ L_{\rm bob} & \text{for } -V_{\rm GbB} \ll -V_{\rm th}^{\rm bdr} \end{cases} \tag{3.10}$$

The extra back gate-drain charge is given by

$$Q_3(Gb,D) = C_{\rm ob}\ W_{\rm dob}\ L_{\rm dob}\ V_{\rm GbD} + C_{\rm ob}\ W_{\rm dob}\ L_{\rm dob}\ \phi_{\rm t}\ \ln(1+\exp(-\frac{V_{\rm GbD}-V_{\rm th}^{\rm bdr}}{\phi_{\rm t}})) \tag{3.11}$$

The first term represents the capacitance between the drift region and the back gate. Because under normal bias conditions $V_{\rm GbD}$ is usually not sufficiently negative to cause

inversion, the surface of the drift region at the buried oxide interface is depleted, and the first term in the above equation gives an approximation for this charge. The second term compensates the first term once the buried oxide surface in the N^- region becomes inverted. The corresponding capacitance is given by

$$C_3(Gb, D) = \begin{cases} 0 & \text{for } -V_{\text{GbD}} >> -V_{\text{th}}^{\text{bdr}} \\ C_{\text{ob}}\, W_{\text{dob}}\, L_{\text{dob}} & \text{for } -V_{\text{GbD}} << -V_{\text{th}}^{\text{bdr}} \end{cases} \tag{3.12}$$

The three extra capacitors are represented in the schematic of Fig. 3.1.

3.2.5 Self Heating

Even more than in small geometry SOI devices, self-heating has a significant impact in SOI LDMOS technology. Self-heating results from the much lower conductivity of the thick buried oxide compared with normal silicon. In ultra-thin RESURF SOI structures the heat generation in the drift region will be non-uniform (with a maximum at the side of the P-N^- junction where the doping concentration is lowest) while it will be quite uniform in thicker devices. In the low and medium voltage LDMOS a uniform temperature distribution can be assumed since these devices are relatively thick and not very long.

Heat flow and temperature rise are modelled with the thermal circuit shown in Fig. 3.4. A resistance term represents the heat path to the substrate, and a capacitor represents

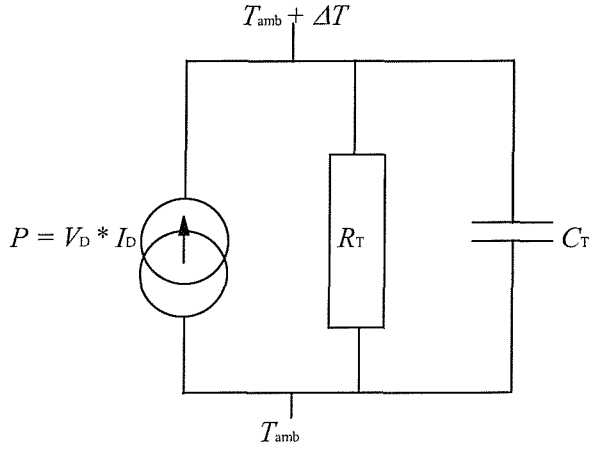

Figure 3.4: Thermal circuit to model self heating

the heat storage effects [11]. This first order approach has been selected, because normally second and third thermal time constants are less important [12]. Therefore, at this stage of the modelling, a single time constant is considered to be sufficient. As a first guess for R_T, we take the thermal resistance of the buried oxide, thus:

$$R_T = \frac{t_{\text{ob}}}{\kappa_{\text{ox}}\, W \cdot (L_{\text{dob}} + L_{\text{bob}})} \tag{3.13}$$

with κ_{ox} the thermal conductivity of SiO_2. Next this value was optimised by fitting measured to simulated current characteristics for different geometries, leading to a more

general equation for R_T. The thermal resistance of the buried oxide is put in series with a second thermal resistance, which is only dependent on the width:

$$R_T = \frac{1}{\frac{\kappa_{ox} W \cdot (L_{dob}+L_{bob})}{t_{ob}} + \frac{W}{r_{thc}}} \tag{3.14}$$

with r_{thc} a constant value. This term can be justified by the fact that we also have a heat path through the side and top LOCOS oxides, which scales with the width. The thermal capacity was not extracted for the subcircuit model, but only calculated from theory.

3.2.6 Model Implementation

The model implementation is done in two main blocks: the first one, referred to as the *process model*, calculates the electrical model parameters from the physical and extracted parameters. This block includes also the geometry scaling of the geometry dependent parameters. In the second block, called the model definition, the subcircuit schematic as shown in Fig. 3.1 is described.

The *process model* can be subdivided into four parts:

- part 1: the geometrical definitions, including the layout and the cross section of the component and all the lengths and widths used in the rest of the process model.
- part 2: list of the MM9.02 parameters for a device with a reference width, list of the width scaling parameters (no length scaling factors necessary since the LDMOS has a fixed length), and a block with the actual geometry scaling pre-processing.
- part 3: M30.02 parameters.
- part 4: JUNCAP parameters and other capacitor parameters (for C_1, C_2 and C_3).

The process model is executed only once during the simulation, while the actual subcircuit model definition is called at every iteration. If we want to account for the static and transient self-heating, we have to do the temperature scaling in the subcircuit model because the temperature change ΔT has to be recalculated at every iteration. In that way, the temperature dependent model parameters are recalculated for every bias point of a DC sweep and self-heating is taken into account. Note however that it is impossible to account for self-heating effects when performing an AC simulation. For this it is necessary to define a temperature node (see Sec. 4.4) within the different compact models used in the subcircuit. Because the output conductance increases with frequency due to the thermal time constant (typically in the range of 100 kHz to 1 MHz) it is important to have a thermal node within the compact model when doing AC simulations. This reasoning will be incorporated into the compact model developed in Chapter 4.

The subcircuit model definition is formulated, using PSTAR code in Table 3.1. Every line contains a comment (written as "c: comment"), explaining the code. This code describes the schematic of Fig. 3.1 and calculates the temperature increase due to static

self-heating.

```
model: LVLDMOS(D,Gf,S,B,Gb) -parameters-;
  MNE1(Dint,Gf,S,B,Gb) -parameters-; c: MM9.02;
  MN1(DX,Gf,Dint,B,Gb) -parameters-; c: M30.02;
  JUNCAP1(S,B) -parameters-; c: source-body diode;
  JUNCAP2(D,B) -parameters-; c: drain-body diode;
  C1(Gf,B) Q = Q1; c: extra capacitance;
  C2(Gf,B) Q = Q2; c: extra capacitance;
  C3(Gf,B) Q = Q3; c: extra capacitance;
  S1(D,DX); c: current source to measure the drain-source current.
       c: This is a trick to obtain the current, which is needed to
       c: calculate the self-heating;
  DTA=R_T*i(S1)*v(D,S); c: ΔT due to static self-heating;
  temp scaling equations;
end;
```

Table 3.1: *The subcircuit model definition as formulated for PSTAR.*

3.2.7 Extraction Strategy with ICCAP and Model Validation

No model is useful unless there is some way of obtaining a set of parameters from measured wafers. Here, a parameter optimisation strategy has been developed which divides the parameter set into groups. Separate optimisations on the different groups of parameters are then performed, using the appropriate measured data.

The parameters for the MOSFET (MM9.02) can be extracted in a way similar to an ordinary NMOS with the following differences: to obtain the threshold voltage (V_{th0}) and the gain factor β it is necessary to limit the linear characteristic to a couple of volts above the threshold voltage; this is before the drift region starts to play an important role. The output characteristics for the MM9.02 extraction procedure need to be measured only for low gate voltages, such that the main part of the applied drain voltage drops over the MOSFET channel.

For high V_{GfS} and medium V_{DS} values, the MOSFET channel has a very low resistance and is not pinched. Therefore the current saturation behaviour originates in the drift region and it is under these conditions that we extract the depletion MOSFET parameters.

The complete extraction procedure for the MM9.02 and the depletion mode MOSFET parameters is described in Table 3.2.

Measurement Set-up	MM9.02	M30.02
I_D-V_{GfS}, V_{GfS} just above V_{th0},V_{DS}=0.1V	β, V_{th0}	-
I_D-V_{GfS},V_{DS}=0.1V	γ_0, θ_2	-
I_D-V_{GfS},V_{DS}=0.1V, high V_{GfS}	-	V_P
I_D-V_{GfS},low V_{GfS}, V_{DS}=V_{Gfmax}/2,V_{Gfmax}	θ_1	-
I_D-V_{GfS},medium V_{GfS}, V_{DS}=V_{Gfmax}/2,V_{Gfmax}	θ_3	-
I_D-V_{GfS},high V_{GfS}, V_{DS}=V_{Gfmax}/2,V_{Gfmax}	-	V_{SAT}
g_{DS}-V_{DS}, V_{BS}=0V, V_{GfS}=V_{th0}+0.1V,..,V_{th0}+3.1	γ_1, α, V_P	-
I_{DS}-V_{DS}, V_{BS}=0V, V_{GfS}=V_{th0}+0.1V,..,V_{th0}+3.1	θ_1, θ_3	-
I_{DS}-V_{DS}, low V_{DS}, V_{GfS}=V_{Gfmax}-3V,..,V_{Gfmax}	-	R_{ON}
I_D-V_{GfS}, V_{GfS}=V_{th0}-0.5V,...,V_{th0}+0.5V, V_{DS}=0.1V,V_{Gfmax}/2,V_{Gfmax}, V_{BS}=0V	γ_{oo}, m_0, ζ_1	-
I_D-V_{GfS}, V_{GfS}=V_{th0}-0.5V,...,V_{th0}+0.5V, V_{DS}=0.1V,V_{Gfmax}/2,V_{Gfmax}, V_{BS}=0,-1,-2V	V_{SBT}	-
I_B-V_{GfS}, V_{DS}=V_{Dmax}-2V,...,V_{Dmax}, V_{BS}=0	A_1, A_2, A_3	-

Table 3.2: *Extraction strategy for the LV LDMOS parameters*

The extraction of the geometry and temperature scaling factors is done just as for the standard MOSFET model (MM9.02).

The measurements and simulations were performed within ICCAP [13]. ICCAP is a software package which is part of Agilent's EEsof's high frequency electronic design automation solutions. ICCAP can be used to measure semiconductor device and circuit characteristics, and to analyse the results. It also allows simulation and parameter optimisation.

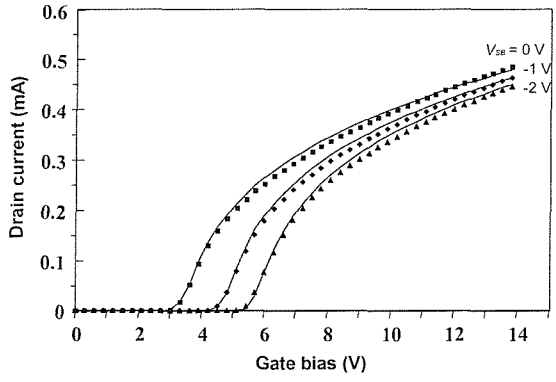

Figure 3.5: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ for V_{BS} = 0, -1, -2 V and V_{DS} = 0.25 V; W = 20 μm.

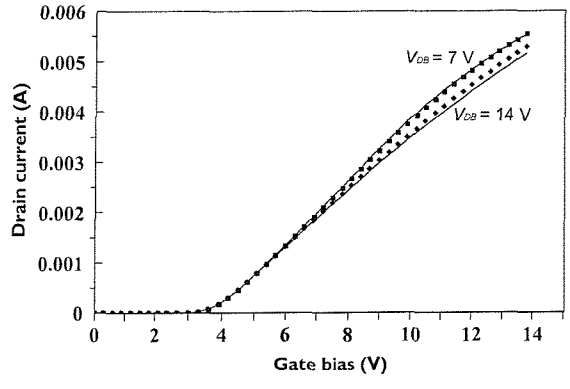

Figure 3.6: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ for V_{DS}=7V, 14V; W = 20 μm.

The ICCAP optimisation procedures are used for the extraction of the parameters,

but a fully convergent automatic extraction strategy has not yet been developed. The optimised parameters for the LV LDMOS can be found in App. B.

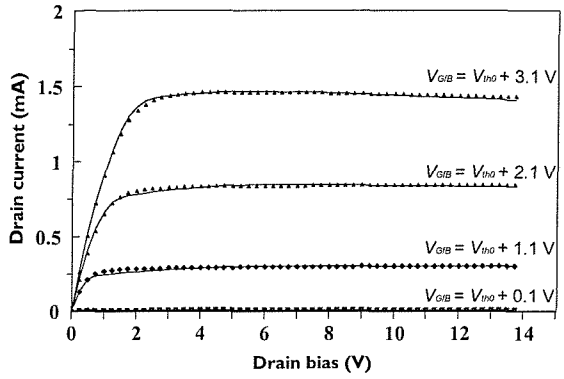

Figure 3.7: Measured (markers) and simulated (full line) $I_D(V_{DS})$ for $V_{BS} = 0$ V and V_{GfS}=$V_{th0} + 0.1$ V, V_{th0}+1.1 V, V_{th0}+2.1 V, V_{th0}+3.1 V; $W = 20$ μm.

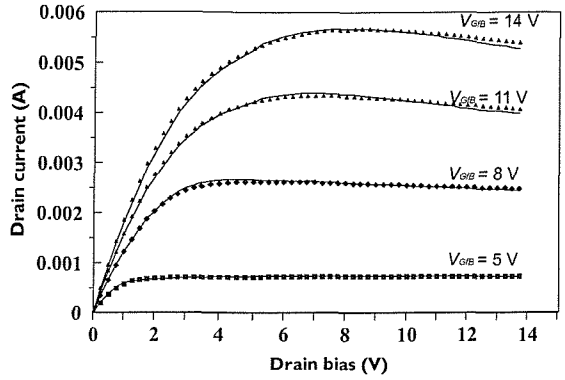

Figure 3.8: Measured (markers) and simulated (full line) $I_D(V_{DS})$ for $V_{BS} = 0$ V and $V_{GfS} = 5, 8, 11, 14$ V; $W = 20$ μm.

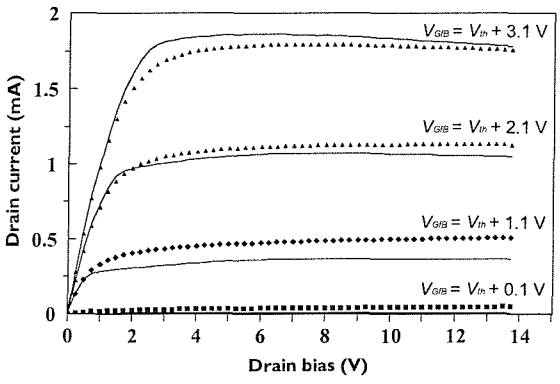

Figure 3.9: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ for $V_{BS} = -2$ V and $V_{GfS} = V_{th} + 0.1$ V, $V_{th} + 1.1$ V, $V_{th} + 2.1$ V, $V_{th} + 3.1$ V; $W = 20$ μm.

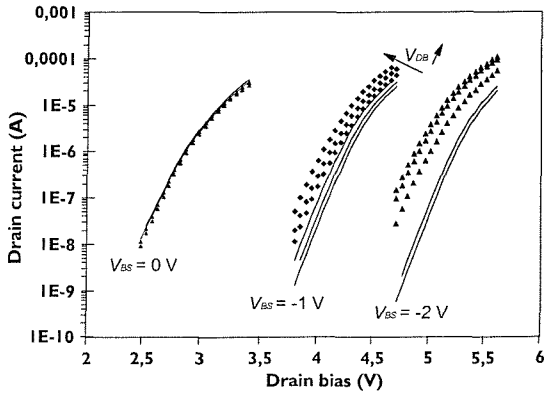

Figure 3.10: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ (around the threshold voltage) for $V_{BS} = 0$, -1, -2 V and $V_{DS} = 1$, 7.5, 14 V; $W = 20$ μm.

The final verification consists of the comparison between the measurements and the simulations from the subcircuit model; the figures above show the measured (marks) and simulated (full line) characteristics for an LV LDMOS with a width of 20 μm and a separate back gate.

Fig. 3.5 shows the linear characteristic for different body voltages. We notice the flattening of the curves for higher gate bias. This is due to the increasing influence of the drift region, which can be approximated as a series resistance. A good fit is obtained

between the simulated and measured values.

Fig. 3.6 shows the drain current as a function of the gate bias for two different high drain biases. For a normal MOSFET in saturation the drain current varies in a quadratic way with the gate voltage. Here this is only the case for very low gate biases, since then the drift region plays a less important role and the drain bias drops almost completely over the MOSFET part of the LDMOS. We also notice that the curve for $V_{DS} = 14$ V lies beneath the curve for $V_{DS} = 7$ V, which is explained by the large amount of self-heating resulting in a negative static output conductance.

Fig. 3.7 and 3.8 show the output characteristics for respectively lower and higher gate biases and a zero body voltage. For the lower gate biases the MM9.02 part plays the main role and for the higher gate biases the drift region modelled by M30.02 is crucial. We can see that both are well modelled and that the fits are very accurate in both plots.

Fig. 3.9 shows the output characteristic for a body voltage of -2 V. The fit is less accurate than for the previous plots. This is due to the fact that the current reduction, caused by increased depletion in the drift region, cannot be described very accurately by M30.02 (see Sec. 3.2.3).

Finally we show the sub-threshold plots in Fig. 3.10. We can see again that the fit is less accurate for non-zero body voltages, as explained above.

3.3 The MV Model

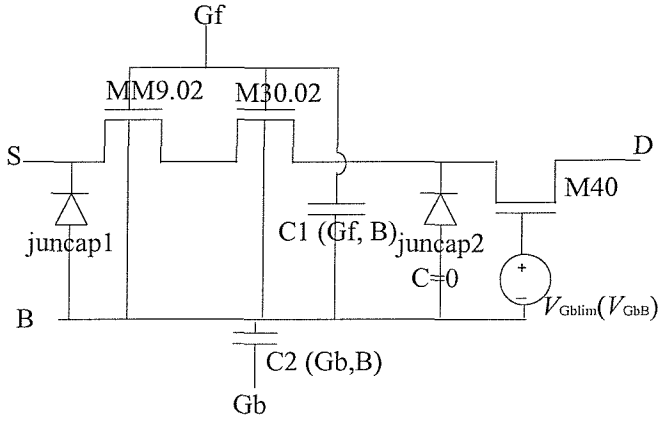

Figure 3.11: The Pstar model for the MV LDMOS

The main difference compared with the LV LDMOS is the longer and thinner drift region which can lead to significant "high side" effects. To model the increase in on-resistance with increasingly negative substrate voltage, a special SOI type depletion mode MOSFET that can describe this effect is added. The complete model, shown in Fig. 3.11, is thus a composite of a MM9.02 (the normal MOST model) in series with a M30.02 (depletion mode MOSFET) in series with a M40 (a special depletion mode MOSFET for SOI). The new model (M40) is used to describe the drift region under the LOCOS oxide. Two

JUNCAP models are used to describe the source to body and the drain to body junctions, along with a couple of voltage dependent capacitances.

For the description of MM9.02 and M30.02, which models the part of the drift region under the thin gate oxide, refer to Sec. 3.2.1 and Sec. 3.2.3 respectively, because the functionality of these models is exactly the same for the LV and MV LDMOS. The self-heating effect is implemented in the same way as for the LV LDMOS (see Sec. 3.2.5) and is not treated again in this section. We find the same extra capacitances in this model, with the exception of the drain-back gate capacitance; this is now included in the SOI depletion type MOSFET (M40).

3.3.1 The SOI Depletion Type MOSFET (M40)

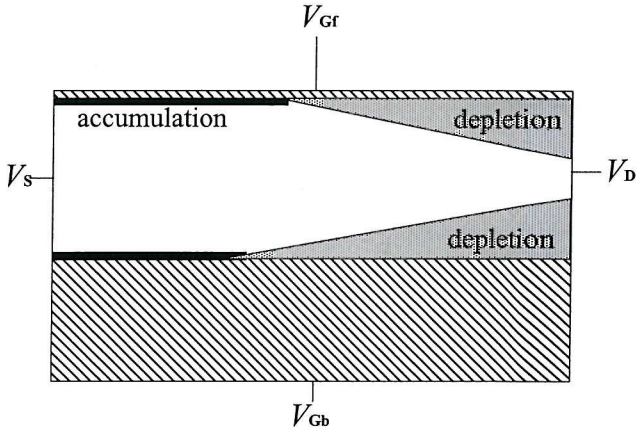

Figure 3.12: Representation of the SOI depletion type MOSFET

The normal representation of the SOI depletion type MOSFET is illustrated in Fig. 3.12. The channel is terminated by a MOS capacitor both at the top and at the bottom. By applying a bias to the front gate and/or the back gate contact, the amount of free charge in the channel, and hence the drift region resistance, is modulated.

This model includes accumulation at the surface and at the buried oxide, depletion from the surface and from the buried oxide, pinch-off mode, velocity saturation, a gate charge model and a box charge model. Two major drawbacks are that the model does not include inversion for negative front gate or back gate biases, and also does not account for the impact ionisation current.

The most important parameters are the on-resistance, $R_{ON,SOI}$ and the pinch-off voltage V_P. $R_{ON,SOI}$ can be calculated from

$$R_{ON,SOI} = \frac{L_{dr}}{W\ \mu_{dr}\ q\ t_{bdr}\ N_D} = R_{shdr}\frac{L_{dr}}{W} \tag{3.15}$$

with L_{dr} the length of the drift region under the field oxide, t_{bdr} the thickness of the silicon film under the field oxide, and R_{shdr} the sheet resistance of the drift region. For the calculation of V_P we only consider the depletion from the buried oxide since the gate field

plate is only extending partly over the LOCOS oxide and this part is included in M30.02. V_{P} is given by [10]

$$V_{\mathrm{P,SOI}} = q\, t_{\mathrm{bdr}}\, N_{\mathrm{D}}\, \frac{C_{\mathrm{ob}}/2 + C_{\mathrm{bdr}}}{C_{\mathrm{ob}}\, C_{\mathrm{bdr}}} \tag{3.16}$$

where

$$C_{\mathrm{ob}} = \frac{\epsilon_{\mathrm{ox}}}{t_{\mathrm{ob}}} \tag{3.17}$$

$$C_{\mathrm{bdr}} = \frac{\epsilon_{\mathrm{si}}}{t_{\mathrm{bdr}}} \tag{3.18}$$

with t_{ob} the thickness of the buried oxide.

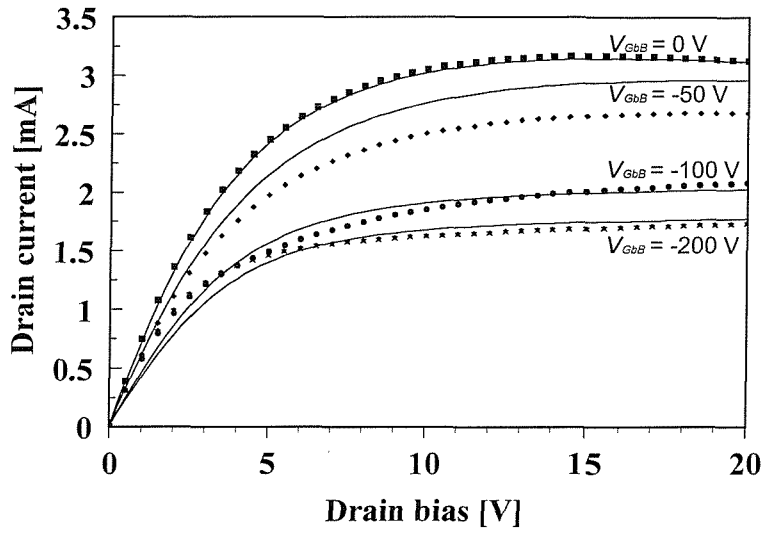

Figure 3.13: Simulated (full line) and measured output characteristic for $V_{\mathrm{GfS}} = 10$ V and $V_{\mathrm{GbS}} = 0$ V, -50, -100, -200 V; $W = 20\mu$m.

For a zero back gate voltage the SOI depletion type MOSFET presents nothing more than an ohmic resistance. Making the back gate bias negative expands the depletion layer at the buried oxide, which increases the resistance of the drift region. Once inversion is established over the whole length of the drift region, the resistance stays constant. This cannot be predicted by the SOI depletion mode MOSFET, because the model does not include inversion. To solve this problem the back gate voltage is limited to a fixed value V_{Gbmax}; here we are using a fitted value of $V_{\mathrm{Gbmax}} = -110$ V. The expression

$$V_{\mathrm{Gblim}} = -\mathrm{min}_{\mathrm{sm}}(-V_{\mathrm{GbB}}, -V_{\mathrm{Gbmax}}) \tag{3.19}$$

is used to describe this limitation of the back gate bias in a smooth way. The function $\mathrm{min}_{\mathrm{sm}}(x, y, \phi_{\mathrm{t}})$ takes the smooth minimum of x and y via a "ln" function and can be found in App. C.6. We optimised V_{P} and V_{Gbmax} (-110 V) using measured high side characteristics, with results shown in Fig. 3.13. The saturation current is predicted quite well, with a maximum error of 20 % for the case of $V_{\mathrm{GbB}} = -50$ V. The overestimated current for $V_{\mathrm{GbB}} = -50$ V indicates that the optimised V_{P} is slightly too low. However

a higher value for V_{P} would underestimate the current for higher V_{GbB} because a partly inverted surface at the buried oxide is not modelled by our simple model; for $-V_{\mathrm{GbB}}$ below $-V_{\mathrm{Gbmax}}$, but above the threshold voltage at the source end of the drift region ($-V_{\mathrm{th0}}^{\mathrm{bdr}} = 45$ V), the current reduction predicted by the model would be too strong, if the correct physical value for V_{P} were to be used.

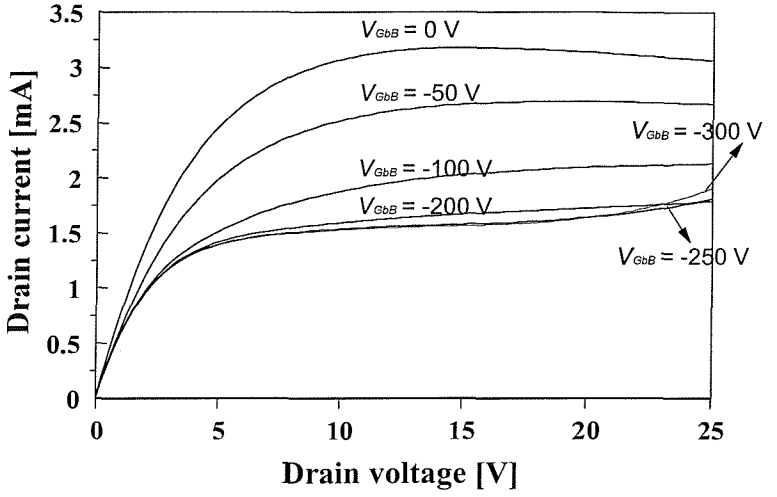

Figure 3.14: Measured output characteristic for $V_{\mathrm{GfS}} = 10$ V and $V_{\mathrm{GbS}} = 0$ V, -50, -100, -200, -250 V; $W = 20\mu$m.

The current in the triode region is less accurately modelled. This can be justified as follows: for lower drain biases the threshold voltage for inversion at the back gate is lower than -110 V. Also, this threshold voltage is not constant over the length of the channel, being lower at the source end of the drift region. The compact model developed in the next chapter includes the possibility of having a fully or partly inverted surface at the buried oxide and describes the current in triode region more accurately.

Fig. 3.14 shows that breakdown happens around $V_{\mathrm{DS}} = 25$ V for a gate voltage of 10 V and $V_{\mathrm{GbS}} < -200$ V. As the gate voltage increases the breakdown voltage decreases, because the impact ionisation current is higher; for the maximum gate voltage (14 V) and maximum back gate voltage (-750 V) the maximum drain voltage that the transistor can stand is 20 V. The SOI depletion type MOSFET model (M40) does not include impact ionisation or other breakdown mechanisms, and so breakdown cannot be simulated.

3.3.2 Model Implementation

Just as for the LV LDMOS the model implemented is in two main blocks, and we refer to Sec. 3.2.6 for the description of the first block and for the explanations behind the chosen implementation.

The subcircuit model definition is formulated using PSTAR code (see Table 3.3). Every line contains a comment (written as "c: comment"), explaining the code. This code describes the schematic of Fig. 3.11 and calculates the temperature increase due to static

self-heating.

```
model: MVLDMOS(D,Gf,S,B,Gb) -parameters-;
 MNE1(D1,Gf,S,B,Gb) -parameters-; c: MM9.02;
 MN1(D2,Gf,D1,B,Gb) -parameters-; c: M30.02;
 MN2(DX,Gb,D2,B,Gb) 40,-parameters-; c: M40;
 JUNCAP1(S,B) -parameters-; c: source-body diode;
 JUNCAP2(D1,B) -parameters-; c: drain-body diode;
 C1(Gf,B) Q = Q1; c: extra capacitance;
 C2(Gb,B) Q = Q2; c: extra capacitance;
 S1(D,DX); c: current source to measure the drain-source current.
      c: This is a trick to obtain the current, which is needed to
      c: calculate the self-heating;
 DTA=RT*i(S1)*v(D,S); c: ΔT due to static self-heating;
 temp scaling equations;
end;
```

Table 3.3: *The MV LDMOS subcircuit model definition as formulated for PSTAR.*

3.3.3 Extraction Strategy with ICCAP and Model Validation

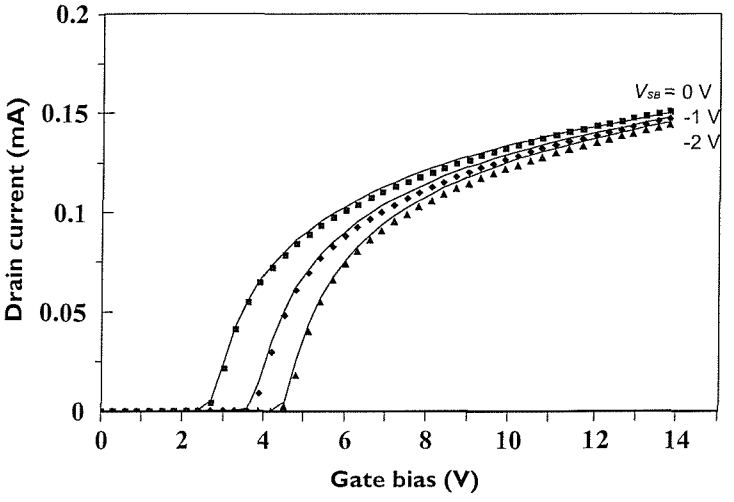

Figure 3.15: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ for V_{BS} = 0, -1, -2 V and $V_{DS} = 0.25$ V; $W = 10\mu$m.

The measurement set-up is identical to the set-up used for the LV LDMOS. We have to extract two main extra parameters: $V_{SAT,SOI}$, the critical drain-source voltage for velocity saturation in the second part of the drift region, and $R_{ON,SOI}$, the on-resistance of the

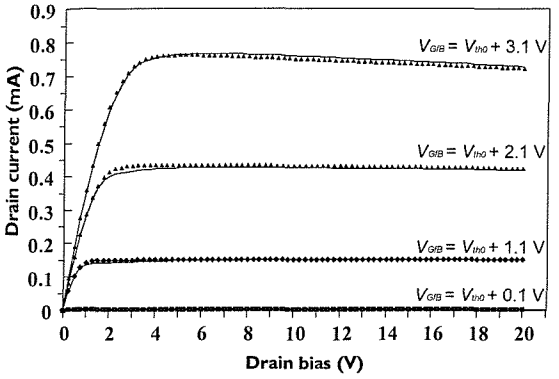

Figure 3.16: Measured (markers) and simulated (full line) $I_D(V_{DS})$ for $V_{BS} = 0$ V and V_{GfS}=$V_{th0} + 0.1$, $V_{th0} + 1.1$, $V_{th0} + 2.1$, $V_{th0} + 3.1$ V; $W = 10\mu$m.

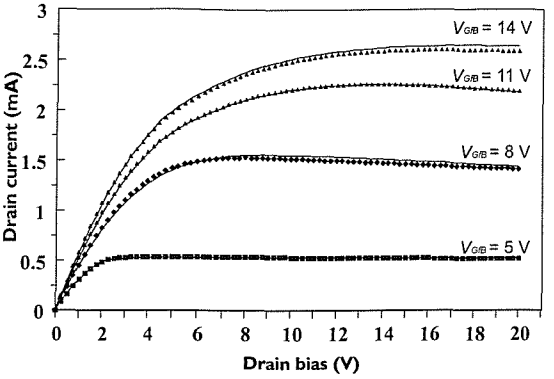

Figure 3.17: Measured (markers) and simulated (full line) $I_D(V_{DS})$ for $V_{BS} = 0$ V and V_{GfS}=5, 8, 11, 14 V; $W = 10\mu$m.

SOI depletion type MOSFET. It is good practice to calculate these from the available process parameters (using the formulas from Sec. 3.3.1), and to keep them constant while optimizing all the other parameters. Once the other parameters are known, the results can be refined by optimizing the values of $V_{SAT,SOI}$ and $R_{ON,SOI}$. As explained in Sec. 3.3.1 the parameter $V_{P,SOI}$ can be optimised using the high-side measurements. The optimised parameter set for the MV LDMOS can be found in App. B

Fig. 3.15 shows the linear characteristic for different body voltages. We again notice the very strong flattening of the curves for higher gate bias due to the long drift region presenting a high series resistance. A good fit is obtained between the simulated and measured values.

Fig. 3.16 and 3.17 show the output characteristics for respectively lower and higher gate biases and a zero body voltage. For the lower gate biases the MM9.02 part plays the main role and for the higher gate biases the drift region modelled by M30.02 and M40 is crucial. We can see that both are well modelled and that the fits are very accurate in both plots.

Fig. 3.18 shows the output characteristic for a body voltage of -2V. Just as for the LV LDMOS, the fits are less accurate than for the previous plots. The negative body voltage increases the depletion in the drift region at the P-N^- junction and the consequent current reduction can not be described very accurately by M30.02 (see Sec. 3.2.3).

Finally we show the sub-threshold plots in Fig. 3.19, which again gives an excellent fit between measured and simulated data. For the subthreshold case, the influence of M30.02 is less important compared with the LV LDMOS, so the fits for non-zero body voltages are also accurate.

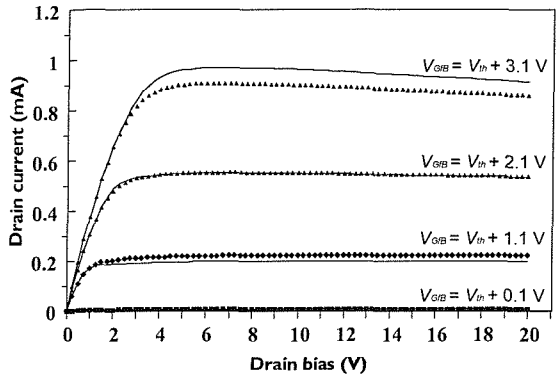

Figure 3.18: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ for $V_{BS} = -2$ V and $V_{GfS} = V_{th} + 0.1$ V, $V_{th} + 1.1$ V, $V_{th} + 2.1$ V, $V_{th} + 3.1$ V; $W = 10\mu$m.

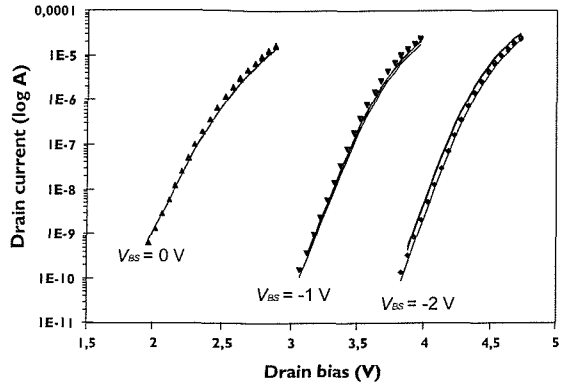

Figure 3.19: Measured (markers) and simulated (full line) $I_D(V_{GfS})$ (around the threshold voltage) for $V_{BS} = 0$, -1, -2 V and $V_{DS} = 1$, 7.5, 14 V; $W = 10\mu$m.

3.4 Limitations of the Models and Conclusion

The first drawback of this modelling approach is the complexity of the circuit and hence the large number of model parameters. These parameters require a considerable effort in extraction while their contribution to the accuracy of the results is not entirely certain. A consequence of this is the increased computation time during simulations which can be very inconvenient for the simulation of large scale circuits.

Secondly we have been restricted in the charge modelling. The different transistor models all contribute to the overall charge behaviour, but the inversion charges along the buried oxide are not included, so we had to add voltage dependent capacitances, which can only describe reciprocal capacitances, which is limiting for the LDMOS. Furthermore, as explained in Sec. 2.2.3 the gradually decreasing doping of the P-region under the gate has a big influence on the capacitance behaviour, and this can not be modelled by MM9.02.

Finally the use of a MOSFET and a depletion mode MOSFET in series, instead of using one compact model, increases the risk of non-convergence during a circuit simulation. The model has been tested on a Schmitt Trigger circuit in PHILIPS, and it has been found that some node settings and simplifications were necessary to make the circuit converge [14].

To conclude, we can say that the subcircuit modelling approach gave a "quick-fix" LDMOS model, which could be used in the PSTAR simulator. The model gives good agreement with DC measurements, and reasonable matching for transient and AC results [15], but has the drawback of complexity and increased computation time. In the next chapter the development of a compact model will overcome these disadvantages.

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Chapter 4

Compact DC Model

4.1 Introduction

In this chapter the compact SOI LDMOS model is developed to facilitate circuit design for smart power applications, where the SOI LDMOS is the most common element of the circuit. The model combines an electrical model with a thermal network to model self- and coupled heating effects in a consistent manner.

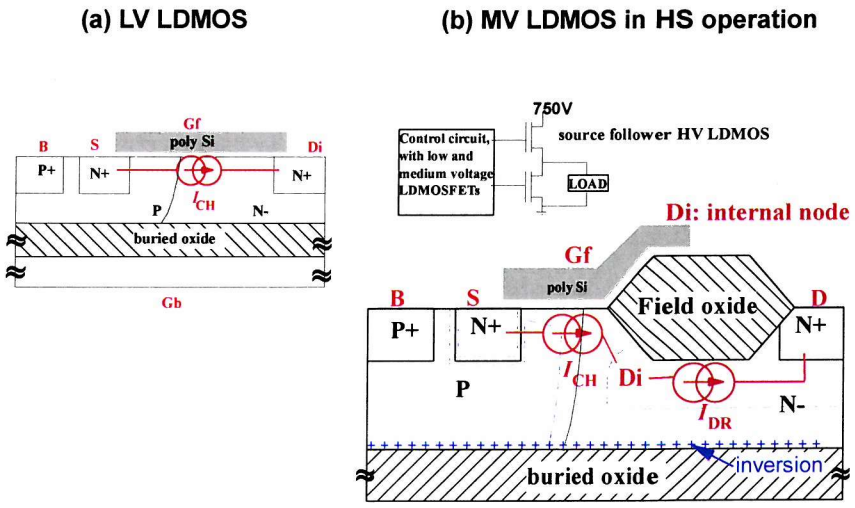

Figure 4.1: Illustration of the use of the DC current expressions: (a) LV LDMOS; (b) MV LDMOS working under high side conditions.

To describe accurately the behaviour of the MV SOI LDMOS we use two current equations, both of which are smooth and continuous in all regions of operation. The first current expression (I_{CH}, see Sec. 4.2) describes the LV LDMOS part, including the drift region under the thin gate oxide. The second expression (I_{DR}, see Sec. 4.3) models the drift region under the field oxide and includes high-side behaviour. Fig. 4.1 illustrates where I_{CH} and I_{DR} are applied in the LV and MV SOI LDMOS structures. These two current

expressions have been matched consistently with the help of limiting procedures and an accurate prediction of the internal node voltage. For this reason, a compact model can converge much more quickly than a subcircuit model, since, in the latter case, the circuit simulator must try to make the state of an isolated internal node converge. With the compact model, the simulations of linear and switching applications can converge without initial node sets. Another advantage is that fewer parameters are required, and these are more physical than for a compound subcircuit model.

The model for the current under the thin gate oxide (Sec. 4.2) is surface potential based, and models both the drift and diffusion currents in all operating regions. Care has been taken to use only continuous and infinitely differentiable expressions. Furthermore, the model ensures a smooth transition between subthreshold and strong inversion and between triode and saturation. Both the lateral doping gradient in the channel and the overlap of the thin gate oxide over the drift region are accounted for in a compact and physical manner.

The model for the current under the field gate oxide (Sec. 4.3) uses both the potential distribution in the drift region and the surface potential at the surface of the buried oxide, ensuring a purely physical prediction of the unique high-side behaviour observed in the SOI LDMOS.

In Sec. 4.4 the implementation of the internal thermal netlist is discussed. The self- and coupled heating effects are much more apparent in SOI HV devices and need particular care if an accurate model is required.

Finally measurements and simulations are compared for SOI LDMOST with different geometries and good agreement proves the model's precision.

4.2 Current under Thin Gate Oxide

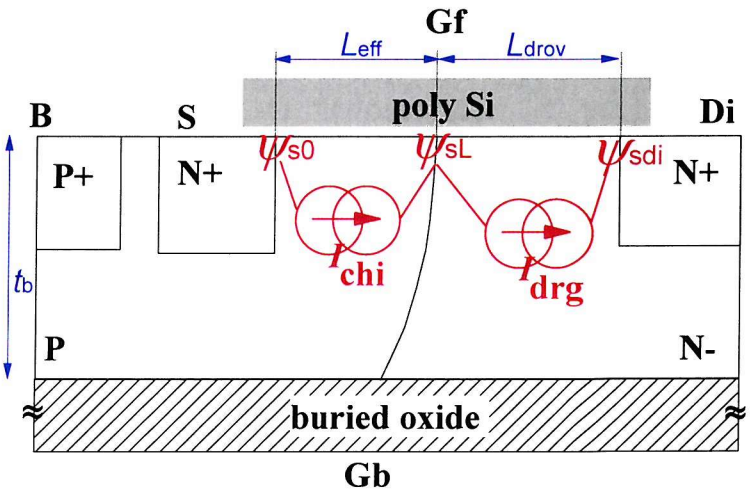

Figure 4.2: Illustration of the symbols used for the calculation of I_{CH}.

To explain our model strategy, let us consider the following three operating regions :

- Under *strong inversion* conditions the potential at the P-N^- junction cannot be calculated immediately from V_{SB}, V_{DiB} and V_{GfB}. However, the inversion channel current (I_{chi}) and the drift current under the front gate (I_{drg}) can be expressed as functions of the surface potentials ψ_{s0}, ψ_{sL} (= ψ_{siL}, where the subscript "si" is used to refer to the strong inversion case) and ψ_{sdi}. The different symbols used in this section are defined in Fig. 4.2; note that all potentials used in this section are referred to the P-body (B). Expressions for I_{chi} and I_{drg} are developed in Secs. 4.2.1 and 4.2.2 respectively.

  The surface potentials at the source (ψ_{s0}) and at the internal drain (ψ_{sdi}) can be calculated immediately from the node voltages. An analytical solution for the surface potential at the P-N^- junction ψ_{sL} can be obtained by equating the two current expressions I_{drg} and I_{chi} (Sec. 4.2.3).

- Under *subthreshold conditions* the current is dominated by the diffusion current in the MOSFET part of the LDMOS, and the surface potential at the left side of the P-N^- junction (ψ_{sL}) is given by the subthreshold surface potential in the channel ($\psi_{sL} = \psi_{ss0}$), which is only a function of V_{GfB} and not of the other nodal voltages.

- Finally, in the *saturation* regime, when the high field effects are included in the channel current (see Sec. 4.2.4), the current saturation potential ψ_{sLsat} can be found from $\frac{dI_{CH}}{d\psi_{sL}}|_{\psi_{sL}=\psi_{sLsat}} = 0$.

These three cases can be joined together smoothly to provide the final expressions for the surface potentials:

$$\psi_{s0} = \phi_t \ln\left(1 + \frac{\exp\left(\frac{\psi_{si0}}{\phi_t}\right)}{1 + \exp\left(\frac{\psi_{si0} - \psi_{sLsatf}}{\phi_t}\right)}\right) \tag{4.1}$$

$$\psi_{sL} = \phi_t \ln\left(1 + \frac{\exp\left(\frac{\psi_{siL}}{\phi_t}\right)}{1 + \exp\left(\frac{\psi_{siL} - \psi_{sLsatf}}{\phi_t}\right)}\right) \tag{4.2}$$

$$\psi_{sdi} = V_{DiB} + \phi_{bid} \tag{4.3}$$

where the expression for ψ_{sLsatf} is developed in Sec. 4.2.4. It is shown that $\psi_{sLsatf} = \psi_{ss0}$ in the subthreshold region and $\psi_{sLsatf} = \psi_{sLsat}$ in the saturation regime. The natural logarithmic function provides a smooth minimum between ψ_{sLsatf} and ψ_{siL} and describes well the transition from subthreshold into inversion. The surface potentials ψ_{si0} and ψ_{ss0} in the inversion and the subthreshold regions respectively are expressed in terms of the nodal voltages in App. C. For more details about the physical background refer to [1].

These expressions for ψ_{sL} and ψ_{s0} are then used in I_{chi}, and hence provide an analytical expression for the current under the front gate (I_{CH}), which is only a function of ψ_{s0} and

ψ_{sdi}.

4.2.1 The Inversion Channel Current

Using standard assumptions for MOSFETs [1], the inversion channel current can be expressed using the classic charge sheet model [2],

$$I_{\mathrm{chi}}(y) = -W\mu_{\mathrm{s}}(y)\; q_{\mathrm{cinv}}(y)\; \frac{d\psi_{\mathrm{s}}}{dy} + W\mu_{\mathrm{s}}(y)\; \phi_{\mathrm{t}} \frac{dq_{\mathrm{cinv}}}{dy}. \tag{4.4}$$

In Eq. 4.4, $q_{\mathrm{cinv}}(y)$ is the channel charge density, ψ_{s} the surface potential at position y, $\phi_{\mathrm{t}} = \frac{kT}{q}$ the thermal voltage, and $\mu_{\mathrm{s}}(y)$ is the surface mobility. Using the electron continuity equation [3] and neglecting recombination and generation currents means $\frac{dI_{\mathrm{chi}}}{dy} = 0$ for all y, yielding

$$I_{\mathrm{chi}} = \frac{W}{L_{\mathrm{eff}}}\Big(-\int_{\psi_{\mathrm{s0}}}^{\psi_{\mathrm{sL}}} \mu_{\mathrm{s}}(y)\; q_{\mathrm{cinv}}(y) \cdot d\psi_{\mathrm{s}} + \phi_{\mathrm{t}} \int_{q_0}^{q_{\mathrm{L}}} \mu_{\mathrm{s}}(y) \cdot dq_{\mathrm{cinv}}\Big). \tag{4.5}$$

Here L_{eff} is the effective length of the channel defined by the length of the under-diffusion of the P-well minus the under-diffusion of the N^+ source well ($L_{\mathrm{eff}} = L - L_{\mathrm{D}}$). The charge densities are denoted by q_0 and q_{L} at $y = 0$ and $y = L_{\mathrm{eff}}$ respectively.

The mobility is assumed to be constant along the channel, although this is not strictly true. The effects of the electrical field on the mobility in the channel will be discussed in Sec. 4.2.4 and will be modelled by an effective mobility in the final expression for the channel current I_{CH}.

Using the depletion approximation, which assumes that the depletion region under the gate is free of mobile carriers [4], the inversion channel charge can be obtained as

$$q_{\mathrm{cinv}}(\psi_{\mathrm{s}}, y) = -C_{\mathrm{of}} \cdot \Big(V_{\mathrm{g}} - \eta_{\mathrm{s}}\; \psi_{\mathrm{s}} - \gamma(y)\; \sqrt{\psi_{\mathrm{s}}}\Big) \tag{4.6}$$

with $V_{\mathrm{g}} = V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}}$, the body factor $\gamma(y) = \frac{\sqrt{2q\,\epsilon_{\mathrm{si}}\,N_{\mathrm{A}}(y)}}{C_{\mathrm{of}}}$, and a factor η_{s} which accounts for the influence of the fast surface states at the silicon-oxide interface. This factor is given by

$$\eta_{\mathrm{s}} = 1 + \frac{D_{\mathrm{itf}}}{C_{\mathrm{of}}} \tag{4.7}$$

with D_{itf} denoting the fast surface state density.

In order to get an analytic closed form expression for the saturation voltage when including high field effects (see Sec. 4.2.4), the body charge is linearised using a Taylor expansion for the square root term [5]:

$$q_{\mathrm{b}} = C_{\mathrm{of}}\; \gamma\; \sqrt{\psi_{\mathrm{s}}} \tag{4.8}$$

$$\cong C_{\mathrm{of}}\; \gamma \cdot \Big(\sqrt{\psi_{\mathrm{st0}}} + \delta \cdot (\psi_{\mathrm{s}} - \psi_{\mathrm{st0}})\Big) \tag{4.9}$$

with $\delta = \frac{1}{2\sqrt{1+\psi_{st0}}}$ and

$$\psi_{st0} = \phi_t \ln\left(1 + \frac{\exp\left(\frac{\psi_{si0}}{\phi_t}\right)}{1 + \exp\left(\frac{\psi_{si0}-\psi_{ss0}}{\phi_t}\right)}\right). \tag{4.10}$$

Note that we are using ψ_{st0} and not ψ_{s0}, as defined at the beginning of the section, because at this point in the development the saturation surface potential is still unknown.

The lateral doping gradient in the channel (k_{N_A}) is brought in by means of $\gamma(y)$, which is a function of $N_A(y)$ and thus of the position y along the channel. In order to perform the integration of Eq. 4.5, q_{cinv} is needed in terms of ψ_s only, or in other words, we have to transform $\gamma(y)$ to $\gamma(\psi_s)$. This can only be done under certain assumptions, which are set out below.

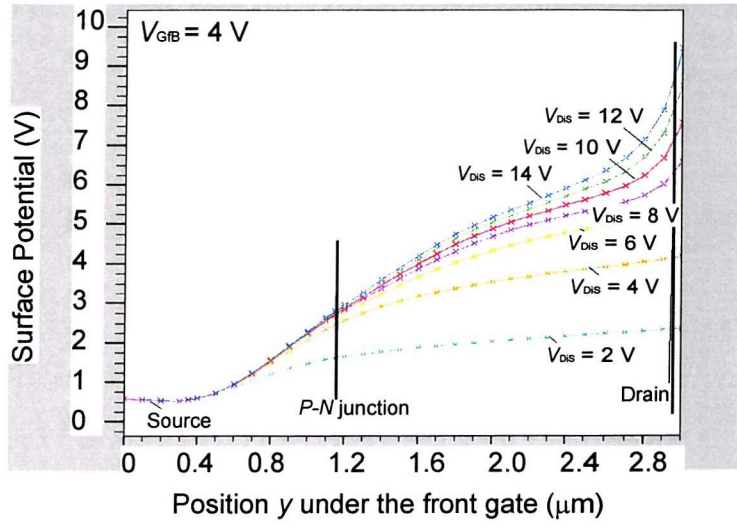

Figure 4.3: ATLAS simulation of the depletion layers and the surface potential under the front gate ($V_{GfB} = 4$ V).

The doping profile is assumed to be exponential ($N_A = N_{As} \exp\left(-k_{N_A}\frac{y}{L_{eff}}\right)$) [6,7] and hence

$$\gamma(y) = \gamma_0 \, exp\left(-\frac{k_{N_A} y}{2\, L_{eff}}\right) \cong \gamma_0 \cdot \left(1 - \frac{k_{N_A} y}{2\, L_{eff}}\right) \tag{4.11}$$

with $\gamma_0 = \frac{\sqrt{2q\,\epsilon_{si}\,N_{As}}}{C_{of}}$. The approximation is valid (see Sec. 2.2.3) for typical values of the doping gradient k_{N_A} ($\cong 1$). To transform $\gamma(y)$ into $\gamma(\psi_s)$, ψ_s is assumed to be a linear function of y, i.e.

$$\psi_s = \psi_{st0} + \frac{y}{L_{eff}}\left(\psi_{sL} - \psi_{st0}\right). \tag{4.12}$$

This yields

$$\gamma(\psi_s) = \gamma_0 \cdot \left(1 - \frac{k_{N_A}}{2\left(\psi_{sL} - \psi_{st0}\right)}\left(\psi_s - \psi_{st0}\right)\right). \tag{4.13}$$

In a standard MOSFET with a constant doping in the channel, the linearity of ψ_s with y is accurate for low drain biases, but deteriorates towards higher drain biases. However,

a decreasing doping concentration in the channel causes a *reduced field effect*, giving a reasonable linearity for higher drain biases. Furthermore, the MOS part of the LDMOS never reaches very deep saturation because the main part of the applied voltage drops over the drift region. These two arguments are illustrated in Fig. 4.3, where we have simulated the surface potential as a function of position y along the channel. The SOI LV LDMOS structure used for this ATLAS simulation is the same as the one described in Chapter 2. One observes the reasonably good linearity of the surface potential between the source and the P-N junction, even when V_{DiS} is very high.

Using Eqs. 4.13 and 4.9, the inversion channel density becomes

$$\begin{aligned} q_{\mathrm{cinv}}(\psi_{\mathrm{s}}) &= -C_{\mathrm{of}} \cdot \left\{ V_{\mathrm{g}} - \eta_{\mathrm{s}}\, \psi_{\mathrm{s}} - \gamma_0 \left(1 - \frac{k_{\mathrm{N_A}}\, (\psi_{\mathrm{s}} - \psi_{\mathrm{st0}})}{2\, (\psi_{\mathrm{sL}} - \psi_{\mathrm{st0}})} \right) \cdot \right. \\ &\qquad \left. \left(\sqrt{\psi_{\mathrm{st0}}} + \delta \cdot (\psi_{\mathrm{s}} - \psi_{\mathrm{st0}}) \right) \right\} . \end{aligned} \tag{4.14}$$

Substituting Eq. 4.14 into Eq. 4.5 results in a closed form continuous equation, which can be used for the inversion channel current in all regions of operation:

$$I_{\mathrm{chi}} = \beta \cdot \left(g \cdot (\psi_{\mathrm{sL}}^2 - \psi_{\mathrm{s0}}^2) + f \cdot (\psi_{\mathrm{sL}} - \psi_{\mathrm{s0}}) \right) \tag{4.15}$$

with

$$\beta = \frac{W}{L_{\mathrm{eff}}}\, \mu_{\mathrm{s}}\, C_{\mathrm{of}} \tag{4.16}$$

$$g = -\frac{1}{2}\, \eta_{\mathrm{s}} + \gamma_0\, \delta \cdot \left(\frac{1}{6}\, k_{\mathrm{N_A}} - \frac{1}{2} \right) \tag{4.17}$$

$$f = f_1 + f_2 \tag{4.18}$$

$$f_1 = V_{\mathrm{g}} - \gamma_0\, \sqrt{\psi_{\mathrm{st0}}} \left(1 - \frac{k_{\mathrm{N_A}}}{4} \right) + \left(1 - \frac{k_{\mathrm{N_A}}}{3} \right) \gamma_0\, \delta\, \psi_{\mathrm{st0}} \tag{4.19}$$

$$f_2 = \phi_{\mathrm{t}} \cdot \left(\eta_{\mathrm{s}} + \gamma_0\, \delta - \frac{1}{2}\, \gamma_0\, k_{\mathrm{N_A}}\, \delta \right) \tag{4.20}$$

Note that β can be recognized as the inversion layer gain factor.

Previous LDMOS models accounting for the lateral doping gradient have the drawback of using a fixed effective value for the body factor in the expression for the inversion charge [7], or having to partition the channel into regions of constant doping [8].

Figs. 4.4 and 4.5 show the influence of the doping gradient ($k_{\mathrm{N_A}}$) on the channel current; the output characteristics illustrate nicely the increase in saturation current with increasing doping gradient. In the linear characteristics we observe that the transition from subthreshold into inversion occurs around the same voltage, which is the threshold voltage at the source end of the channel defined as V_{th0}. However, this transition is faster for a higher doping gradient. This is to be expected, since the higher the doping gradient, the more inversion charge will be present at the drain end of the channel, and hence the quicker the current rises when the source threshold voltage is reached.

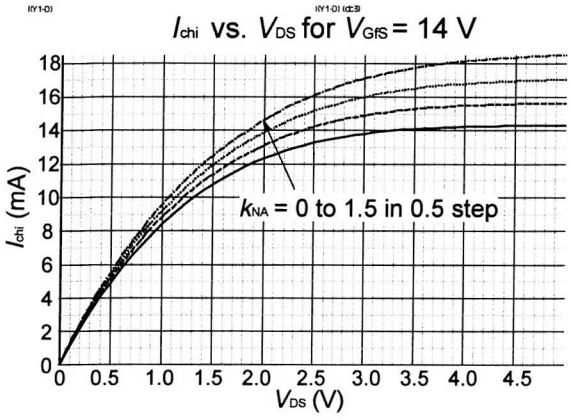

Figure 4.4: Influence of k_{N_A} on I_{chi} vs. V_{DS}; V_{GfS} = 14 V and $L_{drov} = L_{dr} = 0$.

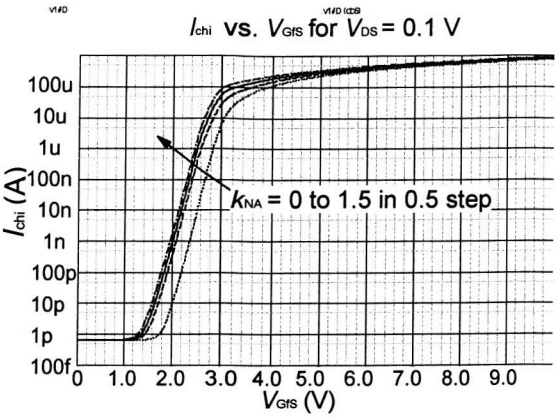

Figure 4.5: Influence of k_{N_A} on I_{chi} vs. V_{GfS}; V_{DS} = 0.1 V and $L_{drov} = L_{dr} = 0$.

4.2.2 The Accumulation/Drift Current under Thin Gate Oxide

In the linear region of operation of the LDMOS an accumulation layer is created in the drift region along the surface of the front oxide, and this makes an important contribution to the device behaviour. In the compact bulk and SOI models published [6, 9, 10] the influence of the gate overlap over the drift region is neglected, or, if taken into account, an extra current source (and hence an extra internal node) is introduced [8], slowing down convergence. Here the overlap of the thin gate oxide over the drift region will be accounted for in an analytical way without introducing an extra node.

Because the overlap length of the front gate over the drift region (L_{drov}) is typically of the same order as the length of the inversion channel, we have made the assumption that the channel current saturates before the accumulation layer starts to disappear at the drain. This assumption is confirmed by ATLAS simulations. Fig. 4.3 shows an ATLAS simulation of the surface potential along the gate oxide for different drain biases. We can see that the surface potential at the P-N^- junction hardly changes when V_{DiS} exceeds $V_{GfS} - V_{FB}^{fdr}$ (where V_{FB}^{fdr} is the flat band voltage in the drift region with respect to the front gate), instead remaining fixed at ψ_{sLsat}, the saturation surface potential. Also, when looking at the measured output characteristics of an LV LDMOS (see Fig. 4.12), it can be observed that the current saturates before V_{DiS} reaches $V_{GfS} - V_{FB}^{fdr}$.

Neglecting the diffusion current and assuming that the surface is completely accumulated, the current in the drift region under the front gate can be expressed by [11]

$$I_{drg} = -\frac{W}{L_{drov}} \int_{\psi_{sL}}^{\psi_{sdi}} \left(\mu_{dr}\, q_b^{dr} + \mu_{acc}\, q_{cacc} \right) \cdot d\psi_s \,. \tag{4.21}$$

The free bulk charge density in the N^- region, q_b^{dr}, and the accumulation charge density,

q_{acc} are

$$q_{\mathrm{b}}^{\mathrm{dr}} = q\, N_{\mathrm{D}}\, t_{\mathrm{b}}\, f_{\mathrm{v}}\,, \tag{4.22}$$

$$q_{\mathrm{cacc}} = C_{\mathrm{of}} \cdot \left(\left(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}}\right) - \psi_{\mathrm{s}}\right)\,, \tag{4.23}$$

where μ_{dr} is the low field mobility factor in the drift region, and f_{v} is a fitting parameter taking into account the fact that the current flow is partially vertical. This is due to the length of the current flow lines being longer than L_{drov}, especially when L_{drov} is of the same order as the silicon film thickness t_{b}. When L_{drov} is considerably larger than t_{b} this factor should approach one.

The surface potentials ψ_{sL}, ψ_{sdi} and ψ_{s} all use the body potential as a reference. So in theory ψ_{sdi} is given by $V_{\mathrm{DiB}} + \phi_{\mathrm{bid}}$. However, when $V_{\mathrm{DiS}} = 0$, the current also has to be zero. For $V_{\mathrm{DiS}} = 0$, when the channel is in strong inversion, $\psi_{\mathrm{sL}} = \psi_{\mathrm{siL}} = \psi_{\mathrm{si0}} \cong 2\phi_{\mathrm{F}} + V_{\mathrm{SB}}$, and ψ_{sdi} has to be equal to ψ_{s0} as well to ensure zero current. Therefore $V_{\mathrm{DiS}} + \psi_{\mathrm{si0}}$ is used instead of $V_{\mathrm{DiB}} + \phi_{\mathrm{bid}}$ as the expression for ψ_{sdi}. The difference between $\phi_{\mathrm{bid}} = \phi_{\mathrm{F}} + \phi_{\mathrm{Fdr}}$ and $2\phi_{\mathrm{F}}$ is usually negligible (<0.1 V), because, considered on a logarithmical scale, the doping concentrations of the P-body and the N^- drift region hardly differ.

After integration of Eq. 4.21 we obtain

$$I_{\mathrm{drg}} = h_1 \cdot (V_{\mathrm{DiS}} + \psi_{\mathrm{si0}} - \psi_{\mathrm{sL}}) + h_2 \cdot \left((V_{\mathrm{DiS}} + \psi_{\mathrm{si0}})^2 - \psi_{\mathrm{sL}}^2\right) \tag{4.24}$$

with

$$h_1 = \frac{f_{\mathrm{v}}}{R_{\mathrm{ON}}} + \beta_{\mathrm{acc}} \cdot \left(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{f}} + (\psi_{\mathrm{si0}} - V_{\mathrm{SB}})\right) \tag{4.25}$$

$$h_2 = -\frac{1}{2}\,\beta_{\mathrm{acc}} \tag{4.26}$$

$$\beta_{\mathrm{acc}} = \frac{W}{L_{\mathrm{drov}}}\,\mu_{\mathrm{acc}}\, C_{\mathrm{of}} \tag{4.27}$$

$$R_{\mathrm{ON}} = \left(\frac{W}{L_{\mathrm{drov}}}\,\mu_{\mathrm{dr}}\, q\, N_{\mathrm{D}}\, t_{\mathrm{b}}\right)^{-1}\,. \tag{4.28}$$

This expression completely describes the drift current under the thin gate oxide with a second order equation in the surface potentials ψ_{sL} and ψ_{sdi}. Note that R_{ON} can be recognized as the ON-resistance of the drift region under the thin gate oxide under zero bias conditions, and β_{acc} is the accumulation layer gain factor.

4.2.3 Solving for Surface Potential at the End of the Inversion Channel

Having obtained expression for the inversion layer channel current (I_{chi}) and the drift current under the thin gate oxide (I_{drg}), an analytical expression for the surface potential at the P-N junction (ψ_{sL}) can be derived. To find ψ_{sL} when the channel is in strong inversion ($\psi_{\mathrm{s0}} = \psi_{\mathrm{si0}}$, $\psi_{\mathrm{sL}} = \psi_{\mathrm{siL}}^*$), Eq. 4.15 is equated to Eq. 4.24. To get a more accurate solution for ψ_{siL}^*, simple expressions for the vertical field effects for the inversion and

accumulation layer mobility are included by substituting β and β_{acc} with respectively

$$\beta_{\mathrm{e}} = \frac{\beta}{1+\theta\cdot(V_{\mathrm{g}}-\psi_{\mathrm{st0}})} \tag{4.29}$$

$$\beta_{\mathrm{acce}} = \frac{\beta_{\mathrm{acc}}}{2\ (1+\theta_{\mathrm{acc}}\cdot(V_{\mathrm{g}}-\psi_{\mathrm{sLsat}}))} \tag{4.30}$$

with θ and θ_{acc} respectively the inversion and accumulation vertical mobility degradation factors. To simplify the derivation we have made the assumption that velocity saturation effects can be accounted for by an identical reduction factor for I_{chi} and I_{drg}. The validity of this assumption is supported by the fact that we are looking for a result for ψ^*_{siL} before saturation occurs, because after that point, ψ_{sL} is given by ψ_{sLsat}, as developed in the next section. Putting $I_{\mathrm{drg}} = I_{\mathrm{chi}}$ now results in

$$\left(\frac{f_{\mathrm{v}}}{R_{\mathrm{ON}}}+\beta_{\mathrm{acce}}\cdot\left(V_{\mathrm{GfB}}-V^{\mathrm{f}}_{\mathrm{FB}}+\phi_{\mathrm{bid}}\right)\right)\cdot(\psi_{\mathrm{sdi}}-\psi^*_{\mathrm{siL}})-\frac{\beta_{\mathrm{acce}}}{2}\left(\psi^2_{\mathrm{sdi}}-(\psi_{\mathrm{siL}})^2\right) = \beta_{\mathrm{e}}\cdot\left(g\cdot((\psi^*_{\mathrm{siL}})^2-\psi^2_{\mathrm{si0}})+f\cdot(\psi^*_{\mathrm{siL}}-\psi_{\mathrm{si0}})\right)\ . \tag{4.31}$$

This yields ψ^*_{siL} as a function of the known surface potentials ψ_{si0} and ψ_{sdi}:

$$\psi^*_{\mathrm{siL}} = \frac{-\frac{B}{2}+\sqrt{\frac{B^2}{4}-A\,C^*}}{A} \tag{4.32}$$

with

$$G = -\frac{\beta_{\mathrm{acce}}}{2\,\beta_{\mathrm{e}}} \tag{4.33}$$

$$F = \frac{f_{\mathrm{v}}}{\beta_{\mathrm{e}}\,R_{\mathrm{ON}}}+\frac{\beta_{\mathrm{acce}}}{\beta_{\mathrm{e}}}\left(V_{\mathrm{GfB}}-V^{\mathrm{f}}_{\mathrm{FB}}+(\psi_{\mathrm{si0}}-V_{\mathrm{SB}})\right) \tag{4.34}$$

$$A = g+G \tag{4.35}$$

$$B = f+F \tag{4.36}$$

$$C^* = -\left(g\,\psi^2_{\mathrm{si0}}+f\,\psi_{\mathrm{si0}}\right)-F\cdot(V_{\mathrm{DiS}}+\psi_{\mathrm{si0}})-G\cdot(V_{\mathrm{DiS}}+\psi_{\mathrm{si0}})^2\ . \tag{4.37}$$

Only the solution given by Eq. 4.32 is correct for ψ^*_{siL}, the second solution of Eq. 4.31 being physically invalid.

4.2.4 Inclusion of High Field Effects

The surface mobility will be reduced due to the presence of a vertical field in the channel and due to velocity saturation. In this section we develop an effective value for the surface mobility including these two high field effects. The approach followed is similar to the standard MOSFET mobility model used in STAG [1], with the difference that root terms in the expression for the vertical electric field will not be neglected.

Vertical Field Mobility Reduction

Due to scattering and two-dimensional confinement effects the mobility in the channel depends on the bias conditions. The mobility decreases with increasing effective transverse electric field ξ_{xeff}, which is defined as the field averaged over the electron distribution. The transverse electric field is given by [12]

$$\xi_{\text{x}} = \frac{1}{\epsilon_{\text{si}}} \left(q_{\text{b}} + \zeta \, q_{\text{cinv}}\right) \tag{4.38}$$

where ζ is an empirical parameter, taking on the value $\frac{1}{2}$ for electrons and $\frac{1}{3}$ for holes. Assuming classical diffuse scattering at the Si-SiO_2 surface, the effective mobility due to the presence of a vertical electrical field can be modelled as

$$\mu_{\text{xeff}} = \frac{\mu_{\text{s}}}{1 + \alpha_\theta \, |\xi_{\text{xeff}}|} \, , \tag{4.39}$$

with the scattering coefficient α_θ. Using the linearised expression for the body and the channel charge densities (Eqs. 4.9 and 4.14), Eq. 4.38 becomes

$$\xi_{\text{x}} = -\frac{\zeta \, C_{\text{of}}}{\epsilon_{\text{si}}} \left\{ V_{\text{g}} - \psi_{\text{s}} - \gamma_{\text{m}} \cdot \left(1 - \frac{1}{\zeta}\right) \left(\sqrt{\psi_{\text{s0}}} + \delta \cdot (\psi_{\text{s}} - \psi_{\text{s0}})\right) \right\} \, , \tag{4.40}$$

where the interface traps have been ignored, and a mean value for the body factor has been defined as

$$\gamma_{\text{m}} = \frac{\gamma_0 + \gamma_{\text{L}}}{2} \, . \tag{4.41}$$

Averaging ξ_{x} over the length of the device results in

$$\begin{aligned} \xi_{\text{xeff}} \;=\; & -\frac{\zeta \, C_{\text{of}}}{\epsilon_{\text{si}}} \cdot \left\{ V_{\text{g}} - \gamma_{\text{m}} \cdot \left(1 - \frac{1}{\zeta}\right) \left(\sqrt{\psi_{\text{s0}}} - \delta \, \psi_{\text{s0}}\right) \right. \\ & \left. - \left(1 + \gamma_{\text{m}} \, \delta \cdot \left(1 - \frac{1}{\zeta}\right)\right) \frac{\psi_{\text{s0}} + \psi_{\text{sL}}}{2} \right\} \, . \end{aligned} \tag{4.42}$$

For an N-type device the effective mobility becomes

$$\mu_{\text{xeff}} = \frac{\mu_{\text{s}}}{1 + \theta \cdot \left(V_{\text{g}} + \gamma_{\text{m}} \cdot (\sqrt{\psi_{\text{s0}}} - \delta \, \psi_{\text{s0}}) - (1 - \gamma_{\text{m}} \, \delta) \, \frac{\psi_{\text{s0}} + \psi_{\text{sL}}}{2}\right)} \tag{4.43}$$

with

$$\theta = -\frac{\alpha_\theta \, \zeta \, C_{\text{of}}}{\epsilon_{\text{si}}} \, . \tag{4.44}$$

Although physical values exist for the parameters in Eq. 4.44, it is usual to treat θ as a fitting parameter; this approach has been chosen in our SOI LDMOS model.

In the original version of the STAG model [1] the linearised root terms were neglected. This resulted in low non-physical low values for the optimised zero-field mobility parameter μ_{s}. Furthermore, in high voltage devices the doping concentration of the P-body is often higher than for standard CMOS. This leads to a higher body factor, which makes the

linearised root terms even more important.

Carrier Velocity Saturation

When the longitudinal field ξ_y increases, the carrier velocity increases proportionally to the field strength, until eventually velocity saturation occurs. This limiting high-field drift velocity is referred to as the saturation velocity v_{sat}. The critical field for which this happens is given by $\xi_c \cong \frac{v_{sat}}{\mu_s}$. The effect of velocity saturation is modelled just as in the original version of STAG [1]:

$$\mu_{yeff} = \frac{\mu_s}{1 + \frac{\mu_s}{v_{sat}} \frac{\psi_{sL} - \psi_{s0}}{L_{eff}}} \,. \tag{4.45}$$

Combined Mobility Model

The two high field effects give rise to the following expression for the high field effective mobility [1]:

$$\mu_{eff} = \frac{\mu_s}{1 + \theta \cdot \left\{ V_g - \frac{\psi_{sL}+\psi_{s0}}{2} + \gamma_m \left(\sqrt{\psi_{s0}} + \frac{\delta}{2} \left(\psi_{sL} - \psi_{s0} \right) \right) \right\} + \frac{\mu_s}{v_{sat}} \frac{\psi_{sL} - \psi_{s0}}{L_{eff}}} \,. \tag{4.46}$$

If μ_s in Eq. 4.15 is simply replaced by μ_{eff} and we use $\psi_{sL} = \min(\psi_{ss0}, \psi_{siL})$, a non-physical rollover is visible in the output current characteristic around the transition from triode into saturation region [1]. This is explained by the fact that the new mobility model reduces the current for $\psi_s < \psi_{ss0}$, where ψ_{ss0} is used as the saturation voltage, while in fact it is necessary to introduce a saturation surface potential ψ_{sLsat}.

In [13], it is claimed that velocity saturation in LDMOS transistors occurs at the source side because the doping concentration is highest there, but this is not proven. The position of the lateral field maximum also depends on the applied biases and, on whether velocity saturation occurs before channel pinch-off, i.e. for very short channel length devices, the onset position will probably move along the channel. For long channel devices pinch-off generally happens before velocity saturation, and velocity saturation takes places at the internal drain junction, where the lateral field is highest. Considering the above arguments, it is not a good idea to characterise saturation by electron velocity saturation at a fixed position, as they do in [13] ($I_{CHsat} = W\, v_{sat}\, q_{cinv}(y = 0)$). To find the saturation surface potential at $y = L_{eff}$, we search for the value of ψ_{sL} for which the channel current becomes maximal and avoid the problem of the peak position of the lateral field:

$$\left. \frac{\partial I_{chi}}{\partial \psi_{sL}} \right|_{\psi_{sL} = \psi_{sLsat}} = 0 \,. \tag{4.47}$$

If we consider only the drift part of the channel current we find

$$(2\,g\,\psi_{\mathrm{sLsat}} + f_1)\,\left(1 + \theta\cdot\left(V_{\mathrm{g}} - \frac{\psi_{\mathrm{sLsat}} + \psi_{\mathrm{st0}}}{2}\right)\right.$$
$$\left. + \gamma_{\mathrm{m}}\cdot\left(\sqrt{\psi_{\mathrm{st0}}} + \frac{\delta}{2}\left(\psi_{\mathrm{sLsat}} - \psi_{\mathrm{st0}}\right)\right) + \frac{\psi_{\mathrm{sLsat}} - \psi_{\mathrm{st0}}}{L\,\xi_{\mathrm{c}}}\right)$$
$$= M_{\mathrm{mob}}\left(g\cdot\left(\psi_{\mathrm{sLsat}}^2 - \psi_{\mathrm{st0}}^2\right) + f_1\cdot\left(\psi_{\mathrm{sLsat}} - \psi_{\mathrm{st0}}\right)\right) \tag{4.48}$$

with

$$M_{\mathrm{mob}} = -\frac{\theta}{2} + \frac{1}{L_{\mathrm{eff}}\,\xi_{\mathrm{c}}} + \theta\,\gamma_{\mathrm{m}}\,\frac{\delta}{2}\,. \tag{4.49}$$

Replacing ψ_{sLsat} by

$$\psi_{\mathrm{sLsat}} = \psi_{\mathrm{st0}} + \frac{\psi}{S} \tag{4.50}$$

with S as a new variable and $\psi = -\psi_{\mathrm{st0}} - \frac{f_1}{2\,g}$, we find a quadratic equation:

$$S^2 - S - \frac{\psi}{2}\frac{M_{\mathrm{mob}}}{1 + \theta\cdot\left(V_{\mathrm{g}} - \psi_{\mathrm{st0}}\right) + \theta\,\gamma_{\mathrm{m}}\,\sqrt{\psi_{\mathrm{s0}}}} = 0 \tag{4.51}$$

with the solution

$$S = \frac{1}{2} + \frac{1}{2}\sqrt{1 + \frac{2\,\psi\,M_{\mathrm{mob}}}{1 + \theta\cdot\left(V_{\mathrm{g}} - \psi_{\mathrm{st0}}\right) + \theta\,\gamma_{\mathrm{m}}\,\sqrt{\psi_{\mathrm{st0}}}}}\,. \tag{4.52}$$

Note that the second solution of Eq. 4.51 would lead to a negative physically impossible solution for S. Let us know have a closer look at the expression for ψ:

$$\psi = -\psi_{\mathrm{st0}} - \frac{f_1}{2\,g} \tag{4.53}$$
$$= \frac{V_{\mathrm{g}} - \eta_{\mathrm{s}}\,\psi_{\mathrm{st0}} - \gamma_0\,\sqrt{\psi_{\mathrm{s0}}}\left(1 - \frac{k_{\mathrm{N_A}}}{4}\right)}{2\,g} \tag{4.54}$$
$$= \frac{\frac{q_0}{C_{\mathrm{of}}} + \gamma_0\,\sqrt{\psi_{\mathrm{st0}}}\,\frac{k_{\mathrm{N_A}}}{4}}{2\,g}\,. \tag{4.55}$$

In the strong inversion case the term $\gamma_0\,\sqrt{\psi_{\mathrm{st0}}}\,\frac{k_{\mathrm{N_A}}}{4}$ can be neglected compared to $\frac{q_0}{C_{\mathrm{of}}}$. On the other hand, in the subthreshold case q_0 is zero, and neglecting the above mentioned term means $\psi = 0$. So, under subthreshold conditions we find $\psi_{\mathrm{sLsat}} = \psi_{\mathrm{st0}} = \psi_{\mathrm{ss0}}$, which is what we want. Rewriting Eq. 4.50 and omitting the described term in ψ gives the final expression for the saturation surface potential at $y = L_{\mathrm{eff}}$

$$\psi_{\mathrm{sLsatf}} = \psi_{\mathrm{st0}} + \frac{V_{\mathrm{g}} - \eta_{\mathrm{s}}\,\psi_{\mathrm{st0}} - \gamma_0\,\sqrt{\psi_{\mathrm{st0}}}}{2\,g\,S}\,. \tag{4.56}$$

Note that ψ_{sLsatf} is slightly smaller than ψ_{sLsat}, which is not a problem. In the hypothetical case of a slightly larger value, the non-physical roll-over mentioned in the beginning of this section would still be visible over a very small voltage range, which would have been

unacceptable.

4.2.5 Calculation of the Saturation Voltage

In the previous section the saturation surface potential at $y = L_{\text{eff}}$ (ψ_{sLsatf}) was calculated. This saturation effect happens for a certain value of the drain voltage, referred to as the drain saturation voltage V_{dsat}. To calculate V_{dsat}, we look for $V_{\text{DiS}} = V_{\text{dsat}}$ for which $I_{\text{chi}}(\psi_{\text{sLsatf}}) = I_{\text{drg}}(\psi_{\text{sLsatf}}, V_{\text{DiS}})$, i.e.

$$g \cdot \left(\psi_{\text{sLsatf}}^2 - \psi_{\text{st0}}^2\right) + f \cdot (\psi_{\text{sLsatf}} - \psi_{\text{st0}}) = F \cdot (V_{\text{dsat}} + \psi_{\text{st0}} - \psi_{\text{sLsatf}}) + G \cdot \left((V_{\text{dsat}} + \psi_{\text{st0}})^2 - \psi_{\text{sLsatf}}^2\right) . \quad (4.57)$$

This results in

$$V_{\text{dsat}} = \frac{1}{G}\left(-\frac{F}{2} + \sqrt{R_{\text{s}}}\right) - \psi_{\text{st0}} \quad (4.58)$$

with

$$R_{\text{s}} = \frac{F^2}{4} + G \cdot \left(g \cdot (\psi_{\text{sLsatf}}^2 - \psi_{\text{st0}}^2) + f \cdot (\psi_{\text{sLsatf}} - \psi_{\text{st0}}) + \psi_{\text{sLsatf}} \cdot (G\,\psi_{\text{sLsatf}} + F)\right) . \quad (4.59)$$

In subthreshold $\psi_{\text{sLsatf}} \cong \psi_{\text{st0}}$, and hence V_{dsat} as calculated from Eq. 4.58 is close to zero. In the LDMOS model a small constant (0.1 V) is added to V_{dsat} to avoid the condition that V_{dsat} reaches zero when the device is working in subthreshold. This is explained in more detail in Sec. 4.2.7, where the subthreshold current is studied.

To attain a smooth transition from triode into saturation region a smoothing function is invoked to limit V_{DiS} to V_{dsat} [14]:

$$V_{\text{DiSn}} = \frac{V_{\text{DiS}} V_{\text{dsat}}}{((V_{\text{DiS}})^{2m} + (V_{\text{dsat}})^{2m})^{1/2m}} \quad (4.60)$$

with m an empirical parameter, which can take integer values only. For a short channel MOSFET $m = 2$ gives good fits. For longer channel lengths larger values for m have to be used.

4.2.6 The Total Current Expression

All the different aspects of the current under the thin gate oxide studied in the previous sections can now be joined to give the final formulation:

$$I_{\text{CH0}} = \frac{\beta}{1 + \theta \cdot \left\{V_{\text{g}} - \frac{\psi_{\text{sL}}+\psi_{\text{s0}}}{2} + \gamma_{\text{m}} \cdot \left(\sqrt{\psi_{\text{s0}}} + \frac{\delta}{2}(\psi_{\text{sL}} - \psi_{\text{s0}})\right)\right\} + \frac{\mu_{\text{s}}}{v_{\text{sat}}} \frac{\psi_{\text{sL}}-\psi_{\text{s0}}}{L_{\text{eff}}}} \cdot \left(g \cdot \left(\psi_{\text{sL}}^2 - \psi_{\text{s0}}^2\right) + f \cdot (\psi_{\text{sL}} - \psi_{\text{s0}})\right) \quad (4.61)$$

with

$$\psi_{s0} = \phi_t \ln\left(1 + \frac{\exp\left(\frac{\psi_{si0}}{\phi_t}\right)}{1 + \exp\left(\frac{\psi_{si0} - \psi_{sLsatf}}{\phi_t}\right)}\right) \tag{4.62}$$

$$\psi_{sL} = \phi_t \ln\left(1 + \frac{\exp\left(\frac{\psi_{siL}}{\phi_t}\right)}{1 + \exp\left(\frac{\psi_{siL} - \psi_{sLsatf}}{\phi_t}\right)}\right) \tag{4.63}$$

The expression for ψ_{siL} is identical to ψ^*_{siL} (Eq. 4.32), with the difference that V_{DiS} is replaced by V_{DiSn} to include the saturation effects, i.e.

$$\psi_{siL} = \frac{-\frac{B}{2} + \sqrt{\frac{B^2}{4} - A\,C}}{A} \tag{4.64}$$

with A and B defined by Eqs. 4.35 and 4.36, and C given by Eq. 4.37, where V_{DiS} is replaced by V_{DiSn}:

$$C = -\left(g\,\psi_{si0}^2 + f\,\psi_{si0}\right) - F \cdot (V_{DiSn} + \psi_{si0}) - G \cdot (V_{DiSn} + \psi_{si0})^2 \ . \tag{4.65}$$

4.2.7 The Sub-Threshold Current

In the sub-threshold regime the current is dominated by the diffusion current in the MOSFET part of the LDMOS and can be approximated as follows using Taylor approximations:

$$I_{CH0,\,sub-threshold} \cong \frac{\beta\mu_{eff}}{\mu_s}\,(f_2 \cdot (\psi_{sL} - \psi_{s0})) \tag{4.66}$$

$$\cong \frac{\beta\mu_{eff}}{\mu_s}\left\{f_2 \cdot \left(\psi_{ss0} + \phi_t\,\exp\left(\frac{-\psi_{ss0}}{\phi_t}\right) - \phi_t \exp\left(\frac{\psi_{ss0} - \psi_{si0} - V_{DiSn}}{\phi_t}\right)\right.\right.$$
$$\left.\left. -\psi_{ss0} - \phi_t \exp\left(\frac{-\psi_{ss0}}{\phi_t}\right) + \phi_t \exp\left(\frac{\psi_{ss0} - \psi_{si0}}{\phi_t}\right)\right)\right\} \tag{4.67}$$

$$\cong \frac{\beta\,\mu_{eff}}{\mu_s}\left\{f_2\,\phi_t\,\exp\left(\frac{\psi_{ss0} - \psi_{si0}}{\phi_t}\right)\left(1 - \exp\left(-\frac{V_{DiSn}}{\phi_t}\right)\right)\right\} \tag{4.68}$$

In Eq. 4.68 we recognise the same exponential functions as for the standard MOSFET [11]. In the sub-threshold regime ψ_{sL} is the minimum of ψ_{siL} and ψ_{ss0}; this value is slightly larger than ψ_{s0} if $V_{DiSn} > 0$.

Let us now come back to the comment made in Sec. 4.2.5. Setting $V_{dsat} = 0$ would result in $V_{DiSn} = 0$ and $\psi_{siL} = \psi_{si0}$, which would give a zero current instead of the subthreshold current. Thus we require a small off-set value for V_{dsat}, usually selected of the order of ϕ_t. For this very reason the value of 0.1 V was added to V_{dsat} in Sec. 4.2.5.

4.2.8 Auxiliary Model

To model the short and narrow channel effects on the value of the threshold voltage we use [1]

$$\gamma_{\text{eff}} = \gamma_0 \cdot \left(1 - \frac{\Delta L}{L_{\text{eff}}}\right)\left(1 - \frac{\Delta W}{W}\right) . \tag{4.69}$$

For the Drain induced barrier lowering (DIBL) effect, we write [1]

$$V_{\text{FBeff}} = V_{\text{FB}}^{\text{f}} - \gamma_{oo}\, V_{\text{DiS}} , \tag{4.70}$$

where $\gamma_{oo} = \frac{\sigma}{L_{\text{eff}}}$. Two models are included for the channel length modulation (CLM) effect. In the saturation region, an increase in V_{DiS} causes the pinch-off point of the channel to move towards the source. The reduction in channel length, referred to as l_{d} can be described by a simple model [1]:

$$l_{\text{d}} = \lambda_{\text{r}} \cdot (V_{\text{DiS}} - V_{\text{DiSn}}) . \tag{4.71}$$

The second short-channel model [1] is given by

$$l_{\text{d}} = l_{\text{x}} \ln\left(1 + \frac{(V_{\text{DiS}} - V_{\text{DiSn}})}{V_{\text{p}}}\right) . \tag{4.72}$$

The simple model is the default. The only way the short-channel model can be invoked, is by specifying a non-zero V_{p} and a non-zero l_{x} and not specifying λ_r. With channel length modulation we obtain

$$I_{\text{CH}} = I_{\text{CH0}}\left(1 + \frac{l_{\text{d}}}{L_{\text{eff}}}\right) \tag{4.73}$$

for the channel current. The CLM and DIBL effect in LDMOS transistors are a lot smaller than in standard MOSFET because a large part of the drain voltage drops over the drift region. However, for low gate biases, it is important to take the CLM effects into account because it determines the value of the output conductance in the saturation regime.

4.3 Drift Current under the Field Oxide

The current flow in the drift region is illustrated in Fig. 4.6. When the back gate voltage is made very negative, the surface at the buried oxide can be partially (which is the case in the example illustrated in Fig. 4.6) or fully inverted, depending on the channel potential ψ.

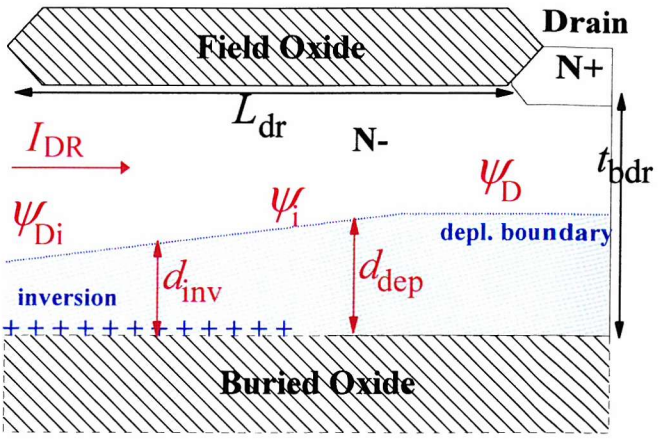

Figure 4.6: Current flow in the drift region under high side conditions.

4.3.1 The Intrinsic Drift Current

Neglecting diffusion current, the channel current can be written as the current in a depletion-type MOSFET with the back gate acting as the gate terminal [11]

$$I_{DR0} = \frac{W}{L_{dr}} \mu_{dr}\, q\, N_D \int_{\psi_{Di}}^{\psi_D} (t_{bdr} - d(\psi)) \cdot d\psi \,, \tag{4.74}$$

where $d(\psi)$ is the depletion layer thickness extending from the buried oxide into the silicon, and t_{bdr} the silicon thickness under the field oxide. The channel potentials ψ_{Di} and ψ_D are shown in Fig. 4.6. In this section all potentials are referenced with respect to the neutral bulk potential minus ϕ_{bid}.

We consider two definitions for the depletion layer thickness, before and after inversion. Before inversion the depletion layer thickness is referred to as d_{dep} and given by [11]

$$\begin{aligned} d_{dep} &= -\frac{\epsilon_{si}}{C_{ob}} + \sqrt{\left(\frac{\epsilon_{si}}{C_{ob}}\right)^2 + \frac{2\,\epsilon_{si}}{q\,N_D}(-V_{gb} + \psi)} \\ &\cong \frac{C_{ob}}{q\,N_D}(-V_{gb} + \psi) \,, \end{aligned} \tag{4.75}$$

with $V_{gb} = V_{GbB} - V_{FB}^{bdr}$, and C_{ob} the buried oxide capacitance per unit area. In standard depletion type MOSFET devices, the possibility of surface inversion is usually excluded for practical devices. However, when an LDMOS is working under high side conditions, the formation of an inversion layer is crucial to limit the further increase in ON-resistance. If the surface at the buried oxide is inverted, the depletion layer thickness is referred to as d_{inv} and can be expressed as

$$d_{inv} = \sqrt{\frac{2\,\epsilon_{si}\,(2\,\phi_{Fdr} + \psi)}{q\,N_D}} \,, \tag{4.76}$$

where we have used the depletion layer approximation from [4], and where the inver-

sion surface potential is approximated as $2\phi_{\mathrm{Fdr}} + \psi$. To obtain closed-form analytical expressions for the saturation potentials in the next section, the square root of the surface potential is linearly approximated with a Taylor approximation around $2\phi_{\mathrm{Fdr}}$:

$$d_{\mathrm{inv}} \cong \sqrt{\frac{2\,\epsilon_{\mathrm{si}}}{q\,N_{\mathrm{D}}}}\left(\sqrt{2\,\phi_{\mathrm{Fdr}}} + \delta_{\mathrm{dr}}\,\psi\right) , \tag{4.77}$$

with $\delta_{\mathrm{dr}} = \frac{1}{2\sqrt{1+2\phi_{\mathrm{Fdr}}}}$. In Fig. 4.7 the linearised and ideal depletion layer thicknesses

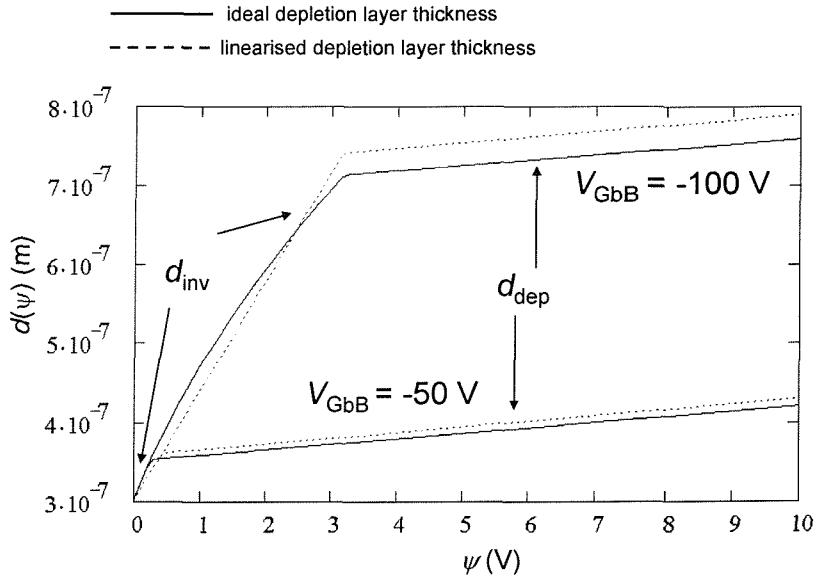

Figure 4.7: Comparison of the linearised (dotted line) and ideal (full line) formulation of the depletion layer thickness: $d(\psi)$ vs. ψ for $V_{\mathrm{GbB}} = -50$ V and -100 V.

d_{dep} and d_{inv} are compared for typical parameters (see Table 1.3 in Chapter 1). Very good agreement is obtained for low values of ψ and V_{GbB}. For higher values the deviation increases, but remains below 5%.

Using the linearised formulations for $d(\psi)$ the integral in Eq. 4.74 can be rewritten as:

$$\int_{\psi_{\mathrm{Di}}}^{\psi_{\mathrm{D}}} (t_{\mathrm{bdr}} - d(\psi)) \cdot d\psi = t_{\mathrm{bdr}} \cdot (\psi_{\mathrm{D}} - \psi_{\mathrm{Di}}) - \int_{\psi_{\mathrm{Di}}}^{\psi_{\mathrm{i}}} d_{\mathrm{inv}}(\psi) \cdot d\psi - \int_{\psi_{\mathrm{i}}}^{\psi_{\mathrm{D}}} d_{\mathrm{dep}}(\psi) \cdot d\psi , \tag{4.78}$$

where ψ_{i} is the potential at the end of the inversion layer as denoted in Fig. 4.6. This potential can be calculated from $d_{\mathrm{inv}}(\psi_{\mathrm{i}}) = d_{\mathrm{dep}}(\psi_{\mathrm{i}})$,

$$\psi_{\mathrm{i}} = \frac{\gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{gb}}}{1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}} , \tag{4.79}$$

with $\gamma^{\mathrm{bdr}} = \frac{\sqrt{2\epsilon_{\mathrm{si}} q N_{\mathrm{D}}}}{C_{\mathrm{ob}}}$ being the back gate body factor in the drift region. The potentials at the internal drain node and at the drain can be expressed in terms of the nodal voltages using $\psi_{\mathrm{Di}} = V_{\mathrm{DiB}}$ and $\psi_{\mathrm{D}} = V_{\mathrm{DB}}$. Substituting Eqs. 4.75, 4.77 and 4.79 into Eq. 4.78

results in

$$I_{\mathrm{DR0}} = \frac{1}{R_{\mathrm{ON}}^{\mathrm{dr}}} \left\{ V_{\mathrm{DB}} - V_{\mathrm{DiB}} - \frac{1}{V_{\mathrm{Pdep}}} \left(\gamma^{\mathrm{bdr}} H_{1\mathrm{t}} + H_{2\mathrm{t}} \right) \right\} , \tag{4.80}$$

with

$$R_{\mathrm{ON}}^{\mathrm{dr}} = \frac{L_{\mathrm{dr}}}{W \, \mu_{\mathrm{dr}} \, q \, N_{\mathrm{D}} \, t_{\mathrm{bdr}}} \tag{4.81}$$

$$V_{\mathrm{Pdep}} = \frac{q \, N_{\mathrm{D}} \, t_{\mathrm{bdr}}}{C_{\mathrm{ob}}} \tag{4.82}$$

$$H_{1\mathrm{t}} = \left((V_{\mathrm{DBf0}} - V_{\mathrm{DiB}}) \sqrt{2 \, \phi_{\mathrm{Fdr}}} + \frac{\delta_{\mathrm{dr}}}{2} \left(V_{\mathrm{DBf0}}^2 - V_{\mathrm{DiB}}^2 \right) \right) \tag{4.83}$$

$$H_{2\mathrm{t}} = \frac{1}{2} \left((-V_{\mathrm{gb}} + V_{\mathrm{DB}})^2 - (-V_{\mathrm{gb}} + V_{\mathrm{DBf0}})^2 \right) \tag{4.84}$$

and $V_{\mathrm{DBf0}} = \min_{\mathrm{hyp}}(V_{\mathrm{DB}}, \max_{\mathrm{hyp}}(V_{\mathrm{DiB}}, \psi_{\mathrm{i}}))$. The "$\min_{\mathrm{hyp}}$" and "$\max_{\mathrm{hyp}}$" functions describe a smooth and continuous minimum and maximum respectively, and can be found in App. C. Note that $R_{\mathrm{ON}}^{\mathrm{dr}}$ can be recognized as the ON-resistance of the drift region under zero bias conditions. V_{Pdep} is the pinch-off voltage when the back surface is not inverted and $V_{\mathrm{gb}} = 0$.

4.3.2 Saturation by Pinch-off

The maximum value for the depletion layer thickness is t_{bdr}. The channel voltage at which this happens is called the pinch-off voltage. Let us assume in the following reasoning that $V_{\mathrm{DB}} > V_{\mathrm{DiB}}$; otherwise V_{DB} and V_{DiB} only need to be swapped in the current equation. To calculate the pinch-off voltage, we have to consider two different bias situations:

- $V_{\mathrm{DiB}} > \psi_{\mathrm{i}}$: no inversion at the buried oxide

  The pinch-off voltage V_{satdep} can be found by equating d_{dep} to t_{bdr}:

$$V_{\mathrm{satdep}} = V_{\mathrm{gb}} + V_{\mathrm{Pdep}} . \tag{4.85}$$

- $\psi_{\mathrm{i}} > V_{\mathrm{DiB}}$: inversion at the buried oxide

  The pinch-off voltage V_{satinv} can be found by equating d_{inv} to t_{bdr}:

$$V_{\mathrm{satinv}} = \frac{V_{\mathrm{Pdep}} - \gamma^{\mathrm{bdr}} \sqrt{2\phi_{\mathrm{Fdr}}}}{\delta \, \gamma^{\mathrm{bdr}}} . \tag{4.86}$$

Both V_{DiB} and V_{DB} are limited smoothly to the maximum of V_{satinv} and V_{satdep}. It can be proven that when $V_{\mathrm{DiB}} > \psi_{\mathrm{i}}$, this maximum corresponds to V_{satdep}, and when $V_{\mathrm{DiB}} < \psi_{\mathrm{i}}$, it corresponds to V_{satinv} (see App. D). In conclusion, we obtain the pinch-off voltage

$$V_{\mathrm{Psat}} = \max_{\mathrm{hyp}}(V_{\mathrm{satdep}}, V_{\mathrm{satinv}}) . \tag{4.87}$$

To include saturation by pinch-off in the drift current expression, V_{DiB} and V_{DB} have to be replaced by

$$V_{\mathrm{DiBs}} = \min_{\mathrm{sm1}}(V_{\mathrm{DiB}}, V_{\mathrm{Psat}}) \tag{4.88}$$

$$V_{\mathrm{DBst}} = \min_{\mathrm{sm1}}(V_{\mathrm{DB}}, V_{\mathrm{Psat}}) \; . \tag{4.89}$$

The smoothing functions "$\max_{\mathrm{hyp}}$" and "$\min_{\mathrm{sm1}}$" can be found in App. C.

4.3.3 Velocity Saturation

For low electric fields the equations developed in the previous section can describe the device behaviour reasonably well. However, for higher drain biases the high field velocity saturation effects can no longer be neglected. To account for the velocity saturation effects we replace the low-field mobility μ_{dr} with [15]

$$\mu_{\mathrm{dreff}} = \frac{\mu_{\mathrm{dr}}}{1 + \theta_{3\mathrm{dr}}(V_{\mathrm{DB}} - V_{\mathrm{DiB}})} \tag{4.90}$$

with $\theta_{3\mathrm{dr}} = \frac{\mu_{\mathrm{dr}}}{v_{\mathrm{satdr}}\, L_{\mathrm{dr}}}$. The quantity v_{satdr} is the saturation value for the drift velocity, which in theory is 10^7 cm/s for silicon [15].

Both V_{DB} and V_{DiB} have to be limited due to velocity saturation effects. To calculate the saturation potential, we have to consider three different bias situations:

- $V_{\mathrm{DB}} > V_{\mathrm{DiB}} > \psi_{\mathrm{i}}$: no inversion at the buried oxide, and hence $V_{\mathrm{DBf0}} = V_{\mathrm{DiB}}$

  To find the velocity saturation potential V_{sat1} we solve

  $$\left.\frac{\partial I_{\mathrm{DR0}}}{\partial V_{\mathrm{DB}}}\right|_{V_{\mathrm{DB}}=V_{\mathrm{sat1}}} = 0 \tag{4.91}$$

  and get

  $$V_{\mathrm{sat1}} = V_{\mathrm{DiBs}} - \frac{1}{\theta_{3\mathrm{dr}}} + \sqrt{\frac{1}{\theta_{3\mathrm{dr}}^2} - 2\frac{V_{\mathrm{DiBs}}}{\theta_{3\mathrm{dr}}} + 2\frac{V_{\mathrm{satdep}}}{\theta_{3\mathrm{dr}}}} \; . \tag{4.92}$$

- $V_{\mathrm{DB}} > \psi_{\mathrm{i}} > V_{\mathrm{DiB}}$: the surface at the buried oxide is partly inverted, and hence $V_{\mathrm{DBf0}} = \psi_{\mathrm{i}}$. To find the saturation potential V_{sat2} we solve

  $$\left.\frac{\partial I_{\mathrm{DR0}}}{\partial V_{\mathrm{DB}}}\right|_{V_{\mathrm{DB}}=V_{\mathrm{sat2}}} = 0 \tag{4.93}$$

  and obtain

  $$V_{\mathrm{sat2}} = V_{\mathrm{DiBs}} - \frac{1}{\theta_{3\mathrm{dr}}} + \sqrt{\frac{1}{\theta_{3\mathrm{dr}}^2} - 2\frac{V_{\mathrm{DiBs}}}{\theta_{3\mathrm{dr}}} + 2\frac{V_{\mathrm{satdep}}}{\theta_{3\mathrm{dr}}} + (\psi_{\mathrm{i}} - V_{\mathrm{DiBs}})^2\,(1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}})} \; . \tag{4.94}$$

- $\psi_{\mathrm{i}} > V_{\mathrm{DB}} > V_{\mathrm{DiB}}$: inversion along the whole length of the buried oxide, and hence

$V_{\mathrm{DBf0}} = V_{\mathrm{DB}}$. To find the saturation potential V_{sat3} we evaluate

$$\left.\frac{\partial I_{\mathrm{DR0}}}{\partial V_{\mathrm{DB}}}\right|_{V_{\mathrm{DB}}=V_{\mathrm{sat3}}} = 0 \tag{4.95}$$

which yields

$$V_{\mathrm{sat3}} = V_{\mathrm{DiBs}} - \frac{1}{\theta_{3\mathrm{dr}}} + \sqrt{\frac{1}{\theta_{3\mathrm{dr}}^2} - 2\frac{V_{\mathrm{DiBs}}}{\theta_{3\mathrm{dr}}} + 2\frac{V_{\mathrm{satinv}}}{\theta_{3\mathrm{dr}}}}\,. \tag{4.96}$$

These three expressions can be transformed into one single expression for the drain saturation potential:

$$V_{\mathrm{sat}}^{*} = V_{\mathrm{DiBs}} - \frac{1}{\theta_{3\mathrm{dr}}} + \sqrt{\frac{1}{\theta_{3\mathrm{dr}}^2} - 2\frac{V_{\mathrm{DiBs}}}{\theta_{3\mathrm{dr}}} + 2\frac{V_{\mathrm{Psat}}}{\theta_{3\mathrm{dr}}} + \left(\psi_{\mathrm{i}} - V_{\mathrm{DiB}}^{\mathrm{e}}\right)^2 \left(1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}\right)}\,, \tag{4.97}$$

with

$$V_{\mathrm{DiB}}^{\mathrm{e}} = \max_{\mathrm{hyp}}\left(\min_{\mathrm{hyp}}\left(V_{\mathrm{DiBs}}, \psi_{\mathrm{i}}\right), \psi_{\mathrm{i}} - \sqrt{\frac{2}{\theta_{3\mathrm{dr}}}\mathrm{pos}_{\mathrm{sm}}\left(V_{\mathrm{Pinv}} - \psi_{\mathrm{i}}\right)}\right)\,. \tag{4.98}$$

Limiting V_{DBst} to V_{sat}^{*} results in the final expression for V_{DBs}:

$$V_{\mathrm{DBs}} = V_{\mathrm{DiBs}} + \min_{\mathrm{sat}}\left(V_{\mathrm{DBst}} - V_{\mathrm{DiBs}}, V_{\mathrm{sat}}^{*} - V_{\mathrm{DiBs}}\right)\,. \tag{4.99}$$

The final expression for the drift current, including pinch-off and velocity saturation

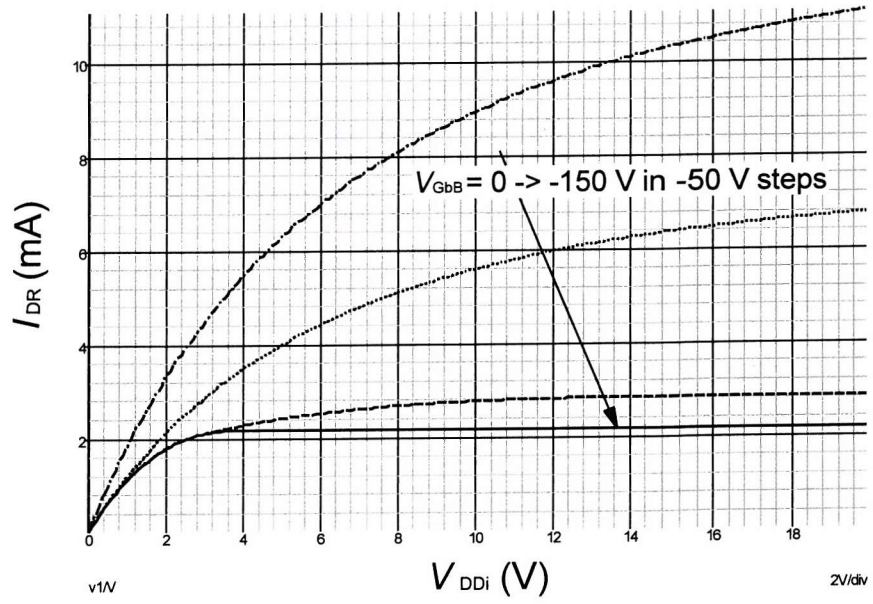

Figure 4.8: Drift current vs. V_{DDi} for different back gate biases.

effects is given by

$$I_{\mathrm{DR}} = \frac{1}{R_{\mathrm{ON}}^{\mathrm{dr}}\left(1+\theta_{3\mathrm{dr}}\cdot\left(V_{\mathrm{DB}}-V_{\mathrm{DiB}}\right)\right)}\left\{V_{\mathrm{DBs}}-V_{\mathrm{DiBs}}-\frac{1}{V_{\mathrm{Pdep}}}\left(\gamma^{\mathrm{bdr}}\,H_1+H_2\right)\right\} \quad (4.100)$$

$$H_1 = \left(V_{\mathrm{DBf}}-V_{\mathrm{DiBs}}\right)\sqrt{2\,\phi_{\mathrm{Fdr}}}+\frac{\delta_{\mathrm{dr}}}{2}\left(V_{\mathrm{DBf}}^2-V_{\mathrm{DiBs}}^2\right) \quad (4.101)$$

$$H_2 = \frac{1}{2}\left(\left(-V_{\mathrm{gb}}+V_{\mathrm{DBs}}\right)^2-\left(-V_{\mathrm{gb}}+V_{\mathrm{DBf}}\right)^2\right) \quad (4.102)$$

and $V_{\mathrm{DBf}} = \min_{\mathrm{hyp}}(V_{\mathrm{DBs}}, \max_{\mathrm{hyp}}(V_{\mathrm{DiBs}}, \psi_{\mathrm{i}}))$. The expressions for $V_{\mathrm{DiB}}^{\mathrm{e}}$, V_{DBs} and V_{DBf} use smoothing functions to ensure the continuity of the equations; these can be found in App. C.

Fig. 4.8 shows the drift current vs. V_{DDi} for different back gate biases. Note the continuous description of the different saturation effects, and the current decrease with increasingly negative back gate voltage.

4.4 Modelling Heating Effects

At room temperature, self-heating effects have been long since well known for high power dissipation levels in DMOS [16–18] and other high voltage devices [19]. Later, self-heating was observed at moderate power dissipation in VLSI bulk MOSFETs [20] and SOI MOSFETs [21].

In any technology there is a finite thermal resistance from the active area to its surroundings, which implies that the device temperature will be higher than the ambient temperature when significant power is dissipated. This causes a reduction in drain current, which can sometimes be sufficiently strong to cause a negative output resistance [22]. In a SOI technology this thermal resistance is much higher than in its bulk counterpart, especially for high voltage devices where the buried oxide layer can be up to 3 μm thick.

The finite thermal capacitance causes the device temperature not to follow the device power instantaneously, and so it is important to consider self-heating as a dynamic effect [23–25]. The effects of self-heating are most noticeable in the saturation region, which is the normal region of operation for analogue circuits. A slow variation of the drain voltage in the saturation region causes a change in device temperature, which in turn affects the current. At higher frequencies, the channel temperature can no longer follow the power dissipation and the heat-flow is effectively low-pass filtered [26]. This increase of the output conductance with frequency due to the thermal time constant (typically in the range of 100 kHz to 1 MHz) is of extreme importance for analogue designers, since the output conductance determines the gain of any amplifier.

In ultra-thin RESURF SOI LDMOS structures, the distribution of the heat generation in the drift region will be highly non-uniform, but will be quite constant in thicker SOI LDMOS devices [27,28]. To model a non-uniform temperature rise of the device, the 2-D

heat flow equation [29] has to be solved using numerical methods. This, however, is very time consuming, and in compact models it is usually preferred [1, 21] to assume thermal equilibrium and use an average temperature rise ΔT.

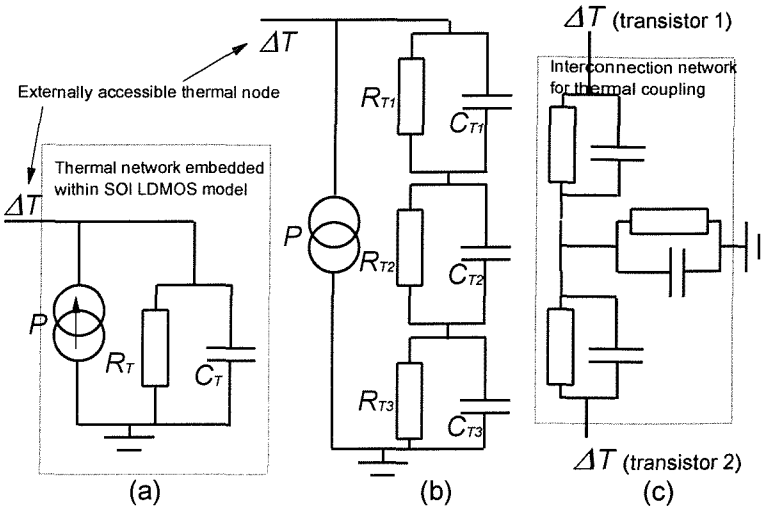

Figure 4.9: (a) First order thermal circuit; (b) Three time constant thermal netlist; (c) Example of an interconnection network for the simulation of thermal coupling.

Because of the analogy between thermal heat flow and electrical current flow, a separate circuit is used to model the thermal behaviour of a device [24, 30]. The thermal circuit consists of a thermal resistance (R_{T}) and a thermal capacitance (C_{T}) and is shown in Fig. 4.9. The thermal network embedded within the model has only one time constant. However, if more thermal time constants have to be taken into account [31] a higher order network can be added externally as shown in Fig. 4.9(b). The thermal node can also be connected to a thermal interconnection network for the simulation of thermal coupling between devices, i.e. the influence of the temperature rise in one device on other neighbouring devices (Fig. 4.9(c)).

In the case of a first order thermal circuit, the simulated temperature rise is obtained from

$$P = \frac{\Delta T}{R_{\mathrm{T}}} + C_{\mathrm{T}} \frac{d(\Delta T)}{dt} \,. \tag{4.103}$$

The dissipated power in the SOI LDMOS is given by

$$P = I_{\mathrm{CH}} V_{\mathrm{DiS}} + I_{\mathrm{DR}} V_{\mathrm{DDi}} \tag{4.104}$$

from which the simulated temperature rise can be determined via Eq. 4.103. To find the small-signal equivalent of the thermal circuit, the thermal dissipation has to be differentiated with respect to ΔT, V_{DiB}, V_{GfB}, V_{GbB}, V_{DB} and V_{SB}, just as with all the other electrical current expressions in the compact model. The temperature rise is treated as another voltage which SPICE has to solve for, and the local device temperature rise is available to model developers as another terminal voltage.

Measurement Set-up	Optimised Parameter
I_D-V_{GfS}, V_{GfS} just above V_{th0},V_{DS}=0.1V	μ_s, μ_{acc}, V_{th0}
I_D-V_{GfS},V_{DS}=0.1V	θ, θ_{acc}
I_D-V_{GfS},V_{DS}=0.1V, high V_{GfS}	N_D
I_D-V_{GfS},low V_{GfS}, V_{DS}=V_{Gfmax}/2,V_{Gfmax}	θ
I_D-V_{GfS},medium-high V_{GfS}, V_{DS}=V_{Gfmax}/2,V_{Gfmax}	v_{sat}
g_{DS}-V_{DS}, V_{BS}=0V, V_{GfS}=V_{th0}+0.1V,..,V_{th0}+3.1	((l_x and V_P) or λ_r), σ
I_{DS}-V_{DS}, V_{BS}=0V, V_{GfS}=V_{th0}+0.1V,..,V_{th0}+3.1	θ, v_{sat}
I_{DS}-V_{DS}, low-medium V_{DS}, V_{GfS}=V_{Gfmax}-3V,..,V_{Gfmax}	v_{satdr}, N_D, μ_{dr}
I_D-V_{GfS}, V_{GfS}=V_{th0}-0.5V,...,V_{th0}+0.5V, V_{DS}=0.1V,V_{Gfmax}/2,V_{Gfmax}, V_{BS}=0V	σ
I_D-V_{GfS}, V_{GfS}=V_{th}-0.5V,...,V_{th}+0.5V, V_{DS}=0.1V,V_{Gfmax}/2,V_{Gfmax}, V_{BS}=0,-1,-2V	N_A

Table 4.1: *Measurement set-ups for parameter extraction*

For all the temperature dependent parameters of the model, a conversion from the nominal temperature (T_{nom}) to the ambient temperature (TEMP = T_{amb}) is performed in a parameter preprocessing stage of the simulation (see Sec. C.5.2 in App. C). T_{nom} is the measurement temperature, and TEMP = T_{amb} is the temperature specified on the instance line of the device. The local self- and coupled heating induced temperature rise, ΔT, is used to modify the values of only those parameters which have a major contribution to the device behaviour (see Sec. C.5.3 in App. C). This is because this operation has to be performed at each Newton-Raphson iteration, and including the effect of ΔT for every temperature dependent parameter would drastically increase computation time.

4.5 Validation

Test chips were fabricated on a commercial HV SOI process containing single LV and MV LDMOS structures with different geometries. In this section, the measured data from the single device characteristics are presented in comparison with the compact SOI LDMOS model simulations. LV LDMOS devices with two different overlap lengths (L_{drov} = 1.2 μm and L_{drov} = 3.2 μm) and MV LDMOS devices with three different drift lengths (L_{dr} = 3.7 μm, L_{dr} = 5.7 μm and L_{drov} = 7.7 μm) were selected for detailed study. This choice represents a comprehensive range of geometries used for the LV and MV SOI LDMOS transistors in the HV SOI process. The parameter extraction procedure used is very similar to the one used in Secs. 3.2.7 and 3.3.3, with the difference that less parameters need to be extracted, which facilitates the optimisation procedure. The initial values for V_{th0} and k_{N_A} can be extracted as explained in Sec. 2.2.3. For the other parameters, their physical values are used as an initial guess prior to an optimisation procedure, which fits simulations to measurements for a particular measurement set-up as shown in Table 4.1.

Using this optimisation technique and starting with a good first guess for all the

Parameter	Initial	Optimised
V_{th0}	2.6 V	2.75 V
N_A	0.95 10^{17}/ cm^3	0.75 10^{17}/ cm^3
k_{N_A}	1	1.4
μ_s	750 $cm^2/(V.s)$	700 $cm^2/(V.s)$
θ	0.03 V^{-1}	0.045 V^{-1}
μ_{acc}	750 $cm^2/(V.s)$	750 $cm^2/(V.s)$
θ_{acc}	0.03 V^{-1}	0.04 V^{-1}
v_{sat}	1 10^7 cm/s	2.2 10^7 cm/s
σ	0	0
N_D	1 10^{16} /cm^3	1.3 10^{16} /cm^3
μ_{dr}	1450 $cm^2/(V.s)$	1250 $cm^2/(V.s)$
v_{satdr}	1 10^7 cm/s	1.4 10^7 cm/s
f_v	1	0.3
λ_r	5 10^{-9} m/V	5 10^{-9} m/V
L	1.5 μm	1.45 μm
L_D	0.3 μm	not optimised
t_{of}	60 nm	not optimised
t_{ob}	3 μm	not optimised
t_b	1.5 μm	not optimised
t_{bdr}	0.9 μm	not optimised
m	2	not optimised
χ_{FB}	-3 10^{-3} (extracted)	not optimised
k	1.7 (extracted)	not optimised
k_{acc}	2 (extracted)	not optimised
k_{dr}	2.2 (extracted)	not optimised

Table 4.2: *The optimised parameters compared to their initial values*

parameters, we have obtained a parameter set for the LV and MV LDMOS, which is given in Table 4.2. Most optimised values are very close to their initial values, indicating that the model is very physical. The only exceptions are the optimised saturation velocities v_{sat} and v_{satdr}, which are considerably higher than the initial physical value. The only difference between the LV and MV LDMOS is that we have added a different drain series resistance for the LV and MV SOI LDMOS (R_D (LV) = 57 Ω for W = 50 μm and R_D (MV) = 30 Ω for W = 50 μm). For completeness the impact ionisation and diode parameters are also given in App. G, but these have not been optimised.

In many processes only a couple of different values for L_{dr} and L_{drov} are available, and different parameter sets can be used for the different geometries to obtain better fits. The reason why this can be advantageous is that, because of 2-D effects, the lateral scaling is not perfect. 2-D effects are more important for the shorter devices. However, here we have chosen to use one single parameter set for the whole range of geometries to show that the scaling is reasonably accurate.

4.5.1 Linear Characteristics

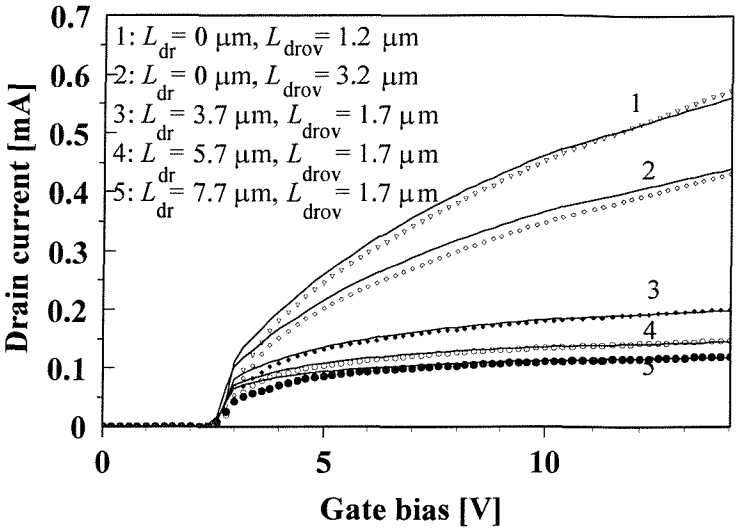

Figure 4.10: Measured (markers) and simulated (full line) drain current in the linear region for different geometries and $V_{DS} = 0.1$ V.

The linear characteristic for the different geometries is shown in Fig. 4.10. As can be seen, the SOI LDMOS model matches the measured data very well in almost all regions.

Curves 1 and 2 show the drain current decrease with increasing L_{drov}, and curves 3, 4 and 5 show the current decrease with increasing L_{dr}. The match is very good for gate voltages more than 2 V above the threshold voltage but just above the threshold, the model over-estimates the measured current. The fit can be made better by using a lower value for the doping gradient, but this is not physical and would also reduce the saturation current for low gate biases, which is otherwise well predicted (see next section) when $k_{N_A} = 1.4$ is used.

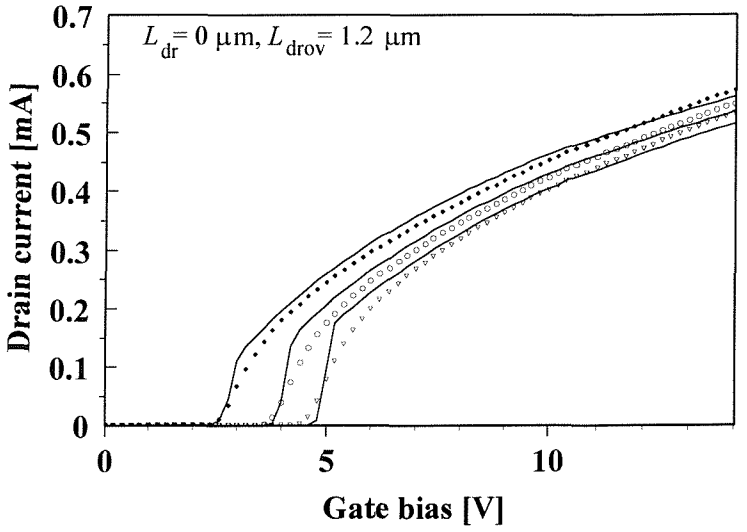

Figure 4.11: Measured (markers) and simulated (full line) current in the linear region for $V_{DS} = 0.1$ V and $V_{BS} = 0$ V, -1 V and -2 V.

Fig. 4.11 shows the linear characteristic for different body voltages. Again the match is very good for gate voltages more than 2 V above the threshold voltage, but just above threshold the simulation results over-estimate the current. The reason for this excessively large simulated current has its origin in the approximation for the body factor employed in Eq. 4.13. Just above the threshold the body factor is not exactly a linear function of the surface potential; the lower threshold at the drain end of the inversion channel causes the inversion at the source end to be considerably less than at the drain end, and hence the main part of the drain voltage will drop over the source end of the inversion layer, becoming almost constant towards the point where $y = L_{\text{eff}}$. Because of the assumption that γ is a linear function of ψ_s, the inversion charge in the intergral of Eq. 4.5 will be over-estimated just above the threshold for values between ψ_{s0} and ψ_{sL}, explaining the slightly over-estimated current.

4.5.2 Output Characteristics

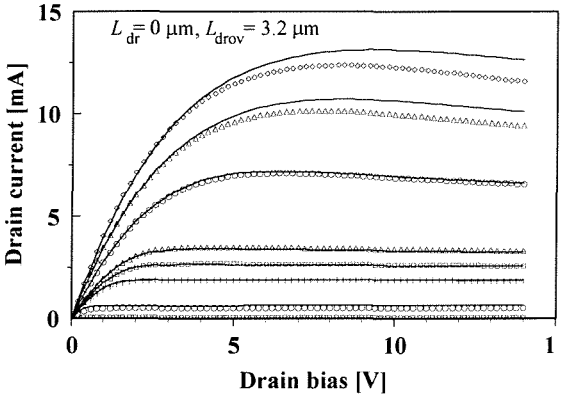

Figure 4.12: LV LDMOS with $L_{\text{drov}} = 3.2\mu$m; measured (markers) and simulated (full line) current vs. V_{DS} for V_{GfS} = 3.5 V, 4.5 V, 5 V, 5.5 V, 8 V, 11 V and 14 V

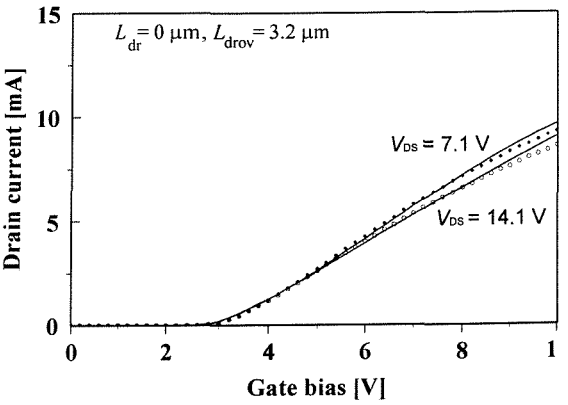

Figure 4.13: LV LDMOS with $L_{\text{drov}} = 3.2\ \mu$m; measured (markers) and simulated (full line) current vs. V_{GfS} for V_{DS} = 7.1 V and V_{DS} = 14.1 V.

Output characteristics for the LV and MV LDMOS are shown in Figs. 4.12 and 4.14 respectively. In almost all cases the model yields a good match with the measured data. The onset of saturation is well predicted, proving that pinch-off and saturation effects in the drift region are well modelled. For the LV LDMOS the drain saturation current keeps increasing with the gate bias, while for the MV LDMOS the drift region limits the current much more noticeably. The model predicts well the decrease in current due to self-heating, which can lead to a negative resistance in some bias situations.

Another interesting characteristic for the SOI LDMOS is the drain current vs. the gate bias for two different high drain biases. These are plotted for the LV and MV LDMOS in Figs. 4.13 and 4.15 respectively. Self-heating is very noticeable in these curves because, above a certain gate voltage, the curves cross each other, leading to a higher current for

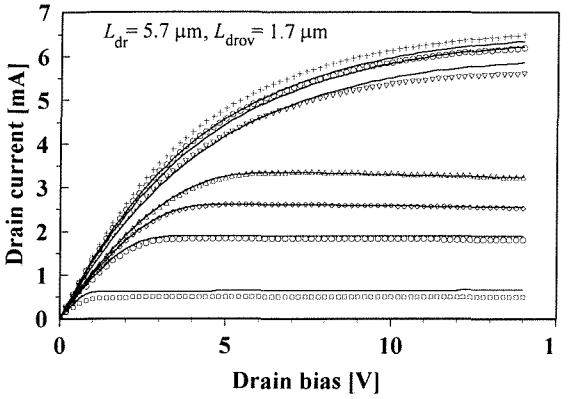

Figure 4.14: MV LDMOS with $L_{\mathrm{drov}} = 1.7\ \mu\mathrm{m}$ and $L_{\mathrm{dr}} = 5.8\ \mu\mathrm{m}$; measured (markers) and simulated (full line) current vs. V_{DS} for $V_{\mathrm{GfS}} =$ 3.5 V, 4.5 V, 5 V, 5.5 V, 8 V, 11 V and 14 V.

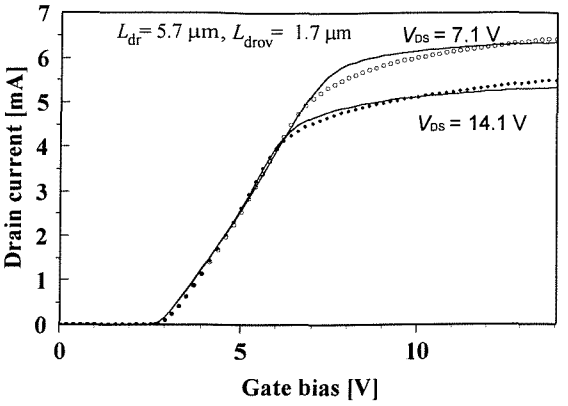

Figure 4.15: MV LDMOS with $L_{\mathrm{drov}} = 1.7\ \mu\mathrm{m}$ and $L_{\mathrm{dr}} = 5.8\ \mu\mathrm{m}$; measured (markers) and simulated (full line) current vs. V_{GfS} for $V_{\mathrm{DS}} =$ 7.1 V and $V_{\mathrm{DS}} = 14.1$ V.

the lower drain bias.

4.5.3 High-Side Behaviour

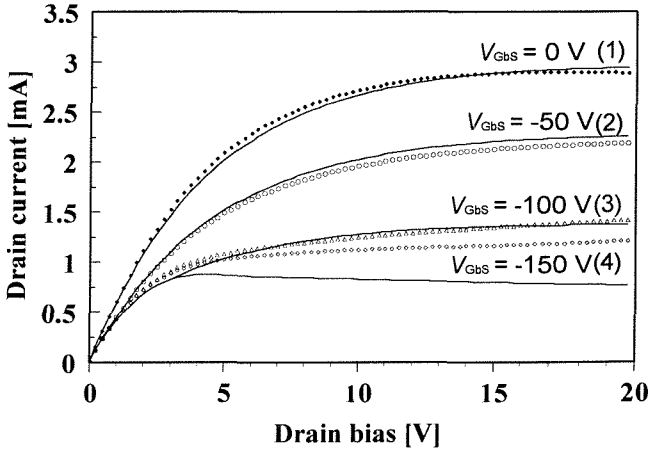

Figure 4.16: Measured (markers) and simulated (full line) current for $V_{\mathrm{GfS}} = 10$ V and $V_{\mathrm{GbS}} = 0$ V, -50 V, -100 V and -150 V.

Fig. 4.16 shows the device working under high-side conditions. We observe a current decrease with increasingly negative back gate bias, but when inversion is established the back gate voltage no longer influences the drain current. Good agreement is found between the simulated and measured data for curves (1) to (3). However, measured curve 4 has a positive slope, while the simulated curve (4) has a negative slope, which is due to the inclusion of self-heating. The reason for the positive slope in the measured curve is not that obvious. One would expect the current to have saturated due to pinch-off of the drift

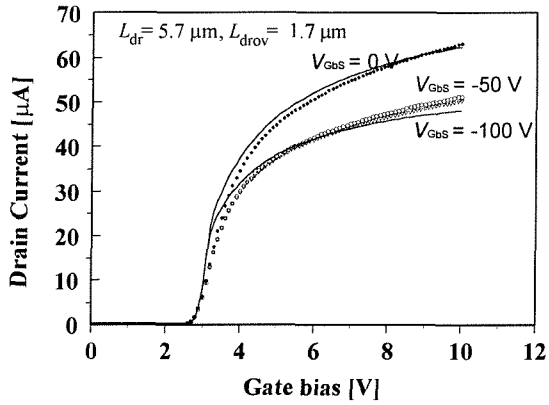

Figure 4.17: MV LDMOS with $L_{\mathrm{drov}} = 1.7\ \mu\mathrm{m}$ and $L_{\mathrm{dr}} = 5.8\ \mu\mathrm{m}$; measured (markers) and simulated (full line) current vs. V_{GfS} for $V_{\mathrm{DS}} = 0.1$ V and $V_{\mathrm{GbS}} = 0$ V, -50 V, -100 V.

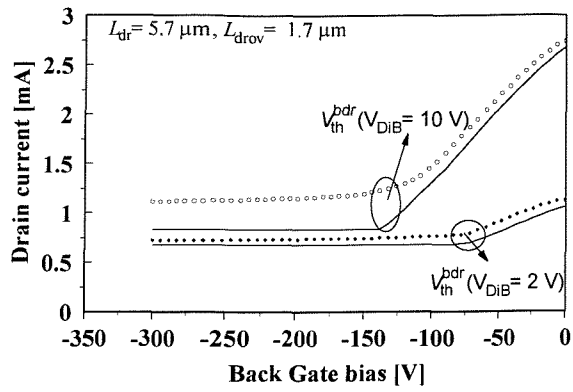

Figure 4.18: MV LDMOS with $L_{\mathrm{drov}} = 1.7\ \mu\mathrm{m}$ and $L_{\mathrm{dr}} = 5.8\ \mu\mathrm{m}$; measured (markers) and simulated (full line) current vs. V_{GbS}; $V_{\mathrm{GfS}} = 10$ V; $V_{\mathrm{DS}} = 2$ V and $V_{\mathrm{DS}} = 10$ V.

region, so that the current decreases with increasing V_{DS} due to self-heating. It is probable that 2-D effects in the drift region change the field distribution when V_{DS} is increased, allowing a higher drain current. Another explanation could be an enhanced channel length modulation effect with increasing back gate bias. However, these hypotheses would need to be investigated with a device simulator to be more certain.

Fig. 4.17 shows the influence of a negative back gate on the linear characteristic. As explained in Sec. 4.5.1, the simulated current just above the threshold overestimates the real current, but the decrease in current due to a negative bach gate bias shows good agreement with the measurements. In Fig. 4.18 we have plotted the current vs. the back gate bias for a fixed front gate bias and two different drain biases. As explained in the previous paragraph, the simulated saturation current is too low for very negative back gate biases. The plot illustrates nicely the decrease in current with increasingly negative back gate bias until the drain voltage dependent back gate threshold voltage of the drift region is reached ($V_{\mathrm{th}}^{\mathrm{bdr}}$), at which point the current stays constant.

4.6 Summary

In this chapter, the complete SOI LDMOS DC model was set out. Expressions for the current under the thin gate oxide and under the field oxide were carefully derived, keeping the model approach as physical as possible. The assumptions made were considered critically and verified where necessary.

First an expression for the current under the thin gate oxide was developed, describing the current in terms of the surface potentials, whilst taking into account the lateral doping gradient and the overlap of the gate over the N^- drift region. Vertical mobility degradation

and velocity saturation effects were included in a robust and continuous way. Furthermore, we accounted for CLM and DIBL.

Next, an expression for the current under the field oxide was developed. The impact on the current of the thickness of the depletion layer at the buried oxide was studied rigorously, leading to a good prediction of the unique high-side behaviour.

The model simulations match the measured characteristics well for a wide range of geometries, with self-heating effects being accounted for.

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Chapter 5

Compact Charge Model

5.1 Introduction

In the previous chapter we have treated the LDMOS transistor under the assumption that all terminal voltages are constant. However a device is usually employed in circuits with time-varying terminal voltages. This dynamic regime causes the charges within an LDMOS to vary, and these charges must be supplied from outside by extra currents flowing into or out of the transistor. The DC currents flowing in the device cannot be used to predict such extra currents.

The subject of this chapter is the evaluation of the charges associated with all the separate terminals. Using these charge expressions, we will be able to deal with the large signal and small signal dynamic operation of the LDMOS. The effective capacitances which result are non-reciprocal and our model strategy guarantees the conservation of charge [1].

We will concentrate on the intrinsic part, which is mainly responsible for transistor action. Just as for the DC case, the intrinsic part will include the overlap of the thin gate oxide over the drift region, and will account for the lateral doping gradient. In the last section the different overlap capacitances (the extrinsic aspect of the LDMOS charge model which is responsible for the parasitic effects) are discussed.

In the following, quasi-static operation is assumed, which means that the variation of the terminal voltages is sufficiently slow so that the charges can instantaneously readjust to the varying terminal voltages. At very high frequencies "transmission line effects" have to be taken into account, and the device then behaves in a non-quasi-static way. For most applications LDMOS devices are not used at such high frequencies, and the non-quasi-static effects exceed the scope of this work. If non-quasi-static effects have to be taken into account, it is always possible, just as for a standard MOSFET, to use the Elmore equivalent circuit to model channel charge build up in the channel [2].

Motorola's RF LDMOS model [3,4] uses hyperbolic trigonometric empirical functions to describe the capacitances, but we are looking for a physical model. The more physical LDMOS models found in the literature account for the lateral doping gradient by using a couple of MOSFET models (in practice 2 or 3) with decreasing threshold voltages, placed

in series [5, 6]. This not only increases the computation time, but also introduces more parameters, which can lead to non-physical situations; the short channel length and DIBL parameters will be different for the 2 or 3 MOSFET transistors and the extraction of these parameters is not straightforward. In [7, 8] a JFET-like model is used to describe the influence of the gate over the drift region, which means an extra internal node, and hence slower convergence.

5.2 Overview of the Charges in the LV LDMOS

Let us consider the charges in the SOI LDMOS for different bias conditions. In Fig. 5.1 the LDMOS is plotted with source, drain and the P^+ body well omitted, to emphasize that only the intrinsic part is considered.

5.2.1 Charges in the OFF-state

Figs. 5.1 (a), (c) and (e) show the charge distribution when the device is in the subthreshold regime ($V_{\mathrm{FB}}^{\mathrm{fdr}} < V_{\mathrm{GfB}} < V_{\mathrm{th0}}$); when the drain voltage is zero, the surface under the front gate in the drift region is in accumulation. As explained in Sec. 2.2.3, the doping concentration in the P-body has a maximum near the source decreasing towards the drain, and hence the threshold voltage for inversion at the source end (V_{th0}) is higher than at the the drain end (V_{thL}). The ATLAS simulation results from Sec. 2.2.3 showed that, for a gate voltage higher than V_{thL}, an inversion layer is present, growing from the P-N junction towards the source as V_{GfB} is increased (case (a)). We define L_{min} as the y position for which inversion in the channel starts, i.e. the y value for which the expression for the strong inversion surface potential equals the subthreshold expression: $\psi_{\mathrm{si}}(y) = \psi_{\mathrm{ss}}(y)$. Below threshold the inversion layer does not reach the source junction, and the channel charge is only dependent on the gate and the drain voltage. Hence, since no conducting path is present between the source and the channel, the intrinsic gate-source capacitance and the charge attributed to the source are negligible.

Increasing the drain voltage slightly reduces the inversion charge ($L_{\mathrm{min}} \gg L_{\mathrm{eff}}$), until the inversion layer disappears completely (case (c)). But as long as $V_{\mathrm{GfDi}} > V_{\mathrm{FB}}^{\mathrm{fdr}}$, the accumulation layer in the drift region stays present.

When the gate-internal drain voltage (V_{GfDi}) is decreased below flat band, the accumulated electrons are driven away from the surface and a depletion layer starts to grow under the front oxide in the drift region (case (e)).

In the unusual bias situation where the gate voltage is made negative, a hole layer can be present at the surface. When the gate-body bias is decreased below flat band, holes accumulate in the P-body at the front oxide interface (case (g)). A gate bias below the negative threshold voltage of the drift region ($V_{\mathrm{th0}}^{\mathrm{fdr}}$) causes surface inversion in the drift region (case (h)).

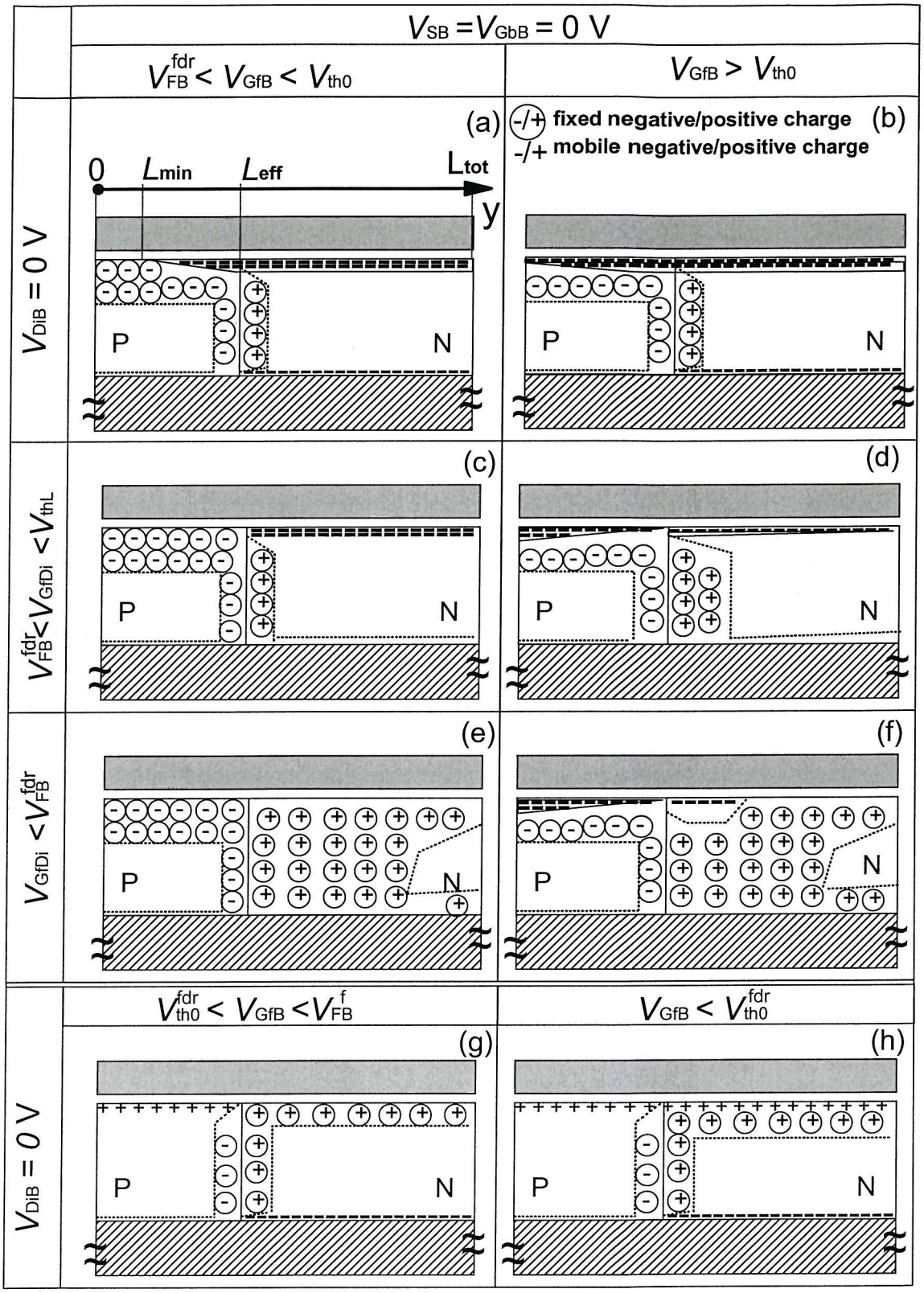


Figure 5.1: Intrinsic charges in the SOI LDMOS for different bias conditions:
(a) $V_{GfB} < V_{th0}$, $V_{DiB} = 0$ V; (b) $V_{GfB} > V_{th0}$, $V_{DiB} = 0$ V;
(c) $V_{GfB} < V_{th0}$, $V_{FB}^{fdr} < V_{GfDi} < V_{th0}$; (d) $V_{GfB} > V_{th0}$, $V_{FB}^{fdr} < V_{GfDi} < V_{thL}$;
(e) $V_{GfB} < V_{th0}$, $V_{GfDi} < V_{FB}^{fdr}$; (f) $V_{GfB} > V_{th0}$, $V_{GfDi} > V_{FB}^{fdr}$;
(g) $V_{th0}^{fdr} < V_{GfB} < V_{FB}^{f}$; (h) $V_{th0}^{fdr} > V_{GfB}$.

5.2.2 Charges in the ON-state

In Figs. 5.1 (b), (d) and (f) the strong inversion case is considered. Now a conducting path exists between the drain and the source ($V_{\mathrm{GfB}} > V_{\mathrm{th0}}$). When the drain voltage is small (case (b)), the channel charge consists of inverted and accumulated electrons.

Increasing the drain voltage, increases the surface potential at the P-N^- junction (ψ_{sL}) until the inversion layer pinches at $y = L_{\mathrm{eff}}$ (case (d)).

When the drain voltage exceeds $V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{fdr}}$ the accumulated electrons are driven away from the drain end of the drift region, leaving the surface depleted. This layer grows towards the P-N^- junction depletion layer as the drain voltage is further increased (case (f)).

5.2.3 Charges at the Back Oxide Interface

Let us consider the bias situation where $V_{\mathrm{GbB}} = 0$ V and V_{DiB} is positive. Since $V_{\mathrm{GbB}} > V_{\mathrm{FB}}^{\mathrm{b}}$, a depletion layer is present at the back oxide interface in the P-region. Assuming a N^+ substrate, $-V_{\mathrm{GbDi}} = 0$ V is smaller than the flat band voltage between the drift region and the back gate ($-V_{\mathrm{FB}}^{\mathrm{bdr}}$), and hence the back oxide in the drift region is accumulated (cases (a), (b), (g) and (h)). For higher drain voltages (cases (c), (d), (e) and (f)) a depletion layer is present at the back oxide.

5.2.4 A Fluid Dynamical Analogue for the Channel Charge

Better intuition about the storage and motion of the inversion and accumulation charges in the channel can be obtained by considering the analogous case in fluid dynamics, which is illustrated in Fig. 5.2. The gate voltage is represented as the height of the piston and the drain and source voltage are the water levels of the water reservoirs respectively left and right of the piston. For a normal MOSFET the piston would have a rectangular shape [9], but because the threshold for inversion ($y < L_{\mathrm{eff}}$) varies with y due to the doping gradient, the piston has the shape used in Fig. 5.2.

When the gate voltage is lower than the threshold voltage (cases (a), (c), (e)), no water flows from the drain to the source. The water in the channel (the region above the piston) can only be provided by the drain reservoir when the piston height or drain level is slightly altered, which in electrical terms means a non-zero drain-gate channel capacitance. The source-gate channel capacitance is zero as no charge/water flows in or out of the source reservoir.

When the piston is lowered below the threshold (cases (b), (d) and (f)), the water can flow from drain to source. For almost equal drain and source levels the water in the channel will be provided by both reservoirs when the piston height is lowered, which means in electrical terms that a change in the gate voltage causes a change in both the charges attributed to the drain and to the source. In other words, both the drain-gate and source-gate capacitances are non-zero.

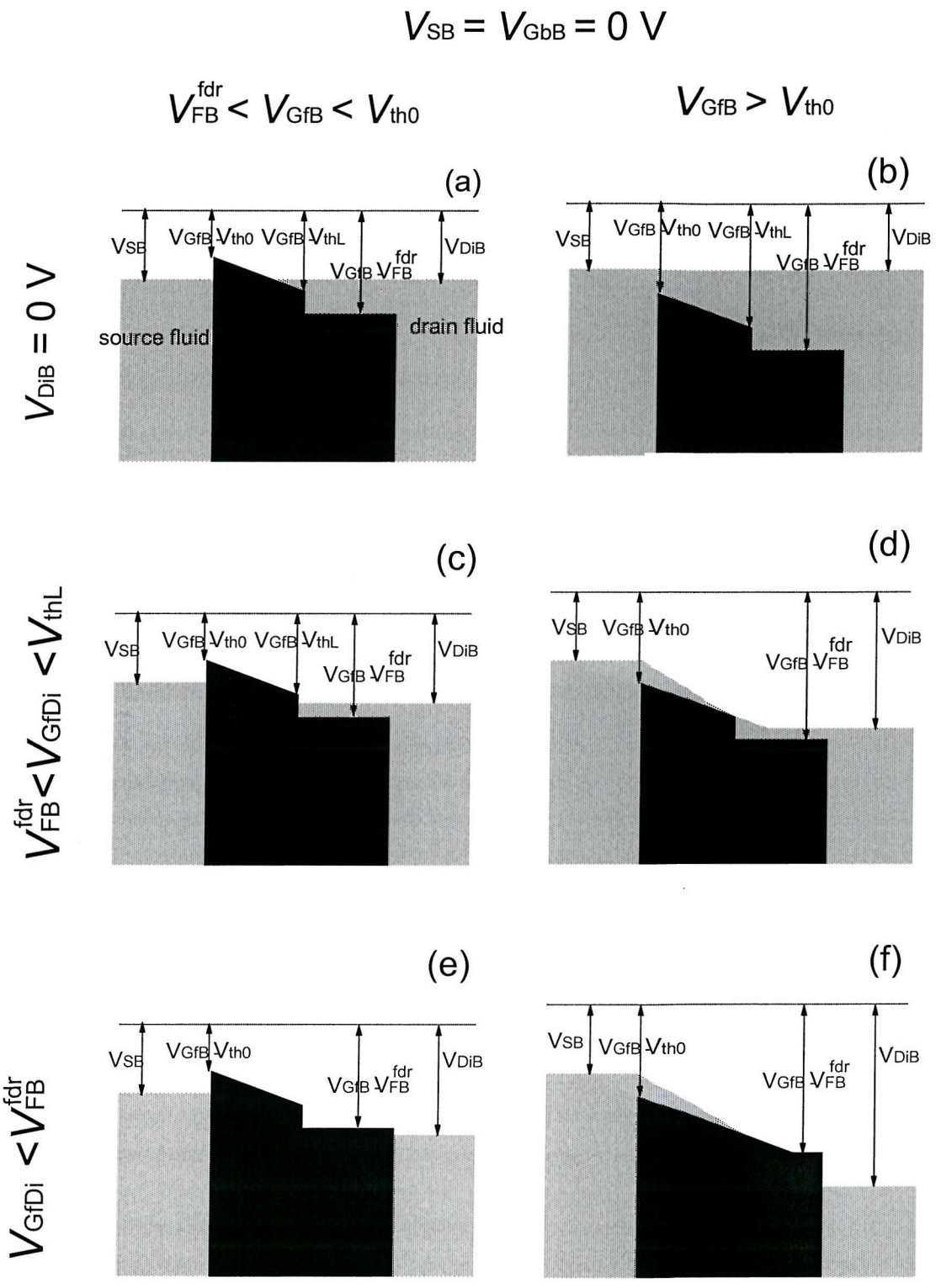


Figure 5.2: Fluid dynamical analogue for illustration of the storage and motion of the channel charge in the SOI LDMOS.

The quasi-static assumption in MOS theory is equivalent to the assumption of a slowly moving piston in the fluid dynamical case.

5.3 Nodal Charges Originating from the Channel Charge

The total channel charge (Q_{CH}) is the sum of the total inversion layer charge (Q_{CHinv}) and the total accumulation layer charge (Q_{CHacc}), and can be obtained as

$$Q_{\mathrm{CH}} = Q_{\mathrm{CHinv}} + Q_{\mathrm{CHacc}} = W \cdot \left(\int_{L_{\mathrm{min}}}^{L_{\mathrm{eff}}} q_{\mathrm{cinv}} \cdot dy + \int_{L_{\mathrm{eff}}}^{L_{\mathrm{tot}}} q_{\mathrm{cacc}} \cdot dy \right) \tag{5.1}$$

where q_{cinv} and q_{cacc} represent respectively the inversion charge density and the accumulation charge density in the channel and $L_{\mathrm{tot}} = L_{\mathrm{eff}} + L_{\mathrm{drov}}$ (cf. Fig. 5.1 (a)). To perform this integration expressions for q_{cinv} and q_{cacc} as a function of position y are needed; they will be derived in Sec. 5.3.4. An expression for L_{min} will be derived in Sec. 5.3.3.

When the total charge present in the channel changes, this extra charge can only leave or enter the channel via the source or drain, which means

$$\frac{dQ_{\mathrm{CH}}}{dt} = i_{\mathrm{di}}(t) + i_{\mathrm{s}}(t) \tag{5.2}$$

$$= \frac{dQ_{\mathrm{Di}}}{dt} + \frac{dQ_{\mathrm{S}}}{dt} \tag{5.3}$$

where $i_{\mathrm{di}}(t)$ and $i_{\mathrm{s}}(t)$ are respectively the drain and source "charging" currents. Q_{Di} and Q_{S} are two fictitious charges associated with the source and drain so that

$$Q_{\mathrm{CH}} = Q_{\mathrm{Di}} + Q_{\mathrm{S}} \, . \tag{5.4}$$

Various approaches can be found in the literature to evaluate these two fictitious charges [1,10,11], but it is only the Ward and Dutton partitioning scheme [12], which is rigorously shown to be correct for a simple MOSFET with a constant channel doping concentration. However, for the LDMOS, which has a varying doping profile as a function of position along the channel, this partitioning scheme is no longer strictly valid. In the next section the derivation of the Ward and Dutton scheme is repeated and we will explain where the derivation is not correct for the LDMOS. In Sec. 5.3.2 we present a modified partitioning scheme for the LDMOS.

5.3.1 The Ward and Dutton Partitioning Scheme

In a standard MOSFET the Ward and Dutton partitioning scheme defines the channel charges associated with the source and the drain as [12] :

$$Q_{\mathrm{Dwd}}^{\mathrm{MOS}} = W \int_0^L \frac{y}{L} \, q_{\mathrm{c}} \cdot dy \tag{5.5}$$

$$Q_{\text{Swd}}^{\text{MOS}} = W \int_0^L \left(1 - \frac{y}{L}\right) q_c \cdot dy \tag{5.6}$$

where the subscript "wd" indicates that the Ward and Dutton partitioning scheme is used, and the superscript "MOS" refers to a standard MOSFET. Using this scheme in the LDMOS gives:

$$Q_{\text{Diwd}} = W \int_{L_{\text{min}}}^{L_{\text{tot}}} \frac{y}{L_{\text{tot}} - L_{\text{min}}} q_c \cdot dy \tag{5.7}$$

$$Q_{\text{Swd}} = W \int_{L_{\text{min}}}^{L_{\text{tot}}} \left(1 - \frac{y}{L_{\text{tot}} - L_{\text{min}}}\right) q_c \cdot dy \tag{5.8}$$

where q_c is the charge density in the channel, which for the LDMOS is the inversion charge density (q_{cinv}) for $y < L_{\text{eff}}$ and the accumulation charge density (q_{cacc}) for $L_{\text{eff}} < y < L_{\text{eff}} + L_{\text{drov}}$.

It is easy to observe that Eq. 5.8 will lead to a non-zero source charge when the gate voltage is lower than the threshold voltage but higher than $V_{\text{DiB}} + V_{\text{FB}}^{\text{fdr}}$. This cannot be correct since, below the threshold voltage, there is no conducting path between the source and the inversion channel charge and hence Q_S should be zero as we explained in the previous section. So why is the Ward and Dutton partitioning scheme not valid in the case of the LDMOS?

Let us consider first the Ward and Dutton partitioning scheme in case of a simple MOSFET with a constant doping profile as a function of the position y along the channel [12]. Assuming that current transport is parallel to the surface, the current transport equation is given by

$$I(y,t) = q\, W\, \mu\, n(y,t)\, \frac{\partial \psi_s(y,t)}{\partial y} \tag{5.9}$$

with μ the mobility in the channel, $n(y,t)$ the mobile carrier density and $\psi_s(y,t)$ the surface potential at the silicon surface in terms of position y and time t. Neglecting recombination, the current continuity equation is given by

$$\frac{\partial n(y,t)}{\partial t} = -\frac{1}{q\, W} \frac{\partial I(y,t)}{\partial y} \,. \tag{5.10}$$

Integrating this equation, and substituting $I(y,t)$ by Eq. 5.9 yields

$$q\, W \int_0^y \frac{\partial n(y',t)}{\partial t} dy' = -q\, W\, \mu\, n(y,t)\, \frac{\partial \psi_s(y,t)}{\partial y} + I(0,t) \,. \tag{5.11}$$

Integrating again from source to drain and rearranging terms results in

$$I(0,t) = q\, \frac{W}{L} \int_0^L \int_0^y \frac{\partial n(y',t)}{\partial t} \cdot dy' \cdot dy + q\, \mu\, \frac{W}{L} \int_0^L n(y,t) \frac{\partial \psi_s(y,t)}{\partial y} \cdot dy \,. \tag{5.12}$$

In the case of a MOSFET with a constant doping concentration along the channel, we can write $n(y,t) = n(\psi_s(y,t), V_{\text{GfB}}(t)) = n(\psi_s, V_{\text{GfB}})$. This cannot be done for the

LDMOS, because, for the same surface potential and the same gate voltage, the channel charge will still be dependent on the doping concentration, which varies with position y. For a MOSFET Eq. 5.12 can be rewritten as

$$I(0,t) = q\,\frac{W}{L}\int_0^L\int_0^y \frac{\partial n(y',t)}{\partial t}\cdot dy'\cdot dy + q\,\mu\,\frac{W}{L}\int_{\psi_S(t)}^{\psi_D(t)} n(\psi_s, V_{GfB})\cdot d\psi_s\ . \tag{5.13}$$

The second term is recognized as the steady-state current, which will be referred to as I_0, and the first term can be identified with $\frac{dQ_{Swd}^{MOS}}{dt}$. By developing a little further the first term via integration by parts, one obtains Eq. 5.8:

$$\begin{aligned} Q_{Swd}^{MOS} &= q\,\frac{W}{L}\int_0^L\int_0^y n(y',t)\cdot dy'\cdot dy & (5.14)\\ &= q\,W\int_0^L (1-\frac{y}{L})\,n(y,t)\cdot dy\ . & (5.15)\end{aligned}$$

For the LDMOS, this simplification of the integral to the steady state current cannot be done, because

$$\int_0^L n(y,\psi_s,t)\,\frac{\partial\psi_s(y,t)}{\partial y}\cdot dy \neq \int_{\psi_S(t)}^{\psi_D(t)} n(\psi_s, V_{GfB})\cdot d\psi_s\ . \tag{5.16}$$

This can be understood in a more physical way; let us consider the case of a gate voltage lower than the threshold voltage. It will be proven that

$$\int_0^{L_{tot}} I(y,t) = \int_0^{L_{tot}} n(y,\psi_s,t)\frac{\partial\psi_s(y,t)}{\partial y}\cdot dy \tag{5.17}$$

is not the steady-state current. Imagine a small decrease in V_{DiB} at $t = t_0$; this causes an instant decrease in $\psi_s(L_{tot})$, the surface potential at the drain end, because the charges can be instantly removed by the drain N^+ region (assuming quasi-static operation). However, the surface potential at L_{min}, the starting point of inversion, cannot decrease instantly because as long as the inversion layer does not reach the source end, this point is isolated from the source and all the extra charge has to come from the drain. At $t = t_0$ we have $\frac{\partial\psi_s(y,t_0)}{\partial y}$ which has a non-zero value in the accumulation-inversion channel and drain current will flow until an equilibrium is reached. So at $t = t_0$, we have

$$\int_0^{L_{tot}} I(y,t)\cdot dy \cong \int_{L_{min}}^{L_{tot}} I(y,t)\cdot dy < 0\ . \tag{5.18}$$

This is not the steady-state current, because the DC current is the very small positive subthreshold current.

When the LDMOS is operated above threshold,

$$n(y,t) = n(\psi_s(y,t), V_{GfB}(t)) \cong n(\psi_s, V_{GfB}) \tag{5.19}$$

is a good approximation (cf. the approximation of the body factor in terms of ψ_s in

Sec. 4.2.1) and the Ward and Dutton partitioning scheme is expected to give valid results for Q_{Di} and Q_{S}.

5.3.2 The Modified Ward and Dutton Partitioning Scheme for LDMOST

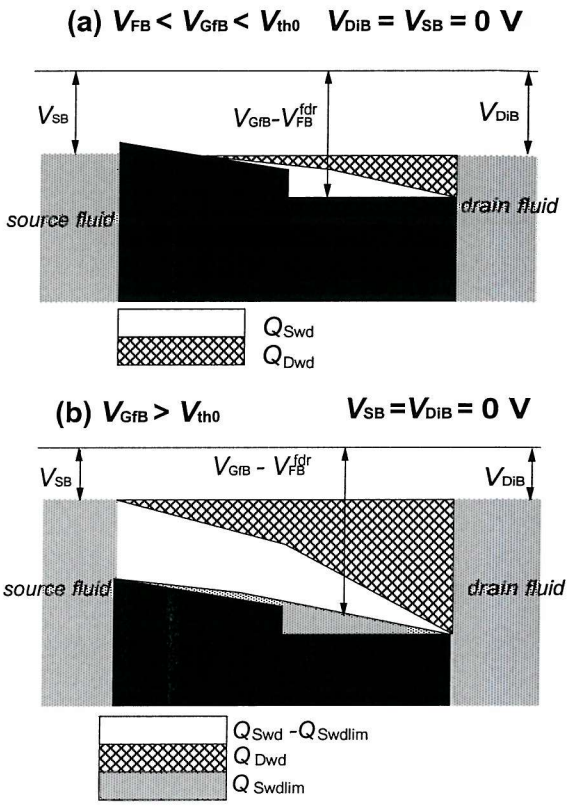


Figure 5.3: Fluid dynamical analogy of the partitioning of the channel charge: (a) $V_{\mathrm{GfB}} < V_{\mathrm{th0}}$, (b) $V_{\mathrm{GfB}} > V_{\mathrm{th0}}$.

To obtain a good model valid from sub-threshold into inversion, the Ward and Dutton scheme has to be slightly modified.

Below threshold, we want $Q_{\mathrm{Di}} = Q_{\mathrm{CH}}$ and $Q_{\mathrm{S}} = 0$, while the Ward and Dutton scheme predicts a partitioning as illustrated in Fig. 5.3 (a). Let us now simply add the source charge found from Eq. 5.8, when $V_{\mathrm{GfB}} < V_{\mathrm{th0}}$, to the drain charge predicted by Ward and Dutton. The same value has to be subtracted from the source charge to maintain $Q_{\mathrm{Di}} + Q_{\mathrm{S}} = Q_{\mathrm{CH}}$.

Following the reasoning above, the equations for the internal drain and the source charge become

$$Q_{\mathrm{Di}} = Q_{\mathrm{Diwd}} + Q_{\mathrm{Swd}}(V_{\mathrm{GfBlim}}) \tag{5.20}$$

$$Q_{\mathrm{S}} = Q_{\mathrm{Swd}} - Q_{\mathrm{Swd}}(V_{\mathrm{GfBlim}}) \; . \tag{5.21}$$

Obviously, once the threshold is reached, the source can also provide electrons to the

channel and Q_S has to increase. This result can be obtained using the following definition for V_{GfBlim} :

$$Q_{Swdlim} = Q_{Swd}(V_{GfBlim}) = \begin{cases} Q_{Swd}(V_{GfB}) & \text{for } V_{GfB} < V_{th0} \\ Q_{Swd}(V_{th0}) & \text{for } V_{GfB} > V_{th0} \end{cases} . \tag{5.22}$$

In Sec. 5.3.5 it will be explained how V_{GfBlim} is implemented in the charge expressions in a continuous way.

In Fig. 5.3 (b) the charge partitioning above threshold is illustrated: the extra charge added to the drain and subtracted from the source charge (Q_{Swdlim}) is now a very small proportion of the total channel charge, and the Ward and Dutton partitioning scheme gives a good approximation for Q_S and Q_{Di}.

5.3.3 Calculation of L_{min}

If $V_{GfB} < V_{th0}$ then we have to calculate the value of L_{min}, the position for which the channel goes into inversion. Two different situations have to be considered: firstly, inversion can start at the drain end of the channel when the gate bias is increased. This is typically the case for $V_{DB} \cong V_{SB}$. Alternatively, when $V_{DB} \gg V_{SB}$ inversion will start at the source end when the source threshold voltage (V_{th0}) is reached.

Let us now consider the first situation and calculate L_{minL}, the position for which the channel becomes inverted under the assumption that inversion starts at the drain end. For $y = L_{minL}$, the expression for the subthreshold surface potential has to equal the value of the inversion surface potential:

$$\psi_{ss}(L_{minL}) = \psi_{si}(L_{minL}) \tag{5.23}$$

where

$$\psi_{ss}(L_{minL}) \cong \left\{ -\frac{\gamma_0}{2} \exp\left(-\frac{k_{N_A} L_{minL}}{2 L_{eff}}\right) + \sqrt{V_{gy} + \frac{\gamma_0^2}{4} \exp\left(-\frac{k_{N_A} L_{minL}}{L_{eff}}\right)} \right\}^2 \tag{5.24}$$

$$\psi_{si}(L_{minL}) \cong \psi_{siLinv} \tag{5.25}$$

with ψ_{siLinv} the inversion surface potential at $x = L_{eff}^-$, where L_{eff}^- is used to indicate the left side of the P-N^- junction. In the ON-state ψ_{siLinv} is equal to ψ_{sLacc}, the surface potential at $x = L_{eff}^+$, but, in the OFF-state, these quantities are different (see next section). To avoid a negative root term in Eq. 5.24, V_{gy} is defined as

$$V_{gy} = 2\,\phi_t \ln\Big(1 + \exp(\frac{V_g}{2\,\phi_t})\Big) , \tag{5.26}$$

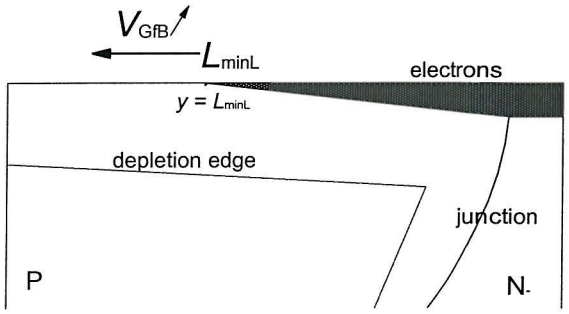
and limits the quantity V_g to positive values. In the expression for the subthreshold surface potential at $y = L_{minL}$ (Eq. 5.24), the approximation consists of using $V_g = V_{GfB} - V_{FB}^f$, where V_{FB}^f is the flatband voltage at $y = 0$. The flatband voltage at $y = L_{minL}$ is in fact

$k_{N_A}\phi_t\frac{L_{minL}}{L_{eff}}$ higher than at $y = 0$, but this value is of the order of ϕ_t and can be neglected. The quantity $\psi_{si}(L_{minL})$ is in theory $k_{N_A}\phi_t\frac{L-L_{minL}}{L_{eff}}$ higher than ψ_{siLinv}, but again this value is of the order of ϕ_t and can be neglected.

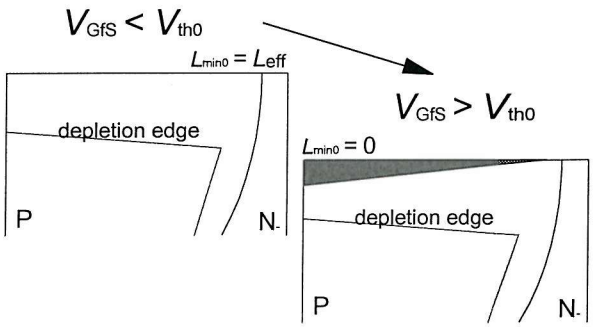
Solving Eq. 5.23 for L_{minL} leads to

$$L_{minL} = \frac{2\,L_{eff}}{k_{N_A}} \ln\left(\frac{\gamma_0\sqrt{\psi_{siLinv}}}{V_{gy} - \psi_{siLinv}}\right) . \tag{5.27}$$

The denominator $V_{gy} - \psi_{siLinv}$ has to be limited in between $\gamma_0\sqrt{\psi_{siLinv}}$ and $\gamma_L\sqrt{\psi_{siLinv}}$. This ensures that L_{minL} stays in between 0 and L_{eff}, reaching the lower bound when the source threshold voltage is reached, and the upper bound when the drain end is no longer in inversion.



(a) Movement of L_{minL} when $V_{DiB} = V_{SB}$



(b) Movement of L_{min0} when $V_{DiB} >> V_{SB}$

Figure 5.4: Movement of L_{min} with increasing gate bias: (a) $V_{DiB} = V_{SB}$, (b) $V_{DiB} >>> V_{SB}$

However, the theory developed in the above paragraphs will only be correct if inversion starts at the drain end of the channel, which is only the case when the drain-body voltage is not much higher than the source-body voltage (Fig. 5.4(a)).

Using Eq. 5.27, one obtains $L_{minL} = L_{eff}$ for a high enough drain voltage, independent of the gate-source voltage. This is not correct, since once the gate-source voltage reaches V_{th0}, an inversion layer is present over the whole length of the channel, and L_{min} should then be 0 (see the "$V_{GfS} > V_{th0}$" case in Fig. 5.4 (b)).

Let us now consider the case when $V_{\mathrm{DiB}} \gg V_{\mathrm{SB}}$, and inversion starts at the source end of the channel. This is not the same gradual process as is the case when inversion starts at the drain end and gradually moves towards the source as V_{GfS} is increased; now, on the contrary, when V_{th0} is reached, an inversion layer will appear over the whole length of the channel. This fast transition is illustrated in Fig. 5.4 (b). This change in L_{min0} between 0 and L_{eff} around the threshold can be achieved in a smooth way using:

$$L_{\mathrm{min0}} = \frac{20\ L_{\mathrm{eff}}}{k_{\mathrm{N_A}}} \ln\left(\frac{\gamma_0\ \exp\left(\frac{k_{\mathrm{N_A}}}{20}\right)\sqrt{\psi_{\mathrm{si0}}}}{V_{\mathrm{gy}} - \psi_{\mathrm{si0}}}\right) \tag{5.28}$$

where the inversion surface potential at the source, ψ_{si0}, is used instead of ψ_{siLmin}. $V_{\mathrm{gy}} - \psi_{\mathrm{si0}}$ has to be limited in between $\gamma_0\sqrt{\psi_{\mathrm{si0}}}$ and $\gamma_0 \exp\left(\frac{k_{\mathrm{N_A}}}{20}\right)\sqrt{\psi_{\mathrm{si0}}}$, to keep L_{min0} between 0 and L_{eff}.

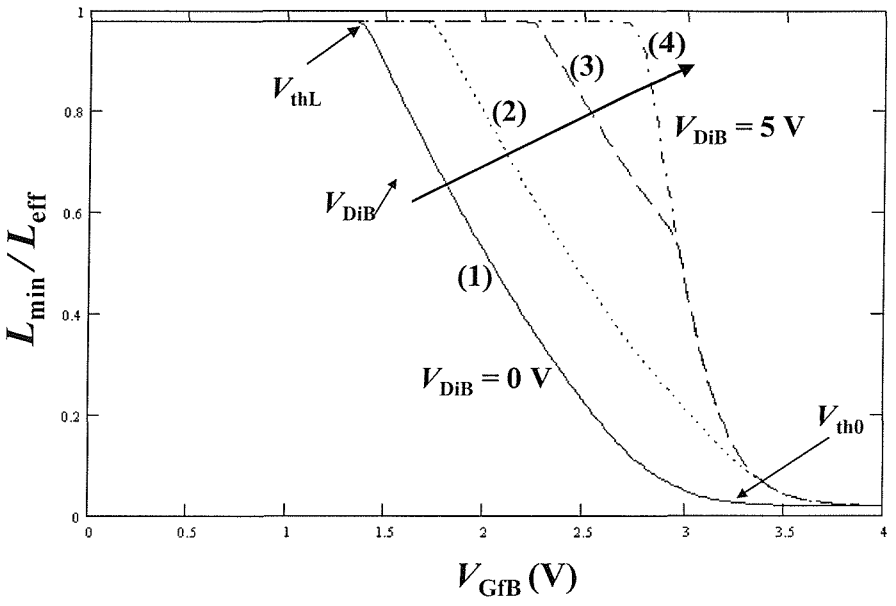


Figure 5.5: L_{min} vs. V_{GfB} for V_{DiB} =0 V, 0.2 V, 0.5 V, 5V and V_{SB} =0 V.

The choice of this empirical function for L_{min0} was made by analogy to L_{minL}; the denominator $V_{\mathrm{gy}} - \psi_{\mathrm{siLinv}}$ in Eq. 5.27 can vary from $\gamma_{\mathrm{L}}\sqrt{\psi_{\mathrm{siLinv}}}$ (when the drain end is on the edge of inversion, $L_{\mathrm{minL}} = L_{\mathrm{eff}}$) to $\gamma_0\sqrt{\psi_{\mathrm{siLinv}}}$ (when the inversion layer has extended all the way to the source, $L_{\mathrm{minL}} = 0$). The ratio of these two quatities is a measure for the slope of L_{minL} when plotted against V_{GfB} in the transition region. This ratio only depends on the doping gradient, and is given by $\exp(k_{\mathrm{N_A}}/2)$. Similarly $V_{\mathrm{gy}} - \psi_{\mathrm{si0}}$ can vary from $\gamma_0\sqrt{\psi_{\mathrm{si0}}}$ (when the whole channel is on the edge of inversion, $L_{\mathrm{min0}} = L_{\mathrm{eff}}$) to $\gamma_0 \exp(k_{\mathrm{N_A}}/20)\sqrt{\psi_{\mathrm{si0}}}$ (when the inversion layer is established, $L_{\mathrm{min0}} = 0$). The ratio of the two quanteties being $\exp(k_{\mathrm{N_A}}/20)$. This ratio was chosen to be ten times smaller on a log scale than for L_{minL} to ensure the fast transition required, and, at the same time,

provide a smooth conversion from L_{minL} to L_{min0}, when taking the minimum of the two (see next paragraph).

The final expression for L_{min} is given by the smooth minimum of L_{minL} and L_{min0}, and is illustrated in Fig. 5.5. For very low V_{DiB} we have $L_{\mathrm{min}} = L_{\mathrm{minL}}$ (see curves (1) and (2) in Fig. 5.5). For very high V_{DiB}, L_{min} is given by L_{min0} (see curve (4) in Fig. 5.5). For intermediate values of V_{DiB}, L_{min} converts from L_{minL} to L_{min0} as V_{GfB} is increased (see curve (3) in Fig. 5.5). The whole set of continuous smoothing functions and factors can be found in Sec. C.9.1 in App. C. We will comment on the suitability of certain smoothing factors, when comparing measurements with simulations (see Sec. 5.12.2). Some numerical issues will be discussed as well in Chapter 7.

5.3.4 The Charge Distribution in the Channel

To obtain the charge distribution in the channel region as a function of position y, an approach is followed which is similar to the ones used in most non-reciprocal standard MOSFET models [13, 14].

Neglecting the diffusion component in the channel current and assuming that all the current flows in the accumulation region present in the drift region, the current in the channel can be written as

$$I_{\mathrm{CH}}(y) = -\mu\, W\, q_{\mathrm{c}}(y) \frac{d\psi_{\mathrm{s}}}{dy} \,. \tag{5.29}$$

This is integrated from L_{min} to L_{eff}, and from L_{eff} to L_{tot}:

$$I_{\mathrm{CH}} = -\mu \frac{W}{L_{\mathrm{eff}} - L_{\mathrm{min}}} \int_{\psi_{\mathrm{sLmin}}}^{\psi_{\mathrm{sL}}} q_{\mathrm{c}}(\psi_{\mathrm{s}}) \cdot d\psi_{\mathrm{s}} \tag{5.30}$$

$$I_{\mathrm{CH}} = -\mu \frac{W}{L_{\mathrm{drov}}} \int_{\psi_{\mathrm{sLacc}}}^{\psi_{\mathrm{sdi}}} q_{\mathrm{c}}(\psi_{\mathrm{s}}) \cdot d\psi_{\mathrm{s}} \,. \tag{5.31}$$

Changing variables, and assuming that the body factor in the expression for q_{c} (see Eq. 4.6) is constant and given by $\frac{\gamma_0+\gamma_{\mathrm{L}}}{2}$, leads to the following result

$$I_{\mathrm{CH}} = -\mu \frac{W}{C_{\mathrm{of}} \cdot (L_{\mathrm{eff}} - L_{\mathrm{min}})} \left(\frac{1}{\alpha} \int_{q_{\mathrm{L_{min}}}}^{q_{\mathrm{L}}} q_{\mathrm{c}} \cdot dq_{\mathrm{c}} \right) \tag{5.32}$$

$$I_{\mathrm{CH}} = -\mu \frac{W}{C_{\mathrm{of}} \cdot (L_{\mathrm{drov}})} \left(\int_{q_{\mathrm{Lacc}}}^{q_{\mathrm{di}}} q_{\mathrm{c}} \cdot dq_{\mathrm{c}} \right) \tag{5.33}$$

where $\alpha = \eta_{\mathrm{s}} + \frac{\gamma_0+\gamma_{\mathrm{L}}}{2}$, $q_{\mathrm{L_{min}}}$ is the channel charge at $y = L_{\mathrm{min}}$, q_{L} the channel charge density in the inversion layer just before the P-N junction, q_{Lacc} the channel charge density in the accumulation layer just after the P-N junction, and q_{di} the channel charge density at the internal drain (the end of the drift region under the thin front gate). They are given by

$$q_{\mathrm{L_{min}}} = C_{\mathrm{of}} \cdot \left(V_{\mathrm{gy}} - \eta_{\mathrm{s}}\, \psi_{\mathrm{sLmin}} - \gamma_{\mathrm{L_{min}}} \sqrt{\psi_{\mathrm{sLmin}}} \right) \tag{5.34}$$

$$q_{\mathrm{L}} = C_{\mathrm{of}} \cdot \left(V_{\mathrm{gy}} - \eta_{\mathrm{s}}\, \psi_{\mathrm{sL}} - \gamma_{\mathrm{L}} \sqrt{\psi_{\mathrm{sL}}} \right) \tag{5.35}$$

$$q_{\mathrm{Lacc}} = C_{\mathrm{of}} \cdot \left(V_{\mathrm{GfB}} - \psi_{\mathrm{sLacc}} - V_{\mathrm{FB}}^{\mathrm{fdr}}\right) \tag{5.36}$$

$$q_{\mathrm{di}} = C_{\mathrm{of}} \cdot \left(V_{\mathrm{GfB}} - \psi_{\mathrm{sdi}} - V_{\mathrm{FB}}^{\mathrm{fdr}}\right). \tag{5.37}$$

The last two equations are limited to be positive in a smooth way (see Sec. C.9.1 in App. C). We notice that $q_{\mathrm{L_{min}}}$ is by definition zero below the threshold, and becomes q_0 once the threshold voltage is reached. But below threshold q_0 is zero as well, so $q_{L_{\mathrm{min}}}$ can be replaced with

$$q_0 = C_{\mathrm{of}} \cdot \left(V_{\mathrm{gy}} - \eta_{\mathrm{s}}\psi_{\mathrm{s0}} - \gamma_0\sqrt{\psi_{\mathrm{s0}}}\right) \tag{5.38}$$

and in that way, the calculation of ψ_{sLmin} is avoided. The surface potentials ψ_{s0} and ψ_{sdi} are straightforward to calculate:

$$\psi_{\mathrm{ss0}} = \left[-\frac{\gamma_0}{2\,\eta_{\mathrm{s}}} + \sqrt{\frac{\gamma_0^2}{4\,\eta_{\mathrm{s}}^2} + \frac{V_{\mathrm{gy}}}{\eta_{\mathrm{s}}}}\right]^2 \tag{5.39}$$

$$\psi_{\mathrm{s0}} = \min{}_{\mathrm{sm2}}(\psi_{\mathrm{si0}}, \psi_{\mathrm{ss0}}, 2\,\phi_{\mathrm{t}}) \tag{5.40}$$

$$\psi_{\mathrm{sdi}} = V_{\mathrm{DiB}} \tag{5.41}$$

where ψ_{s0} is the same value as the one calculated for the DC current, with the difference that a slightly modified smoothing function is used to switch from subthreshold into inversion. The reason behind this change is the need for a good transition between depletion and accumulation charge regimes, as will be explained later (see Sec. 6.2.2). We note as well that we are referring ψ_{s0} and ψ_{sL} to the body potential, while ψ_{sLacc} and ψ_{sdi} use the body potential plus ϕ_{bid} as a reference. This explains why Eqs. 5.36 and 5.37 use the flat band voltage between the drain and the gate, and not between the body and the gate.

The calculation of the surface potential at $y = L_{\mathrm{eff}}^{-}$ (ψ_{sL}) and $y = L_{\mathrm{eff}}^{+}$ (ψ_{sLacc}) is less evident. In the ON-state ψ_{sLacc} should be equal to ψ_{sL} (they actually differ by ϕ_{bid}, because of the difference in reference potential). However, when no inversion layer is present, the main part of the drain voltage drops over the P-N^- junction and ψ_{sLacc} differs from ψ_{sL}. For the DC current, only ψ_{sL} was of interest, because this value was sufficient to determine the DC current in the SOI LDMOS.

To find the value of ψ_{sLacc}, we rewrite the expression for the DC current ($I_{\mathrm{CH}} = I_{\mathrm{drg}}$) and solve this equation for ψ_{sLacc}. This is the same expression as Eq. 4.24 derived in Chapter 4 with the difference that we use the body potential + ϕ_{bid} as a reference, and that V_{DiB} is replaced by $V' = \min(V_{\mathrm{g}}^{\mathrm{dr}}, V_{\mathrm{DiB}})$ in the accumulation term. The reason for this is that not only is the case of a fully accumulated surface being considered, but also the possibility of a partly accumulated surface [1]. In the latter case the potential at the

[1] This was not necessary for the calculation of the DC current, because I_{CH} has already saturated ($\psi_{\mathrm{sL}} = \psi_{\mathrm{sLsat}}$) when the accumulation layer starts to disappear at the drain end.

end of the accumulation layer is given by $V_g^{dr} = V_{GfB} - V_{FB}^{fdr}$. We have

$$I_{drg} = \beta_{acc}^{e} \cdot (V' - \psi_{sLacc}) \left(V_g^{dr} - \frac{1}{2}(V' + \psi_{sLacc}) \right) + \frac{f_v}{R_{ON}} (V' - \psi_{sLacc}) \quad (5.42)$$

with $\beta_{acc}^{e} = \frac{\beta_{acc}}{1+\theta_{acc} \cdot (V_g^{dr} - V_{DiB})}$. Solving for ψ_{sLacc} gives :

$$\psi_{sLacc} = V_g^{dr} + \frac{f_v}{R_{ON}\,\beta_{acc}^{e}} - \left(\left(V_g^{dr} - V_{DiBn} \right) + \frac{f_v}{R_{ON}\,\beta_{acc}^{e}} \right) \cdot \sqrt{1 + \frac{2 I_{CH}}{\beta_{acc}^{e} \cdot \left(\mathrm{pos}(V_g^{dr} - V_{DiBn}) + \frac{f_v}{R_{ON}\,\beta_{acc}^{e}} \right)^2}} \quad (5.43)$$

with V_{DiBn} defined as

$$V_{DiBn} = \begin{cases} \min(V_{DiB}, V_g^{dr}) & \text{if } V_{GfB} > V_{th} \\ V_{DiB} & \text{otherwise.} \end{cases} \quad (5.44)$$

where V_{DiBn} is used instead of V' to ensure that, when $V_{GfB} < V_{th}$ (i.e. the device is in sub-threshold), ψ_{sLacc} equals V_{DiB} in any case. The smoothing function which describes this behaviour in a continuous way can be found in Sec. C.9.1 of App. C.

The strong inversion surface potential ψ_{siLinv} at $y = L_{eff}^{-}$ can now be calculated in exactly the same way as ψ_{si0}, the strong inversion surface potential at $y = 0$: V_{SB} is replaced by ψ_{sLacc}, which has the function of drain voltage for the MOSFET part of the LDMOS. The rest of the derivation is identical and refer to [13] for the physical background. The expression for ψ_{siLinv} is given in Sec. C.9 (block 1B) in App. C. ψ_{sL} is then obtained by taking the smooth minimum of the subthreshold surface potential (ψ_{ssL}) and ψ_{siLinv}:

$$\psi_{ssL} = \left[-\frac{\gamma_L}{2\,\eta_s} + \sqrt{\frac{\gamma_L^2}{4\,\eta_s^2} + \frac{V_{gy}}{\eta_s}} \right]^2 \quad (5.45)$$

$$\psi_{sL} = \min_{sm2}(\psi_{siLinv}, \psi_{ssL}, 2\,\phi_t)\ . \quad (5.46)$$

Now that the expressions for the four main surface potentials used to calculate the charge densities have been formulated, let us return to the principal aim of this section, which is to find the charge distribution as a function of position y in the channel. Eq. 5.29 can also be integrated from L_{min} to some point y in the channel, or from L_{eff} to some point y in the channel:

$$I_{CH} = \begin{cases} -\mu \frac{W}{C_{of} \cdot (y - L_{min})} \left(\frac{1}{\alpha} \int_{q_0}^{q_c(y)} q_c \cdot dq_c \right) & \text{for } L_{min} < y < L_{eff}: \\ -\mu \frac{W}{C_{of} \cdot (y - L_{eff})} \left(\int_{q_{Lacc}}^{q_c(y)} q_c \cdot dq_c \right) & \text{for } L_{eff} < y < L_{tot}: \end{cases} . \quad (5.47)$$

Knowing that I_{CH} must be constant at each point along the length of the channel, allows

us to equate Eq. 5.32 to 5.47 and 5.33 to 5.47 for respectively $y < L_{\text{eff}}$ and $y > L_{\text{eff}}$. This then provides us with the charge distributions:

$$q_{\text{cinv}} = \sqrt{q_0^2 + \frac{y - L_{\text{min}}}{L_{\text{eff}} - L_{min}} \left(q_{\text{L}}^2 - q_0^2\right)} \quad \text{for } L_{\text{min}} < y < L_{\text{eff}} \tag{5.48}$$

$$q_{\text{cacc}} = \sqrt{q_{\text{Lacc}}^2 + \frac{y - L_{\text{eff}}}{L_{\text{drov}}} \left(q_{\text{di}}^2 - q_{\text{Lacc}}^2\right)} \quad \text{for } L_{\text{eff}} < y < L_{\text{tot}}. \tag{5.49}$$

5.3.5 Final Expression for the Nodal Charges Originating from the Channel Charge

Substituting Eqs. 5.48 and 5.49 into Eqs. 5.1, 5.7 and 5.8 and performing the integrations, gives the analytical expressions for the nodal charges originating from the inversion and accumulation channel charges. For the channel charge we find:

$$Q_{\text{CH}} = -\frac{2}{3} W \left\{ (L_{\text{eff}} - L_{\text{min}})\, q_0\, \frac{F^2 + F + 1}{F + 1} + L_{\text{drov}}\, q_{\text{Lacc}}\, \frac{F_{\text{acc}}^2 + F_{\text{acc}} + 1}{F_{\text{acc}} + 1} \right\} \tag{5.50}$$

where

$$F = \frac{q_{\text{L}}}{q_0} \tag{5.51}$$

$$F_{\text{acc}} = \frac{q_{\text{di}}}{q_{\text{Lacc}}}. \tag{5.52}$$

The charge associated with the drain as predicted by the Ward and Dutton partitioning scheme, results in:

$$Q_{\text{Diwd}} = Q_{\text{Dinv}} + Q_{\text{Dacc}} \tag{5.53}$$

where

$$\begin{aligned} Q_{\text{Dinv}} &= W \left(\int_{L_{\text{min}}}^{L_{\text{eff}}} \frac{y}{L_{\text{tot}} - L_{\text{min}}}\, q_{\text{cinv}} \cdot dy \right) \\ &= -\frac{2}{15} W \frac{(L_{\text{eff}} - L_{\text{min}})^2}{L_{\text{tot}} - L_{\text{min}}}\, q_0\, \frac{3\,F^3 + 6\,F^2 + 4\,F + 2}{(F+1)^2} \end{aligned} \tag{5.54}$$

$$\begin{aligned} Q_{\text{Dacc}} &= W \left(\int_{L_{\text{eff}}}^{L_{\text{tot}}} \frac{y}{L_{\text{tot}} - L_{\text{min}}}\, q_{\text{cacc}} \cdot dy \right) \\ &= -\frac{2}{15} W \frac{(L_{\text{drov}})^2}{L_{\text{tot}} - L_{\text{min}}}\, q_{\text{Lacc}}\, \frac{3\,F_{\text{acc}}^3 + 6\,F_{\text{acc}}^2 + 4\,F_{\text{acc}} + 2}{(F_{\text{acc}} + 1)^2} \\ &\quad + \frac{2}{3} W \frac{(L_{\text{eff}} - L_{\text{min}}) L_{\text{drov}}}{L_{\text{tot}} - L_{\text{min}}}\, q_{\text{Lacc}}\, \frac{F_{\text{acc}}^2 + F_{\text{acc}} + 1}{F_{\text{acc}} + 1}. \end{aligned} \tag{5.55}$$

Let us now have a look at the extra charge Q_{Swdlim}, which has to be added to the drain charge to account for the doping profile along the channel. The subscript "lim" is added to the different charge densities to indicate that V_{GfB} is replaced by V_{GfBlim} where appropriate, resulting in q_{Llim}, q_{Lacclim}, q_{dilim} and q_{0lim}. Note that by definition $q_{\text{0lim}} = 0$.

Substituting these into the equations for the charge density as a function of y (Eqs. 5.48 and 5.49) yields

$$q_{\text{cinvlim}} = \sqrt{\frac{y - L_{\text{min}}}{L_{\text{eff}} - L_{\text{min}}}(q^2_{\text{Llim}})} \qquad \text{for } L_{\text{min}} < y < L_{\text{eff}} \text{ and} \tag{5.56}$$

$$q_{\text{cacclim}} = \sqrt{q^2_{\text{Lacclim}} + \frac{y - L_{\text{eff}}}{L_{\text{drov}}}(q^2_{\text{dilim}} - q^2_{\text{Lacclim}})} \text{ for } L_{\text{eff}} < y < L_{\text{tot}}. \tag{5.57}$$

We refer to App. E for the derivation of the expression for q_{Llim}, q_{dilim} and q_{Lacclim}. The extra charge can now be found from

$$\begin{aligned} Q_{\text{Swdlim}} &= W \int_{L_{\text{min}}}^{L_{\text{eff}}} \left(1 - \frac{y}{L_{\text{tot}} - L_{\text{min}}}\right) q_{\text{cinvlim}} \cdot dy \\ &\quad + W \int_{L_{\text{eff}}}^{L_{\text{tot}}} \left(1 - \frac{y}{L_{\text{tot}} - L_{\text{min}}}\right) q_{\text{cacclim}} \cdot dy \\ &= Q_{\text{Sinvlim}} + Q_{\text{Sacclim}} \end{aligned} \tag{5.58}$$

where

$$Q_{\text{Sinvlim}} = W\, q_{\text{Llim}} \cdot \left(-\frac{4}{15} \frac{(L_{\text{eff}} - L_{\text{min}})^2}{L_{\text{tot}} - L_{\text{min}}} - \frac{2}{3} \frac{(L_{\text{eff}} - L_{\text{min}}) L_{\text{drov}}}{L_{\text{tot}} - L_{\text{min}}} \right) \tag{5.59}$$

$$Q_{\text{Sacclim}} = -\frac{2}{15} W \frac{L^2_{\text{drov}}}{L_{\text{tot}} - L_{\text{min}}} q_{\text{Lacclim}} \cdot \left(\frac{2\, F^3_{\text{acclim}} + 4\, F^2_{\text{acclim}} + 6\, F_{\text{acclim}} + 3}{(F_{\text{acclim}} + 1)^2} \right) \tag{5.60}$$

with

$$F_{\text{acclim}} = \frac{q_{\text{dilim}}}{q_{\text{Lacclim}}} \,. \tag{5.61}$$

Using Eqs. 5.50, 5.53 and 5.58 the total charges associated with the source and the drain can be written as

$$Q_{\text{Di}} = Q_{\text{Diwd}} + Q_{\text{Swdlim}} \tag{5.62}$$

$$Q_{\text{S}} = Q_{\text{CH}} - Q_{\text{Di}} \,. \tag{5.63}$$

5.4 Nodal Charge Originating from Depletion under the Front Gate in the P-Body

The total body depletion charge in the P-body under the thin gate oxide is found by integrating the body depletion charge density from 0 to L_{eff}:

$$Q_{\text{Bdep}} = W \int_0^{L_{\text{eff}}} q_b(y) \cdot dy \tag{5.64}$$

where $q_{\text{b}}(y)$ is the body charge density at position y. Using the depletion approximation, which assumes that the mobile carrier concentrations are negligible in comparison with

the acceptor concentration inside the depletion region, q_b can be expressed as [9]

$$q_b(y) = -C_{of}\,\gamma(y)\,\sqrt{\psi_s}\,. \tag{5.65}$$

In order to perform the integration, ψ_s is needed as a function of y. For this we proceed as follows: from the relation $q_{cinv} = -C_{of}\,(V_{gy} - \eta_s\psi_s - \gamma(y)\,\sqrt{\psi_s})$, ψ_s can be expressed as a function of $q_{cinv}(y)$, which yields

$$q_b(y) = -\frac{C_{of}}{2}\left(-\frac{\gamma(y)^2}{\eta_s} + \gamma(y)\,\sqrt{\frac{\gamma(y)^2}{4\,\eta_s} + V_{gy} + \frac{q_{cinv}(y)}{C_{of}}}\right) \tag{5.66}$$

where $q_{cinv}(y)$ is given by Eq. 5.48. Substituting Eq. 5.66 in Eq. 5.64 results in

$$\begin{aligned} Q_{Bdep} &= W\int_0^{L_{min}} q_b(y, q_c = 0)\cdot dy + W\int_{L_{min}}^{L_{eff}} q_b(y)\cdot dy \\ &= W\cdot\left(\frac{C_{of}}{2\eta_s}\int_0^{L_{eff}}\gamma(y)^2\cdot dy - \int_0^{L_{min}}\gamma(y)\sqrt{\frac{\gamma(y)^2}{4\eta_s} + V_{gy}}\cdot dy\right. \\ &\quad \left. - \int_{L_{min}}^{L_{eff}}\gamma(y)\sqrt{\frac{\gamma(y)^2}{4\eta_s} + V_{gy} + \frac{q_{cinv}(y)}{C_{of}}}\cdot dy\right). \end{aligned} \tag{5.67}$$

The first two terms of Eq. 5.67 can be calculated analytically when an exponential profile is used for the body factor ($\gamma(y) = \gamma_0 \exp(-k_{N_A} y/(2L_{eff}))$). The third term cannot be integrated analytically. A good approximation is found by splitting the integral in two, using two mean values for $\gamma(y)$, i.e.

$$\begin{aligned} &\int_{L_{min}}^{L_{eff}}\gamma(y)\,\sqrt{\frac{\gamma(y)^2}{4\,\eta_s} + V_{gy} + \frac{q_{cinv}(y)}{C_{of}}}\cdot dy \cong \\ &\int_{L_{min}}^{L_i}\gamma_{e1}\sqrt{\frac{\gamma_{e1}^2}{4\,\eta_s} + V_{gy} + \frac{q_{cinv}(y)}{C_{of}}}\cdot dy + \int_{L_i}^{L_{eff}}\gamma_{e2}\sqrt{\frac{\gamma_{e2}^2}{4\eta_s} + V_{gy} + \frac{q_{cinv}(y)}{C_{of}}}\cdot dy \end{aligned} \tag{5.68}$$

with

$$L_i = \frac{L_{min} + L_{eff}}{2} \tag{5.69}$$

$$\gamma_{e1} = \frac{1}{L_i}\int_{L_{min}}^{L_i}\gamma(y)\cdot dy = \frac{4\,L_{eff}\cdot(\gamma(L_{min}) - \gamma(L_i))}{k_{N_A}\cdot(L_{eff} - L_{min})} \tag{5.70}$$

$$\gamma_{e2} = \frac{1}{L_i}\int_{L_i}^{L_{eff}}\gamma(y)\cdot dy = \frac{4\,L_{eff}\cdot(\gamma(L_i) - \gamma(L_{eff}))}{k_{N_A}\cdot(L_{eff} - L_{min})} \tag{5.71}$$

Now the full integration of the depletion charge can be performed and we refer to Sec. C.9.2 of App. C for the final expression.

In Figs. 5.6 and 5.7 the exact solution for the body depletion charge, evaluated by numerical integration, is compared with the approximated solution, where two effective values for the body factor (Eqs. 5.70 and 5.71) are used. In this comparison a large value for the doping gradient ($k_{N_A} = 1.5$) was chosen, because the discrepancy increases with

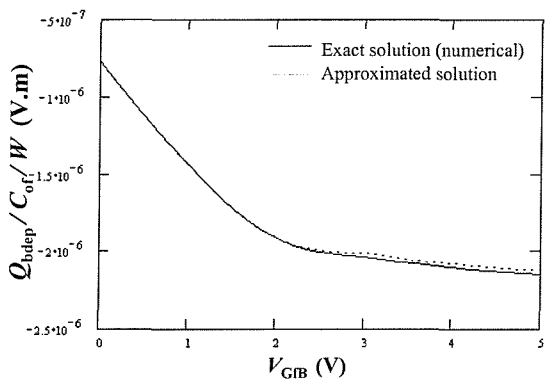


Figure 5.6: Comparison of the exact and approximated body depletion charge vs. V_{GfB} for $V_{DB} = V_{SB} = 0$ V

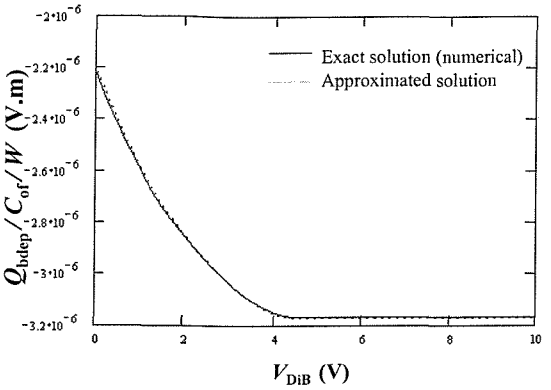


Figure 5.7: Comparison of the exact and approximated body depletion charge vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V

the doping gradient. It can be seen that the approximated solution gives an almost perfect prediction of the body depletion charge.

It is important to compare the derivatives of the body charge as well, as they will determine the body (trans)capacitances. In Figs. 5.8 and 5.9 the (trans)capacitances are compared, and it can be seen that our approximation gives a very good match with the exact solution. Therefore, in the following treatment our model will be based on the approximate solution.

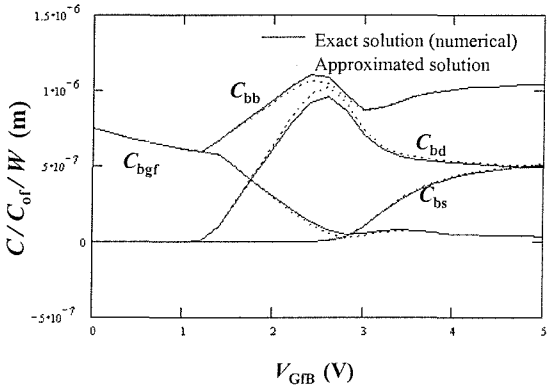


Figure 5.8: Comparison of the exact and approximated body depletion (trans)capacitances vs. V_{GfB} for $V_{DB} = V_{SB} = 0$ V

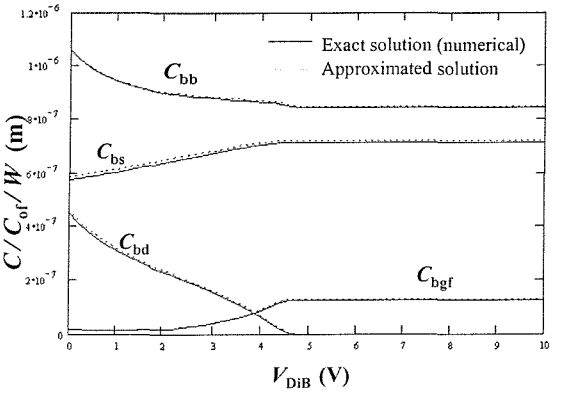


Figure 5.9: Comparison of the exact and approximated body depletion (trans)capacitances vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V

5.5 Nodal Charges Originating from Accumulation under the Front Gate in the *P*-Body

Consider the case where a gate-body voltage decreases below the flat band voltage $V_{\mathrm{FB}}^{\mathrm{f}}$. Now holes accumulate at the surface. In deep accumulation a conductive sheet of holes is present under the oxide, and the total hole charge is given by

$$Q_{\mathrm{Bacc}} = W\ L_{\mathrm{eff}}\ C_{\mathrm{of}} \cdot \left(2\ \phi_{\mathrm{t}} \ln\!\left(1 + \exp(\frac{-V_{\mathrm{g}}}{2\ \phi_{\mathrm{t}}})\right)\right). \tag{5.72}$$

The conversion from weak into deep accumulation is made continuous with a logarithmic smoothing function which limits $-V_{\mathrm{g}}$ to positive values.

5.6 Capacitances for a MOSFET with Lateral Doping Gradient in the Channel

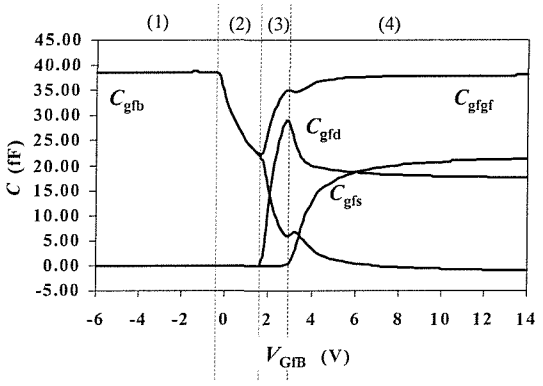


Figure 5.10: C_{gfgf}, C_{gfd}, C_{gfs}, C_{gfb} vs. V_{GfB} for $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V; $k_{\mathrm{N_A}} = 1.5$

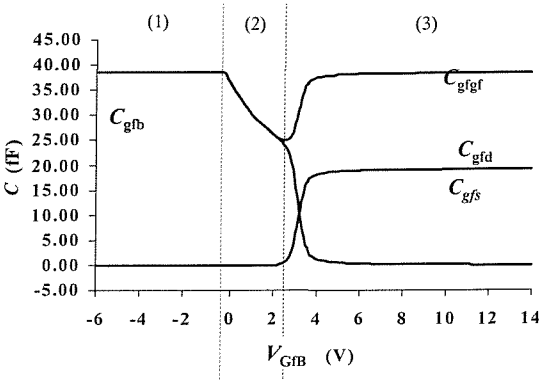


Figure 5.11: C_{gfgf}, C_{gfd}, C_{gfs}, C_{gfb} vs. V_{GfB} for $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V; $k_{\mathrm{N_A}} = 0$

At this point in the development of the charge model for the SOI LDMOS, it is interesting to have a look at the capacitance behaviour when $L_{\mathrm{drov}} = L_{\mathrm{dr}} = 0$, i.e. only the MOSFET part with lateral doping gradient is considered. The partial derivatives of the charges are known as the capacitances and transcapacitances, and are usually defined as:

$$C_{ij} = \begin{cases} \frac{\partial Q_{\mathrm{i}}}{\partial V_j} & \text{for } i = j \\ -\frac{\partial Q_{\mathrm{i}}}{\partial V_j} & \text{for } i \neq j \end{cases} \tag{5.73}$$

where the subscripts denote the terminals controlling the charges, and where the signs have been defined to keep most of them positive. This gives rise to sixteen (trans)capacitances for the intrinsic part of the SOI LDMOS, out of which only nine are independent because of charge conservation and Kirchoff's voltage law [15]. Depending on the details under

study, either all 16 quantities will be plotted in the following, or else we will limit ourselves to 9 independent trans(capacitances).

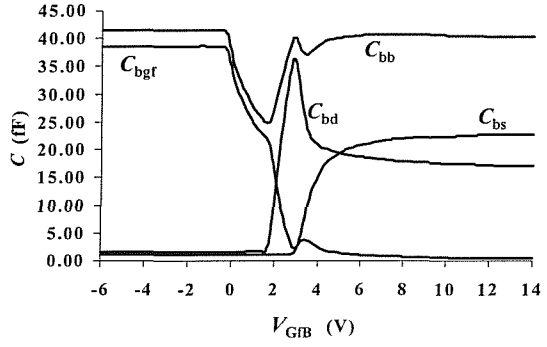


Figure 5.12: C_{bgf}, C_{bd}, C_{bs}, C_{bb} vs. V_{GfB} for $V_{DB} = V_{SB} = 0$ V; $k_{N_A} = 1.5$

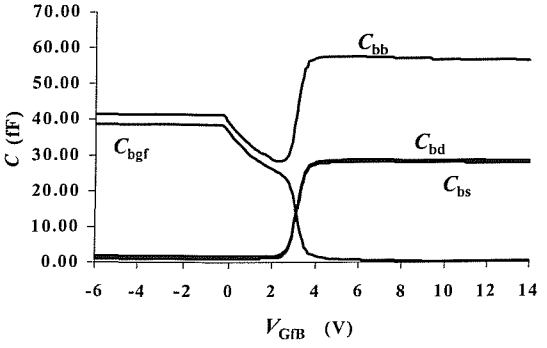


Figure 5.13: C_{bgf}, C_{bd}, C_{bs}, C_{bb} vs. V_{GfB} for $V_{DB} = V_{SB} = 0$ V; $k_{N_A} = 0$

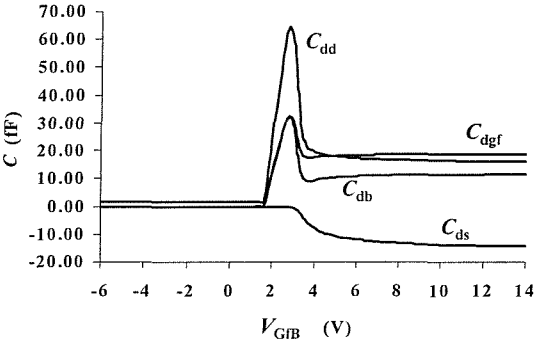


Figure 5.14: C_{dgf}, C_{dd}, C_{ds}, C_{db} vs. V_{GfB} for $V_{DB} = V_{SB} = 0$ V; $k_{N_A} = 1.5$

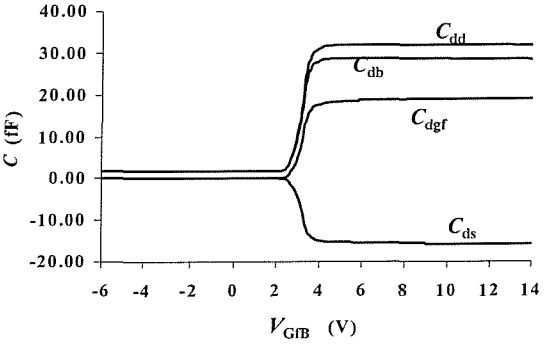


Figure 5.15: C_{dgf}, C_{dd}, C_{ds}, C_{db} vs. V_{GfB} for $V_{DB} = V_{SB} = 0$ V; $k_{N_A} = 0$

Let us now have a look at these capacitances as a function of V_{GfB}. In Fig. 5.10 the partial derivative of the gate charge with respect to the different bias voltages is shown. In region (1) the gate bias is negative and the surface is accumulated (cf. Sec. 5.5), leaving only C_{gfb} and C_{gfgf} non-zero. In region (2), the accumulation layer has disappeared and a depletion layer is growing. When the threshold voltage at the drain side of the channel is reached, C_{gfd} starts to rise (see region (3)). In region (4) the source threshold voltage (V_{th0}) is reached. This allows the source to provide electrons to the channel and reduces the number of electrons the drain can exchange with the channel when the gate bias is varied. Hence we see a decrease in C_{gfd}. These transitions are also illustrated in the other capacitances (see Figs. 5.12 and 5.14). The little bump in the curve for C_{bgf} (and

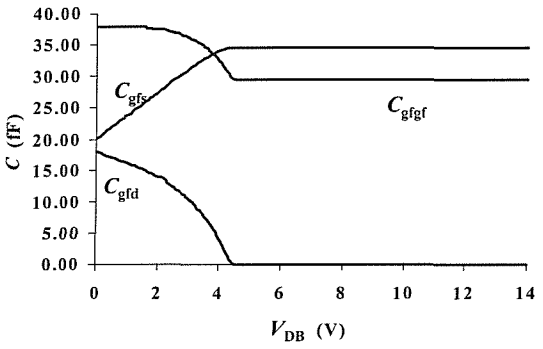


Figure 5.16: C_{gfgf}, C_{gfd}, C_{gfs} vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V; $k_{N_A} = 1.5$

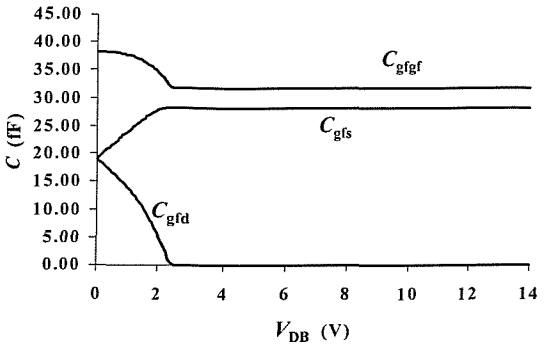


Figure 5.17: C_{gfgf}, C_{gfd}, C_{gfs} vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V; $k_{N_A} = 0$

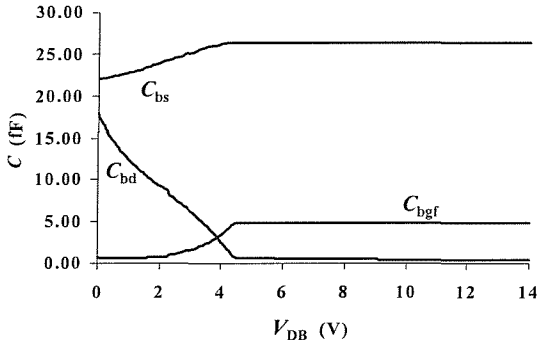


Figure 5.18: C_{bgf}, C_{bd}, C_{bs} vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V; $k_{N_A} = 1.5$

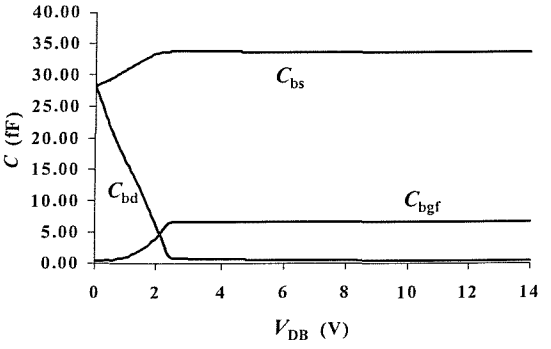


Figure 5.19: C_{bgf}, C_{bd}, C_{bs} vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V; $k_{N_A} = 0$

C_{bb}) in Fig. 5.12 is due to the use of L_{min}, which is not perfectly matched with the other expressions. For comparison, Figs. 5.11, 5.13 and 5.15 show the zero doping gradient case, but otherwise use identical parameters as Figs. 5.10, 5.12 and 5.14. If the doping in the channel is constant and $V_{DB} = V_{SB} = 0$, the device behaves in a perfectly symmetrical way, leading to equal derivatives of any charge with respect to the drain and the source (i.e. $C_{gfs} = C_{gfd}$, etc.).

It is also interesting to have a look at the same capacitances as a function of V_{DS}, when the channel is in deep inversion ($V_{GfS} = 8$ V). The trends of these curves should not differ a lot from standard MOSFET capacitances curves. Figs. 5.16-5.19 illustrate a higher saturation voltage for the case where $k_{N_A} = 1.5$, which is logical since the saturation voltage is roughly given by $V_{GfB} - V_{thL}$ and V_{thL} is lower when the doping is decreasing towards the drain. The (trans)capacitances coupled to the drain charge follow quite a

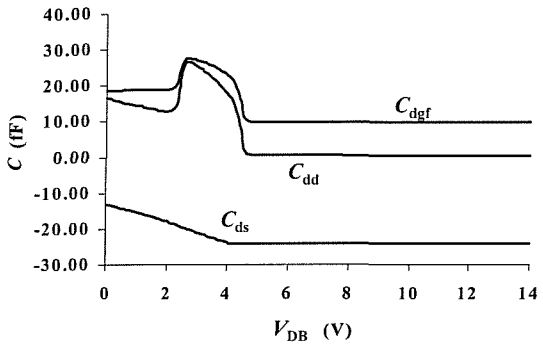


Figure 5.20: C_{dgf}, C_{dd}, C_{ds} vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V

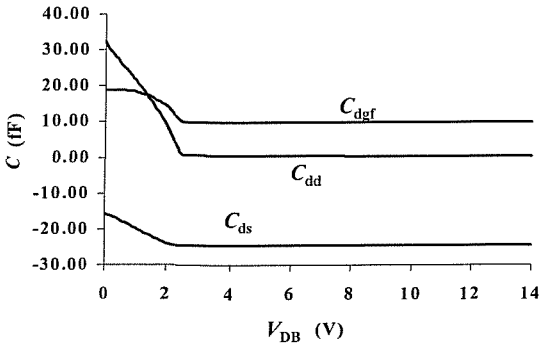


Figure 5.21: C_{dgf}, C_{dd}, C_{ds} vs. V_{DB} for $V_{GfB} = 8$ V and $V_{SB} = 0$ V

different course for the high doping gradient case at low drain biases (Fig. 5.20), compared with the constant doping case (Fig. 5.21). The slight increase of C_{dgf} before decreasing when the saturation voltage is reached is due to the use of the modified Ward and Dutton scheme, but even though the trend of the curve is correct, measurements predict a more gradual increase of C_{dgf} with V_{DB}.

5.7 Nodal Charges Originating from the Depletion under the Front Gate in the Drift Region

When V_{DiGf} exceeds the flat band voltage in the drift region (V_{FB}^{dr}), the electrons under the thin gate oxide are driven away, leaving a depletion region behind. Again using the depletion approximation [9], the depletion charge density under the front gate in the N^- region can be written as

$$q_{dep}^{dr} = C_{of}\, \gamma^{fdr} \sqrt{\psi_s^{dr}} \tag{5.74}$$

where γ^{fdr} is the body factor in the drift region given by $\gamma^{fdr} = \frac{\sqrt{2q\epsilon_{si}N_D}}{C_{of}}$.

The calculation of the surface potential can be easily understood if the N^- region under the thin gate oxide is considered to be the body of a PMOS; the internal drain voltage then plays the role of "body voltage" in the PMOS, and the body voltage plays the role of the "source voltage" in the PMOS. This is illustrated in Fig. 5.22.

Making identical assumptions as the ones used to calculate the surface potential for the MOS part of the LDMOS, the subthreshold surface potential can be written as [13]

$$\psi_{ss}^{dr} = \left\{ -\frac{\gamma^{fdr}}{2\,\eta_s} + \sqrt{\frac{(\gamma^{fdr})^2}{4\,\eta_s^2} + \frac{V_{dgy}^{dr}}{\eta_s}} \right\}^2 \tag{5.75}$$

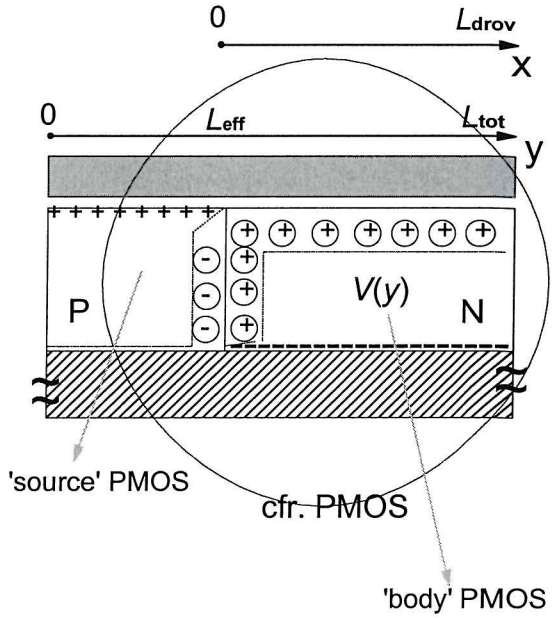


Figure 5.22: Recognition of PMOS like device in the SOI LDMOS, to explain the formulation of the surface potential in the N^- region under the thin gate oxide

with the short-hand notation

$$V_{\mathrm{dgy}}^{\mathrm{dr}} = \mathrm{pos}\Big(-V_{\mathrm{GfB}} + V_{\mathrm{FB}}^{\mathrm{fdr}} + V(y)\Big) \tag{5.76}$$

where V(y) is the potential in the bulk of the drift region with respect to the body. The inversion surface potential is given by [13]

$$\psi_{\mathrm{si}}^{\mathrm{dr}} = A_{\mathrm{dr}} + \phi_{\mathrm{t}}\ \ln\left(\frac{1}{\phi_{\mathrm{t}}}\left\{\frac{1}{(\gamma^{\mathrm{fdr}})^2}(V_{\mathrm{gxdr}} - \eta_{\mathrm{s}}\ A_{\mathrm{dr}})^2 - A_{\mathrm{dr}} + \phi_{\mathrm{t}}\right\}\right) \tag{5.77}$$

with

$$A_{\mathrm{dr}} = 2\ \phi_{\mathrm{Fdr}} + V(y) \tag{5.78}$$

$$V_{\mathrm{gxdr}} = \mathrm{pos}_{\mathrm{sm}}\Big(V(y) - V_{\mathrm{g}}^{\mathrm{dr}} - (\eta_{\mathrm{s}}\ A_{\mathrm{dr}} - \phi_{\mathrm{t}}(\eta_{\mathrm{s}} - 1) + \gamma^{\mathrm{fdr}}\ \sqrt{A_{\mathrm{dr}}}), 5\ \phi_{\mathrm{t}}\Big)\ . \tag{5.79}$$

Joining Eqs. 5.75 and 5.77 together gives the expression for the surface potential:

$$\psi_{\mathrm{s}}^{\mathrm{dr}} = \mathrm{min}_{\mathrm{sm2}}\Big(\psi_{\mathrm{ss}}^{\mathrm{dr}}, \psi_{\mathrm{si}}^{\mathrm{dr}}, \phi_{\mathrm{t}}\Big)\ . \tag{5.80}$$

The functions $\mathrm{pos}_{\mathrm{sm}}$ and $\mathrm{min}_{\mathrm{sm2}}$ can be found in App. C. The surface potential at the

two extremes of the channel is given by:

$$\psi_{\rm s}^{\rm dr} = \begin{cases} \psi_{\rm s}^{\rm dr}(V = \psi_{\rm sLacc}) & \text{for } y = L_{\rm eff}^{+} \\ \psi_{\rm s}^{\rm dr}(V = V_{\rm DiB}) & \text{for } y = L_{\rm tot} \end{cases} . \tag{5.81}$$

Using these two expressions provides the depletion charge densities $q_{\rm depL}^{\rm dr}$ and $q_{\rm depdi}^{\rm dr}$ for respectively $y = L_{\rm eff}^{+}$ and $y = L_{\rm tot}$. Looking at the depletion boundaries in the drift region of the LV and MV SOI LDMOS simulated in Chapter 2, illustrates that the distribution of the depletion charge in the drift region is a two-dimensional problem, which is very difficult to solve analytically. For this reason an empirical distribution for the depletion charge density in the drift region is used:

$$q_{\rm dep}^{\rm dr}(x) \;=\; q_{\rm depL}^{\rm dr} \cdot \left(\frac{q_{\rm depdi}^{\rm dr}}{q_{\rm depL}^{\rm dr}}\right)^{\frac{x}{L_{\rm drov}}} \tag{5.82}$$

Integrating gives the total charge :

$$Q_{\rm Ddep} \;=\; W\, C_{\rm of} \int_0^{L_{\rm drov}} q_{\rm dep}^{\rm dr}(x) \cdot dx \tag{5.83}$$

$$\;=\; W\, C_{\rm of}\, L_{\rm drov}\, q_{\rm depL}^{\rm dr} \cdot \left(\frac{F_{\rm dep} - 1}{ln(F_{\rm dep})}\right) \tag{5.84}$$

with $F_{\rm dep} = \frac{q_{\rm depdi}^{\rm dr}}{q_{\rm depL}^{\rm dr}}$. The justification for this empirical distribution is as follows:

- Obviously in the *OFF-state* of the device, when $\psi_{\rm Lacc} = \psi_{\rm di} = V_{\rm DiB}$, the distribution has to be constant over the whole length of the drift region; we want $q_{\rm dep}^{\rm dr}(x) = q_{\rm depdi}^{\rm dr} = q_{\rm depL}^{\rm dr}$.
- In the *ON-state* of the device, the distribution function has to increase continuously from $q_{\rm depL}^{\rm dr}$ to $q_{\rm depdi}^{\rm dr}$. Let us now consider the case where $q_{\rm depL}^{\rm dr}$ is zero and $q_{\rm depdi}^{\rm dr} > 0$. From our simulations in Chapter 2 we know that the accumulation layer no longer extends all the way to the drain. However, in our model, $q_{\rm cacc}(y)$ is given by Eq. 5.49, and as long as $q_{\rm caccL} > 0$, $q_{\rm cacc}(y)$ only becomes zero right at the drain end. Hence, as long as $q_{\rm caccL} > 0$, the total capacitance between the gate and the accumulation channel is given by $(C_{\rm of}\ W\ L_{\rm drov})$, so we do not want to add any depletion capacitance to this value. Returning to our discussion about the choice of a distribution function, the required function needs the following property: $q_{\rm dep}^{\rm dr}(x) = 0$ for $0 < x < L_{\rm drov}$, as long as $q_{\rm depL}^{\rm dr} = 0$ (or as long as $q_{\rm caccL} > 0$).

It can be seen that the requirements mentioned in the two paragraphs above are fulfilled by the chosen distribution function.

5.8 Nodal Charges Originating from Inversion under the Front Gate in the Drift Region

When V_{DiGf}, the internal drain-gate voltage, exceeds the negative drain dependent threshold voltage in the drift region ($\cong V_{\mathrm{FB}}^{\mathrm{fdr}} - 2\phi_{\mathrm{dr}} - V_{\mathrm{DiB}} - \gamma^{\mathrm{fdr}}\sqrt{2\phi_{\mathrm{dr}} + V_{\mathrm{DiB}}}$), free holes (coming from the P-body) are attracted under the thin gate oxide in the drift region, forming a surface inversion layer. The inversion charge density under the front gate in the N^- region can be written as

$$q_{\mathrm{cinv}}^{\mathrm{dr}} = C_{\mathrm{of}} \cdot \left(V_{\mathrm{dgy}}^{\mathrm{dr}} - \eta_{\mathrm{s}}\, \psi_{\mathrm{s}}^{\mathrm{dr}} - \gamma^{\mathrm{fdr}} \sqrt{\psi_{\mathrm{s}}^{\mathrm{dr}}} \right) \tag{5.85}$$

where $\psi_{\mathrm{s}}^{\mathrm{dr}}$ is the surface potential in the N^- region. This situation can only occur in the OFF-state of the device, and hence the potential in the undepleted area of the drift region is the same everywhere, and is given by V_{DiB}. This means that $\psi_{\mathrm{s}}^{\mathrm{dr}}$ in Eq. 5.85 is constant and given by $\psi_{\mathrm{s}}^{\mathrm{dr}}(V_{\mathrm{DiB}})$, as defined by Eq. 5.80. The total inversion charge is simply the product of the inversion charge density and the total surface area of the drift region,

$$Q_{\mathrm{Binv}} = W\, L_{\mathrm{drov}}\, q_{\mathrm{cinv}}^{\mathrm{dr}} \,. \tag{5.86}$$

5.9 Total of all Nodal Charges in the intrinsic part of the SOI LDMOS

Adding the nodal charges calculated in the previous sections to the corresponding nodes gives:

$$Q_{\mathrm{B}} = Q_{\mathrm{Bdep}} + Q_{\mathrm{Bacc}} + Q_{\mathrm{Binv}} \tag{5.87}$$

$$Q_{\mathrm{Di}} = Q_{\mathrm{Dinv}} + Q_{\mathrm{Dacc}} + Q_{\mathrm{Ddep}} \tag{5.88}$$

$$Q_{\mathrm{Gf}} = -(Q_{\mathrm{CHinv}} + Q_{\mathrm{CHacc}} + Q_{\mathrm{Bdep}} + Q_{\mathrm{Bacc}} + Q_{\mathrm{Ddep}} + Q_{\mathrm{Binv}}) \tag{5.89}$$

$$Q_{\mathrm{S}} = -(Q_{\mathrm{Gf}} + Q_{\mathrm{D}} + Q_{\mathrm{Di}} + Q_{\mathrm{B}}) \,. \tag{5.90}$$

5.10 The Extrinsic Part

We have added the standard constant overlap capacitances between the front gate and the drain (C_{gfdo}), the gate and the source (C_{gfso}) and the gate and the body (C_{gfbo}).

Let us now have a look at the charges at the buried oxide. Exactly the same analysis as we did for the front gate in Sec. 5.2 can be repeated for the back gate. The following situations can be distinguished:

- A very high positive back gate bias causes inversion at the buried oxide interface in the P-body, and accumulation in the N^- drift region. This electron sheet creates a capacitance between the back gate and the drain, which is to a good approximation given by $A_{\mathrm{box}}C_{\mathrm{ob}}$, where A_{box} is the total area of the buried oxide interface of the

device. The depletion layer present at the buried oxide interface in the P-body creates a capacitance between the body and the back gate terminal.

- A very high negative back gate bias causes accumulation at the buried oxide interface in the P-body, and inversion in the N^- drift region. This hole sheet creates a capacitance between the back gate and the body, given by $A_{\text{box}}C_{\text{ob}}$. The depletion layer present at the buried oxide interface in the drift region creates a capacitance between the drain and the back gate terminal.

The influence of the back gate parasitic capacitances on the switching characteristics of the SOI LDMOS can be considerable [16, 17]; for thin buried oxide thicknesses the drain-back gate capacitance can add an important contribution to the output capacitance, and needs to be taken into account. In our model we have added constant capacitances between the back gate and the drain (C_{gbd}), the back gate and the body (C_{gbb}) and the back gate and the source (C_{gbs}). The latter is only necessary if the source junction reaches the buried oxide, which is usually not the case in LDMOS devices, but C_{gbs} was added for completeness. To get a really accurate description of the capacitance behaviour at the back gate, it is clear that one has to do a quantitative analysis of the charges at the buried oxide leading to non-constant non-reciprocal capacitance values.

Finally, our model also accounts for the junction capacitances of the parasitic bipolar transistor with the body acting as the base. This behaviour was extensively studied in [13] for a PD depleted SOI MOSFET and will not be repeated here. The model equations are given in Sec. C.10.3 in App. C.

5.11 The Large and Small Signal Model

In our model the transient currents are modelled as the time derivatives of the nodal charges. Three current sources $\frac{dQ_{\text{Gf}}}{dt}$, $\frac{dQ_{\text{S}}}{dt}$ and $\frac{dQ_{\text{Di}}}{dt}$ account for the time variation of the nodal charges, and are placed between the respective terminals and the body. The choice of the body as a recipient node is purely arbitrary and, since our device is absolutely assymetrical, any node would have been a worthy choice. It is only for consistency with Southampton's PD SOI model that the body was chosen as a reference, and as recipient node for the transient current. Fig. 5.23 shows the complete large signal model, including the time derivatives of the nodal charges for the intrinsic part of the model, and the extrinsic capacitances.

In a SPICE transient analysis the time domain derivatives are numerically integrated using either the trapezoidal or Gear method, according to an option which can be specified in the analysis set-up. The charges then need to be linearised for the Newton Raphson solver, which requires the calculation of the partial derivatives of each of the nodal charges with respect to each of the terminal voltages (or in other words, the (trans)capacitances as specified in Sec. 5.6) and with respect to ΔT.

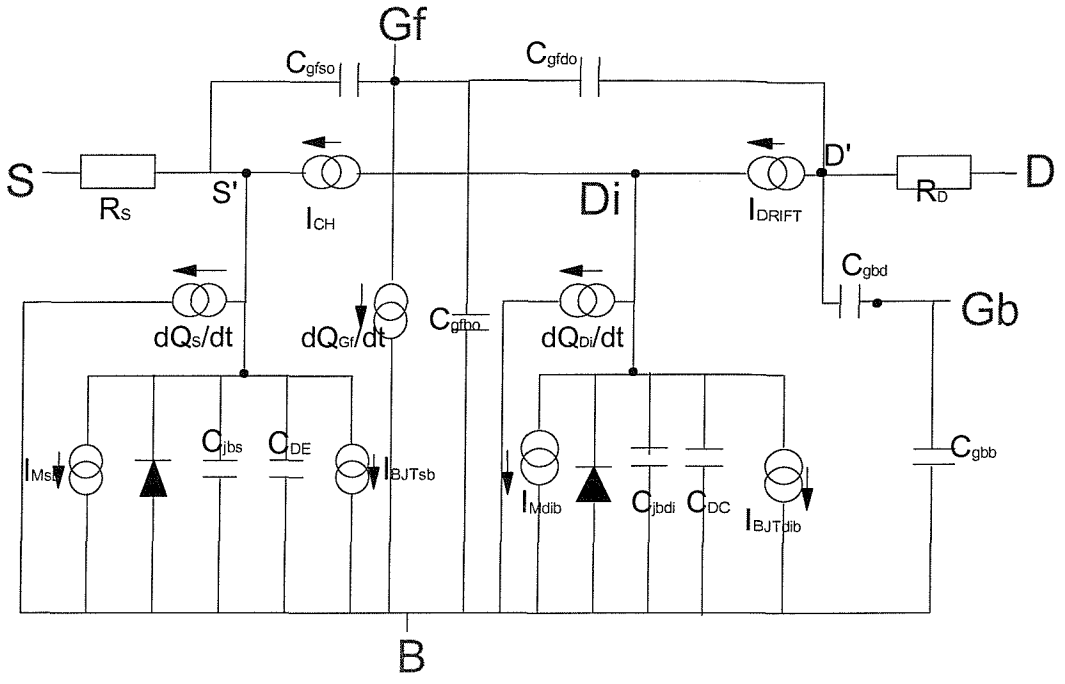


Figure 5.23: The compete large signal model

The SPICE AC analysis determines the perturbation response of the circuit by using linearised models for each non-linear element. The DC operating analysis provides the elements for these linearised models in the form of conductances and (trans)capacitances, which are converted to susceptances. These are then loaded respectively into the real and imaginary parts of the admittance matrix, and the network is solved as a linear set of equations. If all the current sources in Fig. 5.23 are replaced by their associated conductances and (trans)capacitances, the small signal equivalent circuit is obtained. It should be noted that the electro-thermal subcircuit is treated in the same way as its purely electrical counterpart; during an AC analysis the output of the thermal node provides the magnitude and phase of the small variations in device temperature with respect to the operating point equilibrium temperature.

5.12 Validation

To investigate the actual charge behaviour of LDMOST, measurements of the (trans) capacitances were performed.

5.12.1 Measurement Method and Test Structures

In general, the small signal current i_{ij} exited by a small signal potential v_j, while all other terminals are short-circuited is given by:

$$i_{ij} = Y_{ij}v_j = (G_{ij} + j\omega C_{ij})v_j \tag{5.91}$$

Hence in reality a small signal admittance is measured, which can be subsequently split into a conductance and a capacitance according to Eq. 5.91.

A possible measurement scheme to achieve this goal can be realised using a HP LCR impedance measurement system and Bias-Tees, configured as passive networks [18]. These networks are needed because the bias networks of most LCR meters are not designed to supply a substantial DC current, and they usually have a relatively high, current dependent internal resistance, which needs to be compensated for [19].

A much easier measurement solution to obtain the capacitances is a low frequency S-parameter analyser (HP8753), in combination with a Cascade probe station. With this set-up, two-port measurements can be performed and the 4 Y-parameters (Y_{11}, Y_{12}, Y_{21} and Y_{22}) can be calculated from the S-parameters [20]. So, for example, in the common source connection, C_{dgf}, C_{dd}, C_{gfd} and C_{gfgf} are derived from the imaginary part of the corresponding Y-parameters.

Specific test structures with a bondpad layout designed for the GSG (Ground-Signal-Ground) probes of the Cascade probe station were used for the capacitance measurements. The devices were all body-tied and we have used common source and common drain configurations, providing access to the following capacitances: C_{dgf}, C_{dd}, C_{gfd}, C_{gfgf}, C_{s^*gf}, $C_{s^*s^*}$ and C_{gfs^*}, where the subscript "s*" is used for the source and the body tied together. An open correction and a correction for the gate resistance were performed. As a verification of these corrections, the corrected C_{gfgf} was compared with the sum of C_{dgf} (obtained from the common source structure) and C_{s^*gf} (obtained from the common drain structure). C_{gfgf} is mainly affected by the open correction, while C_{dgf} and C_{s^*gf} are hardly influenced by the open correction, but undergo a significant change when the gate resistance is accounted for. Good agreement between C_{gfgf} and the sum of C_{dgf} and C_{s^*gf} confirmed the reliability of our correction method.

5.12.2 Results

An LV LDMOS device with $L_{tot} = 5$ μm and $L_{drov} = 3.2$ μm and an MV LDMOS device with $L_{tot} = 3$ μm and $L_{dr} = 5.7$ μm were selected for detailed study.

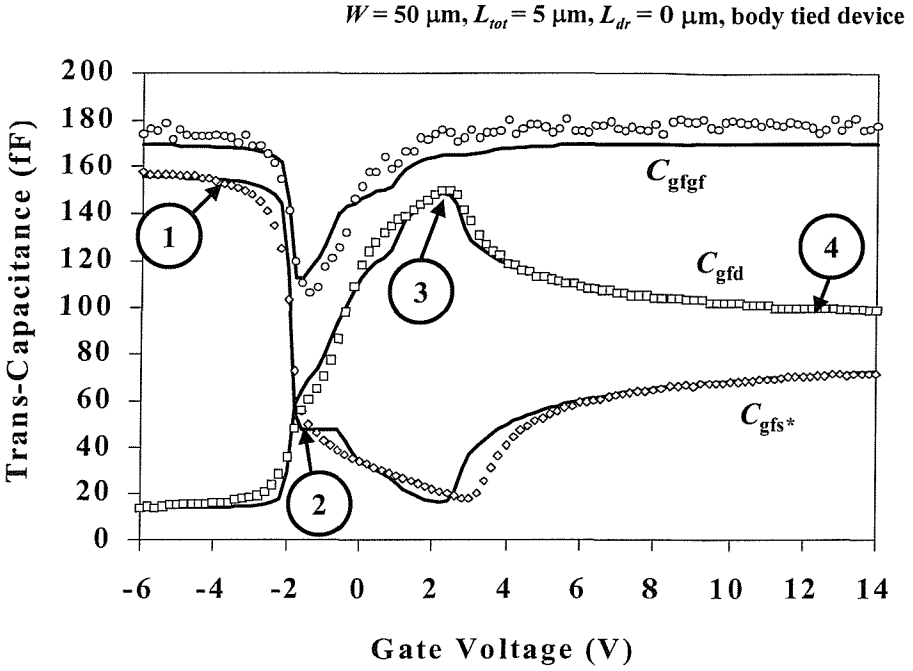


Figure 5.24: LV LDMOS $L_{\mathrm{drov}} = 3.2$ μm; simulated (full line) and measured C_{gfd}, C_{gfgf} and $C_{\mathrm{gfs*}}$ vs. V_{GfB} for $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V

Figs. 5.24 and 5.25 show C_{gfd}, C_{gfgf} and $C_{\mathrm{gfs*}}$ in terms of V_{GfB} for $V_{\mathrm{DS}} = 0$ V. The transition from subthreshold into inversion is well modelled for $V_{\mathrm{DS}} = 0$ V. For clarity the different regions are indicated. In region (1) a hole layer (due to accumulation in the MOSFET layer/inversion in the drift region) is present at the oxide surface, and hence the intrinsic gate body capacitance is given by $WL_{\mathrm{tot}}C_{\mathrm{of}}$. In region (2), the hole inversion layer has disappeared leaving the surface depleted, but the hole accumulation layer is still present. Around $V_{\mathrm{GfB}} = 1$ V, which is the value corresponding to the threshold voltage at the drain end of the MOS channel, electrons start to create an inversion layer at $y = L_{\mathrm{eff}}$, leading to an extra increase in C_{gfd}. The gate drain capacitance is at its maximum just before the source goes into inversion (region (3)), and then drops as the gate bias is further increased (region (4)).

The smoothing factors $k_{\mathrm{N_A}}/10$ and $k_{\mathrm{N_A}}/100$ used in Sec. C.9.1 in App. C were chosen in order to get a smooth transition from subthreshold into strong inversion. A larger $k_{\mathrm{N_A}}$ value causes a lower threshold voltage at the drain end, and hence L_{min} shifts from L_{eff} to 0 over a longer voltage interval ($V_{\mathrm{thL}} - V_{\mathrm{th0}}$). So the smaller $k_{\mathrm{N_A}}$ is, the faster L_{min} goes to 0, and the smaller the smoothing factors have to be. This is why the smoothing factors in the calculation of L_{min} were chosen to be dependent on k_{N_A}.

The higher the resistance of the drift region, the more the gate-drain transcapacitance drops with V_{GfB}, or in other words, the more channel charge is associated with the source. This is clear from Fig. 5.25 where the gate-drain capacitance reduces to approximately 20 % of the total gate capacitance.

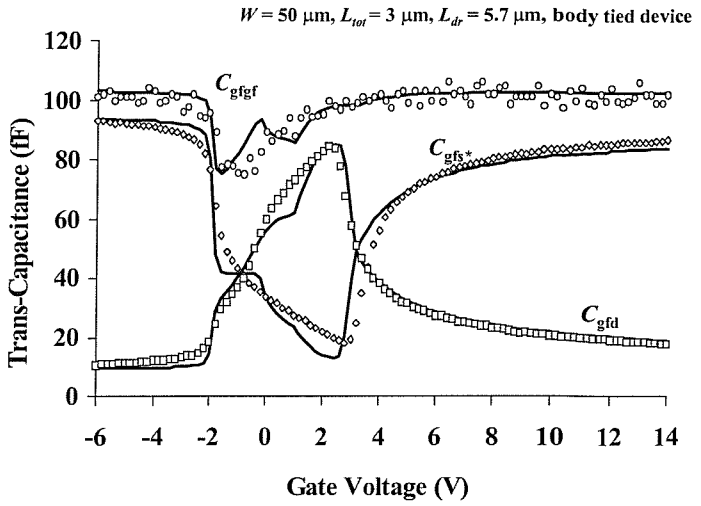


Figure 5.25: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu$m; simulated (full line) and measured C_{gfd}, C_{gfgf} and $C_{\mathrm{gfs*}}$ vs. V_{GfB} for $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V

Figs. 5.26 and 5.27 show C_{dd} and $C_{\mathrm{s*s*}}$ under the same bias conditions. It can be observed that the simulated curves follow the trends of the measured curves, but the deviation can become considerable. For the LV LDMOS the agreement is good below and a couple of volts above the threshold voltage, but for C_{dd} a difference of up to 50% is observed, just above the threshold. The reason is that Q_{Swdlim} (see Eq. 5.58), which is added to Q_{D}, changes from $Q_{\mathrm{Swd}}(V_{\mathrm{GfB}})$ to $Q_{\mathrm{Swd}}(V_{\mathrm{th0}})$ around the threshold, and this transition happens too fast in our model. For a better fit a detailed study of an appropriate function to describe this transition is needed.

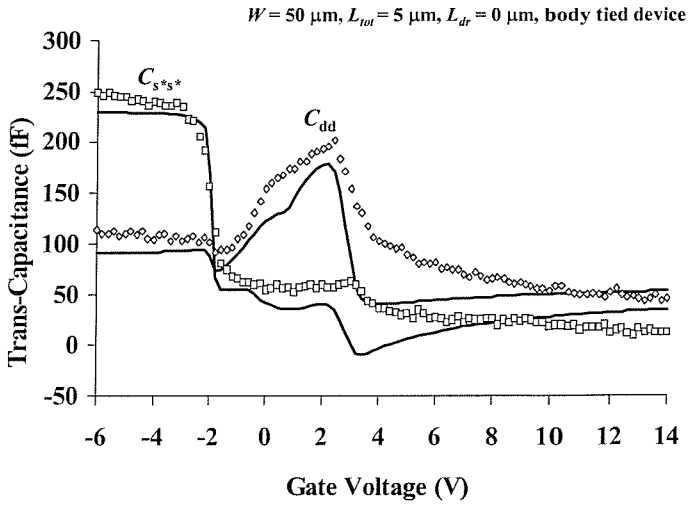


Figure 5.26: LV LDMOS $L_{\mathrm{drov}} = 3.2\ \mu$m; simulated (full line) and measured C_{dd} and $C_{\mathrm{s*s*}}$ vs. V_{GfB} for $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V

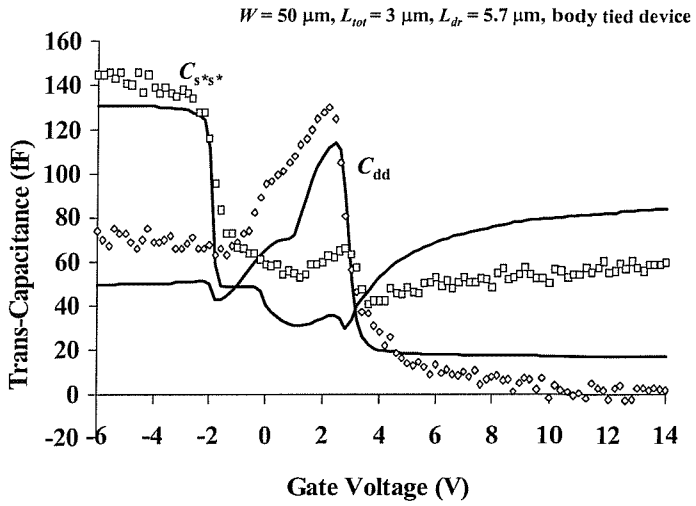


Figure 5.27: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu$m; simulated (full line) and measured C_{dd} and $C_{\mathrm{s^*s^*}}$ vs. V_{GfB} for $V_{\mathrm{DB}} = V_{\mathrm{SB}} = 0$ V

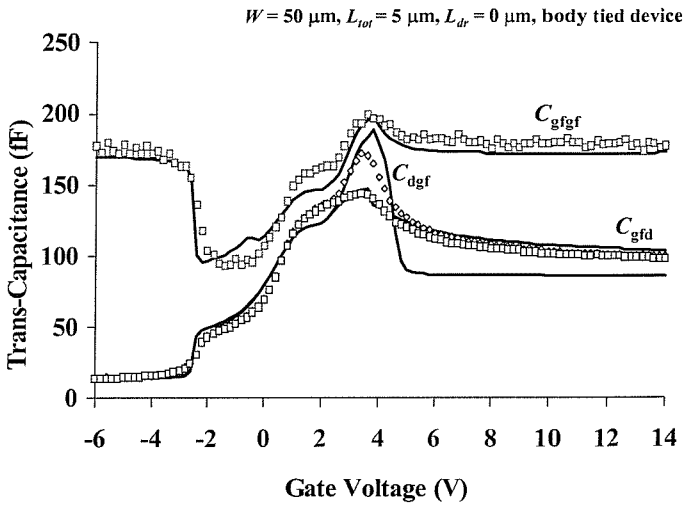


Figure 5.28: LV LDMOS $L_{\mathrm{drov}} = 3.2\ \mu$m; simulated (full line) and measured C_{gfd}, C_{gfgf} and C_{dgf} vs. V_{GfB} for $V_{\mathrm{DB}} = 1$ V, $V_{\mathrm{SB}} = 0$ V

Figs. 5.28 and 5.29 show the transition from subthreshold to inversion for $V_{\mathrm{DS}} = 1$ V. The gate-drain transcapacitance is well modelled for the two different structures. The drain-gate transcapacitance shows the correct trends, increasing above C_{gfd} when the device is in saturation, and decreasing sharply when entering the linear region. However, the simulated curve can overestimate the measured curve by 20%. This increase in C_{dgf} in the saturation region when $V_{GfD} > V_{\mathrm{FB}}^{\mathrm{dr}}$ is typical for LDMOS transistors. It can be explained by the strong dependence of ψ_{sLacc} on the gate voltage, leading to a strong dependance of the accumulation channel charge on the gate voltage, and hence causing an increased C_{dgf}. In Fig. 5.28 we note that the decrease of the simulated C_{dgf} is too steep. This can again be explained by the too abrupt conversion of Q_{Swdlim} around V_{th0} (see previous paragraph).

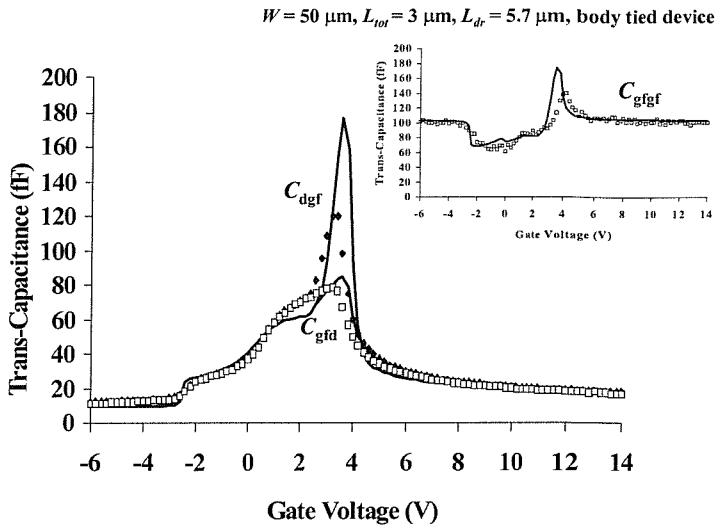


Figure 5.29: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu$m; simulated (full line) and measured C_{gfd}, C_{gfgf} and C_{dgf} vs. V_{GfB} for $V_{\mathrm{DB}} = 1$ V, $V_{\mathrm{SB}} = 0$ V

Figs. 5.30 and 5.31 show C_{dd} and C_{ss} under the same bias conditions ($V_{\mathrm{DB}} = 1$ V). It can be observed that the simulated curves follow the trends of the measured curves, but just as for the $V_{\mathrm{DB}} = 0$ V case, the deviation can become considerable. Again this is due to Q_{Swdlim}.

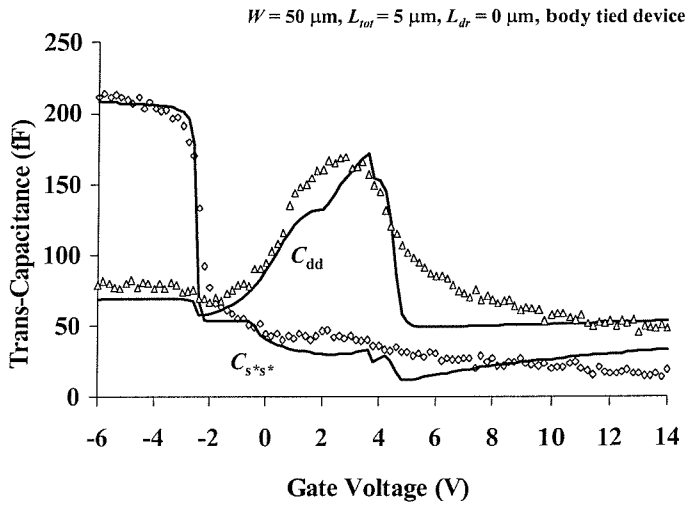


Figure 5.30: LV LDMOS $L_{\mathrm{drov}} = 3.2\ \mu$m; simulated (full line) and measured C_{dd} and $C_{\mathrm{s*s*}}$ vs. V_{GfB} for $V_{\mathrm{DB}} = 1$ V, $V_{\mathrm{SB}} = 0$ V

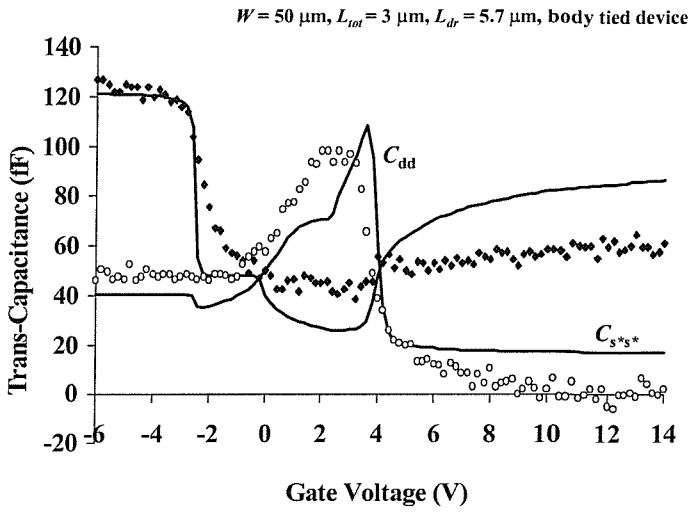


Figure 5.31: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu\mathrm{m}$; simulated (full line) and measured C_{dd} and $C_{\mathrm{s^*s^*}}$ vs. V_{GfB} for $V_{\mathrm{DB}} = 1$ V, $V_{\mathrm{SB}} = 0$ V

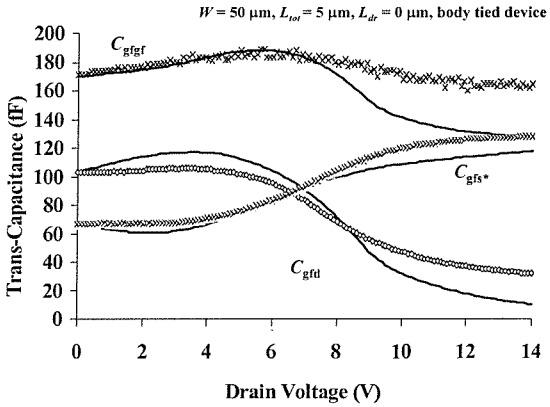


Figure 5.32: LV LDMOS $L_{\mathrm{drov}} = 3.2\ \mu\mathrm{m}$; simulated (full line) and measured C_{gfd} and $C_{\mathrm{gfs^*}}$ vs. V_{DB} for $V_{\mathrm{GfB}} = 9$ V, $V_{\mathrm{SB}} = 0$ V

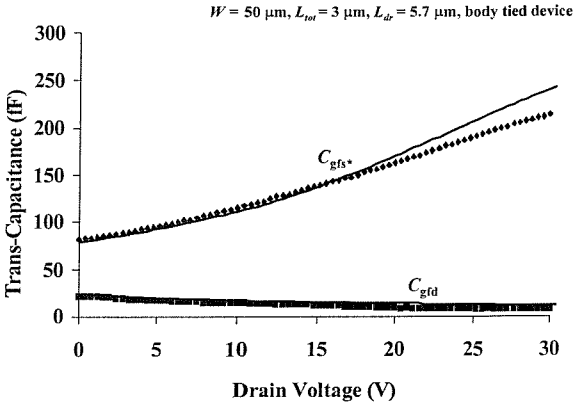


Figure 5.33: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu\mathrm{m}$; simulated (full line) and measured C_{gfd} and $C_{\mathrm{gfs^*}}$ vs. V_{DB} for $V_{\mathrm{GfB}} = 9$ V, $V_{\mathrm{SB}} = 0$ V

Figs. 5.32 and 5.33 illustrate $C_{\mathrm{gfs^*}}$, C_{gfgf} and C_{gfd} as a function of the drain bias. For the LV LDMOS good agreement is found for $C_{\mathrm{gfs^*}}$ and C_{gfd}, although the simulated curves both decrease too quickly compared with the measured values at high V_{DB}. In theory one would expect this decrease, because as V_{GfB} exceeds V_{DB}, the accumulated electrons should be driven away from the surface at the drain end. A possible explanation for the high measured values for C_{gfgf} at high V_{DB} could be the injection of electrons extending the accumulation layer in the drift region depletion layer for $V_{\mathrm{DB}} > V_{\mathrm{GfB}}$. For the MV LDMOS very good agreement was found up to 20 V. For high V_{DB} the simulated $C_{\mathrm{gfs^*}}$ mainly depends on the DC current dependence on V_{GfB}, and so the deviation between the measured and simulated $C_{\mathrm{gfs^*}}$ for high V_{DB} is mostly due to imperfections in the conductance model.

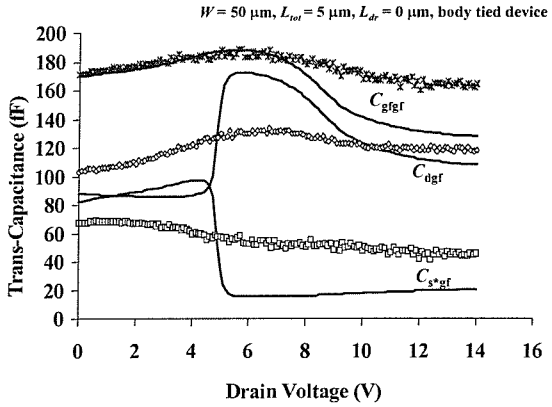


Figure 5.34: LV LDMOS $L_{\mathrm{drov}} = 3.2\ \mu$m; simulated (full line) and measured C_{dgf} and $C_{\mathrm{s^*gf}}$ vs. V_{DB} for $V_{\mathrm{GfB}} = 9$ V, $V_{\mathrm{SB}} = 0$ V

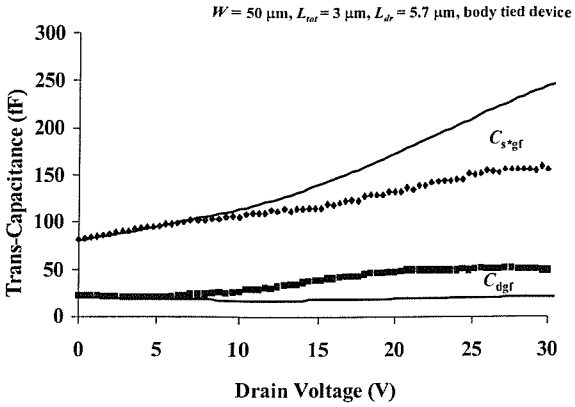


Figure 5.35: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu$m; simulated (full line) and measured C_{dgf} and $C_{\mathrm{s^*gf}}$ vs. V_{DB} for $V_{\mathrm{GfB}} = 9$ V, $V_{\mathrm{SB}} = 0$ V

In Figs. 5.34 and 5.35, $C_{\mathrm{s^*gf}}$ and C_{dgf} are plotted as a function of the drain bias. Fig. 5.34 shows the partitioning of C_{gfgf} between $C_{\mathrm{s^*gf}}$ and C_{dgf}. It can be seen that the charge associated with the drain as predicted by the modified Ward and Dutton scheme is underestimated by about 20% in the linear region and overestimated by about 20% when entering the saturation region. Our modified scheme does predict an increase in C_{dgf}, just as for the measured curve, but this increase is too abrupt and any further model development should focus on making this transition from triode into saturation more gradual. Again, for the MV LDMOS (see Fig. 5.35) the behaviour is mainly influenced by the DC current dependence on V_{DB} and V_{SB}, and the deviations can be mostly attributed to imperfections in the conductance model.

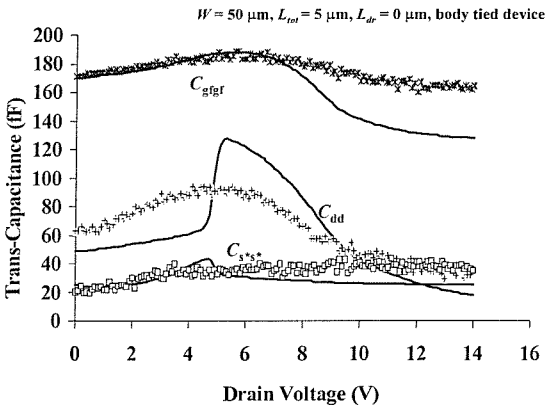


Figure 5.36: LV LDMOS $L_{\mathrm{drov}} = 3.2\ \mu$m; simulated (full line) and measured C_{dd} and $C_{\mathrm{s^*s^*}}$ vs. V_{DB} for $V_{\mathrm{GfB}} = 9$ V, $V_{\mathrm{SB}} = 0$ V

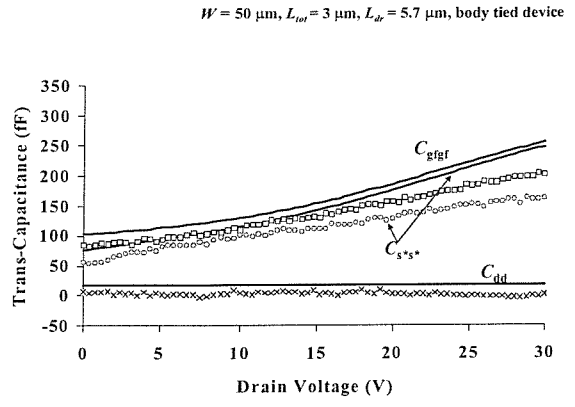


Figure 5.37: MV LDMOS device $L_{\mathrm{dr}} = 5.7\ \mu$m; simulated (full line) and measured C_{dd} and $C_{\mathrm{s^*s^*}}$ vs. V_{DB} for $V_{\mathrm{GfB}} = 9$ V, $V_{\mathrm{SB}} = 0$ V

Figs. 5.36 and 5.37 show $C_{s^*s^*}$ and C_{dd} as functions of the drain bias. Just as was the case for C_{dgf}, C_{dd} for the LV LDMOS is underestimated by about 20% in the linear region and overestimated by about 20% when entering the saturation region.

Generally, after having compared the different measured and simulated (trans)-capacitances, we found that the trends of the curves were mostly identical, and very good agreement was found for the $V_{DS} = 0$ V case. One should note as well that derivatives of charges were being compared and that even a small difference between measured and simulated charge can lead to significant differences when looking at the derivatives.

5.13 Summary

In this chapter, the complete SOI LDMOS charge model was set out. A promising new approach to deal with the charge partitioning in the LDMOS was presented. The model is based on a detailed study of the device physics and accounts for the influence of the lateral doping gradient in a compact way. The assumptions made were carefully considered and verified where necessary. The model simulations and measured characteristics for a range of geometries support the accuracy of the model; the use of a bias dependent length for the inversion channel gives very good transition for the gate charge dependence (C_{gfd}, C_{gfgf} and C_{gfs^*}) from subthreshold into the ON-state. However, the simulated transitions for the drain and source charge dependence (C_{dgf}, C_{dd}, C_{s^*gf} and $C_{s^*s^*}$) from sub-threshold into strong inversion, and from triode into saturation, do not describe the reality perfectly, and will require more work in the future.

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Chapter 6

Implementation of the Model in Spice3

6.1 Introduction

SPICE [1–3] is the industry standard for circuit design. A free version is available from Berkeley and different commercial versions can be bought from CAD vendors. At Southampton University a commercial variant, SIMetrix [4] was used for implementation.

As with Southampton's partially depleted SOI MOS model (STAG), the SOI LDMOS model has been implemented in SPICE3f5, which was the source code for the latest available version of Berkeley SPICE at the time. The model was subsequently adapted for use in the commercial simulator SIMetrix [4], which is based upon SPICE3e2. The SOI LDMOS and the STAG model both have 6 external nodes: the front gate, the source , the drain, the back gate, the body and the thermal node. One internal node had to be added for the SOI LDMOS model, which leads to an extra row and column in the SPICE sparse matrix [5].

The main issue of concern to circuit designers using SPICE or any other simulator is that of good convergence. Most convergence problems occur during a DC operating point analysis or during abrupt transitions in transient simulations. SPICE uses the Newton Raphson algorithm to solve a system of non-linear equations and this algorithm is very sensitive to discontinuities in the first order derivatives [6]. Often, the cause of non-convergence is a discontinuity in the first derivative of one of the currents or charges. Only the former are important in a DC operating point analysis. During a fast transient analysis, when the behaviour cannot be predicted due to discontinuities in the (trans)-capacitances or conductances, an error message "internal time step too small" is reported. Another reason for non-convergence can be the big excursions that the node voltages can make during the Newton Raphson iterations.

To meet the problems described in the previous paragraph, the SOI LDMOS model was formulated with continuous derivatives and node voltage limiting procedures. In order to get continuous derivatives over the whole range of bias conditions, smoothing functions

need to be used to realise continuous transitions from one operating region into another. In Sec. 6.2 an overview of different smoothing functions is given together with a discussion about the careful choice of such a function. Sec. 6.3 discusses the problems of over- and underflow and explains how they can be avoided. In the last section voltage limiting procedures are discussed, and in particular, the voltage limiting of the internal node for enhanced convergence is examined.

6.2 Smoothing functions

6.2.1 Overview

This section gives a critical comparison of different smoothing functions. We classified them in three categories: the "ln"-type , the "root"-type and the "power"-type smoothing functions. An important requirement for a smoothing function is that it has to be infinitely differentiable with respect to all its variables. This class of functions are referred to as C_∞ functions.

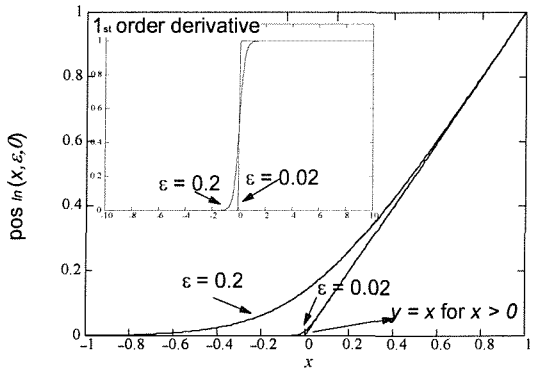

Figure 6.1: "ln"-type smoothing function to limit x positive, compared with $y = x$ for $x > 0$.

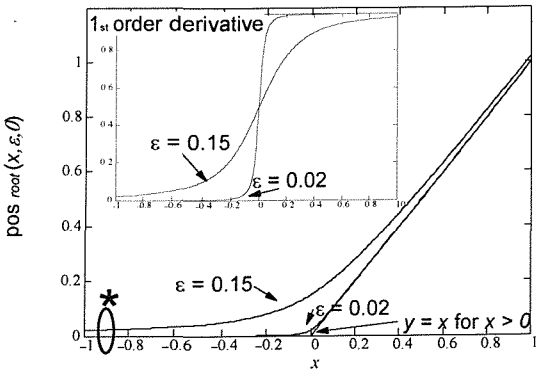

Figure 6.2: "root"-type to limit x positive, compared with $y = x$ for $x > 0$.

Let us now first look at two smoothing functions to limit a value x within a positive range. The "ln"-type function often used in STAG [6] is given by

$$\mathrm{pos}_{\ln}(x, \epsilon_1, \epsilon_2) = \begin{cases} \epsilon_1 \cdot \ln\left(1 + \exp\left(\frac{x}{\epsilon_1}\right)\right) + \epsilon_2 & \text{if } x < (\epsilon_1 \cdot M_{\exp}) \\ x + \epsilon_2 & \text{otherwise} \end{cases} \tag{6.1}$$

where clipping is performed to avoid overflow (see next section) and $M_{\exp}$ is the maximum argument allowable in an exponential function. The quantities ϵ_1 and ϵ_2 represent two small values, ϵ_2 being added to avoid overflow due to division by zero when $\mathrm{pos}_{\ln}$ is used in the denominator of an expression. This function is illustrated in Fig. 6.1. Another way

to limit x within a positive range is as follows (see Fig. 6.2):

$$\mathrm{pos}_{\mathrm{root}}(x,\epsilon) \quad = \quad 0.5\,x + 0.5\,\sqrt{x^2+4\epsilon^2}\,. \tag{6.2}$$

From the figures it can be seen that for a certain deviation at $x = 0$, the "ln"-type function returns faster to 0 for $x < 0$ or to x for $x > 0$ compared with the "root"-type function (see * in Fig. 6.2). This can be desirable in certain cases, where a smooth, fast transition is needed. The function $\mathrm{pos}_{\mathrm{ln}}$ has been implemented using the C function "log1p", which calculates $\ln(1+x)$ in a more accurate way than if the normal "log" function were to be used. The precision of the normal "log" function, as implemented in C, is only 10^{-9}. According to an error analysis, the "log1p" function has an error which is always less than 1 ulp (unit in the last place).

In the code the $\mathrm{pos}_{\mathrm{ln}}$ was preferred to the $\mathrm{pos}_{\mathrm{root}}$ function for the reason given above and also because of consistency, when two smoothing functions are used in the same transition region (see Sec. 6.2.2).

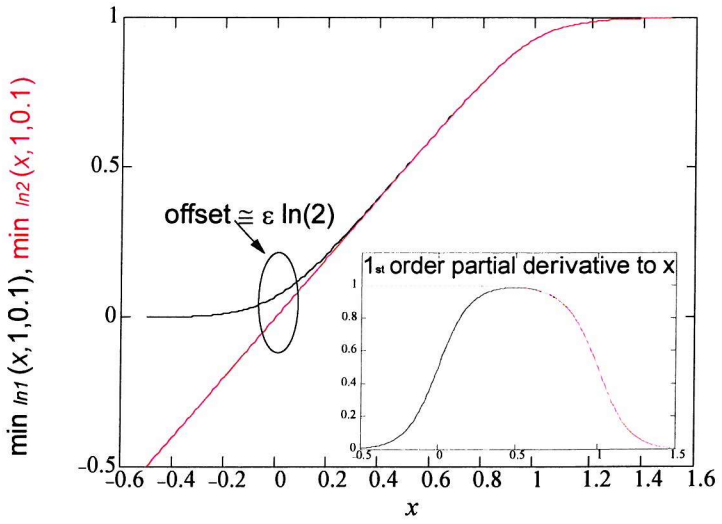

Figure 6.3: Comparison between $\mathrm{min}_{\mathrm{ln1}}$ and $\mathrm{min}_{\mathrm{ln2}}$ to model the smooth minimum of x and $y = 1$ ($\epsilon = 0.1$).

Another smoothing function which is frequently needed when modelling transistor behaviour is the minimum of two values x and y. Again an "ln"-type function can be used:

$$\mathrm{min}_{\mathrm{ln1}}(x,y,\epsilon) \quad = \quad \begin{cases} \epsilon \cdot \ln\left[1+\frac{\exp\left(\frac{x}{\epsilon}\right)}{1+\exp\left(\frac{x-y}{\epsilon}\right)}\right] & \text{if } x-y < (\epsilon \cdot M_{\mathrm{exp}}) \text{ and } x < (\epsilon \cdot M_{\mathrm{exp}}) \\ x - \epsilon \cdot \ln\left[1+\exp\left(\frac{x-y}{\epsilon}\right)\right] & \text{if } x-y < (\epsilon \cdot M_{\mathrm{exp}}) \text{ and } x > (\epsilon \cdot M_{\mathrm{exp}}) \\ y & \text{otherwise} \end{cases} \tag{6.3}$$

This function was to be found ideal to model the transition of the surface potential from subthreshold into the strong inversion region [6]. One inconvenience is the offset when

$x = 0$ and $y \gg \epsilon$: $\min_{\ln 1} \cong \epsilon \ln(2)$ instead of being 0. This can cause an undesired delayed transition in the modelled depletion layer charge, as will be explained in the next section. To avoid this offset, and if y is always larger than ϵ, the following "ln"-type function can be used instead:

$$\min_{\ln 2}(x, y, \epsilon) = \begin{cases} x + \epsilon \cdot \ln\left(\frac{\exp\left(-\frac{y}{\epsilon}\right)+1}{\exp\left(\frac{x-y}{\epsilon}\right)+1}\right) & \text{if } x - y < (\epsilon \cdot M_{\exp}) \\ y - \epsilon \cdot \ln\left(1 + \exp\left(-\frac{y}{\epsilon}\right)\right) & \text{otherwise.} \end{cases} \tag{6.4}$$

The two functions $\min_{\ln 1}$ and $\min_{\ln 2}$ are compared in Fig. 6.3 for $y = 1$. It can be observed that $\min_{\ln 2}(0, 1, 0.1) = 0$, while $\min_{\ln 1}(0, 1, 0.1)$ is roughly $\epsilon \ln(2)$.

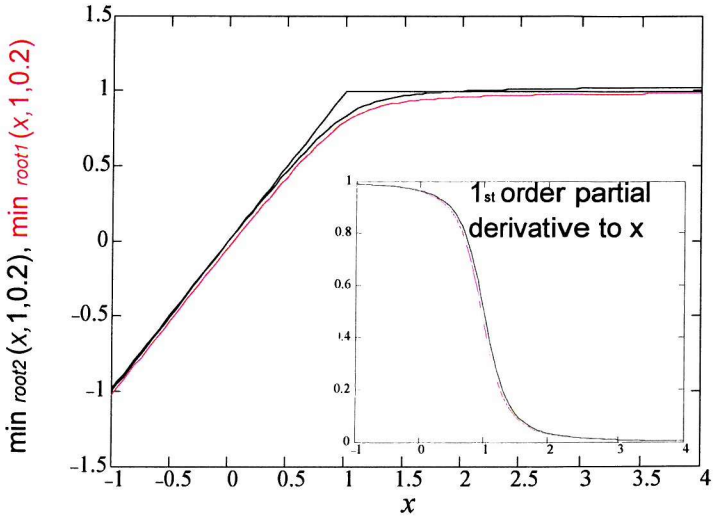

Figure 6.4: Comparison between $\min_{\text{root1}}$ and $\min_{\text{root2}}$ to model the smooth minimum of x and $y = 1$ ($\epsilon = 0.2$).

Let us now consider some "root"-type functions to calculate the smooth minimum of two values x and y. Two possible functions are given by [7]

$$min_{\text{root1}}(x, y, \epsilon) = x - 0.5 \cdot \left((x - y) + \sqrt{(x - y)^2 + 4\,\epsilon^2}\right) \tag{6.5}$$

$$min_{\text{root2}}(x, y, \epsilon) = 0.5\,x - 0.5 \cdot \left(\sqrt{(x - y)^2 + 4\,\epsilon^2} - \sqrt{y^2 + 4\,\epsilon^2}\right). \tag{6.6}$$

These two functions are compared in Fig. 6.4. Compared with the "ln"-type functions, it takes longer to settle to the minimum value before or after the transition point. One also has to take into account the slightly underestimated (min_{root1}) or overestimated (min_{root2}) minimum. Note as well that the second function can only be used for $y > 0$.

Finally, a third type of smoothing function can be considered [8]:

$$\min_{\text{power}}(x, y, m) = \frac{x \cdot y}{(x^{2m} + y^{2m})^{1/2m}} \tag{6.7}$$

where m is an integer fitting parameter and y a positive value. With this function x is

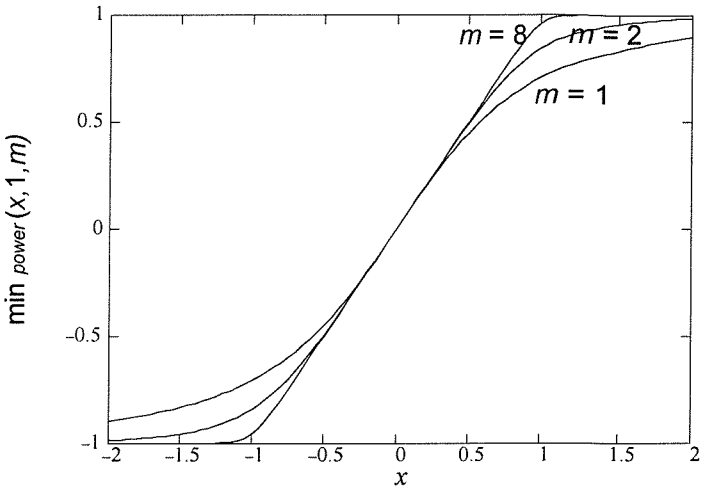

Figure 6.5: Illustration of the function $\min_{\text{power}}$ and to model the smooth minimum of x and $y = 1$ for different values of m.

limited to y for $x > 0$, and $-x$ is limited to $-y$ for $x < 0$. The big advantage of this function is that it is perfectly symmetrical and that the derivative with respect to x is 1 when $x = 0$. This function was to be found ideal for the limiting of V_{DS} to V_{Dsat} when a MOSFET converts from triode into saturation [8, 9]. We have also used this function for the same purpose in Sec. 4.2.5.

Depending on the physical behaviour of the transistor in a specific transition region, certain smoothing functions are preferred to others, and each of the three different types of smoothing function was used where appropriate.

6.2.2 Combining Different Smoothing Functions

To get a concrete idea of the problems which can arise when using smoothing functions, an example from the source code is examined in detail. Let us consider the capacitance $C_{\text{gfgf}} = dQ_{Gf}/dV_{\text{GfB}}$ when in the transition regime from depletion into accumulation in the drift region, with $V_{\text{DB}} = V_{\text{SB}} = 0$ V. Under these conditions, the expression for the depletion charge is given by

$$Q_{\text{Ddep}} = W\, C_{\text{of}}\, L_{\text{drov}}\, \gamma^{\text{fdr}} \sqrt{\psi_{\text{s}}^{\text{dr}}} \tag{6.8}$$

with

$$\psi_{\text{s}}^{\text{dr}} = \min_{\ln*}(\psi_{\text{ss}}^{\text{dr}}, \psi_{\text{si}}^{\text{dr}}, \phi_{\text{t}}) \tag{6.9}$$

where

$$\psi_{\text{si}}^{\text{dr}} = 2\,\phi_{\text{Fdr}} \tag{6.10}$$

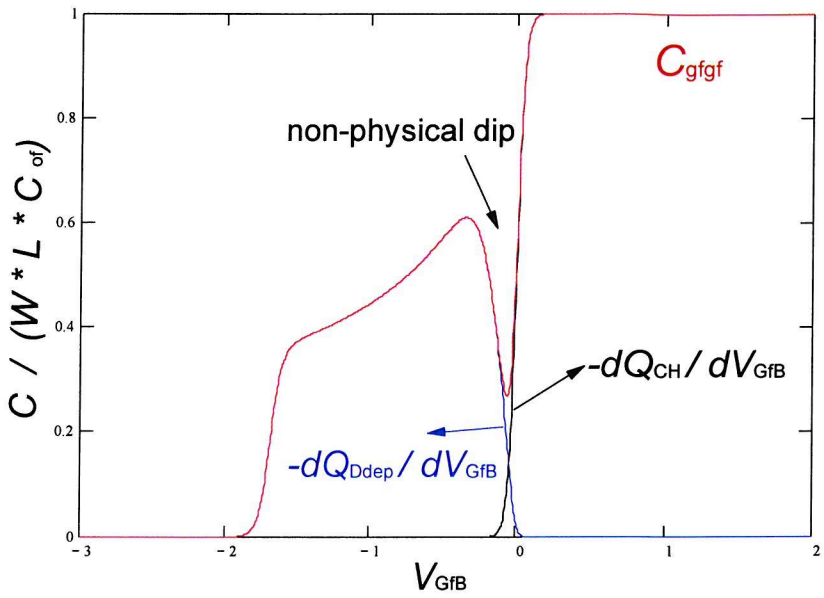

Figure 6.6: C_{gfgf} in terms of V_{GfB} during the transition from depletion into accumulation in the drift region using $\min_{\mathrm{ln1}}$.

$$\psi_{\mathrm{ss}}^{\mathrm{dr}} = \left(-\frac{\gamma^{\mathrm{fdr}}}{2} + \sqrt{\frac{(\gamma^{\mathrm{fdr}})^2}{4} + V_{\mathrm{gy-}}^{\mathrm{dr}}}\right)^2 \tag{6.11}$$

$$V_{\mathrm{gy-}}^{\mathrm{dr}} = \mathrm{pos}_{\mathrm{ln}}(-V_{\mathrm{GfB}} + V_{\mathrm{FB}}^{\mathrm{dr}}, \phi_{\mathrm{t}}) \,. \tag{6.12}$$

The expression for the accumulation charge is

$$Q_{\mathrm{CHacc}} = W\, C_{\mathrm{of}}\, L_{\mathrm{drov}}\, V_{\mathrm{gy+}}^{\mathrm{dr}} \tag{6.13}$$

where

$$V_{\mathrm{gy+}}^{\mathrm{dr}} = \mathrm{pos}_{\mathrm{ln}}(V_{\mathrm{GfB}} - V_{\mathrm{FB}}^{\mathrm{dr}}, \phi_{\mathrm{t}}) \,. \tag{6.14}$$

And the total gate charge is given by

$$Q_{\mathrm{Gf}} = -(Q_{\mathrm{Ddep}} + Q_{\mathrm{CHacc}}) \,. \tag{6.15}$$

In Figs. 6.6 and 6.7 the quantity C_{gfgf} is plotted in terms of the gate voltage using two different smoothing functions in Eq. 6.9.

In the first figure $\min_{\mathrm{ln1}}$ is used in Eq. 6.9. This clearly results in a non-physical dip in the C_{gfgf} curve. This is due to the fact that the quantity $\psi_{\mathrm{s}}^{\mathrm{dr}}$ is not exactly $\psi_{\mathrm{ss}}^{\mathrm{dr}}$ when $V_{\mathrm{gy-}}^{\mathrm{dr}}$ goes to 0 (and hence $\psi_{\mathrm{ss}}^{\mathrm{dr}}$ goes to 0), but is approximately $\phi_{\mathrm{t}} ln(2)$ too big, and hence the derivative of Q_{Ddep} lowers too quickly.

In the second figure $\min_{\mathrm{ln2}}$ is used in Eq. 6.9. Now the decrease in $-dQ_{\mathrm{Ddep}}/dV_{\mathrm{GfB}}$ happens at exactly the right gate voltage and the non-physical dip has disappeared. This

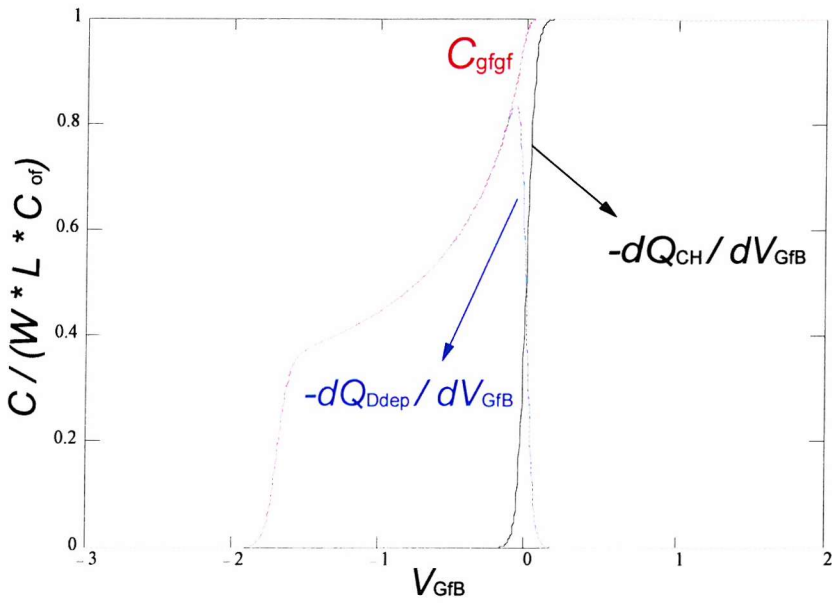

Figure 6.7: C_{gfgf} in terms of V_{GfB} during the transition from depletion into accumulation in the drift region using $\min_{\ln 2}$.

shows how important it is to chose the right smoothing function for certain transitions.

6.3 Underflow, Overflow and Accuracy Problems

In SPICE the double precision floating point format is used, which limits the minimum and maximum values that can be represented. Special care has to be taken when using exponential functions or when big values are divided by very small values.

To avoid overflow when using an exponential function, the argument has to be limited. The maximum value that can be represented by a "double" is $1.7 \cdot 10^{308}$, so the maximum allowable argument of the exponential function is $M_{\text{exp}} = ln(1.7 \cdot 10^{308}) \cong 709$. It is advisable to check the argument of any exponential, and to use the limit of the expression when M_{exp} is exceeded. This explains why the clipping done in Eqs. 6.1, 6.3 and 6.4 was necessary. This is especially important for high voltage applications where $\exp(x/\phi_{\text{t}})$ can easily become very large. Also, during Newton Raphson iterations some node voltages can significantly exceed the supply voltage, and if no contingency measures were taken, this would definitely result in overflow. Note that the clipping done in the above-mentioned smoothing functions is as close to C_∞ as machine code allows.

Underflow is not usually a problem as such, but becomes a problem when it leads to overflow in certain expressions. The most straightforward example is in division: consider $1/x$ when x goes to 0 due to underflow. The quantity $1/x$ now becomes infinite leading to a "NaN" (Not a Number) error message. Another example is the quantity $\ln(x)$ when x underflows, and $\ln(x)$ tends to negative infinity. To avoid this sort of problem, it is common practice to add a small value to variables appearing in the denominator of a

division. This explains the term ϵ_2 in Eq. 6.1. If x is a voltage, the value of 10^{-25} is chosen for ϵ_2 because this is well below any measurable potential. Note as well the term $4\epsilon^2$ in the root expressions of Eqs. 6.2, 6.5 and 6.6. Firstly, this is necessary to make the expressions continuous, but furthermore when differentiating these expressions, the root term appears in the denominator and could cause overflow if ϵ was chosen as zero.

Another consequence of the limited precision of the variables is that some results are not guaranteed to be accurate. When, for example, a long expression appears as the argument of a square root or of a "ln" function, care has to be taken that this expression cannot become negative. Even if this expression can never become smaller than or equal to zero analytically, numerical problems can still result in a negative value. To avoid these numerical anomalies, clipping has to be introduced where inaccurate results are expected, or else the evaluation of certain expressions can be split into parts. To visualise this solution, let us consider a specific example where the precision is improved by careful splitting of a certain expression:

$$C = \frac{A}{A'} \cdot \frac{B}{B'} \tag{6.16}$$

where A and A' are both very big and of the same order of magnitude, as are B and B'. Let us now consider the following three ways of evaluating this expression, as in Eqs. 6.17, 6.18 and 6.19. The expressions between brackets are evaluated first and stored before performing the evaluation of the total expression, C:

$$C = \left(\frac{A}{A'}\right) \cdot \left(\frac{B}{B'}\right) \tag{6.17}$$

$$= \left(\frac{1}{A'B'}\right) \cdot \left(AB\right) \tag{6.18}$$

$$= \left(\frac{AB}{A'}\right) \cdot \left(\frac{1}{B'}\right) \tag{6.19}$$

Eq. 6.18 can lead to underflow in the first factor and overflow in the second, yielding in an inaccurate result. Eq. 6.19 is a slightly better choice, but can still become inaccurate if B' is very big. Eq. 6.17 is definitely the best choice for a numerically exact result.

6.4 Voltage Limiting Scheme

In the STAG model it was found that the Newton Raphson algorithm allows large excursions of the body voltage (when used under floating body conditions) and of ΔT, the temperature rise due to self-heating. To avoid these non-physical values, and to speed up convergence, several measures were taken [6]. The solution for the body voltage consists of limiting the diode potentials in both positive and negative going directions. To avoid the large ΔT excursions, limiting of ΔT is performed each iteration in a similar fashion to the p-n junction limiting.

In the SOI LDMOS model, an extra internal node was introduced and this node can

also experience significant excursions of the internal drain voltage if no limiting procedures are used. A solution to this problem in the SOI LDMOS model is to limit V_{DiS} and V_{DDi} each iteration. A simple algorithm, which is commonly used for the limiting of V_{DS} in a standard MOSFET model, was introduced for this purpose. The value saved from the previous iteration is referred to as V_0, $\widehat{V}$ is defined as the value predicted during the Newton Raphson iteration and V^1 is the limited value, which is going to be used in the next iteration. For a positive value from the previous iteration ($V_0 > 0$) the following algorithm is executed at every iteration:

$$V^1 = \begin{cases} 3V_0 + 2 & \widehat{V} > 3V_0 + 2 \text{ and } V_0 \geq 3.5 \\ 2 & 2 > \widehat{V} \text{ and } V_0 \geq 3.5 \\ -1 \cdot 10^{-12} & \widehat{V} < -1 \cdot 10^{-12} \text{ and } V_0 < 3.5 \\ 4 & \widehat{V} > 4 \text{ and } V_0 < 3.5 \\ \widehat{V} & \text{otherwise.} \end{cases}$$

If V_0 is negative ($V_0 < 0$) the algorithm is executed with $-V_0$. This algorithm is performed first on V_{DiS}. Then the value of V_{DDi} is recalculated as $V_{\mathrm{DS}} - V^1_{\mathrm{DiS}}$, and the same algorithm is then performed on the new V_{DDi}. The only difference from the algorithm used in normal MOSFETs is the numerical values that are used. It was found that the internal drain voltage can go first positive and then negative in successive iterations before finally converging to zero, thus slowing down convergence. With the chosen limiting scheme V_{DiS} can only jump from a positive value to a very small negative value ($-1 \cdot 10^{-12}$), or vice versa for a negative value of V_{DiS}. Furthermore, supply voltages are usually quite large, so the drain voltage should be able to rise fairly quickly. This is why the other numerical quantities in the algorithm should not be chosen to be too small.

6.5 Summary

In this chapter we have treated the numerical bottlenecks and particularities which were encountered during the implementation and testing phase of the model in a commercial SPICE simulator (SIMetrix).

Easy debugging was possible due to Borland C++'s integrated debugger [10], which allows running of the simulator within the Borland debugging environment, and allows placing of breakpoints where necessary or when a C++ exception is caught or thrown.

Various clipping solutions to avoid over- and underflow were discussed and a new voltage limiting scheme for the internal drain voltage was presented. Furthermore, techniques to improve the precision of certain evaluations were explained. These measures have led to a very robust SOI LDMOS model, which converges easily without the need for node setting.

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Chapter 7

Model Evaluation

7.1 Introduction

In this chapter the model is tested extensively in the circuit simulator SPICE [1], in terms of its suitability for simulating single device characteristics and circuits. DC and AC single device characteristics were already verified against measurements in Chapters 4 and 5 respectively. In this chapter the model is tested qualitatively and its ability to simulate circuits is demonstrated.

In Sec. 7.2 single device characteristics are analysed qualitatively using a slightly adapted set of the SEMATECH tests [2]. The SEMATECH evaluation consists of a set of tests which were originally designed for bulk MOSFET devices. It checks for any weaknesses, discontinuities or non-physical behaviour in the model.

To test the circuit simulation performance, two typical high voltage circuits were designed and fabricated using the model parameters extracted in Chapters 4 and 5. The model predictions are compared with measurements in Sec. 7.3.

7.2 Qualitative Tests

7.2.1 Introduction

The SEMATECH evaluation consists of a set of tests which are aimed at showing up any weaknesses or discontinuities in the model. The transitions between operating regions are of special concern, because any discontinuities can cause convergence problems in a circuit simulator. The tests also try to trace non-physical model behaviour in static, transient or small signal analyses. Simple visual checks and more sophisticated numerical techniques are used to detect discontinuities or non-physical kinks in the model. These tests were originally designed for bulk MOSFET and later extended to SOI MOSFET transistors. In this section the SEMATECH tests are adapted and used for SOI LDMOS transistors as appropriate.

The tests are performed on four different devices, two with field oxide and two without field oxide ($L_{\mathrm{dr}} = 0$). This set of devices is illustrated in Table 7.1. Parameter set 1

consists of the values extracted in Chapter 4 for the MV LDMOS. Parameter set 2 is not extracted, but describes a typical medium voltage process, with thinner gate oxides and higher drift region doping concentrations compared with Parameter set 1. We have added the tests with the second parameter set to ensure that our model is also robust, and that the smoothness of the simulated characteristics is not affected when choosing a completely different realistic parameter set. These two parameter sets can be found in App. F. In this section the interesting results for devices 1 and 2 will be discussed. The interested reader can find the full set of SEMATECH tests for all four devices in App. F.

Device	L_{dr}	Parameter Set
1	0	1
2	4 μm	1
3	0	2
4	1 μm	2

Table 7.1: *Overview of devices evaluated by the SEMATECH tests.*

7.2.2 DC tests

The Output Characteristics

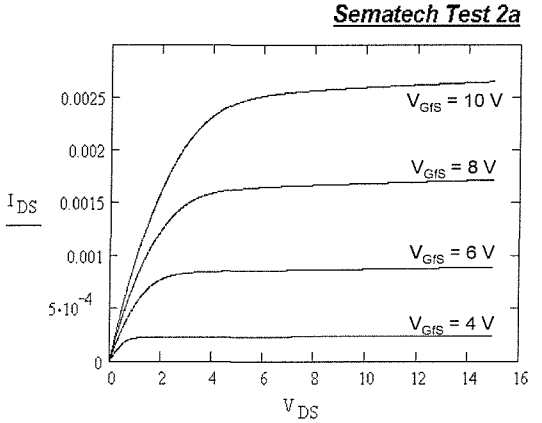

Figure 7.1: Test 2a: fine resolution plot of I_{D} vs. V_{DS} (Device 1).

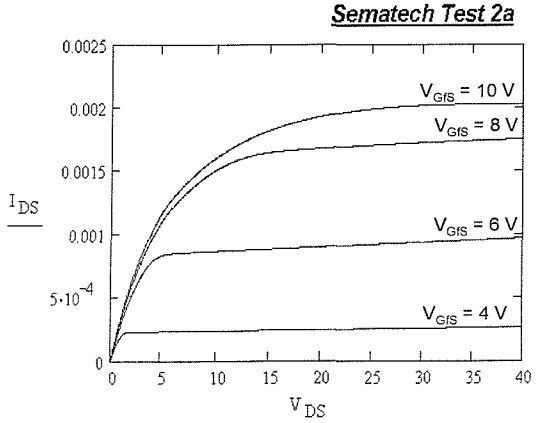

Figure 7.2: Test 2a: fine resolution plot of I_{D} vs. V_{DS} (Device 2).

In Test 2a the output characteristics are plotted using a fine grid for V_{DS} (Figs. 7.1 and 7.2). Test 2b considers the output conductance, obtained as the derivative of I_{D} vs. V_{DS} from Test 2a (Figs. 7.3 and 7.4). Both tests require a visual check to investigate the smoothness and continuity of the transition from the linear into the saturation region. Because Test 2b requires the output conductance to be plotted on a log-linear scale, self-heating was not included in the simulation. A non-zero thermal resistance would mean a negative slope in the output characteristics for high V_{DS}, leading to a negative value for

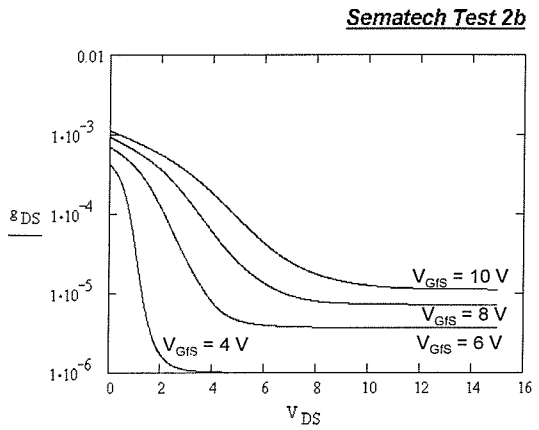

Figure 7.3: Test 2b: fine resolution plot of g_o vs. V_{DS} (Device 1).

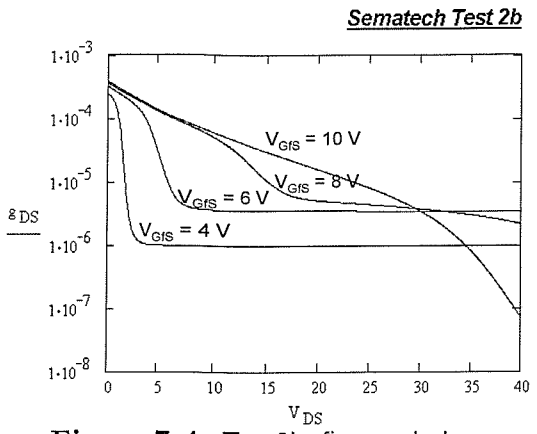

Figure 7.4: Test 2b: fine resolution plot of g_o vs. V_{DS} (Device 2).

the output conductance, which cannot be plotted on a log scale. The effect of self-heating on the output characteristics will be looked at in Tests 11 and 12.

It is clearly visible that the model behaves well in both tests. Note the lower value of the output conductance for the LDMOS with field oxide at high currents (see Fig. 7.4). The reason for this is that channel length modulation is almost negligible because the main part of V_{DS} drops over the drift region, which is saturated by pinch-off at high V_{DS} and V_{GfS}.

The Subthreshold Characteristics

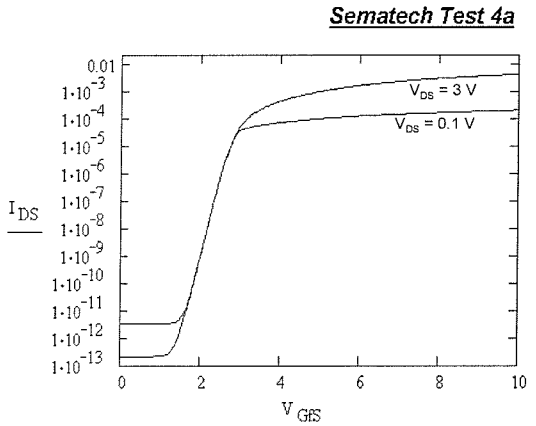

Figure 7.5: Test 4a: fine resolution plot (step is 0.04 V) of I_D vs. V_{GfS} for $V_{DS} = 0.1$ V and 3 V.

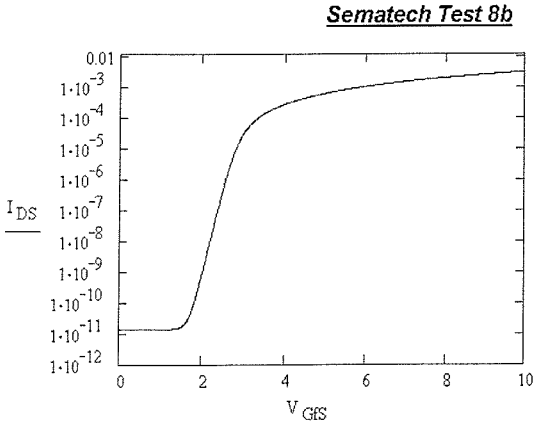

Figure 7.6: Test 8b: very fine resolution plot of I_D vs. V_{GfS} for $V_{DS} = 14$ V.

In tests 3, 4, 8 and 9 the transition from subthreshold into strong inversion is investigated. Again this has to happen in a smooth manner, and must provide physical modelling of the moderate inversion region. The full set of results for devices 1 to 4 can be found in

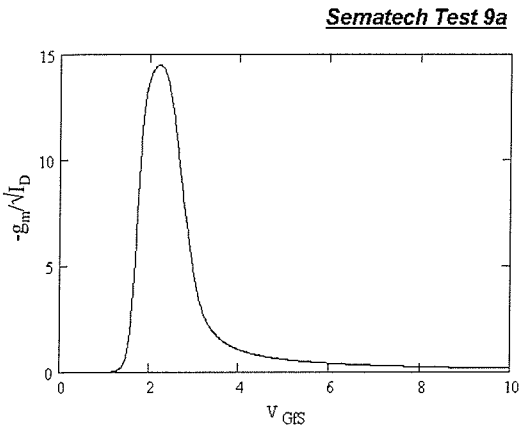

Figure 7.7: Test 9a: very fine resolution plot (step is 0.01V) of g_m/I_D vs. V_{GfS} for $V_{DS} = 14$ V.

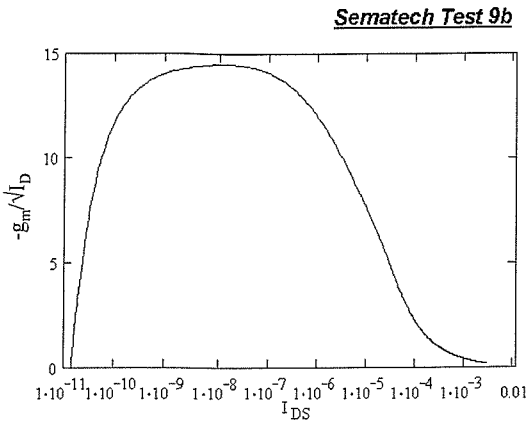

Figure 7.8: Test 9b: very fine resolution plot of g_m/I_D vs. I_D for $V_{DS} = 14$ V.

App. F, and in this section only the most interesting results for Device 1 are considered. Furthermore, the effect of the field oxide on the subthreshold characteristics is almost negligible, and hence the results for devices 1 and 2 are almost identical.

Test 4a (Fig. 7.5) plots the subthreshold current in terms of V_{GfS} for two different values of V_{DS}. Test 8b (Fig. 7.6) repeats this plot for $V_{DS} = V_{DD}$, but with a grid that is four times finer. For both tests the simulated current is smooth and continuous as required, and behaves in a physically correct manner, predicting the same shape for the subthreshold characteristics as for ordinary MOSFET devices.

Test 9 examines the ratio of g_m over I_D, which is a scaling independent measure of the device gain. Test 9a (Fig. 7.7) plots g_m/I_D vs. V_{GfS}, and Test 9b (Fig. 7.8) vs. I_D. Again the curves are smooth and continuous.

Geometry Tests

Tests 6 and 7 check the geometry dependence of respectively I_D and V_{DS} for a diode connected transistor. For MOSFET devices this means plotting I_D and V_{DS} in terms of L, and g_m/I_D and V_{DS} in terms of $\sqrt{W}$. For the LDMOS an extra test verifying the dependence on L_{dr} was added.

The width dependence in an LDMOS is very similar to an ordinary MOSFET device and we refer to test 7a and 7b in App. F for the results. The length dependence for an LV LDMOST with $L_{dr} = 0$ (Devices 1 and 3) shows very similar behaviour to an ordinary MOSFET. However, for devices 2 and 4 the drift region modifies the length dependence; for very high drain biases the drift region is saturated, and the channel length hardly influences the current. This is illustrated in Fig. 7.9. Note as well the continuity of the curves. In Fig. 7.10 the current is plotted in terms of L_{dr}. Here an inverse effect can be observed. For high drain voltages the drift length influences the current quite strongly, while for low V_{DS} values the dependence on L_{dr} is almost nil. Again the results are smooth

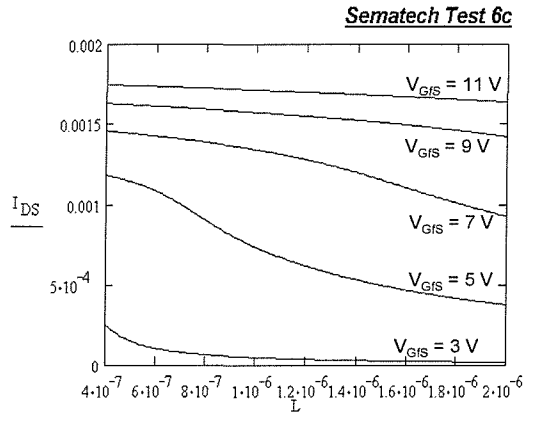

Figure 7.9: Test 6c: I_D vs. L for diode connected LDMOS (Device 2).

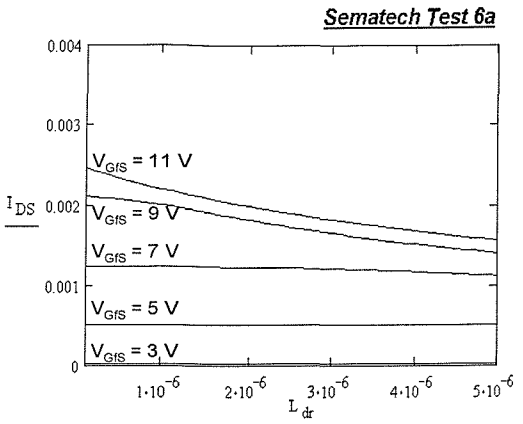

Figure 7.10: Test 6a: I_D vs. L_{dr} for diode connected LDMOS (Device 2).

and continuous. Note that in practice L and L_{dr} in an LDMOS transistor are fixed and should not be varied by the circuit designer. However, a good model must ensure the continuity of the current plotted against any parameter within its valid range.

Continuity and Gummel Tests

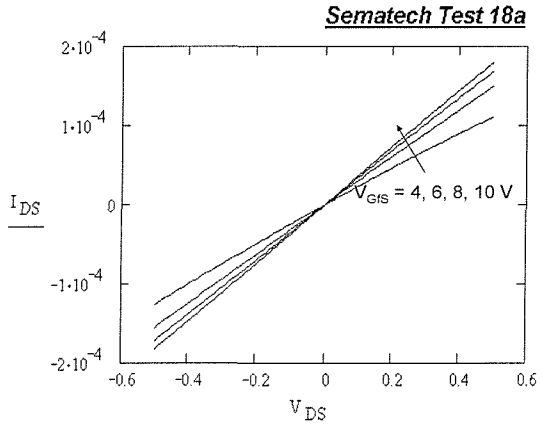

Figure 7.11: Test 18a: I_D vs. V_{DS} around $V_{DS} = 0$ (Device 2).

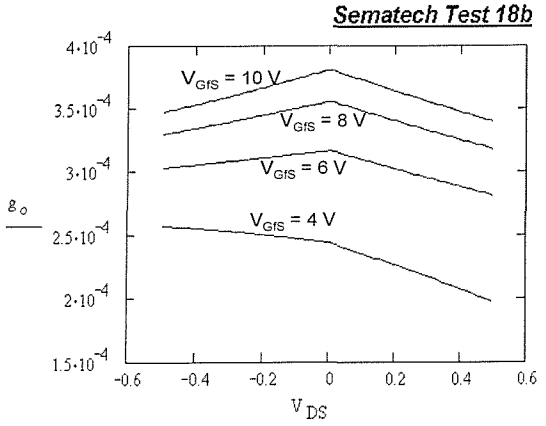

Figure 7.12: Test 18b: g_o vs. V_{DS} around $V_{DS} = 0$ (Device 2).

The continuity test is an adapted version of the Gummel symmetry test, which verifies the symmetry of the drain current around $V_{DS} = 0$, with the body connected to the source for $V_{DS} > 0$ and to the drain for $V_{DS} < 0$. This test is very useful for a MOSFET, because this device is usually perfectly symmetrical. An LDMOS device, on the contrary, is asymmetrical and renders the test inappropriate. However, it is important to have a continuous current around $V_{DS} = 0$, and Test 18 checks this behaviour with the body connected to the source. The results are illustrated in Figs. 7.11 and 7.12 for the current

and the output conductance respectively. The curves do not show any irregularities and the current passes smoothly through $V_{DS} = 0$.

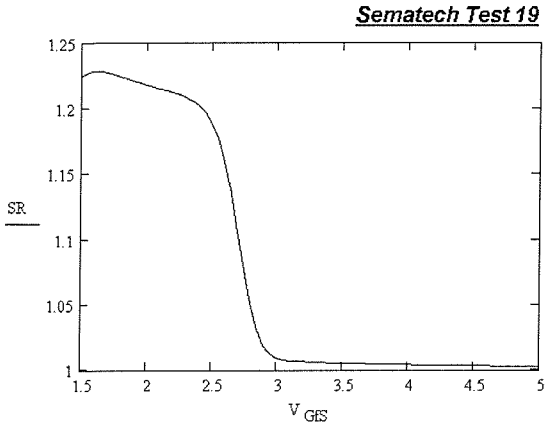

Figure 7.13: Test 19: Gummel slope ratio test for device 1.

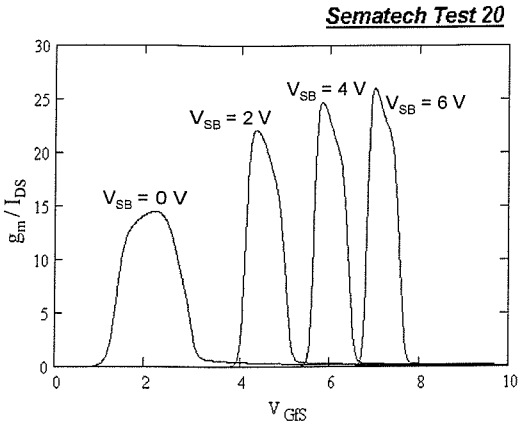

Figure 7.14: Test 20: Gummel tree-top test for device 1.

The Gummel slope ratio and tree-top tests are very sensitive to any non-physical behaviour and form a fundamental model verification. The Gummel slope ratio test looks at the asymptotic behaviour of the model with V_{DB} variation. The slope ratio (SR) is defined as

$$\mathrm{SR} = \frac{(I_1 + I_2)(V_1 - V_2)}{(I_1 - I_2)(V_1 + V_2)} \tag{7.1}$$

with V_1 and V_2 being two small values for V_{DB}, I_1 and I_2 the corresponding drain currents and $V_{SB} = 0$. For values much higher than the threshold voltage, the slope ratio should tend to 1, while in subthreshold, it should asymptotically approach a value determined by the temperature and the values of V_1 and V_2. This is shown in Fig. 7.13 for the values $V_1 = 0.011$ V, $V_2 = 0.01$ V, and $T = 25$ °C. It can be observed that the slope ratio moves smoothly, and is free of glitches between the two asymptotes. The use of the smoothing function for V_{DS}, as described in Sec. 4.2.5, has removed the non-physical hump observed in the moderate inversion region in the Southampton SOI MOSFET (STAG) model [3]. This hump was attributed to an error in the surface potential approximation in this region.

The Gummel tree-top test studies the asymptotic behaviour of the model with V_{GfS} variation. The quantity g_m/I_D is plotted against V_{GfS} for different values of V_{SB} (Fig. 7.14) and moves smoothly from subthreshold into strong inversion, as required.

Self-Heating Characteristics (Tests 11 and 12)

Self-heating gives rise to a reduction in the drain current and can become particularly important at high power levels. In the LDMOS output characteristics this effect typically leads to a negative output conductance. In Fig. 7.15 the output characteristics are simulated with and without self-heating.

As explained in Sec. 4.4, self-heating is a dynamic phenomenon; at high frequencies

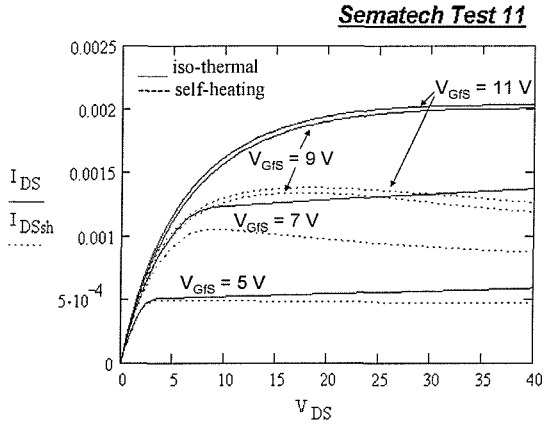

Figure 7.15: Test 11: influence of static self-heating on the output characteristics (Device 2).

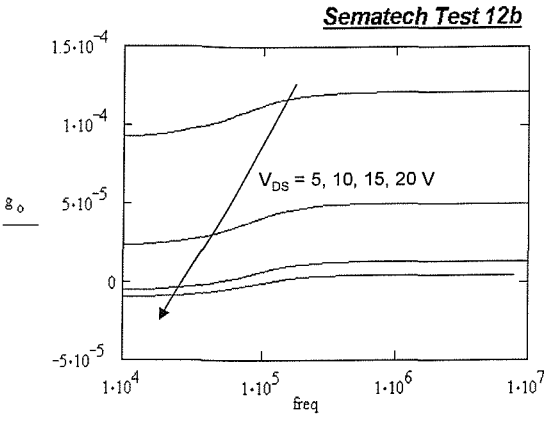

Figure 7.16: Test 12b: influence of dynamic self-heating. Output conductance vs. frequency for V_{GfS} = 8 V (Device 2).

the device temperature can no longer follow the power dissipation, and hence the self-heating effects are greatly reduced. Fig. 7.16 shows the output conductance in terms of the frequency. A smooth increase with frequency is observed around the thermal cut-off frequency ($\cong 1/(R_T C_T)$). For high V_{DS} values, the output conductance moves from a negative value for low frequencies to a positive value when the self-heating is filtered out.

Body Resistance Test (Test 13)

In LDMOS technology it is common to place the body contact parallel to the source contact. This can lead to a relatively high body resistance R_{body}, which is formed by the pinched region underneath the source junction. This body resistance, together with the impact ionisation back gate current, can switch on the lateral parasitic bipolar transistor, and this can determine the safe operating area of the LV and MV LDMOS [4]. This effect is enhanced by self-heating; when the device heats up the effective body source voltage necessary to trigger the parasitic BJT becomes smaller. Furthermore, because the BJT has a positive temperature dependent factor in the expression for the collector current, this effect can lead to early breakdown of the device.

In Fig. 7.17 the influence of the output characteristics are simulated for different values of the body resistance with a thermal resistance $R_T = 5$ kK/W. For very high values of the body resistance, the LDMOS behaves as a floating body SOI MOSFET and shows a clear kink in the output characteristics. This is explained by the well known "kink effect" [5]. When the fields in the transistor are high enough, the electron current creates electron-hole pairs (impact ionisation). The holes will naturally migrate to the body, and increase the body voltage significantly if the body resistance in very high. This reduces the threshold voltage via the well known body-effect, and hence the drain current increases. This generates even more impact ionisation current, creating a positive feed-

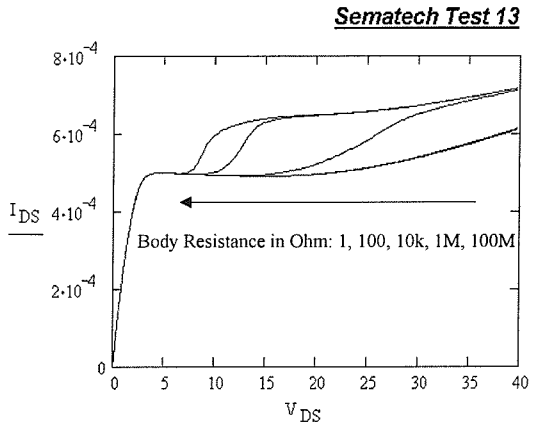

Figure 7.17: Test 13: influence of the body resistance on the output characteristics. $R_{\mathrm{T}} = 5$ kK/W (Device 2).

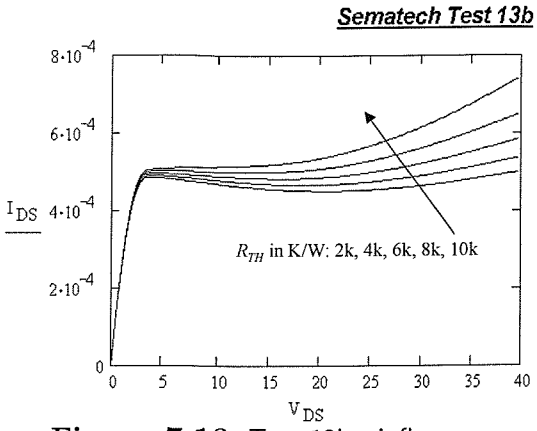

Figure 7.18: Test 12b: influence of the thermal resistance on the parasitic bipolar effect. $R_{\mathrm{body}} = 100\ \Omega$ (Device 2).

back loop, which stabilises only when the body-source junction becomes forward biased. The generated holes can then recombine with electrons from the source and an equilibrium is reached. This kink effect disappears for lower values of the body resistance. For higher values of the drain voltage the parasitic bipolar switches on, causing a continuous increase in the drain current, which will finally lead to breakdown.

Fig. 7.18 shows the output characteristics for different values of the thermal resistance, and a low body resistance ($R_{\mathrm{body}} = 100\ \Omega$). The body resistance is too low to cause the kink-effect, but the increased temperature rise due to self-heating causes the parasitic BJT to switch on earlier as the thermal resistance is increased.

Figs. 7.17 and 7.18 prove that our model can account for this anomalous behaviour and that it simulates these effects smoothly.

7.2.3 Transient tests

Push-Pull Inverter

Figs. 7.19 (Device 1) and 7.20 (Device 2) show the transfer characteristics for a simple push-pull inverter consisting of an N-type and P-type LDMOS. The longer drift region of device 2 reduces the gain and leads to variations in the slope of the transfer characteristics.

Figs. 7.21 (Device 1) and 7.22 (Device 2) show input and output voltages for a positive and negative going pulse. The effect of the longer drift region of device 2 mainly manifests itself as a higher over- or undershoot of the output voltage at the start of the rising and falling edge respectively of the input voltage.

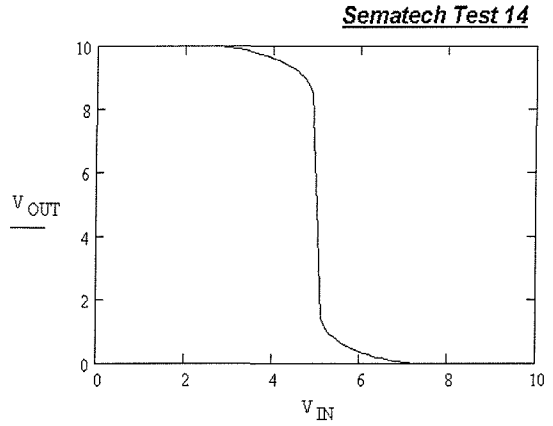

Figure 7.19: Test 14: inverter transfer characteristic (Device 1).

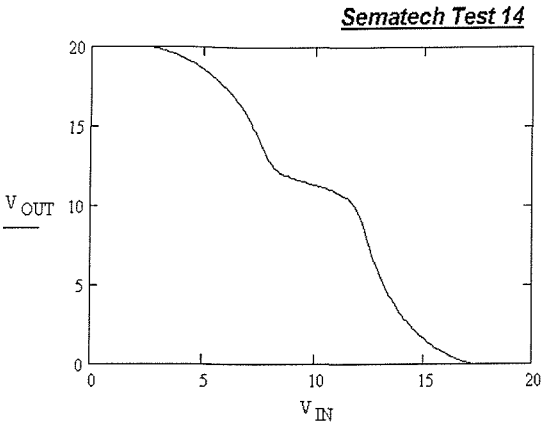

Figure 7.20: Test 14: inverter transfer characteristic (Device 2).

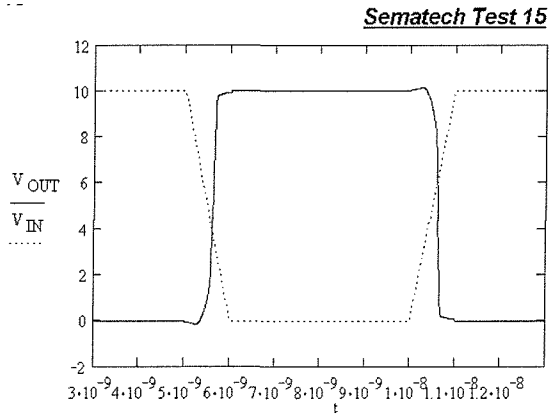

Figure 7.21: Test 15: inverter charge/discharge characteristic (Device 1).

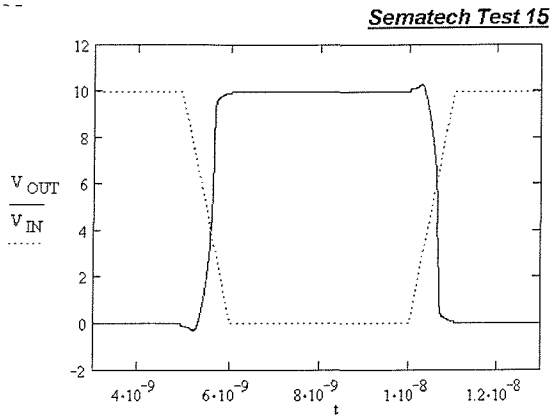

Figure 7.22: Test 15: inverter charge/discharge characteristic (Device 2).

Inverter with Resistive Load

An interesting single transistor circuit to test the transient behaviour of the LDMOS is shown in the inset of Fig. 7.23. It consists of a simple invertor with resistive load and a very high resistance connected to the gate. This gate resistance is added deliberately to show the gate-drain capacitance effects. The simulated wave forms for devices 1 and 2 are shown in Figs. 7.24 and 7.23 respectively. Let us have a look at the results for a rising pulse for V_{IN}. As V_{IN} rises, the gate is charged until the channel is inverted and the device is conducting. Now the drain voltage starts dropping and the drift region becomes more and more accumulated. During the charging time of the large gate-drain capacitance, the gate voltage stays almost constant while V_{DB} goes to zero. After that, V_{GfB} can rise further until it reaches V_{IN}. This effect is typical for LDMOS transistors because the overlap of the gate over the drift region creates a considerable gate-drain overlap capacitance,

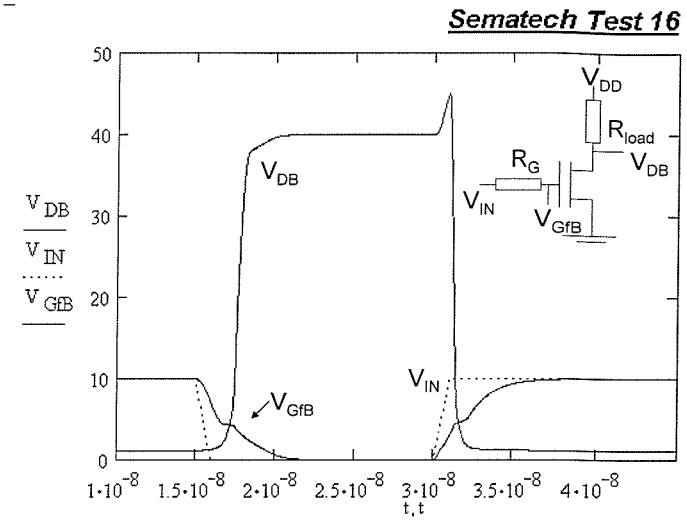

Figure 7.23: Test 16: resistive load inverter charge/discharge characteristic. $R_{\text{load}} = R_{\text{G}} = 100$ kΩ (Device 2).

which is much larger than for standard MOSFETs. From the results of Figs. 7.24 and 7.23, one observes that our model predicts this charge behaviour without discontinuities. Furthermore, all these characteristics were simulated without any convergence problems.

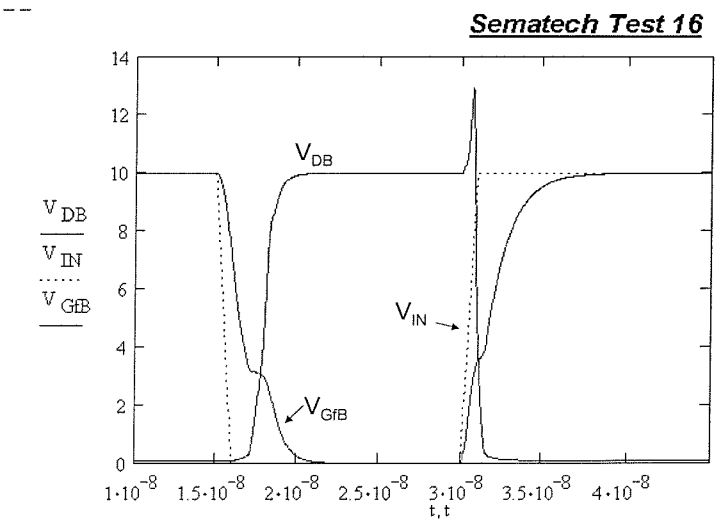

Figure 7.24: Test 16: resistive load inverter charge/discharge characteristic. $R_{\text{load}} = R_{\text{G}} = 100$ kΩ (Device 1).

7.2.4 Capacitance Tests

Tests 21 and 22 check the simulation behaviour of the (trans)capacitances with swept drain and gate voltages. These values are derived from AC simulation in SPICE and not from the derivatives of the internal charges. In this way, the model is checked for inconsistent

implementation or coding errors of the charge model.

The results of these tests on devices 1, 2, 3 and 4 are shown in App. F. However, since very similar simulations have already been compared with measurements in Chapter 5, these tests will not be treated in detail. The model produces continuous (trans)capacitance values for all tests (see App. F); refer to Chapter 5 for a discussion of the shortcomings and the slightly non-physical behaviour of the SOI LDMOS charge model.

7.3 Circuit Simulation Performance

In this section the simulation and measurement results of two common analogue circuits are presented. These circuits form a good test for the convergence behaviour of our model in the simulator. The first circuit is a switching power circuit and tests the transient simulation capability of the compact LDMOS model in a switching application. The second circuit under study is one of the most versatile and important building blocks in analogue circuit design: the operational amplifier.

The circuits have been fabricated in the HV SOI process and the simulation results are compared with measurements of the circuit. The influence of self-heating on some circuit blocks has been investigated and further insights about the compact model are set out.

7.3.1 Switching Power Circuit

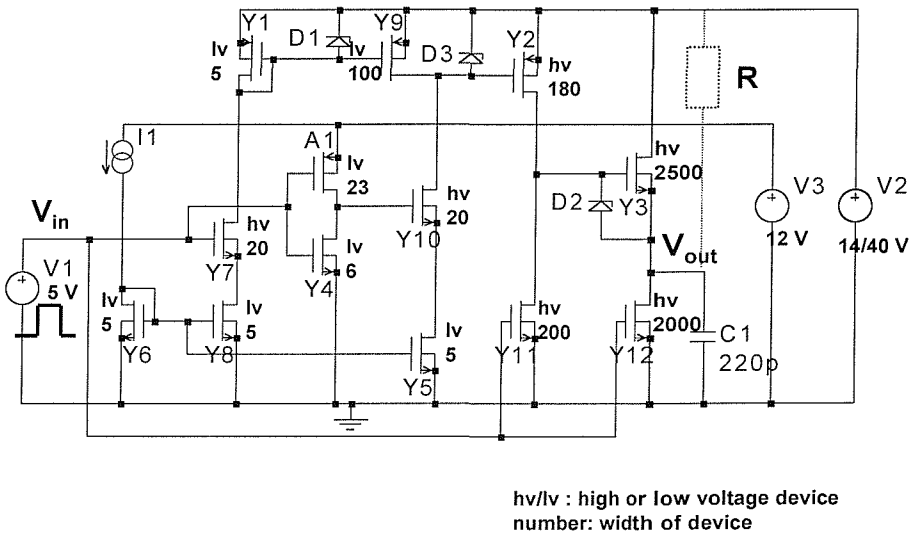

Figure 7.25: Circuit schematic for a switching power block.

This particular switching power circuit was chosen as a test circuit because convergence problems were encountered with it when simulating with the subcircuit model presented

in Chapter 3 [6]. The circuit consists of a simplified driver circuit for plasma displays, and was designed and fabricated in PHILIPS Nijmegen. The original, more sophisticated circuit drives the horizontal lines of a plasma display, which forms a capacitive load, and the lines have to switch between 0 and 200 V. In recent years, colour plasma displays have attracted a lot of attention, and the number of HV driving circuits with a driving capability ranging from 80 V to 200 V has been increasing [7–9].

To test the LV and MV LDMOS, two similar circuits were designed for 14 V and 40 V. In the first one the HV LDMOS transistors were replaced with LV LDMOS transistors, and in the second one with MV LDMOS transistors.

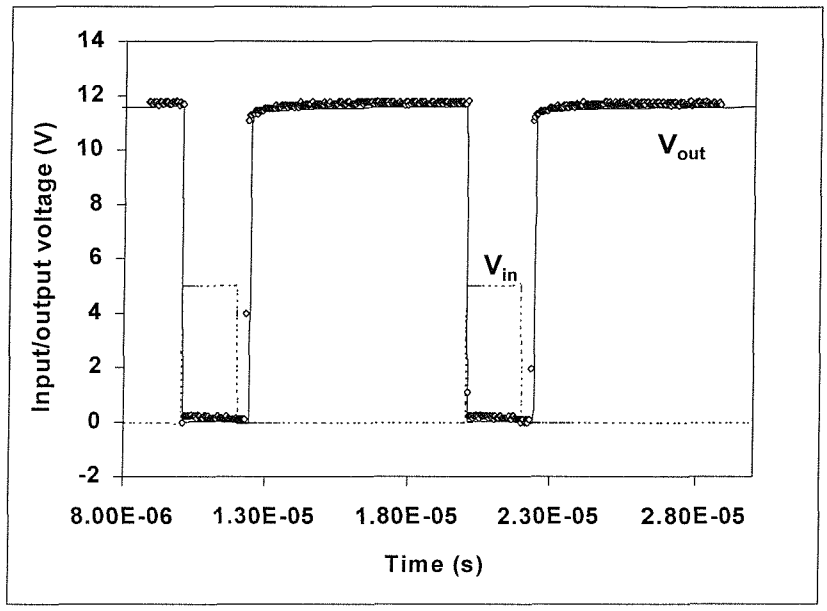

Figure 7.26: Charge and discharge characteristics for the LV driver circuit.

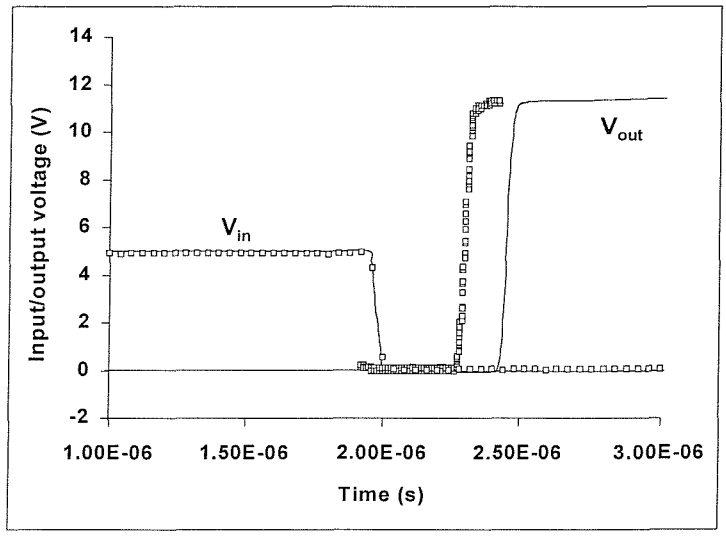

Figure 7.27: Detail of the rising edge of the simulated (full line) and measured (markers) output voltage (LV circuit).

The circuit is shown schematically in Fig. 7.25. The output transistors Y3 and Y12 have to charge and discharge the capacitive load. Y12 and Y11 are directly switched on by V_{in}, and at that moment Y2 has to be off. This is realised by the current mirror Y1-Y9, which pulls up the gate of Y2. When V_{in} switches to zero, Y12 and Y11 are turned off and the gate of Y2 is pulled down, but limited by the zener diode (D3) for the MV and HV version of the circuit. This turns on Y3, charging the capacitive load. Measured and simulated charge and discharge characteristics are compared in Fig. 7.26. Details of the rising and falling edges are shown in Figs. 7.27 and 7.28. The rise and fall times are well predicted by the simulation results, but the delay time is slightly overestimated by the simulator. The reason could be the less accurate modelling of the LV PMOS transistors (Y2 and A1) which are partly responsible for the delay.

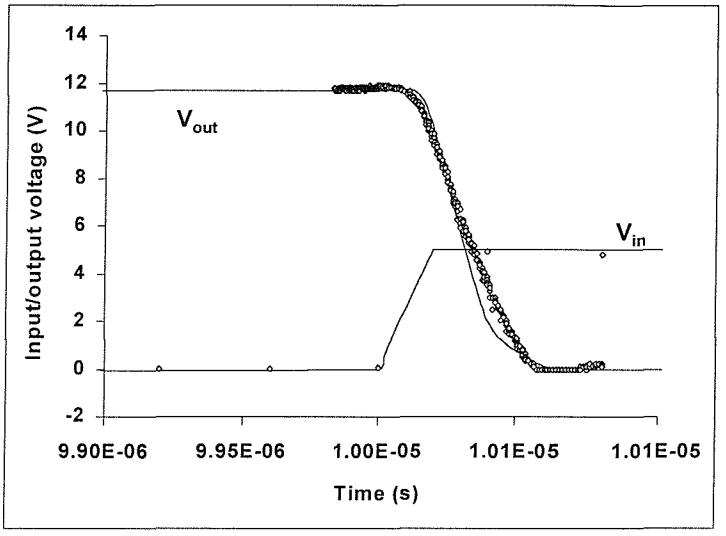

Figure 7.28: Detail of the falling edge of the simulated (full line) and measured (markers) output voltage (LV circuit).

To investigate the self-heating behaviour of the circuit, a load resistor was added between the output and the positive supply (see dotted lines in Fig. 7.25). Now the output voltage does not go all the way back to 0 V when Y12 is switched on, but reduces to a value determined by Y12 and the load resistor. The measured and simulated results for the MV circuit when R = 120 Ω, and for the LV circuit when R = 73.3 Ω are shown in Figs. 7.30 and 7.29 respectively. Due to self-heating the temperature of Y12 increases with time when Y12 is switched on. This reduces the current in Y12 and causes a slight rise in the output voltage to compensate for this decreased current value. In Fig. 7.31 the output voltage is plotted in detail and one can clearly observe the positive slope. In the same figure the output voltage is simulated with and without self-heating, and it is clear that including self-heating correctly predicts the positive slope while the iso-thermal result shows a constant value for V_{out}. Fig. 7.32 shows the simulated temperature rise of Y12 during the transient simulation, and for a frequency of 150 kHz and a duty cycle of 20 %, a temperature rise of 10 K is observed. Measuring the circuit at higher frequencies with

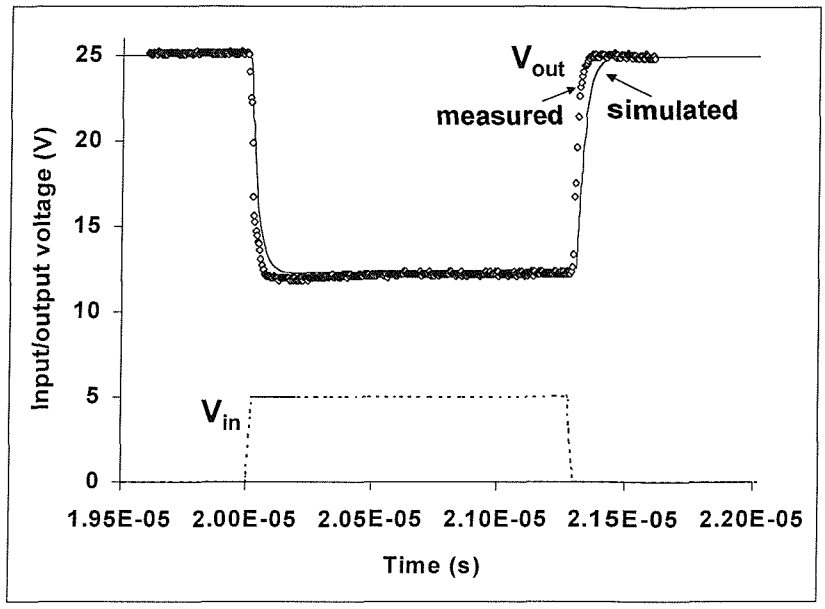

Figure 7.29: Simulated (full line) and measured (markers) output voltage with a resistive load (R = 73 Ω) to the supply voltage (LV circuit).

a higher duty cycle can lead to very high temperatures with the possibility of destroying the circuit.

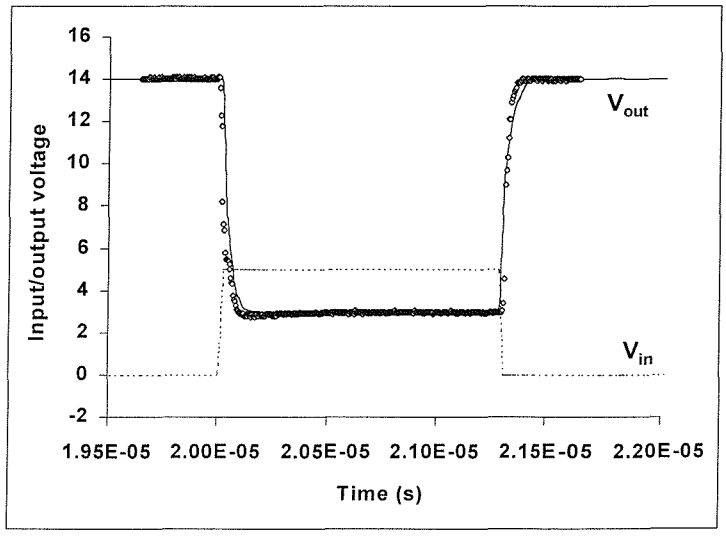

Figure 7.30: Simulated (full line) and measured (markers) output voltage with a resistive load (R = 120 Ω) to the supply voltage (MV circuit).

Finally, the HV driver circuit was also measured and simulated. The HV N and P-type LDMOS do not have a constant doping profile in the drift region, and therefore our model will give less accurate results than for the LV and MV LDMOS. The HV LDMOS was characterised using an effective value for the doping concentration in the drift region and its model parameters can be found in App. G. Fig. 7.33 shows the charge and discharge characteristics and the details of the rising and falling edge can be found in Figs. 7.34 and

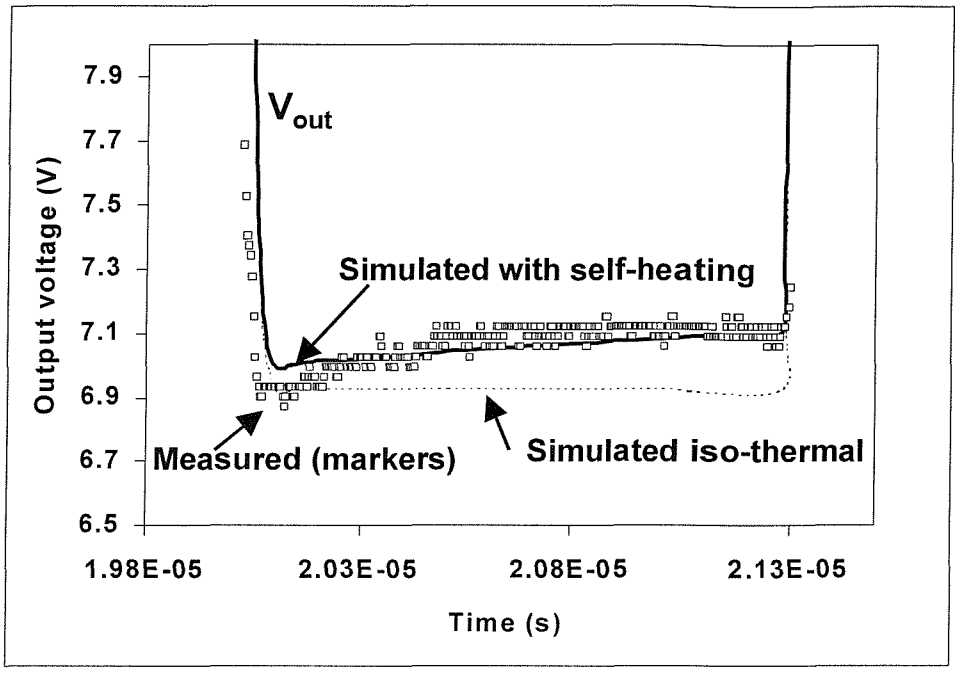

Figure 7.31: Detail of the measured (markers) and simulated (with (full line) and without (dotted line) self-heating) positive slope from the previous figure.

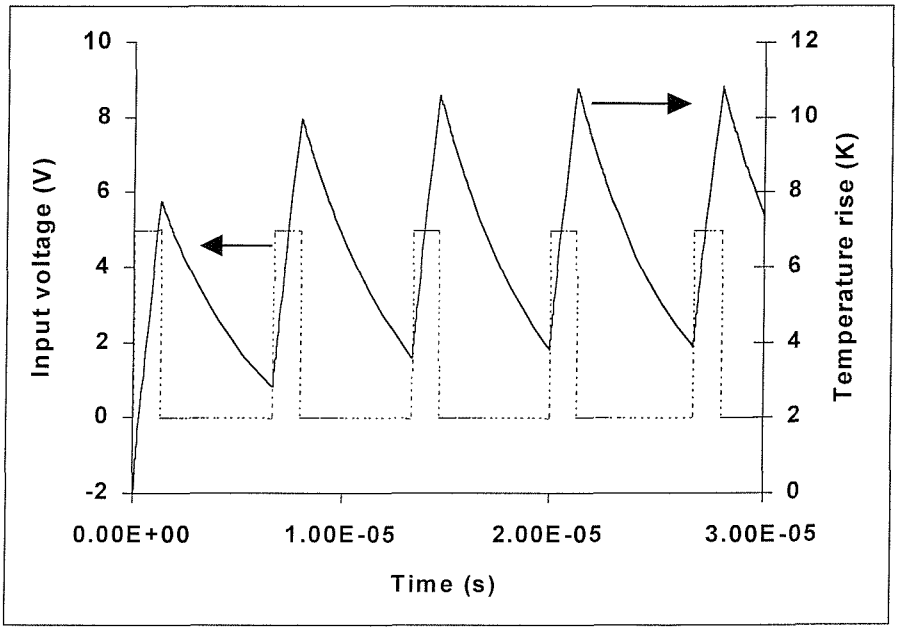

Figure 7.32: Simulated temperature rise of the output transistor Y12 when R = 73 Ω.

7.35.

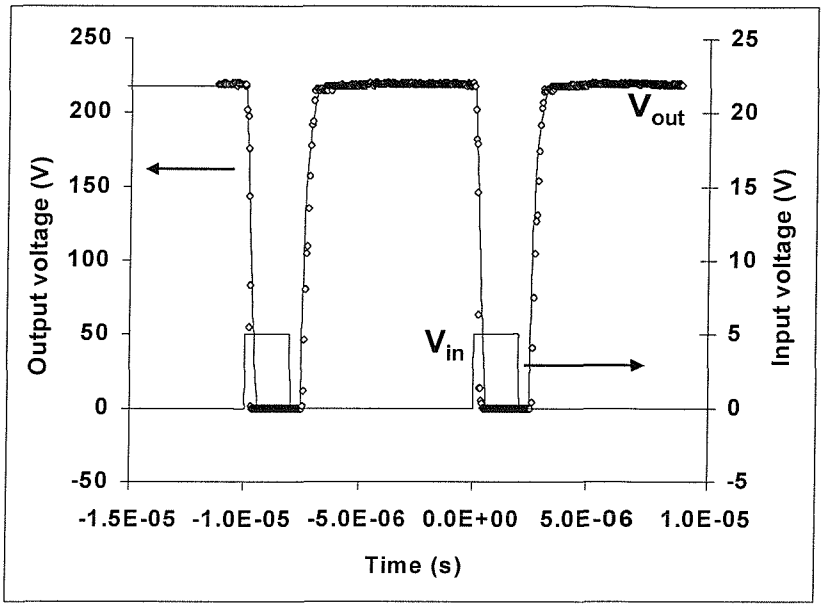

Figure 7.33: Charge and discharge characteristics for the HV driver circuit.

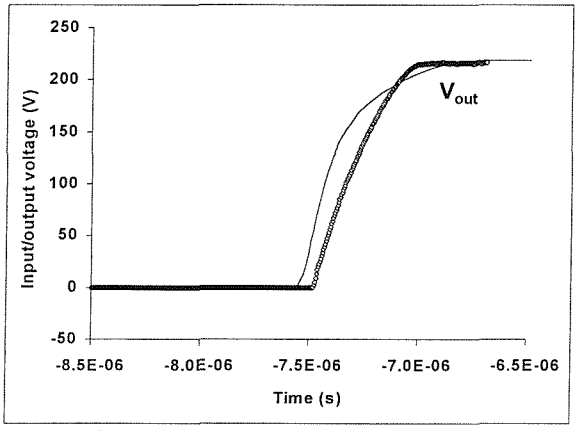

Figure 7.34: Detail of the rising edge of the simulated (full line) and measured (markers) output voltage (HV circuit).

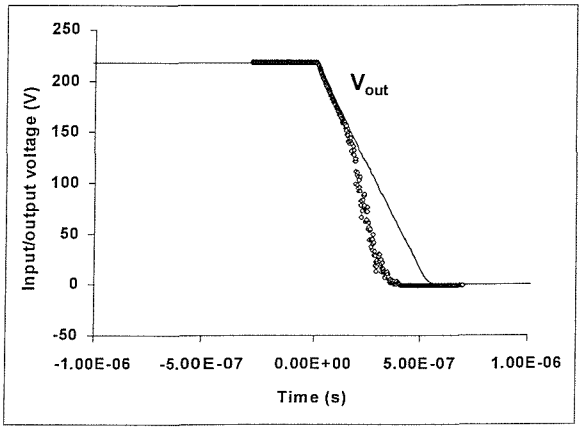

Figure 7.35: Detail of the falling edge of the simulated (full line) and measured (markers) output voltage (HV circuit).

7.3.2 Operational Amplifier Circuit

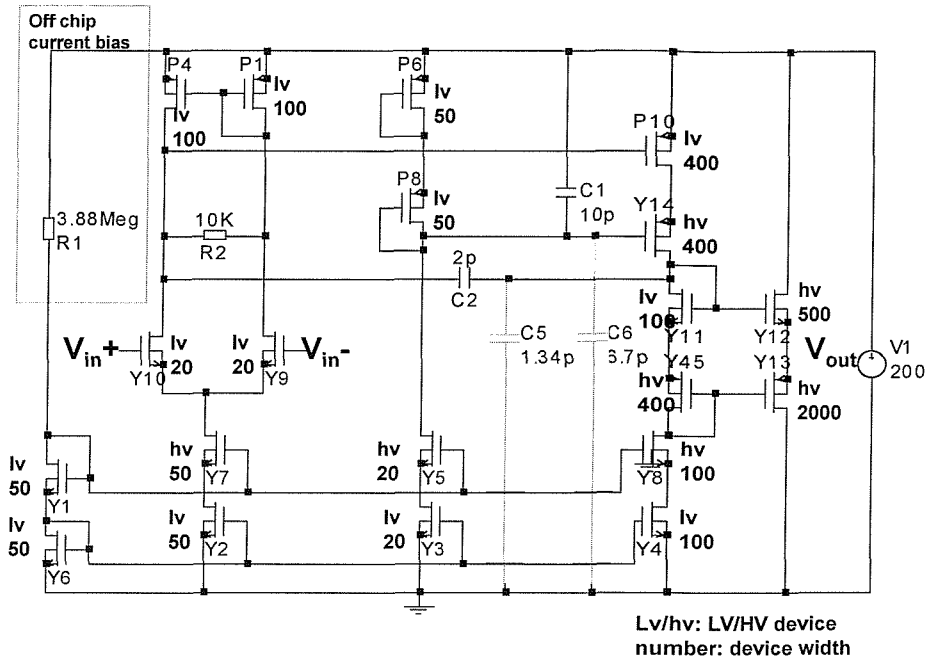

Figure 7.36: Circuit schematic of the HV opamp.

The next circuit we will analyse is a class AB operational amplifier. The opamp topology is based on a design commonly used in CMOS technology [10, 11]. It is a two-stage configuration with an additional low output impedance stage. The circuit schematic is shown in Fig. 7.36. For clarity the protecting zener diodes have been left out of the picture, but they will be mentioned later on in this section.

The opamp circuit utilises a 200 V power supply and is biased externally through a resistor (R1) to obtain a bias current of 50 μA. Transistors Y9 and Y10, together with the current source (Y7/Y2), form the differential input stage. Transistors P1 and P4 in the current mirror configuration convert the output differential signal to a single-ended signal. Transistor P10 along with biasing transistors Y4 and Y8 form the second stage. Y11 and Y45 provide a bias voltage for the source-follower buffers Y12 and Y13 of the output stage. The capacitor C2 is a compensation capacitor required to set the unity gain frequency. Y14 is a cascode transistor to limit the V_{DS} on the LV P-type LDMOS P10. It is controlled by a control voltage provided by two diode connected transistors (P6 and P8). The capacitors in the HV SOI process have a parasitic component to the substrate, which is connected to earth: C5 is the parasitic part of C2, and C6 of C1.

The threshold voltages of the LV and HV N-type LDMOS transistors are exactly the same, and hence the choice of a LV or HV device depends only on the drain voltage that it has to withstand. However, for the P-type devices the threshold voltage differs slightly for the LV and HV devices. Therefore Y45, which does not have to withstand a high voltage, still needs to be a HV P-type LDMOS in order to obtain a good current mirror. The

current mirrors are designed using cascode configurations to improve their performance.

To protect the gate oxides of the input transistors in the differential pair, two zener diodes in series and opposite to each other were added in between the gate and source of each input transistor. For the same reason another zener diode was added between the positive supply and the gate of P10. The parameter sets for the N and P-type HV LDMOS and for the LV PDMOS can be found in App. G. The parameter set for the LV LDMOS was derived in Chapters 4 and 5.

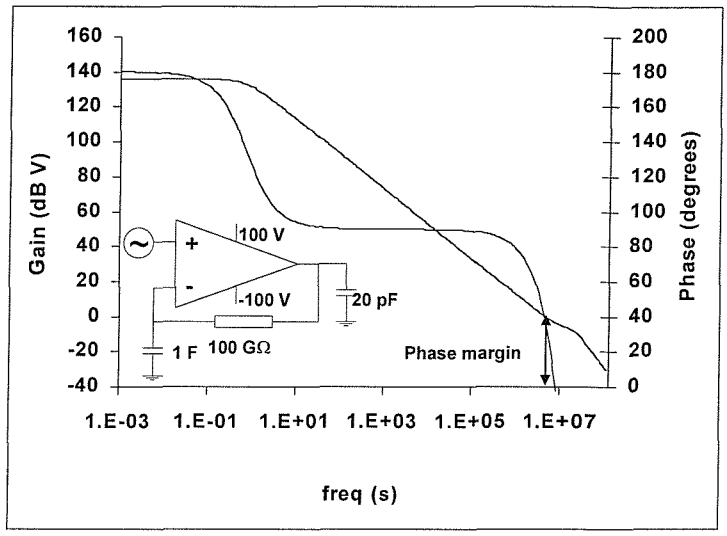

Figure 7.37: The simulated open loop opamp gain with a load capacitance of 20 pF.

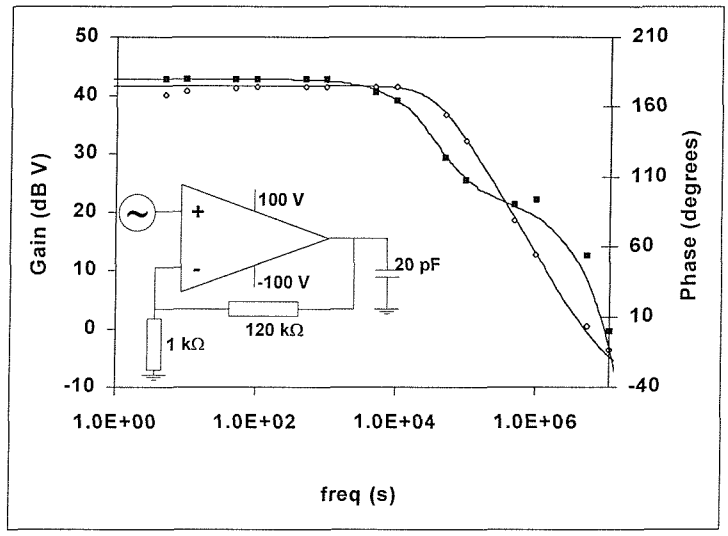

Figure 7.38: The measured (markers) and simulated (full line) opamp gain in a non-invertor arrangement with $R_1 = 1$ kΩ and $R_2 = 120$ kΩ, and a load capacitance of 20 pF.

In Fig. 7.37 the open loop gain is simulated. The DC gain is very high (almost 140 dB) and the dominant pole is quite low (1 Hz). The second pole is situated around 10 MHz and the simulated phase margin is 40^o. In practice it is very difficult to measure such

high gains, and with the available equipment, it was only possible to measure up to a gain of roughly 40 dB. For these reasons it was decided to measure the non-inverter arrangement of Fig. 7.38, for which the maximum gain is determined by the ratio of the resistors. Good agreement is observed between the measurements and the simulations, which predict the phase behaviour and the cut-off frequency accurately. Note that, if an open-loop gain measurement were to be done by means of a resistor and capacitor in the negative feedback path as illustrated in Fig. 7.37, one has to make sure that the reciprocal of the RC time constant is a factor of $A_v(0)$ (the maximum gain) less than the anticipated dominant pole of the opamp. This would mean that RC has to be more than 10^7, which is not very practical.

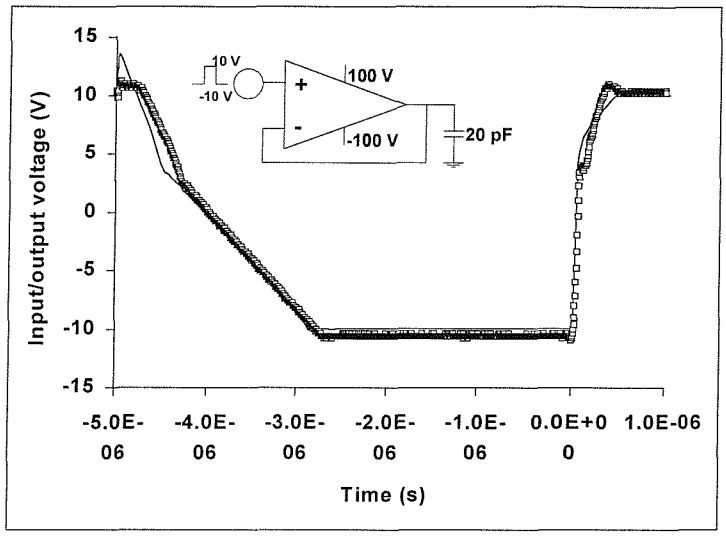

Figure 7.39: The measured (markers) and simulated (full line) output voltage of the opamp with a load capacitance of 22 pF.

This non-inverter measurement arrangement can also be used to determine the input offset voltage of the opamp, which can be simply obtained as the the DC value of the negative input of the opamp. This results in a value of 44 mV for the input offset. The consequence of this offset is that the output voltage will be about 5 V (120 kΩ · 44 mV/1 kΩ), instead of the theoretical value of 0 V when using the resistor divider of Fig. 7.38 in the negative feedback path.

The configuration shown in the inset of Fig. 7.39 is useful to measure the slew rate, overshoot, and the settling time of the opamp. This measurement is repeated for different values of the load capacitance and the load resistance for a -10 V to 10 V step input into the follower. Figs. 7.39, 7.40 and 7.41 show the slew rate characteristics for $C_{\text{load}} = 22$ pF, $C_{\text{load}} = 184$ pF and $C_{\text{load}} = 1$ nF respectively with $R_{\text{load}} = 0\ \Omega$. The falling edge clearly shows the slew rate limitations of the opamp. However, the rising input pulse switches on the protective zeners at the input, and the output voltage rises quickly, showing only a little bit of slewing in the tail of the output voltage. Figs. 7.42 and 7.43 show the slew rate characteristics for $R_{\text{load}} = 1.5$ kΩ and $R_{\text{load}} = 800$ kΩ respectively with $C_{\text{load}} = 22$ pF.

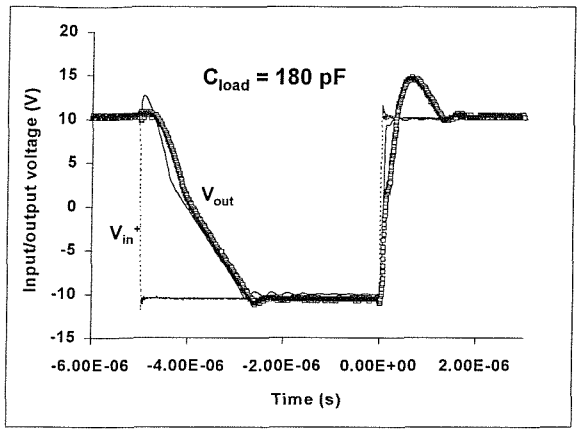

Figure 7.40: The measured (markers) and simulated (full line) output voltage of the opamp with a load capacitance of 184 pF.

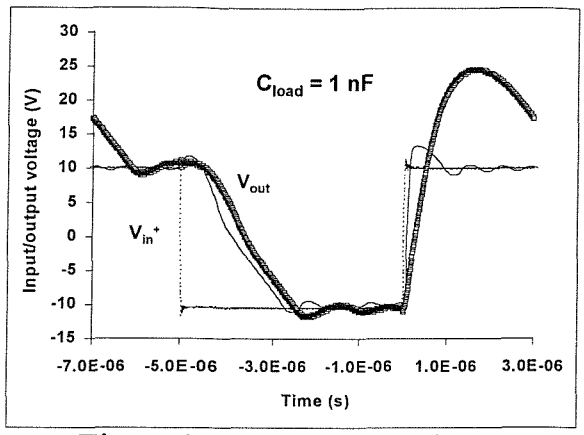

Figure 7.41: The measured (markers) and simulated (full line) output voltage of the opamp with a load capacitance of 1000 pF.

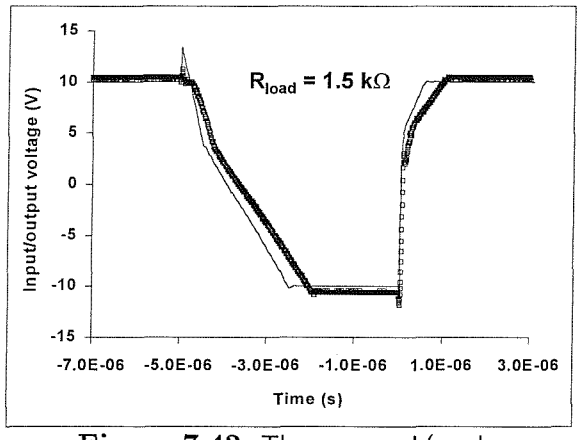

Figure 7.42: The measured (markers) and simulated (full line) output voltage of the opamp with $C_{\text{load}} = 22$ pF and $R_{\text{load}} = 1500\ \Omega$.

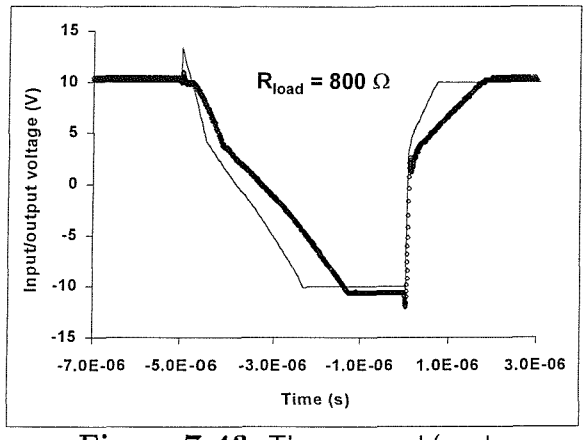

Figure 7.43: The measured (markers) and simulated (full line) output voltage of the opamp with a load capacitance of $C_{\text{load}} = 22$ pF and $R_{\text{load}} = 800\ \Omega$.

The differences between the measurements and the simulations are probably due to the fact that the circuit contains a couple of high voltage N and P-type LDMOS transistors, which cannot be modelled perfectly with our model because of the doping profile in the drift region. In particular the simulated overshoot of the rising edge of the output voltage with a high capacitive load (see Fig. 7.41) is a lot smaller than the measured overshoot. The reason is probably that the high-side behaviour of Y12, which is an HV LDMOS is not very well predicted by the model, since the doping gradient in the drift region will strongly affect the high-side behaviour. In our model we use an effective value for the doping concentration, which is higher than the doping concentration at the source end of the drift region. As a result, the pinch-off voltage used in the simulation is lower than in

a real device, and hence the predicted current reduction due to the high-side behaviour is too low. However the gain, phase and slew rate were all well predicted.

7.4 Summary

This chapter has evaluated the SOI LDMOS model thoroughly using a set of simulation scripts, based on the SEMATECH tests. It has been shown that the model is well behaved in all regions of operation, and moves smoothly and continuously from one region into another. The model was also tested on two typical analogue circuits. The model predicts the measurement results well for circuits containing only LV and MV transistors and gives also a reasonable prediction of the HV circuits. We can conclude that the compact SOI LDMOS model is a useful tool for analogue circuit design in an SOI DMOS technology, and with further optimisation a good modelling capability can be expected.

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Chapter 8

Conclusions and Further Work

8.1 Conclusions

As the scaling down of smart power ICs is gaining in importance, SOI technology is becoming more attractive. The LDMOS transistor is one of the key devices in HV ICs, and a good model is indispensable in order to perform accurate circuit design. The modelling and characterisation work in this thesis is aimed at improving the CAD capability for designers, to provide better static and dynamic accuracy in a consistent and robust simulation model system. Some subcircuit models for bulk and SOI LDMOS devices are readily available, but when certain special aspects of device behaviour become critical, they are not always sufficient. Furthermore, the use of subcircuit models increases the complexity and computation time of the simulation. The need for a good compact model which specifically addresses SOI LDMOS behaviour is apparent!

Development of such a model requires a full comprehension of the physics of the device. Therefore, an overview of the typical structures for LV, MV and HV LDMOS transistors was first presented, and the special electrical and thermal behaviour was described and explained physically. The effect of the lateral doping gradient on the charges in the LDMOS was studied in detail, and a new characterisation method for this lateral body doping gradient coefficient was developed. The impact ionisation phenomenon was fully explained, measured, and simulated in ATLAS for both the LV and MV LDMOS. Also, the important parameters for thermal and switching behaviour were discussed.

High side operation for CMOS or LDMOS is associated with very large bias values across the back oxide. For an N-type LDMOS this leads to an increased on-resistance, and for a PMOS this can result in inversion of the back interface, with consequent leakage and unaccounted charges. These unique effects were examined in detail and simulated with a device simulator to ascertain the physical causes.

With this knowledge of the device physics of the LDMOS, the development of a circuit simulator model could begin. First, the subcircuit modelling approach was followed, resulting in a "quick-fix" LDMOS model, which could be used in the PSTAR circuit simulator. This type of model gave good DC agreement with measurements, and reasonable

transient and AC results, but had several drawbacks: complexity, increased computation time, and poor convergence. In addition the model could not be used to duplicate certain effects particular to the LDMOS. Most notably, the high-side effects could not be simulated very accurately, and we were also restricted in the charge modelling.

To overcome these disadvantages a compact model was developed. Such a model has the advantage of simplicity, and aims to predict as accurately as possible the device behaviour with simple mathematics, making it possible to use the formulations in a circuit simulator.

First the DC model was set out. The model needed only one internal node, situated in the channel at the transition point from thin gate oxide into field oxide. Both the current under the thin gate oxide and under the field oxide were carefully derived, to keep the model as physical as possible. All assumptions made were considered critically, and verified where necessary. The current under the thin gate oxide was described in terms of the surface potentials, whilst taking into account the lateral doping gradient and the overlap of the gate over the N^- drift region. Vertical mobility degradation and velocity saturation effects were included in a robust and continuous way. Furthermore, we accounted for CLM and DIBL. The impact of the thickness of the depletion layer at the buried oxide on the current under the field oxide was studied rigorously, leading to a good prediction of the unique high-side behaviour. The DC simulations performed with the compact model matched well with the measured characteristics for a wide range of geometries, with self-heating and high-side effects being properly accounted for.

Next, the complete SOI LDMOS charge model was set out, presenting a promising new approach to deal with the charge partitioning in the LDMOS. The use of a bias dependent length for the inversion channel to account for the lateral doping gradient gives an accurate, smooth transition from subthreshold into the on-state. The simulated capacitance characteristics, obtained for a range of geometries, show the right trends overall. And although not always completely accurate, the new expressions form the basis for a good charge model.

The model has been implemented in a SPICE circuit simulator. Although the model equations are quite mathematically robust, numerical bottlenecks and particularities were encountered during the implementation and testing phase of the model. Various clipping solutions to avoid over- and underflow have been discussed, and a new voltage limiting scheme for the internal drain voltage was presented. Furthermore, techniques to improve the precision of certain evaluations have been explained. These measures have led to a very robust SOI LDMOS model, which converges easily without the need for node setting.

The SOI LDMOS model was evaluated thoroughly, using a set of simulations based on the SEMATECH tests. It has been shown that the model is well behaved in all regions of operation, and moves smoothly and continuously from one region into another.

Finally, two special analogue circuits were designed and fabricated to allow circuit level evaluation of the accuracy and robustness of our model. The model predicted the measurement results well for circuits containing only LV and MV transistors, and also

gave a reasonable prediction for the HV circuits. We can conclude that the compact SOI LDMOS model is a useful and reliable design tool for analogue circuits using an SOI DMOS technology.

8.2 Ideas for Future Work

The developed SOI compact model was specially derived for LV and MV SOI LDMOS transistors, assuming constant doping in the drift region. However, HV LDMOS transistors are usually fabricated with a graded doping profile under the field oxide, and the field oxide can be thinner at the drain end. Ideally, the influence of these effects should be included in a HV LDMOS model. However, a HV LDMOS transistor can be realised in different ways. Various RESURF techniques [1, 2] exist, or one can opt to use a superjunction (or COOLMOS) [3, 4] device. This makes the drift region of an HV LDMOS very technology dependent, and it will be very difficult to make a general physical model for the drift region under the field oxide. But still, more modelling work for the drift region of an HV LDMOS is desirable.

Another feature of HV LDMOS transistors is that the drift region can become quite long, creating a significant variation in temperature along the device. To account accurately for self-heating would therefore require two or more temperature nodes for a single device. Finally, in some technologies the effect of the overlap of the gate or source/drain contacts over the field oxide should also be considered.

The impact ionisation phenomenon was examined in considerable depth in Chapter 2. Our insights into this effect have not yet been exploited in the circuit model, which still uses standard MOSFET equations for the impact ionisation current. These standard expressions need to be adapted to account accurately for the avalanche current in the SOI LDMOS. It would also be interesting to verify the effect of a correctly simulated impact ionisation current on the parasitic bipolar behaviour, because the avalanche current flows through the body, and hence rises the base voltage of the parasitic BJT. Furthermore, the temperature strongly influences the parasitic BJT current, and thus heating effects should be taken into account [5].

As explained in Chapter 2, the current flow can be highly two dimensional, which will have a non-negligible influence on the charge behaviour, and although accounted for in an empirical way, a more general physical study could be conducted.

The topic of noise in SOI LDMOS transistors was beyond the scope of this project, but a study is under way by researchers in PHILIPS Eindhoven. The model will probably combine noise contributions generated in MOSFET and JFET devices, and some reports have suggested that there may be an additional anomalous effect in the noise behaviour of an SOI technology compared to its bulk counterpart [6–8].

In our model, constant capacitances were used to model the back gate-drain capacitance, the back gate-body capacitance and the back gate-source capacitance. However, it is clear that, to obtain a really accurate description of the capacitance behaviour at the

back gate, one has to do a quantitative analysis of the charges at the buried oxide, leading to non-constant, non-reciprocal capacitance values. The first step in the development of a good back gate capacitance model consists of finding a good measurement strategy for these capacitances. Next, the influence of all the different terminal voltages on the charges at the back gate has to be derived. This will involve a similar analysis to the study performed in Chapter 5 for the front gate charge.

In addition to the SEMATECH and circuit tests performed in Chapter 7, more convergence tests on large scale ICs are necessary to check further the stability and robustness of the model equations. These tests are currently being done in PHILIPS with the PSTAR version of the compact model.

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Appendix A

ATLAS Results for the LDMOS

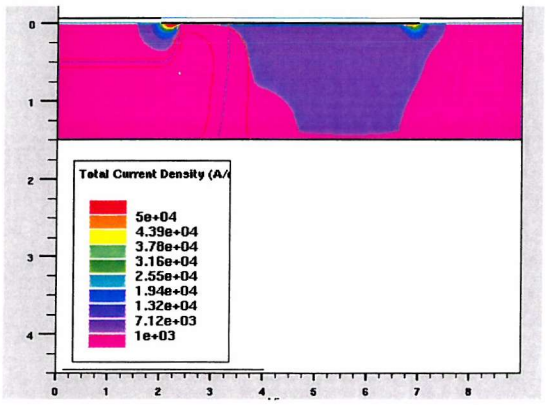

Figure A.1: The current density in the LV LDMOS for $V_{DS} = 1$ V and $V_{GfS} = 8$ V

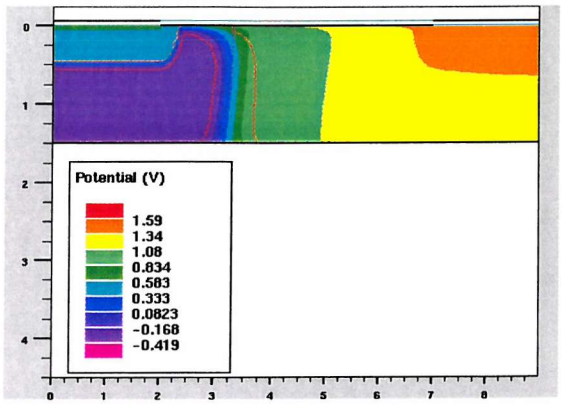

Figure A.2: The potential in the LV LDMOS for $V_{DS} = 1$ V and $V_{GfS} = 8$ V

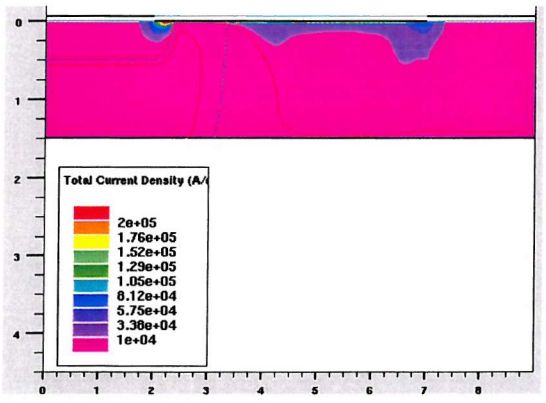

Figure A.3: The current density in the LV LDMOS for $V_{DS} = 8$ V and $V_{GfS} = 8$ V

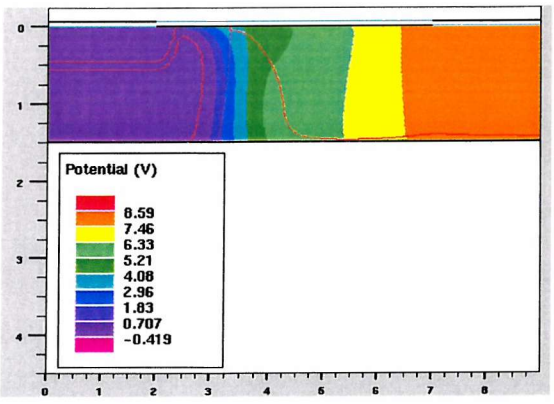

Figure A.4: The potential in the LV LDMOS for $V_{DS} = 8$ V and $V_{GfS} = 8$ V

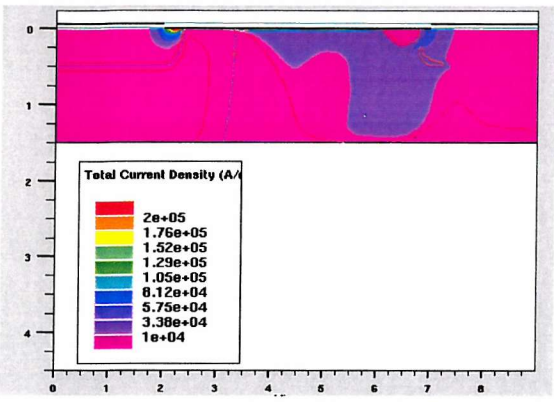

Figure A.5: Current density (LV LDMOS); $V_{\mathrm{DS}} = 15$ V, $V_{\mathrm{GfS}} = 8$ V

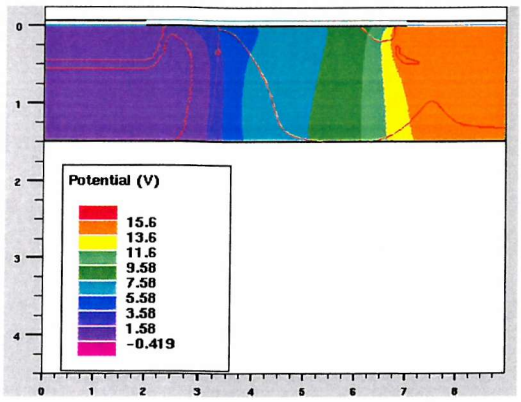

Figure A.6: The potential (LV LDMOS); $V_{\mathrm{DS}} = 15$ V, $V_{\mathrm{GfS}} = 8$ V

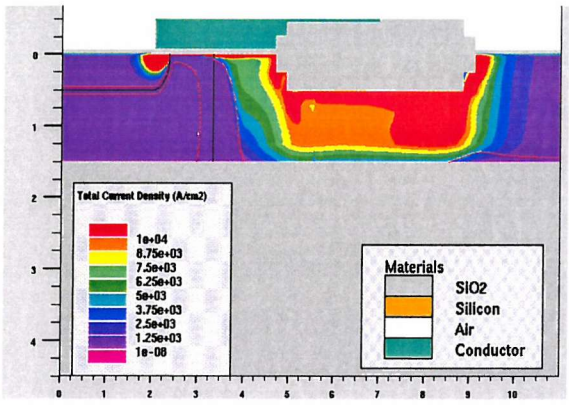

Figure A.7: Current density (MV LDMOS); $V_{\mathrm{DS}} = 8$ V, $V_{\mathrm{GfS}} = 8$ V

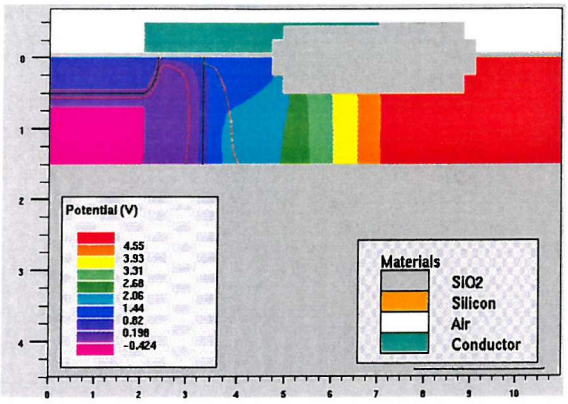

Figure A.8: The potential (MV LDMOS); $V_{\mathrm{DS}} = 8$ V, $V_{\mathrm{GfS}} = 8$ V

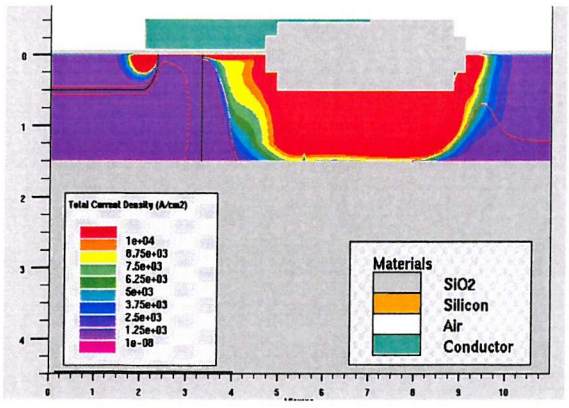

Figure A.9: Current density (MV LDMOS); $V_{\mathrm{DS}} = 20$ V, $V_{\mathrm{GfS}} = 8$ V

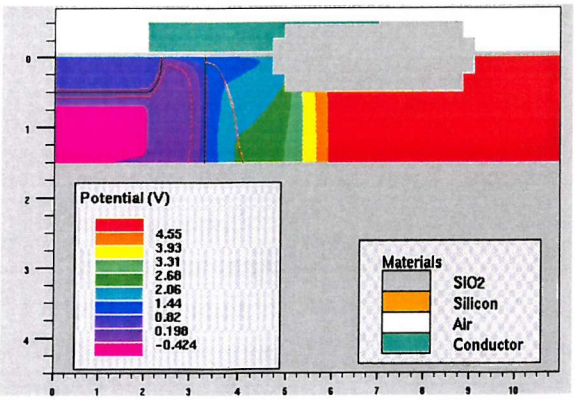

Figure A.10: The potential (MV LDMOS); $V_{\mathrm{DS}} = 20$ V, $V_{\mathrm{GfS}} = 8$ V

Appendix B

PHILIPS model parameters for MM902, M30 and M40

Table B.1 on the following page gives the names, descriptions and units for all electrical parameters of MM9.02.
Table B.2 on page 187 gives the names, descriptions and units for all electrical parameters of M30.02.
Table B.3 on page 188 gives the names, descriptions and units for all electrical parameters of M40.
Table B.4 on page 189 gives the optimised parameter set for the LV LDMOS.
Table B.5 on page 190 gives the optimised parameter set for the MV LDMOS.

In the following parameter description the Philips terminology is used. This means that the body is referred to as the substrate, and the back gate is referred to as the handle wafer. We have
BODY (B) = SUBSTRATE (SUB)
BACK GATE (Gb) = HANDLE WAFER (HW)

Name	Symbol	Parameter	Units
VTO	V_{th0}	Threshold voltage at zero back-bias for the actual transistor at the actual temperature	V
KO	γ_0	Low-back-bias body factor for the actual transistor at the actual temperature	$1/\mathrm{V}^{\frac{1}{2}}$
K	γ_h	High-back-bias body factor for the actual transistor at the actual temperature	$1/\mathrm{V}^{\frac{1}{2}}$
VSBX	V_{SBX}	Transition voltage for the dual-k-factor model for the actual transistor	V
BET	β	Gain factor for the actual transistor at the actual temperature	AV^{-2}
THE1	θ_1	Coefficient of mobility reduction due to the gate-induced field for the actual transistor at the actual temperature	1/V
THE2	θ_2	Coefficient of mobility reduction due to the back-bias for the actual transistor at the actual temperature	$1/\mathrm{V}^{\frac{1}{2}}$
THE3	θ_3	Coefficient of mobility reduction due to the lateral field for the actual transistor at the actual temperature	1/V
GAM1	γ_1	Coefficient for the drain induced threshold shift for large gate drive for the actual transistor	$\mathrm{V}^{1-\eta_{\mathrm{DS}}}$
ALP	α	Factor of the channel-length modulation for the actual transistor	-
VP	V_P	Characteristic voltage for channel-length modulation for the actual transistor	V
GAM00	γ_{oo}	Coefficient for the drain induced threshold shift at zero gate drive for the actual transistor	-
MO	m_0	Factor of the subthreshold slope for the actual transistor at the actual temperature	-
ZET1	ζ_1	Weak inversion correction factor for the actual transistor	-
VSBT	V_{SBT}	Limiting voltage for the V_{SB} dependence of GAM0 and MO for the actual transistor	V

Table B.1: *Names, descriptions and units for all electrical parameters of MM9.02.* *Continued on next page ...*

Name	Symbol	Parameter	Units
ETADS	η_{DS}	Exponent of the V_{DS} dependence of GAM1 for the actual transistor	-
ETAGAM	η_{γ}	Exponent of the back-bias dependence of GAM0 for the actual transistor	-
ETAM	η_{m}	Exponent of the back-bias dependence of M for the actual transistor	-
A1	A_1	Factor of weak avalanche current for the actual transistor at the actual temperature	-
A2	A_2	Exponent of weak avalanche current for the actual transistor	V
A3	A_3	Factor of the drain-source voltage above which weak avalanche occurs for the actual transistor	-
COX	C_{OX}	Gate-to-channel capacitance for the actual transistor	F
CGDO	C_{GDO}	Gate-drain overlap capacitance for the actual transistor	F
CGSO	C_{GSO}	Gate-source overlap capacitance for the actual transistor	F
NT	N_{T}	Coefficient of the thermal noise for the actual transistor	J
NF	N_{F}	Coefficient of the flicker noise for the actual transistor	V^2
ETABET	η_{β}	Exponent of the temperature dependence of BET for the actual transistor	-
STVTO	$s^T_{\mathrm{V_{th0}}}$	Temperature dependence of VTO for the actual transistor	-

Name	Parameter	Units	
LEVEL		Model level, must be set to 30	-
RON	R_{ON}	Ohmic resistance at zero bias	Ω
RSAT	R_{SAT}	Space charge resistance at zero bias	Ω
VSAT	V_{SAT}	Critical drain-source voltage for hot carriers	V
PSAT	P_{SAT}	Velocity saturation coefficient	-
VP	V_{P}	Pinch off voltage for zero gate bias and substrate voltages ; VP <= 0 no depletion and/or accumulation in the channel	V
TOX	t_{of}	Gate oxide thickness TOX > 0 MOSFET device TOX <= 0 No depletion at the surface	cm
DCH	N_{D}	Doping level channel	cm^{-3}
DSUB	N_{A}	Doping level substrate ; DSUB <= 0 no depletion from the substrate	cm^{-3}
VSUB	V_{SUB}	Substrate diffusion voltage	V
VGAP	V_{GAP}	Band gap voltage	-
CGATE	C_{GATE}	Gate capacitance at zero bias	F
CSUB	C_{SUB}	Substrate capacitance at zero bias	F
TAUSC	τ_{SC}	Space charge transit time in the channel	s
ACH	A_{CH}	Temperature coefficient in the channel	-
KF	K_{F}	Flicker noise coefficient	-
AF	A_{F}	Flicker noise exponent	-
TREF	T_{ref}	Reference temperature; default = 25 ^{o}C	^{o}C
DTA	ΔT	Difference of the device temperature to the ambient temperature ($T = T_{\mathrm{amb}} + \Delta T$)	^{o}C
MULT	m_{m}	Multiplication factor	-

Table B.2: *Names, descriptions and units for all parameters of M30.02.*

Name	Parameter	Units	
LEVEL		Model level, must be set to 40	-
RON	R_{ON}	Ohmic resistance at zero bias	Ω
RSAT	R_{SAT}	Space charge resistance at zero bias	Ω
VSAT	V_{SAT}	Critical drain-source voltage for hot carriers	V
PSAT	P_{SAT}	Velocity saturation coefficient	-
VP	V_{P}	Pinch off voltage for zero gate bias and substrate voltages ; VP <= 0 no depletion and/or accumulation in the channel	V
TOX	t_{of}	Gate oxide thickness TOX > 0 MOSFET device TOX <= 0 No depletion at the surface	cm
DCH	N_{D}	Doping level channel	cm^{-3}
TBOX	t_{ob}	Box oxide thickness TBOX <= 0 No depletion and/or accumulation at the box	cm
CGATE	C_{GATE}	Gate capacitance at zero bias	F
CBOX	C_{BOX}	Handle wafer capacitance at zero bias	F
TAUSC	τ_{SC}	Space charge transit time in the channel	s
ACH	A_{CH}	Temperature coefficient in the channel	-
TREF	T_{ref}	Reference temperature; default = 25 ^{o}C	^{o}C
DTA	ΔT	Difference of the device temperature to the ambient temperature ($T = T_{\mathrm{amb}} + \Delta T$)	^{o}C
MULT	m_{m}	Multiplication factor	-

Table B.3: *Names, descriptions and units for all parameters of M40.*

MM902	Value	M3002	Value
VTO	$(2.98 + 2.75\ 10^{-6} f_W^{**})$ V	RON	$\frac{1}{0.18+24500W}$ kΩ
KO	$(2.97 + 2.89\ 10^{-6} f_W^{**})\ V^{-\frac{1}{2}}$	RSAT	$\frac{1.05}{W+3.85\ 10^{-6}}$ Ω
K	$3.0\ V^{-\frac{1}{2}}$	VSAT	3.45 V
VSBX	100 V	PSAT	2
BET	$43(\frac{W+3.85\ 10^{-6}}{1.06\ 10^{-6}})\ \mu A{\cdot}V^{-2}$	VP	4.0 V
THE1	$(156.8\ 10^{-3} + 1.6\ 10^{-6} f_W^{**})\ V^{-1}$	TOX	$6\ 10^{-6}$ cm
THE2	$10\ 10^{-3}\ V^{-\frac{1}{2}}$	DCH	$1.1\ 10^{16}\ cm^{-3}$
THE3	$(53.5\ 10^{-3}$ - $0.49\ 10^{-6} f_W^{**})\ V^{-1}$	DSUB	$1.0\ 10^{17}\ cm^{-3}$
GAM1	$(9.62\ 10^{-3} + 190\ 10^{-6} f_W^{**})\ V^{1-\eta_{DS}}$	VSUB	0.67 V
ALP	$21.3\ 10^{-3}$	VGAP	1.206
VP	0.3 V	CGATE	$23\ 10^{-10}\ W$ F
GAM00	$2.7\ 10^{-3}$	CSUB	$3.7\ 10^{-10}\ W$ F
MO	2.13	TAUSC	0 s
ZET1	1.4	ACH	1.6
VSBT	0.5 V	KF	0
ETADS	0.6	AF	1
ETAGAM	1	TREF	25 °C
ETAM	1	MULT	1
A1	0.5		
A2	$6.25\ 10^{-6}$ V		
A3	0.65		
COX	$4\ 10^{-10}\ W$ F		
CGDO	0 F		
CGSO	$1.73\ 10^{-10}\ W$ F		
NT	0 J		
NF	0		
ETABET	1.4		
STVTO	$-3.3\ 10^{-3}\ °C^{-1}$		

Table B.4: *Optimised parameter set for the LV LDMOS.*

$$** \qquad f_W = \frac{1}{W + 3.85\ 10^{-6}} - \frac{1}{(20 + 3.85)\ 10^{-6}}$$

MM902	Value	M3002	Value
VTO	$(2.98 + 0.63\ 10^{-6} f_W^{**})$ V	RON	$\frac{0.027}{W+5\ 10^{-6}}\ \Omega$
KO	$2.4\ V^{-\frac{1}{2}}$	RSAT	50 kΩ
K	$0\ V^{-\frac{1}{2}}$	VSAT	2.07 V
VSBX	100 V	PSAT	1.1
BET	$43(\frac{W}{0.93\ 10^{-6}})\ \mu A{\cdot}V^{-2}$	VP	6.5 V
THE1	$0.22\ V^{-1}$	TOX	$6\ 10^{-6}$ cm
THE2	$0.01\ V^{-\frac{1}{2}}$	DCH	$1.1\ 10^{16}\ cm^{-3}$
THE3	$0.01\ V^{-1}$	DSUB	$1.0\ 10^{17}\ cm^{-3}$
GAM1	$(0.01 - 0.011\ 10^{-6} f_W^{**})\ V^{1-\eta_{DS}}$	VSUB	0.67 V
ALP	0.005	VGAP	1.206
VP	1.5 V	CGATE	$11.5\ 10^{-10}\ W$ F
GAM00	0.003	CSUB	$3.7\ 10^{-10}$ F
MO	2.7	TAUSC	0 s
ZET1	0.8	ACH	1.7
VSBT	0.75 V	KF	0
ETADS	0.6	AF	1
ETAGAM	2	TREF	25 ^oC
ETAM	1	MULT	1
A1	0.5	**M40**	**Value**
A2	35 V	RON	$\frac{1}{49.5W+1.28\ 10^{-3}}\ \Omega$
A3	0.65	RSAT	100 kΩ
COX	$4\ 10^{-10}\ W$ F	VSAT	2.9 V
CGDO	0 F	PSAT	2
CGSO	$1.73\ 10^{-10}\ W$ F	VP	180 V
NT	0 J	TOX	0 cm
NF	0	DCH	$1.1\ 10^{16}\ cm^{-3}$
ETABET	1.4	TBOX	$0.3\ 10^{-6}$ cm
STVTO	$-3.3\ 10^{-3}\ ^oC^{-1}$	CGATE	0 F
		CBOX	$1.8\ 10^{-10}\ W$ F
		TAUSC	0 s
		ACH	1.7
		TREF	25 ^oC
		MULT	1

Table B.5: *Optimised parameter set for the MV LDMOS.*

$$** \qquad f_W = \frac{1}{W} - \frac{1}{20\ 10^{-6}}$$

Appendix C

Model Description

C.1 Model Card

A model card specifying the SOI LDMOS parameters in the Simetrix implementation of SPICE3 has the following general format:

`.MODEL MNAME [NDSOI/PDSOI] <LEVEL=VAL>` ...*model parameters* ...

After the model name MNAME, the parameter NDSOI or PDSOI must be specified to indicate that the model is used for either an N-channel or P-channel SOI LDMOS respectively. After this comes a list of model parameters which are assigned values via the format

parameter_name `= VAL.`

Table C.1 on the following page gives the names, descriptions, symbols and default values for all parameters of the SOI LDMOS model.

Name	Symbol	Parameter	Units	Default
LEVEL	-	model index	-	6
SWITCH	-	0 for geometrical parameter set	-	0
TNOM	T_{nom}	parameter measurement temperature	°C	27
TOF	t_{of}	front oxide thickness	m	required
TOB	t_{ob}	back oxide thickness	m	required
TB	t_{b}	silicon film thickness	m	required
TBDR	t_{bdr}	silicon film thickness in the drift region	m	required
TPG	-	type of gate material: 1 N type -1 P type 0 aluminium gate	-	1
L	L	length of the under-diffusion under the gate	m	required
LD	L_{D}	lateral diffusion	m	0
LDROV	L_{drov}	overlap of the front gate over the drift region	m	0
NQFF	N_{QFF}	front fixed charge density	cm^{-2}	0
NQFB	N_{QFB}	back fixed charge density	cm^{-2}	0
NSSF	D_{itf}	front fast surface state density	$\mathrm{cm}^{-2}\mathrm{eV}^{-1}$	0
NSSB	D_{itb}	back fast surface state density	$\mathrm{cm}^{-2}\mathrm{eV}^{-1}$	0
NSUB	N_{As}	silicon film doping concentration	cm^{-3}	required
DOPGRAD	k_{N_A}	doping gradient coefficient (set to 0 if $< 10^{-2}$)	-	0
PHIB	ϕ_{nom}	surface potential ($= 2\phi_{\mathrm{Fnom}}$)	V	derived †
GAMMA0	γ_0	body factor	$\mathrm{V}^{\frac{1}{2}}$	derived †
GAMMAB	γ^{b}	body factor at the back gate	$\mathrm{V}^{\frac{1}{2}}$	derived †
VTO	V_{th0nom}	zero bias threshold voltage (front)	V	derived †
DELTAL	ΔL	threshold roll-off with channel length	m	0
DELTAW	ΔW	threshold roll-up with channel width	m	0
SIGMA	σ	drain induced barrier lowering factor	m	0
VFBF	$V^{\mathrm{f}}_{\mathrm{FBnom}}$	flatband voltage (front)	V	derived †
CHIFB	χ_{FB}	flatband voltage temperature dependence	V/K	0
VT0B	V^{b}_{th0nom}	zero bias threshold voltage (back)	V	derived †
VFBB	$V^{\mathrm{b}}_{\mathrm{FBnom}}$	flatband voltage (back)	V	derived †

Table C.1: *Names, descriptions and default values for all parameters of the SOI LDMOS model.* *Continued on next page ...*

Name	Symbol	Parameter	Units	Default
U0	μ_{snom}	zero field inversion surface mobility	cm^2/Vs	600
THETA	θ	vertical field inversion mobility degradation factor	V^{-1}	0
VSAT	v_{satnom}	carrier saturation velocity	cm/s	0 ††
MEXP	m	smoothing factor	–	1
K	k	inversion mobility temperature exponent	–	1.5
UACC	μ_{accnom}	zero field accumulation surface mobility	cm^2/Vs	600
THETAACC	θ_{acc}	vertical field accumulation mobility degradation factor	V^{-1}	0
KACC	k_{acc}	accumulation mobility temperature exponent	–	1.5
KP	-	transconductance parameter	A/V^2	derived †
LAMBDAR	λ_{r}	channel length modulation factor	m/V	0
VP	V_{p}	fitting parameter (second CLM model)	V	0 †††
LX	l_{x}	effective pinch-off region length (second CLM model)	m	0 †††
ALPHA0	α_0	first impact ionisation constant	1/cm	0
BETA0	β_0	second impact ionisation constant	V/cm	1.92E6
CHIBETA	χ_β	temperature coefficient of BETA0	V/cmK	0
ETA	η	effective field factor	–	1
LM	l_{m}	effective ionisation length	m	0
LM1	l_{m1}	LM variation with gate voltage	m/V	0
LM2	l_{m2}	LM variation with gate voltage squared	m/V^2	0
LAMBDADR	λ_{dr}	fitting factor for capacitance in saturation	-	0
NDR	N_{D}	drift region doping concentration	cm^{-3}	††††
PHIDR	ϕ_{drnom}	surface potential ($2\phi_{\text{Fdrnom}}$)	V	derived †
GAMMAFDR	γ^{fdr}	drift body factor (front)	$\text{V}^{\frac{1}{2}}$	derived †
GAMMABDR	γ^{bdr}	drift body factor (back)	$\text{V}^{\frac{1}{2}}$	derived †
VFBFDR	$V^{\text{fdr}}_{\text{FBnom}}$	drift flatband voltage (front)	V	derived †
VTODR	$V^{\text{fdr}}_{\text{th0nom}}$	zero bias drift threshold voltage (front)	V	derived †
VFBBDR	$V^{\text{bdr}}_{\text{FBnom}}$	drift flatband voltage (back)	V	derived †
VTBDR	$V^{\text{bdr}}_{\text{th0nom}}$	zero bias drift threshold voltage (back)	V	derived †
MOBDR	μ_{drnom}	mobility in the drift region	cm^2/Vs	1000
FAC	f_{v}	fitting factor for 2-D current flow under the gate	–	1
KDR	k_{dr}	drift region mobility temperature exponent	–	1.5
VSATDR	v_{satdrnom}	carrier saturation velocity in the drift region	cm/s	0 ††

continued on next page ...

Name	Symbol	Parameter	Units	Default
JSS	J_{sSnom}	S-B junction saturation current density per metre width	A/m	1e-10
ETADS	η_{DS}	S-B junction ideality coefficient	–	1
JS1S	J_{s1Snom}	second S-B junction saturation current density per metre width	A/m	0
ETAD1S	η_{D1S}	second S-B junction ideality coefficient	–	1
ISS	I_{sSnom}	S-B junction saturation current	A	derived ‡‡
IS1S	I_{s1Snom}	second S-B junction saturation current	A	derived ‡‡
CHIDS	χ_{DS}	temperature coefficient of ISS	eV.K/J	E_{g}/k
CHID1S	χ_{D1S}	temperature coefficient of IS1S	eV.K/J	E_{g}/k
CJS	C_{JS}	zero-bias S-B junction capacitance per square metre of (sidewall) junction area	F/m	0
CBS	C_{J0S}	zero bias body-source junction capacitance	F	derived ‡‡‡
PBS	PB_{Snom}	S-B junction potential	V	0.8
MJS	M_{S}	S-B junction grading coefficient	–	0.5
FCS	FC_{S}	S-B junction forward bias coefficient	–	0.5
JSD	J_{sDnom}	D-B junction saturation current density per metre width	A/m	1e-10
ETADD	η_{DD}	D-B junction ideality coefficient	–	1
JS1D	J_{s1Dnom}	second D-B junction saturation current density per metre width	A/m	0
ETAD1D	η_{D1D}	second D-B junction ideality coefficient	–	1
ISD	I_{sDnom}	D-B junction saturation current	A	derived ‡‡
IS1D	I_{s1Dnom}	second D-B junction saturation current	A	derived ‡‡
CHIDD	χ_{DD}	temperature coefficient of ISD	eV.K/J	E_{g}/k
CHID1D	χ_{D1D}	temperature coefficient of IS1D	eV.K/J	E_{g}/k
DVT	χ_{ϕ}	switch for ϕ_{t} temperature dependence (diodes only)	–	1
CJD	C_{JD}	zero-bias D-B junction capacitance per square metre of (sidewall) junction area	F/m	0
CBD	C_{J0D}	zero bias body-drain junction capacitance	F	derived ‡‡‡
PBD	PB_{Dnom}	D-B junction potential	V	0.8
MJD	M_{D}	D-B junction grading coefficient	–	0.5
FCD	FC_{D}	D-B junction forward bias coefficient	–	0.5
BETABJTR	β_{BJTr}	parasitic bipolar current gain parameter	m^2	0
TAUF	τ_{F}	bipolar forward transit time	s	0
TAUR	τ_{R}	bipolar reverse transit time	s	0

continued on next page ...

Name	Symbol	Parameter	Units	Default
RSH	R_{sh}	drain and source diffusion sheet resistance	Ω/sq	0
NRS	-	source squares	-	0
NRD	-	drain squares	-	0
RD	R_{D}	drain series resistance	Ω	derived ‡
RS	R_{S}	source series resistance	Ω	derived ‡
NLEV	-	1/f noise model level: 0 $1/f$ $(\text{KF} \,.\, I_{\text{D}}^{\text{AF}})/(L^2 \,.\, C_{of})$ 1 $1/f$ $(\text{KF} \,.\, I_{\text{D}}^{\text{AF}})/(W \,.\, L \,.\, C_{of})$ 2 $1/f^{\text{AF}}$ $(\text{KF} \,.\, g_{\text{m}}^2)/(W \,.\, L \,.\, C_{of})$	–	0
AF	-	1/f noise exponent	–	1
KF	-	1/f noise coefficient	see NLEV	0
CGFSOR	C_{gfsor}	front gate-source overlap capacitance per metre channel width	F/m	0
CGFDOR	C_{gfdor}	front gate-drain overlap capacitance per metre channel width (for LV LDMOS)	F/m	0
CGFBOR	C_{gfbor}	front gate-bulk overlap capacitance per metre channel length	F/m	0
CGBSOR	C_{gbsor}	back gate-source overlap capacitance per metre channel width	F/m	0
CGBDOR	C_{gbdor}	back gate-drain overlap capacitance per metre channel width	F/m	0
CGBBOR	C_{gbbor}	back gate-bulk overlap capacitance per metre channel length	F/m	0
KOX	κ_{ox}	oxide thermal conductivity factor	V.A/mK	0
TCF	TCF	thermal capacitance factor	V.A.s/m^3K	0

† When not given, an estimate is derived from other model parameters.

†† A value of 0 is a switch to exclude velocity saturation effects.

††† To select the second channel length modulation model, specify VP and LX *and do not specify* LAMBDA.

†††† if NDR is given this parameter is not used. RSHDR is used to calculate NDR when NDR not given

‡ Calculated from the sheet resistance RSH, and NRS or NRD.

‡‡ Calculated from the current density JS or JS1, and the channel width.

‡‡‡ Calculated from the capacitance per unit area CJ, the channel width and the film thickness.

C.2 Element Card

An element card specifying an SOI LDMOSFET modelled in Simetrix has the following format:

```
Yxxxx ND NGf NS NGb NB NT MNAME <W=VAL> <LDR=VAL>
+ <NRD=VAL> <NRS=VAL> <RT=VAL> <CT=VAL>
+ <IC=VDS,VGfS,VGbS,VBS> <OFF> <TEMP=T>
```

Very few letters of the alphabet remained unused by the normal SPICE program. As the letter S is used by a SOS model developed previously at Southampton University and the letter A is used for the STAG model, it was decided to use the letter Y to denote an LDMOS SOI device. ND, NGf, NS, NGb and NB are the drain, front gate, source, back gate (substrate) and body contact respectively. NT is the thermal node representing the local MOSFET temperature rise, and can be used to construct a thermal netlist. Both NT and NB can be left floating by specifying dummy node names. SPICE3 allows the node names to be alphanumeric, so a useful convention may be to have thermal nodes called T1, T2, ...etc.

MNAME is the model name. W and LDR are the nominal gate width and the nominal length of the drift region of the device respectively, given in metres. If W or LDR are not given, default values are used. NRD and NRS are the equivalent number of squares of the drain and source respectively and both default to 1. These are used with RSH in the **.MODEL** card to obtain the drain and source resistances. RT and CT are the (first order) thermal resistance and thermal capacitance of the device. If RT is zero, simulations are carried out without self-heating. The optional IC and OFF statements are for use in transient analyses to allow the user to set the device initial conditions. The optional TEMP value allows the user to specify the ambient temperature of the device and overrides the temperature specification in the .OPTION control line.

C.3 Electrical Parameter set

Below a second parameter set is formulated. This set is meant to be used for an individual transistor and does not contain any width or length scaling parameters. This parameter set will be referred to as an electrical parameter set, because some of the parameters can be extracted immediately from the electrical measurements. To find the full parameter set, valid for a whole range of widths and lengths, it is convenient to extract first the electrical parameter set for every different transistor. Then the full parameter can be derived, which is valid for the whole range of geometries.

Name	Symbol	Parameter	Units	Default
LEVEL	-	model index	-	6
SWITCH	-	1 for electrical parameter set	-	0
TNOM	T_{nom}	parameter measurement temperature	°C	27
TPG	-	type of gate material: 1: N type, 2: P type, 0: Alum	-	1
VTO	V_{th0nom}	zero bias threshold voltage (front)	V	3
STVTO	χ_{FB}	temperature dependence of V_{th0}	V/K	0
KO	γ_{eff}	body factor	$\mathrm{V}^{\frac{1}{2}}$	3
DOPGRAD	k_{N_A}	doping gradient coefficient (set to 0 if $< 10^{-2}$)	-	0
PHIB	ϕ_{nom}	surface potential ($= 2\phi_{\mathrm{Fnom}}$)	V	0.8
BET	β_{nom}	inversion layer gain factor	$\mathrm{A/V}^2$	-
ETABET	k	temperature exponent of β_{nom}	–	1.5
BETACC	β_{accnom}	accumulation layer gain factor	$\mathrm{cm}^2/\mathrm{Vs}$	0
ETABETACC	k	temperature exponent of β_{accnom}	–	1.5
THE1	θ	vertical field inversion layer gain degradation factor	V^{-1}	0
THE1ACC	θ_{acc}	vertical field accumulation layer gain degradation factor	V^{-1}	0
THE3	θ_{3nom}	horizontal field mobility degradation factor	V^{-1}	0
MEXP	m	smoothing factor	–	1
LAMBDA	λ	channel length modulation factor	1/V	0
VP	V_{p}	fitting parameter (second CLM model)	V	0 †††
ALP	α	pinch-off factor (second CLM model)	-	0 †††
GAMOO	γ_{oo}	drain induced barrier lowering factor	-	0
KB	γ^{b}	body factor at the back gate	$\mathrm{V}^{\frac{1}{2}}$	-
VT0B	V^{b}_{th0nom}	zero bias threshold voltage (back)	V	-
RON	R_{onnom}	drift region on-resistance under gate oxide	Ω	0
FAC	f_{v}	fitting factor for 2-D current flow under the gate	–	1
RONDR	R_{ondrnom}	drift region on-resistance under field oxide	Ω	0
ETARONDR	k_{dr}	$R^{\mathrm{dr}}_{\mathrm{ON}}$ temperature exponent	–	1.5
PHIDR	ϕ_{drnom}	surface potential ($2\phi_{\mathrm{Fdrnom}}$)	V	-
KODR	γ^{fdr}	drift body factor (front)	$\mathrm{V}^{\frac{1}{2}}$	-
KBDR	γ^{bdr}	drift body factor (back)	$\mathrm{V}^{\frac{1}{2}}$	-
VTODR	$V^{\mathrm{fdr}}_{\mathrm{th0nom}}$	zero bias drift threshold voltage (front)	V	-
VTOBDR	$V^{\mathrm{bdr}}_{\mathrm{th0nom}}$	zero bias drift threshold voltage (back)	V	-

continued on next page ...

Name	Symbol	Parameter	Units	Default
VPDEP	V_{Pdep}	pinch-off voltage without inversion at box	V	-
THE3DR	θ_{3drnom}	horizontal field mobility degradation in the drift region	V^{-1}	0
LAMBDADR	λ_{dr}	fitting factor for capacitance in saturation	-	0
ALPHA0	α_0	first impact ionisation constant	1/cm	0
BETA0	β_0	second impact ionisation constant	V/cm	1.92E6
CHIBETA	χ_β	temperature coefficient of BETA0	V/cmK	0
ETA	η	effective field factor	–	1
LM	l_{m}	effective ionisation length	m	0
LM1	l_{m1}	LM variation with gate voltage	m/V	0
LM2	l_{m2}	LM variation with gate voltage squared	$\mathrm{m/V}^2$	0
DVT	χ_ϕ	switch for ϕ_{t} temperature dependence (diodes only)	–	1
ETADS	η_{DS}	S-B junction ideality coefficient	–	1
ETAD1S	η_{D1S}	second S-B junction ideality coefficient	–	1
ISS	I_{sSnom}	S-B junction saturation current	A	0
IS1S	I_{s1Snom}	second S-B junction saturation current	A	0
CHIDS	χ_{DS}	temperature coefficient of ISS	eV.K/J	E_{g}/k
CHID1S	χ_{D1S}	temperature coefficient of IS1S	eV.K/J	E_{g}/k
CBS	C_{J0S}	zero bias body-source junction capacitance	F	0
PBS	PB_{Snom}	S-B junction potential	V	0.8
MJS	M_{S}	S-B junction grading coefficient	–	0.5
FCS	FC_{S}	S-B junction forward bias coefficient	–	0.5
ETADD	η_{DD}	D-B junction ideality coefficient	–	1
ETAD1D	η_{D1D}	second D-B junction ideality coefficient	–	1
ISD	I_{sDnom}	D-B junction saturation current	A	0
IS1D	I_{s1Dnom}	second D-B junction saturation current	A	0
CHIDD	χ_{DD}	temperature coefficient of ISD	eV.K/J	E_{g}/k
CHID1D	χ_{D1D}	temperature coefficient of IS1D	eV.K/J	E_{g}/k
CBD	C_{J0D}	zero bias body-drain junction capacitance	F	0
PBD	PB_{Dnom}	D-B junction potential	V	0.8
MJD	M_{D}	D-B junction grading coefficient	–	0.5
FCD	FC_{D}	D-B junction forward bias coefficient	–	0.5

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Name	Symbol	Parameter	Units	Default
BETABJT	β_{BJT}	parasitic bipolar current gain parameter	-	0
TAUF	τ_{F}	bipolar forward transit time	s	0
TAUR	τ_{R}	bipolar reverse transit time	s	0
RD	R_{D}	drain series resistance	Ω	0
RS	R_{S}	source series resistance	Ω	0
NLEV	-	1/f noise model level:	–	0
		0 $1/f\ (\mathrm{KF}\,.\,I_{\mathrm{D}}^{\mathrm{AF}})/(L^2\,.\,C_{of})$		
		1 $1/f\ (\mathrm{KF}\,.\,I_{\mathrm{D}}^{\mathrm{AF}})/(W\,.\,L\,.\,C_{of})$		
		2 $1/f^{\mathrm{AF}}\ (\mathrm{KF}\,.\,g_{\mathrm{m}}^2)/(W\,.\,L\,.\,C_{of})$		
AF	-	1/f noise exponent	–	1
KF	-	1/f noise coefficient	see NLEV	0
CGFSO	C_{gfso}	front gate-source overlap capacitance	F	0
CGFDO	C_{gfdo}	front gate-drain overlap capacitance (for LV LDMOS)	F	0
CGFBO	C_{gfbo}	front gate-bulk overlap capacitance	F	0
CGBSO	C_{gbso}	back gate-source overlap capacitance	F	0
CGBDO	C_{gbdo}	back gate-drain overlap capacitance	F	0
CGBBO	C_{gbbo}	back gate-bulk overlap capacitance	F	0
COXINV	C_{oxinv}	inversion gate oxide capacitance	F	0
COXACC	C_{oxacc}	accumulation gate oxide capacitance	F	0

††† To select the second channel length modulation model, specify VP and LX *and do not specify* LAMBDA.

C.4 Conversion from Geometrical to Electrical Parameter Set

C.4.1 Calculation of Some Temperature Independent Parameters

$$C_{\mathrm{of}} = \frac{3.9 \cdot \epsilon_0}{t_{\mathrm{of}}} \tag{C.1}$$

$$C_{\mathrm{ob}} = \frac{3.9 \cdot \epsilon_0}{t_{\mathrm{ob}}} \tag{C.2}$$

$$C_{\mathrm{ssf}} = q \cdot D_{\mathrm{itf}} \tag{C.3}$$

$$C_{\mathrm{ssb}} = q \cdot D_{\mathrm{itb}} \tag{C.4}$$

$$\eta_{\mathrm{s}} = 1 + \frac{C_{\mathrm{ssf}}}{C_{\mathrm{of}}} \tag{C.5}$$

$$\text{If } \gamma_0 \text{ is not given: } \gamma_0 = \frac{\sqrt{2q\epsilon_{si} \cdot N_{As}}}{C_{of}} \tag{C.6}$$

$$\text{If } \gamma^b \text{ is not given: } \gamma^b = \frac{\sqrt{2q\,\epsilon_{si} \cdot N_{As}}}{C_{ob}} \tag{C.7}$$

$$\text{If } V_{Pdep} \text{ is not given: } V_{Pdep} = \frac{qN_D t_{bdr}}{C_{ob}} \tag{C.8}$$

$$\text{If } N_D \text{ is not given: } N_D = \frac{1}{q \cdot R_{shdr} \cdot \mu_{drnom} \cdot t_{bdr}} \tag{C.9}$$

$$\text{If } \gamma^{fdr} \text{ is not given: } \gamma^{fdr} = \frac{\sqrt{2q\epsilon_{si} \cdot N_D}}{C_{of}} \tag{C.10}$$

$$\text{If } \gamma^{bdr} \text{ is not given: } \gamma^{bdr} = \frac{\sqrt{2q\,\epsilon_{si} \cdot N_D}}{C_{ob}} \tag{C.11}$$

$$\text{If } C_{JOS/D} \text{ is not given: } C_{JOS/D} = W \cdot C_{JS/D} \tag{C.12}$$

If the current densities per metre width are given:

$$I_{sS/D} = W \cdot J_{sS/Dnom} \tag{C.13}$$

$$I_{s1S/D} = W \cdot J_{s1S/Dnom} \tag{C.14}$$

$$L_{eff} = L - L_D \tag{C.15}$$

$$\gamma_{eff} = \gamma_0(1 - \frac{\Delta L}{L_{eff}})(1 - \frac{\Delta W}{W}) \tag{C.16}$$

$$\gamma_{oo} = \frac{\sigma}{L_{eff}} \tag{C.17}$$

$$\lambda = \frac{\lambda_r}{L_{eff}} \tag{C.18}$$

$$\alpha = \frac{l_x}{L_{eff}} \tag{C.19}$$

$$\beta_{BJT} = \frac{\beta_{BJTr}}{L_{eff}^2} \tag{C.20}$$

C.4.2 Calculation of the Temperature Dependent Parameters at the Nominal Temperature

First all the parameters are calculated at the nominal temperature, which is the parameter measurement temperature. The extension "$_{nom}$" was added to the subscript of these quantities.

$$\beta_{nom} = \frac{W}{L_{eff}} \mu_{snom}\, C_{of} \tag{C.21}$$

$$\beta_{accnom} = \frac{W}{L_{drov}} \mu_{accnom}\, C_{of} \tag{C.22}$$

$$\theta_{3\mathrm{nom}} = \frac{\mu_{\mathrm{snom}}}{v_{\mathrm{satnom}}\, L_{\mathrm{eff}}} \tag{C.23}$$

$$R_{\mathrm{onnom}} = \frac{L_{\mathrm{drov}}}{q\, W\, \mu_{\mathrm{drnom}}\, N_{\mathrm{D}}\, t_{\mathrm{b}}} \tag{C.24}$$

$$R_{\mathrm{ondrnom}} = \frac{L_{\mathrm{dr}}}{q\, W\, \mu_{\mathrm{drnom}}\, N_{\mathrm{D}}\, t_{\mathrm{bdr}}} \tag{C.25}$$

$$\theta_{3\mathrm{drnom}} = \frac{\mu_{\mathrm{drnom}}}{v_{\mathrm{satdrnom}}\, L_{\mathrm{dr}}} \tag{C.26}$$

$$E_{\mathrm{gnom}} = \left(1.16 - \frac{7.02\ 10^{-4} \cdot T_{\mathrm{nom}}^2}{T_{\mathrm{nom}} + 1108}\right)\ eV \tag{C.27}$$

$$\phi_{\mathrm{tnom}} = \frac{k \cdot T_{\mathrm{nom}}}{q} \tag{C.28}$$

$$\text{If } \phi \text{ not given: } \phi_{\mathrm{Fnom}} = \phi_{\mathrm{tnom}} \ln\left(\frac{N_{\mathrm{As}}}{n_{\mathrm{inom}}}\right) \tag{C.29}$$

$$\text{If } V^{\mathrm{f}}_{\mathrm{FBnom}} \text{ not given: } V^{\mathrm{f}}_{\mathrm{FBnom}} = -\mathtt{TPG} \cdot \frac{E_{\mathrm{g}}}{2\, q} - \mathtt{TP} \cdot \phi_{\mathrm{Fnom}} - \frac{q \cdot N_{\mathrm{QFF}}}{C_{\mathrm{of}}} \tag{C.30}$$

$$\text{If } V_{\mathrm{th0nom}} \text{ given: } V^{\mathrm{f}}_{\mathrm{FBnom}} = V_{\mathrm{th0nom}} - \mathtt{TP}(\eta_{\mathrm{s}} 2\phi_{\mathrm{Fnom}} + \gamma_0 \sqrt{2\phi_{\mathrm{Fnom}}}) \tag{C.31}$$

$$\text{If } V^{\mathrm{b}}_{\mathrm{FBnom}} \text{ not given: } V^{\mathrm{b}}_{\mathrm{FBnom}} = -(1 + \mathtt{TP}) \cdot \phi_{\mathrm{Fnom}} - \frac{q \cdot N_{\mathrm{QFB}}}{C_{\mathrm{ob}}} \tag{C.32}$$

$$\text{If } V^{b}_{\mathrm{th0nom}} \text{ given: } V^{\mathrm{b}}_{\mathrm{FBnom}} = V^{b}_{\mathrm{th0nom}} + \mathtt{TP} \cdot (\eta_{\mathrm{s}}\, 2\phi_{\mathrm{Fnom}} + \gamma^{\mathrm{b}}\, \sqrt{2\phi_{\mathrm{Fnom}}}) \tag{C.33}$$

$$\text{If } \phi_{\mathrm{dr}} \text{ not given: } \phi_{\mathrm{Fdrnom}} = \phi_{\mathrm{tnom}} \ln\left(\frac{N_{\mathrm{D}}}{n_{\mathrm{inom}}}\right) \tag{C.34}$$

$$\text{If } V^{\mathrm{fdr}}_{\mathrm{FBnom}} \text{ not given: } V^{\mathrm{fdr}}_{\mathrm{FBnom}} = -\mathtt{TPG} \cdot \frac{E_{\mathrm{g}}}{2\, q} + \mathtt{TP} \cdot \phi_{\mathrm{Fdrnom}} - \frac{q \cdot N_{\mathrm{QFF}}}{C_{\mathrm{of}}} \tag{C.35}$$

$$\text{If } V^{\mathrm{fdr}}_{\mathrm{th0nom}} \text{ given: } V^{\mathrm{fdr}}_{\mathrm{FBnom}} = V^{\mathrm{fdr}}_{\mathrm{th0nom}} + \mathtt{TP}(\eta_{\mathrm{s}} 2\phi_{\mathrm{Fdrnom}} + \gamma_{fdr} \sqrt{2\phi_{\mathrm{Fdrnom}}}) \tag{C.36}$$

$$\text{If } V^{\mathrm{bdr}}_{\mathrm{FBnom}} \text{ not given: } V^{\mathrm{bdr}}_{\mathrm{FBnom}} = -(1 - \mathtt{TP}) \cdot \phi_{\mathrm{Fdrnom}} - \frac{q \cdot N_{\mathrm{QFB}}}{C_{\mathrm{ob}}} \tag{C.37}$$

$$\text{If } V^{\mathrm{bdr}}_{\mathrm{th0}} \text{ given: } V^{\mathrm{bdr}}_{\mathrm{FBnom}} = V^{\mathrm{bdr}}_{\mathrm{th0nom}} + \mathtt{TP} \cdot (\eta_{\mathrm{s}}\, 2\phi_{\mathrm{Fdrnom}} + \gamma^{\mathrm{bdr}}\, \sqrt{2\phi_{\mathrm{Fdrnom}}}) \tag{C.38}$$

C.5 Parameter Preprocessing from electrical parameter set

C.5.1 Calculation of the Temperature Dependent Electrical Parameters at the Nominal Temperature

In this section the parameters are calculated at the nominal temperature, which is the parameter measurement temperature. The extension "$_{\mathrm{nom}}$" was added to the subscript of these quantities.

$$V^{\mathrm{f}}_{\mathrm{FBnom}} = V_{\mathrm{th0nom}} - \mathtt{TP}(\eta_{\mathrm{s}} 2\phi_{\mathrm{Fnom}} + \gamma_0 \sqrt{2\phi_{\mathrm{Fnom}}}) \tag{C.39}$$

$$V^{\mathrm{b}}_{\mathrm{FBnom}} = V^{b}_{\mathrm{th0nom}} + \mathtt{TP} \cdot (\eta_{\mathrm{s}}\, 2\phi_{\mathrm{Fnom}} + \gamma^{\mathrm{b}}\, \sqrt{2\phi_{\mathrm{Fnom}}}) \tag{C.40}$$

$$V^{\mathrm{fdr}}_{\mathrm{FBnom}} = V^{\mathrm{fdr}}_{\mathrm{th0nom}} + \mathtt{TP}(\eta_{\mathrm{s}} 2\phi_{\mathrm{Fdrnom}} + \gamma^{\mathrm{fdr}} \sqrt{2\phi_{\mathrm{Fdrnom}}}) \tag{C.41}$$

$$V^{\mathrm{bdr}}_{\mathrm{FBnom}} = V^{\mathrm{bdr}}_{\mathrm{th0nom}} + \mathtt{TP} \cdot (\eta_{\mathrm{s}}\, 2\phi_{\mathrm{Fdrnom}} + \gamma^{\mathrm{bdr}}\, \sqrt{2\phi_{\mathrm{Fdrnom}}}) \tag{C.42}$$

C.5.2 Calculation of the Temperature Dependent Electrical Parameters at the Ambient Temperature

Now an adjustment is performed from T_{nom} to TEMP($= T_{\mathrm{amb}}$), the ambient temperature given in the instance line of a device. This adjustment is done for all the temperature dependent instance parameters used in the model equations.

$$E_{\mathrm{g}} = \left(1.16 - \frac{7.02\,10^{-4} \cdot T_{\mathrm{amb}}^2}{T_{\mathrm{amb}} + 1108}\right) \mathrm{eV} \tag{C.43}$$

$$\phi_{\mathrm{t}} = \frac{k \cdot T_{\mathrm{amb}}}{q} \tag{C.44}$$

The Diodes and BJT Parameters

$$\text{If } \chi_{\mathrm{DS/D}} \text{ is not given: } \chi_{\mathrm{DS/D}} = \frac{E_{\mathrm{g}}}{k} \tag{C.45}$$

$$\text{If } \chi_{\mathrm{D1S/D}} \text{ is not given: } \chi_{\mathrm{D1S/D}} = \frac{E_{\mathrm{g}}}{k} \tag{C.46}$$

$$I_{\mathrm{sS/D}}(T_{\mathrm{amb}}) = I_{\mathrm{sS/Dnom}} \cdot \exp(-\frac{E_{\mathrm{g}}}{q\,\phi_{\mathrm{t}}} + \frac{E_{\mathrm{gnom}}}{q\,\phi_{\mathrm{tnom}}}) \tag{C.47}$$

$$I_{\mathrm{s1S/D}}(T_{\mathrm{amb}}) = I_{\mathrm{s1S/Dnom}} \cdot \exp(-\frac{E_{\mathrm{g}}}{q\,\phi_{\mathrm{t}}} + \frac{E_{\mathrm{gnom}}}{q\,\phi_{\mathrm{tnom}}}) \tag{C.48}$$

$$PB_{\mathrm{S/D}} = \left(PB_{\mathrm{S/Dnom}} - \phi_{\mathrm{tnom}}\left(-1.5 \cdot \ln(\frac{T_{\mathrm{nom}}}{T_{\mathrm{amb}}}) + \frac{1}{2k}(\frac{E_{\mathrm{gnom}}}{T_{\mathrm{nom}}} - \frac{E_{\mathrm{g}}}{T_{\mathrm{amb}}})\right)\right) \cdot \frac{T_{\mathrm{nom}}}{T_{\mathrm{amb}}} \tag{C.49}$$

The Channel and Drift current Parameters

$$\beta(T_{\mathrm{amb}}) = \beta_{\mathrm{nom}} \cdot \left(\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}}\right)^{-k} \tag{C.50}$$

$$\beta_{\mathrm{acc}}(T_{\mathrm{amb}}) = \beta_{\mathrm{accnom}} \cdot \left(\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}}\right)^{-k_{\mathrm{acc}}} \tag{C.51}$$

$$R_{\mathrm{ON}}(T_{\mathrm{amb}}) = R_{\mathrm{onnom}} \cdot \left(\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}}\right)^{k_{\mathrm{dr}}} \tag{C.52}$$

$$R_{\mathrm{ON}}^{\mathrm{dr}}(T_{\mathrm{amb}}) = R_{\mathrm{ondrnom}} \cdot \left(\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}}\right)^{k_{\mathrm{dr}}} \tag{C.53}$$

$$\theta_3(T_{\mathrm{amb}}) = \theta_{3\mathrm{nom}} \cdot \left(\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}}\right)^{-k} \cdot \frac{1 + 0.8 \exp\frac{T_{\mathrm{amb}}}{600}}{1 + 0.8 \exp\frac{T_{\mathrm{nom}}}{600}} \tag{C.54}$$

$$\theta_{3\mathrm{dr}}(T_{\mathrm{amb}}) = \theta_{3\mathrm{drnom}} \cdot \left(\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}}\right)^{-kdr} \cdot \frac{1+0.8\exp\frac{T_{\mathrm{amb}}}{600}}{1+0.8\exp\frac{T_{\mathrm{nom}}}{600}} \tag{C.55}$$

$$\phi_{\mathrm{F}} = \phi_{\mathrm{Fnom}}\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}} \tag{C.56}$$

$$V_{\mathrm{FB}}^{\mathrm{f}}(T_{\mathrm{amb}}) = V_{\mathrm{FBnom}}^{\mathrm{f}} + \mathtt{TPG} \cdot \frac{E_{\mathrm{gnom}} - E_{\mathrm{g}}}{2\,q} + \mathtt{TP} \cdot (\phi_{\mathrm{Fnom}} - \phi_{\mathrm{F}}) \tag{C.57}$$

$$V_{\mathrm{FB}}^{\mathrm{b}} = V_{\mathrm{FBnom}}^{\mathrm{b}} + (1+\mathtt{TP}) \cdot (\phi_{\mathrm{Fnom}} - \phi_{\mathrm{F}}) \tag{C.58}$$

$$\phi_{\mathrm{Fdr}} = \phi_{\mathrm{Fdrnom}}\frac{T_{\mathrm{amb}}}{T_{\mathrm{nom}}} \tag{C.59}$$

$$V_{\mathrm{FB}}^{\mathrm{fdr}} = V_{\mathrm{FBnom}}^{\mathrm{fdr}} + \mathtt{TPG} \cdot \frac{E_{\mathrm{gnom}} - E_{\mathrm{g}}}{2\,q} - \mathtt{TP} \cdot (\phi_{\mathrm{Fdrnom}} - \phi_{\mathrm{Fdr}}) \tag{C.60}$$

$$V_{\mathrm{FB}}^{\mathrm{bdr}} = V_{\mathrm{FBnom}}^{\mathrm{bdr}} + (1-\mathtt{TP}) \cdot (\phi_{\mathrm{Fdrnom}} - \phi_{\mathrm{Fdr}}) \tag{C.61}$$

C.5.3 Inclusion of Self and Coupled Heating for the Major Temperature Dependent Model Parameters

The local self- and coupled heating induced temperature rise ΔT is used to modify the values of only those parameters which have a major contribution to the device behaviour. This is because this operation has to be performed at each Newton-Raphson iteration and making the relations very complex would result in a severely increased computation time.

The Channel and Drift Current Parameters

$$\beta = \beta(T_{\mathrm{amb}}) \cdot \left(1+\frac{\Delta T}{T_{\mathrm{amb}}}\right)^{-k} \tag{C.62}$$

$$\beta_{\mathrm{acc}} = \beta_{\mathrm{acc}}(T_{\mathrm{amb}}) \cdot \left(1+\frac{\Delta T}{T_{\mathrm{amb}}}\right)^{-k_{\mathrm{acc}}} \tag{C.63}$$

$$R_{\mathrm{ON}}^{\mathrm{dr}} = R_{\mathrm{ON}}^{\mathrm{dr}}(T_{\mathrm{amb}}) \cdot \left(1+\frac{\Delta T}{T_{\mathrm{amb}}}\right)^{k_{\mathrm{dr}}} \tag{C.64}$$

$$R_{\mathrm{ON}} = R_{\mathrm{ON}}(T_{\mathrm{amb}}) \cdot \left(1+\frac{\Delta T}{T_{\mathrm{amb}}}\right)^{k_{\mathrm{dr}}} \tag{C.65}$$

$$\theta_3 = \theta_{3\mathrm{nom}} \cdot \left(1+\frac{\Delta T}{T_{\mathrm{amb}}}\right)^{-k} \cdot \frac{1+0.8\exp\frac{T_{\mathrm{amb}}+\Delta T}{600}}{1+0.8\exp\frac{T_{\mathrm{amb}}}{600}} \tag{C.66}$$

$$\theta_{3\mathrm{dr}} = \theta_{3\mathrm{drnom}} \cdot \left(1+\frac{\Delta T}{T_{\mathrm{amb}}}\right)^{-kdr} \cdot \frac{1+0.8\exp\frac{T_{\mathrm{amb}}+\Delta T}{600}}{1+0.8\exp\frac{T_{\mathrm{amb}}}{600}} \tag{C.67}$$

$$V_{\mathrm{FB}}^{\mathrm{f}} = V_{\mathrm{FB}}^{\mathrm{f}}(T_{\mathrm{amb}}) + \chi_{\mathrm{FB}} \cdot \Delta T \tag{C.68}$$

The Diode and BJT Parameters

$$I_{\mathrm{sS/D}} = I_{\mathrm{sS/D}}(T_{\mathrm{amb}}) \cdot \exp\left(\frac{\chi_{\mathrm{DS/D}}}{T_{\mathrm{amb}}} \cdot \frac{\Delta T}{T_{\mathrm{amb}} + \Delta T}\right) \tag{C.69}$$

$$I_{\mathrm{s1S/D}} = I_{\mathrm{s1S/D}}(T_{\mathrm{amb}}) \cdot \exp\left(\frac{\chi_{\mathrm{D1S/D}}}{T_{\mathrm{amb}}} \cdot \frac{\Delta T}{T_{\mathrm{amb}} + \Delta T}\right) \tag{C.70}$$

$$\phi_{\mathrm{T}} = \frac{k(T_{\mathrm{amb}} + \chi_{\phi}\Delta T)}{q} \tag{C.71}$$

$$\beta_{\mathrm{M}} = \beta_0 + \chi_{\beta} \cdot \Delta T \tag{C.72}$$

C.6 Smoothing Functions

The constant M_{exp} used in this section represents the maximum argument allowable in the exponential function when floating point variables are used.

$$\text{pos}_{\text{sm}}(x, \epsilon_1, \epsilon_2) = \begin{cases} \epsilon_1 \ln\left[1 + \exp(\frac{x}{\epsilon_1})\right] + \epsilon_2 & \text{if } x < (\epsilon_1\, M_{\text{exp}}) \\ x + \epsilon_2 & \text{otherwise} \end{cases} \tag{C.73}$$

$$\min_{\text{sm}}(x, y, \epsilon) = \begin{cases} \epsilon \ln\left[1 + \frac{\exp(\frac{x}{\epsilon})}{1+\exp(\frac{x-y}{\epsilon})}\right] & \text{if } x - y < (\epsilon\, M_{\text{exp}}) \text{ and } x < (\epsilon\, M_{\text{exp}}) \\ x - \epsilon \ln\left[1 + \exp(\frac{x-y}{\epsilon})\right] & \text{if } x - y < (\epsilon\, M_{\text{exp}}) \text{ and } x > (\epsilon\, M_{\text{exp}}) \\ y & \text{otherwise} \end{cases} \tag{C.74}$$

$$\min_{\text{smsp}}(x, y, \epsilon) = \begin{cases} \epsilon \ln\left[1 + \frac{\exp(\frac{x}{\epsilon})}{1+\exp(\frac{x-y}{\epsilon})}\right] - 0.68\epsilon & \text{if } x - y < (\epsilon\, M_{\text{exp}}) \text{ and } x < (\epsilon\, M_{\text{exp}}) \\ x - \epsilon \ln\left[1 + \exp(\frac{x-y}{\epsilon})\right] & \text{if } x - y < (\epsilon\, M_{\text{exp}}) \text{ and } x > (\epsilon\, M_{\text{exp}}) \\ y & \text{otherwise} \end{cases} \tag{C.75}$$

$$\min_{\text{sm1}}(x, y, \epsilon) = \begin{cases} x - \epsilon \ln\left[1 + \exp(\frac{x-y}{\epsilon})\right] & \text{if } x - y < (\epsilon\, M_{\text{exp}}) \\ y & \text{otherwise} \end{cases} \tag{C.76}$$

$$\min_{\text{sm2}}(x, y, \epsilon) = \begin{cases} x + \epsilon\, \ln\left[\frac{\exp\left(-\frac{y}{\epsilon}\right)+1}{\exp\left(\frac{x-y}{\epsilon}\right)+1}\right] & \text{if } x - y < (\epsilon\, M_{\text{exp}}) \\ y - \epsilon\, \ln\left[1 + \exp(-\frac{y}{\epsilon})\right] & \text{otherwise} \end{cases} \tag{C.77}$$

$$\max_{\text{hyp}}(x, y, \epsilon) = x - 0.5\left((x - y) - \sqrt{(x - y)^2 + 4\epsilon^2}\right) \tag{C.78}$$

$$\min_{\text{hyp}}(x, y, \epsilon) = x - 0.5\left((x - y) + \sqrt{(x - y)^2 + 4\epsilon^2}\right) \tag{C.79}$$

$$\min_{\text{sat}}(x, y, m) = \frac{xy}{(x^{2m} + y^{2m})^{1/2m}} \tag{C.80}$$

C.7 The LV LDMOS Current

The subsections are entitled as block numbers, which correspond to the different blocks in the code.

The equations below are for $V_{\mathrm{DiS}} > 0$. If $V_{\mathrm{DiS}} < 0$, V_{DiB} and V_{SB} have to be swapped.

C.7.1 Block 1A

$$\gamma_{\mathrm{L}} = \gamma_{\mathrm{eff}} \exp(-\frac{k_{\mathrm{N}_A}}{2}) \tag{C.81}$$

$$\gamma_{\mathrm{m}} = \frac{\gamma_{\mathrm{L}} + \gamma_{\mathrm{eff}}}{2} \tag{C.82}$$

$$V_{\mathrm{FBeff}} = V_{\mathrm{FB}}^{\mathrm{f}} - \gamma_{\mathrm{oo}} V_{\mathrm{DiS}} \tag{C.83}$$

$$V_{\mathrm{g}} = V_{\mathrm{GfB}} - V_{\mathrm{FBeff}} \tag{C.84}$$

$$V_{\mathrm{gy}} = \mathrm{pos}_{\mathrm{sm}}(V_{\mathrm{g}}, \phi_{\mathrm{t}}, 1E-25) \tag{C.85}$$

$$\phi = \mathrm{MIN}(2\phi_{\mathrm{F}}, 2\phi_{\mathrm{Fdr}}) - 0.1 \tag{C.86}$$

$$V_{\mathrm{sby}} = \mathrm{pos}_{\mathrm{sm}}(V_{\mathrm{SB}} + \phi, \phi_{\mathrm{t}}, 0) - \phi \tag{C.87}$$

C.7.2 Block 1B

$$\psi_{\mathrm{ss0}} = \left[-\frac{\gamma_{\mathrm{eff}}}{2\eta_{\mathrm{s}}} + \sqrt{\frac{\gamma_{\mathrm{eff}}^2}{4\eta_{\mathrm{s}}^2} + \frac{V_{\mathrm{gy}}}{\eta_{\mathrm{s}}}} \right]^2 \tag{C.88}$$

$$A = 2\phi_{\mathrm{F}} + V_{\mathrm{sby}} \tag{C.89}$$

$$V_{\mathrm{gconst}} = \eta_{\mathrm{s}} A - \phi_{\mathrm{t}}(\eta_{\mathrm{s}} - 1) + \gamma_{\mathrm{eff}}\sqrt{A} \tag{C.90}$$

$$V_{\mathrm{gx}} = \mathrm{pos}_{\mathrm{sm}}(V_{\mathrm{g}} - V_{\mathrm{gconst}}, 5\phi_{\mathrm{t}}, 0) + V_{\mathrm{gconst}} \tag{C.91}$$

$$T_{\mathrm{log0}} = \frac{1}{\phi_{\mathrm{t}}} \left[\frac{1}{\gamma_{\mathrm{eff}}^2} (V_{\mathrm{gx}} - \eta_{\mathrm{s}} A)^2 - A + \phi_{\mathrm{t}} \right] \tag{C.92}$$

$$\psi_{\mathrm{si0}} = \begin{cases} A + \phi_{\mathrm{t}} \ln\left(T_{\mathrm{log0}}\right) & \text{if } T_{\mathrm{log0}} > 1 \\ A & \text{otherwise} \end{cases} \tag{C.93}$$

note: build-in protection in code for $T_{\mathrm{log0}} <= 1$

(this can only happen due to numerical problems)

$$\psi_{\mathrm{st0}} = \mathrm{min}_{\mathrm{smsp}}(\psi_{\mathrm{si0}}, \psi_{\mathrm{ss0}}, \phi_{\mathrm{t}}) \tag{C.94}$$

C.7.3 Block 1C

$$\delta = \frac{1}{2\sqrt{1 + \psi_{\mathrm{st0}}}} \tag{C.95}$$

$$g = -\frac{1}{2}\eta_{\mathrm{s}} + \gamma_{\mathrm{eff}}\ \delta\ (\frac{1}{6}\ k_{\mathrm{N}_A} - \frac{1}{2}) \tag{C.96}$$

$$f_1 = V_{\mathrm{gy}} - \gamma_{\mathrm{eff}}\ \sqrt{\psi_{\mathrm{st0}}}(1 - \frac{k_{\mathrm{N}_A}}{4}) + (1 - \frac{1}{3}\ k_{\mathrm{N}_A})\gamma_{\mathrm{eff}}\ \delta\ \psi_{\mathrm{st0}} \tag{C.97}$$

$$f_{1n} = V_{gy} - \gamma_{eff}\sqrt{\psi_{st0}} + (1 - \frac{1}{3}k_{N_A})\gamma_{eff}\,\delta\,\psi_{st0} \quad \text{(C.98)}$$

$$f_2 = \phi_t\,(\eta_s + \gamma_{eff}\delta - \frac{1}{2}\gamma_{eff}\,k_{N_A}\,\delta) \quad \text{(C.99)}$$

$$M_{mob} = -\frac{\theta}{2} + \theta_3 + \theta\,\gamma_m\,\frac{\delta}{2} \quad \text{(C.100)}$$

$$\psi = -\psi_{st0} - \frac{f_{1n}}{2g} + 0.015\phi_t + \frac{\gamma_{eff}\sqrt{\phi_t * 0.015}}{\eta_s + \gamma_{eff}\frac{0.5}{\sqrt{1+0.015\phi_t}}(1 - \frac{1}{3}k_{N_A})} \quad \text{(C.101)}$$

$$S_{fac} = pos_{sm}(1 + \frac{2\psi\,M_{mob}}{1 + \theta\,(V_{gy} - \psi_{st0}) + \theta\,\gamma_m\sqrt{\psi_{st0}}}, \phi_t, 1E-25) \quad \text{(C.102)}$$

$$S = \frac{1}{2} + \frac{1}{2}\sqrt{S_{fac}} \quad \text{(C.103)}$$

$$\psi_{sLsat} = \psi_{st0} + \frac{\psi}{S} \quad \text{(C.104)}$$

C.7.4 Block 1D

$$V_{gdry} = pos_{sm}(V_{GfB} - V_{FB}^{fdr}, \phi_t * 1E-6, 1E-25) \quad \text{(C.105)}$$

$$f_\theta = 1 + \theta(V_{gy} - \psi_{st0}) \quad \text{(C.106)}$$

$$f_\beta = \frac{f_v}{\beta\,R_{ON}} \quad \text{(C.107)}$$

$$f_{\theta acc} = \frac{1 + \theta(V_{gy} - \psi_{st0})}{1 + \theta_{acc}(V_{gy} - \psi_{sLsat})} \quad \text{(C.108)}$$

$$f_{\beta acc} = \frac{\beta_{acc}}{\beta} \quad \text{(C.109)}$$

$$F = f_\theta f_\beta + f_{\theta acc} f_{\beta acc}(V_{gy} + \psi_{si0} - V_{sby}) \quad \text{(C.110)}$$

$$G = -\frac{1}{2}\,f_{\theta acc} f_{\beta acc} \quad \text{(C.111)}$$

$$R_s = pos_{sm}\Big(\frac{F^2}{4} + G\Big(g\,(\psi_{sLsat}^2 - \psi_{st0}^2) \quad \text{(C.112)}$$

$$+(f_1 + f_2)\,(\psi_{sLsat} - \psi_{st0}) + \psi_{sLsat}(G\psi_{sLsat} + F)\Big), \phi_t, 1E-25\Big)$$

$$V_{dsat} = \begin{cases} \frac{1}{G}(-\frac{F}{2} + \sqrt{R_s}) - \psi_{st0} + \phi_t * 0.015 & \text{if } \beta_{acc} > 0 \\ \psi_{sLsat} - \psi_{st0} + \phi_t * 0.015 & \text{otherwise} \end{cases} \quad \text{(C.113)}$$

$$V_{DiSn} = min_{sat}(V_{DiS}, V_{dsat}, m) \quad \text{(C.114)}$$

$$V_{DiBn} = V_{DiSn} + V_{sby} \quad \text{(C.115)}$$

C.7.5 Block 1E

$$\psi_{s0} = min_{sm}(\psi_{si0}, \psi_{sLsat}, \phi_t) \quad \text{(C.116)}$$

C.7.6 Block 1F

$$A = g + G \tag{C.117}$$

$$B = (f_1 + f_2) + F \tag{C.118}$$

$$C = -(g\ \psi_{\mathrm{si0}}^2 + (f_1 + f_2)\ \psi_{\mathrm{si0}}) - F(V_{\mathrm{DiSn}} + \psi_{\mathrm{si0}}) - G(V_{\mathrm{DiSn}} + \psi_{\mathrm{si0}})^2 \tag{C.119}$$

$$R_{\mathrm{acc}} = \mathrm{pos}_{\mathrm{sm}}(\frac{B^2}{4} - AC, \phi_{\mathrm{t}} * 1E-6, 1E-25) \tag{C.120}$$

$$\psi_{\mathrm{siL}} = \frac{-\frac{B}{2} + \sqrt{R_{\mathrm{acc}}}}{A} \tag{C.121}$$

$$\psi_{\mathrm{sL}} = \mathrm{min}_{\mathrm{sm}}(\psi_{\mathrm{siL}}, \psi_{\mathrm{sLsat}}, \phi_{\mathrm{t}}) \tag{C.122}$$

$$f_{\mathrm{eff}} = \frac{1}{1 + \theta\left[V_{\mathrm{gy}} - \frac{\psi_{\mathrm{sL}} + \psi_{\mathrm{s0}}}{2} + \gamma_{\mathrm{m}}(\sqrt{\psi_{\mathrm{st0}}} + \frac{\delta}{2}(\psi_{\mathrm{sL}} - \psi_{\mathrm{s0}}))\right] + \theta_3(\psi_{\mathrm{sL}} - \psi_{\mathrm{s0}})} \tag{C.123}$$

$$I_{\mathrm{CH0}} = \beta\ f_{\mathrm{eff}}\ [g\ (\psi_{\mathrm{sL}}^2 - \psi_{\mathrm{s0}}^2) + (f_1 + f_2)\ (\psi_{\mathrm{sL}} - \psi_{\mathrm{s0}})] \tag{C.124}$$

$$f_{\mathrm{l}_d} = \begin{cases} \lambda\,(V_{\mathrm{DiS}} - V_{\mathrm{DiSn}}) & \text{if } \lambda \text{ given.} \\ \alpha\ \ln\left(1 + \frac{(V_{\mathrm{DiS}} - V_{\mathrm{DiSn}})}{V_{\mathrm{p}}}\right) & \text{otherwise} \end{cases} \tag{C.125}$$

$$I_{\mathrm{CH}} = I_{\mathrm{CH0}}\ (1 + f_{\mathrm{l}_d}) \tag{C.126}$$

C.8 The Drift Region Current Under the Field Oxide

$$\delta_{\mathrm{dr}} = \frac{1}{2\sqrt{1+2\,\phi_{\mathrm{Fdr}}}} \tag{C.127}$$

$$V_{\mathrm{satinv}} = \frac{V_{\mathrm{Pdep}} - \gamma^{\mathrm{bdr}}\sqrt{2\phi_{\mathrm{Fdr}}}}{\delta_{\mathrm{dr}}\,\gamma^{\mathrm{bdr}}} \tag{C.128}$$

$$V_{\mathrm{gb}} = V_{\mathrm{GbB}} - V_{\mathrm{FB}}^{\mathrm{bdr}} \tag{C.129}$$

$$V_{\mathrm{gby}} = -\mathrm{pos}_{\mathrm{sm}}(-V_{\mathrm{gb}}, \phi_{\mathrm{t}}, 1E-25) \tag{C.130}$$

$$\psi_{\mathrm{i}} = \frac{\gamma^{\mathrm{bdr}}\sqrt{2\phi_{\mathrm{Fdr}}} + V_{\mathrm{gby}}}{1-\delta_{\mathrm{dr}}\gamma^{\mathrm{bdr}}} \tag{C.131}$$

$$V_{\mathrm{satdep}} = V_{\mathrm{gby}} + V_{\mathrm{Pdep}} \tag{C.132}$$

$$V_{\mathrm{Psat}} = \max_{\mathrm{hyp}}(V_{\mathrm{satinv}}, V_{\mathrm{satdep}}, 1E-25) \tag{C.133}$$

$$V_{\mathrm{DiBs}} = \min_{\mathrm{sm1}}(V_{\mathrm{DiB}}, V_{\mathrm{Psat}}, \phi_{\mathrm{t}}) \tag{C.134}$$

$$V_{\mathrm{DBst}} = \min_{\mathrm{sm1}}(V_{DB}, V_{\mathrm{Psat}}, \phi_{\mathrm{t}}) \tag{C.135}$$

$$V_{\mathrm{min}} = \psi_{\mathrm{i}} - \sqrt{\frac{2}{\theta_{3\mathrm{dr}}} * (\mathrm{pos}_{\mathrm{sm}}(V_{\mathrm{satinv}} - \psi_{\mathrm{i}}, \phi_{\mathrm{t}}, 1E-50))} \tag{C.136}$$

$$V_{\mathrm{DiB}}^{\mathrm{e}} = \max_{\mathrm{hyp}}(\min_{\mathrm{hyp}}(V_{\mathrm{DiBs}}, \psi_{\mathrm{i}}, 1E-25), V_{\mathrm{min}}, 1E-50) \tag{C.137}$$

$$R = \sqrt{\frac{1}{\theta_{3\mathrm{dr}}^2} - 2\frac{V_{\mathrm{DiBs}}}{\theta_{3\mathrm{dr}}} + 2\frac{V_{\mathrm{Psat}}}{\theta_{3\mathrm{dr}}} + (\psi_{\mathrm{i}} - V_{\mathrm{DiB}}^{\mathrm{e}})^2(1-\gamma^{\mathrm{bdr}}\delta_{\mathrm{dr}})} \tag{C.138}$$

$$V_{\mathrm{sat}} = -\frac{1}{\theta_{3\mathrm{dr}}} + R \tag{C.139}$$

$$V_{\mathrm{DDis}} = V_{\mathrm{DBst}} - V_{\mathrm{DiBs}} \tag{C.140}$$

$$V_{\mathrm{DDin}} = \min_{\mathrm{sat}}(V_{\mathrm{DDis}}, V_{\mathrm{sat}}, 6) \tag{C.141}$$

$$V_{\mathrm{DBs}} = V_{\mathrm{DiBs}} + V_{\mathrm{DDin}} \tag{C.142}$$

$$V_{\mathrm{DiBl}} = \max_{\mathrm{hyp}}(V_{\mathrm{DiBs}}, \psi_{\mathrm{i}}, 1E-50) \tag{C.143}$$

$$V_{\mathrm{DBf}} = \min_{\mathrm{hyp}}(V_{\mathrm{DBs}}, V_{\mathrm{DiBl}}, 1E-50) \tag{C.144}$$

$$f_{\mathrm{dreff}} = \frac{1}{1+\theta_{3\mathrm{dr}}(V_{\mathrm{DBs}} - V_{\mathrm{DiBs}})} \tag{C.145}$$

$$H_1 = ((V_{\mathrm{DBf}} - V_{\mathrm{DiBs}})\sqrt{2\phi_{\mathrm{Fdr}}} + \frac{\delta_{\mathrm{dr}}}{2}(V_{\mathrm{DBf}}^2 - V_{\mathrm{DiBs}}^2)) \tag{C.146}$$

$$H_2 = \frac{1}{2}((-V_{\mathrm{gby}} + V_{\mathrm{DBs}})^2 - (-V_{\mathrm{gby}} + V_{\mathrm{DBf}})^2) \tag{C.147}$$

$$I_{\mathrm{DR}} = \frac{f_{\mathrm{dreff}}}{R_{\mathrm{ON}}^{\mathrm{dr}}}\left[V_{\mathrm{DBs}} - V_{\mathrm{DiBs}} - \left(\gamma_{bdr}\frac{H_1}{V_{\mathrm{Pdep}}} + \frac{H_2}{V_{\mathrm{Pdep}}}\right)\right] \tag{C.148}$$

C.9 The Charge Equations

C.9.1 The Body Channel Charge

USE REAL VALUE for $I_{\rm CH}$: positive when $V_{\rm DS}$ is positive, and negative otherwise. DO NOT SWAP the drain and the source, if $V_{\rm DS}$ is negative!

Block 0

$$V_{\rm DiBs} = \min_{\rm sat}(V_{\rm DiB}, V_{\rm gdry} + 0.01, 2) \tag{C.149}$$

$$V_{\rm g}^{\rm dr} = V_{\rm GfB} - V_{\rm FB}^{\rm fdr} \tag{C.150}$$

$$V_{\rm sby} = {\rm pos}_{\rm sm}(V_{\rm SB} + \phi, \phi_{\rm t}, 0) - \phi \tag{C.151}$$

$$V_{\rm th} = V_{\rm FB}^{\rm f} + \mathbf{TP}(2\phi_{\rm F} + V_{\rm sby} + \gamma_{\rm eff}\sqrt{2\phi_{\rm F} + V_{\rm sby}}) \tag{C.152}$$

$$P_1 = {\rm pos}_{\rm sm}(V_{\rm GfB} - V_{\rm th}, 0.005, 10^{-25}) \tag{C.153}$$

$$P_2 = {\rm pos}_{\rm sm}(-V_{\rm GfB} + V_{\rm th}, 0.005, 10^{-25}) \tag{C.154}$$

$$V_{\rm DiBn} = \begin{cases} \frac{(P_1+P_2)V_{\rm DiB}V_{\rm DiBs}}{P_1V_{\rm DiB}+P_2V_{\rm DiBs}} & \text{if } |V_{\rm DiB}| > 10^{-10} \\ 0 & \text{otherwise, BUT DERIVATIVES NOT 0!} \end{cases} \tag{C.155}$$

$$V_{\rm dibc} = \begin{cases} V_{\rm DiBn} - \ln\left(\frac{V_{\rm DiB}}{V_{\rm DiBs}}\right)\lambda_{\rm dr}R_{\rm ON}I_{\rm CH} & \text{if } |V_{\rm DiB}| > 10^{-10} \\ V_{\rm DiBn} & \text{otherwise} \end{cases} \tag{C.156}$$

$$V_{\rm gdc}^{\rm dr} = V_{\rm g}^{\rm dr} - V_{\rm dibc} \tag{C.157}$$

$$V_{\rm gdy}^{\rm dr} = {\rm pos}_{\rm sm}(V_{\rm gdc}^{\rm dr}, 10\phi_{\rm t}, 1E-25) \tag{C.158}$$

$$h_1 = \frac{f_{\rm v}(1+\theta_{\rm acc}V_{\rm gdy}^{\rm dr})}{\beta_{\rm acc}R_{\rm ON}} \tag{C.159}$$

$$I_{\rm CHlim} = \frac{\beta_{\rm acc}(V_{\rm gdy}^{\rm dr}+h_1)^2}{2(1+\theta_{\rm acc}V_{\rm gdy}^{\rm dr})} - 1E-49 \tag{C.160}$$

$$I_{\rm CHy} = -\min_{\rm hyp}(-I_{\rm CH}, I_{\rm CHlim}, 1E-50) \tag{C.161}$$

$$h_2 = 1 + 2\frac{I_{\rm CHy}(1+\theta_{\rm acc}V_{\rm gdy}^{\rm dr})}{\beta_{\rm acc}(V_{\rm gdy}^{\rm dr}+h_1)^2} \tag{C.162}$$

$$\psi_{\rm sLacc} = V_{\rm g}^{\rm dr} + h_1 - (V_{\rm gdc}^{\rm dr}+h_1)\sqrt{h_2} \tag{C.163}$$

Block 1A

$$\gamma_{\rm L} = \gamma_{\rm eff}\exp(-\frac{k_{\rm N_A}}{2}) \tag{C.164}$$

$$V_{\rm g} = V_{\rm GfB} - V_{\rm FB}^{\rm f} \tag{C.165}$$

$$V_{\rm gy} = {\rm pos}_{\rm sm}(V_{\rm g}, 2\phi_{\rm t}, 1E-12) \tag{C.166}$$

$$V_{\rm gL} = V_{\rm GfB} - V_{\rm FB}^{\rm f} - \phi_{\rm t}k_{\rm N_A} \tag{C.167}$$

$$V_{\rm gyL} = {\rm pos}_{\rm sm}(V_{\rm gL}, 2\phi_{\rm t}, 1E-12) \tag{C.168}$$

$$\phi = {\rm MIN}(2\phi_{\rm F}, 2\phi_{\rm Fdr}) - 0.1 \tag{C.169}$$

$$V_{\text{diby}} = \text{pos}_{\text{sm}}(V_{\text{DiB}} + \phi, \phi_{\text{t}}, 0) - \phi \tag{C.170}$$

Block 1B

$$\psi_{\text{sLaccy1}} = \text{pos}_{\text{sm}}(\psi_{\text{sLacc}} + (\phi - 2\phi_{\text{t}} k_{\text{N}_A}), \phi_{\text{t}}, 0) - (\phi - 2\phi_{\text{t}} k_{\text{N}_A}) \tag{C.171}$$

$$A_{\text{L}} = 2\phi_{\text{F}} + \psi_{\text{sLaccy1}} - 2\phi_{\text{t}} k_{\text{N}_A} \tag{C.172}$$

$$V_{\text{gconstL}} = \eta_{\text{s}} A_{\text{L}} - \phi_{\text{t}}(\eta_{\text{s}} - 1) + \gamma_{\text{L}} \sqrt{A_{\text{L}}} \tag{C.173}$$

$$V_{\text{gxL}} = \text{pos}_{\text{sm}}(V_{\text{gL}} - V_{\text{gconstL}}, 5\phi_{\text{t}}, 0) + V_{\text{gconstL}} \tag{C.174}$$

$$T_{\text{logL}} = \frac{1}{\phi_{\text{t}}}\left[\frac{1}{\gamma_{\text{L}}^2}(V_{\text{gxL}} - \eta_{\text{s}} A_{\text{L}})^2 - A_{\text{L}} + \phi_{\text{t}}\right] \tag{C.175}$$

$$\psi_{\text{siLinv}} = A_{\text{L}} + \phi_{\text{t}} \ln(T_{\text{logL}}) \tag{C.176}$$

Block 1C

$$A_0 = 2\phi_{\text{F}} + V_{\text{sby}} \tag{C.177}$$

$$V_{\text{gconst0}} = \eta_{\text{s}} A_0 - \phi_{\text{t}}(\eta_{\text{s}} - 1) + \gamma_{\text{eff}} \sqrt{A_0} \tag{C.178}$$

$$V_{\text{gx0}} = \text{pos}_{\text{sm}}(V_{\text{g}} - V_{\text{gconst0}}, 5\phi_{\text{t}}, 0) + V_{\text{gconst0}} \tag{C.179}$$

$$T_{\text{log0}} = \frac{1}{\phi_{\text{t}}}\left[\frac{1}{\gamma_{\text{eff}}^2}(V_{\text{gx0}} - \eta_{\text{s}} A_0)^2 - A_0 + \phi_{\text{t}}\right] \tag{C.180}$$

$$\psi_{\text{si0}} = A_0 + \phi_{\text{t}} \ln(T_{\text{log0}}) \tag{C.181}$$

Block 1D

$$\psi_{\text{sLaccy2}} = \text{pos}_{\text{sm}}(\psi_{\text{sLacc}} + \phi, \phi_{\text{t}}, 0) - \phi \tag{C.182}$$

$$A_{\text{L0}} = 2\phi_{\text{F}} + \psi_{\text{sLaccy2}} \tag{C.183}$$

$$V_{\text{gconstL0}} = \eta_{\text{s}} A_{\text{L0}} - \phi_{\text{t}}(\eta_{\text{s}} - 1) + \gamma_{\text{eff}} \sqrt{A_{\text{L0}}} \tag{C.184}$$

$$V_{\text{gxL0}} = \text{pos}_{\text{sm}}(V_{\text{g}} - V_{\text{gconstL0}}, 5\phi_{\text{t}}, 0) + V_{\text{gconstL0}} \tag{C.185}$$

$$T_{\text{logL0}} = \frac{1}{\phi_{\text{t}}}\left[\frac{1}{\gamma_{\text{eff}}^2}(V_{\text{gxL0}} - \eta_{\text{s}} A_{\text{L0}})^2 - A_{\text{L0}} + \phi_{\text{t}}\right] \tag{C.186}$$

$$\psi_{\text{siL0}} = A_{\text{L0}} + \phi_{\text{t}} \ln(T_{\text{logL0}}) \tag{C.187}$$

Block 3A

$$a_{\text{t}} = \text{min}_{\text{sm}}(V_{\text{gy}} - \psi_{\text{siLinv}}, (1 - \frac{k_{\text{N}_A}}{100})\gamma_{\text{eff}} \sqrt{\psi_{\text{siLinv}}}, \frac{k_{\text{N}_A}}{10}) \tag{C.188}$$

$$a = \text{max}_{\text{sm}}(a_{\text{t}}, (1 + \frac{k_{\text{N}_A}}{100})\gamma_{\text{L}} \sqrt{\psi_{\text{siLinv}}}, \frac{k_{\text{N}_A}}{100}) \tag{C.189}$$

$$L_{\text{minL}} = \frac{2\,L_{\text{eff}}}{k_{\text{N}_A}} \ln\left(\frac{\gamma_{\text{eff}}\sqrt{\psi_{\text{siLinv}}}}{a}\right) \tag{C.190}$$

$$a_{t0} = \min_{\text{sm}}\left(V_{\text{gy}} - \psi_{\text{si0}}, \left(1 - \frac{k_{\text{N}_A}}{1000}\right)\gamma_{\text{eff}} \exp\left(\frac{k_{\text{N}_A}}{20}\right)\sqrt{\psi_{\text{si0}}}, \frac{k_{\text{N}_A}}{10}\right) \tag{C.191}$$

$$a_0 = \max_{\text{sm}}\left(a_{t0}, \left(1 + \frac{k_{\text{N}_A}}{1000}\right)\gamma_{\text{eff}}\sqrt{\psi_{\text{si0}}}, \frac{k_{\text{N}_A}}{100}\right) \tag{C.192}$$

$$L_{\text{min0}} = \frac{20\,L_{\text{eff}}}{k_{\text{N}_A}} \ln\left(\frac{\gamma_{\text{eff}} \exp\left(\frac{k_{\text{N}_A}}{20}\right)\sqrt{\psi_{\text{si0}}}}{a_0}\right) \tag{C.193}$$

$$L_{\text{min}} = \begin{cases} \min_{\text{sm}}\left(\frac{L_{\text{min0}}}{L_{\text{eff}}}, \frac{L_{\text{minL}}}{L_{\text{eff}}}, \frac{k_{\text{N}_A}}{1000}\right) & \text{if } k_{\text{N}_A} > 0 \\ 0 & \text{otherwise} \end{cases} \tag{C.194}$$

Block 3B

$$\gamma_{\text{Lmin}} = \gamma_{\text{eff}} \exp\left(-\frac{k_{\text{N}_A} f_{\text{Lmin}}}{2}\right) \tag{C.195}$$

$$C_{\text{oxinvp}} = C_{\text{oxinv}}(1 - f_{\text{Lmin}}) \tag{C.196}$$

$$C_{\text{oxtot}} = C_{\text{oxinvp}} + C_{\text{oxacc}} \tag{C.197}$$

$$f_{\text{cap1}} = if\left(C_{\text{oxtot}} > 0, \frac{C_{\text{oxinvp}}}{C_{\text{oxtot}}}, if\left(C_{\text{oxinv}} > 0, 1, if\left(C_{\text{oxacc}} > 0, 0, 1\right)\right)\right) \tag{C.198}$$

$$f_{\text{cap2}} = if\left(C_{\text{oxtot}} > 0, \frac{C_{\text{oxacc}}}{C_{\text{oxtot}}}, if\left(C_{\text{oxinv}} > 0, 0, 1\right)\right) \tag{C.199}$$

Block 4

$$\psi_{\text{ss0}} = \left[-\frac{\gamma_{\text{eff}}}{2\eta_{\text{s}}} + \sqrt{\frac{\gamma_{\text{eff}}^2}{4\eta_{\text{s}}^2} + \frac{V_{\text{gy}}}{\eta_{\text{s}}}}\right]^2 \tag{C.200}$$

$$\psi_{\text{ssL}} = \left[-\frac{\gamma_{\text{L}}}{2\eta_{\text{s}}} + \sqrt{\frac{\gamma_{\text{L}}^2}{4\eta_{\text{s}}^2} + \frac{V_{\text{gyL}}}{\eta_{\text{s}}}}\right]^2 \tag{C.201}$$

$$\psi_{\text{s0}} = \min_{\text{sm2}}(\psi_{\text{ss0}}\psi_{\text{si0}},, 2\phi_{\text{t}}) \tag{C.202}$$

$$\psi_{\text{sL0}} = \min_{\text{sm2}}(\psi_{\text{ss0}}, \psi_{\text{siL0}}, 2\phi_{\text{t}}) \tag{C.203}$$

$$\psi_{\text{sL}} = \min_{\text{sm2}}(\psi_{\text{ssL}}, \psi_{\text{siLinv}}, 2\phi_{\text{t}}) \tag{C.204}$$

Block 5

$$V_{\text{q0}} = \left(V_{\text{gy}} - \eta_{\text{s}}\psi_{\text{s0}} - \gamma_{\text{eff}}\sqrt{\psi_{\text{s0}}}\right) \tag{C.205}$$

$$V_{\text{qL}} = \left(V_{\text{gyL}} - \eta_{\text{s}}\psi_{\text{sL}} - \gamma_{\text{L}}\sqrt{\psi_{\text{sL}}}\right) \tag{C.206}$$

$$V_{\text{q0L}} = \left(V_{\text{gy}} - \eta_{\text{s}}\psi_{\text{sL0}} - \gamma_{\text{eff}}\sqrt{\psi_{\text{sL0}}}\right) \tag{C.207}$$

Block 6

$$V_{\mathrm{qLlim}} = V_{\mathrm{qL}} - V_{\mathrm{q0L}} \tag{C.208}$$

Block 7

$$\sigma = 1E-10 \tag{C.209}$$

$$F = \frac{V_{\mathrm{qL}}}{V_{\mathrm{q0}}} \tag{C.210}$$

$$Q_{\mathrm{CHinv}} = \begin{cases} -\frac{2}{3}C_{\mathrm{oxinvp}}V_{\mathrm{q0}}\frac{F^2+F+1}{F+1} & \text{if } V_{\mathrm{q0}} > \sigma \\ -\frac{2}{3}C_{\mathrm{oxinvp}}V_{\mathrm{qL}} & \text{if } V_{\mathrm{q0}} < \sigma \text{ and } V_{\mathrm{qL}} > \sigma \\ 0 & \text{if } V_{\mathrm{q0}} < \sigma \text{ and } V_{\mathrm{qL}} < \sigma \end{cases} \tag{C.211}$$

$$Q_{\mathrm{CHinvn}} = -C_{\mathrm{oxinvp}}\mathrm{pos}_{\mathrm{sm}}(-\frac{Q_{\mathrm{CHinv}}}{C_{\mathrm{oxinvp}}}, 1E-8, 0) \tag{C.212}$$

$$Q_{\mathrm{Dinv}} = \begin{cases} -\frac{2}{15}C_{\mathrm{oxinvp}}f_{\mathrm{cap1}}V_{\mathrm{q0}}\frac{3F^3+6F^2+4F+2}{(F+1)^2} & \text{if } V_{\mathrm{q0}} > \sigma \\ -\frac{2}{5}C_{\mathrm{oxinvp}}f_{\mathrm{cap1}}V_{\mathrm{qL}} & \text{if } V_{\mathrm{q0}} < \sigma \text{ and } V_{\mathrm{qL}} > \sigma \\ 0 & \text{if } V_{\mathrm{q0}} < \sigma \text{ and } V_{\mathrm{qL}} < \sigma \end{cases} \tag{C.213}$$

$$Q_{\mathrm{Sinvlim}} = \begin{cases} C_{\mathrm{oxinvp}}(-\frac{4}{15}f_{\mathrm{cap1}}V_{\mathrm{qLlim}} - \frac{2}{3}f_{\mathrm{cap2}}V_{\mathrm{qLlim}}) & \text{if } V_{\mathrm{q0}} > \sigma \text{ or } V_{\mathrm{qL}} > \sigma \\ 0 & \text{otherwise} \end{cases} \tag{C.214}$$

$$Q_{\mathrm{Dinvn}} = -C_{\mathrm{oxinvp}}\mathrm{pos}_{\mathrm{sm}}(-\frac{(Q_{\mathrm{Dinv}} + Q_{\mathrm{Sinvlim}})}{C_{\mathrm{oxinvp}}}, 1E-8, 0) \tag{C.215}$$

C.9.2 The Body Charge (Block 8)

$$a = \sqrt{1 + \frac{4V_{\mathrm{gy}}}{\gamma_{\mathrm{eff}}^2}} \tag{C.216}$$

$$b = \sqrt{1 + \frac{4V_{\mathrm{gy}}}{\gamma_{L\mathrm{min}}^2}} \tag{C.217}$$

$$f_{\mathrm{ab}} = \ln\frac{a-1}{a+1} - \ln\frac{b-1}{b+1} - \frac{1}{a-1} - \frac{1}{a+1} + \frac{1}{b-1} + \frac{1}{b+1} \tag{C.218}$$

$$\gamma_{\mathrm{L1}} = \gamma_{\mathrm{eff}}\exp(-\frac{k_{\mathrm{N}_A}(1+f_{L\mathrm{min}})}{4}) \tag{C.219}$$

$$\gamma_{\mathrm{e1}} = \begin{cases} \frac{4(\gamma_{L\mathrm{min}}-\gamma_{\mathrm{L1}})}{k_{\mathrm{N}_A}(1-f_{L\mathrm{min}})} & \text{if } (k_{\mathrm{N}_A} > 0 \text{ and } f_{L\mathrm{min}} < 1-\sigma) \\ \gamma_{\mathrm{L}} & \text{if } (k_{\mathrm{N}_A} > 0 \text{ and } f_{L\mathrm{min}} > 1-\sigma) \\ \gamma_{\mathrm{eff}} & \text{otherwise} \end{cases} \tag{C.220}$$

$$\gamma_{\mathrm{e2}} = \begin{cases} \frac{4(\gamma_{\mathrm{L1}}-\gamma_{\mathrm{L}})}{k_{\mathrm{N}_A}(1-f_{L\mathrm{min}})} & \text{if } (k_{\mathrm{N}_A} > 0 \text{ and } f_{L\mathrm{min}} < 1-\sigma) \\ \gamma_{\mathrm{L}} & \text{if } (k_{\mathrm{N}_A} > 0 \text{ and } f_{L\mathrm{min}} > 1-\sigma) \\ \gamma_{\mathrm{eff}} & \text{otherwise} \end{cases} \tag{C.221}$$

$$S_{e1} = V_{gy} + \frac{\gamma_{e1}^2}{4\eta_s} \tag{C.222}$$

$$S_{e2} = V_{gy} + \frac{\gamma_{e2}^2}{4\eta_s} \tag{C.223}$$

$$V_{qL1} = if(V_{qL} \text{ or } V_{q0} > 10^{-10}, \sqrt{V_{q0}^2 + 0.5(V_{qL}^2 - V_{q0}^2)}, 0) \tag{C.224}$$

$$f_L = S_{e2} - V_{qL} \tag{C.225}$$

$$f_{L1p} = S_{e2} - V_{qL1} \tag{C.226}$$

$$f_{L1} = S_{e1} - V_{qL1} \tag{C.227}$$

$$f_0 = S_{e1} - V_{q0} \tag{C.228}$$

$$f_{e1} = \frac{f_{L1}^{2.5} - f_0^{2.5}}{5} - \frac{f_{L1}^{1.5} - f_0^{1.5}}{3} * S_{e1} \tag{C.229}$$

$$f_{e2} = \frac{f_L^{2.5} - f_{L1p}^{2.5}}{5} - \frac{f_L^{1.5} - f_{L1p}^{1.5}}{3} * S_{e2} \tag{C.230}$$

$$V_{qb1} = \begin{cases} -\frac{4(\gamma_{e1} f_{e1} + \gamma_{e2} f_{e2})}{V_{qL}^2 - V_{q0}^2} & \text{if } \|V_{qL}^2 - V_{q0}^2\| > 10^{-6} \\ & \text{and } (V_{qL} > 10^{-6} \text{ or } V_{q0} > 10^{-6}) \\ -\frac{\gamma_{e1}\sqrt{f_0} + \gamma_{e2}\sqrt{f_L}}{2} & \text{otherwise} \end{cases} \tag{C.231}$$

$$V_{qb2} = if(k_{N_A} > 0, \frac{\gamma_{eff}^2 - \gamma_L^2}{2k_{N_A}} + \frac{V_{gy}}{k_{N_A}} f_{ab}, \frac{\gamma_{eff}^2}{2}) \tag{C.232}$$

$$Q_{Bdep} = C_{oxinv}((1 - f_{Lmin}) * V_{qb1} + V_{qb2}) \tag{C.233}$$

NOTE: pay attention to the derivatives in the else case of V_{qb1}!

C.9.3 The Body Accumulation Charge (Block 9)

$$V_{gacc} = -\text{pos}_{sm}(-V_g, 2\phi_t, 0) \tag{C.234}$$

$$Q_{Bacc} = -C_{oxinv} V_{gacc} \tag{C.235}$$

C.9.4 The Drain Gate Depletion Charge (Block 10)

$$c = 10^{-12} \tag{C.236}$$

$$V_{dgy}^{dr} = \text{pos}_{sm}(V_{DiB} - V_g^{dr}, 20\phi_t, c) \tag{C.237}$$

$$\psi_{ss}^{dr} = \left[-\frac{\gamma^{fdr}}{2\eta_s} + \sqrt{\frac{\gamma^{fdr\,2}}{4\eta_s^2} + \frac{V_{dgy}^{dr}}{\eta_s}} \right]^2 \tag{C.238}$$

$$A_{dr} = 2\phi_{Fdr} + V_{diby} \tag{C.239}$$

$$V_{gconst}^{dr} = \eta_s A_{dr} - \phi_t(\eta_s - 1) + \gamma^{fdr}\sqrt{A_{dr}} \tag{C.240}$$

$$V_{gxdr} = \text{pos}_{sm}(V_{DiB} - V_g^{dr} - V_{gconst}^{dr}, 5\phi_t, 0) + V_{gconst}^{dr} \tag{C.241}$$

$$T_{\log}^{\mathrm{dr}} = \frac{1}{\phi_t}\left[\frac{1}{\gamma^{fdr\,2}}(V_{\mathrm{gxdr}} - \eta_s A_{\mathrm{dr}})^2 - A_{\mathrm{dr}} + \phi_t\right] \tag{C.242}$$

$$\psi_{\mathrm{si}}^{\mathrm{dr}} = \begin{cases} A_{\mathrm{dr}} + \phi_t \ln\left(T_{\log}^{\mathrm{dr}}\right) & \text{if } T_{\log}^{\mathrm{dr}} > 1 \\ A_{\mathrm{dr}} & \text{otherwise} \end{cases}$$

$$\psi_s^{\mathrm{dr}} = \mathrm{min}_{\mathrm{sm2}}\left(\psi_{\mathrm{ss}}^{\mathrm{dr}}, \psi_{\mathrm{si}}^{\mathrm{dr}}, \phi_t\right) \tag{C.243}$$

$$V_{\mathrm{qdepdi}} = \gamma^{\mathrm{fdr}}\sqrt{\psi_s^{\mathrm{dr}}} \tag{C.244}$$

$$V_{\mathrm{Lgy}}^{\mathrm{dr}} = \mathrm{pos}_{\mathrm{sm}}(\psi_{\mathrm{sLacc}} - V_g^{\mathrm{dr}}, 20\phi_t, c) \tag{C.245}$$

$$\psi_{\mathrm{ssL}}^{\mathrm{dr}} = \left[-\frac{\gamma^{\mathrm{fdr}}}{2\eta_s} + \sqrt{\frac{\gamma^{fdr\,2}}{4\eta_s^2} + \frac{V_{\mathrm{Lgy}}^{\mathrm{dr}}}{\eta_s}}\right]^2 \tag{C.246}$$

$$\psi_{\mathrm{sL}}^{\mathrm{dr}} = \mathrm{min}_{\mathrm{sm2}}\left(\psi_{\mathrm{ssL}}^{\mathrm{dr}}, \psi_{\mathrm{si}}^{\mathrm{dr}}, \phi_t\right) \tag{C.247}$$

$$V_{\mathrm{qdepL}} = \gamma^{\mathrm{fdr}}\sqrt{\psi_{\mathrm{sL}}^{\mathrm{dr}}} \tag{C.248}$$

$$F_{\mathrm{dr}} = \frac{V_{\mathrm{qdepdi}}}{V_{\mathrm{qdepL}}} \tag{C.249}$$

$$Q_{\mathrm{Ddep}} = \begin{cases} C_{\mathrm{oxacc}} V_{\mathrm{qdepL}}\left(\frac{F_{\mathrm{dr}}-1}{\ln(F_{\mathrm{dr}})}\right) & \text{if } (V_{\mathrm{qdepdi}} \;\&\; V_{\mathrm{qdepL}} > c) \\ & \text{and } (F_{\mathrm{dr}} < 1-c \text{ or } F_{\mathrm{dr}} > 1+c) \\ 0.5\; C_{\mathrm{oxacc}}(V_{\mathrm{qdepL}} + V_{\mathrm{qdepdi}}) & \text{if } (V_{\mathrm{qdepdi}} \;\&\; V_{\mathrm{qdepL}} > c) \\ & \text{and } 1-c < F_{\mathrm{dr}} < 1+c \\ 0 & \text{otherwise} \end{cases} \tag{C.250}$$

C.9.5 The Drift Accumulation charge (Block 11)

$$V_{\mathrm{qLacc}} = \mathrm{pos}_{\mathrm{sm}}\left(V_g^{\mathrm{dr}} - \psi_{\mathrm{sLacc}}, 20\phi_t, c\right) \tag{C.251}$$

$$V_{\mathrm{qdi}} = \mathrm{pos}_{\mathrm{sm}}\left(V_g^{\mathrm{dr}} - V_{\mathrm{DiB}}, 20\phi_t, c\right) \tag{C.252}$$

$$V_{\mathrm{qLacclim}} = \mathrm{pos}_{\mathrm{sm}}\left(V_g^{\mathrm{dr}} - \psi_{\mathrm{sLacc}} - \left(V_{\mathrm{gy}} - \eta_s\psi_{\mathrm{sL0}} - \gamma_{\mathrm{eff}}\sqrt{\psi_{\mathrm{s0}}}\right), 20\;\phi_t, c\right) \tag{C.253}$$

$$V_{\mathrm{qdilim}} = \mathrm{pos}_{\mathrm{sm}}\left(V_g^{\mathrm{dr}} - V_{\mathrm{DiB}} - \left(V_{\mathrm{gy}} - \eta_s\psi_{\mathrm{sL0}} - \gamma_{\mathrm{eff}}\sqrt{\psi_{\mathrm{s0}}}\right), 20\;\phi_t, c\right) \tag{C.254}$$

$$F_1 = \frac{V_{\mathrm{qdi}}}{V_{\mathrm{qLacc}}} \tag{C.255}$$

$$F_2 = \frac{V_{\mathrm{qdilim}}}{V_{\mathrm{qLacclim}}} \tag{C.256}$$

$$Q_{\mathrm{CHacc}} = \begin{cases} -\frac{2}{3}C_{\mathrm{oxacc}} V_{\mathrm{qLacc}}\left(\frac{F_1^2+F_1+1}{F_1+1}\right) & \text{if } V_{\mathrm{qLacc}} > c \\ -\frac{2}{3}C_{\mathrm{oxacc}} V_{\mathrm{qdi}} & \text{if } V_{\mathrm{qLacc}} < c \text{ and } V_{\mathrm{qdi}} > c \\ 0 & \text{otherwise} \end{cases} \tag{C.257}$$

$$Q_{\mathrm{Dacc}} = \begin{cases} -\frac{2}{15}C_{\mathrm{oxacc}}f_{\mathrm{cap2}}V_{\mathrm{qLacc}}\left(\frac{3F_1^3+6F_1^2+4F_1+2}{(F_1+1)^2}\right) & \\ -\frac{2}{3}C_{\mathrm{oxinvp}}f_{\mathrm{cap2}}V_{\mathrm{qLacc}}\left(\frac{F_1^2+F_1+1}{F_1+1}\right) & \text{if } V_{\mathrm{qLacc}} > c \\ -(\frac{2}{5}C_{\mathrm{oxacc}}+\frac{2}{3}C_{\mathrm{oxinvp}})f_{\mathrm{cap2}}V_{\mathrm{qdi}} & \text{if } V_{\mathrm{qLacc}} < c \text{ and } V_{\mathrm{qdi}} > c \\ 0 & \text{otherwise} \end{cases} \tag{C.258}$$

$$Q_{\mathrm{Sacclim}} = \begin{cases} -\frac{2}{15}C_{\mathrm{oxacc}}f_{\mathrm{cap2}}V_{\mathrm{qLacclim}}\left(\frac{2F_2^3+4F_2^2+6F_2+3}{(F_2+1)^2}\right) & \text{if } V_{\mathrm{qLacclim}} > 1E-8 \\ -\frac{4}{15}C_{\mathrm{oxacc}}f_{\mathrm{cap2}}V_{\mathrm{qdilim}} & \text{otherwise} \end{cases} \tag{C.259}$$

$$Q_{\mathrm{Daccn}} = Q_{\mathrm{Dacc}} + Q_{\mathrm{Sacclim}} \tag{C.260}$$

C.9.6 The Drift Inversion charge

$$Q_{\mathrm{Binv}} = \begin{cases} C_{\mathrm{oxacc}}\left(V_{\mathrm{dgy}}^{\mathrm{dr}} - \eta_{\mathrm{s}}\psi_{\mathrm{s}}^{\mathrm{dr}} - \gamma^{\mathrm{fdr}}\sqrt{\psi_{\mathrm{s}}^{\mathrm{dr}}}\right) & \text{if } V_{\mathrm{qdepdi}} > c \\ 0 & \text{otherwise} \end{cases} \tag{C.261}$$

C.9.7 The Nodal Charges

The nodal charges are given by:

$$Q_{\mathrm{B}} = Q_{\mathrm{Bdep}} + Q_{\mathrm{Bacc}} + Q_{\mathrm{Binv}} \tag{C.262}$$

$$Q_{\mathrm{Di}} = Q_{\mathrm{Dinvn}} + Q_{\mathrm{Daccn}} + Q_{\mathrm{Ddep}} \tag{C.263}$$

$$Q_{\mathrm{Gf}} = -(Q_{\mathrm{CHinvn}} + Q_{\mathrm{CHacc}} + Q_{\mathrm{Bdep}} + Q_{\mathrm{Bacc}} + Q_{\mathrm{Ddep}} + Q_{\mathrm{Binv}}) \tag{C.264}$$

$$Q_{D} = 0 \tag{C.265}$$

$$Q_{\mathrm{S}} = -(Q_{\mathrm{Gf}} + Q_{\mathrm{D}} + Q_{\mathrm{Di}} + Q_{\mathrm{B}}) \tag{C.266}$$

C.10 The Extrinsic Model (copied from the STAG model)

C.10.1 Series Resistance

The series resistance of the source and drain regions are included as separate resistor elements with fixed values R_S and R_D. This approach gives rise to two additional internal nodes in the SOI LDMOS model. If R_S and R_D are not given but R_{sh} is given, the series resistance values are calculated from the source and drain areas as:

$$R_S = R_{sh} \cdot \texttt{NRS}$$

$$R_D = R_{sh} \cdot \texttt{NRD}$$

C.10.2 Impact Ionisation Model

The impact ionisation current is modelled as:

$$I_M = (M-1)I_{CH}$$

with

$$M - 1 = \frac{\alpha_0}{\beta_M}(V_{DS} - \eta \cdot V_{dsat}) \exp\left\{\frac{-l_m \beta_M}{(V_{DS} - \eta \cdot V_{dsat})}\right\} \tag{C.267}$$

$$l_m = l_{m0} + l_{m1} \cdot (V_{DS} - V_{geff}) + l_{m2} \cdot (V_{DS} - V_{geff})^2 \tag{C.268}$$

$$V_{geff} = V_g - V_{SB} - \eta_s 2\phi_F - \gamma_0\sqrt{2\phi_F} \tag{C.269}$$

C.10.3 Diodes and Parasitic Bipolar Transistor

A modified Ebers-Moll model is used to represent the parasitic bipolar transistor. The forward current through each body-drain or body-source junction is modelled as:

$$\begin{aligned} I_{DS/D} &= I_{D1S/D} + I_{D2S/D} \\ I_{D1S/D} &= I_{sS/D}\left[\exp\left(\frac{V_{BS/D}}{\eta_{DS/D}\phi_T}\right) - 1\right] \\ I_{D2S/D} &= I_{s1S/D}\left[\exp\left(\frac{V_{BS/D}}{\eta_{D1S/D}\phi_T}\right) - 1\right] \end{aligned}$$

The parasitic bipolar current injected at the opposite junction is calculated as:

$$I_{\mathrm{BJT}} = \frac{\beta_{\mathrm{BJT}}}{1+\beta_{\mathrm{BJT}}} I_{\mathrm{D1S/D}}$$

The junction capacitance models and parameters are identical to the standard SPICE MOSFET models:

$$C_{\mathrm{dep}} = \begin{cases} \frac{C_{\mathrm{J0S/D}}}{(1-\frac{V_{\mathrm{DB}}}{PB_{\mathrm{S/D}}})^{M}_{\mathrm{S/D}}} & \text{if } V_{\mathrm{DB}} < FC_{\mathrm{S/D}} \cdot PB_{\mathrm{S/D}} \\ \frac{C_{\mathrm{J0S/D}}}{(1-FC_{\mathrm{S/D}})^{(M_{\mathrm{S/D}}+1)}} \left(1 - FC_{\mathrm{S/D}}(1+M_{\mathrm{S/D}}) + \frac{V_{\mathrm{DB}}}{PB_{S/D}} M_{\mathrm{S/D}}\right) & \text{if } V_{\mathrm{DB}} >= FC_{\mathrm{S/D}} \cdot PB_{\mathrm{S/D}} \end{cases} \tag{C.270}$$

The charge storage due to the mobile carriers in the diodes are modelled via C_{DE} and C_{DC}, the diffusion capacitances associated with the $P-N$ junctions. The charges associated with these capacitances are given as

$$Q_{\mathrm{DE}} = \tau_{\mathrm{F}} \alpha_{\mathrm{BJT}} I_{\mathrm{D1S}} \tag{C.271}$$

$$Q_{\mathrm{DC}} = \tau_R \alpha_{\mathrm{BJT}} I_{\mathrm{D1D}} \tag{C.272}$$

(C.273)

The parameters τ_{F} and τ_{R} denote the forward and reverse transit times respectively of the Ebers-Moll model.

C.10.4 Self-Heating Model

The heat generated by the device in the self-heating model is given as:

$$P_{\mathrm{t}} = I_{\mathrm{CH}} V_{\mathrm{DiS}} + I^2_{\mathrm{CH}} R_{\mathrm{S}} + I_{\mathrm{DR}} V_{\mathrm{DDi}} + I^2_{\mathrm{DR}} R_{\mathrm{D}}$$

C.10.5 Noise Models

The channel charge is used for the thermal noise model and so is valid in all regions of operation. The thermal noise associated with the source and drain series resistances is also included. The $1/f$ noise model used is determined by the switch `NLEV`:

`NLEV` $= 0$(default)

$$\frac{\overline{i^2_{\mathrm{f}}}}{\Delta f} = \frac{\mathtt{KF} \cdot I_{\mathrm{D}}^{\mathtt{AF}}}{L^2_{\mathrm{eff}} C_{\mathrm{of}}} \cdot \frac{1}{f}$$

`NLEV` $= 1$

$$\frac{\overline{i^2_{\mathrm{f}}}}{\Delta f} = \frac{\mathtt{KF} \cdot I_{\mathrm{D}}^{\mathtt{AF}}}{W L_{\mathrm{eff}} C_{\mathrm{of}}} \cdot \frac{1}{f}$$

`NLEV` $= 2$

$$\frac{\overline{i^2_{\mathrm{f}}}}{\Delta f} = \frac{\mathtt{KF} \cdot g^2_{mf}}{W L_{\mathrm{eff}} C_{\mathrm{of}}} \cdot \frac{1}{f^{\,\mathtt{AF}}}$$

Appendix D

Proof for V_{Psat} used in I_{DR}

In this appendix we will prove that

$$\begin{aligned} V_{\mathrm{satdep}} > \psi_{\mathrm{i}} \quad \text{or} \quad V_{\mathrm{satinv}} > \psi_{\mathrm{i}} \quad &\Leftrightarrow \quad V_{\mathrm{satdep}} > V_{\mathrm{satinv}} \\ &\Leftrightarrow \quad \max(V_{\mathrm{satdep}}, V_{\mathrm{satinv}}) = V_{\mathrm{satdep}} \qquad \text{(D.1)} \\ V_{\mathrm{satdep}} < \psi_{\mathrm{i}} \quad \text{or} \quad V_{\mathrm{satinv}} < \psi_{\mathrm{i}} \quad &\Leftrightarrow \quad V_{\mathrm{satdep}} < V_{\mathrm{satinv}} \\ &\Leftrightarrow \quad \max(V_{\mathrm{satdep}}, V_{\mathrm{satinv}}) = V_{\mathrm{satinv}} \qquad \text{(D.2)} \end{aligned}$$

Let us first consider the case of $V_{\mathrm{satdep}} > \psi_{\mathrm{i}}$. We write

$$\begin{aligned} V_{\mathrm{satdep}} > \psi_{\mathrm{i}} \quad &\Leftrightarrow \quad V_{\mathrm{gb}} + V_{\mathrm{Pdep}} > \frac{\gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{gb}}}{1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}} \qquad \text{(D.3)} \\ &\overset{\gamma^{\mathrm{bdr}}>3,\phi_{\mathrm{Fdr}}<0.5}{\Longleftrightarrow} \quad (V_{\mathrm{gb}} + V_{\mathrm{Pdep}}) \cdot (1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}) < \gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{gb}} \qquad \text{(D.4)} \\ &\Leftrightarrow \quad V_{\mathrm{gb}} > V_{\mathrm{satinv}} - V_{\mathrm{Pdep}} \qquad \text{(D.5)} \\ &\Leftrightarrow \quad V_{\mathrm{satdep}} > V_{\mathrm{satinv}} \,. \qquad \text{(D.6)} \end{aligned}$$

Let us now look at the second case where $V_{\mathrm{satinv}} > \psi_{\mathrm{i}}$. We write

$$\begin{aligned} V_{\mathrm{satinv}} > \psi_{\mathrm{i}} \quad &\Leftrightarrow \quad \frac{-\gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{Pdep}}}{\gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}} > \frac{\gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{gb}}}{1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}} \qquad \text{(D.7)} \\ &\overset{\gamma^{\mathrm{bdr}}>3,\phi_{\mathrm{Fdr}}<0.5}{\Longleftrightarrow} \quad (V_{\mathrm{gb}} + V_{\mathrm{Pdep}}) > \frac{-\gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{Pdep}}}{\gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}} \qquad \text{(D.8)} \\ &\Leftrightarrow \quad V_{\mathrm{satdep}} > V_{\mathrm{satinv}} \,. \qquad \text{(D.9)} \end{aligned}$$

Similarly we write

$$\begin{aligned} V_{\mathrm{satdep}} < \psi_{\mathrm{i}} \quad &\Leftrightarrow \quad V_{\mathrm{gb}} + V_{\mathrm{Pdep}} < \frac{\gamma^{\mathrm{bdr}}\sqrt{2\,\phi_{\mathrm{Fdr}}} + V_{\mathrm{gb}}}{1 - \gamma^{\mathrm{bdr}}\,\delta_{\mathrm{dr}}} \qquad \text{(D.10)} \\ &\overset{\gamma^{\mathrm{bdr}}>3,\,\phi_{\mathrm{Fdr}}<0.5}{\Longleftrightarrow} \quad V_{\mathrm{satdep}} < V_{\mathrm{satinv}} \qquad \text{(D.11)} \end{aligned}$$

and

$$V_{\text{satinv}} < \psi_{\text{i}} \quad \Leftrightarrow \quad \frac{-\gamma^{\text{bdr}}\sqrt{2\,\phi_{\text{Fdr}}} + V_{\text{Pdep}}}{\gamma^{\text{bdr}}\,\delta_{\text{dr}}} < \frac{\gamma^{\text{bdr}}\sqrt{2\,\phi_{\text{Fdr}}} + V_{\text{gb}}}{1-\gamma^{\text{bdr}}\,\delta_{\text{dr}}} \tag{D.12}$$

$$\overset{\gamma^{\text{bdr}}>3,\ \phi_{\text{Fdr}}<0.5}{\Longleftrightarrow} \quad V_{\text{satdep}} < V_{\text{satinv}}\ . \tag{D.13}$$

Note that the conditions used in the derived statements are ensured by parameter clipping: γ^{bdr} is clipped above 3, and ϕ_{Fdr} is clipped below 0.5.

Appendix E

Derivation of q_{Llim}, q_{Lacclim} and q_{dilim}

The charge densities to be used in the calculation of the compensated source charge have to fulfill the following requirements:

$$q_{\mathrm{Llim}} = q_{\mathrm{L}}(V_{\mathrm{GfBlim}}) = \begin{cases} q_{\mathrm{L}} & \text{for } V_{\mathrm{GfB}} < V_{\mathrm{th}} \\ 0 & \text{for } V_{\mathrm{GfB}} \gg V_{\mathrm{th}} \end{cases} \tag{E.1}$$

$$q_{\mathrm{Lacclim}} = q_{\mathrm{Lacc}}(V_{\mathrm{GfBlim}}) = \begin{cases} q_{\mathrm{Lacc}} & \text{for } V_{\mathrm{GfB}} < V_{\mathrm{th}} \\ 0 & \text{for } V_{\mathrm{GfB}} \gg V_{\mathrm{th}} \end{cases} \tag{E.2}$$

$$q_{\mathrm{dilim}} = q_{\mathrm{di}}(V_{\mathrm{GfBlim}}) = \begin{cases} q_{\mathrm{di}} & \text{for } V_{\mathrm{GfB}} < V_{\mathrm{th}} \\ 0 & \text{for } V_{\mathrm{GfB}} \gg V_{\mathrm{th}}. \end{cases} \tag{E.3}$$

Or in words, this means that below the threshold voltage the charge attributed to the source by the Ward and Dutton partitioning scheme, is compensated, and is attributed to the drain instead. For gate voltages which are a lot higher than the threshold voltage Ward and Dutton is valid with good approximation, and the compensation charge Q_{Swdlim} has to go to zero. This is implemented in a continuous way as follows:

$$q_{\mathrm{Llim}} = \underline{-C_{\mathrm{of}}\ (V_{\mathrm{gy}} - \eta_s \psi_{\mathrm{sL0}} - \gamma_{\mathrm{eff}} \sqrt{\psi_{\mathrm{sL0}}})} + q_L \tag{E.4}$$

$$\begin{cases} = 0 & \text{if } V_{\mathrm{GfD}} < V_{\mathrm{th}} \\ \cong -q_{\mathrm{L}} & \text{if } V_{\mathrm{GfD}} \gg V_{\mathrm{th}} \end{cases} \tag{E.5}$$

where ψ_{sL0} is calculated in exactly the same way as ψ_{s0}, but the internal drain potential (ψ_{sLacc}) is used in the expression of ψ_{si0} instead of the source voltage (see Sec. C.9.1 in App. C). The first term can be recognised as the expression for the inversion charge density at the drain end with $N_{\mathrm{Ad}} = N_{\mathrm{As}}$. This term will is defined as $q_{0\mathrm{L}}$. Note that $q_{0\mathrm{L}}$ goes to 0 for $V_{\mathrm{GfD}} < V_{\mathrm{th}}$, and to $-q_{\mathrm{L}}$ if $V_{\mathrm{GfD}} \gg V_{\mathrm{th}}$. The same approach is followed for q_{Lacclim} and q_{dilim}:

$$q_{\mathrm{Lacclim}} = -\mathrm{pos}_{\mathrm{sm}}(C_{\mathrm{of}}\ (V_{\mathrm{gy}} - \eta_s \psi_{\mathrm{sL0}} - \gamma_{\mathrm{eff}} \sqrt{\psi_{\mathrm{s0}}}) - q_{\mathrm{Lacc}}, 20\ \phi_{\mathrm{t}}, 0) \tag{E.6}$$

$$q_{\mathrm{dilim}} = -\mathrm{pos}_{\mathrm{sm}}(-C_{\mathrm{of}}\ (V_{\mathrm{gy}} - \eta_s \psi_{\mathrm{sL0}} - \gamma_{\mathrm{eff}} \sqrt{\psi_{\mathrm{s0}}}) - q_{\mathrm{di}}, 20\ \phi_{\mathrm{t}}, 0) \tag{E.7}$$

Exactly the same smoothing functions as for q_{Lacc} and q_{di} are used here to limit these quantities to positive values (see Sec. C.9.5 in App. C).

Appendix F

SEMATECH Tests

F.1 Parameter Sets of the Evaluated Devices

The tests are performed on four different devices, two with field oxide and two without field oxide ($L_{\mathrm{dr}} = 0$). This set of devices is illustrated in Table F.1. Parameter set 1 consists of the values extracted in Chapter 4 for the MV LDMOS. Parameter set 2 is not extracted, but describes a typical medium voltage process with thinner gate oxides and higher drift region doping concentrations compared with Parameter set 1. These two parameter sets are given in Table F.2.

Device	L_{dr}	Parameter Set
LDMOS 1	0	1
LDMOS 2	4 μm	1
LDMOS 3	0	2
LDMOS 4	1 μm	2

Table F.1: *Overview of devices evaluated by the SEMATECH tests.*

Parameter	Parameter Set 1	Parameter Set 2
L	1.45 μm	1.0 μm
l_{d}	0.3 μm	0.3 μm
L_{drov}	1.2 μm	0.5 μm
t_{of}	60 nm	20 nm
t_{ob}	3 μm	1 μm
t_{b}	1.5 μm	1 μm
t_{bdr}	0.9 μm	0.8 μm

Table F.2: *Parameter Set 1 and 2; to be continued on the next page.*

Parameter	Parameter Set 1	Parameter Set 2
V_{th0}	2.75 V	1 V
N_A	0.75 10^{17}/ cm^3	0.5 10^{17}/ cm^3
$k_{\mathrm{N_A}}$	1.4	0.5
μ_{s}	700 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$	700 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$
θ	0.045 V^{-1}	0.045 V^{-1}
μ_{acc}	750 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$	750 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$
θ_{acc}	0.04 V^{-1}	0.04 V^{-1}
v_{sat}	2.2 10^7 cm/s	1 10^7 cm/s
σ	0	0
N_{D}	1.3 10^{16} /cm^3	1.3 10^{16} /cm^3
μ_{dr}	1250 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$	1250 $\mathrm{cm}^2/(\mathrm{V{\cdot}s})$
v_{satdr}	1.4 10^7 cm/s	1.5 10^7 cm/s
f_{v}	0.3	0.3
λ_{r}	5 10^{-9} m/V	5 10^{-9} m/V
m	2	2
χ_{FB}	-3 10^{-3}	-3 10^{-3}
k	1.7	1.7
k_{acc}	2	2
k_{dr}	2.2	2.2
J_{s1Snom}	9.596 10^{-9} A/m	9.596 10^{-9} A/m
η_{D1S}	1.65	1.65
J_{sSnom}	6.818 10^{-11} A/m	6.818 10^{-11} A/m
η_{DS}	1.23	1.23
C_{JS}	0.2 10^{-10} F/m	0.2 10^{-10} F/m
J_{sDnom}	6.818 10^{-11} A/m	6.818 10^{-11} A/m
η_{DD}	1.23	1.23
J_{s1Dnom}	9.596 10^{-9} A/m	9.596 10^{-9} A/m
η_{D1D}	1.65	1.65
C_{JD}	0.3 10^{-10} F/m	0.3 10^{-10} F/m
α_0	5 10^5/cm	5.5 10^5/cm
β_0	5.5 10^6 V/cm	1.5 10^6 V/cm
χ_β	9000 V/cmK	9000 V/cmK
η	1	1
l_{m}	1.2 10^{-7} m	1.2 10^{-7} m
l_{m1}	1 10^{-15} m/V	1 10^{-15} m/V
l_{m2}	1 10^{-15} $\mathrm{m/V}^2$	1 10^{-15} $\mathrm{m/V}^2$
R_{D}	57 Ω	57 Ω
R_{S}	0 Ω	0 Ω
C_{gfsor}	0 F/m	0 F/m
C_{gfdor}	0 F/m	0 F/m
C_{gfbor}	0 F/m	0 F/m
C_{gbsor}	0 F/m	0 F/m
C_{gbdor}	0 F/m	0 F/m
C_{gbbor}	0 F/m	0 F/m

F.2 SEMATECH Tests

This section presents the results obtained with the adapted SEMATECH tests for the compact SOI LDMOS model. These test are summarised in Table F.3. The evaluation results for devices 1 to 4, as defined in Sec. F.1, are plotted below.

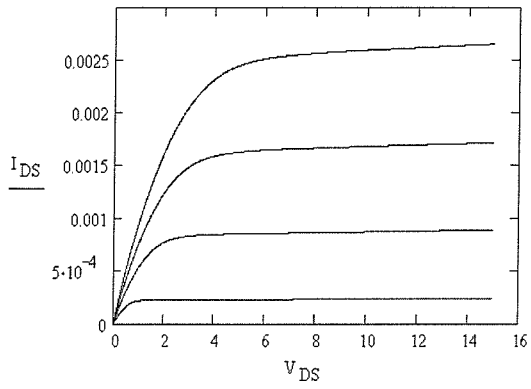
No.	Description
1	Statement of desired model capabilities together with actual model capabilities.
2a	Output characteristics. Fine resolution plot of I_D vs. V_{DS}. Step of 0.01 V for devices 1 and 3, 0.04 V for devices 2 and 4.
2b	Output characteristics. Fine resolution plot of g_o vs. V_{DS} (log-lin scale). Step of 0.01 V for devices 1 and 3, 0.04 V for devices 2 and 4.
3a	Threshold characteristics. Fine resolution plot of I_D vs. V_{GfS}. Step of 0.04 V; $V_{DS} = 0.1$ V, 3 V.
3b	Threshold characteristics. Fine resolution plot of g_m vs. V_{GfS}. Step of 0.04 V; $V_{DS} = 0.1$ V, 3 V.
4a	Subthreshold characteristics. Fine resolution plot of I_D vs. V_{GfS} (log-lin scale). Step of 0.04 V; $V_{DS} = 0.1$ V, 3 V.
4b	Subthreshold characteristics. Fine resolution plot of g_m/I_D vs. V_{GfS} (lin-log scale). Step of 0.04 V; $V_{DS} = 0.1$ V, 3 V.
5a	Diode connected LDMOS. Plot of I_{Dsat} vs. ambient temperature. Device 1 and 2: $V_{GfS} = 3, 5, 7, 9, 11$ V. Device 3 and 4: $V_{GfS} = 2, 3.5, 5, 6.5, 8$ V.
5b	Diode connected LDMOS. Plot of V_{Dsat} vs. ambient temperature. Device 1 and 2: $I_G = 1000, 200, 40, 8, 1.6$ μA. Device 3 and 4: $I_G = 2000, 400, 80, 16, 3.2$ μA.
6a	Diode connected LDMOS. Plot of I_{Dsat} vs. L_{dr}. Device 1 : $V_{GfS} = 3, 5, 7, 9, 11$ V. Device 3 : $V_{GfS} = 2, 3.5, 5, 6.5, 8$ V.
6b	Diode connected LDMOS. Plot of V_{Dsat} vs. L_{dr}. Device 1 : $I_G = 1000, 200, 40, 8, 1.6$ μA. Device 3 : $I_G = 2000, 400, 80, 16, 3.2$ μA.
6c	Diode connected LDMOS. Plot of I_{Dsat} vs. L. Device 1 and 2: $V_{GfS} = 3, 5, 7, 9, 11$ V. Device 3 and 4: $V_{GfS} = 2, 3.5, 5, 6.5, 8$ V.
6d	Diode connected LDMOS. Plot of V_{Dsat} vs. L. Device 1 and 2: $I_G = 1000, 200, 40, 8, 1.6$ μA. Device 3 and 4: $I_G = 2000, 400, 80, 16, 3.2$ μA.
7a	Diode connected LDMOS. Plot of $g_m/\sqrt{I_D}$ vs. $\sqrt{W}$. Device 1 and 2: $V_{GfS} = 3, 5, 7, 9, 11$ V. Device 3 and 4: $V_{GfS} = 2, 3.5, 5, 6.5, 8$ V.
7b	Diode connected LDMOS. Plot of V_{DS} vs. $\sqrt{W}$. Device 1 and 2: $I_G = 1000, 200, 40, 8, 1.6$ μA. Device 3 and 4: $I_G = 2000, 400, 80, 16, 3.2$ μA.
8a	Weak/moderate inversion test (Tsividius #1). Very fine resolution plot (step = 0.01 V) of I_D vs. V_{GfS} for $V_{DS} = V_{DD}$. Device 1: $V_{DS} = 14$ V, 2: $V_{DS} = 40$ V, 3: $V_{DS} = 10$ V, 4: $V_{DS} = 20$ V;.
8b	Weak/moderate inversion test (Tsividius #1). Very fine resolution plot (step = 0.01 V) of I_D vs. V_{GfS} (log-lin scale). Device 1: $V_{DS} = 14$ V, 2: $V_{DS} = 40$ V, 3: $V_{DS} = 10$ V, 4: $V_{DS} = 20$ V;.

Table F.3: *Adapted SEMATECH Tests for SOI LDMOS; continued on next page.*

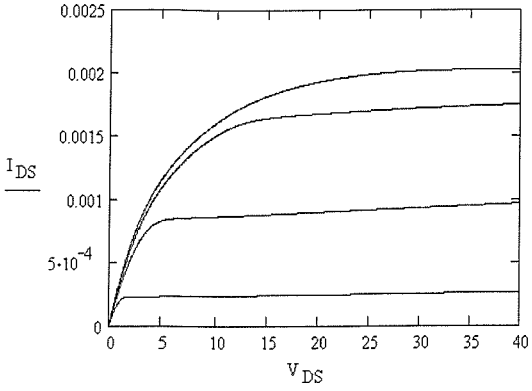
No.	Description
9a	Very fine resolution plot (step = 0.01 V) of g_m/I_D vs. V_{GfS} (Tsividius #2). Device 1: V_{DS} = 14 V, 2: V_{DS} = 40 V, 3: V_{DS} = 10 V, 4: V_{DS} = 20 V;.
9b	Very fine resolution plot (step = 0.01 V) of g_m/I_D vs. V_{GfS} (log-lin scale). Device 1: V_{DS} = 14 V, 2: V_{DS} = 40 V, 3: V_{DS} = 10 V, 4: V_{DS} = 20 V;.
10	Very fine resolution plot of $\ln(g_o)$ vs. $ln(I_{DS})$ diode configuration: I_{DS} is stepped from 10 pA to 0.4 mA.
11	Test for self-heating capability. Influence of self-heating on the output characteristics. Device 1, 2 : V_{GfS} = 3, 5, 7, 9, 11 V. Device 3, 4 : V_{GfS} = 2, 3.5, 5, 6.5, 8 V.
12a	Test for self-heating capability. Influence of self-heating on g_o vs. V_{DS} for different frequencies.
12b	Test for self-heating capability. Influence of self-heating on g_o vs. frequency for different V_{DS}.
13	Body resistance test: variation of the output characteristics with body resistance. V_{GfS} = 5 V, R_{body} = 1, 100, 10k, 1M, 100MΩ.
14	Inverter transfer characteristic.
15	Inverter charge/discharge test. Input/output voltages for rising and falling pulse.
16	Single transistor charge/discharge test. Gate/Drain voltages for a repetitive pulse on the gate through a very high gate, with a very high load resistance at the drain.
18a	Continuity test for the drain current around $V_{DS} = 0$. V_{GfS} = 4, 6, 8, 10 V.
18b	Continuity test for the output conductance around $V_{DS} = 0$. V_{GfS} = 4, 6, 8, 10 V.
19	Gummel slope ratio test. $SR = \frac{(I_1+I_2)(V_1-V_2)}{(I_1-I_2)(V_1+V_2)}$ with V_1 and V_2 two small values for V_{DS} (V_1 = 0.011 V and V_2 = 0.01 V).
20	Gummel tree-top test. g_m/I_{DS} vs. V_{GfS} for V_{SB} = 0, 2, 4, 6 V.
21a	Capacitance vs. drain bias (V_{GfS} = 8 V). Derivatives of gate charge
21b	Capacitance vs. drain bias (V_{GfS} = 8 V). Derivatives of drain charge
21c	Capacitance vs. drain bias (V_{GfS} = 8 V). Derivatives of source charge
21d	Capacitance vs. drain bias (V_{GfS} = 8 V). Derivatives of body charge
22a.a	Capacitance vs. front gate bias (V_{DS} = 0 V). Derivatives of gate charge
22a.b	Capacitance vs. front gate bias (V_{DS} = 0 V). Derivatives of drain charge
22a.c	Capacitance vs. front gate bias (V_{DS} = 0 V). Derivatives of source charge
22a.d	Capacitance vs. front gate bias (V_{DS} = 0 V). Derivatives of body charge
22b.a	Capacitance vs. front gate bias (V_{DS} = 1 V). Derivatives of gate charge
22b.b	Capacitance vs. front gate bias (V_{DS} = 1 V). Derivatives of drain charge
22b.c	Capacitance vs. front gate bias (V_{DS} = 1 V). Derivatives of source charge
22b.d	Capacitance vs. front gate bias (V_{DS} = 1 V). Derivatives of body charge

Device 1	Device 2

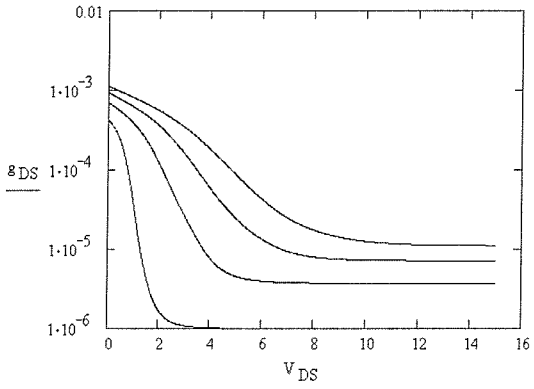
Sematech Test 2a



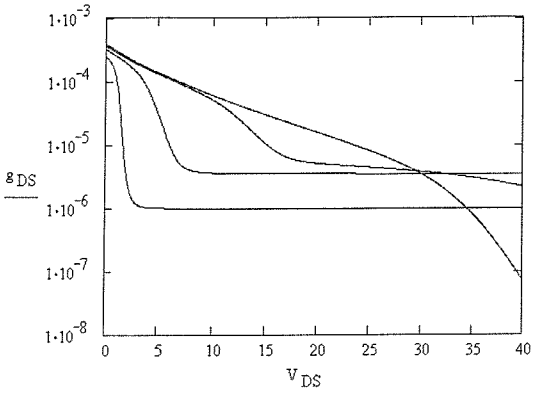
Sematech Test 2a



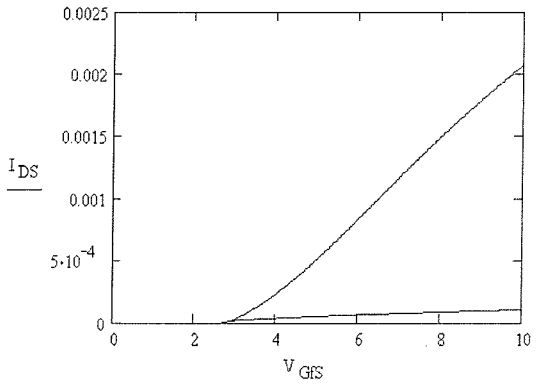
Sematech Test 2b



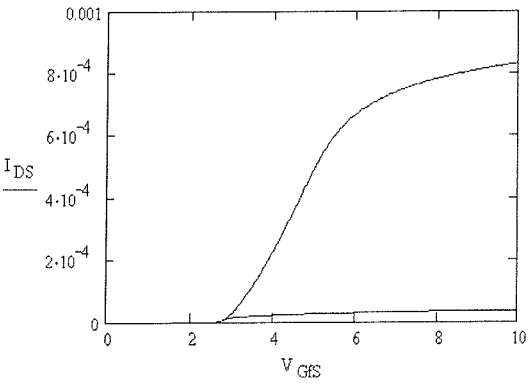
Sematech Test 2b



Sematech Test 3a

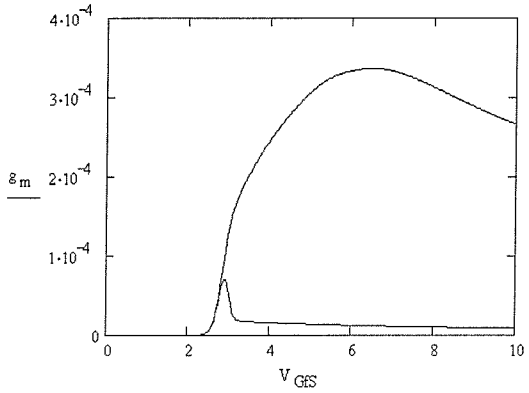


Sematech Test 3a

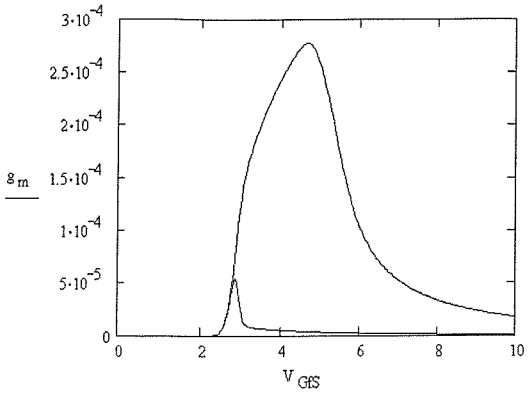


Device 1	Device 2

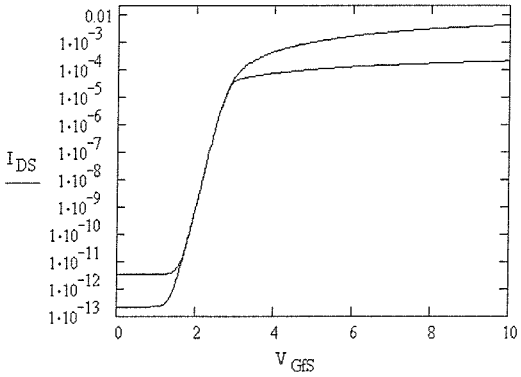
Sematech Test 3b



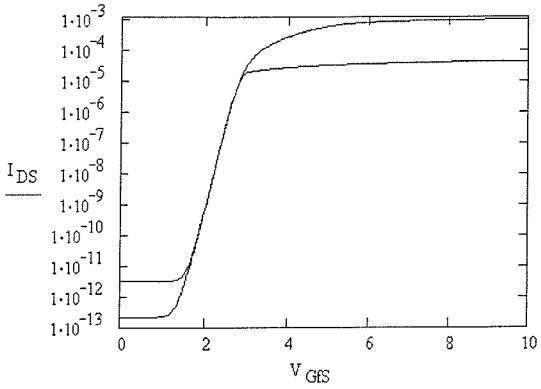
Sematech Test 3b



Sematech Test 4a



Sematech Test 4a



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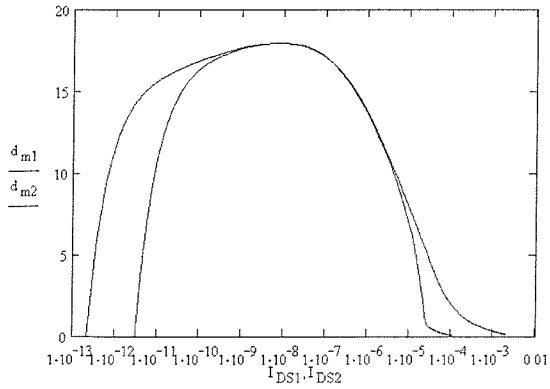
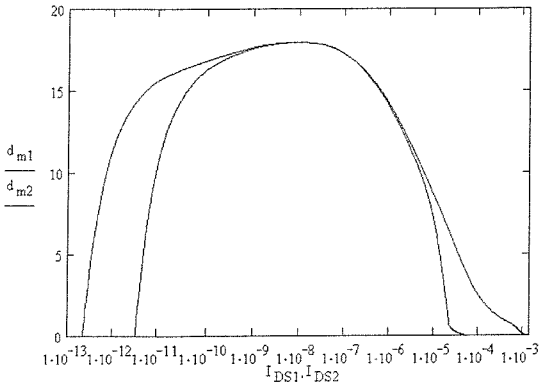
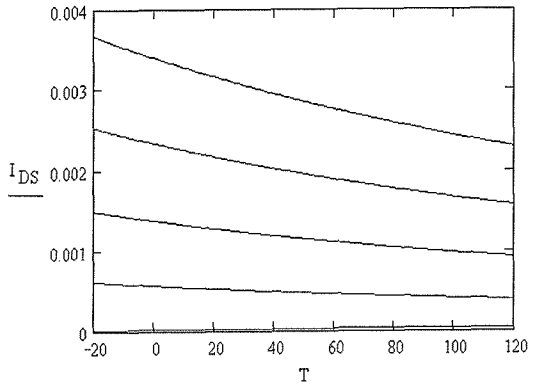


Sematech Test 4b

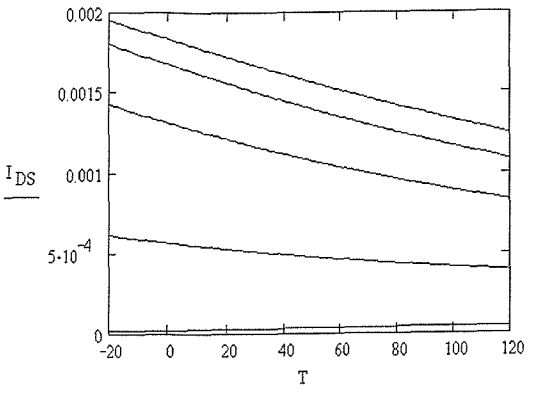


Device 1	Device 2

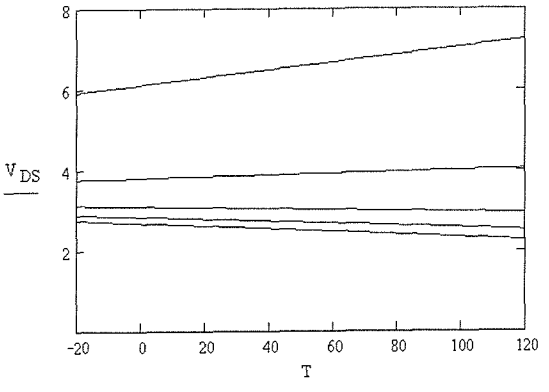
Sematech Test 5a



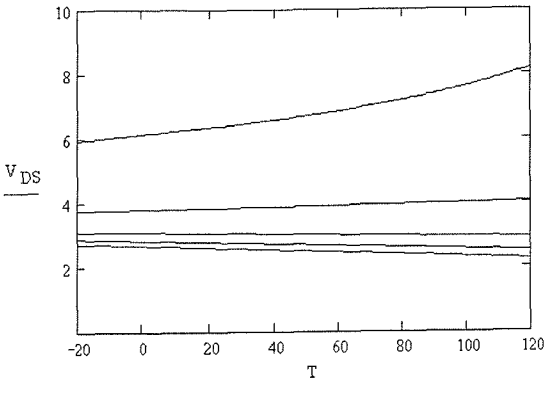
Sematech Test 5a



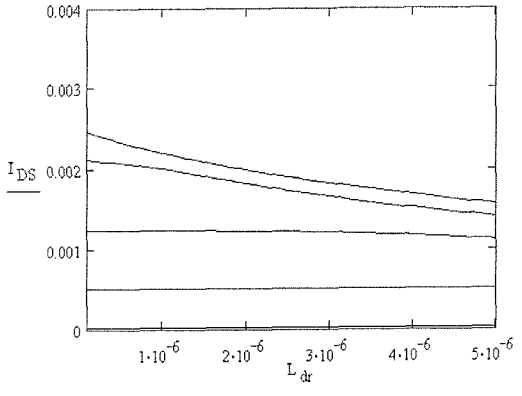
Sematech Test 5b



Sematech Test 5b

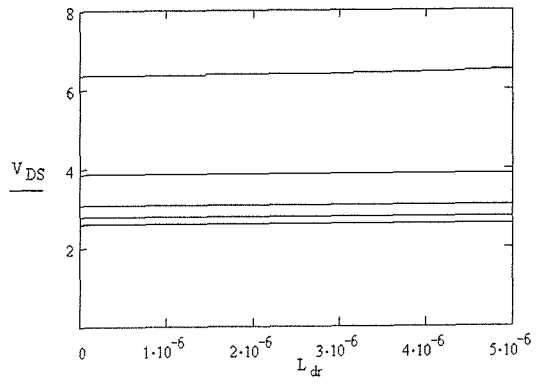


Sematech Test 6a

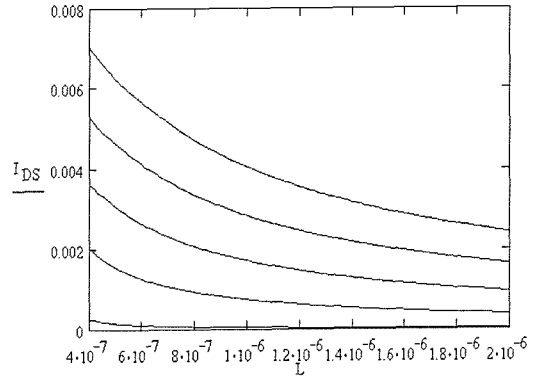


Device 1	Device 2

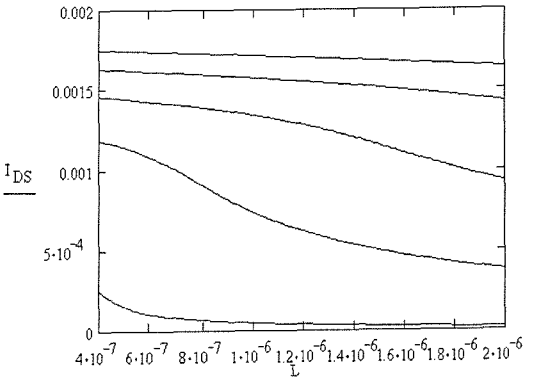
Sematech Test 6b



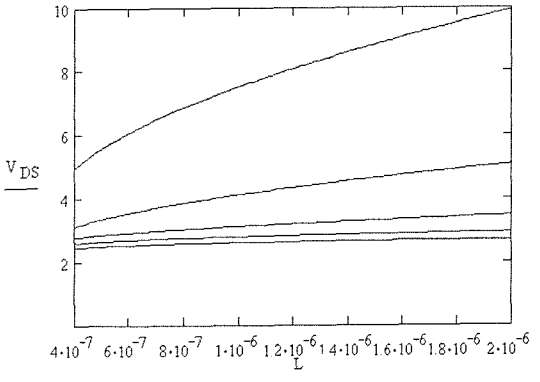
Sematech Test 6c



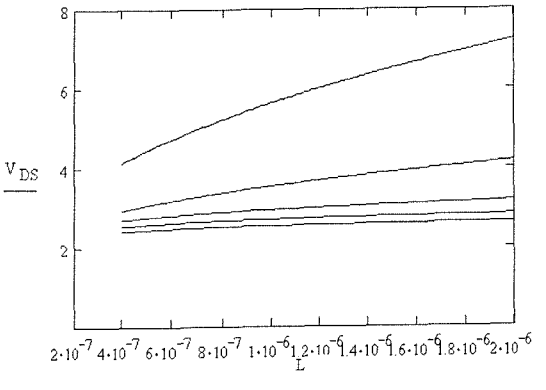
Sematech Test 6c



Sematech Test 6d

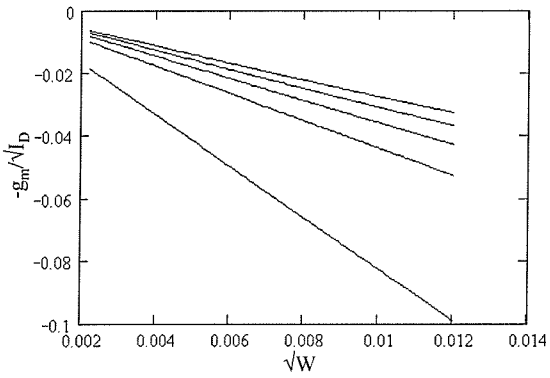


Sematech Test 6d

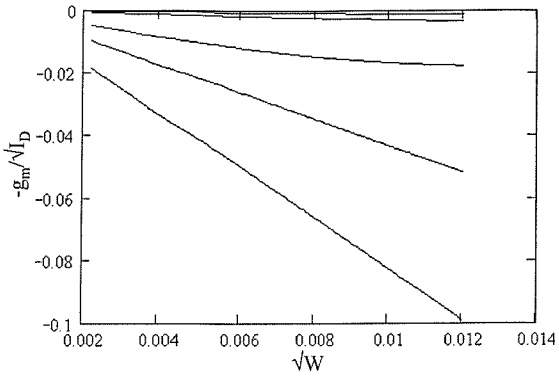


Device 1	Device 2

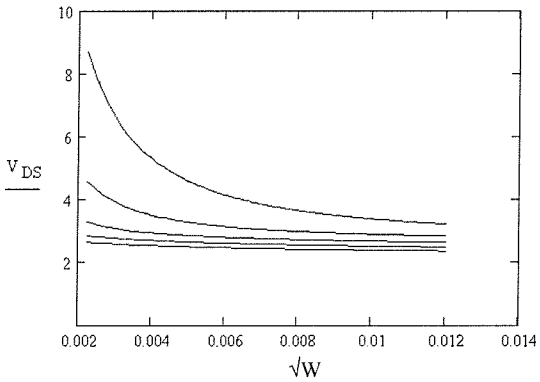
Sematech Test 7a



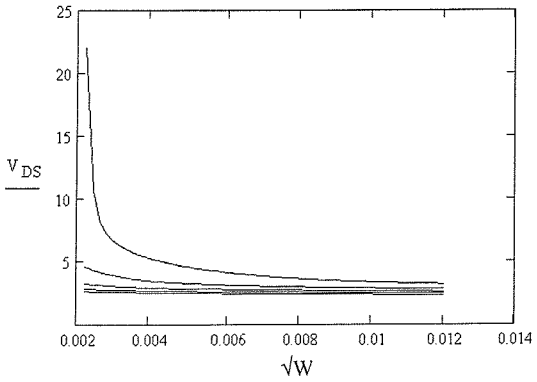
Sematech Test 7a



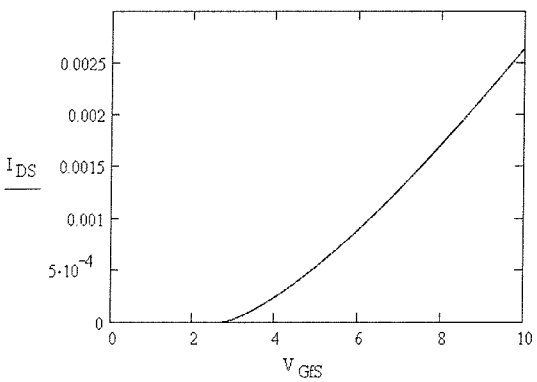
Sematech Test 7b



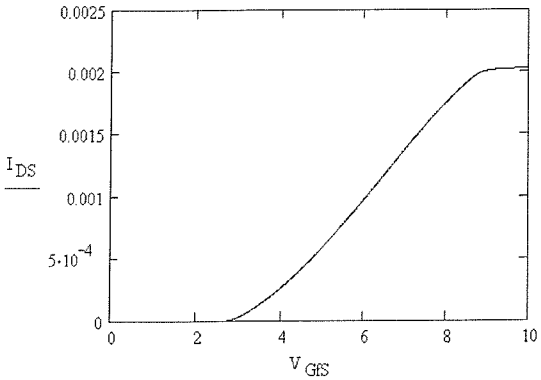
Sematech Test 7b



Sematech Test 8a

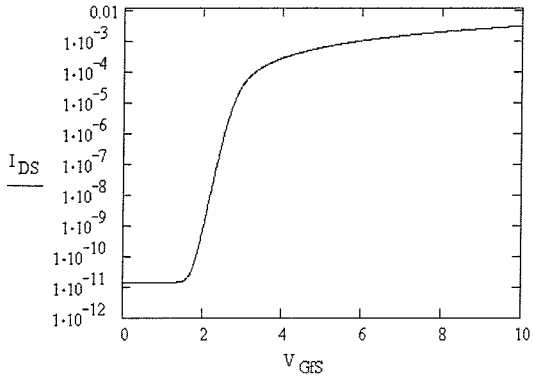


Sematech Test 8a

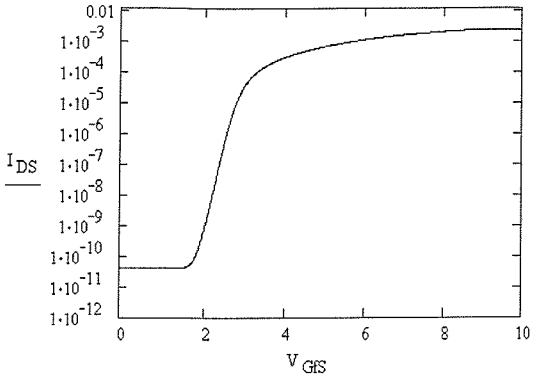


Device 1	Device 2

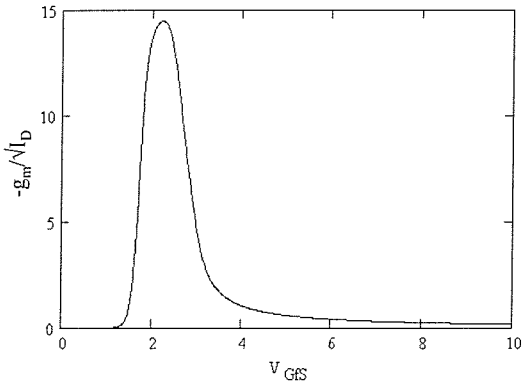
Sematech Test 8b



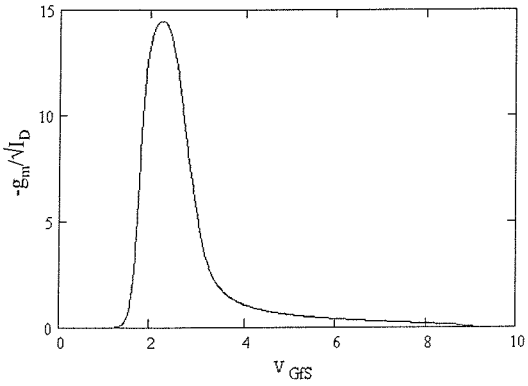
Sematech Test 8b



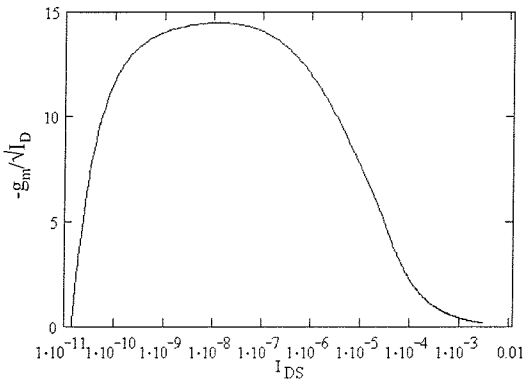
Sematech Test 9a



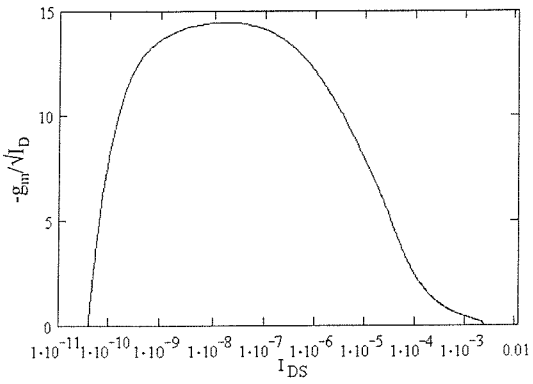
Sematech Test 9a



Sematech Test 9b

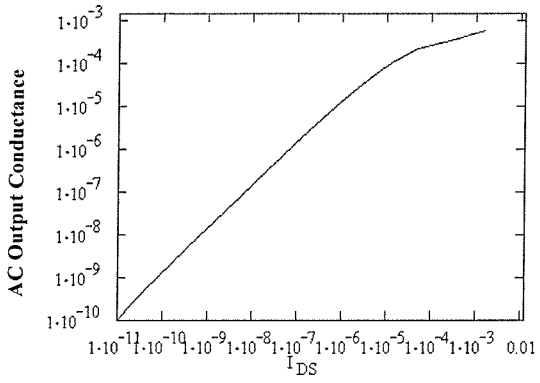


Sematech Test 9b

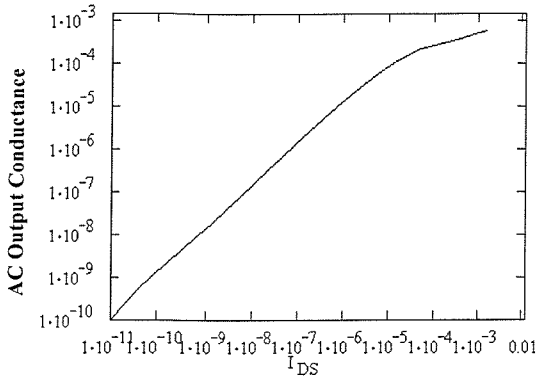


Device 1	Device 2

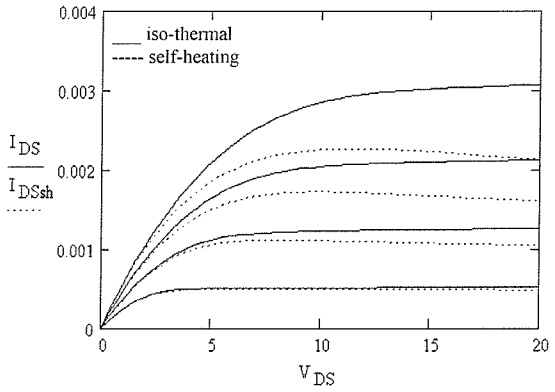
Sematech Test 10



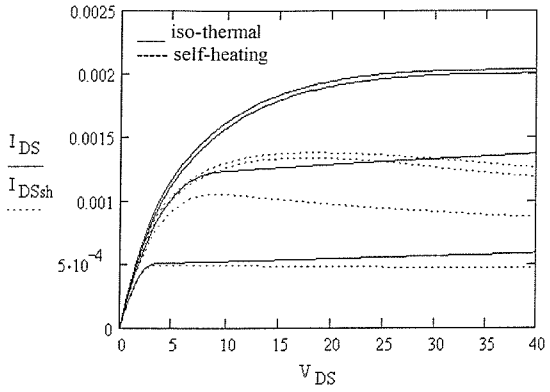
Sematech Test 10



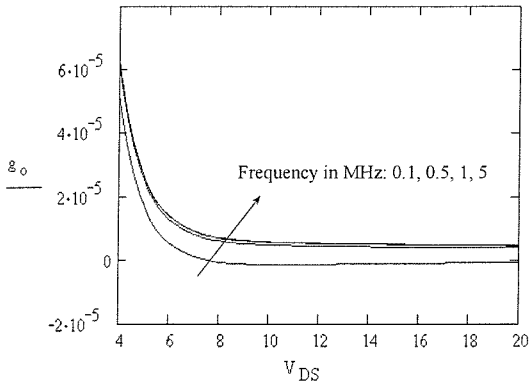
Sematech Test 11



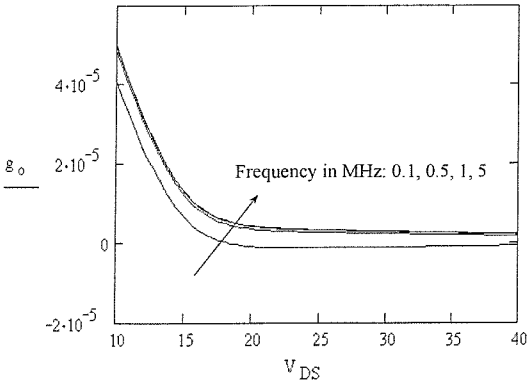
Sematech Test 11



Sematech Test 12a

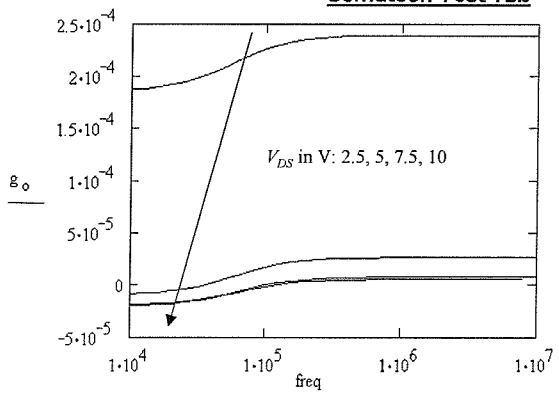


Sematech Test 12a

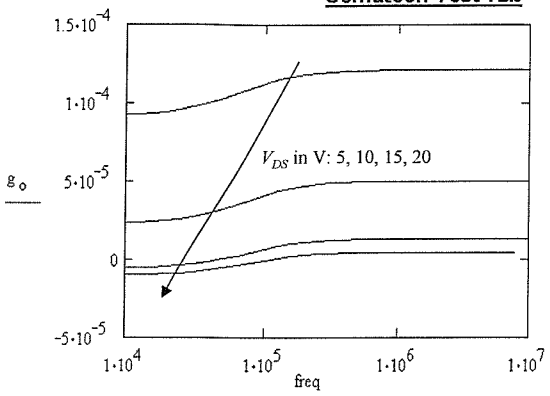


Device 1	Device 2

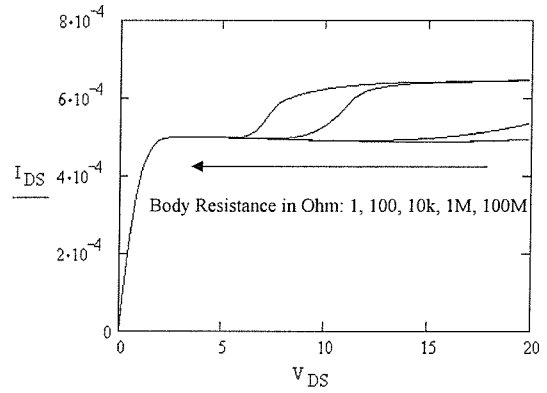
Sematech Test 12b



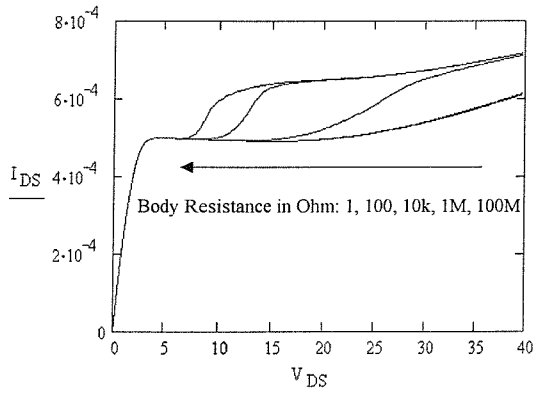
Sematech Test 12b



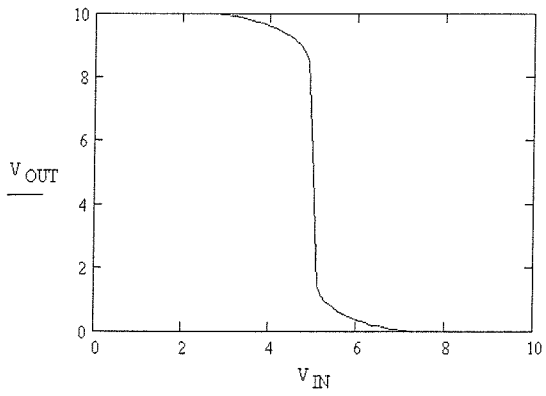
Sematech Test 13



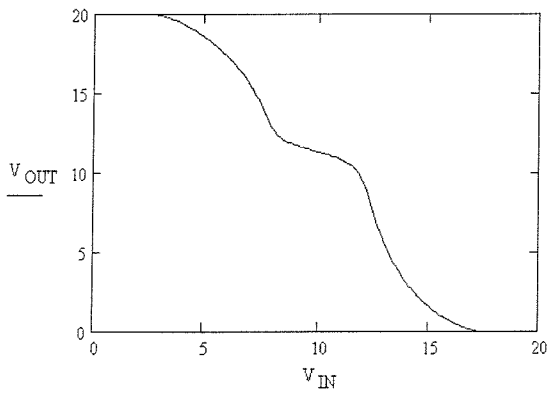
Sematech Test 13



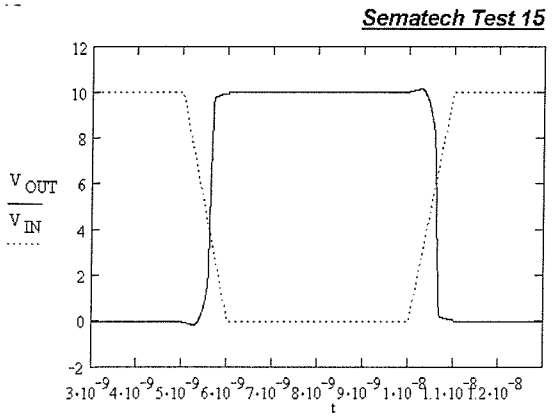
Sematech Test 14

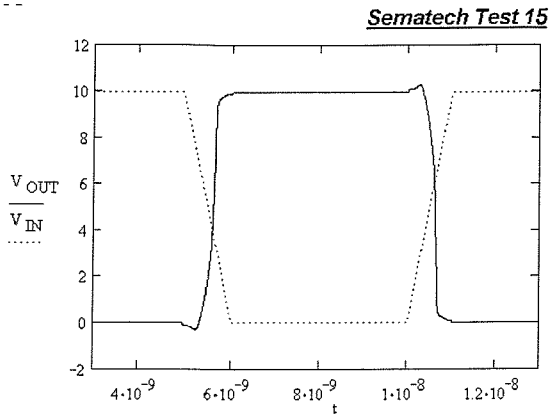


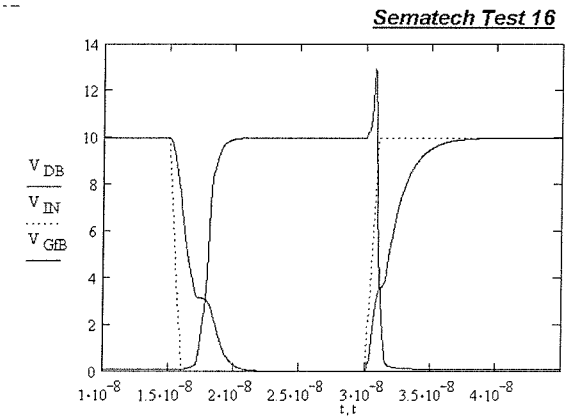
Sematech Test 14

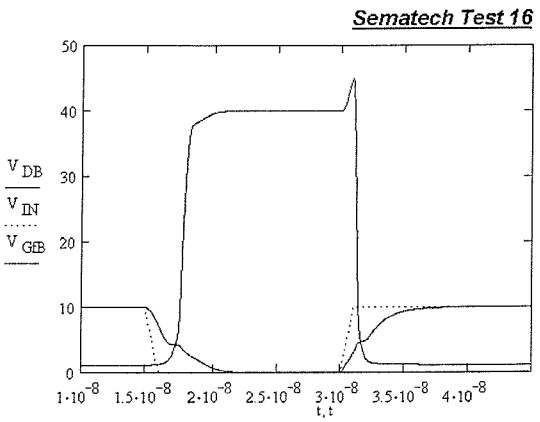


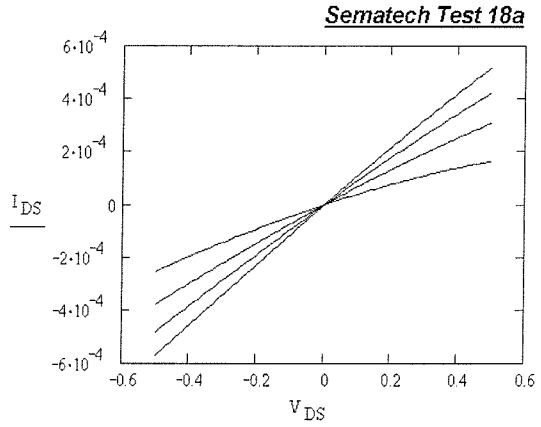
Device 1	Device 2

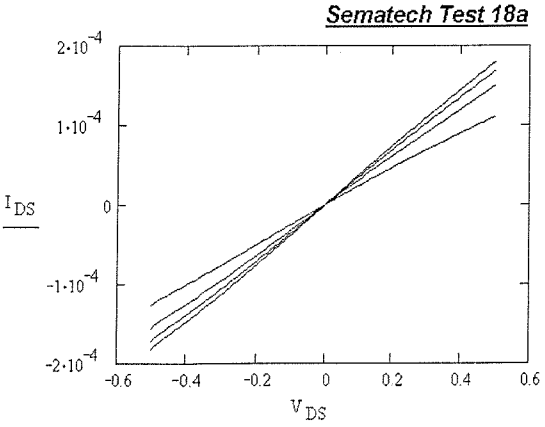






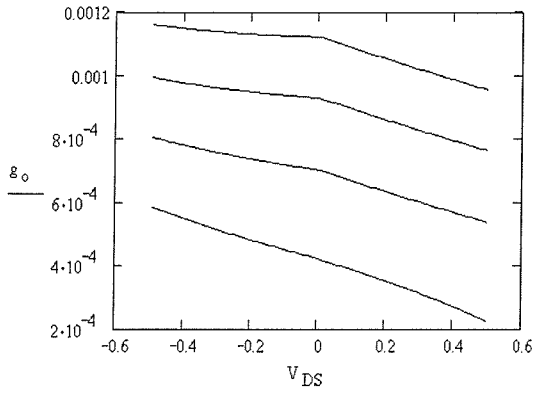




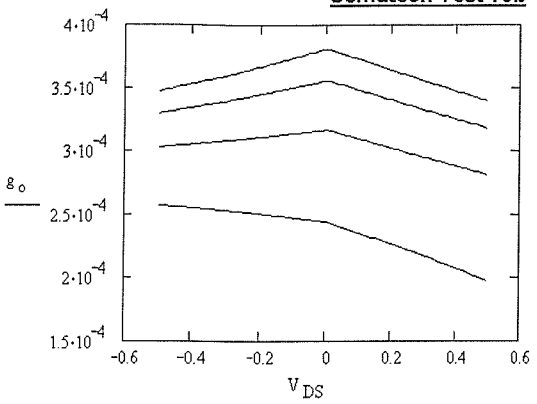


Device 1	Device 2

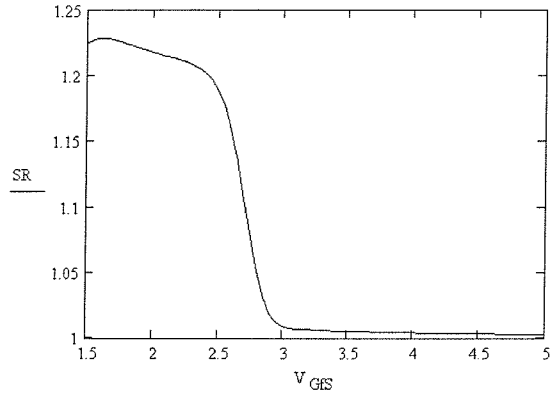
Sematech Test 18b



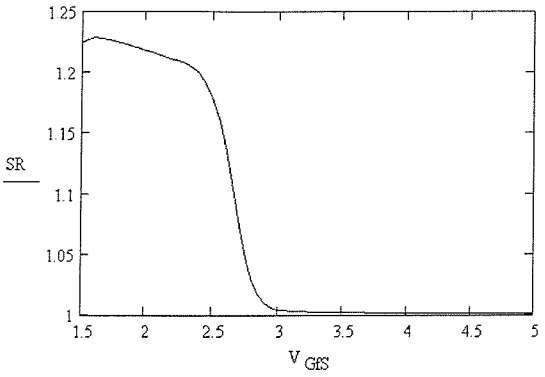
Sematech Test 18b



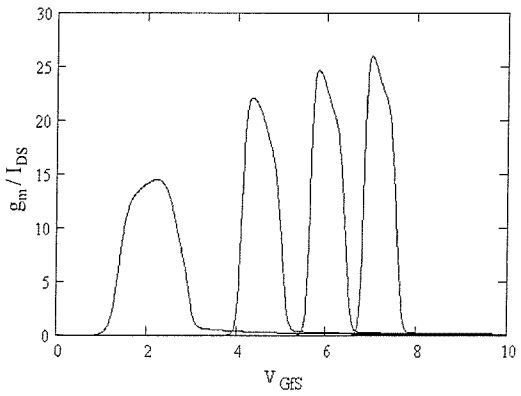
Sematech Test 19



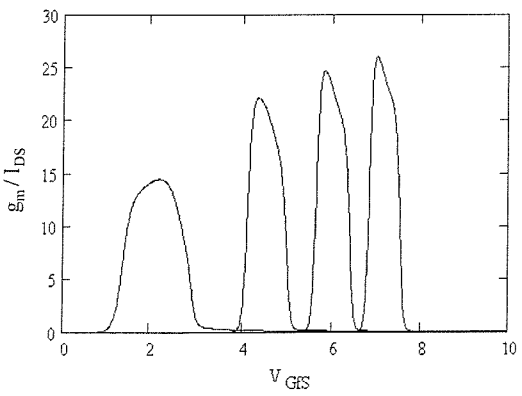
Sematech Test 19



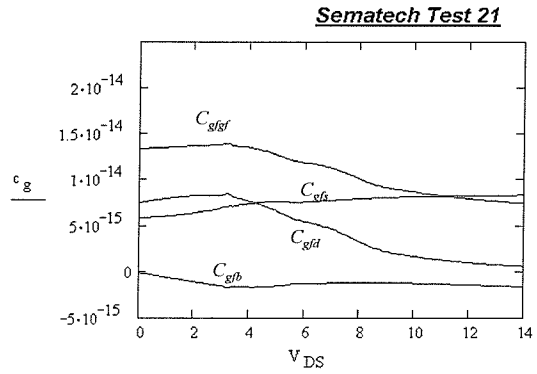
Sematech Test 20

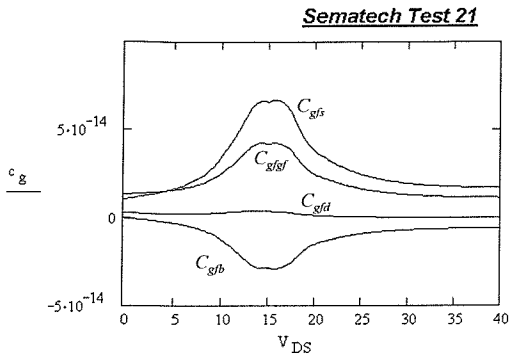


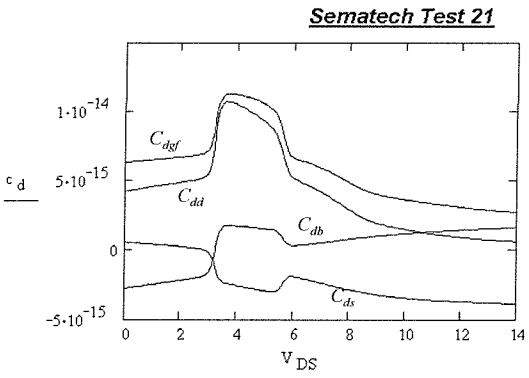
Sematech Test 20

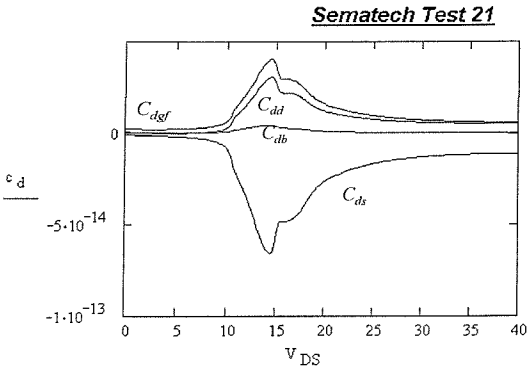


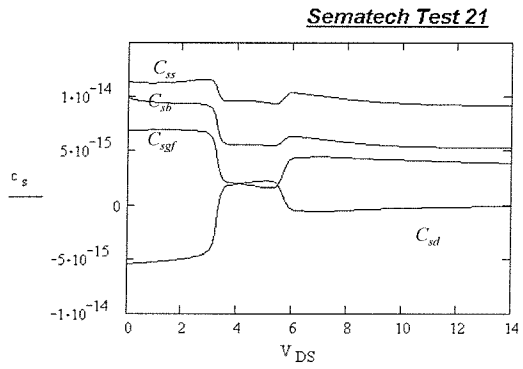
Device 1	Device 2

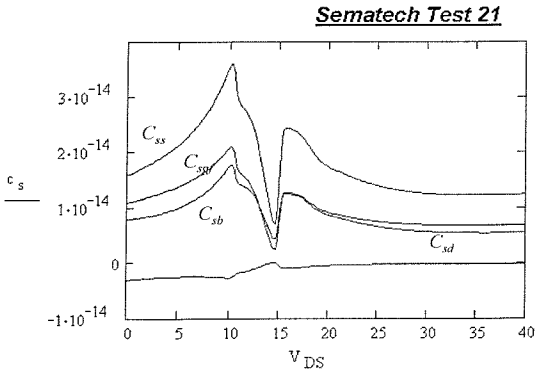




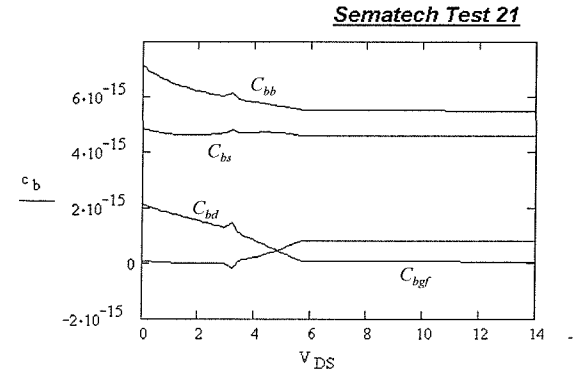


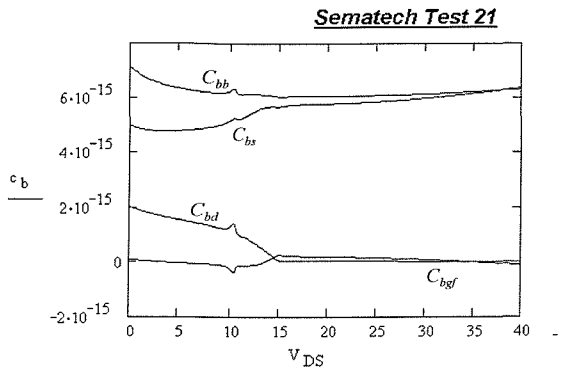


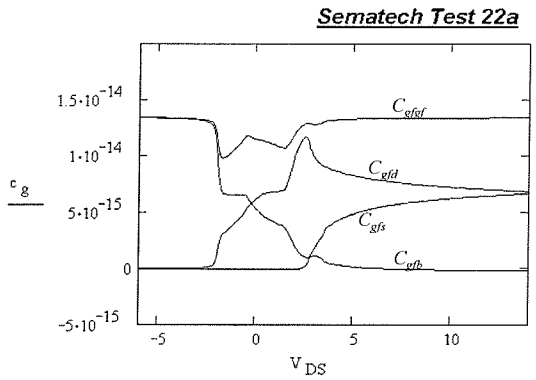


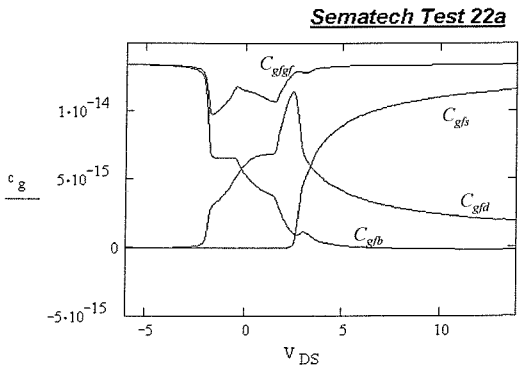


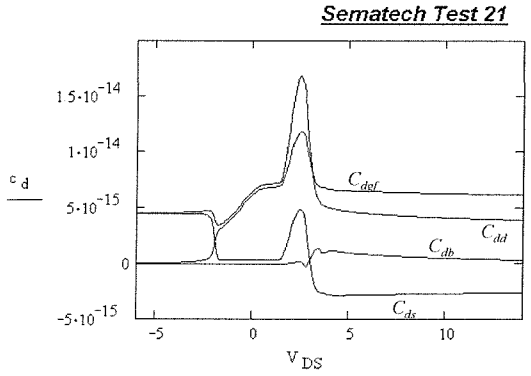
Device 1	Device 2

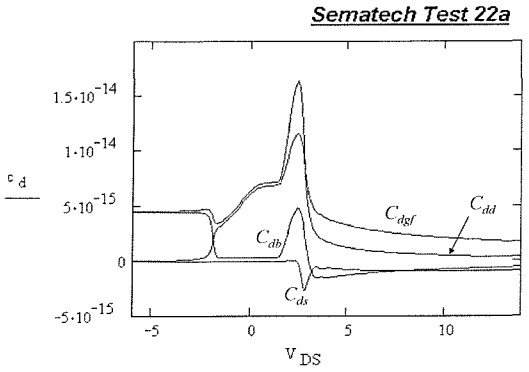






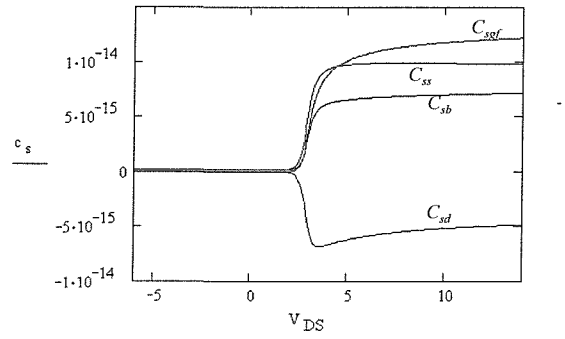




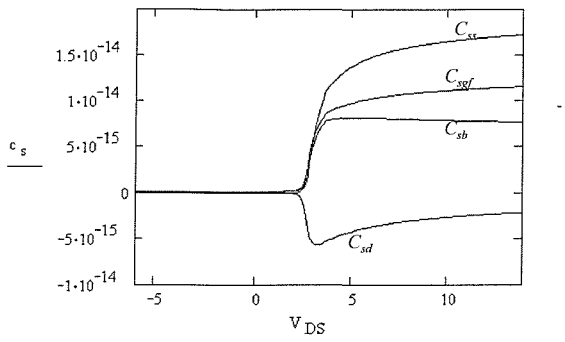


Device 1	Device 2

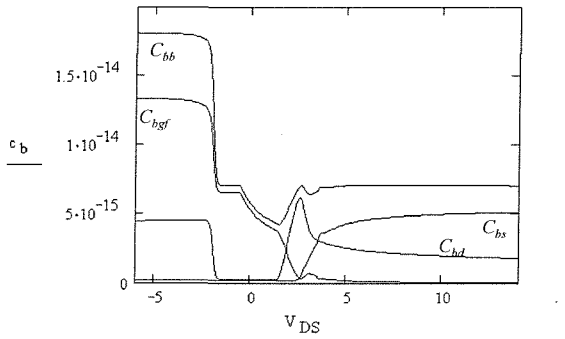
Sematech Test 22a



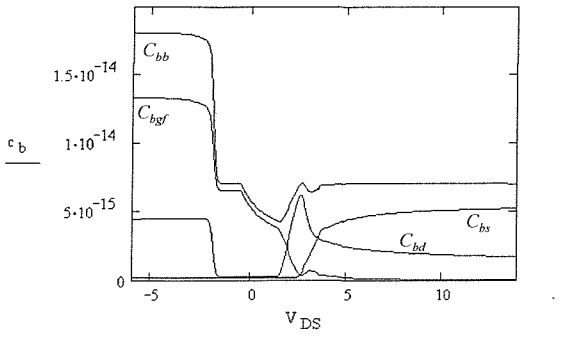
Sematech Test 22a



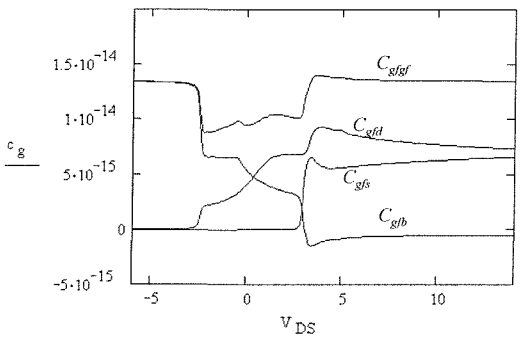
Sematech Test 22a



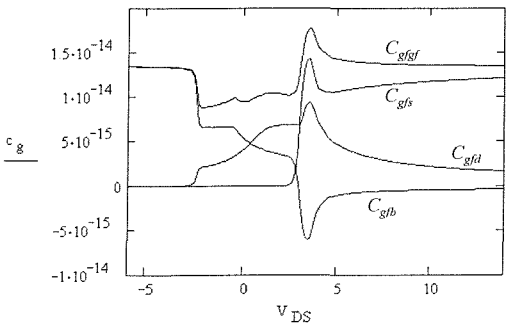
Sematech Test 22a



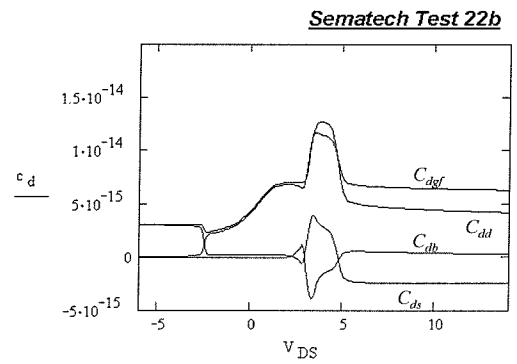
Sematech Test 22b

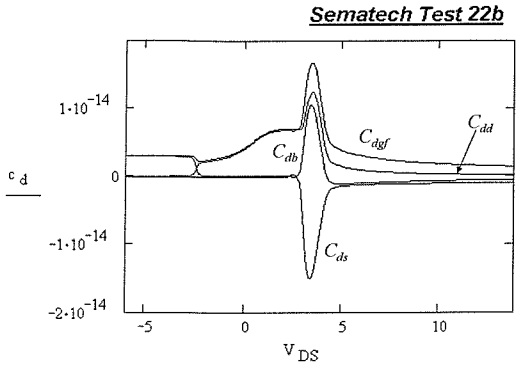


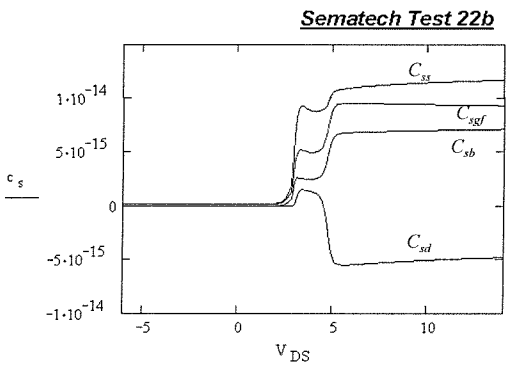
Sematech Test 22b

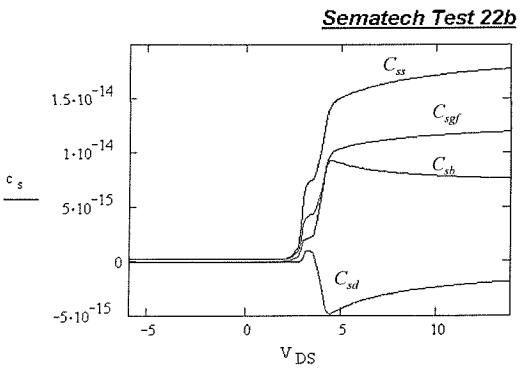


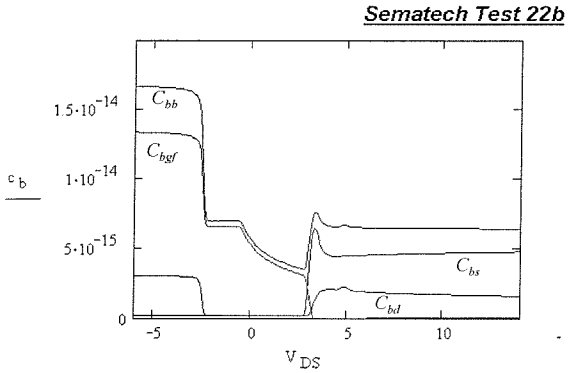
Device 1	Device 2





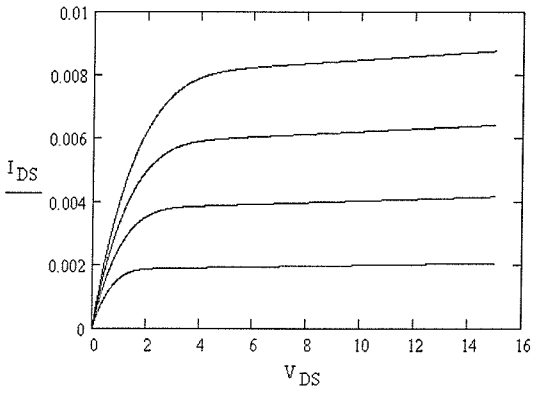




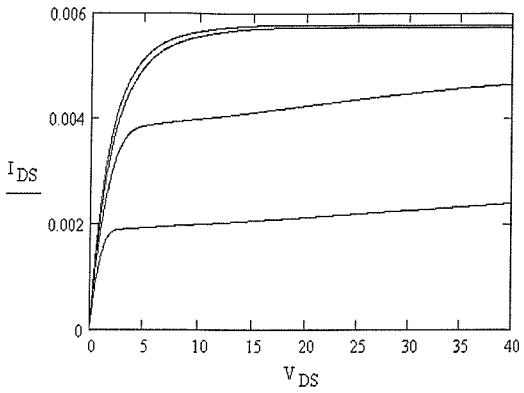


Device 3	Device 4

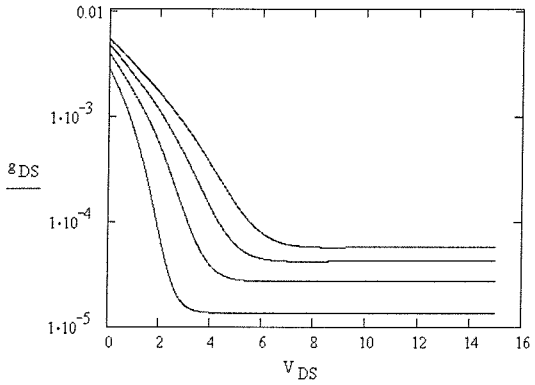
Sematech Test 2a



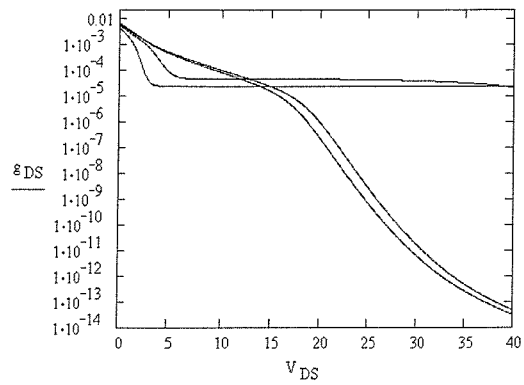
Sematech Test 2a



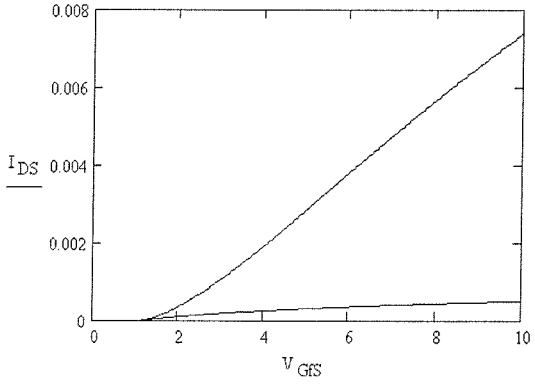
Sematech Test 2b



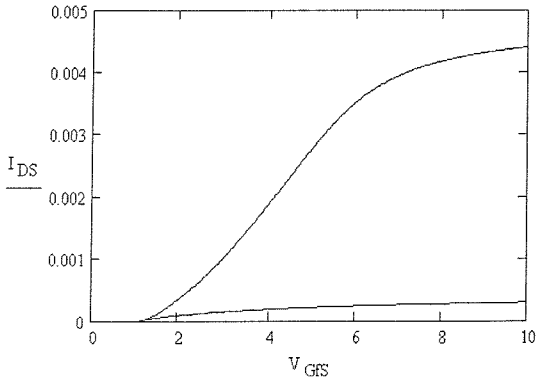
Sematech Test 2b



Sematech Test 3a

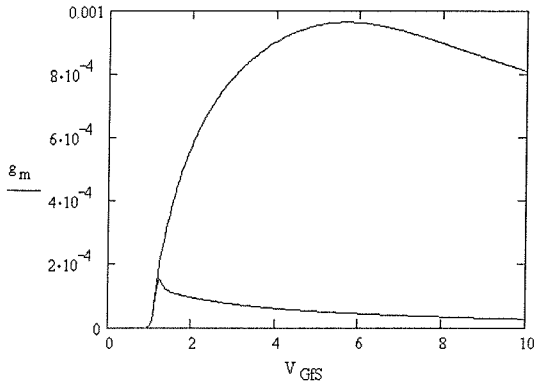


Sematech Test 3a

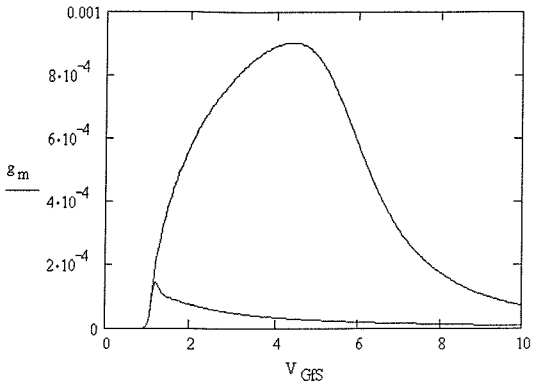


Device 3	Device 4

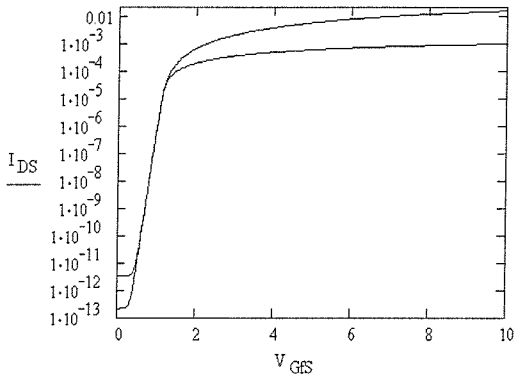
Sematech Test 3b



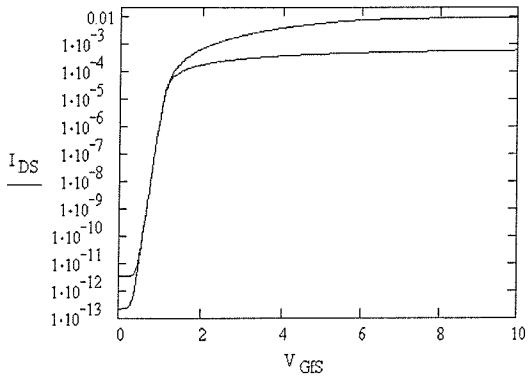
Sematech Test 3b



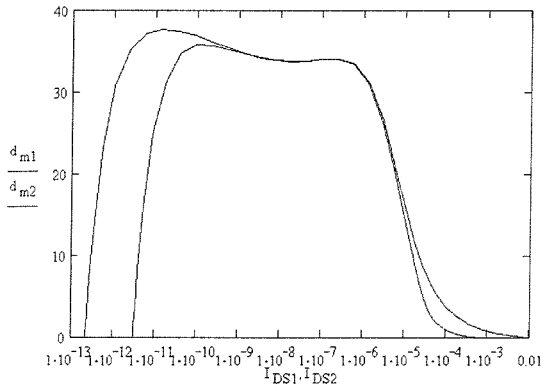
Sematech Test 4a



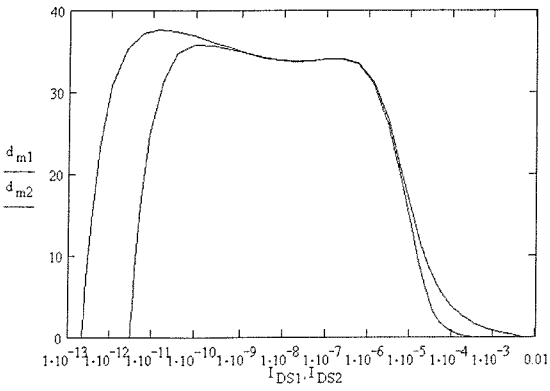
Sematech Test 4a



Sematech Test 4b

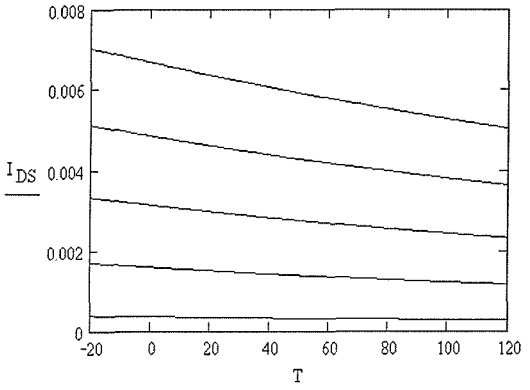


Sematech Test 4b

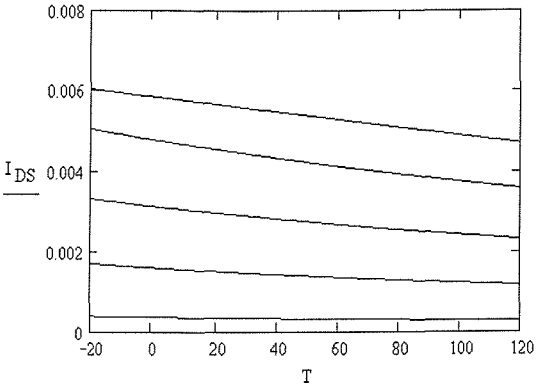


Device 3	Device 4

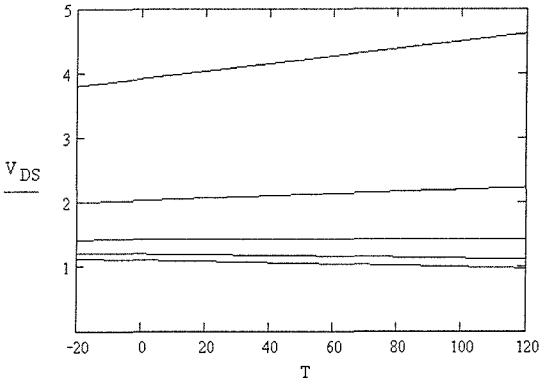
Sematech Test 5a



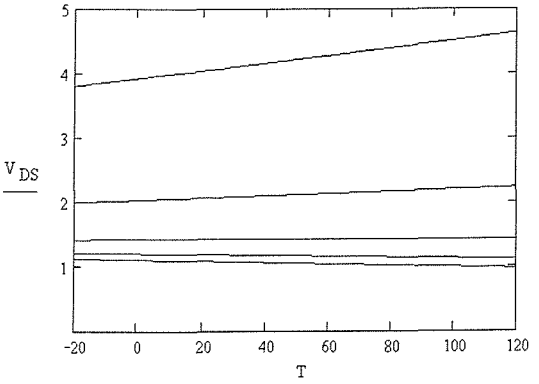
Sematech Test 5a



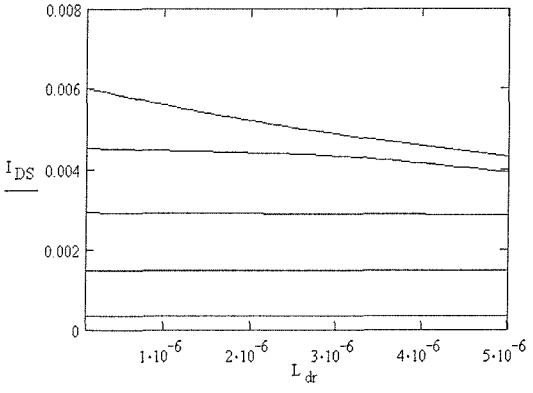
Sematech Test 5b



Sematech Test 5b

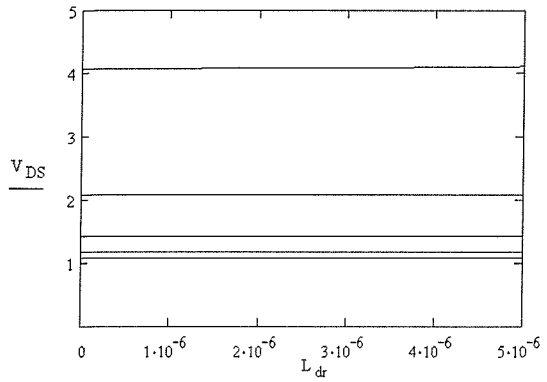


Sematech Test 6a

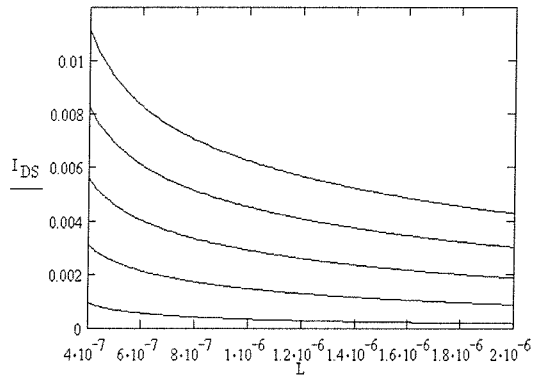


Device 3	Device 4

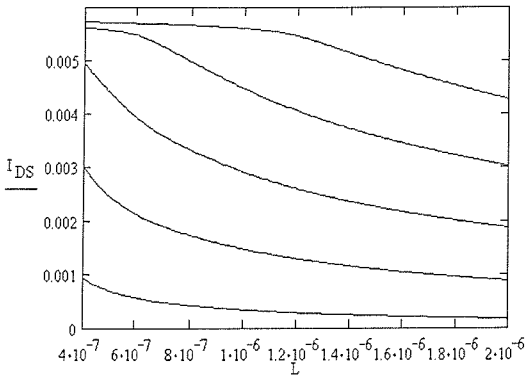
Sematech Test 6b



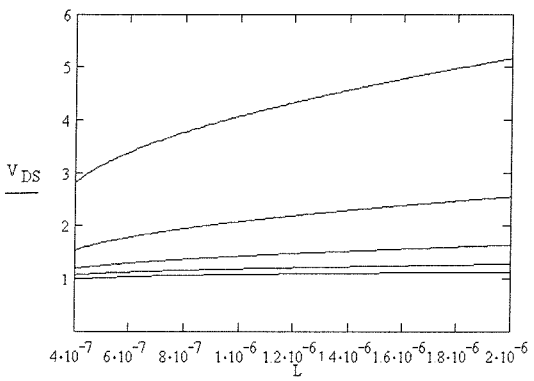
Sematech Test 6c



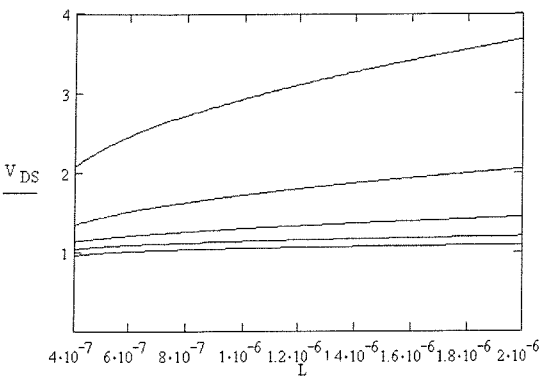
Sematech Test 6c



Sematech Test 6d

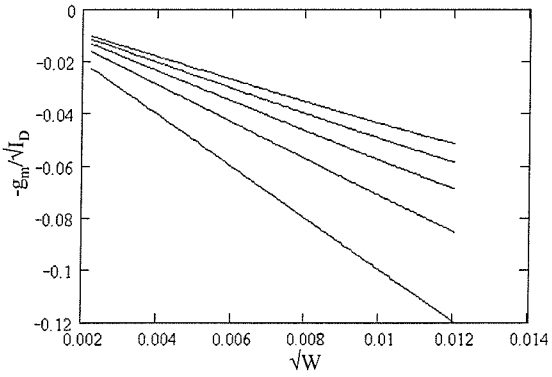


Sematech Test 6d

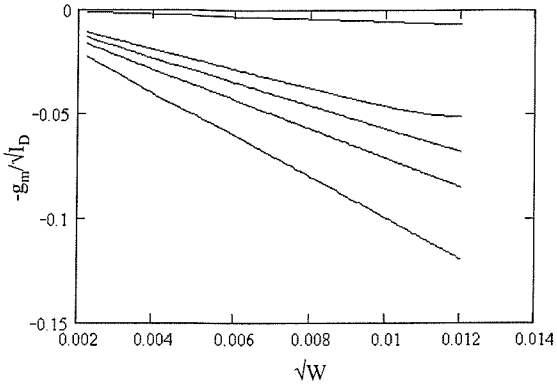


Device 3	Device 4

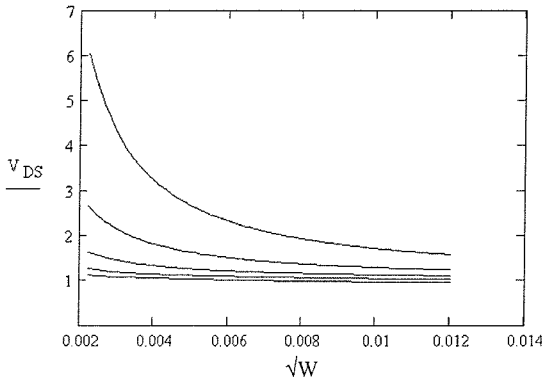
Sematech Test 7a



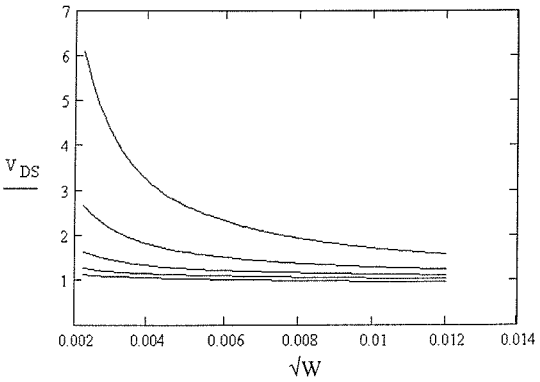
Sematech Test 7a



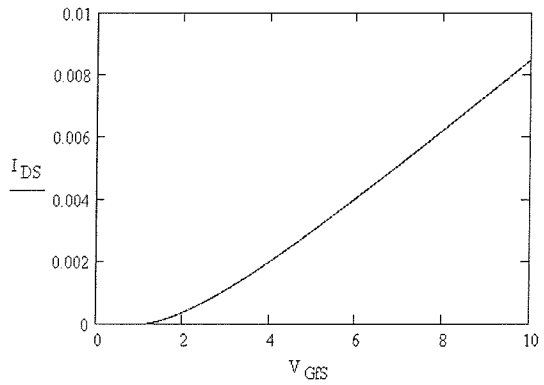
Sematech Test 7b



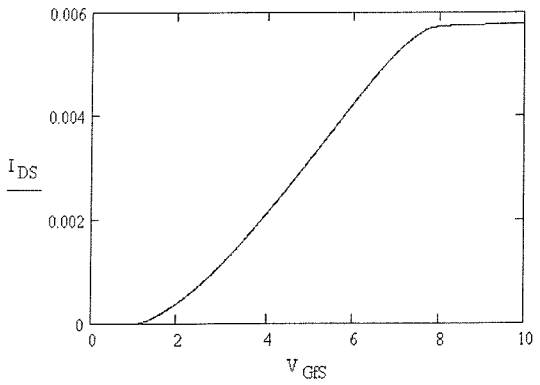
Sematech Test 7b



Sematech Test 8a

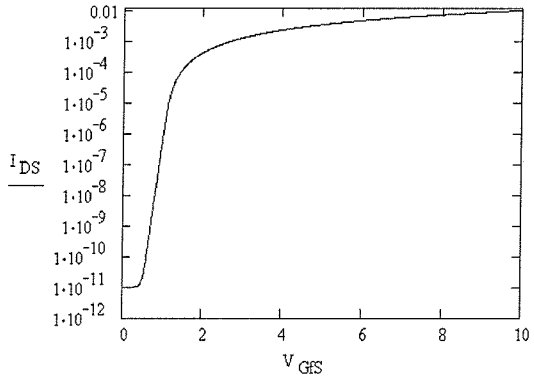


Sematech Test 8a

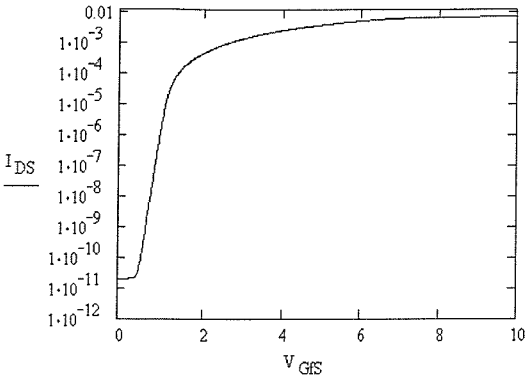


Device 3	Device 4

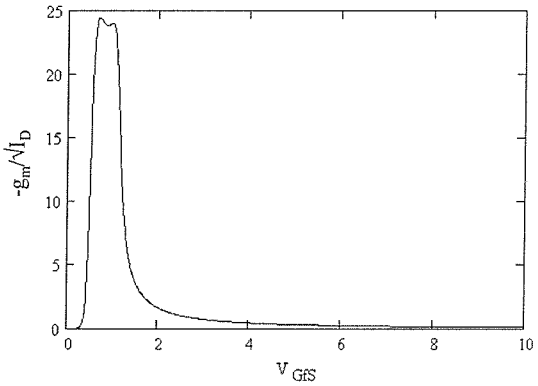
Sematech Test 8b



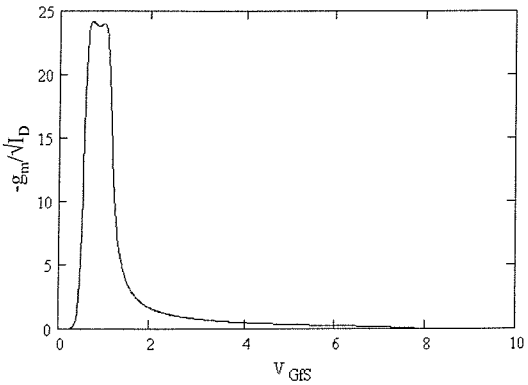
Sematech Test 8b



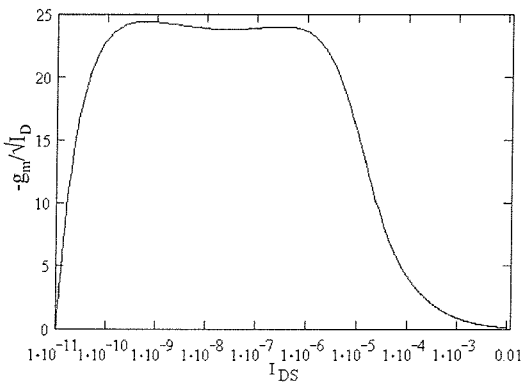
Sematech Test 9a



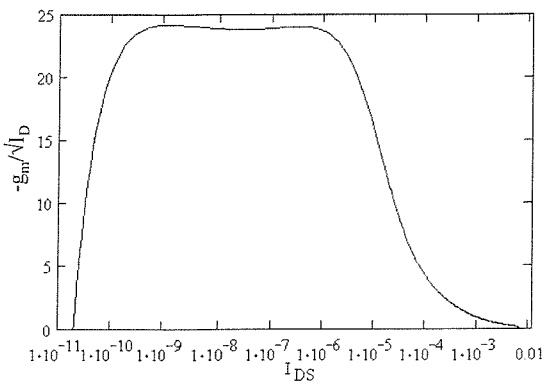
Sematech Test 9a



Sematech Test 9b

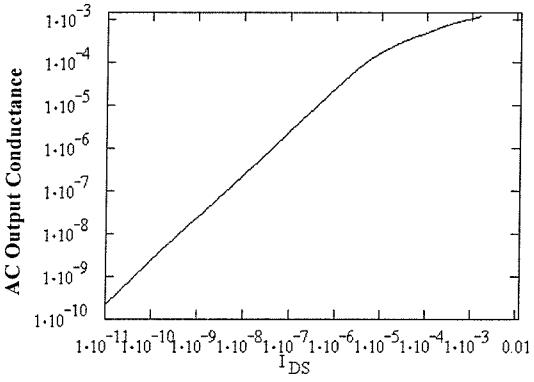


Sematech Test 9b

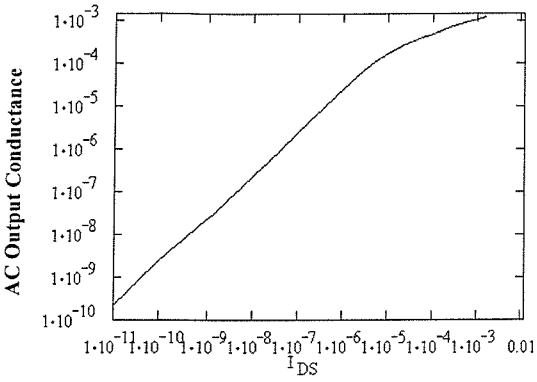


Device 3	Device 4

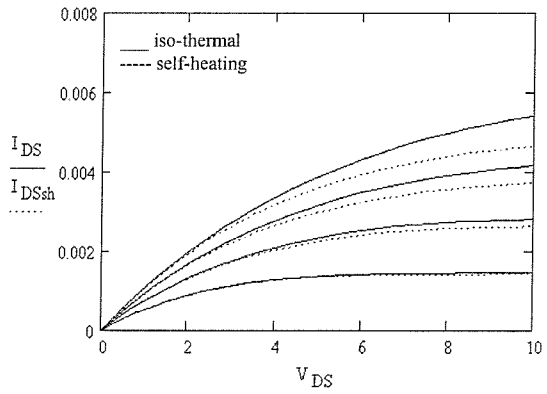
Sematech Test 10



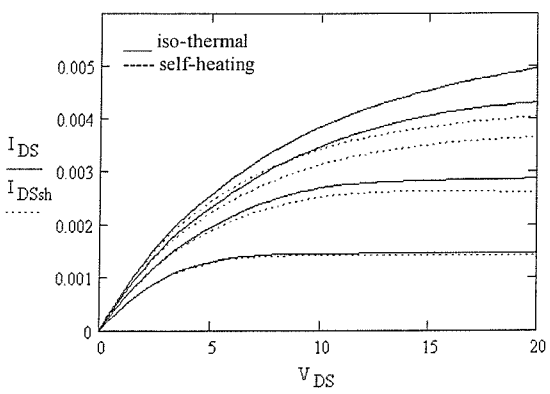
Sematech Test 10



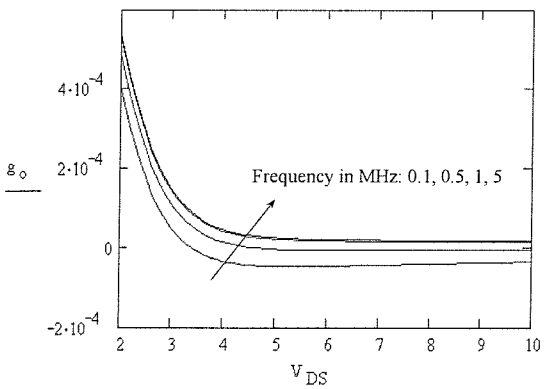
Sematech Test 11



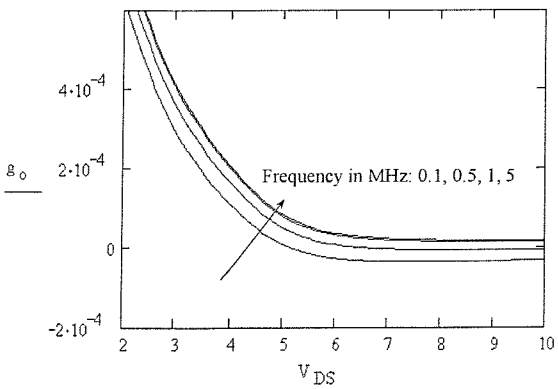
Sematech Test 11



Sematech Test 12a

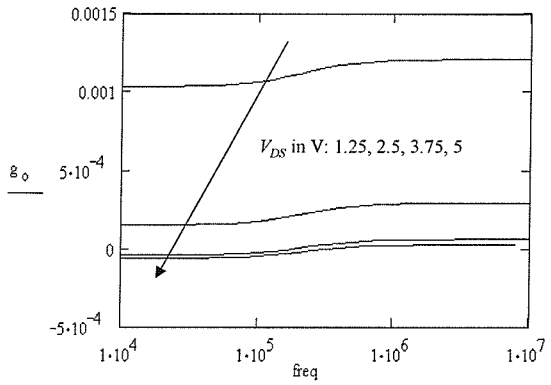


Sematech Test 12a

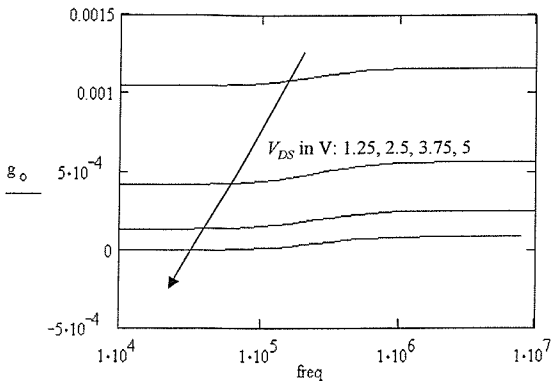


Device 3	Device 4

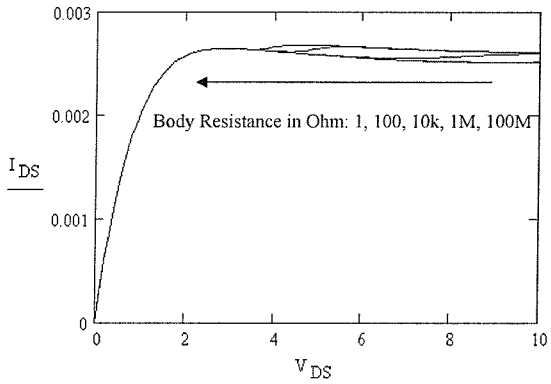
Sematech Test 12b



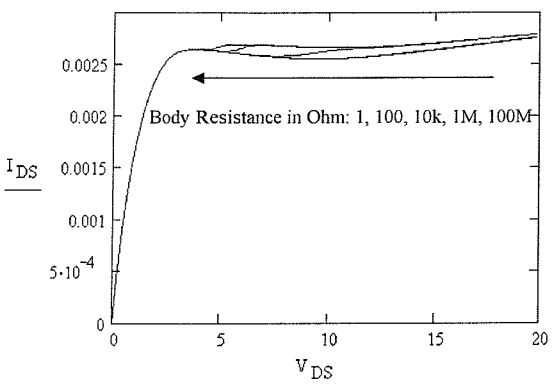
Sematech Test 12b



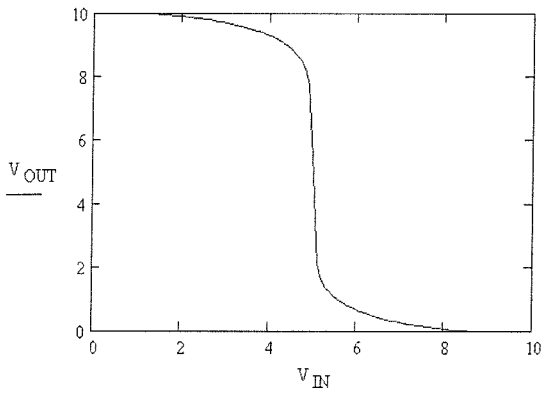
Sematech Test 13



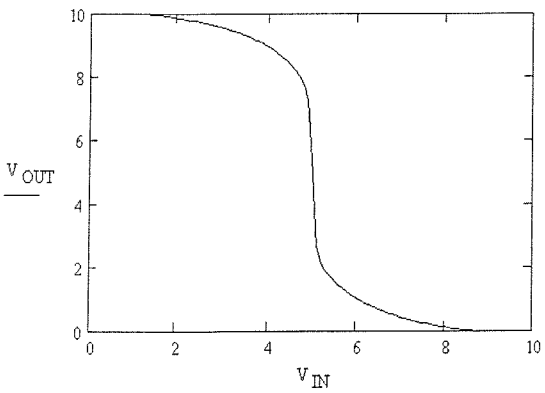
Sematech Test 13



Sematech Test 14

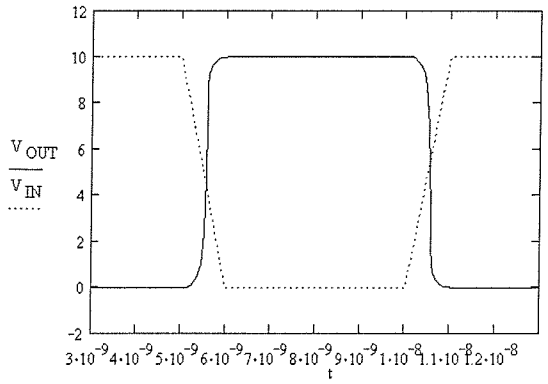


Sematech Test 14

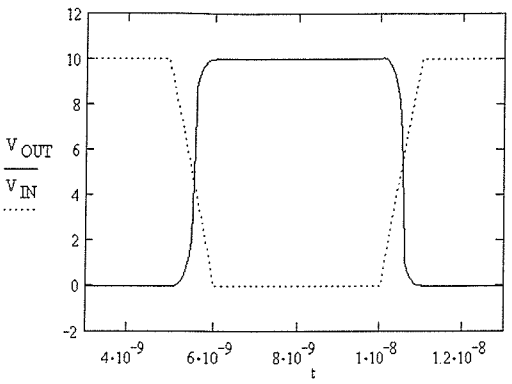


Device 3	Device 4

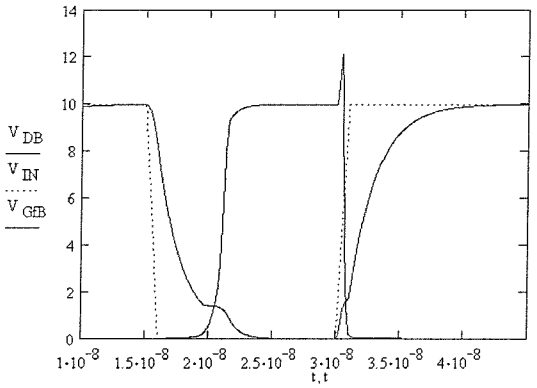
Sematech Test 15



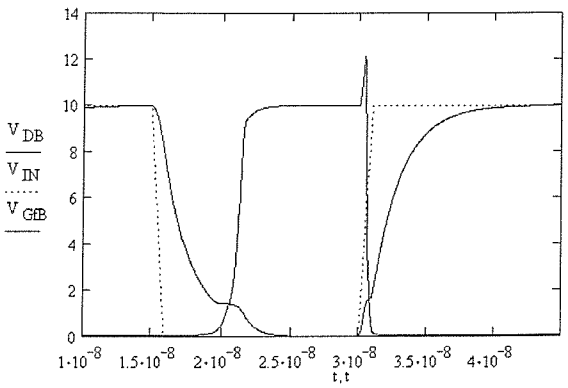
Sematech Test 15



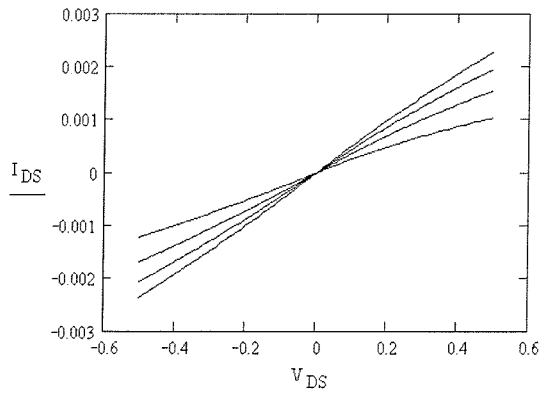
Sematech Test 16



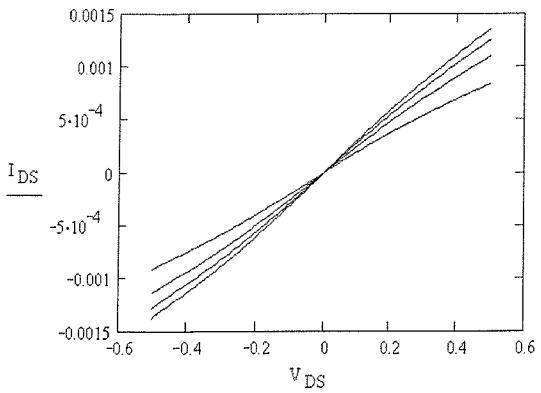
Sematech Test 16



Sematech Test 18a

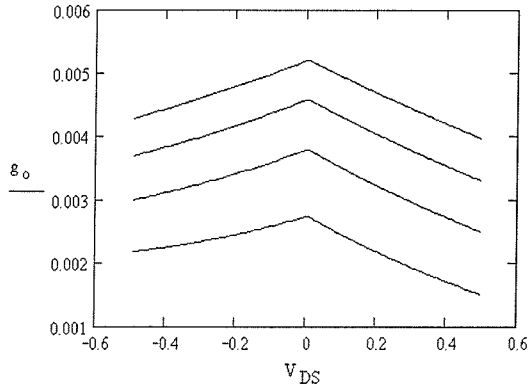


Sematech Test 18a

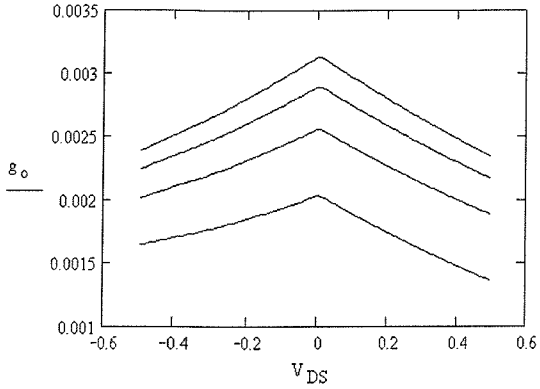


Device 3	Device 4

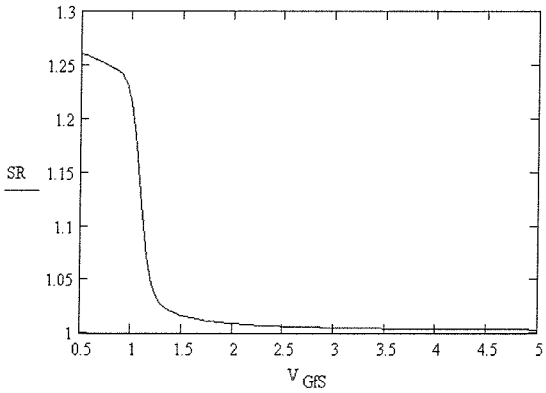
Sematech Test 18b



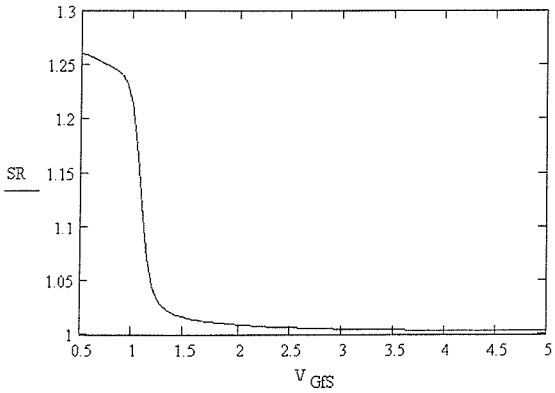
Sematech Test 18b



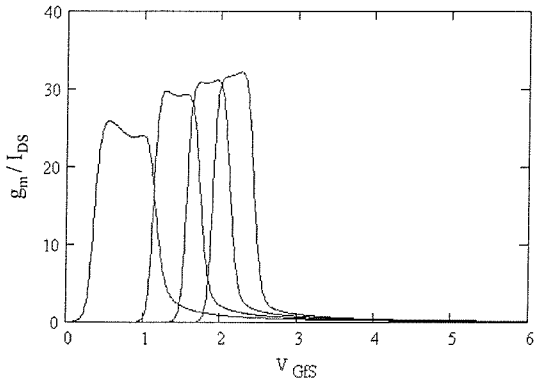
Sematech Test 19



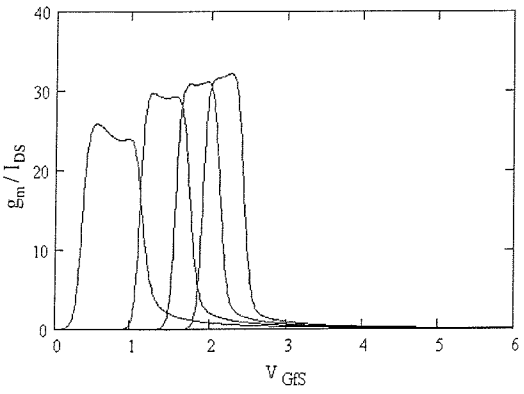
Sematech Test 19



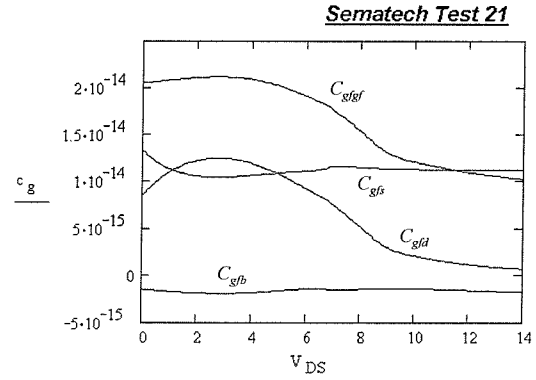
Sematech Test 20

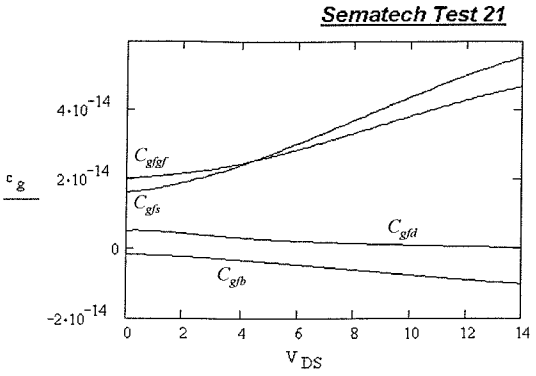


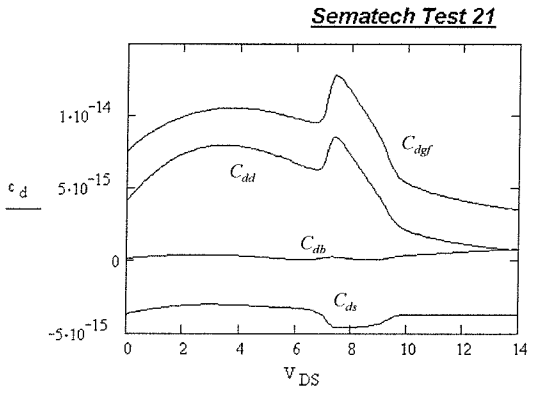
Sematech Test 20

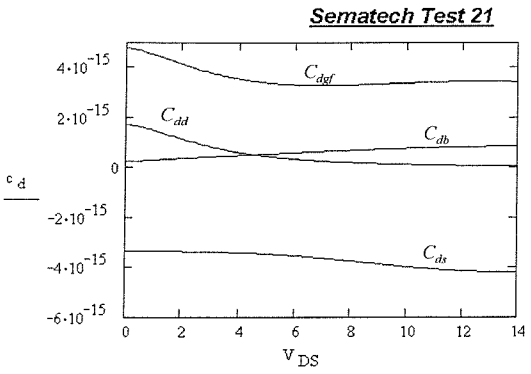


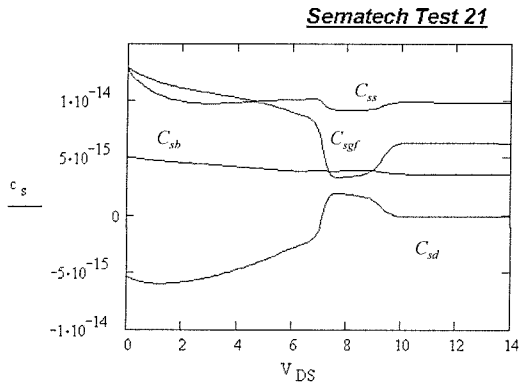
Device 3	Device 4

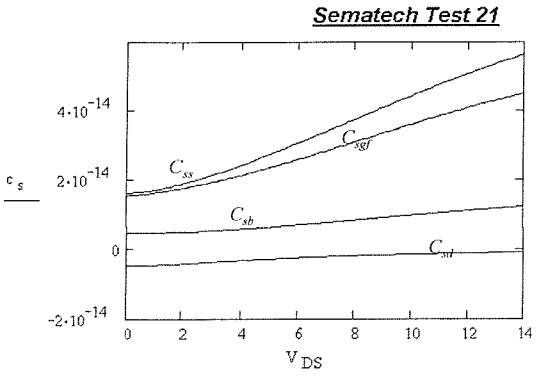






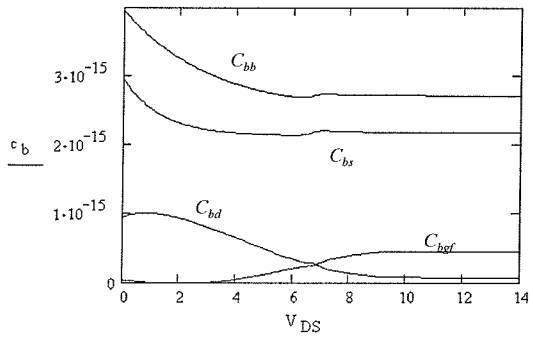




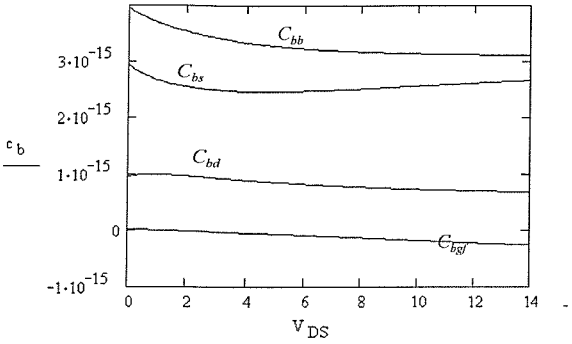


Device 3	Device 4

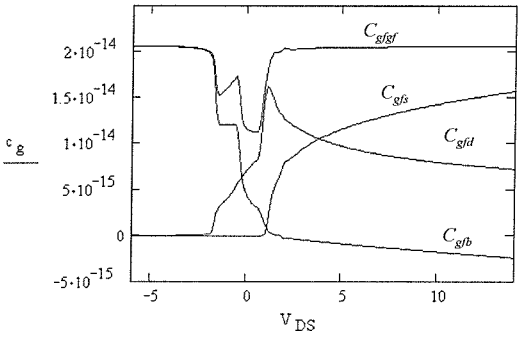
Sematech Test 21



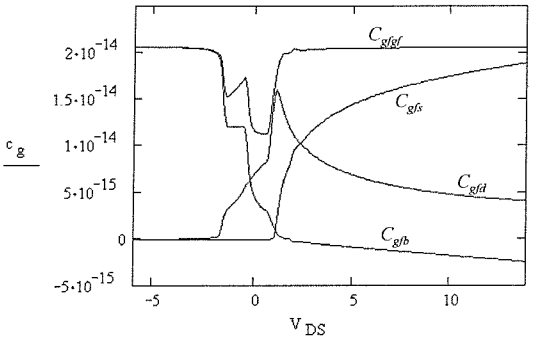
Sematech Test 21



Sematech Test 22a



Sematech Test 22a



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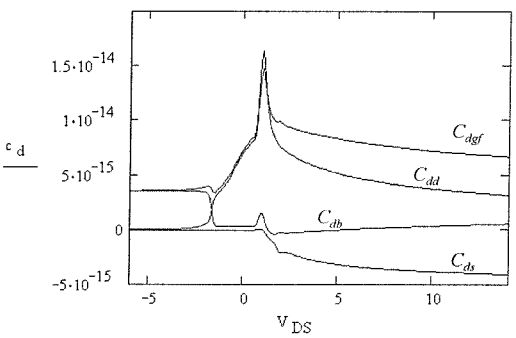

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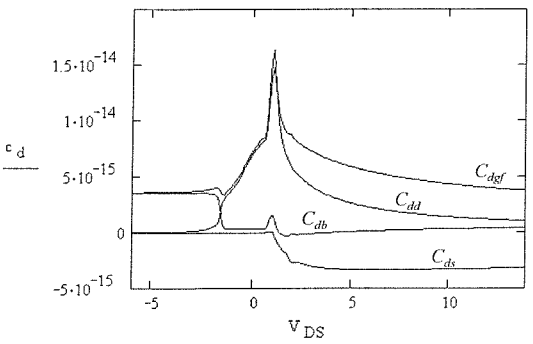
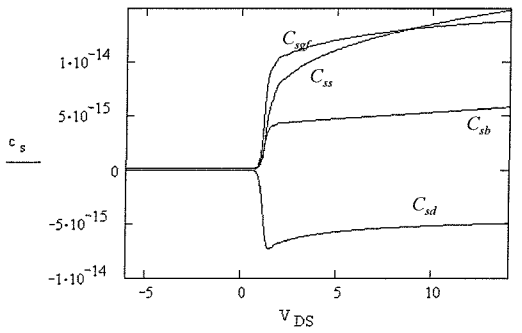
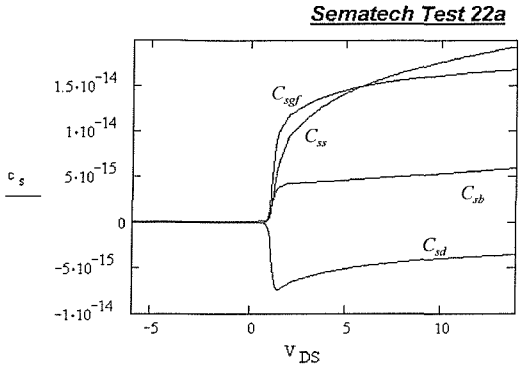


Device 3	Device 4

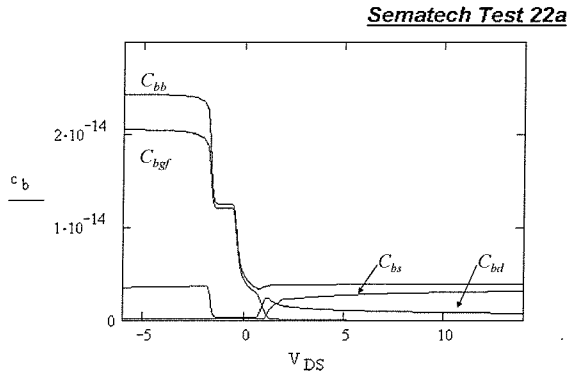
Sematech Test 22a



Sematech Test 22a



Sematech Test 22a



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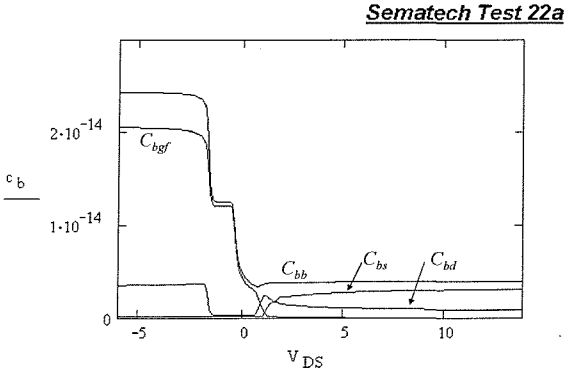
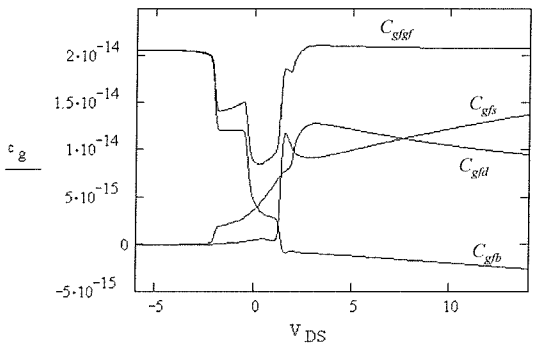
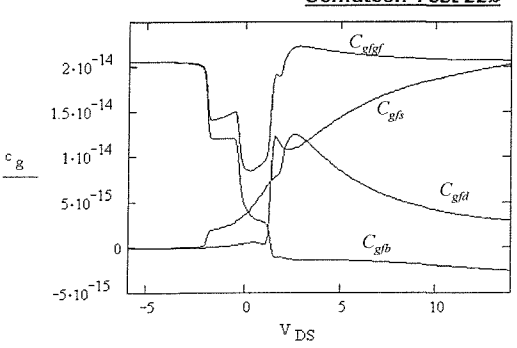


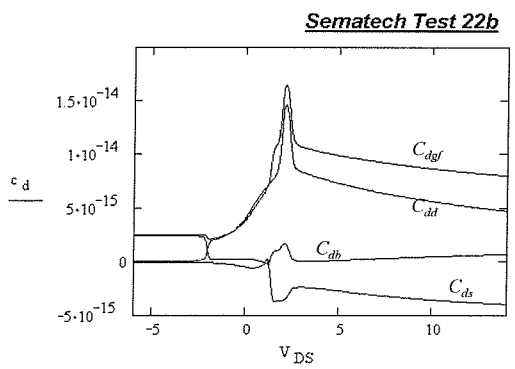
Sematech Test 22b

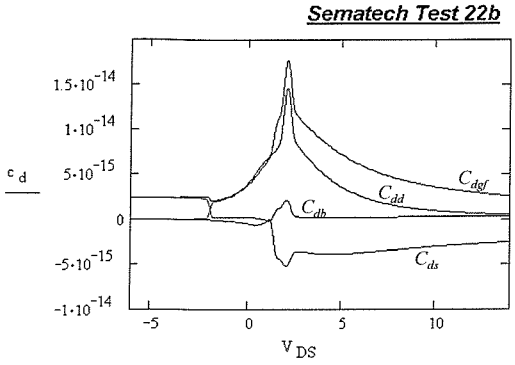


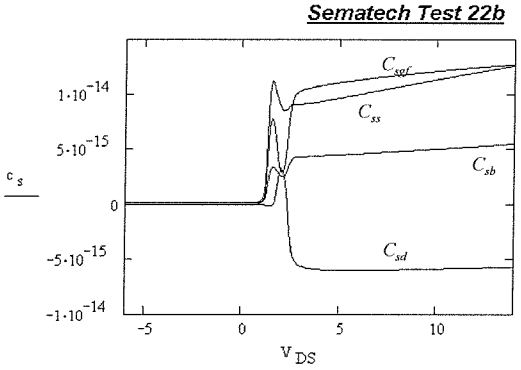
Sematech Test 22b

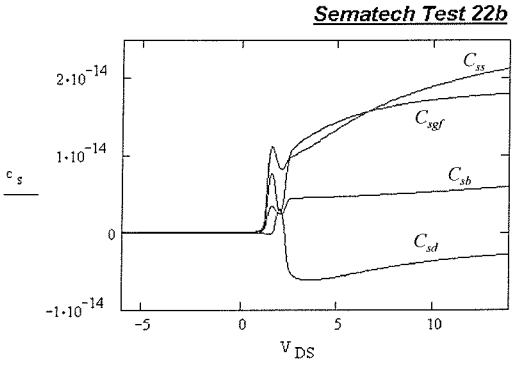


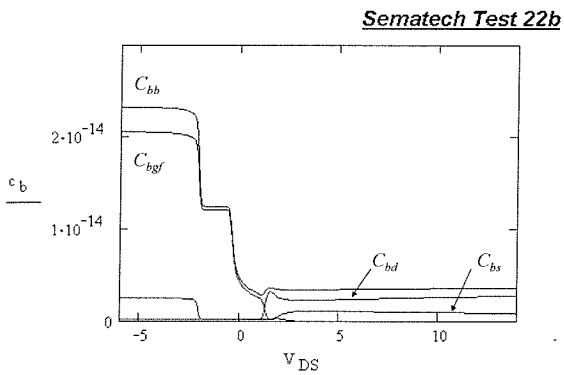
Device 3	Device 4

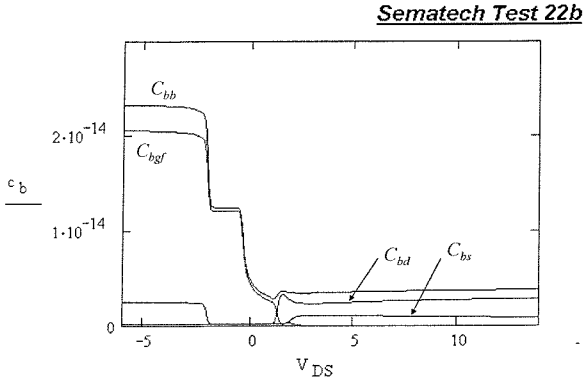












Appendix G

Parameter Set for the LV, MV and HV LDMOS

Parameter	LV N-LDMOS	MV N-LDMOS	HV N-LDMOS	HV P-LDMOS
L	1.45 μm	1.45 μm	1.45 μm	1.3 μm
L_{D}	0.3 μm	0.3 μm	0.3 μm	0 μm
L_{drov}	3.2 μm	1.7 μm	1.2 μm	2 μm
t_{of}	60 nm	60 nm	60 nm	60 nm
t_{ob}	3 μm	3 μm	3 μm	3 μm
t_{b}	1.5 μm	1.5 μm	1.5 μm	1.5 μm
t_{bdr}	0.9 μm	0.9 μm	0.5 μm	0.9 μm
V_{th0}	2.75 V	2.75 V	2.75 V	-3.7 V
N_{A}	0.75 10^{17}/ cm^3	0.75 10^{17}/ cm^3	0.75 10^{17}/ cm^3	0.75 10^{17}/ cm^3
$k_{\mathrm{N_A}}$	1.4	1.4	1.4	0.5
μ_{s}	700 cm^2/(V·s)	700 cm^2/(V·s)	600 cm^2/(V·s)	150 cm^2/(V·s)
θ	0.045 V^{-1}	0.045 V^{-1}	0.01 V^{-1}	0.11 V^{-1}
μ_{acc}	750 cm^2/(V·s)	750 cm^2/(V·s)	650 cm^2/(V·s)	200 cm^2/(V·s)
θ_{acc}	0.04 V^{-1}	0.04 V^{-1}	0.04 V^{-1}	0.081 V^{-1}
v_{sat}	2.2 10^7 cm/s	2.2 10^7 cm/s	5 10^7 cm/s	0.5 10^7 cm/s
σ	0	0	0	0
N_{D}	1.3 10^{16} /cm^3	1.3 10^{16} /cm^3	3 10^{16} /cm^3	0.7 10^{16} /cm^3
μ_{dr}	1250 cm^2/(V·s)	1250 cm^2/(V·s)	1250 cm^2/(V·s)	500 cm^2/(V·s)
v_{satdr}	1.4 10^7 cm/s	1.4 10^7 cm/s	5 10^7 cm/s	0.5 10^7 cm/s
f_{v}	0.5	0.3	1	0.1
λ_{r}	5 10^{-9} m/V	5 10^{-9} m/V	1 10^{-9} m/V	1 10^{-9} m/V
m	2	2	2	2
χ_{FB}	-3 10^{-3}	-3 10^{-3}	-3 10^{-3}	-4 10^{-3}
k	1.7	1.7	1.7	1.6
k_{acc}	2	2	2	1.6
k_{dr}	2.2	2.2	2.2	2.4
J_{s1Snom}	9.6 10^{-9} A/m	9.6 10^{-9} A/m	0 A/m	0 A/m
η_{D1S}	1.65	1.65	1.65	1.65
J_{sSnom}	6.8 10^{-11} A/m	6.8 10^{-11} A/m	0.32 10^{-12} A/m	4 10^{-12} A/m
η_{DS}	1.23	1.23	1.23	1.0
C_{JS}	0.2 10^{-10} F/m	0.2 10^{-10} F/m	0.2 10^{-10} F/m	1 10^{-10} F/m
J_{sDnom}	9.6 10^{-12} A/m	9.6 10^{-12} A/m	0.32 10^{-12} A/m	4 10^{-12} A/m
η_{DD}	1.23	1.23	1.23	1.0
J_{s1Dnom}	6.8 10^{-11} A/m	6.8 10^{-11} A/m	0 A/m	0 A/m
η_{D1D}	1.65	1.65	1.65	1.65
C_{JD}	0.3 10^{-10} F/m	0.3 10^{-10} F/m	0.2 10^{-10} F/m	1 10^{-10} F/m
C_{gfsor}	0.15 10^{-9} F/m	0.10 10^{-9} F/m	0.17 10^{-9} F/m	0.2 10^{-9} F/m
C_{gfdor}	0.24 10^{-9} F/m	0.18 10^{-9} F/m	0.8 10^{-9} F/m	0.2 10^{-9} F/m
C_{gfbor}	0.05 10^{-9} F/m	0.05 10^{-9} F/m	0.05 10^{-9} F/m	0.0 10^{-9} F/m
C_{gbsor}	0 F/m	0 F/m	0 F/m	0 F/m
C_{gbdor}	0.15 10^{-9} F/m	0.15 10^{-9} F/m	0.3 10^{-9} F/m	0.3 10^{-9} F/m
C_{gbbor}	0.1 10^{-9} F/m	0.1 10^{-9} F/m	0.1 10^{-9} F/m	0.1 10^{-9} F/m

Table G.1: *Parameter Set for the LV SOI N-LDMOS, the MV SOI N-LDMOS, the HV SOI N-LDMOS and the HV SOI P-LDMOS.*