DESIGN, FABRICATION AND CHARACTERISATION OF ADVANCED SUBSTRATE CROSSTALK SUPPRESSION STRUCTURES IN SILICON-ON-INSULATOR SUBSTRATES WITH BURIED GROUND PLANES (GPSOI)

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ABSTRACT

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Design, Fabrication and Characterisation of Advanced Substrate Crosstalk Suppression Structures in Silicon-on-Insulator Substrates with Buried Ground Planes (GPSOI)

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Substrate crosstalk or coupling has been acknowledged to be a limiting factor in mixed signal RF integration. Although, high levels of integration and high frequencies of operation are desirable for mixed mode RF and microwave circuits, they make substrate crosstalk more pronounced and may lead to circuit performance degradation. High signal isolation is dictated by requirements for low power dissipation, reduced number of components and lower integration costs for feasible system-on-chip (SoC) solutions.

Substrate crosstalk suppression in ground plane silicon-on-insulator (GPSOI) substrates is investigated in this thesis. Test structures are designed and fabricated on SOI substrates with a buried WSi_2 plane that is connected to ground; hence it is called a ground plane. A Faraday cage structure that exhibits very high degrees of signal isolation is presented and compared to other SOI isolation schemes. The Faraday cage structure is shown to achieve 20 dB increased isolation in the frequency range of 0.5-50 GHz compared to published data for high resistivity (200 Ω.cm) thin film SOI substrates with no ground planes, but where capacitive guard rings were used. The measurement results are analysed with the aid of planar electromagnetic simulators and compact lumped element models of all the fabricated test structures are developed. The accuracy of the lumped models is validated against experimental measurements.

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Last, but certainly not least, I would like to thank and dedicate this work to my parents and my brother. Their love and support helped me through the most difficult of times during the past three years.

Stefanos Stefanou

To my parents,
Niko and Anastasia
Στούς γονείς μου,
Νίκο και Αναστασία

List of Symbols

C	capacitance
C_a	active layer capacitance
C_{BOX}	buried oxide capacitance
C_e	even mode capacitance
C_J	junction capacitance
C_o	odd mode capacitance
C_{OX}	oxide capacitance
C_{SUB}	handle substrate capacitance
ϵ_0	permittivity of free space
ϵ_r	relative permittivity
f	frequency
f_c	cutoff frequency
G	conductivity
H	substrate thickness
$K(k_1)$	complete elliptic integral
ρ	resistivity
R	resistance
R_a	active layer resistance
R_{SUB}	handle substrate resistance
R_0	50 Ω source and load
S	spacing
s_{21}	forward transmission scattering coefficient
ω	angular frequency $(2 \cdot \pi \cdot f)$
W	width
y	admittance parameters

Acronyms

ACP	Air CoPlanar
BiCMOS	Bipolar Complementary Metal Oxide Semiconductor
CAD	Computer Aided Design
CMOS	Complementary Metal Oxide Semiconductor
CPW	CoPlanar Waveguide
DUT	Device Under Test
EM	ElectroMagnetic
FET	Field Effect Transistor
GP	Ground Plane
GPSOI	Ground Plane Silicon On Insulator
GSG	Ground Signal Ground
IC	Integrated Circuit
ITRS	International Technology Roadmap for Semiconductors
LPCVD	Low Pressure Chemical Vapour Deposition
LRRM	Load-Reflect-Reflect-Match
MCM	Multi-Chip Module
MOS	Metal Oxide Semiconductor
PECVD	Plasma Enhanced Chemical Vapour Deposition
RF	Radio Frequency
Rx	Receiver
SEM	Scanning Electron Microscope
SOA	Silicon-On-Anything
SoC	System on Chip
SOI	Silicon-On-Insulator
SOS	Silicon-On-Sapphire
SSOI	Silicide Silicon-On-Insulator
TEOS	TetraEthOxySilane
Tx	Transmitter

Chapter 1

Introduction

The continuous trend towards miniaturisation and the increase of the operating speed of Integrated Circuits (IC's) has nowadays made the influence of on chip parasitics very important. The interaction between several parts of an IC or its packaging, referred as crosstalk or noise coupling, has been the subject of research for many years, since it represents a limiting factor in IC technology especially at very high operating frequencies. Higher levels of integration deteriorate the problem, which appears in its worst form in radio frequency (RF), microwave mixed signal ICs, including switched capacitor filters and A/D and D/A converters.

Noise coupling within an IC occurs through the common substrate and through the capacitances of interconnect lines. The common substrate acts as a collector, integrator and distributor of coupled noise. The analogue part of a mixed signal IC suffers the most from substrate crosstalk. The digital part is characterised by strong and sudden signal switching which has as an immediate effect the injection of significant levels of noise into the substrate. Sensitive analogue circuitry lying on the same substrate is affected significantly by the transmitted noise. The performance degradation can be so severe, it can lead to physical separation of the digital and analogue parts in different chips. Although hybrid multi-chip modules (MCM) may be adequate they are limited by inter-chip interconnect parasitics. Single chip implementations, however, are often the smallest, lower cost and lowest power solutions. Hence, substrate crosstalk is a fundamental limitation of today's mixed signal IC design and fabrication.

It must be noted that apart from the analogue part, high speed sequential circuits sharing a common substrate can be affected by noise coupling transients. Aragones et. al. [5] have demonstrated how noise transients can cause permanent errors on a RAM cell during read and write cycles.

Crosstalk reduction techniques can be categorized as follows: (a) those that minimize the strength of the noise source, and (b) those that reduce the noise coupling. The first approach requires fundamental changes in the design methodologies and incorporation of additional circuitry to compensate for the substrate losses. Liu et. al. [6] have proposed an active technique based on negative feedback. Coupling minimisation has been addressed by introducing new structures such as capacitive guard rings [1], [7], [8], [9], [10], [11], [12] that surround the sensitive devices and break the coupling path of the substrate. More sophisticated substrates, compared to bulk, can also provide increased isolation. Several studies have been performed on SOI substrates and it has been shown that they offer superior isolation performance at least for frequencies up to 1 GHz [1]. Higher frequencies of operation for RF IC's dictate the use of high resistivity substrates as preferred substrate for mixed signal integration. Raskin et. al. [1] have shown the efficiency of the latter in conjunction with the use of guard rings. High resistivity SOI substrates present, however, a more expensive solution compared to substrates used in mainstream CMOS processes. Bulk CMOS substrates usually have a resistivity at least ten times lower than that of high resistivity substrates.

Besides measuring the absolute isolation level of different substrates structures, it is vital that a deeper understanding of the dynamics and physics involved in substrate coupling is acquired. The effect of parameters such as the separation distance of the noise source from the sensor and the effect of different dielectrics has to be known, in order to be able to predict the behaviour of such substrates under operating conditions. Such research can be accomplished with the help of Computer Aided Design (CAD) Tools and particularly numerical simulators.

A great deal of research on numerical methods that attempt to accurately evaluate and model substrate parasitics has been done over the past few years [13], [14], [6]. The disadvantages, however, of these methods are the long simulation times and the large requirements of computer resources. Simpler lumped element models are needed that can accurately capture the behaviour of substrate parasitics and that can simultaneously be used in circuit simulators, such as SPICE. These models ideally have to be scalable and valid over a wide frequency range [1]-[15].

This work investigates the isolation performance of SOI substrates with buried ground planes. The ground plane SOI (GPSOI) substrate is effectively an SOI substrate with a thin buried metallic layer below the insulator. The buried metallic plane is called buried ground plane because it is connected to ground. The material is new and is manufactured as described in [16], [17], [18]. Substrate crosstalk studies for this material are performed for the first time and its noise suppression

performance is compared to different existing isolations schemes. The studies are concentrated on frequencies in the GHz range.

This thesis is organised as follows: Chapter 2 discusses different existing crosstalk reduction schemes studies. A detailed reference to all the schemes and their performance is included along with the advantages and disadvantages of each of them. A methodology of studying substrate coupling along with the figures of merit for isolation performance is explained in detail. Such methodology has been used for most high frequency crosstalk studies. Modelling issues are also discussed along with a description of the capabilities and the efficiency of the CAD tools used to model the specific substrate. Finally, lumped element models introduced so far in the literature are presented as a base for future use with the ground plane substrate.

Chapter 3 presents the test structures fabricated on the GPSOI substrate to evaluate its noise suppression performance. The choice of such structures is justified as part of the methodology mentioned in the previous chapter. Issues regarding the fabrication process are also presented along with a detailed description of the measurement technique. Such a discussion will provide insight into the problems that may appear when measuring low crosstalk structures at very high frequencies. Careful control of the measurement conditions is necessary to ensure high levels of repeatability and consistency over a number of measurements.

Electromagnetic and lumped element modelling of crosstalk in substrates with buried ground planes is presented and discussed in Chapter 4 with emphasis on the specific test structures presented in Chapter 3. Simulation results from two electromagnetic solvers verify the measurement results of the previous chapter. Lumped element equivalent circuits that are based on the theory of coupled microstrip lines and model the behaviour of the test structures are also presented and validated against simulation and measurement data. Chapter 5 presents experimental results of pseudo-ground plane test structures used to emulate the behaviour of the buried ground plane test structures of chapters 3 and 4. These test structures are realised using a two metal layer process, where the first metal acts as a buried ground plane. The effects of the buried oxide thickness and the resistivity of the ground plane are discussed not only for the conventional test structures already shown in previous chapters but also for long (500 μm) microstrip lines. Measurement results and analysis of test structures with variable oxide thickness and ground planes of different materials (aluminium and titanium silicide) are included.

An analysis of crosstalk between two diodes realised on standard (9-15 Ω.cm) and high (200 Ω.cm) resistivity substrates is presented in Chapter 6. Electromagnetic simulations and microwave strip line theory are employed and equivalent circuits of

substrate crosstalk in similar test structures are developed. This chapter acts as a "bridge" between the analysis of a buried ground plane in a substrate and the SOI substrates of Chapter 6.

Having analysed separately the impact of a ground plane on crosstalk and the coupling between two devices on a SOI substrate, Chapter 7 presents a model of substrate crosstalk in GPSOI substrates. The development of the model is based on the conclusions drawn from the analyses of previous chapters. Measurement results of test structures on GPSOI are compared with SOI substrates and the model is validated against them.

Chapter 8 of this work introduces a Faraday cage structure having advanced crosstalk suppression capabilities. Vertical metal-filled trenches and the buried ground plane underneath the oxide form a cage and surround the noise transmitter and receiver nodes. The superior performance of this structure is explained with the aid of electromagnetic simulations.

Chapter 9 summarises the results of this work, focusing at the same time at research topics that may be pursued in the future.

Chapter 2

Substrate Crosstalk Theory and Literature Review

2.1 Introduction

Substrate crosstalk or coupling is defined in this chapter. Metrics of performance are discussed and several isolation schemes that have been researched previously in the literature are presented. Comparison of these isolation schemes provides some insight into the level of the crosstalk suppression that have been achieved to date in SOI substrates. A brief reference to the electromagnetic solvers that will be used to analyse substrate crosstalk concludes this chapter.

2.2 Substrate Crosstalk Definition and Metrics

The undesirable interaction between different parts of an integrated circuit is referred to as crosstalk. When this interaction exists through the common silicon substrate, where the different components of an IC are fabricated, it is called substrate crosstalk or substrate coupling. Decreasing the substrate crosstalk can result in higher degrees of isolation between devices, circuits and systems. Crosstalk is measured under small signal operation and the measurement techniques can be divided into two categories: time domain measurements and frequency domain measurements.

Time domain measurements employ transient analysis of the test structure and measurement of a time dependent parameter [19], [5], [20]. This kind of technique has been used to model crosstalk between interconnect lines, where one line acts as a noise transmitter ("aggressor" line) and the other lines are the noise receivers or "victim" lines. A noise transient can also be injected into the substrate through a transistor (usually MOS). As a result fluctuations are caused and propagate through the substrate to a remote sensor, usually a diffused contact. The level of substrate

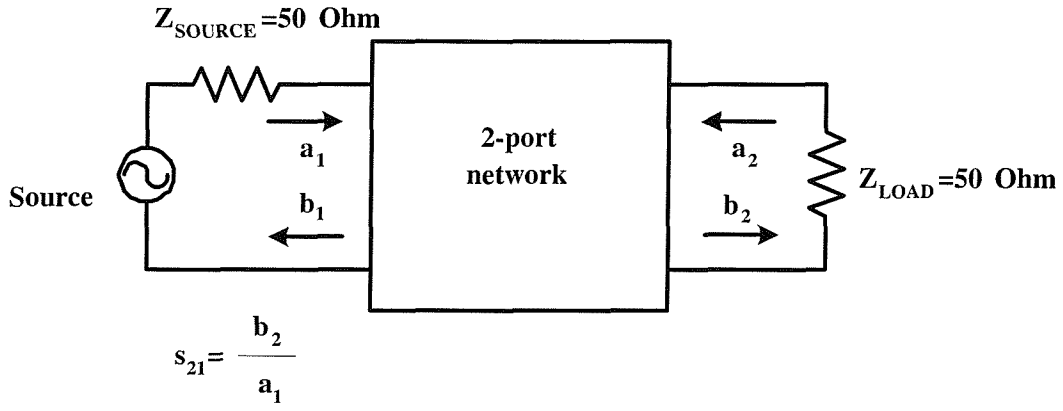


Figure 2.1: Scattering transmission coefficient definition.

crosstalk is then determined by measuring the peak-to-peak level of the fluctuations at the sensor.

When the level of crosstalk is determined in the frequency domain, a particular parameter is measured over a certain frequency range. Scattering parameters (S parameters) are used for RF measurements and have been established as the preferred parameters for system characterisation compared to impedance, admittance, hybrid, and transmission parameters because they overcome the problem of practically unachievable open- or short-circuit conditions for measurement. Scattering parameters describe a network's input-output properties in terms of incident and reflected power waves. An accepted quantitative measure of crosstalk in the frequency domain is the magnitude of the forward scattering coefficient s_{21} [1]-[10]. S_{21} is the ratio of the transmitted power wave at port 2 over the incident power at port 1 of a two-port network. In the case of crosstalk studies, port one is a noise transmitter and port two is the noise receiver. The lower the magnitude of s_{21}, the lower the crosstalk and hence the higher the degree of isolation. Crosstalk suppression in this work is accessed only by measuring the magnitude of s_{21} and not through time domain measurements.

2.3 Comparison of Crosstalk in Different Technologies

In standard bulk CMOS processes the devices are integrated at the surface of a uniformly doped Si substrate. Figure 2.2 shows the coupling path of the noise injected from an input node and received by an output node. It can be observed that crosstalk is a surface phenomenon since the most important coupling path is located at the surface of the substrate [1]. The coupling decreases with depth. Crosstalk can be decreased by increasing the separation between the crosstalk source (input) and sensor (output).

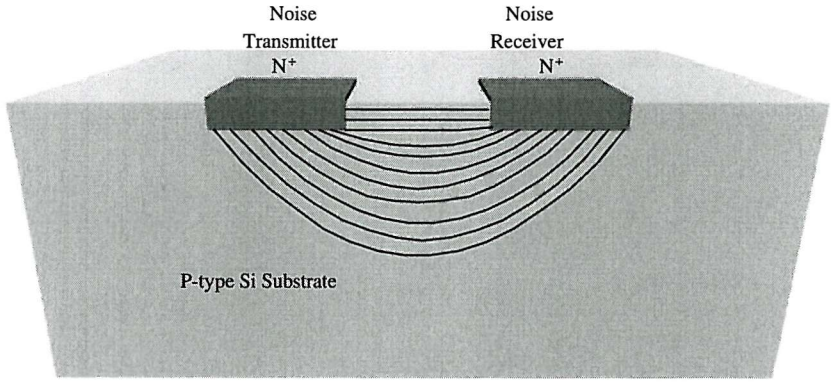


Figure 2.2: Bulk CMOS coupling path.

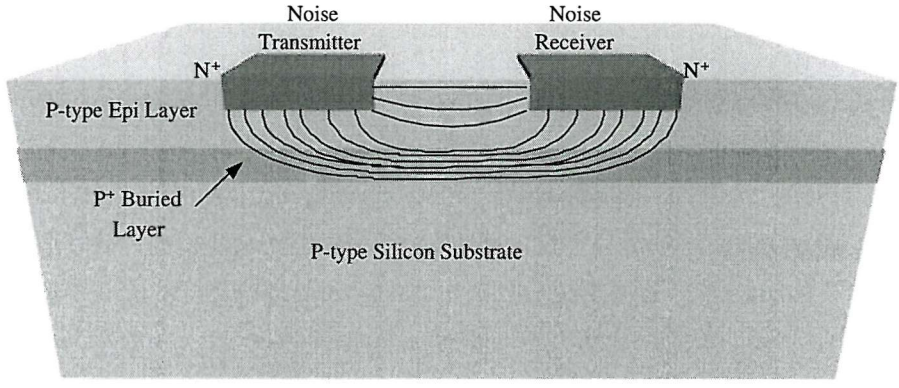


Figure 2.3: Heavily doped p^+ buried layer coupling path.

Recent bipolar and BiCMOS processes integrate transistors on a standard resistivity epitaxial silicon layer grown on the top of a heavily doped substrate [1]. The main reason for this is to reduce latch-up problems. The buried plane, however, acts as a collector and distributor of noise. The higher doping of the buried layer compared to the doping of the epitaxial layer results in a less resistive coupling path located in the buried layer (Figure 2.3). Alternatively, it can be viewed as a single node located under the noise transmitter and receiver. The current injected by the noise source flows almost directly down to the buried layer and is propagated to the entire chip. Physical separation of the noise transmitter and receiver does not affect drastically the isolation properties of such substrates [1], [11], [21].

Crosstalk studies have been carried out in thin-film SOI technology [1], [7], [8], [10]. The devices are built in a thin (80 nm) silicon film, which is located on top of a buried oxide that separates it from the silicon substrate. This structure allows easy

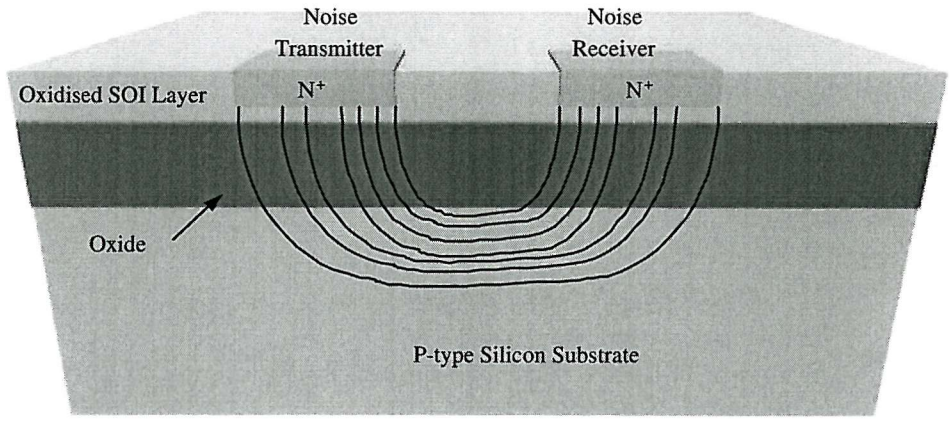


Figure 2.4: Thin film SOI coupling path [1].

integration of shallow junctions and complete elimination of the dc coupling between the noise transmitter and receiver. (Figure 2.4). Compared to the heavily doped buried layer technology mentioned previously, the coupling path is now shifted even further below the buried oxide. The coupling is now purely capacitive nature down to the substrate and is found to be proportional to the separation distance [1]. At higher frequencies the buried oxide gradually becomes "transparent", increasing the crosstalk. An advantage of the SOI substrates is the possibility of using a high resistivity handle wafer to improve crosstalk suppression while at the same time not influencing latch-up susceptibility. High resistivity bulk CMOS substrates present technological difficulties in processing that increase cost. It is difficult to retain the high resistivity nature (i.e. reduced doping) of the substrate because of the diffusion of small quantities of dopants.

2.4 Isolation Schemes

Guard rings have been investigated to determine their suitability to suppress crosstalk [1]-[10]. Guard rings are substrate contacts that completely surround a region [22]. They are essentially p^+ diffusions in a p-type substrate or n^+ diffusions in an n-type substrate. They are connected to a ground potential and provide isolation by "absorbing" the substrate potential fluctuations generated by the devices located adjacent to them. Guard rings are applicable to all the technologies mentioned above. Their efficiency, however, is strongly dependent on the technology itself. Bulk CMOS technologies can benefit from the use of guard rings because of the surface nature of crosstalk. In other technologies, where crosstalk is not a surface phenomenon, guard rings are not as efficient. Raskin et. al. [1] showed that in a thin film SOI substrate guard rings provide a significant improvement in isolation if they are combined with high resistivity substrates. At very high frequencies, where

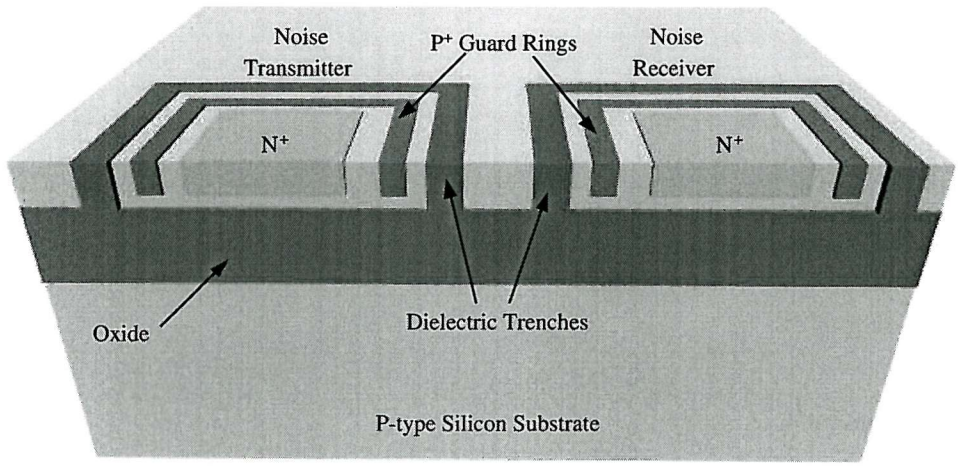


Figure 2.5: Combination of guard rings and dielectric trenches in a SOI substrate.

the buried oxide becomes transparent, guard rings have been shown to be the only crosstalk reduction scheme that can improve isolation in SOI substrates [7], [8], [10].

Dielectric trenches are another isolation scheme that can be implemented in bulk and SOI technologies. The trenches are usually filled with a dielectric or lined with a dielectric and filled with polysilicon. They surround the areas of interest and in SOI substrates they extend in depth all the way down to the buried oxide. Complete dc isolation can be achieved with this scheme. High frequency crosstalk however, cannot be suppressed by buried oxides and trenches. The coupling (oxide or junction) capacitances associated with them have negligibly small impedance that offers no isolation at all. Combinations of guard rings and trenches in various substrates can also exist for improved isolation and are only dependent on the extra processing costs required (Figure 2.5).

A detailed comparison of the aforementioned isolation schemes was carried out by Raskin et. al. [1]. Figure 2.6 depicts some the results of these studies. It can be observed that the use of any kind of isolation schemes provides considerable isolation improvement over none at all. Bulk silicon exhibited the highest crosstalk starting from frequencies below the GHz range. The degree of isolation is increased when guard rings are introduced. The best isolation is achieved by a combination of guard rings and high resistivity SOI substrates. The improvement however is seen only up to 10 GHz. This implies that at higher frequencies the only scheme that provides crosstalk suppression is the guard rings.

Other technologies make use of the principles of low crosstalk shown in high resisitivity SOI substrates. Silicon on Sapphire (SOS) or Silicon on Anything (SoA) both provide superior crosstalk suppression. However, they are not available for

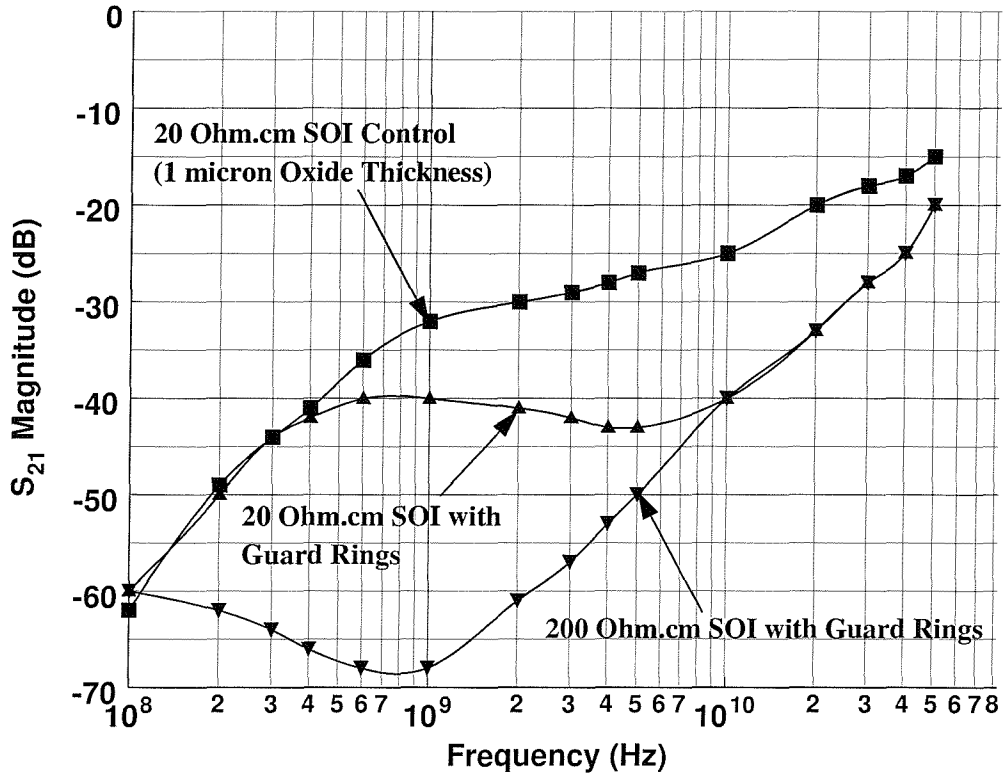


Figure 2.6: Comparison of high resistivity thin film SOI substrate with guard rings with standard resistivity SOI with guard rings and bulk. The oxide thickness is 0.4 μm for the SOI cases and 0.95 μm for the bulk case [1].

large-scale manufacture, although they have been around for a few years. Compatibility with existing processing and manufacturing practices is the key for a possible migration to new low crosstalk technologies. A post processing modification to an existing CMOS process that adds a ground plane below the devices and circuits by etching the backside of the wafer, has been proposed by [23], [24], [25].

The ground plane SOI (GPSOI) substrate that is discussed in this thesis exploits the same principle by incorporating a buried metallic plane in the SOI layer stack. The only modification to an existing SOI process is a ground connection from the top of the wafer down to the buried metallic plane.

2.5 Simulation and Modelling Tools

Substrate crosstalk simulation is an active area of research and depending on the test structures several simulators can be employed to provide an initial estimation of the coupling through the substrate. Semiconductor solvers have been used [1],[7] to investigate crosstalk in test structures that include active components as noise receivers and transmitters. Although they have been proven to be accurate for these cases, these solvers can not model magnetic effects that are present in other cases

like interconnect crosstalk or electromagnetic coupling between passive components (inductors). Electromagnetic solvers on the other hand model both electric and magnetic effects but they are not suitable for silicon device simulation. This work only considers test structures without silicon devices and investigates how electromagnetic solvers can be used to estimate substrate crosstalk in these test structures. Electromagnetic solvers are used to solve Maxwell's electromagnetic equations (Table 2.1) for planar structures embedded in a multilayered dielectric substrate. They are based on a numerical discretization technique called the Method of Moments. The planar metallisation patterns in the signal layers are meshed using rectangular and triangular cells. Each cell has unknown electric and magnetic current distributions, which are simulated by functions called basis functions. The amplitude of the basis functions is determined by boundary conditions. For example, the voltage drop across an ideal (zero thickness, infinite conductivity conductor) must be zero. This discretization process transforms the electromagnetic equations into an equivalent network model of self and mutual inductive and capacitive elements. In this network, the nodes correspond to the cells in the mesh and hold the cell charges. Each cell corresponds to a capacitor to ground. All nodes are connected with branches, which carry the current flowing through the edges of the cells. Each branch has an inductor representing the magnetic self-coupling of the associated current basis function. All capacitors and inductors in the network are complex, frequency dependent and mutually coupled, as all basis functions interact electrically and magnetically.

Reference	**Differential Form**	**Integral Form**
Gauss's Law	$\nabla \cdot D = \rho_v$	$\oint_S D \cdot ds = Q$
Faraday's Law	$\nabla \times E = -\frac{\partial B}{\partial t}$	$\oint_S E \cdot dl = -\int_S \frac{\partial B}{\partial t} \cdot ds$
Gauss's Law for Magnetism	$\nabla \cdot \mathrm{B} = 0$	$\oint_S B \cdot ds = 0$
Ampere's Law	$\nabla \times H = J + \frac{\partial D}{\partial t}$	$\oint_C H \cdot dl = \int_S \left(J + \frac{\partial D}{\partial t}\right) \cdot ds$

Table 2.1: Maxwell's Electromagnetic Equations

In order to simulate a circuit a substrate must be defined first. A substrate definition describes the medium where a circuit exists. An example is the substrate of a multilayer circuit board, which consists of layers of metal tracks, insulating material, ground planes, vias that connect tracks, and the air that surrounds the board. A substrate definition enables the user to specify properties such as the number of layers in the substrate, the dielectric constant, and the thickness of each layer of the circuit. A substrate definition is made up of substrate layers and metallization layers. Substrate layers define the dielectric media, ground planes, air or other

layered material. Metallization layers are the conductive layers in between the substrate layers. Once the substrate definition is complete, ports are assigned to the circuit and the solution process begins.

For the purposes of this work, two electromagnetic solvers have been used. These are *Momentum*, part of the Advanced Design System by Agilent Technologies [26] and *EM-Sight*, part of the Microwave Office software, provided by Applied Wave Research [27].

2.6 Conclusion

The substrate crosstalk figure of performance used throughout this thesis has been presented in this chapter. A comparison of current thin film SOI technology with bulk revealed the superiority of the former [1]. SOI substrates have a clear advantage over bulk silicon but suffer at high frequencies, when the buried oxide becomes "transparent". The use of dielectric trenches, guard rings and high resistivity handles enhances the isolation performance in different frequency ranges. Published studies [1], [7], [8] have shown that, in SOI substrates, the most efficient method of substrate crosstalk suppression at low frequencies is the addition of dielectric trenches, whereas high frequency crosstalk can be suppressed only by guard rings.

Chapter 3

Substrate Crosstalk Suppression with Buried Ground Planes

3.1 Introduction

Chapter 3 presents experimental results of test structures fabricated on a substrate with a buried ground plane. The substrate does not include the silicon layer of the GPSOI substrate, so that the effect of the ground plane to substrate crosstalk can be isolated from any other effects caused by the presence of additional silicon layers. The absence of ground contacts leaves the buried metallic plane of the GPSOI electrically floating and that case is investigated and compared to a substrate that does not have a ground plane at all.

3.2 Buried Ground Plane and GPSOI Substrates

The buried ground plane substrate contains a buried metallic layer, which is located between the silicon substrate and an oxide layer deposited above it. This substrate is part of the ground plane silicon on insulator (GPSOI) substrate. The buried ground plane substrate (or handle substrate) is bonded to a silicon substrate with a layer of oxide. Then the active substrate is polished down to the desired thickness and the GPSOI is formed. The GPSOI is manufactured by the Northern Ireland Semiconductor Research Centre (NISRC). This work has been a collaboration between the Department of Electrical and Electronic Engineering, Queens University of Belfast, Northern Ireland and The Department of electronics and Computer Science, University of Southampton, England. Similar technologies, which combine buried ground layers and silicon bonding techniques include the silicon-on-metal and silicon-on-silicide-on-insulator (SMI-SSOI) substrates. More information on the manufacturing aspect of these substrates can be obtained from [16], [17], [18], as they are beyond the scope of this work. The GPSOI substrates discussed in this work contain a tungsten silicide (WSi_2) buried metallic plane. Figures 3.1 and 3.2

show a cross-sectional view of the GPSOI substrates and a pictorial representation of the manufacturing process respectively. It must be noted that the thin polysilicon cap layer is assumed to be either part of the insulator (oxide) or the ground plane (tungsten silicide) depending on its doping and thickness.

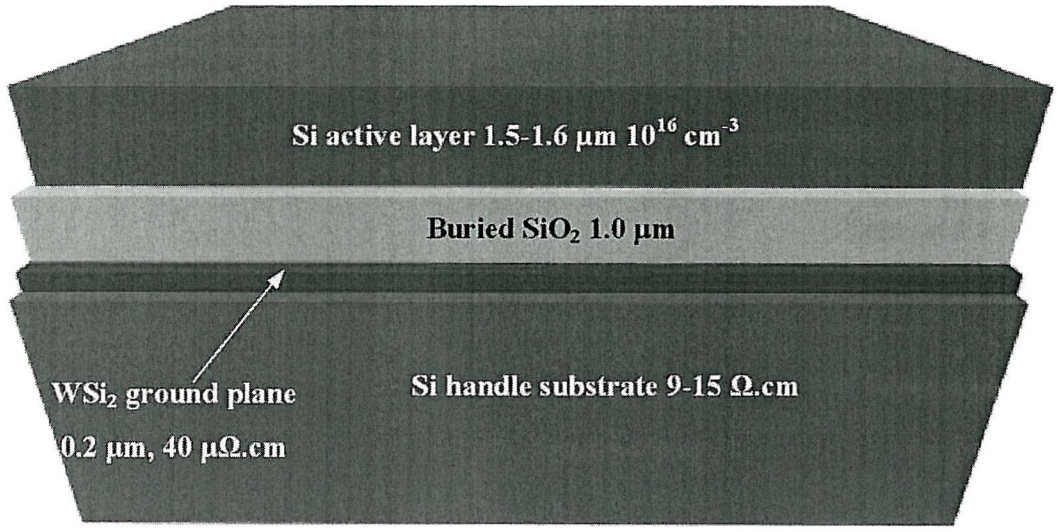


Figure 3.1: Cross-sectional view of the GPSOI substrate.

3.3 Substrate Crosstalk Test Structures and Experiments

The crosstalk suppression capability of the GPSOI substrate has been initially assessed on substrates without a silicon active layer. The purpose of these studies was twofold. Firstly, they provide an initial estimation of the isolation improvement when compared to bulk silicon substrates. Secondly, they can help towards the understanding and the modelling of the effects of buried ground planes without the extra complexity introduced by the silicon active layer. This kind of partitioning can be viewed in the context of a methodology for studying substrate effects. Such a methodology includes simplified representations of complex devices, such as transistors, that help de-embed the substrate coupling effects from additional complex effects introduced by the devices themselves. The behaviour of active or passive devices on substrates with buried ground planes such as the GPSOI, is not fully understood and constitutes a research field on its own.

Figure 3.3 shows the two substrates considered. The buried ground plane substrates will be referred to as the GPSOI for these initial studies. The term GPSOI is a misnomer at this stage since it does not include the active silicon layer and is therefore not a SOI substrate.

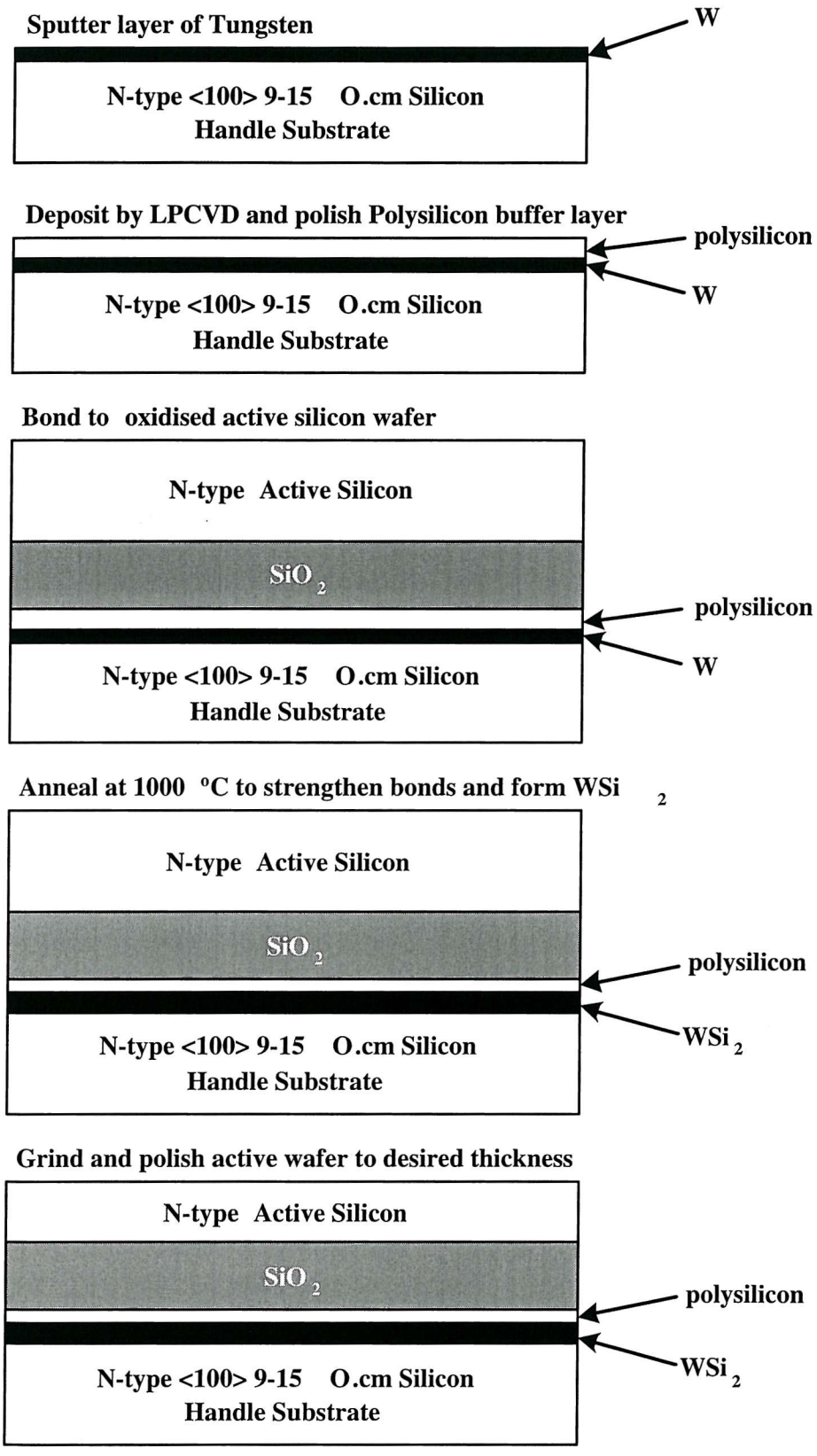


Figure 3.2: GPSOI substrate manufacturing process.

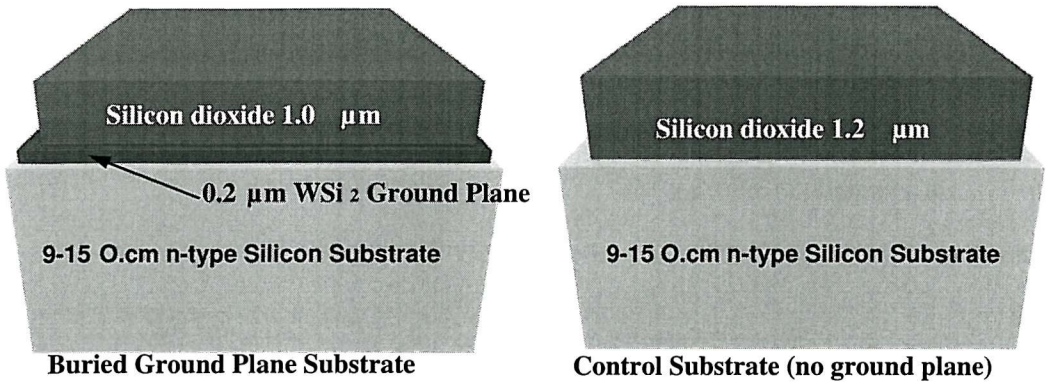


Figure 3.3: The two substrate configurations under investigation: GPSOI substrate (left), control SOI (right)

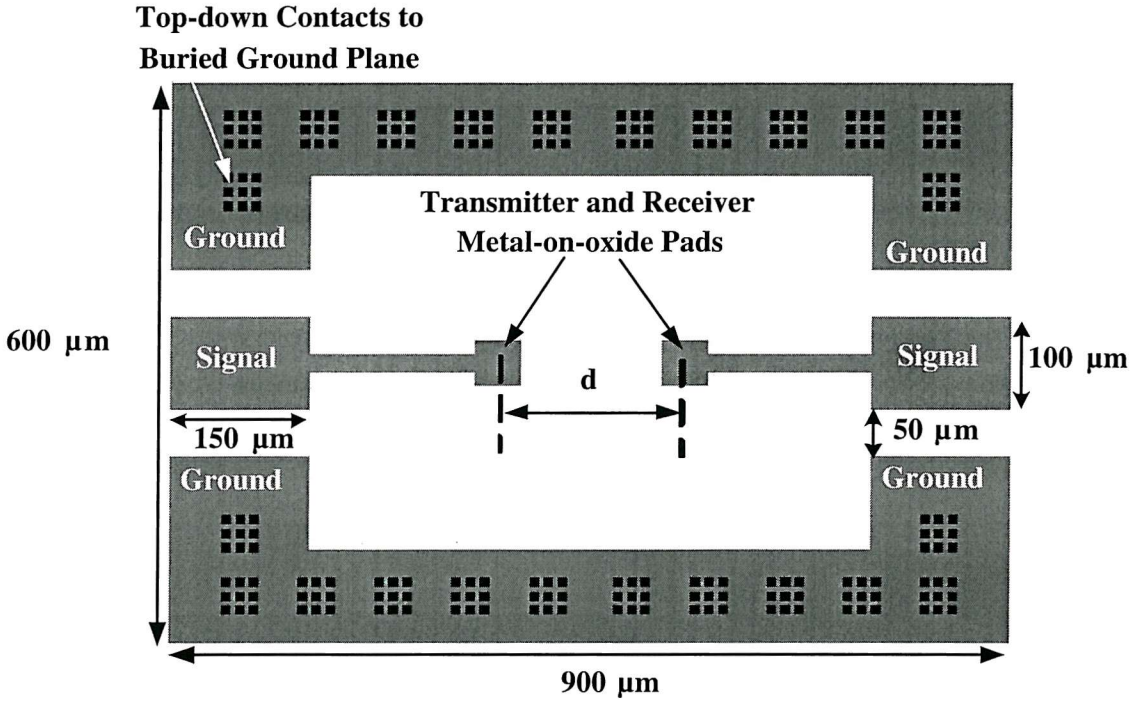


Figure 3.4: Plan view of the test structure for substrate crosstalk studies on ground plane substrates.

Figure 3.4 shows a plan view of the test structure that was designed for these studies. The crosstalk suppression capability of the substrate was assessed by measuring the magnitude of the forward transmission scattering parameter s_{21} between the two square metal pads at the centre of the structure. The separation of the metal pads was varied from 75 μm to 200 μm. The two square pads were embedded in the coplanar wave-guide (CPW) ground-signal-ground (GSG) structure shown in Figure 3.4. The dimensions of the transmitter and receiver metal pads was chosen to be 50μm x 50μm in agreement with test structures from previously published

studies [1] and in order to facilitate comparison with previously published results. The dimensions of the CPW structure were in large degree dictated by the measuring equipment. The spacing between the ground and signal pads on each port was the recommended one by the manufacturer of the measurement probes. The lateral spacing between the probing pads of the two ports was approximately 750 μm. The probe pads were placed as far apart as possible to minimize noise and crosstalk between the probes.

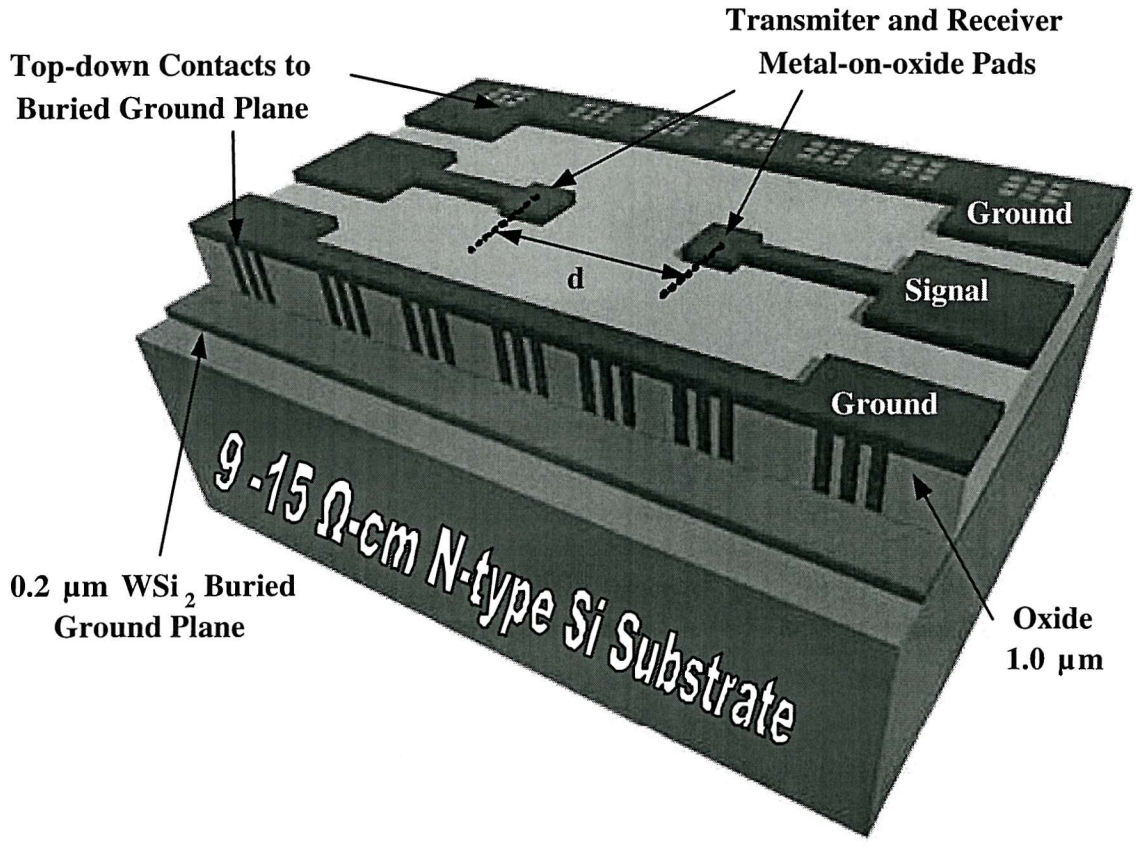


Figure 3.5: The CPW crosstalk test structure with a grounded buried WSi_2 plane (Grounded GPSOI).

The GPSOI substrate allows two configurations to be studied, depending on whether the buried WSi_2 plane is connected to ground or left electrically floating. Both configurations were studied. In the first configuration the buried ground plane was contacted from the top by metallised vias and was locally connected to the coplanar RF ground pads on the surface. This configuration will be referred to as the "grounded GPSOI" from now on. The test structure for the grounded GPSOI is identical to that of Figure 3.4. When the top-down contacts to the WSi_2 plane are absent, then the buried ground plane is floating electrically. This configuration will be referred to as the "floating GPSOI". The third and final substrate that was

considered did not include a buried ground plane. It was the "control" configuration and represented conventional SOI substrates.

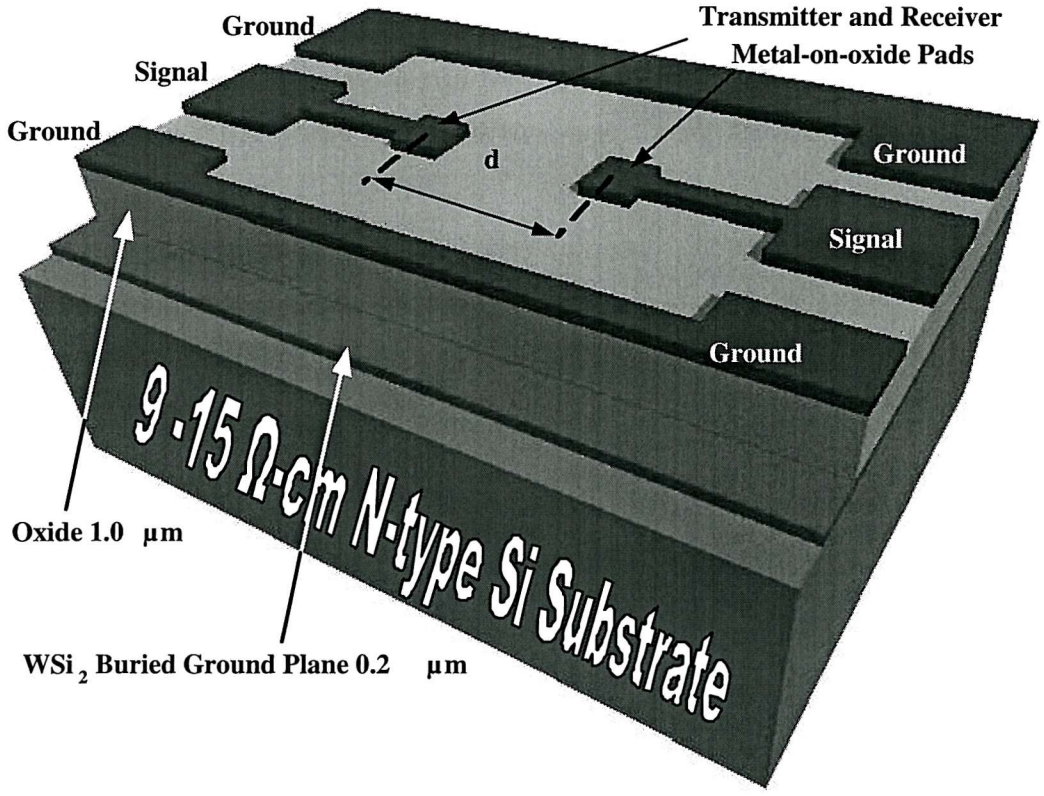


Figure 3.6: The CPW crosstalk test structure with a floating buried WSi_2 plane (Floating GPSOI).

The oxide thickness in the GPSOI substrates was 1.0 μm and the WSi_2 layer thickness 0.2 μm. The resistivity of the WSi_2 layer, as measured by the substrate manufacturer, was 40 $\mu\Omega$.cm and corresponds to a sheet resistance of 2 Ω per square. In the case of the control substrates the oxide thickness was 1.2 μm, equivalent to the combined thickness of the oxide and WSi_2 layers of the GPSOI. The silicon substrate resistivity was 9-15 Ω.cm for all substrates. Figures 3.5 to 3.7 show combined plan and cross-sectional views of the test structures and the corresponding substrate configurations. The test structures were fabricated at Southampton University's Microelectronics Centre and a full listing of the fabrication process is given in Appendix B. The process listing does not include the fabrication of the GPSOI substrates themselves.

3.4 Measurement Considerations

The scattering parameters were measured using a HP 85109C on-wafer characterisation system. The 85109C was calibrated with the Load- Reflect-Reflect-Match (LRRM) standard in the frequency range of 500 MHz to 50 GHz. 150 μm pitch

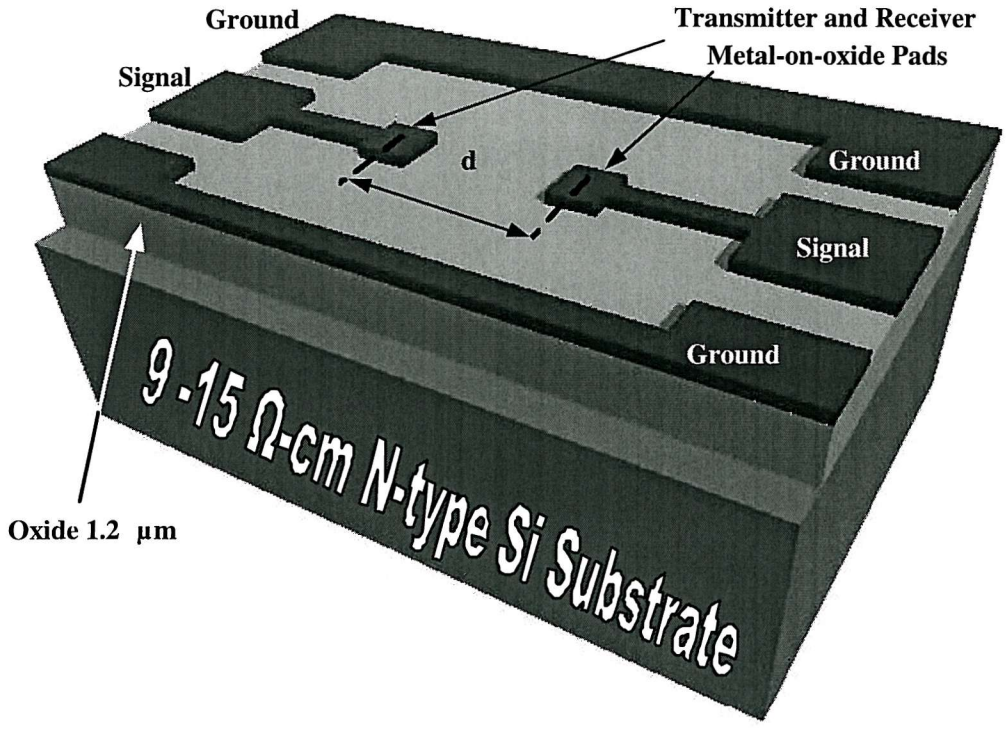


Figure 3.7: The CPW crosstalk test structure without a buried WSi_2 plane (Control SOI).

Cascade Microtech air coplanar (ACP) probes with tungsten tips were also used. The dynamic range of the instrument was enhanced by enabling the averaging feature for 256 points. With this feature activated, the s-parameters are measured 256 times at each frequency and the average value for each point is recorded. In addition, several test structures at different die locations were measured to ensure repeatability and reliability of the measurements. In order to maintain consistency and repeatability over a large number of measurements, care was taken to keep the measurement conditions constant and as close to the calibration conditions as possible. This involved maintaining a constant amount of mechanical pressure to the probes for each measurement. The amount of pressure that is applied to the probes is critical. Too little pressure can result in poor contact between the probes and the device under test. Increased pressure, however, can compromise the calibration because of the additional applied mechanical strain. Application of less than adequate pressure poses a potential threat to the reliability of the measurement. The measurement data may correspond in this case to crosstalk between the probes rather than the device under test. For the measurements presented in this work however, this case could be identified because the measured value of the forward transmission coefficient s_{21} is lower in the case of the device under test (DUT) than in the case of the two probes not contacting the DUT and effectively floating in the air above it.

Nevertheless, the applied pressure was in agreement with the probe manufacturer's specification and was kept constant during the course of all measurements.

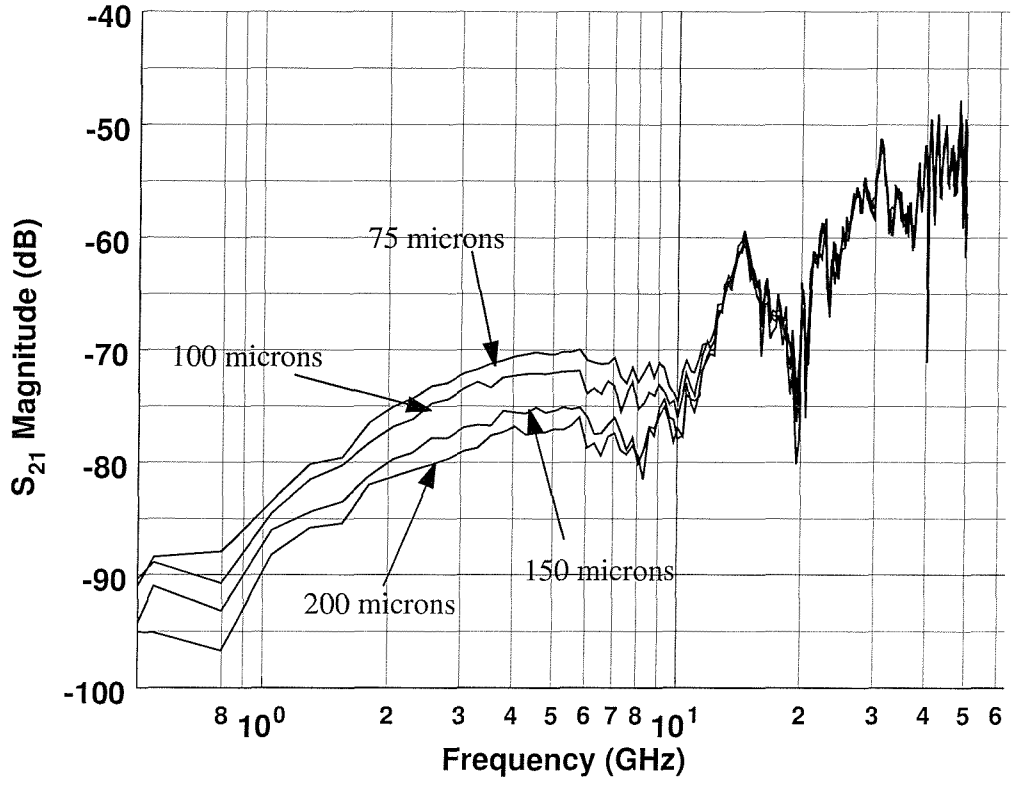


Figure 3.8: Measurements of the magnitude of s_{21} from test structures with a grounded buried WSi_2 plane for 75, 100, 150 and 200 μm Tx/Rx pad separations.

3.5 Measurement Results

S_{21} magnitude transmission versus frequency plots from 500 MHz to 50 GHz for the three substrate configurations are shown in Figures 3.8 to 3.10. Figure 3.8 shows isolation measurements for the grounded GPSOI substrate. The separation distance between the receiver and transmitter pads varied from 75 μm to 200 μm. The grounded GPSOI substrate test structures achieve a high degree of isolation ranging from 90 dB at 500 MHz to 50 dB at 50 GHz. Increasing the pad separation from 75 μm to 200 μm offered a 10 dB improvement but only up to 10 GHz. Crosstalk isolation was observed to increase by approximately 2 dB per 50 μm of pad separation below 10 GHz. Above this frequency, the four traces in Figure 3.8 converge to one pattern, shown that isolation is not affected by the separation distance.

Measured data for the control SOI wafers are shown in Figure 3.9. No buried ground plane existed on these substrates. Isolation ranges from -35 to -20 dB over the aforementioned frequency range. Low frequency crosstalk is constant with

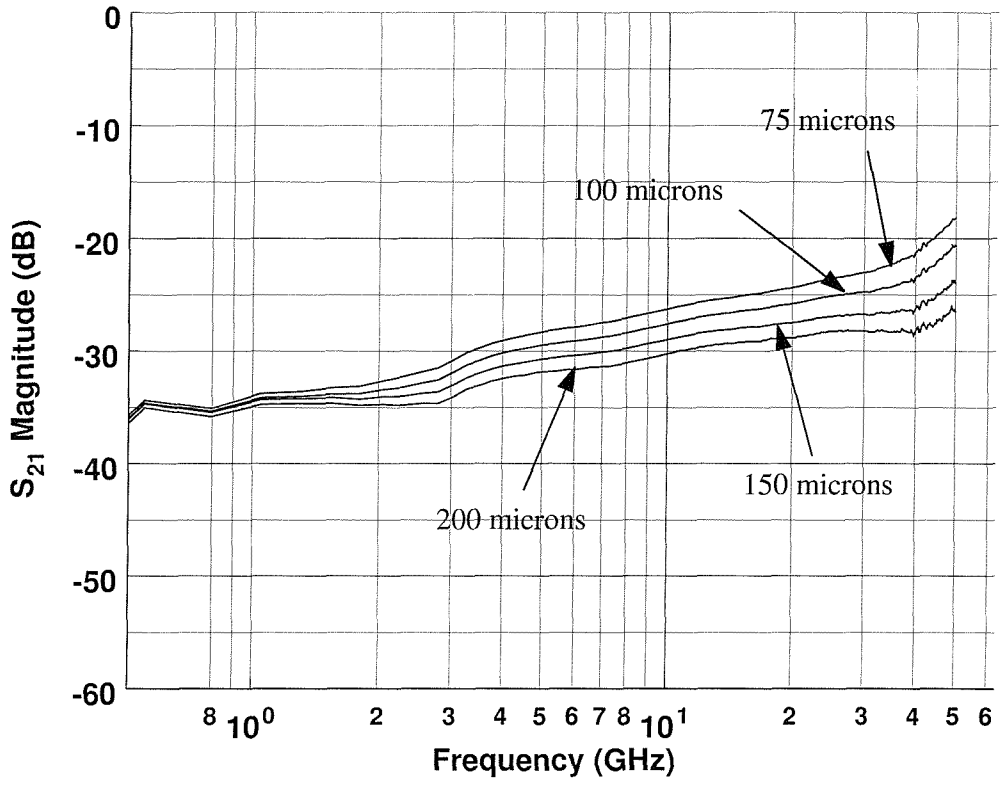


Figure 3.9: Measurements of the magnitude of s_{21} from test structures without a buried WSi_2 plane (control SOI) for 75, 100, 150 and 200 μm Tx/Rx pad separations.

variable pad spacing and increases slightly with decreasing separation for higher frequencies, above 1 GHz.

Measurements for the third substrate configuration, the floating GPSOI substrate, are shown in Figure 3.10, where the buried plane is left to float electrically. This substrate exhibited a poor isolation performance compared to the other two substrates. It can be observed that there is virtually no variation of s_{21} as the separation distance changes.

A comparison of the isolation performance of the three substrates is shown in Figure 3.11. The grounded GPSOI substrate clearly offers the highest crosstalk suppression. The existence of a buried WSi_2 plane, however, dictates the requirement of a grounding solution, which in this case, was achieved by using top down contacts to connect the WSi_2 plane to the surface RF ground. If the buried plane, under any circumstances, is left to float electrically, crosstalk is increased dramatically. The substrate loses its crosstalk suppression ability and becomes worse than the control SOI.

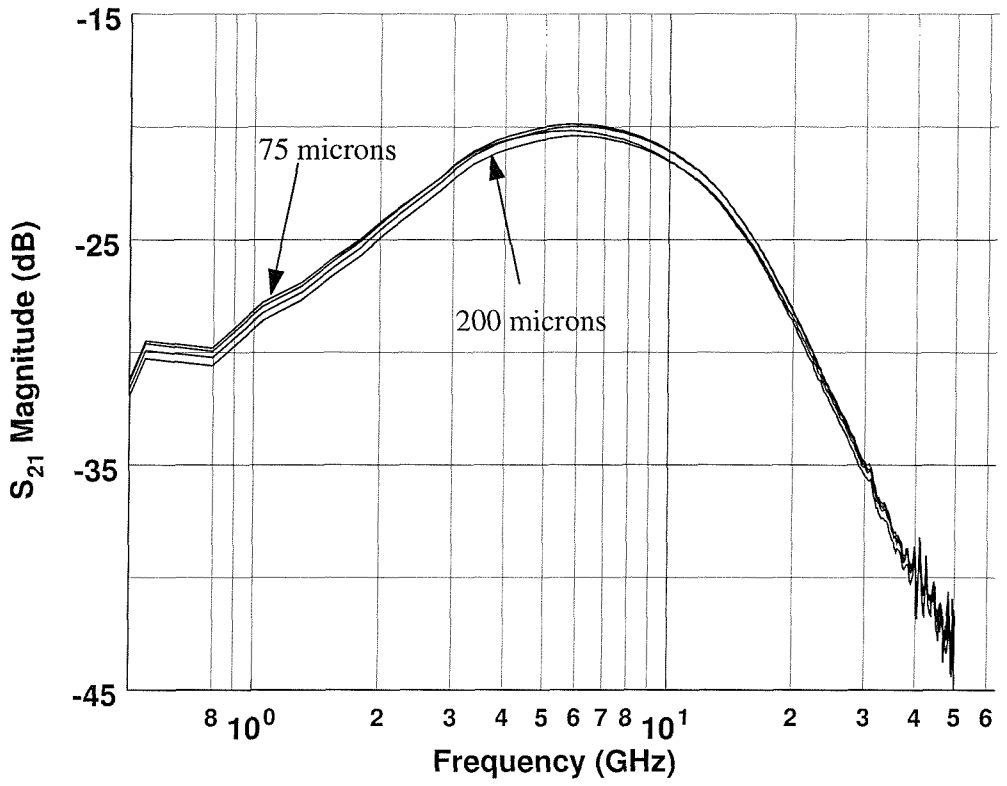


Figure 3.10: Measurements of the magnitude of s_{21} from test structures without an electrically floating WSi_2 plane for 75, 100, 150 and 200 μm Tx/Rx pad separations.

3.6 Discussion

Figure 3.12 compares the noise suppression capability of the GPSOI substrate with other published data by [1] that used the same s_{21} characterisation technique. The pad separation for the data in Figure 3.12 is 100 μm. Measurement reliability is confirmed by the fact that the control substrate results agree reasonably well with previously published measurements. Raskin et. al [1] also fabricated structures with metal pads directly on oxide and without any Si active layer. The oxide thickness, however, for these structures was 0.95 μm, whereas the control wafers for this work had an oxide thickness of 1.2 μm. Another difference in the two experiments is the substrate resistivity being 9-15 Ω.cm for this work and 20 Ω.cm for the studies by Raskin et. al [1]. These variations in the experiments conditions for the two studies can account for the slight mismatch of the two SOI control data in Figure 3.12. The standard and high resistivity SOI with guard rings data of Figure 3.11 are from structures with diodes as receiver and transmitters. The diodes were $50\mu m \times 50\mu m$ and fabricated on a thin film (80 nm) active silicon layer.

The locally grounded GPSOI results shown in Figure 3.12 appear to exhibit the greatest degree of substrate crosstalk suppression reported to date. Figure 3.12 shows that the isolation improvement is approximately 20 dB compared to the high

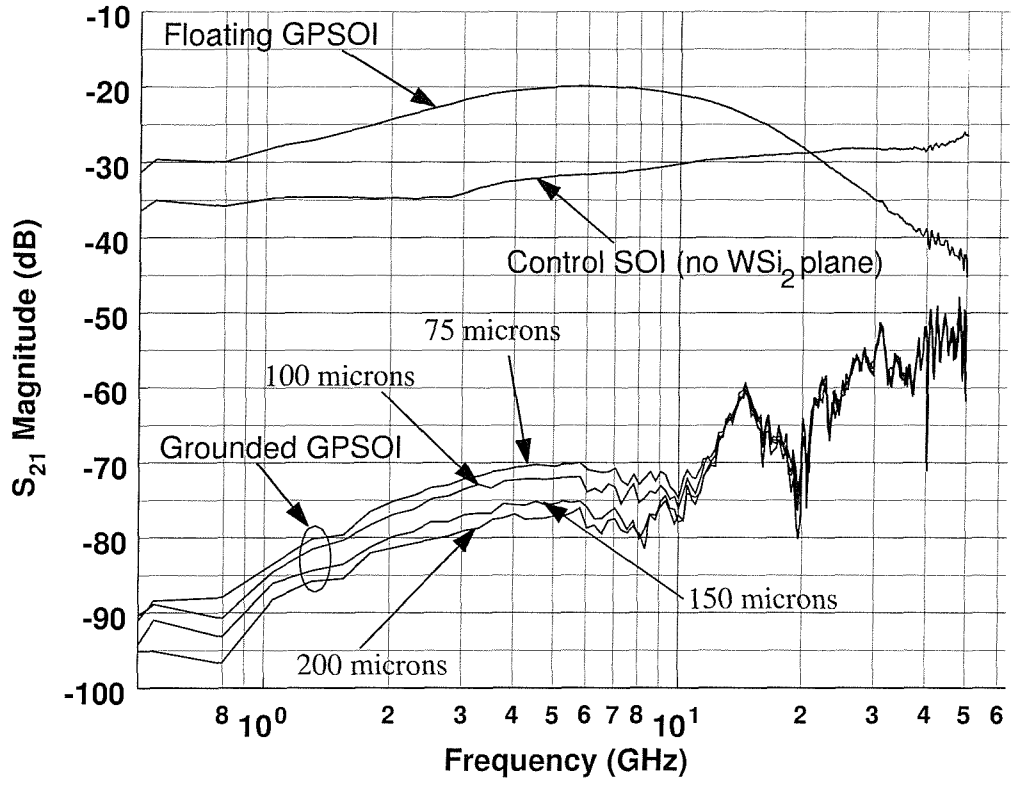


Figure 3.11: Comparison of the GPSOI (grounded and floating) with the control SOI measurements.

resistivity SOI substrate researched by [1]. An interesting finding from Figure 3.12 is the fact that the crosstalk of the structures with the guard rings is the same above 10 GHz. This is an indication that guard rings are the only effective noise suppression scheme at these frequencies. The locally grounded GPSOI parallels the 200 Ω.cm with guard rings over the entire frequency range. The frequency response of the GPSOI substrate at the entire frequency range has a slope of 20 dB per decade, which indicates a single pole response.

As previously mentioned, increasing pad separation improves isolation with a rate of 2 dB per 50 μm. It is generally important for a crosstalk suppression strategy to exhibit increased crosstalk isolation with increased separation so that the circuit designer can use separation as a design strategy in meeting crosstalk immunity specifications. The high resistivity SOI substrate studies by [1] have also exhibited this kind of behaviour with approximately the same rate of isolation improvement.

3.7 Conclusion

Test structures fabricated on a buried ground plane substrate were described in this chapter. Three substrate configurations were considered and their crosstalk suppression performance was measured. These substrate configurations were a grounded

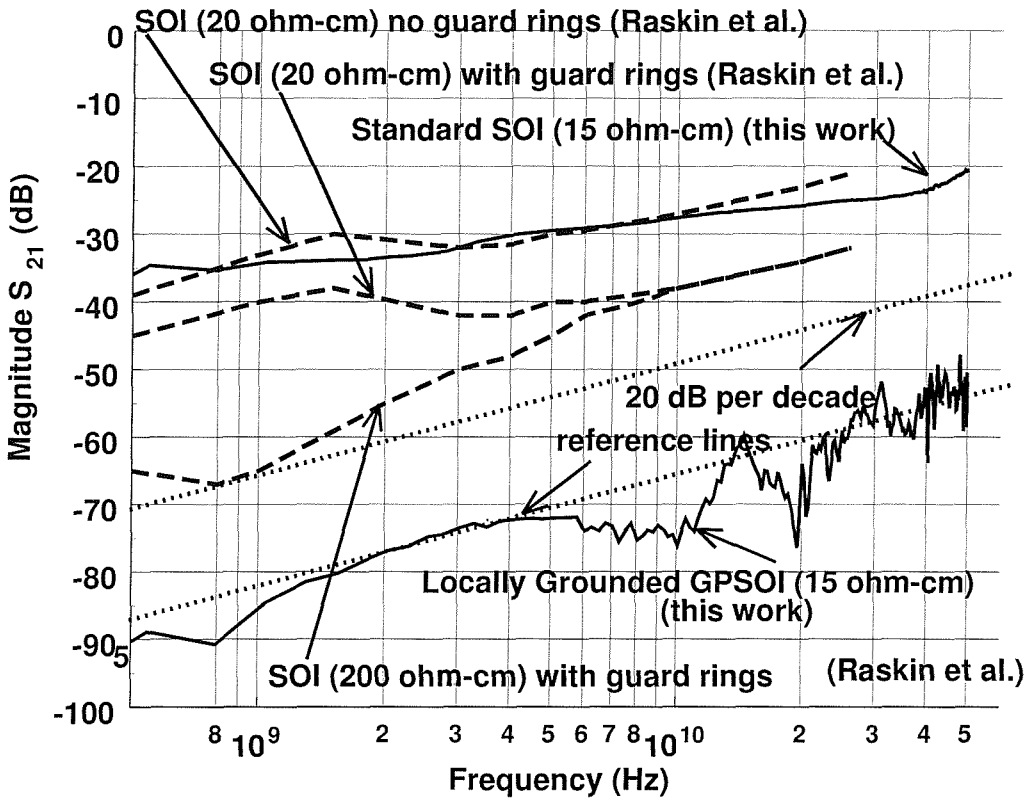


Figure 3.12: Measurements of the magnitude of the s_{21} transmission parameter for the locally grounded cross-talk structure on GPSOI and the standard SOI. Results from previous work on low and high resistivity substrate SOI with and without guard rings [1] are shown for comparison [2].

buried plane (grounded GPSOI), a floating buried plane (floating GPSOI) and a substrate without a buried plane at all (control SOI). The grounded GPSOI substrate exhibited the highest degree of isolation of the three configurations. On the other hand, the lowest degree of isolation was observed on the floating GPSOI. A comparison with published data from a high resistivity (200 Ω.cm) thin film SOI substrate revealed approximately a 20 dB improvement in isolation for the locally grounded GPSOI. The improvement was constant over the whole frequency range (500 MHz - 50 GHz). A very good agreement between the measurements, the simulations and published data [1] of the standard SOI substrate was also observed. The existence of a buried plane connected to ground yields in the best isolation figure a SOI substrate has ever achieved. The locally grounded GPSOI combines the high isolation capabilities of high resistivity SOI with the reduced manufacturing costs of a low-resistivity SOI substrate making it an attractive alternative for high frequency integration of mixed signal IC's. The conclusion drawn from these preliminary studies provide the corner stone of further studies on GPSOI substrates that are presented in the following chapters.

Chapter 4

Modelling Substrate Crosstalk on GPSOI Substrates

4.1 Introduction

Electromagnetic and lumped element modelling of the crosstalk effects in the GPSOI structures presented in the previous chapter are discussed here. Simulation results from two electromagnetic solvers are compared with the measurements showing good agreement between them. A compact lumped element model is then presented and analysed. Coupled microstrip line theory is employed in order to analyse the capacitance elements of the model.

4.2 Electromagnetic Modelling

The development of simulation tools that accurately model substrate crosstalk is an active area of research in itself [19], [13], [14], [28]. For the purpose of this work, two widely available commercial electromagnetic simulators were used. As mentioned earlier, both of them are used to simulate planar structures embedded in a multilayer dielectric substrate. The simulators used for these experiments were *Momentum*, part of the Advanced Design System suite, and *EM-Sight*, part of the Microwave Office suite [29], [27]. The substrate definition used for the simulation is shown in Table 4.1. The entire test structure design was imported to the simulator and simulations of the three configurations were carried out. Results from these simulations are shown in Figures 4.3 to 4.6 and are compared with measurements. In the case of the locally grounded GPSOI substrate both simulators succeed in capturing the dynamic behaviour of s_{21} up to the frequency of 10 GHz. Beyond that frequency all measurement traces converge to a single irregular pattern that in not modelled by either of the simulators. This is an indication that higher frequencies may be dominated by noise between the coplanar probes of the measurement

Substrate Layer Name	Thickness (μm)	Conductivity (S/m)	Permittivity
Si	525/100[1]	8.33	11.8
WSi_2	0.2	$2.5 \cdot 10^6$	11.8
Oxide	1	0	3.85
Via	1	Infinite	N/A
Al	1	$38.16 \cdot 10^6$	N/A

Table 4.1: Substrate definition used for the electromagnetic simulations with ADS Momentum and *EM-Sight*.

equipment. According to simulations s_{21} has a tendency to decrease at higher frequencies after peaking at about 5-6 GHz. Given the fact that the dynamic range of the equipment reduces with frequency, the pattern above the frequency of 10 GHz could be attributable to crosstalk between the probes themselves through the air above the substrate. The spacing between the probes remains constant for all transmitter/receiver (Tx/Rx) pad spacing, resulting in convergence of s_{21}. The control SOI and the floating GPSOI substrate simulations were also in good agreement with the measurements.

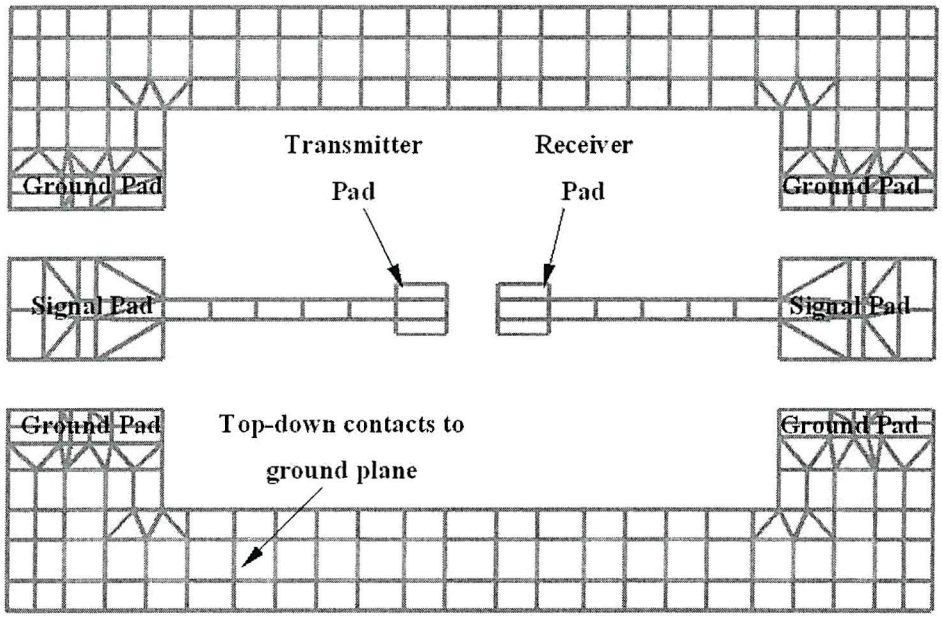


Figure 4.1: Grounded GPSOI test structure after meshing by ADS Momentum.

4.3 A Lumped Element Model for GPSOI crosstalk

Although numerical simulations allow a more detailed computation of substrate crosstalk, they are slow and require vast amounts of computing resources making simulation at circuit level a very time consuming task. Substrate crosstalk effects must be integrated into the design process, to allow a circuit designer to include these effects easily. Developing circuit practices that minimise substrate crosstalk

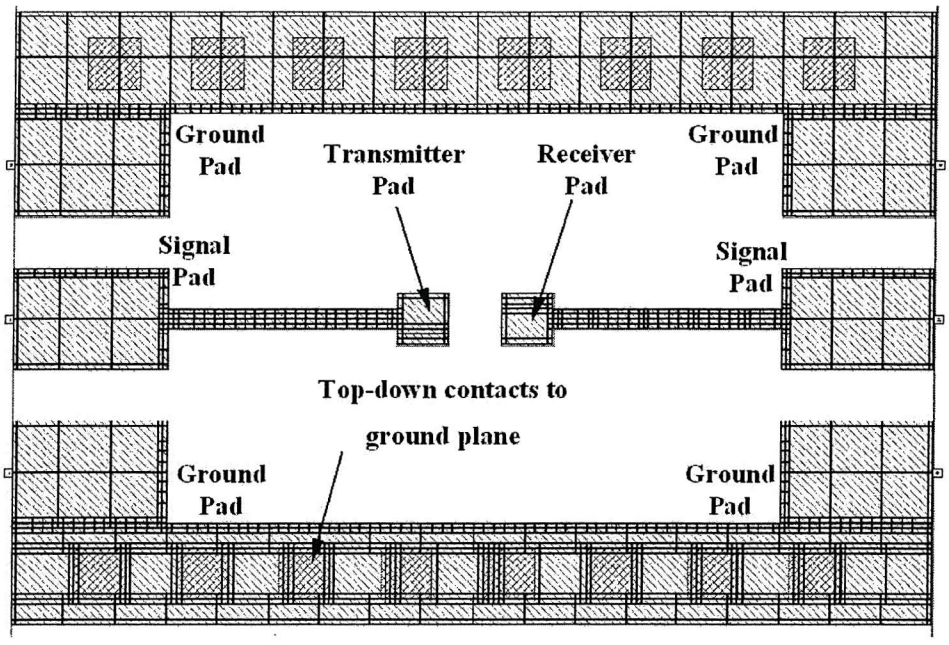


Figure 4.2: Grounded GPSOI test structure after meshing by *EM-Sight.*

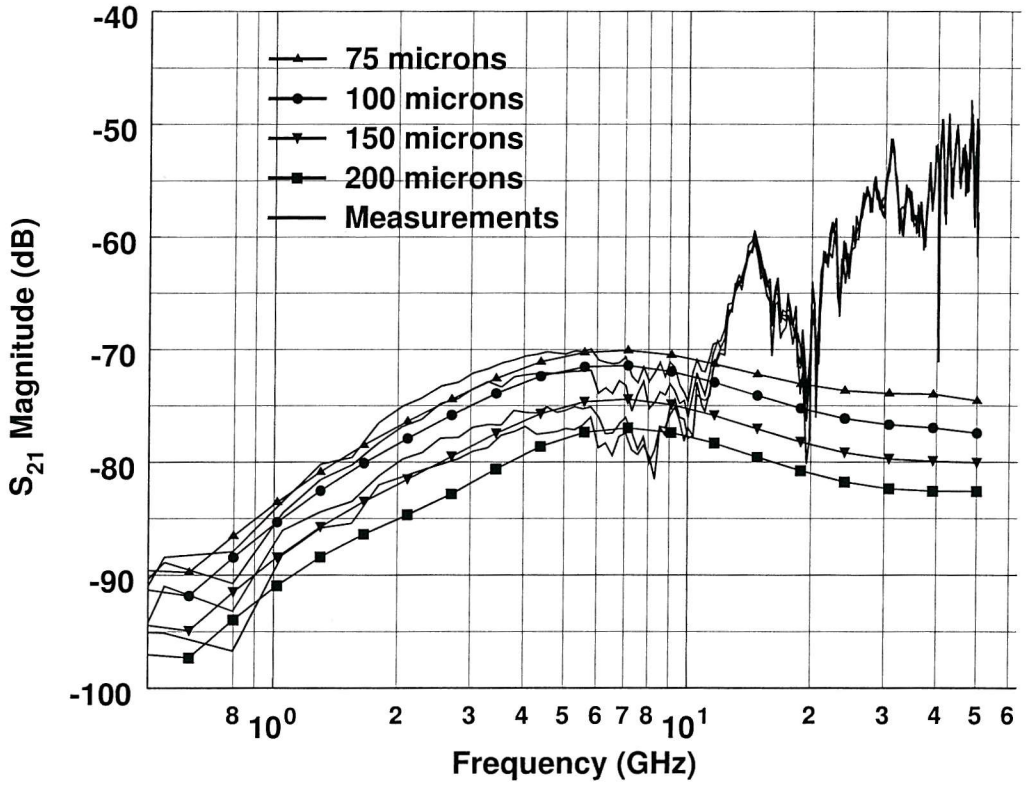


Figure 4.3: Numerical Simulation Data from ADS *Momentum* of the grounded GPSOI test structures for different separation distances in comparison to measurements.

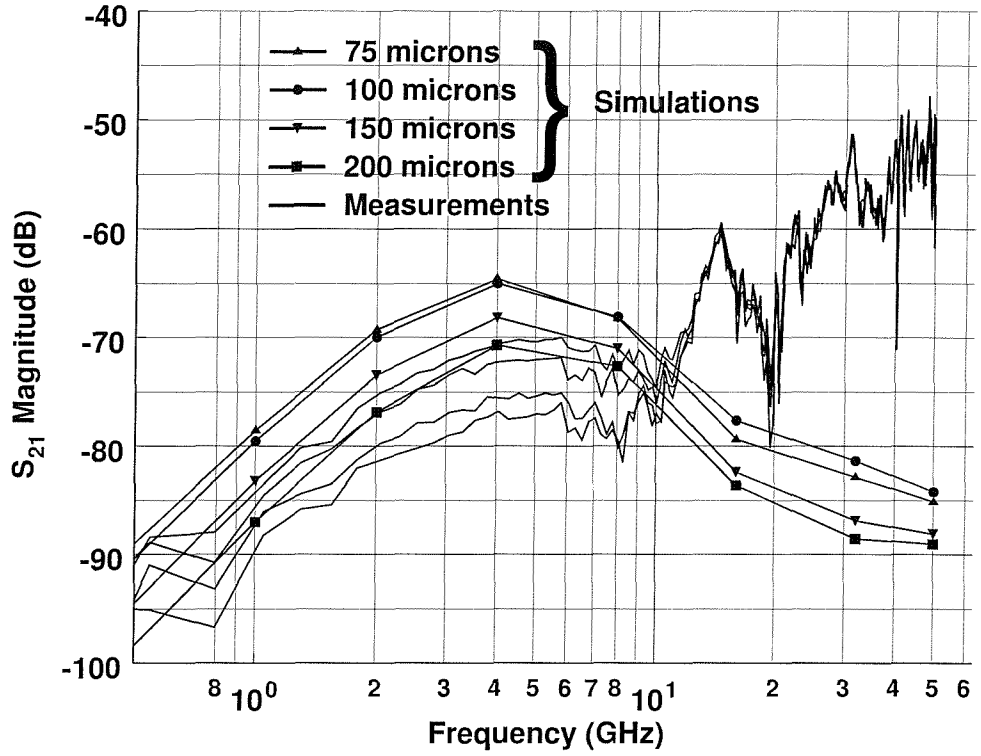


Figure 4.4: Numerical simulation data from *EM-Sight* of the grounded GPSOI test structures for different separation distances in comparison to measurements.

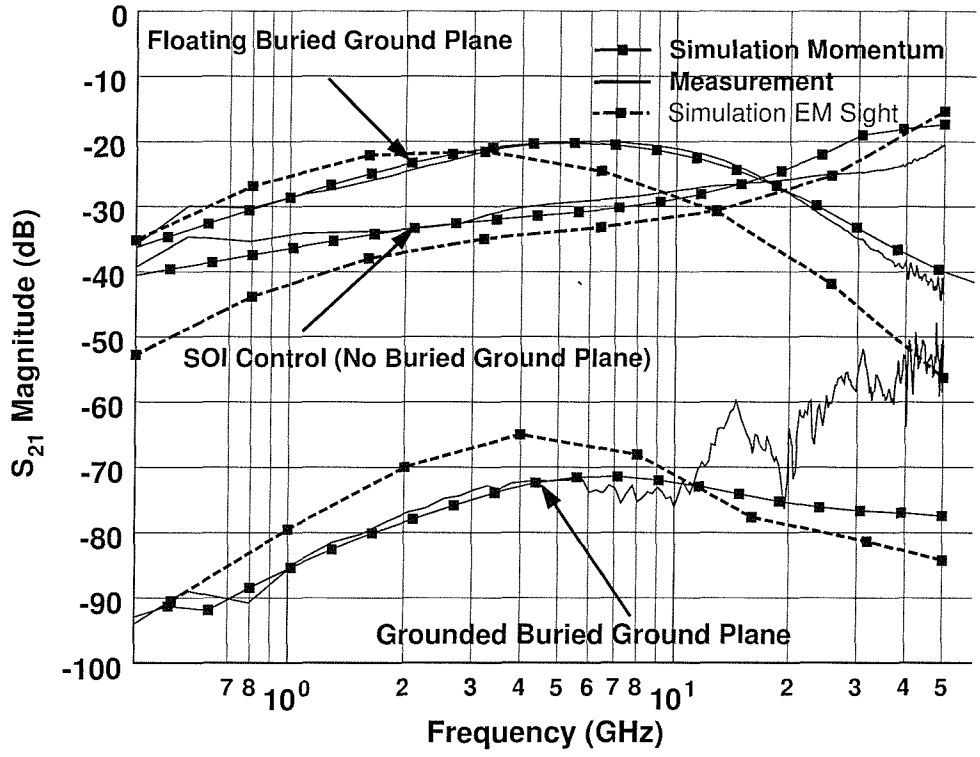


Figure 4.5: Comparison of measurement and simulation data for the locally grounded, electrically floating GPSOI and control SOI. Tx/Rx pad separation distance is 100 μm.

requires fundamental changes to long-established methodologies. Integration of these parasitic effects into the design practice, allows the designers to estimate the performance before fabrication. Furthermore, certain substrate crosstalk properties can be exploited as design practices by the designers at pre-fabrication circuit simulation level. For instance, the effect of separation distance to isolation can be used in order to achieve the desired isolation specification. At the same time such a model allows for a deeper physical understanding of the crosstalk mechanisms and the schemes that could be developed to reduce them.

4.3.1 A Thin Film SOI Crosstalk Model

A compact lumped element model for SOI crosstalk has been presented by [1] and is shown in Figure 4.6. It describes the substrate crosstalk between two square rectangular pads (Tx/Rx pads), with a width of W μm, separated by a distance of d μm. The two pads lie on oxide of H μm thickness. The substrate underneath the oxide is assumed to be much thicker than H.

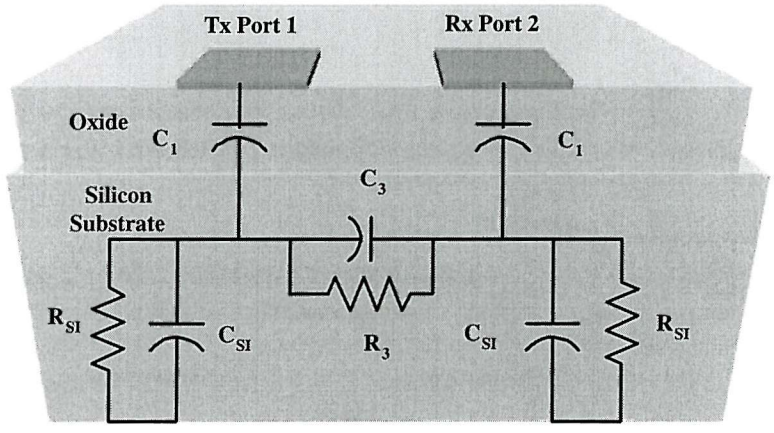


Figure 4.6: Lumped element equivalent model describing the crosstalk effects between two devices realized on the control SOI substrate [1].

Each model element is associated with the substrate and test structure parameters. The capacitor C_1 represents the capacitance through the oxide and can be calculated by a simple parallel plate formula:

$$C_1 = \varepsilon_0 \varepsilon_r \frac{S}{H} \tag{4.1}$$

where S is the area of each Tx/Rx pad and H is the oxide thickness. R_3 and C_3 represent the lateral coupling between the Tx and Rx pads, through the air, oxide and, more importantly, the silicon substrate. R_{SI} and C_{SI} model the substrate's resistive and capacitive properties with respect to its backside. R_3, C_3, R_{SI}, C_{SI} can be calculated by formulae provided by [1]. It can be observed from Figure 4.6

that the dominant path of crosstalk is located underneath the oxide at the surface of the resistive silicon substrate. This path is both capacitive and resistive.

4.3.2 A Crosstalk Model in GPSOI Substrates

The addition of a ground plane at the SiO_2-Si interface modifies the lumped model shown in Figure 4.6 to that of Figure 4.7. The ground plane's finite resistivity is modelled by the resistors R_1 and R_2 that are now introduced to the model. R_1 represents the resistance between the node underneath each pad and the actual surface RF ground connection. The resistance between the Tx and Rx pad nodes on the ground plane is modelled by R_2. In addition to these components another capacitor C_2 is also included in the model. C_2 models the lateral coupling between the Tx and Rx pads through the air and the oxide. It is this capacitance that is responsible for the observed 20 dB per decade slope in the s_{21} versus frequency measurements discussed in the previous chapter. The introduction of the ground plane causes C_{SI} and R_{SI} to appear in parallel with R_1 and R_2. The values of R_1 and R_2 are small compared to R_{SI} because of the lower resistivity of the WSi_2 plane (40 $\mu\Omega$-cm) compared to that of the silicon substrate (9-15 Ω-cm). Because the backside of the substrate was kept floating R_{SI} appears in parallel with R_2, hence the whole R_{SI}-C_{SI} network may be omitted from the model. Finally, $C_{PROBEPAD}$ represents the additional capacitance in parallel with C_1 introduced by the coplanar probe pads.

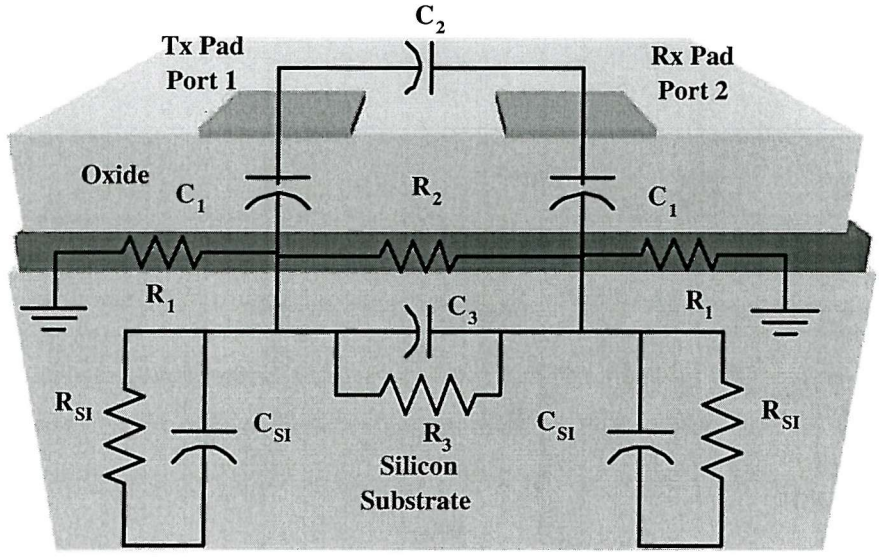


Figure 4.7: Lumped element crosstalk model of the grounded GPSOI test structure.

Numerical optimisation has been used to estimate the values of the model elements. A first order estimation of the values was made using formulae from the layout dimensions of the structure. C_1 and C_2 were calculated from the simple parallel plate

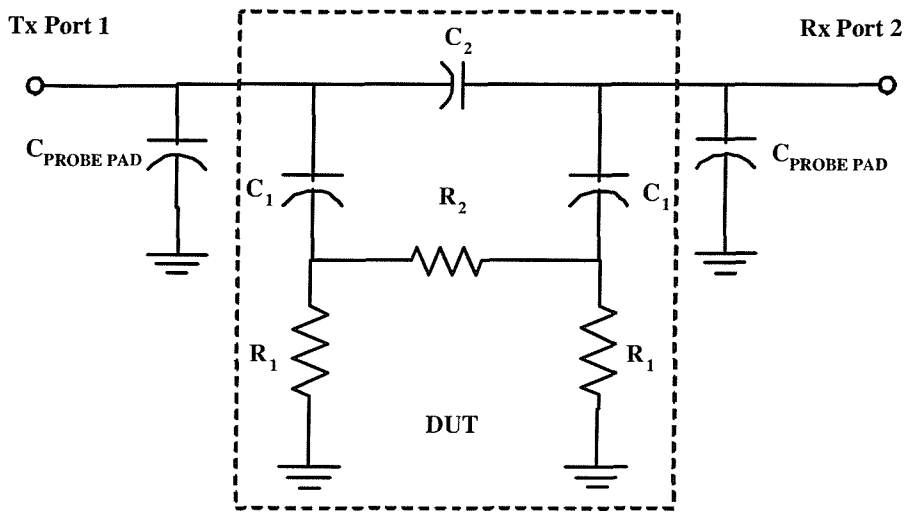


Figure 4.8: Simplified equivalent crosstalk model of the grounded GPSOI.

d (μm)	75	100	150	200
C_1 (pF)	0.09	0.09	0.09	0.09
C_2 (fF)	0.112	0.093	0.064	0.046
R_1 (Ω)	0.5	0.4	0.4	0.4
R_2 (Ω)	2.2	2.2	2.8	3.4

Table 4.2: Lumped element model parameters of the simplified grounded GPSOI model as described in Figure 4.8

formula and the resistors R_1 and R_2 were approximated from the sheet resistance of the ground plane (2 Ω per square). The model was then fine-tuned by a numerical optimiser to fit the measurements. The tuning was performed on the values of R_1, R_2 and C_2, which model highly distributed quantities. The three-dimensional nature of the test structure and therefore the measured crosstalk does not allow simple equations to be used to predict the values of these components. The capacitive components of the model have fringing electric fields that are not accounted for by simple parallel plate formulae equations. Although, as will be shown, C_1 can be approximated by a parallel plate capacitor, this is not true for C_2, because the spacing between the Tx/Rx pads and their lateral area dimensions are comparable to each other. The dielectric medium of this capacitance is also inhomogeneous (air-oxide) and a ground plane is located very close to it as well. Similarly, R_1 and R_2 are highly distributed elements, especially at higher frequencies, as they attempt to model the finite resistance of an infinitely large ground plane. These points highlight the difficulty in capturing the behaviour of distributed physical quantities, such as the electric field between the receiver and transmitter, in a single lumped component, which may be described by a single, simple equation.

The values of the model elements for each of the grounded GPSOI structures after the numerical optimisation are shown in Table 4.2. Figure 4.9 shows a comparison of the lumped model with he measurements and the electromagnetic simulations. Reasonable agreement is observed with the EM simulations for the whole frequency range but only up to 10 GHz for the measurements. Higher frequencies are dominated by noise between the probes, as it will be discussed in the following sections.

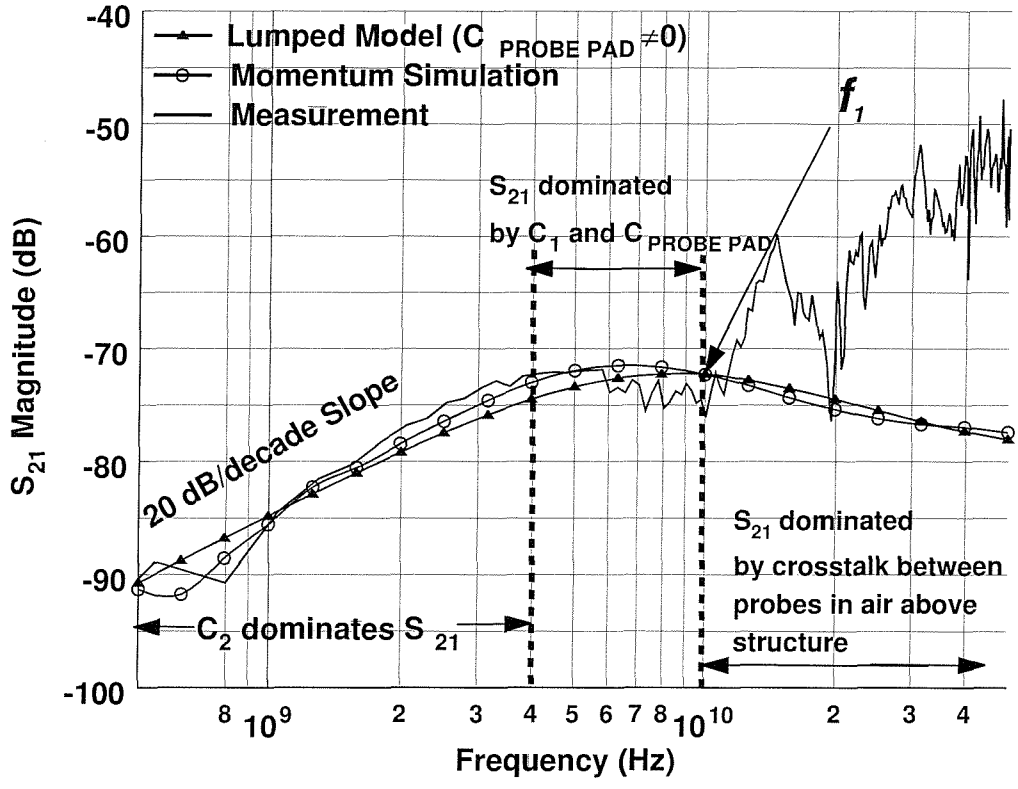


Figure 4.9: Comparison of Grounded GPSOI measurements, numerical simulations and lumped model for a Tx/Rx pad separation of 100 μm.

4.3.3 Model Analysis - The Capacitive π Network

The core of the simplified GPSOI model is the capacitive π-network of C_1 and C_2. Figure 4.10 shows a capacitive π-network embedded in a 50 Ω source and load environment, similar to the source and termination impedance of the scattering parameter set-up. From this simple model one can calculate s_{21} as a function of frequency.

The s_{21} characteristic has one zero at DC that is caused by the capacitance C_2. It also has two poles due to C_1 and C_2. The frequencies of the poles are:

$$f_1 = \frac{1}{2 \cdot \pi \cdot R_0 \cdot C_1} \tag{4.2}$$

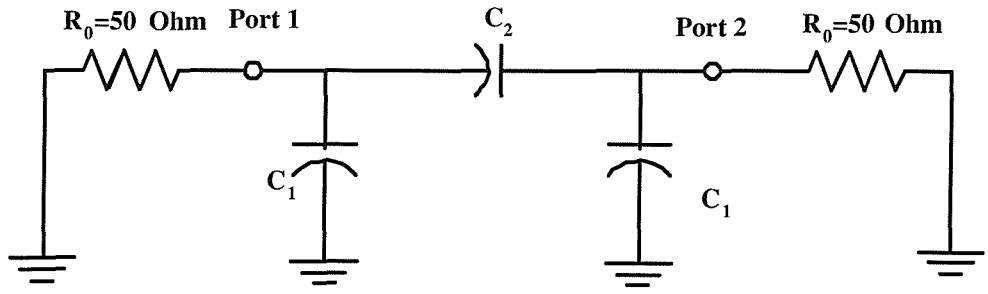


Figure 4.10: A capacitive π-network.

$$f_2 = \frac{1}{2 \cdot \pi \cdot R_0 \cdot (C_1 + 2 \cdot C_2)} \tag{4.3}$$

The two poles exist effectively at the same frequency because the value of C_1 is much greater than the value of C_2. Hence, this double pole changes the slope of the s_{21} characteristic from 20 dB to -20 dB per decade. This analysis reveals the two distinct regions of operation of the capacitive π-network. Below the double pole frequency C_2 dominates the response, whereas C_1 dominates above that frequency.

4.3.4 Model Analysis - Simplified Substrate Crosstalk Model

The analysis of the simple capacitive π-network can be repeated for the equivalent circuit of Figure 4.11 that includes R_1 and R_2, which represent the finite resistance of the ground plane. From the analytical derivation of s_{21} one can identify the existence of three poles and three zeros. The first zero is again at dc and forces a 20 dB per decade slope throughout the entire frequency spectrum. As before, the lateral capacitance C_2 is creating this zero.

The first pole exists at frequency f_{P1}, which is given by the following equation:

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot C_1 \cdot (R_0 + R_1)} \tag{4.4}$$

An additional pole exists at the frequency given by a very complicated equation and is approximately at the same frequency as the first pole f_{P1}. This effectively makes this pair of poles a single double pole, that forces a 40 dB per decade negative slope on s_{21}. The second zero occurs at

$$\begin{aligned} f_Z \;=\; & \frac{1}{4 \cdot \pi \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2} \cdot [2 \cdot R_2 \cdot C_2 + 2 \cdot R_1 \cdot C_2 + R_1 \cdot C_1 - \\ & - \left(4 \cdot R_1 \cdot R_2 \cdot C_1 \cdot C_2 + 4 \cdot {R_1}^2 \cdot {C_2}^2 + 4 \cdot C_1 \cdot C_2 \cdot {R_1}^2 + {R_1}^2 \cdot {C_1}^2\right)^{(\frac{1}{2})}] \end{aligned} \tag{4.5}$$

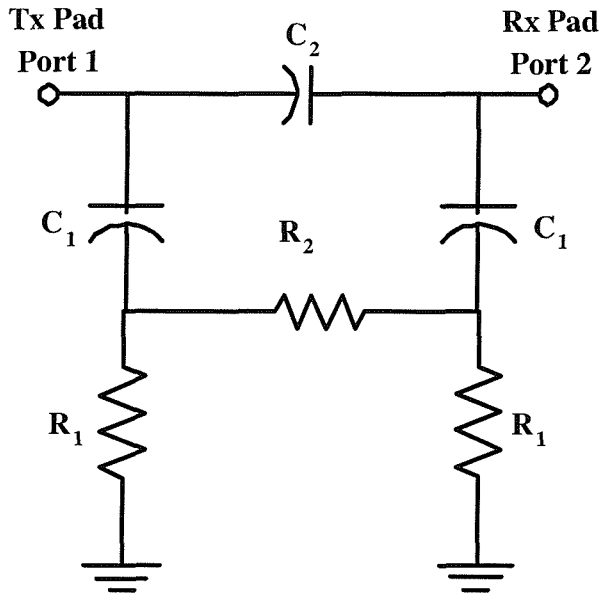


Figure 4.11: Substrate crosstalk model without the additional probe pad capacitances.

The remaining poles and zeros occur at very high frequencies and are not of interest. An example of the frequencies where these poles occur can be given by substituting R_1, R_2, C_1 and C_2 with their corresponding values for a specific Tx/Rx pad spacing. For 100 μm separation, the two poles occur at 36.7 GHz (a double pole) and the zero at 37 GHz. The location of the zero at approximately the same frequency as the double pole cancels one of the poles and therefore from that frequency onwards, s_{21} will remain at a constant level. This analysis is only concerned with frequencies up to 50 GHz, so the latter effect is not clearly visible in Figure 4.11. The electromagnetic simulations, and the model that include the probe pad capacitances, however, predict that at high frequencies s_{21} tends to flatten, which is in agreement with the aforementioned analysis. Chapter 5 also includes an analysis of the movement of poles as various model parameters are changed.

4.3.5 Importance of De-embedding - The "AC loading" Effect

The model of the grounded GPSOI substrate also include the capacitor $C_{PROBEPAD}$ that models the additional capacitance in parallel with that of the Tx/Rx pads of the probe pads and lines. This capacitance is of great importance because it appears in parallel with the pad capacitance and in fact has a higher value that C_1, mainly due to the larger dimensions of the probe pad (150 μm $\times$ 100 μm). Its effect on the magnitude of s_{21} can be demonstrated be omitting $C_{PROBEPAD}$ from the lumped element model (Figure 4.12). The pole introduced by the equivalent capacitance to ground now appears at a much higher frequency. This is an indirect method of

de-embedding the additional shunt capacitance introduced by the CPW structure from the Tx/Rx crosstalk model.

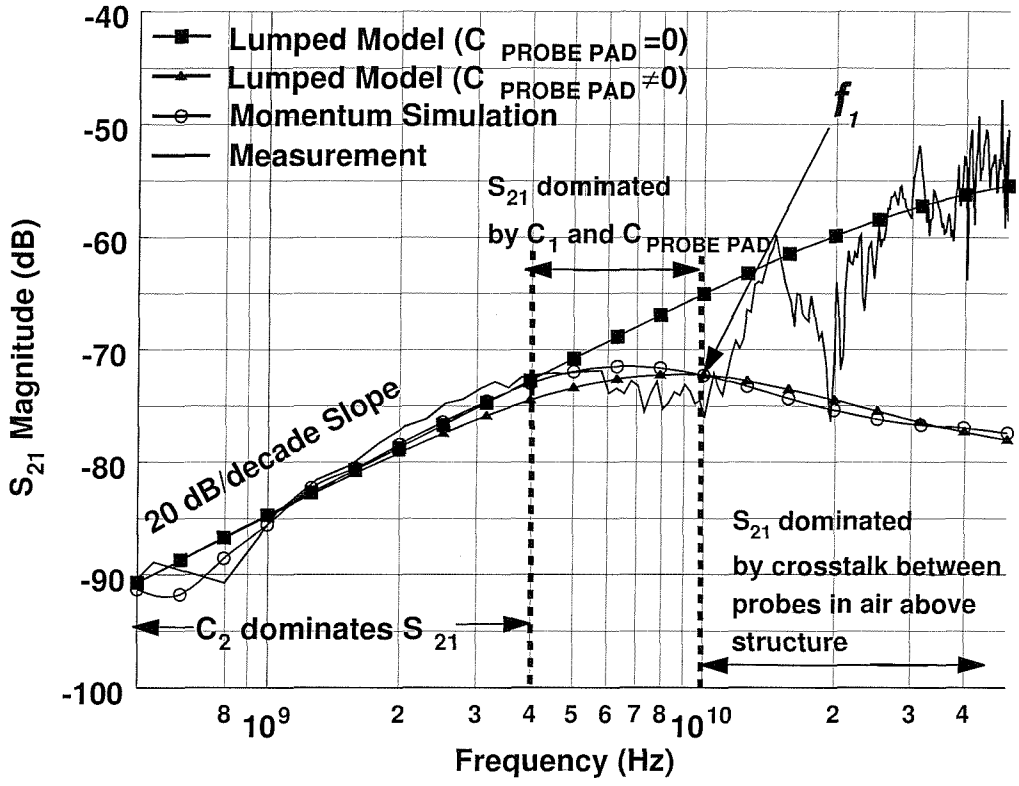


Figure 4.12: Effect of the probe pad capacitance ($C_{PROBEPAD}$) on the magnitude of s_{21}

Careful observation of the s_{21} characteristic reveals three distinct regions of operation that correspond to the aforementioned analysis. The first region extends up to 2 GHz and is clearly characterised by a slope of 20 dB per decade. The dominant model element for this region is the capacitance C_2, which will be referred to as the crosstalk capacitance from now on. Then, as frequency increases, the impedance through C_1 and $C_{PROBEPAD}$ reduces and more energy is shunted to ground rather than propagated through C_2. At very high frequencies C_1 and $C_{PROBEPAD}$ fully dominate the response by changing the slope to -20 dB per decade. This effect is only visible in the measurements below the frequency of 10 GHz because of the appearance of probe crosstalk beyond this point.

The effect of the equivalent capacitance C_1 can also be observed by varying its value on the capacitive π-network and keeping the values of other components constant. Figure 4.13 shows the results of these simulations for different values of C_1. As the transmitter pad node becomes "loaded" with a higher capacitance, the frequency where the slope of s_{21} becomes negative is decreasing. In the case of a 50 μm $\times$ 50

μm pad on 1 μm of oxide, this frequency is 37 GHz. Beyond that frequency, the Tx node is connected to ground through an increasingly lower impedance. This may not be a desirable effect for a device or a circuit and may in fact compromise its performance or even its operation. Depending on the application, the presence of a ground plane and the value of C_1 may impose a limit for the highest operational frequency of the GPSOI substrate. The capacitive elements of the model depend on substrate parameters such as the thickness of the oxide. The following chapter presents and analyses measurements from structures on substrates with variable oxide thickness and ground plane resistivity to provide more conclusive results on the scalability of s_{21}.

4.3.6 Predicting the Value of Crosstalk Capacitance

As mentioned before, the values of the lumped model elements were derived from numerical optimisation. This set of values, however, although providing a model that agrees very well with the measurements, lacks a physical background as to how these values are computed. Since, the dominant path of crosstalk is though the crosstalk capacitance C_2, the following analysis will be focused on understanding how its value can be derived. It has to be noted, that this task proved to be rather complex for a number of reasons, many of which were mentioned earlier. Firstly, a lumped component, such as the capacitor C_2, is used to model highly distributed electric field lines in an inhomogeneous dielectric. Secondly, the electric field between the receiver and transmitter, especially in the case of large spacing, is mostly fringing field. That is difficult to calculate analytically. Moreover, this field cannot be distinguished by the electric field between the pad and ground, which also has a fringing element. For these reasons, predicting the value of crosstalk capacitance from closed expressions derived from theoretical analysis proves to be a difficult task. The purpose however of this analysis is to identify how close to the values suggested by the numerical optimiser one could get, before resorting to the aid of an electromagnetic solver for increased accuracy.

The coupling between the Tx and Rx pads of the test structure can be viewed as similar case to coupled microstrip lines. A pair of coupled microstrip lines is shown in Figure 4.13. These are very long strips on a dielectric that separates them from an infinite perfect ground plane. The coupling between them is described by a set of capacitances that model the electric field between them through the air and the dielectric, together with the field between each line and the ground plane. Analytical expressions that describe the microwave characteristics of microstrip lines are not possible because of the existence of an inhomogeneous dielectric medium (air - dielectric). For a single microstrip line it can be shown through Maxwell

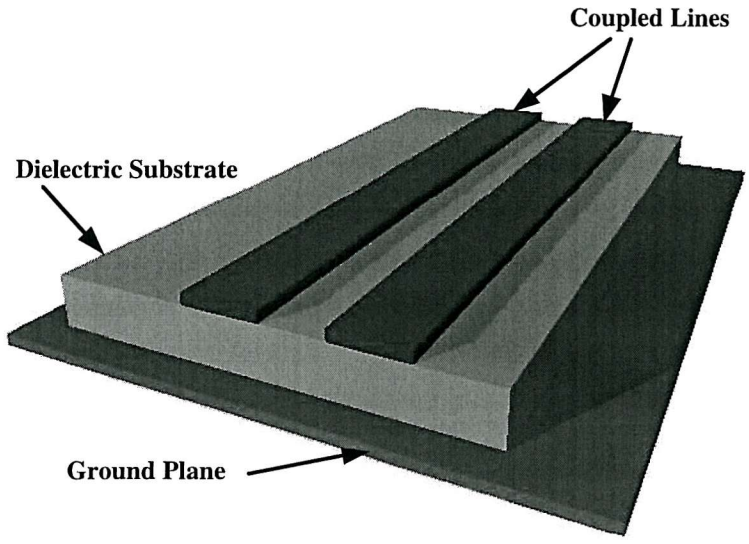


Figure 4.13: A pair of coupled microstrip lines.

equations that an applied wave will result in longitudinal components of the electric and magnetic fields [30]. These components, however, are very small and one can safely ignore them. Under the quasi TEM approximation, all components of the electric and magnetic fields are perpendicular to the direction of propagation. Numerical methods can be used to provide an exact solution of the microstrip line problem. Empirical expressions based on measurements and simulations have also been proposed by researchers [31], [32] for the derivation of a set of equations for coupled microstrip line design. These expressions, however, have been fine-tuned with data from specific line geometries (width and spacing) and substrate properties (permittivity and thickness) and tend to give large errors when they are used outside their limit of accuracy. As they are only numerical equations they also do not provide any insight to the physics of the problem.

Since the main objective is to model a capacitance, the method of analysing coupled microstrip lines in terms of their even and odd mode capacitances, as presented by [3], has been utilised. [3] and [30] define all the capacitances that are present in coupled microstrip geometry in the even and odd mode cases (Figure 4.14). For the even mode case, where both lines are excited by phased voltages, only the capacitances between each line and the ground plane exist because both lines are equipotential (Figure 4.14a). Hence,

$$C_e = C_P + C_f + C'_f \tag{4.6}$$

These capacitances are C_P, C_f, and C'_f. C_P is the capacitance to ground and is obtained by the geometry of the line. C_f and C'_f are fringing capacitances that are

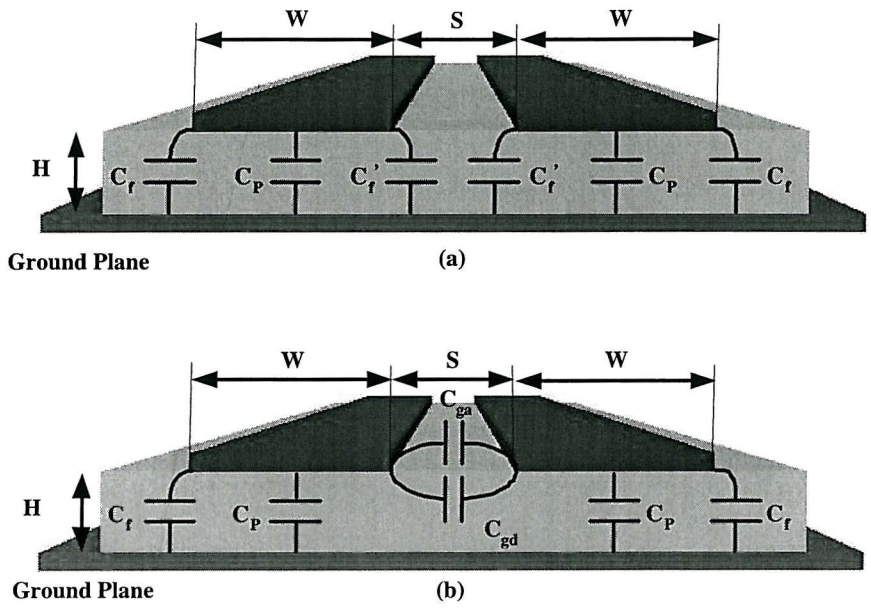


Figure 4.14: Decomposition of total capacitance of coupled microstrip lines in terms of various capacitances (a) Even-mode capacitances. (b) Odd-mode capacitances.

calculated by semi-empirical formulae:

$$C_P = \varepsilon_0 \varepsilon_r \frac{W}{H} \tag{4.7}$$

$$2 \cdot C_f = \frac{\sqrt{\varepsilon_{reff}}}{C \cdot Z_0} - C_P \tag{4.8}$$

$$C_f' = \frac{C_f}{1 + A \cdot \frac{H}{S} \cdot \tanh \frac{8S}{H}} \tag{4.9}$$

where

$$A = exp\left[-0.1 \cdot exp\left(2.33 - 2.53\frac{W}{H}\right)\right] \tag{4.10}$$

In the odd case (Figure 4.14b), the two lines are excited by out-of-phase voltages [33], which gives rise to the coupling capacitances C_{ga} and C_{gd} that account for the fringing fields across the gap in the air and dielectric regions respectively. C_{ga} and C_{gd} are obtained by the equivalent geometry of coplanar striplines (strip lines on dielectric without a ground plane) through conformal mapping transformations [33] The odd mode capacitance is therefore

$$C_o = C_P + C_f + C_{ga} + C_{gd} \tag{4.11}$$

where

$$2 \cdot C_{ga} = \varepsilon_0 \cdot \frac{K(k')}{K(k)} \tag{4.12}$$

and

$$k' = \sqrt{1 - k^2} \tag{4.13}$$

Also,

$$\frac{K(k')}{K(k)} = \begin{cases} \frac{1}{\pi} \ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right] \\ \frac{\pi}{\ln\left[2\frac{1+\sqrt{k}}{1-\sqrt{k}}\right]} \end{cases} \tag{4.14}$$

$$C_{gd} = \frac{\varepsilon_r \varepsilon_0}{\pi} \ln \coth\left(\frac{\pi}{4} \cdot \frac{S}{H}\right) + 0.52 \cdot C_f \left[\frac{0.02}{\frac{S}{H}}\sqrt{\varepsilon_r} + 1 - \varepsilon_r^2\right] \tag{4.15}$$

The coupled microstrip line pair is modelled with a purely capacitive network in the same way as the π-network described earlier. If i and v are vectors representing port currents and port voltages respectively, the capacitance matrix [C] may be defined as:

$$i = j \cdot \omega \cdot [C] \cdot v \tag{4.16}$$

The even and odd mode capacitance are related to the capacitance [34],[30],[3] as follows:

$$[C] = \begin{bmatrix} C_{11} & C_{12} \\ C_{21} & C_{12} \end{bmatrix} = \begin{bmatrix} \frac{C_e+C_o}{2} & \frac{C_e-C_o}{2} \\ \frac{C_e-C_o}{2} & \frac{C_e+C_o}{2} \end{bmatrix} \tag{4.17}$$

On the other hand the capacitance matrix of the π-network is:

$$[C] = \begin{bmatrix} C_1 + C_2 & -C_2 \\ -C_2 & C_1 + C_2 \end{bmatrix} \tag{4.18}$$

Hence, the capacitive π-network parameters are related to even and odd mode capacitances by the following expressions:

$$C_2 = \frac{C_o - C_e}{2} \tag{4.19}$$

$$C_1 = \frac{C_e - C_o}{2} - C_2 = C_e \tag{4.20}$$

The previous expressions correspond to capacitance per unit length values. It can also be observed that there is a direct dependence on the width of the line and the spacing between the lines. Therefore, since the total area of the lines affects the values of the lumped model, the entire area of the receiver and transmitter in the GPSOI test structure has to be considered. The total area varies with the variable spacing because the probe pads were kept the same distance apart for all the test structures and only the spacing between the Tx and Rx pads changed. The aforementioned formulae can be enhanced to include the effect of the thickness of

Spacing (μm)	Numerical Optimiser	C_2 (fF) from (4.6) to (4.20)		C_2 (fF) from 4.21	
		Analytical	%Error	Analytical	% Error
75	0.112	0.206	84	0.113	1.25
100	0.093	0.131	41	0.098	5.37
150	0.064	0.071	11	0.075	17
200	0.046	0.039	15	0.048	4.34

Table 4.3: Comparison of analytically derived crosstalk capacitance C_2 values with those extracted from the numerical optimiser.

the line, which can be a significant component in their accuracy since the thickness of the substrate is comparable (equal) to the thickness of the aluminium lines (1 μm). Although not shown analytically here, these modifications were included in the calculations and can also be found in [3] and [30].

Another point that should be noted is that these expressions can take into account the effect of the total area but not the effect of the different geometrical characteristics of the structure such as the steps in width (Figure 4.15) that result in abrupt changes of the pattern of the electric field. Furthermore, since all expressions calculate values per unit length, fringing fields from the sides of the Tx/Rx pads are not taken into account. Figure 4.15 illustrates these issues by showing the equivalent geometry that is applicable to the capacitance expressions.

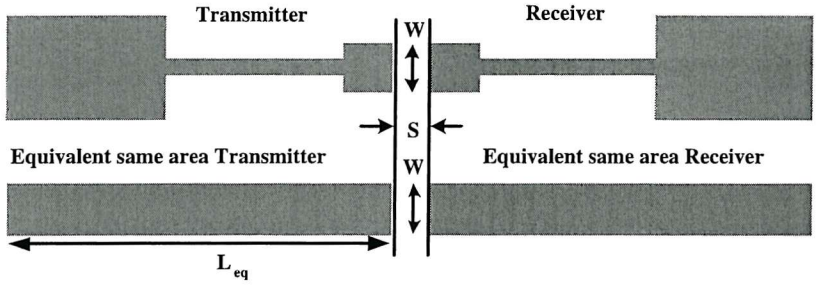


Figure 4.15: Equivalent microstrip line geometry used to calculate the crosstalk capacitance according to formulae by [3].

Table 4.3 and Figure 4.16 compare the crosstalk capacitance C_2 values of the lumped element model as produced by the numerical optimiser with the values derived by the previous formulas. The analytical expressions agree well (within 15%) for the highest separation distances (150 and 200 μm) but their accuracy decreases rapidly as the separation decreases. Figure 4.16 shows that this is due to the linear behaviour of the extracted values of C_2 with respect to distance, whereas the net effect of C_2 from the analytical calculation is not linear.

The accuracy of the model equations can be enhanced by modifying the empirical parts of some of the expressions that are used in the calculation of C_2. For instance,

Garg et. al [3] mention that C_{gd} is derived from the equivalent geometry of coplanar striplines (striplines on dielectric without a ground plane) but is modified for use with microstrip lines. A further modification, which reduces the error between the analytical and extracted (by the optimiser) values could be the introduction of an additional empirical term, which is related to the ratio S/H, where S is the spacing between the pads and H is the oxide thickness. The modified expression of C_{gd} now becomes:

$$\begin{aligned} C_{gd} &= \frac{\varepsilon_r \varepsilon_0}{\pi} \ln \coth\left(\frac{\pi}{4} \cdot \frac{S}{H}\right) + \\ &+ \left(2 \cdot 10^{-7} \cdot \left(\frac{S}{H}^3\right) + (-7 \cdot 10^{-5}) \frac{\dot{S}}{H}^2 + 0.0082 \frac{S}{H} + 0.5222\right) \cdot \\ &\cdot C_f \left[\frac{0.02}{\frac{S}{H}} \sqrt{\varepsilon_r} + 1 - \varepsilon_r^2\right] \end{aligned} \tag{4.21}$$

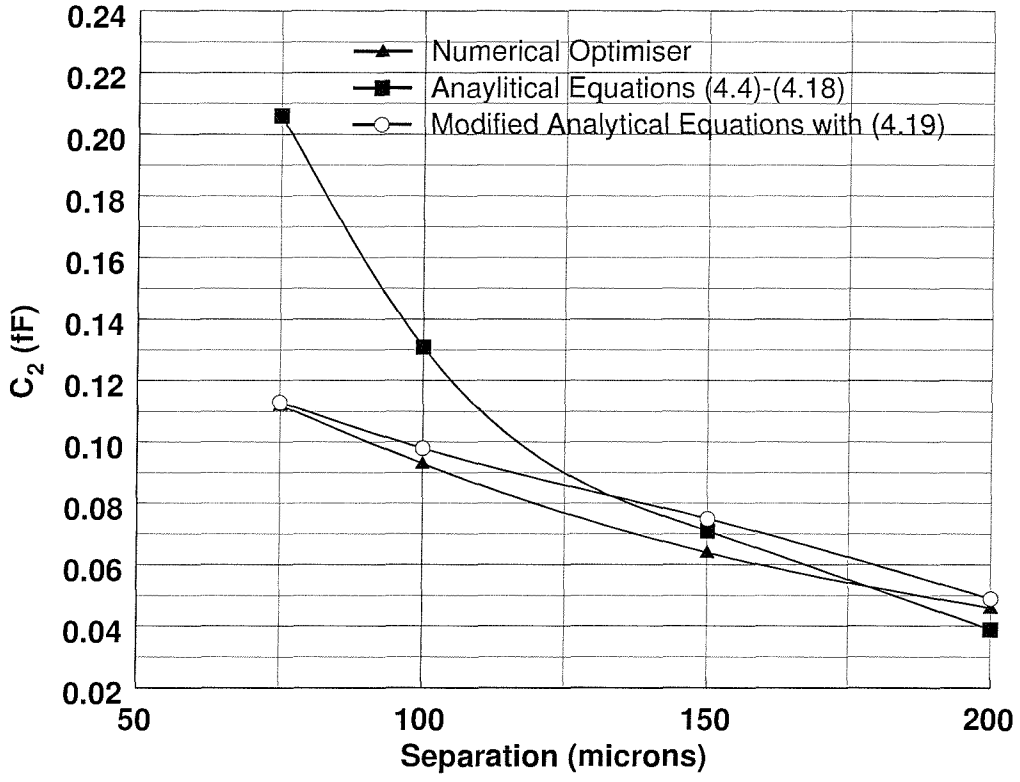


Figure 4.16: Comparison of crosstalk capacitance calculations based on the analytical expressions and numerical optimizer values for variable separation distances.

The new values of the crosstalk capacitance C_2 are also shown in Table 4.3 and Figure 4.16. The introduction of the new empirical term has greatly improved the

agreement between the extracted and the analytical data. This procedure demonstrates that once experimental data are available, a model can be extracted and fitted to these data by using empirical expressions at the expense of physically derived analytical solutions. In principle, by applying functional approximation techniques, one could create a set of model equations that simply fit the model parameters to the experimental data, while reducing at the same time the understanding of the physical origin of the model. In addition, in order for an empirical model to be applicable to a wide range of parameter values, a large number of experimental data have to be input to the model during the fitting process.

4.4 Conclusions

Electromagnetic solvers have been used to simulate the crosstalk effects of the GPSOI test structures presented in the previous chapter. The modelling was targeted at the grounded GPSOI test structures that exhibited the highest degree of isolation. The simulation results were validated against the measurement data and good agreement was observed showing that these tools can also be utilised, in addition to specialised CAD software, to predict substrate crosstalk. A compact lumped element model was presented. Although the physical origin of the model elements was clear, their values were initially derived using numerical optimisation. Microstrip line theory was then used to estimate the value of the crosstalk capacitance, which corresponds to the electric field coupling between the transmitter and receiver of the test structure and accounts for the crosstalk between them. This analysis demonstrated how close theory can be to the extracted values before utilising a time consuming electromagnetic solver It also highlighted the limitations in producing analytical formulae that describe highly distributed components such as the electric field coupling lines. Finally, the importance of de-embedding the structure under test from the surrounding coplanar structure that has to included for the measurements was also investigated. The additional probe pad capacitance has a drastic effect on the crosstalk characteristic and highlights a potential frequency limitation of the GPSOI substrate.

Chapter 5

Analysis Of Buried Oxide And Ground Plane Resistivity Effects On Pseudo-Ground Plane Substrate Crosstalk

5.1 Introduction

Chapters 3 and 4 presented and analysed the crosstalk behaviour of a buried ground plane substrate with a specific buried oxide thickness and a ground plane of a certain thickness and resistivity. The thickness of the buried oxide is crucial, since it determines the separation of the Tx/Rx pads (or circuitry in general) from the ground plane and is therefore associated with the overall level of crosstalk and the shape of the s_{21} frequency response.

The ground plane technology, as described in Chapter 3, was not available to the author and test structures with pseudo-ground planes had to be designed and fabricated so that the effect of the buried oxide thickness and ground plane resistivity could be investigated. Chapter 5 presents these structures along with experimental data and modelling analysis of their crosstalk behaviour. A brief analysis of coupled microstrip lines on aluminium and $TiSi_2$ pseudo-ground plane substrates is also included at the end of the chapter.

5.2 Pseudo-Ground Plane Test Structures

The behaviour of a buried ground plane substrate structure with WSi_2 ground plane can be emulated by fabricating a double metal layer structure. The first metal layer can be deposited or sputtered on the silicon substrate (handle) and form the ground plane. A layer of oxide has to be deposited next that emulates the buried oxide of the GPSOI. After etching the top down contacts to the ground plane, the second

metal layer is sputtered and patterned to form a structure identical to those of Chapter 3, but with the desired ground plane and oxide layer properties. The objective of these experiments is not to a create a new ground plane structure but only to emulate the behaviour of the fabricated buried ground plane test structures, even if the processing steps are different from those of GPSOI technology.

Fabrication of these test structures took place at the Microelectronics Centre of Southampton University (SUMEC). Tungsten deposition was not available at the time of fabrication and a different metal had to be used. A titanium silicide ($TiSi_2$) process that produces a metallic plane with similar sheet resistance to that of the WSi_2 plane was available. Aluminium (Al) may also be sputtered as a ground plane and its use can investigate the effect on crosstalk of a very conductive, almost "perfect" (compared to WSi_2 and $TiSi_2$) ground plane. Both Al and $TiSi_2$ layers were chosen to be 0.2 μm thick, equal to the thickness of the WSi_2 layer of the GPSOI experiments.

After the ground plane is sputtered on the silicon handle, a dielectric has to be deposited that emulates the buried oxide. This step was carried out by plasma oxide deposition (PECVD) and the oxide thicknesses were 0.25, 0.5, 1.0, 1.5 and 2.0 μm. The next processing step is the top-down contact etch that will provide the grounding connection of the buried Al or $TiSi_2$ plane to the surface RF ground. Finally, the entire test structure is formed by sputtering and patterning the top metal layer. A detailed listing of the entire fabrication process is included in Appendix C. Figure 5.1 shows the organisation of the experiments in terms of the substrate parameters that are varied.

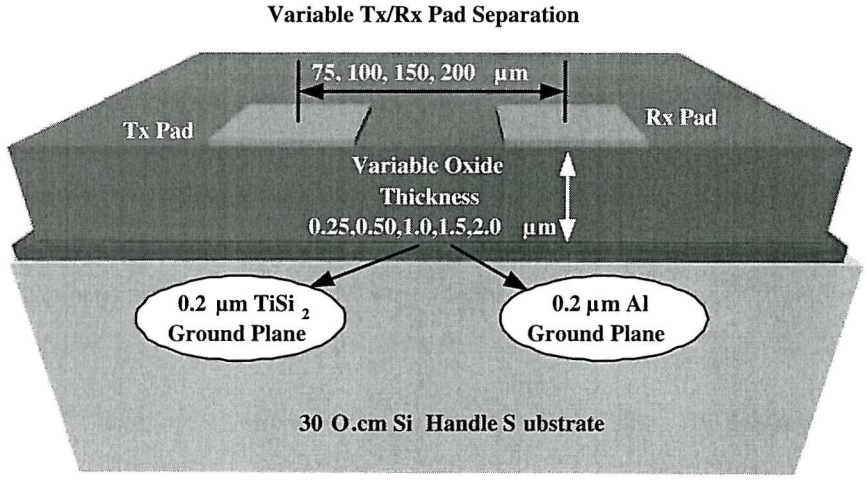


Figure 5.1: Process and layout parameter variations for the experiments of this Chapter. The thicknesses of the oxide and the ground plane are the process variables and the Tx/Rx separation distance the layout variable.

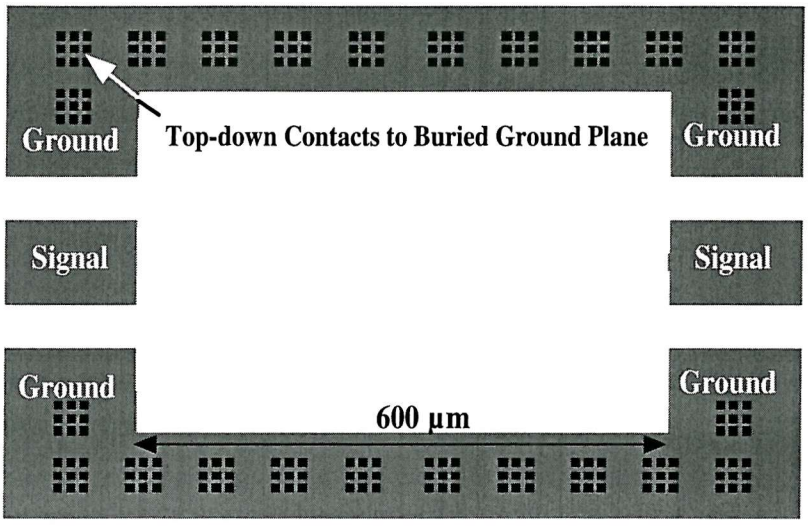


Figure 5.2: Plan view of the structure for probe crosstalk and noise-floor measurements.

5.3 Probe-to-Probe Crosstalk - A Noise "Floor" of the Measurement Equipment

Measurements in Chapters 3 and 4 have shown that a significant amount of crosstalk is not visible at frequencies above 10 GHz because it is screened by probe crosstalk. Probe crosstalk through air was significantly higher than the measurements when the probes were in air far away from the substrate. The conclusion that high frequency measurements were screened by probe crosstalk was based on two observations. The first one was the convergence of all measurement trances for different Tx/Rx pad separation distances to a single trace that followed a rather irregular pattern. The convergence occurred at approximately 10 GHz and indicated that the geometry of the structure itself and the Tx/Rx pad separation in particular did not affect the magnitude of s_{21}. The second observation was that neither the electromagnetic simulators nor the lumped element model topology could predict such high frequency behaviour. Hence, it was indirectly deduced that s_{21} response over 10 GHz is due to probe crosstalk.

The pseudo ground plane experiments in this chapter allow measurement of the crosstalk between the probes and signal and ground probe pads, by placing the probes very close to the ground plane at 0.25 μm. This can be accomplished by the structure of Figure 5.2 where there are no feedlines and no Tx/Rx pads. Measurement of s_{21} in this structure reveals the amount of crosstalk between signal and probe pads and through the air. The dimensions of this structure are identical to

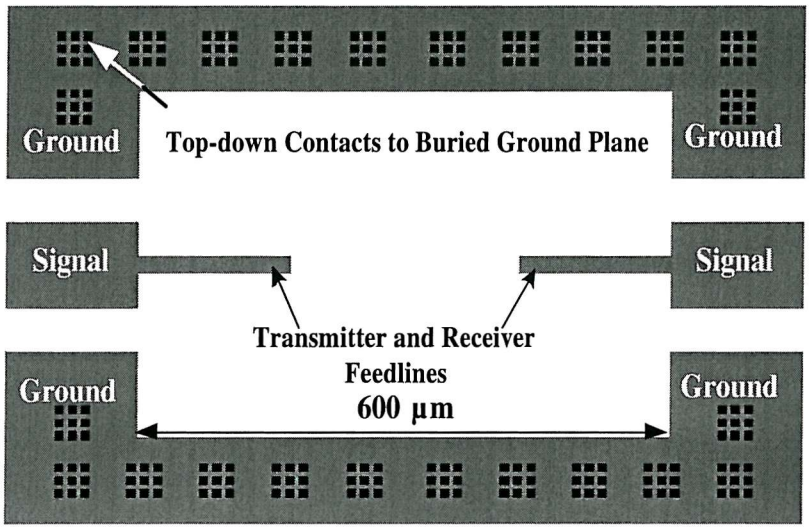


Figure 5.3: Plan view of "open" structure for de-embedding.

those of the test structures presented so far in this work. Hence, probe crosstalk is expected to be the same as before, since the probe pads are spaced the same distance as in the measured crosstalk test structures. By adding feedlines to the structure (Figure 5.3) it is possible to construct a de-embedding structure for the crosstalk test structure of Figure 5.4. The magnitude of s_{21} is expected to increase as new features are added to the initial GSG CPW structure.

Figure 5.5 shows how s_{21} varies in a structure without feedlines and Tx/Rx pads for different oxide thicknesses. There is no variation on s_{21} that could be clear and quantified. Hence, such response constitutes a "noise floor" for the equipment set and the kind of measurements that are performed. The location of the s_{21} response with respect to both the de-embedding structure and the entire test structure reveals how efficiently de-embedding can be done.

Comparison of the measurements for the three structures on a substrate with 2.0 μm of oxide, a $TiSi_2$ ground plane and 75 μm Tx/Rx pad separation is shown in Figure 5.6.

The measurement of the test structure is clearly above the open structure and the structure without the feedlines and Tx/Rx pads, as expected. On the other hand, the structure without the feedlines and Tx/Rx pads exhibits clearly the lowest amount of crosstalk but not much lower than the open structure. It is therefore clear that lateral crosstalk between the two feedlines is much lower than Tx/Rx pad crosstalk and does not affect s_{21} of the DUT. Such behaviour is expected because the

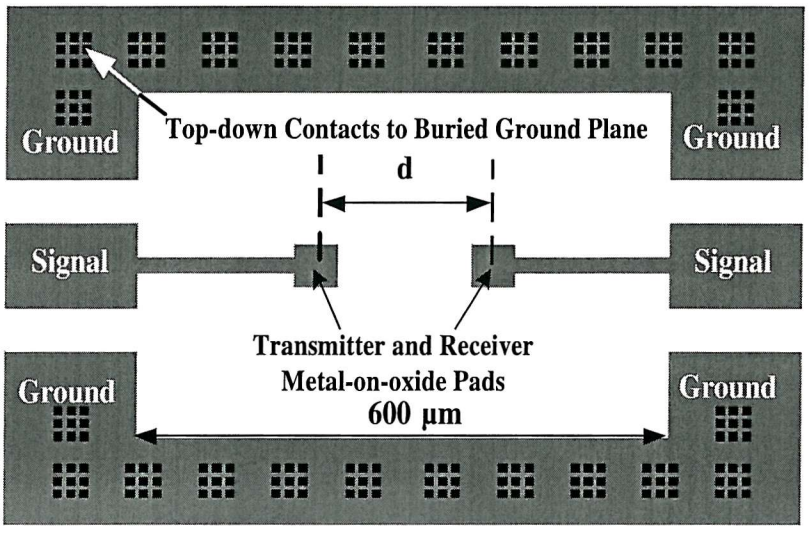


Figure 5.4: Plan view of complete substrate crosstalk structure with two square Tx/Rx pads (50 μm wide)

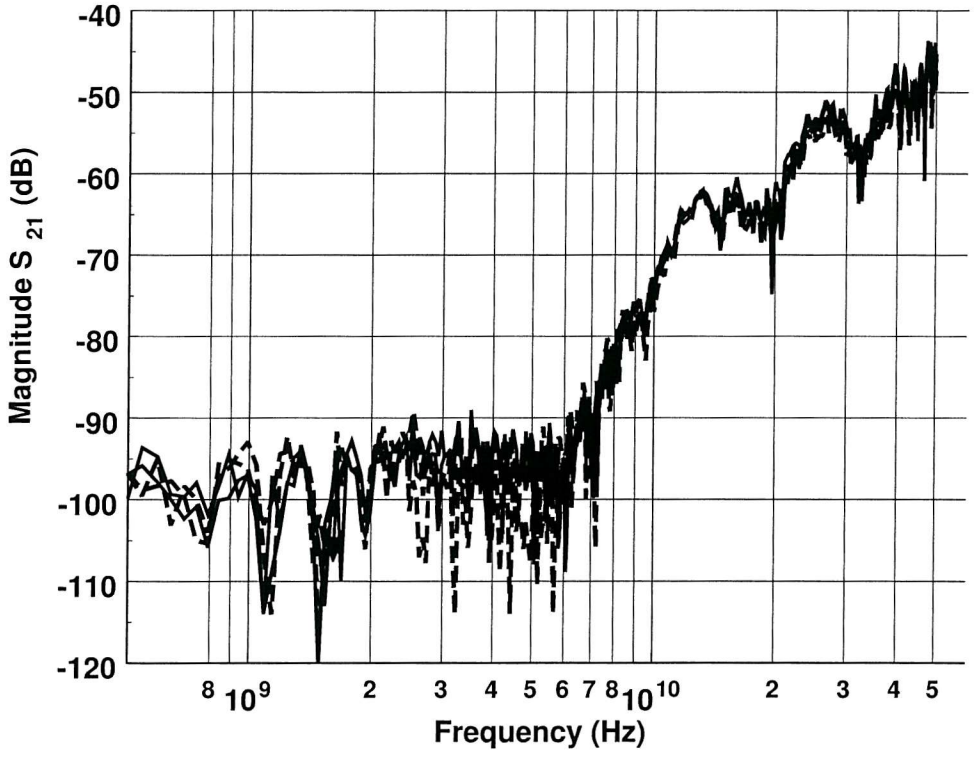


Figure 5.5: Measurement data taken from the structure of Figure 5.2 for different oxide thicknesses on both Al and $TiSi_2$ ground planes. Probe pad separation is 600 μm.

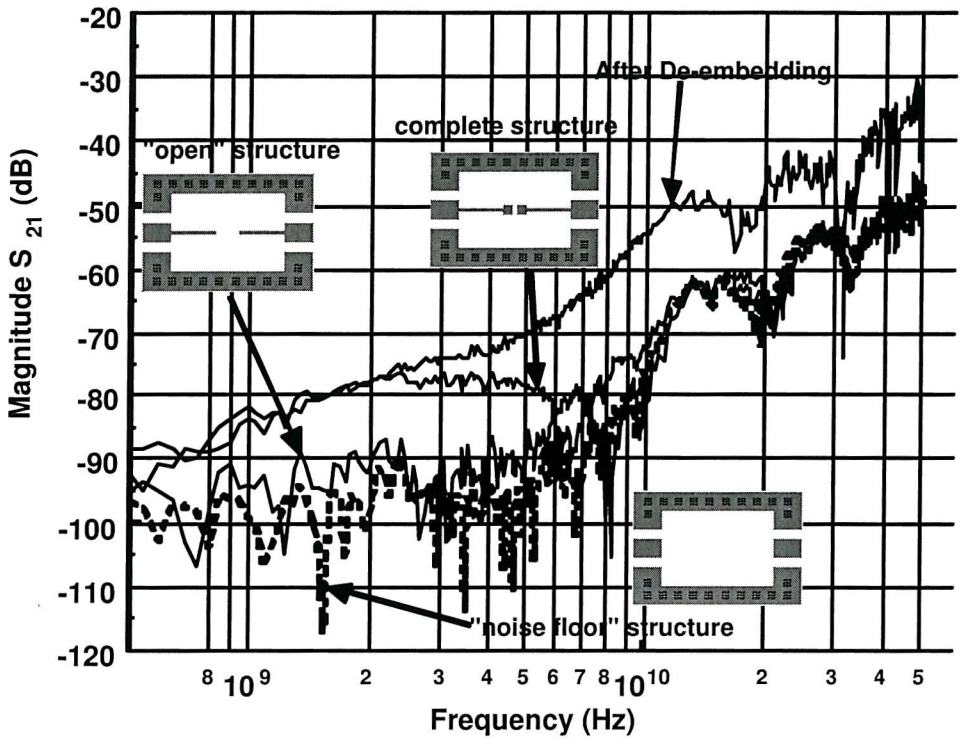


Figure 5.6: Measurement data from a "noise-floor", an open and a complete test structure before and after de-embedding for a Tx/Rx pad separation of 75 μm, on 1.0 μm of oxide and a $TiSi_2$ ground plane.

feedlines are spaced 125 μm and are only 25 μm wide, constituting weaker Tx/Rx noise sources. All three traces seem to converge at 15 GHz and additionally the whole test structure is clearly affected by probe crosstalk at a lower frequency. De-embedding the open structure from the entire test structure produces an artificial increase of crosstalk, which is due to the screening of the measurement data from the probe crosstalk and results in compromising the efficiency of the de-embedding.

5.4 The Effect of Oxide Thickness and Ground Plane Resistivity on Substrate Crosstalk

The effect of oxide thickness to substrate crosstalk can be explained with the aid of the lumped element model of Chapter 4, shown also in Figure 5.7. By decreasing the oxide thickness, the Tx/Rx pads are placed closer to the ground plane. The vertical capacitance C_1 between each pad and the ground plane, increases and therefore the ac loading frequency increases. On the other hand, C_2 should decrease because it represents the lateral electric field lines between the Tx/Rx pads and the closer the ground plane exists, more electric field lines are terminated on the ground plane.

Measurements of the magnitude of s_{21} versus frequency for variable oxide thickness for an aluminium ground plane are shown in Figure 5.8. The separation of the

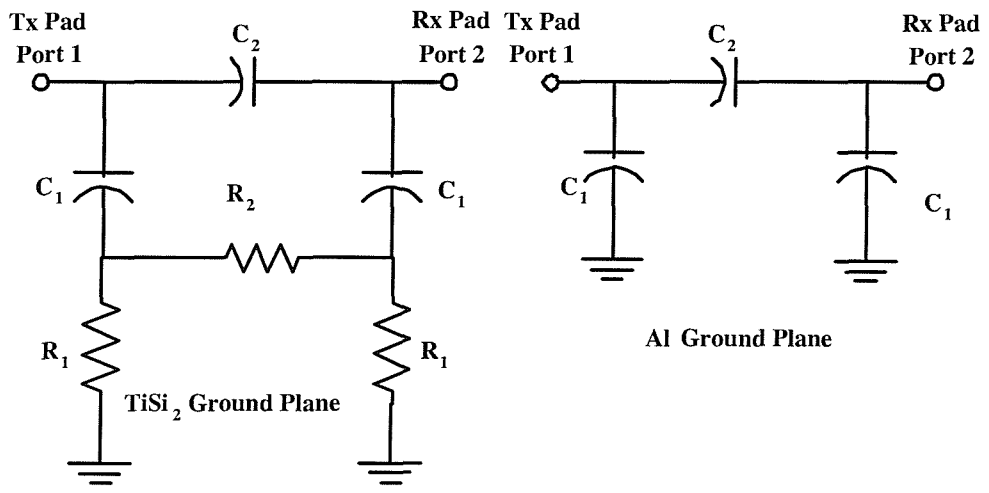


Figure 5.7: Lumped model of crosstalk in a buried ground plane test structure and its reduction to a capacitive π-network when R_1 and R_2 are assumed negligible.

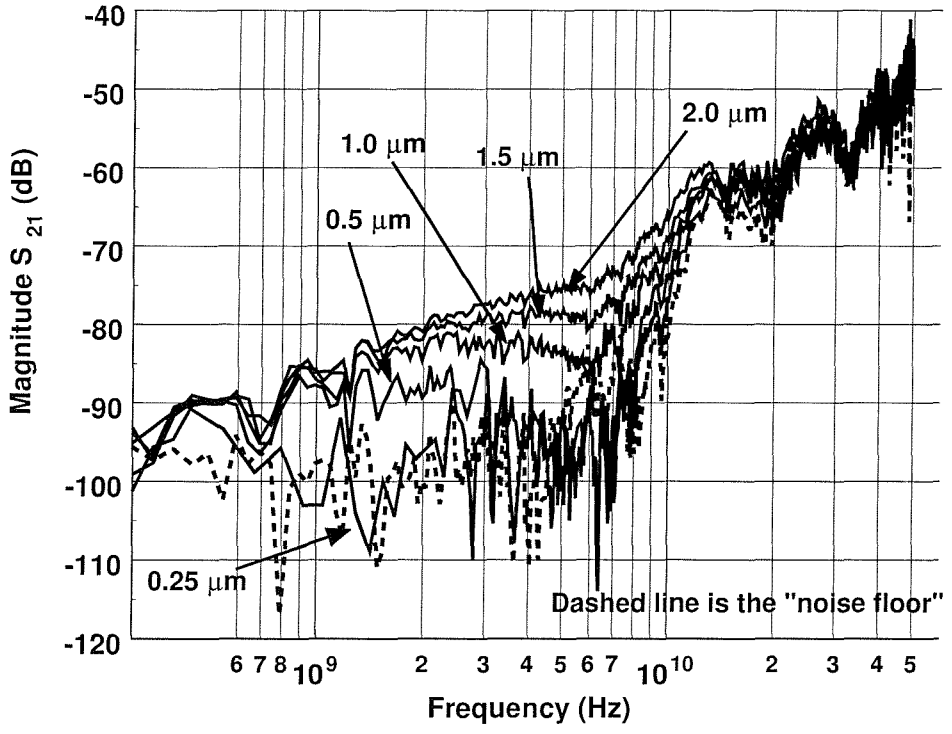


Figure 5.8: Crosstalk measurement data for a test structure with 100 μm Tx/Rx pad separation, aluminium ground plane and variable oxide thickness (0.25, 0.5, 1, 1.5, 2.0 μm).

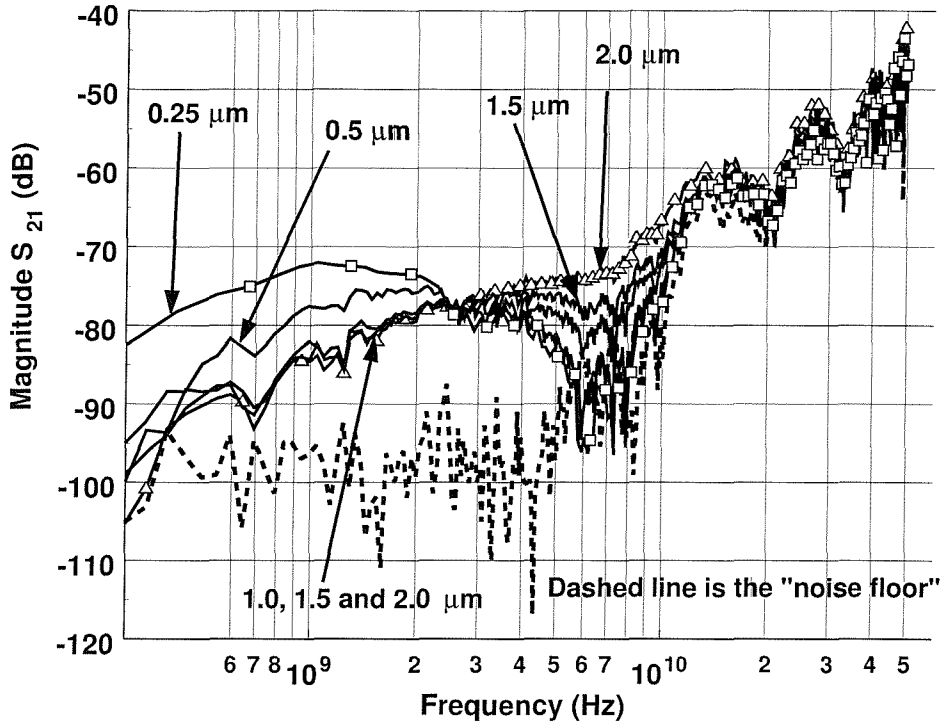


Figure 5.9: Crosstalk measurement data for a test structure with 100 μm Tx/Rx pad separation, a $TiSi_2$ ground plane and variable oxide thickness (0.25, 0.5, 1, 1.5, 2.0 μm).

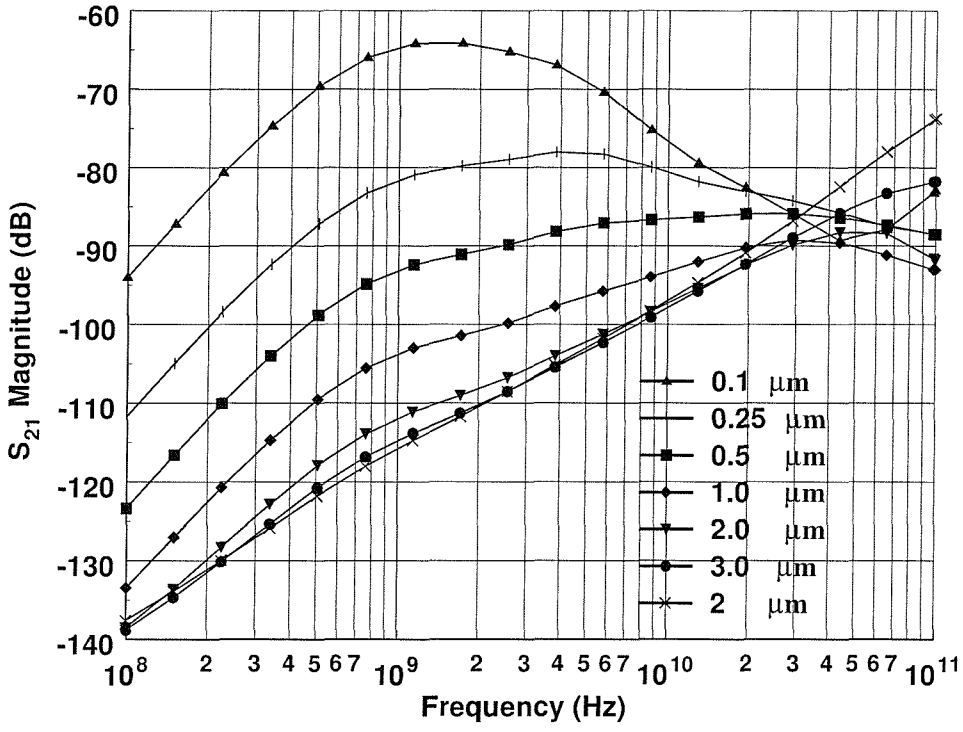


Figure 5.10: *EM-Sight* simulations of variable oxide thickness on $TiSi_2$ lossy ground plane.

Tx/Rx pads is 100 μm. Since the ground plane is aluminium and therefore much more conductive (approximately 20 times) than WSi_2 or $TiSi_2$, the lumped model of Figure 5.7 can be reduced to a simple capacitive π-network consisting only of the capacitances C_1 and C_2. The effect of C_1 and hence the oxide thickness is shown by the lower values of the ac loading frequency as the oxide thickness increases. Low measurement frequencies are not affected significantly.

Figure 5.9 shows the same measurements for a $TiSi_2$ ground plane. The sheet resistance of the $TiSi_2$ layer was measured during processing to be 1.1 Ω per square, slightly lower the intended 2 Ω per square, but still a lot higher than that of the aluminium ground plane. A reverse trend in s_{21} is shown when a lossy $TiSi_2$ ground plane exists, with thinner oxides producing higher crosstalk at low measurement frequencies (below 3 GHz). Such behaviour indicates that the combination of thinner oxides and perfect or lossy ground planes results in opposite trends in overall isolation performance.

Electromagnetic simulations have also been employed to verify the aforementioned behaviour. Simulations results are shown in Figure 5.10 and allow a more detailed investigation of this behaviour because they do not suffer from measurement noise and other artefacts. Apart from the different levels of crosstalk that are simulated for different oxide thicknesses and constitute the reverse trend in s_{21}, a different slope is also observed at low simulations frequencies. Thinner oxides exhibit a 40 dB per decade slope until the loading frequency is reached. One could therefore conclude that there are two regimes of operation that depend on the combination of oxide thickness and ground plane resistivity. When the oxide thickness is 1.0 μm, the slope of the s_{21} response remains 20 dB per decade, which is in agreement with the observations and the analysis of the buried ground plane substrates in Chapters 3 and 4.

An interesting finding of the simulations is that the amount of crosstalk seems to saturate when the oxide thickness is varied from 1.0 μm to 2.0 μm. If it is assumed that the frequency range from valid operation is below the ac loading frequency, one could find an optimum pair of oxide thickness and ground plane resistivity that causes the structure to exhibit the lowest amount of crosstalk. Thicker oxides exhibit high ac loading frequency at the expense of high crosstalk. Thinner oxides on the other hand, increase crosstalk and at the same time decrease the loading frequency. This effect is only observed at the lossy $TiSi_2$ case but not on the aluminium ground plane structure. The latter does not exhibit significantly low frequency crosstalk variation with oxide thickness. Very thick oxides will obviously

result in higher crosstalk but oxide thicknesses up to 2.0 μm only affect the ac loading frequency.

The reverse trend in the isolation performance of increasingly thinner oxides on lossy ($TiSi_2$) buried ground planes may be analytically explained with the help of the lumped element model crosstalk model for buried ground planes Figure 5.7. The slope of the lower s_{21} frequency response indicated that the location of the poles and zeros has been such that a 40 dB per decade slope was forced between two frequencies. Figure 5.11 shows how the location of the poles and zeros, which are calculated according to equations 4.6 to 4.20, changes when C_1 is increased. Thinner oxides do not only affect C_1 but also C_2 and possibly the other parameters. However, varying only C_1 is sufficient to show how the change of slope is introduced in the response. According to Figure 5.11, when the zero frequencies are lower than the poles frequencies, the frequency response exhibits a 40 dB per decade slope because of the pole. No visible change in the slope response occurs, so long as both poles and zero are in close proximity. As C_1 increases, the zero moves further away from the double pole and imposes a change in the slope of the response at an increasingly lower frequency as shown in Figure 5.12.

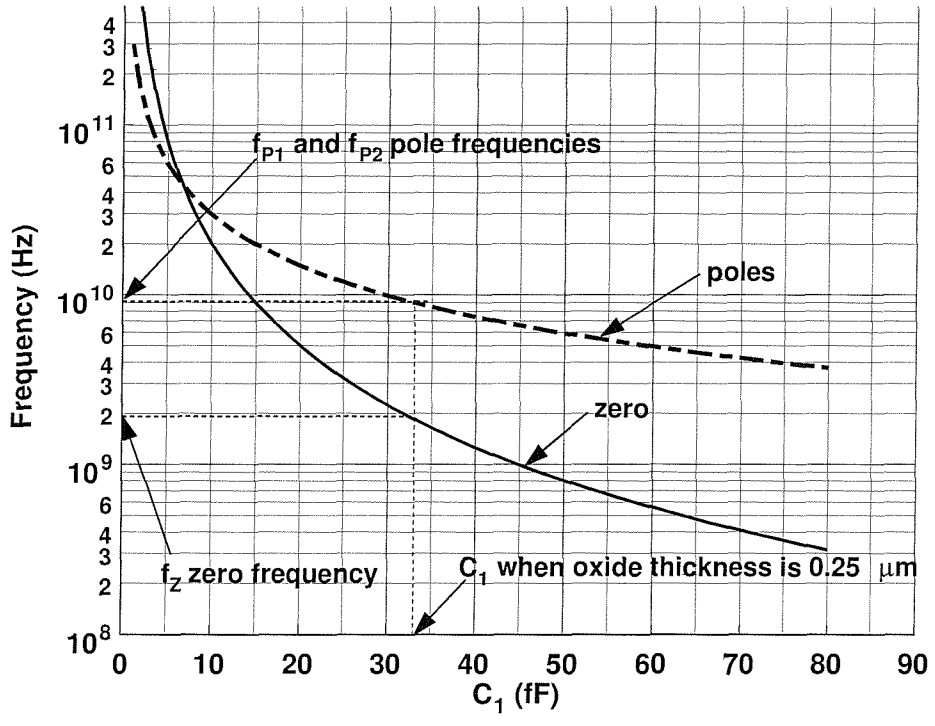


Figure 5.11: Location of zeros and poles according to equations (4.6) to (4.20) as a function of the oxide capacitance C_1. An example of poles and zero frequency values for an oxide of 0.25 μm is also shown.

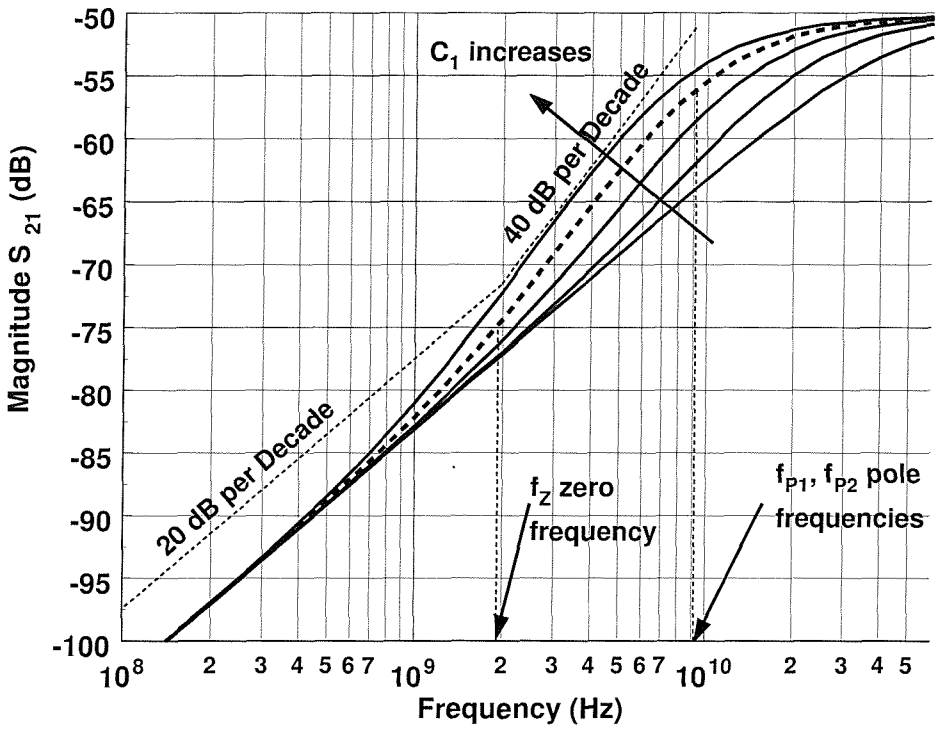


Figure 5.12: Magnitude of s_{21} frequency response of the lumped model of Figure 5.7 when C_1 is increased and C_2, R_1, R_2 are kept constant. The dashed line shows the response, when the value of C_1 corresponds to an oxide thickness of 0.25 μm.

5.5 Coupled Microstrip Lines on Pseudo-Buried Ground Plane Substrates

The analysis of substrate crosstalk has so far been closely related to the studies of microstrip lines and the relevant theory has been employed in order to derive a suitable substrate crosstalk model. This section presents experimental measurement data from microstrip line pairs fabricated on pseudo ground plane substrates with either Al or $TiSi_2$ buried ground planes, with different oxide thicknesses. These studies reveal the importance of accurate microstrip line pair models for the modelling of substrate crosstalk effects in substrates with buried ground planes. A coupled microstrip line configuration allows validation of the analytical solutions presented in earlier chapters as it takes into account the long line approximation that is assumed. In other words, an analytical solution based on microstrip coupled line theory assumes that the length of the line is much higher that the width, the spacing between the lines and the distance from the ground plane (i.e. thickness of the dielectric that separates the lines from the ground plane). From a measurements point of view, long microstrip lines are expected to exhibit higher amounts of coupling and therefore are easier to measure, since their s_{21} response lies further away from the "noise-floor" of the measurement set-up that has been shown to

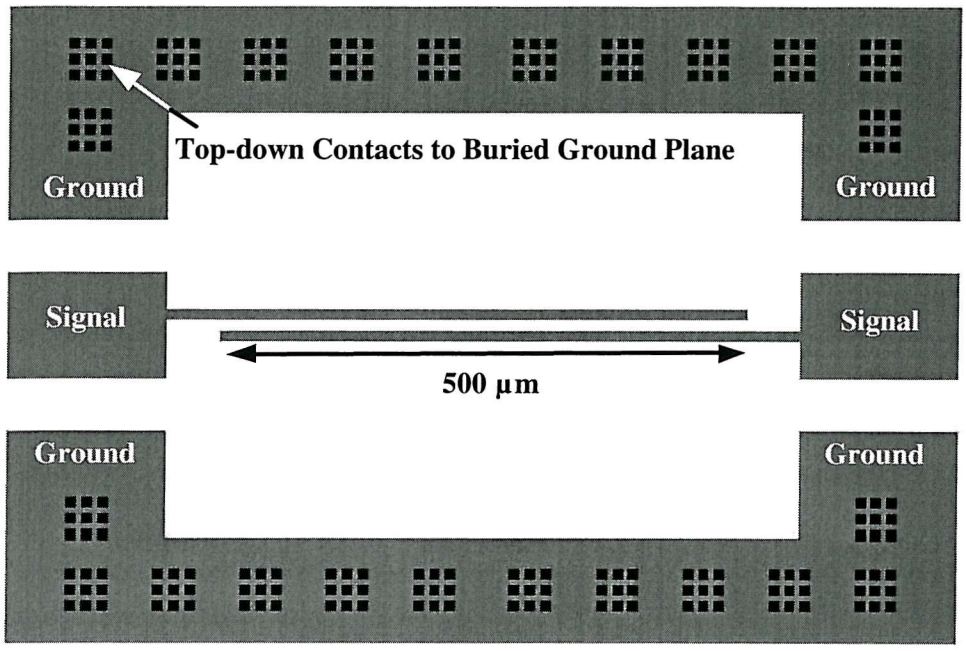


Figure 5.13: Coplanar waveguide structure containing two 500 μm long, 10 μm wide coupled microstrip lines, separated by 10 μm.

interfere significantly in the measurement of the crosstalk test structures.

5.5.1 Coupled Microstrip Lines on Aluminium ("Perfect") Ground Planes

Four microstrip line pairs were fabricated on aluminium pseudo-buried ground plane substrates. The length of each line was 500 μm and the width 10 μm. The lines of each pair were separated by 10, 25, 50 or 75 μm respectively. A layer of oxide separated the lines from the 0.2 μm thick aluminium ground plane, which was sputtered on a silicon substrate. The coupled lines were embedded in a coplanar structure as shown in Figure 5.13.

Measurement data of s_{21} as a function of frequency for variable coupled line spacing and variable oxide thickness are shown in Figures 5.14 and 5.15 respectively. The exhibited behaviour in both plots is in agreement with the analysis of the crosstalk test structures presented in chapters three and four. The magnitude of s_{21} is increasing at a rate of 20 dB per decade at low frequencies due to lateral capacitive coupling. At approximately 3.5 GHz, the coupling reaches its maximum level and then begins to decrease at a rate of -20 dB per decade as the vertical capacitance of the coupled line through the oxide down to the ground plane loads the Tx pad and begins to dominate the response. The loading effect is not fully visible because at approximately 10 GHz the noise-floor of the measurement equipment and the surrounding coplanar structure interferes and dominates the measurement data. The point of the ac loading frequency remains the same for all measurements regardless of the spacing because the total area of the structure remains the same.

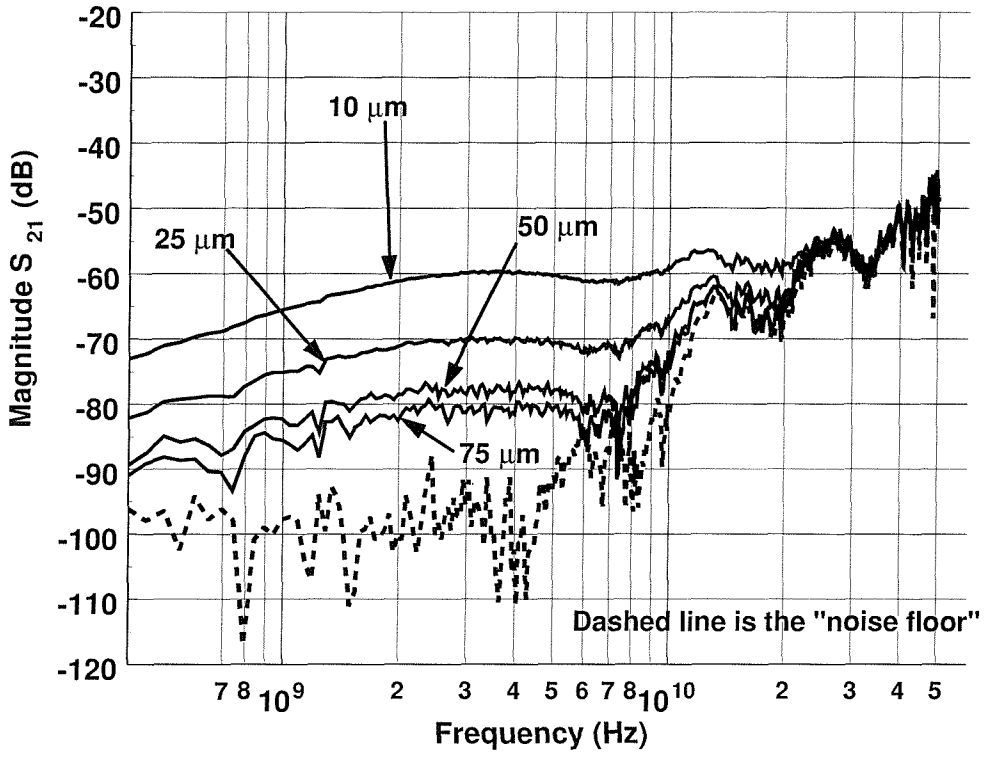


Figure 5.14: Measurement data from two coupled microstrip lines of 500 μm length, 10 μm width and variable spacing on an aluminum ground plane. The oxide thickness is 1 μm.

The loading effect is shown more clearly in Figure 5.15, where the oxide thickness is varied.

The additional capacitance of the probe pads that are used for the measurement of the coupled lines can be subtracted from the response by de-embedding with a suitable open structure. These structures were fabricated for all coupled microstrip lines and the measurement data of Figures 5.14 and 5.15 are shown after the de-embedding procedure in Figures 5.16 and 5.17 respectively. The de-embedding procedure involves converting all s-parameters to y-parameters and then subtracting the parameters of the open structure from the entire structure, before converting the resulting parameters to the s domain again.

The de-embedding procedure shifted the loading frequency to a higher point revealing that a slope of 20 dB per decade characterizes the coupling. There is also a slight artificial increase just before 10 GHz before the probe crosstalk dominates the response. The de-embedding procedure cannot remove the effect of probe crosstalk across the entire frequency range and also introduces artefacts when measured response and probe crosstalk have similar levels.

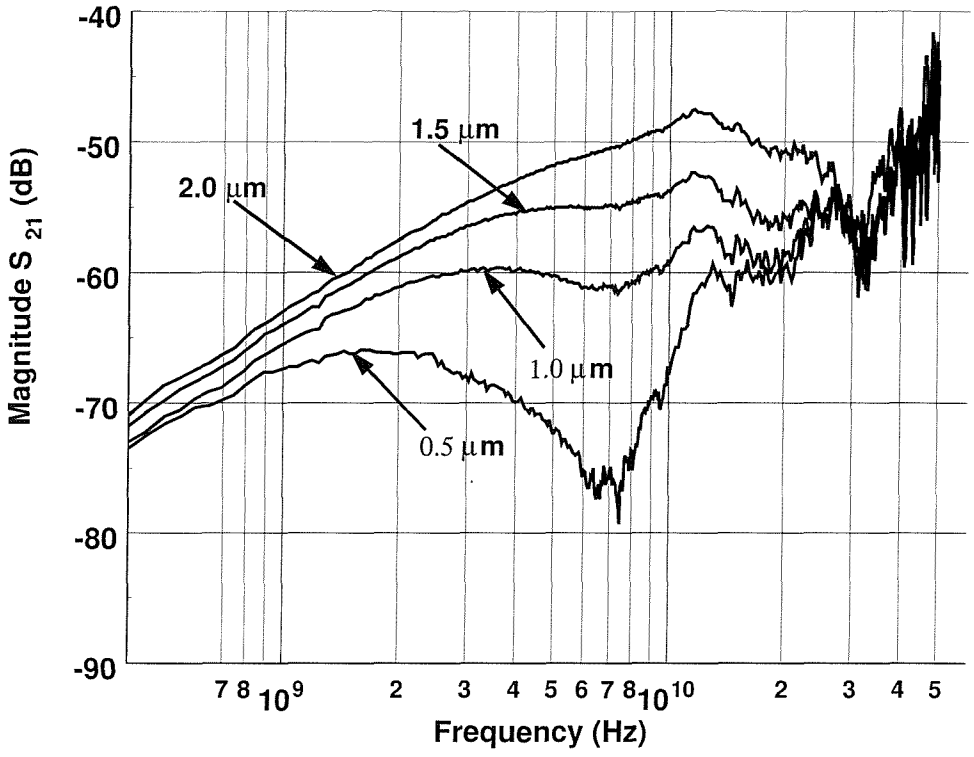


Figure 5.15: Measurement data from two coupled microstrip lines of 500 μm length, 10 μm width and variable oxide thickness on an aluminium ground plane. The separation is 10 μm.

The amount of coupling between the lines is stronger as the lines are closer to each other, but as the separation distance increases to high values (e.g. 75 μm), the coupling seems to saturate. In particular, increasing separation from 10μm to 25 μm results in a 10 dB loss of coupling. To achieve an additional 10 dB of decoupling, the lines have to be separated to 75 μm or an additional 50 μm, occupying a much larger area.

5.5.2 Coupled Microstrip Lumped Model Validation

Coupled microstrip lines on aluminium ground planes can be modelled by the capacitive π-network of Figure 5.7 that has been analysed in chapter four. The capacitances C_1 and C_2 represent the oxide capacitance of each line and the lateral capacitance through the air and oxide respectively. The measurement data presented in Figures 5.16 and 5.17 show clearly the 20 dB per decade slope of s_{21} as a function of frequency that is caused by C_2. By converting the measured s-parameters to y-parameters, the model parameters C_1 and C_2 can be extracted easily according to the following equations:

$$C_2 = -\frac{imaginary(y_{21})}{2 \cdot \pi \cdot f} \tag{5.1}$$

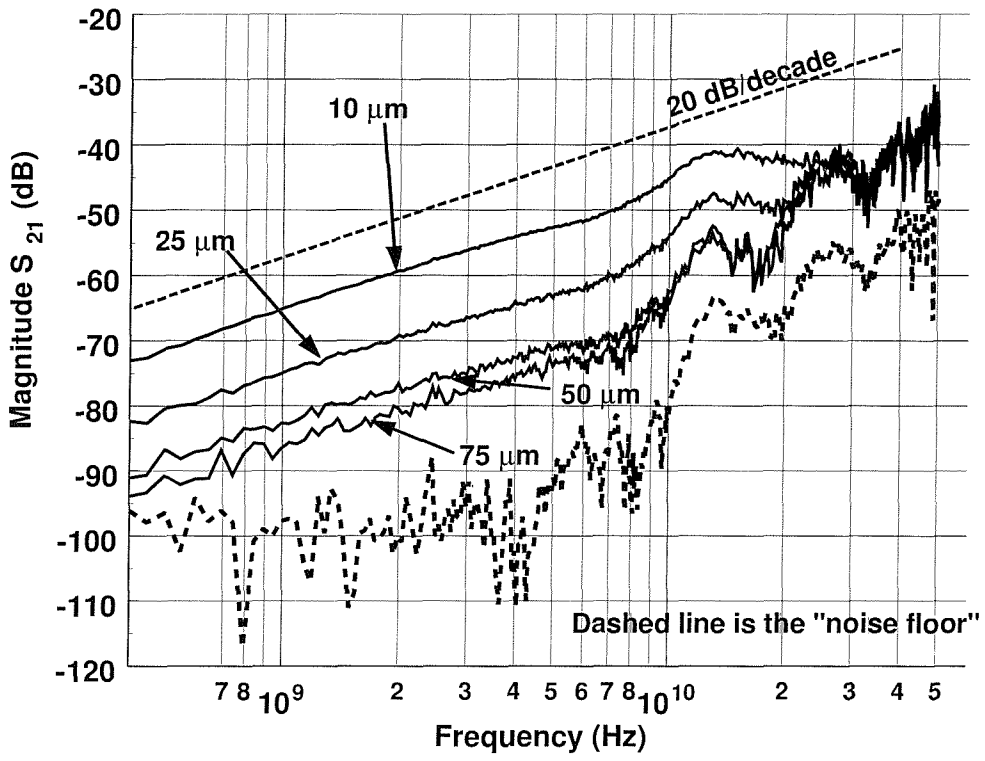


Figure 5.16: De-embedded measurement data from two coupled microstrip lines of 500 μm length, 10 μm width and variable spacing on an aluminum ground plane. The oxide thickness is 1.0 μm.

$$C_1 = \frac{imaginary(y_{11} - y_{21})}{2 \cdot \pi \cdot f} \tag{5.2}$$

Since the entire structure and therefore the model is symmetrical, y_{11}=y_{22} and y_{21}=y_{12}. The extracted values of C_1 and C_2 are presented in Table 5.1 and are compared with the values extracted by the analytical expressions (4.6) to (4.20) shown in chapter four.

S	C_1 (fF)			C_2 (aF)		
(μm)	Extracted	Analytical	Error (%)	Extracted	Analytical	Error (%)
10	209.9	201	4.24	895.6	2333.5	160.55
25	211.1	201.7	4.45	285.2	721.5	152.98
50	210.9	201.9	4.26	119.4	97.94	17.97
75	210.6	202	4.08	75.6	83.3	10.18

Table 5.1: Comparison of extracted (from measurements) and analytical (from equations (4.6) to (4.20)) model parameters for coupled microstrip lines of different spacing S, on 1.0 μm of oxide and aluminum ground plane.

The correlation between the studies of the buried ground plane crosstalk test structures and the microstrip lines is now clearly shown in Table 5.1. The analytical

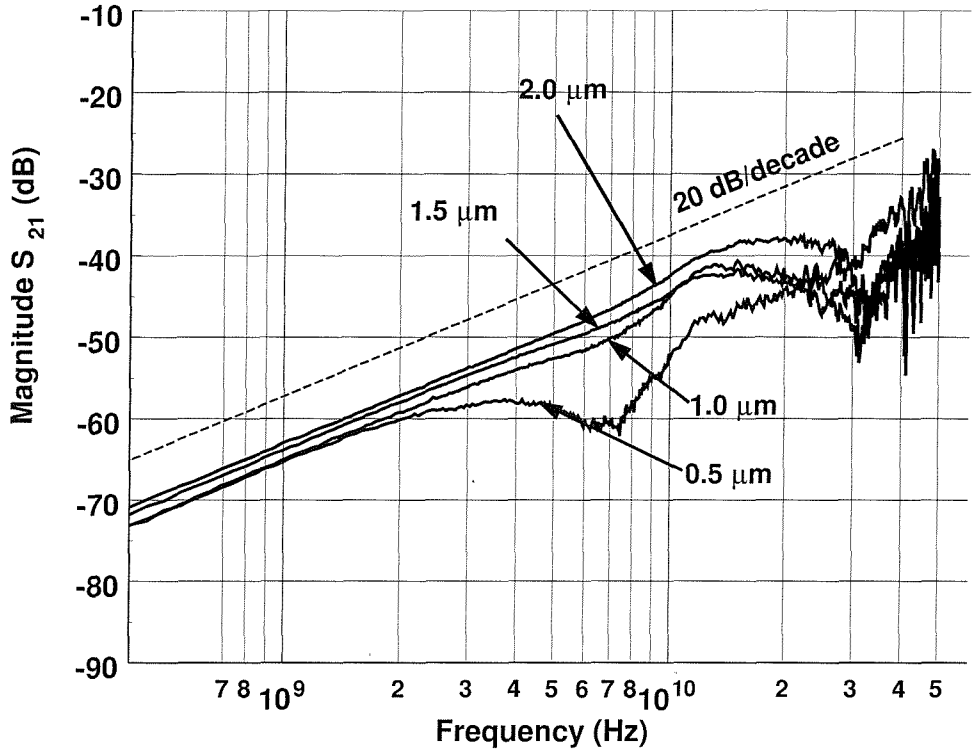


Figure 5.17: De-embedded measurement data from two coupled microstrip lines of 500 μm length, 10 μm width and variable oxide thickness on an aluminum ground plane. The separation is 10 μm.

expression of equations (4.6) to (4.20) manage to predict the value of C_1 with an accuracy of better than 5%, but exhibit the same error behaviour even when they are applied to very long microstrip lines.

The sources of error in the analytical expressions arise from the existence of empirical terms in the expressions that are only applicable to specific (usually small for coupled microstrip lines) S/H and W/H ratios, (where W is the width of the lines, S is the spacing between them and H is the thickness of the oxide). When substrate crosstalk in ground plane substrates is viewed as a coupled microstrip problem, the long line assumption is not applicable because the Tx/Rx pads are square. Additionally, even for the aforementioned coupled microstrip lines, the W/H and S/H ratios were very high (from 10 to 75 μm), resulting in very large oxide capacitances and therefore large, compared to the lateral coupling capacitance C_2, even (C_e) and odd (C_o) mode capacitances. Since the latter is derived by the subtraction of C_e and C_o, any error in their estimation is reflected in C_2, which has values an order of magnitude lower. For instance, an error of 5% in the value of C_1 is approximately 10 fF, which is significantly (approximately 10 times) higher than the maximum value of C_2 and can affect its accuracy. The complexity of estimating the exact values of the even and odd mode capacitances can also be highlighted by comparing the

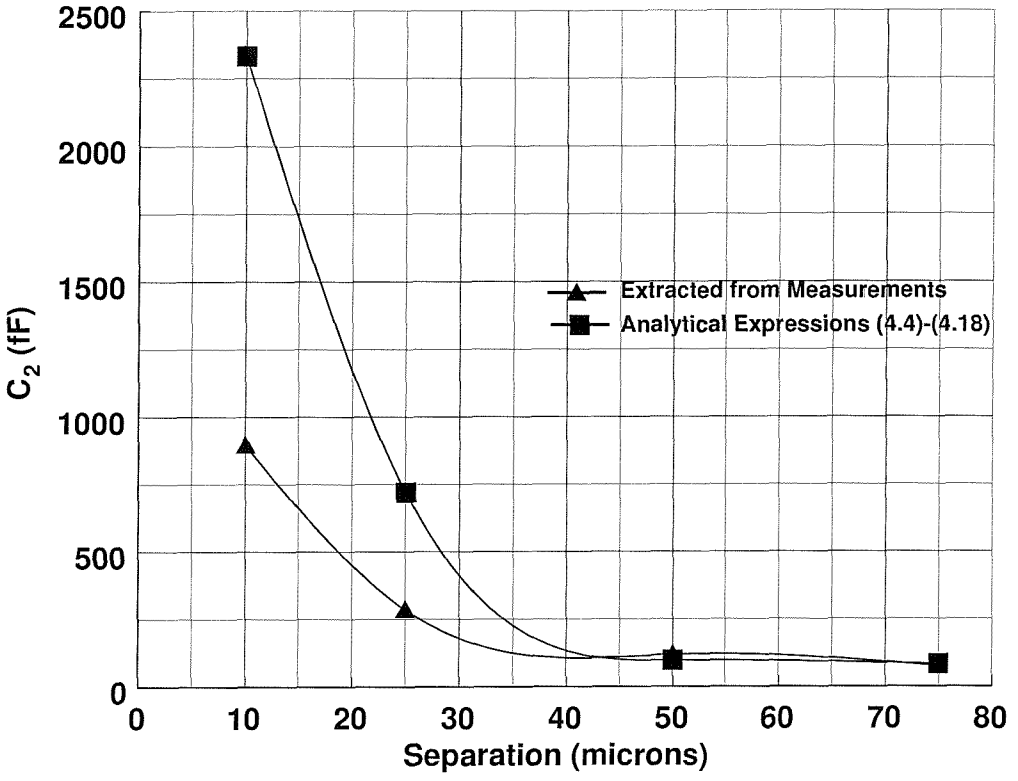


Figure 5.18: Comparison of values for C_2 extracted from measurements and the analytical expressions (4.6) to (4.20) for two coupled microstrip lines on 1.0 μm of oxide and aluminium ground plane and variable line spacing.

values of C_e and C_1 when a parallel plate formula is used for the calculation of the oxide capacitance. The oxide capacitance of a microstrip from the parallel plate formula is 177 fF where as the inclusion of the fringing fields around each line increase it to approximately 210 fF, an increase of 18%. The fringing fields are mainly responsible for the estimation of C_2 because they determine how many electric field lines are terminated on the other line rather than to ground. Although the vertical oxide capacitance, as estimated by a parallel plate formula, is the same for the even and odd cases and therefore is completly eliminated from the estimation of C_2, the fringing capacitances are not. Moreover, these fringing capacitances can only be estimated by empirical expressions running the risk of producing large errors.

5.5.3 Coupled Microstrip Lines on $TiSi_2$ (lossy) Ground Planes

Measurement data from coupled microstrip lines on $TiSi_2$ ground planes are shown in Figures 5.19 to 5.22. The de-embedded data are in agreement with the analysis of the square Tx/Rx pads at the beginning of this chapter.

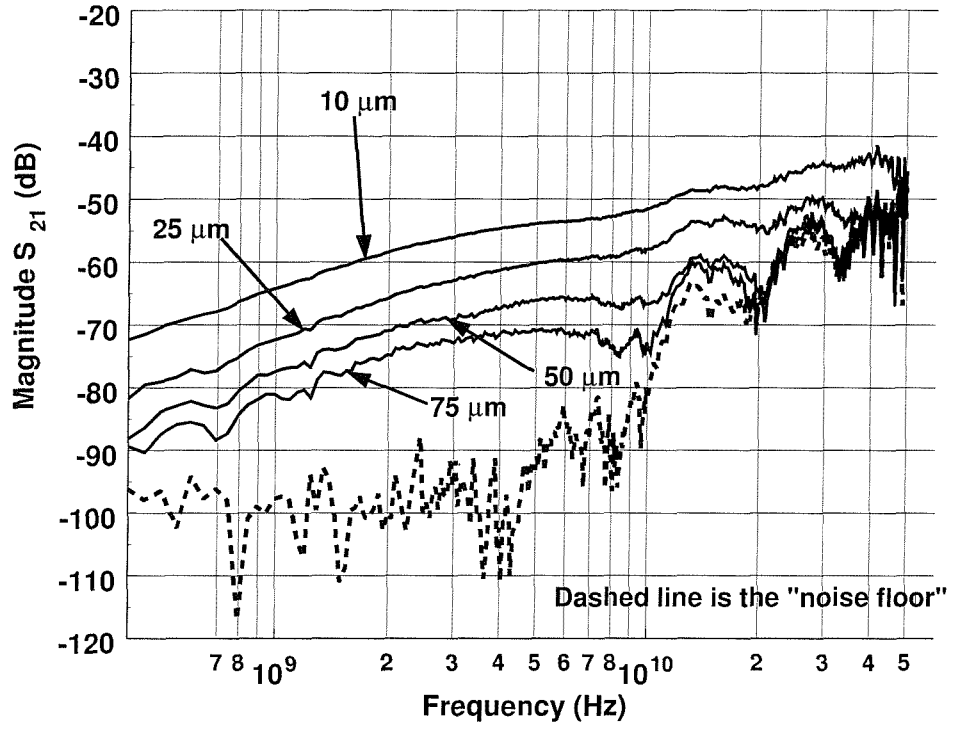


Figure 5.19: Measurement data from two coupled microstrip lines of 500 μm length, 10 μm width and variable spacing on a lossy $TiSi_2$ plane. The oxide thickness is 1.0 μm.

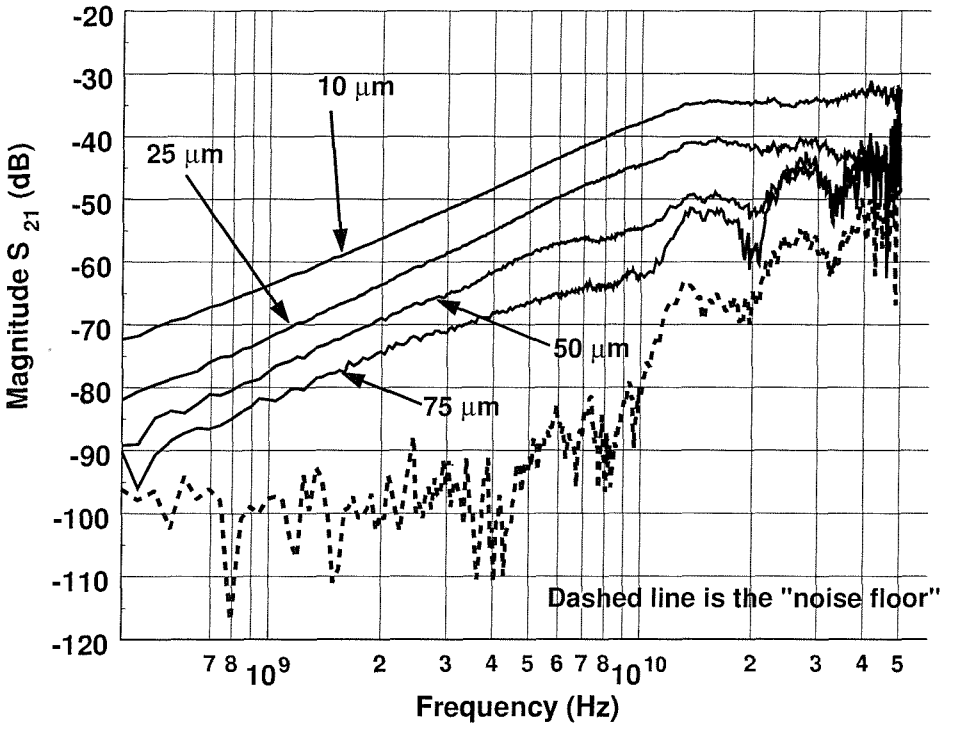


Figure 5.20: De-embedded measurement data from two coupled microstrip lines of 500 μm length, 10 μm width and variable spacing on a lossy $TiSi_2$ plane. The oxide thickness is 1.0 μm.

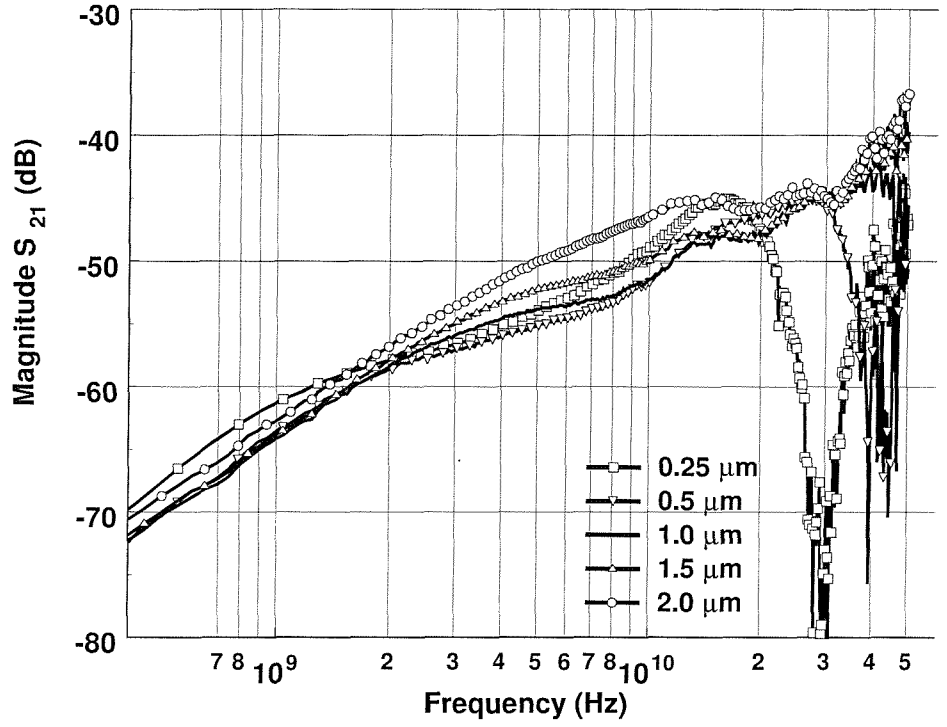


Figure 5.21: Measurement data from two coupled microstrip lines of 500 μm length, 10 μm width on a lossy $TiSi_2$ plane. The oxide thickness is varied from 0.5 μm to 2.0 μm and the line spacing is 10 μm.

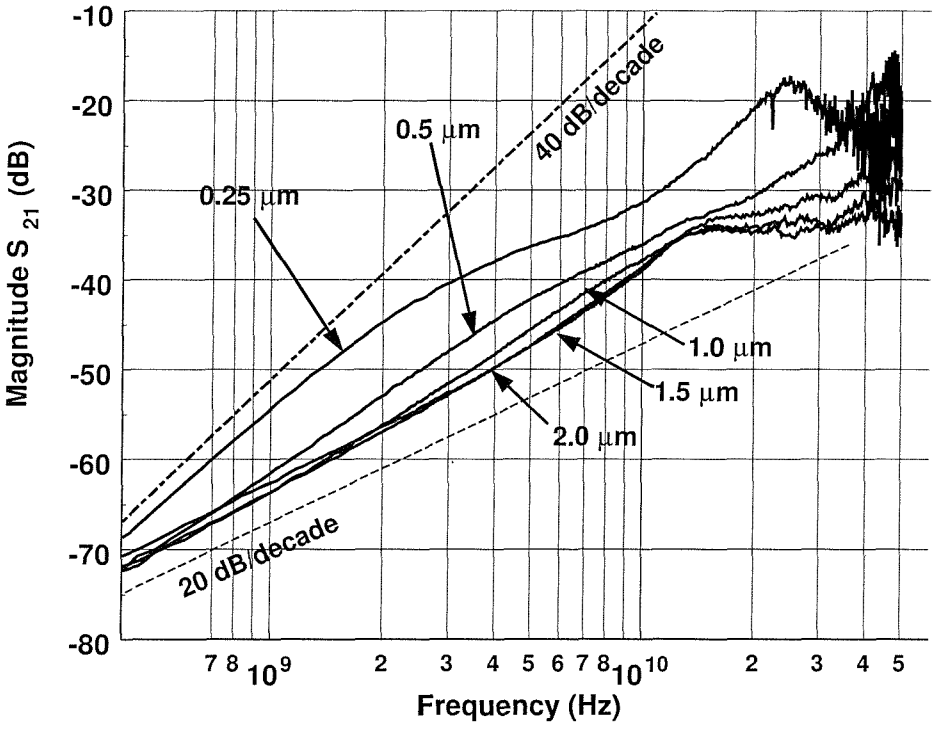


Figure 5.22: De-embedded measurement data from two coupled microstrip lines of 500 μm length, 10 μm width on a lossy $TiSi_2$ plane. The oxide thickness is varied from 0.25 μm to 2.0 μm and the line spacing is 10 μm.

5.6 Conclusions

This chapter investigated the effect of the oxide thickness and the ground plane resistivity in buried ground plane substrates, Pseudo-ground plane test structures similar to those presented in chapters 3 and 4 were fabricated and measured. The term pseudo-ground plane is used because the fabrication involved a standard two-metal layer process for the buried metallic plane and the coplanar structure at the surface. A pseudo-ground plane substrate cannot be used to form a GPSOI substrate, but it yields the same behaviour as the WSi_2 buried ground plane substrate of chapters 3 and 4. Aluminium and $TiSi_2$ ground planes were considered. The latter was forced by the unavailability of WSi_2 processing to the author but had a resistivity close to WSi_2. The loading frequency of the s_{21} response of all structures was decreased as the oxide thickness increased. The choice of two different ground planes, in conjunction with the oxide thickness variation, revealed two different regimes of low frequency operation. Thinner oxides on aluminium ground planes does not affect significantly the level of crosstalk at low frequencies, but only affect the loading frequency that may define a valid operational frequency range for the model and the entire structure. On the other hand, thinner oxides on a lossy $TiSi_2$ ground plane revealed an opposite trend by increasing the level of crosstalk, while also decreasing the ac loading frequency resulting in worse overall isolation behaviour. Electromagnetic simulations were employed to show that an optimum oxide thickness exists where the lowest level of crosstalk occurs.

Finally, experimental measurement results from coplanar coupled microstrip lines fabricated on both aluminium and $TiSi_2$ ground planes were presented. The increased length of the microstrip lines allowed higher degrees of coupling to be measured and visualised much more clearly because their response lay further away from the measurement noise-floor. At the same time, these experiments verified the correlation between coupled microstrip and substrate crosstalk models, as both cases exhibited similar dynamic behaviour.

The accuracy of a substrate crosstalk model depends largely on the accuracy of microstrip coupled line models. The coupled microstrip model presented in these studies is only valid for certain values of line spacing. Its validity range can be extended by introducing additional empirical terms or by resorting to fully empirical expressions. Such a methodology, however, reduces the modelling effort to a purely mathematical, functional approximation problem and requires additional experimental data.

Chapter 6

A Substrate Crosstalk Analysis Of Silicon-On-Insulator (SOI) Substrates

6.1 Introduction

Mixed signal RF integration demands high isolation requirements that cannot be met by bulk CMOS processes. According to the 2001 edition of the International Technology Roadmap for Semiconductors (ITRS) [35], "Silicon-On-Insulator SOI technologies will be one key solution in obtaining high signal isolations and low parasitic capacitance values". SOI processes and substrates are already being utilised in production and they are expected to dominate in mixed signal RF applications. This chapter analyses substrate coupling in SOI substrates and provides compact lumped element models that may be used for accurate and fast circuit level simulation. Electromagnetic modelling and simulation of the substrate coupling is also included and coupled strip line theory is utilised in order to provide accurate closed form expressions that can allow prediction of the model parameters. The work presented here also serves as a bridge between the crosstalk studies of buried ground planes presented in the previous chapters and Ground Plane SOI (GPSOI) substrates that follows in Chapter 7.

6.2 Substrate Coupling in Bulk Silicon Substrates

Since a SOI substrate consists of two Si layers of different doping (and hence resistivity) separated by the buried insulator layer (silicon dioxide SiO_2), it is important to consider firstly the case of substrate coupling in bulk Si substrates. Figure 6.1 shows a cross-sectional view of a SOI substrate. Two coupling paths exist through the Si active layer and the silicon substrate (handle substrate). The problem can then be partitioned into two different substrate configurations, each representing a

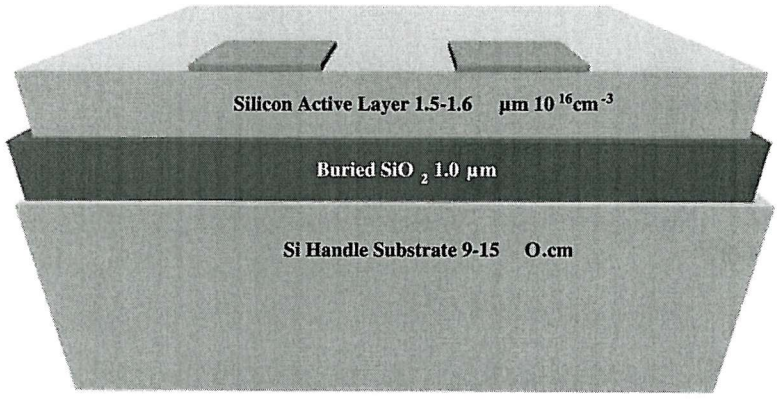


Figure 6.1: Cross-sectional view of the SOI substrate.

coupling path. Hence, it is essential to analyse and initially understand the simplest case of a bulk Si substrate and the crosstalk effects associated with it, before moving further and determining how the two coupling paths interact with each other.

The nature of the coupling between two points or two conductors on a silicon substrate is determined primarily by the physical properties of silicon itself. The dielectric permittivity of silicon is responsible for the amount of capacitive coupling. Capacitive coupling also exists through the air although its contribution to the total coupling is much smaller due to the (approximately twelve times) smaller permittivity of air. The finite resistivity of silicon accounts also for the conductive coupling through a silicon layer.

The substrate coupling between two zero thickness conductors on a silicon substrate can be represented by the RC network of Figure 6.2, where R_{SUB} and C_{SUB} model the conductive and capacitive nature of the coupling path. [36] and [15] have shown that the relation ship between R_{SUB}, C_{SUB} and the permittivity ε_{SI} and resistivity ρ_{SUB} of the silicon substrate is :

$$R_{SUB} \cdot C_{SUB} = \varepsilon_{SI} \cdot \rho_{SUB} \tag{6.1}$$

This relationship is important because it reveals a major limitation of bulk Si substrates. A simple analysis of the equivalent RC model of Figure 6.2 shows that the s_{21} characteristic defines a cut off frequency f_C for the substrate, which is given by the following relation:

$$f_C = \frac{1}{2 \cdot \pi \cdot (R_{SUB} \cdot C_{SUB})} = \frac{1}{2 \cdot \pi \cdot (\varepsilon_{SI} \cdot \rho_{SUB})} \tag{6.2}$$

Electromagnetic simulation can be used to verify equation (6.2) and show the effect of the substrate resistivity on the absolute level of crosstalk (i.e. magnitude

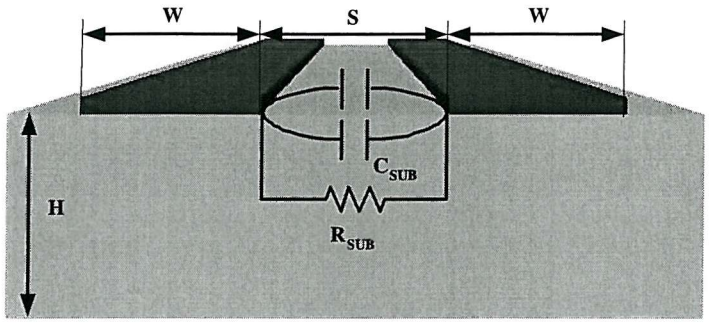


Figure 6.2: Substrate coupling lumped model for two zero thickness conductors on a silicon substrate.

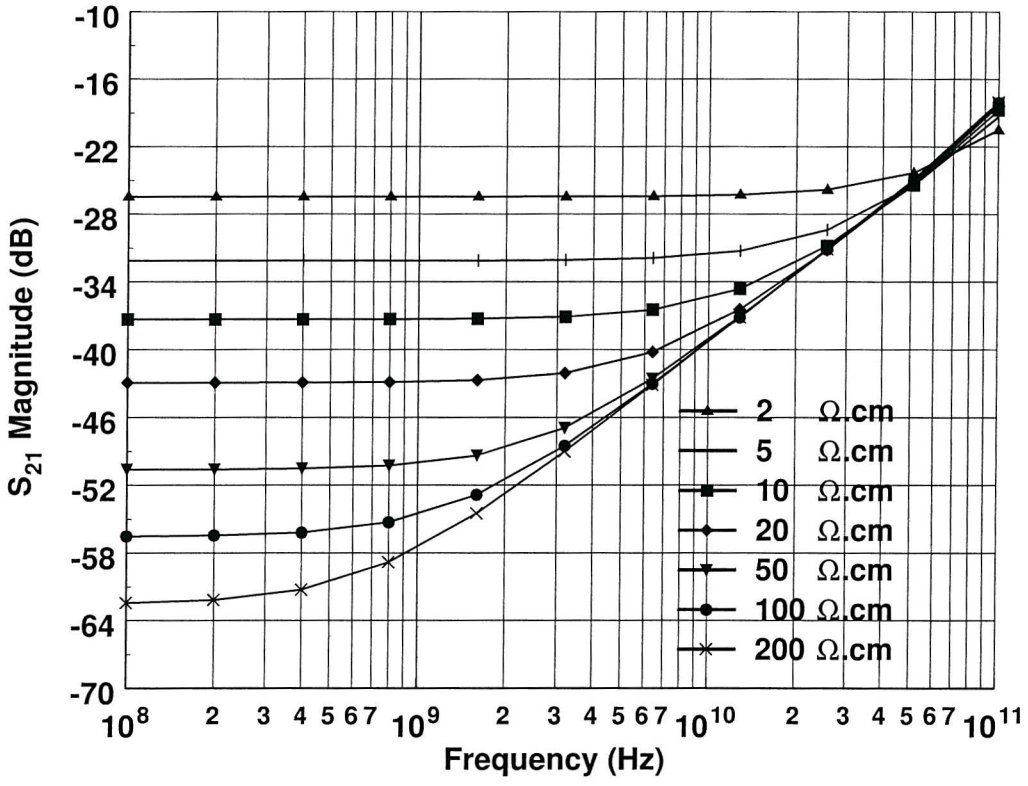


Figure 6.3: Magnitude of s_{21} (dB) versus frequency for various substrate resistivity values of two square metal pads (50×50 μm^2) of zero thickness on a very high thickness Si substrate.

of s_{21}) and the cut off frequency. Figure 6.3 shows the effect of the substrate resistivity (that is controlled by the doping of the substrate) on s_{21} over a certain frequency range (0.1 to 100 GHz). These results were generated by *EM-Sight* for two zero thickness square pads (50 μm $\times$50 μm) of perfect (zero thickness, infinite conductivity) metal on a silicon substrate with variable resistivity (5, 10, 20, 50, 100, 200 Ω.cm).

Careful observation of Figure 6.3 reveals several characteristics that can lead to useful conclusions about isolation in bulk Si substrates. Firstly, low frequency crosstalk is constant as a function of frequency for a given value of the substrate resistivity. This is an indication that low frequency crosstalk is dominated by the resistive component of the lumped model R_{SUB}. As frequency increases crosstalk remains constant until it reaches a specific frequency. Above that frequency, which has been defined in (6.2) as the cut off frequency, it increases at a rate of approximately 20 dB per decade. As the frequency increases towards the cut-off frequency, the capacitive part of the coupling becomes more significant and finally dominates the s_{21} response. The slope of increase of s_{21} can be analytically shown to be 20 dB per decade due to a zero at the cut off frequency.

Another point worth mentioning is the trade off between the cut off frequency of the substrate and the absolute level of crosstalk (magnitude of s_{21}). The cut off frequency defines a frequency range (or high isolation bandwidth), where crosstalk is constant and lower than the levels of crosstalk at higher frequencies. High resistivity substrates result in higher values of R_{SUB} and hence, lower crosstalk. At the same time, the cut off frequency of the substrate decreases considerably and crosstalk begins to increase at a lower frequency reducing the high isolation bandwidth. In other words, high isolation bandwidth is sacrificed for lower levels of crosstalk at lower frequencies.

The values of R_{SUB} and C_{SUB} can be extracted from electromagnetic simulations by measuring the parameter y_{21}:

$$R_{SUB} = \frac{-1}{real(y_{21})} \tag{6.3}$$

$$C_{SUB} = \frac{-imaginary(y_{21})}{2 \cdot \pi \cdot frequency} \tag{6.4}$$

6.3 Substrate Coupling in SOI Substrates

SOI substrates have a thin silicon active layer on top of a buried insulator layer, usually SiO_2. Below the oxide, bulk silicon forms the handle wafer. Devices and circuitry are integrated on the active layer, which for this work has a doping of 10^{16} cm^{-3} (i.e. 0.5 Ω.cm). The handle wafer may have a resistivity of 9-15 Ω.cm or higher (200 Ω.cm). Assuming that the same two noise transmitter and receiver pads mentioned in the previous paragraph for the bulk Si substrate now lie on a SOI, one can identify two coupling paths though each silicon layer as shown in Figure 6.4. These two paths are dc isolated from each other but may be capacitively coupled to each other through the buried oxide. The significantly lower resistivity of the

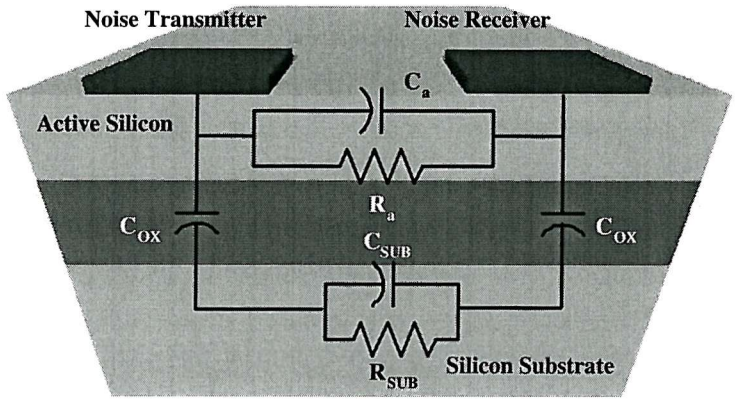


Figure 6.4: SOI substrate and substrate crosstalk model of two pads lying on this substrate.

silicon active layer compared to the handle substrate (approximately 20 times for the standard 9-15 Ω.cm case) indicated that the coupling path through the active layer tends to dominate over the path through the substrate. Also the active layer is the surface of the substrate, where the coupling is strongest and the amount of noise penetration vertically through the buried oxide to the handle substrate is expected to be small. Furthermore, the propagation of noise signals that have reached the handle substrate will also be determined by its resistivity.

Based on this mostly qualitative analysis of the noise coupling, a model can be developed for SOI substrate crosstalk structures, which is shown in Figure 6.5. The capacitive and conductive coupling properties of the active layer are represented by the RC network of R_a and C_a in the same manner as they were described in the previous section. Similarly, R_{SUB} and C_{SUB} now account for the coupling through the handle substrate. The two paths interact with each other through vertical capacitances C_{BOX} associated with the buried oxide layer. As in the case of the bulk Si substrate, it is assumed that the lateral capacitive coupling through the remaining layers (i.e. the air and the buried oxide) is negligible compared to that through the silicon layers.

6.4 Parameter Extraction in SOI Substrates

Unlike the model presented in the previous section about bulk Si substrates, the element extraction for the SOI substrate coupling is not easy due to the existence of the two coupling paths. In order to facilitate the analysis of the model, a high resistivity handle substrate may be initially considered. In that case $R_{SUB} \gg R_a$ and the equivalent circuit of Figure 6.5 becomes that of Figure 6.6.

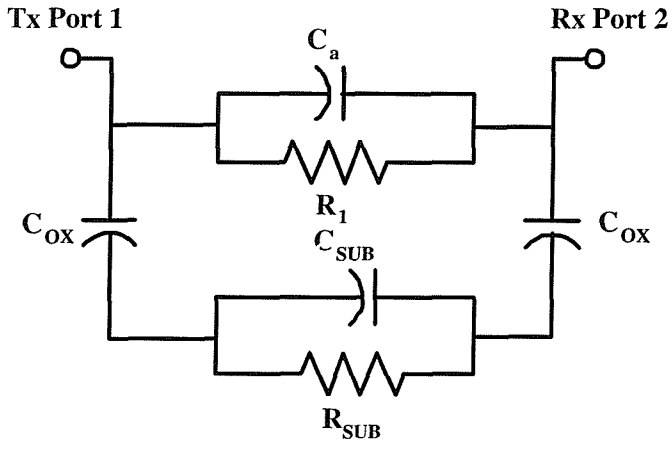


Figure 6.5: Equivalent circuit of the SOI substrate crosstalk model.

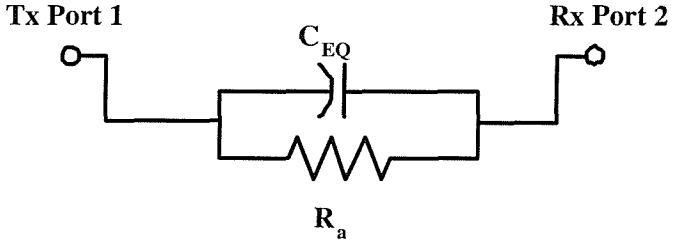
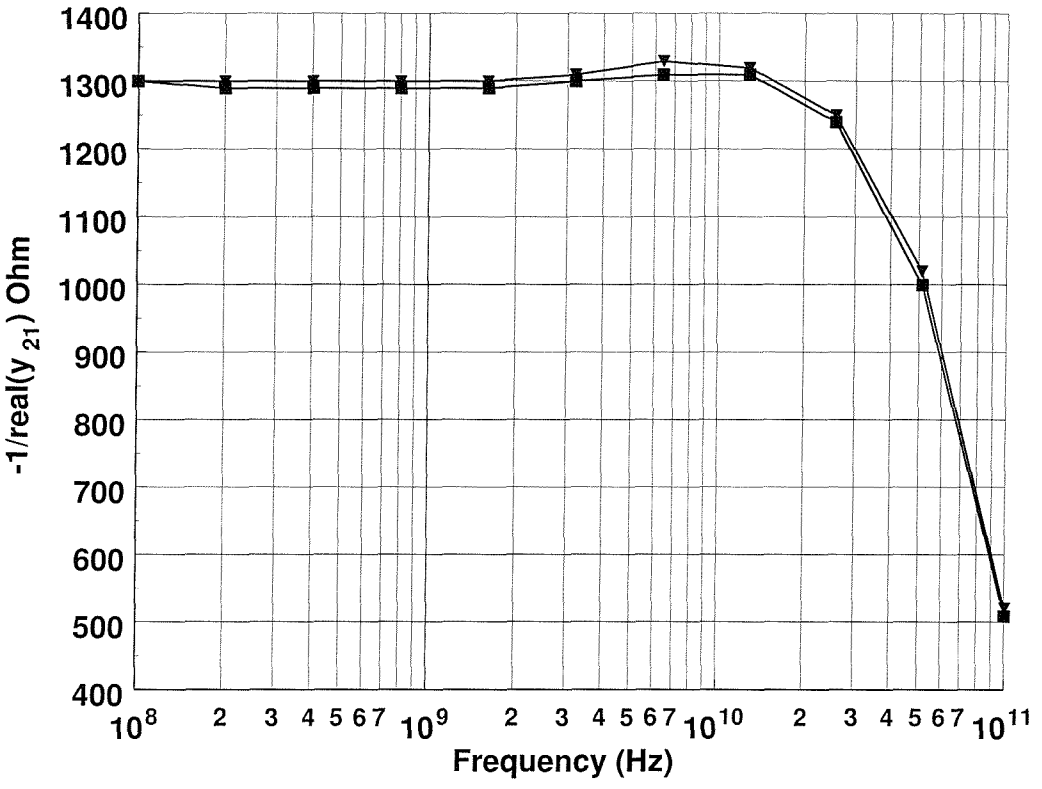


Figure 6.6: Equivalent circuit of a crosstalk model for a SOI substrate with a handle substrate of very high resistivity compared to the active layer.

The capacitance C_{EQ} is the equivalent combination of C_{BOX} and C_{SUB}. For the latter model it is now easy to extract the the resistance and equivalent capacitance using (6.4) and (6.5). In practice, $C_{BOX} \gg C_{SUB}$ and C_a, therefore C_{EQ}=C_a+C_{SUB}. The equivalent capacitance C_{EQ} of the model, in the case of the high resisitivity handle substrates, accounts for the entire lateral coupling through the active silicon layer and the handle substrate.

Although considering a high resistivity SOI handle simplifies considerably the topology of the coupling model, the parameter extraction still remains difficult because of the finite resistivity of the handle. In the ideal case where R_{SUB} is infinite the above analysis is valid and R_a, C_{EQ} can be extracted from (6.3) and (6.4). The finite resistivity however, results in R_a and C_{EQ} being functions of frequency when they are calculated from (6.5) and (6.6). Figure 6.7 shows the imaginary and real parts of y_{21} versus frequency for a SOI substrate with a finite (200 Ω.cm) high resistivity handle substrate. The data shown are generated by *EM-Sight* for two square (50×50 μm_2) zero thickness pads on a high resistivity SOI substrate and an infinite resistivity handle substrate.



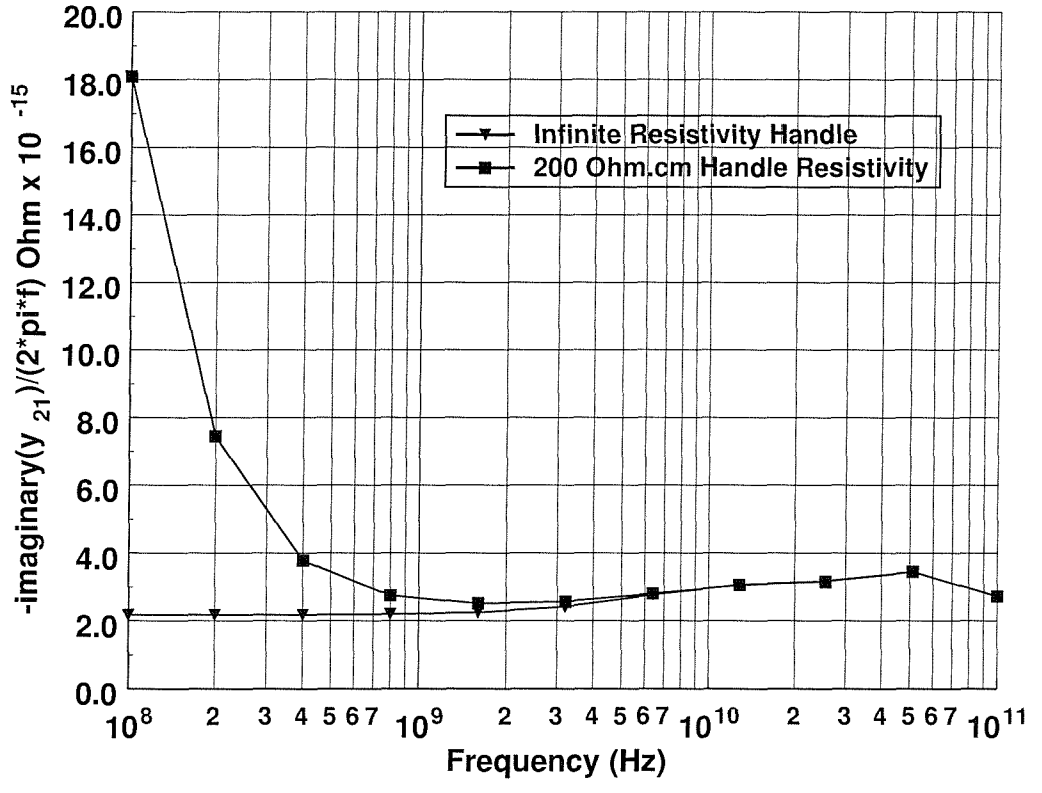


Figure 6.7: Real part of y_{21} as a function of frequency for two zero thickness square pads on a SOI substrate with high (200 Ω.cm)(top) and infinite resistivity handle (bottom). Active layer doping is 10^{16} cm^{-3}.

The imaginary part of y_{21} that is used in (6.4) to extract the lateral capacitive coupling is affected in such way that C_{EQ} has to be extracted at high frequencies. This is not at all practical because at high frequencies the distributed nature of the coupling is more pronounced and y_{21} may vary significantly over a certain frequency range not allowing a single value of y_{21} to be extracted but a set of values. A solution for this problem may be the acquisition of an average value over a certain frequency span where y_{21} appears to become constant. As a result of such solution, the accuracy of the extraction procedure is compromised.

Verification of the above can be achieved by analytically calculating y_{21} from the equivalent circuits of Figures 6.5 and 6.6. The following expressions show the real and imaginary parts of y_{21} as functions of the model elements R_a, R_{SUB}, C_a, C_{SUB}, C_{BOX} and the frequency f.

$$\begin{aligned} R_{SUB} &= real(y_{21}(\omega)) = \\ &= G_a - 2\cdot\omega^2\cdot C_{OX}\cdot C_{SUB}\cdot\frac{G_{SUB}}{4\cdot G_{SUB}^2+(2\cdot\omega\cdot C_{SUB}+\omega\cdot C_{OX})^2}+ \\ &\quad +\omega\cdot C_{OX}\cdot G_{SUB}\cdot\frac{2\cdot\omega\cdot C_{SUB}+\omega\cdot C_{OX}}{4\cdot G_{SUB}^2+(2\cdot\omega\cdot C_{SUB}+\omega\cdot C_{OX})^2} \end{aligned} \tag{6.5}$$

where $G_a=\frac{1}{R_a}$,$G_{SUB}=\frac{1}{R_{SUB}}$ are the admittances of R_a and R_{SUB} and $\omega = 2\cdot\pi\cdot frequency$

$$\begin{aligned} C_{SUB} &= \frac{imaginary(y_{21}(\omega))}{\omega} = \\ &= C_a + 2\cdot C_{OX}\cdot\frac{G_{SUB}}{4\cdot G_{SUB}^2+(2\cdot\omega\cdot C_{SUB}+\omega\cdot C_{OX})^2}+ \\ &\quad +\omega\cdot C_{OX}\cdot G_{SUB}\cdot\frac{2\cdot\omega\cdot C_{SUB}+\omega\cdot C_{OX}}{4\cdot G_{SUB}^2+(2\cdot\omega\cdot C_{SUB}+\omega\cdot C_{OX})^2} \end{aligned} \tag{6.6}$$

Figure 6.8 depicts plots of (6.5) and (6.6) as functions of frequency after values were estimated for the model elements. The frequency dependence is obvious in both the real and imaginary parts. In the case of the real part that is used to extract the conductive coupling, the variation is insignificant and the value of R_a can be extracted with a practically negligible error. However, in the case of the imaginary part used to extract C_{EQ}, it can be observed that the line converges to the expected value of C_{EQ} only at high frequencies. High frequency measurements and simulations may not be reliable as they are sensitive to noise and may be dominated by distributed effects.

The extraction procedure discussed in this section identifies potential problems that may occur when the parameters of a SOI substrate coupling model are extracted

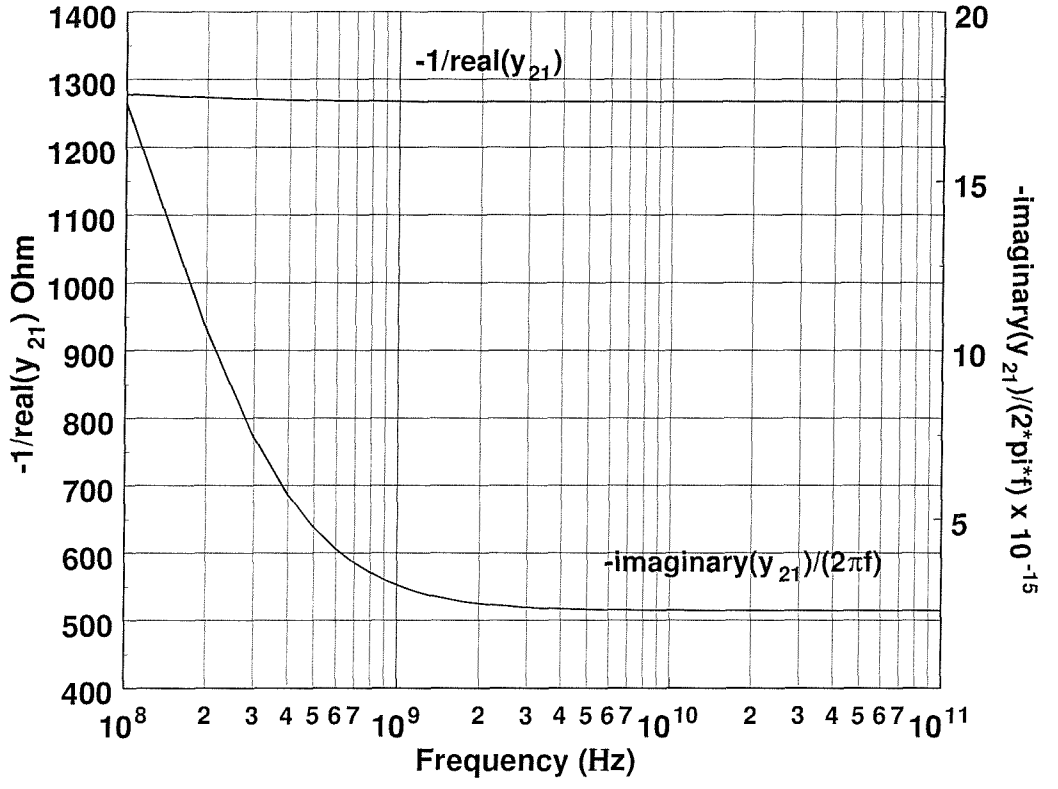


Figure 6.8: Real and Imaginary parts of y_{21} as extracted from (6.5) and (6.5).

from y_{21} measurements. It has to be noted that these problems become worse as the resistivity of the handle substrate becomes lower and closer to typical values of 9-15 Ω.cm. In standard resistivity SOI substrates the coupling path through the handle substrate becomes more significant and the model of Figure 6.5 cannot be transformed to the simplified equivalent model of Figure 6.6. Hence, the model parameters cannot be extracted directly from (6.3) and (6.4), since y_{21} is given by the complicated expressions of (6.5) and (6.6). In addition, as it has been previously discussed in Chapter 3 of this work, substrate coupling is a distributed effect and it is not easy to identify paths that can be easily modelled by lumped components.

6.5 Model Parameter Prediction

Although the equivalent model parameters can be extracted from electromagnetic simulation data and measurements, ideally closed form expressions could be used to predict their value and reduce design and simulation times. As in the case of the square metal pads on insulator on ground planes described in Chapter 3, empirical formulae that fully describe substrate crosstalk can be derived at the expense of valuable insight into the physical properties, origin and behaviour of those parameter expressions. Furthermore, fully empirical expressions are only applicable for a

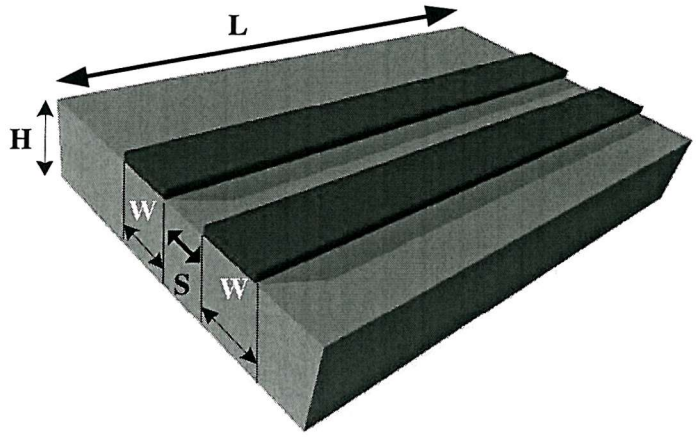


Figure 6.9: Symmetrical double-strip coplanar waveguide on a substrate with finite thickness.

certain range of parameters and frequencies. On the other hand, applying established and well-researched theory into the substrate coupling problem provides a deeper and better understanding and most of the times can be applicable to wider parameter and frequency ranges or in other words. Also, the model scaling is easier since it is built into the model, whereas in the empirical expressions exhaustive testing has to be performed.

6.5.1 The Symmetrical Double-Strip Coplanar Waveguide Problem

Substrate coupling between two pads or conductors on a silicon substrate can be related to the study of the coupling properties of a symmetrical double-strip coplanar waveguide on a silicon substrate of finite thickness. As shown in Figure 6.9 a symmetrical double-strip coplanar waveguide is composed of two strip transmission lines of the same width W and separation S on a substrate of relative permittivity μr and thickness H. The capacitive coupling between the two lines can be calculated from the method of superposition of partial capacitances [33]. According to this method the capacitance between the two lines is the sum of two capacitances:

$$C = C_o + C_e \tag{6.7}$$

where C_o is the capacitance when the dielectric is replaced with air (Figure 6.10a) and C_e is the capacitance of the equivalent circuit with magnetic walls at the dielectric border and a relative permittivity of $\varepsilon_r - 1$, shown in Figure 6.10b. No electric field lines exist outside the boundaries of the substrate.

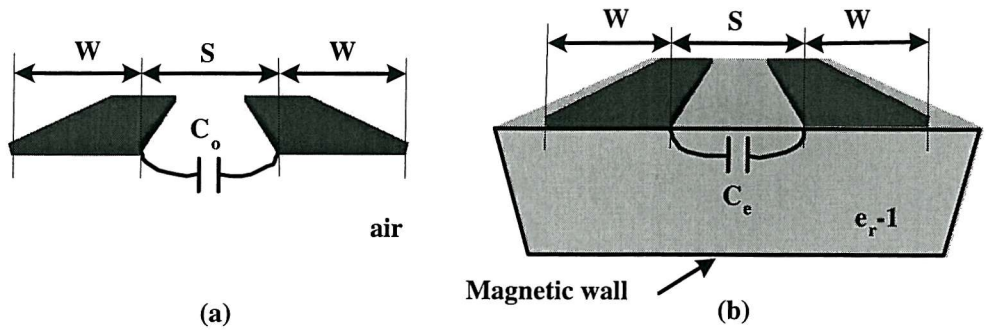


Figure 6.10: Partial capacitances for coupling capacitance calculation in the double-strip coplanar waveguide problem.

Unlike the coupled microstrip problem, described in Chapter 3, where the existence of a ground plane prohibits that analytical solution of this problem, analytical expressions that evaluate the coupling capacitance C have been developed from conformal mapping techniques [33], [30].

$$C_o = \varepsilon_0 \cdot \frac{K(k')}{K(k)} \tag{6.8}$$

$$C_e = \varepsilon_0 \cdot (\varepsilon_r - 1) \cdot \frac{K(k_1')}{2 \cdot K(k_1)} \tag{6.9}$$

where

$$k_1 = \frac{\tanh\left(\frac{\pi \cdot s}{4 \cdot h}\right)}{\tanh\left(\frac{\pi \cdot d}{4 \cdot h}\right)} \tag{6.10}$$

$$k_1 = \sqrt{1 - k_1^2} \tag{6.11}$$

and $K(k_1')$ is the complete elliptic integral of the first order and can be computed either numerically or approximated by the following expressions:

$$\frac{K(k')}{K(k)} = \frac{4}{\pi} \cdot \ln 2\sqrt{k} \; for \; 0 < k \leq 0.173 \tag{6.12}$$

$$\frac{K(k')}{K(k)} = \frac{\pi}{\ln\left(2 \cdot \frac{1+\sqrt{k}}{1-\sqrt{k}}\right)} \; for \; 0.173 < k \leq 1 \tag{6.13}$$

6.5.2 Application to SOI Substrate Crosstalk

The aforementioned symmetrical double-strip coplanar waveguide theory can be utilised to model the substrate coupling through the two silicon layers, the active layer on the surface and the handle substrate. Figure 6.11 shows how the substrate

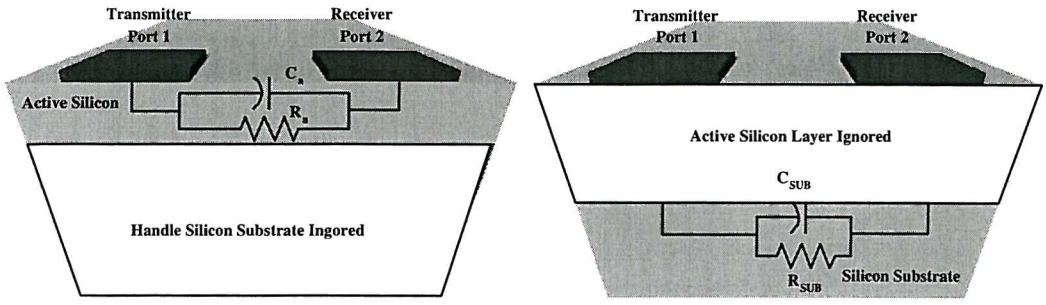


Figure 6.11: Two configurations for the derivation of the two coupling models through the silicon layers.

can be partitioned so that the previous single layer formulae can be applied to each coupling path.

The coupling through the active silicon layer can be considered to be as the capacitive coupling between two coplanar strip waveguides of equal width on a silicon substrate with a finite thickness equal to that of the SOI layer (typically 2 μm). In other words, the oxide of the SOI and the handle substrate are completely ignored at this face and using (6.7) to (6.14), the coupling capacitance can be determined as in the case of a symmetrical double strip waveguide on a finite thickness substrate. For this case, only the silicon layer and the air above it are considered and the results include the capacitive coupling through both the silicon layer and the air.

The capacitive coupling through the handle substrate could be modelled in a similar way, but given now that the thickness of the handle substrate is much larger than that of the active layer (typically 525 μm), equations (6.7) to (6.14) will now approximate the case of the double-strip coplanar waveguide on an infinite thickness substrate case. Following the entire procedure of the partial capacitance method can now prove to be more problematic. If the silicon handle substrate is considered along with the oxide above it as a pair, in the same way as the active layer and the air above it were considered, the assumptions and the conclusions drawn in the analysis of bulk silicon substrate coupling would be violated. As shown in (6.7), the total capacitance consists of C_o and C_e. If the pair of the handle substrate and the oxide above is considered, then C_o would be the coupling capacitance if the entire space is filled with oxide. This is undesirable because the oxide thickness is finite and small compared to the lateral separation between the pads. The relatively thin oxide (1 μm) allows for significant vertical (parallel plate) capacitances C_{BOX} but no lateral capacitances because the lateral coupling is mostly assumed to be through the silicon layers above and below it. The lateral coupling through the

oxide is assumed weak because it only has a capacitive nature and no ohmic that dominates the lower and middle frequency range. On the other hand, C_e is now defined in a similar manner as in the active layer case and is equal to the total coupling through the handle substrate if there is no field outside the boundaries. The substrate permittivity is now equal to that of silicon rather than $(\varepsilon_r - 1)$ because C_o is now ignored. Hence the total capacitive coupling through the silicon handle substrate is described by the following expression:

$$C_{SUB} = \varepsilon_0 \cdot (\varepsilon_r) \cdot \frac{K(k_1')}{2 \cdot K(k_1)} \tag{6.14}$$

It is worth noticing that substrate coupling in SOI substrates is a multilayer and therefore multidimensional problem. Utilising what effectively is a single layer approach is a compromise that intends to approximate the substrate's coupling behaviour but at the same time attempts to avoid oversimplification that may lead to significant errors. It must be noted that the aforementioned partitioning of the problem is based on the assumption that the resulting equivalent model consists of linear components. Linearity allows the superposition of the equivalent coupling models through each silicon layer.

6.5.3 Calculation of Conductive Coupling

Once the capacitive coupling properties have been determined, the conductive nature of the coupling may also be evaluated from the above formulas by taking into account that silicon is a lossy dielectric. Therefore its permittivity can be replaced by a complex value ε^* that relates its actual permittivity ε_r with its conductivity ρ and the frequency f. This concept has been utilised by [1], [37], where initially the complex admittance is calculated based on the capacitance expressions.

For both active silicon layers, it is sensible to derive the conductance only from C_e, the part of the capacitance that is associated with the substrate and not C_o, which is a capacitance through air, whose conductance should be zero.

$$Y_a = j \cdot \omega \cdot C_e = j \cdot \omega \cdot \varepsilon_0 \cdot (\varepsilon_r^*) \cdot \frac{K(k_1')}{2 \cdot K(k_1)} \tag{6.15}$$

Then the imaginary and real part of the admittance will give the capacitance (that is already known) and some conductance related to the conductivity of the silicon layer. As with the capacitances, all expressions give per unit length values.

$$R_a^1 = real(Y_a) = \sigma \cdot \frac{K(k_1')}{2 \cdot K(k_1)} \tag{6.16}$$

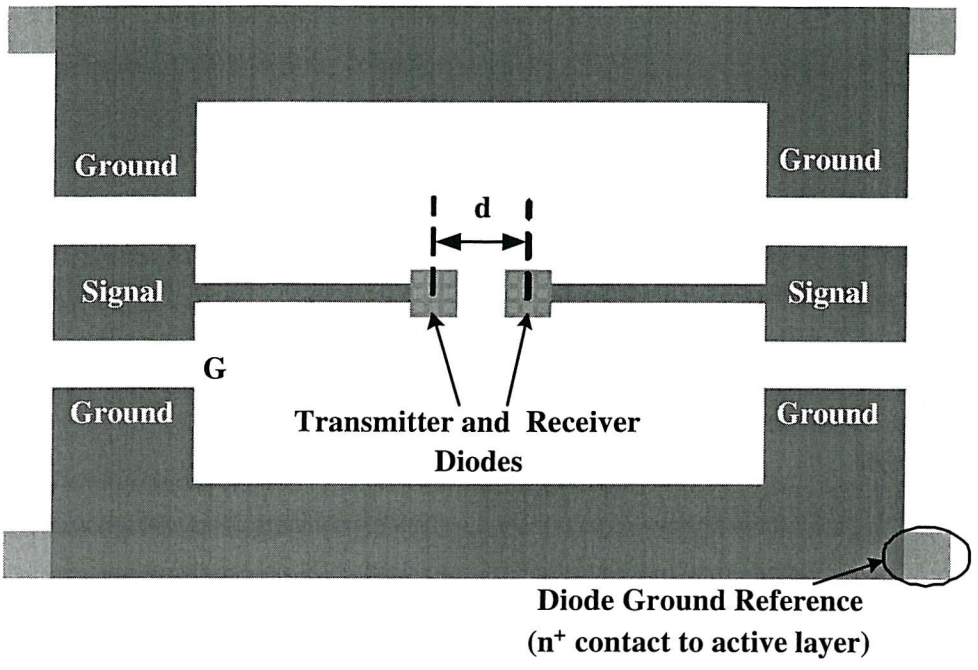


Figure 6.12: Plan view of the test structures for the SOI crosstalk experiments.

The previous expression is identical for the handle substrate as well, and as it will be shown later predicts the conductive coupling very well, when the two conductors are long.

6.6 Experimental Verification and Model Validation

6.6.1 Description of Experiments

For the purpose of this work, test structures similar to those presented in chapters 3 and 4 were designed and fabricated on SOI substrates. The SOI substrates consisted of a n-type silicon (active) layer of approximately 2.0 μm thickness on top of 1 μm of oxide (insulator). The doping of the active layer was constant for all experiments and equal to 10^{16} cm^{-3}, corresponding to a resistivity of 0.5 Ω.cm. The n-type handle substrate had a variable resistivity to account for both the standard (9-15 Ω.cm) and high (200 Ω.cm) cases.

The test structure that was fabricated on the SOI substrate is also shown in Figure 6.12. It is very similar to those presented so far in previous chapters but with some modifications. The Tx/Rx pads were connected from the surface to square p-type implants in the active layer that formed p-n junctions as noise transmitters and receivers. The dimensions of the junctions were identical to the metal pads on top of them (50x50 μm^2) and their depth was 0.5 μm. Figure 6.12 shows a top view of the test structure and Figure 6.13 a partial cross-sectional view. On the surface of the active layer a 0.5 μm thick layer of thermal oxide was initially grown to insulate the coplanar waveguide metal structure at the surface from the active silicon layer.

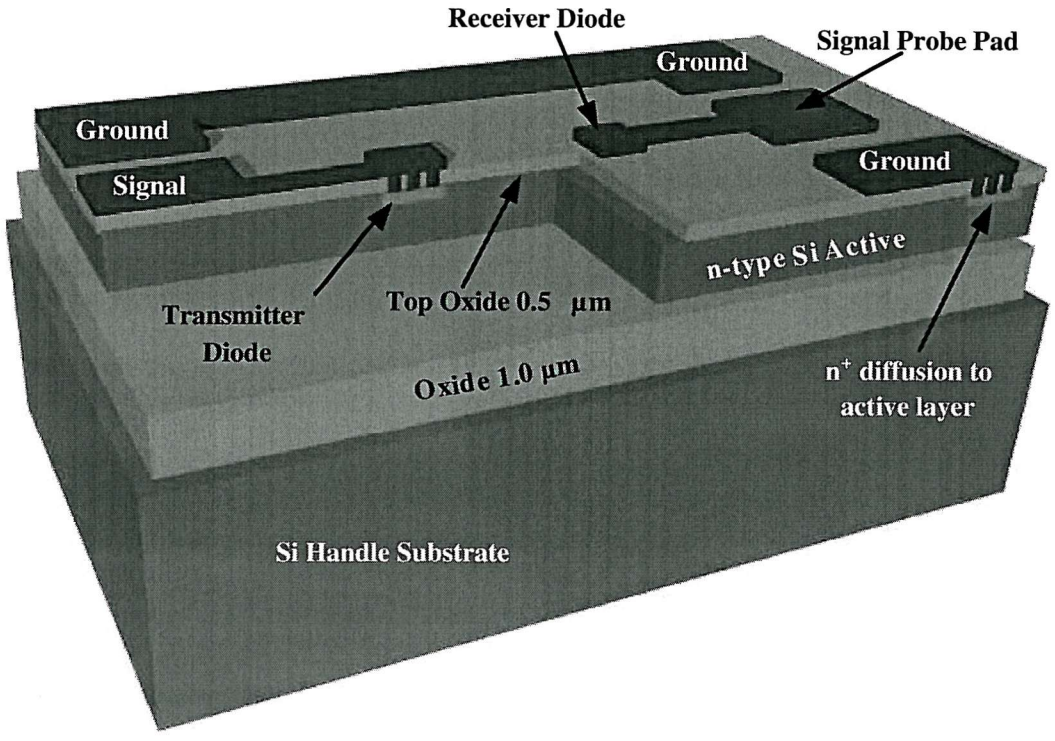


Figure 6.13: Cross-sectional view of the test structure for the SOI experiments, showing in detail the different layers of the substrate and test structure.

The metal pads were connected to the junctions through contact windows etched through the thermal oxide. To prevent the active layer from electrically floating and to provide a reference point for the two junctions, top-down contacts were included at the four edges of the coplanar structure that connected the active layer to the surface RF ground. The pad separations were 75, 100, 150, 200 μm.

Using p-n junctions as noise receivers and transmitters allows us to inject directly into the substrate the "noise" signal and investigate the noise coupling between two fundamental semiconductor elements. One could view one junction as the drain of a MOS transistor that generates the noise and the other junction the source or drain of a neighbouring sensitive MOS transistor. Alternatively, the sheer dimensions of the two junctions allow us to view them as concentrated noise sources and sensors of neighbouring circuits, where for instance the noise transmitter might be the equivalent noise injected by all junctions in a circuit. Hence, this approach addresses the substrate coupling problem from a more practical view, since circuit components are now involved and not just metal pads on insulator. On the other hand, as will be shown, the presence of junctions affects significantly some parts of the isolation characteristic and adds a component that was not included in the aforementioned strip line analysis. The fabrication of these test structures took

place in the Department of Electrical and Electronic Engineering, Queens University of Belfast, Northern Ireland and a full listing of the fabrication process is given in Appendix D.

6.6.2 Measurements

The scattering parameters were measured using a HP 85109C on-wafer characterisation system. The 85109C was calibrated with the Load- Reflect-Reflect-Match (LRRM) standard in the frequency range of 500 MHz to 50 GHz. 150 μm pitch Cascade Microtech air coplanar (ACP) probes with tungsten tips were also used. The dynamic range of the instrument was enhanced by enabling the averaging feature for 256 points.

Measurements of the high resistivity SOI wafers have exhibited high levels of crosstalk between the Tx and Rx junctions (Figure 6.14). Crosstalk ranges from -32 dB at 0.1 GHz to -16 dB at 50 GHz, for a separation of Tx/Rx pads ranging from 200 to 75 μm. Such levels of crosstalk were expected because the main coupling path between the two junctions is the conductive active layer and noise in now injected directly into active layer, allowing it to propagate easier. In a way, this case resembles a very conductive floating buried layer that mainly due to its conductivity allows easier propagation, as shown earlier in Chapter 3 and mentioned also in Chapter 2 and [1].

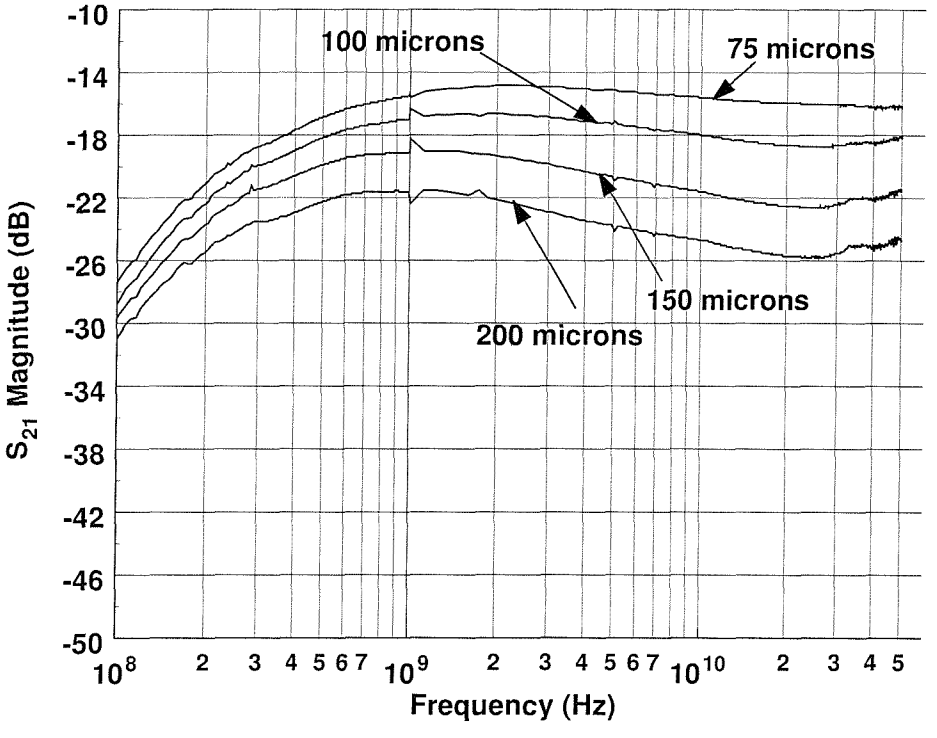


Figure 6.14: Measurements of substrate crosstalk on a high resistivity SOI wafer with variable pad separation before de-embedding the coplanar GSG structure.

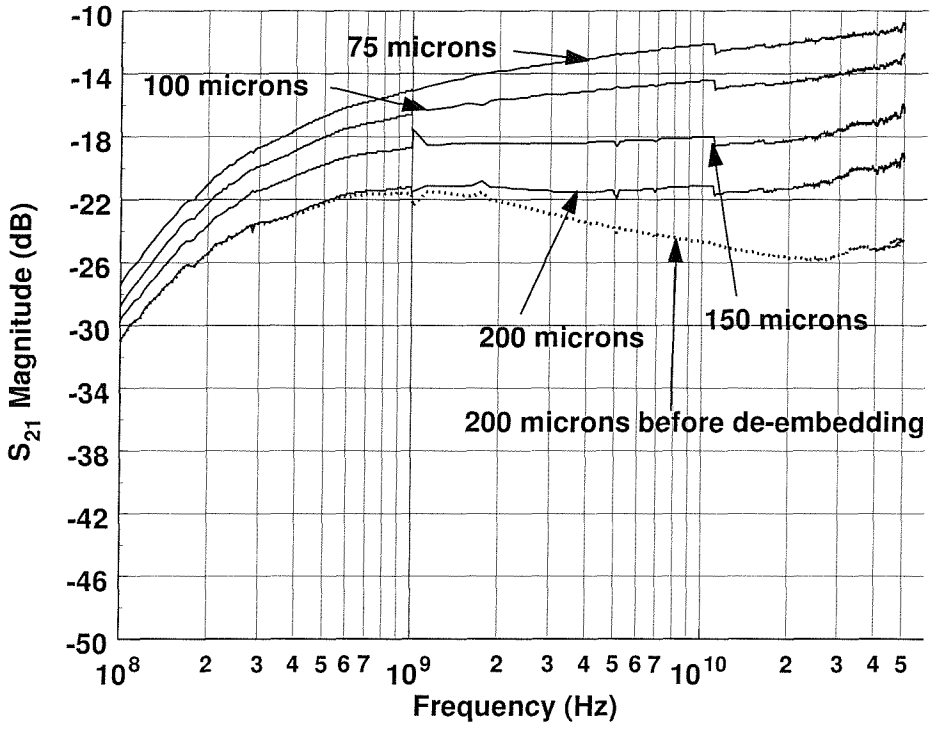


Figure 6.15: De-embedded measurements of substrate crosstalk on a high resistivity SOI wafer with variable pad separation. The dashed line indicates the difference between deembedded and non-dembedded measurements for the 200 μm separation case.

Appropriate 'open' structures were also included in this design, so that their effect could be de-embedded from the initial measurements. The contribution of the capacitances between the ground and signal probe pads and also the effect of the feedlines, both of which appear in parallel with the two pads can then be subtracted from the measurement. The probe pad due to its large dimensions and the small distance between itself and the ground pad can shunt part of the available input energy to ground before it is applied to the transmitter pad. The input signal capacitively couples through the 0.5 μm surface oxide to the active layer and forms an RC network from the input to the ground that appears in parallel with the device under test. By eliminating the Tx/Rx pads an "open" structure is formed and the coupling between the signal and ground probe pads and between the transmitter and receiver feedlines can be measured.

Figure 6.15 shows the effect of de-embedding on the measurements and the final measurement data that represent the coupling between the two junctions without any interference from the surrounding coplanar waveguide structure. After careful observation of the de-embedded measurement data, one can identify three distinct regions of crosstalk. Low frequencies up to 1 GHz exhibit a 20 dB per decade slope that tends to increase crosstalk. At mid range frequencies s_{21} seems to remain

constant until it reaches high frequencies, above 30 GHz, where it starts to increase again. From these observations, clearly s_{21} follows the pattern that has been described in the theoretical qualitative analysis at the beginning of this chapter. The unknown so far is the low frequency behaviour, which will be explained in the following sections with the aid of electromagnetic and lumped element modelling.

6.7 Electromagnetic Modelling and Lumped Model Validation

6.7.1 Electromagnetic Modelling

Electromagnetic simulations were performed with *EM-Sight* on two square Tx/Rx pads 50 μm wide and 0.5 μm deep embedded on a high resistivity SOI substrate of the same properties as the fabricated one. Having available de-embedded measurements simplifies greatly the simulation procedure because the design that has to be entered in the simulator only has to include the two pads and not the entire coplanar structure. This results in little use of available computer resources and faster simulation times.

In order to simulate the effect the junctions have on the s_{21} response, the depletion region associated with each junction has to be entered in the simulator. The depletion region is effectively a layer of non-conductive silicon of specific thickness that surrounds each junction from the sides and below. The simulator software however, did not allow a substrate layer to be entered only underneath each junction but it had to be extended throughout the whole substrate. This limitation did not present significant problems because it still allows the capacitive properties of the substrate coupling to be calculated without any loss. The conductive coupling may be underestimated since the depletion region layer is non-conductive.

Given the previously mentioned limitations and approximations, Figure 6.16 shows simulation data compared to measurements for one Tx/Rx pad separation distance. Reasonable agreement has been observed and the deviation can be explained by the simulators limitation to accurately model the depletion capacitance.

6.7.2 Lumped Element Model Formulation and Validation

Although the topology of the lumped model for the SOI coupling has been established at the beginning of this chapter, the presence of the junctions as noise receivers and transmitter introduces a modification to the model. As was mentioned before, each junction is associated with a depletion region and therefore a depletion capacitance. This capacitance extends to the bottom and the periphery of the junctions. Since the bottom area of the junction occupies an area of 50×50 μm^2 and the sidewall is only 0.5 μm deep, it is safe to assume that most of the depletion capacitance will be associated with the bottom part.

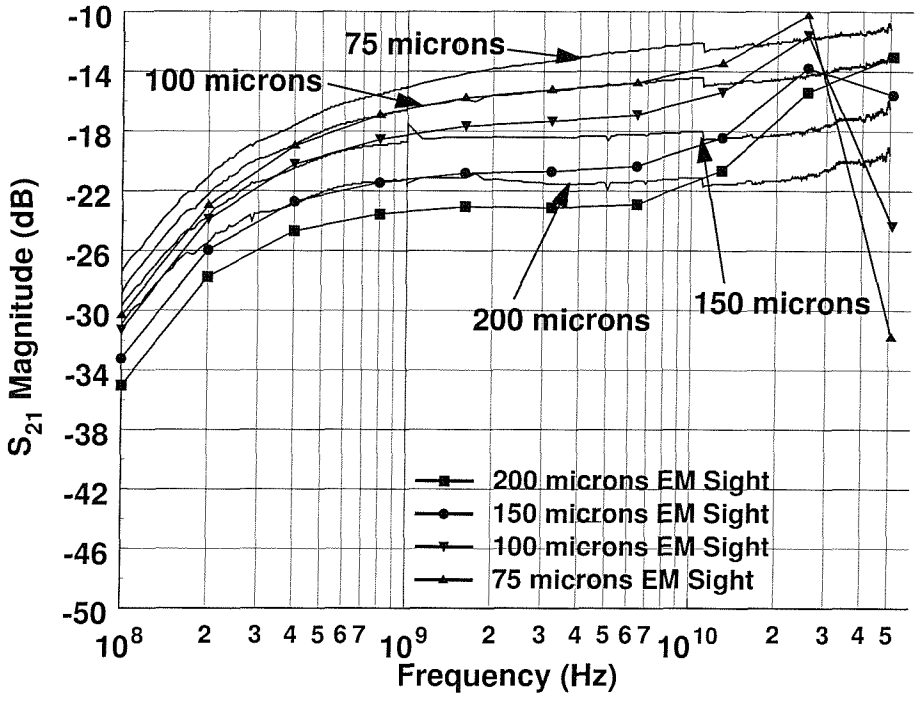


Figure 6.16: Electromagnetic simulation data and comparison with measurements for different Tx/Rx pad separations.

The depletion capacitance now appears in series with the coupling model of the silicon active layer as shown in Figure 6.17. A simple analysis of this circuit reveals a response similar to the measurements and is shown in Figure 6.18. Because the depletion capacitance appears in series with the coupling model, it introduces the 20 dB per decade rising slope observed at low frequencies. By calculating analytically s_{21}, it can be shown that this behaviour is caused by a zero located at dc. Then, this zero is cancelled by a pole at f_2 that gives s_{21} a constant value. Analytically calculating f_2 results in:

$$\begin{aligned} f_2 \;=\; & -\frac{1}{2\cdot\pi}\cdot\frac{1}{4\cdot R_0\cdot C_J\cdot R_a\cdot C_{EQ}}\cdot\{-2\cdot R_0\cdot C_J - R_a\cdot C_J - 2\cdot R_a\cdot C_{EQ}+ \\ & +\left(4\cdot R_0^2\cdot C_J^2 + 4\cdot R_0\cdot C_J^2\cdot R_a - 8\cdot R_0\cdot C_J\cdot R_a\cdot C_{EQ} + R_a^2\cdot C_J^2+\right. \\ & \left.+4\cdot R_a^2\cdot C_J\cdot C_{EQ} + 4\cdot R_a^2\cdot C_{EQ}\right)^{\frac{1}{2}}\} \end{aligned} \tag{6.17}$$

Finally, at very high frequencies another zero is causing the second increase and is located at f_3

$$f_3 = \frac{1}{2\cdot\pi\cdot(R_a\cdot C_{EQ})} \tag{6.18}$$

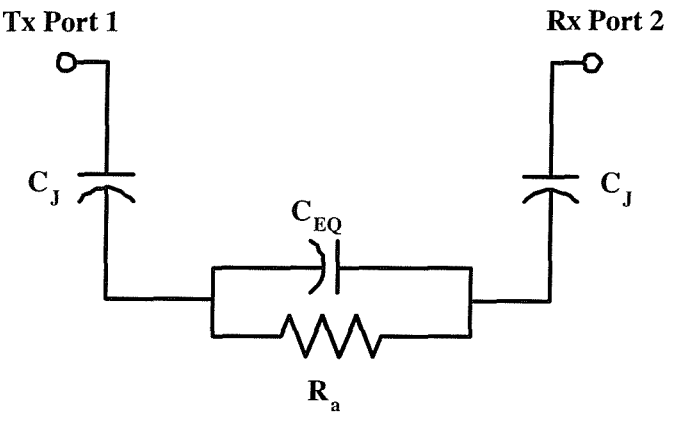


Figure 6.17: Equivalent lumped element model of high resistivity SOI crosstalk after the introduction of the depletion capacitance C_J.

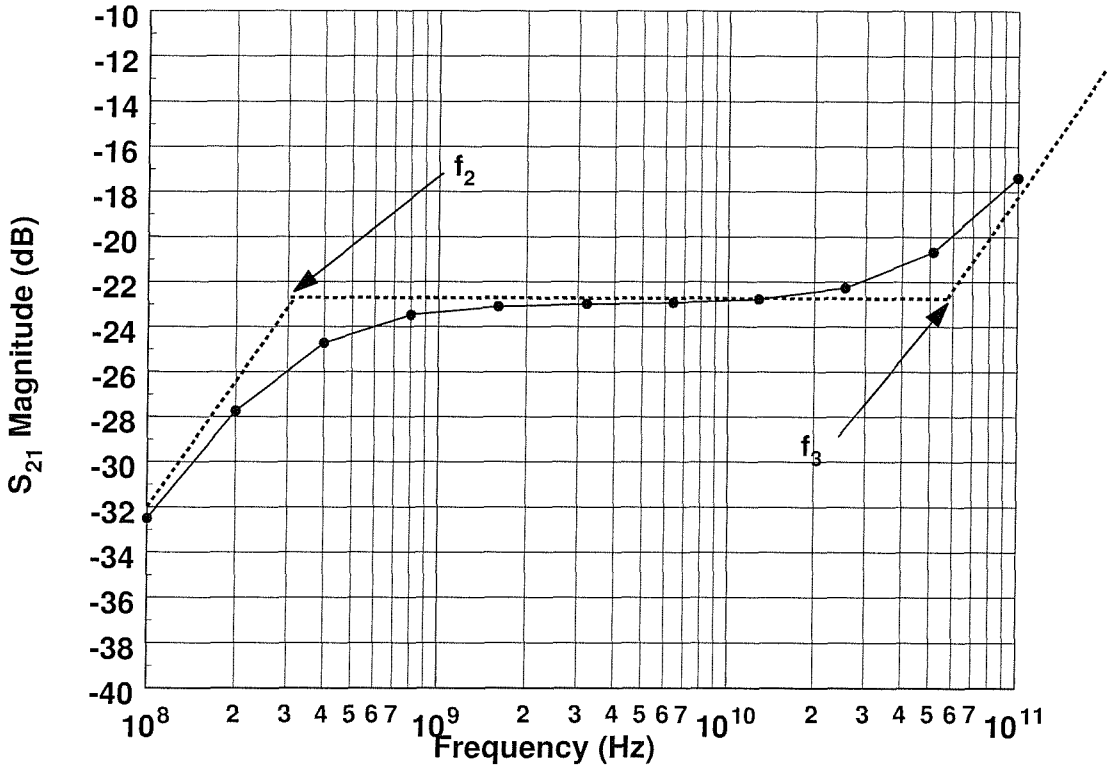


Figure 6.18: S_{21} response of the model of Figure 6.17 when C_J=0.8 pF R_a=1300 Ω and C_{EQ}=2fF.

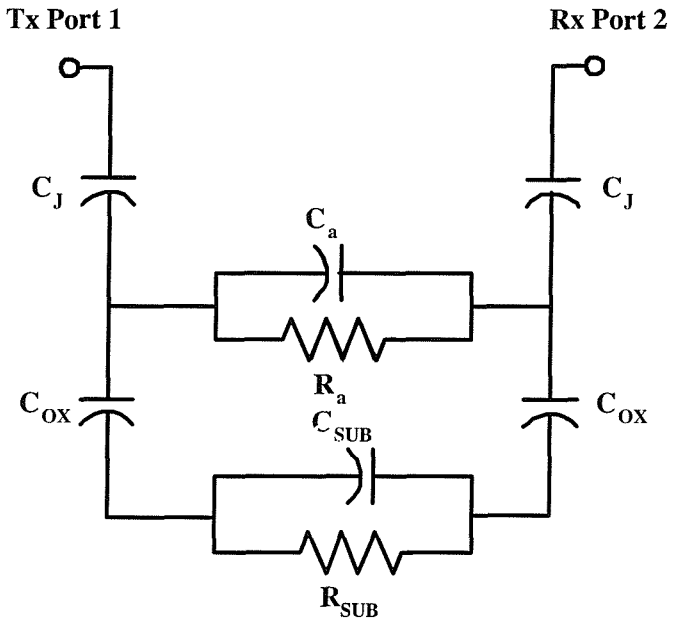


Figure 6.19: Lumped element model topology for SOI substrate crosstalk with diode noise transmitters and receivers.

Introducing the depletion capacitance also changes the noise level that reaches the substrate because the noise signal has to go through the impedance associated with the depletion capacitance. This may, in turn, affect the amount of noise that will propagate to the noise receiver pad, rendering the coupling analysis less accurate.

6.7.3 Lumped Model Validation

With the topology of the SOI crosstalk model established, the model parameter values can now be checked against the values predicted by theory. The final SOI crosstalk model in shown in Figure 6.19 and is derived from the test structures that have been measured and their results presented in previous sections. The model only takes into account the coupling between the two junctions and compares the response with de-embedded measurements. C_J is the depletion capacitance of each junction. From the fabrication data the doping of the junction implant can be extracted and a value of the depletion region can be calculated. The vast amount of depletion capacitance originates from the bottom part of the junction and the periphery component is ignored. A simple calculation of the depletion capacitance can be initially performed assuming uniform doping profiles and the "abrupt-junction approximation". The vertical oxide capacitance C_{BOX} is due to the buried oxide layer of the SOI and is calculated by a parallel plate formula. R_a, C_a and R_{SUB}, C_{SUB} are the coupling components of each silicon layer as described at the beginning of this chapter.

A similar approach to that of Chapter 3 was utilised for the model validation. Initially, the values of the model parameters as predicted by theory were entered in the model. These values were then numerically optimised in order to achieve good agreement between the measurements and the model simulation.

Table 6.1 presents the initial values of the model elements for the different Tx/Rx pad separations. The analysis is performed on a high resistivity SOI wafer. Numerical optimisation and fine-tuning was performed so that the final values of the model parameters were in good agreement (within 5%) with the measurements. Figure 6.20 also shows the optimisation procedure for one model corresponding to the 100 μm Tx/Rx pad separation case. When the theoretical values are entered into the model, the deviation is considerable. However, the basic shape of the response is in agreement with the analysis. It can be observed from the model response, that the coupling is predicted to be lower and also the frequency where the depletion capacitance forces the 20 dB per decade slope. These observations indicate the parameters that may be overestimated by the theoretical formulae. Given the fact that the dominant coupling path is through the active layer at the surface, the parameters that could be altered by the optimiser may be C_a and R_a. Of these two, however, R_a is responsible for the flatness of the s_{21} response at the range of 1-20 GHz and C_a is causing the slight increase visible only towards the upper limit of the frequency spectrum. Therefore, decreasing R_a would increase the level of crosstalk to that shown in the measurements.

The junction capacitance could also be optimised because according to measurements, the point where it affects the response is located at a lower frequency and therefore C_J must be increased. Table 6.2 shows the optimised values of R_a, C_J and the amount of alteration that had to take place in order for the model response to be within 5% of the measurement data. The values of the rest of the parameters were not changed. It must be noted that these values are not unique in any way. It is possible to let the optimiser change the values of all parameters at once and therefore achieve a good agreement. However, each parameter change undermines the theoretical background and physical origin of the model.

According to the tables, the parameter that was clearly overestimated by the theoretical analysis was R_a. In other words, since R_a was extracted by C_a, the conductive coupling between the two pads was heavily underestimated. A brief analysis of this finding is included in the next section, where the effect of the pad length is analysed.

6.7.4 Effect of Finite Pad Length

The modelling theory for the substrate coupling that has been presented so far is based on the symmetrical double-strip coplanar waveguide configuration, where

	200μm	150μm	100μm	75μm
C_J (pF)	0.747	0.747	0.747	0.747
C_{BOX}(pF)	0.085	0.085	0.085	0.085
C_a (fF)	0.712	0.774	0.900	1.205
C_{SUB} (fF)	2.96	3.35	4.12	5.02
R_a (Ω)	2339	2339	2333	1330
R_{SUB} (Ω)	71.65	63.34	51.51	42

Table 6.1: Theoretical parameters of a high resistivity SOI substrate crosstalk model for different Tx/Rx pad separations.

	Theoretical	Optimised	% Error
C_J (pF)	0.747	1.24	39.75
R_a (Ω)	2333	481	385

Table 6.2: Optimised R_a and C_J of a high resistivity SOI substrate crosstalk model for 100 μm Tx/Rx pad separation.

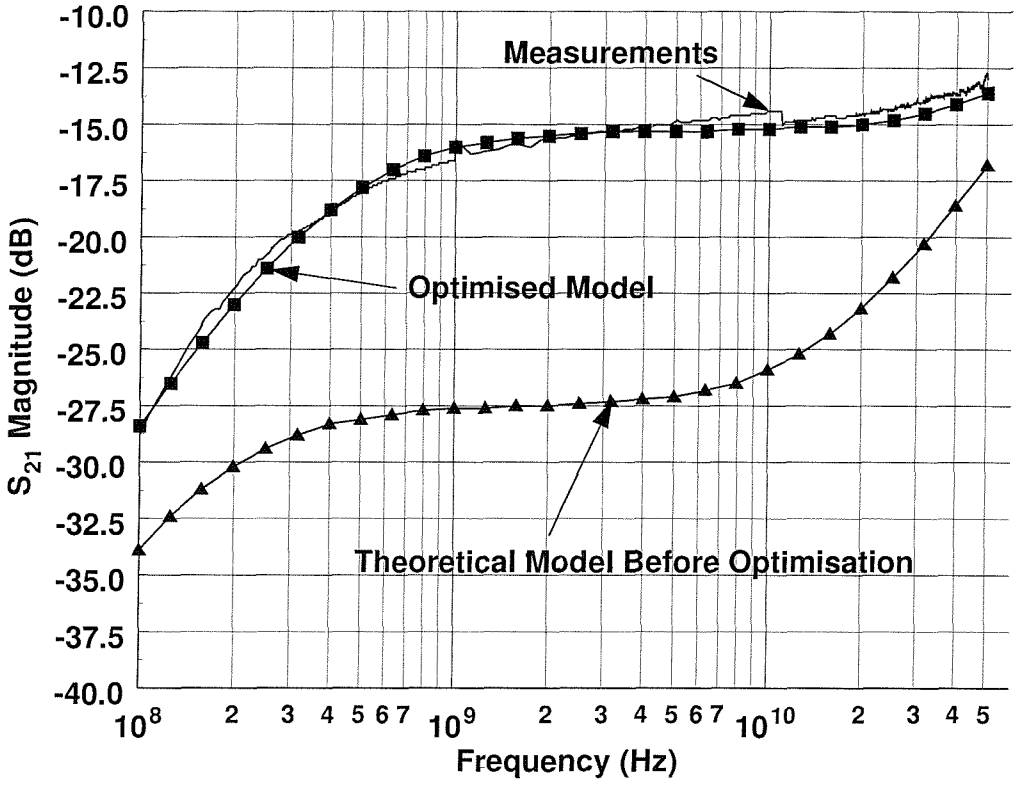


Figure 6.20: Theoretical and optimised substrate crosstalk model response of two diode pads on a high resistivity SOI substrate separated by 100 μm.

the length of the two striplines is assumed to be very long and the values of the capacitances are per unit length. This assumption is valid when the length is much bigger than the width and the separation between the lines because only a small, usually negligible, amount of coupling is due to the fringing fields at the edges or other open-end effects.

The test structures under investigation however, are square and coupling from the sides of the pads that do not face each other is significant. In other words, a per unit length calculation of capacitances tends to underestimate the real amount of coupling because the fringing fields of the sides are not considered. The same observation applies for the resistive coupling that is extracted from the initial capacitance formulae and is also expressed in per unit length values.

The effect of the pad length can be illustrated by a series of EM simulations with *EM-Sight*. Two zero thickness conductors with variable length L, equal width (50 μm) and constant spacing from each other were simulated on a finite thickness Si substrate. The length of the conductors ranged from 50 to 500 μm, or in other words, square pads to relatively long conductors. The thickness of Si substrate was 2.0 μm and its resistivity 0.5 Ω.cm identical to that of the active layer in the SOI. Such a configuration was chosen in order to be simple and directly comparable with the double-strip configuration.

The model parameters were extracted at the lowest simulation frequency using equation (6.3) and (6.4) for each case and were plotted against the value predicted by theory. Figure 6.21 shows R_{SUB} versus conductor length L for simulations and measurements. As the length of the conductors decreases, the deviation between theory and the extracted values increases. This is an indication that the derivation of resistive coupling through the capacitive coupling is only applicable to rectangular pads where the length of the pads is much higher than their width for a given spacing. The calculation of capacitive coupling is based on per unit length values because very long conductors (pads) are assumed. As their length decreases fringing fields from the sides become more and more significant. These effects can be compensated by introducing empirical terms to the formulas but will only be applicable for certain experimental configurations and not cover a wider range of parameters.

6.7.5 Effect of Handle Substrate Resistivity

The analysis and modelling of crosstalk in SOI substrates was targeted at configurations with high resistivity handle substrates mainly because of the approximations that can be made when a lumped model is produced. As has been mentioned, the finite resistivity of the handle substrate causes significant problems in the extraction

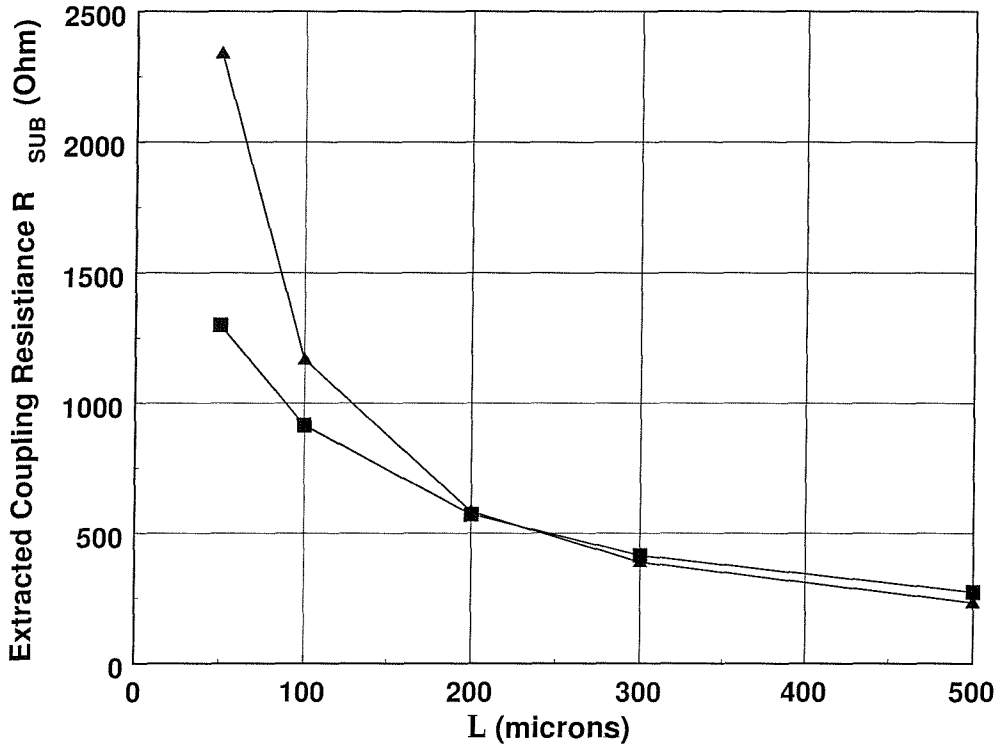


Figure 6.21: Theoretical and extracted R_{SUB} versus pad length L for two pads with 50 μm width and 50 μm spacing on 2.0 μm of silicon.

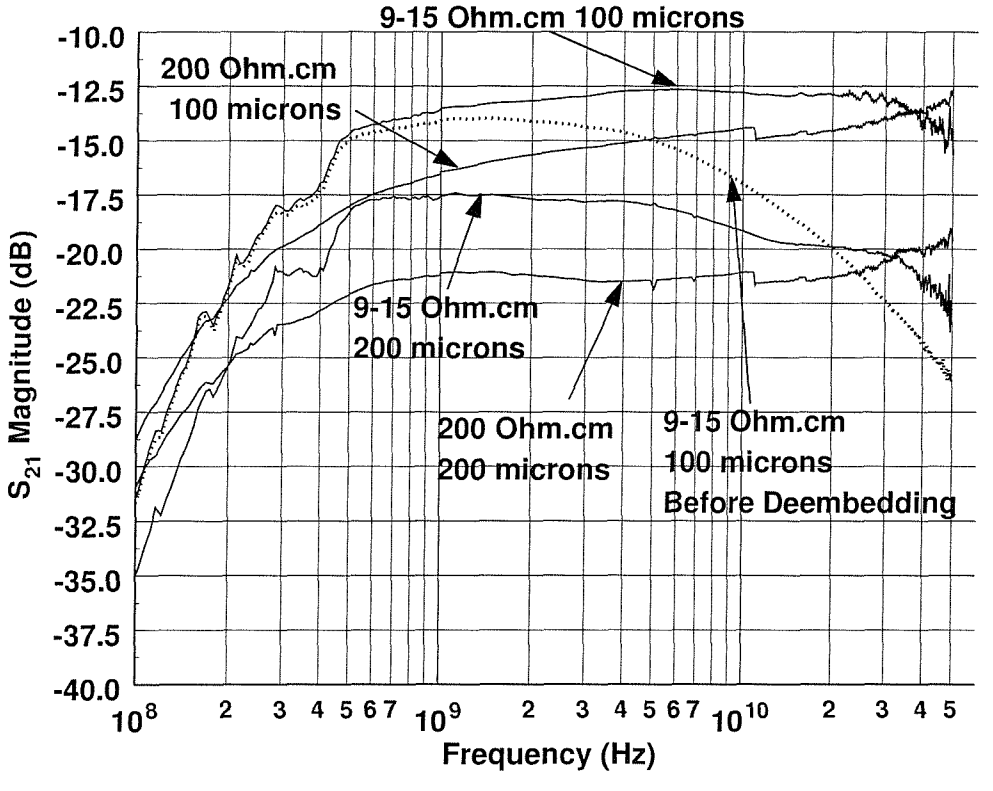


Figure 6.22: Measurements of crosstalk in high (200 Ω.cm) and standard (9-15 Ω.cm) resistivity SOI substrates for 200 μm and 100 μm Tx/Rx pad separation.

of the capacitive and resistive coupling parameters, even in high resistivity handles. This problem becomes worse in the case of a lower resistivity (9-15 Ω.cm) handle, making the parameter extraction even more difficult. However, a comparison of crosstalk between two SOI substrates with standard (9-15 Ω.cm) and high (200 Ω.cm) resistivity handles can be made based on the measurements. Figure 6.22 shows the cases of two test structures with 100 μm and 200 μm Tx/Rx pad separation. The standard resistivity handle exhibited higher crosstalk than the high resistivity one as expected. The existence of a less resistive path through the Si handle is obviously responsible for that behaviour. As mentioned before, deembedding the Tx/Rx pads from the surrounding structure has a significant effect on the crosstalk response. The low frequency behaviour is once again dominated by the depletion capacitance of the diodes at the Tx/Rx pads. The remaining differences of the shape of the response are due to a different location of the zeros and poles caused by the different value of the handle substrate resistivity.

6.8 Conclusions

Substrate crosstalk on an SOI substrate was analysed in this chapter with the aid of electromagnetic and lumped element models. Test structures with pn junctions as noise transmitters and receivers were designed and fabricated on SOI substrates. Measurements of these structures showed that crosstalk is very high due to the direct coupling of the structures at the active silicon layer. The active layer is the dominant coupling path but the handle substrate also affects the response considerably. Comparison of the measurements of the same test structures but with standard (9-15 Ω.cm) and high (200 Ω.cm) resistivity handles showed that the latter have better isolation performance, since the conductive part of the coupling is suppressed when the resistivity is high. That was one of the reasons the analysis was targeted at high resistivity SOI substrates.

High resistivity SOI substrates were also easier to study because the coupling through the handle substrate can be simplified and the analysis can be concentrated on the active layer. The problem of modelling substrate coupling between two pads was addressed by using the coupling model of a double-strip coplanar waveguide of infinite length on a finite thickness substrate. The shape of the pads has proved to be a limiting factor for the successful modelling of the resistive coupling between the two square noise receiver and transmitter pads. The assumption that the conductors are very long is not applicable to square conductors and causes significant errors in the modelling. In order to predict some of the model parameters it is therefore better to resort to electromagnetic simulations where the cross-coupling between the different layers of the SOI substrate is taken into account.

Overall, the crosstalk response of the studies configuration exhibits three distinct regions of operation. Low frequency coupling below 1 GHz is dominated by the junction capacitance of the diode Tx/Rx pads. As frequency increases above 1 GHz the coupling becomes constant due to resistive coupling mainly through the active layer. At high frequencies, close to 50 GHz, a slight increase is only barely visible and is caused by the capacitive coupling components.

Chapter 7

Ground Plane Silicon on Insulator (GPSOI) Substrate Crosstalk Analysis and Modelling

7.1 Introduction

Following the analysis and modelling of substrate crosstalk effects on substrates with buried ground planes in Chapter 3 and SOI substrates in the previous chapter, this chapter presents and analyses the crosstalk performance of GPSOI substrates. The analysis and modelling is carried out with the aid of electromagnetic simulations and its behaviour is modelled by lumped element equivalent circuits that are derived as a combination of the work presented in the previous chapters. These models are, in turn, validated against experimental data acquired from suitable fabricated test structures in the range of 0.5 – 50 GHz. Comparison with control SOI substrates and other previously published studies of crosstalk reveal the relative performance and potential advantages and disadvantages of GPSOI substrates.

7.2 The Ground Plane Silicon-On-Insulator (GPSOI) Substrate

An illustrative view and an SEM image of a fabricated GPSOI substrate are shown in Figures 7.1 and 7.2 respectively. Both figures show the different layers that the GPSOI substrate consists of and their relative thicknesses. Figure 7.2 also includes a top layer of thermally grown oxide, which is not part of the GPSOI substrate. All GPSOI substrates used in these studies had a buried oxide of 1.0 μm thickness. Underneath the buried oxide there is an n^+ doped layer of polysilicon on top of the buried WSi_2 metallic plane, which form the ground plane. The nominal resistivity of the WSi_2 layer, as quoted by the manufacturer of the substrate , is 40 $\mu\Omega$.cm and its thickness is 0.2 μm. All silicon layers in the substrate are n-type. The handle substrate is 525 μm thick with a resistivity of 9-15 Ω.cm, while the thickness of

the silicon active layer is determined by the polishing and grinding that takes place in order to achieve the desirable thickness. For the substrates of this work the thickness was between 1.5 μm and 1.6 μm and the doping of the silicon active layer was 10^{16} cm^{-3}.

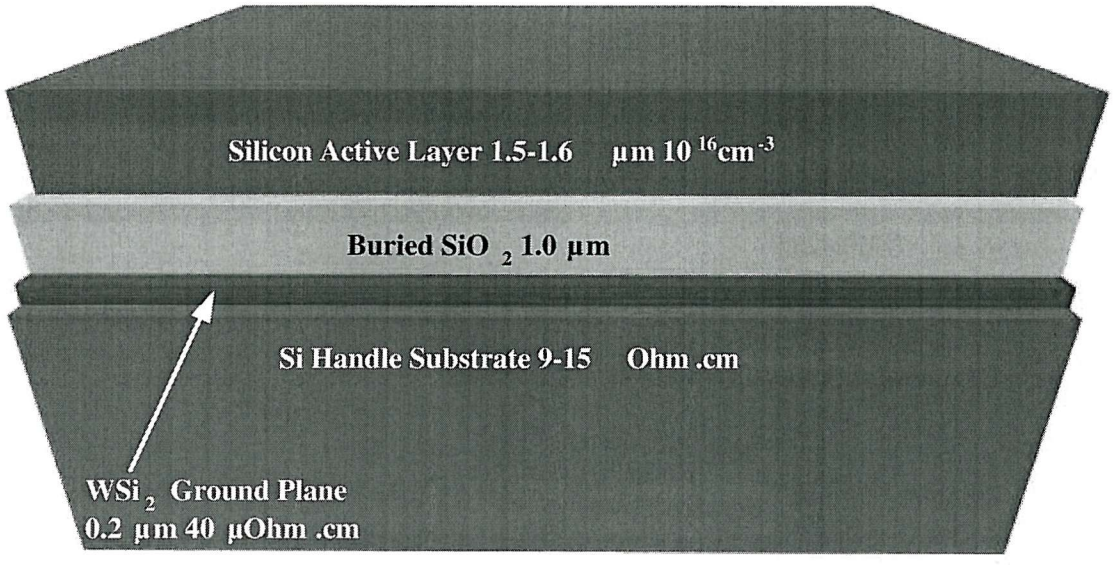


Figure 7.1: Cross-sectional illustration of the GPSOI substrate

7.3 Test Structure Description and Fabrication

A set of test structures similar to those designed for the buried ground plane and SOI experiments was also designed and fabricated on GPSOI substrates. The test structures include two square pads 50 μm wide that serve as noise transmitter (Tx) and receiver (Rx) nodes. The Tx/Rx pads are either aluminium pads that lie on the top oxide of the GPSOI or, as in the case of the SOI substrates of chapter 6, they are connected to p^+ regions on the active layer and form diodes. The distance between the centers of the Tx/Rx pads varies from 75 μm to 200 μm for both cases. The Tx/Rx pads were embedded in a ground-signal-ground (GSG) CPW structure with dimensions identical to those discussed in the previous chapters.

The GPSOI substrate as a noise suppression strategy relies on two factors for its operation and performance. Firstly, the existence of the ground plane itself, which located in close proximity to the Tx/Rx pads. In order for the buried WSi_2 plane to become a ground plane, top down contacts are etched through the silicon and oxide layers and provide an electrical connection to the surface RF ground of the GSG CPW structure. There is an initial etch of the oxide and silicon layers until

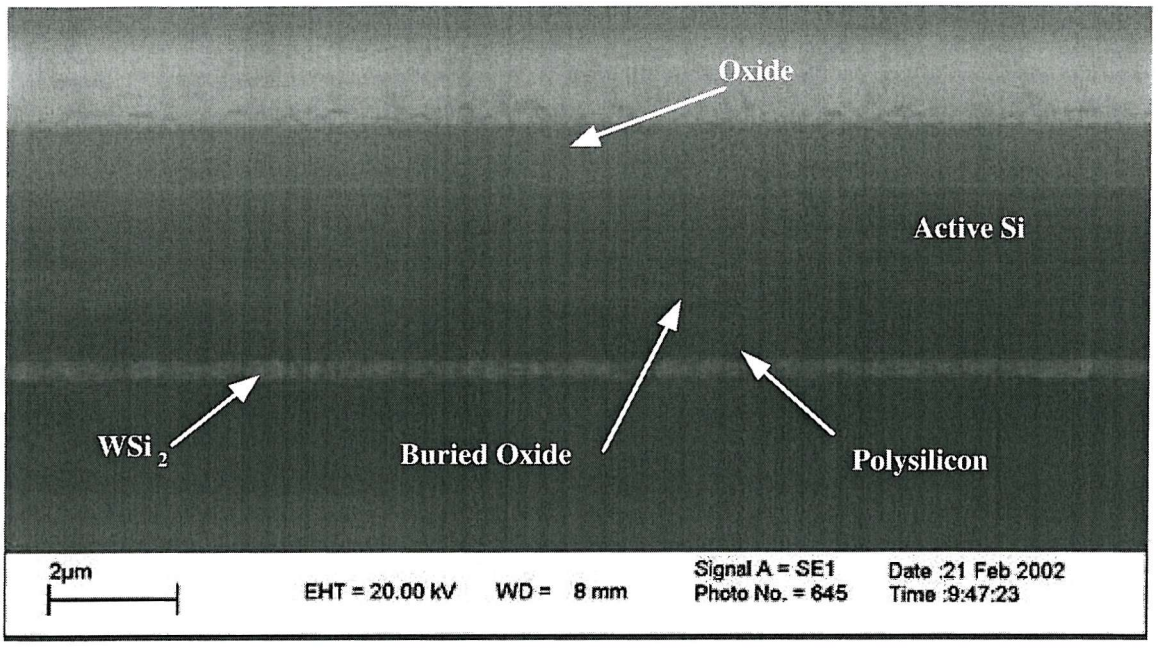


Figure 7.2: SEM image of a fabricated GPSOI substrate showing in detail the different layers. The surface of the active layer has been oxidised.

the WSi_2 plane is reached, which is followed by a short oxidation that creates the sidewall insulating oxide of the trench. After a short anisotropic etch that removes the oxide off the bottom of the trench, the trench is lined with WSi_2 and filled with n^+ doped polysilicon so that the buried plane can be contacted from the top metal. A more detailed description of the fabrication process of these contacts is included in the next chapter, where the Faraday cage structures, which utilise the same process, are discussed. The second factor that affects crosstalk suppression is the distance between the Tx/Rx pads. Cross-sectional illustrations and SEM images of the test structures are shown in Figure 7.3.

7.4 GPSOI Substrate Crosstalk Analysis and Modelling

With the aid of electromagnetic simulations it is possible to analyse the substrate crosstalk behaviour of the GPSOI substrate by initially starting with the much simpler multilayer configuration of Figure 7.5. Two zero-thickness square pads are simulated on top of a silicon layer that has the properties of the active silicon layer. This top layer is separated from an infinite perfect ground plane by 1.0 μm of buried oxide. Such a substrate configuration may not include the silicon handle layer and the finite resistivity ground plane but allows fast simulation times and removes the additional numerical complexity that may be introduced. On the other hand, the entire GPSOI substrate layer stack has to be simulated, so that the efficiency of the simulator can be validated against experimental data and will be shown in a later section.

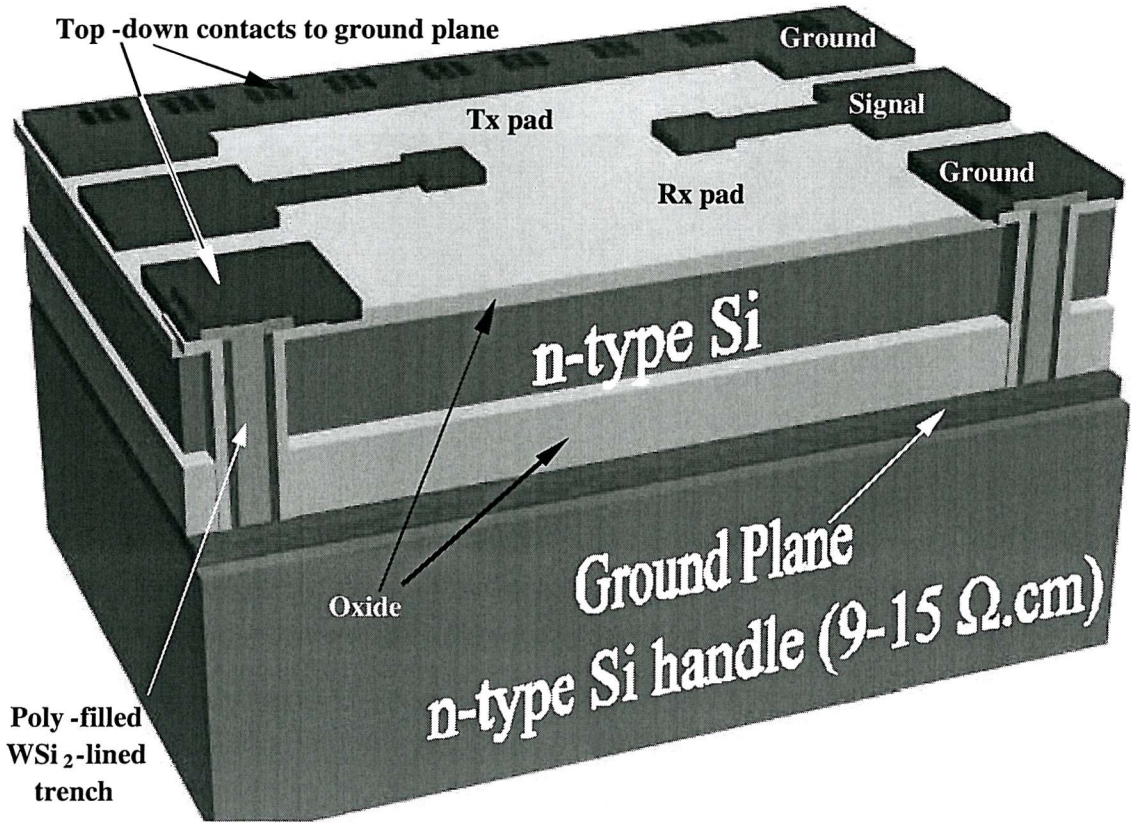


Figure 7.3: Cross-sectional illustration of a crosstalk test structure on GPSOI. The Tx/Rx may be diode or metal-on-oxide pads.

The relation between the GPSOI substrate and the buried ground plane substrate of Chapter 3 can be seen by varying the silicon active layer resistivity. Figure 7.6 shows the transition of the s_{21} characteristic between the two extreme case of an active layer with 0.1 Ω.cm and 100 Ω.cm respectively. Low resistivity values result in a constant s_{21} at low frequencies in a manner similar to that of the SOI substrates of Chapter 6. At higher frequencies however there is a rapid decrease of s_{21}. As active layer resistivities become higher, s_{21} begins to decrease rapidly at high frequencies, but decreases at lower frequencies until the decrease of s_{21} is reversed. In theory, infinite resistivity makes the active layer a pure dielectric and the GPSOI substrate reduces to a substrate with a combination of dielectrics over a ground plane, which effectively is the buried ground plane substrate presented in Chapters 3 and 4. Such behaviour is confirmed by the electromagnetic simulator, when very high values of active layer resistivity are entered, by exhibiting the familiar 20 dB per decade slope of s_{21} across a large part of the frequency range.

It must be noted though, that when the resistivity of the active layer becomes very high, these approximations are not valid because the coupling path through C_{air}, C_a and C_2 becomes significant compared to the resistive coupling through R_a. Ideally, for infinite resistivity the model reduces to a topology very similar to that of Figure

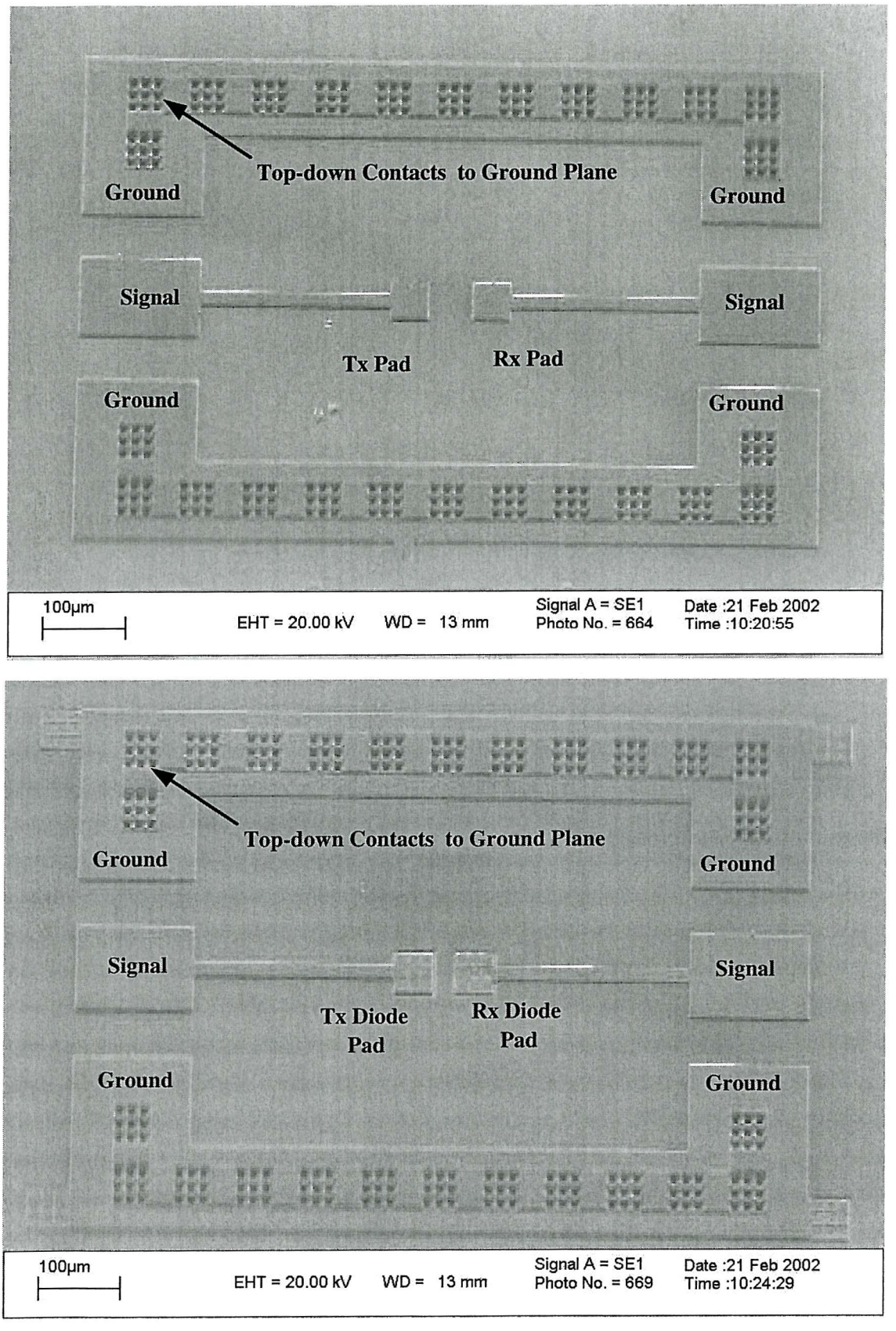


Figure 7.4: SEM images of the fabricated test structures with (a) metal-on-oxide and (b) diode Tx/Rx pads.

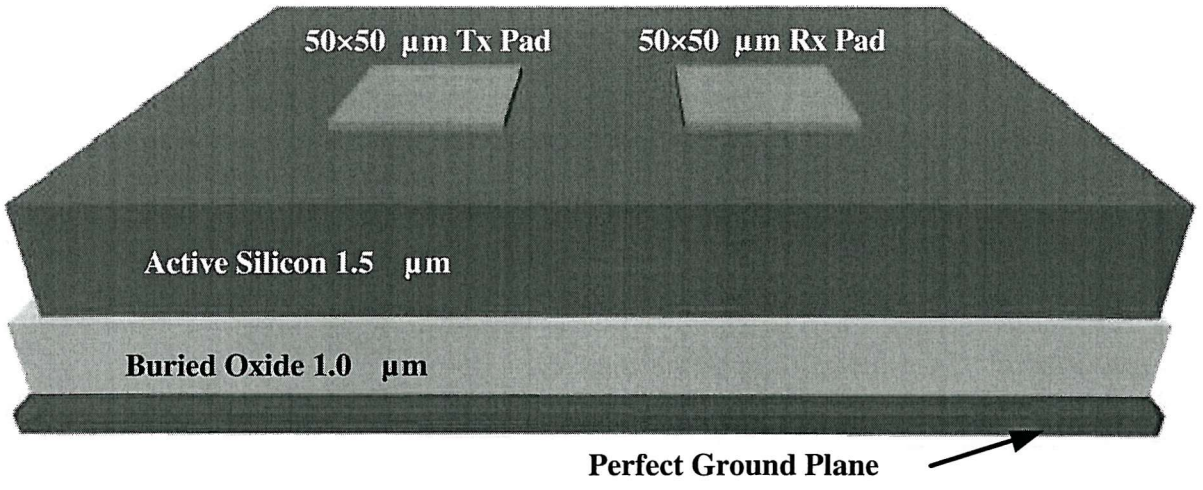


Figure 7.5: Simplified GPSOI substrate structure simulated with EM-Sight.

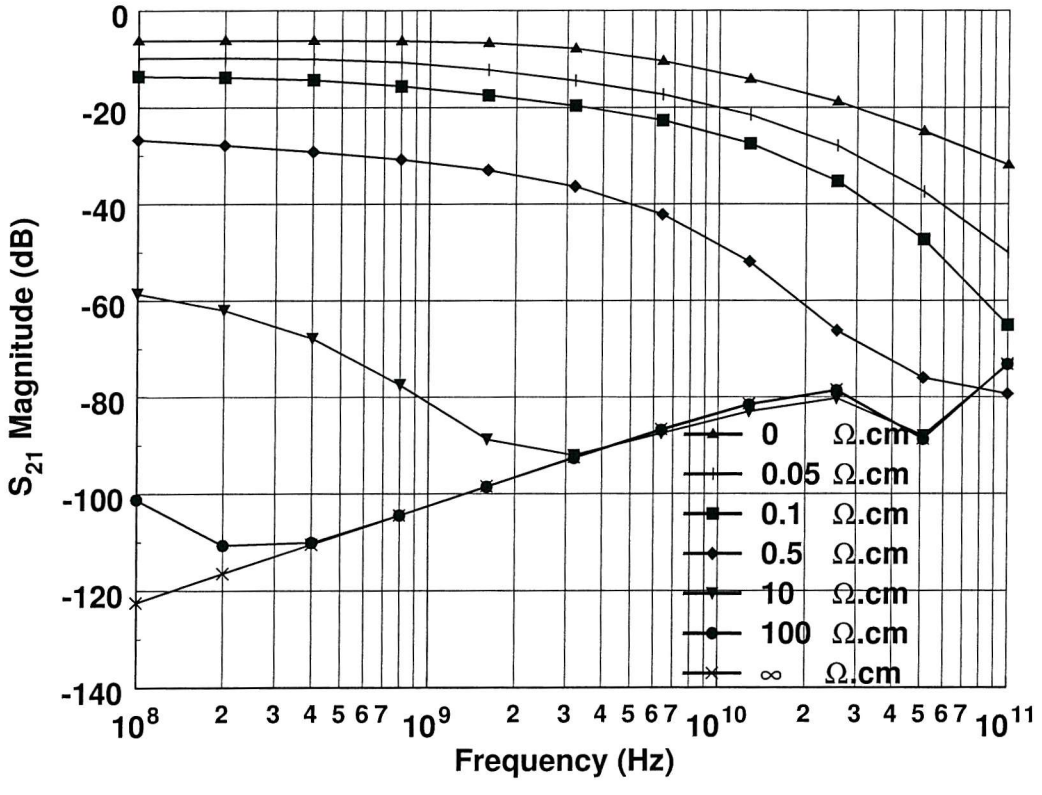


Figure 7.6: Magnitude of s_{21} versus frequency simulations of the substrate shown in Figure 7.5 with variable active layer resistivity.

4.8 with the lateral coupling capacitance being the parallel combination of C_2, C_{air} and C_a.

Varying the thickness of the buried oxide layer also reveals interesting results about the low frequency behaviour of the GPSOI. As shown in Figure 7.7, the low frequency behaviour is not affected significantly by the thickness of the buried oxide. At high frequencies, however, the rapid decrease of s_{21} appears at a lower frequency as the buried oxide thickness is decreased or the closer the two pads lie to the ground plane.

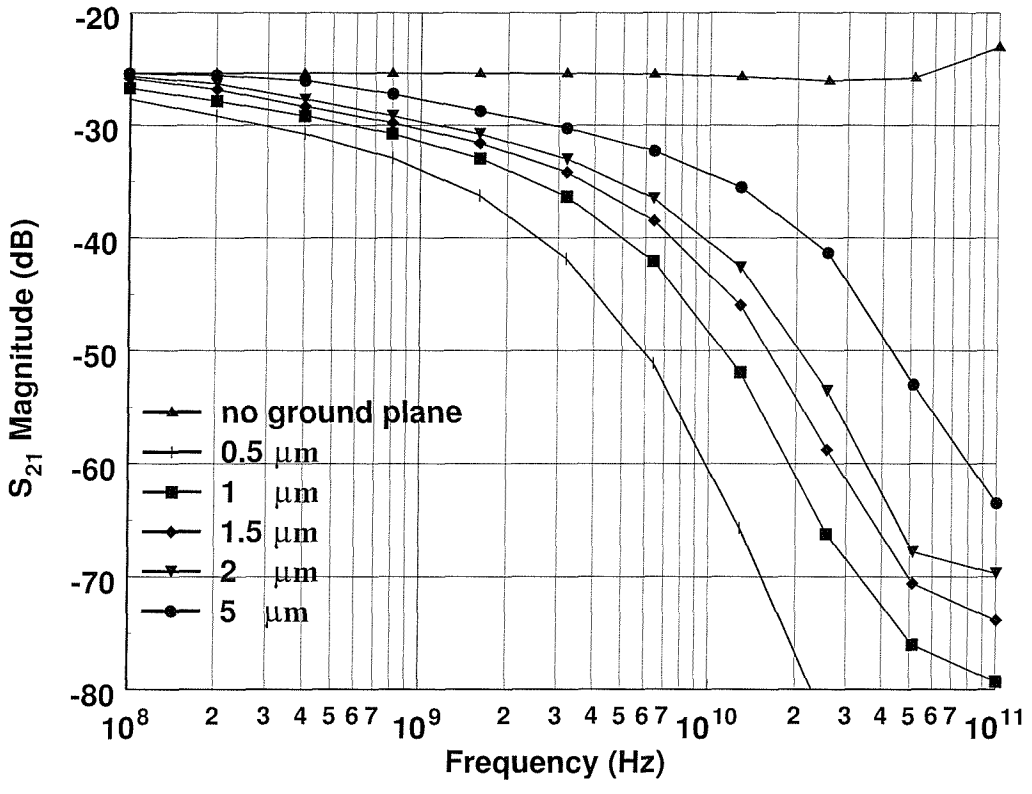


Figure 7.7: Magnitude of s_{21} versus frequency simulations of the substrate shown in Figure 7.5 with variable buried oxide layer thickness.

Both of these observations indicate that low frequency behaviour is very similar to SOI substrates, where the resistive coupling through the active layer dominates. At the other end, high frequencies are related to the ac loading effect that has been analysed in chapter 4 and is caused by a vertical capacitance to the ground plane.

Based on these two observations and the aforementioned qualitative analysis of the GPSOI substrate, a lumped element model can be constructed through the combination of the lumped models of the buried ground plane and SOI substrates. Figure 7.8 shows how the two models can be combined to produce the GPSOI crosstalk model. C_2 is the capacitance through the air and top oxide that was

responsible for the crosstalk in buried ground plane substrates. The RC network of R_a and C_a describe the resistive and capacitive coupling through the active layer. The capacitance between the active layer and the ground plane is taken into account by C_{BOX}, while the coupling through the handle substrate is described by R_{SUB} and C_{SUB}. Finally, R_1 and R_2 represent the finite resistance of the ground plane. These models describe substrate crosstalk between two pads on a buried ground plane and a SOI substrate respectively. No reference is made yet to the nature of the pads (i.e. metal-on-oxide or diode Tx/Rx pads).

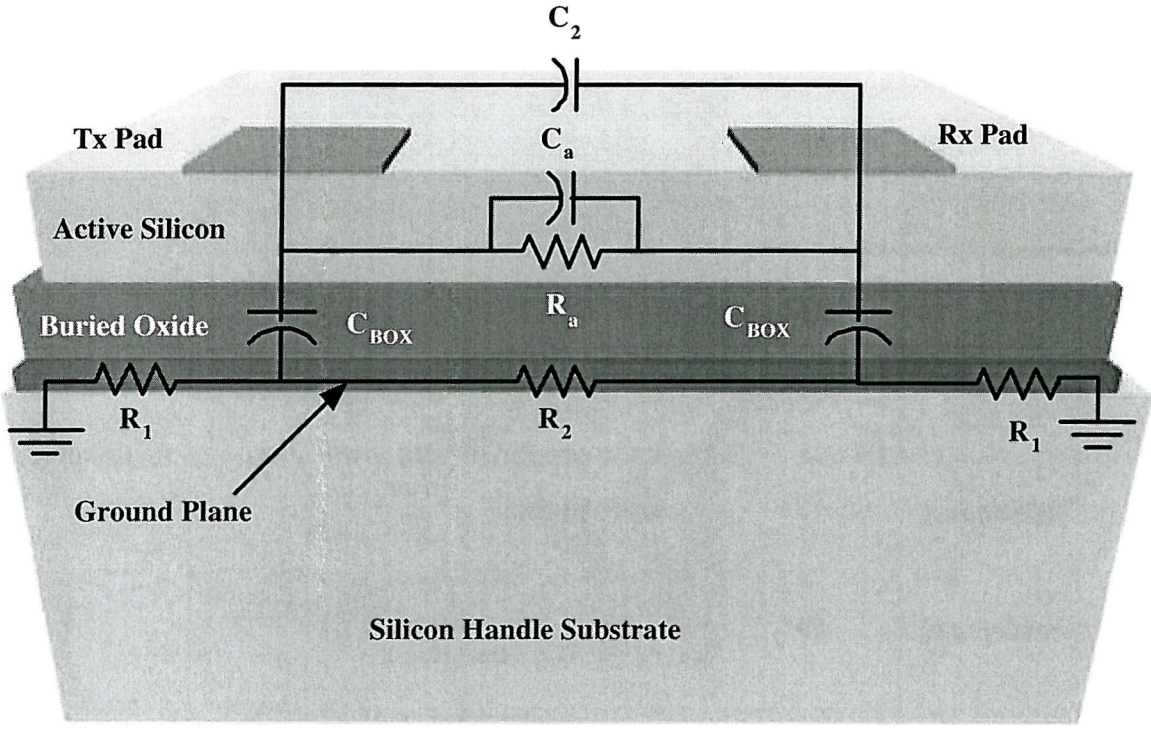


Figure 7.8: The GPSOI substrate crosstalk model before its simplification.

The topology of the lumped model of Figure 7.8 can be significantly simplified by taking into account the conclusions derived from the previous electromagnetic analysis and the analysis of the SOI and buried ground plane substrates. The capacitive coupling through the air, represented by C_2, can be ignored in favour of the network of R_a and C_a, due to the higher conductivity and permittivity of the active layer compared to air. The analysis of crosstalk in SOI substrates (chapter 6) showed that for two contacts on silicon the capacitive coupling is only visible at high frequencies because low frequencies are dominated by the conductive coupling through R_a. The trade-off between isolation and substrate cut off frequency can be seen in Figure 6.3. At the same time, high frequencies are dominated by the equivalent vertical capacitance to ground through the different layers of the GPSOI,

which also defines the ac loading frequency and is much higher in value than C_a. Furthermore, the combination of low crosstalk (<-60 dB) at frequencies above 20 GHz and the dominance of the vertical capacitances to ground, has resulted in screening of the measurement by probe crosstalk. Hence, it is safe to assume that the effect of C_a will not be visible, since it is a very high frequency effect and consequently may be ignored with potentially little loss of model accuracy.

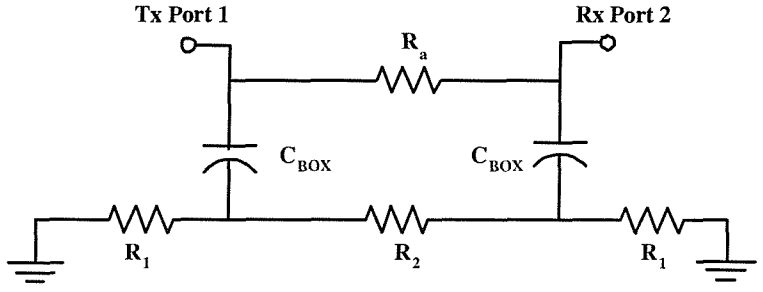


Figure 7.9: A simplified compact lumped element GPSOI crosstalk model.

A further simplification may be achieved by ignoring the effect of the finite ground plane resistance, manifested through R_1 and R_2. The effect of R_2 is only visible at very high frequencies at the analysis of the buried ground plane substrates before the addition of the active layer. The significance of this effect was extracted indirectly through electromagnetic and lumped model analysis because of the dominance of probe crosstalk at high frequencies. For similar reasons to those mentioned for C_a, and because of its small value (<3 Ω), R_2 is not expected to have a significant contribution to the model's overall s_{21} response.

A simplified version of the lumped model of crosstalk in GPSOI substrate is shown in Figure 7.9. It has to be noted that the topology of this model remains the same regardless of the nature of the Tx/Rx nodes. For instance, if the Tx/Rx pads are metal-on-oxide pads (Figure 7.10), an additional capacitance C_{TOP} is introduced that couples the noise to the underlying GPSOI substrate through the surface layer of oxide. Similarly, when diode Tx/Rx pads are considered (Figure 7.11), the capacitance of the depletion region of each junction C_J exists instead of C_{TOP}. Although the topology of the model remains the same, the values of the remaining components may be different between the two cases, because of the different values of the impedance associated with these two capacitances.

7.5 Electromagnetic Analysis of the Buried Oxide Capacitance in a GPSOI Substrate.

The analysis of the capacitance though the different layers of the GPSOI is important, because it determines the amount of the lateral coupling and also the

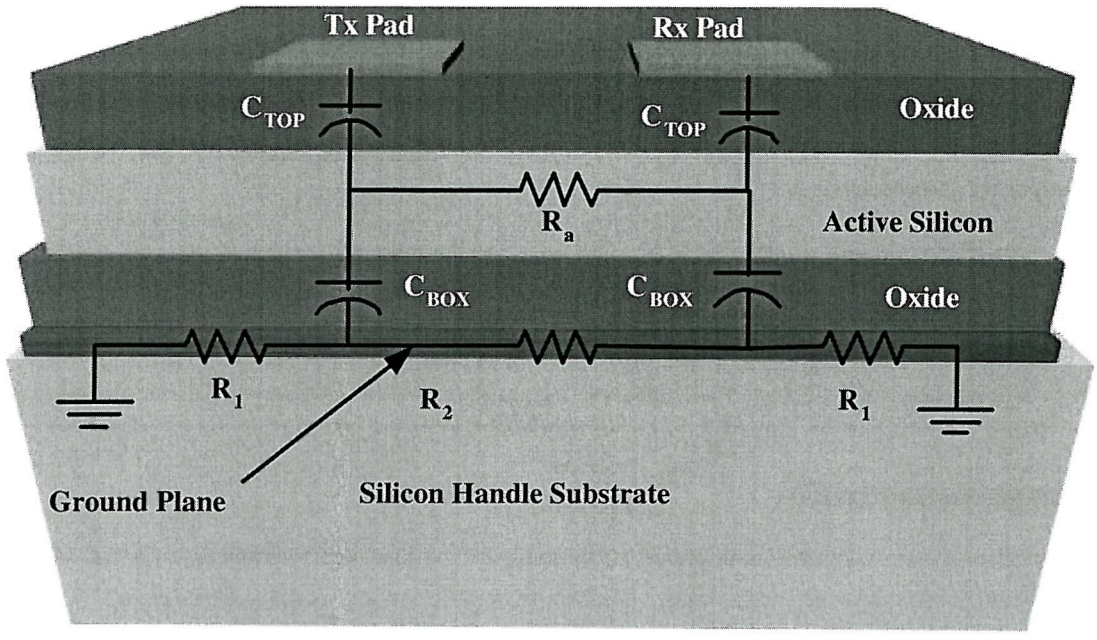


Figure 7.10: Lumped element crosstalk model of two metal-on-oxide pads fabricated on the GPSOI substrate.

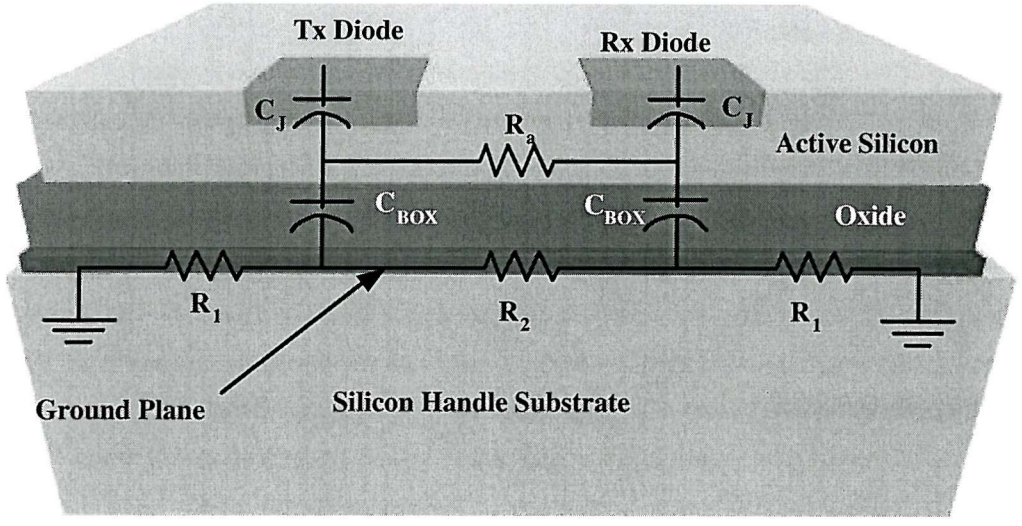


Figure 7.11: Lumped element crosstalk model of two diode Tx/Rx pads fabricated on the GPSOI substrate.

loading frequency of the structure, which may impose a limitation on ground plane SOI technology. The analysis of this capacitance is not entirely straightforward, as it involves a multilayer substrate with a layer that possesses both dielectric and conductive properties (the active layer). Electromagnetic simulations are therefore employed in order to investigate the value of this capacitance in three different substrate configurations.

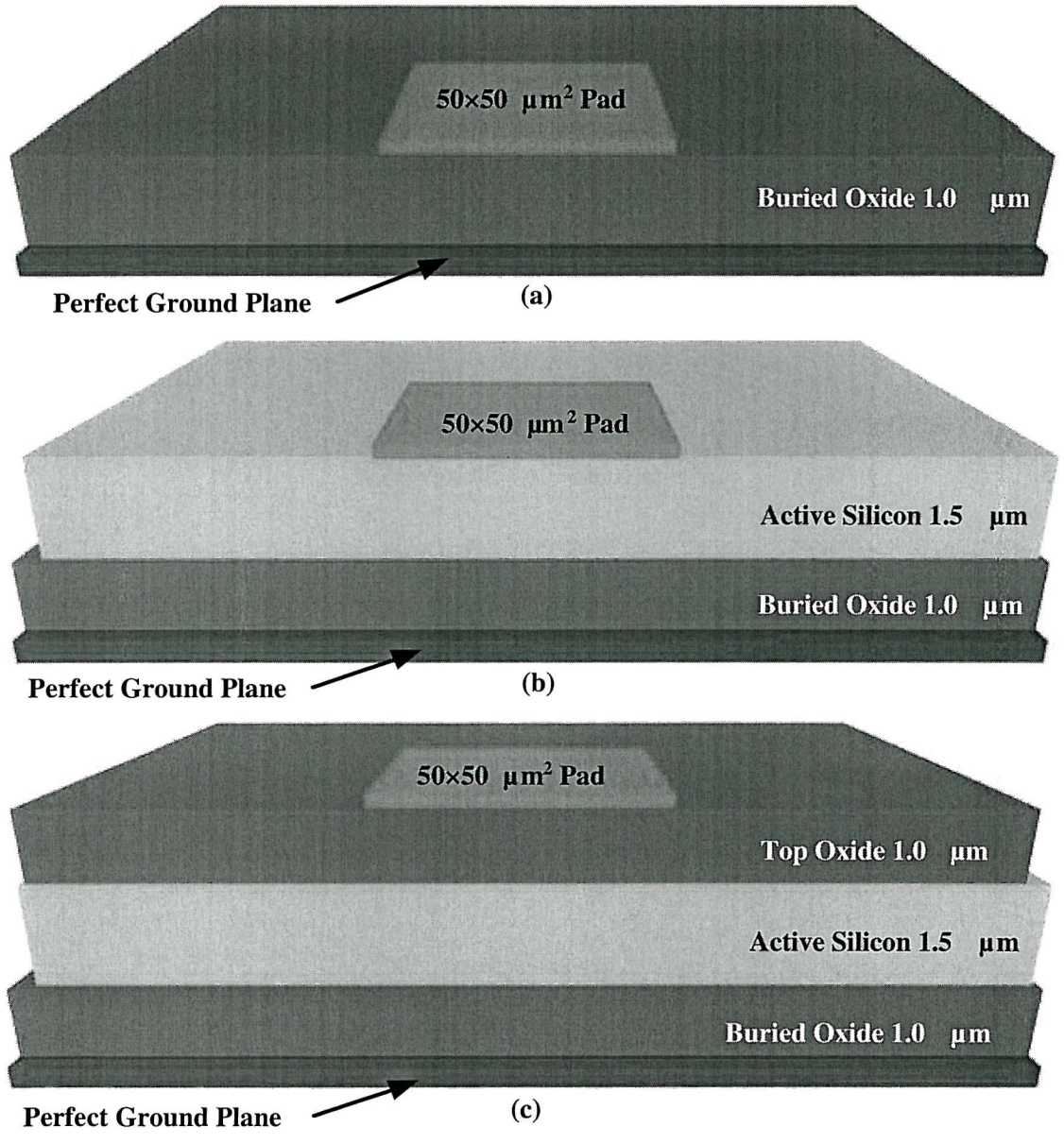


Figure 7.12: 50×50 μm^2 pad on: (a) 1.0 μm of oxide (b) 1.5 μm silicon on oxide 1.0 μm (c) on 1.0 μm of oxide on GPSOI. A ground plane exists at the bottom of each structure.

Initially, a 50×50 μm^2 zero thickness pad is simulated on top of 1.0 μm of oxide (equal to the buried oxide thickness), which lies over a ground plane (Figure 7.12). The capacitance of the pad to the ground plane is expected to have at least the

value calculated by a parallel plate formula, with the top plate being the pad and the bottom the ground plane. Fringing fields are expected to increase the total value since the ground plane is also infinite in dimension.

The capacitance is extracted from the following formula at very low frequencies as close to dc as possible.

$$C = \frac{imaginary(y_{11})}{2 \cdot \pi \cdot frequency} \tag{7.1}$$

When the active layer is added above the oxide, a different layer of capacitance is expected because of the conductivity of this layer. The pad now makes contact to a conductive layer, which now become the top "plate" of the parallel plate capacitance. If the resistivity of the active layer was zero, then the total capacitance would be infinite, as the entire active layer would be charged with the potential of the pads. In the opposite case, if the conductivity was zero, then the active layer would behave as a dielectric and the total capacitance would be the series combination of the individual capacitances through the consecutive layers of the substrate stack, supplemented by the fringing capacitances as well. The finite resistivity of the active layer that tends to make it behave more like a conductor than a dielectric causes the buried oxide capacitance to increase. This increase can be viewed as an increase of the "top" plate area of the buried oxide capacitor, due to lateral spreading of the electric field lines along the active layer. The spreading increases the effective top "plate" area to a value larger than 50×50 μm^2.

Finally, an additional layer of 1.0 μm of oxide is added above the GPSOI layer stack. The substrate layer stack now is similar to the case of metal-on-oxide Tx/Rx pads on GPSOI. The additional top oxide capacitance dominates because of its much lower (approximately 10 times) value compared to the buried oxide capacitance. The total capacitance is therefore determined by the top oxide capacitance that determines the amount of electric field lines that enter the active layer. The results of this analysis are summarized in Tables 7.1 and 7.2

	Extracted	Parallel Plate Formula	% Error
C_{BOX}(pF)	0.092	0.086	6.5

Table 7.1: Extracted and calculated value of the buried oxide capacitance for a buried ground plane substrate without a silicon active layer.

The buried oxide capacitance in the simulations without the active layer can be predicted with a parallel plate capacitance formula with 6.5% error. The error represents the fringing capacitance that is not taken into account by the formula. The addition of the active layer increases the total capacitance to 0.5 pF approximately

	Extracted
C_{BOX} without top oxidation (pF)	0.517
C_{TOTAL} with top oxidation (pF)	0.077

Table 7.2: Extracted and calculated values of the buried oxide capacitance for a buried ground plane substrate with a silicon active layer and top oxidation.

six times higher than before. When, however, the top oxide is introduced the total capacitance is reduced to 0.077 pF. This latter result is very significant because it shows how the vertical capacitance varies between the two GPSOI crosstalk models with metal-on-oxide or diode Tx/Rx pads, due to the different value of C_{TOP} and C_J respectively. C_{TOP} is approximately ten times smaller than C_J as shown in Chapter 6. On the other hand, the extracted value of the buried oxide capacitance according to Table 7.2 is much closer to the value of C_J. Consequently, the series combination of the two will result in a higher value compared to the metal-on-oxide Tx/Rx case.

7.6 Experimental Verification and Model Validation

Test structures with metal-on-oxide and diode Tx/Rx pads were fabricated on GPSOI substrates. The separation between the Tx and Rx pads was varied from 75 μm to 200 μm. The GPSOI substrate itself consisted of 1.0 μm of buried oxide and 1.5 μm of active silicon with a doping of 10^{16}cm^{-3}. The handle substrate resistivity was 9-15 Ω.cm. An insulating layer of 0.8 μm of oxide was initially grown on the surface of the GPSOI but subsequent processing steps have increased its thickness to approximately 1.0 μm. The junction depth for the Tx/Rx diode pads was 0.5 μm.

Measurements of the magnitude of s_{21} in the frequency range of 0.5 – 50 GHz from test structures with diode and metal-on-oxide Tx/Rx pads are shown in Figures 7.13 and 7.14, respectively. Appropriate open structures were also designed and the effects of the probe pads and the surrounding coplanar structure were subtracted.

The topology of a substrate crosstalk model that has been qualitatively derived through the electromagnetic simulations at the beginning of this chapter and the conclusions drawn from the SOI and buried ground plane analyses of chapters 4 and 6 is shown in Figure 7.15. The top oxide and junction capacitances are modelled by C_{TOP} and C_J depending on the nature of the Tx/Rx pads. The coupling through the conductive active layer is modelled by R_a and the buried oxide capacitance by C_{BOX}.

The values of the different model elements for two test structures with diode and metal-on-oxide Tx/Rx pads separated by 100 μm are shown in Table 7.3. The

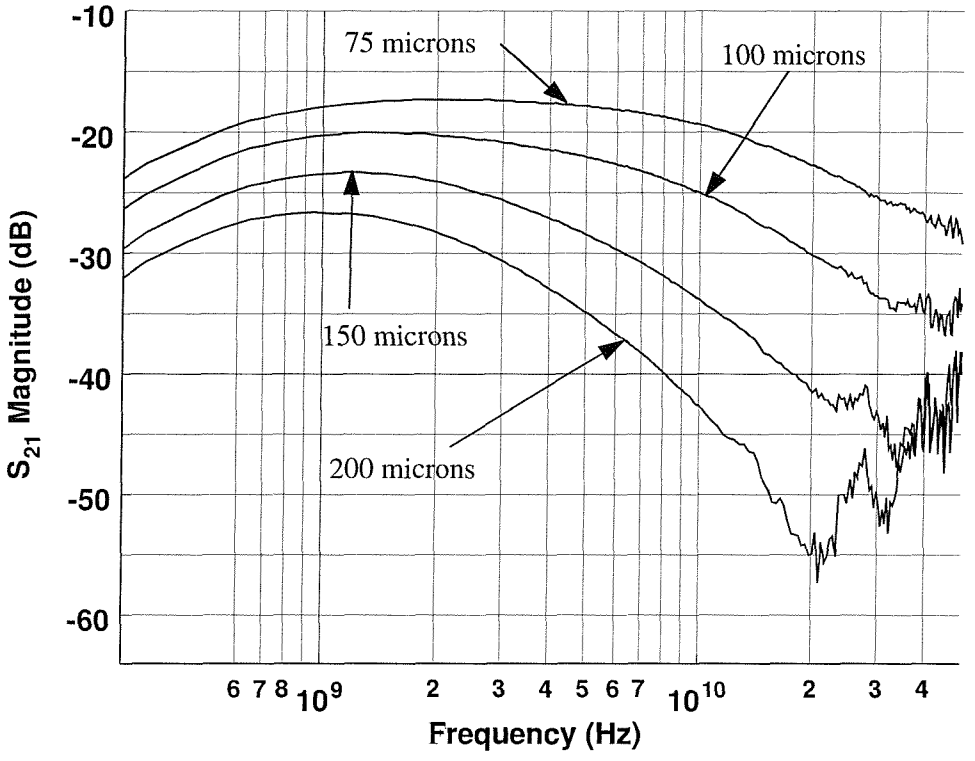


Figure 7.13: De-embedded measurements from test structures on GPSOI with diode Tx/Rx pads separated by 75, 100, 150 and 200 μm.

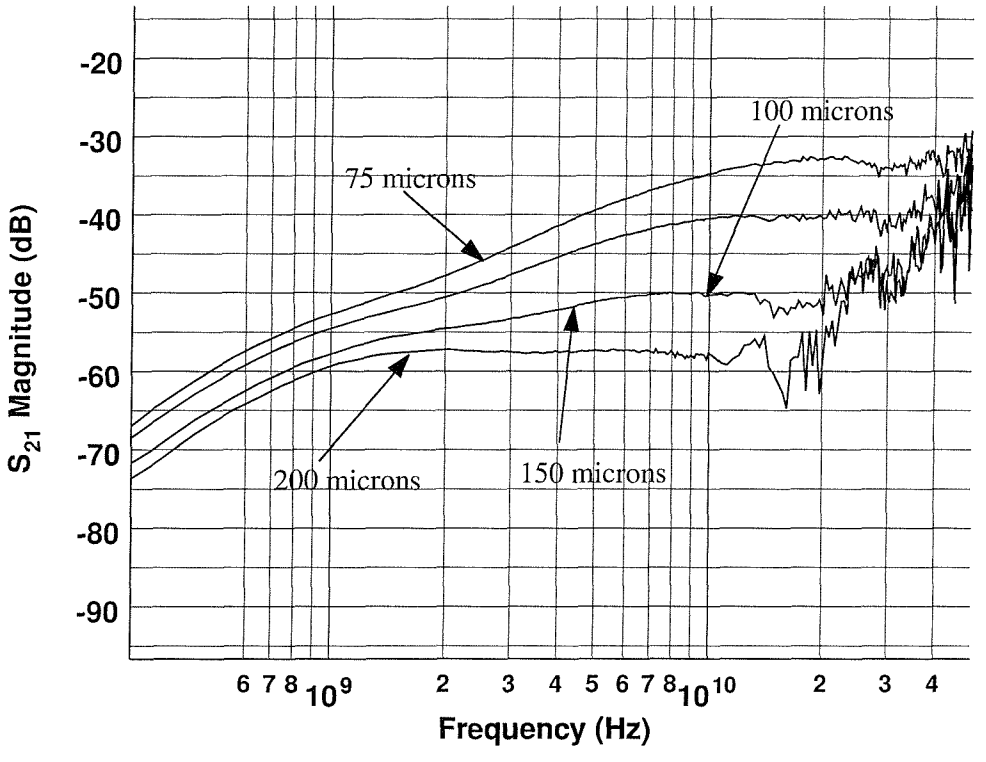


Figure 7.14: De-embedded measurements from test structures on GPSOI with metal-on-oxide Tx/Rx pads separated by 75, 100, 150 and 200 μm.

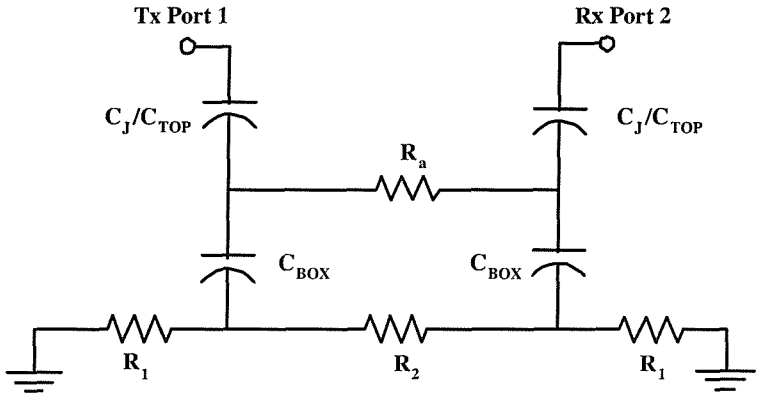


Figure 7.15: Equivalent GPSOI substrate crosstalk model, applicable to both diode and metal-on-oxide Tx/Rx pads.

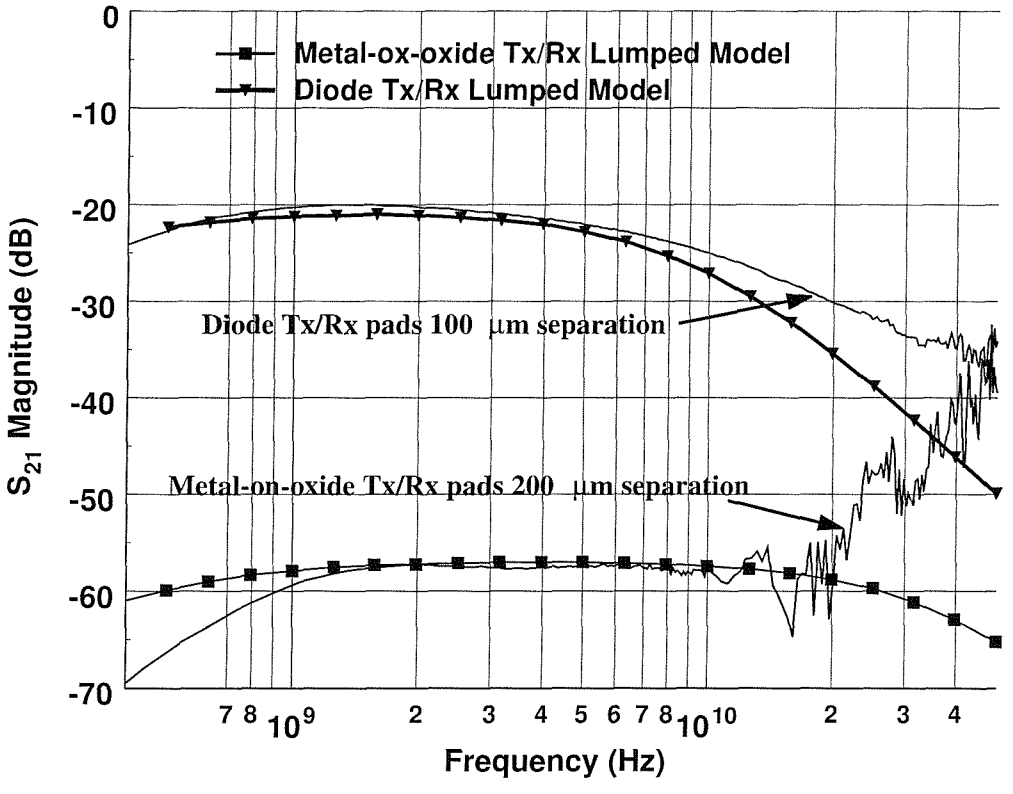


Figure 7.16: Model validation for two GPSOI test structures with 100 μm diode Tx/Rx pad separation and 200 μm metal-on-oxide Tx/Rx pad separation.

value of R_a is taken from the analysis of SOI crosstalk of chapter 6, while C_{BOX} is estimated from the electromagnetic analysis in this chapter in Tables 7.1 and 7.2. The model s_{21} characteristic for those values is plotted against measurements in Figure 7.16. Good agreement (<10% error up to 10 GHz and <30% up to 50 GHz) is accomplished over the entire frequency range. The model parameters for the metal-on-oxide case are valid for high Tx/Rx separations (i.e. 200 μm) and they were fitted for good model accuracy. However, for smaller Tx/Rx separations this specific model topology tends to collapse, as it exhibits an increase of crosstalk at a rate of 20 dB per decade that cannot be justified with values calculated from the theory. Such behaviour may be attributed to additional coupling paths through the top oxide and the air above the structure that become significant, as the Tx/Rx spacing is decreased and tend to alter the topology of the equivalent model. Analytical calculation of these components may prove to be difficult due to the multilayer nature of the substrate. Hence, Figure 7.16 only shows the model response for a separation of 200 μm.

	Diode Tx/Rx pads	Metal-on-oxide Tx/Rx pads
C_J or C_{TOP}(pF)	1.2	0.086
R_a Ω	480	750
C_{BOX} (pF)	0.50	0.75

Table 7.3: Crosstalk model parameters of two diodes and metal-on-oxide Tx/Rx pads separated by 100 and 200 μm respectively.

7.7 Active Layer Thickness and Crosstalk

Throughout his work, the active layer thickness of the SOI substrates was a lot higher than any junction diode depth. Typical thicknesses were between 1.5 and 2.0 μm and all presented measurement data came from partially depleted diode Tx/Rx pads. The GPSOI substrate, however, is manufactured by a process that involves grinding and polishing of the active wafer down to the desired active layer thickness. Inevitably, the active layer thickness varies significantly across each wafer. Figure 7.17 documents this variation after cleaving a GPSOI wafer.

According to Figure 7.18, fully depleted Tx/Rx diodes exhibit lower crosstalk than their partially depleted counterparts. The improved isolation is attributed partially to the higher resistivity of the active layer, due to its lower thickness. In addition, the effective area of the fully depleted Tx/Rx diodes is smaller because only the junction sidewall couples noise to the active layer. The junction sidewall (or depth) is only 0.5 μm compared to the 50 μm of the bottom part that makes contact to the buried oxide and couples noise to the ground plane. Consequently, the diodes are reduced to p^+ top down contacts, through the active layer, to the surface of the

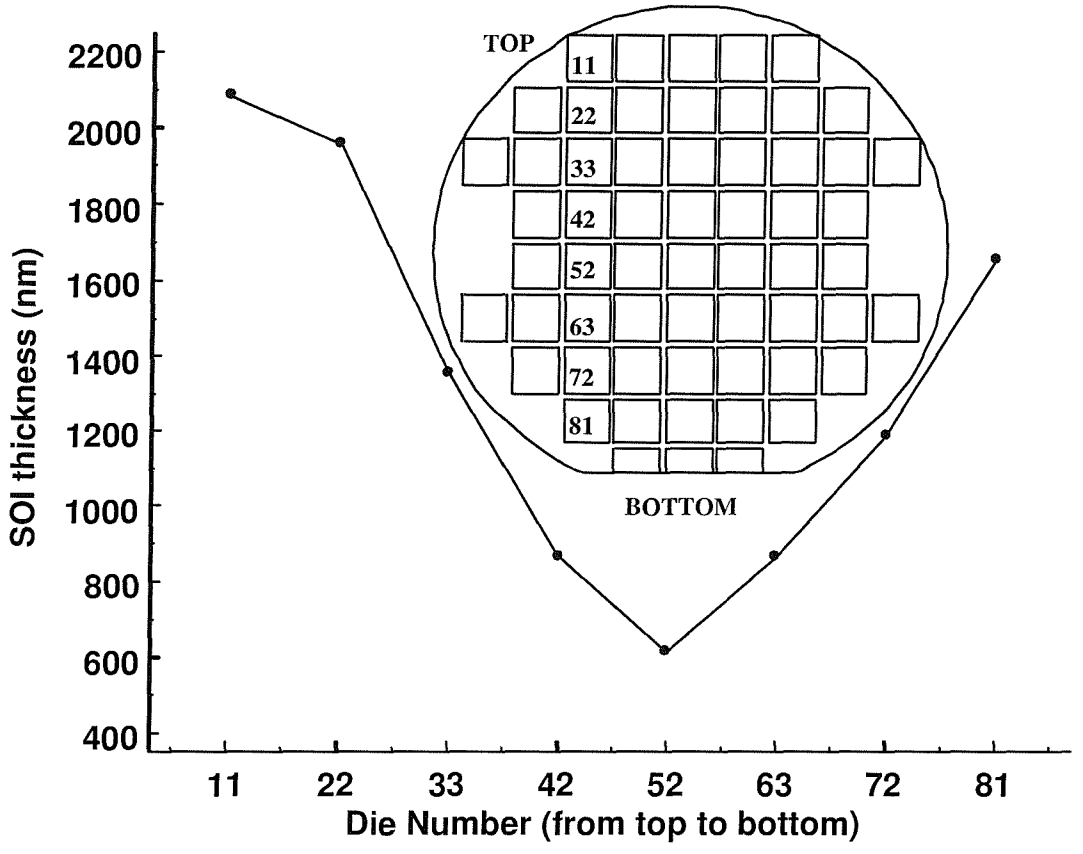


Figure 7.17: Active layer thickness variation on a GPSOI wafer.

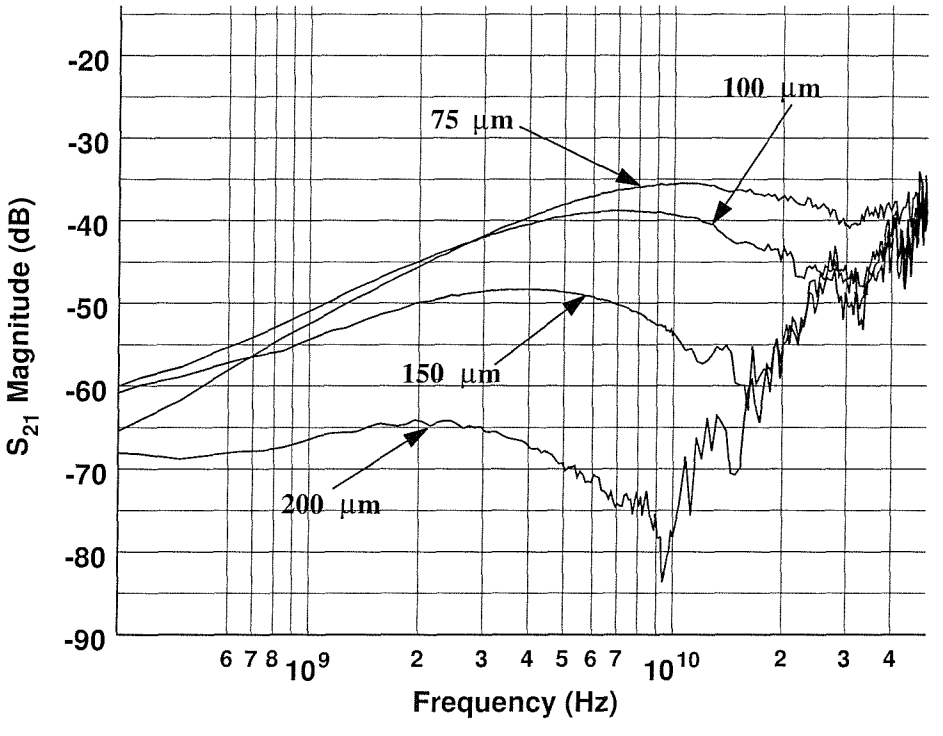


Figure 7.18: Measurements of signal isolation between two diode Tx/Rx pads on a GPSOI substrate with 0.62 μm of active silicon. The junction depth is 0.5 μm.

buried oxide. Further investigation of this behaviour should be pursued, so that the trade-offs between isolation and device performance could be identified.

7.8 Discussion

The objective of the studies in this chapter has been to characterise the isolation performance of the GPSOI and compare it with SOI. The studies of SOI substrate crosstalk in chapter 6 have revealed their low isolation capabilities, due to the presence of two noise coupling paths along the active and handle silicon substrates. The active layer's low resistance is responsible for most of the coupling throughout much of the frequency range of interest. Only at very high frequencies does capacitive coupling through both silicon layers begin to increase crosstalk significantly.

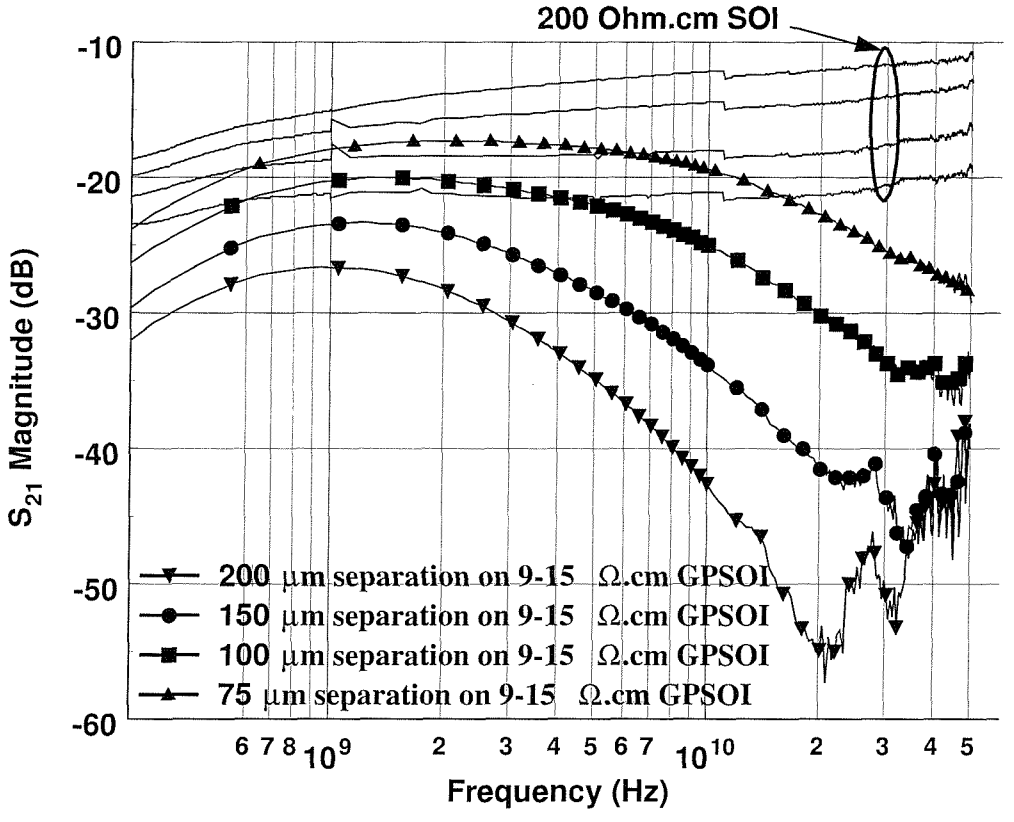


Figure 7.19: Comparison of signal isolation between diode Tx/Rx pads in higher resistivity (200 Ω.cm) SOI and standard (9-15 Ω.cm) GPSOI substrates for different separations.

The ground plane of the GPSOI substrate is intended to shield the handle substrate from any interference induced by the devices on the active layer. Figure 7.19 compares the same test structure of two diode Tx/Rx pads separated by 100 μm on standard (9-15 Ω.cm) GPSOI and high resistivity (200 Ω.cm) SOI. The only difference between the two configurations is the presence of the buried ground plane.

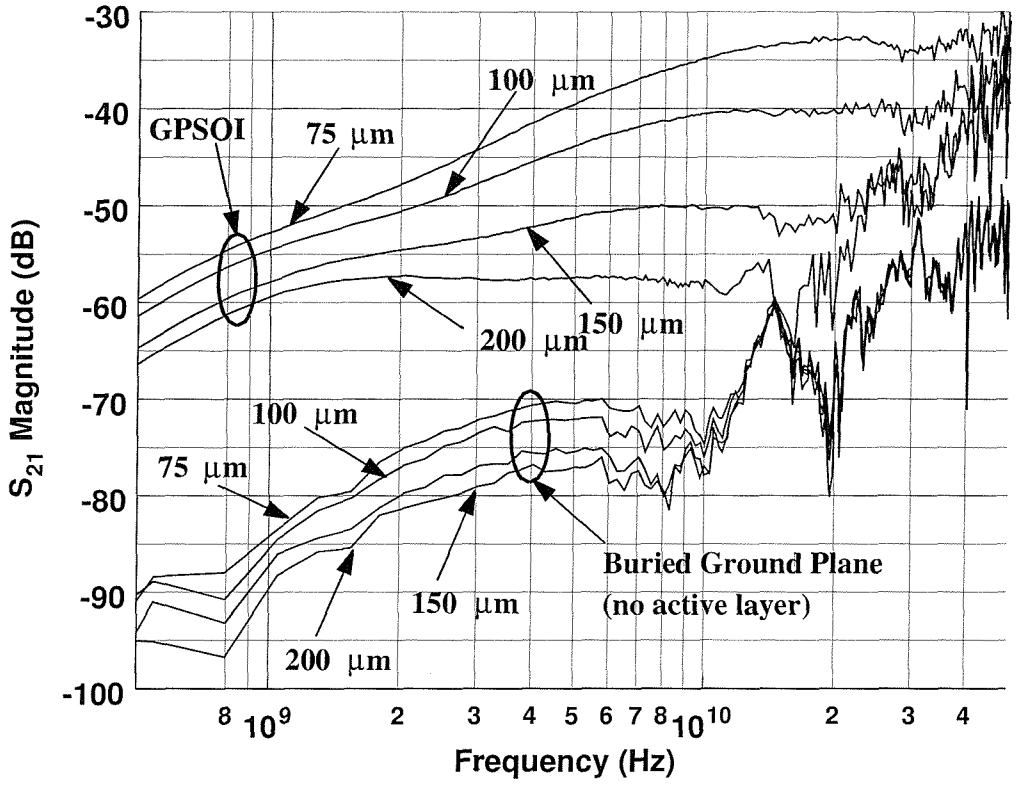


Figure 7.20: Comparison of signal isolation between metal-on-oxide Tx/Rx pads standard (9-15 Ω.cm) GPSOI and buried ground plane substrate (without an active layer) for different separations.

The observed improvement is only approximately 5 dB at low frequencies and corresponds to the coupling through the handle wafer. The dominant coupling is still through the active layer and is not significantly reduced, until higher frequencies are reached and the buried oxide capacitance begin to provide a low impedance path to ground rather than the Rx pad.

Another comparison can be made between the buried ground plane substrates of chapter 3 and the GPSOI test structures with metal-on-oxide Tx/Rx pads. The difference now between the two structures is the presence of the active layer, which is sandwiched between the top and buried oxides of the GPSOI. The isolation performance degradation can be as high as 40 dB, as shown in Figure 7.20. An additional suppression strategy is absolutely vital in order to minimise the coupling through the active layer. Such a strategy may come in the form of guard rings, dielectric trenches or a Faraday cage structure, which is presented and discussed in the next chapter.

7.9 Conclusions

The substrate crosstalk behaviour of GPSOI substrates has been investigated in this chapter. Electromagnetic simulations have been carried out in order to analyse that behaviour in conjunction with the studies presented so far in this work. A lumped element model has been presented and validated against measurements. Good agreement is shown when diode and widely separated metal-on-oxide Tx/Rx pads are considered. The GPSOI substrate with diode Tx/Rx pads does not offer significant improvement over the SOI substrate at low frequencies. Higher frequencies tend to exhibit higher isolation performance, but still a lot worse than the buried ground plane test structures (chapters 3 and 4). The observed high levels of crosstalk are caused by the coupling path through the active layer of the SOI. Since the handle substrate is shielded, the small noise suppression improvement of the GPSOI over the SOI test structures represents the coupling path through the handle substrate,which has proved not to be significant. Consequently, a noise suppression measure that minimises the coupling through the active layer is necessary.

Chapter 8

A Novel Faraday Cage Structure For Advanced Substrate Crosstalk Suppression

8.1 Introduction

As shown in Chapter 7, the introduction of a ground plane underneath the insulator of a SOI substrate, results in reduction of crosstalk of at least 5 dB. There is however still a significant substrate coupling path that contributes to the total amount of crosstalk through the active silicon layer of the GPSOI. Previous studies [1], [7], [8], [9], [23] have shown techniques and examined their efficiency in reducing substrate crosstalk through the active layers. These techniques include the introduction of dielectric trenches that isolate the Tx and Rx pads at dc. Diffused guard rings have also been shown to decrease the amount of crosstalk through the active layer. [1] and [7] have shown that at high frequencies, even when trenches and guard rings are combined, the only effective crosstalk suppression measure is guard rings, since the dielectric trenches and buried oxide layers become "transparent".

A different approach that utilises a Faraday cage structure for reducing crosstalk has been recently presented by Wu et. al [4]. A Faraday cage combines the advantages of dielectric trenches and guard rings. Having a dielectric trench only provides crosstalk suppression until the trench becomes transparent. On the other hand, guard rings are not as efficient at lower frequencies as trenches, but they become the only means of noise suppression at high frequencies.

A novel Faraday cage structure that is fabricated on a GPSOI substrate is presented in this chapter. Details of the fabrication process are discussed and measurement data from fabricated test structures are also shown. Comparisons with previously

published data and other technologies reveal that, to the best of the author's knowledge, such a Faraday cage structure provides the highest degree of isolation ever recorded on SOI substrates.

8.2 Faraday Cage Structure Description and Fabrication

A Faraday Cage structure is fabricated in an identical way to the test structure of the GPSOI substrate. An illustrative cross-sectional view of such structure is shown in Figure 8.1, while Figure 8.2 shows an SEM image of a fabricated structure.

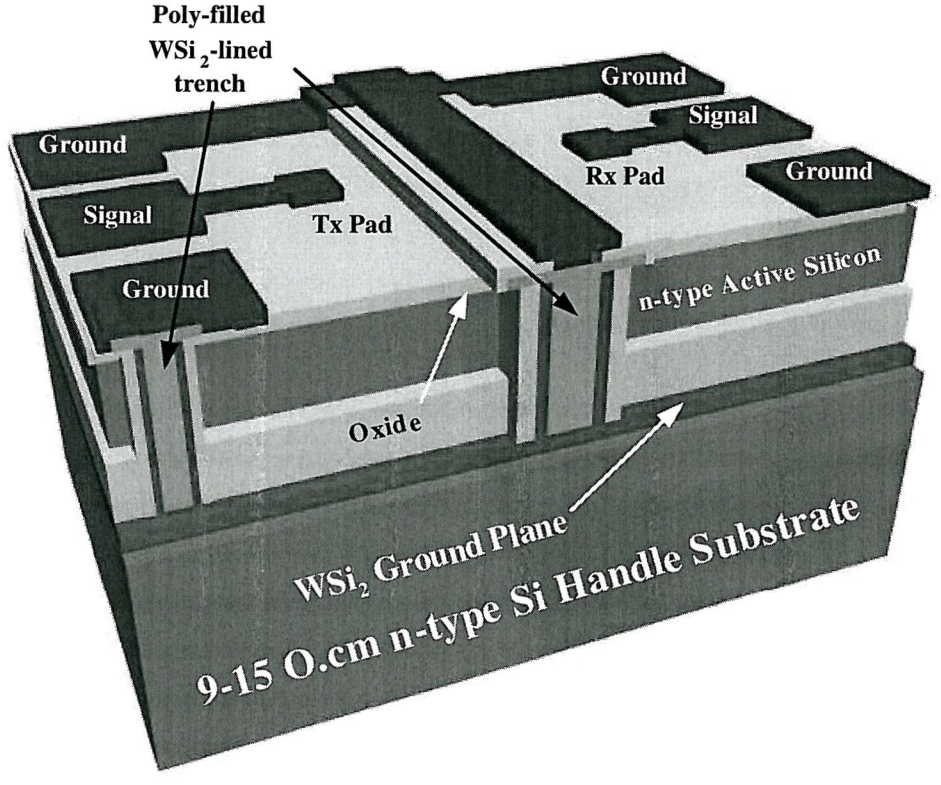


Figure 8.1: Three-dimensional illustration of a Faraday cage structure realised on a GPSOI substrate

The Faraday Cage structure contains a trench between the Tx/Rx pads that forms a conductive wall and extends across the entire width of the structure. The Faraday cage trench is connected to the ground plane, and hence to the surface RF ground, via the metallisation at the surface. The trench width was designed to be 2 μm and is extended along the ground pads, so that it surrounds each Tx/Rx pad. The grounding of the ground plane is achieved through the trench, rather than the arrays of top-down contacts that was used so far in the GPSOI experiments. As in previous experiments, two types of Tx/Rx pads were fabricated: metal-on-oxide and diode Tx/Rx pads.

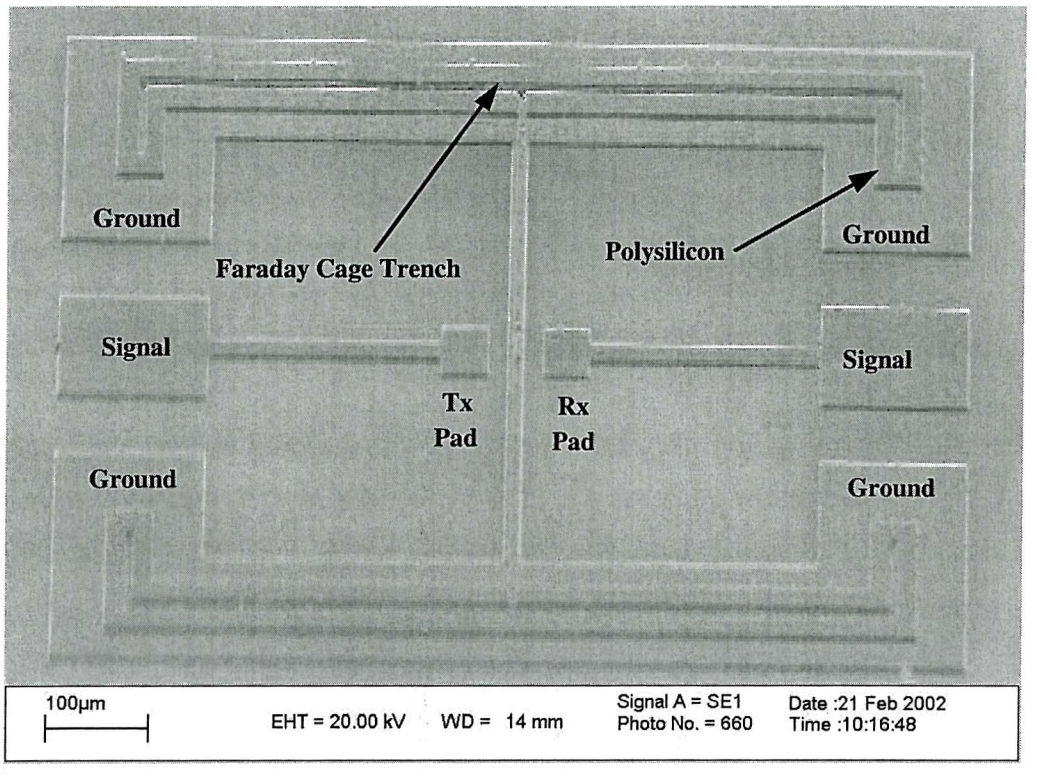


Figure 8.2: SEM plan view of a Faraday cage structure with metal-on-oxide Tx/Rx pads.

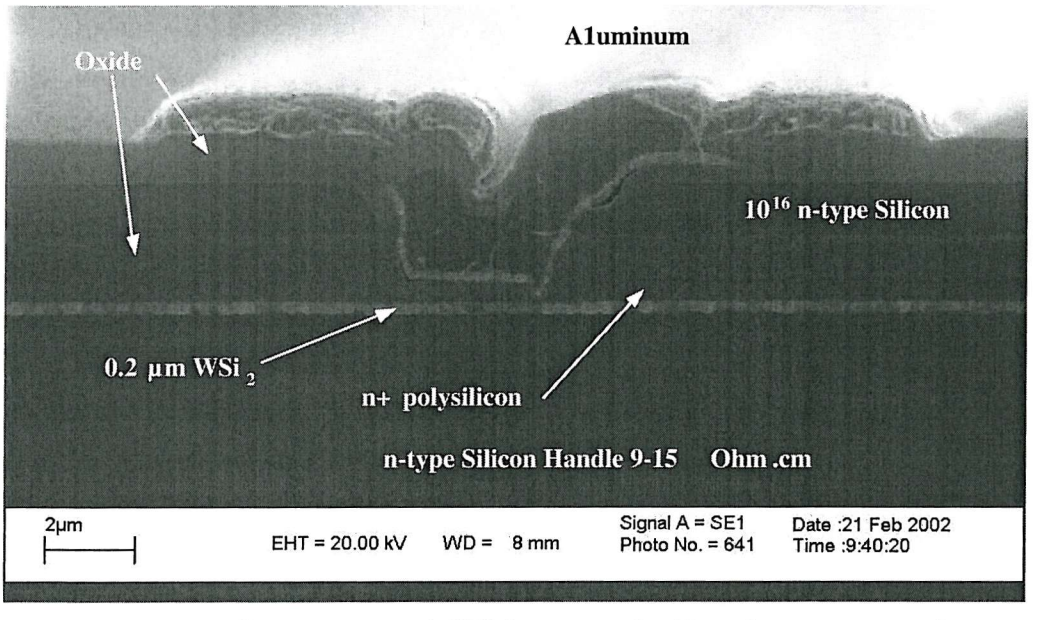


Figure 8.3: Cross-sectional SEM image of a Faraday cage trench.

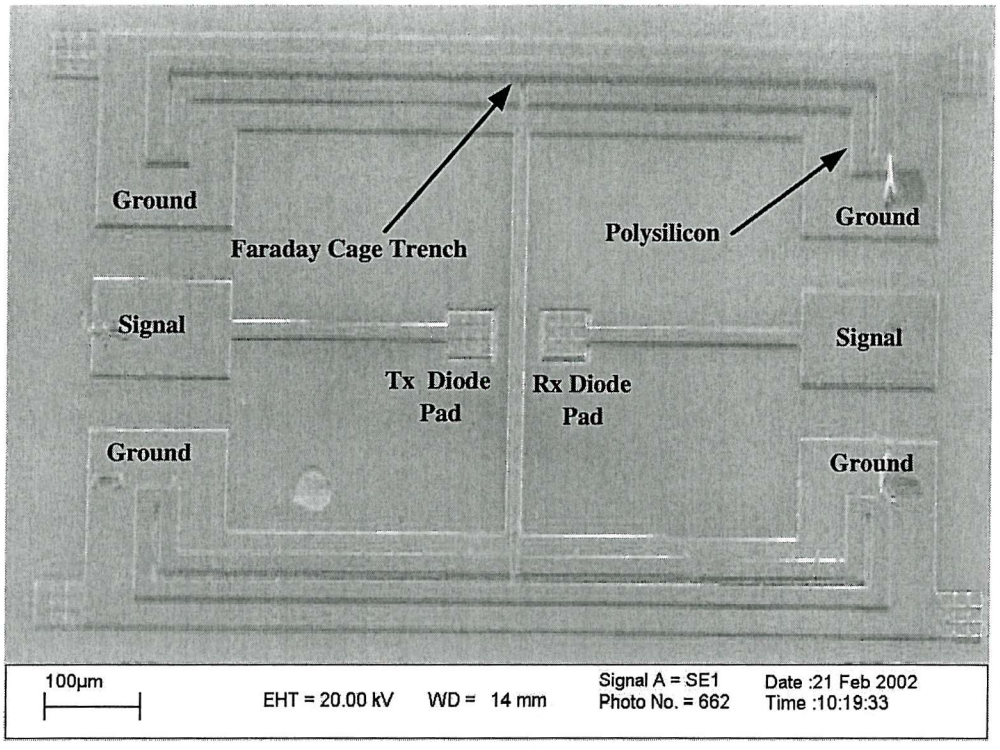


Figure 8.4: Plan SEM image of a Faraday cage test structure with diode Tx/Rx pads.

An SEM image of the Faraday cage trench is shown in detail in Figure 8.3. Fabrication of the trench is started by an anisotropic dry etch through the different layers of the GPSOI, until the buried WSi_2 plane is reached and exposed. Then an oxidation follows that forms the trench sidewall and surface insulating oxides. A blanket deposition of WSi_2 ensures that the trench is lined with WSi_2 before it is filled with n^+-doped polysilicon. The polysilicon layer is patterned in such way that completely covers the area where the trench is etched. This is done because the trench etch mask is used twice during processing. The first time it is used to etch the trench, and then re-used at the late stages of the process to etch at the same place the contacts between the top metallisation and the trench polysilicon. By covering the trench completely with polysilicon and extending the polysilicon pattern mask sideways, it is possible to minimise the risk of exposing the silicon active layer to the top metallisation due to any mask alignment errors.

It can be observed from Figure 8.3 that the Faraday cage fabrication was compromised, since the WSi_2 layer at the bottom of he trench is not connected to the WSi_2 layer of the ground plane, but it is connected to the n^+ doped layer between the WSi_2 and the buried oxide. This does not, however, indicate that either the ground plane or the Faraday cage are not properly grounded, since both of them are connected via the top metallisation the RF ground.

An SEM image of the fabricated Faraday cage structure for diode Tx/Rx pads is shown in Figure 8.4.

8.3 Measurement Results

The scattering parameters of the Faraday cage structures were measured using a HP 85109C on-wafer characterisation system in the frequency range of 500 MHz to 50 GHz. Tungsten tip air coplanar (ACP) probes were used of 150 μm pitch made by Cascade Microtech. Measurement results are shown in Figures 8.5 and 8.6.

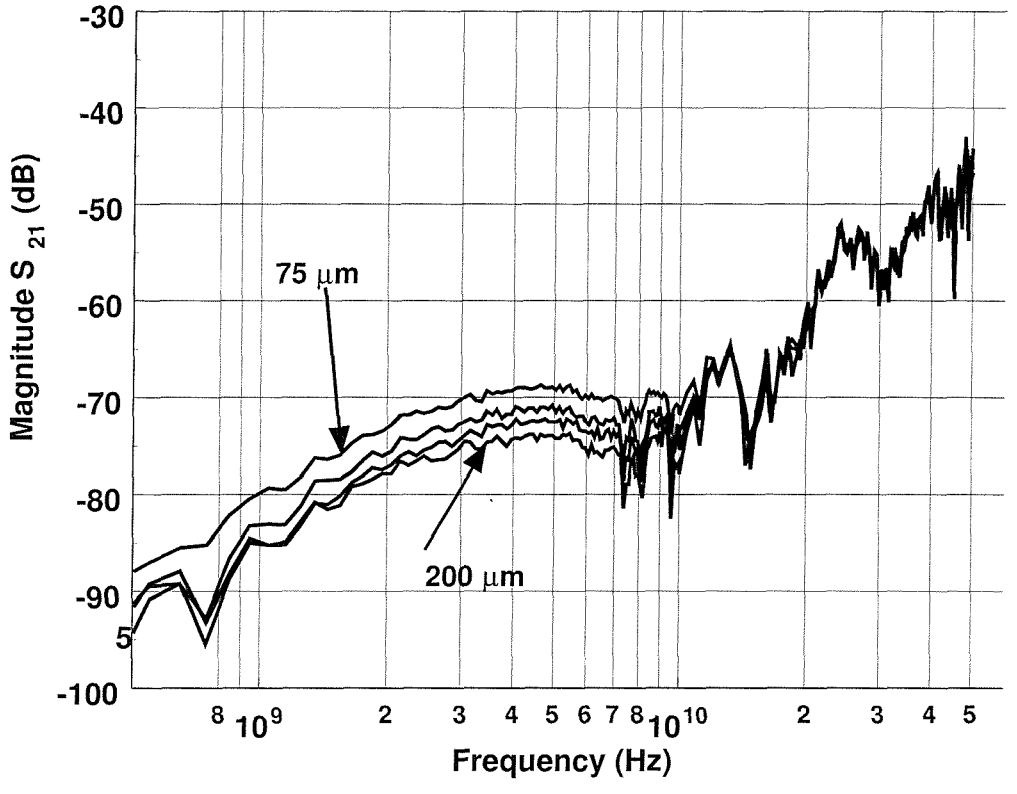


Figure 8.5: Magnitude of s_{21} measurements of Faraday cage test structures with diode Tx/Rx pads separated by 75, 100, 150 and 200 μm.

Figure 8.5 shows measurements of Faraday cage structures with separations varying from 75 to 200 μm. The structures consist of diode Tx/Rx pads as shown in Figure 8.5. The handle silicon substrate resistivity for all structures is 10 Ω.cm. The test structures have exhibited high degrees of isolation, ranging from –85 dB at 1 GHz for 200 μm Tx/Rx pads separation, to –68 dB at 5 GHz for 75 μm separation.

Similar results have been measured on the metal-on-oxide Tx/Rx pad test structures, which appear to exhibit slightly better isolation. Structures with metal on oxide pads have been consistently shown through the SOI and GPSOI crosstalk studies to exhibit lower levels of crosstalk. This is the case also for the Faraday

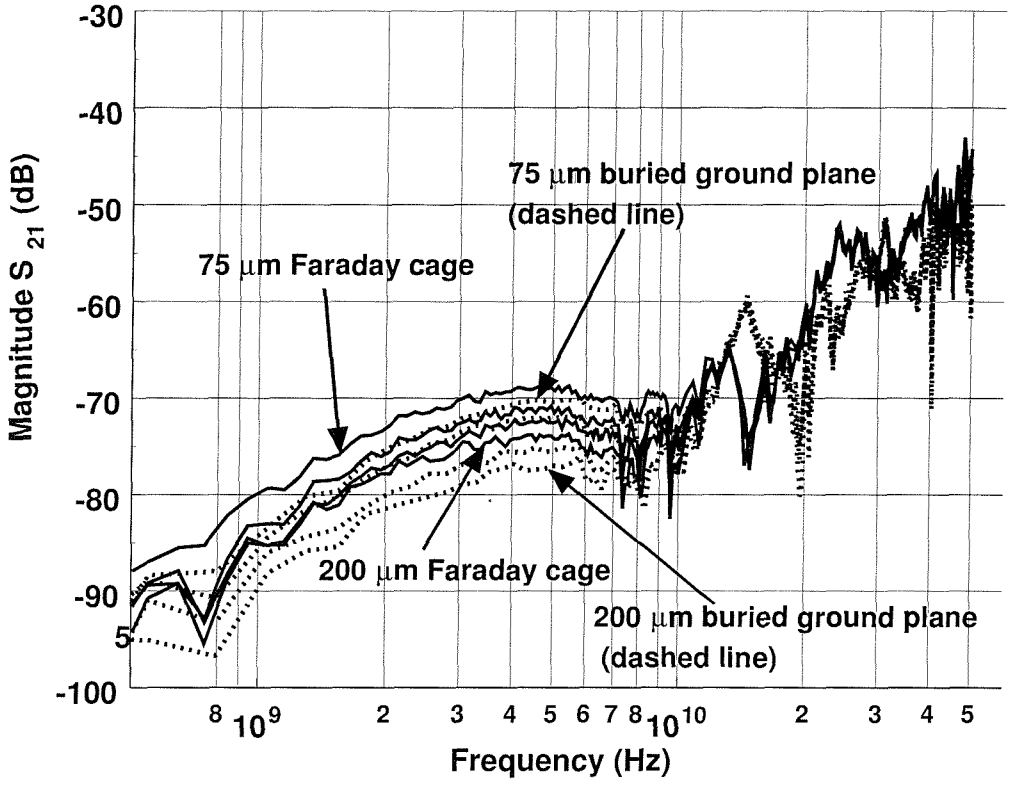


Figure 8.6: Comparison of s_{21} measurements between the Faraday cage test structures with diode Tx/Rx pads and the buried ground plane measurements of Chapters 3 and 4.

cage structures. However, the relative difference of the isolation performance between the two is now reduced to a very small amount that cannot be quantified and attributed to a specific property of a structure. Therefore, regardless of the nature of the Tx/Rx pads (or effectively the way the source noise signal is induced to the substrate), the Faraday cage is able to suppress the noise coupling in the same manner for both structures.

8.4 Analysis Using EM Simulations and Comparison with Buried Ground Plane Substrates

Careful observation of the absolute levels of crosstalk in the Faraday Cage structures shows that it is very similar to the measured s_{21} curves of the buried ground planes substrate test structures (Chapters 3 and 4). Figures 8.6 and 8.7 show how the Faraday cage measurements are compared to measurements from the buried ground plane studies. Both types of Tx/Rx pads are considered.

The two structures are fabricated on different substrates and different layout geometries involved in each case. For instance, the Tx/Rx pads are only separated by 1.0 μm of oxide from the ground plane in the buried ground plane structures,

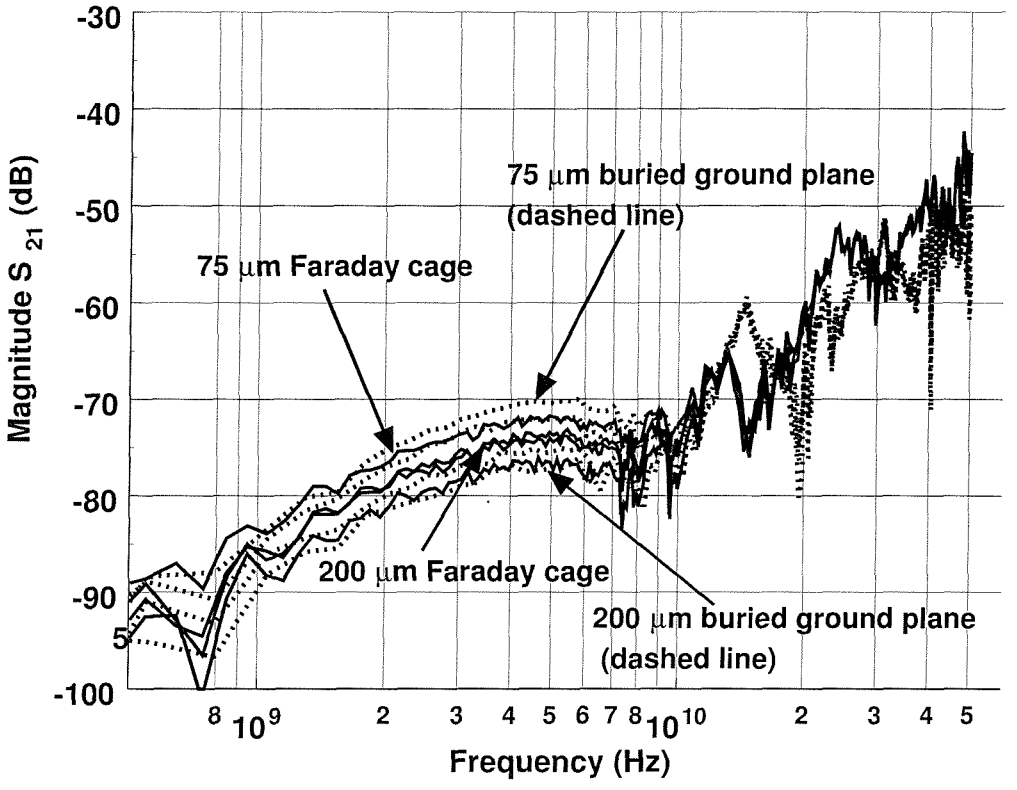


Figure 8.7: Comparison of s_{21} measurements between the Faraday cage test structures with metal on oxide Tx/Rx pads and the buried ground plane measurements of Chapters 3 and 4.

whereas the separation approximately triples in the Faraday cages with the addition of the active silicon and surface oxide layers. The Faraday cage also introduces a wall between the two pads that completely separates them up to the surface of the structure, blocking any potential coupling paths through the surface oxide and leaving only the path through the air.

The similar levels of crosstalk are an indication that a similar path exists with the Faraday cages. The Faraday cage trench introduces a line of symmetry along the middle of the structure. The structure is therefore divided into two identical halves that are completely isolated from each other up to the surface of the structure. The line of symmetry, however, cannot be extended to the layer of air above the structure because it will result in s_{21} being zero (or approaching $-\infty$ in decibels). In order for s_{21} to exist, there has to be a coupling path and as shown in Figure 8.8, this path exists only through the air above the structure.

From a modelling point of view, Figure 8.8 shows how the model of GPSOI crosstalk is reduced to a capacitive π-network with the addition of the Faraday cage trench. The only source of coupling is through the air and the capacitor C_2. C_2 is therefore expected to have similar values to those extracted in Chapter 4.

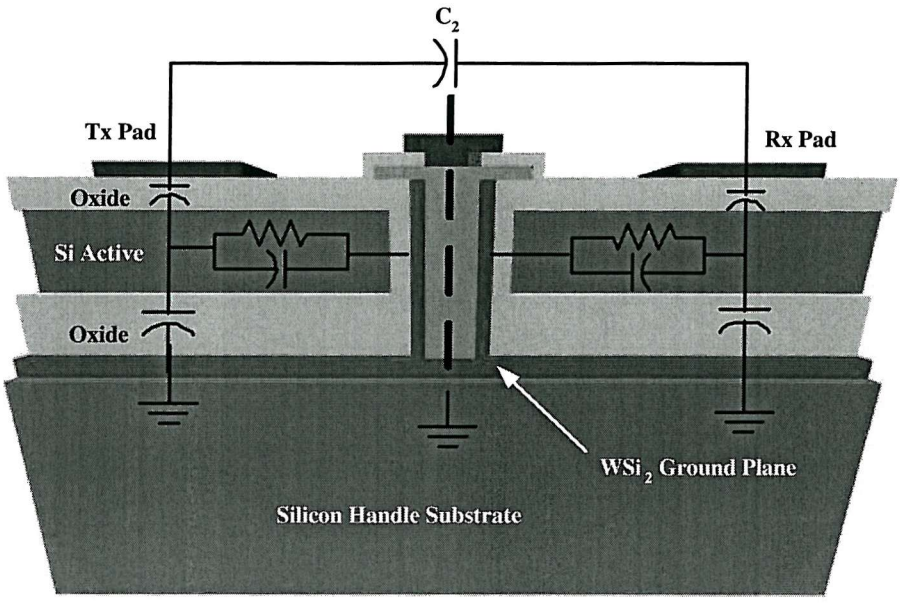


Figure 8.8: Three-dimensional illustration of the Faraday cage structure showing the symmetry line, imposed by the trench, that reduces the equivalent lumped element model to a simpler π-network. The resistances of the buried ground plane have been omitted.

Similar levels of crosstalk also indicate that the effect of the Faraday cage wall is negligible as regards to the amount of coupling through the air. The electric field between the Tx/Rx pads through the air is not affected by the Faraday Cage trench and only a negligible number of air field lines terminate at the surface metallisation of the trench wall. In other words, the field lines in both Faraday cage structures and buried ground plane structures that are responsible for the measured coupling, are located far away from the surface of the substrate and any additional surface metallisation between the Tx/Rx pads is not able to upset them significantly. The capacitive coupling at the surface of the structures is strong because of the higher dielectric constant of oxide and because the ground plane is located very close to the pads.

Throughout this work, planar quasi three-dimensional electromagnetic solvers have been used to simulate different structures. The third dimension is not fully simulated and therefore, it is not possible to visualize currents and field lines along that third dimension. Nevertheless, it is entirely possible to emulate the coupling through the air of a Faraday cage structure using the two dimensions that are fully simulated and be able to visualize the field lines at the substrate layers above the structure.

Simulations so far have been performed by entering the entire layout of the structure along the x- and y-axes (Figure 8.9). The third dimension along the z-axis was implicitly defined in the substrate definition but with little control of the shapes and geometries involved. Only thicknesses and dielectric properties could be defined but not shapes with finite dimensions. The current flow along the z-axis though vias was assumed to be constant and visualization of current and field lines was only possible along the x- and y-axes.

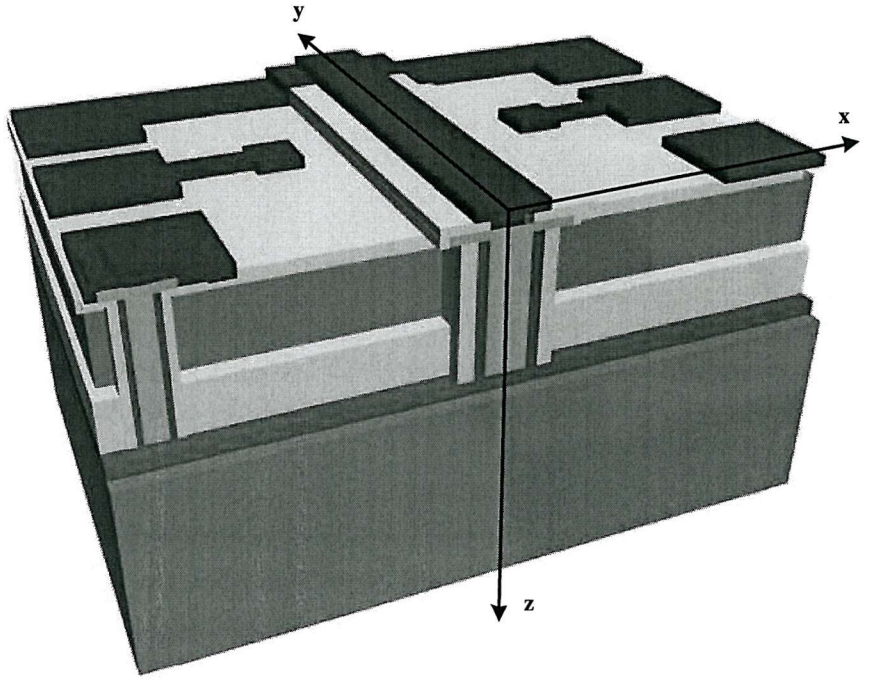


Figure 8.9: Three-dimensional illustration of the Faraday cage structure with the x, y and z-axes as defined for use by the electromagnetic solvers.

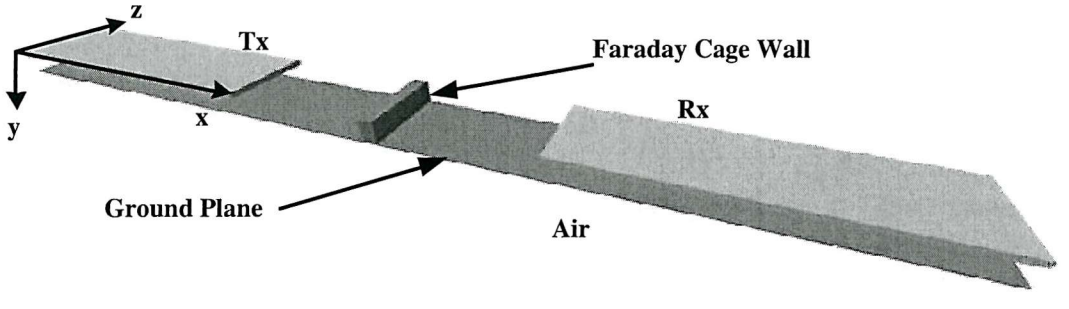


Figure 8.10: Graphical illustration of a strip line structure that along the x and y axes emulates the air coupling of the Faraday cage structures.

In order to visualise the field lines along the x and z axes, strips that emulate the part of the structure that is seen in a cross-section may be entered in the simulator. The disadvantage of this approach is that the dielectric between strips is assumed

uniform and therefore consecutive layers of oxide and silicon should be treated as a single dielectric. Such a strip structure is shown in Figure 8.10.

It consists of two conductor strips with 50 μm length and 1 μm width. The length is equal to the length of each Tx/Rx pad and the width to its thickness. A third strip that is spaced 3.0 μm away from the other two runs through the entire length of the structure and is connected to ground representing the ground plane underneath the two Tx/Rx pads. A short strip in the middle of the Tx/Rx separation distance emulated the Faraday cage wall. Since it is not possible to change the properties of the area between the ground strip and the Tx/Rx pads strips that entire structure is placed in air as its dielectric.

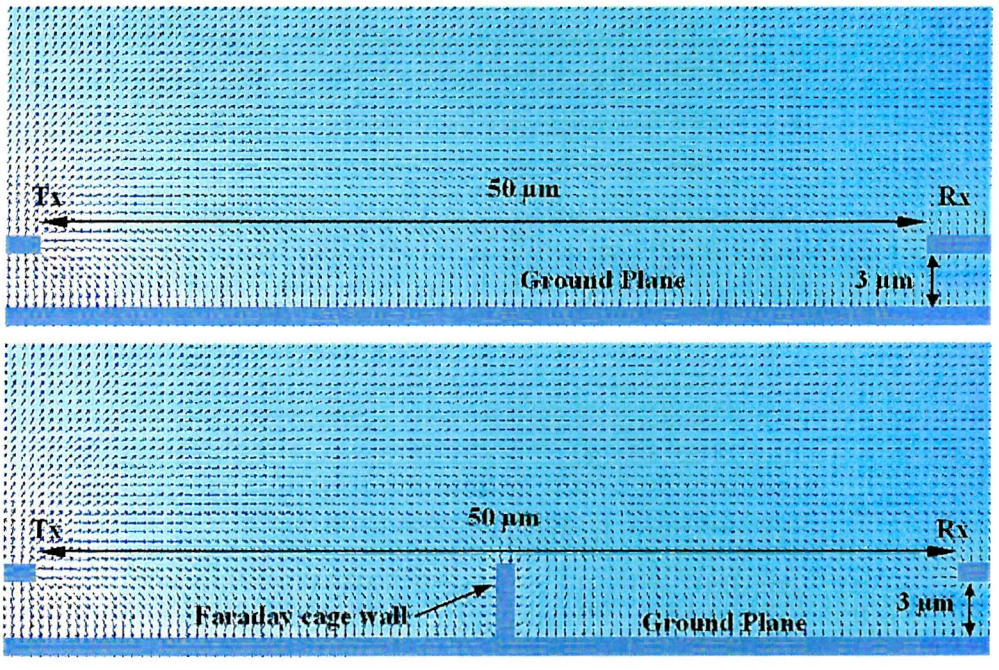


Figure 8.11: EM simulations of two strip lines in air emulating the electric field lines between Tx and Rx pads based on the structure of Figure 8.10, with and without the Faraday cage strip.

Figure 8.11 shows the field lines as vectors between the two pads through the air at a frequency of 5 GHz, where most of the highest crosstalk is measured. Most of the coupling occurs between each pad and the ground strip. The coupling between the Tx pad and the Faraday cage strip does not change significantly the pattern of the electric field. The coupling along the area where the surface of the structure is strong because of the close proximity to the buried ground plane. The Faraday cage completely isolates the Tx /Rx pads from each other by blocking any coupling through the active and oxide layers making at the same time the air component of the coupling the only and dominant crosstalk path.

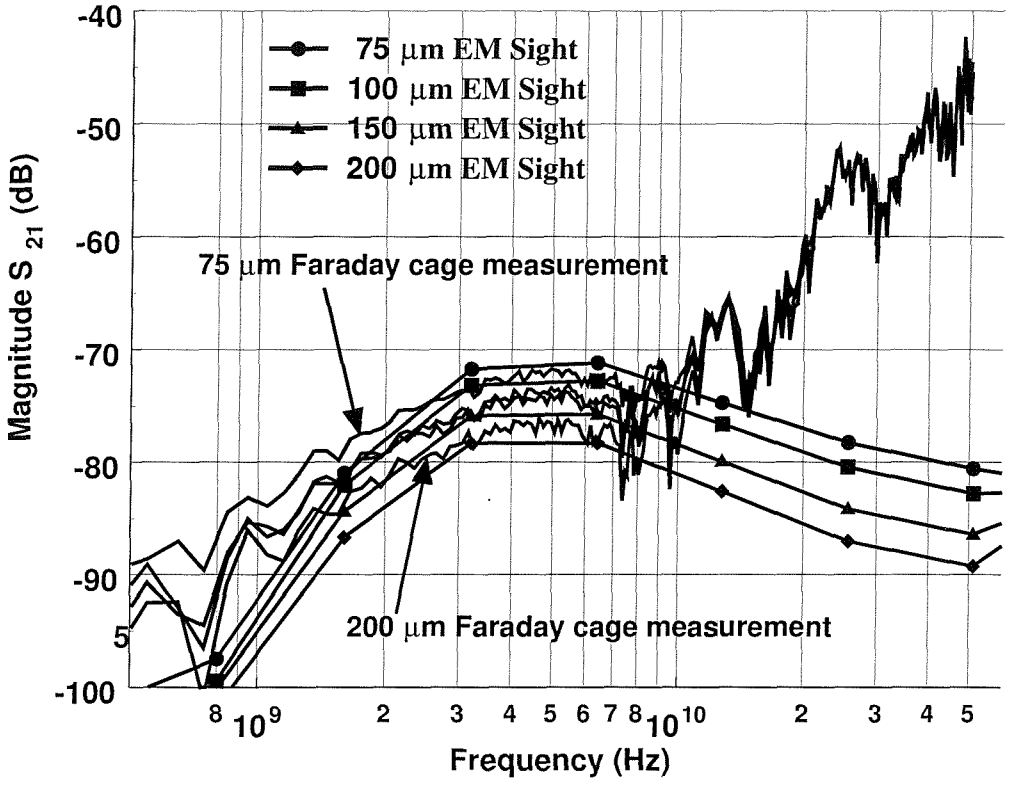


Figure 8.12: Electromagnetic simulations of the Faraday cage structures with metal-on-oxide Tx/Rx pads with EM Sight and comparison with measurements for different Tx/Rx separations.

More detailed electromagnetic modelling can be performed using a full three dimensional solver. *EM-Sight* simulation data from the Faraday cage structures with metal-on-oxide Tx/Rx pad are also shown in Figure 8.12 and verify the aforementioned qualitative analysis of the measurement data by achieving good agreement with the measurements.

8.5 Discussion

The superiority of the Faraday cage structures compared to SOI and GPSOI, where the only means of crosstalk suppression is the distance between the Tx/Rx pads is clearly shown in Figure 8.13. The active layer is a buried conductive layer that provides a low resistance path from the Tx to the Rx pads. The introduction of a ground plane does little to improve isolation since the active layer remains the dominant source of noise coupling. It is therefore essential to break this coupling path by introducing additional means of crosstalk suppression The advantages of dielectric trenches and guard rings are combined in a polysilicon filled metal lined trench that comprises the Faraday cage wall. Figure 8.14 compares other crosstalk reduction technologies to that of the GPSOI Faraday cage. The results by Raskin et al [1] on thin film SOI are clearly better than the SOI results of this work because

Raskin et al have diodes embedded in oxide and no dc path between them exists. The absence of a dc path forces the noise to follow a coupling path through the handle substrate. At the same time the use of guard rings around the noise source reduces the amount of noise entering the substrate. Increasing the handle resistivity improves isolation because it reduces the conductive coupling.

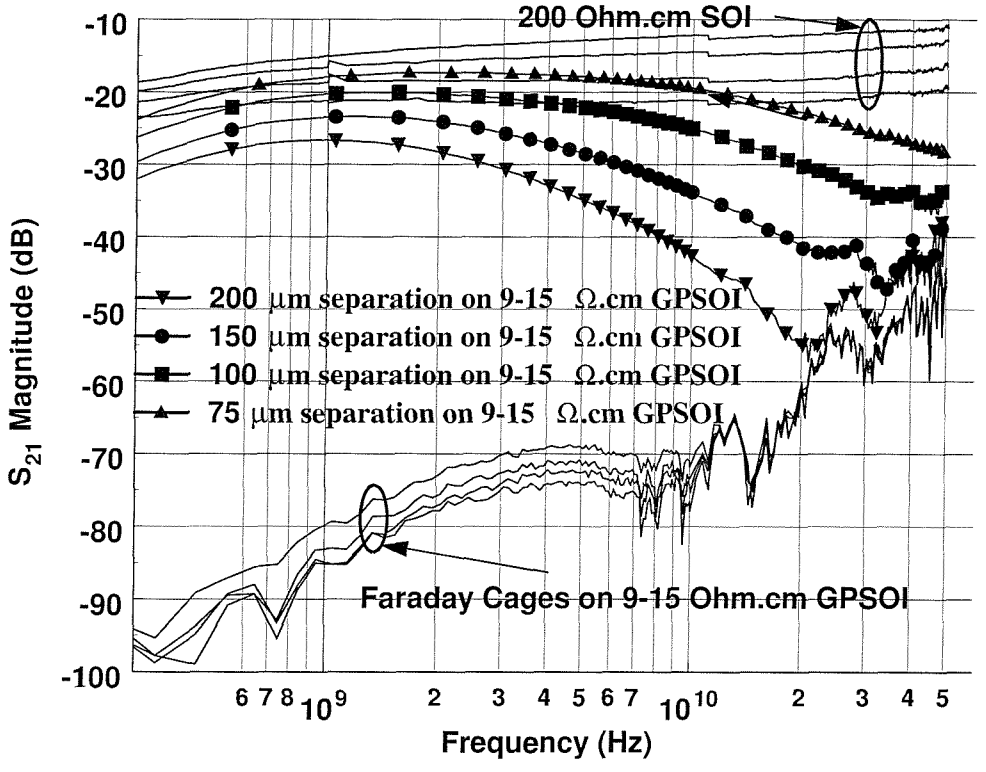


Figure 8.13: Comparison of measurements of Faraday cage test structures with the SOI and GPSOI test structures of chapters 6 and 7 for different Tx/Rx separations.

This improvement, however, is still approximately 20 dB worse than the Faraday cage structures because no further action is taken to eliminate the coupling through the handle substrate. The addition of a ground plane shields the handle substrate from any noise induced from the devices at the surface of the substrate. From a technology point of view, the GPSOI substrate facilitates the integration of a Faraday cage to block any paths above the ground plane, namely through the active layer. The Faraday cage is constructed in a similar way to the top-down contacts of the GPSOI test structures. Since, the GPSOI technology requires a ground contact to the buried WSi_2 plane, a Faraday cage trench comes at no additional cost.

Another Faraday cage structure presented recently in literature by J. H. Wu et. al [4] exhibits similar amounts of isolation, although direct comparison of the two structures is not possible due to the different geometries and substrate involved.

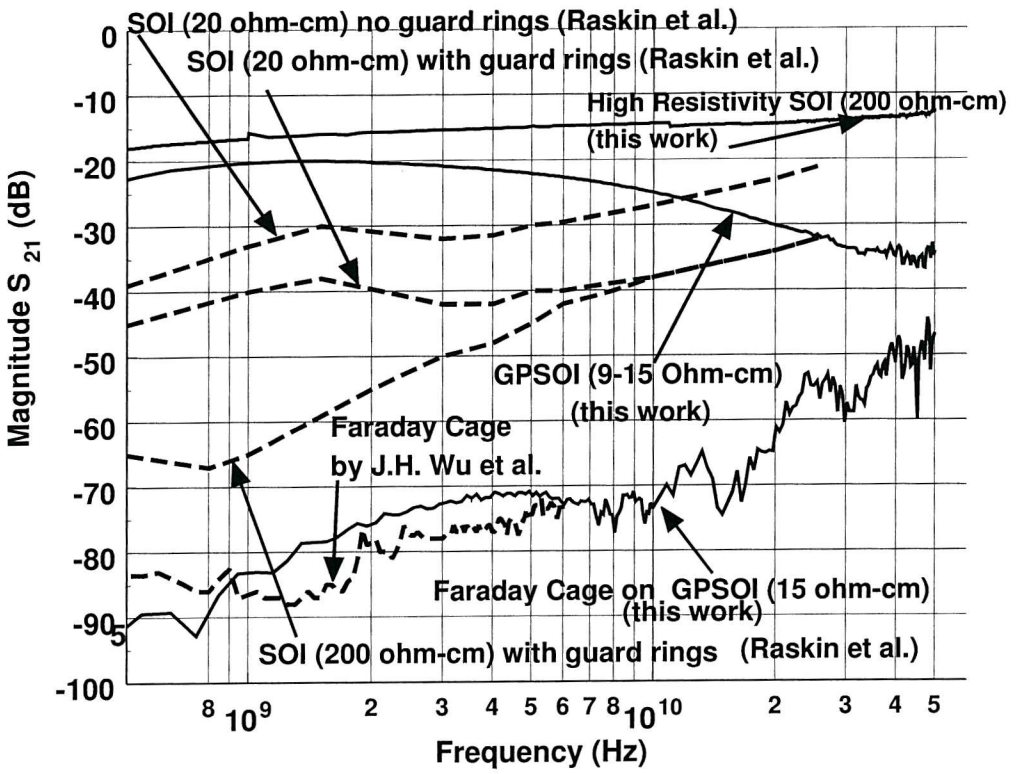


Figure 8.14: Comparison of the Faraday cage with other technologies, including high resistivity thin film SOI [1] and a Faraday cage structure by Wu et. al [4]. The Tx/Rx pad separation is 100 μm.

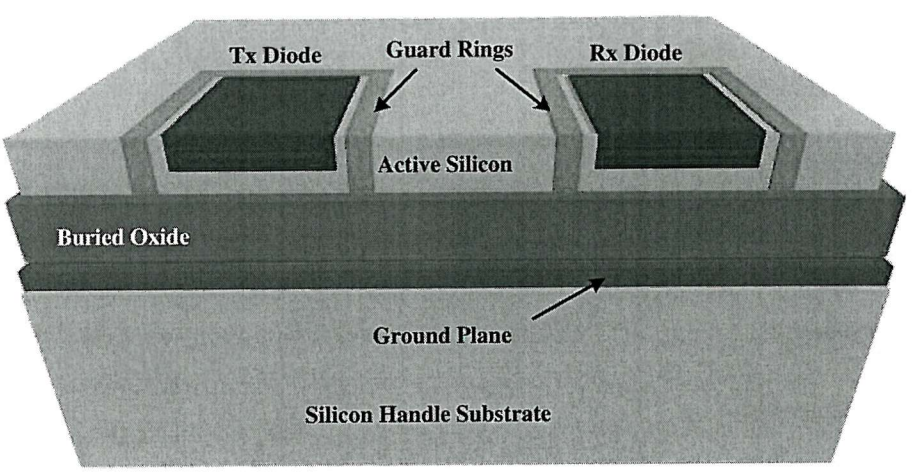


Figure 8.15: Crosse-sectional illustration of a structure with diode Tx/Rx pads surrounded by guard rings, which are deep enough to make contact to the buried oxide of the GPSOI.

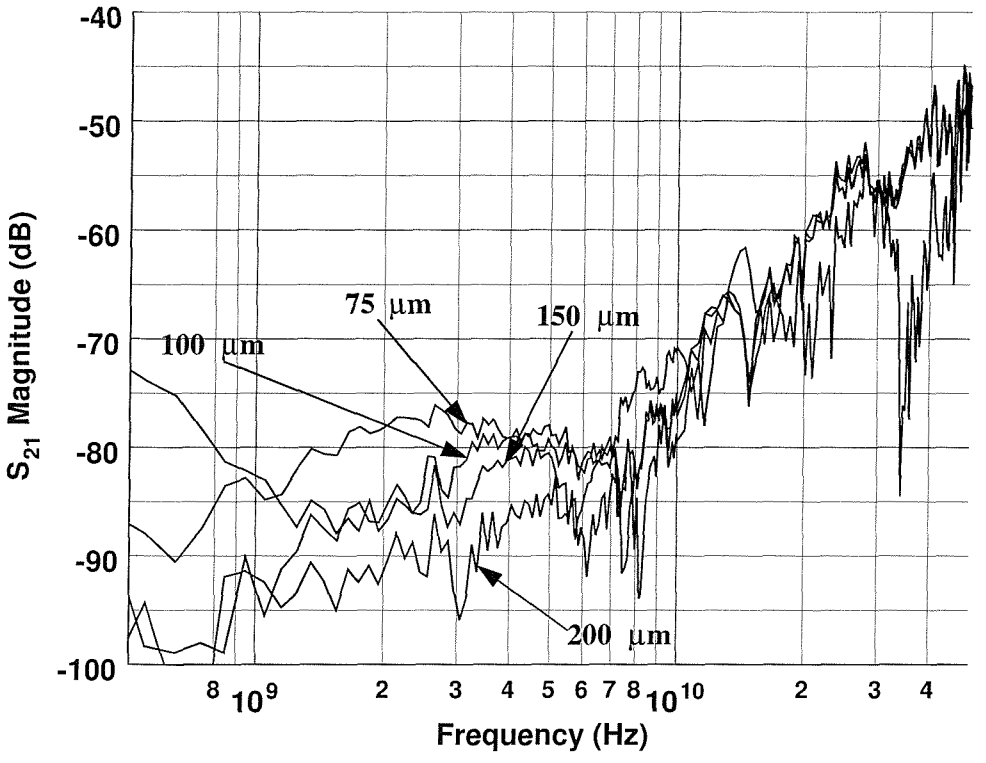


Figure 8.16: Measurements of a GPSOI test structure with Tx/Rx diode pads surrounded by deep n^+ guard rings. The thickness of the active layer is 0.62 μm and the diode junction depth 0.5 μm.

Alternative noise suppression strategies that rely on the Faraday cage principle may be exploited in GPSOI substrates. Guard rings may replace a Faraday cage on a substrate with a thin active layer. Thin active layers allow easy fabrication of guard rings that are deep enough to contact the buried oxide and form a conductive cage around the Tx/Rx pads that blocks any path through the active layer. Figure 8.15 shows such a guard ring structure and the corresponding measurements of isolation are shown in Figure 8.16.

8.6 Conclusions

A crosstalk suppression structure that resembles a Faraday cage has been presented in this chapter. It is integrated easily in a GPSOI substrate and provides a very effective noise suppression strategy. Faraday cage test structures fabricated on GPSOI substrates have exhibited high degrees of signal isolation that are approximately ten times better than high resistivity thin film SOI results presented in the literature. The Faraday cage accomplishes such high performance by relying on the requirement that the buried WSi_2 plane of the GPSOI must be connected to ground. The connection can be made in such way that it forms a Faraday cage around each of the noise Tx and Rx pads. The coupling path through the active

layer is therefore broken and since the handle substrate is already shielded by the ground plane itself, the only coupling path is through the air above the device, resulting in high (<-70 dB at 0.5 – 50 GHz) signal isolation. Such improvement comes at no additional cost compared to GPSOI structures without a Faraday cage and at the cost of providing a top-down contact from the surface of the substrate, when compared to SOI substrates.

Chapter 9

Conclusions and Future Work

9.1 Conclusions

Mixed signal integration has been the subject of extensive research in the past few years mainly due to the growing demand for portable mobile communication products. RF and microwave IC's operating at frequencies in the GHz range are expected to become the focus of research and development even more as wireless telecommunications products flourish in the consumer market. Although, there is an ongoing debate about the current efficiency of system-on-chip (SoC) solutions, the future dictates a movement towards the integration of both analogue and digital systems of mixed signal IC's on a single chip that is compact, consumes little power and provides the signal processing capabilities of powerful, complex digital systems.

Digital circuits are now capable of operating at GHz frequencies and provide tremendous signal processing capabilities. This digital part of mixed signal IC's will have to be integrated alongside a delicately balanced analogue part sharing a common substrate. Despite the on going saga regarding the approaching end of silicon as a semiconductor manufacturing solution for tomorrow's IC's an equally appealing material is yet to be found. The decades of applied knowledge, research and development are not going to be easy to overcome by any other rivals that have appeared in the market but have failed to reach the universal acceptance of silicon. Furthermore, the limits of silicon technology have only been pushed by digital system design and manufacture, in an effort to keep up with Moore's law [38]. Analogue IC's, on the other hand, are not expected to reach them as fast as their digital counterparts. Although digital IC's will continue to challenge silicon's dominance and push it towards smaller geometries, mixed signal IC's are expected to focus more on achieving viable SoC solutions, before increasing chip device densities [39].

For all the aforementioned reasons, it is absolutely essential to research areas in mixed signal silicon technology that would allow efficient SoC integration at high

frequencies. One of the fundamental limitations of mixed signal technology is the parasitic noise coupling through the common silicon substrate. The absence of literature in this area highlights the complexity of substrate coupling and also signifies that it has yet to become an intolerable problem due to the relatively low operating frequencies. With higher operating frequencies in search of additional bandwidth for signal transmission and processing, it will have to be addressed in order for SoC mixed signal solutions to exist.

Substrate coupling can be addressed in principal in two ways. Firstly, the level of noise induced by a circuit or a device will have to be reduced at source. Minimising the coupling of noise from one node to different parts of a circuit that may be sensitive to it, is the other way to reduce the effects of noise coupling. The latter approach is more appealing because it does not involve additional circuit design techniques that cancel the amounts of noise generated by a device or a part of a circuit and induced into the substrate. Existing circuit techniques that do not depend on the manufacturing technology can be readily applied to any substrate with noise coupling suppression properties and benefit instantaneously.

Substrate coupling may be reduced by introducing additional features on the substrate during the manufacturing process, such as diffused guard rings and dielectric trenches. Changing the properties of the substrate material itself is also another option. High resistivity substrates provide additional isolation, since they reduce the conductive part of the coupling, at the potential expense of increased processing and manufacturing costs due to the difficulty in retaining the low doping nature of the substrate throughout the entire process.

Silicon-on-insulator (SOI) substrates have been the next step towards reducing substrate crosstalk. When combined with high resistivity handle substrates, they have been shown to offer increased isolation [1],[7],[8]. Guard rings and dielectric trenches may also be used in conjunction with high resistivity SOI substrates for additional noise suppression. Although, SOI substrates represent a significant improvement over bulk silicon substrates, they tend to suffer at high frequencies. The buried oxide layer of the SOI that at low frequencies is providing increased isolation performance, becomes "transparent" at high frequencies, leaving guard rings as the only means of suppression.

These limitations of SOI technology have given rise to a new breed of solutions that are based on the same principle of guard rings. Guard rings surround potential noise sources and sensors and behave like noise sinks by shunting any noise signals to ground instead of letting them propagate through the substrate towards noise sensitive elements and components. Since they are placed alongside noise sources,

they are successful in reducing the lateral component of noise coupling, as they cannot exist underneath a noise source. The amount of noise that is induced to the substrate underneath a noise source can be shunted to ground by a ground plane. Ground planes have been incorporated into existing bulk silicon substrates by a micromachining technique that etches the backside of the substrate until a specified distance from the surface circuitry is reached [23], [24],[40],[25]. The ground plane is then sputtered under the circuits. A disadvantage of such techniques may be the increased fabrication costs.

This work investigated another solution to substrate crosstalk in the form of SOI substrates with buried ground planes. The ground plane SOI substrate (GPSOI) includes a buried metallic plane underneath the insulator (buried oxide) of the SOI. Once manufactured by a bonding process, the GPSOI can be treated as a SOI substrate. Extensive research is performed nowadays on devices fabricated on GPSOI substrates. This work, however, only focused on the substrate crosstalk suppression capabilities of GPSOI and some manufacturing aspects associated with them.

The crosstalk studies of the GPSOI substrate were divivded into two parts. Initially, the effect of a ground plane on a silicon substrate without a silicon active layer was investigated. The ground plane was separated from the noise Tx/Rx nodes by a layer of oxide. Test structures, similar to those presented in the literature, were fabricated on a substrate with a buried WSi_2 plane. One of the first most important results of these studies was that the buried WSi_2 plane had to be connected to ground in order for the structures to exhibit very small amounts of crosstalk. A floating buried WSi_2 plane exhibited much worse isolation performance, with crosstalk levels higher than a substrate with only a surface oxide and no buried WSi_2 plane at all. Although this requirement may seem rather obvious, it represents a processing challenge for the rest of the studies, where a top down ground contact to the buried WSi_2 plane needs to be achieved in the multilayer GPSOI substrate.

The effect of the buried ground plane resistivity in conjunction with the oxide thickness was investigated by repeating the aforementioned experiments with Al ground planes and variable oxide thicknesses. A trade off between the isolation performance and the minimum oxide thickness was revealed when thin oxides were deposited on lossy WSi_2 ground planes increasing the measured crosstalk. Additional experiments have shown that the modelling of crosstalk relates to coupling of microstrip lines. Closed form expressions of microstrip line coupling were used to model the

capacitive coupling of the test structures. However, the inhomogeneity of the dielectric medium and the existence of a ground plane in close proximity to the Tx/Rx pads do not allow a fully analytical solution. Empirical formulae are therefore the most accurate way to model substrate coupling, sacrificing at the same time some physical insight into the mechanisms behind crosstalk.

An investigation of crosstalk in SOI substrates revealed the amount of crosstalk that exists through the active and handle silicon substrates. The low resistivity nature of the active layer dramatically increases crosstalk and makes it the dominant coupling path in SOI substrates. Furthermore, the handle substrate also contributes significantly to crosstalk as it provides another coupling path. Increasing the handle substrate resistivity slightly improves the isolation as the dominant path is through the surface of the active layer. It is therefore essential to utilise a crosstalk solution that will reduce or even eliminate surface coupling. Dielectric trenches and guard rings are established solutions that have been used so far. The results of SOI crosstalk studies provide a benchmark for the studies on GPSOI substrates and the isolation improvement that can be achieved when a ground plane is present. A partially successful model based on analytical expressions extracted from coupled stripline theory was also presented and discussed. The accuracy of the model was compromised by the assumption of long lines that is used throughout all coupled microstrip and strip line analyses. Empirical terms can however be included in the analytical expression to improve and extend the range of accuracy.

The introduction of a ground plane in the SOI substrate, thus forming a GPSOI substrate, did not improve isolation appreciably, as the main coupling path continued to exist at the surface in the active layer. The requirement that the buried WSi_2 plane must be connected locally to ground presented a processing challenge and at the same time provided a solution to breaking the coupling path through the active layer. From a processing point of view, providing a ground contact from the surface of the GPSOI involved etching through the different materials of different thicknesses of the substrate. A top-down contact to the buried WSi_2 plane was essentially a polysilicon-refilled, WSi_2 lined trench. Since such trenches must exist in order to provide the necessary ground potential to the buried metallic plane, there is no reason why it should not also exist in between the Tx/Rx noise pads, as a means of eliminating coupling through the active layer. In such way, it is entirely possible to form a structure that resembles a Faraday cage. The cage, formed by a trench surrounding the Tx/Rx pads and the buried ground plane, exhibited very high degrees of isolation. A Faraday cage structure relies on the buried ground plane to shield the handle substrate from the induced noise and the cage trench,

which is effectively a vertical extension of the ground plane, to cut off the all important coupling path through the active layer. The amount of crosstalk that was measured in the Faraday cage structures was similar to that of the buried ground plane test structures without the active layer. This was a rather important observation because it revealed that in both experiments the ground plane, which was the common feature in both structures, is responsible for the advanced noise suppression performance.

Substrate	s_{21} (dB) at 1 GHz	Isolation Performance
Oxide-on-Silicon	-35	Poor
Oxide-Floating WSi_2-Silicon	-29	Poor
Oxide-Grounded WSi_2-Silicon	-85	Excellent
SOI (Silicon-Oxide-Silicon)	-15	Poor
GPSOI (Silicon-Oxide-WSi_2-Silicon)	-52	Moderate
Faraday Cage in GPSOI	-85	Excellent
Guard Rings in GPSOI	-90	Excellent

Table 9.1: Summary of isolation performance of the substrates investigated in this work.

To summarize, the GPSOI substrate is capable of producing the lowest (in the author's knowledge) crosstalk figure ever reported on SOI substrates (Table 9.1). The existence of the ground plane underneath the insulator of the GPSOI does not affect significantly crosstalk performance compared to SOI substrates, unless supplemented by a solution that minimises or even eliminates coupling through the active layer at the surface of the substrate. Dielectric trenches and guard rings are known noise suppression strategies that can break surface coupling. The existence of the ground plane, however, facilitates the development of a Faraday cage solution, which comes at no additional manufacturing cost, since it utilises the same processing steps that are required to provide a top-down ground contact to the buried metallic plane in the first place.

9.2 Future Work

The conclusions drawn from the very first crosstalk characterisation studies on GPSOI substrates presented in this work can be used as a cornerstone for future research in the same area. This work cannot be considered complete by any means, as different research and development pathways have emerged.

From a development point of view, the experiments can be extended to cover a wider range of substrate and layout parameters (resistivities and layer thicknesses, Tx/Rx pad dimensions and spacing). Scalable models may be extracted from these

studies and reveal potential limitations and optimised parameter ranges for the best isolation performance.

A subsequent research step is to fabricate active devices on GPSOI and use them as more realistic noise Tx and Rx nodes. A MOS transistor on GPSOI may be used as a noise source to emulate the behaviour of the digital part of mixed signal IC. Ultimately, entire benchmark circuits, known for their performance degradation in other manufacturing technologies, can be fabricated on GPSOI and compared to them. At the same time, equivalent lumped element SPICE models, similar to those presented in this work, could be validated as CAD tools that aid and speed up the design process.

Another important aspect of IC design and fabrication on GPSOI substrates is the integration of passive components. Inductors in particular are known to suffer from sever performance degradation, when they are fabricated on silicon substrates [41],[42],[43],[44],[41], [45],[46]. The quality factor degradation is attributed to image currents generated and supported by the conductive nature of the silicon substrate. Integration of inductors on GPSOI is expected to decrease their performance even more because of the presence of the very conductive buried ground plane underneath them. Consequently, ways to shield the GPSOI substrate from any parasitics induced by inductors, while at the same time retaining the advanced crosstalk suppression capabilities is another future research topic.

The crosstalk performance of the GPSOI substrate can also be characterised in the time domain. Time domain analyses techniques have been used to model interconnect crosstalk. Interconnects occupy a significant amount of area especial in digital circuits and can also be a significant source of noise to the substrate.

The crosstalk suppression capabilities of the GPSOI undoubtedly render it a future candidate for mixed signal silicon RF IC's. Given the demand for higher bandwidth and operating frequencies that could accommodate and exchange faster more information , substrate crosstalk is expected to play a key role in the development of tomorrow's wireless communication consumer products. This work highlighted the promising aspects and identified potential limitations of a new technology. Only through further research and development would it be possible to discover whether it will succeed in becoming a mainstream manufacturing technology of future silicon RF IC's.

Appendix A

List of Publications

J.S. Hamel, S.Stefanou, M.Bain, B.M. Armstrong, and H.S. Gamble, "Substrate Crosstalk Suppression Capability of Silicon-On-Insulator Substrates With Buried Ground Planes (gpsoi)",*IEEE Microwave and Guided Waves Letters*, Vol 10, No 4, April 2000, pp. 134-135.

S. Stefanou, J.S. Hamel, P. Baine, M. Bain, B.M. Armstrong, H.S. Gamble, Rick Mauntel, Margaret Huang "Physics and Compact Modelling of SOI substrates with Buried Ground Planes (GPSOI) for substrate Noise Suppression", International Microwave Symposium Digest, Vol 3, May 2001, pp. 1877-1880.

S.Stefanou, J.S. Hamel, P. Baine, M. Bain, B.M. Armstrong, H.S. Gamble, M. Kraft, H.A. Kemhadjian and K. Osman, "Cross-Talk Suppression Faraday Cage Structure in Silicon-On-Insulator", submitted to IEEE 2002 International SOI Conference.

J.S. Hamel, S.Stefanou, P. Baine, M. Bain, B.M. Armstrong, H.S. Gamble, M. Kraft, H.A. Kemhadjian "Substrate Crosstalk Reduction In Silicon-On-Insulator With Buried Ground Planes, Faraday Cages and Diffused Guard Rings", submitted to IEEE 2002 International Electron Devices Meeting (IEDM).

S. Stefanou, J.S. Hamel, P. Baine, M. Bain, B.M. Armstrong, H.S. Gamble, Rick Mauntel, Margaret Huang, "Ground Plane Silicon-on-Insulator (GPSOI) Substrates: A Substrate Crosstalk Suppression Strategy for Integrated RF/Microwave Mixed Signal ICs", to be submitted to IEEE Journal of Solid State Circuits.

S.Stefanou, J.S. Hamel, P. Baine, M. Bain, B.M. Armstrong, H.S. Gamble, M. Kraft, H.A. Kemhadjian, "Substrate Crosstalk Characterisation of Ground Plane Silicon-on-Insulator Technology", to be submitted to IEEE Journal of Solid State Circuits.

S.Stefanou, J.S. Hamel, M. Kraft, H.A. Kemhadjian, P. Baine, M. Bain, B.M. Armstrong, H.S. Gamble,"Effect of Ground Plane Resistivity on Crosstalk in Substrates With Lossy Buried Ground Planes", to be submitted to IEEE Microwave and Wireless Component Letters.

Appendix B

Listing of the Buried Ground Plane Test Structure Fabrication Process

Running k1791dt on 03-21-2000

	ID	Description	XCost
1	G-S12	Title page 6 wafers	0
2	G-1P	Lithography Notes	0
3	G-1	Wafer Split Wafers 1-4 n-type Si, WSi 0.2um, TEOS 1.0um Wafers 5,6 n-type Si, TEOS 1.2um	0
		Wafers 7,8 are n-type, with 1.2 um TEOS grown (same as wafers 5,6) and can be used as check wafers for TEOS Etch Rate Experiments and Measurements	
4	W-C3	* Fuming Nitric Acid clean, metallised wafers	0
		PROCESS SPLIT FOR WAFERS 1,2 ONLY (with Metal to W Silicide Vias)	
5	P-GS1	* STEPPER Photolith: reticle K914r CW dark field: nom. 1.1um resist #1,2	0
6	G-2	* See Engineer for instructions	0
7	P-RHBW	* Hardbake for wet etch #1,2	0
		ETCH VIAS FOR WAFERS 1,2 (TEOS Etch Rate is approx. 170nm/min in 7:1 Buffered HF)	
8	WH-7E3	+ Wet etch oxide, 7:1 BHF 25degC. To hydrophobic Si + 20secs. #1,2 Specify Time According to TEOS Etch Rates Metal Area	0
9	P-RS	* Resist strip wafer 2 Metal Area	0
10	D-0	Dry etch: Specify process #1,2	0
11	W-R3	* Resist strip FN acid, post metal, use special equipment	0
12	X-I1	Inspect wafers for residue after wet or dry etch. #1,2	0
13	WH-20D	Dip etch, 200:1 BHF (Pre-metallization for silicided CW) Metal Area #1,2	0
		SPUTTER METAL WAFERS 1-6	
14	W-C3	* Fuming Nitric Acid clean, metallised wafers ALL WAFERS	0
15	MS-TA1(	Sputter 1000nm Ti-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED	0
16	P-GS2	* STEPPER Photolith: reticle K914R, M1 Light Field: 2.2um resist	0
17	G-2	* See Engineer for Instructions	0
18	P-RHBW	* Hardbake for wet etch	0
19	WM-AS1	Wet etch Al/Si+Ti, 3 Stage etch: Phos acid, Ti etch, Defreckle.	0
20	P-RS	* Resist strip	0
		BACKPLANE METALISATION (Wafers 1-6)	
21	P-RF	* Frontspin resist	0
22	WH-7E3	Wet etch oxide, 7:1 BHF. Metallized wafers. To hydrophobic + 20secs	0
23	W-R3	* Resist strip FN acid, post metal, use special equipment	0
24	MS-TA1(	Sputter 1000nm Ti-Al/Si 1% in TRIKON SIGMA for BACKS	0
25	F9-H42	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.	0

Figure B.1: Process listing of the fabrication of the buried ground plane test structures

Appendix C

Listing of the "Pseudo" Buried Ground Plane Test Structure Fabrication Process

Running k2167s on 05-29-2002

	ID	Description
1	P-EM	E-BEAM Mask/Reticle Writing 2 Reticles
2	G-S12	Title Page: 15 wafers, MATERIAL:n-type Si 9-15 Ohm-cm
3	G-1P	Lithography Notes
4	G-1	Notebook page
5	WH-2I	Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation)
		Sputter Ground Planes
		Al Ground Plane
6	MS-0	Sputter 200nm Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED Wafers 1,3,5,7,9
		TiSi2 Ground Plane Silicidation - Wafers 2,4,6,8,10 C1,C2,C3 Check Wafers
7	W-0	Dip Wafers in 2% HF solution until Hydrophobic Wafers 2,4,6,8,10+C1,C2,C3 Check Wafers
8	MS-0	Sputter 60 nm Ti + 25 nm TiN Wafers 2,4,6,8,10+C1,C2,C3 Check Wafers
9	G-2	* See Engineer for instructions - Decide on RTA schedule for thick Ti
10	RL-0	LEISK RTA : 60s(?) 730 deg C Wafers 2,4,6,8,10+C1,C2,C3 Check Wafer
11	W-0	SPM in Metals Area of Wet Bench Wafers 2,4,6,8,10+C1,C2,C3 Check Wafers
12	W-0	SPM in Metals Area of Wet Bench Wafers 2,4,6,8,10+C1,C2,C3 Check Wafers
13	RL-0	LEISK RTA stage : 30s 850 deg C Wafers 2,4,6,8,10+C1,C2,C3 Check Wafers
14	W-0	SPM in Metals Area of Wet Bench Wafers 2,4,6,8,10+C1,C2,C3 Check Wafers
15	G-2	* See Engineer for instructions - MEASURE Ground Plane SHEET RESISTANCE WITH 4-POINT PROBE
16	W-C3	* Fuming Nitric Acid clean, metallised wafers ALL WAFERS
		SPLIT FOR VARIABLE OXIDE THICKNESS
17	LD-O(	PECVD OXIDE deposition; 250nm thickness (UP TO 3000nm) WAFERS #1,2
18	LD-O(	PECVD OXIDE deposition; 500nm thickness (UP TO 3000nm) WAFERS #3,4 +Check Wafers C1,C2,C3
19	LD-O(	PECVD OXIDE deposition; 1000nm thickness (UP TO 3000nm) WAFERS #5,6
20	LD-O(	PECVD OXIDE deposition; 1500nm thickness (UP TO 3000nm) WAFERS #7,8
21	LD-O(	PECVD OXIDE deposition; 2000nm thickness (UP TO 3000nm) WAFERS #9.10
22	LD-O(	PECVD OXIDE deposition; 1200nm thickness (UP TO 3000nm) WAFERS #11,12
		TiSi Etch Rate Check in Oxide Dry Etch Process Wafers C1,C2,C3 ONLY USE BACK END COVER PLATE
23	P-0	+ Blank sheet for non standard process STEPPER LITHOGRAPHY See TONY for clear drop-in sites on wafers for 4-point probe measurements
24	P-RHE	* Hardbake for dry etch
25	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar (500nm Oxide) Check Wafers as necessary USE BACK END COVER PLATE
26	G-2	* See Engineer for instructions Measure TiSi Sheet Res with 4-point probe in drop-in areas
27	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar (500nm Oxide) Check Wafers as necessary USE BACK END COVER PLATE
28	G-2	* See Engineer for instructions Measure TiSi Sheet Res with 4-point probe in drop-in areas
29	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar (500nm Oxide) Check Wafers as necessary USE BACK END COVER PLATE
30	G-2	* See Engineer for instructions Measure TiSi Sheet Res with 4-point probe in drop-in areas

Figure C.1: Process listing of the fabrication of the "pseudo"-buried ground plane test structures

Running k2167s on 05-29-2002

	1 2 3 4 5 6	ID	Description	ou
31		G-2	* See Engineer for instructions Deduce TiSi etch rate from Sheet Res Measurements	
			SPLIT FOR CONTROLS - DONT ETCH CWs ON WAFERS #11,12	
32		W-C3	* Fuming Nitric Acid clean, metallised wafers Wafers #1,2,3,4,5,6,7,8,9,10	1
33		P-GS2	* STEPPER Photolith: reticle KA29R, CW, Dark Field: nom. 2.2um resist (For Si etch>1um or metal) Wafers #1,2,3,4,5,6,7,8,9,10	1
34		G-2	* See Engineer for instructions	
35		P-RHE	* Hardbake for dry etch Wafers #1,2,3,4,5,6,7,8,9,10	1
			ETCH CONTACT WINDOWS ON EACH SPLIT USE BACK END COVER PLATE	
36		D-01F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFERS #1,2 (250nm Oxide) USE BACK END COVER PLATE	
37		D-01F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFERS #3,4 (500nm Oxide) USE BACK END COVER PLATE	
38		D-01F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFERS #5,6 (1000nm Oxide) USE BACK END COVER PLATE	
39		D-01F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFERS #7,8 (1500nm Oxide) USE BACK END COVER PLATE	
40		D-01F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFERS #9,10 (2000nm Oxide) USE BACK END COVER PLATE	
41		P-RS	* Resist strip	1
42		X-I1	Inspect 10 wafers for residue after wet or dry etch.	1
			METALLISATION (ALL WAFERS)	
43		G-2	* See Engineer for instructions SEE TONY FOR HSE PROCESS WAFERS 1,3,5,7,9 (AL GROUND PLANE)	
44		W-C3	* Fuming Nitric Acid clean, metallised wafers WAFERS 1,3,5,7,9 (AL GROUND PLANE)	
45		MS-0	Blank sheet for TRIKON SIGMA sputtered films. HSE+1000nm Al/Si RESIST PROHIBITED WAFERS 1,3,5,7,9 (AL GROUND PLANE)	
46		W-C4	* Sulphuric/peroxide clean WAFERS 2,4,6,8,10 (TiSi GROUND PLANE)	
47		WH-2(	Dip etch, 200:1 BHF (Pre-metallization for silicided CW) WAFERS 2,4,6,8,10 (TiSi GROUND PLANE)	
48		MS-T/	Sputter 1000nm Ti-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED WAFERS 2,4,6,8,10	
49		P-GS2	* STEPPER Photolith: reticle KA29R, M1, LIGHT Field: nom. 2.2um resist (For Si etch>1um or metal) ALL Wafers	1
50		G-2	* See Engineer for instructions	
51		P-RHE	* Hardbake for wet etch	1
52		WM-A	Wet etch Al/Si+Ti, 3 Stage etch: Phos acid, Ti etch, Defreckle.	1
53		P-RS	* Resist strip	1
			BACKSIDE METALLISATION (ALL WAFERS)	
54		WH-7(	Remove oxide from backside using cotton bud in 7:1 BHF	1
55		MS-T/	Sputter 1000nm Ti-Al/Si 1% in TRIKON SIGMA for Capacitor BACKS RESIST PROHIBITED	1
56		W-C3	* Fuming Nitric Acid clean, metallised wafers	
57		F9-H4	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.	1

Figure C.2: Process listing of the fabrication of the "pseudo"-buried ground plane test structures (continued)

Appendix D

Listing of the SOI Test Structure Fabrication Process

Fabrication Process	**Comments**	
SOI Thickness (μm)		
STD Clean		
P Diffussion for back contact	1000 ^{o}C, 20 minutes	
STD Clean		
Oxidation (0.5 μm)	1050 ^{o}C	
Photo: ND-Mask (N-type Diffusions)	EV Proximity Alignment System	
Oxide Dry Etching	150W, 2 minutes, Recipe CPOXIDE	
STD Clean		
Phosphorus Implantation, Energy=30 KeV Dose=3×10^{15}	Aiming for 0.5 μm junctions Depth Anneal time 6.65 Minutes at 1000 C.	
STD Clean		
Oxidation (0.5 μm) LPCVD TEOS	Temperature 720 C	
Photo: PD-Mask P+ Diffusions	EV Proximity Alignment System	
Oxide Dry Etching		
STD Clean		
Boron Implantation Energy=20 KeV Dose=3×10^{15}		
STD Clean		
Oxidation (0.5 μm) LPCVD TEOS	Temperature 720 C	
TEOS Densification and Implant Activation	1000 C, 67 minutes	
Photo: CW-Mask	EV Proximity Alignment System	
Dry Etch Contact Windows		
STD Clean		
30:1 H_20: HF Dip 30 secs		
Al Sputtering (1μm)		
Photo: MM-Mask	EV Proximity Alignment System	
Etch Al (Wet Chemical Etch)		
Resist on Front		
Remove Back Oxide		
Al Sputtering onto Back of Substrate		
N_2/H_2 Anneal	440 C, 15 minutes	

Appendix E

Listing of the GPSOI and Faraday Cage Test Structure Fabrication Process

Fabrication Process	**Comments**	
STD Clean		
P Diffusion for back contact	1000 °C, 20 minutes	
STD Clean		
Oxidation (0.5 μm)	1050 °C	
Photo: TR-Mask (Trenches)	EV Proximity Alignment System	
Oxide Etch	STS Dry Etch or Wet Etch	
Trench Etch to Ground Plane	STS Dry Etch to Remove Si and Buried Oxide	
Strip Resist	May use top oxide as barrier for Si etching. Resist unable to withstand all three dry etch processes	
STD Clean		
Sidewall Oxidation	Dry Oxidation, 1050 C	
Oxide Dry Etch to Remove Oxide from Trench Bottom	STS Dry Etch	
Tungsten Silicide deposition		
Polysilicon Deposition	LPCVD 620 C	
Polysilicon Doping (N+)	Diffusion/Implantation	
Dopant Drive-in	1000 C	
Photo: PL-Mask (Polysilicon Pattern)	EV Proximity Alignment System	
Etch Polysilicon	Dry Etch	
Etch Tungsten Silicide	Dry Etch	
Strip Resist		
STD Clean		
Photo: ND-Mask (N-type Diffusions)	EV Proximity Alignment System	
Oxide Dry Etching	150W, 2 minutes, Recipe CPOXIDE	
STD Clean		
Phosphorus Implantation, Energy=30 KeV Dose=3×10^{15}	Aiming for 0.5 μm junctions Depth Anneal time 6.65 Minutes at 1000 C.	
STD Clean		
Oxidation (0.5 μm) LPCVD TEOS	Temperature 720 C	
Photo: PD-Mask P+ Diffusions	EV Proximity Alignment System	
Oxide Dry Etching		
STD Clean		

Fabrication Process	**Comments**	
Boron Implantation Energy=20 KeV Dose=3×10^{15}	Aiming for 0.5 μm junctions Depth Anneal time 67 Minutes at 1000 C.	
STD Clean		
Oxidation (0.5 μm) LPCVD TEOS	Temperature 720 C	
TEOS Densification and Implant Activation	1000 C, 67 minutes	
Photo: CW-Mask	EV Proximity Alignment System	
Dry Etch Contact Windows		
STD Clean		
30:1 H_20: HF Dip 30 secs		
Al Sputtering (1μm)		
Photo: MM-Mask	EV Proximity Alignment System	
Etch Al (Wet Chemical Etch)		
Resist on Front		
Remove Back Oxide		
Al Sputtering onto Back of Substrate		
N_2/H_2 Anneal	440 C, 15 minutes	

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