

*SYNTHESIS AND
STRUCTURES of
TRANSCONDUCTAN
CE AMPLIFIER
AND CURRENT
CONVEYOR-BASED
FILTERS*

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*Synthesis and Structures of
Transconductance Amplifier and
Current Conveyor-Based Filters*

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ABSTRACT

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Synthesis and Structures of Transconductance Amplifier
and Current Conveyor Based Filters

by Chun-Ming Chang

This thesis investigates the development of new synthesis methods and structures of analogue filters considering two types of active elements: operational transconductance amplifiers and current conveyors. Starting from an n th-order generic transfer function, it is shown how an analytical synthesis approach can be used to generate systematically filters that have less component count than previously known filters whilst maintaining the desirable features of grounded passive components and the employment of single-input active devices. Two new synthesis methods for current-mode filters and two new synthesis methods for voltage-mode filters have been developed including their associate structures to provide n th-order filtering functions. Equal transconductance and equal capacitance appear in the voltage-mode synthesized filter structures particularly suitable for VLSI implementation. Simulation results of various filter circuits obtained from the proposed synthesis methods are given based on CMOS design of the active elements.

Despite the numerous publications reporting filter biquads based on transconductance amplifiers and current conveyors, it is shown how such biquads normally make trade-offs with respect to some key performance parameters including excessive number of passive and active elements and the need to impose component choice conditions in order to provide universal filtering. This includes low-pass, high-pass, band-pass, notch and all-pass functions. This thesis proposes the concept and design of *unified* filter model based on nullators, norators, current mirrors, resistors and capacitors, from which two new biquad implementations based on two different active elements have been developed. It is shown that such biquads can achieve five key performance parameters simultaneously and without trade-offs.

Finally, a comparative analysis between the various synthesis methods and filter structures reported throughout the thesis has been carried out with the general aim of assisting the designer to develop the appropriate filter circuit given a filtering problem and an implementation style.

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Abbreviations

CCII	Second-Generation Current Conveyor
CCII+	Plus-Type Second-Generation Current Conveyor
CCII-	Minus-Type Second-Generation Current Conveyor
CCII±	Plus-/Minus-Type Second-Generation Current Conveyor
CCCII	Second-Generation Current-Controlled Conveyor
CCCII-C	Second-Generation Current-Controlled Conveyor and Capacitor
CFA	Current Feedback Amplifier
CFCCII _p	Four Terminal P-Type Active Current Conveyor
DIMOC	Double Input and Multiple Output Currents
DVCCS	Differential Voltage-Controlled Current Source
IC	Integrated Circuit
MISOC	Multiple Input Currents and a Single Output
OA	Operational Amplifier
OTA	Operational Transconductance Amplifier
OTA-C	Operational Transconductance Amplifier and Capacitor

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Chapter 1

Introduction

The most elegant solution to a filter synthesis problem is to decompose analytically the required filter transfer function into a set of equations that can be realized using simple analogue processing blocks such as integrators. The analytical synthesis approach has many benefits; for example the ability to generate filter circuits in a systematic and structured way, and the ability to obtain filter circuits with different transfer functions (i.e. responses) simply by suitable choice of equations. Furthermore, analytical synthesis offers the designer explicit relations that provide insight into the filter's behaviour. This analytical synthesis method was demonstrated in the following three approaches.

I. Differential-analyzer technique [1-2]: In many electrical problems involving transducers or energy conversion, an input variable (stimulus) $x(t)$ produces an output (response) $y(t)$ related to $x(t)$ by a linear differential equation

$$\frac{d^n y}{dt^n} + a_{n-1} \frac{d^{n-1} y}{dt^{n-1}} + \dots + a_0 y = b_m \frac{d^m x}{dt^m} + b_{m-1} \frac{d^{m-1} x}{dt^{m-1}} + \dots + b_0 x \quad (1-1)$$

where the a_i , b_k are given constant coefficients, and $n \geq m$. The dynamic input-output relationship expressed by Eq. (1-1) is brought out more clearly if we write it in terms of a time-invariant linear transfer operator $H(p)$, i.e.,

$$y(t) = H(p)x(t) = \frac{b_m p^m + b_{m-1} p^{m-1} + \dots + b_0}{p^n + a_{n-1} p^{n-1} + \dots + a_0} x(t) \quad \left(p \equiv \frac{d}{dt} \right) \quad (1-2)$$

Eq. (1-2) is rewritten as

$$y = b_n x + \frac{1}{p}(b_{n-1}x - a_{n-1}y) + \frac{1}{p^2}(b_{n-2}x - a_{n-2}y) + \dots + \frac{1}{p^n}(b_0x - a_0y) \quad (1-3)$$

where $b_i = 0$ for $i > m$. Introduce the n new variables

$$\begin{aligned} v_1 &= y - b_n x \\ v_2 &= a_{n-1}y - b_{n-1}x + \frac{dv_1}{dt} \\ v_3 &= a_{n-2}y - b_{n-2}x + \frac{dv_2}{dt} \\ &\dots \\ v_n &= a_1y - b_1x + \frac{dv_{n-1}}{dt} \\ 0 &= a_0y - b_0x + \frac{dv_n}{dt} \end{aligned} \quad (1-4)$$

The given differential equation (1-4) is equivalent to the system of n first-order equations

$$\begin{aligned} \frac{dv_n}{dt} &= b_0x - a_0y \\ \frac{dv_{n-1}}{dt} &= v_n + b_1x - a_1y \\ \frac{dv_{n-2}}{dt} &= v_{n-1} + b_2x - a_2y \\ &\dots \\ \frac{dv_1}{dt} &= v_2 + b_{n-1}x - a_{n-1}y \\ y &= v_1 + b_n x \end{aligned} \quad (1-5)$$

These relations are implemented by a number of operational amplifiers (OAs) and resistors to realize integrators, summer/phase inverters, and coefficient-setting potentiometers, shown in Fig. 1-1.

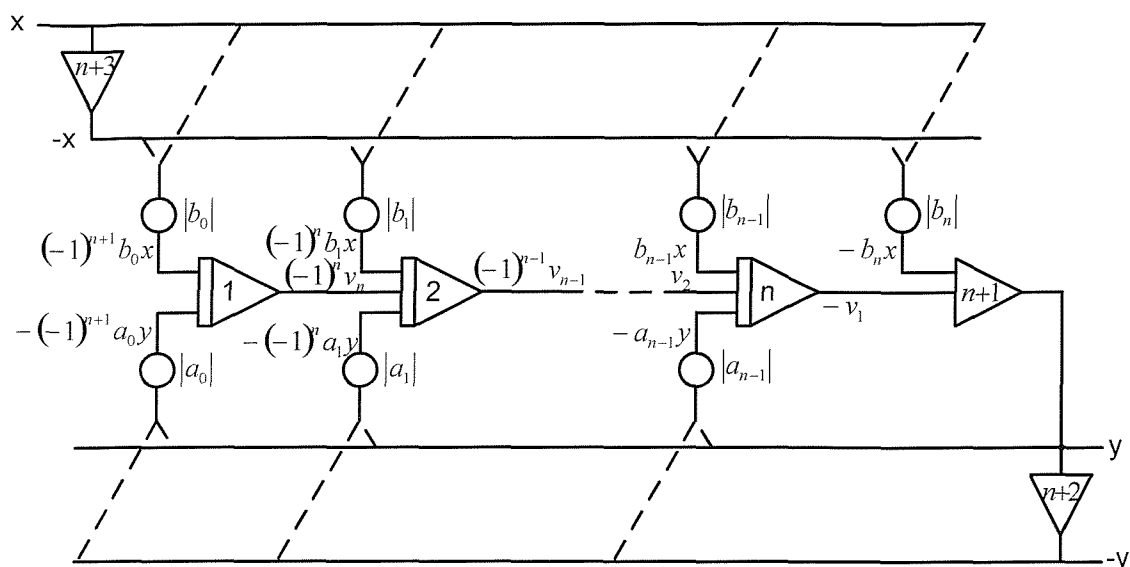


Fig. 1-1 Implementation of the differential-analyzer technique [1-2]

Although the iterative approach of the differential-analyzer technique is quite attractive, the implementation shown in Fig. 1-1 suffers from the use of too many active elements and resistors.

II. Tow-Thomas algebraic decomposition technique [3-5]: The disadvantage, use of too many components, of the above approach was improved by the analytical synthesis method for the Tow-Thomas biquad [3-5], where the second-order low-pass transfer function is manipulated algebraically until a set of equations are produced which are then realized using two integrators and an inverting amplifier. It is also sometimes called the “ring of 3 circuit”. The analytical synthesis method is shown as follows. Let the voltage-mode low-pass transfer function be

$$\frac{V_{out}}{V_{in}} = \frac{-b_0}{s^2 + a_1 s + a_0} \quad (1-6)$$

We wish to manipulate the equation until it has a form that can be identified with simple circuits. Rewrite Eq. (1-6) as

$$(s^2 + a_1s + a_0)V_{out} = -b_0V_{in} \quad (1-7)$$

Divide this equation by the factor $(s^2 + a_1s)$, it becomes

$$\left[1 + \frac{a_0}{s(s + a_1)}\right]V_{out} = \frac{-b_0}{s(s + a_1)}V_{in} \quad (1-8)$$

This equation can be manipulated to produce

$$V_{out} = \left[\frac{-a_0}{(s + a_1)}V_{out} + \frac{-b_0}{(s + a_1)}V_{in} \right] \left(\frac{-1}{s} \right) (-1) \quad (1-9)$$

Starting at the right-hand side of this equation, we recognize that the (-1) term may be realized by an inverting circuit of gain 1. Similarly, the factor $(-1/s)$ is realized by an inverting integrator. Two operations are indicated by the remaining factor. The circuit realization must produce a sum of voltages, and it must have a transfer function of the form $1/(s + a_1)$. The three circuits that provide these three operations are shown in Fig. 1-2. The circuit marked T_1 , where the OA is the active element, sums voltages V_{out} and V_{in} with appropriate multiplication, and also realizes the first-order transfer function with a circuit called a lossy integrator. The circuit marked T_2 is the standard inverting integrator circuit, and the circuit marked T_3 is an inverting circuit of unity gain. If we connect the three circuits together, including a feedback connection of the output V_{out} to the input, the result is the circuit shown in Fig. 1-3 (in which the component values are normalized and can be de-normalized to meet the designer's requirement). This is called the biquad circuit, the ring of 3 circuit, or the Tow-Thomas biquad.

Therefore, the Tow-Thomas biquad uses 3 OAs, 6 resistors, and 2 capacitors much simpler than 7 OAs, 15 resistors, and 2 capacitors employed by differential-analyzer technique for realizing a second-order low-pass transfer function.

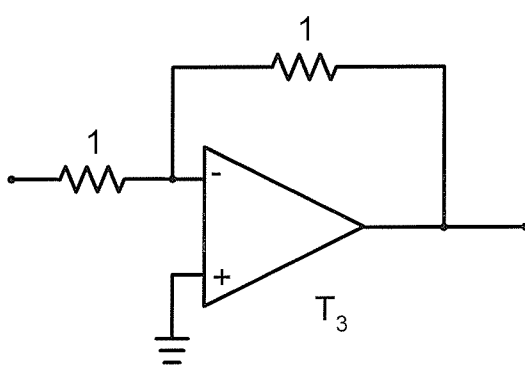
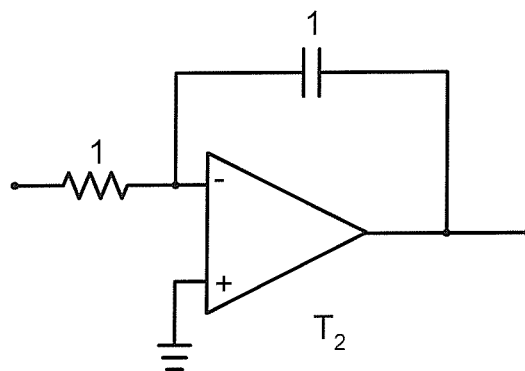
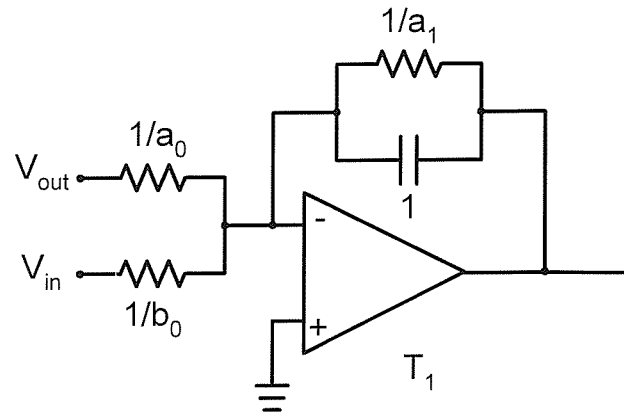


Fig. 1-2 Three circuits provided for the three parts in Eq. (1-9)

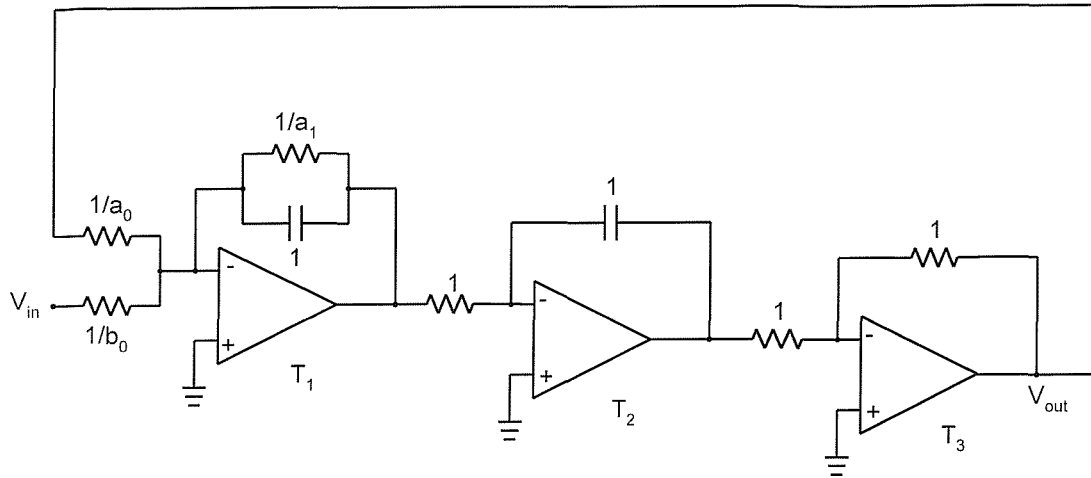


Fig. 1-3 Tow-Thomas biquad [3-5]

III. Ping-Sewell matrix decomposition technique [6]: A methodology has been developed for the design of switched-capacitor (SC) ladder simulation filters by using OAs. The design procedures for integrated ladder filter design by operational simulation are regularized in terms of matrix decomposition. This provides a systematic framework for the derivation of standard circuits. A wide range of circuits can be derived by adopting different matrix factorizations, notably LU and UL decomposition, including both existing and novel structure. Each circuit is now seen to belong to a certain family, dependent on the type of matrix factorization employed. A detailed comparison of various SC circuit structures has been undertaken and some notable conclusions are: the left-LUD method is the best choice for filters with very narrow and very wide passbands; the leapfrog method is the best choice for sharp transition low-pass filter design; and cascade biquads are the best choice for moderately selective low-pass and band-pass filter design. A 20th-order band-pass ladder (Fig. 1-4) is simulated by the left-LUD circuit (Fig. 1-5). As can be seen, the structure is very regular and the long unswitched capacitor op-amp chains have been broken by introducing two negative elements into the prototype. Some special design techniques can be applied to produce efficient circuits in other techniques such as continuous-time active-RC filters.

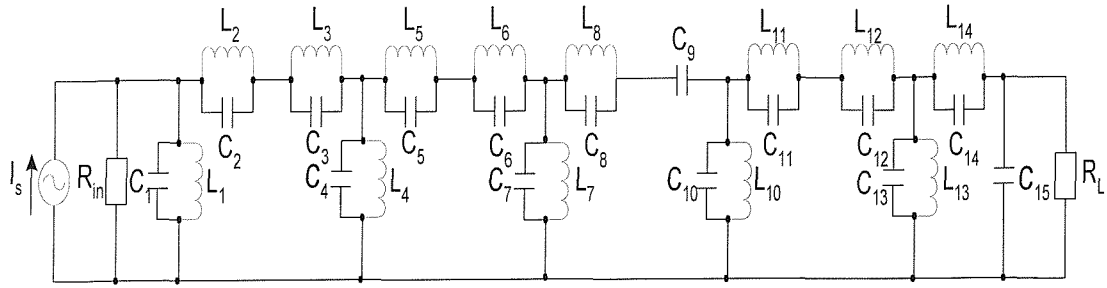


Fig. 1-4 20th-order band-pass ladder prototype

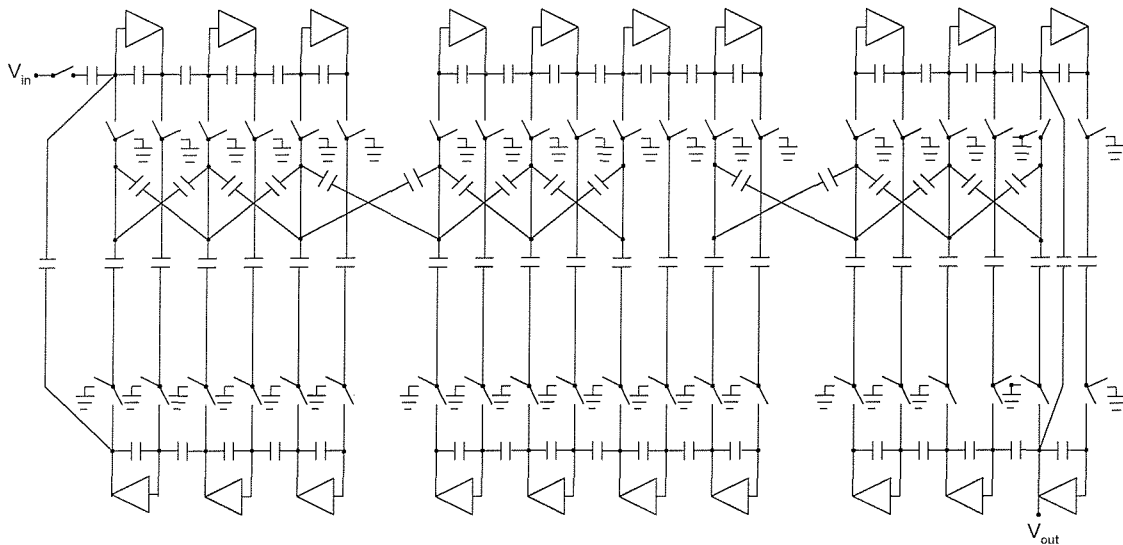


Fig. 1-5 Left-LUD SC ladder simulation with broken loops

The three synthesis methods described are very useful in developing filter structures in a formal manner. Particularly, since methods I and III can be used to design n th-order filters with different filtering functions but method II (algebraic decomposition technique) only for the second-order filtering synthesis, this thesis presents a new formal method for synthesizing n th-order filters starting from algebraically decomposing a single complicated equation representing an n th-order filter transfer function with different responses; under the constraint that the generated set of

equations must be realizable using simple circuitry. The motivation behind this work is to develop an efficient analytical synthesis approach for high-order current-/voltage-mode filters.

Which active element is appropriately used in the new analytical synthesis method? Two active elements that have received considerable attention from the research community over the last two decades in analogue filter design are: operational transconductance amplifiers (OTAs), and second-generation current conveyors (CCIIs). The most attractive tunable transconductance element is the operational transconductance amplifier (OTA). The transconductance g of an OTA is adjustable within the range of several decades by a supplied bias current I_{abc} (amplifier bias current). Therefore, the OTA provides linear electronic tunability and a wide tunable range of its transconductance gain. Moreover, it is easy to control its parasitic distortion due to only ordinary parasitic capacitances and conductances existed at its input and output ports unlike the second-generation current conveyor (CCII) with additional parasitic inductance, and non-ideal frequency-dependent current and voltage transfer constraints (referring to Appendix 4). Few recently reported CCII-based high-order filter structures [67-72] were proposed and had shown that too many resistors were unavoidable unlike complimentary OTA-based high-order filter structures [7-20] without the need of resistors. The following three main advantages of the OTA,

- tunable transconductances,
- easier control of its non-ideal factors,
- suitable for integration due to the absence of resistors,

lead us to choose the OTA as the active element to synthesize high-order voltage/current-mode filter transfer functions in this thesis.

Over the last decade or so numerous voltage-mode and current-mode high-order OTA-C filter structures have been reported [7-20]. Such structures have often been developed with different design criteria in mind, including reduced number of active elements, single-input OTAs, grounded capacitors, and simple design methods. It has shown in

[13], that there are *three main important criteria* that need to be considered when generating OTA-C filter structures. The *three main important criteria* are:

- filters use grounded capacitors because they have smaller chip area than the floating counterpart, and because they can absorb equivalent shunt capacitive parasitics;
- filters employ only single-input OTAs to overcome the feed-through effects due to finite input parasitic capacitances associated with double-input OTAs;
- filters have the least number of components (passive and active) for a given order to reduce power consumption, chip areas, and noise.

Despite the extensive literature on active filters [7-20], none of the high-order OTA-C filters are capable of achieving the above *three main important criteria* simultaneously and without trade-offs. Therefore, there is still a need to develop new high-order filter structures that offer more advantages than existing structures which is the main motivation of the research discussed in this thesis.

On the other hand, the OTAs and CCIIs mentioned earlier are powerful analogue building blocks, combining voltage and current-mode capability. A number of novel filter functions and topologies [7-72] have been explored on the broader front of current-mode and voltage-mode analogue filters, opening up wider areas of interest. Despite the extensive literature on active filters, none of the biquads are capable of achieving the following *five performance parameters* simultaneously and without trade-offs,

- universal filtering (low-pass, high-pass, band-pass, notch, and all-pass),
- minimum components count (three active elements, two grounded capacitors, and no resistors),
- independent ω_o and ω_o/Q tunability,
- no need to impose component choice conditions to realize specific filtering functions (which leads to no influence resulted from fabrication tolerances and drifts during operating), and

- no need to employ additional active elements to provide filter current outputs explicitly.

Therefore, there is still a need to develop new biquadratic structures that offer more advantages than existing structures which is another motivation of the research described in this thesis.

Motivation Summary of This Thesis

Following the above statements, the motivation, for this thesis, has two main strands:

(i) Develop an efficient analytical synthesis approach to decompose a single complicated equation representing an n th-order filter transfer function with different responses into a set of simple equations for realising high-order current-/voltage-mode OTA-C filters which are optimal in terms of the *three main important criteria* stated above and without trade-offs.

(ii) Despite the extensive literature on voltage-mode and current-mode filter design as outlined earlier [21-66], there is still a need to investigate and develop new active filter biquads that have less component counts, only three active elements and two grounded capacitors but without any resistors, and exhibit desirable VLSI features including grounded passive elements, or enjoy the *five performance parameters* stated above without trade-offs.

Contributions and Thesis Structure

This research has shown that the new analytical synthesis method decomposes a complicated n th-order filter transfer function with different responses into a set of simple equations which can be implemented using simple circuitry. Two current-mode and three voltage-mode n th-order filter structures with the least passive and active component count are presented. Furthermore, the produced filter circuits have two attractive features: grounded capacitors and single-input OTAs, and two more beneficial VLSI realisations: equal transconductance and equal capacitance for two

new voltage-mode filter structures. This research has also demonstrated how a filter model based on nullators and norators (whose definitions are shown in Section 5.2 based on Fig. 5-14) can facilitate the development of two *unified* biquads that are capable of achieving simultaneously a number of key important performance parameters and without trade-offs. Therefore, it is hoped that the methods and structures proposed in this thesis will contribute to the area of analogue signal processing and IC design.

The remainder of this thesis is organized as follows.

Chapter 2 provides a survey of the most relevant and related works and outlines the necessary background information that is helpful for the understanding of the discussed subject. Based upon four design principles (in order to meet the three important criteria: using single-input OTAs, grounded capacitors, and the least number of components).

Chapter 3 presents two new current-mode analytical synthesis methods for high-order current mode OTA-C (Operational Transconductance Amplifier and Capacitor) filters by using a succession of innovative algebra manipulation to solve an n th-order current transfer function and generate n simple and realizable equations. Their two associated canonical filtering structures are then proposed. Different filter orders and functions can be obtained from the general filter structures by suitable selection either of current injection(s) at the filter inputs or of current extraction(s) at the filter outputs.

Chapter 4 presents two new voltage-mode analytical synthesis methods and three new high-order voltage-mode filter structures that employ only single-input OTAs, grounded capacitors, and the least number of components when compared with recently reported structures [7-20]. It has been shown how decomposing analytically an n th-order voltage transfer function into $n+1$ simple realisable transfer functions using OTA-C circuits produces the first filter structure that employs fewer active elements than the recently reported methods and offers simultaneous multiple outputs. Realizing the general transfer function by using the more effective synthesis approach different from the linear combination of each output signal of the first filter structure leads to the second filter structure which can realize any kind of voltage transfer functions, for

example, elliptic filter functions, employing the minimum components, only $2n+2$ single-input OTAs, and only n grounded capacitors. The first filter structure enjoys the advantage of single biasing and easy control due to equal transconductance design. The second filter structure achieves the benefit of easy integrated circuit fabrication without tuning the values of capacitors due to equal capacitance design [86]. The second analytical synthesis method produces the third filter structure, a new n th-order OTA-C all-pass filter, far simpler in structure than the recently reported work [7-20].

Chapter 5 designs a new *unified* biquad filter model based on nullators, norators, current mirrors and passive R (resistor) and C (capacitor) elements. Two implementations derived from the new biquad filter model by using second generation current-controlled conveyors (CCCIIs) and operational transconductance amplifiers (OTAs) are also proposed. The two biquad implementations are capable of achieving *five filter performance parameters* simultaneously and without trade-offs, including universal filtering, minimum components count and independent control of ω_o and ω_o/Q . This is unlike recently reported filter structures which make certain trade-offs that emphasize some parameters at the cost of others.

Chapter 6 presents a comparative analysis including a comparison between the current-mode and voltage-mode analytical synthesis methods presented in Chapters 3 and 4, and a comparison between the unified OTA-based and CCCII-based biquad filters presented in Chapter 5. It is supplied for the designers to select an appropriate synthesis method and filter structure.

Chapter 7 summarizes the new current-mode and voltage-mode analytical synthesis methods and their associated filter structure achieving the *three main important criteria*, and two unified OTA-based and CCCII-based biquad filters achieving the *five performance parameters*. Moreover, the complimentary parts of the researches, expanding the innovative core methods to surrounding useful techniques and promoting the theoretical basement to the practical applications, are suggested in Chapter 7 to be the prospective future work.

List of Publications

The work presented in this thesis has resulted in the following conference and journal publications:

[1] Chun-Ming Chang, and Bashir M. Al-Hashimi, “Analytical synthesis of current-mode high-order OTA-C filters”, IEEE Trans. Circuits & Syst.-I, vol. 50, no. 9, pp. 1188-1192, Sept. 2003. (This paper is relevant to the synthesis method discussed in Chapter 3.)

[2] Chun-Ming Chang, Bashir M. Al-Hashimi, Yichuang Sun, and J. Neil Ross, “New high-order filter structures using single-ended-input OTAs and grounded capacitors”, IEEE Trans. Circuits & Syst.-I, accepted for publication on 2 Dec. 2003. (This paper is relevant to the first synthesis method discussed in Chapter 4.)

[3] Chun-Ming Chang, and Bashir M. Al-Hashimi, “Analytical synthesis of voltage-mode OTA-C all-pass filters for high frequency operation”, Proc. IEEE/ISCAS, vol. I, pp. 461-464, Bangkok, Thailand, May, 2003. (This paper is relevant to the second synthesis method discussed in Chapter 4.)

[4] Chun-Ming Chang, Bashir M. Al-Hashimi, and J. Neil Ross, “Unified active filter biquad structures”, IEE Proc.-Circuits Devices Syst., accepted for publication on 7 Jan. 2004. (This paper is relevant to Chapter 5.)

Chapter 2

Background and Literature Review

This Chapter outlines the necessary background information, including OTA and CCII symbols and biquads are introduced in Sections 2.1 and 2.2. The active current-mode and voltage-mode filters are discussed in Section 2.3 and their biquad classification in Section 2.4. A survey of the most relevant and related works is reviewed in Section 2.5 and concluded in Section 2.6 to lead to the research direction of this thesis.

2.1 OTA Symbol and Biquad

The operational transconductance amplifier (OTA) is one of the powerful analogue building blocks. Its functional block is shown in Fig. 2-1 (a). The input-output relationship of an OTA is

$$I_{out} = gV_d \quad (2-1)$$

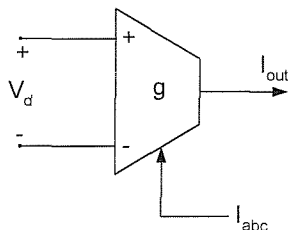


Fig. 2-1 (a) OTA functional block

The transconductance g represents the output current/input voltage ratio I_{out}/V_d . It is adjustable within the range of several decades by a supplied bias current I_{abc} (amplifier bias current). The CMOS implementations of the plus-type and minus-type OTAs are shown in Fig. 2-1 (b) and (c) [80], respectively. The simulated relationship between g and I_{abc} is shown in Fig. 2-1 (d) under $\pm 2.5V$ supply voltages, and $W/L=5\mu/1\mu$ and $10\mu/1\mu$ for NMOS transistors and PMOS transistors, respectively. (Note that the CMOS implementations and the relevant simulated relationship between g and I_{abc} are used to validate the filter simulation described through out this thesis.) Therefore, the OTA provides linear electronic tunability and a wide tunable range of its transconductance gain.

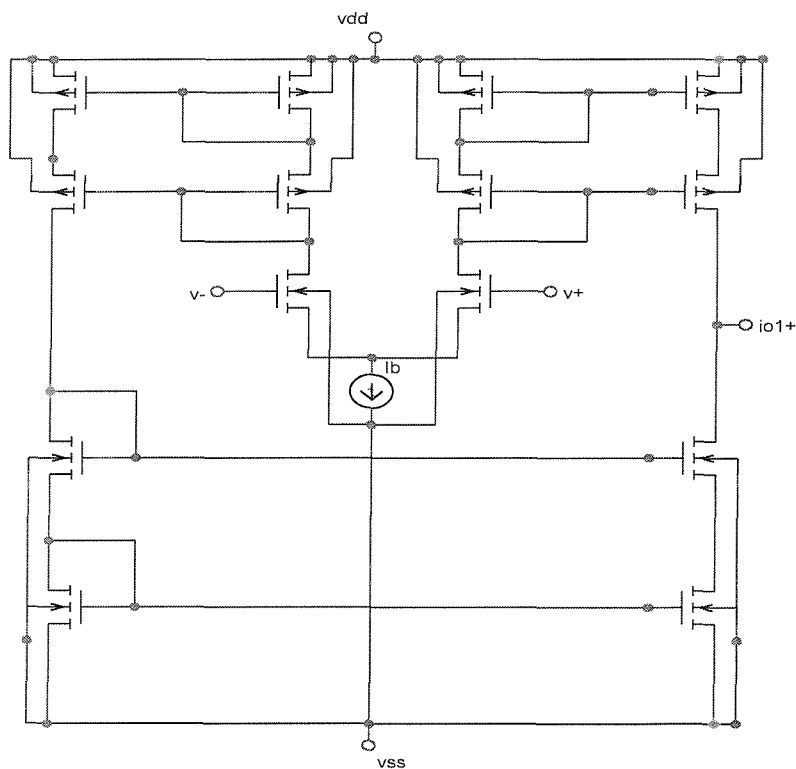


Fig. 2-1 (b) CMOS implementation of a plus-type OTA [80]

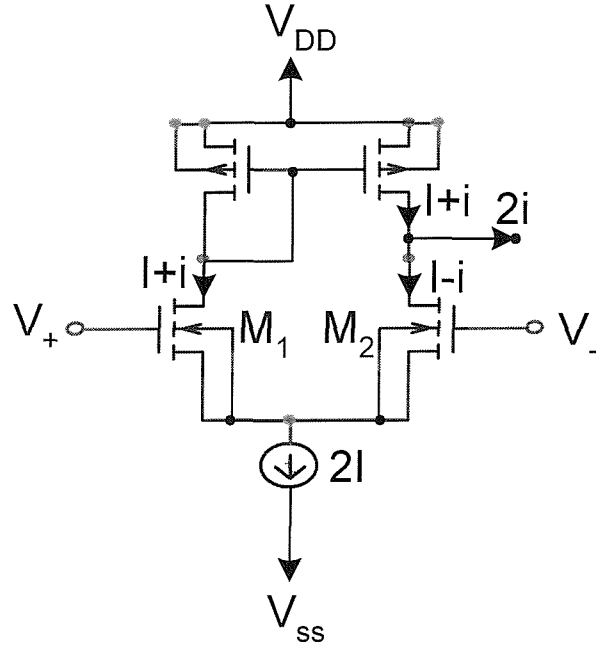


Fig. 2-2 Matched differential pair in the CMOS implementation of an OTA

The core theory of the CMOS implementation of an OTA is relevant to the matched differential pair shown in Fig. 2-2. The detail relationship [74, 75] between the output current signal, $2i$, and the input voltage difference, $V_+ - V_-$, is derived as follows.

Suppose $k_1 = k_2 = k$ and $V_{T1} = V_{T2} = V_T$ because of two matched transistors.

$$\text{Then } I + i = k(V_{GS1} - V_T)^2 \quad (2-2)$$

$$I - i = k(V_{GS2} - V_T)^2 \quad (2-3)$$

And

$$V_+ - V_- \equiv V = V_{GS1} - V_{GS2} = \left(\sqrt{\frac{I+i}{k}} + V_T \right) - \left(\sqrt{\frac{I-i}{k}} + V_T \right) = \sqrt{\frac{I+i}{k}} - \sqrt{\frac{I-i}{k}} \quad (2-4)$$

Do the square operation for both sides of Eq. (2-4).

$$V^2 = \frac{2I}{k} - 2\sqrt{\frac{I^2 - i^2}{k^2}} = \left(\frac{2}{k} \right) \left(I - \sqrt{I^2 - i^2} \right) \quad (2-5)$$

$$\text{Namely, } \sqrt{I^2 - i^2} = I - \frac{kV^2}{2} \quad (2-6)$$

Do the square operation for both sides of Eq. (2-6).

$$I^2 - i^2 = I^2 + \frac{k^2V^4}{4} - kIV^2, \text{ i.e., } i^2 = kIV^2 - \frac{k^2V^4}{4} \quad (2-7)$$

Do the square root for both sides of Eq. (2-7).

$$i = \sqrt{kIV} \sqrt{1 - \frac{kV^2}{4I}} \quad (2-8)$$

Therefore, the transconductance

$$g \equiv \frac{2i}{V_+ - V_-} = \frac{2i}{V} = 2\sqrt{kI} \sqrt{1 - \frac{kV^2}{4I}} = 2\sqrt{kI} \left(1 - \frac{kV^2}{8I}\right) \quad (2-9)$$

The term $\sqrt{1 - \frac{kV^2}{4I}}$, or $\left(1 - \frac{kV^2}{8I}\right)$ causes the nonlinear distortion for large signal inputs.

An OTA-based realisation of a universal biquad proposed by Nawrocki and Klein [21] in 1986 is shown in Fig. 2-3.

(v) all-pass filter: $a_0 = b_0$, $a_1 = -b_1$, and $a_2 = b_2$

The other way of the above filter analysis, i.e., filter synthesis, may be interesting to the reader. Using the new voltage-mode synthesis method proposed in Section 4.2, a new synthesized filter structure is obtained and has two fewer OTAs than that shown in Fig. 2-3. Appendix 1 shows the detailed synthesis process.

2.2 CCII Symbol and Biquad

Although the design using OTAs shown in Fig. 2-3 is most suitable for integration due to the absence of resistors in the circuit, performance limitations of OTAs such as poor bandwidths and poor output drive capabilities may restrict the overall operating performance [28]. The high-performance second-generation current conveyor (CCII) is an attractive alternative to the OTA in this application because of their higher bandwidths and improved current drive capabilities [28]. From its introduction in 1970 by Sedra and Smith [29], CCII, whose functional block is shown in Fig. 2-4, have been proved to be functionally flexible and versatile, rapidly gaining acceptance as both a theoretical and practical building block. From 1985 to 1990, high performance implementations have emerged, to enable conveyors to challenge successfully traditional voltage operational amplifier circuits in areas such as active filters, oscillators, and amplifiers [30]. The input-output relationship of a CCII is

$$\begin{bmatrix} I_y \\ I_{z\pm} \\ V_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix} \quad (2-11)$$

where the positive and negative signs refer to output terminals z^+ and z^- , respectively.

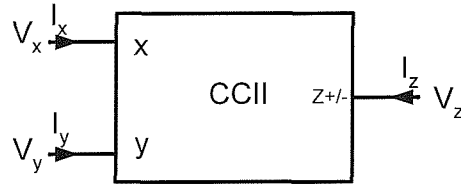


Fig. 2-4 CCII functional block

A CCII-based universal biquad, which is the counterpart of Fig. 2-3, proposed by Toumazou and Lidgey [28] in 1986 is shown in Fig. 2-5.

Circuit analysis of Fig. 2-5 yields the following voltage transfer function:

$$\frac{V_{out}}{V_{in}} = \frac{s^2 C_1 C_2 R_4 R_5 / R_3 + s C_1 R_4 / R_2 + 1 / R_1}{s^2 C_1 C_2 R_4 R_5 / R_8 + s C_1 R_4 / R_7 + 1 / R_6} \quad (2-12)$$

Specialisations of the numerator in Eq. (2-12) result in the following filter functions:

- (i) highpass filter: $R_2 = R_1 = \infty$
- (ii) lowpass filter: $R_3 = R_2 = \infty$
- (iii) bandpass filter: $R_1 = R_3 = \infty$
- (iv) bandreject filter: $R_2 = \infty$, and $R_3 = R_1$
- (v) allpass filter: $R_1 = R_2 = R_3$, $R_6 = R_7 = R_8$, and current conveyor with grounded resistor R_2 must change its output to be z-.

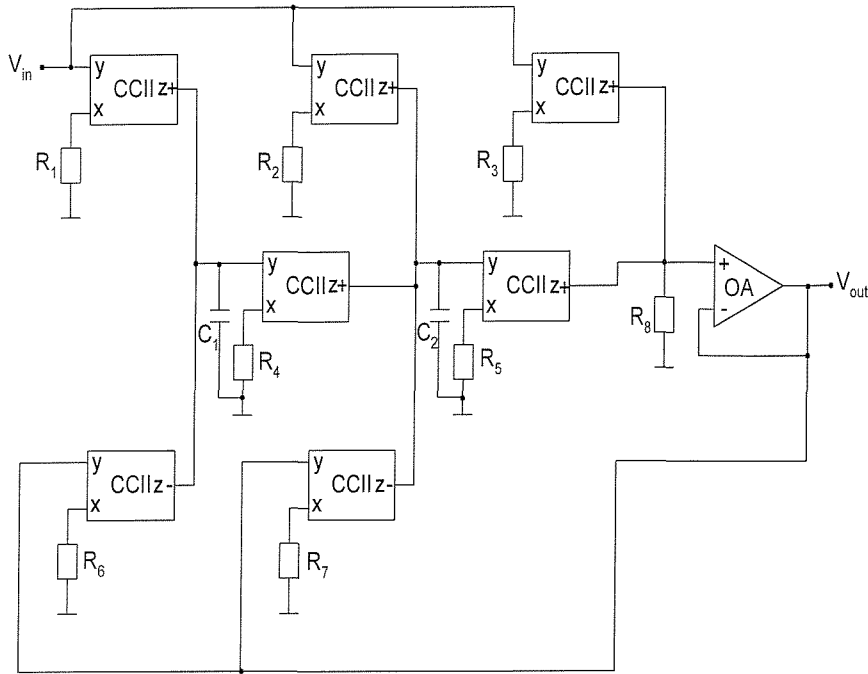


Fig. 2-5 Block diagram of voltage-mode CCII-based universal biquad [28]

In this thesis, Chapter 5 will introduce the CMOS implementations and the simulated relationship between transconductance $g_x (= 1/R_x)$ and bias current I_o of the second-generation current-controlled conveyor (CCCII) which is an improved active element of the CCII and will be used to implement a unified biquad.

2.3 Active Current-Mode and Voltage-Mode Filters

In 1989, Roberts and Sedra proposed that circuits based on current amplifiers operate at higher signal bandwidths, greater linearity and larger dynamic range, than their voltage-based circuit counter-parts [73]. Current-mode circuits have emerged over the last decade as an important class of analogue circuits. One particularly important aspect of the current amplifier is found in the influence of feedback on the amplifier bandwidth. It has been shown that properly applied current feedback will cause the upper -3dB frequency to remain constant and independent of the closed loop gain. This characteristic is extremely important in a circuit like a pipeline analogue-digital converter where the residue amplifier must have large bandwidth. A current amplifier

having a gain of 2^N where N is the number of bits in the pipe would not lose bandwidth compared to a voltage amplifier [76]. These recent advances in integrated circuit technologies have meant that state-of-the-art analogue IC design is now able to exploit the potential of current-mode analogue signal processing, providing attractive solutions for many circuit and system problems. Active filters can be divided into two classes: voltage-mode and current-mode, shown in Fig. 2-6. A voltage mode circuit is defined as a circuit which both the input and output signals are voltages. A current mode circuit has input and output signals which are both currents. Internally, however, the signal may transfer repeatedly between voltage and current [81].

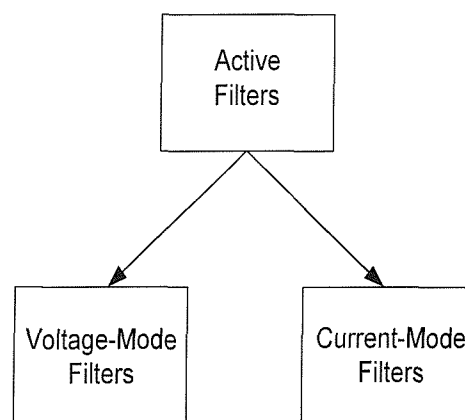


Fig. 2-6 Active filter classification

The OTAs and CCII's described in Sections 2.1 and 2.2 are powerful analogue building blocks, combining voltage and current-mode capability. A number of novel circuit functions and topologies have been explored on the broader front of current-mode analogue circuits, opening up wider areas of interest. A current-mode OTA-based universal biquad and a CCII-based universal biquad proposed by Chang et al. [26] and Toker and Özoğuz [31] in 2000 are shown in Figs. 2-7 and 2-8, respectively.

Using current mirrors, an OTA may have multiple output terminals of both positive and negative polarity as shown in Fig. 2-7. Circuit analysis yields the following current transfer functions of Fig. 2-7:

$$I_{out1} = \frac{[s^2 C_1 C_2 I_{in3} + s C_1 g_2 (I_{in3} - I_{in2}) + g_1 g_2 (I_{in3} - I_{in1})]}{s^2 C_1 C_2 + s C_1 g_2 + g_1 g_2} \quad (2-13)$$

$$I_{out2} = \frac{[-s C_2 g_1 I_{in1} - g_1 g_2 (I_{in1} - I_{in2})]}{s^2 C_1 C_2 + s C_1 g_2 + g_1 g_2} \quad (2-14)$$

$$I_{out3} = \frac{[s C_1 g_2 I_{in2} + g_1 g_2 I_{in1}]}{s^2 C_1 C_2 + s C_1 g_2 + g_1 g_2} \quad (2-15)$$

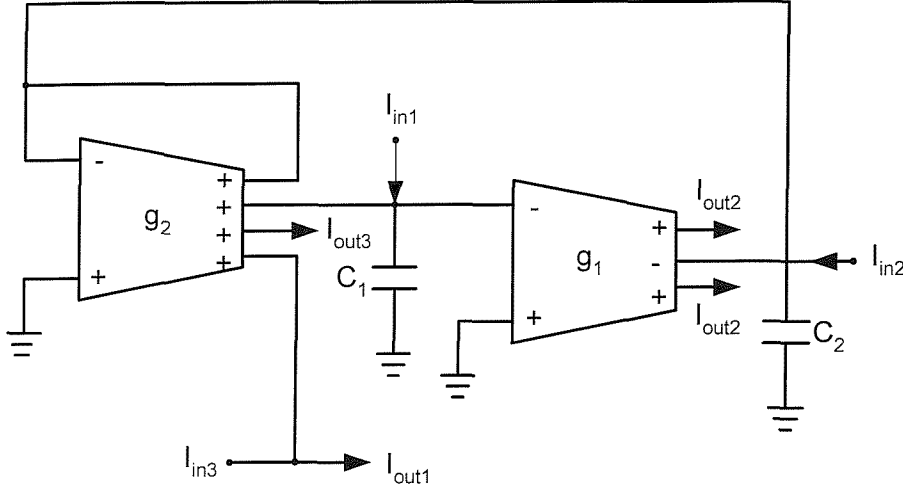


Fig. 2-7 Current-mode OTA-C universal biquad [26]

Similarly, current mirrors make additional output terminals for the CCII's shown in Fig. 2-8. Circuit analysis of Fig. 2-8 yields the following transfer functions:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_2 G_3 + G_1 G_2} \quad (2-16)$$

$$\frac{I_{LP}}{I_{in}} = \frac{G_1 G_2}{s^2 C_1 C_2 + s C_2 G_1 + G_1 G_2} \quad (2-17)$$

$$\frac{I_{BP}}{I_{in}} = \frac{s C_2 G_1}{s^2 C_1 C_2 + s C_2 G_1 + G_1 G_2} \quad (2-18)$$

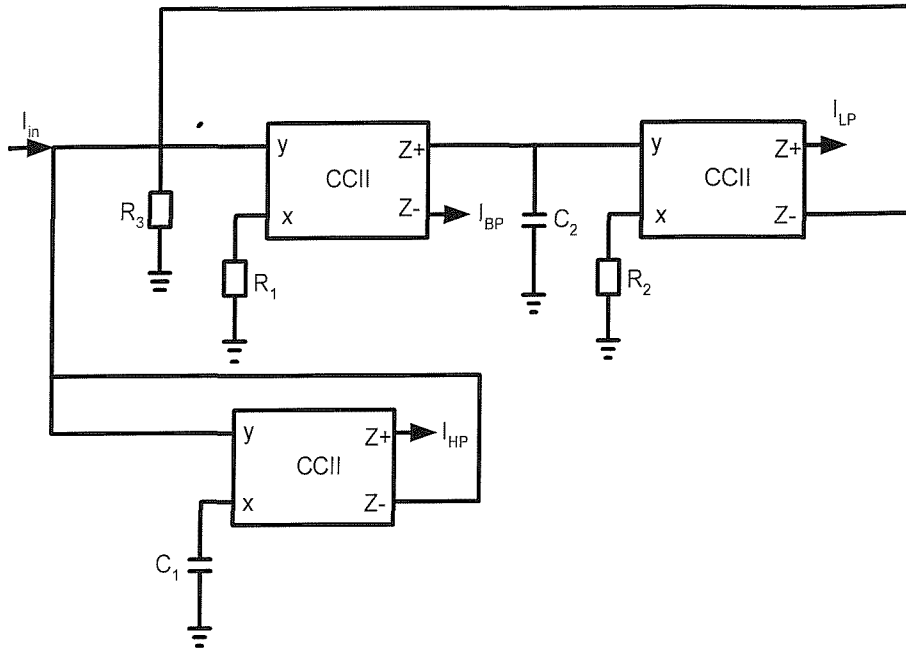


Fig. 2-8 Current-mode CCII-based universal biquad [31]

2.4 Biquad Classification

There are five generic, normalized, biquadratic filtering transfer functions which are:

$$\begin{aligned}
 & \frac{a_0}{a_2 s^2 + a_1 s + a_0}, (\text{low-pass}) \\
 & \frac{a_1 s}{a_2 s^2 + a_1 s + a_0}, (\text{band-pass}) \\
 & \frac{a_2 s^2}{a_2 s^2 + a_1 s + a_0}, (\text{high-pass}) \\
 & \frac{a_2 s^2 + a_0}{a_2 s^2 + a_1 s + a_0}, (\text{band-reject}) \\
 & \frac{a_2 s^2 - a_1 s + a_0}{a_2 s^2 + a_1 s + a_0}, (\text{all-pass})
 \end{aligned} \tag{2-19}$$

Summing a low-pass output signal, and a high-pass output signal, a band-reject output signal can be obtained:

$$\frac{a_2 s^2}{a_2 s^2 + a_1 s + a_0} + \frac{a_0}{a_2 s^2 + a_1 s + a_0} = \frac{a_2 s^2 + a_0}{a_2 s^2 + a_1 s + a_0} \quad (2-20)$$

An all-pass output signal can be obtained by summing a high-pass output, an inverting-type band-pass output, and a low-pass output signals.

$$\frac{a_2 s^2}{a_2 s^2 + a_1 s + a_0} + \frac{-a_1 s}{a_2 s^2 + a_1 s + a_0} + \frac{a_0}{a_2 s^2 + a_1 s + a_0} = \frac{a_2 s^2 - a_1 s + a_0}{a_2 s^2 + a_1 s + a_0} \quad (2-21)$$

Therefore, a low-pass output signal, an inverting-type band-pass output signal, and a high-pass output signal are a set of fundamental generic filtering signals to construct all of the five generic filtering signals, i.e., low-pass, band-pass, high-pass, band-reject, and all-pass. The block diagram of multifunction biquad I is shown in Fig. 2-9 (a).

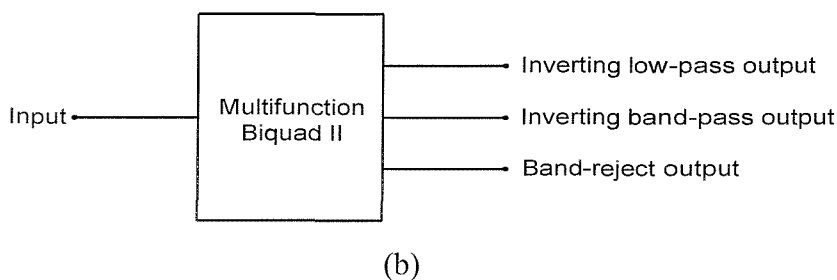
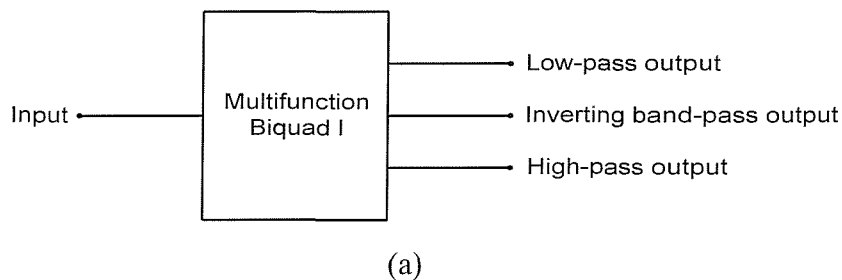


Fig. 2-9 (a) and (b) Block diagrams of single-input, three-output multifunction biquads I and II

The other set of fundamental generic filtering signals to construct all of the five generic filtering signals are an inverting-type low-pass output signal, an inverting-type band-pass output signal, and a band-reject output signal. A high-pass signal can be

obtained by summing a band-reject and an inverting-type low-pass output signals, namely:

$$\frac{a_2s^2 + a_0}{a_2s^2 + a_1s + a_0} + \frac{-a_0}{a_2s^2 + a_1s + a_0} = \frac{a_2s^2}{a_2s^2 + a_1s + a_0} \quad (2-22)$$

An all-pass signal can be obtained by summing a band-reject and an inverting-type band-pass output signals, namely,

$$\frac{a_2s^2 + a_0}{a_2s^2 + a_1s + a_0} + \frac{-a_1s}{a_2s^2 + a_1s + a_0} = \frac{a_2s^2 - a_1s + a_0}{a_2s^2 + a_1s + a_0} \quad (2-23)$$

The block diagram of multifunction biquad II is shown in Fig. 2-9 (b).

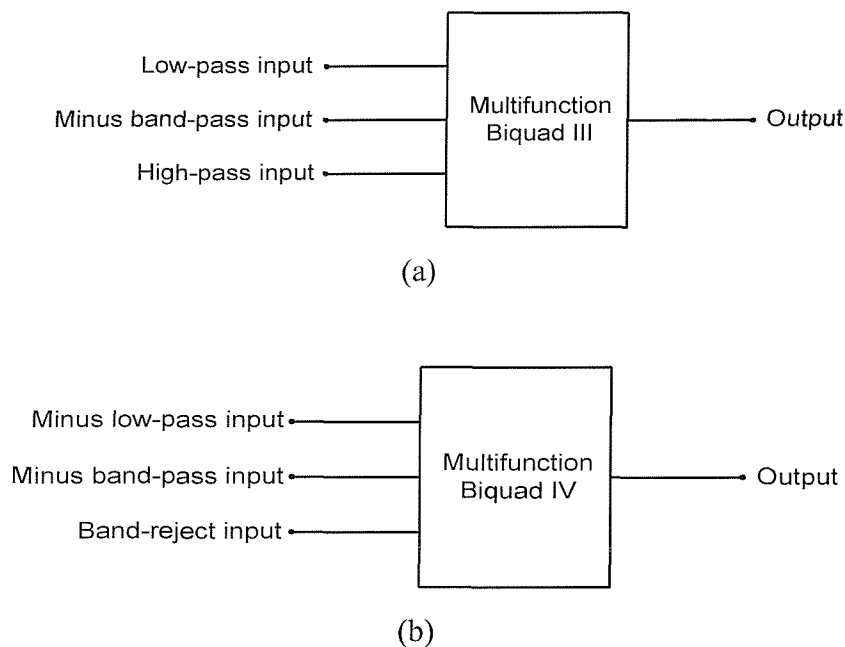


Fig. 2-10 (a) and (b) Block diagrams of three-input, single-output multifunction biquads III and IV

It is also possible to obtain multifunction biquads using three inputs and single output. The block diagrams of multifunction biquads III and IV are shown in Figs. 2-10 (a) and (b). Note that the “low-pass input” presented in Fig. 2-10 (a) means “the input

leading to a low-pass output”, the “minus band-pass input” presented in Figs. 2-10 (a) and (b) means “the input leading to an inverting-type band-pass output”, and so on.

The classification is used to simplify the review of the recently reported various biquads in the next section.

2.5 Literature Review

In Sections 2.5.1 and 2.5.2, the detailed literature reviews will be focused on OTA- and CCII-based biquad filters and high-order filters, respectively. The literature review will lead to the research direction of this thesis presented in the next section.

2.5.1 Review of OTA- and CCII-Based Biquads

To simplify the review, OTA-based biquads are separated from CCII-based biquads.

OTA-Based Biquads

To simplify the review, the biquad has been divided into two parts, current mode and voltage mode as shown in Fig. 2-6.

Current-Mode OTA-Based biquads

A second-order current-mode filter using four OTAs and two grounded capacitors was presented in 1996 [22]. It can realize low-pass, band-pass, high-pass, and band-reject filtering functions but without all-pass filtering function unless component matching conditions is used. Also, independent control of ω_o and ω_o/Q cannot be achieved. In the same year, although a variety of current-mode continuous-time integrator loop filter architectures incorporating OTA and grounded capacitors were generated [23], the best one in [23] retains the same advantages and disadvantages as that in [22]. Employing one fewer OTA, i.e., only three OTAs, but one floating capacitor in addition to one grounded capacitor to construct a current-mode biquad was proposed [24]. The current-mode filter in [24] needs one component matching condition to realize five generic biquadratic functions and cannot provide independent control of

ω_o and ω_o/Q . The current-mode biquad proposed in [24] was improved by the circuit [25], which employed two grounded capacitors instead of one floating and one grounded capacitors. All the biquads proposed in [25] don't require any component matching conditions. However, they cannot enjoy the independent control of ω_o and ω_o/Q . In 2000, Chang and Pai [26] proposed employing only two OTAs and two grounded capacitors, the minimum active and passive components, to realize a current-mode universal biquad which can simultaneously realize low-pass, band-pass, high-pass, band-reject, and all-pass filtering functions without the need of any critical constraints. However, it still suffers from the disadvantage: no independent control of ω_o and ω_o/Q .

Voltage-Mode OTA-Based biquads

In 1998, a voltage-mode OTA-C biquad using three OTAs, one floating and one grounded capacitors was proposed [24]. The voltage-mode biquad needs component matching conditions to realize low-pass and all-pass filtering functions and does not provide the independent control of ω_o and ω_o/Q . The voltage-mode biquad proposed in [24] was improved by three further circuits in [25]. The first two biquads employed two grounded capacitors instead of one floating and one grounded capacitors, and the third biquad employed only two instead of three OTAs. Moreover, all the biquads in [25] don't require any component matching conditions. However, they cannot enjoy the independent control of ω_o and ω_o/Q . In 2002, a voltage-mode universal biquadratic filter with one input and five outputs was proposed [27]. However, it uses five OTAs to realize such a multifunction biquad filter.

CCII-Based Biquads

To simplify the review, the biquad has been divided into two parts, current mode and voltage mode as shown in Fig. 2-6, and classified as multifunction biquads I, II, III, and IV as outlined in Section 2.4.

Current-Mode Multifunction Biquad I/II:

In 1992, Senani [46] proposed a universal current-mode biquad which employs seven current conveyors in addition to two grounded capacitors and three grounded resistors.

This biquad suffers from the following two disadvantages: requirement of one matching condition to realize an all-pass signal, and no orthogonal control of ω_o and Q . The universal filter was improved by Chang [47] in 1993. It does not need any component matching conditions and enjoys the orthogonal control of ω_o and Q . The component count of the universal filter in [47] was reduced in [48] to five current conveyors, two grounded capacitors, and three resistors. Moreover, the proposed universal filter [48] enjoys no component matching and the independent control of ω_o and Q . In 1995, Soliman presented a current-mode universal filter using four CCII, three grounded capacitors, and three grounded resistors with independent control of ω_o and Q but poor performance at high frequency [49]. Abuelma'atti and Khan [50] replaced one CCII with one operational transconductance amplifier (OTA) from Soliman's biquad to design a low component current-mode universal filter. The universal biquad was further improved by Chang and Tu using four dual-output CCII, two grounded capacitors, and two grounded resistors to realize five generic biquad functions from the same structure [51]. In 1997, Özoğuz and Acar used four CCII, two floating capacitors, and two floating resistors to realize a universal current-mode biquad [52]. In 1998, a high output impedance current-mode multifunction filter employing three CCII, one grounded capacitor, one floating capacitor, two grounded resistors, and one floating resistor was proposed by Özoğuz et al. [53]. The use of a floating capacitor and a floating resistor makes the circuit unsuitable for integrated circuit implementation. Moreover, it cannot enjoy low active sensitivities as high quality factor is necessary. Wang and Lee presented a versatile multi-input-multi-output biquad structure [54], which can realize either a three-input single-output or a single-input three-output universal biquad by using three current conveyors. The proposed construction has many advantageous features but still has the two disadvantages: no independent control of ω_o and ω_o/Q and the limitation for high frequency operation. In 2000, Toker and Özoğuz proposed an insensitive current-mode universal filter using three dual output current conveyors, two grounded capacitors, and three grounded resistors which, again, suffered from the limitation for high frequency operation [31]. In 2002, the three-current-output universal biquad filter without the advantage: independent control of ω_o and ω_o/Q was realized by using only two plus-type CCII, two capacitors, and two resistors [58]. Recently, a single-CCII-based universal biquad filter with three inputs and three outputs was proposed using

one active element, two grounded capacitors and two grounded resistors which cannot enjoy the independent control of ω_o and ω_o/Q [59].

In summary, the current-mode CCII-based universal biquads started with seven active elements and two capacitors [46-47], reduced to five active elements and two capacitors [48], four active elements and three capacitors [49-50], four active elements and two capacitors [51-52], then three active elements and two capacitors [53-54, 31], and then two active elements and two capacitors [58], and finally one active element and two capacitors [59].

Voltage-Mode Multifunction Biquad I/II:

In 1991, a current-feedback amplifier (CFA), which is equivalent to a plus-type second-generation current conveyor (CCII) with a voltage follower [32], was proposed. In 1994, Chang *et al.* [33] presented a voltage-mode notch, low-pass, and band-pass filter using three CFAs, which are equivalent to three plus-type second-generation current conveyors and three voltage followers, six active elements in total. In 1994 and 1995, Soliman [34] and Senani *et al.* [35] proposed two different types of Kerwin-Huelsman-Newcomb-equivalent biquads. Each realizes low-pass, band-pass, and high-pass filter transfer functions, using five plus-/minus-type second-generation current conveyors (CCII \pm), two capacitors and six or seven resistors, respectively. In 1995, Celma *et al.* presented a voltage-mode universal biquad using three CCII \pm s, and three voltage followers [36], still six active elements in total. Therefore, before 1996, voltage-mode CCII-based biquads were realized by employing five to six active elements. In 1997, Horng *et al.* [37] proposed a voltage-mode multifunction filter, using four CCII \pm , but three capacitors, and five resistors. In the same year, Chang [38] presented five voltage-mode multifunction biquadratic filters, each of which employs four CCII \pm , two grounded capacitors, and three-five resistors. In 1999, Chang and Lee [39] proposed a simpler voltage-mode low-pass, band-pass, and high-pass filter. This employed only two current conveyors, two grounded capacitors, and three grounded/floating resistors. Recently, a single-CCII-based low-pass, band-pass, high-pass, and band-reject biquad filter was presented using one CCII, two grounded capacitors and two grounded resistors [59]. Both the multifunction biquads [39, 59] suffer from no independent control of ω_o and ω_o/Q .

In summary, the voltage-mode CCII-based biquads started by employing six active elements and two capacitors [33, 36], were reduced to five active elements and two capacitors [34-35], four active elements and three capacitors [37], four active elements and two capacitors [38], then two active elements and two capacitors [39], and finally one active element and two capacitors [59].

Current-Mode Multifunction Biquad III/IV:

In 1991, Chang and Chen [54] published a universal active current biquad with independent control of ω_o and Q using five CCII, two grounded capacitors, and five grounded resistors. Chang et al. improved their previous universal current-mode biquad by using one fewer CCII [55]. In 1999, a universal current-mode active filter was presented by Günes et al., which contains three dual-output current conveyors, two grounded capacitors and two grounded resistors [56]. Recently, Wang and Lee [57] presented a versatile multi-input-multi-output biquad structure, which can realize either a three-input single-output or a single-input three-output universal biquad by using three current conveyors. The proposed circuit has a number of advantageous features but still has the two disadvantages: no independent ω_o and Q control and the limitation for high frequency operation. In 2002, the three-current-input universal biquad filter was realized by using only two plus-type CCII, two capacitors, and two resistors [58] (which is a three-input and three-output universal biquad filter). Recently, a single-CCII-based universal biquad filter with three inputs and three outputs was proposed using one active element, two grounded capacitors and two grounded resistors [59]. The latest two universal biquads [58, 59] suffer from no independent control of ω_o and ω_o/Q .

In summary, the current-mode CCII-based universal biquads started with five active elements [54], were reduced to four active elements [55], then three active elements [56-57], and then two active elements and two capacitors [58], and finally one active element and two capacitors [59].

Voltage-Mode Multifunction Biquad III/IV:

The earlier work [40-44] cannot be realized by using only grounded passive elements, namely, capacitors and resistors. Also, they cannot enjoy the independent control of ω_o and ω_o/Q and the high-input impedance at their three input terminals

simultaneously. Furthermore, they suffer from either inverting type input signals or component choice conditions. Although a high-input impedance universal biquad was proposed [45], the biquad suffers from all of the earlier existing disadvantages. In 2003, the author presented a biquad filter [60] with the addition of advantages such as employment of only grounded capacitors, no need of inverting type input signals, and no need of component matching condition. However, the biquad filter still suffers from (i) employment of one floating resistor, (ii) one input terminal without high-input impedance, and (iii) no independent control of ω_o and ω_o/Q .

2.5.2 Review of OTA- and CCH-Based High-Order Filters

Section 2.5.1 has provided literature review of biquad filters capable of generating second-order filtering functions. In this section, to simplify the review, OTA-based high-order filters are separate from CCII-based high-order filters.

OTA-Based High-Order Filters

In 1989, a generalized approach based on signal flow graph methods for designing filters with only transconductance elements and grounded capacitors was presented [7]. For generating active simulations of the LC-ladder filters, the methods result in circuits where all transconductors except one are identical, making the approach extremely convenient for monolithic realization with systematic design and dense layout. Although derived for single-input transconductance elements, it is shown how the methods can be extended to designs based on differential input or even fully balanced transconductors. As an example, the method employs 23 single-input OTAs and 10 grounded capacitors to realize an eighth-order elliptic band-pass LC-ladder filter. In 1991, a third-order elliptic low-pass filter was proposed [8] which employed 3 single-input OTAs, 5 double-input OTAs, and 4 grounded capacitors. In 1993, an OTA-C realization of general voltage-mode n th-order transfer functions, which is different from simulating passive ladders [7], was presented [9] which used n double-input OTAs, $n+2$ single-input OTAs, and n grounded capacitors. In 1994, a technique employing 3 single-input OTAs, 4 double-input OTAs, and 4 grounded capacitors to realize third-order elliptic filters was presented [10]. In 1994, a methodology to

compensate for the non-ideal performance of the OTA, current-mode filters using single-input multiple-output OTAs and based on RLC ladder filter prototypes was presented [11]. It realized a 5th-order all-pole RLC ladder filter by using seven single-input OTAs, and 5 grounded capacitors, and a third-order elliptic low-pass filter by using seven single-input OTAs, three grounded capacitors and 2 current buffers.

Employing a current-mode integrator and a proportional block as basic building units to reduce the component count, a current-mode n th-order filter configuration was introduced in 1996 [12]. It employs $n+2$ single-input OTAs and n grounded capacitors. In the same year, the voltage-mode filter structure proposed in [13] employs $n+1$ single-input OTAs, $n-1$ double-input OTAs, and n grounded capacitors in order to realize an n th-order voltage-mode transfer function but without the n th-order term in the numerator. On the other hand, employing $2n+2/2n+3$ single-input OTAs and n grounded capacitors to realize an n th-order current-mode general transfer function was also proposed [14]. A systematic generation of current-mode dual-output OTA filters using a building block approach was developed in 1997 [15]. It uses four single-input OTAs and two grounded capacitors to realize a second-order high-pass or notch, namely, band-reject filter under some component matching conditions. In the same year, employing n double-input OTAs, $n+2$ single-input OTAs, and n grounded capacitors to realize a general n th-order voltage-mode transfer function was proposed [16]. In 1998, a design approach based on simulating RLC ladder networks using coupled-biquad structures was presented [17]. Applying this approach, it needs 7 single-input OTAs, and 7 grounded capacitors to realize a fifth-order all-pole low-pass ladder filter, needs 9 single-input OTAs, and 6 grounded capacitors to realize a sixth-order all-pole band-pass ladder filter, and needs five OTAs, one of which is double-input OTA, four grounded capacitors, and a current buffer to realize a third-order elliptic low-pass filter. In the same year, using inductor substitution and Bruton transformation methods to realize an LC ladder filter was proposed [18]. To realize a third-order voltage-mode low-pass ladder filter needs five OTAs, two of which are double-input OTAs, and three grounded capacitors. Then, it was demonstrated that the two predominant methods for simulating an active LC ladder result in the same OTA-C filter circuit [19]. To realize fourth-order shunt or series ladder arms need seven single-input OTAs and four grounded capacitors. Recently, in order to minimize the feed-through effects or unexpected signal paths due to the finite parasitic input

capacitance of the OTA, a circuit was developed which employed $3n+3$ OTAs, only one of which is double-input OTA, and n grounded capacitors to realize a general voltage-mode n th-order transfer function [20].

Table 2-1 Comparison of recently reported high-order OTA-C filters

Advantages Methods	The least number of OTAs	Employment of single-input OTAs	Employment of grounded capacitors	The least number of capacitors
Tan and Schaumann in 1989 [7]	No (23 for 8 th -order band-pass)	Yes	Yes	No (10 for 8 th -order band-pass)
Ananda Mohan in 1991 [8]	No (8 for 3rd-order low-pass)	No (e.g. 3 single-input but 5 double-input OTAs)	Yes	No (4 for 3rd-order low-pass)
Sun and Fidler in 1993 [9]	No ($2n+2$ for n th-order transfer functions)	No (e.g. $n+2$ single-input but n double-input OTAs)	Yes	Yes
Hwang et al. In 1994 [10]	No (7 for 3rd-order low-pass)	No (e.g. 3 single-input but 4 double-input OTAs)	Yes	No (4 for 3rd-order low-pass)
Ramirez-Angulo et al. In 1994 [11]	Yes (Sometimes) No (Sometimes)	No	Yes	Yes
Tsukutani et al. in 1996 [12]	No ($n+2$ for n th-order transfer functions)	Yes	Yes	Yes
Sun and Fidler in 1996 [13]	No ($2n$ for ($n-1$)th-order transfer functions)	No (e.g. $n+1$ single-input but $n-1$ double-input OTAs)	Yes	No (n for ($n-1$)th-order transfer functions)
Sun and Fidler (CM) in 1996 [14]	No ($2n+2/2n+3$ for n th-order filters)	Yes	Yes	Yes
Moniri and Al-Hashimi in 1997 [15]	Yes (Sometimes) No (Sometimes)	Yes	Yes	Yes
Sun and Fidler in 1997 [16]	No ($2n+2$ for n th-order transfer functions)	No (e.g. $n+2$ single-input but n double-input OTAs)	Yes	Yes
Wu and El-Masry in 1998 [17]	No (7 for 5 th -order low-pass)	Yes (Sometimes) No (Sometimes)	Yes	Yes (Sometimes) No (Sometimes)

Sun in 1998 [18]	Yes (Sometimes) No (Sometimes)	No (e.g. 3 single-input but 2 double-input OTAs)	Yes (Sometimes) No (Sometimes)	Yes
Schaumann in 1998 [19]	No (7 for 4 th -order ladder arms)	Yes	Yes	Yes (4 for 4 th -order ladder arms)
Barbargires in 1999 [20]	No (3n+3 for nth-order transfer functions)	No e.g. 3n+2 single-input but 1 double-input OTAs)	Yes	Yes

Based upon the *three main important criteria* already outlined in Chapter 1, a summary of the performance parameters of the filter reported in [7-20] are given in Table 2-1. As can be seen, none of the filters are capable of achieving the *three main important criteria* simultaneously.

Moreover, none of the filters in [7-20] use the analytical synthesis method such as differential analyzer [1-2], Tow-Thomas algebraic decomposition [3-5], and Ping-Sewell matrix decomposition [6].

High-Order CCH-Based Filters

In 1995, Günes and Anday employed $3n+2$ CCII, $n+1$ grounded capacitors and $3n-1$ grounded resistors to realize an n th-order voltage-mode general filter structure [67]. In [68], it was shown that $n+1$ CCII, n grounded capacitors and resistors are needed to realize an n th-order current-mode low-pass filter structure. In 1996, Acar replaced grounded passive elements with floating passive elements to reduce the number of active elements (CCII) for realizing voltage transfer functions [69-72]. Firstly, Acar employed n grounded or floating capacitors, n floating resistors, and n CCII to realize an n th-order voltage-mode low-pass transfer function [69]. Secondly, Acar employed n grounded or floating capacitors, $2n+1$ floating resistors, 2 grounded resistors, and $n+1$ CCII to realize an n th-order voltage-mode all-pass transfer function [70]. The same author also showed that the CFA could be used in place of the CCII to realize an n th-order voltage-mode general transfer function [71]. Finally, Acar and Özoğuz employed n grounded capacitors, $2n+2$ floating and one grounded resistors, and $n+2$

CCIIs to realize an n th-order voltage-mode general transfer function [72]. A summary of the performance parameters of the filter reported in [67-72] is given in Table 2-2. As can be seen, all the CCII-based high-order filters except the low-pass filters use many resistors, unlike the OTA-based high-order filters without resistors.

Table 2-2 Comparison of recently reported high-order CCII-based filters

Item Case	Number of CCIIs	Number of Capacitors	Number of Resistors	Functions
[67]	$3n+2$	$n+1$ grounded capacitors	$3n-1$ grounded resistors	General Functions (VM)
[68]	$n+1$	n grounded capacitors	n grounded resistors	Low-pass (CM)
[69]	n	n capacitors	n floating resistors	Low-pass (VM)
[70]	$n+1$	n capacitors	$2n+3$ resistors	All-pass (VM)
[71]	$n+1^*$	n grounded capacitors	$5n+3$ resistors	General Functions (VM)
[72]	$n+2$	n grounded capacitors	$2n+3$ resistors	General Functions (VM)

* The active element is the CFA, which is obtained by one plus-type CCII in cascade with a voltage follower.

2.6 Concluding Remarks

The background and literature review relevant to the subject concerned in this thesis has been presented in Sections 2.5 and 5.1. As can be seen, despite the extensive literature on active filters:

1. None of the high-order filters use the analytical synthesis method such as differential analyzer [1-2], Tow-Thomas algebraic decomposition [3-5], and Ping-Sewell matrix decomposition [6].

2. None of the high-order OTA-C filters are capable of achieving the *three main important criteria*, described in Chapter 1, simultaneously.

3. None of the biquads are capable of achieving the *five performance parameters*, described in Chapter 1, simultaneously.

Problems 1 and 2 have been addressed and new synthesis methods for high-order current-mode and voltage-mode OTA-C filters have been presented in Chapters 3 and 4. Problem 3 has been achieved and presented in Chapter 5.

Chapter 3

Current-Mode High-Order OTA-C

Filters Synthesis

Arguably, the most elegant solution to a filter synthesis problem is to decompose analytically the required filter transfer function into a set of equations that can be realized using simple analogue processing blocks such as integrators. This analytical approach is clearly demonstrated in [3-5, 84] in the case of the well-known Tow-Thomas active RC biquad, where the second-order transfer function is manipulated algebraically until a set of equations are produced which are then realized using two integrators and an inverting amplifier. The analytical synthesis approach has many benefits; for example the ability to generate filter circuits in a systematic and structured way, and the ability to obtain filter circuits with different transfer functions (i.e. responses) simply by suitable choice of equations. Furthermore, analytical synthesis offers the designer explicit relations that provide insight into the filters behaviour.

Despite the importance of analytical synthesis approach, few current-mode methods have been reported [11-12, 14-15, 17]. Probably, one of the main reasons for the lack of reported work on analytical synthesis of high-order active filters is due to the difficulties involved in developing a coherent approach for solving a single complicated equation representing an n th-order filter transfer function with different responses; under the constraint that the generated set of equations must be realizable using simple circuitry. Also, mechanisms need to be developed for managing efficiently the intermediate solutions generated throughout the synthesis process, and deriving meaningful conclusions from the final solutions. The motivation behind this work is to develop an efficient analytical synthesis approach for high-order current mode OTA-C filters. The method is based on the analytical decomposition of a single,

nth-order generic filter transfer function into n simple and feasible equations, produced following the application of a succession of innovative algebra manipulation operations. Such filters have now become a creditable alternative to switched-capacitor filters in low and high frequency applications, recent examples [77-79].

This chapter presents two new current-mode analytical synthesis methods and their filter architectures (Sections 3.3 and 3.4). The sensitivity analysis (Section 3.5), comparison with previous work (Section 3.6), and simulation results (Section 3.7) are also included.

3.1 Preliminaries

Any linear electronic systems may be described by a transfer function. Therefore, to design an electronic system is to realize a corresponding transfer function. To facilitate the understanding of the described synthesis methods, we divide transfer functions into two types, simple and complicated, defined as follows:

Definition 3.1: A simple transfer function is a transfer function which can be realized easily.

Example 3.1: The transfer function $\frac{V_{out}}{V_{in}} = \frac{1}{1+s}$ is a simple transfer function because it

is easily manipulated to $\frac{1/s}{1/s+1}$ which is realized by the simple circuit shown in Fig.

3-1.

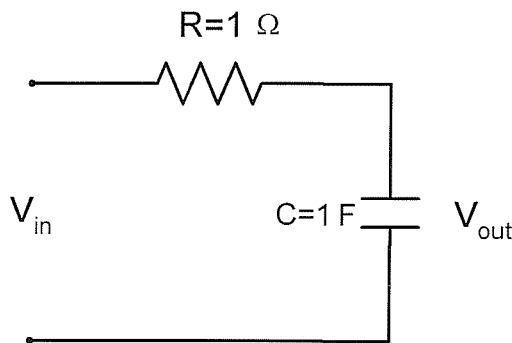


Fig. 3-1 Example 3.1 circuit

Definition 3.2: A complicated transfer function is a transfer function which cannot be realized easily.

Example 3.2: The transfer function

$$I_{out} = \frac{a_n I_n s^n + a_{n-1} I_{n-1} s^{n-1} + a_{n-2} I_{n-2} s^{n-2} + a_{n-3} I_{n-3} s^{n-3} + \dots + a_1 I_1 s + a_0 I_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0}, \quad \text{where}$$

$I_0, I_1, I_2, \dots, I_{n-3}, I_{n-2}, I_{n-1}, I_n$ are the $n+1$ input current signals and I_{out} is the only output current signal. Clearly, This transfer function cannot be easily realized. How to realize a complicated transfer function is a question which this chapter aims to address. Since a simple transfer function is easily realized, to decompose a complicated transfer function into many simple transfer functions become a natural approach to realize a complicated transfer function.

With the increasing emphasis on system design in fully integrated form, it is important that continuous-time filter circuits can also be realizable monolithically, in a method that is compatible with common IC technologies. Their topologies and component types should be such that the circuits are easy to realize and they should be electronically tunable to allow for unavoidable fabrication tolerances and drifts during operating. Furthermore, if the filters can be constructed in a way that minimizes the number of different fundamental building blocks or sub-circuits, IC implementation will be simplified significantly because of the resulting systematic and easy-to-automate IC layout and design. Clearly, the minimal set of components must be able to realize the required frequency-parameters (time constants) and, therefore, must contain conductances and capacitors. In addition, gain is necessary for the realization of complex poles because the poles of passive RC-circuits are restricted to the negative real axis. Combining gain with conductances into transconductances, it may be concluded that tunable transconductors and grounded capacitors form the optimal minimal set of components necessary for building any active filter and, in particular, fully integrated active filters. Tunable transconductors and grounded capacitors are easy to implement in all IC technologies. Although the dynamic range and efficiency of the differential pair of a tunable transconductor are limited due to its large signal nonlinear characteristics (see Section 2.1), several techniques, for example, adaptive

biasing, class-AB, source degeneration, and current differencing have recently been proposed [76] to improve the linearity of MOS transconductance elements. Therefore, tunable transconductors and grounded capacitors are particularly convenient and compatible with digital system implementations using CMOS technology where several linear tunable transconductance elements are already available [15-18] and grounded capacitors are natural for the simplest single-poly process and absorbing shunt parasitic capacitances. Therefore, the operational transconductance amplifier (OTA) and grounded capacitors will be the building blocks of the presented synthesized circuits as shown in Sections 3.3 and 3.4.

3.2 Criteria and Design Notes of the Synthesis Methods

In section 2.5.2 of Chapter 2, the review of high-order OTA-C filters shows that there are not any previous works [7-20], which achieve simultaneously the *three main important criteria* as outlined in Chapter 1. To achieve the *three main important criteria*, the simple transfer function decomposed from a complicated transfer function must be consistent with the following four corresponding notes.

Note 3.1: Any terms, derived from a complicated transfer function, should avoid the form: $sC(V_i - V_j)$ where C is a capacitance and V_i, V_j are two different nonzero voltages.

Clearly, the term $sC(V_i - V_j)$ leads to a floating capacitor with the following structure:

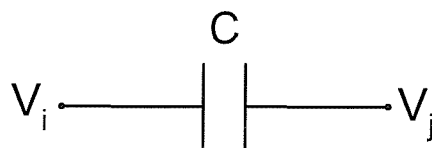


Fig. 3-2 Floating capacitor

Note 3.2: Any terms, derived from a complicated transfer function, should avoid the form: $g(V_i - V_j)$, where g is a transconductance, and V_i, V_j are two different nonzero voltages.

Clearly, the term $g(V_i - V_j)$ leads to a double-input OTA shown in Fig. 3-3.

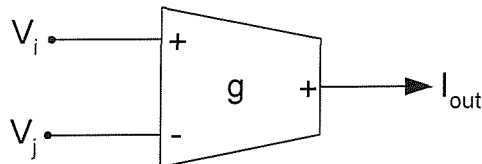


Fig. 3-3 Double-input OTA

Note 3.3: In the decomposition of a complicated transfer function, the separation or division of any of the coefficients into several parts should be avoided.

For example, one should avoid $a_i = a_{i1} + a_{i2}$ in our derivation because, in general, each coefficient is realized by an element. Therefore, if one wants to have the least number of components in the realized circuit, the separation or division of a coefficient should be avoided.

Kirchhoff's voltage law and Kirchhoff's current law are two fundamental laws in an ordinary analysis process. However, Kirchhoff's voltage law leads to components in series such as the case shown in Fig. 3-4 where the rectangle block represents a passive element (resistor or capacitor). Note that all the components in Fig. 3-4 need to be floating. However, Kirchhoff's current law leads to shunt components such as the case shown in Fig. 2-5, where all the components in Fig. 3-5 are grounded. If only grounded capacitors and the single-input OTAs are required, the following important note is needed in the new synthesis method.

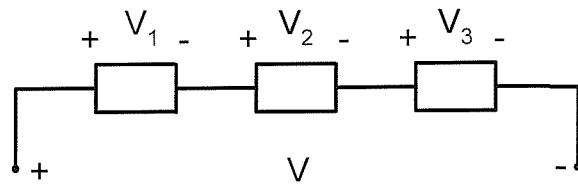


Fig. 3-4 Series of components

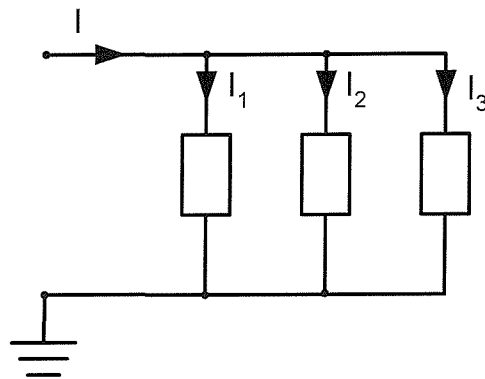


Fig. 3-5 Shunt of components

Note 3.4: The use of Kirchhoff's voltage law to perform the analytical synthesis approach should be avoided. On the contrary, the use of Kirchhoff's current law should be encouraged.

The above four notes are combined and applied to two new analytical synthesis methods, shown in Sections 3.3 and 3.4, for realizing current-mode high-order OTA-C filters.

3.3 Analytical Synthesis Method I: MISOC Method

The analytical synthesis method is based on the analytical decomposition of a single, n th-order generic filter transfer function into n first order current mode transfer functions generated by the application of a succession of innovative algebra manipulation operations. The simple transfer functions are realized using integrator circuits with suitably selected current injection(s) at their inputs or current

extraction(s) at their outputs, and connected using easy-to-follow rules, to yield the required filter order and function (low-pass, high-pass, band-pass, band-reject, all-pass).

The first method is based on an n th-order generic filter structure with multiple input currents, and a single output current (MISOC).

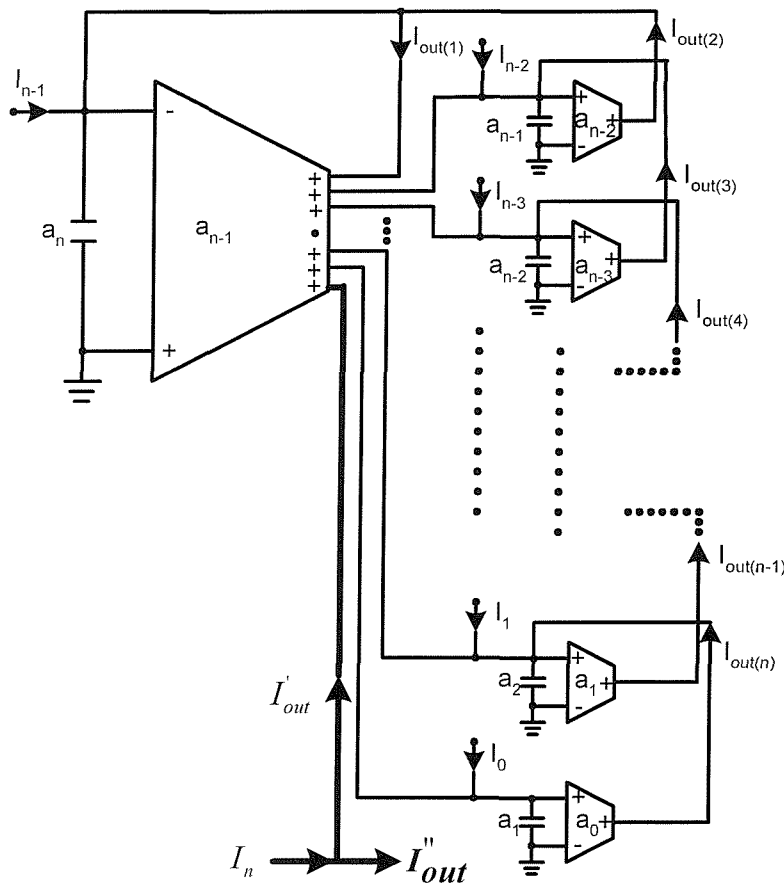


Fig. 3-6 Nth-order OTA-C generic filter structure of the MISOC synthesis method

The n th-order generic filter structure of the MISOC synthesis method is shown in Fig. 3-6, where I_n, I_{n-1}, \dots, I_0 are the filter input currents whose setting determines the filter function (LP, HP, BP, BR, AP) as shown later, and I_{out}'' is the filter current output. The filter structure of Fig. 3-6 was obtained as follows.

The transfer function of the nth-order filter which will be considered, where the value of the coefficients $(a_n, a_{n-1}, a_{n-2}, \dots, a_1, a_0)$ determine the filter function may be written in the form:

$$I_{out} = \frac{a_n I_n s^n + a_{n-1} I_{n-1} s^{n-1} + a_{n-2} I_{n-2} s^{n-2} + a_{n-3} I_{n-3} s^{n-3} + \dots + a_1 I_1 s + a_0 I_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0} \quad (3-1)$$

where the a_i are positive real numbers and the I_i are the current signals relevant to the input current signal, I_{in} . The above transfer function is obtained by the expansion of the three-input and a single output universal biquad structure whose block diagram is shown in Fig. 2-11. In fact, it leads to a much simpler circuit structure to have more input signals (this is like a job will be done much easier if many people do it together). On the other hand, we notice that the coefficients, a_i , in the numerator are given by the same as those in the denominator. To realize a general transfer function with the coefficients in the numerator different from those in the denominator was proposed in [14]. The fewer the different coefficients in a transfer function the simpler is the synthesized circuit structure. Therefore, some special filters, such as Causer or Elliptic filters, whose transfer functions are not consistent with the form shown in Eq. (3-1), cannot be obtained by realizing Eq. (3-1). However, the proposed synthesis method can realize the filters such as Butterworth, Chebyshev, and Bessel-Thomson filters.

The proposed new analytical synthesis method has five steps, they are explained as follows.

Step 1: Decompose the output current I_{out} into two parts, I'_{out} and I''_{out} , namely,

$$\text{Let, } I_{out} = I''_{out} + I'_{out}$$

$$\text{where, } I''_{out} = \frac{a_n I_n s^n}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0} \quad (3-2)$$

$$I'_{out} = \frac{a_{n-1} I_{n-1} s^{n-1} + a_{n-2} I_{n-2} s^{n-2} + a_{n-3} I_{n-3} s^{n-3} + \dots + a_1 I_1 s + a_0 I_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0} \quad (3-3)$$

Step 2: Deal with the I'_{out} part shown in Eq. (3-3) algebraically.

Cross multiply Eq. (3-3),

$$(a_n s^n + a_{n-1} s^{n-1} + \dots + a_1 s + a_0) I'_{out} = a_{n-1} I_{n-1} s^{n-1} + a_{n-2} I_{n-2} s^{n-2} + \dots + a_1 I_1 s + a_0 I_0$$

Divide it by $a_n s^n$,

$$\left(1 + \frac{a_{n-1}}{a_n s} + \dots + \frac{a_1}{a_n s^{n-1}} + \frac{a_0}{a_n s^n}\right) I'_{out} = \frac{a_{n-1}}{a_n s} I_{n-1} + \frac{a_{n-2}}{a_n s^2} I_{n-2} + \dots + \frac{a_1}{a_n s^{n-1}} I_1 + \frac{a_0}{a_n s^n} I_0$$

And re-arrange,

$$I'_{out} = \sum_{i=0}^{i=n-1} \left(\frac{a_i}{a_n s^{n-i}} \right) (I_i - I'_{out}) \quad (3-4)$$

$$\text{Let, } \frac{a_{n-2}}{a_n s^2} = \left(\frac{a_{n-2}}{a_{n-1} s} \right) \left(\frac{a_{n-1}}{a_n s} \right), \quad \frac{a_{n-3}}{a_n s^3} = \left(\frac{a_{n-3}}{a_{n-2} s} \right) \left(\frac{a_{n-2}}{a_{n-1} s} \right) \left(\frac{a_{n-1}}{a_n s} \right)$$

$$\text{Generally, } \frac{a_{n-i}}{a_n s^i} = \prod_{j=0}^{j=i-1} \left(\frac{a_{n-j-1}}{a_{n-j} s} \right) \text{ for } i = 1, 2, 3, \dots, n-1, n. \quad (3-5)$$

Substituting Eq. (3-5) into the last three terms of Eq. (3-4), we have

$$\begin{aligned} & \left(\frac{a_{n-1}}{a_n s} \right) (I_{n-1} - I'_{out}) + \left(\frac{a_{n-2}}{a_{n-1} s} \right) \left(\frac{a_{n-1}}{a_n s} \right) (I_{n-2} - I'_{out}) + \left(\frac{a_{n-3}}{a_{n-2} s} \right) \left(\frac{a_{n-2}}{a_{n-1} s} \right) \left(\frac{a_{n-1}}{a_n s} \right) (I_{n-3} - I'_{out}) \\ &= \left[(I_{n-1} - I'_{out}) + \left[(I_{n-2} - I'_{out}) + \left(\frac{a_{n-3}}{a_{n-2} s} \right) (I_{n-3} - I'_{out}) \right] \left(\frac{a_{n-2}}{a_{n-1} s} \right) \right] \left(\frac{a_{n-1}}{a_n s} \right) \end{aligned}$$

Generally, Eq. (3-4) becomes:

$$I'_{out} = \left[(I_{n-1} - I'_{out}) + \left[(I_{n-2} - I'_{out}) + \dots + \left[(I_1 - I'_{out}) + \left(\frac{a_0}{a_1 s} \right) (I_0 - I'_{out}) \right] \left(\frac{a_1}{a_2 s} \right) \dots \left[\left(\frac{a_{n-2}}{a_{n-1} s} \right) \right] \left(\frac{a_{n-1}}{a_n s} \right) \right] \right] \quad (3-6)$$

Step 3: From the derived equation given by Step 2, n realizable simple equations, each of which represents an integrator circuit, can be extracted out and realized, i.e.,

$$\text{If we let, } I_{out(n)} = \left(\frac{a_0}{a_1 s} \right) (I_0 - I'_{out}), \quad (3-7a)$$

Then from Eq. (3-6), we have the following (n-1) individual equations:

$$I_{out(i)} = (I_{n-i} - I'_{out} + I_{out(i+1)}) \left(\frac{a_{n-i}}{a_{n-i+1} s} \right), \text{ for } i = 1, 2, 3, \dots, n-1,$$

$$\text{where, } I_{out(1)} \equiv I'_{out} \quad (3-7b)$$

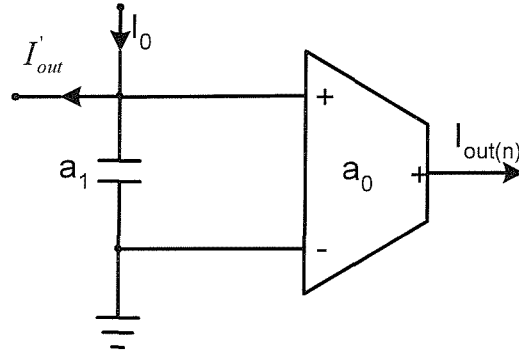


Fig. 3-7. OTA-C realization of the integrator given by Eq. (3-7a)

Eq.(3-7a) represents an integrator, and can be realized using the circuit shown in Fig. 3-7, where a_o is the transconductance of the OTA, and a_1 is the value of the capacitor. Both a_o and a_1 are normalized to $f_o=1\text{Hz}$. Note that we replace an output “+” sign in the previous OTA with an arrow pointing out the output terminal of the

OTA, shown in Fig. 3-7. Implementing Eqs. 3-7(b) using similar circuits to that shown in Fig. 3-7, the combination of the individual circuit yields the generic filter structure shown in Fig. 3-6, apart from the two currents, I_n and I_{out}'' , marked bold in Fig. 3-6. Note that all the OTA's are single-input active elements. The multiple output terminals of the OTA with transconductance a_{n-1} are easily obtained by using current mirrors.

Up to this point, only I_{out}' of the general transfer function has been implemented.

Now, I_{out}'' of Eq. (3-1) is implemented. From Eq. (3-2),

$$\frac{I_{out}''}{I_n} = \frac{a_n s^n}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0}$$

Step 4: Realize the I_{out}'' part shown in Eq. (3-2) by using the mathematical relationship between I_{out}'' and I_{out}' .

Eq. (3-2) can be re-written as

$$\frac{I_{out}''}{I_n} = 1 - \frac{a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0} \quad (3-8)$$

Let, $I_{n-1} = I_{n-2} = I_{n-3} = \dots = I_1 = I_o = I_n$ in Eq. (3-3) gives

$$\frac{I_{out}'}{I_n} = \frac{a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0} \quad (3-9)$$

$$\text{Substituting Eq. (3-9) into Eq. (3-8) yields: } I_{out}'' = I_n - I_{out}' \quad (3-10)$$

Eq.(3-10) is easily realized as shown marked bold in the circuit of Fig.3-6 but $I_{out}'' = I_{out}'$ under the only condition: $I_n = I_{n-1} = I_{n-2} = \dots = I_1 = I_o = I_n$. Note if all the input currents of the structure in Fig. 3-6 are equal, i.e.,

$I_n = I_{n-1} = I_{n-2} = I_{n-3} = \dots = I_1 = I_0 = I_{in}$, then the circuit shown in Fig. 3-6 implements a high-pass filter of nth-order.

Step 5: To generate other filtering functions beside high-pass from the circuit shown in Fig. 3-6, suitable setting of the filter input currents are needed as follows. Substituting Eq. (3-3) into $I''_{out} = I_n - I'_{out}$, shown in Fig. 3-6, yields

$$I''_{out} = \left(\frac{1}{\Delta} \right) \left[a_n I_n s^n + \sum_{i=0}^{i=n-1} a_i s^i (I_n - I_i) \right] \quad (3-11)$$

where $\Delta = a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_2 s^2 + a_1 s + a_0$. This shows that if an nth-order inverting low-pass filter is required, setting $I_o = I_{in}$ and $I_1 = I_2 = I_3 = \dots = I_{n-2} = I_{n-1} = I_n = 0$ in Eq. (3-11) will produce a low-pass response. Fig.3-8 shows a 7th-order low-pass filter obtained using the MISOC synthesis method. The filter output is:

$$I''_{out} = \frac{-a_0 I_{in}}{a_7 s^7 + a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (3-12)$$

Other filter transfer functions are obtained according to the following input current conditions:

(i) Band-pass: If n is even, then $I_{(n/2)} = I_{in}$, whilst all the other input currents are zero. If n is odd, then the input current I_{in} , is applied to either $I_{[(n/2)-(1/2)]}$ or $I_{[(n/2)+(1/2)]}$. For example, Fig.3-9 shows a 6th-order band-pass filter using the MISOC synthesis technique. The filter output is

$$I''_{out} = \frac{-a_3 s^3 I_{in}}{a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (3-13)$$

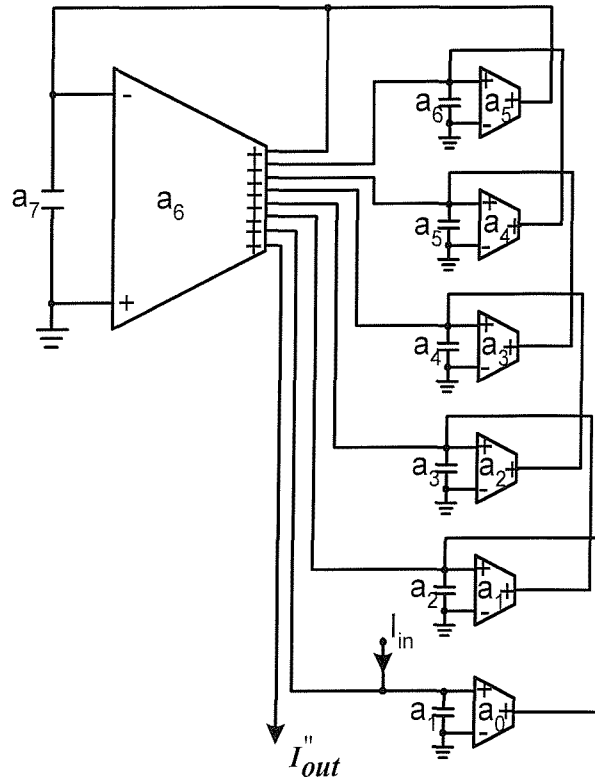


Fig.3-8 7th-order low-pass OTA-C filter using the MISOC synthesis method

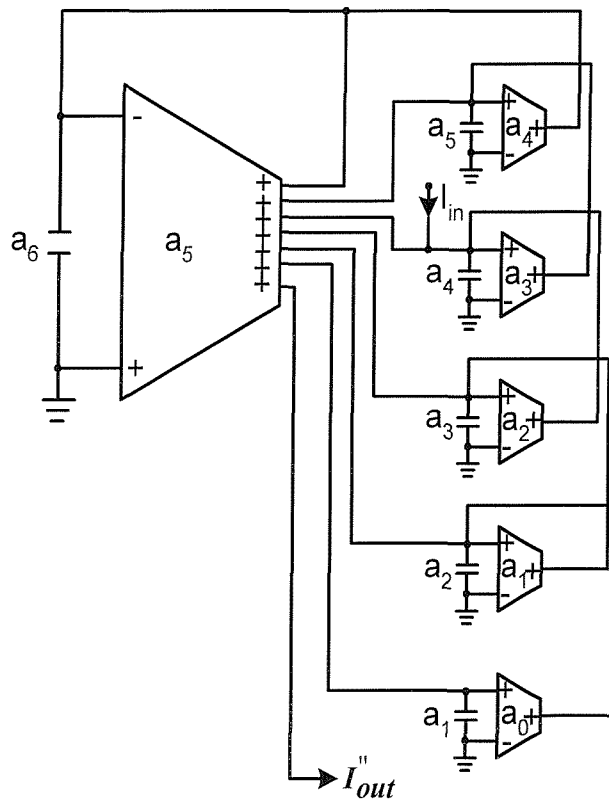


Fig.3-9 6th-order band-pass OTA-C filter using the MISOC synthesis method

(ii) Band-reject: Set $I_n = I_o = I_{in}$, whilst all the other input currents of the filter structure in Fig.3-6 are zero. For example, a proposed 6th-order band-reject filter has the output function shown as below.

$$I_{out}'' = \frac{(a_6s^6 + a_0)I_{in}}{a_6s^6 + a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0} \quad (3-14)$$

(iii) All-pass: If n is even, then $I_n = I_{in}$, $I_{n-1} = 2I_{in}$, $I_{n-2} = 0$, $I_{n-3} = 2I_{in}$, $I_{n-4} = 0$, ..., $I_2 = 0$, $I_1 = 2I_{in}$, and $I_0 = 0$. If n is odd, then $I_n = I_{in}$, $I_{n-1} = 2I_{in}$, $I_{n-2} = 0$, $I_{n-3} = 2I_{in}$, $I_{n-4} = 0$, ..., $I_2 = 2I_{in}$, $I_1 = 0$ and $I_0 = 2I_{in}$. For example, a proposed 6th-order all-pass filter has the output function shown as below.

$$I_{out}'' = \frac{a_6s^6 - a_5s^5 + a_4s^4 - a_3s^3 + a_2s^2 - a_1s + a_0}{a_6s^6 + a_5s^5 + a_4s^4 + a_3s^3 + a_2s^2 + a_1s + a_0} I_{in} \quad (3-15)$$

3.4 Analytical Synthesis Method II: DIMOC Method

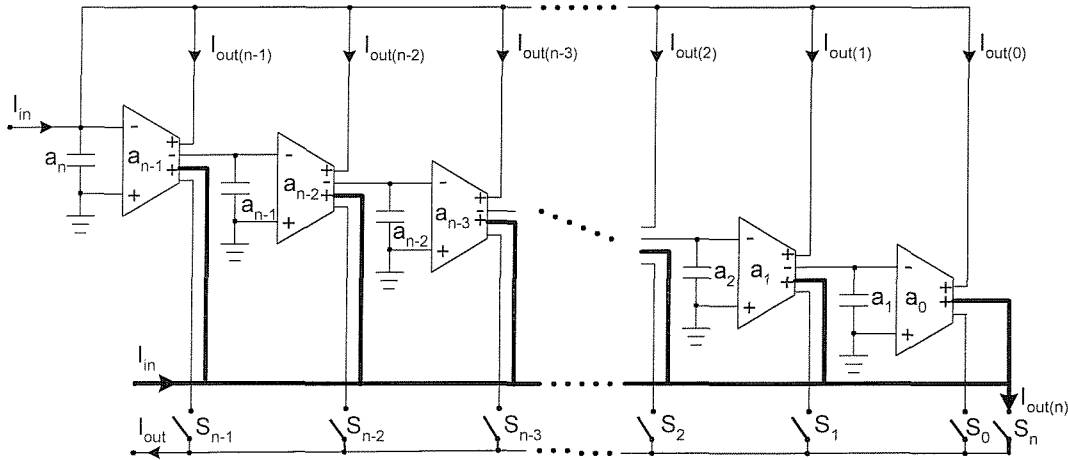


Fig. 3-10 Nth-order OTA-C generic filter structure of the DIMOC synthesis method

The second synthesis method is based on an nth-order generic filter structure with double input and multiple output currents (DIMOC). The nth-order generic filter

structure of the DIMOC synthesis method is shown in Fig. 3-10. The filter has one input, I_{in} , applied to two different points in the filter, and multiple output currents: $I_{out(0)}$, $I_{out(1)}$, $I_{out(2)}$, \dots , $I_{out(n-1)}$, and $I_{out(n)}$. The output currents are controlled by the switches S_n, S_{n-1}, \dots, S_1 and S_0 and their setting (closed or open) determine the filter function as shown later. Note I_{out} in Fig. 3-10 is the output current of the chosen filter. The transfer function of the filter structure in Fig. 3-10 is given by:

$$I_{out(n)} + I_{out(n-1)} + \dots + I_{out(0)} = \frac{a_n I_{in} s^n + a_{n-1} I_{in} s^{n-1} + a_{n-2} I_{in} s^{n-2} + \dots + a_1 I_{in} s + a_0 I_{in}}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_1 s + a_0}$$

where the a_i are positive real numbers. This can be re-written as:

$$\sum_{i=0}^{i=n} I_{out(i)} = \sum_{i=0}^{i=n} \frac{a_i I_{in} s^i}{\Delta},$$

$$\text{or } I_{out(i)} = \frac{a_i I_{in} s^i}{\Delta} \text{ for } i = 0, 1, 2, \dots, n-1, n,$$

$$\text{where } \Delta = a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0. \quad (3-16)$$

Based on the characteristic of easy summation for current signals, the single output current signal I_{out} given by Eq. (3-1) is divided into $n+1$ output current signals, $I_{out(0)}$, $I_{out(1)}$, $I_{out(2)}$, \dots , $I_{out(n-1)}$, and $I_{out(n)}$, shown in the above equation. The division makes the transfer function given by Eq. (3-1) be decomposed into $n+1$ less complex transfer functions shown in Eq. (3-16). The less complicated the transfer function is the easier the realization.

The proposed new analytical synthesis method has six steps, they are explained as follows.

Step 1: Derive one of the transfer functions shown in Eq. (3-16).

Equating the first term of both sides of Eq. (3-16) gives

$$I_{out(0)} = \frac{a_0 I_{in}}{\Delta}, \text{ i.e.,}$$

$$\text{Cross multiply, } I_{out(0)}(a_n s^n + a_{n-1} s^{n-1} + \dots + a_1 s + a_0) = a_0 I_{in}$$

And re-arrange,

$$\begin{aligned} I_{out(0)} a_n s^n &= \left[I_{in} - I_{out(0)} - I_{out(0)} \frac{a_{n-1} s^{n-1}}{a_0} - I_{out(0)} \frac{a_{n-2} s^{n-2}}{a_0} + \dots + I_{out(0)} \frac{a_1 s}{a_0} \right] a_0 \\ &= \left[I_{in} - I_{out(0)} - I_{out(0)} \sum_{i=1}^{i=n-1} \frac{a_i s^i}{a_0} \right] a_0 \end{aligned} \quad (3-17)$$

Step 2: Substitute the relations between each $I_{out(i)}$ and $I_{out(0)}$ into the derived equation given by Step 1.

$$\text{From Eq. (3-16), we have } I_{out(0)} = \frac{a_0 I_{in}}{\Delta} \quad (3-18a)$$

$$I_{out(1)} = \frac{a_1 I_{in} s}{\Delta} \quad (3-18b)$$

$$I_{out(2)} = \frac{a_2 I_{in} s^2}{\Delta} \quad (3-18c)$$

$$I_{out(3)} = \frac{a_3 I_{in} s^3}{\Delta} \quad (3-18d)$$

$$\text{Dividing Eq. (3-18b) by Eq. (3-18a) gives } I_{out(1)} = I_{out(0)} \frac{a_1 s}{a_0}$$

$$\text{Similarly dividing Eq. (3-18c) by Eq. (3-18a) gives } I_{out(2)} = I_{out(0)} \frac{a_2 s^2}{a_0}$$

$$\text{or in general, } I_{out(i)} = I_{out(0)} \frac{a_i s^i}{a_0} \text{ for } i = 1, 2, \dots, n-1. \quad (3-18e)$$

$$\text{Substituting Eq. (3-18e) into Eq. (3-17) gives } I_{out(0)} a_n s^n = \left[I_{in} - \sum_{i=0}^{i=n-1} I_{out(i)} \right] a_0 \quad (3-18f)$$

From Eq. (3-18e), we have $I_{out(n-1)} = I_{out(0)} \frac{a_{n-1} s^{n-1}}{a_0}$

$$\text{or } I_{out(0)} = I_{out(n-1)} \frac{a_0}{a_{n-1} s^{n-1}} \quad (3-18g)$$

Substitute Eq. (3-18g) into Eq. (3-18f) gives:

$$I_{out(n-1)} = \left[I_{in} - \sum_{i=0}^{i=n-1} I_{out(i)} \right] \frac{a_{n-1}}{a_n s} \quad (3-19)$$

Step 3: Synthesize the realizable simple equation, with a single integrator, given by step 2.

Eq. (3-19) is realised using the first integrator from the left in Fig. 3-10 and the output currents of all of the OTAs in the general filter structure.

Now we need to work out the connections between the remaining integrators of the general filter and their output currents.

Step 4: Find out the relationships, each of which is with a single integrator, between every two $I_{out(i)}$.

To do this, we divide Eq. (3-18a) by Eq. (3-18b) gives

$$I_{out(0)} = I_{out(1)} \frac{a_0}{a_1 s} \quad (3-20a)$$

Eq.(3-18a) is realised by the first integrator from the right in Fig. 3-10. Similarly, dividing Eq. (3-18b) by Eq.(3-18c) gives

$$I_{out(1)} = I_{out(2)} \frac{a_1}{a_2 s} \quad (3-20b)$$

or, in general

$$I_{out(i)} = I_{out(i+1)} \frac{a_i}{a_{i+1}S} \quad \text{for } i = 0, 1, 2, \dots, n-2. \quad (3-20c)$$

Step 5: Synthesize the realizable simple equations given by step 4.

Eq. (3-20c) are realised by those integrators from the second to the last in Fig.3-10.

Step 6: Having developed the general filter structure of the DIMOC synthesis method, now we show how different filter functions are obtained.

(i) Low-pass: If a low-pass filter is required, then the switch S_0 is closed, whilst all the other switches of the general filter structure (Fig. 3-10) are open. The filter output is

$$I_{out(0)} = I_{out}.$$

(ii) Band-pass: If a band-pass filter is required, then the switch controlling the output current $I_{out(n/2)}$ is closed, whilst all the other switches of the general filter structure (Fig. 3-10) are open if the filter order n , is even. Or the switch controlling either of the two output currents $I_{out[(n/2)-(1/2)]}$ and $I_{out[(n/2)+(1/2)]}$ is closed if n is odd.

(iii) High-pass: A high-pass filter is obtained as follows: From Eq. (3-16), we have

$$I_{out(n)} = \frac{a_n I_{in} S^n}{\Delta} \quad (3-21a)$$

$$\text{Then, } \frac{I_{out(n)}}{I_{in}} = \frac{a_n S^n}{\Delta} = 1 - \sum_{i=0}^{i=n-1} \frac{a_i S^i}{\Delta} = 1 - \frac{\sum_{i=0}^{i=n-1} I_{out(i)}}{I_{in}} \quad (3-21b)$$

$$\text{or, } I_{out(n)} = I_{in} - \sum_{i=0}^{i=n-1} I_{out(i)} \quad (3-21c)$$

Eq.(3-21c) is implemented as marked bold in the filter structure of Fig. 3-10. The filter output is $I_{out(n)}$, and only switch S_n is closed.

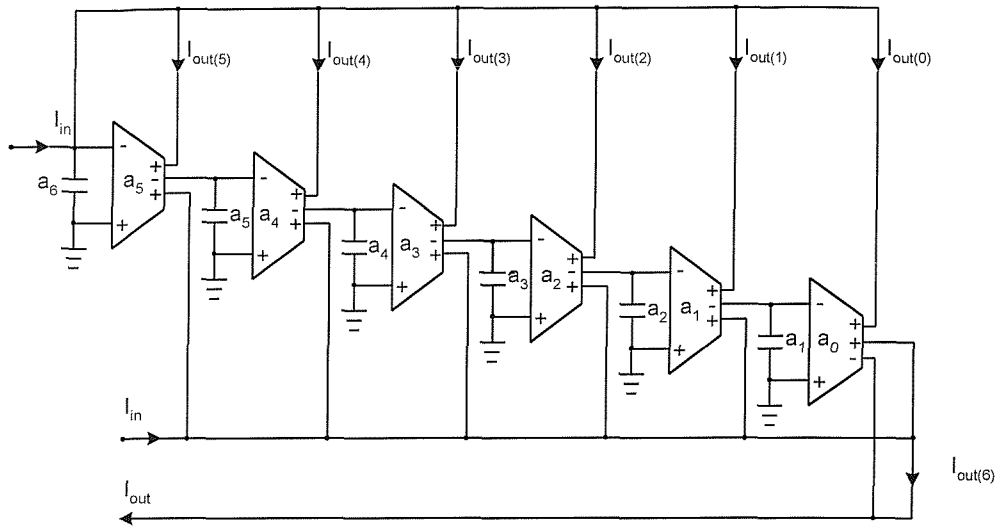


Fig. 3-11 6th-order band-reject OTA-C filter obtained using the DIMOC synthesis method

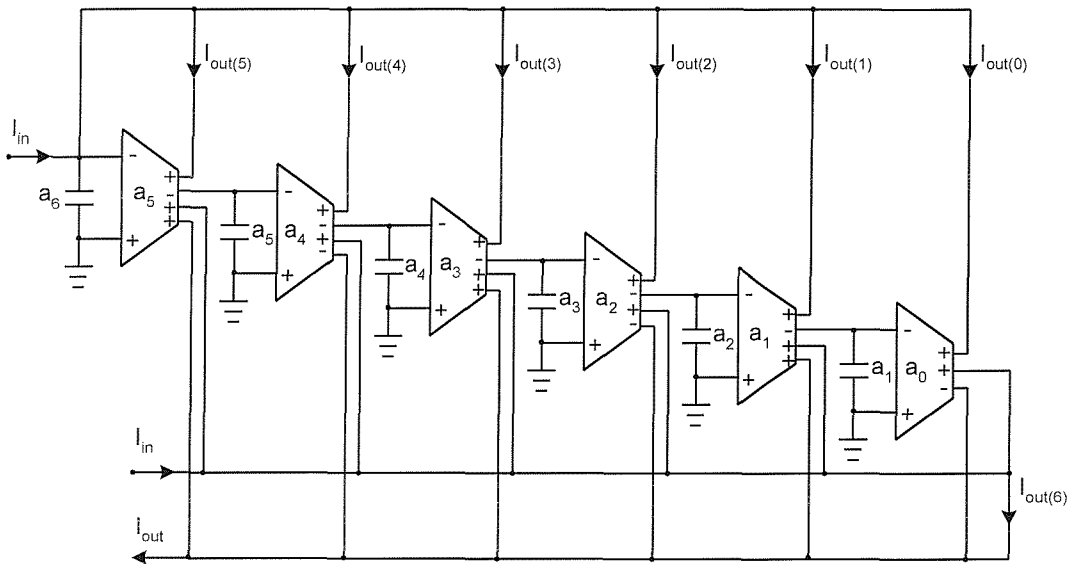


Fig.3-12 6th-order all-pass OTA-C filter obtained using the DIMOC synthesis method

(iv) Band-reject: If a band-reject filter is required, then only two filter switches, S_o and S_n , controlling the output currents $I_{out(0)}$ and $I_{out(n)}$ need to be closed, whilst all the other switches of the general filter structure (Fig. 3-10) are open. The filter output in this case is the summation of both the available filter currents. For example, Fig. 3-11 shows a 6th-order band-reject filter with the transfer function:

$$\frac{I_{out}}{I_{in}} = \frac{a_6 s^6 + 0s^5 + 0s^4 + 0s^3 + 0s^2 + 0s + a_0}{a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (3-22)$$

(v) All-pass: If an all-pass filter is required, then the summation, $\sum_{i=0}^{i=n} (-1)^i I_{out(i)}$, will produce an all-pass response. Fig. 3-12 shows a 6th-order all-pass filter with the transfer function:

$$\frac{I_{out}}{I_{in}} = \frac{a_6 s^6 - a_5 s^5 + a_4 s^4 - a_3 s^3 + a_2 s^2 - a_1 s + a_0}{a_6 s^6 + a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0} \quad (3-23)$$

3.5 Sensitivity Analysis

This section provides sensitivity analysis for the analytical synthesis methods I and II outlined in Sections 3.3 and 3.4.

If we replace the transconductances $a_0, a_1, a_2, \dots, a_{n-2}$, and a_{n-1} with $g_1, g_2, g_3, \dots, g_{n-1}$, and g_n and the capacitors $a_1, a_2, a_3, \dots, a_{n-1}$, and a_n with $C_1, C_2, C_3, \dots, C_{n-1}$, and C_n in Fig. 3-6. Then the transfer function of the circuit in Fig. 3-6 is shown as follows.

$$\begin{aligned} & I_{out}'' \\ &= \frac{\left[I_n s^n + (I_n - I_{n-1}) s^{n-1} b_n + (I_n - I_{n-2}) s^{n-2} b_n b_{n-1} + \dots \right. \\ & \quad \left. \dots + (I_n - I_1) s b_n b_{n-1} b_{n-2} \dots b_3 b_2 + (I_n - I_0) b_n b_{n-1} b_{n-2} \dots b_3 b_2 b_1 \right]}{s^n + s^{n-1} b_n + s^{n-2} b_n b_{n-1} + \dots + s b_n b_{n-1} b_{n-2} \dots b_3 b_2 + b_n b_{n-1} b_{n-2} \dots b_3 b_2 b_1} \end{aligned}$$

$$= \frac{I_n s^n + \sum_{i=0}^{n-1} \left[(I_n - I_{n-i-1}) s^{n-i-1} \prod_{j=n-i}^{j=n} b_j \right]}{s^n + \sum_{i=0}^{n-1} \left[s^{n-i-1} \prod_{j=n-i}^{j=n} b_j \right]} \text{ where } b_j = \frac{g_j}{C_j} \text{ for } j = 1, 2, 3, \dots, n-1, n. \quad (3-24)$$

On the other hand, if we replace the transconductances $a_0, a_1, a_2, \dots, a_{n-2}$, and a_{n-1} with $g_1, g_2, g_3, \dots, g_{n-1}$, and g_n and the capacitors $a_1, a_2, a_3, \dots, a_{n-1}$, and a_n with $C_1, C_2, C_3, \dots, C_{n-1}$, and C_n in Fig. 3-10. Then the transfer functions of the output circuits in Fig. 3-10 is shown as follows.

$$I_{out(n)} = \frac{s^n I_{in}}{s^n + s^{n-1} b_n + s^{n-2} b_n b_{n-1} + \dots + s b_n b_{n-1} b_{n-2} \dots b_3 b_2 + b_n b_{n-1} b_{n-2} \dots b_3 b_2 b_1}$$

$$= \frac{s^n I_{in}}{s^n + \sum_{i=0}^{n-1} \left[s^i \prod_{j=i+1}^n b_j \right]}$$

$$\text{where } b_j = \frac{g_j}{C_j} \text{ for } j = 1, 2, 3, \dots, n-1, n, \quad (3-25)$$

and

$$I_{out(i)} = \frac{s^i b_n b_{n-1} b_{n-2} \dots b_{i+3} b_{i+2} b_{i+1} I_{in}}{s^n + s^{n-1} b_n + s^{n-2} b_n b_{n-1} + \dots + s b_n b_{n-1} b_{n-2} \dots b_3 b_2 + b_n b_{n-1} b_{n-2} \dots b_3 b_2 b_1}$$

$$= \frac{\left[s^i \prod_{j=i+1}^n b_j \right] I_{in}}{s^n + \sum_{i=0}^{n-1} \left[s^i \prod_{j=i+1}^n b_j \right]}$$

$$\text{where } b_j = \frac{g_j}{C_j} \text{ for } j = 1, 2, 3, \dots, n-1, n, \text{ and } i = 0, 1, 2, 3, \dots, n-2, n-1. \quad (3-26)$$

The coefficient sensitivities, $S_x^Y = (x/Y)(\partial Y/\partial x)$, are defined as the values of transfer function coefficients with respect to circuit elements. For the general pole (resp. zero) realisation of Eqs. (3-24) to (3-25), the denominator (resp. numerator) coefficient sensitivities to g_j are 0 and 1 and to C_j are 0, and -1, all of which are small. Appendix 5 gives a demonstration of sensitivity performance for the OTA-C biquad filter by using MISOC method.

3.6 Comparison with Previous Work

Two comparison parameters, component count and component spread, are considered in this section.

Component Count

A number of methods for designing current mode OTA-C filters have been reported. In this section, a comparison in terms components count (passive and active) between filters generated using the new synthesis methods and five recently proposed methods. In [17] a method for the design of high order OTA based filters using coupled biquads was proposed. It was shown that a fifth-order all-pole low-pass filter has seven OTAs and seven capacitors, shown in Fig.3-13. Using the MISOC (Section 3.3) and DIMOC (Section 3.4) synthesis methods, a fifth-order low-pass filter has five OTAs and five capacitors.

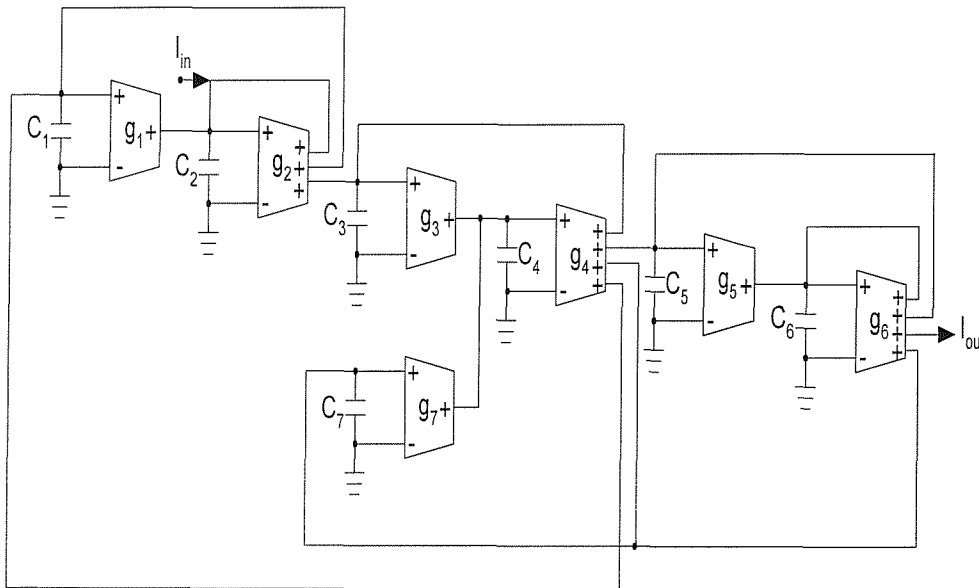


Fig. 3-13 5th-order all-pole low-pass ladder filter [17]

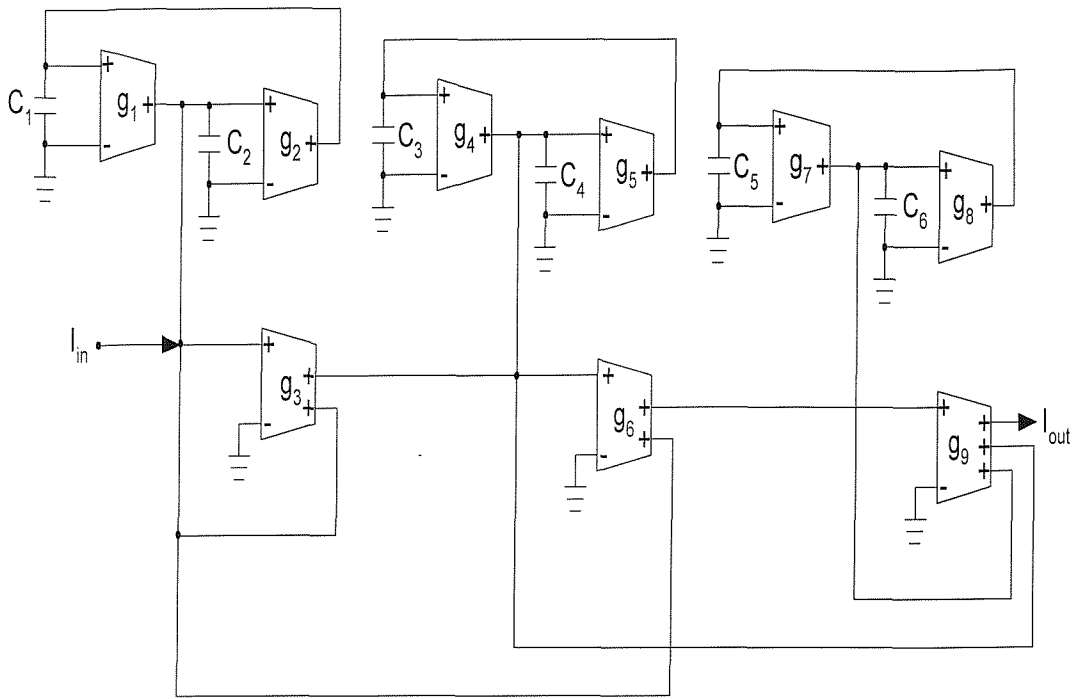


Fig. 3-14 6th-order all-pole band-pass ladder filter [17]

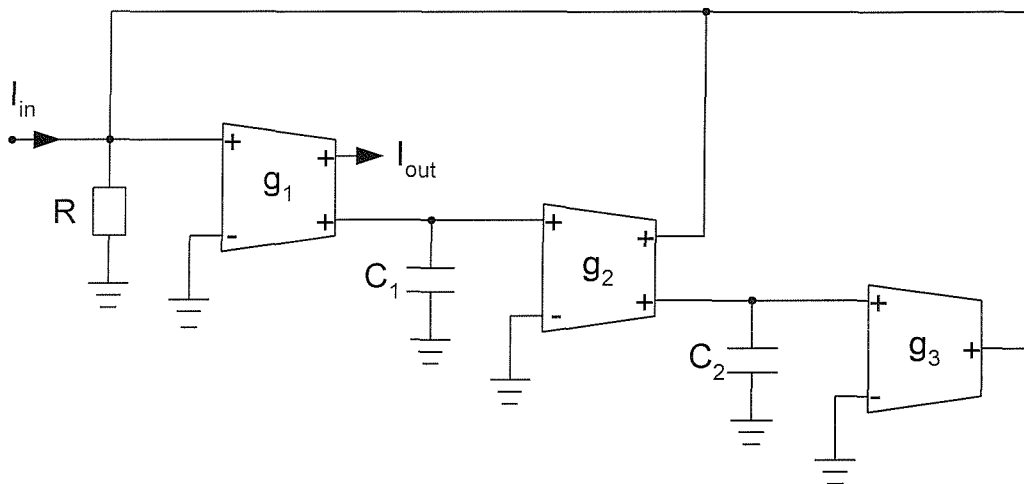


Fig. 3-15 (a) 2nd-order high-pass filter [15]

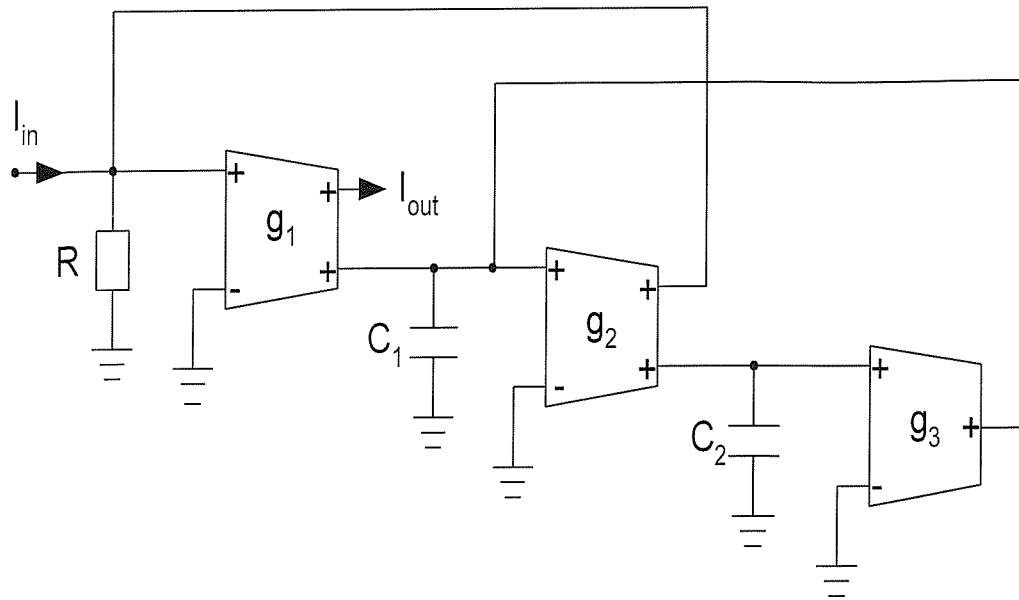


Fig. 3-15 (b) 2nd-order notch filter [15]

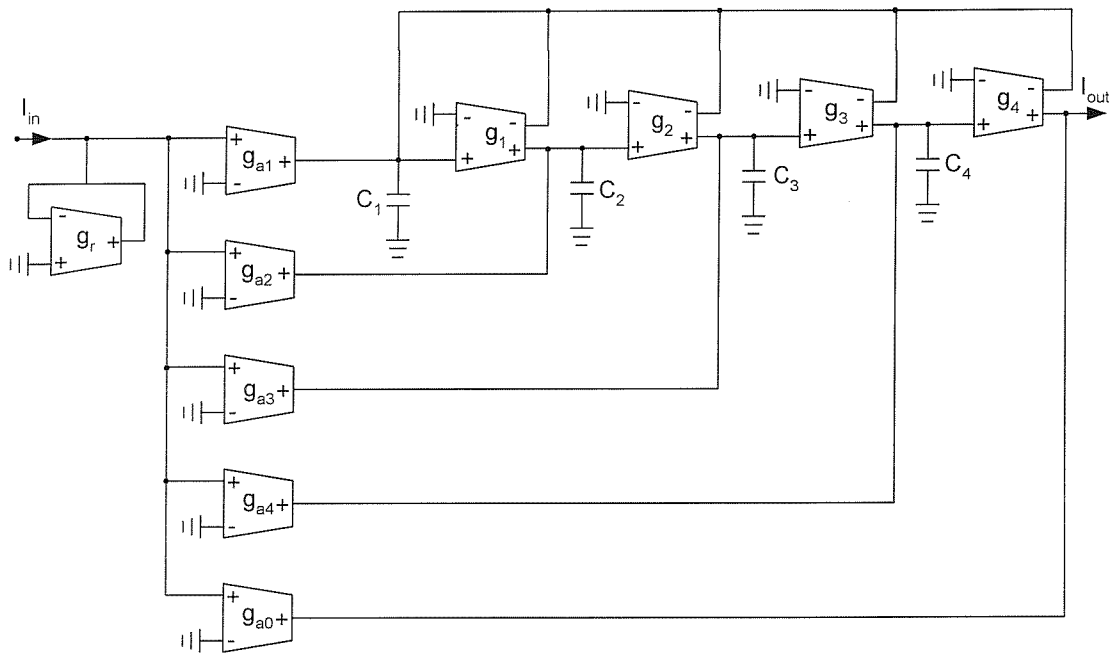


Fig. 3-16 4th-order high-pass filter [14]

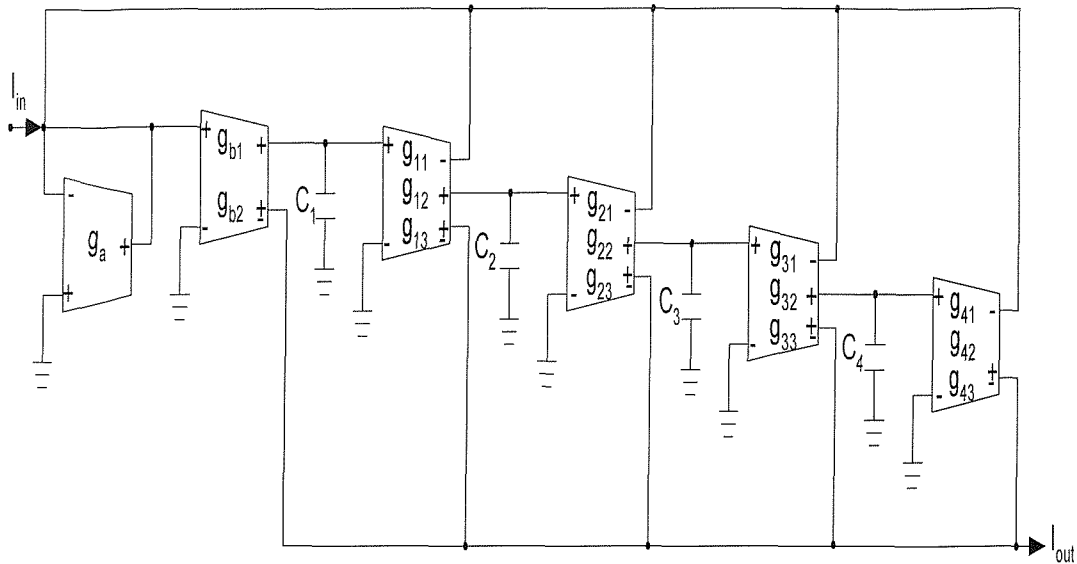


Fig. 3-17 4th-order high-pass filter [12]

Also, it was shown in [17] that a 6th-order band-pass filter has nine OTAs, and six capacitors, shown in Fig. 3-14, compared with six OTAs and six capacitors when the MISOC and DIMOC methods are used. Consider the method in [15], it was shown that a second-order notch filter or second-order high-pass filter has three OTAs, two capacitors and one resistor, shown in Figs. 3-15 (a) and 15 (b), compared with two OTAs and two capacitors when the proposed synthesis methods are used to design the same filters. In [11], a method for designing current mode OTA-C filters based on simulation of LC ladder was reported. Although, the method produces filters that have n , single-ended OTAs and n , grounded capacitors, they also require current amplifiers and buffers, increasing the complexity of the filter circuit. In [12], a general class of current-mode high-order OTA-C filters employing a current-mode integrator and a proportional block as basic building units was proposed. It was shown that six OTAs and four capacitors are required to realise a fourth-order filter, shown in Fig. 3-17. However, only four OTAs and four capacitors are required to realise the same filter by using the above two new synthesis methods. In [14], the current-mode OTA-C realization for arbitrary filters was proposed. It was shown that ten OTAs and four capacitors are required to realise a fourth-order high-pass filter, shown in Fig. 3-16. However, only four OTAs and four capacitors are required to realise the same filter by using the MISOC and DIMOC methods.

In summary, the proposed methods, shown in sections 3.3 and 3.4, generally produce filters that have fewer components (passive and active) than any of the other reported design methods for current mode OTA filters, this includes cascade [15], coupled biquad [17], LC ladder simulation [11], integrator and proportional block [12], and arbitrary filter structure [14]. This is because an optimal n th-order OTA-C filter has n , single-ended OTAs, and n , grounded capacitors, and such filters can be produced using the two proposed synthesis methods. Before proceeding, a further comment is worth making. When realizing high-order filters, simulation of LC ladder results in circuits with good performance. The reason for this fact is the excellent pass-band sensitivity of doubly terminated LC ladder filters. However, pass-band sensitivity is not always the deciding factor in choosing a filter design method [82]. Other properties may become important. For example, ease of design, regular structure leading to simplified layout, and the ability to change the filter order and function without the need for complete re-design. The proposed synthesis methods not only produce high-order filters that have less components but also exhibit some attractive VLSI features, employment of grounded capacitors and single-input OTAs, when compared with the LC simulation method.

Component Spread

Another parameter which needs to be compared when considering different synthesis methods is the span (or spread) of filter component values which may be large for high-order filters. To give insight into what the component spans of the new filter structures using the new MISOC and DIMOC synthesis methods are, as an example, we have compared the component spread of fourth-order Butterworth high-pass filters, with the numerator s^4 and the denominator $s^4 + 2.6131259s^3 + 3.4142136s^2 + 2.6131259s + 1$, realised using the circuits shown in Fig. 3-17 [12] and 3-16 [14], respectively, and the new OTA-C filters shown in Figs. 3-18 and 3-20 using the new MISOC and DIMOC synthesis methods, respectively. The transfer functions of the fourth-order high-pass filters shown in Figs 3-18(or 3-20), 3-17, and 3-16, are presented in Eqs. (3-27), (3-28), and (3-29), respectively.

$$\frac{I_{out}}{I_{in}} = \frac{s^4 C_1 C_2 C_3 C_4}{s^4 C_1 C_2 C_3 C_4 + s^3 C_1 C_2 C_3 g_4 + s^2 C_1 C_2 g_3 g_4 + s C_1 g_2 g_3 g_4 + g_1 g_2 g_3 g_4} \quad (3-27)$$

$$\frac{I_{out}}{I_{in}} = \frac{s^4 C_4 C_3 C_2 C_1 g_{b2}}{\left(s^4 C_4 C_3 C_2 C_1 g_a + s^3 C_4 C_3 C_2 g_{11} g_{b1} + s^2 C_4 C_3 g_{21} g_{b1} g_{12} + \right. \\ \left. s C_4 g_{31} g_{b1} g_{12} g_{22} + g_4 g_{b1} g_{12} g_{22} g_{32} \right)} \quad (3-28)$$

$$\frac{I_{out}}{I_{in}} = \frac{\left[g_{a0} \left(s^4 C_4 C_3 C_2 C_1 + s^3 C_4 C_3 C_2 g_1 + s^2 C_4 C_3 g_1 g_2 + s C_4 g_1 g_2 g_3 + g_1 g_2 g_3 g_4 \right) + \right. \\ \left. g_{a1} \left(g_1 g_2 g_3 g_4 \right) + g_{a2} \left(s C_1 g_2 g_3 g_4 + g_1 g_2 g_3 g_4 \right) + g_{a3} \left(\begin{array}{l} s^2 C_2 C_1 g_3 g_4 + s C_2 g_1 g_3 g_4 + \\ g_1 g_2 g_3 g_4 \end{array} \right) \right] \\ \left. + g_{a4} \left(s^3 C_3 C_2 C_1 g_4 + s^2 C_3 C_2 g_1 g_4 + s C_3 g_1 g_2 g_4 + g_1 g_2 g_3 g_4 \right) \right] \\ \left(s^4 C_4 C_3 C_2 C_1 + s^3 C_4 C_3 C_2 g_1 + s^2 C_4 C_3 g_1 g_2 + s C_4 g_1 g_2 g_3 + g_1 g_2 g_3 g_4 \right)} \quad (3-29)$$

Assuming equal transconductance design, the former two transfer functions have the same capacitance spread from 0.383 (C_{min}) to 2.613 (C_{max}). The third transfer function needs extra transconductance spread from 0.353 (g_{min}) to 1 (g_{max}) in addition to the same capacitance spread from 0.383 (C_{min}) to 2.613 (C_{max}). Similarly assuming equal capacitance design, the transconductance spreads are (i) from 0.635 (g_{min}) to 1.617 (g_{max}) (the smallest) for the circuit in [12], (ii) from 0.383 to 2.613 (the middle) for the proposed circuit structures (Figs.3-18 and 3-20), and (iii) from 0.383 to 11.657 (the largest) for the circuit in [14].

In summary, Fig. 3-17 has the lowest component spread, Fig. 3-16 has the largest component spread, whilst Fig. 3-18 and 3-20 have better component spread than that of Fig. 3-16 but worse component spread than that of Fig. 3-17.

Cascadability

For a current-mode circuit, low input impedance and high output impedance lead to the attractive feature: cascadability at the input and output ports, respectively (referring to Appendix 2). Due to high input and output impedances of an OTA, both the two current-mode filter structures shown in Figs. 3-6 and 3-10 have rather high input

impedances and need the current buffer to do the connection with the previous stage. However, their very high output impedances achieve the advantage: cascadability at their output ports. If we do the comparison about the output impedance between the MISOC and DISOC methods, the output impedance of MISOC filter structure is higher than that of DISOC filter structure because the output terminals of DIMOC filter structure is more or no less, generally, in number than those of MISOC filter structure. For example, consider the fourth-order high-pass filters designed using the DIMOC and MISOC methods shown in Figs. 3-18 and 3-20, respectively. Suppose both the output impedances of an OTA and an input current signal to be the same Z_{out} . Then, the output impedances of Figs. 3-18 (MISOC) and 3-20 (DIMOC) are $Z_{out}/2$ and $Z_{out}/5$, respectively. Observing both recently reported work [12, 14], they are also with high input and output impedances, namely, both are cascadable at their output ports. We also note that the output impedances of the fourth-order high-pass filters shown in Figs. 3-17 [12] and 3-16 [14] are $Z_{out}/5$ and $Z_{out}/2$, respectively.

3.7 Simulation Results

Two filtering functions, high-pass and all-pass are chosen to do the simulations. The fourth-order OTA-C high-pass and all-pass filters using the new MISOC and DIMOC synthesis methods are shown in Figs. 3-18 to 3-21, respectively.

The simulations use H-Spice with UMC05 (0.5 μ m) level-49 process and the CMOS implementations described in Section 2.2. The component values are given by $g_1 = g_2 = g_3 = g_4 = 157\mu$ S ($I_{abc} = 60.73\mu$ A), $C_1 = 32.5$ pF, $C_2 = 16.25$ pF, $C_3 = 9.53$ pF, and $C_4 = 4.75$ pF. The fourth-order high-pass simulation results are shown in Figs. 3-22 and 3-23. As can be seen, there is a close agreement between theory and simulation, for example, their simulated lower 3dB frequencies are 1.93MHz (MISOC) and 1.90MHz (DIMOC), compared to 2.01MHz in the ideal case, and their peak values are 0.506dB (MISOC) and 0.748dB (DIMOC), compared to 0dB in the ideal case. The superimposed diagram of Figs. 3-22 and 3-23 is shown in Fig. 3-24 for better comparison. Note that the two simulation results are nearly the same.

The fourth order all-pass simulation results are shown in Figs. 3-25 and 3-26. As can be seen, there is a close agreement between theory and simulation, for example, their simulated centre frequencies (as phase shift equals 360°) are 2.0MHz (MISOC) and 2.0MHz (DIMOC), compared to 2.01MHz in the ideal case, and their peak values are 1.108dB (MISOC) and 1.889dB (DIMOC), compared to 0dB in the ideal case. The superposed diagram of Figs. 3-25 and 3-26 is shown in Fig. 3-27 for better comparison. Note that the two simulation results are nearly the same. Other filters with different orders and responses have also been synthesized using the presented two synthesis methods and found to perform as theory prediction. Moreover, noise simulation results of Fig. 3-18 and 3-20 are shown in Figs. 3-28 and 3-29 in which the maximum noise magnitudes are 40.648pA and 40.596pA, respectively, compared to 1mA output current.

To examine the voltages and currents in the internal nodes and branches of the filter structure, a third-order OTA-C high-pass and low-pass filter shown in Fig. 3-30 has been simulated. The given component values are $g_0 = 73.5\mu\text{S}$, $g_1 = 147\mu\text{S}$, $g_2 = 294\mu\text{S}$, and $C_0 = C_1 = C_2 = 23.4\text{pF}$. All the curves have limited ranges, for example, the curves shown in Figs. 3-31 (a) and (b), which confirm the feasibility of the new filter structure.

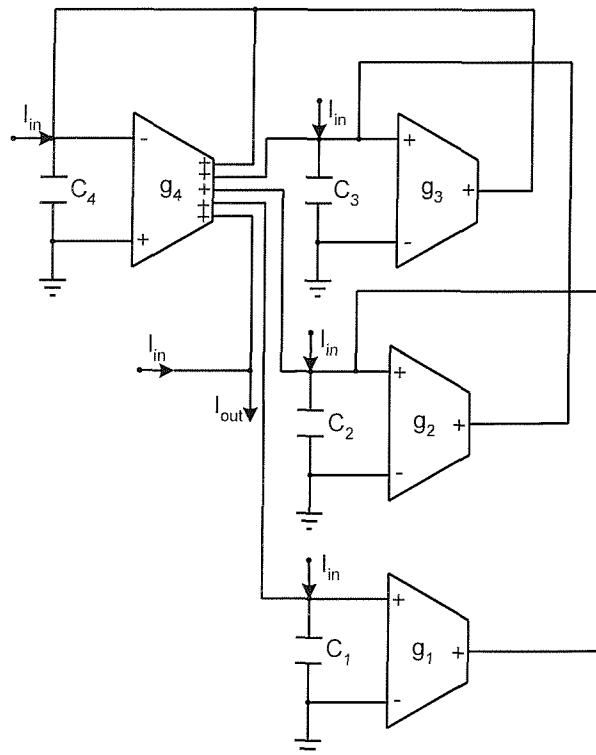


Fig. 3-18 Fourth-order OTA-C high-pass filter using MISOC synthesis method

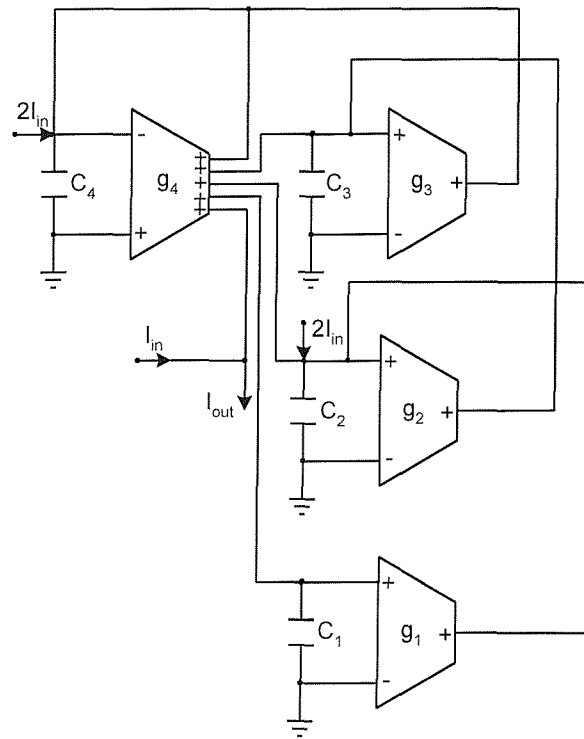


Fig. 3-19 Fourth-order OTA-C all-pass filter using MISOC synthesis method

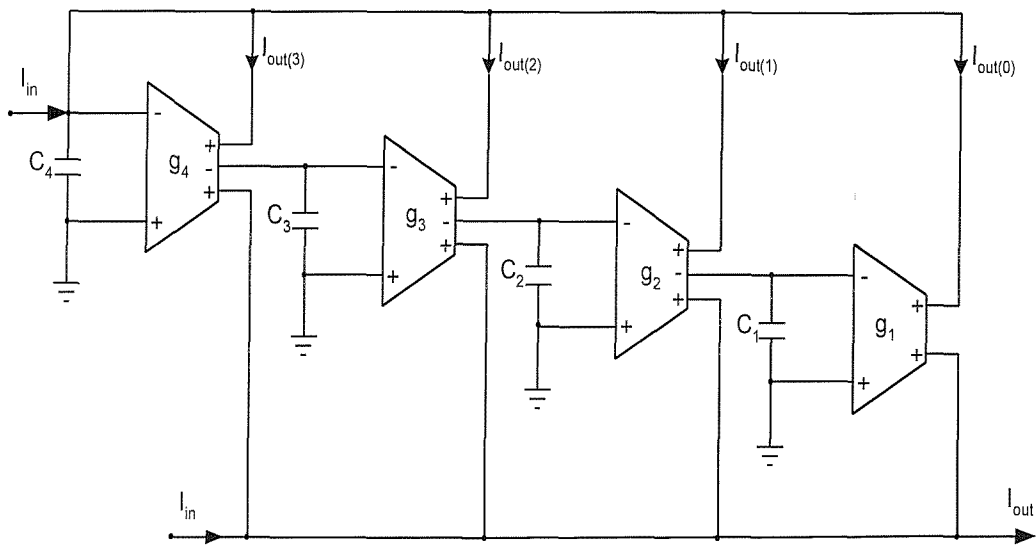


Fig. 3-20 Fourth-order OTA-C high-pass filter using DIMOC synthesis method

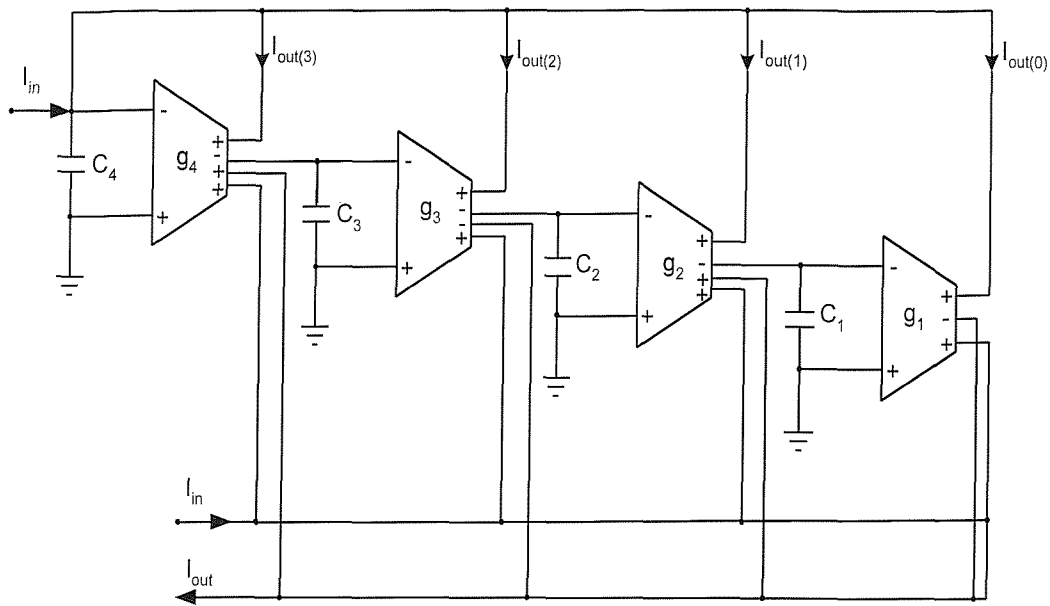


Fig. 3-21 Fourth-order OTA-C all-pass filter using DIMOC synthesis method

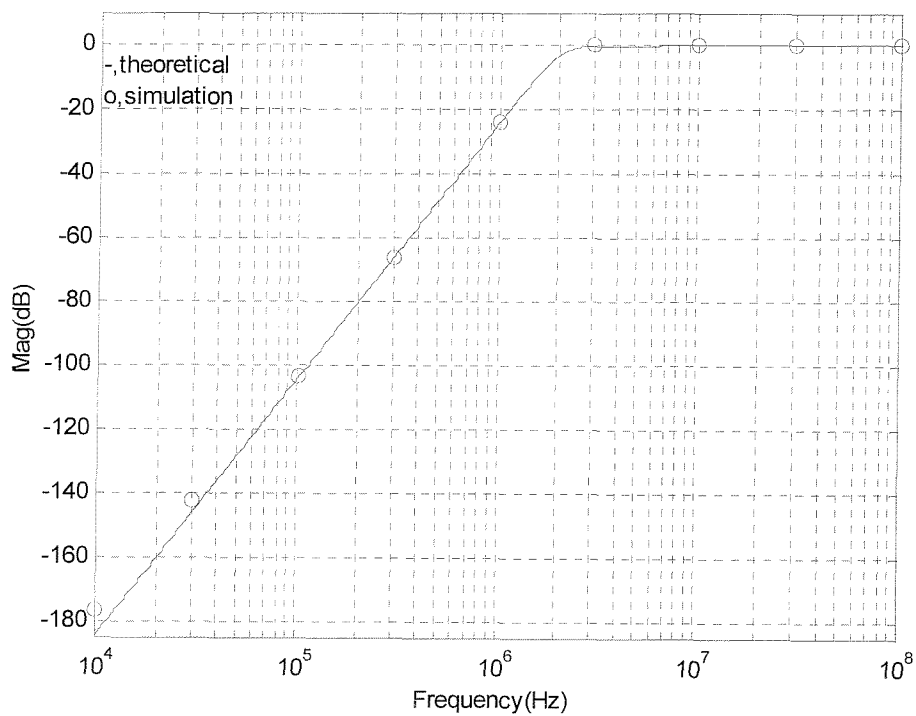


Fig. 3-22 Amplitude-frequency response of Fig. 3-18

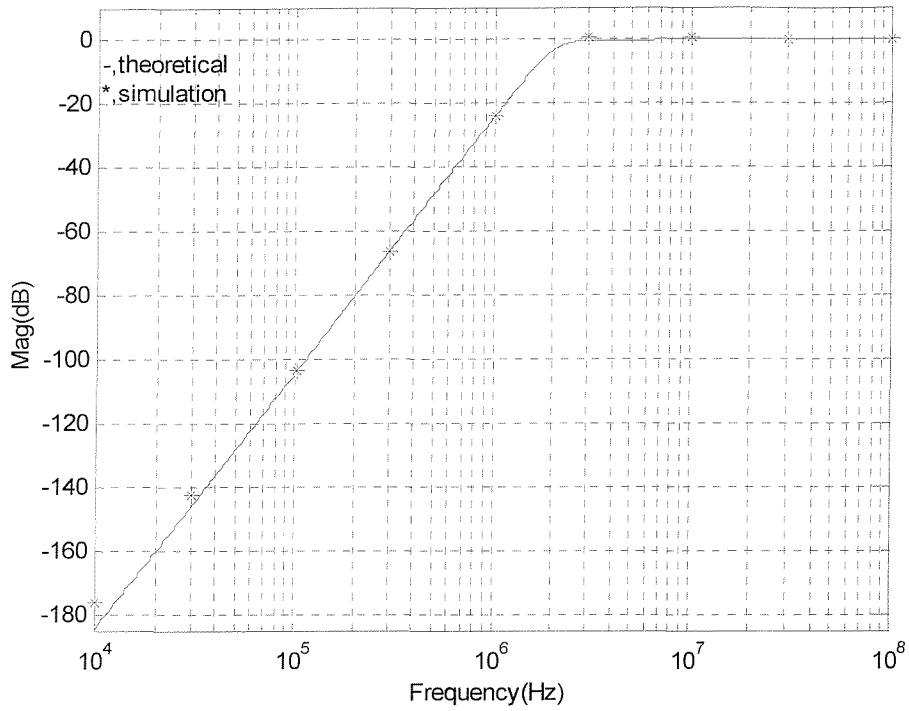


Fig. 3-23 Amplitude-frequency response of Fig. 3-20

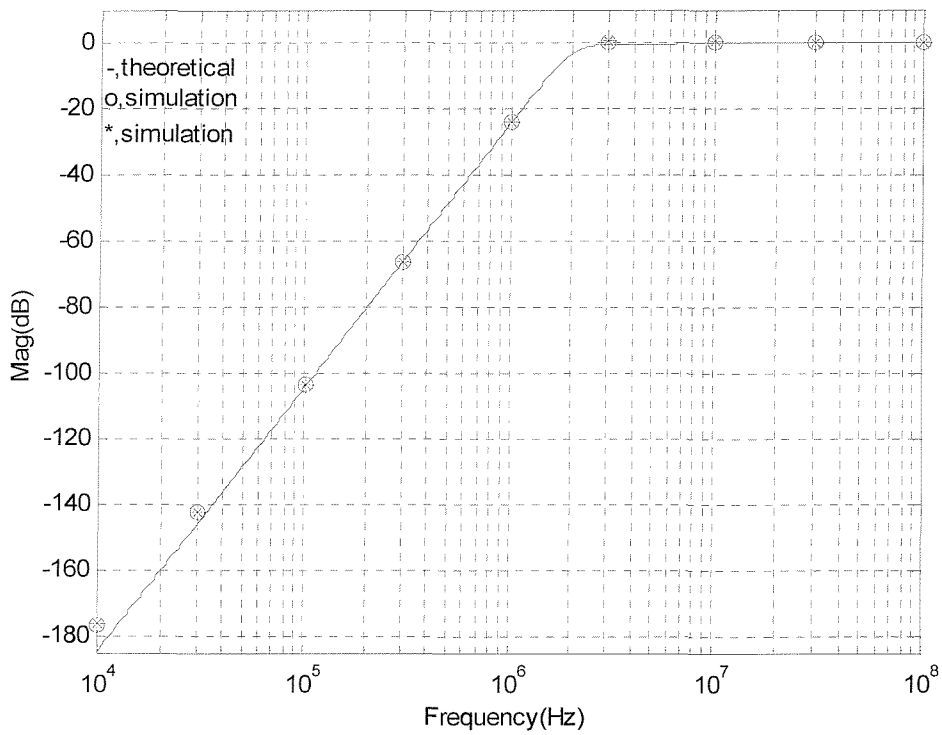


Fig. 3-24 Superposed diagram of Figs. 3-22 and 3-23

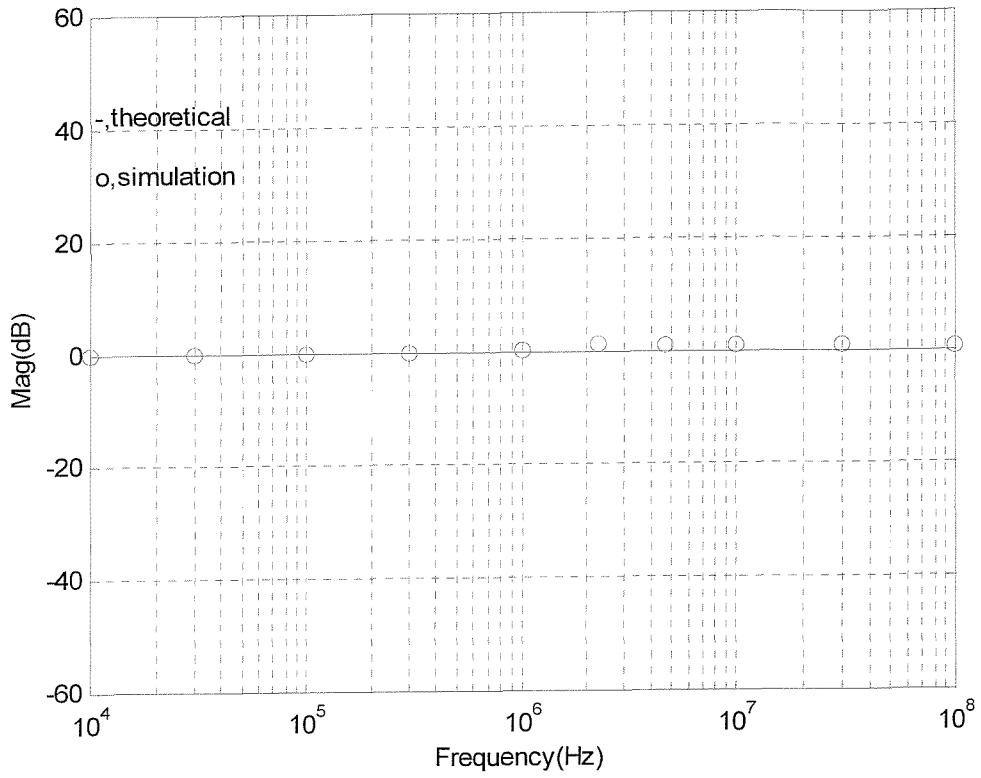


Fig. 3-25 (a) Amplitude-frequency response of Fig. 3-19

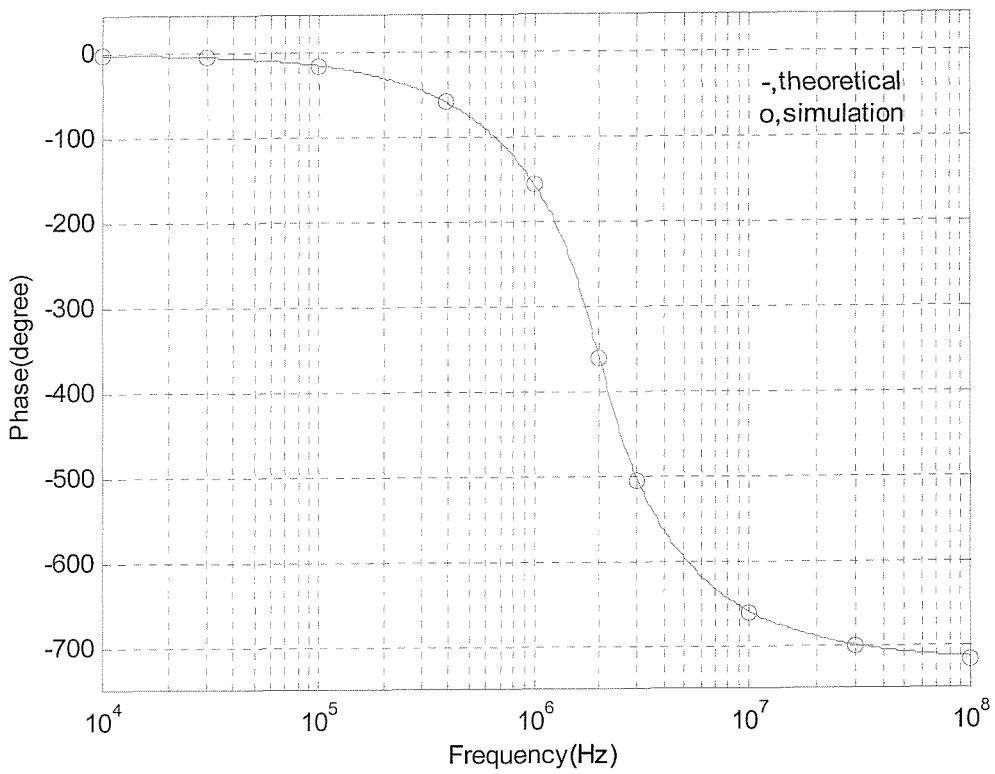


Fig. 3-25 (b) Phase-frequency response of Fig. 3-19

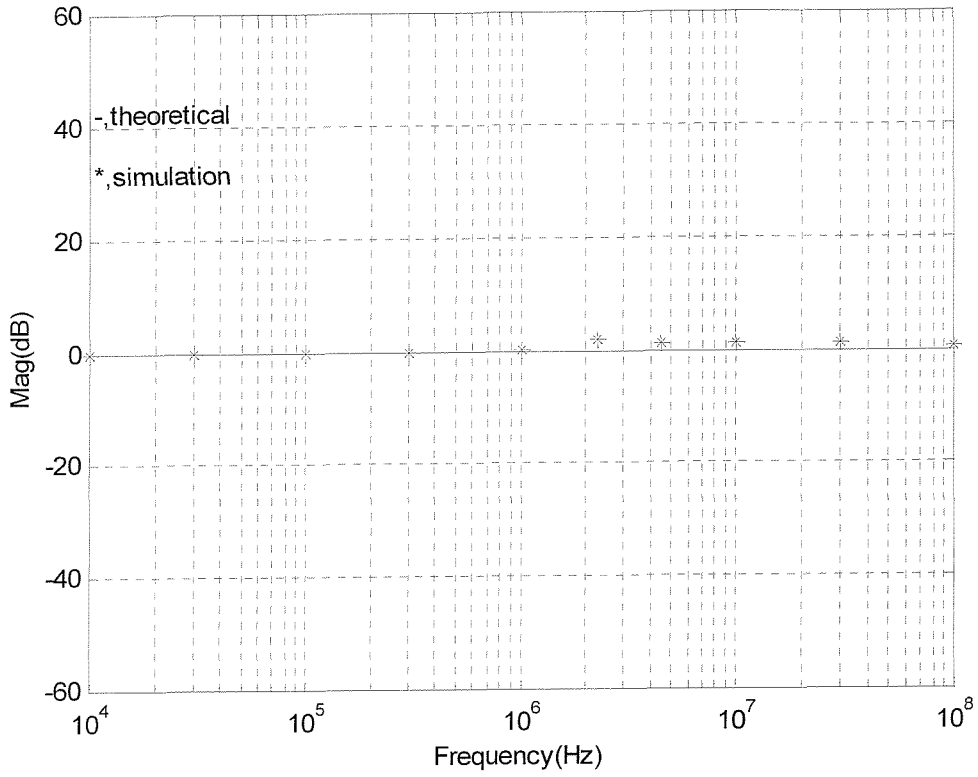


Fig. 3-26 (a) Amplitude-frequency response of Fig. 3-21

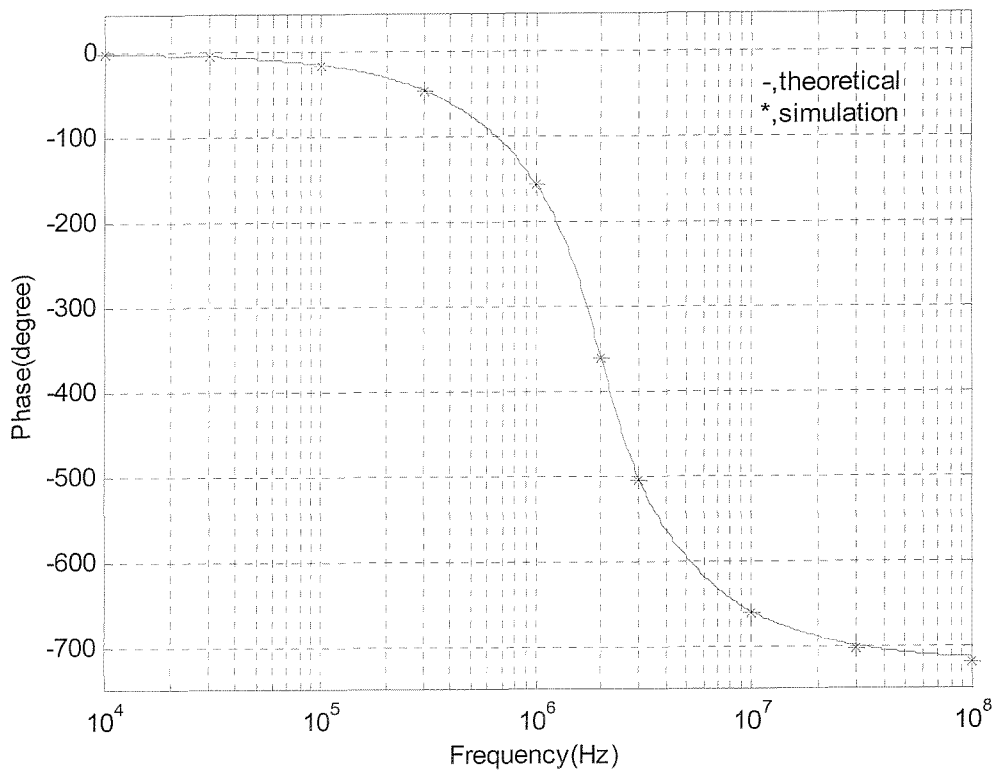


Fig. 3-26 (b) Phase-frequency response of Fig. 3-21

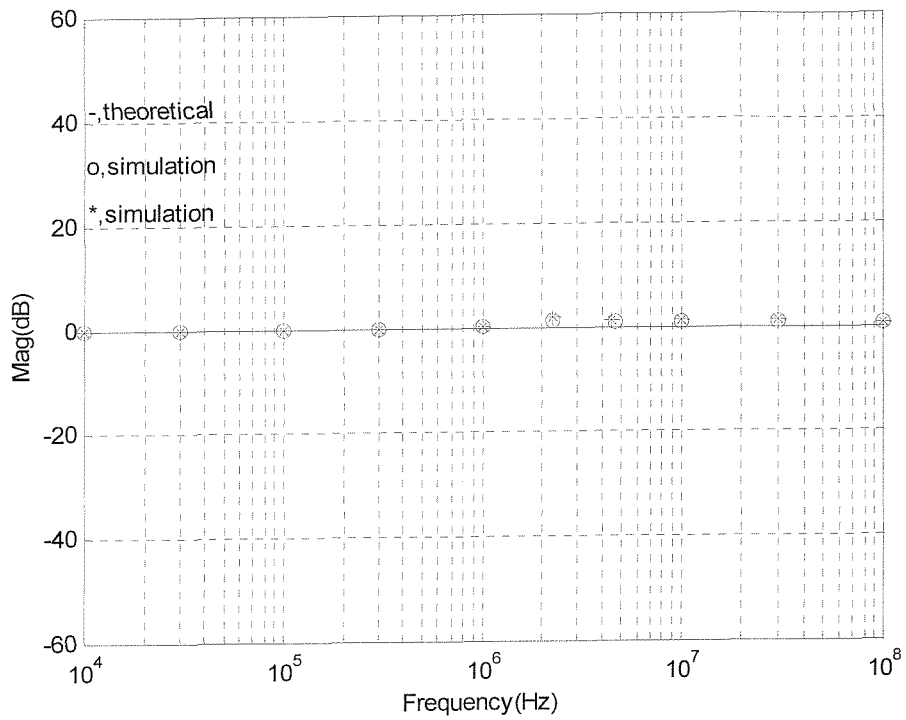


Fig. 3-27 (a) Superposed diagram of Figs. 3-25 (a) and 3-26 (a)

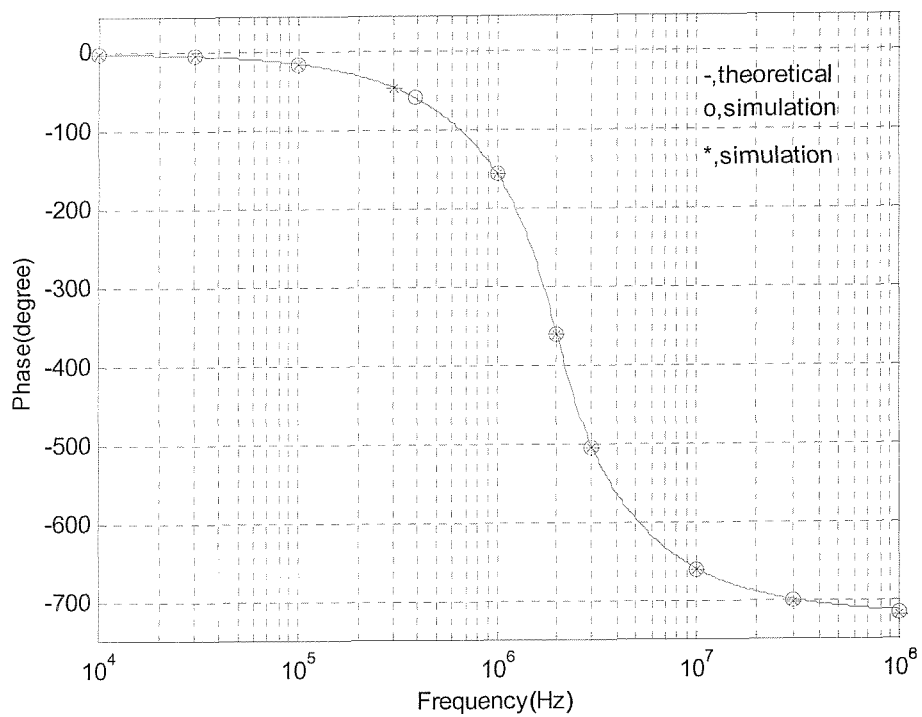


Fig. 3-27 (b) Superposed diagram of Figs. 3-25 (b) and 3-26 (b)

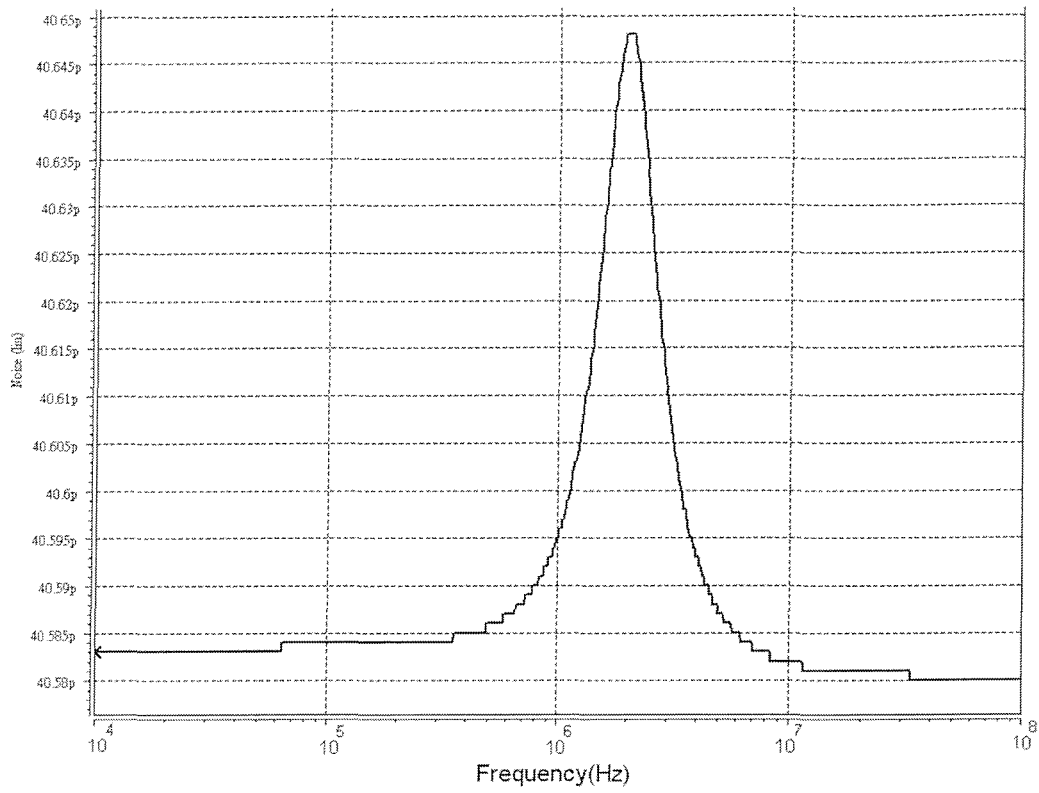


Fig. 3-28 Noise simulation result: amplitude-frequency response of Fig. 3-18

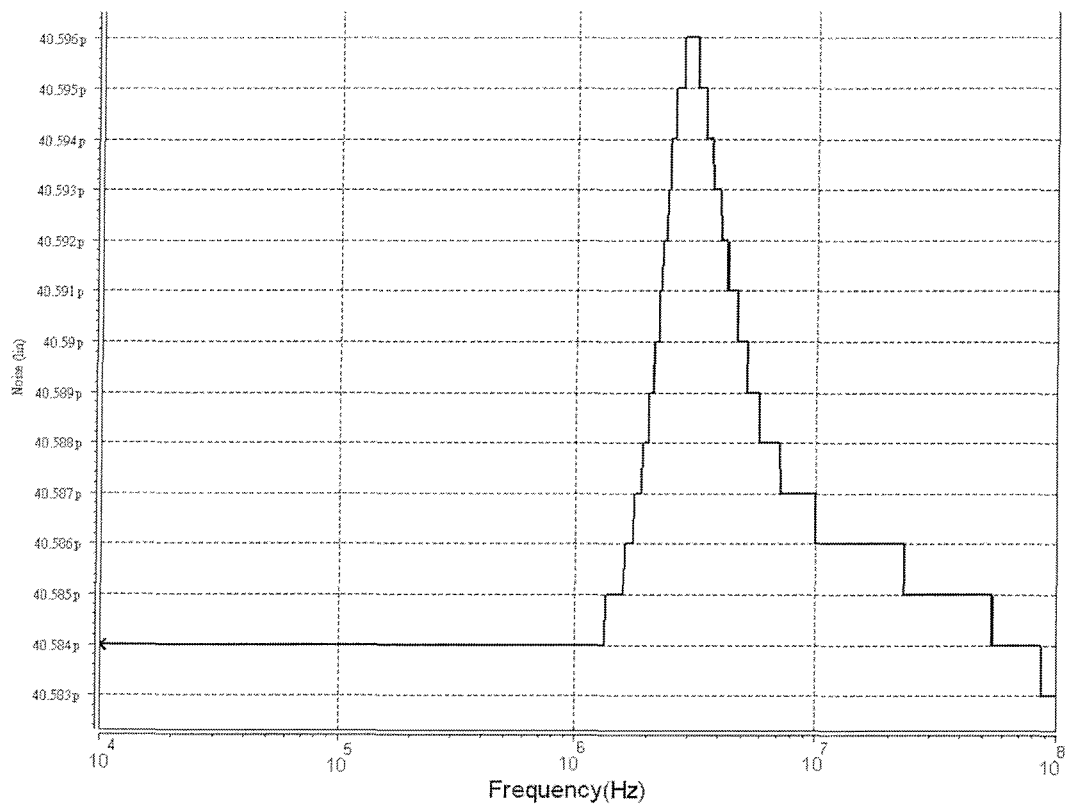


Fig. 3-29 Noise simulation result: amplitude-frequency response of Fig. 3-20

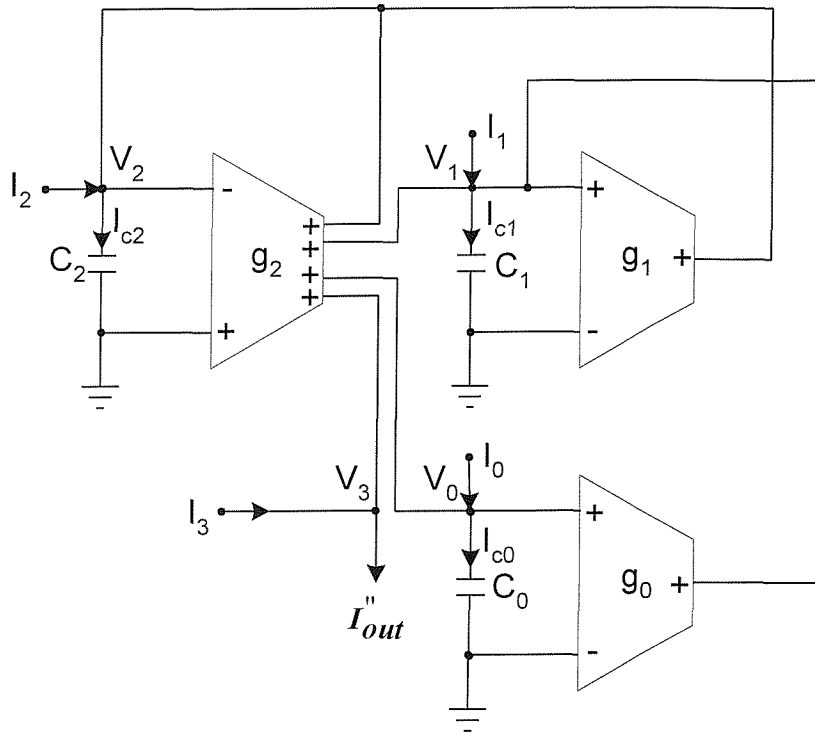


Fig. 3-30. 3rd-order current-mode OTA-C filter using the MISOC synthesis method.

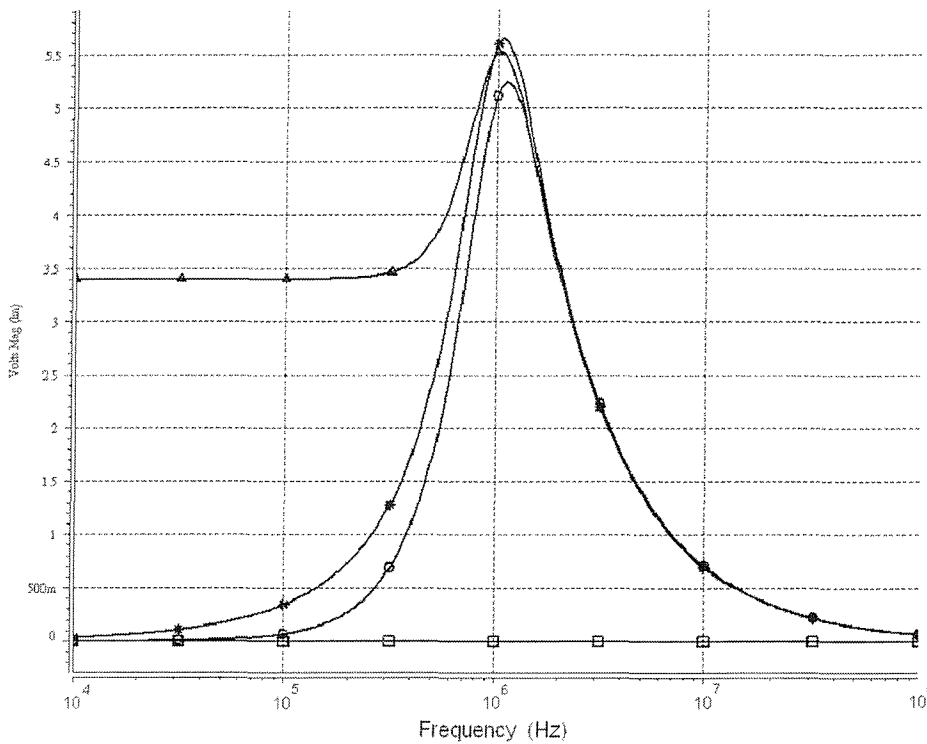


Fig. 3-31(a) Amplitude-frequency responses of node voltages, V_0 (o), V_1 (*), V_2 (Δ), and V_3 (\square) in Fig. 3-30 (high-pass)

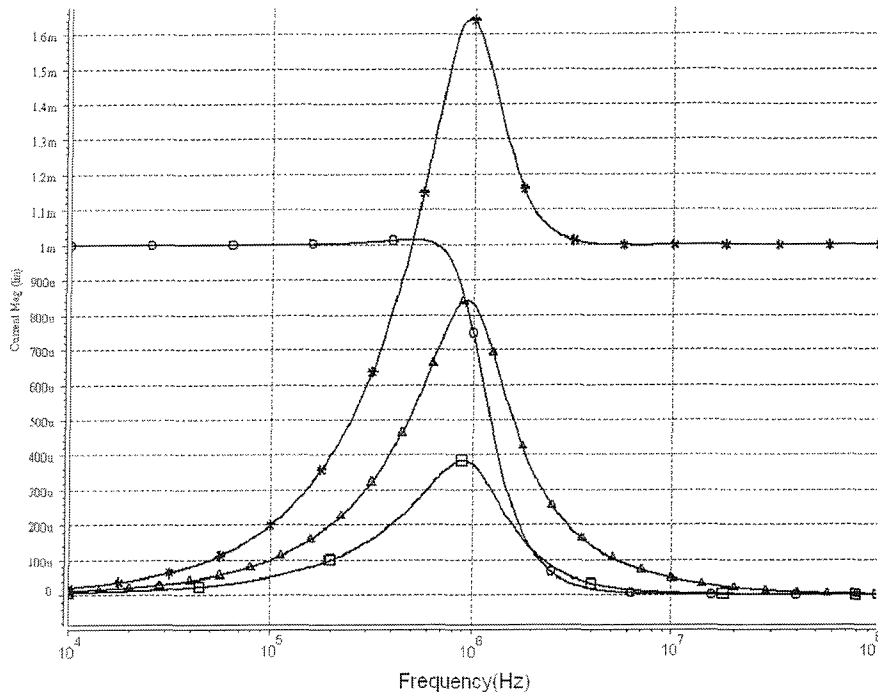


Fig. 3-31(b) Amplitude-frequency responses of branch currents, I_{out} (o), I_{co} (*), I_{cl} (Δ), and I_{c2} (\square) in Fig. 3-30 (low-pass)

3.8 Concluding Remarks

This chapter has presented two new analytical synthesis methods (MISOC and DIMOC) by using a succession of innovative algebra manipulation operations and their associated two filtering structures. The presented analytical synthesis method develops a coherent approach for solving a single complex equation representing an n th-order filter transfer function with different responses; under the constraint that the generated set of equations must be realizable using simple circuitry. The methods produce filters that have the *least* number of passive and active components and meet the other two design criteria: employment of single-input OTAs and grounded capacitors; indeed they generate canonical structures. Moreover, a useful feature of the synthesis methods is that different filter orders and functions can be obtained from the general filter structures either by suitable selection of current injection(s) at the filter inputs as the case in method, MISOC, or by current extraction(s) at the filter outputs as the case in method, DIMOC.

Chapter 4

Voltage-Mode High-Order OTA-C Filters Synthesis

Over the last decade or so numerous voltage-mode and current-mode high-order OTA-C filter structures have been reported [7-20]. Such structures have often been developed with different design criteria in mind, including reduced number of active elements, grounded capacitors, and simple design methods. It has described in Chapter 1, that there are *three main important criteria* [13], that need to be considered when generating OTA-C filter structures.

The aim of this chapter is to present two new analytical synthesis methods and three new voltage-mode high-order OTA-C filter structures employing only single-input OTAs, and grounded capacitors. The first analytical synthesis method realizes the first new filter structure which is capable of providing different filtering functions (LP, HP, BP) from different nodes without changing the filter topology. This is achieved without increasing the number of active elements; in fact, it has the least number of active and passive elements when compared with recently reported voltage-mode work including [16, 20]. It needs to be noticed that the equal transconductance design leads to single biasing technique and then easy control. The second filter structure is obtained by adding a linear input distribution OTA network to the first filter structure. Any voltage n th-order transfer functions. For example, elliptic filter transfer functions can be realized by the second filter structure which simultaneously enjoys the *three main important criteria*: the minimum components, only single-input OTAs, and only grounded capacitors. Moreover, its equal capacitance characteristic doesn't need to

adjust the values of capacitors in discrete steps [86] and then easy integrated circuit fabrication with precise requirement.

Despite the wealth of literature on voltage mode OTA-C filters, there is little reported work on the design of all-pass filters. All-pass filters find applications where phase linearity or group delay flatness is a major design consideration. Typical applications are high-frequency communications systems and disk read channels. The existing voltage mode OTA-C all-pass filters in the literature cannot achieve the *above three main important criteria* simultaneously. The filters in [16, 20] meet criteria (1) but not (2) and (3). The last aim of this chapter is to present a new analytical synthesis method which facilitates the development of voltage mode OTA-C all-pass filters capable of achieving all *three main important criteria* simultaneously. The least component count for the n th-order all-pass OTA-C filter is only $n+2$ single-input OTAs and n grounded capacitors.

This chapter presents two new voltage-mode analytical synthesis methods, presented in Sections 4.2 and 4.3, and three associated filter structures shown in Figs. 4-1, 4-4, and 4-6. Section 4.1 explains how to extend the current-mode analytical synthesis method to the voltage mode. Section 4.4 calculates the sensitivities of the new filter structure. A comparison with previous work is discussed in Section 4.5. The simulation results to validate the feasibility of the new filter structure are given in Section 4.6.

4.1 Extension Approach

In Chapter 3, four design principles about the new synthesis method were proposed. In order to obtain grounded capacitors and single-input OTAs, the latter of which may be called grounded OTAs (since the OTAs with one grounded input terminal are called the single-input OTAs), Kirchhoff's current law (other than Kirchhoff's voltage law) is suggested and used in the new synthesis method. Clearly, it is simple to do the analytical synthesis for a current-mode transfer function by using Kirchhoff's current law. However, it becomes difficult to do the analytical synthesis for a voltage-mode

transfer function by using Kirchhoff's current law because a voltage transfer function is a relationship between voltages, not currents, but Kirchhoff's current law is a relationship between currents, not voltages. The contradiction leads to the difficulty for realizing a voltage-mode transfer function by using the new synthesis method.

Then, how to solve the difficulty? An example of the transfer process is illustrated as follows.

Let a general n th-order voltage-mode all-pass transfer function be

$$\frac{V_{out}}{V_{in}} = \frac{\sum_{i=0}^n (-1)^i a_i s^i}{(-1)^n \sum_{i=0}^n a_i s^i} \quad (4-1)$$

Multiply both sides of Eq. (4-1) by a factor $\frac{a}{b}$, we obtain

$$\left(\frac{a}{b}\right) \frac{V_{out}}{V_{in}} = \left(\frac{a}{b}\right) \frac{\sum_{i=0}^n (-1)^i a_i s^i}{(-1)^n \sum_{i=0}^n a_i s^i} \quad (4-2)$$

If we regard a and b as the transconductances of the OTAs, then both aV_{out} and bV_{in} represent two "current" signals. Furthermore, if we let aV_{out} and bV_{in} be

$$V'_{out} \text{ and } V'_{in}, \text{ then Eq. (4-2) becomes } \frac{V'_{out}}{V'_{in}} = \left(\frac{a}{b}\right) \frac{\sum_{i=0}^n (-1)^i a_i s^i}{(-1)^n \sum_{i=0}^n a_i s^i} \quad (4-3)$$

Therefore, we can begin our analytical synthesis with the following initial transfer function:

$$\frac{V_{out}}{V_{in}} = \left(\frac{a}{b}\right) \frac{\sum_{i=0}^n (-1)^i a_i s^i}{(-1)^n \sum_{i=0}^n a_i s^i} \quad (4-4)$$

Although the difference between Eq. (4-1) and Eq. (4-4) is an amplification ratio a/b , it will lead to an easy analytical synthesis, because Eq. (4-4) is equivalent to the form of Eq. (4-2) with “current”-mode relationship. Moreover, due to the addition of the transconductances a and b in Eq. (4-4), the realized circuit from a voltage transfer function has two more OTAs in structure than that from a current transfer function without the transconductances a and b .

4.2 Analytical Synthesis Method I

Fig.4-1 shows the proposed n th-order filter structure where V_{in} is the filter input voltage, and $V_{out(0)}$, $V_{out(1)}$, $V_{out(2)}$, $V_{out(3)}$, ..., $V_{out(n-1)}$, and $V_{out(n)}$ are the $n+1$ filter voltage outputs. The settings of the $n+1$ filter output voltages determine the filter functions (LP, HP, BP). It can be seen that the structure employs only single-input OTAs and grounded capacitors.

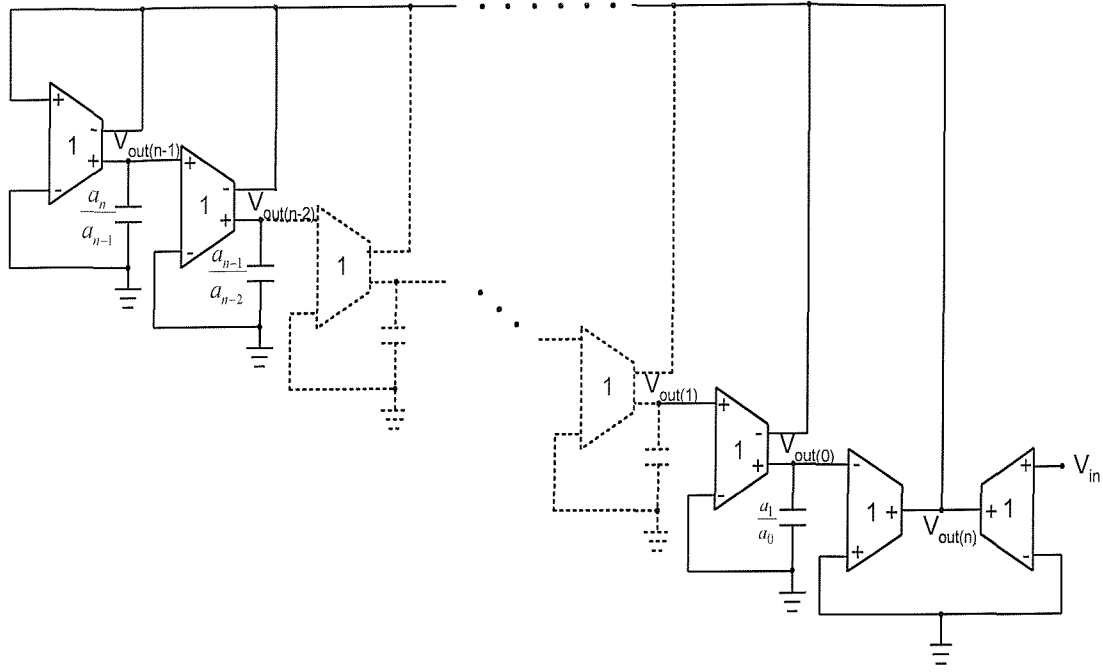


Fig.4-1. Nth-order OTA-C filter structure of the proposed analytical synthesis method

The filter structure of Fig.4-1 is obtained as follows. The general transfer functions of an nth-order low-pass, band-pass, and high-pass filter at different outputs can be written as:

$$V_{out(i)} = V_{in} \left(\frac{a_i s^i}{\Delta} \right), \text{ for } i = 0, 1, 2, \dots, n, \quad (4-5)$$

where $\Delta = a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0$.

The proposed new analytical synthesis method has five steps, they are explained as follows.

Step 1: Deal with the first transfer function, i.e., $i = 0$, algebraically.

If $i = 0$, Eq. (4-5) becomes

$$V_{out(0)} = \frac{a_0 V_{in}}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + a_{n-3} s^{n-3} + \dots + a_1 s + a_0} \quad (4-6)$$

Cross multiply Eq. (4-6), divide it by a_0 , and re-arrange,

$$V_{out(0)} \left(\frac{a_n s^n}{a_0} \right) = V_{in} - V_{out(0)} - V_{out(0)} \sum_{i=1}^{n-1} \left(\frac{a_i s^i}{a_0} \right) \quad (4-7)$$

Step 2: Combine the relationships of Eq. (4-5) with Eq. (4-7).

From Eq. (4-5), we have

$$V_{out(i)} = V_{out(0)} \left(\frac{a_i s^i}{a_0} \right); \quad (i = 1, 2, 3, \dots, n) \quad (4-8)$$

and

$$V_{out(i)} = V_{out(i-1)} \left(\frac{a_i s}{a_{i-1}} \right); \quad (i = 1, 2, 3, \dots, n) \quad (4-9)$$

Combining Eq. (4-8) with Eq. (4-9) yields

$$V_{out(i)} = V_{out(0)} \left(\frac{a_i s^i}{a_0} \right) = V_{out(i-1)} \left(\frac{a_i s}{a_{i-1}} \right); \quad (i = 1, 2, \dots, n) \quad (4-10)$$

Substituting Eq. (4-10) into Eq. (4-7) gives

$$V_{in} - V_{out(0)} = \sum_{i=1}^n V_{out(i-1)} \left(\frac{a_i s}{a_{i-1}} \right) \quad (4-11)$$

Step 3: Transfer the voltage mode formats to their corresponding current-mode formats for Eqs. (4-11) and (4-9).

Eq. (4-11) is a voltage relationship. In order to be consistent with the input-and-output current relationship of an OTA, i.e., $(V_+ - V_-)g_m = I_{out}$, we multiply each side of Eq. (4-11)

by an equal transconductance of unity value (1), leading to

$$(V_{in} - V_{out(0)})(1) = \sum_{i=1}^n V_{out(i-1)} \left(\frac{a_i s}{a_{i-1}} \right) (1) = \sum_{i=1}^n V_{out(i-1)} \left[\left(\frac{a_i s}{a_{i-1}} \right) / (1) \right] (1) \quad (4-12)$$

Then, Eq. (4-9) can be derived as $V_{out(i)} = V_{out(i-1)} \left[\left(\frac{a_i s}{a_{i-1}} \right) / (1) \right]; (i = 1, 2, 3, \dots, n)$,

$$\text{Namely, } V_{out(i)}(1) = V_{out(i-1)} \left(\frac{a_i s}{a_{i-1}} \right); (i = 1, 2, 3, \dots, n). \quad (4-13)$$

Step 4: Substituting Eq. (4-13) into Eq. (4-12) yields

$$(V_{in} - V_{out(0)})(1) = \sum_{i=1}^n V_{out(i)}(1) \quad (4-14)$$

Step 5: Realize the simple equations, i.e., Eqs. (4-13) and (4-14) and combine all the realized circuit structures.

By using the active element, OTA, whose characteristic relationship is $I_{out} = g_m V_{in}$, and the grounded capacitor, whose admittance is sC , to implement Eq. (4-13), a fundamental OTA-grounded capacitor structure is shown in Fig. 4-2, in which $\left(\frac{a_i}{a_{i-1}} \right)$ are the values of the capacitors, and the unity is the value of the transconductance of the OTA. Next, we implement Eq. (4-14) using the output currents of the OTAs and Kirchhoff's current law. The combination of the individual circuit yields the circuit shown in Fig. 4-1. Note that the values of all the transconductances are unity. It means that only one biasing current is required for the whole circuit leading to the benefit: easy control with simple circuitry.

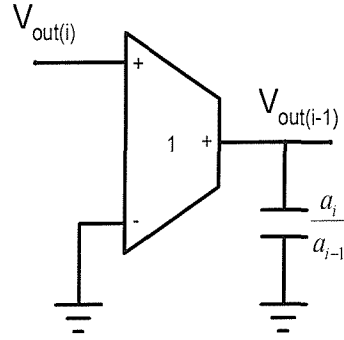


Fig.4-2. OTA-grounded C realization of the integrator given by Eq. (4-13)

In summary, the proposed synthesis method has decomposed the n th-order transfer function (Eq. (4-5)) into $n+1$ transfer functions including n^{th} , 1^{st} -order transfer functions (Eq.(4-13)) and one constraint equation (Eq. (4-14)).

To illustrate the synthesis method, consider the structure generation of a 4^{th} -order filter. The synthesis method uses Eqs. (4-13) and (4-14). Based on these equations, when $n=4$, we have the following 5 equations:

$$V_{out(1)}(1) = V_{out(0)} \left(\frac{a_1 s}{a_0} \right), \text{ from Eq. (4-13);}$$

$$V_{out(2)}(1) = V_{out(1)} \left(\frac{a_2 s}{a_1} \right), \text{ from Eq. (4-13);}$$

$$V_{out(3)}(1) = V_{out(2)} \left(\frac{a_3 s}{a_2} \right), \text{ from Eq. (4-13);}$$

$$V_{out(4)}(1) = V_{out(3)} \left(\frac{a_4 s}{a_3} \right), \text{ from Eq. (4-13); and}$$

$$(V_{in} - V_{out(0)})(1) = \sum_{i=1}^4 V_{out(i)}(1), \text{ from Eq. (4-14).}$$

Implementing the above equations using single-ended-input OTAs and grounded capacitors, the 4^{th} -order OTA-C filter is shown in Fig. 4-3 with the following three transfer functions

$$\frac{V_{out(0)}}{V_{in}} = \left(\frac{a_0}{\Delta} \right) \text{ (Low-pass);}$$

$$\frac{V_{out(2)}}{V_{in}} = \left(\frac{a_2 s^2}{\Delta} \right) \text{ (Band-pass);}$$

$$\frac{V_{out(4)}}{V_{in}} = \left(\frac{a_4 s^4}{\Delta} \right) \text{ (High-pass);}$$

$$\text{where } \Delta = a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s + a_0. \quad (4-15)$$

It should be noted that, in general, a voltage follower may be necessary at the output of the filter to buffer the output and avoid the effects of load capacitance or resistance changing the response of the filter.

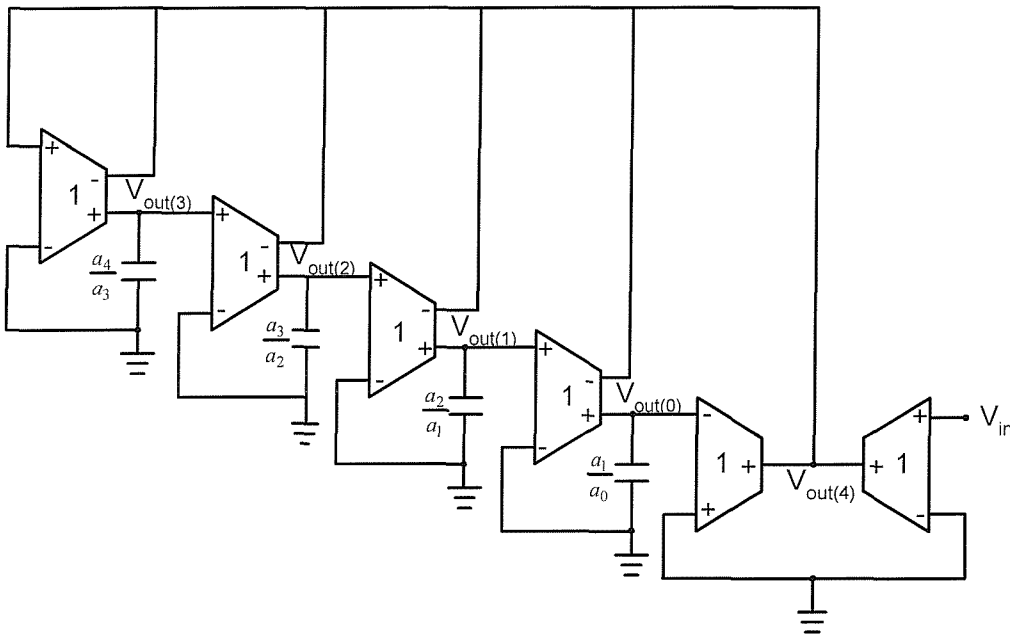


Fig.4-3. 4th-order OTA-C LP, BP, and HP filters derived from Fig.4-1

For realizing n th-order OTA-C low-pass, band-pass, and high-pass filters, we proposed a new filter structure, shown in Fig.4-1. Eq. (4-5), corresponding to Fig.4-1, shows that there are $n+1$ different-order transfer functions which can be realized at $n+1$ different nodes in Fig.4-1, respectively. The general n th-order voltage transfer function, shown as below,

$$\frac{V_{out}}{V_{in}} = \frac{b_n s^n + b_{n-1} s^{n-1} + b_{n-2} s^{n-2} + \dots + b_2 s^2 + b_1 s + b_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_2 s^2 + a_1 s + a_0} \quad (4-16)$$

is the linear combination of the n+1 different-order transfer functions shown in Eq. (4-5), i.e.,

$$\frac{V_{out}}{V_{in}} = \frac{b_n s^n + b_{n-1} s^{n-1} + b_{n-2} s^{n-2} + \dots + b_2 s^2 + b_1 s + b_0}{a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_2 s^2 + a_1 s + a_0} = \sum_{i=0}^n \left[\left(\frac{b_i}{a_i} \right) \left(\frac{a_i s^i}{\Delta} \right) \right]$$

$$\text{where } \Delta = a_n s^n + a_{n-1} s^{n-1} + a_{n-2} s^{n-2} + \dots + a_2 s^2 + a_1 s + a_0. \quad (4-17)$$

Two synthesis approaches to realize the above relationship are proposed as follows.

(i) Using the linear combination method to perform the synthesis, multiply both sides of Eq. (4-17) by V_{in} and obtain

$$V_{out} = (1) \times \sum_{i=0}^n \left[\left(\frac{b_i}{a_i} \right) \left(\frac{a_i s^i}{\Delta} V_{in} \right) \right] \quad (4-18)$$

Then, we take each nodal voltage in the circuit structure of Fig. 4-1, i.e., $V_{out(i)}$ ($= \frac{a_i s^i}{\Delta} V_{in}$) in which $i = 0, 1, 2, \dots, n-1, \text{ and } n$, as the input voltage of an extra OTA with the transconductance b_i/a_i . Join all of the output terminals of the n+1 extra OTAs and connect the summing point with an equivalent grounded resistor realized by a single-ended-input OTA with unity transconductance. The realized circuit structure shown in Fig. 4-5 uses 2n+4 single-ended-input OTAs and n grounded capacitors.

(ii) A more effective synthesis approach is explained as follows. Multiply both sides of Eq. (4-17) by V_{in} and obtain the following other form (different from Eq. (4-18))

$$V_{out} = \sum_{i=0}^n \left[\left(V_{in} \frac{b_i}{a_i} \right) \left(\frac{a_i s^i}{\Delta} \right) \right] \quad (4-19)$$

The physical meaning of the above relationship is “to insert different weights of the input voltage signal, V_{in} , into each node in the filter structure shown in Fig.4-1 and then obtain the output voltage signal”. According to this approach [14, 16, 83], giving a forward signal, with a weight of input voltage signal, from input voltage node to each inner node in the filter structure shown in Fig.4-1, we obtain the other new OTA-C filter structure, shown in Fig.4-4, for realizing the general nth-order voltage transfer function, including elliptic filter functions, shown in Eq. (4-16). The realized circuit structure uses $2n+2$ single-ended-input OTAs and n grounded capacitors.

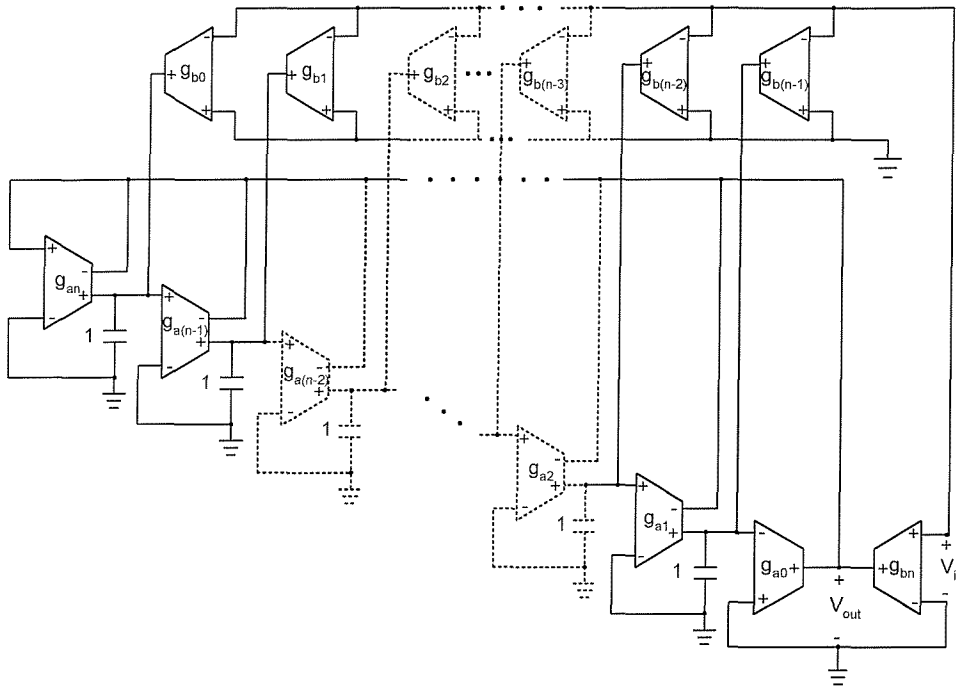


Fig.4-4. OTA-C filter structure II for realizing general nth-order transfer functions

Note that the values of all the capacitances are unity. Because the values of a capacitor cannot be adjusted in any continuous fashion in thin film circuits [86], the equal capacitance characteristic makes the IC fabrication much easier under a precise requirement.

The circuit structure (Fig.4-4) of approach (ii) uses two fewer single-input OTAs than that (Fig.4-5) of approach (i) and is recommended to realize the general nth-order voltage transfer function shown in Eq. (4-16). Note that, in Fig.4-4, all $2n+2$ OTAs have single-ended input and all n capacitors are grounded. The numbers of active OTAs

and grounded capacitors are the minimum numbers [16] to realize such a general nth-order voltage transfer function shown in Eq. (4-16).

In Fig.4-1, although we let all the transconductances of the OTAs be unity and the capacitances of n grounded capacitors be $a_1/a_0, a_2/a_1, a_3/a_2 \dots \dots, a_{n-1}/a_{n-2},$ and $a_n/a_{n-1},$ in fact, all the values of the transconductances and the capacitances can be given flexibly. The restriction of the values of the transconductances and the capacitances shown in Fig.4-1 is used for being consistent with the derivation process and the original given transfer functions shown in Eq. (4-5). Similarly, in order to simplify and clarify the network analysis of Fig.4-4, we let the value of each grounded capacitor be unity although, as a matter of fact, it can be given by any different required value. Circuit analysis yields the following transfer function for Fig.4-4:

$$\frac{V_{out}}{V_{in}} = \frac{s^n g_{bn} + \sum_{i=1}^{n-1} s^i \left[\sum_{j=0}^i g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right] + g_{b0} \left(\prod_{j=0}^{n-1} g_{aj} \right)}{\sum_{i=0}^n s^i \left(\prod_{j=0}^{n-i} g_{a(n-j)} \right)} = \frac{\sum_{i=0}^n s^i B_i}{\sum_{i=0}^n s^i A_i} \quad (4-20)$$

All $g_{ai}, i = 0, 1, 2 \dots \dots, n-1, n,$ can be found exactly, i.e.,

$$g_{an} = a_n, \text{ and } g_{ai} = \frac{a_i}{a_{i+1}} \text{ for } i = 0, 1, 2 \dots \dots, n-2, n-1, \quad (4-21)$$

by solving the following $n+1$ equations

$$\prod_{j=0}^{n-i} g_{a(n-j)} = a_i, \quad i = 0, 1, 2 \dots \dots, n-1, n. \quad (4-22)$$

And all $g_{bi}, i = 0, 1, 2 \dots \dots, n-1, n,$ can be found exactly by solving the following another $n+1$ equations

$$\begin{aligned} g_{bn} &= b_n \\ \sum_{j=0}^i g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) &= b_i, \quad i = 1, 2 \dots \dots, n-1. \\ g_{b0} \left(\prod_{j=0}^{n-1} g_{aj} \right) &= b_0 \end{aligned} \quad (4-23)$$

In any cases, if the calculated $g_{bj} = 0$, then the corresponding OTA should be eliminated; and if the calculated g_{bj} is a negative value, then the two input terminals of the corresponding OTA should be interchanged.

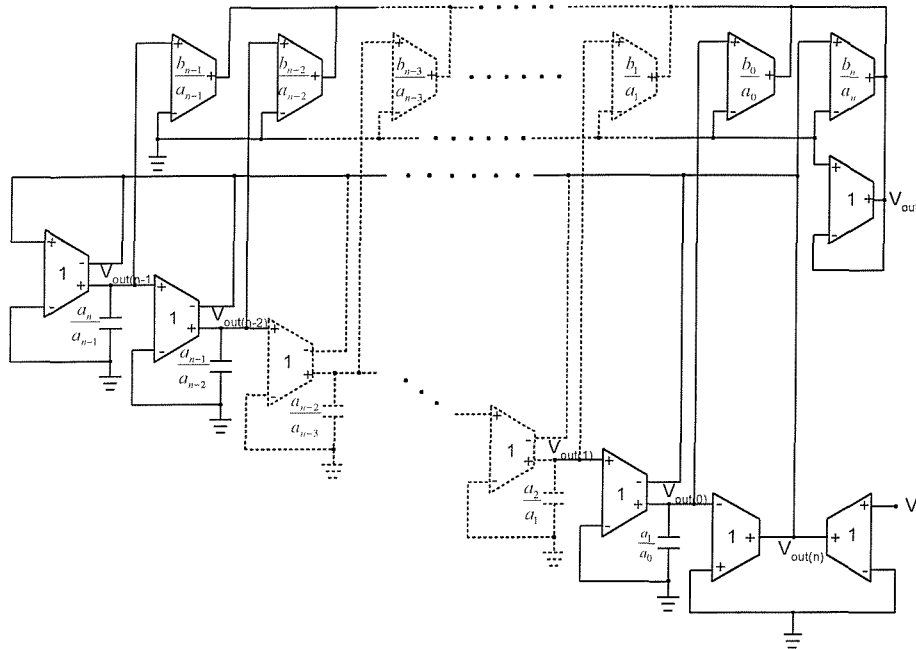


Fig.4-5. OTA-C filter structure I for realizing general nth-order transfer functions

4.3 Analytical Synthesis Method II

Analytical synthesis method I discussed in Section 4.2 can also realize an nth-order voltage-mode all-pass filter. However, the component count necessary, $2n+2$ single-input OTAs and n grounded capacitors shown in Fig. 4-4, is much more than those, $n+2$ single-input OTAs and n grounded capacitors, needed to realize an nth-order voltage-mode low-pass, band-pass, and high-pass filter shown in Fig. 4-1. It means that a filter structure with the general case is much complicated in structure than a filter structure with a single or some function(s). Therefore, it is needed to develop another analytical synthesis method for high-order voltage-mode OTA-C all-pass filters which is discussed next.

The method is based on the analytical decomposition of a single, n th-order all-pass filter transfer function into n first order voltage mode transfer functions and one constraint. A succession of innovative algebra manipulation operations goes through the derivation. The method is based on an n th-order all-pass filter structure with single input, and single output voltage (Fig.4-6). The general transfer function of an n th-order all-pass filter is:

$$\frac{V_{out}}{V_{in}} = \left(\frac{a}{b}\right) \frac{\sum_{i=0}^n (-1)^i a_i s^i}{(-1)^n \sum_{i=0}^n a_i s^i} \quad (4-24)$$

The proposed new analytical synthesis method has two steps, they are explained as follows.

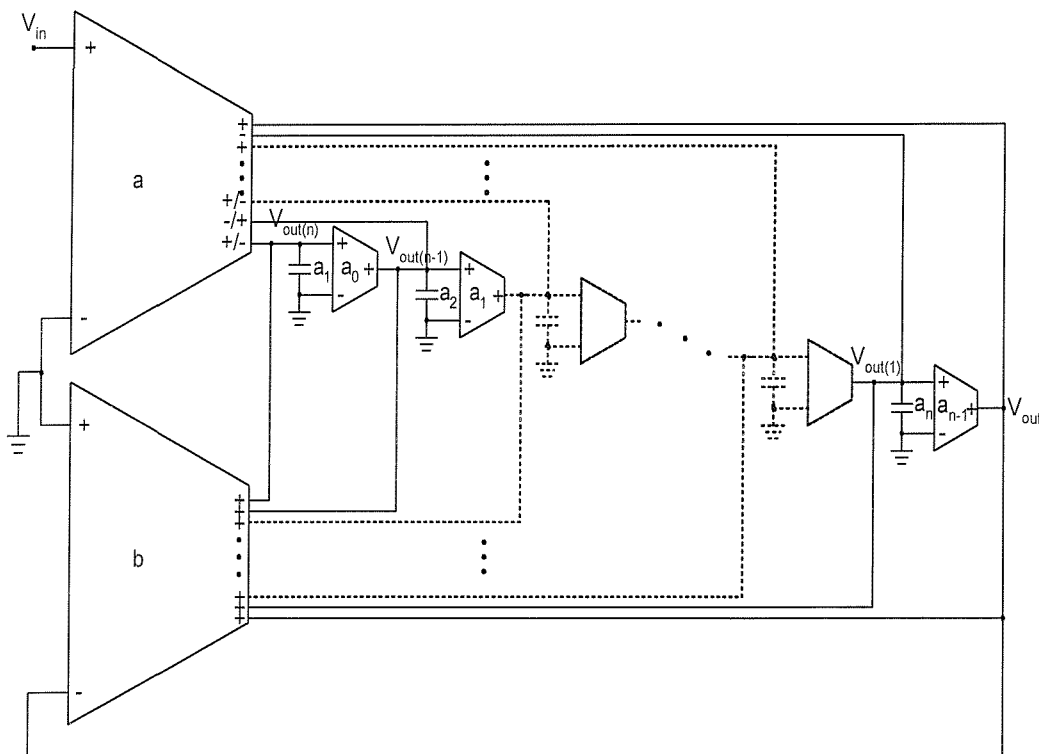


Fig.4-6. Nth-order OTA-C all-pass filter structure

Step 1: Deal with Eq. (4-24) algebraically.

Cross multiply Eq. (4-24), $(-1)^n bV_{out} \sum_{i=0}^n a_i s^i = aV_{in} \sum_{i=0}^n (-1)^i a_i s^i$

Divide it by $a_n s^n$ and $(-1)^n$, and re-arrange,

$$bV_{out} - aV_{in} = \sum_{i=1}^{i=n} \left[(-1)^{-i} aV_{in} - bV_{out} \right] \frac{a_{n-i}}{a_n s^i} \quad (4-25)$$

To give insight into the analytical decomposition of Eq. (4-25) into n first-order transfer functions and one additional constraint, it is better if we illustrate the decomposition with reference to the first two terms of Eq. (4-25) and then generalise the synthesis method. The first two terms of Eq. (4-25) are:

$$bV_{out} - aV_{in} = \left[(-1)^{-1} aV_{in} - bV_{out} \right] \frac{a_{n-1}}{a_n s} + \left[(-1)^{-2} aV_{in} - bV_{out} \right] \frac{a_{n-2}}{a_n s^2} \quad (4-26)$$

$$\text{Let } \left(\frac{a_{n-2}}{a_n s^2} \right) = \left(\frac{a_{n-2}}{a_{n-1} s} \right) \left(\frac{a_{n-1}}{a_n s} \right) \quad (4-27)$$

Substitute Eq. (4-27) into Eq. (4-26) produces:

$$bV_{out} - aV_{in} = \left[(-1)^{-1} aV_{in} - bV_{out} \right] \frac{a_{n-1}}{a_n s} + \left[(-1)^{-2} aV_{in} - bV_{out} \right] \frac{a_{n-2}}{a_{n-1} s} \frac{a_{n-1}}{a_n s} \quad (4-28)$$

Taking the common term $\left(\frac{a_{n-1}}{a_n s} \right)$ out from above equation gives:

$$bV_{out} - aV_{in} = \left[\left[(-1)^{-1} aV_{in} - bV_{out} \right] + \left[(-1)^{-2} aV_{in} - bV_{out} \right] \frac{a_{n-2}}{a_{n-1}s} \right] \frac{a_{n-1}}{a_n s} \quad (4-28)$$

In general, Eq. (4-27) can be rewritten as:

$$\frac{a_{n-i}}{a_n s^i} = \prod_{j=0}^{i-1} \left(\frac{a_{n-j-1}}{a_{n-j}s} \right); \quad (i = 1, 2, \dots, n-1, n.) \quad (4-29)$$

Substitute Eq. (4-29) into Eq. (4-25) and follow same procedure used to obtain Eq. (4-28) yields Eq. (4-30).

$$bV_{out} - aV_{in} = \left[\left[(-1)^{-1} aV_{in} - bV_{out} \right] + \left[\left[(-1)^{-2} aV_{in} - bV_{out} \right] + \dots \right. \right. \left. \left. \left[(-1)^{1-n} aV_{in} - bV_{out} \right] \right] \frac{a_1}{a_2 s} \dots \left[(-1)^{-n} aV_{in} - bV_{out} \right] \frac{a_0}{a_1 s} \right] \frac{a_{n-2}}{a_{n-1}s} \frac{a_{n-1}}{a_n s} \quad (4-30)$$

Step 2: Extract out $n+1$ simple parts and assume $n+1$ simple equations from the complicated Eq. (4-30). Then realize and combine all of them.

Observing Eq. (4-30), we let

$$\left[(-1)^{-n} aV_{in} - bV_{out} \right] \frac{a_0}{a_1 s} = a_0 V_{out(n)} \quad (4-31a)$$

Eq. (4-31a) can be realised using the OTA-C structure shown in Fig.4-7, in which we use three single-input OTAs with three different trans-conductances, a_0 , a , and b , and one grounded capacitor with capacitance a_1 . The choice of the output +/- of the input OTA with transconductance a , is based upon an even/odd order n of Eq. (4-31a).

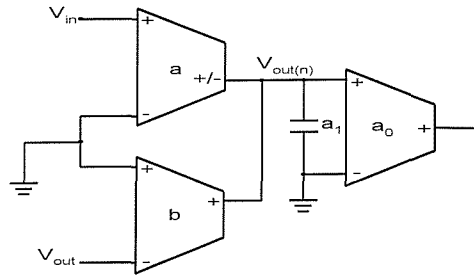


Fig.4-7. OTA-C implementation of Eq. (4-31a)

Substitute Eq. (4-31a) into Eq. (4-30) yields

$$bV_{out} - aV_{in} = \left[\left[(-1)^{-1} aV_{in} - bV_{out} \right] + \left[\left[(-1)^{-2} aV_{in} - bV_{out} \right] + \dots \right] + \left[\left[(-1)^{1-n} aV_{in} - bV_{out} \right] + \left[a_0 V_{out(n)} \right] \right] \frac{a_1}{a_2^s} \dots \frac{a_{n-2}}{a_{n-1}^s} \frac{a_{n-1}}{a_n^s} \quad (4-32)$$

Observing Eq. (4-32), we then let

$$\left[(-1)^{1-n} aV_{in} - bV_{out} + a_0 V_{out(n)} \right] \frac{a_1}{a_2^s} = a_1 V_{out(n-1)} \quad (4-31b)$$

Fig.4-8 shows the OTA-C structure implementation of Eqs. (4-31a) and (4-31b).

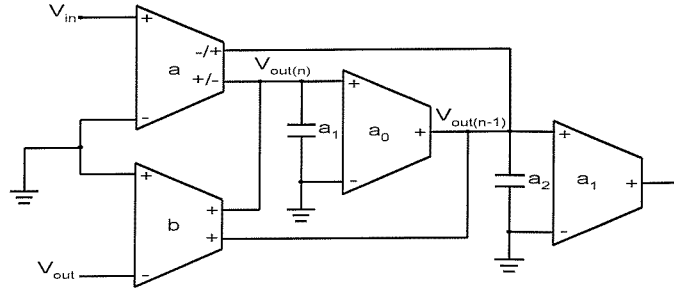


Fig.4-8. OTA-C implementation of Eqs. (4-31a) and (4-31b).

Using Eq. (4-31a) and (4-31b), we can obtain the following general $n-1$ individual equations from Eq. (4-32).

$$\left[(-1)^{-i} a V_{in} - b V_{out} + a_{n-i-1} V_{out(i+1)} \right] \frac{a_{n-i}}{a_{n-i+1} s} = a_{n-i} V_{out(i)} ; (i = 1, 2, 3, \dots, n-2) \quad (4-31c)$$

and

$$V_{out} = \left(a_{n-1} V_{out(1)} + a V_{in} \right) \left(\frac{1}{b} \right) \quad (4-31d)$$

Implementing Eqs. (4-31c) and (4-31d) using similar circuits of Figs.4-7 and 4-8 yields the n th-order OTA-C all-pass filter structure shown in Fig.4-6. Note that all the $n+2$ active elements are single-input OTAs and all the n capacitors are grounded. In summary, the proposed synthesis method has decomposed an n th-order all-pass transfer function (Eq. (4-24)) into n first-order transfer functions and one constraint given by Eqs. (4-31a) to (4-31d).

To illustrate the proposed synthesis method, consider the structure generation of a 6th-order all-pass filter. The synthesis method uses Eqs. (4-31a) to (4-31d), based on these equations, when $n=6$, we have the following 7 equations:

$$\left[(-1)^{-6} aV_{in} - bV_{out}\right] \frac{a_0}{a_1 s} = a_0 V_{out(6)}, \text{ from Eq. (4-31a)}$$

$$\left[(-1)^{-5} aV_{in} - bV_{out} + a_0 V_{out(6)}\right] \frac{a_1}{a_2 s} = a_1 V_{out(5)}, \text{ from Eq. (4-31b)}$$

$$\left[(-1)^{-4} aV_{in} - bV_{out} + a_1 V_{out(5)}\right] \frac{a_2}{a_3 s} = a_2 V_{out(4)}$$

$$\left[(-1)^{-3} aV_{in} - bV_{out} + a_2 V_{out(4)}\right] \frac{a_3}{a_4 s} = a_3 V_{out(3)}$$

$$\left[(-1)^{-2} aV_{in} - bV_{out} + a_3 V_{out(3)}\right] \frac{a_4}{a_5 s} = a_4 V_{out(2)}$$

$$\left[(-1)^{-1} aV_{in} - bV_{out} + a_4 V_{out(2)}\right] \frac{a_5}{a_6 s} = a_5 V_{out(1)}, \text{ from Eq. (4-31c)}$$

$$bV_{out} - aV_{in} = a_5 V_{out(1)}, \text{ from Eq. (4-31d)}$$

Implementing the above equations using single-input OTAs and grounded capacitors, the 6th-order OTA-C all-pass filter is shown in Fig.4-9.

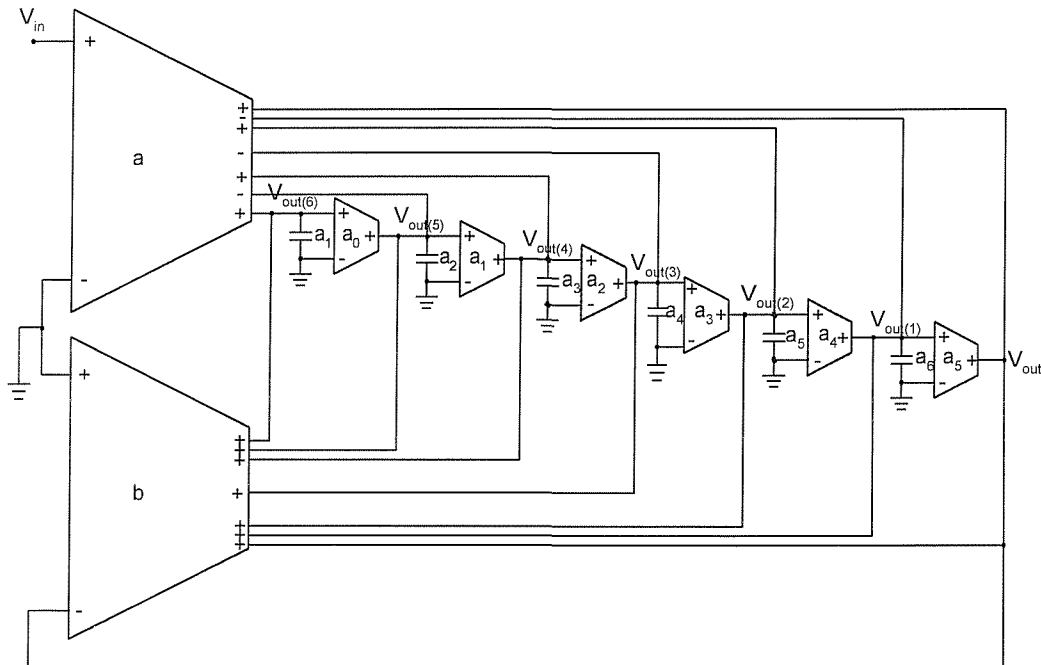


Fig.4-9. 6th-order OTA-C all-pass filter derived from Fig.4-6

4.4 Sensitivity Analysis

The relative sensitivities, $S_x^Y = \left(\frac{x}{Y}\right)\left(\frac{\partial Y}{\partial x}\right)$, are the values of filter transfer function coefficients with respect to circuit elements. If we let the values of all capacitors from the right side in Fig.4-4 be $C_0, C_1, C_2, \dots, C_{n-2}$, and C_{n-1} , respectively, as we divide both numerator and denominator of its transfer function by $(C_0 C_1 C_2 \dots C_{n-2} C_{n-1})$, the transfer function of Fig.4-4 is similar to Eq. (4-20) by replacing g_{ai} with g_{ai}/C_i for $i = 0, 1, 2, \dots, n-2$ and $n-1$. Since the sensitivities to C_i , g_{ai} , and g_{bi} can be easily derived and obtained from the sensitivities of Eq. (4-20), we will only give the results of the sensitivities of Eq. (4-20) which are shown as follows.

For the general pole realisation, the denominator coefficient sensitivities to g_{ai} and g_{bi} are unity and zero, respectively. For the zero implementation, the numerator coefficient sensitivities are

$$S_{g_{bi}}^{B_n} = 0 \text{ for } i = 0, 1, 2, \dots, n-1, S_{g_{bn}}^{B_n} = 1, \quad (4-33)$$

$$S_{g_{bi}}^{B_0} = 0 \text{ for } i = 1, 2, \dots, n-1, n, S_{g_{b0}}^{B_0} = 1, \quad (4-34)$$

$$S_{g_{bj}}^{B_i} = \frac{g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right)}{\sum_{j=0}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]} \text{ for } i = 1, 2, 3, \dots, n-1, \text{ and } j = 0, 1, 2, \dots, i. \quad (4-35)$$

$$S_{g_{ai}}^{B_n} = 0 \text{ for } i = 0, 1, 2, 3, \dots, n-1, n. \quad (4-36)$$

$$S_{g_{a(n-1)}, g_{a(n-2)}, \dots, g_{a1}, g_{a0}}^{B_0} = 1, S_{g_{an}}^{B_0} = 0, \quad (4-37)$$

$$S_{g_{ai}, g_{a(i+1)}, \dots, g_{a(n-1-i)}}^{B_i} = 1 \text{ for } i = 1, 2, 3, \dots, n-1, \text{ and } n-1-i \geq i. \quad (4-38)$$

If there exist positive integer i which is a solution of $n-1-i \geq i$, then

$$S_{g_{am}}^{B_i} = \frac{\sum_{j=i-m}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]}{\sum_{j=0}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]} \text{ for } m = 0, 1, 2, 3, \dots, i-1, \quad (4-39)$$

$$S_{g_{am}}^{B_i} = \frac{\sum_{j=0}^{n-m-1} \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]}{\sum_{j=0}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]} \text{ for } m = n-i, n-i+1, \dots, n-1. \quad (4-40)$$

If there don't exist positive integer i which is a solution of $n-1-i \geq i$, then

$$S_{g_{a(n-i+0) \cdot g_{a(n-i+1)} \cdots g_{a(n-i+m)} \cdots g_{a(i-1)}}^{B_i} = \frac{\sum_{j=2i-n-m}^{i-1-m} \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]}{\sum_{j=0}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]}$$

for $m = 0, 1, 2, \dots$ and $i-1 \geq n-i$, (4-41)

$$S_{g_{am}}^{B_i} = \frac{\sum_{j=i-m}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]}{\sum_{j=0}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]} \text{ for } m = 0, 1, 2, 3, \dots, n-i-1, \quad (4-42)$$

$$S_{g_{am}}^{B_i} = \frac{\sum_{j=0}^{n-m-1} \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]}{\sum_{j=0}^i \left[g_{bj} \left(\prod_{k=0}^{n-1-i} g_{a(i-j+k)} \right) \right]} \text{ for } m = n-i, n-i+1, \dots, n-1. \quad (4-43)$$

The above denominator and numerator coefficient sensitivities are in the range from -1 to 1 provided that all g_{ai} and g_{bi} are positive.

In Fig.4-6, although we let all the transconductances of the OTAs be $a_0, a_1, a_2, \dots, a_{n-2},$ and a_{n-1} and the capacitances of n grounded capacitors be $a_1, a_2, a_3, \dots, a_{n-1},$ and a_n in fact, all the values of the transconductances and the capacitances can be given flexibly. The restriction of the values of the transconductances and the capacitances shown in Fig.4-6 is used for being consistent with the derivation process and the original given transfer functions shown in Eq. (4-24). If we replace the values of the grounded capacitors with $C_1, C_2, C_3, \dots, C_{n-1},$ and C_n and the values of the transconductances with $g_1, g_2, g_3, \dots, g_{n-1},$ and $g_n,$ respectively, then circuit analysis yields the following transfer function of Fig.4-6:

$$\frac{V_{out}}{V_{in}} = \frac{a(-1)^n s^n \left(\prod_{j=1}^n C_j \right) + a \sum_{i=1}^{n-1} \left[(-1)^i s^i \left(\prod_{j=1}^i C_j \right) \left(\prod_{k=i+1}^n g_k \right) \right] + a(-1)^0 \left(\prod_{k=1}^n g_k \right)}{bs^n \left(\prod_{j=1}^n C_j \right) + b \sum_{i=1}^{n-1} \left[s^i \left(\prod_{j=1}^i C_j \right) \left(\prod_{k=i+1}^n g_k \right) \right] + b \left(\prod_{k=1}^n g_k \right)} = \frac{\sum_{i=0}^n s^i B_i}{\sum_{i=0}^n s^i A_i} \quad (4-44)$$

For the general pole and zero realisations, the denominator and numerator coefficient sensitivities to $C_j,$ $a,$ $b,$ and g_k are unity or zero, all of which are small.

4.5 Comparison with Previous Work

In this chapter, two new analytical synthesis methods I and II, shown in Sections 4.2 and 4.3, have been proposed. To simplify the comparison, the comparison for synthesis method I is separate from that for synthesis method II. Two comparison parameters, component count and component spread, are considered.

Comparison for Synthesis Method I

Component Count

Fig.4-3 shows how the new filter structure provides 4th-order low-pass ($V_{out(0)}$), high-pass ($V_{out(4)}$) and band-pass ($V_{out(2)}$) responses at different nodes. It can be seen that the

filter has six single-input OTAs and four grounded capacitors. In general the new filter structure, shown in Fig. 4-1, for a given order of n , has $n+2$ single-input OTAs, and n grounded capacitors. Fig.4-10 (a) and (b) show 4th-order high-pass and band-pass filter circuits obtained using the structure in [16]. As can be seen both circuits not only employ double-input and single-input OTAs, but also more active elements than the circuits (Fig.4-3) obtained using the new structure. For example the high-pass circuit has ten OTAs, and the band-pass circuit has eight OTAs. Similarly, Fig.4-11 (a) and (b) show 4th-order high-pass and band-pass circuits obtained using the structure in [20]. Again, it can be seen that the circuits (Fig.4-3) obtained using the new structure employ less active components than the circuits in Fig.4-11. Table 4-1 shows a comparison in terms of number of OTAs, types of OTAs, number of capacitors and types of capacitors between the proposed filter structures (Figs.4-1 and 4-4), and those recently reported in [16] and [20]. It can be seen that the proposed first filter structure (Fig.4-1), which can realize low-pass, band-pass, and high-pass filters, has the least number of OTAs, $n+2$, compared with $2n+2$ [16] and $3n+3$ [20]. The table also shows how the proposed filter structure (Fig.4-4) compares with those of [16] and [20]. As can be seen it has the same number of OTAs as that of [16] but fewer OTAs than [20]. Moreover, the proposed second filter structure (Fig.4-4) uses all single-input OTAs unlike those in [16] and [20].

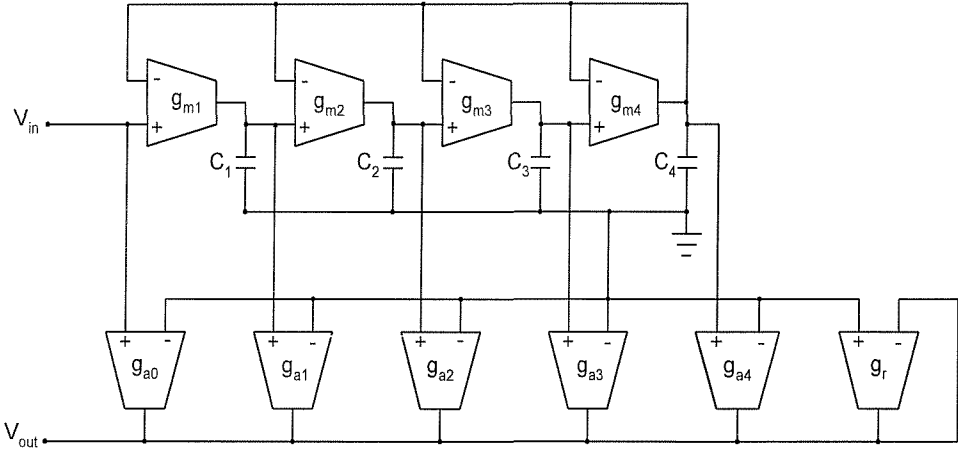


Fig.4-10 (a) 4th-order voltage-mode OTA-C high-pass filter [16]

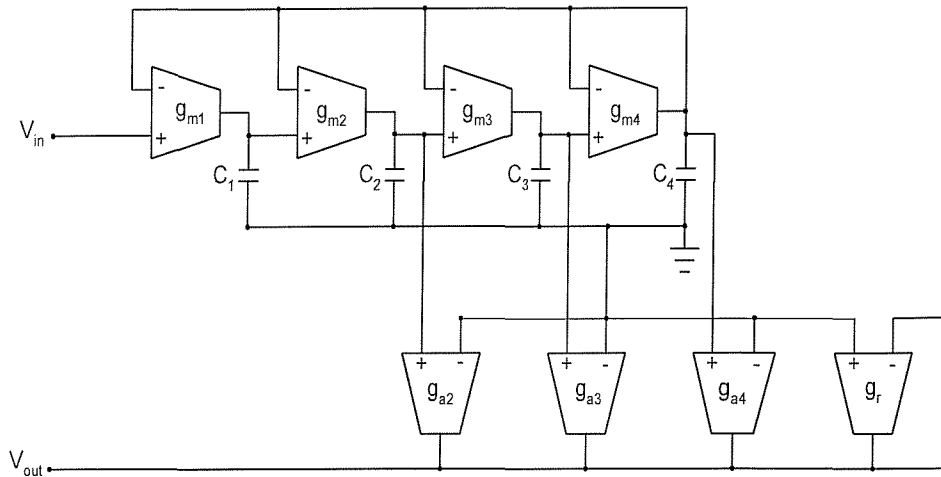


Fig.4-10 (b) 4th-order voltage-mode OTA-C band-pass filter [16]

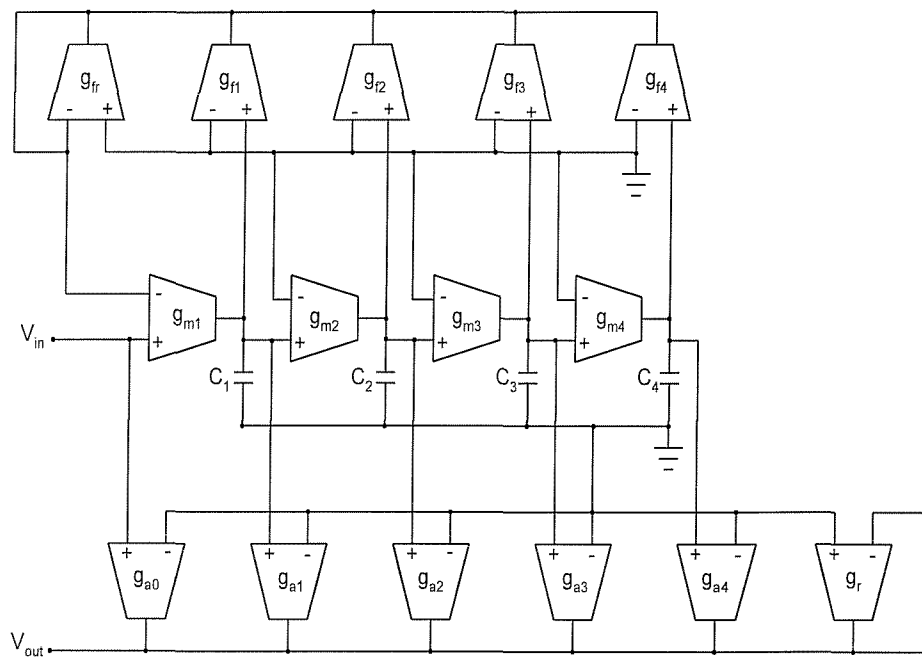


Fig.4-11 (a) 4th-order voltage-mode OTA-C high-pass filter [20]



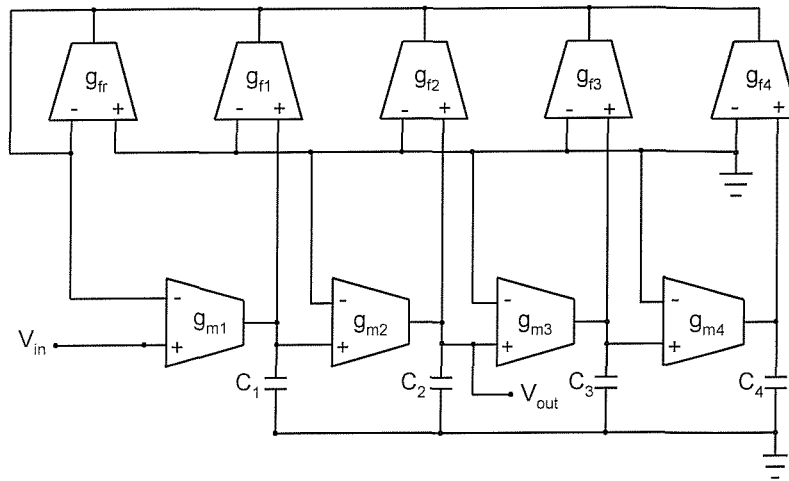


Fig.4-11 (b) 4th-order voltage-mode OTA-C band-pass filter [20]

Table 4-1 Comparison with recently reported nth-order OTA-based filters

Parameter Case	Number of OTAs	Type of OTAs	Number of capacitors	Type of capacitors
4 th -order HP filter in [16]	10	Single-input (6), double-input (4)	4	Grounded
4 th -order HP filter in [20]	15	Single-input (14), double-input (1)	4	Grounded
4 th -order HP filter in Fig.4-1	6	Single-input (6)	4	Grounded
4 th -order BP filter in [16]	8	Single-input (4), double-input (4)	4	Grounded
4 th -order BP filter in [20]	9	Single-input (8), double-input (1)	4	Grounded
4 th -order BP filter in Fig.4-1	6	Single-input (6)	4	Grounded
N th -order general filter in [16]	2n+2	Single-input (n+2), double-input (n)	n	Grounded
N th -order general filter in [20]	3n+3	Single-input (3n+2), double-input (1)	n	Grounded
Proposed nth-order filter in Fig.4-4	2n+2	Single-input (2n+2)	n	Grounded
Proposed nth-order filter in Fig.4-1	n+2	Single-input (n+2)	n	Grounded

Component Spread

Another parameter which needs to be compared when considering different filter structures is the span (or spread) of filter component values which may be large for high-order filters. A comparison with the recently reported filters [16, 20] for the span (or spread) of component values is illustrated by using their 4th-order high-pass transfer functions shown as below.

$$\frac{V_{HP}}{V_{in}} = \frac{g_{b4}s^4 C_4 C_3 C_2 C_1}{\left(g_{a4}s^4 C_4 C_3 C_2 C_1 + g_{a4}g_{a3}s^3 C_3 C_2 C_1 + g_{a4}g_{a3}g_{a2}s^2 C_2 C_1 + g_{a4}g_{a3}g_{a2}g_{a1}s C_1 + g_{a4}g_{a3}g_{a2}g_{a1}g_{a0} \right)} \quad (4-45)$$

$$\frac{V_{HP}}{V_{in}} = \frac{\left[g_{a0}s^4 C_4 C_3 C_2 C_1 + g_{a0}g_{m4}s^3 C_3 C_2 C_1 + g_{m1}g_{a1}s^3 C_3 C_2 C_1 + g_{a0}g_{m4}g_{m3}s^2 C_2 C_1 + g_{m1}s^2 (g_{m4}g_{a1}C_3 C_2 + g_{m2}g_{a2}C_4 C_3) + g_{a0}g_{m4}g_{m3}g_{m2}s C_1 + g_{m1}s (g_{m3}g_{m2}g_{a3}C_4 + g_{m4}g_{m2}g_{a2}C_3 + g_{m4}g_{m3}g_{a1}C_2) + g_{a0}g_{m4}g_{m3}g_{m2}g_{m1} + g_{m1}g_{m2}g_{m3}g_{m4} (g_{a4} + g_{a3} + g_{a2} + g_{a1}) \right]}{\left(g_r s^4 C_4 C_3 C_2 C_1 + g_r g_{m4} s^3 C_3 C_2 C_1 + g_r g_{m4} g_{m3} s^2 C_2 C_1 + g_r g_{m4} g_{m3} g_{m2} s C_1 + g_r g_{m4} g_{m3} g_{m2} g_{m1} \right)} \quad (4-46)$$

$$\frac{V_{HP}}{V_{in}} = \frac{\left[g_{a0}g_{fr}s^4 C_4 C_3 C_2 C_1 + g_{a0}g_{m1}g_{f1}s^3 C_4 C_3 C_2 + g_{a1}g_{m1}g_{fr}s^3 C_4 C_3 C_2 + g_{a0}g_{m1}g_{m2}g_{f2}s^2 C_4 C_3 + g_{a2}g_{m1}g_{m2}g_{fr}s^2 C_4 C_3 + g_{a0}g_{m1}g_{m2}g_{m3}g_{f3}s C_4 + g_{a3}g_{m1}g_{m2}g_{m3}g_{fr}s C_4 + g_{a0}g_{m1}g_{m2}g_{m3}g_{m4}g_{f4} + g_{a4}g_{m1}g_{m2}g_{m3}g_{m4}g_{fr} \right]}{\left(g_r g_{fr} s^4 C_4 C_3 C_2 C_1 + g_r g_{m1} g_{f1} s^3 C_4 C_3 C_2 + g_r g_{m1} g_{m2} g_{f2} s^2 C_4 C_3 + g_r g_{m1} g_{m2} g_{m3} g_{f3} s C_4 + g_r g_{m1} g_{m2} g_{m3} g_{m4} g_{f4} \right)} \quad (4-47)$$

Eqs. (4-45) to (4-47) represent the first high-pass transfer function derived from Fig. 4-1 after the replacement of all the unity transconductances with g_{b4} , g_{a0} , g_{a1} , g_{a2} , g_{a3} and g_{a4} from the right side, and the capacitances a_1/a_0 , a_2/a_1 , a_3/a_2 , and a_4/a_3 with C_1 , C_2 , C_3 , and C_4 , the second one derived from [16], and the third one derived

from [20], respectively. To give insight into what the component span of the new filter structure, shown in Fig. 4-1, is, as an example, we have compared the component span of 4th-order Butterworth high-pass filters, which have the transfer function with the denominator $s^4 + 2.6131259s^3 + 3.4142136s^2 + 2.6131259s + 1$ and the numerator s^4 [84], realised using the circuits in [16], [20] and the filter derived from Fig. 4-1. Assuming equal transconductance design, all filters have the same capacitance span from 0.383 (C_{\min}) to 2.613 (C_{\max}). Similarly assuming equal capacitance design, the transconductance spans are (i) from 0.635 (g_{\min}) to 1.617 (g_{\max}) (the smallest) for the circuit in [20], (ii) from 0.383 to 2.613 (the middle) for the proposed circuit structure (Fig.4-1), and (iii) from 0.383 to 11.657 (the largest) for the circuit in [16]. However, different type and different order of filters lead to different component span. For example, assuming equal capacitance design, the transconductance span for the 4th-order Butterworth low-pass filter in [16] is from 0.383 to 2.613.

Cascadability

For a voltage-mode circuit, high input impedance and low output impedance lead to the attractive feature: cascadability at the input and output ports, respectively (referring to Appendix 2). Due to high input and output impedances of an OTA, both the two voltage-mode filter structures shown in Figs. 4-1 and 4-4 have rather high output impedances and need the voltage buffer to do the connection with the next stage. However, their very high input impedances achieve the advantage: cascadability at their input ports. Closer examination of the two filter structures reveals interesting information. Because the input impedance of the general case (Fig. 4-4) in section 4.2 is equal to $Z_{in}/(n+1)$, where Z_{in} is the input impedance of an OTA and n is the filter order, which is lower than Z_i of the low-pass, band-pass, and high-pass case (Fig. 4-1) in Section 4.2. Therefore, the effect of cascadability of the first filter structure (Fig. 4-1) is much better than that of the second filter structure (Fig. 4-4). Observing both recently reported work [16, 20], they are also with high input and output impedances, namely, both are cascadable at their input ports. We also note that the input impedances of the fourth-order high-pass filters shown in Figs. 4-10(a) [16] and 4-11(a) [20] are $Z_{in}/2$ and $Z_{in}/2$, respectively.

Comparison for Synthesis Method II

Component Count

Fig.4-12 shows how the new filter structure provides 3rd-order all-pass response. It can be seen that the filter has five single-input OTAs and three grounded capacitors. In general the new filter structure, shown in Fig. 4-6, for a given order of n , has $n+2$ single-input OTAs, and n grounded capacitors. Fig.4-13 shows the 3rd-order all-pass filter circuit obtained using the structure in [16]. As can be seen it not only employs double-input and single-input OTAs, but also three more active elements than the circuit (Fig.4-12) obtained using the new structure. Similarly, Fig.4-14 shows the 3rd-order all-pass circuit obtained using the structure in [20]. Again, it can be seen that the circuit (Fig.4-12) obtained using the new structure employs seven less active components than the circuit in Fig.4-14. Table 4-2 shows a comparison in terms of number of OTAs, types of OTAs, number of capacitors and types of capacitors between the proposed filter structure (Fig.4-6), and those recently reported in [16] and [20]. It can be seen that the proposed filter structure (Fig.4-6), which can realize all-pass filters, has the least number of OTAs, $n+2$, compared with $2n+2$ [16] and $3n+3$ [20]. Moreover, the proposed filter structure (Fig.4-6) uses all single-input OTAs unlike those in [16] and [20].

Table 4-2 Comparison with recently reported n th-order OTA-based filters

Parameter Case	Number of OTAs	Type of OTAs	Number of capacitors	Type of capacitors
3 rd -order AP filter in [16]	8	Single-input (6), double-input (4)	3	Grounded
3 rd -order AP filter in [20]	12	Single-input (14), double-input (1)	3	Grounded
3 rd -order AP filter in Fig.4-6	5	Single-input (6)	3	Grounded
Nth-order general filter in [16]	$2n+2$	Single-input ($n+2$), double-input (n)	n	Grounded
Nth-order general filter in [20]	$3n+3$	Single-input ($3n+2$), double-input (1)	n	Grounded
Nth-order AP filter in Fig.4-6	$n+2$	Single-input ($n+2$)	n	Grounded

Component Spread

To give insight into what the component span of the new filter structure is, as an example, we have compared the component span of third-order Butterworth all-pass filters realised using the circuits in [16], [20] and the filter derived from Fig. 4-6. The common transfer functions are given by

$$\frac{V_{out}}{V_{in}} = (\pm 1) \frac{s^3 - 2s^2 + 2s - 1}{s^3 + 2s^2 + 2s + 1} \quad (4-48)$$

The transfer functions of the three third-order OTA-C all-pass filters, shown in Figs. 4-12, 4-13, and 4-14, are presented in Eqs. (4-49), (4-50), and (4-51), respectively.

$$\frac{V_{out}}{V_{in}} = \left(\frac{g_a}{g_b} \right) \frac{-s^3 C_1 C_2 C_3 + s^2 C_1 C_2 g_3 - s C_1 g_2 g_3 + g_1 g_2 g_3}{s^3 C_1 C_2 C_3 + s^2 C_1 C_2 g_3 + s C_1 g_2 g_3 + g_1 g_2 g_3} \quad (4-49)$$

$$\frac{V_{out}}{V_{in}} = \frac{\left[\begin{aligned} &(g_{a0})(s^3 C_1 C_2 C_3 + s^2 C_1 C_2 g_{m3} + s C_1 g_{m2} g_{m3} + g_{m1} g_{m2} g_{m3}) \\ &+ (g_{m1} g_{a1})(s^2 C_2 C_3 + s C_2 g_{m3} + g_{m2} g_{m3}) + \\ &(g_{m1} g_{a2})(s C_3 g_{m2} + g_{m2} g_{m3}) + g_{a3} g_{m1} g_{m2} g_{m3} \end{aligned} \right]}{(g_r)[s^3 C_1 C_2 C_3 + s^2 C_1 C_2 g_{m3} + s C_1 g_{m2} g_{m3} + g_{m1} g_{m2} g_{m3}]} \quad (4-50)$$

$$\frac{V_{out}}{V_{in}} = \frac{\left[\begin{aligned} &(g_{a0} g_{fr})(s^3 C_1 C_2 C_3) + (g_{a0} g_1)(s^2 C_2 C_3 g_{f1} + s C_3 g_2 g_{f2} + g_2 g_3 g_m) \\ &+ (g_1 g_{fr})(s^2 C_2 C_3 g_{a1}) + s C_3 g_1 g_{fr} g_2 g_{a2} + g_{a3} g_1 g_{fr} g_2 g_3 \end{aligned} \right]}{(g_{ar})[(g_{fr})s^3 C_1 C_2 C_3 + (g_1)(s^2 C_2 C_3 g_{f1} + s C_3 g_2 g_{f2} + g_2 g_3 g_m)]} \quad (4-51)$$

If we give equal transconductance in the denominators of the three transfer functions shown in Eqs. (4-49), (4-50), and (4-51), then all filters have the same capacitance span from 0.5 (C_{min}) to 2 (C_{max}) and the transconductance spans in the numerators are (i) from 1 (g_{min}) to 1 (g_{max}) (the smallest) for the proposed circuit structure (Fig.4-12), (ii) from 1 to 16 (the largest) for the circuit structure (Fig. 4-13), and (iii) from 1 to 2 (the middle) for the circuit structure (Fig. 4-14). If we give equal capacitance design, then the transconductance spans are (i) from 0.5 (g_{min}) to 2 (g_{max}) (the middle) for the proposed circuit structure (Fig.4-12), (ii) from 0.5 to 16 (the largest) for the circuit

structure (Fig. 4-13), and (iii) from 0.5946 to 2.1213 (the smallest) for the circuit structure (Fig. 4-14).

Cascadability

For a voltage-mode circuit, high input impedance and low output impedance lead to the attractive feature: cascadability at the input and output ports, respectively (referring to Appendix 2). Due to high input and output impedances of an OTA, the third voltage-mode filter structure shown in Fig. 4-12 has rather high output impedances and need the voltage buffer to do the connection with the next stage. However, its very high input impedances achieve the advantage: cascadability at the input port. Observing both recently reported work [16, 20], they are also with high input and output impedances, namely, both are cascadable at their input ports. We also note that the input impedances of the third-order all-pass filters shown in Figs. 4-12, 4-13 [16] and 4-14 [20] are Z_{in} (the highest), $Z_{in}/2$ and $Z_{in}/2$, respectively.

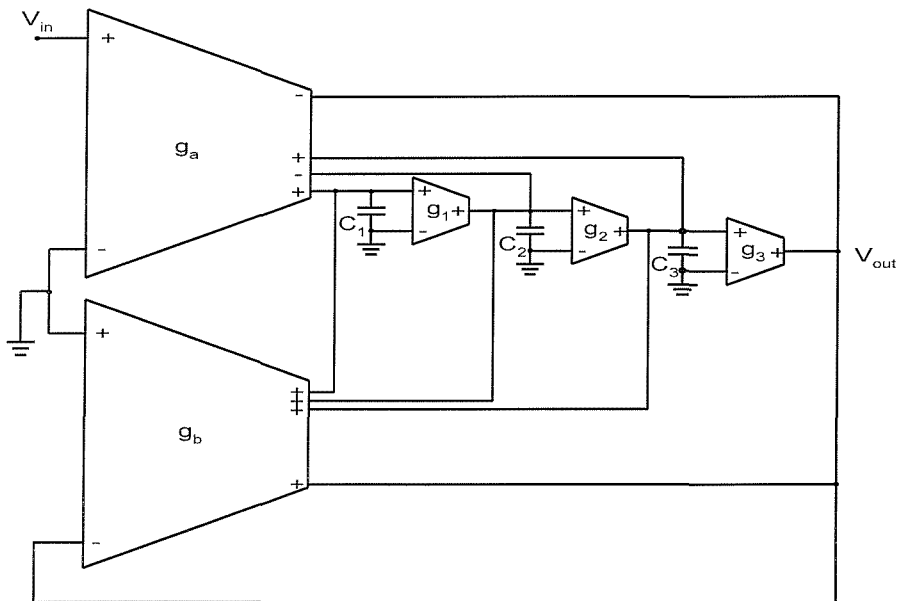


Fig. 4-12 Third-order OTA-C all-pass filter derived from Fig. 4-6

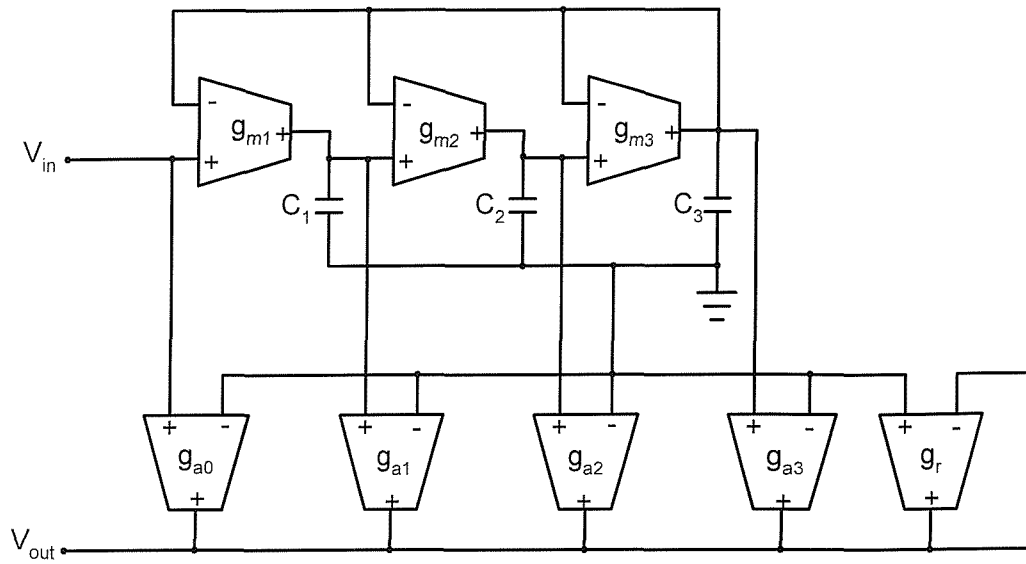


Fig. 4-13 Third-order OTA-C all-pass filter [16]

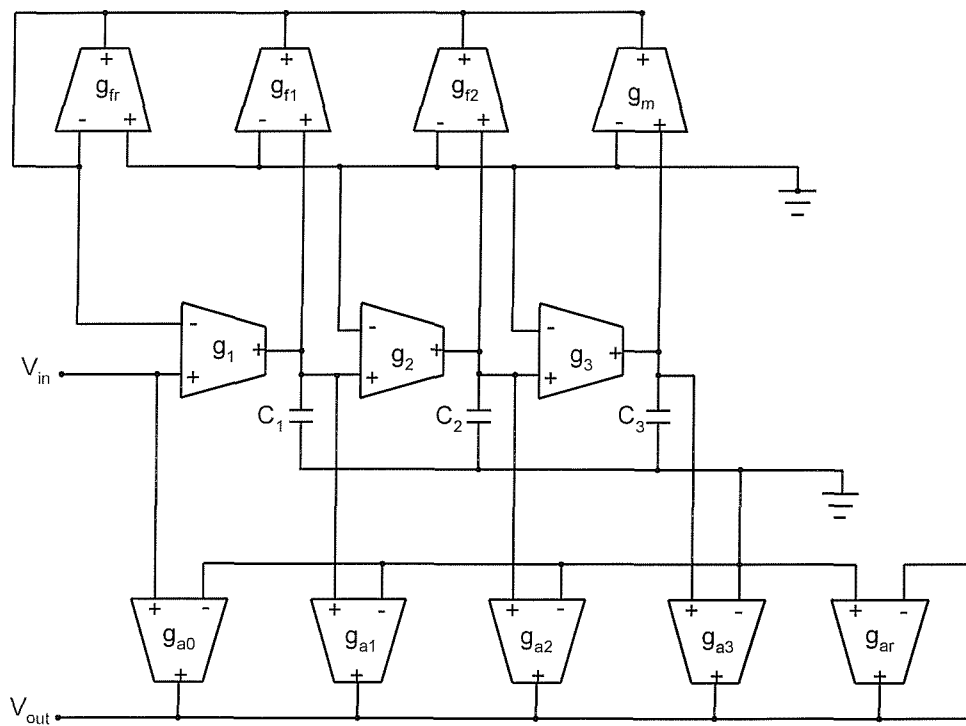


Fig. 4-14 Third-order OTA-C all-pass filter [20]

4.6 Simulation Results

To verify the theoretical analysis of the proposed filter structure shown in Fig.4-1, a third-order low-pass and high-pass OTA-C filter has been simulated using H-Spice with the UMC05 level-49 parameters, the CMOS implementations, described in Section 2.2, and the component values: (i) each $g=56\mu\text{S}$ ($I_{abc}=8.852\mu\text{A}$), $C_1=18\text{pF}$, $C_2=9\text{pF}$, and $C_3=4.5\text{pF}$ for the responses with $f_o=0.990\text{MHz}$, and (ii) each $g=62.8\mu\text{S}$ ($I_{abc}=10.495\mu\text{A}$), $C_1=10\text{pF}$, $C_2=5\text{pF}$, and $C_3=2.5\text{pF}$ for the responses with $f_o=1.999\text{MHz}$. Fig. 4-15 shows the simulated low-pass and high-pass responses of the filter. As can be seen there is a close agreement between theory and simulation, for example, the simulated 3dB frequencies are 0.94MHz (high-pass) and 1.04MHz (low-pass), compared to 0.990MHz in the ideal case, and 1.83MHz (high-pass) and 2.02MHz (low-pass), compared to 1.999MHz in the ideal case.

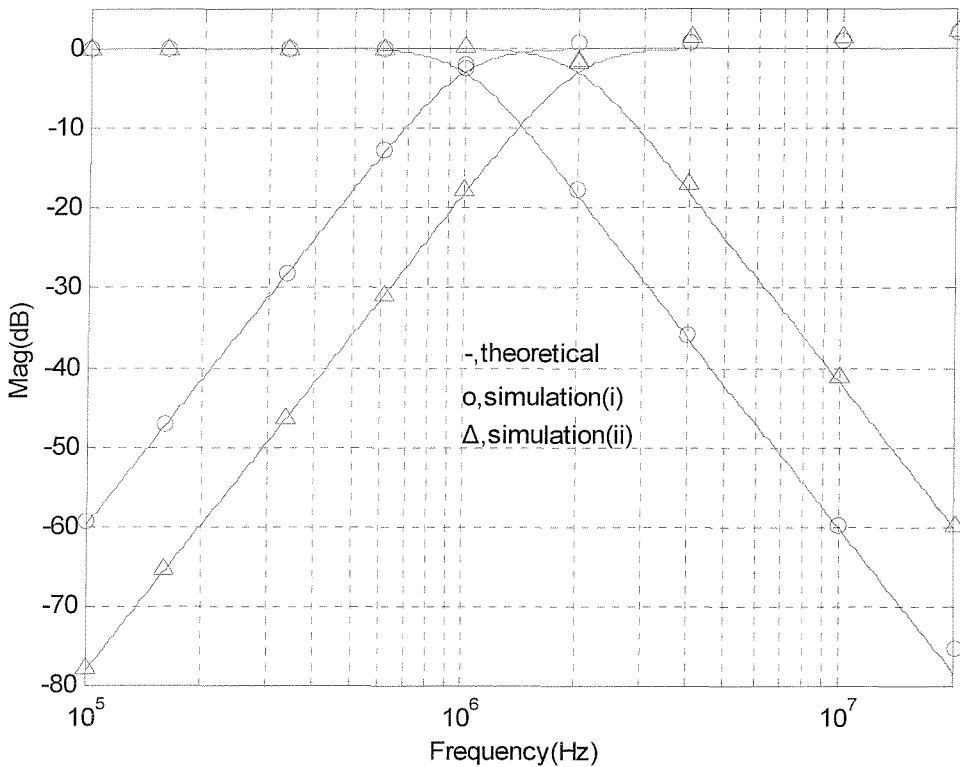


Fig.4-15 LP and HP amplitude-frequency responses of the third-order filter

The other simulation is carried out for the fourth-order OTA-C all-pass filter shown in Fig. 4-12. The simulations use the same H-Spice with the same CMOS implementations as those of the low-pass and high-pass simulations in this section. The

component values are given by each $g=157\mu\text{S}$, $C_1=32.5\text{pF}$, $C_2=16.25\text{pF}$, $C_3=9.53\text{pF}$, and $C_4=4.75\text{pF}$. The fourth-order all-pass simulation results are shown in Figs. 4-16 (a) and (b), respectively. As can be seen, there is a close agreement between theory and simulation, for example, the simulated resonance angular frequency is 1.98MHz, compared to 2MHz in the ideal case, and the simulated peak value is 2.923dB, compared to 0dB in the ideal case.

To examine the voltages and currents in the internal nodes and branches of the filter structure, the second-order OTA-C high-pass and all-pass filters shown in Fig. 4-17 and 4-18 has been simulated. The given component values are $164\mu\text{S}$ for every g , $C_0=36.9\text{pF}$, and $C_1=18.45\text{pF}$. All the curves have limited ranges, for example, the curves shown in Figs. 4-19 and 4-20, which confirm the feasibility of the new filter structure. Their rather low noise simulation results of Fogs. 4-17 and 4-18 are shown in Figs. 4-21 and 4-22 in which the maximum noise magnitudes are 47.5nV and 45nV, compared to 1V output voltage.

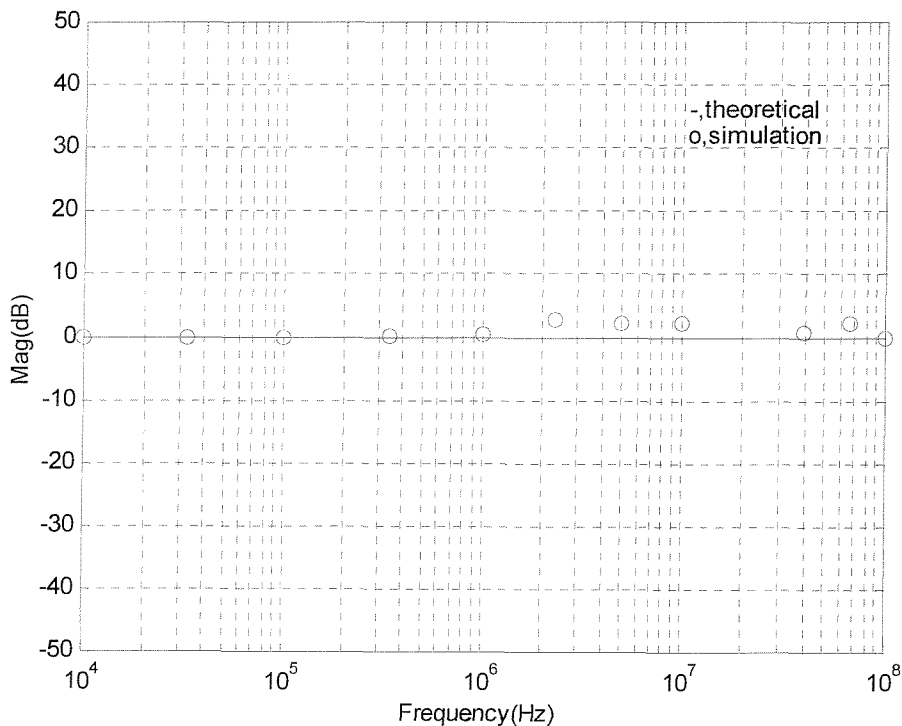


Fig. 4-16 (a) Amplitude-frequency response of the 3rd-order all-pass filter

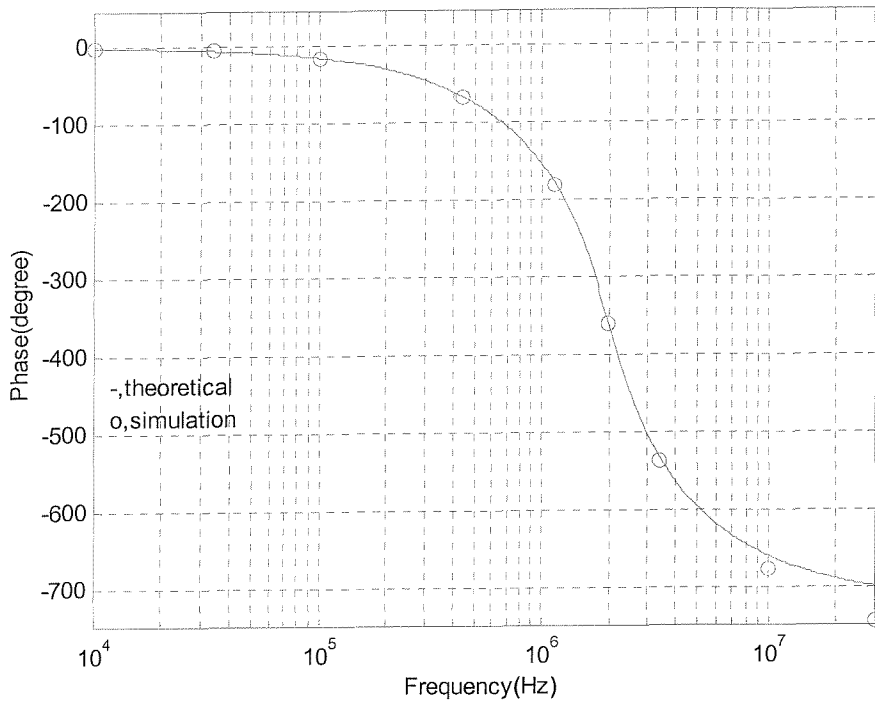


Fig. 4-16 (b) Phase-frequency response of the 3rd-order all-pass filter

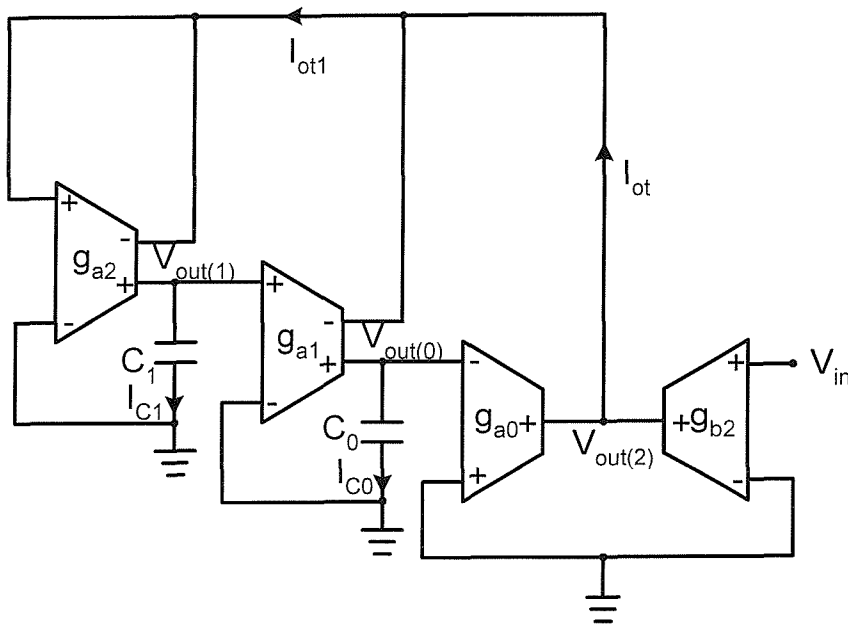


Fig. 4-17 2nd-order OTA-C high-pass filter derived from Fig.4-1

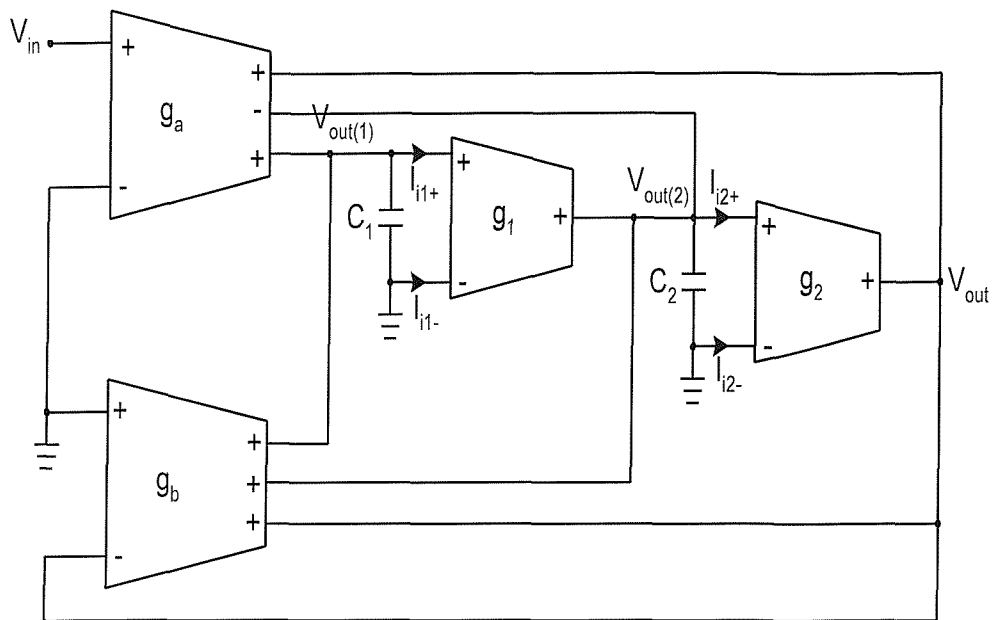


Fig. 4-18 2nd-order OTA-C all-pass filter derived from Fig.4-6

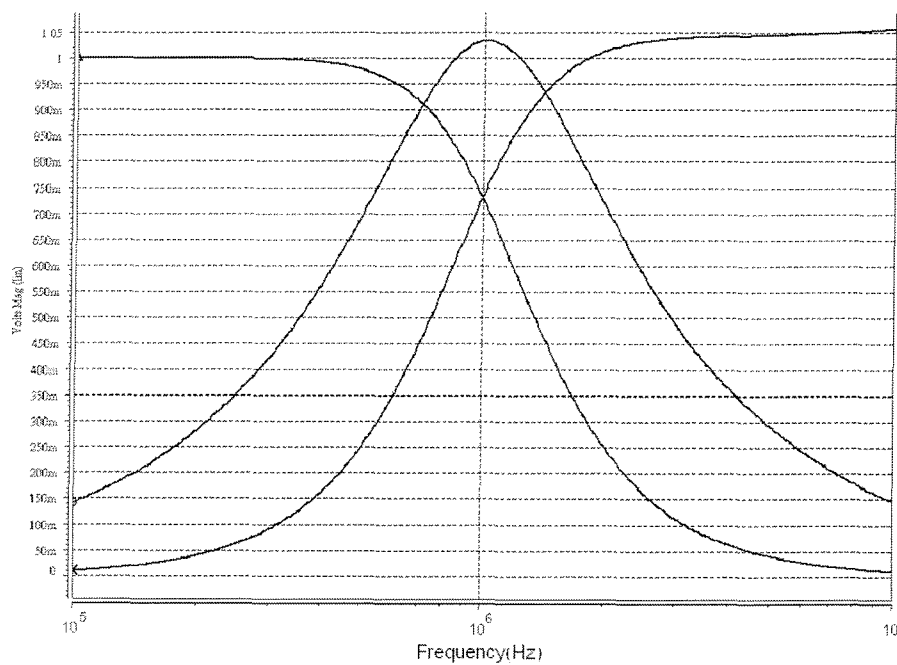


Fig. 4-19 (a) Amplitude-frequency responses of node voltages, $V_{out(2)}$ (high-pass), $V_{out(1)}$ (band-pass), and $V_{out(0)}$ (low-pass)

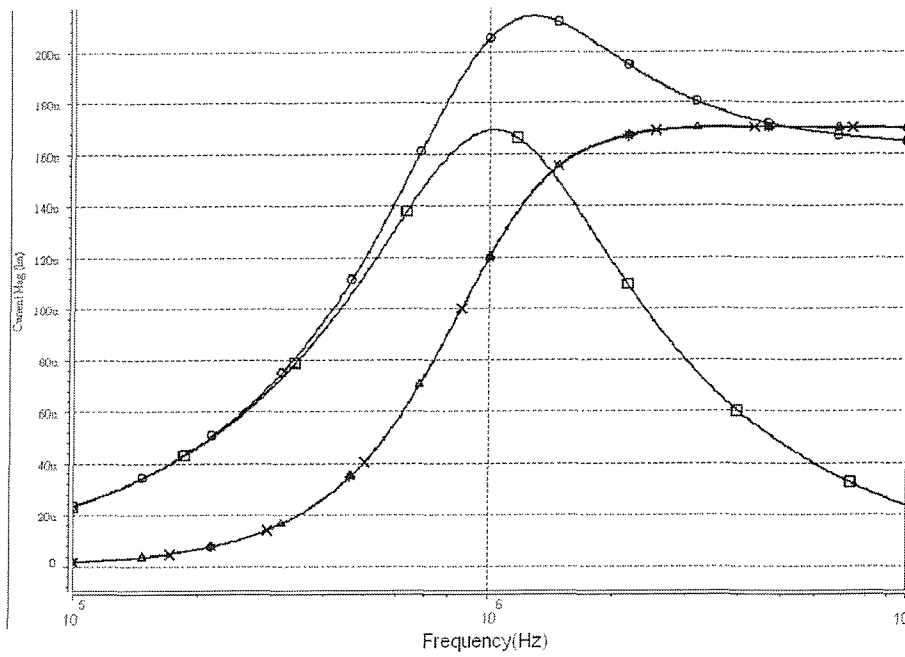


Fig. 4-19 (b) Amplitude-frequency responses of branch currents, I_{ot} (o), I_{ot1} (Δ), I_{co} (\square), and I_{cl} (*)

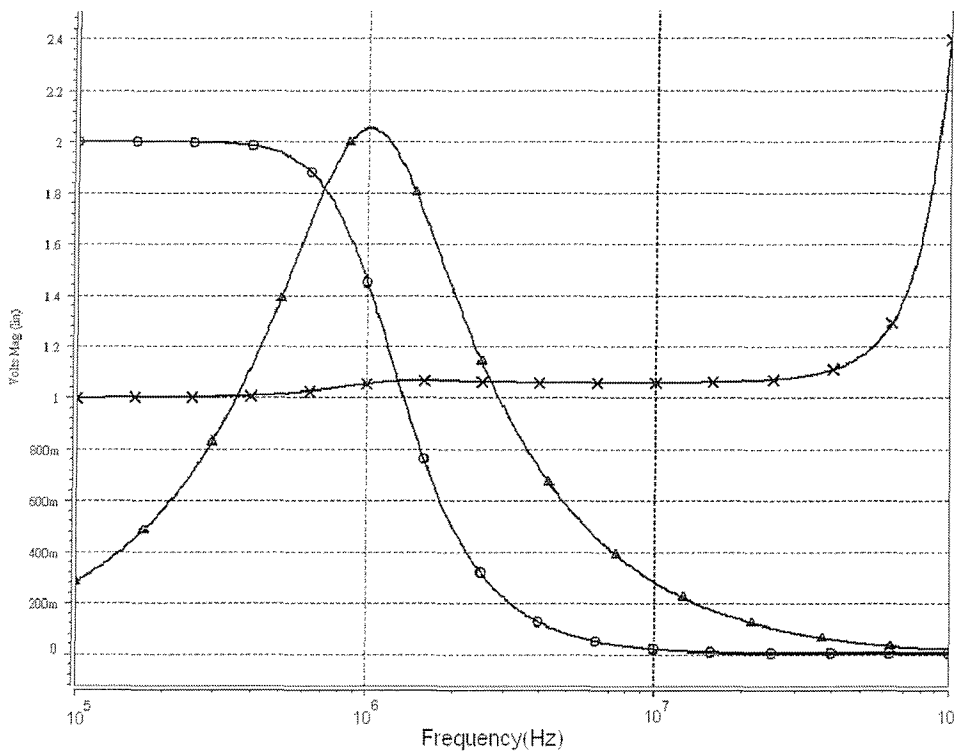


Fig. 4-20 (a) Amplitude-frequency responses of node voltages, V_{out} (x), $V_{out(1)}$ (o), and $V_{out(2)}$ (Δ)

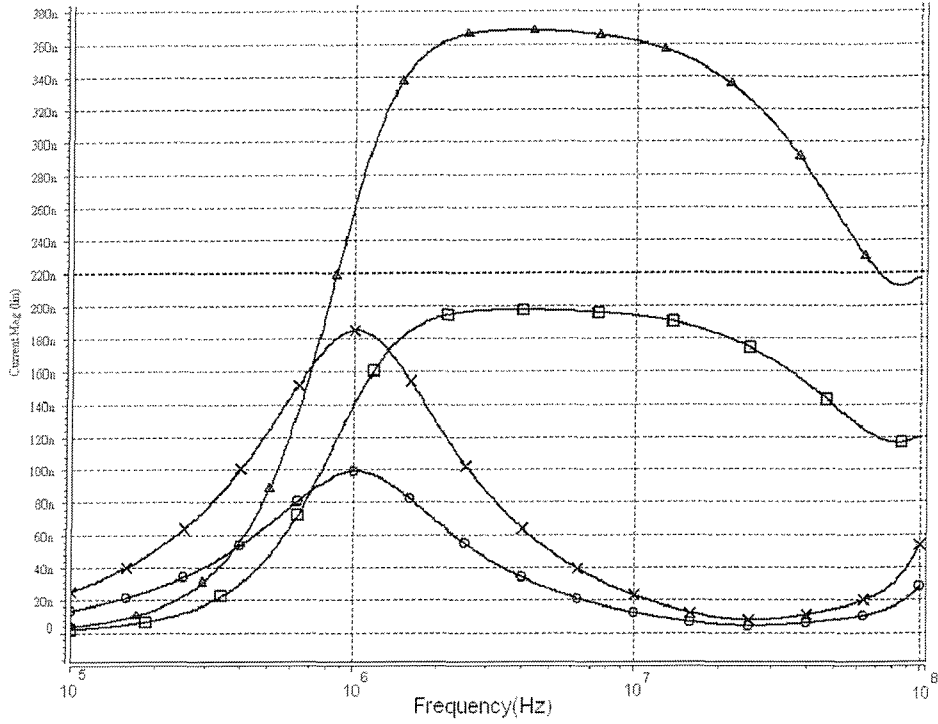


Fig. 4-20 (b) Amplitude-frequency responses of branch currents, I_{i1+} (x), I_{i1-} (o), I_{i2+} (Δ), and I_{i2-} (□)

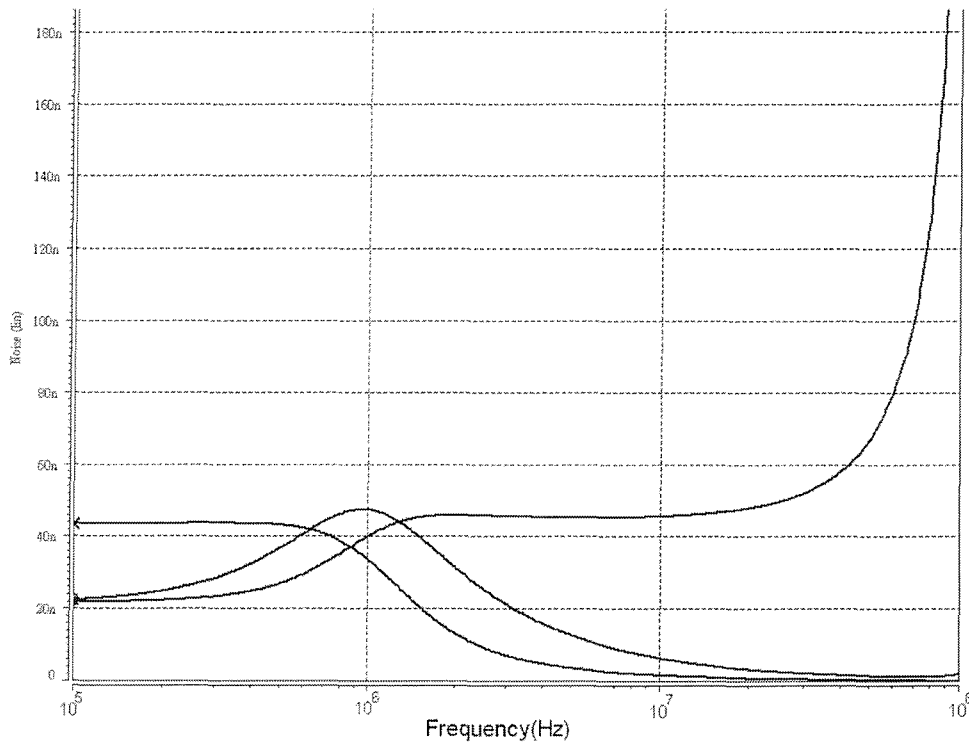


Fig. 4-21 Noise simulation results: amplitude-frequency responses of node voltages, $V_{out(2)}$ (high-pass), $V_{out(1)}$ (band-pass), and $V_{out(0)}$ (low-pass) of Fig. 4-17

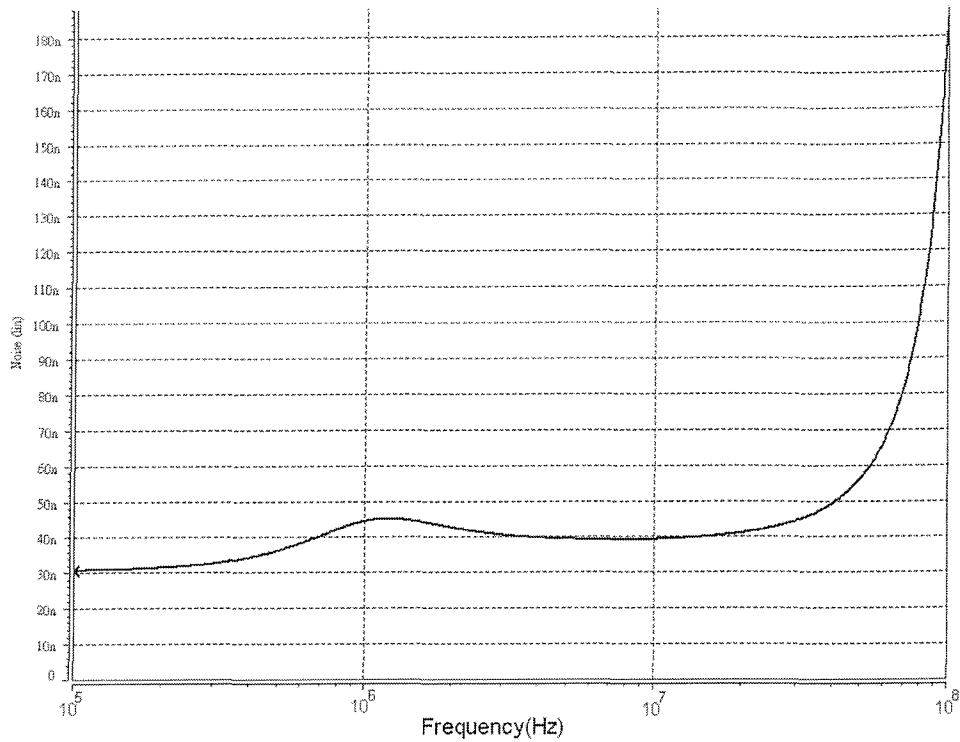


Fig. 4-22 Noise simulation results: amplitude-frequency responses of Fig. 4-18

4.7 Concluding Remarks

This chapter has presented two new analytical synthesis methods and three new voltage-mode high-order filter structures, shown in Figs. 4-1, 4-4, and 4-6, that employ only single-input OTAs and grounded capacitors, features known to be attractive for practical applications [13]. It has been shown how to algebraically decompose an n th-order voltage transfer function into $n+1$ simple transfer functions realizable by using OTA-C circuits. The first synthesis method realizes the first filter structure, Fig. 4-1, employs only $n+2$ OTAs much fewer than the recently reported work and offers simultaneous multiple outputs. It is needed to be noticed that the equal transconductance characteristic makes the benefit: use of single biasing circuitry and easy control. Adding input distribution to every node of the first filter structure leads to the second filter structure, Fig. 4-4, with the minimum components, $2n+2$ single-input OTAs, and n grounded capacitors which can realize any kind of voltage transfer functions for example, elliptic filter functions. Equal capacitance design of the second filter structure, Fig. 4-4, achieves the precise result of IC fabrication without the need to

adjust the different values of capacitors in discrete steps [86]. The second analytical synthesis method gives a new n th-order OTA-C all-pass filter (Fig. 4-6) employing only $n+2$ single-input OTAs, and n grounded capacitors, far simpler in circuit structure than the recently reported filters.

Chapter 5

Unified Biquad Filters

It has been well-known that a high-order filter can be realized using several biquadratic filters in cascade. The main benefits of cascade approach are (i) much easier in design, and (ii) independently tunable in control of the quality factor and resonant angular frequency. Chapters 3 and 4 have presented current-mode and voltage-mode high-order filter synthesis methods. This chapter is devoted to the biquadratic filter structures.

One new biquad filter model is presented in this chapter based on nullators, norators, current mirrors and passive R (resistor) and C (capacitor) elements. Two implementations derived from the new biquad filter model by using second generation current-controlled conveyors (CCCIIs) and operational transconductance amplifiers (OTAs) are also proposed. The two biquad implementations are capable of achieving the *five performance parameters*, described in Chapter 1, simultaneously and without trade-offs unlike recently reported filter structures which make certain trade-offs that emphasize some parameters at the cost of others. A unified biquad filter is defined as the biquad achieving the *five performance parameters*, described in Chapter 1, simultaneously.

Before the new biquad filter is introduced, Section 5.1 provides literature review and motivation. A new RC-nullor biquad filter model is presented in Section 5.2. Two unified CCCII-based and OTA-based implementations transformed from the new biquad filter model are proposed in Sections 5.3 and 5.4, respectively. Section 5.5 gives the simulation results to validate the realizations.

5.1 Literature Review and Motivation

Although the literature review of the CCII-based filters has been done in Section 2.6, the new active element, second-generation current-controlled conveyor (CCCII) [61-62], improved from the CCII, hasn't been introduced and reviewed. Section 5.1 will do it first and leads to the motivation of this Chapter.

In 1996, Fabre et al. identified that the intrinsic resistance R_x at the terminal X of a CCII can be controlled by varying its bias current [61-62]. A new electronically tunable CCII was proposed.

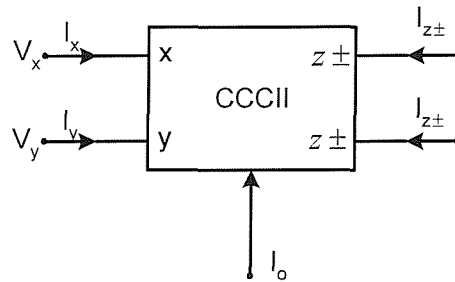


Fig. 5-1 CCCII functional block

Fig. 5-1 shows the functional block of the dual-output CCCII whose input-output relationship is

$$\begin{bmatrix} I_y \\ I_{z\pm} \\ V_x \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm 1 & 0 & 0 \\ R_x & 1 & 0 \end{bmatrix} \begin{bmatrix} I_x \\ V_y \\ V_z \end{bmatrix} \quad (5-1)$$

where R_x is a finite input resistance at the X-terminal of the CCCII and is given by (i) $V_T/2I_o$ for a bipolar implementation [61-62], where V_T is the thermal voltage and I_o is the bias current of the CCCII, or (ii) the relationship with I_o shown in Fig. 5-2 (c) under $\pm 2.5V$ supply voltages and $W/L=5\mu/1\mu$ and $10\mu/1\mu$ for NMOS transistors and PMOS transistors, respectively, for a CMOS implementation (shown in Figs. 5-2 (a) and (b)).

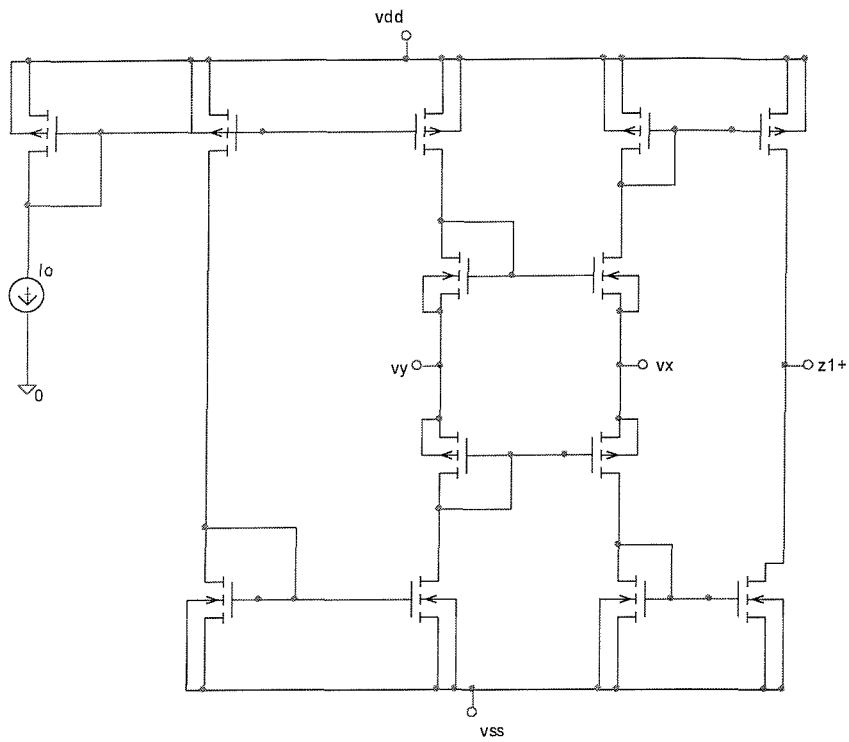


Fig. 5-2 (a) CMOS implementation of a plus-type CCCII

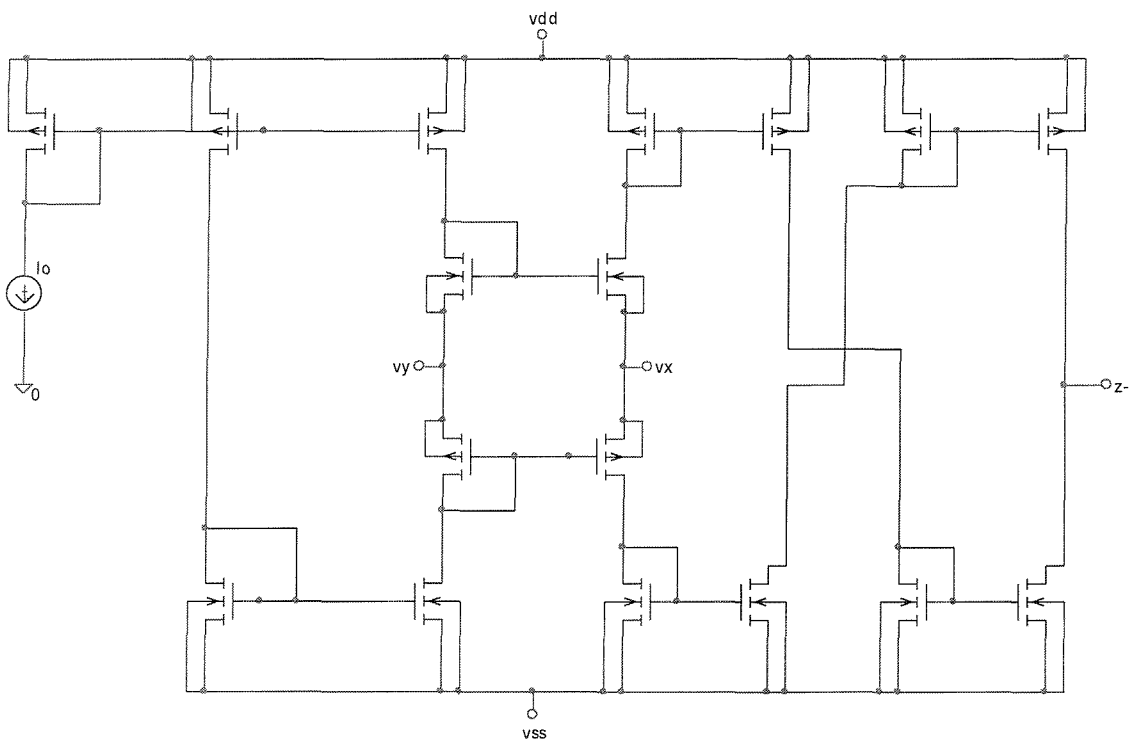


Fig. 5-2 (b) CMOS implementation of a minus-type CCCII

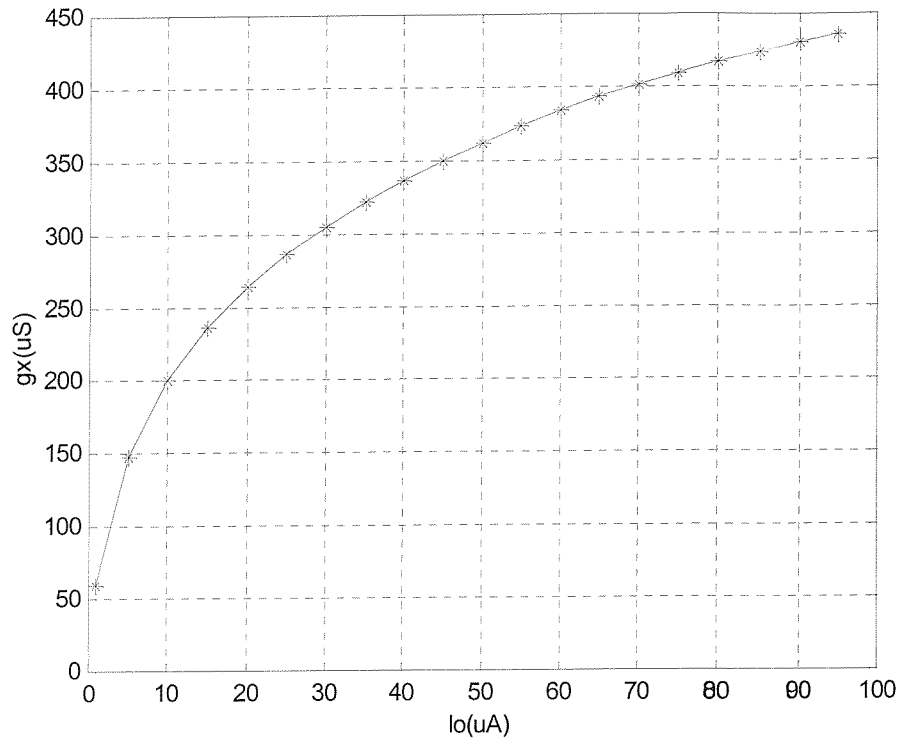


Fig. 5-2 (c) Relationship between $G_x (=1/R_x)$ and I_o for the CMOS CCCII [61-62]

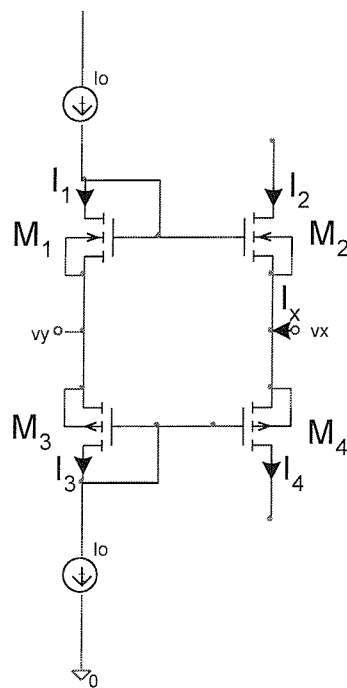


Fig. 5-3 Translinear loop in the CMOS implementation of a CCCII

The core theory of the CMOS implementation of a CCCII is relevant to the translinear loop shown in Fig. 5-3. The detail relationship between the intrinsic resistance R_x and the voltage difference, $V_x - V_y$, is derived as follows.

Suppose that M_1 and M_2 are the same and M_3 and M_4 are the same, which imply

$$k_1 = k_2 = k_{1,2}, \quad k_3 = k_4 = k_{3,4}, \quad V_{T1} = V_{T2}, \quad V_{T3} = V_{T4}, \quad V_{GS1} = V_{GS2}, \quad \text{and} \quad V_{GS3} = V_{GS4}.$$

$$\text{These lead to } I_{D1} = k_1 (V_{GS1} - V_T)^2 = k_2 (V_{GS2} - V_T)^2 = I_{D2},$$

$$\text{and } I_{D3} = k_3 (V_{GS3} - V_T)^2 = k_4 (V_{GS4} - V_T)^2 = I_{D4}.$$

$$\text{Then, we obtain } I_{D1} I_{D3} = I_{D2} I_{D4}. \quad (5-2)$$

$$\text{Because } I_{D1} = I_{D3} = I_o, \text{ Eq. (5-2) becomes } I_o^2 = I_{D2} (I_{D2} + I_x). \quad (5-3)$$

I_{D2} is solved as follows provided that $2I_o > I_x$.

$$\begin{aligned} I_{D2} &= \frac{-I_x + \sqrt{I_x^2 + 4I_o^2}}{2} \\ &\cong \left(\frac{1}{2}\right) \left[-I_x + (4I_o^2)^{1/2} + \left(\frac{1}{2}\right) (4I_o^2)^{-1/2} (I_x^2) \right] = I_o - \frac{I_x}{2} + \frac{I_x^2}{8I_o} \end{aligned} \quad (5-4)$$

And,

$$\begin{aligned} V_x - V_y \cong V &= -V_{GS2} + V_{GS1} = -\left(\sqrt{\frac{I_{D2}}{k_2}} + V_T\right) + \left(\sqrt{\frac{I_{D1}}{k_1}} + V_T\right) \\ &= \sqrt{\frac{1}{k_{1,2}}} (\sqrt{I_o} - \sqrt{I_{D2}}) \cong \sqrt{\frac{1}{k_{1,2}}} \left(\sqrt{I_o} - \sqrt{I_o - \frac{I_x}{2} + \frac{I_x^2}{8I_o}} \right) \\ &\cong \sqrt{\frac{1}{k_{1,2}}} \left[(I_o^{1/2}) - (I_o^{1/2}) - \left(\frac{1}{2}\right) (I_o^{-1/2}) \left(-\frac{I_x}{2} + \frac{I_x^2}{8I_o} \right) \right] = \frac{I_x}{4\sqrt{k_{1,2}I_o}} \left(1 - \frac{I_x}{4I_o} \right) \end{aligned} \quad (5-5)$$

$$\text{Let } V_x - V_y = V = R_x I_x. \quad G_x = 1/R_x = \frac{4\sqrt{k_{1,2}I_o}}{\left(1 - \frac{I_x}{4I_o}\right)} \cong 4\sqrt{k_{1,2}I_o} \left(1 + \frac{I_x}{4I_o} \right) \quad (5-6)$$

The term $\left(1 + \frac{I_x}{4I_o}\right)$ causes the nonlinear distortion for large signal inputs. Note that the magnitude of G_x shown in Eq. (5-6) is a little bit larger than double of the value of g , the transconductance of an OTA, where $g = 2\sqrt{kI}\left(1 - \frac{kV^2}{8I}\right)$, shown in Eq. (2-9).

Examination of the literature on analogue filters shows that no unified filter biquads based on CCCII or OTA has yet been published. Firstly, we consider recently reported CCCII filters that make certain trade-offs with reference to the above five performance parameters. For example, the filter in [63], shown in Fig. 5-4, has features (ii) and (iv) but none of the other features, this is because it has non-independent ω_o and Q tuning, it cannot realize notch and all-pass functions; and three additional current conveyors are needed to sense and provide explicit current outputs of the filter functions. The filter reported in [64], shown in Fig. 5-5, has features (i), (ii) and (iii), but not features (iv), and (v) since to obtain an all-pass filter, it is necessary to place the following condition on component choice: $R_{x2}=2R_{x1}=2R_{x3}$. Furthermore, to obtain high-pass, notch, and all-pass functions, an additional current conveyor is needed to sense the output current of the high-pass filter. The filter reported in [65], shown in Fig. 5-6, has features (ii), (iii), and (iv) but not features (i), and (v). This is because it cannot realize notch and all-pass functions and it needs three additional current conveyors to sense and provide explicit current outputs of the filter functions. The filter proposed in [66], shown in Fig. 5-7, has features (i), (iii), and (v) but not features (ii) and (iv) since it employs four CCCIIs, one CCII, and three grounded capacitors, and it needs the component choice condition: $C_1=C_3$ to obtain an all-pass filter function. A summary of the performance parameters of the filter reported in [66], and some recently reported filters are given in Table.5-1. As can be seen, none of the filters are capable of achieving the five performance parameters simultaneously.

Table 5-1 Performance parameters of recently reported CCCII based filters

Case \ Parameter	(i)	(ii)	(iii)	(iv)	(v)
[63]	Yes	Yes	Yes	No	No
[64]	Yes	Yes	Yes	No	No

[65]	Yes	Yes	Yes	Yes	No
[66]	Yes	No	Yes	No	Yes

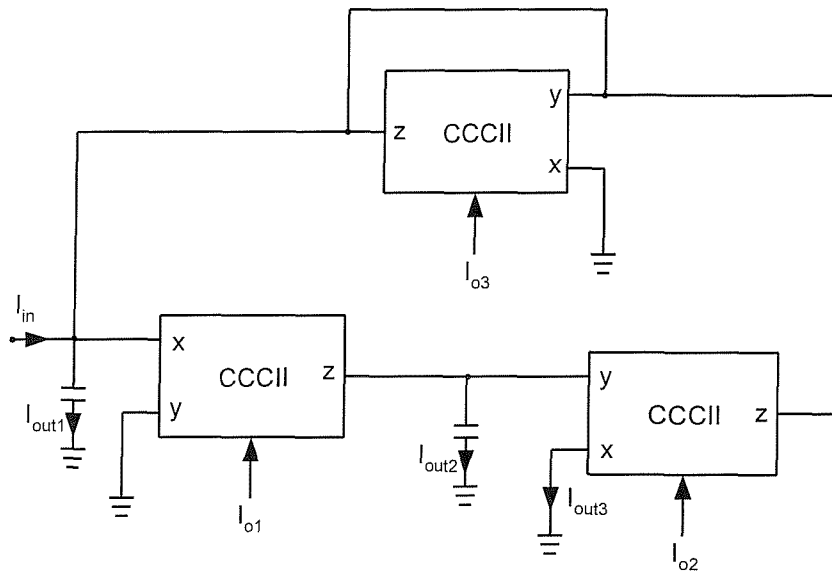


Fig. 5-4 Multifunctional CCCII-C biquad [63]

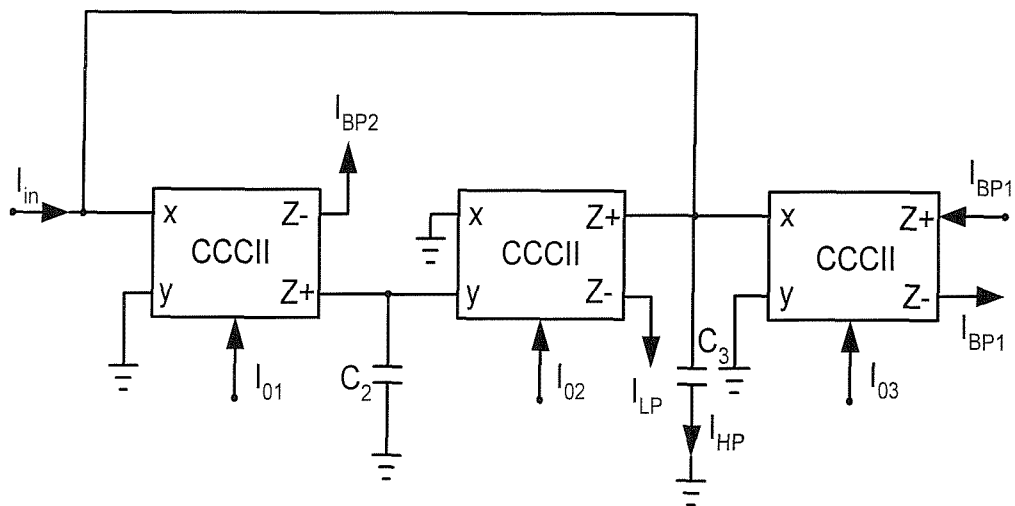


Fig. 5-5 Multifunctional CCCII-C biquad [64]

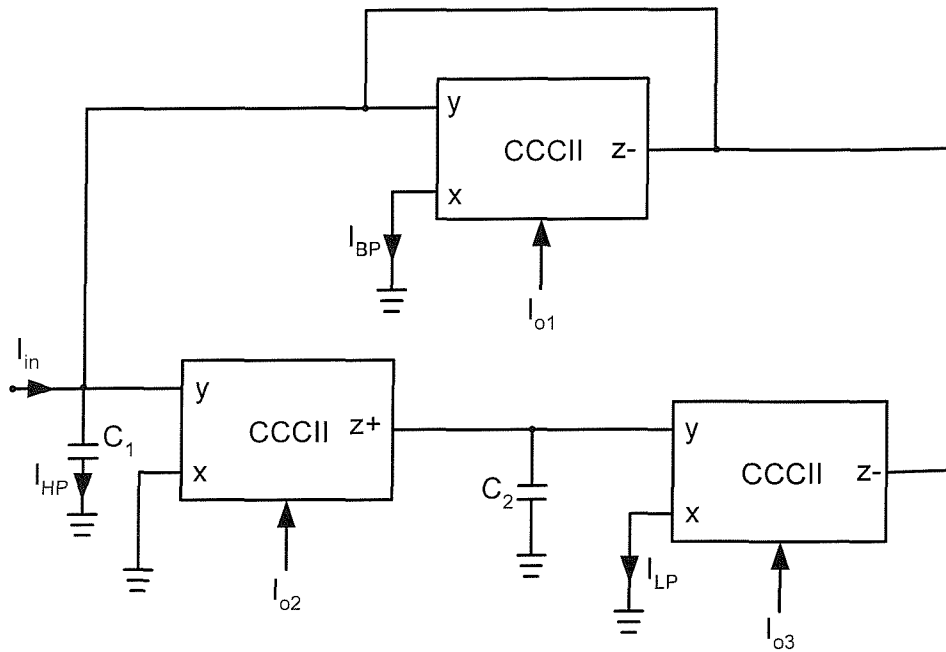


Fig. 5-6 Multifunctional CCCII-C biquad [65]

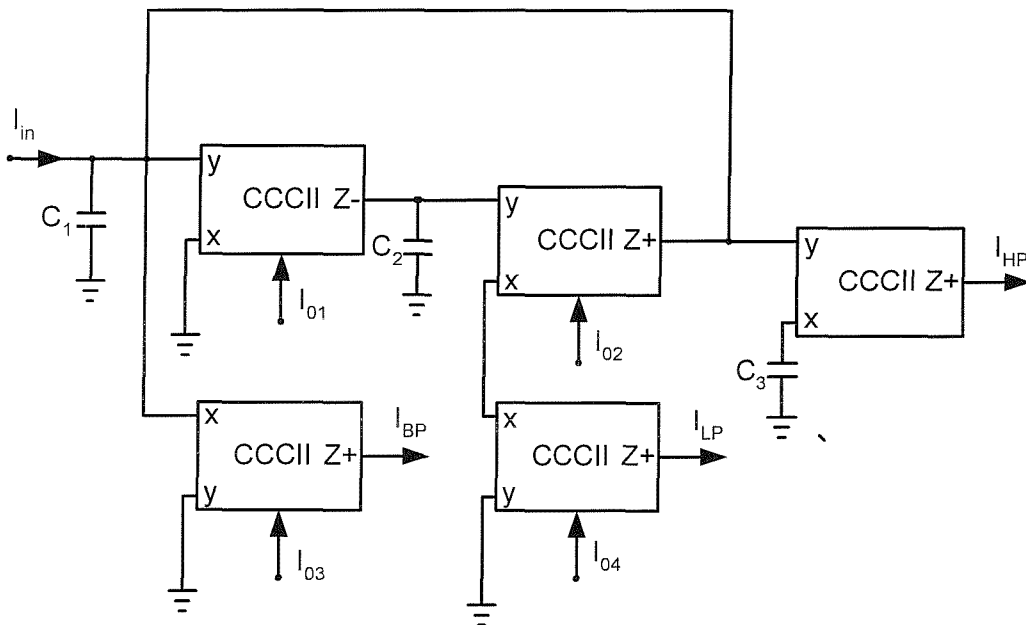


Fig. 5-7 Multifunctional CCCII-C biquad [66]

Secondly, we consider recently reported OTA based filter biquads that also make trade-offs with respect to the above five features. Examination of the literature on OTA filters shows that no single filter capable of simultaneously achieving all the above features has yet been published. Recently reported OTA filters make certain trade-offs and emphasise some aspects at the cost of others. For example, the filter in [22], shown in Fig. 5-8, has features (i) and (v) but none of the other features, this is because it uses four OTAs in addition to two grounded capacitors, it has non-independent ω_o and Q tuning, and it realizes notch and all-pass functions with several component choice conditions. The filters reported in [23], shown in Figs. 5-9 and 5-10, have the same features as those in [22] but one more feature (iii) because they have independent ω_o and Q tuning. In [24], the presented current-mode biquad, shown in Fig. 5-11, meets features (i) and (v) but not features (ii) (using one floating capacitor), (iii), and (iv) (using one matching condition). The filters reported in [25], shown in Fig. 5-12, and [26], shown in Fig. 5-12, have features (i), (ii), (iv), and (v) but not feature (iii). A summary of the performance parameters of the filter reported in [24], and some recently reported filters are given in Table.5-2. As can be seen, none of the filters are capable of achieving the five performance parameters simultaneously.

Table 5-2 Performance parameters of recently reported OTA-based filters

Case \ Parameter	(i)	(ii)	(iii)	(iv)	(v)
[22]	Yes	No	No	No	Yes
Filters 4(a) and 5(a) [23]	Yes	No	Yes	No	Yes
[24]	Yes	No	No	No	Yes
Filter 4 [25]	Yes	Yes	No	Yes	Yes
[26]	Yes	Yes	No	Yes	Yes

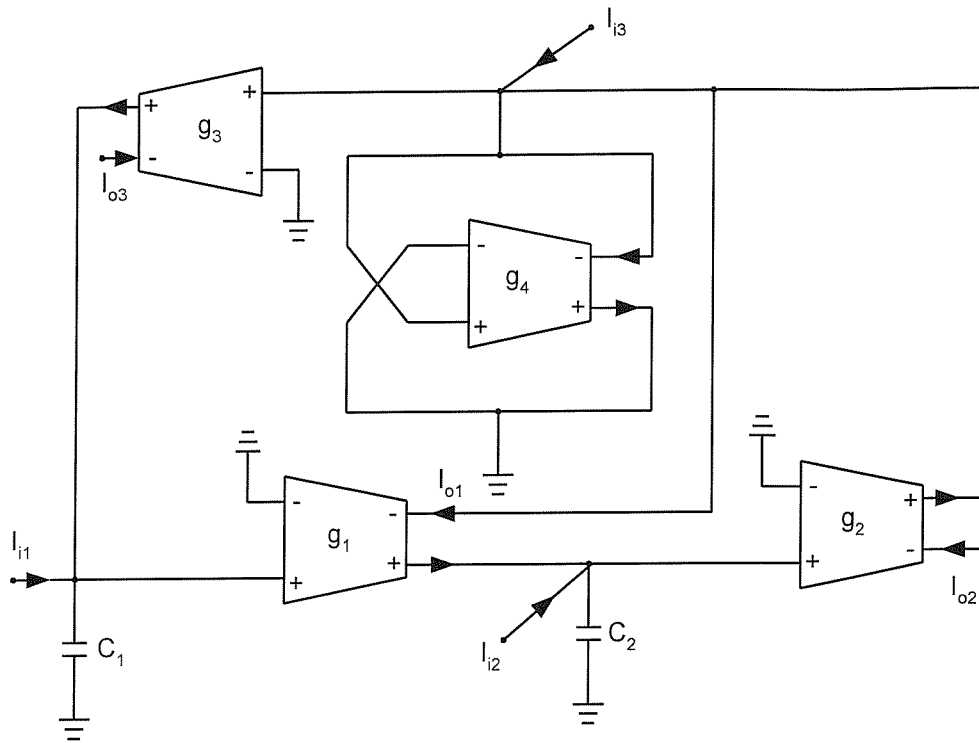


Fig. 5-8 Multifunctional OTA-C biquad [22]

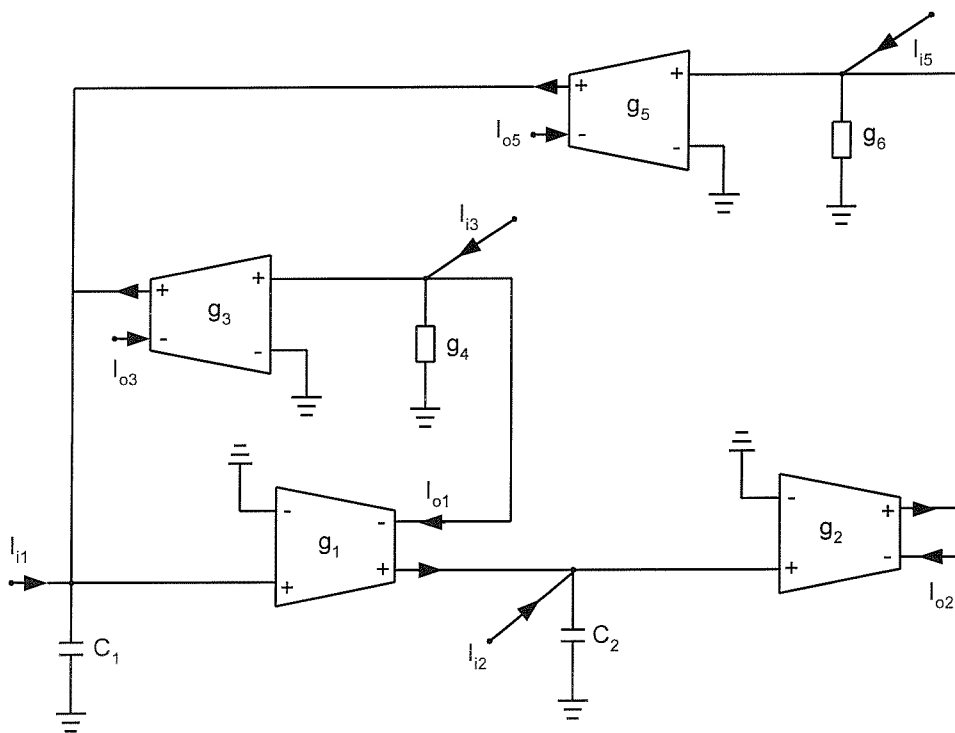


Fig. 5-9 Multifunctional OTA-C biquad [23-4(a)]

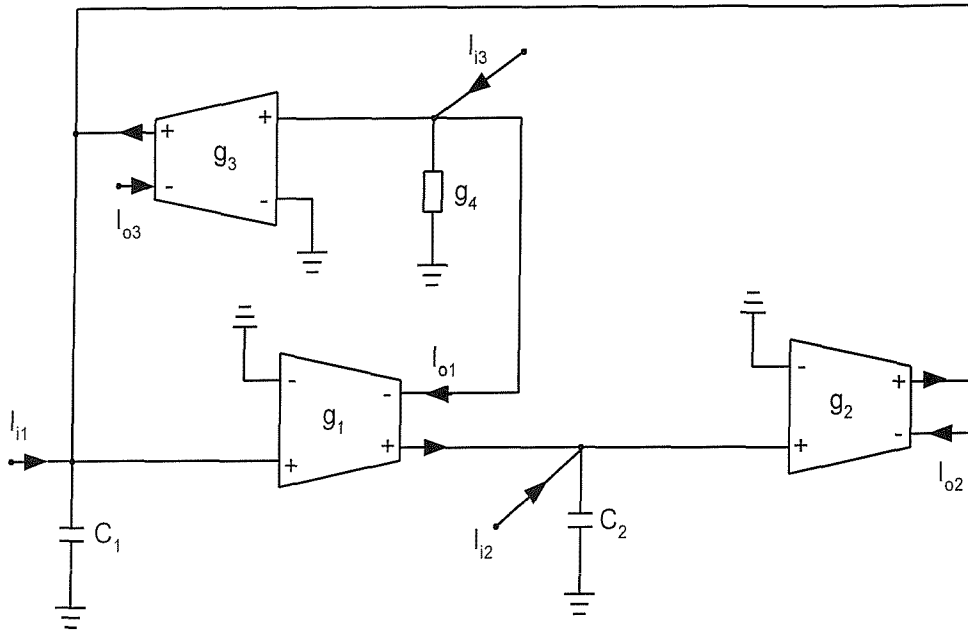


Fig. 5-10 Multifunctional OTA-C biquad [23-5(a)]

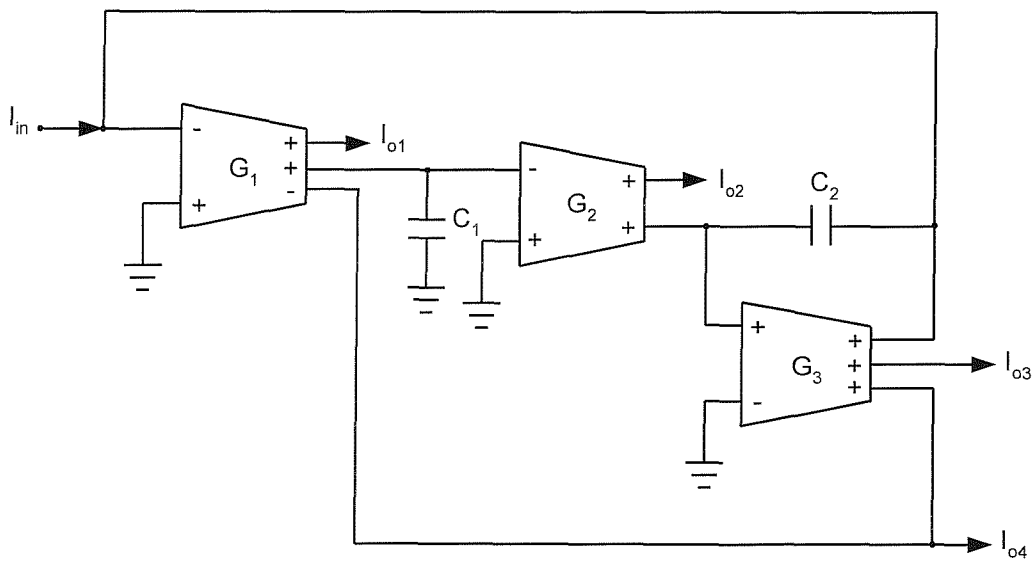


Fig. 5-11 Universal OTA-C biquad [24]

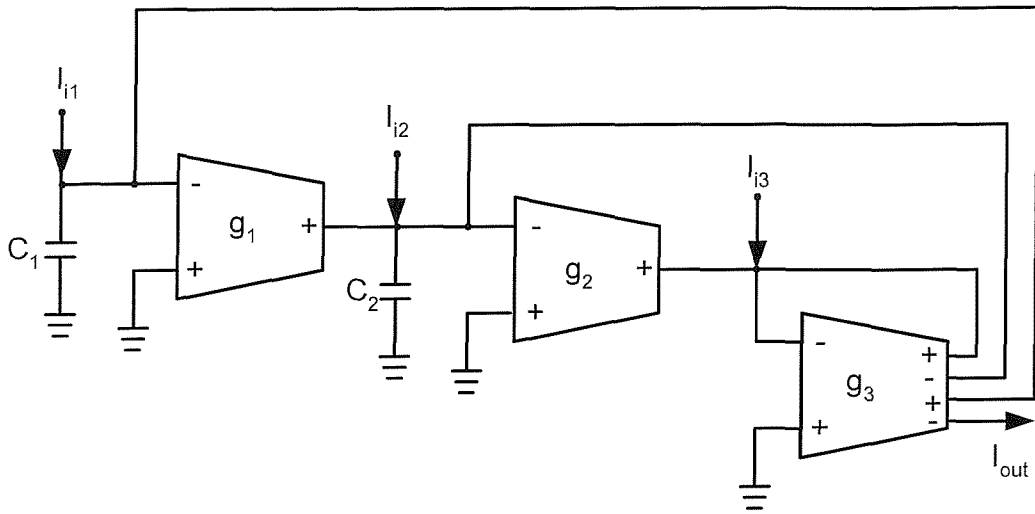


Fig. 5-12 Universal OTA-C biquad [25]

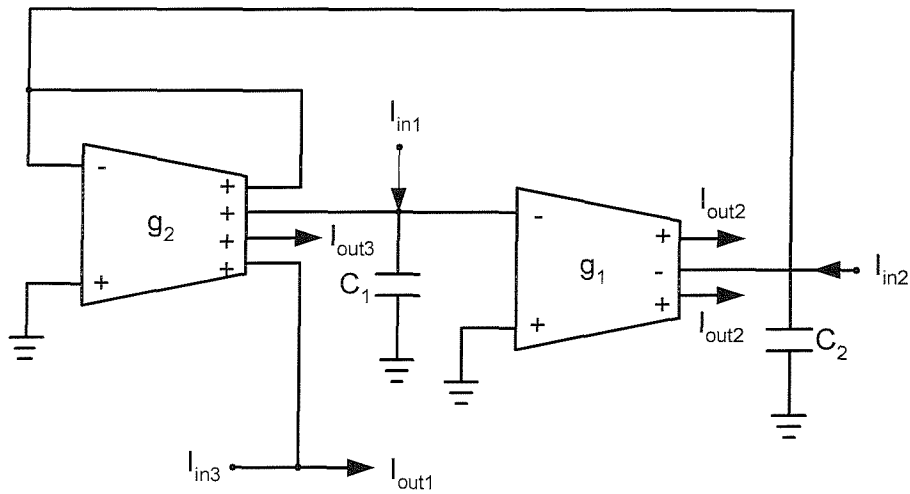


Fig. 5-13 Universal OTA-C biquad [26]

The motivation of this chapter is to develop a new biquad filter model constructed by an active nullor, current mirrors and passive R and C elements. Based on this model, two new implementations by using CCCII and OTAs are capable of achieving the above mentioned *five performance parameters* simultaneously and without trade-offs.

5.2 Biquad Filter Model

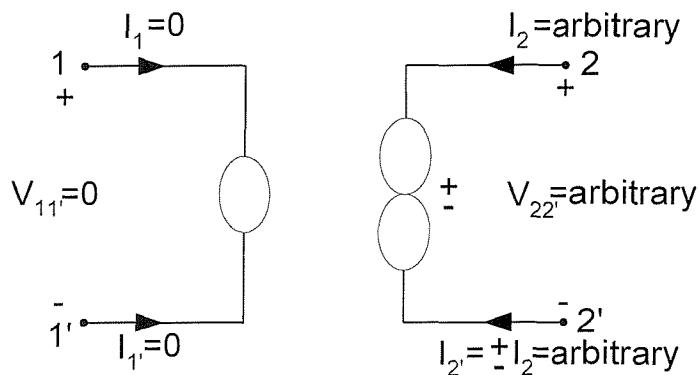


Fig. 5-14 A nullor symbol with a nullator and a norator

The proposed new biquad filter model is shown in Fig. 5-19 where a nullor symbol is shown in Fig. 5-14. A nullor includes a nullator with the characteristic: $I_1 = I_{1'} = 0$ A and $V_{11'} = 0$ V at its input port, and a norator with the characteristic: $I_2 = \pm I_{2'}$ (The + or – sign is consistent with the + or – type of the norator.) = arbitrary and $V_{22'} =$ arbitrary at its output port [30, 85].

The design process of the new biquad filter model shown in Fig. 5-19 is presented step by step as follows.

Step 1: Suppose only two internal nodes to be arranged in the biquad filter model. Let the two nodal voltages be V_1 and V_2 . Suppose only one input current signal, I_{in} , to be given in the model.

Step 2: To obtain the denominator, i.e., $a_2s^2+a_1s+a_0$, of a second-order biquad transfer function, the relevant current matrix equation with admittance coefficient matrix is arranged as below.

$$\begin{bmatrix} sC_1 + G_1 & -G_2 \\ G_3 & sC_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} I_{in} \\ 0 \end{bmatrix} \quad (5-7)$$

Then,
$$\frac{V_1}{I_{in}} = \frac{sC_2}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \quad (5-8)$$

$$\frac{V_2}{I_{in}} = \frac{-G_3}{s^2C_1C_2 + sC_2G_1 + G_2G_3} \quad (5-9)$$

Note that both transfer functions shown in Eqs. (5-8) and (5-9) have the desired denominator form, i.e., $a_2s^2+a_1s+a_0$.

Step 3: The realization of the first equation in Eq. (5-7), $(sC_1 + G_1)V_1 + (-G_2)V_2 = I_{in}$, using norators, nullators, and grounded passive elements, is shown in Fig. 5-15.

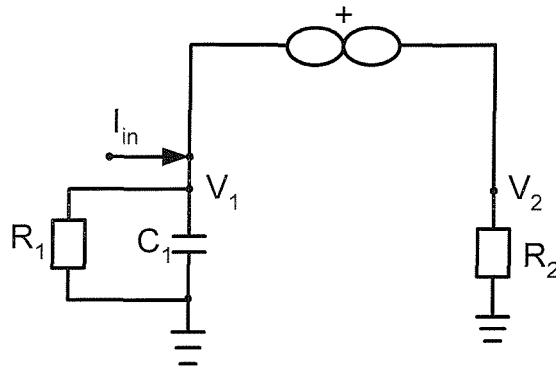


Fig. 5-15 Realization of the first equation in Eq. (5-7)

Step 4: Realize the second equation of Eq. (5-7), i.e., $G_3V_1 + sC_2V_2 = 0$, using norators, nullators, and grounded passive elements. After the combination with the structure of

Fig. 5-15, Fig. 5-16 is obtained and the part bounded by a closed virtual line shows the realization of the second equation of Eq. (5-7).

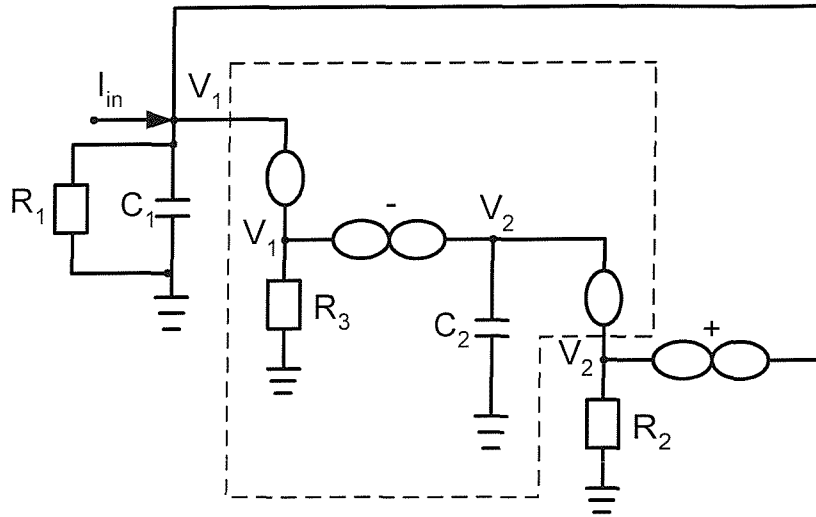


Fig. 5-16 Realization of Eq. (5-7)

Step 5: From Eq. (5-8), we obtain $\frac{V_1 G_1}{I_{in}} = \frac{-I_{BP}}{I_{in}} = \frac{sC_2 G_1}{s^2 C_1 C_2 + sC_2 G_1 + G_2 G_3}$. It is needed to take the current $V_1 G_1$ or $(-I_{BP})$ out from the circuit structure shown in Fig. 5-16. Then, Fig. 5-16 is expanded to be Fig. 5-17 with the available output current signal, I_{BP} , whose related transfer function is presented below.

$$\frac{I_{BP}}{I_{in}} = \frac{-sC_2 G_1}{s^2 C_1 C_2 + sC_2 G_1 + G_2 G_3} \quad (5-10)$$

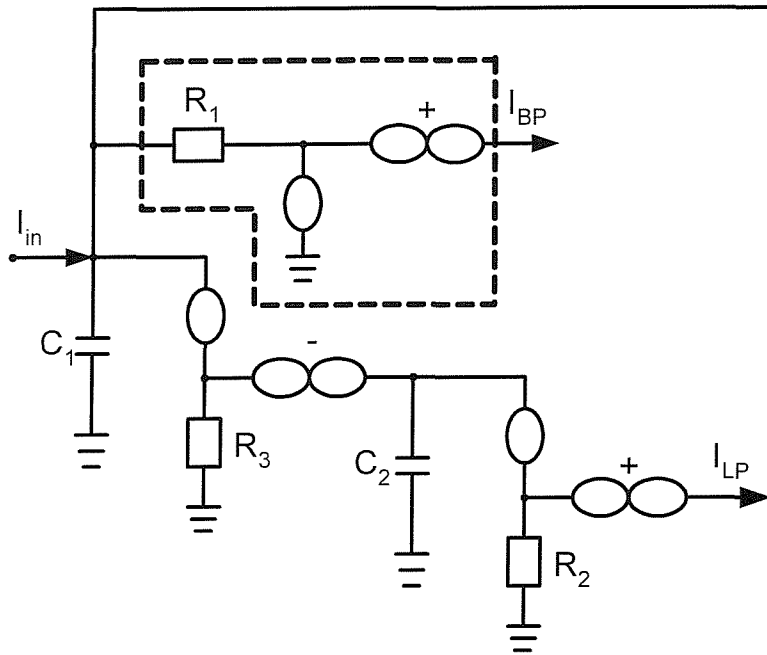


Fig. 5-17 Realization of Eq. (5-7) with an available output current signal, I_{BP}

Step 6: Similarly, from Eq. (5-9), we obtain

$$\frac{V_2 G_2}{I_{in}} = \frac{I_{LP}}{I_{in}} = \frac{-G_2 G_3}{s^2 C_1 C_2 + s C_2 G_1 + G_2 G_3}. \quad (5-11)$$

It is also needed to take the current $V_2 G_2$ or I_{LP} out from the circuit structure shown in Fig. 5-17. A current mirror, used for duplicating the current signal, is added and connected following the output current signal I_{LP} . The circuit structure becomes that shown in Fig. 5-18 with an extra output current signal, I_{LP} .

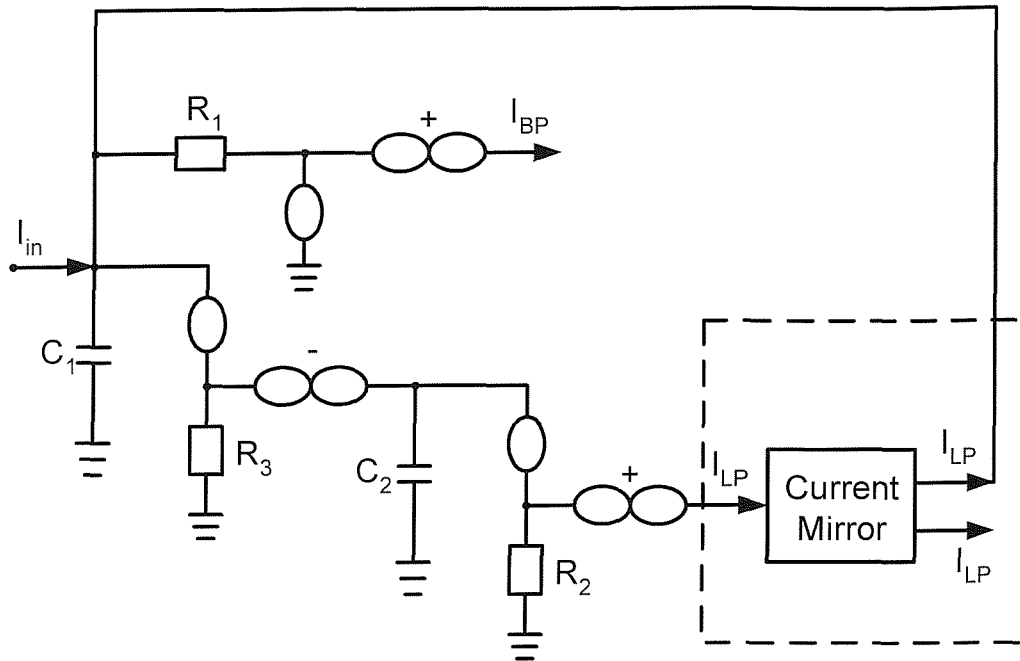


Fig. 5-18 Realization of Eq. (5-7) with two available output current signals, I_{BP} and I_{LP}

Step 7: A notch current signal can be obtained by using the following algebraic relationship:

$$1 + \frac{I_{BP}}{I_{in}} = 1 + \frac{-sC_2G_1}{s^2C_1C_2 + sC_2G_1 + G_2G_3} = \frac{s^2C_1C_2 + G_2G_3}{s^2C_1C_2 + sC_2G_1 + G_2G_3} = \frac{I_{NH}}{I_{in}} \quad (5-12)$$

$$\text{Namely, } I_{in} + I_{BP} = I_{NH} \quad (5-13)$$

Use the current mirror to take out two I_{BP} 's. One of the two I_{BP} 's is added by the I_{in} , shown in the part structure bounded by a closed virtual line in Fig. 5-19. A notch output current signal, I_{NH} , is available in Fig. 5-19 which shows the new proposed biquad filter model.

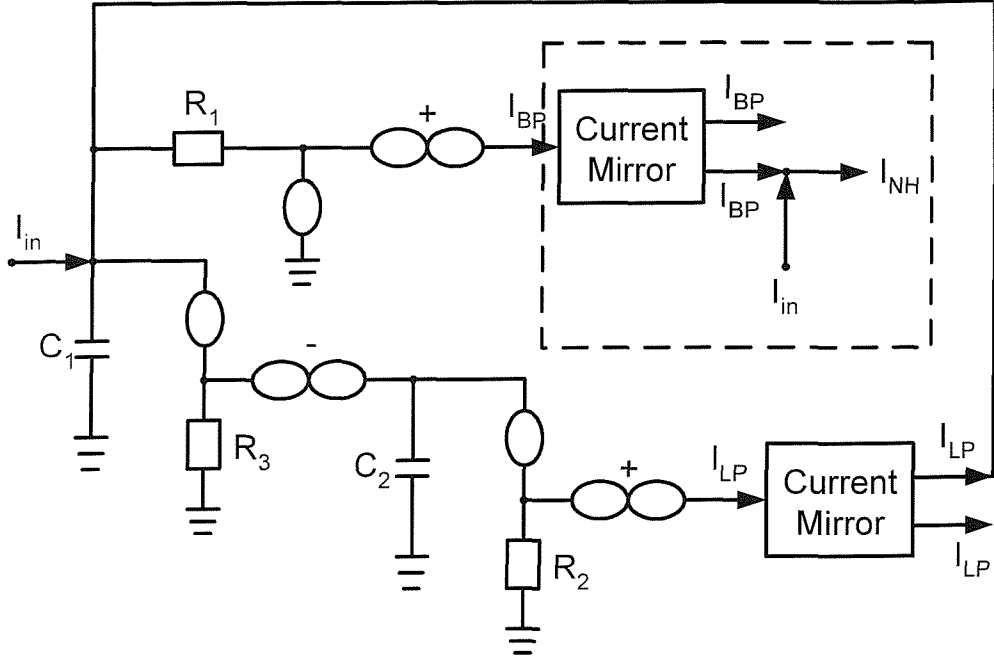


Fig. 5-19 New biquad filter model

Eqs. (5-10), (5-11), and (5-12) show an inverting band-pass at current output I_{BP} , an inverting low-pass function at current output I_{LP} , and a notch function at current output I_{NH} . An all-pass response can be obtained by summing Eqs. (5-10) and (5-12), i.e., joining the two output terminals, I_{BP} and I_{NH} , with the following transfer function:

$$\frac{I_{AP}}{I_{in}} = \frac{s^2 C_1 C_2 - s C_2 G_1 + G_2 G_3}{s^2 C_1 C_2 + s C_2 G_1 + G_2 G_3} \quad (5-14)$$

Similarly, a high-pass response can be obtained by summing Eqs. (5-12) and (5-11), i.e., joining the two output terminals, I_{NH} and I_{LP} , with the following transfer function:

$$\frac{I_{HP}}{I_{in}} = \frac{s^2 C_1 C_2}{s^2 C_1 C_2 + s C_2 G_1 + G_2 G_3} \quad (5-15)$$

The proposed filter topology enjoys independent ω_o and ω_o/Q tunability as shown:

$$\omega_o = \sqrt{\frac{G_2 G_3}{C_1 C_2}}$$

$$\frac{\omega_o}{Q} = \frac{G_1}{C_1} \quad (5-16)$$

The parameter ω_o can be changed either by G_2 ($=1/R_2$) or G_3 ($=1/R_3$), without disturbing Q , which can be independently varied by G_1 ($=1/R_1$). Note ω_o can also be changed by both components (G_2, G_3) if wider tuning range of ω_o is required, without affecting Q .

The sensitivities of ω_o and $\frac{\omega_o}{Q}$ are easily calculated and shown as follows.

$$S_{G_2, G_3}^{\omega_o} = 1/2 = -S_{C_1, C_2}^{\omega_o}, \quad S_{G_1}^{\omega_o} = 0, \quad S_{G_1}^{\omega_o/Q} = 1 = -S_{C_1}^{\omega_o/Q}, \quad \text{and} \quad S_{G_2, G_3, C_2}^{\omega_o/Q} = 0 \quad (5-17)$$

all of which are small.

5.3 CCCII-based Implementation

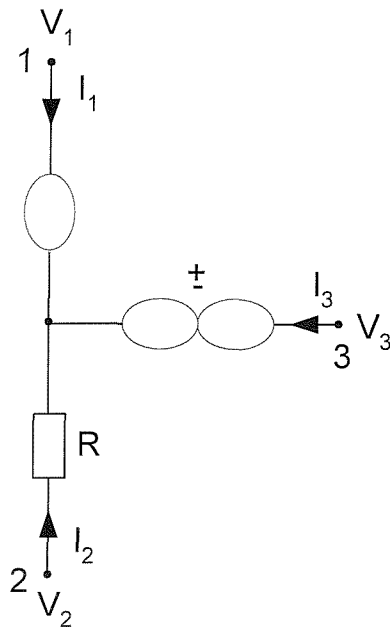


Fig. 5-20 Fundamental nullor- R topology

A fundamental nullor- R topology is shown in Fig. 5-20 which is a three-terminal topology. The characteristic of the three-terminal fundamental topology can be derived and presented in the following matrix relationship:

$$\begin{bmatrix} I_1 \\ I_{3\pm} \\ V_2 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm 1 & 0 & 0 \\ R & 1 & 0 \end{bmatrix} \begin{bmatrix} I_2 \\ V_1 \\ V_3 \end{bmatrix} \quad (5-18)$$

However, a dual-output second generation current-controlled conveyor (CCCII) is characterised by the matrix relationship [63-66] shown in Eq. (5-1). Eq. (5-18) is the same as Eq. (5-1) provided $R_x = R$, $y = 1$, $x = 2$, and $z = 3$. A dual-output CCCII has two output terminals, the other of which is realized by using current mirror for duplicating the output current signal such as I_{BP} and I_{LP} shown in Fig. 5-19. Therefore, the proposed new biquad filter model can be implemented by using one single-output and two dual-output CCCIIs. The CCCII-based biquad implementation of the proposed new biquad filter model is shown in Fig. 5-21.

Circuit analysis yields the same current transfer functions and the same ω_o and ω_o/Q as Eqs. (5-10) to (5-16) by the replacement of G_1 , G_2 , and G_3 with G_{x1} , G_{x2} , and G_{x3} . The implemented CCCII-based biquad enjoys the *five performance parameters* simultaneously described in Chapter 1 and is called a *unified* biquad.

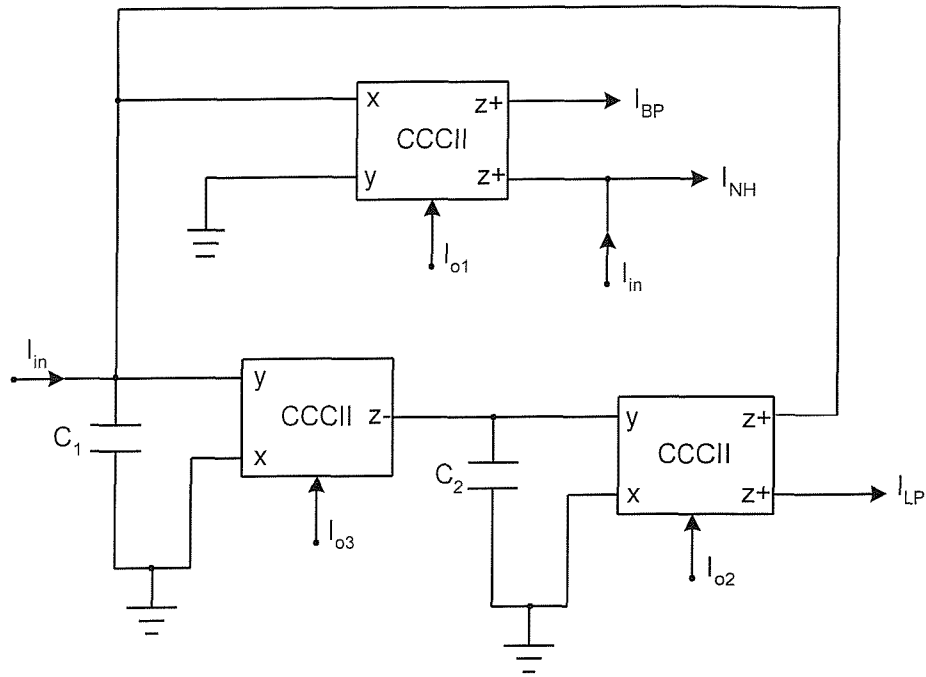


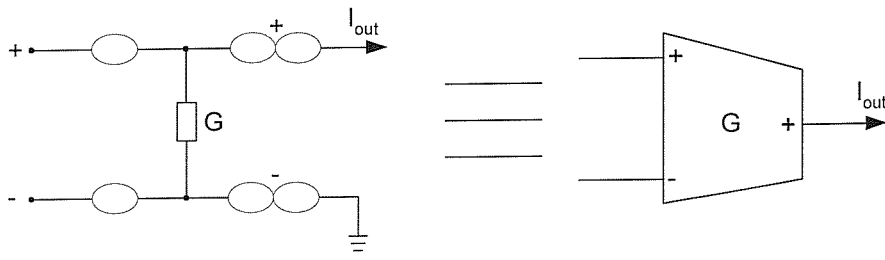
Fig. 5-21 Implementation derived from the new biquad filter model based on CCCIIs.

5.4 OTA-based Implementation

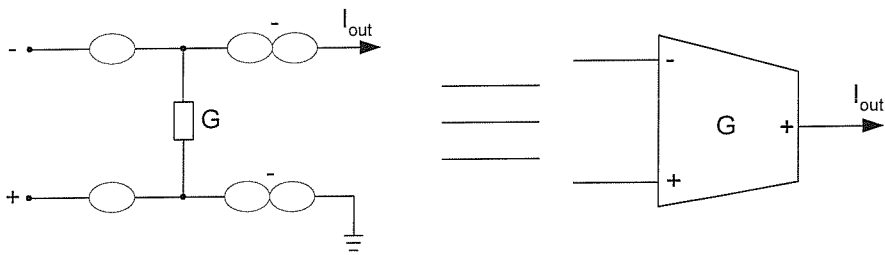
The characteristic of an operational transconductance amplifier (OTA) is shown in the following matrix relationship:

$$\begin{bmatrix} I_+ \\ I_- \\ I_{out} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ G & -G & 0 \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \\ V_{out} \end{bmatrix} \quad (5-19)$$

where I_+ , I_- , and I_{out} are the input current flowing into terminal +, the input current flowing into terminal -, and the output current flowing out of the output terminal,



5-22 (a)



5-22 (b)

Fig. 5-22 Two equivalent nullor- G topologies of an OTA

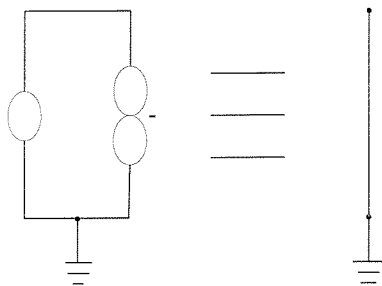
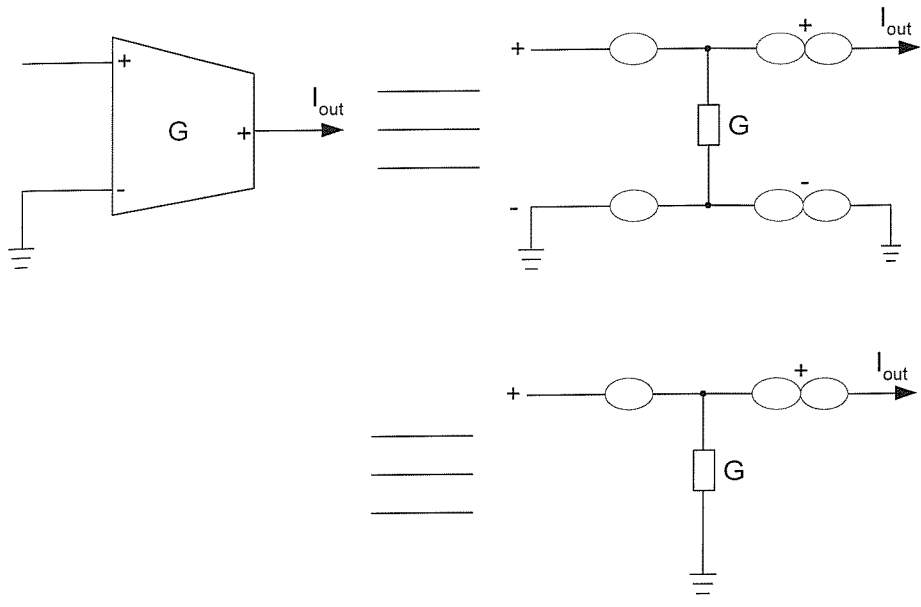
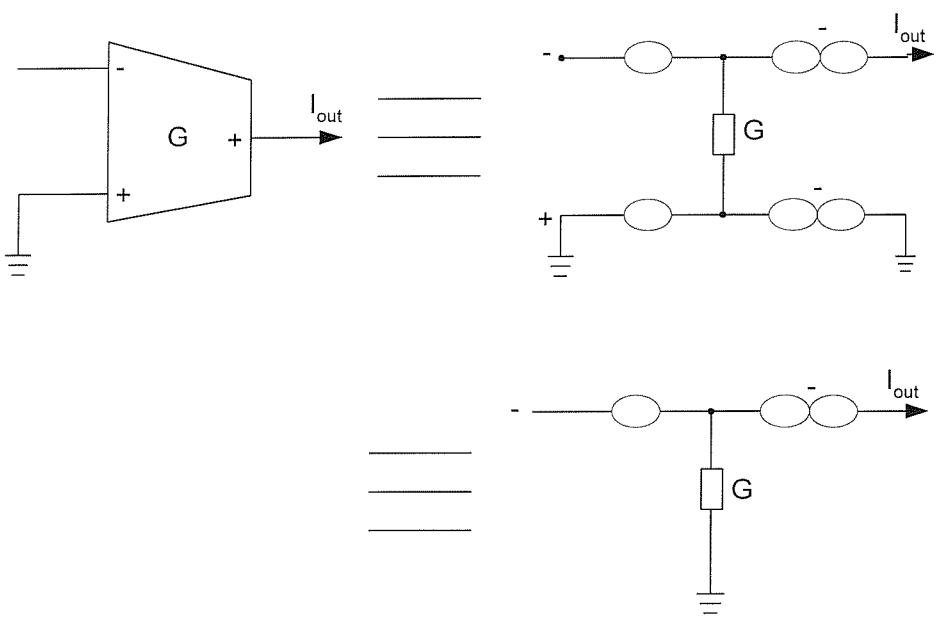


Fig.5-23 Nullor equivalence

respectively. The two equivalent nullor- G topologies of an OTA have been shown in Figs. 5-22 (a) and 5-22 (b) [85]. It has been proved that a nullator in parallel with a norator is equivalent to a short circuit [85] which is shown in Fig. 5-23. Therefore, if we let the negative (resp. positive) terminal in Fig. 5-22 (a) (resp. 5-22 (b)) be grounded, shown in Fig. 5-24 (a) (resp. 5-24 (b)), then both of the two nullor- G topologies shown in Figs. 5-22 (a) and 5-22 (b) are going to become the fundamental nullor- R topology shown in Fig. 5-20, which appears in the new biquad filter model shown in Fig. 5-19, provided $G = 1/R$ but with a grounded terminal 2, and can be realized by a single-input OTA with a grounded “-” (resp. “+”) input terminal, shown in Fig. 5-24 (a) (resp. 5-24 (b)). Moreover, the part model bounded by a closed virtual line shown in Fig. 5-17 is easily proved and equivalent to the nullor- R_I or G_I topology shown in Fig. 5-25 provided $R_I=1/G_I$. It means that the proposed new biquad filter model can also be implemented by using one single-output and two multiple-output OTAs. The OTA-based biquad implementation of the proposed new biquad filter model is shown in Fig. 5-26. Circuit analysis yields the same current transfer functions and the same ω_o and ω_o/Q as Eqs. (5-10) to (5-16). The implemented OTA-based biquad is also a *unified* biquad enjoying the *five performance parameters* simultaneously described in Chapter 1.



5-24 (a)



5-24 (b)

Fig. 5-24 Two equivalent nullor- G topologies of a single-input OTA

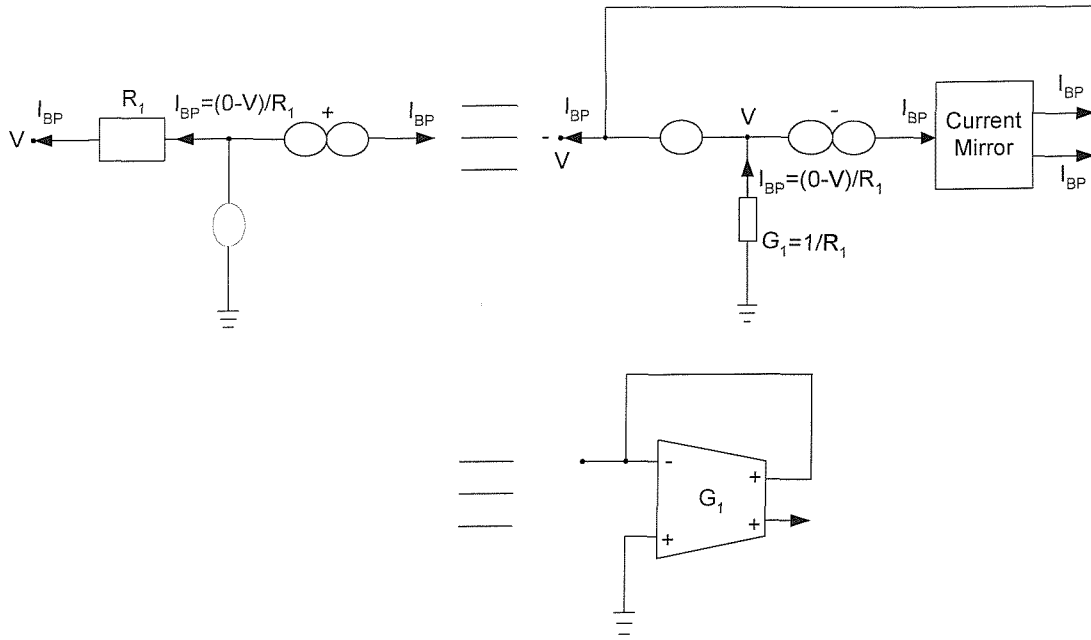


Fig. 5-25 Two Equivalent nullor- R_1 or G_1 topologies

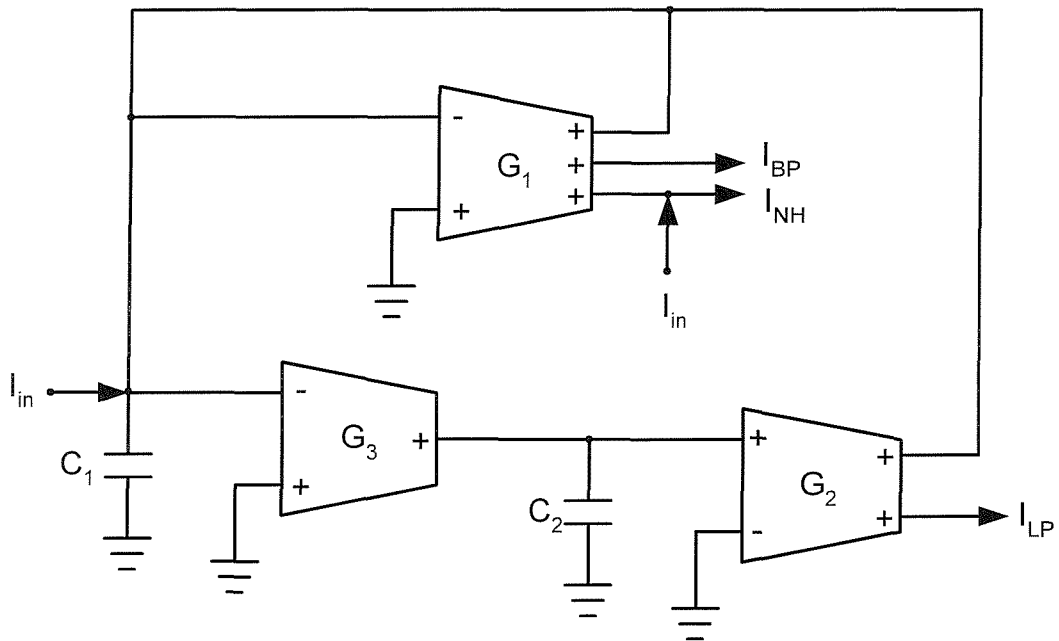


Fig. 5-26 Implementation derived from the new biquad filter model based on OTAs.

5.5 Simulation Results

To verify the theoretical analysis of the implemented OTA-based biquad shown in Fig. 5-26, 2 MHz low-pass, band-pass and band-reject filtering responses with Q of 0.707 have been simulated using UMC05 level-49 H-Spice with the following supply voltages, bias current, transconductance and capacitances: $V_{dd}=2.5V$, $V_{ss}=-2.5V$, $I_{abc}=95.385\mu A$ leading to $G_1=G_2=G_3=180\ \mu S$ and $C_1=10.13\ pF$, $C_2=20.25\ pF$. The OTAs were implemented using the CMOS circuit described in Section 2.2. Fig. 5-27 shows the simulated low-pass, band-pass and band-reject filtering responses. By keeping the values of $G_2(=1/R_2)$, $G_3(=1/R_3)$, C_1 , and C_2 , and varying only $G_1(=1/R_1)$, we obtain band-pass and band-reject filter signals with different Q 's as shown in Figs. 5-28 and 5-29, respectively. The simulation values of passive components and their corresponding bias currents are shown in Table 5-3.

Table 5-3 Component values for simulating the BP and BR filter with different Q

Element \ Q	0.707	2	6	9
G_1	180 μS ($I_{abc}=95.385\mu A$)	90 μS ($I_{abc}=18.84\mu A$)	30 μS ($I_{abc}=3.822\mu A$)	20.5 μS ($I_{abc}=2.402\mu A$)
G_2	180 μS ($I_{abc}=95.385\mu A$)	180 μS ($I_{abc}=95.385\mu A$)	180 μS ($I_{abc}=95.385\mu A$)	180 μS ($I_{abc}=95.385\mu A$)
G_3	180 μS ($I_{abc}=95.385\mu A$)	180 μS ($I_{abc}=95.385\mu A$)	180 μS ($I_{abc}=95.385\mu A$)	180 μS ($I_{abc}=95.385\mu A$)
C_1	20.25pF	28.65pF	28.65pF	28.65pF
C_2	40.50pF	28.65pF	28.65pF	28.65pF

To examine the voltages and currents in the internal nodes and branches of the unified biquad filters, shown in Fig. 5-30 (CCCI-based biquad) and Fig. 5-32 (OTA-based biquad), has been simulated. The given component values are $g_1=164\mu S$, $g_2=116\mu S$, $g_3=116\mu S$, and $C_1=C_2=18.45pF$. The CMOS implementations of the CCCIs and the OTAs are described in Section 5.1 and Section 2.2. All the curves have limited ranges, for example, the curves shown in Figs. 5-31 and 5-33, which confirm the feasibility of the new filter structure. Noise simulation results of Figs. 5-30 and 5-32 are shown in

Figs. 5-34 and 5-35 in which the maximum noise magnitudes are 40.586pA and 40.584pA, compared to 1mA output current.

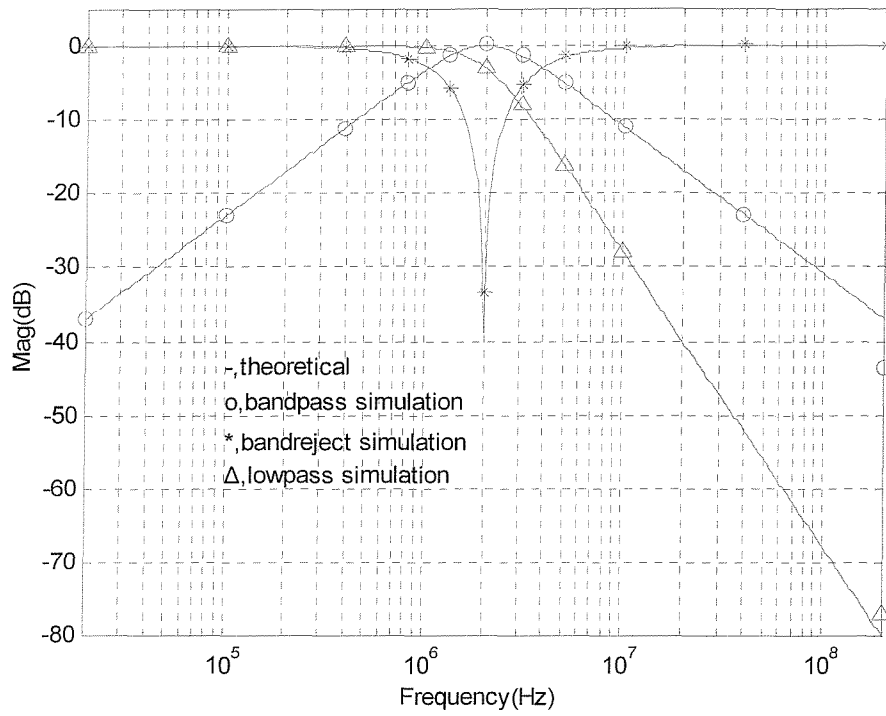


Fig. 5-27 LP, BP and BR amplitude frequency responses Fig. 5-26

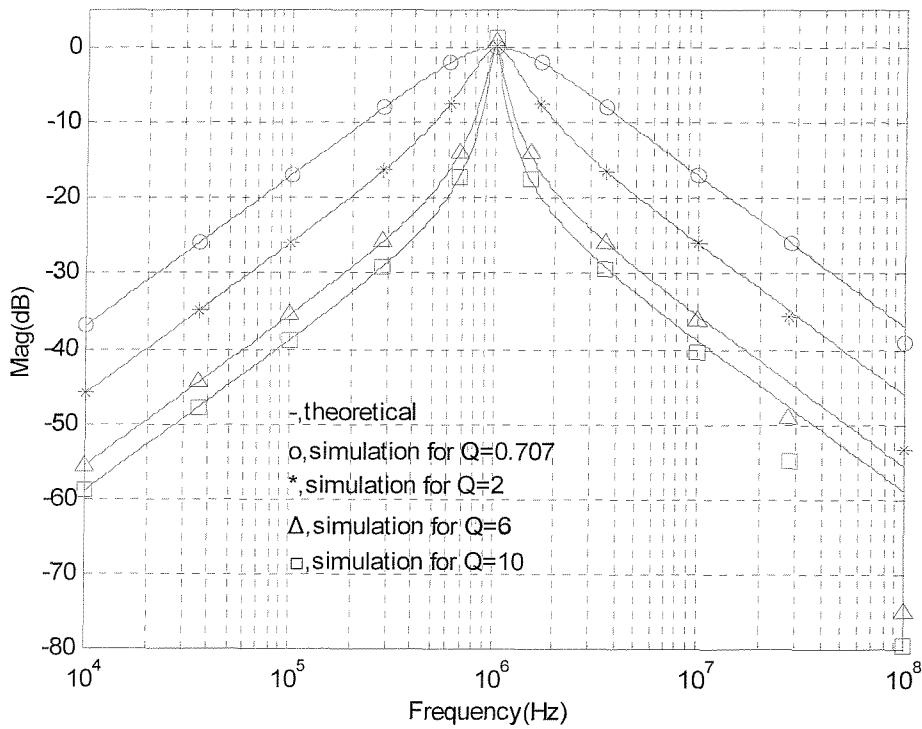


Fig. 5-28 Band-pass amplitude frequency responses with $Q=0.707, 2, 6,$ and 10

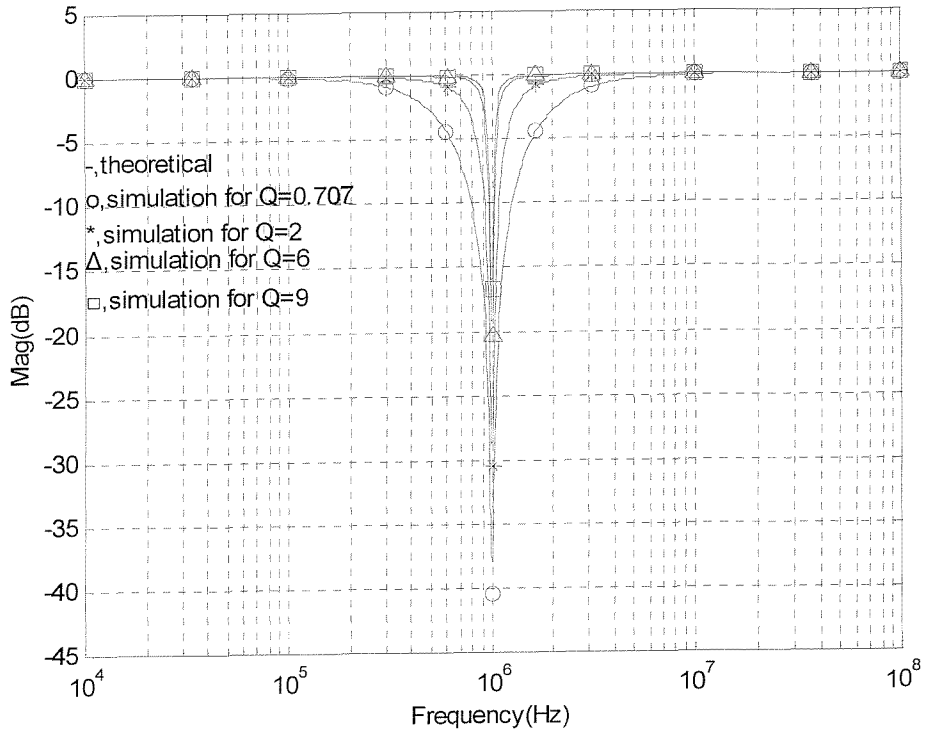


Fig. 5-29 Band-reject amplitude frequency responses with $Q=0.707, 2, 6,$ and 10

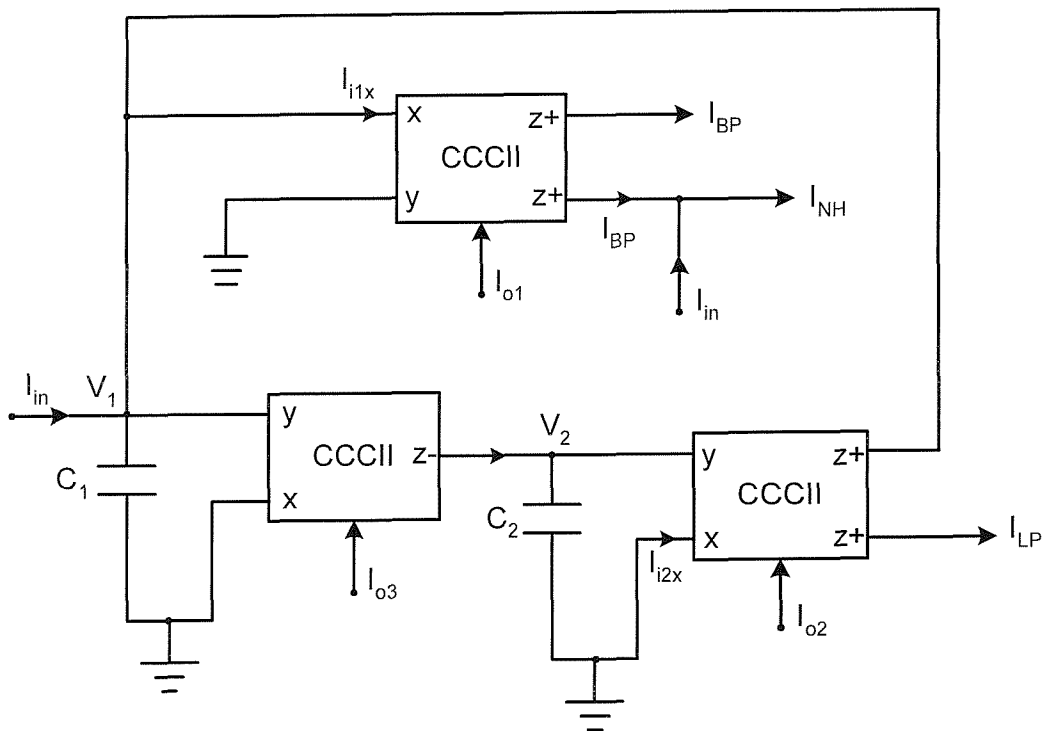


Fig. 5-30 CCCII-based implementation

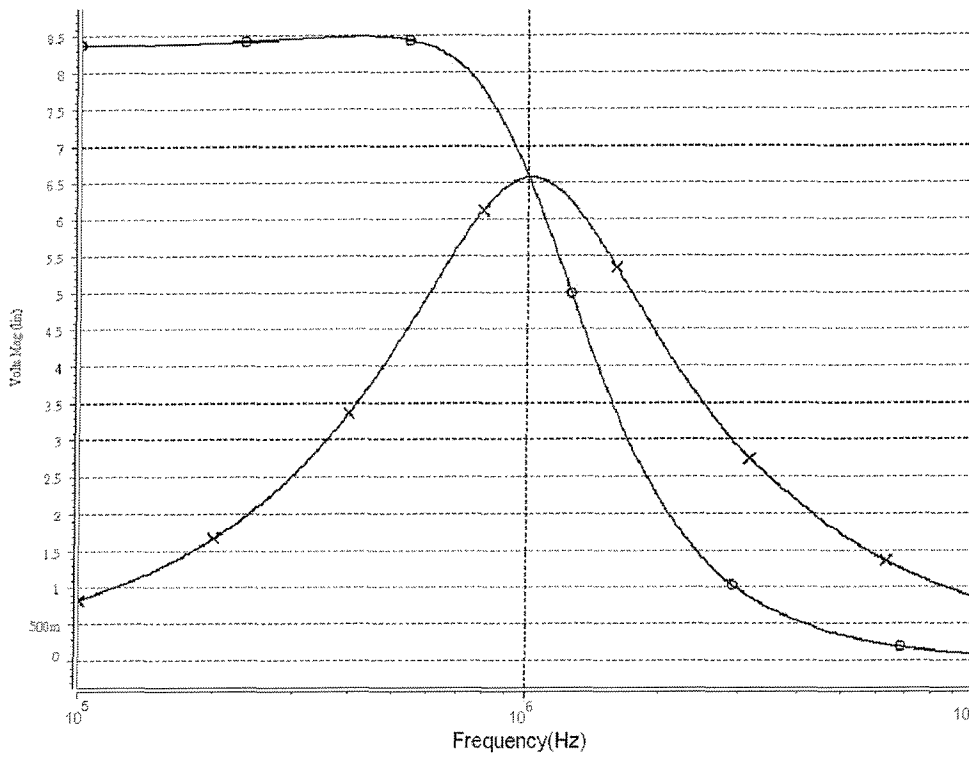


Fig. 5-31 (a) Amplitude-frequency responses of node voltages, $V_1(x)$, and $V_2(o)$

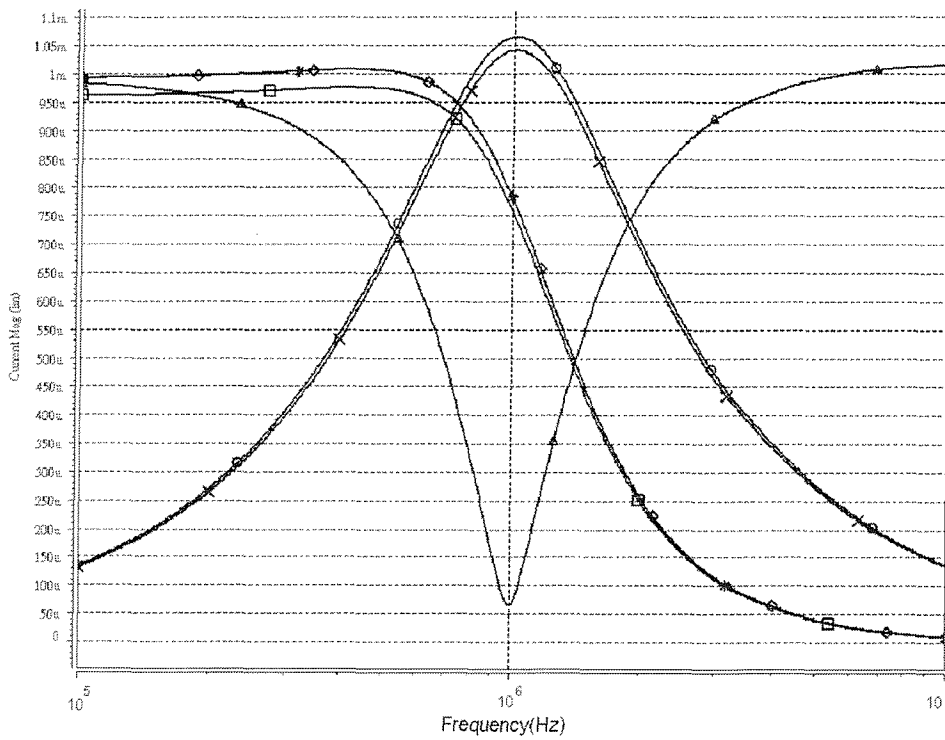


Fig. 5-31 (b) Amplitude-frequency responses of branch currents, $I_{1x}(x)$, $I_{BP}(o)$, $I_{NH}(\Delta)$, $I_{2x}(\square)$, and $I_{LP}(*, \diamond)$

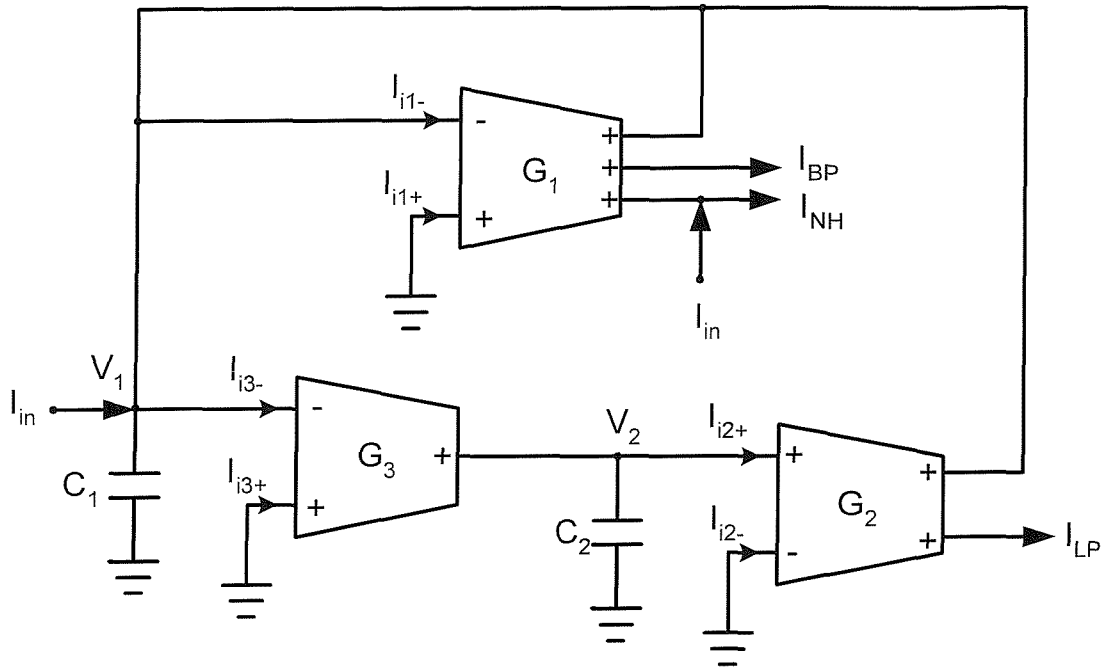


Fig. 5-32 OTA-based implementation

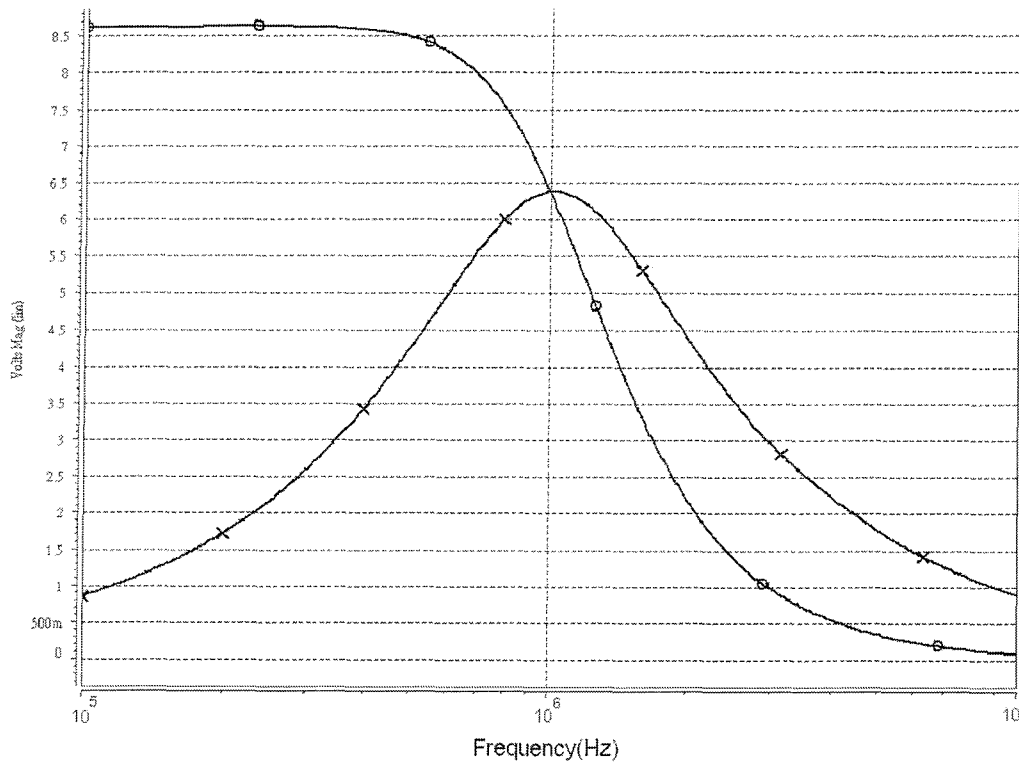


Fig. 5-33 (a) Amplitude-frequency responses of node voltages, V_1 (x), and V_2 (o)

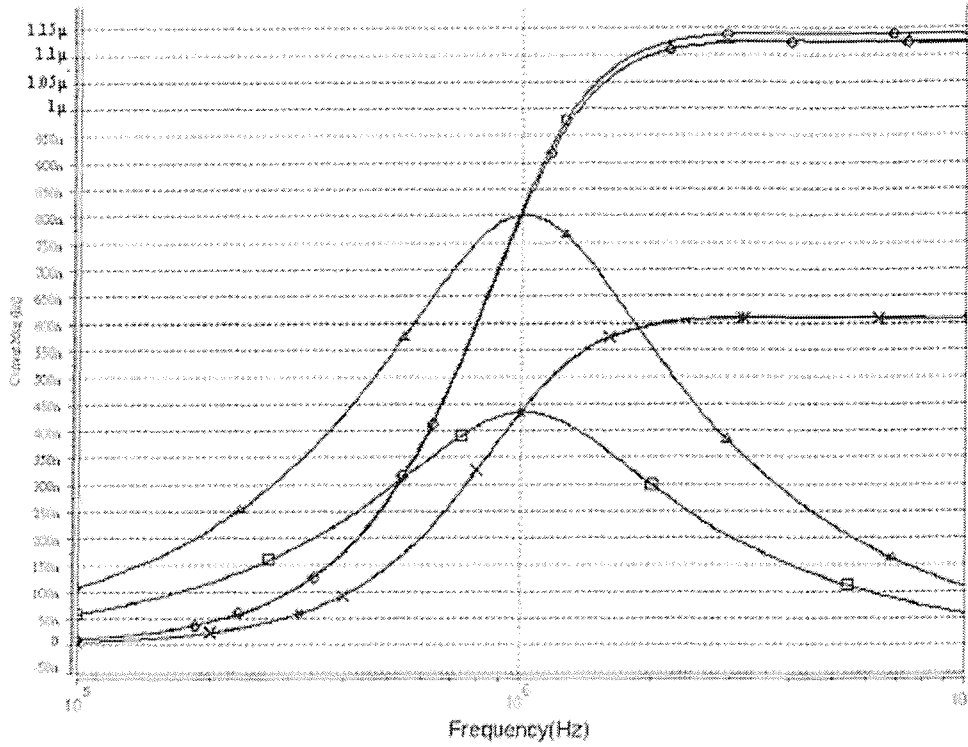


Fig. 5-33 (b) Amplitude-frequency responses of branch currents, I_{i1+} (x), I_{i1-} (o), I_{i2-} (Δ), I_{i2+} (\square), I_{i3+} (*), and I_{i3-} (\diamond)

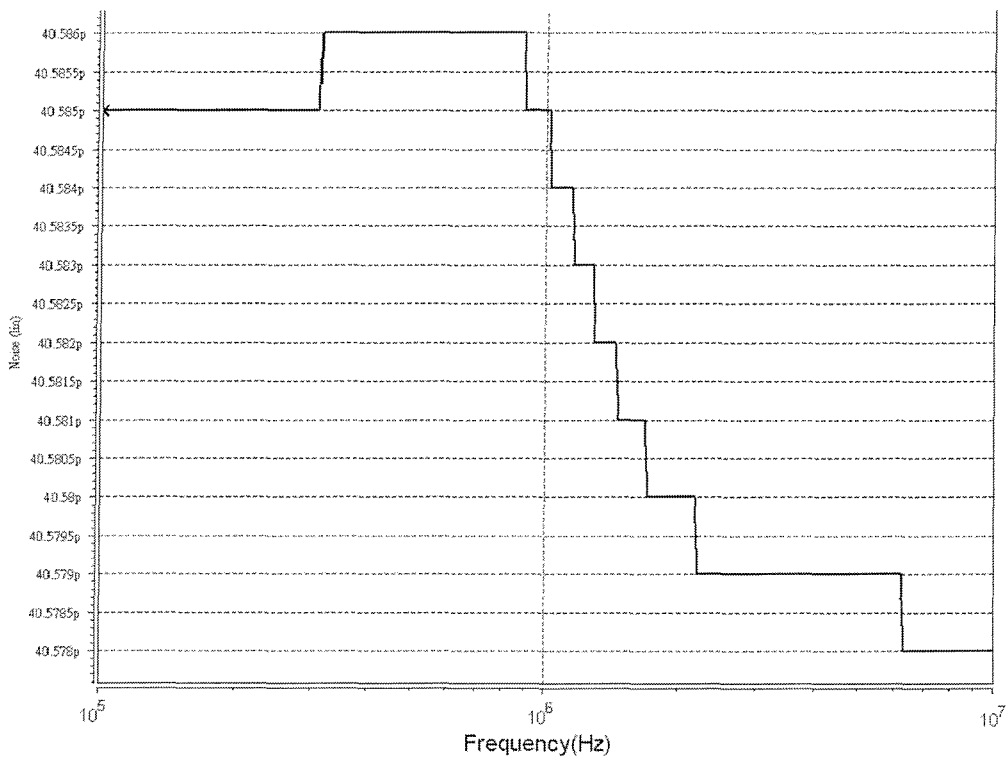


Fig. 5-34 Noise simulation result: low-pass amplitude-frequency response of Fig. 5-30

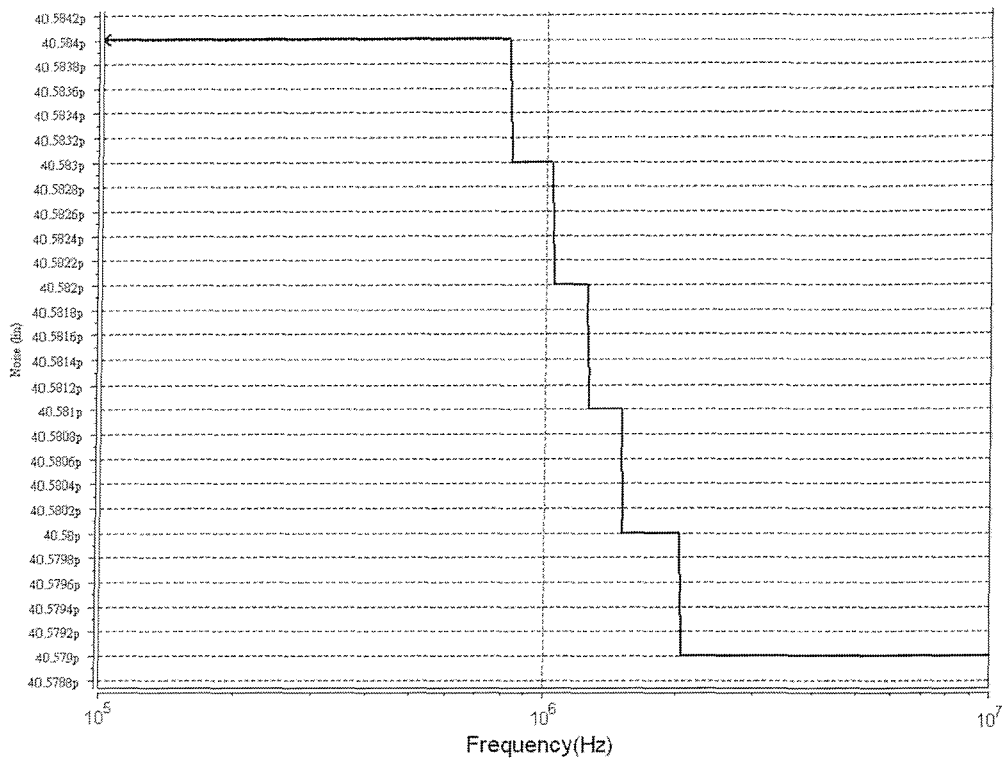


Fig. 5-35 Noise simulation result: low-pass amplitude-frequency response of Fig. 5-32

5.6 Concluding remarks

One new RC-nullor biquad filter model and its two *unified* biquad implementations, including their transformation approaches, based upon CCCIs and OTAs have been presented. The two biquad implementations are capable of achieving *five performance parameters* simultaneously and without trade-offs, unlike some recently reported filter circuits [22-26, 63-66] and those cited therein. They represent an attractive option in applications where size and cost are important since they employ the least number of passive and active components necessary to realise 2nd-order filtering function. Independent tunability is an attractive advantage. Furthermore, the two biquad implementations are useful in applications where operational flexibility is required since they provide numerous filtering functions from the same structure, and without imposing component choice conditions.

Chapter 6

Comparative Analysis of Filter

Structures and Synthesis Methods

Chapters 3, 4 and 5 have presented different synthesis methods and biquad structures based on different operating mode (voltage, current) and different active elements (OTA and CCCII). Due to the diversity of the choice of design methods and the various possible tradeoffs in terms of performance and implementation parameters, this chapter compares the various synthesis methods and filter structures outlined in the previous chapters with the aim of assisting the designer to select a suitable circuit given a filtering problem and implementation style.

The comparative analysis is divided into two parts. The first part is devoted to current-mode and voltage-mode analytical synthesis methods presented in Chapters 3 and 4, and is discussed in Section 6.1. The second part compares the unified OTA-based and CCCII-based biquad filters considered in Chapter 5 and is discussed in Section 6.2.

6.1 Analytical Synthesis Methods Comparison

The comparison is carried out in terms of seven parameters. The parameters are: (i) component count, (ii) single-input OTAs, (iii) grounded capacitors, (iv) function types, (v) equal g or C , (vi) cascadability, and (vii) sensitivity. Section 6.1.1 covers the comparison between the two current-mode analytical synthesis methods, i.e., MISOC and DIMOC methods. Section 6.1.2 considers the comparison between the voltage-mode synthesis methods outlined in Chapter 4. Finally, Section 6.1.3 compares the current-mode synthesis methods with the voltage-mode synthesis methods.

6.1.1 Comparison between Current-Mode Synthesis Methods

Table 6.1 gives the comparison between the two synthesis methods (MISOC and DIMOC methods) in terms of the above six identified parameters. As can be seen both methods produce filters that have the same characteristics including same component count, and functions types.

Table 6-1 Comparison between two current-mode synthesis methods

Method Parameter	MISOC	DIMOC
Component count	n OTAs and n capacitors	n OTAs and n capacitors
Single-input OTAs	Yes	Yes
Grounded capacitors	Yes	Yes
Function types	Generic 5*	Generic 5*
Equal g or C	No	No
Cascadability	Yes (output port) No (input port)**	Yes (output port) No (input port)**
Sensitivities	0, +1, or -1	0, +1, or -1

*Generic (LP, HP, BP, BR, AP)

**A current buffer is needed to do the connection with the previous stage.

Whilst the table shows that both methods provide filters that have the same number of OTAs, and capacitors, closer examination of the circuits produced by both methods reveal interesting information. For example, consider a fourth-order all-pass filter designed using the DIMOC and MISCO methods, Figures 3-19 and 3-21 show the circuits. Because the number of output terminals of an OTA and the number of input signals shown in the two filter structures using MISOC and DIMOC methods are different, the complexity of the two filter structures is different. For example, the filter in Fig. 3-21 has 3 four-output OTAs and 1 three-output OTA, leading to 15 output terminals, compared with that in Fig. 3-19 which has 3 single-output OTAs and one five-output OTA, leading to 8 output terminals, in addition to 3 and 2 input current signals for those in Figs. 3-19 and 3-21, respectively. The total output terminals using

the MISOC synthesis method is fewer in number, in general, than that using the DIMOC synthesis method. However, the multiple copies of the input current using the MISOC synthesis method need more transistors, in general, than those using the DIMOC synthesis method. For example, a typical 4th-order high-pass filter would have 8 and 2 transistors for 4 and 1 copies of the input current using MISOC (Fig. 3-18) and DIMOC (Fig. 3-20) methods, respectively.

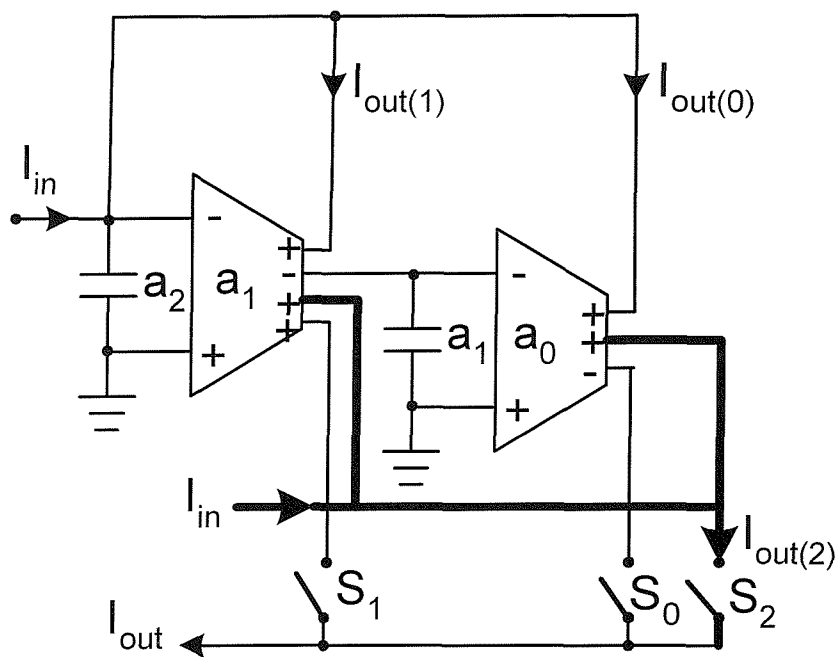


Fig. 6-1 2nd-order DIMOC filter structure

There is one more feature which can be used to compare the filters obtained using both synthesis methods. It should be noted that the DIMOC synthesis method may prove more convenient for digitally programmable filters where filter function is changed by closing and opening the appropriate switches [79]. For example, the second-order DIMOC filter structure is shown in Fig. 6-1. The relationship between filtering functions and switches of Fig. 6-1 is shown in Table 6-2.

Table 6-2 Relationship between filtering functions and switches

Function \ Switch	S_0	S_1	S_2
Low-pass	Close	Open	Open
Band-pass	Open	Close	Open
High-pass	Open	Open	Close
Band-reject	Close	Open	Close
All-pass	Close	Close	Close

6.1.2 Comparison between Voltage-Mode Synthesis Methods

The comparison between the two new voltage-mode analytical synthesis methods, and the three filter structures (Figs. 4-1, 4-4, and 4-6, presented in Sections 4.2 and 4.3) is shown in Table 6-3.

Table 6-3 Comparison between two voltage-mode synthesis methods

Case \ Parameter	Sec. 4.2 Fig. 4-4	Sec. 4.2 Fig. 4-1	Sec. 4.3 Fig. 4-6
Component count	$2n+2$ OTAs, n capacitors	$n+2$ OTAs, n capacitors	$n+2$ OTAs, n capacitors
Single-input OTAs	Yes	Yes	Yes
Grounded capacitors	Yes	Yes	Yes
Function types	Arbitrary including elliptic	Low-pass, band-pass, and high-pass	All-pass
Equal g or C	Equal C	Equal g	No
Cascadability	Yes (input port) No (output port)*	Yes (input port) No (output port)*	Yes (input port) No (output port)*
Sensitivities	From -1 to +1**	0, +1, or -1	0, +1, or -1

* A voltage buffer is needed to do the connection with the next stage.

**The range is under the condition that all the transconductances in

Fig. 4-4 are positive.

Table 6-3 shows that the case shown in Section 4.2 with arbitrary function types (Fig. 4-4) needs n more OTAs than the cases shown in (i) Section 4.2 with low-pass, band-pass, and high-pass functions (Fig. 4-1), and (ii) Section 4.3 with a single all-pass function (Fig. 4-6). It is needed to be noted that the first filter structure (Fig. 4-1) enjoys the attractive equal transconductance design which makes the biasing circuitry the simplest and the control the easiest. Also, the second filter structure (Fig. 4-4) achieves the equal capacitance characteristic which leads to easy IC fabrication without the need to tune different values of capacitors.

6.1.3 Comparison between Filters Operating Modes

Section 6.1.1 and 6.1.2 provided comparisons between filters that operate in the same mode, in other words, either voltage mode or current mode. Such comparisons are useful if the operating mode is important in the filtering application. This section compares current mode against voltage mode filters, in applications where the operating mode is not the driving factor in choosing the filter circuit, but other parameters such as circuit complexity and flexibility are more important. Examining Tables 6-1 and 6-2, it is clear that the two particular voltage-mode cases (Figs. 4-1 and 4-6) in Sections 4.2 and 4.3 require 2 more OTAs than the current-mode MISOC and DIMOC methods. Moreover, the general voltage-mode synthesis method (Fig. 4-4) for realizing arbitrary functions needs $n+2$ more OTAs than the current-mode MISOC and DIMOC methods for realizing five generic filtering functions. For example, the fourth-order high-pass and all-pass filters designed using the current-mode MISOC and DIMOC methods shown in Figs. 3-18 to 3-21 have four OTAs. The fourth-order high-pass and all-pass filters designed using the two particular voltage-mode synthesis methods shown in Figs. 6-2 (derived from Fig. 4-1) and 6-3 (derived from Fig. 4-6), respectively, have six OTAs. The fourth-order all-pass filter designed using the general voltage-mode synthesis method shown in Fig. 6-4 (derived from Fig. 4-4) has ten OTAs. However, the VLSI realizations of the two voltage-mode filter structures (Figs. 4-1 and 4-4) are much better than those of the two current-mode filter structures (Figs. 3-6 and 3-10) due to equal transconductance or equal capacitance design.

However, all other parameters have the same/similar comparison results.

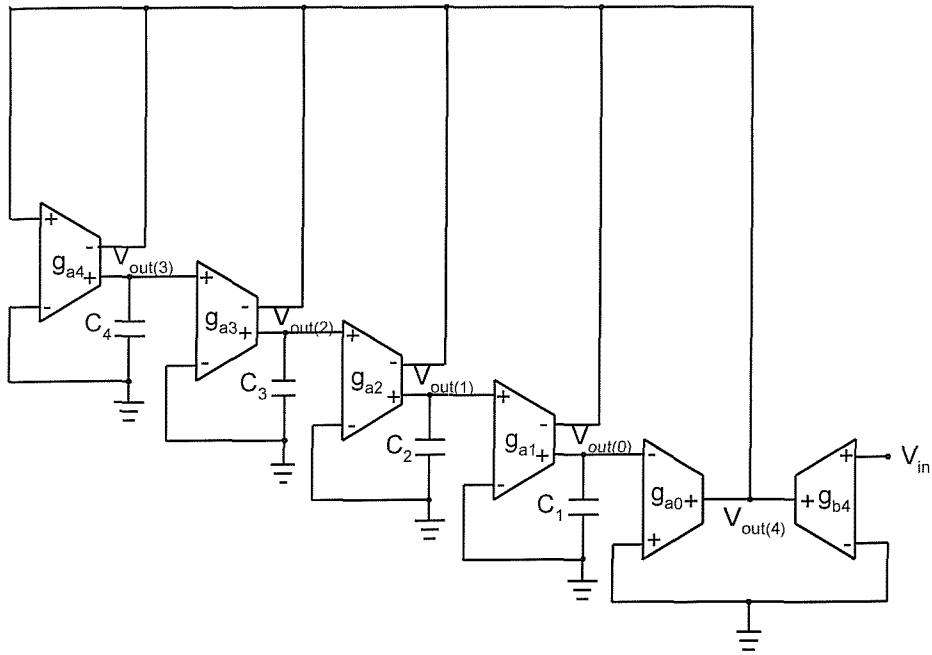


Fig. 6-2 Fourth-order voltage-mode OTA-C high-pass filter

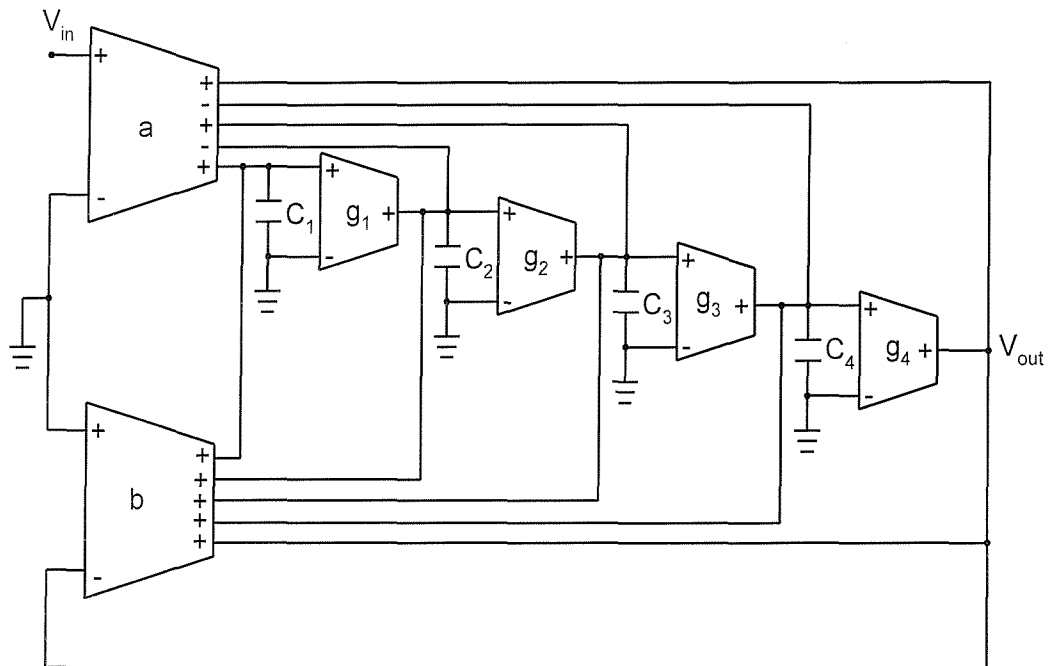


Fig. 6-3 Fourth-order voltage-mode OTA-C all-pass filter

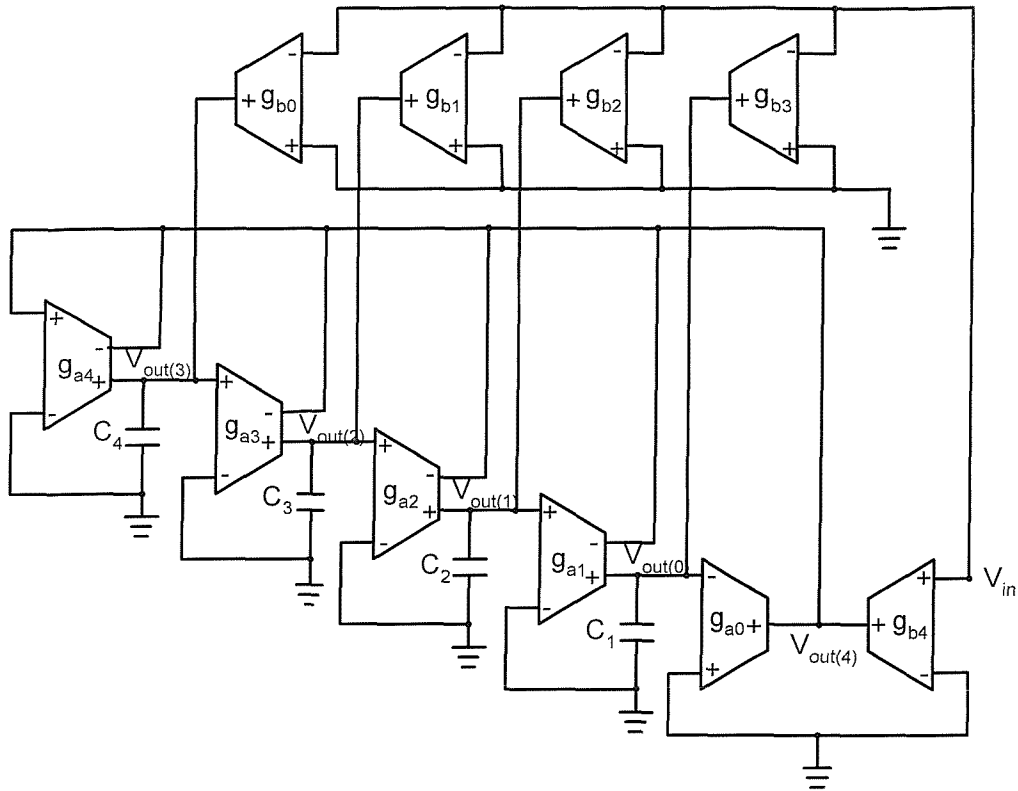


Fig. 6-4 Fourth-order voltage-mode OTA-C general all-pass filter

6.2 Comparison between Unified Biquad Filters

As outlined in Chapter 1, biquads need to have *five performance parameters* if they are to provide more features than what is possible with existing biquads [21-66]. The parameters are repeated here for convenience.

- universal filtering (low-pass, high-pass, band-pass, notch, and all-pass),
- minimum components count (three active elements, two grounded capacitors, and no resistors),
- independent ω_o and ω_o/Q tunability,
- no need to impose component choice conditions to realize specific filtering functions (which doesn't lead to the influence resulted from fabrication tolerances and drifts during operating), and
- no need to employ additional active elements to provide filter current outputs explicitly.

This section compares the unified OTA-based and CCCII-based biquad filters presented in Chapter 5 by the above *five performance parameters*. Because the two implementations are derived from the same biquad filter model shown in Fig. 5-19, both of them enjoy the above *five performance parameters* simultaneously. In fact, both the unified OTA-based and CCCII-based biquad filters have the same other features such as single-input OTAs, grounded capacitors, function types, and cascadability.

To aid the designer to choose between the two OTA and CCCII based biquads, it is worthwhile to examine the biquads frequency response based on transistor-level simulation. The characteristic of an OTA is different from that of a CCCII. The simulations have been done to compare the unified OTA-based biquad filter (Fig. 5-26) with the unified CCCII-based biquad filter (Fig. 5-21).

The simulations are carried out for the fourth-order OTA-based and CCCII-based high-pass and all-pass filters, constructed by cascading two unified OTA-based and CCCII-based high-pass and all-pass biquad filters, respectively. The simulations use H-Spice with UMC05 (0.5 μ m) level-49 process and the CMOS implementations, described in Sections 2.1 and 5.1, whose netlists are shown in Appendix 3. The component values are given by $C_1=13.07\text{pF}$, $C_2=7.65\text{pF}$, $C_3=5.41\text{pF}$, $C_4=18.48\text{pF}$, and 125.66 μ S for all transconductances. The fourth-order high-pass simulation results are shown in Figs. 6-5 and 6-6. As can be seen, there is a close agreement between theory and simulation, for example, their simulated lower 3dB frequencies are 1.90MHz (OTA-based) and 1.56MHz (CCCI-based), compared to 2MHz in the ideal case. Their peak values are 0.749dB (OTA-based) and 5.933dB (CCCI-based), compared to 0dB in the ideal case. The super posed diagram of Figs. 6-5 and 6-6 is shown in Fig. 6-7 for better comparison.

On the other hand, the fourth-order all-pass simulation results are shown in Figs. 6-8 and 6-9. As can be seen, there is a close agreement between theory and simulation, for example, their simulated centre frequencies (as phase shift equals 360 $^\circ$) are 1.99MHz (OTA-based) and 1.94MHz (CCCI-based), compared to 2MHz in the ideal case. Their peak values are 1.584dB (OTA-based) and 2.477dB (CCCI-based), compared to 0dB

in the ideal case. The superposed diagrams of Figs. 6-8 and 6-9 is shown in Fig. 6-10 for better comparison.

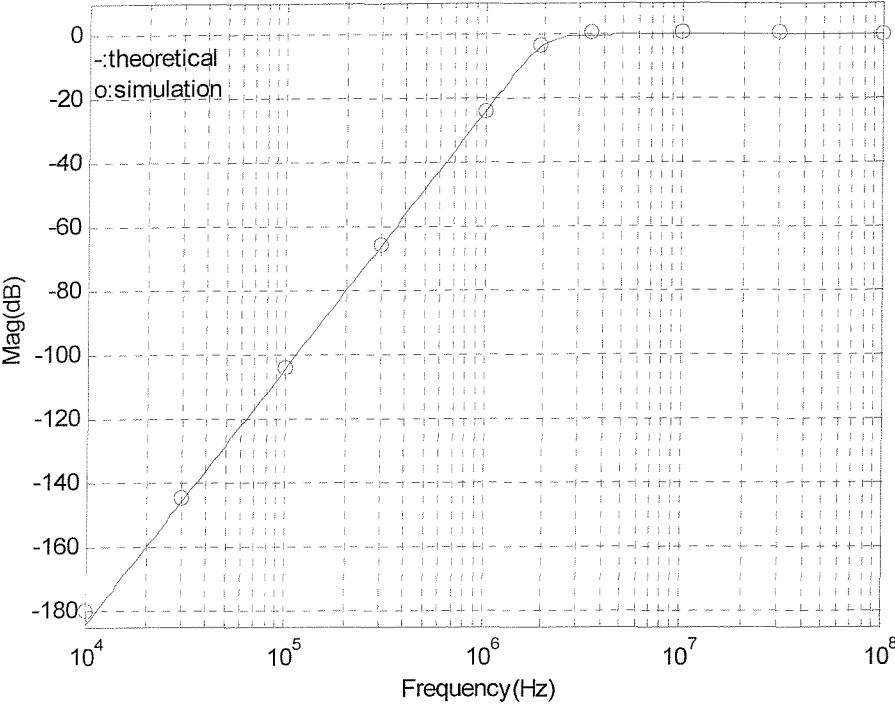


Fig. 6-5 Amplitude-frequency response (OTA-based high-pass)

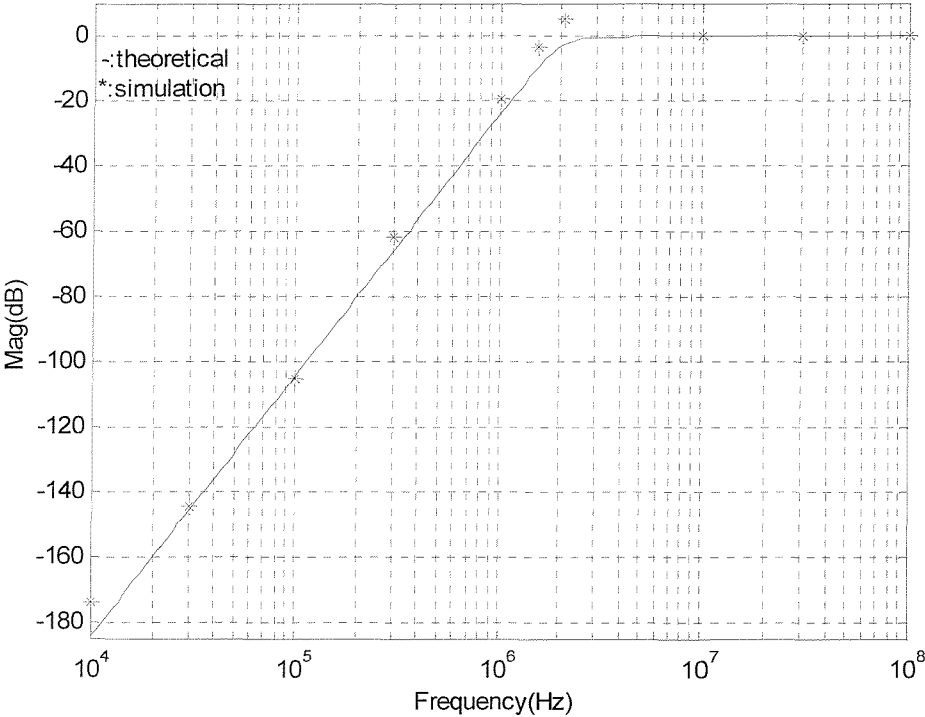


Fig. 6-6 Amplitude-frequency response (CCCII-based high-pass)

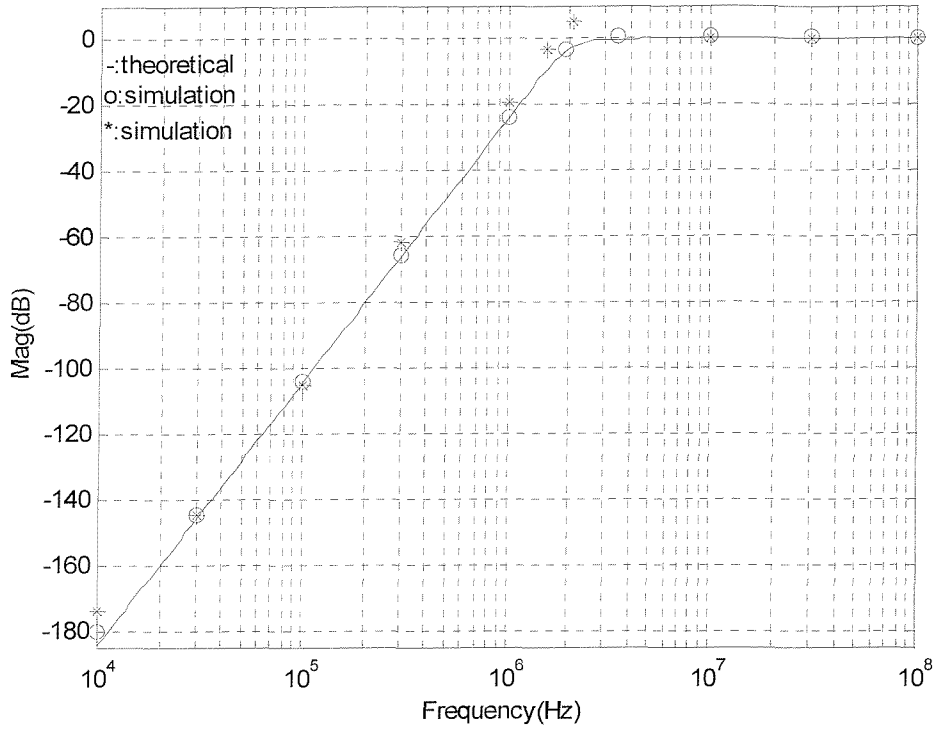


Fig. 6-7 Superposed diagram of Fogs. 6-5 and 6-6

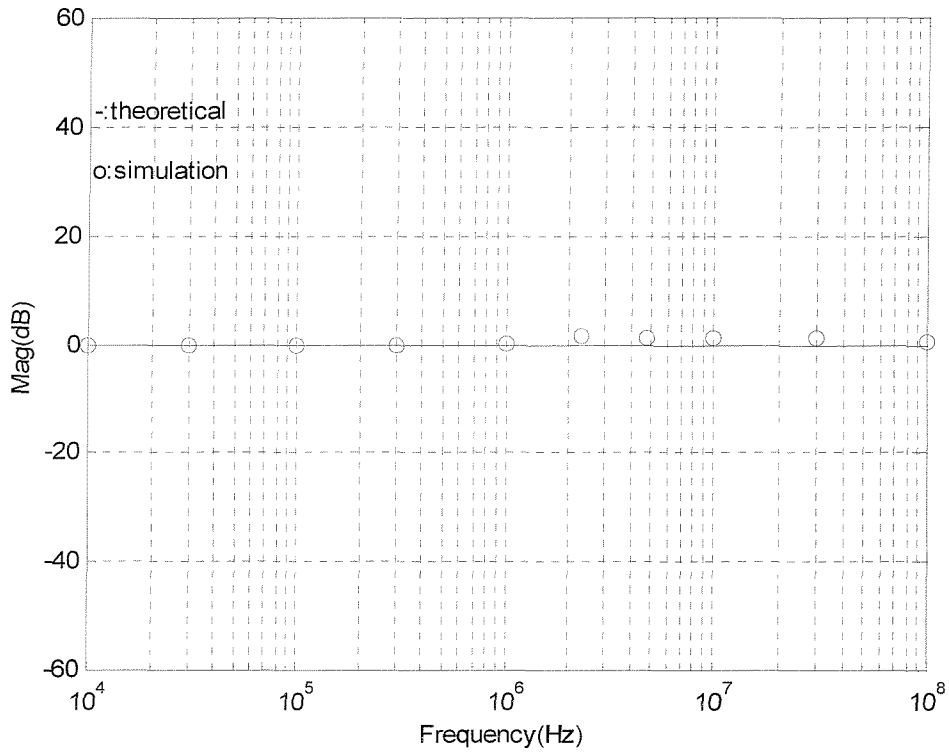


Fig. 6-8 (a) Amplitude-frequency response (OTA-based all-pass)

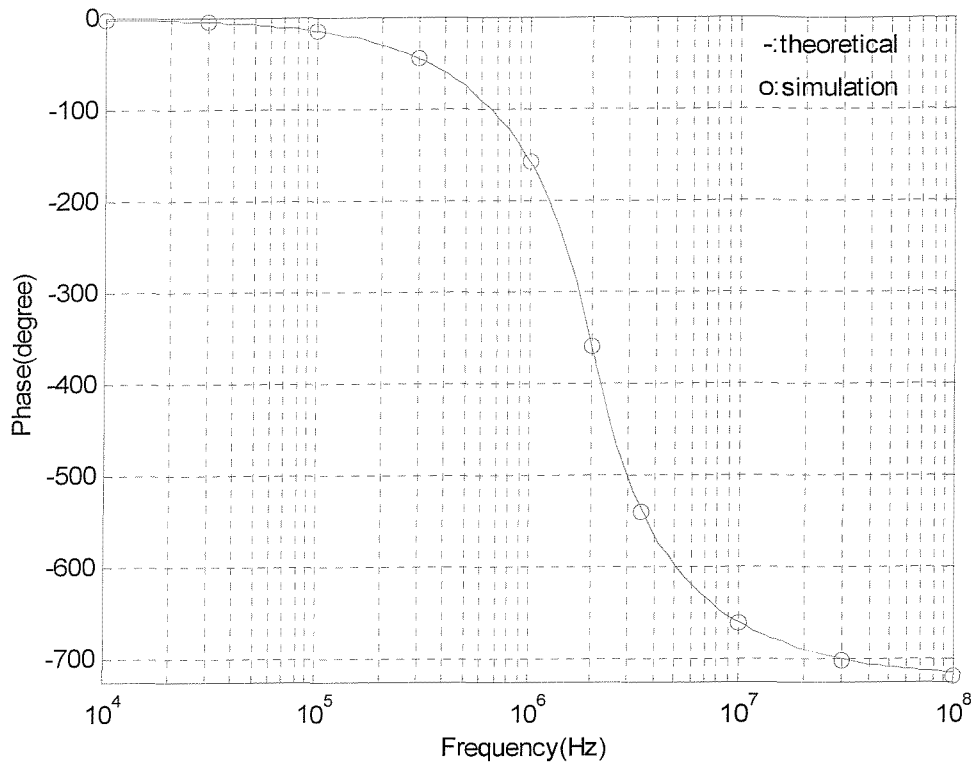


Fig. 6-8 (b) Phase-frequency response (OTA-based all-pass)

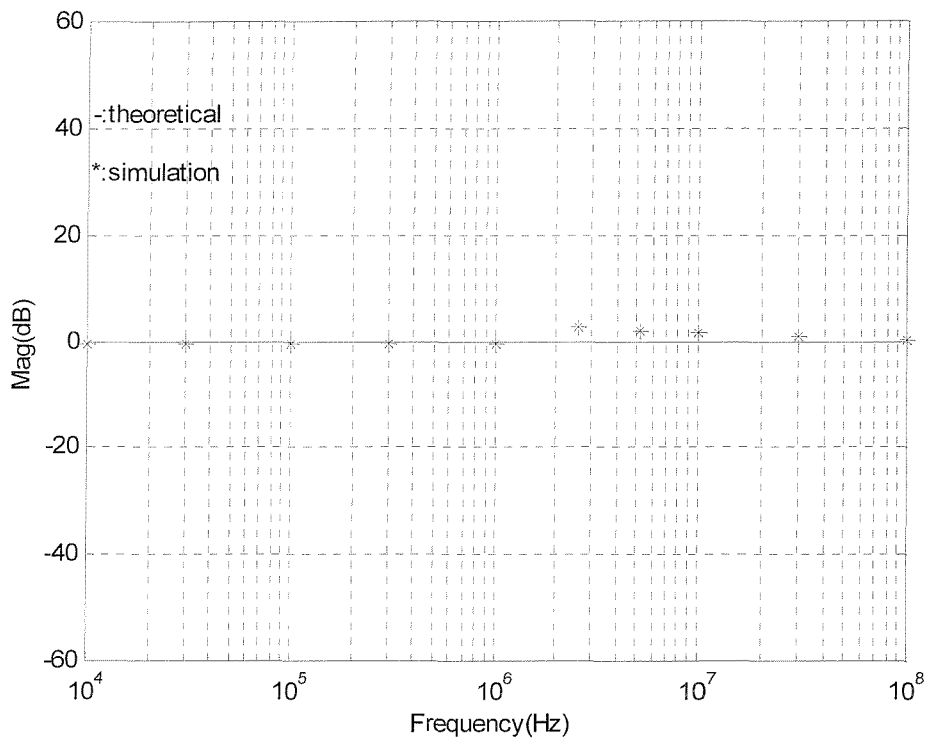


Fig. 6-9 (a) Amplitude-frequency response (CCCII-based all-pass)

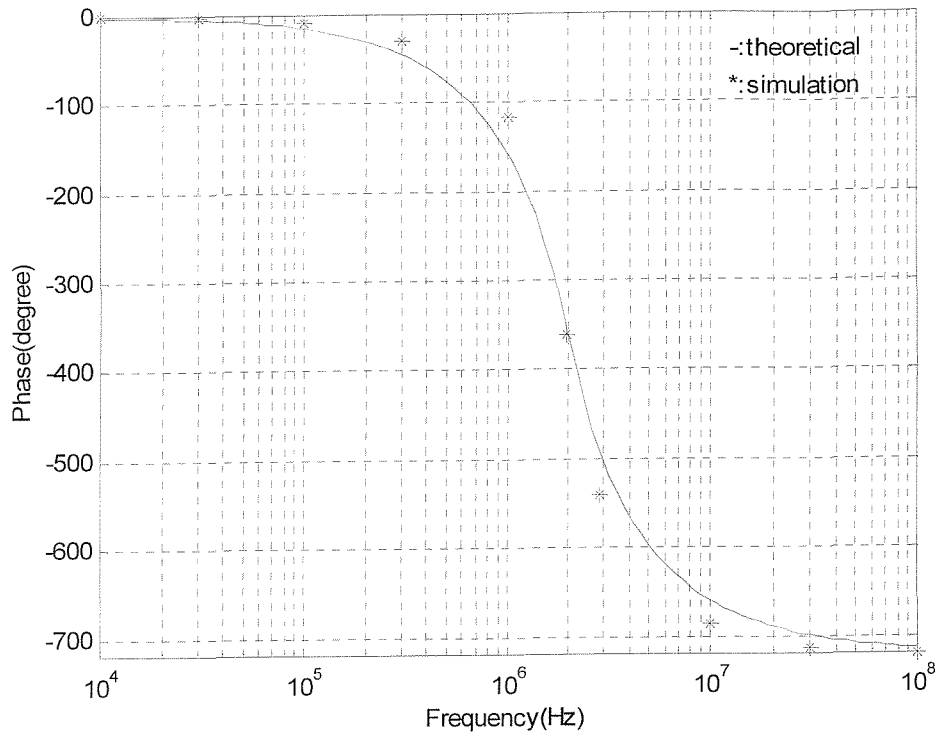


Fig. 6-9 (b) Phase-frequency response (CCCII-based all-pass)

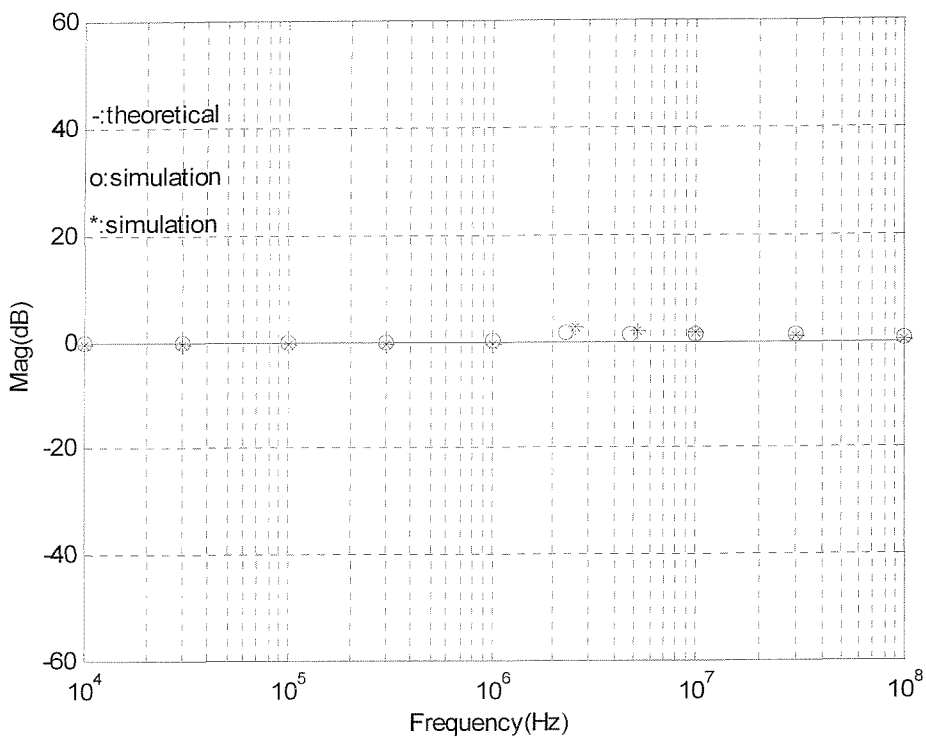


Fig. 6-10 (a) Superposed diagram of Figs. 6-8 (a) and 6-9 (a)

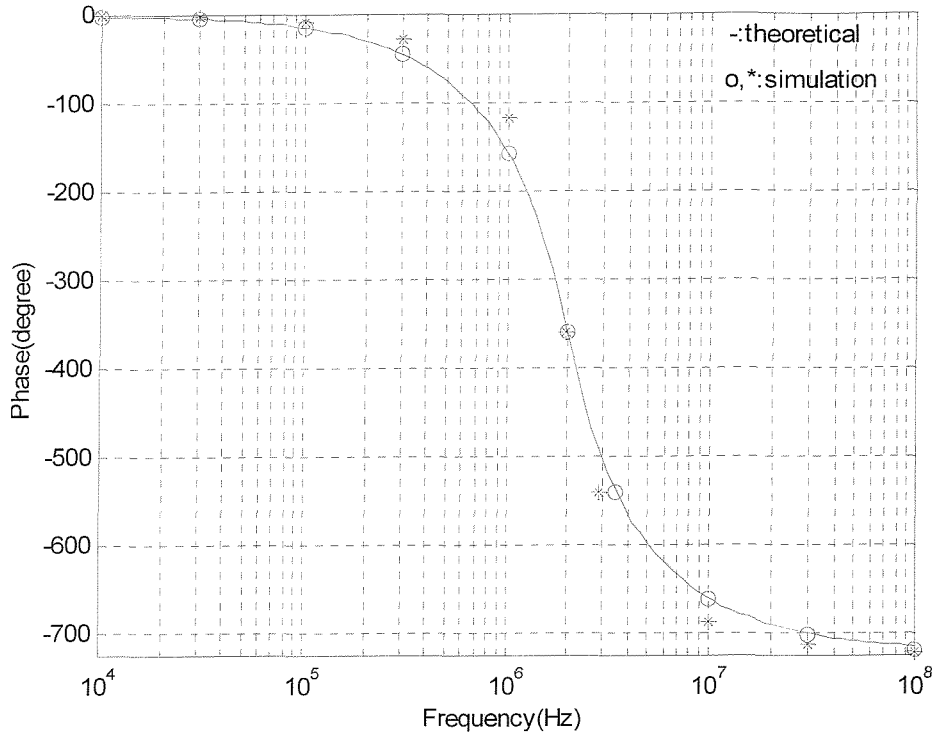


Fig. 6-10 (b) Superposed diagram of Figs. 6-8 (b) and 6-9 (b)

Based on the presented simulation results, it is reasonably accurate to observe the following conclusion. The unified OTA-based biquad filter (Fig. 5-26) produces better filtering responses than the unified CCCII-based biquad filter (Fig. 5-21). The reason is that there are only parasitic capacitances and conductances existed at the input and output ports of an OTA unlike the CCCII with additional parasitic inductance, and non-ideal frequency-dependent current and voltage transfer constraints (referring to Appendix 4).

6.3 Concluding Remarks

This chapter has presented numerous comparisons between the synthesis methods and filter structures outlined in the previous chapters of the thesis. The following conclusions can be drawn:

I: For current mode filters,

- MISOC synthesis method produces circuits that have less or no more transistor count than those produced by DISOC synthesis method.
- DIMOC synthesis method may prove more convenient for digitally programmable filters where filter function is changed by closing and opening the appropriate switches.

II: For voltage mode filters,

- multifunction (low-pass, band-pass, and high-pass) and particular function (all-pass) filter structures (Figs. 4-1 and 4-6, respectively) have less active elements, i.e., OTAs, than arbitrary function filter structure (Fig. 4-4).
- the first filter structure (Fig. 4-1) enjoys the benefit of equal transconductance characteristic.
- the second filter structure can realize all of the filter functions (including elliptic filter functions) and enjoys the advantage of equal capacitance characteristic.

III: For a given filtering function,

- CM filters have less component count than VM filters.
- VM filters enjoy the attractive advantage of equal transconductance or capacitance characteristic which is unavailable for CM filters.

IV: For unified biquad filters, OTA-based biquads perform better in practice than CCCII-based biquad now. In fact, the performances of OTA-based and CCCII-based biquads depend on the performances of the OTA and the CCCII, respectively. The performance of a CCCII may be improved and better than that of an OTA in the future.

Therefore, we may say: “None of the filter structures meet all the designers’ requirements, and different kinds of filter structures are capable of achieving different kinds of advantages”. The above conclusions might aid the designer to do the *preliminary* selection for an appropriate design method and filter structure given a filtering problem and some requirements.

Chapter 7

Conclusion

The main aim of this research has been to investigate and develop new synthesis methods and filter structures that are better than existing methods and circuits. Two types of active elements have been considered, the operational transconductance amplifiers and the current conveyors. Also, two different modes of operation have been investigated, the current-mode and the voltage-mode.

In Chapter 2, the first outcome of the literature review has identified that there are numerous filter biquads based on the OTA and the CCII that operates in voltage-mode and current-mode. The second outcome of the literature review has shown that there exist a number of methods for designing high-order (>2) voltage-mode and current-mode filters. Chapter 2 has concluded that despite the extensive available literature on active filter biquads, it appears that the biquads often trade-offs some performance parameters against others. In particular, the biquads employ excessive number of active and passive elements. The chapter has outlined *five important performance parameters* which biquads should achieve simultaneously if new filtering structures are to be developed. The performance parameters are: (i) universal filtering (low-pass, high-pass, band-pass, notch, and all-pass), (ii) minimum components count (three active elements, two grounded capacitors, and no resistors), (iii) independent ω_o and ω_o/Q tunability, (iv) no need to impose component choice conditions to realize specific filtering functions, and (v) no need to employ additional active elements to provide filter current outputs explicitly. Furthermore, it was concluded in Chapter 2 that the synthesis methods reported in the literature for high-order filters are not thoroughly analytical and ad hoc. The chapter has identified *three main important criteria* (least number of components, single-input OTAs, and grounded capacitors) that high-order filters need to exhibit when developing new synthesis methods.

Chapter 3 presented four design notes (Section 3.2) to develop the new analytical synthesis methods for realizing high-order current-mode filter transfer functions. The first current-mode analytical synthesis method has been developed (Section 3.3) and obtained an n th-order generic filter structure with multiple input currents, and a single output current (MISOC). Section 3.4 has outlined the second current-mode analytical synthesis method and obtained an n th-order generic filter structure with double input currents, and multiple output currents (DIMOC). Both MISOC and DIMOC synthesis methods need a succession of innovative algebra manipulation process to decompose the complex n th-order filter transfer function into n first-order simple equations, all of which are easily realised. It has been shown how the two filter structures (Figs 3-6 and 3-10) synthesized from the MISOC and DIMOC methods achieve the above outlined *three main important criteria*: least number of components, single-input OTAs, and grounded capacitors. Component sensitivities of the filters obtained from the two synthesis methods have been carried out and shown that their ranges are rather low from -1 to 1, demonstrated by simulations shown in Appendix 5. Also, comparison between the two synthesis methods and some recently reported filter structures in terms of component count has been carried out and it has been shown that the proposed synthesis methods produce circuits that employ the least number of passive and active elements for a given filtering function. Indeed, the produced filters are canonical optimal filter structures. The comparison in terms of component spread has also been carried out and it has been shown that the proposed synthesis methods produce circuits that still enjoy rather low component spread although their component spreads are not the lowest. Furthermore, the comparison in terms of cascadability has also been carried out and it has been shown that the proposed synthesis methods produce circuits that enjoy the property of cascadability at the output port as those recently reported work. Finally, Section 3.7 validated the synthesis methods through simulation and found to perform very well.

In order to extend the new analytical synthesis method of Chapter 3 from current mode to voltage mode, an extension approach was presented in Chapter 4. Based upon this extension approach and another innovative algebra manipulation, the first voltage-mode analytical synthesis method has been developed (Section 4.2) and obtained an n th-order general filter structure (Fig. 4-4), employing $2n+2$ single-input OTAs and n

grounded capacitors, which can realize an n th-order arbitrary filtering function, for example, elliptic filter functions, and achieve the above *three main important criteria*. Equal capacitance design prevents the general filter structure (Fig. 4-4) from the difficulty to fabricate accurate capacitors with different values in the integrated circuit [86]. The particular case (Fig. 4-1) of the n th-order general filter structure can realize n th-order low-pass, band-pass, and high-pass filtering functions employing only $n+2$ single-input OTAs and n grounded capacitors, much fewer in component count than the recently reported work [67, 71]. It is valuable to note that equal transconductance design leads to the use of single biasing circuitry. Employing the same number of active and passive components, an n th-order all-pass filter structure (Fig. 4-6) was presented by using the second voltage-mode analytical synthesis method (Section 4.3). Both the two voltage-mode synthesis methods decompose a complex n th-order filter transfer function into n first-order differential equations and one constraint, all of which are easily realized by using a simple circuitry. It has been shown how the three filter structures (Figs 4-1, 4-4 and 4-6) synthesized from the two synthesis methods achieve the above outlined *three main important criteria*. Component sensitivities of the filters obtained from the two synthesis methods have been carried out and shown that their ranges are rather low from -1 to 1, demonstrated by simulations shown in Appendix 5. Also, comparison between the two synthesis methods and some recently reported filter structures in terms of component count has been carried out and it has been shown that the proposed synthesis methods produce circuits that employ the least number of passive and active elements for a given filtering function. Indeed, the produced filters are canonical optimal filter structures. The comparison in terms of component spread has also been carried out and it has been shown that the proposed synthesis methods produce circuits that still enjoy rather low component spread although their component spreads are not the lowest. Furthermore, the comparison in terms of cascadability has also been carried out and it has been shown that the proposed synthesis methods produce circuits that enjoy the property of cascadability at the input port as those recently reported work. Finally, Section 4.6 validated the synthesis methods through simulation and found to perform very well.

Chapter 5 proposed the concept of a *unified* biquad and presented a filter model based on nullators, norators, current mirrors, grounded resistors, and grounded capacitors. Based upon this model, two implementations, an OTA-based and a CCCII-based

biquad filters have been derived. Both implementations produce *unified* biquads and are capable of achieving simultaneously the *five important performance parameters* identified in Chapter 1. The theoretical analysis of the two new biquads has been validated using simulation based on CMOS design of the active elements. Low-pass, high-pass, variable Q band-pass and band-reject filters, and component sensitivity (Appendix 5) have been simulated and performed as expected.

Finally, Chapter 6 presented a comparative analysis between the synthesis methods of Chapter 3 and 4 and the filter biquads of Chapter 5 with the main aim of assisting the designer to develop the appropriate filter circuit given a filtering problem and an implementation style. It is shown that, for current mode filters, MISOC synthesis method produces circuits that have less transistor count than those produced by DISOC synthesis method. For example, the typical 4th-order all-pass filter using MISOC synthesis method, shown in Fig. 3-19, would have 20 fewer transistors than the same type filter using DISOC synthesis method, shown in Fig. 3-21. However, DIMOC synthesis method may prove more convenient for digitally programmable filters where filter function is changed by closing and opening the appropriate switches. For voltage mode filters, multifunction (low-pass, band-pass, and high-pass) and particular function (all-pass) filter structures (Figs. 4-1 and 4-6, respectively) have less active elements, i.e., OTAs, than arbitrary function filter structure (Fig. 4-4). However, the first filter structure (Fig. 4-1) enjoys the benefit of equal transconductance characteristic, and the second filter structure can realize all of the filter functions (including elliptic filter functions) and enjoys the advantage of equal capacitance characteristic [86]. For a given filtering function, CM filters have less component count than VM filters. However, VM filters enjoy the attractive advantage of equal transconductance or capacitance characteristic which is unavailable for CM filters. For *unified* biquad filters, OTA-based biquads perform better in practice than CCCII-based biquad now. However, the situation may be changed as the performance of a CCCII is improved much better than that of an OTA someday. The final concluding remark of this Chapter is that none of the proposed filter structures have achieved all the requirements. Different kinds of filter structures meet different kinds of necessities.

This research has shown that analytical synthesis approach provides a method by which n th-order filters of different responses can be developed systematically and synthesized using simple circuitry resulting in optimal circuits in terms of passive and active component count. Furthermore the produced filter circuits are capable of achieving the other two main criteria: grounded capacitors and single-input OTAs and the two more attractive VLSI realizations: equal transconductance and equal capacitance for two new voltage-mode filter structures. This research has also demonstrated how a filter model based on nullators and norators can facilitate the development of two unified biquads that are capable of achieving simultaneously a number of key important performance parameters and without trade-offs. Therefore, it is hoped that the methods and structures proposed in this thesis, and validated through transistor-level simulation, will contribute to the area of analogue signal processing and IC design in general and more specifically to filter synthesis and design.

Future Research Directions

Based on the work performed in this thesis, a number of future research directions are outlined next.

Current Conveyor-Based Analytical Synthesis Methods: Due to the recent improvement of the characteristics of a CCII [88], a low power class AB circuit realisation implemented in $1.2\mu\text{m}$ CMOS technique, to investigate and develop the analytical synthesis methods using CCIIs is a complimentary part of those using OTAs and is a valuable prospective research work.

Analytical Synthesis of Elliptic Filters: The presented synthesis methods have targeted all-pole filters and notch responses. Elliptic filters are normally employed when sharp filtering responses are needed, it would be worthwhile to extend the presented analytical synthesis to design such filters directly. This presents some of the following challenges: some more complicated decompositions for the high-order current-mode and voltage-mode elliptic filter transfer functions and the need to achieve the *three main important criteria* simultaneously described in Chapter 1. Therefore, this requires further investigation.

Alternative Approaches of the Norator and Nullator-Based Biquad Filter Model (Fig. 5-19): Different types of norators and different topologies of the circuit structures constructed by norators and nullators may achieve the same theoretical response. To investigate all of the type combinations and structure topologies is helpful for understanding their insight into the filter's behaviour and helpful for developing new synthesis approaches of the norator and nullator-based models.

Design Automation of Filters: As shown in Chapters 3 and 4, synthesis methods for designing n th-order current-mode and voltage-mode filters with different responses can be used. There has always been interested in design automation of analogue IC design. Since the presented synthesis methods are focused on solving a complex n th-order filter transfer function, it would be interesting to investigate the possibility of developing a CAD tool that incorporates the proposed synthesis methods. Also, it would be of extra value if the synthesis methods and the transistor level designs are combined so that optimisation can be carried out on the way into which component scaling is performed as the best.

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Appendix 1

Example of New Voltage-Mode Analytical Synthesis Method

The detailed synthesis process to realize the following second-order voltage transfer function (which is also shown in Eq. (2-10))

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{a_2s^2 + a_1s + a_0}{b_2s^2 + b_1s + b_0} \quad (\text{A1-1})$$

is shown step by step as below.

Step 1: Use the first voltage-mode synthesis method presented in Section 4.2. Suppose that there are three output voltages in the synthesized circuit whose voltages are

$$V_{out(i)} = V_{in} \left(\frac{b_i s^i}{\Delta} \right), \text{ for } i = 0, 1, 2, \quad (\text{A1-2})$$

where $\Delta = b_2s^2 + b_1s + b_0$.

Step 2: From Eq. (A1-2), we have

$$V_{out(i)} = V_{out(0)} \left(\frac{b_i s^i}{b_0} \right) \quad (i = 1, 2) \quad (\text{A1-3})$$

and

$$V_{out(i)} = V_{out(i-1)} \left(\frac{b_i s}{b_{i-1}} \right) \quad (i = 1, 2) \quad (\text{A1-4})$$

Combining Eq. (A1-3) with Eq. (A1-4) yields

$$V_{out(i)} = V_{out(0)} \left(\frac{b_i s^i}{b_0} \right) = V_{out(i-1)} \left(\frac{b_i s}{b_{i-1}} \right); \quad (i = 1, 2) \quad (\text{A1-5})$$

Step 3: If $i = 0$, Eq. (A1-2) becomes

$$V_{out(0)} = \frac{b_0 V_{in}}{b_2 s^2 + b_1 s + b_0} \quad (\text{A1-6})$$

Cross multiply Eq. (A1-6), divide it by b_0 , and rearrange,

$$V_{out(0)} \left(\frac{b_2 s^2}{b_0} \right) = V_{in} - V_{out(0)} - V_{out(0)} \left(\frac{b_1 s}{b_0} \right) \quad (\text{A1-7})$$

Step 4: Substituting Eq. (A1-5) into Eq. (A1-7) gives

$$V_{in} - V_{out(0)} = \sum_{i=1}^2 V_{out(i-1)} \left(\frac{b_i s}{b_{i-1}} \right) \quad (\text{A1-8})$$

Step 5: Eq. (A1-8) is a voltage relationship. In order to be consistent with the input-and-output current relationship of an OTA, i.e., $(V_+ - V_-)g_m = I_{out}$, we multiply each side of Eq. (A1-8) by an equal transconductance of unity value (1), leading to

$$\left(V_{in} - V_{out(0)} \right) (1) = \sum_{i=1}^2 V_{out(i-1)} \left(\frac{b_i s}{b_{i-1}} \right) (1) = \sum_{i=1}^2 V_{out(i-1)} \left[\left(\frac{b_i s}{b_{i-1}} \right) / (1) \right] (1) \quad (\text{A1-9})$$

Then, Eq. (A2-4) can be derived as $V_{out(i)} = V_{out(i-1)} \left[\left(\frac{b_i s}{b_{i-1}} \right) / (1) \right] \quad (i = 1, 2)$,

namely,
$$V_{out(i)}(1) = V_{out(i-1)} \left(\frac{b_i s}{b_{i-1}} \right) \quad (i = 1, 2). \quad (\text{A1-10})$$

Step 6: Substituting Eq. (A1-10) into Eq. (A1-9) yields

$$(V_{in} - V_{out(0)})(1) = \sum_{i=1}^2 V_{out(i)}(1) \quad (\text{A1-11})$$

Step 5: Realize the simple equations, i.e., Eqs. (A1-10) and (A1-11), and combine all the realized circuit structures. The preliminary synthesized filter structure is shown as below.

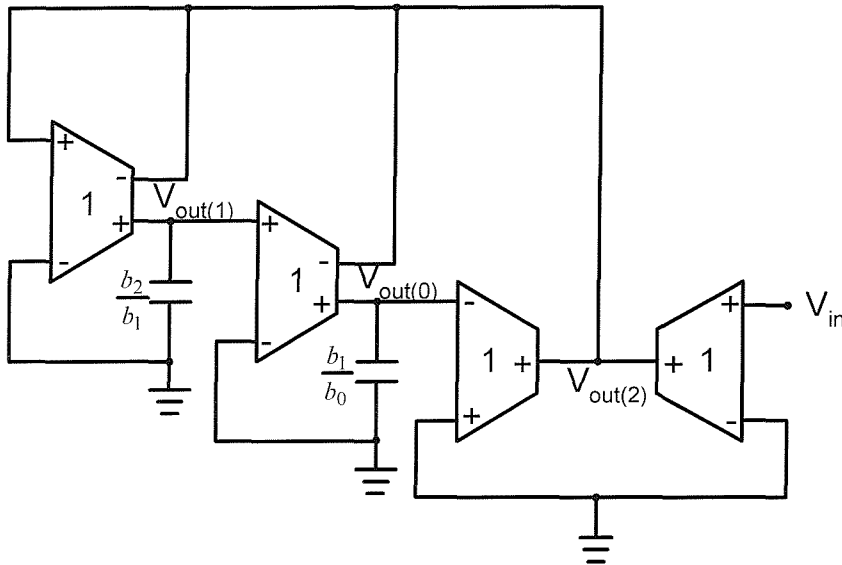


Fig. A1-1 Preliminary synthesized filter structure

Step 6: Because
$$H(s) = \frac{V_{out}}{V_{in}} = \frac{a_2 s^2 + a_1 s + a_0}{b_2 s^2 + b_1 s + b_0} = \sum_{i=0}^2 \left[\left(V_{in} \frac{a_i}{b_i} \right) \left(\frac{b_i s^i}{\Delta} \right) \right] \quad (\text{A1-12})$$

where $\Delta = b_2 s^2 + b_1 s + b_0$. The physical meaning of the above relationship is “to insert different weights of the input voltage signal, V_{in} , into each node in the filter structure shown in Fig. A1-1 and then obtain the output voltage signal”. According to this approach, giving a forward signal, with a weight of input voltage signal, from input voltage node to each inner node in the filter structure shown in Fig. A1-1, we obtain the

other new OTA-C filter structure, shown in Fig. A1-2, for realizing the general second-order voltage transfer function shown in Eq. (A1-1). The realized circuit structure uses 6 single-input OTAs and 2 grounded capacitors simpler in structure than 8 single-input OTAs and 2 grounded capacitors in Fig. 2-3.

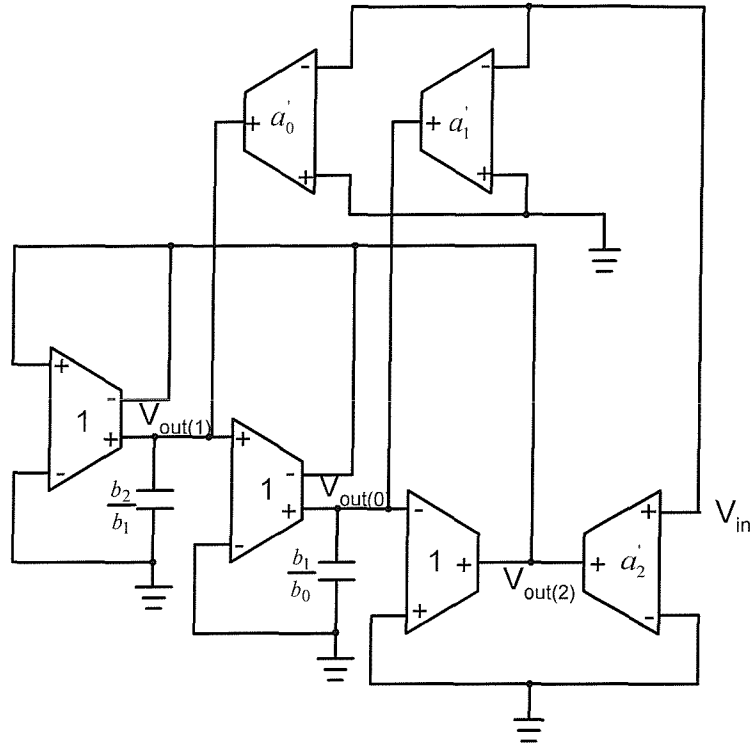


Fig. A1-2 Synthesized filter structure of Eq. (A1-1)

$$\text{Routine analysis yields } \frac{V_{out(2)}}{V_{in}} = \frac{(a_2' b_2) s^2 + \left(a_0' b_1 + a_1' \frac{b_2 b_0}{b_1} \right) s + a_0'}{b_2 s^2 + b_1 s + b_0} \quad (\text{A1-13})$$

in which $a_2' b_2 = a_2$,

$$a_0' b_1 + a_1' \frac{b_2 b_0}{b_1} = a_1,$$

$$a_0' = a_0. \quad (\text{A1-14})$$

Appendix 2

Theory of Cascadability

The theory is used for the reference of Secs. 3-6 and 4-5.

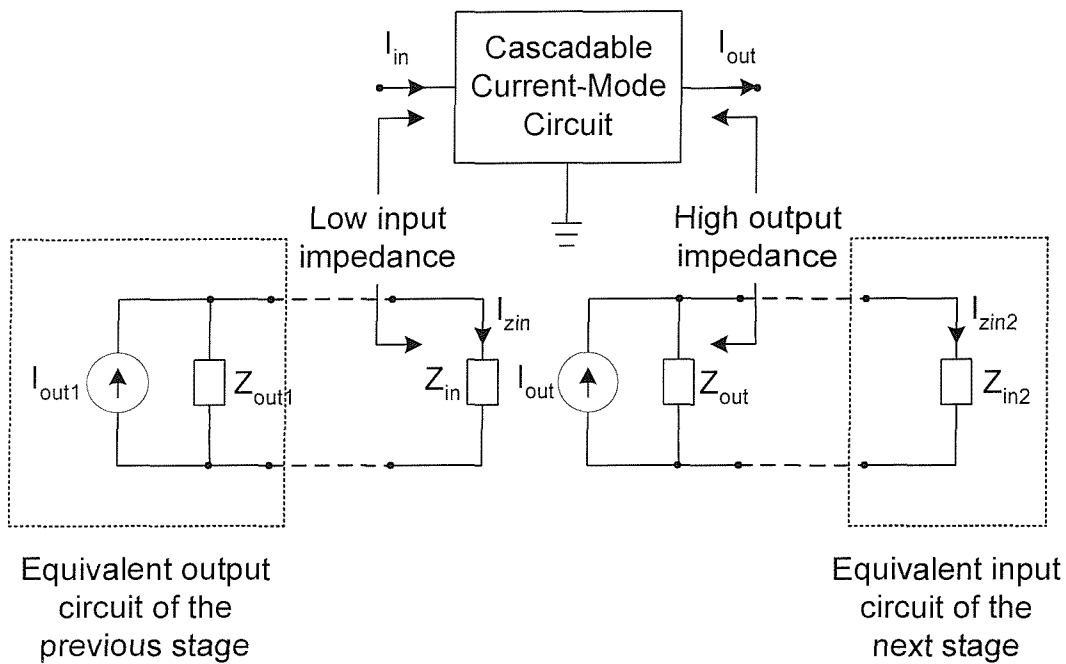


Fig. A2-1 Input and output relationships of a cascable current-mode circuit

Figs. A2-1 and A2-2 show the impedance requirements for cascable current-mode and voltage-mode circuit structures, respectively.

The impedance requirements for cascable current-mode circuit structures are

- (i) Low input impedance which leads to

$$I_{zin} = I_{out1} \left(\frac{Z_{out1}}{Z_{out1} + Z_{in}} \right) \cong I_{out1} \left(\frac{Z_{out1}}{Z_{out1} + 0} \right) = I_{out1} \quad (\text{A2-1})$$

The 0 in Eq. (A2-1) is the value as the low input impedance approaches zero. Hence, the lower the input impedance of a current-mode circuit structure is the better for the cascade with the previous stage.

(ii) High output impedance which leads to

$$I_{zin2} = I_{out} \left(\frac{Z_{out}}{Z_{out} + Z_{in2}} \right) \cong I_{out} \left(\frac{\infty}{\infty + Z_{in2}} \right) = I_{out} \quad (\text{A2-2})$$

The ∞ in Eq. (A2-2) is the value as the high output impedance approaches infinity. Hence, the higher the output impedance of a current-mode circuit structure is the better for the cascade with the next stage.

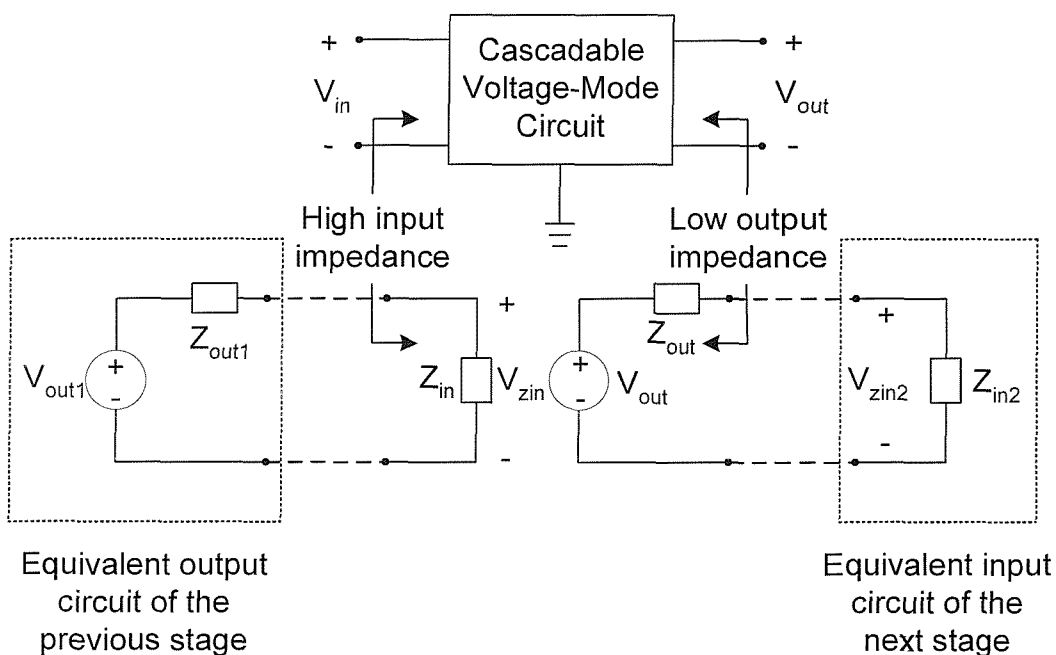


Fig. A2-2 Input and output relationships of a cascadable voltage-mode circuit

On the other hand, the impedance requirements for cascadable voltage-mode circuit structures are

(iii) High input impedance which leads to

$$V_{zin} = V_{out1} \left(\frac{Z_{in}}{Z_{out1} + Z_{in}} \right) \cong V_{out1} \left(\frac{\infty}{Z_{out1} + \infty} \right) = V_{out1} \quad (\text{A2-3})$$

The ∞ in Eq. (A2-3) is the value asf the high input impedance approaches infinity. Hence, the higher the input impedance of a voltage-mode circuit structure is the better for the cascade with the previous stage.

(iv) Low output impedance which leads to

$$V_{zin2} = V_{out} \left(\frac{Z_{in2}}{Z_{out} + Z_{in2}} \right) \cong V_{out} \left(\frac{Z_{in2}}{0 + Z_{in2}} \right) = V_{out} \quad (\text{A2-4})$$

The 0 in Eq. (A2-4) is the value as the low output impedance approaches zero. Hence, the lower the output impedance of a voltage-mode circuit structure is the better for the cascade with the next stage.

Otherwise, a current or voltage buffer is needed for the cascade with the previous or next stage.

Appendix 3

H-SPICE Netlists

In this Appendix, two netlists needed in Section 6.2 are listed as follows for exhibiting the details of H-Spice transistor-level simulations for the two fourth-order high-pass filters, constructed by cascading two unified OTA and CCCII based high-pass biquads, shown in Figs. 5-26 and 5-21 respectively. The simulations use UMC05 (0.5 μ m) level-49 process and the CMOS implementations, described in Sections 2.1 and 5.1. The component values are given by $C_1=13.07\text{pF}$, $C_2=7.65\text{pF}$, $C_3=5.41\text{pF}$, $C_4=18.48\text{pF}$ and $125.66\mu\text{S}$ for all transconductances.

Schematics Netlist I: Fourth-order unified OTA-based high-pass filter

```
* Schematics Netlist *

.protect
.lib 'c:\avanti\Hspice2001.4\lib\umc05.lib' pm
.lib 'c:\avanti\Hspice2001.4\lib\umc05.lib' nm
.unprotect

.global vdd vss
vdd vdd 0 2.5
vss vss 0 -2.5

.subckt otal+ v1+ v1- io1
M_M5          N_0002  N_0002  N_0001 vss nm
+ L=1u
+ W=5u
M_M6          N_0001  N_0001 vss vss nm
+ L=1u
+ W=5u
```

```

M_M13          N_0004 v1+  N_0003 vss nm
+ L=1u
+ W=5u
M_M14          N_0005 v1-  N_0003 vss nm
+ L=1u
+ W=5u
M_M1          io1  N_0004  N_0006 vdd pm
+ L=1u
+ W=10u
M_M3           io1  N_0002  N_0007 vss nm
+ L=1u
+ W=5u
M_M4           N_0007  N_0001 vss vss nm
+ L=1u
+ W=5u
M_M2           N_0006  N_0008 vdd vdd pm
+ L=1u
+ W=10u
M_M7           N_0004  N_0004  N_0008 vdd pm
+ L=1u
+ W=10u
M_M8           N_0008  N_0008 vdd vdd pm
+ L=1u
+ W=10u
M_M9           N_0010  N_0009 vdd vdd pm
+ L=1u
+ W=10u
M_M10          N_0009  N_0009 vdd vdd pm
+ L=1u
+ W=10u
M_M11          N_0002  N_0005  N_0010 vdd pm
+ L=1u
+ W=10u
M_M12          N_0005  N_0005  N_0009 vdd pm
+ L=1u
+ W=10u
I_I1           N_0003 vss DC 35.905u
.ends

```

```

.subckt ota2+ x y io1 io2
M_M1          N_0002  N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M2          N_0004  N_0003  N_0002 vdd pm
+ L=1u
+ W=10u
M_M3          N_0001  N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M4          N_0003  N_0003  N_0001 vdd pm
+ L=1u

```

```

+ W=10u
M_M5          N_0005  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M6          N_0006  N_0006  N_0005 vdd pm
+ L=1u
+ W=10u
M_M7          N_0003  y  N_0007  vss nm
+ L=1u
+ W=5u
M_M8          N_0006  x  N_0007  vss nm
+ L=1u
+ W=5u
M_M9          N_0004  N_0004  N_0008 vss nm
+ L=1u
+ W=5u
M_M10         N_0008  N_0008  vss vss nm
+ L=1u
+ W=5u
M_M11         N_0009  N_0008  vss vss nm
+ L=1u
+ W=5u
M_M12         N_0010  N_0008  vss vss nm
+ L=1u
+ W=5u
M_M13         io1  N_0004  N_0009  vss nm
+ L=1u
+ W=5u
M_M14         io2  N_0004  N_0010  vss nm
+ L=1u
+ W=5u
M_M15         N_0011  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M16         N_0012  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M17         io2  N_0006  N_0012  vdd pm
+ L=1u
+ W=10u
M_M18         io1  N_0006  N_0011  vdd pm
+ L=1u
+ W=10u
I_I1          N_0007  vss DC 35.905u
.ends

.subckt ota3+ x y io1 io2 io3
M_M1          N_0002  N_0001  vdd vdd pm
+ L=1u
+ W=10u
M_M2          N_0004  N_0003  N_0002 vdd pm

```

```

+ L=1u
+ W=10u
M_M3          N_0001  N_0001  vdd vdd pm
+ L=1u
+ W=10u
M_M4          N_0003  N_0003  N_0001 vdd pm
+ L=1u
+ W=10u
M_M5          N_0005  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M6          N_0006  N_0006  N_0005 vdd pm
+ L=1u
+ W=10u
M_M7          N_0007  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M8          io1   N_0006  N_0007 vdd pm
+ L=1u
+ W=10u
M_M9          N_0008  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M10         io2   N_0006  N_0008 vdd pm
+ L=1u
+ W=10u
M_M11         N_0009  N_0005  vdd vdd pm
+ L=1u
+ W=10u
M_M12         io3   N_0006  N_0009 vdd pm
+ L=1u
+ W=10u
M_M13         N_0004  N_0004  N_0010 vss nm
+ L=1u
+ W=5u
M_M14         N_0010  N_0010  vss vss nm
+ L=1u
+ W=5u
M_M15         N_0003  y   N_0011 vss nm
+ L=1u
+ W=5u
M_M16         N_0006  x   N_0011 vss nm
+ L=1u
+ W=5u
M_M17         io1   N_0004  N_0012 vss nm
+ L=1u
+ W=5u
M_M18         N_0012  N_0010  vss vss nm
+ L=1u
+ W=5u
M_M19         io2   N_0004  N_0013 vss nm

```

```

+ L=1u
+ W=5u
M_M20          N_0013  N_0010 vss vss nm
+ L=1u
+ W=5u
M_M21          io3   N_0004  N_0014 vss nm
+ L=1u
+ W=5u
M_M22          N_0014  N_0010 vss vss nm
+ L=1u
+ W=5u
I_I1           N_0011 vss DC 35.905u
.ends

```

```
x1 0 v1 v1 v5 v3 ota3+
```

```
x2 v2 0 v1 v5 v3 ota3+
```

```
x3 0 v1 v2 ota1+
```

```
x4 0 v3 v3 v5 ota2+
```

```
x5 v4 0 v3 v5 ota2+
```

```
x6 0 v3 v4 ota1+
```

```
ro v5 0 1u
```

```
c1 v1 0 13.07p
```

```
c2 v2 0 7.65p
```

```
c3 v3 0 5.41p
```

```
c4 v4 0 18.48p
```

```
i1 0 v1 ac 1m
```

```
i3 0 v3 ac 1m
```

```
i5 0 v5 ac 1m
```

```
.ac dec 150 10k 100x
```

```
.print im(ro) ip(ro)
```

```
.end
```

Schematics Netlist II: Fourth-order unified CCCII-based high-pass filter

```
* Schematics Netlist *
```

```
.protect
```

```

.lib 'c:\avanti\Hspice2001.4\lib\umc05.lib' pm
.lib 'c:\avanti\Hspice2001.4\lib\umc05.lib' nm
.unprotect

.global vdd vss
vdd vdd 0 2.5
vss vss 0 -2.5

.subckt cccii1+ x y z+
M_M7          N_0001 N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M6          N_0002 N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M5          N_0003 N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M3          N_0004 N_0004 vdd vdd pm
+ L=1u
+ W=10u
M_M4          z+ N_0004 vdd vdd pm
+ L=1u
+ W=10u
M_M8          N_0005 N_0005 y y pm
+ L=1u
+ W=10u
M_M9          N_0006 N_0005 x x pm
+ L=1u
+ W=10u
M_M12         N_0002 N_0002 vss vss nm
+ L=1u
+ W=5u
M_M13         N_0005 N_0002 vss vss nm
+ L=1u
+ W=5u
M_M15         N_0006 N_0006 vss vss nm
+ L=1u
+ W=5u
M_M14         z+ N_0006 vss vss nm
+ L=1u
+ W=5u
M_M11         N_0003 N_0003 y y nm
+ L=1u
+ W=5u
M_M10         N_0004 N_0003 x x nm
+ L=1u
+ W=5u
I_I1          N_0001 0 DC 3.517u
.ends

```

```

.subckt cccli2+ x y z1+ z2+
M_M7          N_0001  N_0001  vdd vdd pm
+ L=3u
+ W=10u
M_M6          N_0002  N_0001  vdd vdd pm

+ L=3u
+ W=10u
M_M5          N_0003  N_0001  vdd vdd pm
+ L=3u
+ W=10u
M_M8          N_0004  N_0004  y y pm
+ L=3u
+ W=10u
M_M9          N_0005  N_0004  x x pm
+ L=3u
+ W=10u
M_M12         N_0002  N_0002  vss vss nm
+ L=3u
+ W=5u
M_M13         N_0004  N_0002  vss vss nm
+ L=3u
+ W=5u
M_M11         N_0003  N_0003  y y nm
+ L=3u
+ W=5u
M_M10         N_0006  N_0003  x x nm
+ L=3u
+ W=5u
M_M15         N_0005  N_0005  vss vss nm
+ L=3u
+ W=5u
M_M14         z1+  N_0005  vss vss nm
+ L=3u
+ W=5u
M_M17         z2+  N_0005  vss vss nm
+ L=3u
+ W=5u
M_M3          N_0006  N_0006  vdd vdd pm
+ L=3u
+ W=10u
M_M4          z1+  N_0006  vdd vdd pm
+ L=3u
+ W=10u
M_M16         z2+  N_0006  vdd vdd pm
+ L=3u
+ W=10u
I_I1          N_0001  0  DC 3.517u
.ends

```

```

.subckt cccli3+ x y z1 z2 z3

```



```

M_M7          N_0001  N_0001  vdd vdd pm
+ L=1u
+ W=10u
M_M6          N_0002  N_0001  vdd vdd pm
+ L=1u
+ W=10u
M_M5          N_0003  N_0001  vdd vdd pm
+ L=1u
+ W=10u
M_M8          N_0004  N_0004  y y pm
+ L=1u
+ W=10u
M_M9          N_0005  N_0004  x x pm
+ L=1u
+ W=10u
M_M12         N_0002  N_0002  vss vss nm
+ L=1u
+ W=5u
M_M13         N_0004  N_0002  vss vss nm
+ L=1u
+ W=5u
M_M11         N_0003  N_0003  y y nm
+ L=1u
+ W=5u
M_M10         N_0006  N_0003  x x nm
+ L=1u
+ W=5u
M_M3          N_0006  N_0006  vdd vdd pm
+ L=1u
+ W=10u
M_M4          z1  N_0006  vdd vdd pm
+ L=1u
+ W=10u
M_M16         z2  N_0006  vdd vdd pm
+ L=1u
+ W=10u
M_M18         z3  N_0006  vdd vdd pm
+ L=1u
+ W=10u
M_M15         N_0005  N_0005  vss vss nm
+ L=1u
+ W=5u
M_M14         z1  N_0005  vss vss nm
+ L=1u
+ W=5u
M_M17         z2  N_0005  vss vss nm
+ L=1u
+ W=5u
M_M19         z3  N_0005  vss vss nm
+ L=1u
+ W=5u

```

```

I_I1          N_0001 0 DC 3.517u
.ends

.subckt cccii1- x y z-
M_M7          N_0001 N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M6          N_0002 N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M5          N_0003 N_0001 vdd vdd pm
+ L=1u
+ W=10u
M_M3          N_0004 N_0004 vdd vdd pm
+ L=1u
+ W=10u
M_M17         N_0005 N_0005 vdd vdd pm
+ L=1u
+ W=10u
M_M18         z- N_0005 vdd vdd pm
+ L=1u
+ W=10u
M_M8          N_0006 N_0006 y y pm
+ L=1u
+ W=10u
M_M9          N_0007 N_0006 x x pm
+ L=1u
+ W=10u
M_M11         N_0003 N_0003 y y nm
+ L=1u
+ W=5u
M_M10         N_0004 N_0003 x x nm
+ L=1u
+ W=5u
M_M12         N_0002 N_0002 vss vss nm
+ L=1u
+ W=5u
M_M13         N_0006 N_0002 vss vss nm
+ L=1u
+ W=5u
M_M15         N_0007 N_0007 vss vss nm
+ L=1u
+ W=5u
M_M14         N_0005 N_0007 vss vss nm
+ L=1u
+ W=5u
M_M16         N_0008 N_0008 vss vss nm
+ L=1u
+ W=5u
M_M19         z- N_0008 vss vss nm
+ L=1u

```

```
+ W=5u
M_M4          N_0008 N_0004 vdd vdd pm
+ L=1u
+ W=10u
I_I1          N_0001 0 DC 2.3385u
.ends
```

```
x1 v1 0 v5 v3 cccii2+
```

```
x2 0 v2 v1 v3 v5 cccii3+
```

```
x3 0 v1 v2 cccii1-
```

```
x4 v3 0 v5 cccii1+
```

```
x5 0 v4 v3 v5 cccii2+
```

```
x6 0 v3 v4 cccii1-
```

```
ro v5 0 1u
```

```
c1 v1 0 13.07p
```

```
c2 v2 0 7.65p
```

```
c3 v3 0 5.41p
```

```
c4 v4 0 18.48p
```

```
i1 0 v1 ac 1m
```

```
i3 0 v3 ac 1m
```

```
i5 0 v5 ac 1m
```

```
.ac dec 150 10k 100x
```

```
.print im(ro) ip(ro)
```

```
.alter
```

```
c1 v1 0 5.41p
```

```
c2 v2 0 18.48p
```

```
c3 v3 0 13.07p
```

```
c4 v4 0 7.65p
```

```
.end
```

Appendix 4

Non-ideal Comparison between Unified OTA and CCCII-Based Biquad Filters

Numerous publications have reported non-ideal effects of OTA-C filters. One of the most recent is [13]. The non-ideal effects [13] of the CMOS OTA include (i) frequency dependent transconductances $A_j(s)$ which can be reasonably represented as $g_j(1 - sT_j)$, (ii) input parasitic capacitances C'_{ipj} , (iii) output parasitic capacitances C'_{opj} , (iv) node parasitic capacitances C'_{npj} , and (v) output parasitic conductances G'_{opj} . If we insert the frequency dependent transconductances and the parasitic capacitances and conductances into the circuit structure shown in Fig. 5-26, the non-ideal circuit structure of the *unified* OTA-based biquad filter is shown in Fig. A4-1 in which C'_j represent the sum of capacitance of the given capacitor and the parasitic capacitances presenting at that position, and G'_j represent the sum of all parasitic conductances presenting at that position.

In Fig. A4-1, $C'_1 = C'_{ip1} + C'_{ip3} + C'_{op1} + C'_{op2} + C'_{np1} + C_1$, $C'_2 = C'_{ip2} + C'_{op3} + C'_{np2} + C_2$,

$G'_1 = G'_{op1} + G'_{op2}$, and $G'_2 = G'_{op3}$, where C_1 and C_2 are given capacitances.

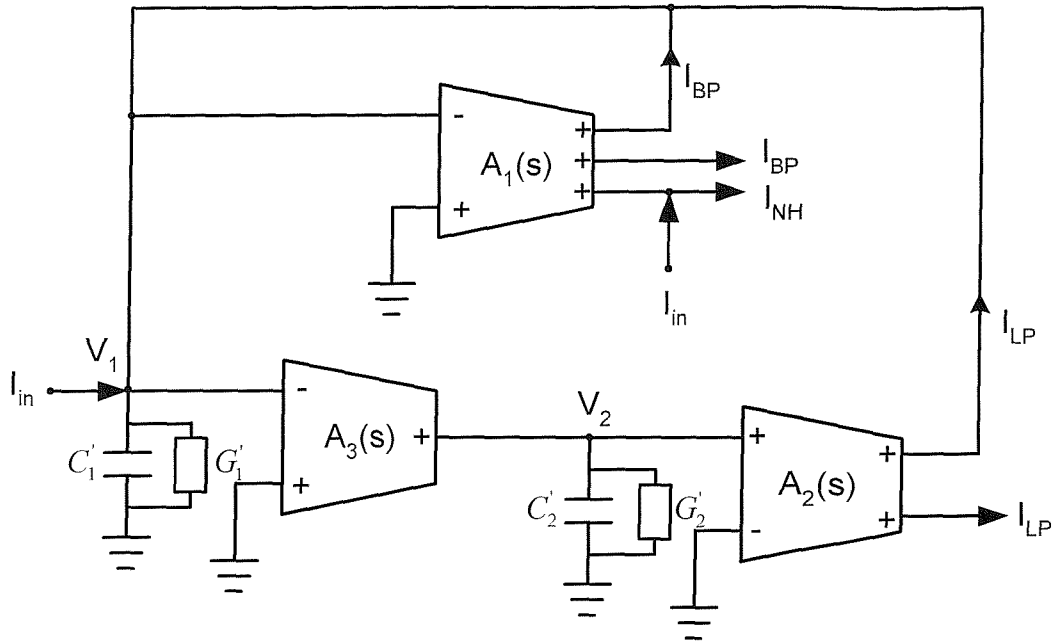


Fig. A4-1 Non-ideal implementation of the *unified* OTA-based biquad filter

On the other hand, in 1997, Fabre et al. presented a general non-ideal CCCII model [87] which includes (i) a parasitic inductance L_x in series with the intrinsic resistance R_x , (ii) a grounded parasitic capacitance C_y in parallel with a grounded parasitic conductance G_y at the terminal y , (iii) a grounded parasitic capacitance C_z in parallel with a grounded parasitic conductance G_z at the terminal z , (iv) a voltage transfer function $\beta(s)$, which equals $\beta/(1+s/\omega_\beta)$, such that $V_x = \beta(s)V_y + I_x(R_x + sL_x)$, and (v) a current transfer function $\alpha(s)$, which equals $\alpha/(1+s/\omega_\alpha)$, such that $I_z = \pm\alpha(s)I_x$. If we insert all the non-ideal parasitic elements into the filter structure shown in Fig. 5-21, the preliminary non-ideal circuit structure of the *unified* CCCII-based biquad filter is shown in Fig. A4-2. Note that this preliminary non-ideal implementation doesn't include the effects of the voltage and current constraints, $\beta(s)$ and $\alpha(s)$.

In Fig. A4-2, $C'_1 = C_{y3} + C_{z2} + C_1$, $C'_2 = C_{z3} + C_{y2} + C_2$, $G'_1 = G_{y3} + G_{z2}$, and $G'_2 = G_{z3} + G_{y2}$, where C_1 and C_2 are given capacitors.

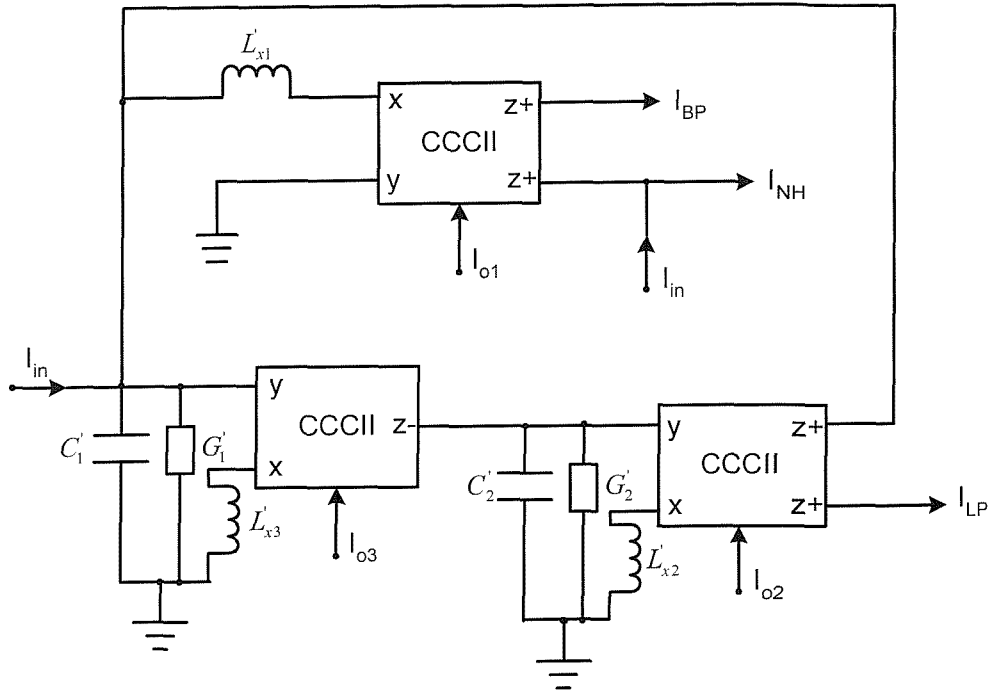


Fig. A4-2 Preliminary non-ideal implementation of the *unified* OTA-based biquad filter without the non-ideal effects of $\beta(s)$ and $\alpha(s)$

Since

$$V_x = \beta(s)V_y + I_x(R_x + sL_x), \quad \frac{V_x - \beta(s)V_y}{(R_x + sL_x)} \cong [V_x - \beta(s)V_y] \left(\frac{1}{R_x} \right) \left(1 - \frac{sL_x}{R_x} \right) \quad (\text{A4-1})$$

provided that R_x is larger than sL_x . Note that $\left(\frac{1}{R_x} \right) \left(1 - \frac{sL_x}{R_x} \right)$ in Eq. (A4-1) has the same

form as the frequency dependent transconductances: $g_j(1 - sT_j)$ of a non-ideal OTA. Then, if we get rid of the effects of the voltage and current constraints, $\beta(s)$ and $\alpha(s)$, the parasitic effects of both Figs. A4-1 and A4-2 have the similar result. However, the extra voltage and current constraints, $\beta(s)$ and $\alpha(s)$, of a non-ideal CCCII lead to the worse performance of CCCII-based biquads than that of OTA-based biquads and the concluding remark in Chapter 6: “OTA-based biquads perform better in practice than CCCII-based biquads”.

Appendix 5

PSpice Sensitivity Analysis and Simulations

In this appendix, three filter structures proposed in Chapters 3, 4, and 5, are used to demonstrate their low sensitivity performance using PSpice simulations. The filters are:

- (i) the current-mode OTA-C low-pass biquad using MISOC synthesis method shown in Fig.A5-1,
- (ii) the voltage-mode OTA-C all-pass biquad using the second voltage-mode synthesis method (Sec. 4.3), shown in Fig. 4-18 (or Fig. A5-4),
- (iii) the *unified* CCCII-based biquad filter shown in Fig. 5-21 (or Fig. A5-7),

We use PSpice 8.0, $\pm 5V$ supply voltages, $W/L = 10\mu/3\mu$ and $5\mu/3\mu$ for PMOS and NMOS transistors of an OTA for case (i), $W/L = 20\mu/5\mu$ and $10\mu/5\mu$ for PMOS and NMOS transistors of an OTA for case (ii), and $W/L = 16\mu/3\mu$ and $16\mu/3\mu$ for PMOS and NMOS transistors of a CCCII for case (iii), and component values: (i) $C_1 = C_2 = 7.96\text{pF}$, $g_1 = 35.36\ \mu\text{S}$ and $g_2 = 70.71\ \mu\text{S}$, (ii) $C_1 = 13.28\text{pF}$, $C_2 = 6.64\text{pF}$, and $g_a = g_b = g_1 = g_2 = 59\ \mu\text{S}$, and (iii) $C_1 = C_2 = 7.96\text{pF}$, $G_{x1} = 70.71\ \mu\text{S}$, and $G_{x2} = G_{x3} = 50\ \mu\text{S}$, to do the simulations.

Fig. A5-2 shows the low-pass amplitude-frequency response of Fig. A5-1 for the nominal and each of the capacitor sensitivity analyses with 5% C_1 tolerance and -5% C_2 tolerance. The biquad nominal 3dB frequency is 0.9999 MHz. The sensitivity analysis of C_1 (resp. C_2) shows that the biquad has a 3dB frequency of 0.9993 MHz (resp. 1.0518 MHz). Therefore, the percentage difference is $[(0.9993-0.9999)/0.9999] \times 100\% = -0.06\%$ (resp. $[(1.0518-0.9999)/0.9999] \times 100\% = 5.18\%$). The nominal and worst-case sensitivity results are shown in Fig.A5-3. The worst case with 5% and -5% tolerances for C_1 and

C_2 , respectively, has a 3dB frequency of 1.05 MHz, namely, $[(1.05-0.9999)/0.9999] \times 100\% = 5.01\%$ percentage difference.

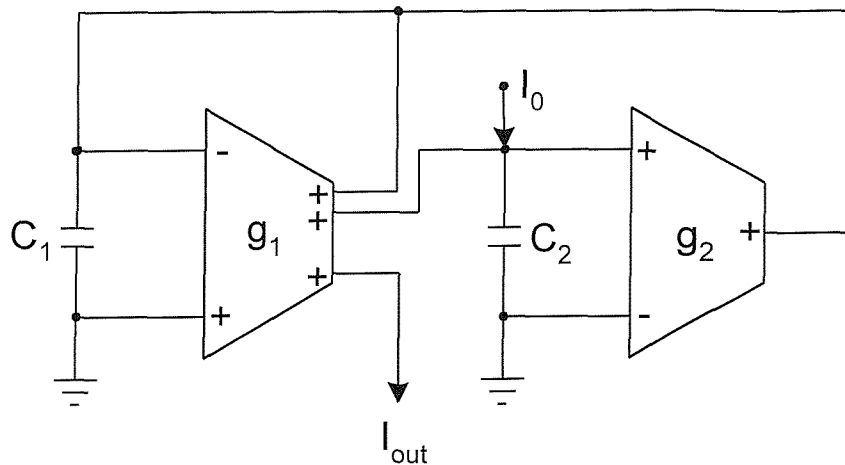


Fig.A5-1 Current-mode OTA-C low-pass biquad using MISOC synthesis method

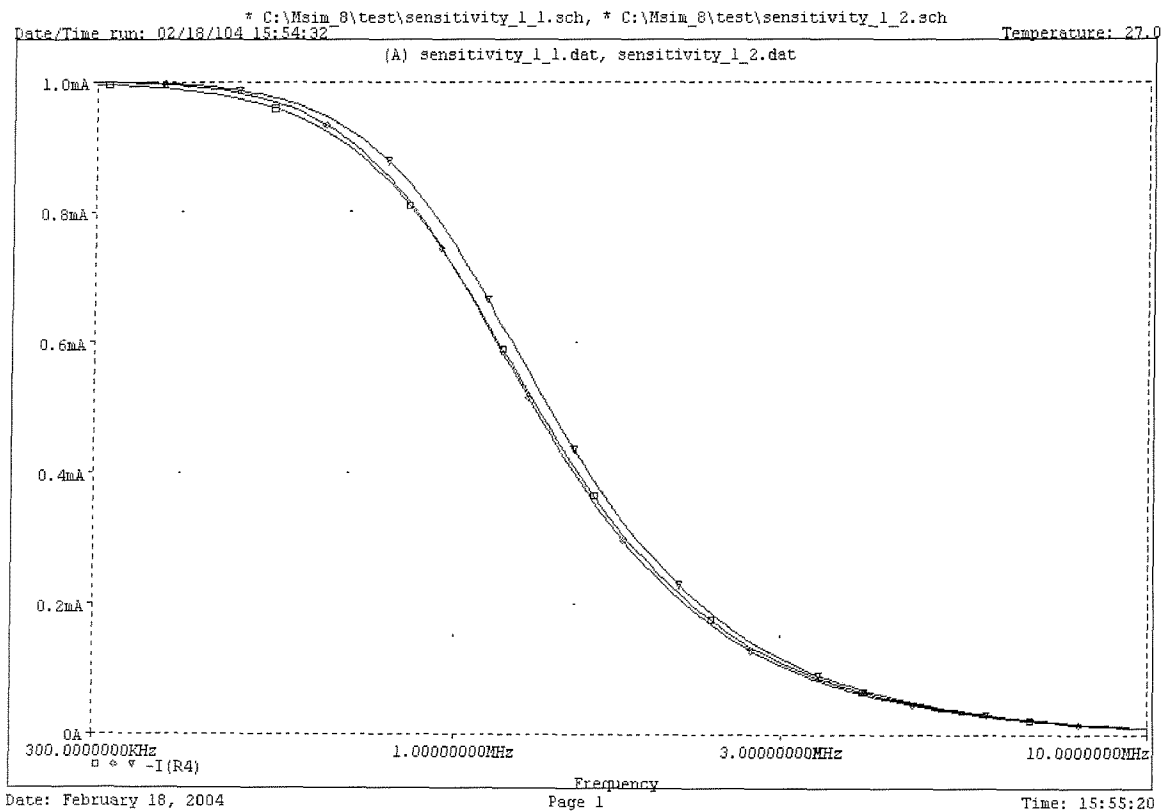


Fig. A5-2 PSpice sensitivity results of Fig. A5-1 with $\pm 5\%$ component tolerance (\square , nominal; \diamond , C_1 with 5% error; ∇ , C_2 with -5% error)

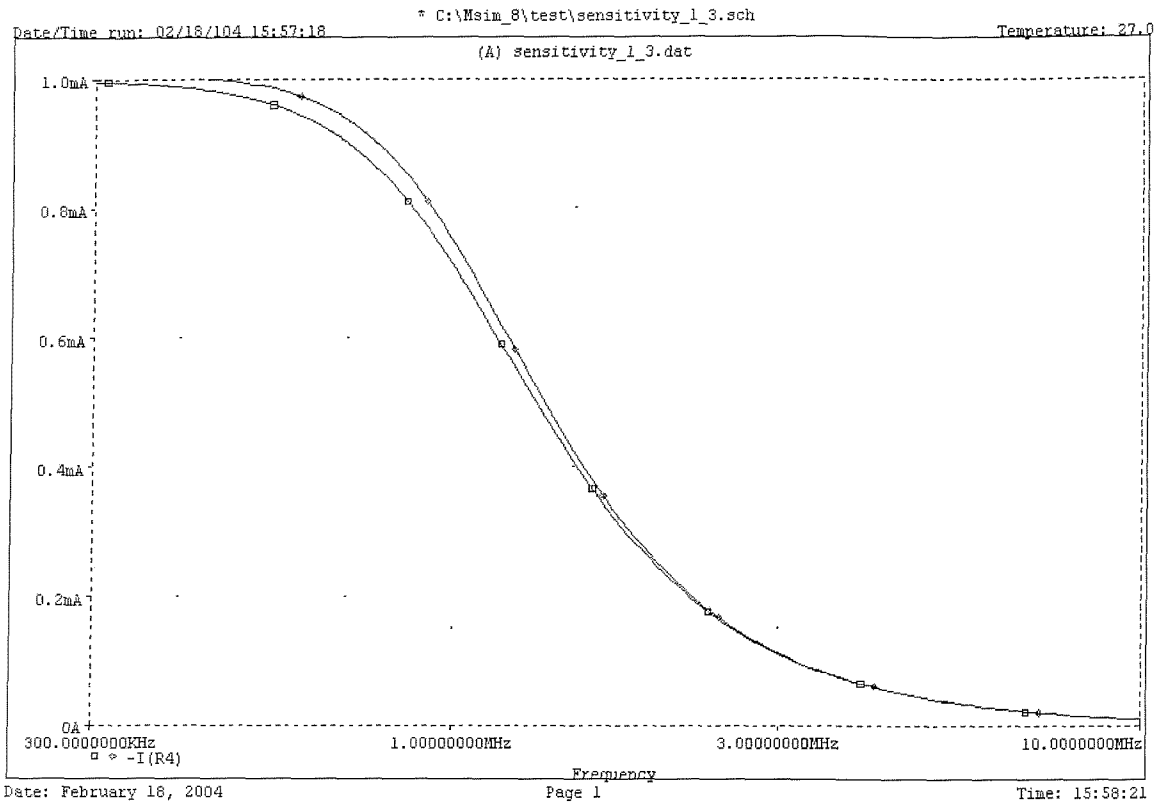


Fig. A5-3 PSpice sensitivity results of Fig. A5-1 with $\pm 5\%$ component tolerance
 (\square , nominal; \diamond , worst case, C_1 with 5% error and C_2 with -5% error)

Fig. A5-5 shows the all-pass phase-frequency response of Fig. A5-4 for the nominal and each of the capacitor sensitivity analyses with -10% C_1 tolerance and 10% C_2 tolerance. The biquad nominal centre frequency is 1.0164 MHz. The sensitivity analysis of C_1 (resp. C_2) shows that the biquad has a centre frequency of 1.0713 MHz (resp. 0.9691 MHz). Therefore, the percentage differences are $[(1.0713-1.0164)/1.0164] \times 100\% = 5.40\%$ and $[(0.9691-1.0164)/1.0164] \times 100\% = -4.65\%$, respectively. The nominal and worst-case sensitivity results are shown in Fig.A5-6. The worst case with -10% and 10% tolerances for C_1 and C_2 , respectively, has a centre frequency of 1.0215 MHz, namely, $[(1.0215-1.0164)/1.0164] \times 100\% = 0.50\%$ percentage difference.

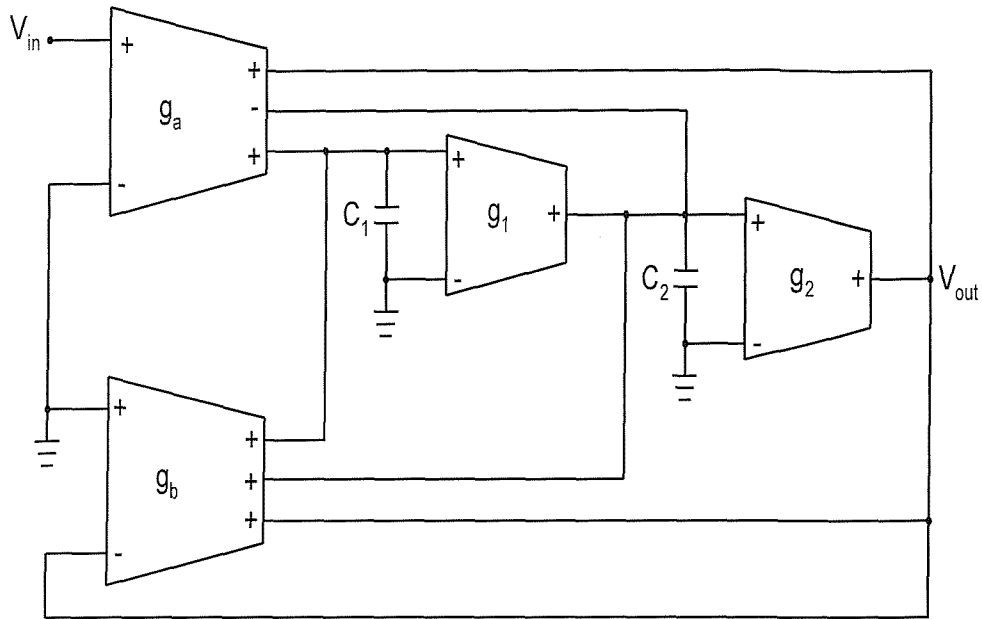


Fig. A5-4 Voltage-mode OTA-C all-pass biquad

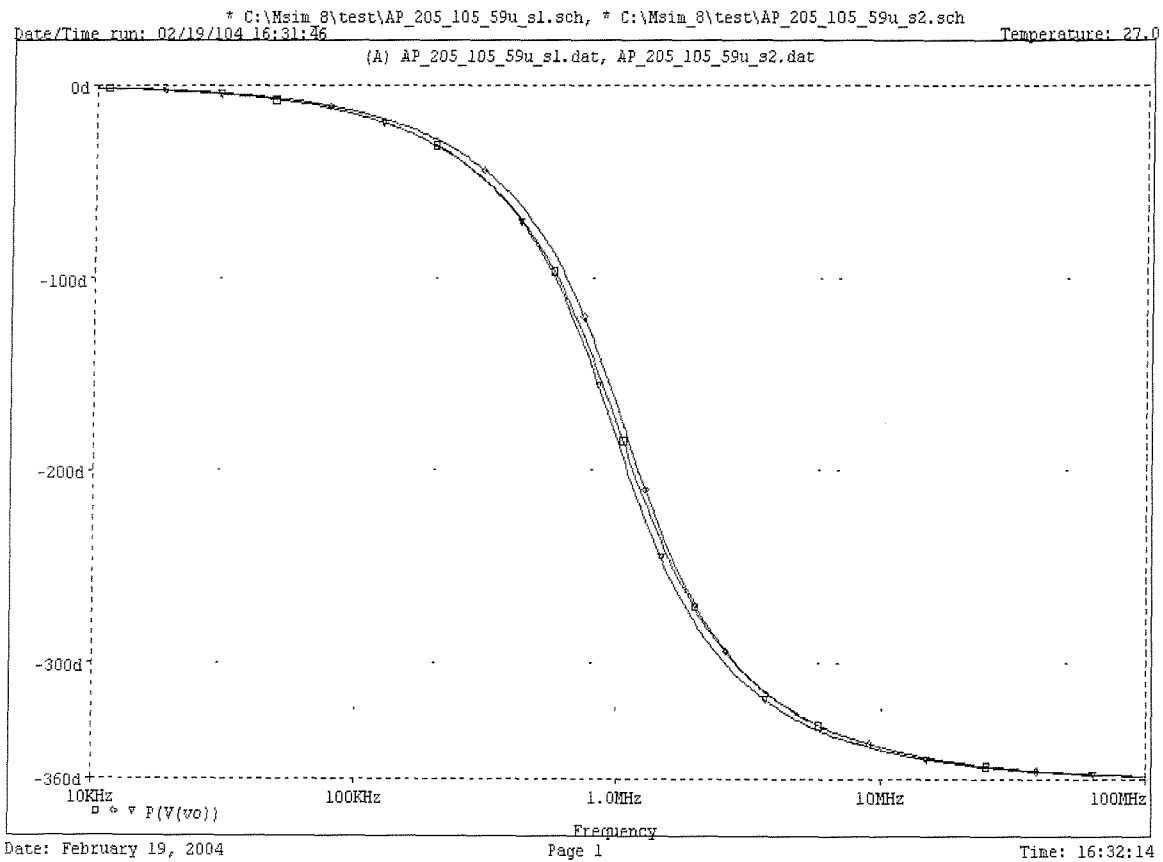


Fig. A5-5 PSpice sensitivity results of Fig. A5-4 with $\pm 10\%$ component tolerance
 (\square , nominal; \diamond , C_1 with -10% error; ∇ , C_2 with 10% error)

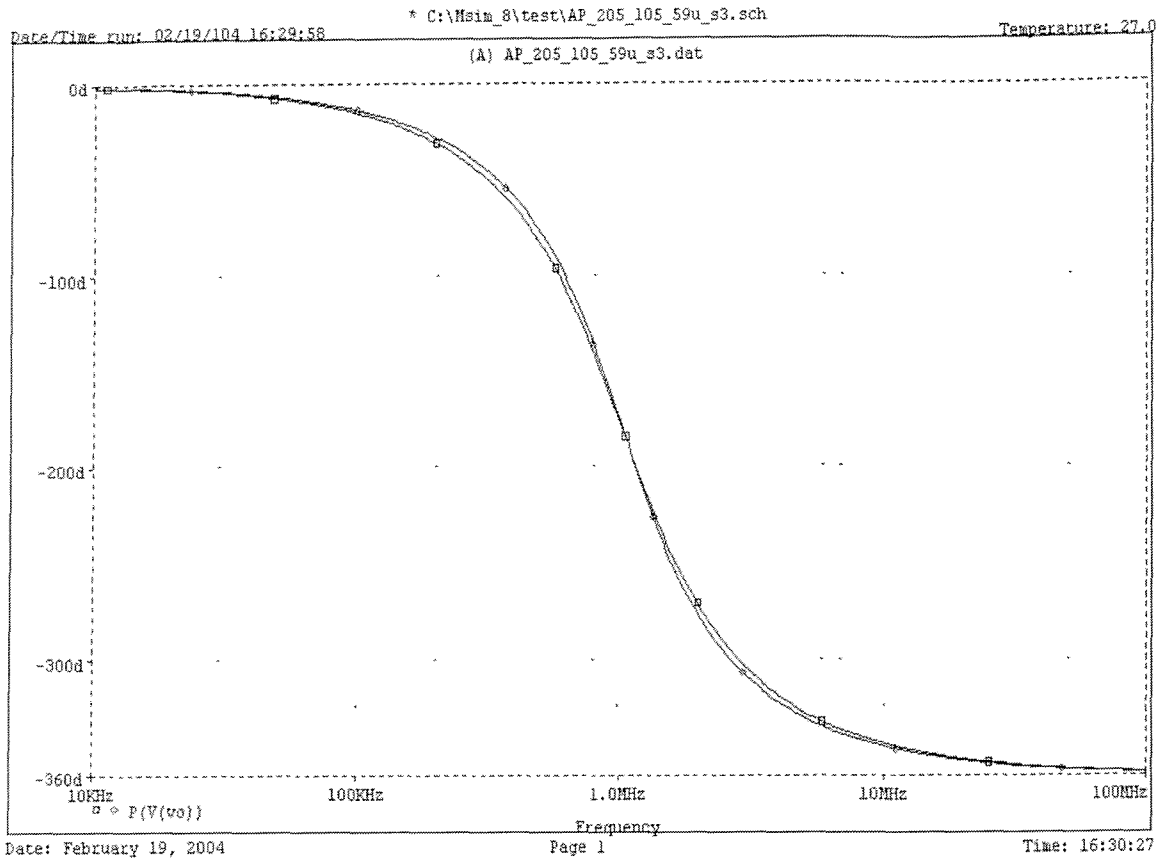


Fig. A5-6 PSpice sensitivity results of Fig. A5-4 with $\pm 10\%$ component tolerance (\square , nominal; \diamond , worst case, C_1 with -10% error and C_2 with 10% error)

Fig. A5-8 shows the low-pass amplitude-frequency response of Fig. A5-7 for the nominal and each of the capacitor sensitivity analyses with -5% component tolerance. The biquad nominal 3dB frequency is 0.995 MHz. The sensitivity analysis of C_1 (resp. C_2) shows that the biquad has a 3dB frequency of 0.994 MHz (resp. 1.0467 MHz). Therefore, the percentage differences are $[(0.994-0.995)/0.995] \times 100\% = -0.10\%$ and $[(1.0467-0.995)/0.995] \times 100\% = 5.20\%$, respectively. The nominal and worst-case sensitivity results are shown in Fig. A5-9. The worst case with -5% tolerance for both C_1 and C_2 has a 3dB frequency of 1.045 MHz, namely, $[(1.045-0.995)/0.995] \times 100\% = 5.03\%$ percentage difference.

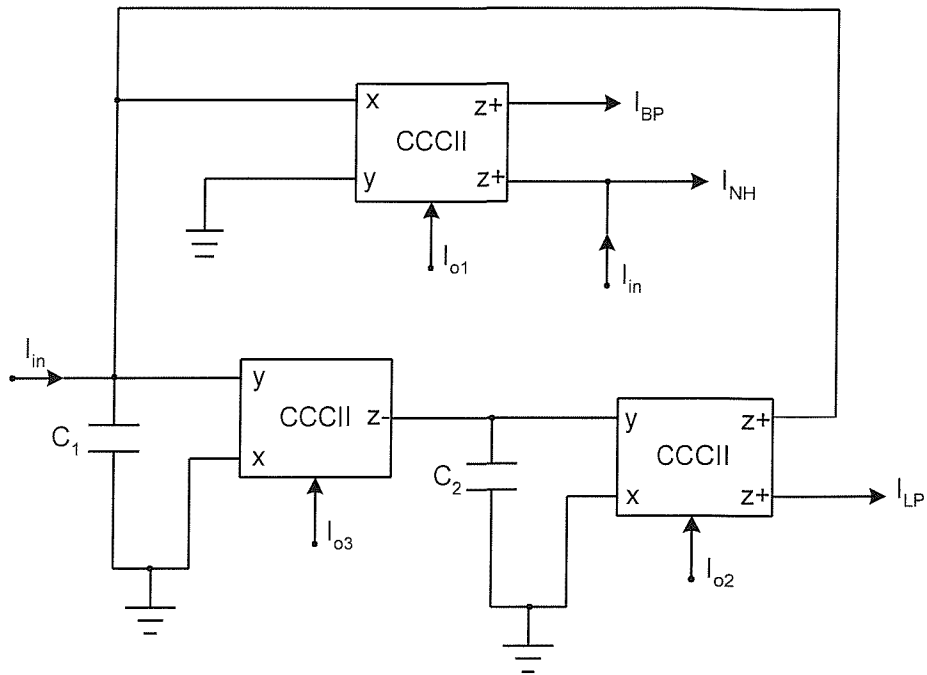


Fig. A5-7 Unified CCCII-based biquad filter

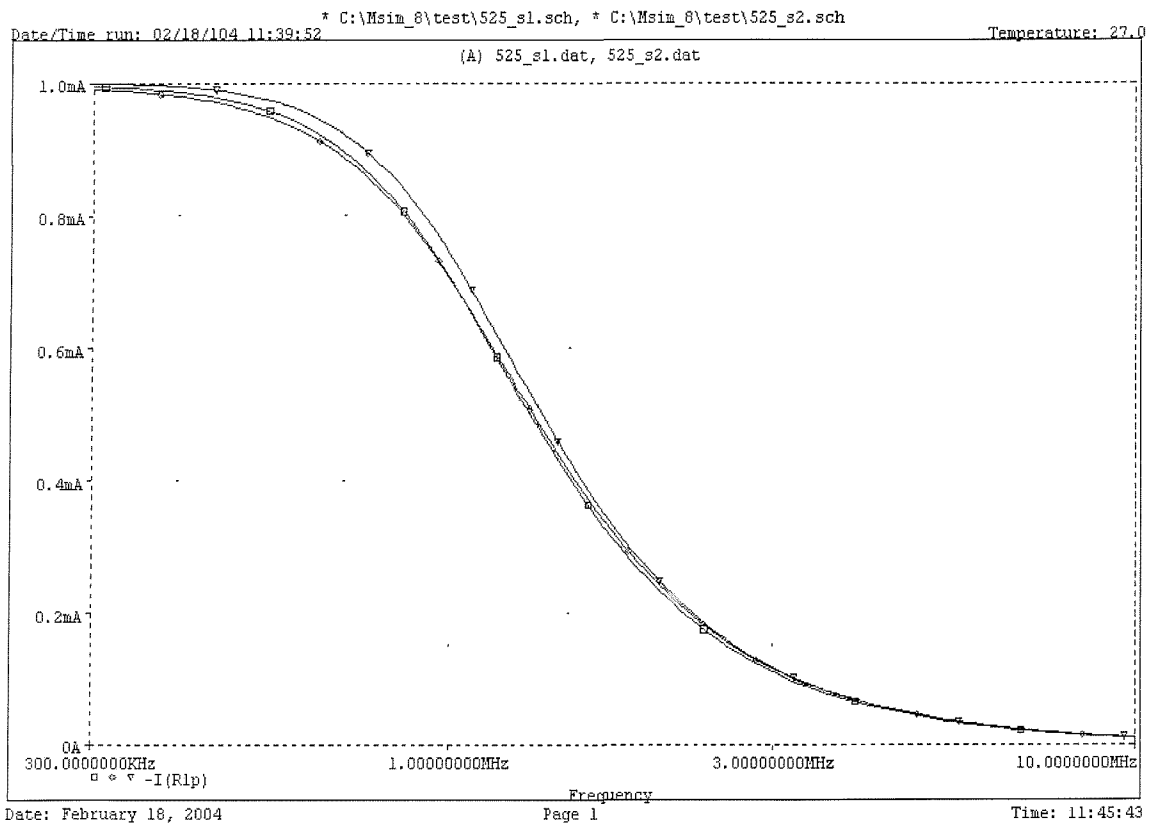


Fig. A5-8 PSpice sensitivity results of Fig. A5-7 with -5 % component tolerances
 (□, nominal; ◇, C_1 with -5% error; ▽, C_2 with -5% error)

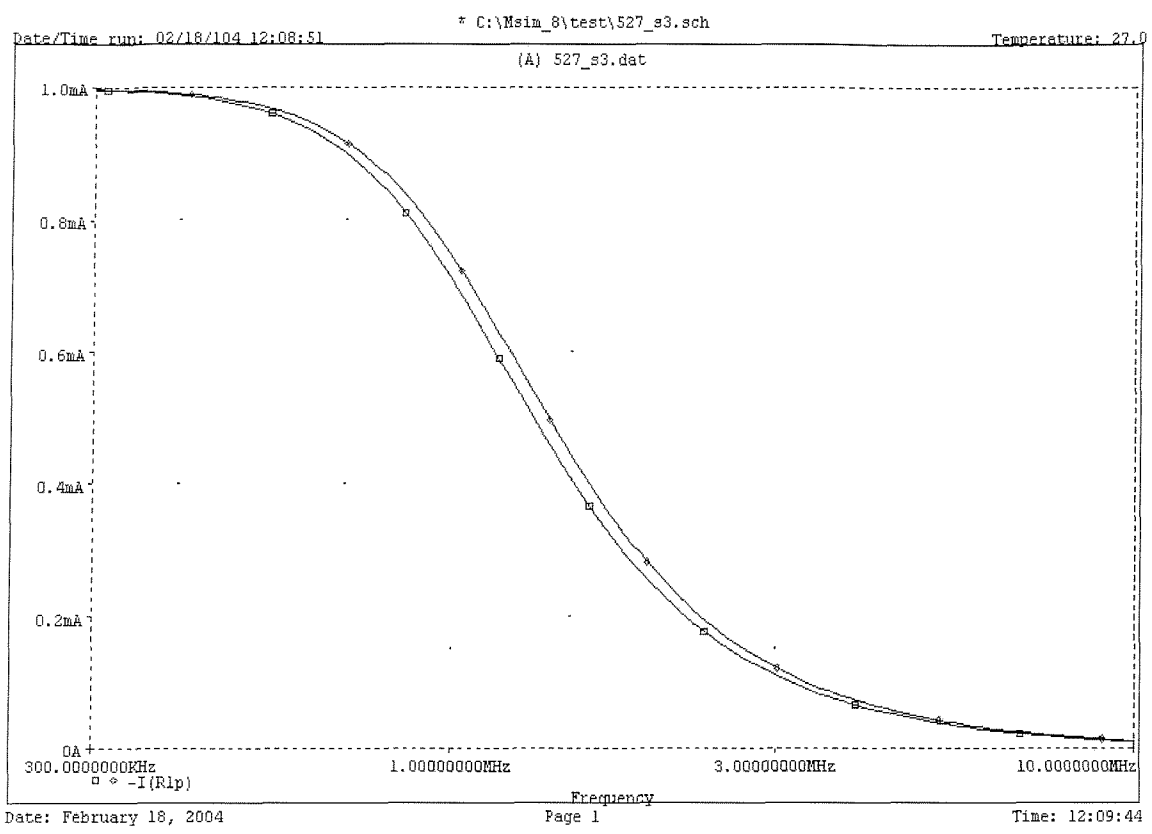


Fig. A5-9 PSpice sensitivity results of Fig. A5-7 with -5 % component tolerances
 (□, nominal; ◇, worst case, both C_1 and C_2 with -5% error)