UNIVERSITY OF SOUTHAMPTON

SWITCHED-CURRENT FILTERS AND GROUP DELAY EQUALIZERS USING WAVE SYNTHESIS TECHNIQUE

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A thesis submitted to the School of Electronics and Computer Science, University of Southampton in partial fulfilment of the requirements for the Degree of Doctor of Philosophy

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This thesis is dedicated to my parents

in Tianjin, China.

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

FACULTY OF ENGINEERING AND APPLIED SCIENCE

Switched-Current Filters and Group Delay Equalizers

Using Wave Synthesis Technique

by Yan Xie

This thesis is concerned with the design, analysis and realization of analogue filters and group delay equalizers using switched-current (SI) technology. A key feature of the described design methods is the employment of wave synthesis technique enabling advantages, such as simple circuit implementation and low sensitivity. Despite their simplicity, SI circuits suffer from some fundamental sources of errors, which produce deviations in their performance. The thesis presents a detailed analysis of the non-ideal performance of the recently reported Bruton transformation SI filters and show how the frequency response of such filters are affected by mismatch and clock-feedthrough errors. To carry out such a detailed investigation, behavioural models of the filter main building blocks have been developed based on their physical implementations and incorporated with *MATLAB*.

To improve elliptic filters time-domain response, group delay equalizers are often cascaded with the filters. This thesis describes a systematic design for SI group delay equalizers based on the wave synthesis technique including the development of new group delay equalizer architecture. Using computer program based on the presented design method and architecture, together with an optimisation technique, a number of equalizers have been designed and they are capable of improving the filters step response. To analyse the practical performance of SI wave filters and group delay equalizers, transistor-level circuits using standard 1.2 μm CMOS process are designed. Simulations show the performances of SI wave filters and group delay equalizers agree well with the theoretical predictions. Finally, new adaptive analogue filters with modified wave structure and adaptive algorithm are developed. It is shown that such filters offer a number of advantages including low sensitivity, simple adaptation process and easy stability checks. Furthermore, an efficient hardware implementation of analogue adaptive wave filters using SI technology is outlined.

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Abbreviations

BE	Backward Euler
BL	Bilinear
CMOS	Complementary Metal Oxide Semiconductor
DLS	Dithered Linear Search
FDNR	Frequency Dependent Negative Resistor
FE	Forward Euler
FFT	Fast Fourier Transformation
FIR	Finite Impulse Response
IC	Integrated Circuit
IIR	Infinite Impulse Response
LD	Lossless Discrete
LDI	Lossless Discrete Integrator
LMS	Least Mean Square
MSE	Mean Squared Error
OTA-C	Operational Transconductance Amplifier and Capacitor
SC	Switched-Capacitor
SCNAP4	Switched-circuit simulator [87]
SGF	Signal Graph Flow
SI	Switched-Current
THD	Total Harmonic Distortion
VLSI	Very Large Scale Integration

Contents:

Chapter 1

Introduction

1.1 VLSI technology

The rapid development in VLSI (very large scale integrated) technology has enabled the integration of powerful digital processing units and analogue circuits into the same chip [1]. This development, coupled with the increasing number of devices fabricated on a single chip, has resulted in the implementation of single-chip mixed analogue/digital systems. A typical mixed-signal IC contains primarily digital blocks for performing the signal processing and small analogue circuits for interfacing with external analogue signal sources [83]. Fig.1.1 illustrates some of the interaction between the analogue and digital domains in state-of-the-art technology. The mixed-signal processing system provides the means for accurately detecting, acquiring, and conditioning various physical data for processing, storage and/or action through digital computer. Applications for these systems are in the areas of communications, robotics, medical instruments and automated manufacturing.

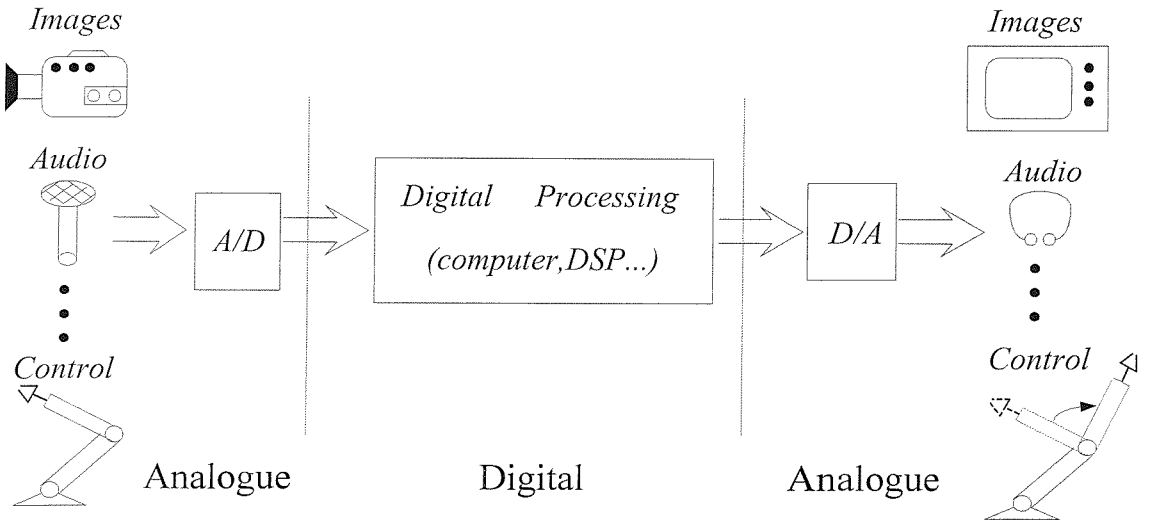


Fig.1.1 The analogue-digital-analogue paradigm

The development of analogue interfacing circuits in the mixed-signal IC is of fundamental importance to the future advances of microelectronics technology. This is because analogue circuitry is needed in acquiring information from analogue external sources and preparing the analogue information for conversion to digital format. In addition, analogue circuitry is able to reduce manufacturing costs, minimize power dissipation and the weight of portable systems.

1.2 Filters and group delay equalizers

An electronic filter can be defined as a network of circuit components (resistors, capacitors, inductors and transistors) that operates on or processes electrical signals. Its objective is to perform frequency selective transmission [79,81]. In mixed-signal IC, the integrated filter is an important analogue subsystem, whose function is to perform anti-aliasing prior to signal conversion, Fig.1.2.

Fig.1.2 Analogue/digital system

When the external analogue signal is introduced into the mixed-signal system, it is first processed through active-RC filters, whose function is to band-limit the input signal in preparation for sampling. Analogue discrete-time filters, such as switched-capacitor (SC) or switched-current (SI) filters, are chosen to perform the function of frequency selection. The main reasons for choosing discrete-time filters are [83]:

1. Monolithic discrete-time filters are much compact and cheaper than continuous-time active-RC filters due to their small die area.
2. In principle, the performance of discrete-time filters is only determined by ratios of same type of components and clock frequency. Consequently, it is more accurate and suffers less drift than implementations relying on absolute component values or ratio between different types of components, such as in active-RC filters.
3. Special fabrication processing used to form precision resistors and capacitor (i.e. in active- RC filters) is not required in the implementation of discrete-time filters.

Group delay equalizer is an allpass filter, whose function is to compensate filters' phase response without changing their magnitude characteristics [81]. Group delay means the time delay experienced by every spectral component of the input signal as it is processed through filters. It is defined as the derivation of phase response with respect to frequency:

$$\tau(\omega) = -\frac{d\theta(\omega)}{d\omega} \qquad (1.1)$$

In voice and audio applications, ignoring the phase or group delay is usually justifiable because the human ear is insensitive to changes in phase or delay with frequency. However in ideal data and video transmission systems the phase is linear with frequency or the group delay is constant with frequency. When the group delay is not constant in such systems, the variation in delay or phase is called *delay distortion* or *phase distortion*. For example, delay distortion produced by filters can impair the detection of the logic 1's and 0's contained in data signals resulting in unacceptable transmission errors. The requirement of linear phase response can be met by cascading group delay equalizer with the filters [81]. The time-domain response of filters will be improved by employing group delay equalizer, Fig.1.3.

Fig.1.3 (a) Step response of filter

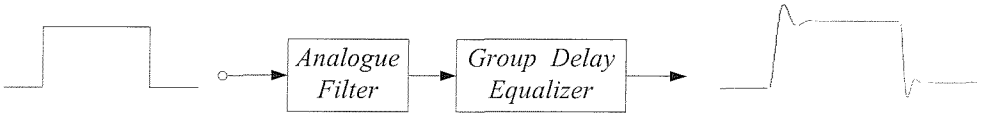


Fig.1.3 (b) Step response of filter cascaded with group delay equalizer

Most filters are implemented using CMOS technology due to the advantages of low power dissipation, the ability to mix analogue and digital subsystems compactly on the same die and the near ideal quality of such components as capacitors and analogue switches. The highest demand for VLSI analogue/digital systems has been in the areas of information acquisition and voice/data telecommunications.

1.3 Switched-current technology

Switched-current (SI) technology is a new analogue discrete-time technique, which has many potential advantages including implementation simplicity, low power operation

and compatibility with standard digital CMOS processes [1,77]. Conventionally, switched-capacitor (SC) technology is used in the design of discrete-time filters [79]. However, it isn't fully compatible with digital CMOS processing technology, because it requires high quality linear floating capacitors, which are implemented using two layers of polysilicon. SI technology, as a current-mode approach, maintains CMOS transistor's drain current through the charge stored on its gate oxide capacitances, so linear floating capacitors are not required in SI circuits. In current-mode circuits, the signal is represented as currents rather than voltages [76]. Therefore, the dynamic range is only indirectly limited by voltage supply and low input impedance will allow large input current-mode signal. In addition, some basic signal processing operations, such as summation, delay and multiplication, can be manipulated conveniently in current-mode circuits, and it means SI circuits have the potential for implementation simplicity and high-speed operation. Due to the numerous advantages of SI technology over SC technology, substantial effort has been devoted to develop the efficient design methods and architectures for the high performance SI filters [1-30].

1.4 Research motivations

Filters and group delay equalizers are main signal processing blocks used in the electronics integrated system. Numerous design methods have been proposed to realize efficient filters. Recently a powerful SI filter design method, Bruton transformation SI wave filters, has been reported [2,3], however there are still problems, including its non-ideal performance and group delay equalization. Therefore, it needs further investigation for the maturity of this design methodology to produce efficient SI filters and equalizers. This research focuses on the analysis and transistor-level design of Bruton transformation SI wave filters and group delay equalizers. In addition, SI adaptive wave filters and their adaptation algorithm are also investigated.

1. Non-ideal performance of Bruton transformation SI wave filters

The simplicity of SI circuits makes them more suitable than SC circuits for analogue signal processing applications in standard low-voltage CMOS digital process technologies. However, SI circuits suffer from fundamental sources of errors, i.e. mismatch in transistors, clock-feedthrough in switches. Previous work has been done in order to model these errors and analyse their effect on the operation of basic SI

circuits [37]. Since practical implementations of Bruton transformation wave filter are based on SI technology, the study of the filter's sensitivity to these errors is necessary for predicting the filter's performance at early design stages. The aim of this research is to develop behavioural models of the building blocks of Bruton transformation SI wave filter taking into account of non-ideal characteristics, make rapid simulation on the whole filter operation using these behavioural models and analyse the sensitivity of these errors to the filter's performance.

2. Group delay equalization

The practical applications often call for filters with high attenuation and linear phase. In order to achieve high attenuation characteristics and narrow transition band, elliptic filters are often chosen. Since elliptic filter generally exhibits non-linear phase response, group delay equalizer will be used to provide flat group delay responses. Although many design methods for SI filters have been proposed [10-27], there has been little reported research on SI group delay equalizers. The aim of this research is to provide an efficient design approach for SI group delay equalizer.

3. Transistor-level circuit design of SI wave filters and group delay equalizers

To analyse the practical performance of SI wave filters and group delay equalizers, the transistor-level circuits need be designed. The aim of this research is to implement SI wave filters and group delay equalizers using practical SI building blocks and validate the performance of these circuits using realistic transistor models and practical fabrication techniques through SPICE simulations.

4. SI adaptive wave filters

Adaptive filters are used in time-varying systems, where the filters' parameters must track the variation of system conditions. Although SI filters with fixed frequency characteristics have been extensively investigated, there has been little reported research on SI filters with adaptive characteristics. The aim of this research is to investigate and develop new SI adaptive wave filter, which has low sensitivity, simple filter structure and efficient implementation.

1.5 Thesis organization and contributions

This thesis contains seven chapters and involves system and transistor-level design of SI wave filters with group delay equalizers. Chapter 2 gives an overview of analogue SI technology and wave synthesis technique. The complete design process for SI filters, based on different system design techniques, are reviewed and their implementations using SI technology are described. From this overview, it is shown that recently reported Bruton transformation SI wave filter is an efficient design method. To facilitate the maturity of this design method, Chapter 3 presents a detailed analysis into non-ideal performance of high frequency Bruton transformation SI wave filters due to mismatch and clock-feedthrough. To improve the time-domain response of SI filters, Chapter 4 provides a systemic design method of SI group delay equalizer, which based on wave synthesis technique. The design process, including optimisation and wave synthesis, is described. The resultant circuit of group delay equalizer has low sensitivity to magnitude response and simple implementation. Chapter 5 discusses the detailed transistor-level circuit design of SI wave filters and group delay equalizers. Non-ideal characteristics of SI circuit are introduced, and circuit design techniques are used to reduce these limitations. SPICE simulations are performed to validate the transistor-level circuit of SI wave filters and group delay equalizers. While Chapter 2, 3, 4 and 5 focus on the SI filters with fixed frequency characteristics, Chapter 6 deals with the design of SI filters with adaptive characteristics. New SI adaptive wave filters with suitable adaptation algorithm are proposed, and they have advantages, such as simple adaptation process, easy stability checks and efficient implementation. Finally, Chapter 7 summarizes the presented research and concludes this thesis. The contribution of this research can be summarized as follows:

1. Presented a detailed analysis of the non-ideal performance of Bruton transformation SI wave filters due to mismatch and clock-feedthrough errors [4].

2. Proposed new efficient design method and circuit architecture for SI wave group delay equalizers [5,6].

3. Applied wave synthesis technique to the design of analogue adaptive filters and presented new SI adaptive wave filters [7,8].

Chapter 2

Switched-Current Filters

2.1 Introduction

In this chapter, the complete design processes of SI filters, which based on different system design techniques, are reviewed and their implementations using SI technology are described. First, the basic SI building blocks are outlined in section 2.2. Then section 2.3 reviews the design methods and implementations of integrator-based SI filters. The wave synthesis technique is introduced in section 2.4, and its implementation using SI technology is described in section 2.5. Section 2.6 gives the recently reported efficient design method, Bruton transformation wave filters, and its advantages over direct SI wave filters are summarized through comparison of design techniques in section 2.7. Finally, section 2.8 provides concluding remarks for this chapter.

2.2 Switched-current building blocks

Switched-current (SI) technology has been established as a reliable alternate to the switched-capacitor (SC) technology in the design of analogue integrated filters [1]. This section describes the building blocks, which perform signal processing operations, such as summation, multiplication and delay, and these building blocks are commonly used to realize SI filter circuits.

2.2.1 Current mirrors

Current mirrors are used to implement signal scaling and filter coefficients in SI filters. The basic current mirror is shown in Fig.2.1(a).

Fig.2.1 (a) Basic current mirror (b) Current-mode summation circuit

Its operation can be analysed as follows: assuming *M1* and *M2* are in saturation region, and gain *G*, is realized by choosing the aspect ratio of current mirror transistors according to $W_1 / L_1 = G \cdot (W_2 / L_2)$. The drain current for *M1* and *M2* can be written as:

$$i_{D1} = I_B + i_{in} = \frac{\mu_0 C_{ox}}{2} \cdot \frac{W_1}{L_1} (V_{GS1} - V_T)^2 \qquad (2.1a)$$

$$i_{D2} = GI_B + i_o = \frac{\mu_0 C_{ox}}{2} \cdot \frac{W_2}{L_2} (V_{GS2} - V_T)^2 \qquad (2.1b)$$

Due to $V_{GS1} = V_{GS2}$, the output current $i_o = G \cdot i_{in}$ and it is in the reverse direction to i_{in}. The basic signal processing functions, such as summation, multiplication and sign inversion, can be implemented through current mirrors, Fig.2.1(b). From the analysis of the basic current mirror, the input-output relationship of Fig.2.1(b) can be seen as:

$$i_o = -G \cdot (i_{in1} + i_{in2} + i_{in3}) \qquad (2.2)$$

2.2.2 SI memory cell

The function of SI memory cell is to 'memorize' the current-mode signal. It is often used to implement the current-mode delay cells and SI integrators, which are the fundamental components in SI filters.

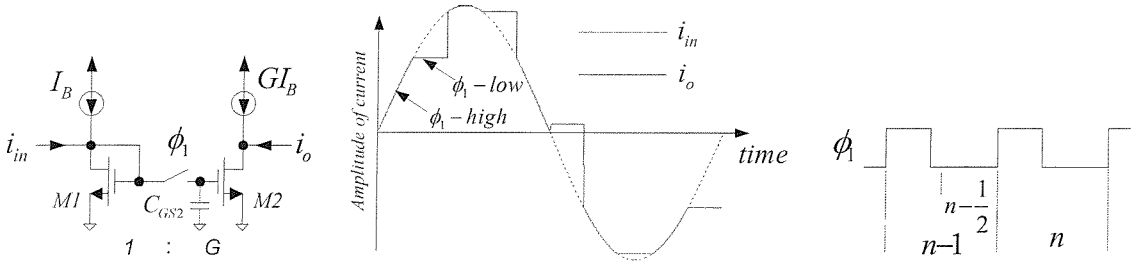


Fig.2.2 1st-generation SI memory cell and its input-output relationship

SI memory cell can be realized in two approaches, known as 1st and 2nd-generation SI memory cell [31,86]. The 1st-generation SI memory cell, shown in Fig.2.2, is controlled by clock signal ϕ_1. If the switch is on (ϕ_1-high), then $V_{GS1} = V_{GS2}$ and the circuit acts as a current mirror, i.e., the output *tracks* the input ($i_o = G \cdot i_{in}$). When the switch is off (ϕ_1-low) at time $t_0 = (n - \frac{1}{2})$, the gate capacitance of *M2*, C_{GS2}, stores the charges corresponding to the voltage at time t_0, $V_{GS2}(t_0)$. Thus, the output signal

current i_o is *held* at the value corresponding to the time when the switch is off, Eq.(2.3):

$$i_o(n) = G \cdot i_{in}(n - \frac{1}{2}) \qquad (2.3)$$

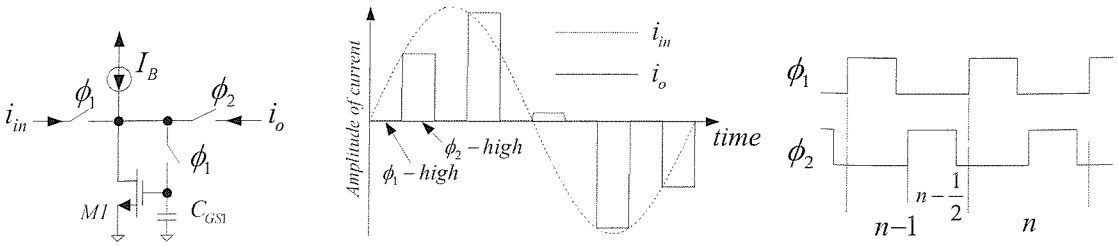


Fig.2.3 2nd-generation SI memory cell and its input-output relationship

The arrangement of 2nd-generation SI memory cell can achieve the memory cell within a single transistor (*M1*) combined with the switches controlled by non-overlapping two-phase clock ϕ_1 and ϕ_2. These switches are used to reconfigure the circuit to operate as both input and output circuit alternately and the output signal alternates between zero and a valid sample. When the switches ϕ_1 are on (ϕ_1-high), *M1* is diode-connected and the gate-source voltage V_{GS1} maintains the drain current $I_B + i_{in}$ as the *track* stage of 1st-generation memory cell. When the switch ϕ_2 is on at time $t_0 = (n - \frac{1}{2})$, the diode-connection of *M1* is broken and output is connected. The gate-source voltage at time t_0, $V_{GS}(t_0)$, is stored on the gate-capacitance C_{GS1}, and thus the output current i_o is *held* at the value corresponding to the time t_0, Eq.(2.4):

$$i_o(n) = i_{in}(n - \frac{1}{2}) \qquad (2.4)$$

It is obvious that 2nd-generation SI memory cell can only has unity gain, since the same transistor *M1* is used in both *track* and *hold* stages. It leads to perfect matching between input and output current signal.

2.2.3 SI integrator cell

In discrete-time filter design, *s* to *z* transformation is a bridge between the continuous and discrete-time domains. To realize this transformation, we need to map *H(s)* into rational *H(z)* by approximating $z = e^{sT}$ with rational first-order functions. From a lot

of numerical analysis in the area of digital signal processing [84], some efficient *s-z* transformations are obtained, as shown in Table 2.1. When applied to the design of discrete-time filters, the *s-z* transformations in Table 2.1, namely: Backward Euler (BE), Forward Euler (FE), Lossless Discrete (LD) and Bilinear (BL) provide contrasting properties.

Table 2.1 *s* to *z* transformations

$s \rightarrow z$ transformation	$s \rightarrow z$ integration	The frequency relation between s and z-domain ($s = j\Omega, z = e^{j\omega T}$)
BE: $s = \frac{1}{T}(1 - z^{-1})$	$\frac{1}{s} = \frac{T}{1 - z^{-1}}$	$\frac{1}{j\Omega} = \frac{T}{2} \frac{e^{j\omega T/2}}{j\sin(\frac{\omega T}{2})}$
FE: $s = \frac{1}{T} \frac{1 - z^{-1}}{z^{-1}}$	$\frac{1}{s} = T \frac{z^{-1}}{1 - z^{-1}}$	$\frac{1}{j\Omega} = \frac{T}{2} \frac{e^{-j\omega T/2}}{j\sin(\frac{\omega T}{2})}$
LD: $s = \frac{1}{T} \frac{1 - z^{-1}}{z^{-1/2}}$	$\frac{1}{s} = T \frac{z^{-1/2}}{1 - z^{-1}}$	$\frac{1}{j\Omega} = \frac{T}{2} \frac{1}{j\sin(\frac{\omega T}{2})}$
BL: $s = \frac{2}{T} \frac{1 - z^{-1}}{1 + z^{-1}}$	$\frac{1}{s} = \frac{T}{2} \frac{1 + z^{-1}}{1 - z^{-1}}$	$\frac{1}{j\Omega} = \frac{T}{2} \frac{1}{j\tan(\frac{\omega T}{2})}$

SI integrators are current-mode circuits, whose purpose is to realize the transformations listed in Table 2.1. In this section, the transistor-level circuits of Euler and Bilinear SI integrators are given in detail. More details about implementation of other SI integrators can be found in [1, 32].

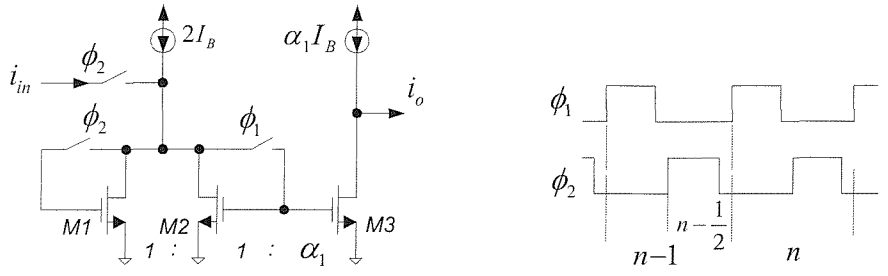


Fig.2.4 FE (Forward Euler) SI integrator

The transfer characteristic of FE SI integrator in Fig.2.4, can be derived as follows: when the switch ϕ_2 is on (ϕ_2-high) at the clock period *(n-1)*, *M1* is diode-connected and receives current from the input $i_{in}(n-1)$, bias $2I_B$ and drain current of *M2* $[I_B - i_o(n-1)/\alpha_1]$. So the drain current of transistor *M1* is:

$$I_{D1} = i_{in}(n-1) + 2I_B - [I_B - i_o(n-1)/\alpha_1] = I_B + i_o(n-1)/\alpha_1 + i_{in}(n-1) \quad (2.5)$$

When the switch ϕ_1 is on (ϕ_1-high) at the clock period *n*, *M2* is diode-connected and its drain current is:

$$I_{D2} = 2I_B - I_{D1} = I_B - i_o(n-1)/\alpha_1 - i_{in}(n-1) \quad (2.6)$$

And the output current is:

$$i_o(n) = -(\alpha_1 I_{D2} - \alpha_1 I_B) = i_o(n-1) + \alpha_1 \cdot i_{in}(n-1) \quad (2.7)$$

Applying z-transformation on (2.7) gives FE (Forward Euler) formula:

$$\frac{i_o}{i_{in}} = \frac{\alpha_1 z^{-1}}{1 - z^{-1}} \quad (2.8)$$

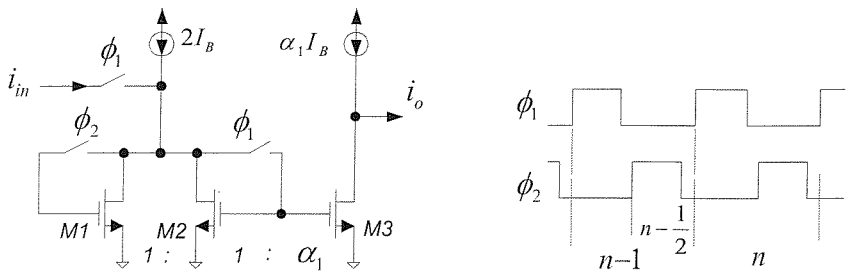


Fig.2.5 BE (Backward Euler) SI integrator

The analysis of BE SI integrator's transfer characteristics is similar to FE SI integrator. When the switch ϕ_2 is on (ϕ_2-high) at the clock period *(n-1)*, the drain current of *M1* is:

$$I_{D1} = 2I_B - [I_B - i_o(n-1)/\alpha_1] = I_B + i_o(n-1)/\alpha_1 \quad (2.9)$$

When the switch ϕ_1 is on (ϕ_1-high) at the clock period *n*, *M2* is diode-connected and its drain current is:

$$I_{D2} = i_{in}(n) + 2I_B - I_{D1} = i_{in}(n) + I_B - i_o(n-1)/\alpha_1 \quad (2.10)$$

And the output current is:

$$i_o(n) = -(\alpha_1 I_{D2} - \alpha_1 I_B) = i_o(n-1) - \alpha_1 \cdot i_{in}(n) \quad (2.11)$$

Applying z-transformation on (2.11) gives BE (Backward Euler) formula:

$$\frac{i_o}{i_{in}} = -\frac{\alpha_1}{1-z^{-1}} \qquad (2.12)$$

The general integrator consists of FE integrator, BE integrator and current amplifier ($\alpha_3 i_3$), as shown in Fig.2.6.

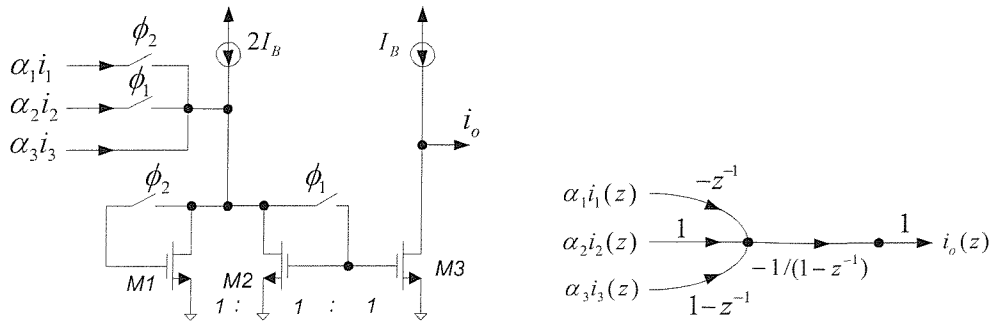


Fig.2.6 General integrator SI circuit and z-domain SFG

By superposition of Eq.(2.8), Eq.(2.12) and the current amplifier function, the z-domain output current i_o is given as:

$$i_o(z) = \frac{\alpha_1 \cdot z^{-1}}{1-z^{-1}} i_1(z) - \frac{\alpha_2}{1-z^{-1}} i_2(z) - \alpha_3 \cdot i_3(z) \qquad (2.13)$$

The input currents, weighted α_1, α_2 and α_3, are accomplished by scaling the aspect ratio of input stages. The z-domain SGF (signal flow graph) is also given in Fig.2.6.

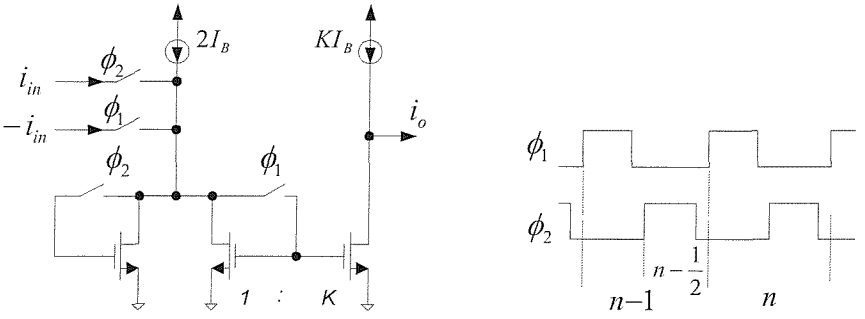


Fig.2.7 BL (Bilinear) SI integrator

The BL SI integrator can be obtained from the circuit of the general integrator if i_{in} and $(-i_{in})$ are used as inputs, shown in Fig.2.7. It can be seen from Eq.(2.13) that the z-domain output current i_o is:

$$i_o(z) = \frac{K \cdot z^{-1}}{1-z^{-1}} i_{in}(z) - \frac{K}{1-z^{-1}}(-i_{in}(z)) = K\frac{1+z^{-1}}{1-z^{-1}} \cdot i_{in}(z) \qquad (2.14)$$

SI bilinear building block has well-known advantages: It has no phase errors and can map to z-plane with guaranteed stability. It gives the resultant filter distortion-free magnitude response and can operate with high cutoff frequency to clock frequency ratios. In common with Euler integrators, BL SI integrator in Fig.2.7 operates with only one phase per clock period. Recently, double sampling BL SI integrator has been proposed [33] and it can achieve the high speed through delivering the samples on both phases (ϕ_1 and ϕ_2) per clock period.

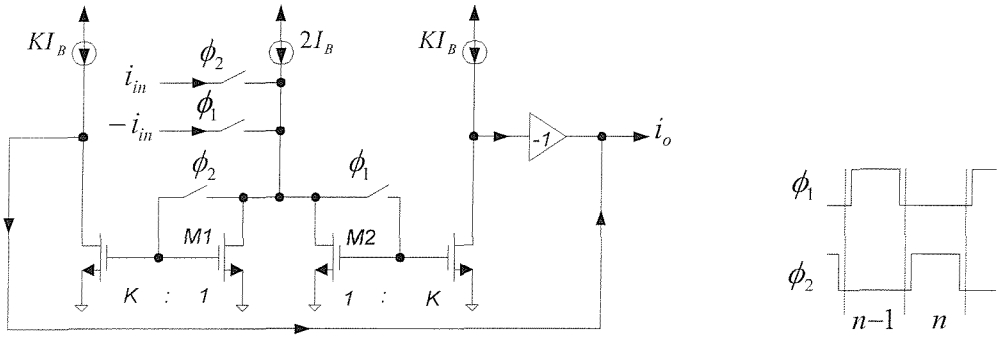


Fig.2.8 Double sampling Bilinear SI integrator

The analysis of this integrator is similar to other integrators, and for simplicity only signal currents are considered in the analysis below:

On phase ϕ_1, *(n-1)* in Fig.2.8, the signal drain current of *M2* is:

$$i_{D2}(n-1) = -i_{in}(n-1) - i_{D1}(n-1) \tag{2.15}$$

On the next phase ϕ_2, *(n)* in Fig.2.8, i_{D2} is held and $i_{D2}(n)$ equals to $i_{D2}(n-1)$:

$$i_{D2}(n) = i_{D2}(n-1) \tag{2.16}$$

The signal drain current of *M1* is:

$$i_{D1}(n) = i_{in}(n) - i_{D2}(n) = i_{in}(n) + i_{in}(n-1) + i_{D1}(n-1) \tag{2.17}$$

This produces an output current $i_o(n)$:

$$i_o(n) = K \cdot i_{D2}(n) - K \cdot i_{D1}(n) = -K \cdot [i_{in}(n) + i_{in}(n-1)] + i_o(n-1) \tag{2.18}$$

where $i_o(n-1) = K \cdot i_{D2}(n-1) - K \cdot i_{D1}(n-1)$

Taking z-domain transformation on Eq.(2.18), the BL transformation is obtained:

$$i_o(z) = -K \frac{1+z^{-1}}{1-z^{-1}} \cdot i_{in}(z) \tag{2.19}$$

It can be seen from the above analysis that double sampling BL SI integrator can operate with double speed of BL SI integrator (Fig.2.7). And this characteristics is suitable to the implementation of high frequency filters.

2.3 Switched-current filter design techniques

This section reviews some fundamental design techniques for SI filters, Fig.2.9. The implementations of these filters are also discussed.

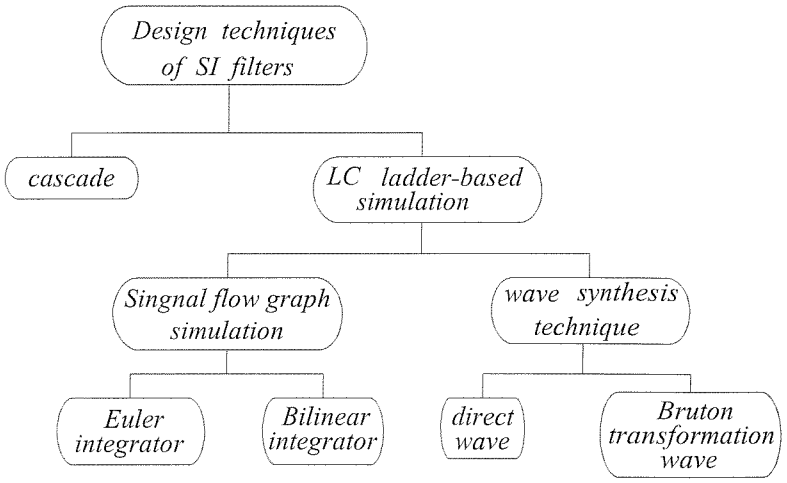


Fig.2.9 Overview of SI filter design techniques

2.3.1 Cascade technique

High-order filter transfer function *H(s)* can be realized through cascading the 1st-order and 2nd-order sections as shown in Eq.(2.20):

$$H(s)=[\frac{a_2s^2+a_1s+a_0}{b_2s^2+b_1s+b_0}][\frac{c_2s^2+c_1s+c_0}{d_2s^2+d_1s+d_0}]\cdots \tag{2.20}$$

The transfer function of 2nd-order (also called biquad) build blocks is commonly written as:

$$H(s)=\frac{k_2s^2+k_1s+k_0}{s^2+(\frac{\omega_0}{Q})s+\omega_0^2} \tag{2.21}$$

Applying BL transformation in Table 2.1 to (2.21) gives the z-domain transfer function *H(z)* as:

$$H(z)=\frac{[\frac{4k_2+2k_1T+k_0T^2}{D}]z^2+[\frac{2k_0T^2-8k_2}{D}]z+[\frac{4k_2-2k_1T+k_0T^2}{D}]}{[\frac{\omega_0T^2+\frac{2\omega_0T}{Q}+4}{D}]z^2+[\frac{2\omega_0^2T^2-8}{D}]z+1} \quad (2.22)$$

where $D=\omega_0^2T^2-\frac{2\omega_0T}{Q}+4$ and T is the clock period

To implement the 2[nd]-order transfer function *H(z)*, the block diagram of the integrator-based SI biquadratic section is illustrated in Fig.2.10.

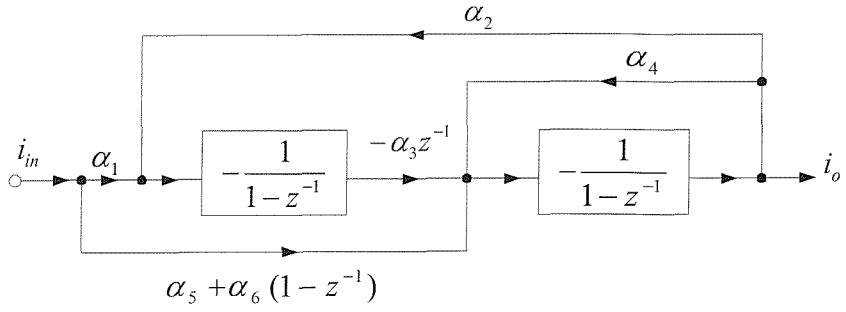


Fig.2.10 Block diagram of integrator-based biquadratic section

To calculate the coefficients in block diagram, the transfer function of the block diagram is first derived and then their coefficients are compared with those of the transformed z-domain biquadratic function, Eq.(2.22). The relation between the coefficients in block diagram and in transformed z-domain biquadratic function is given in Table 2.2, and it is used to choose the coefficients in block diagram according to the given transformed z-domain biquadratic function.

Table 2.2 Coefficients of integrator-based biquadratic section

Coefficient	*Value*
$\alpha_1\alpha_3$	$4k_0T^2/D$
$\alpha_2\alpha_3$	$4\omega_0^2T^2/D$
α_4	$4\omega_0T/QD$
α_5	$4k_1T/D$
α_6	$(4k_2-2k_1T+k_0T^2)/D$
D	$\omega_0^2T^2-2(\omega_0/Q)T+4$

To implement the block diagram of Fig.2.10, a loop containing two integrators with appropriate weighed feedback paths is constructed. The resultant transistor-level circuit is shown in Fig.2.11.

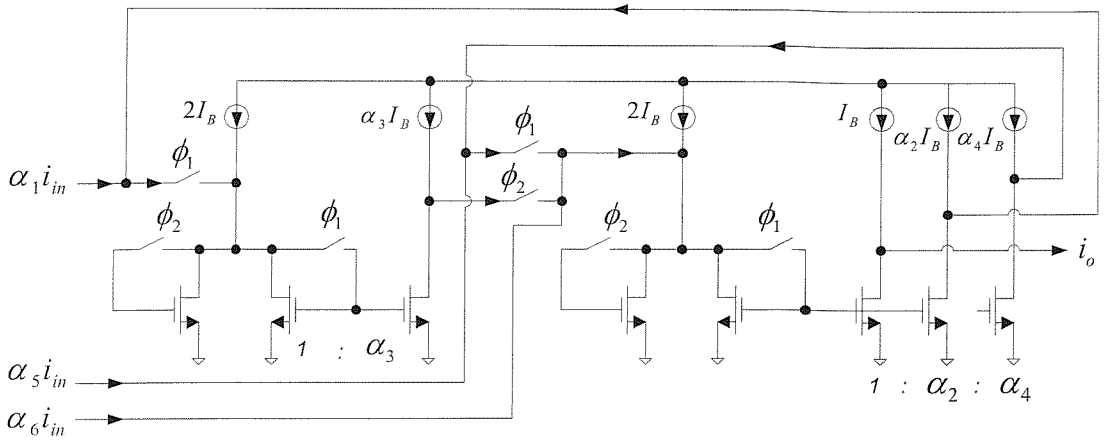


Fig.2.11 Transistor-level circuit of integrator-based biquadratic section

Each biquadratic function is realized in a separate block using an appropriate SI biquad. These SI biquad sections are cascaded to form the high-order filter. The main advantages of the cascade technique are its modularity and simplicity. The wide use of this technique has resulted in extensive publication [78,79] and available software for the optimisation of dynamic range and the pairing of poles and zeros [88].

2.3.2 Ladder-based technique

The passive *LC* ladder filter has been proved to be inherently insensitive to component variation, particular in its passband [81]. SI ladder-based filter simulates the behaviour of passive *LC* network, so it inherits the low-sensitivity of its passive counterpart. This low-sensitivity property is suitable to the implementation of high-order and high-Q filters. There are two design methods to simulate *LC* ladder filter:

1. SGF (signal-graph-flow) simulation, which converts the passive *LC* ladder network into SGF and implement the SGF using SI technology.
2. Wave synthesis technique, which simulates the passive network ladder using wave quantities and realizes the resultant wave filter using SI technology.

The SGF synthesis technique first maps the passive *LC* ladder network to an equivalent interconnected collection of mathematical equations and expresses these equations in

the form of SGF. The SI ladder filter is synthesized from the SGF and implemented using SI technology.

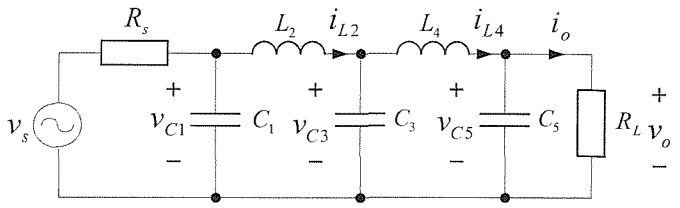


Fig.2.12 (a) 5th-order *LC* lowpass filter with voltage source

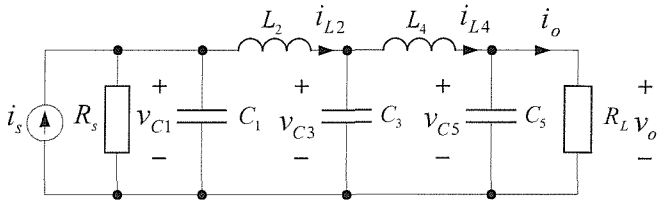


Fig.2.12 (b) 5th-order *LC* lowpass filter with current source

To illustrate this design method, the procedure to realize the 5th-order lowpass ladder filter is described. As shown in Fig.2.12(a), voltage and current variables are assigned to each branch in the *LC* ladder filter, and the doubly terminated structure provides minimum sensitivity to component variations.. In order to process the signal in current-mode, Norton principle is used to transform the voltage source into current source, Fig.2.12(b). In the *LC* prototype the normalized terminated resistors R_s and R_L are 1ohm, so the values of current-mode input and output signals (i_s and i_o) are the same as those of voltage-mode counterparts (v_s and v_o). The signal flow graph of Fig.2.12(b) is constructed to satisfy Kirchhoff's loop and node equations:

$$v_{C1} = \frac{1}{sC_1}(i_s - i_{Rs} - i_{L2}) \qquad (2.23a)$$

$$i_{L2} = \frac{1}{sL_2}(v_{C1} - v_{C3}) \qquad (2.23b)$$

$$v_{C3} = \frac{1}{sC_3}(i_{L2} - i_{L4}) \qquad (2.23c)$$

$$i_{L4} = \frac{1}{sL_4}(v_{C3} - v_{C5}) \qquad (2.23d)$$

$$v_{C5} = \frac{1}{sC_5}(i_{L4} - i_o) \qquad (2.23e)$$

Because SI circuits process current-mode signals, all of the voltage variables in signal-flow-graph must be transformed to current variables using a scaling resistor (chosen to be 1ohm for convenience), and the outputs are expressed as:

$$'i_{C1}' = \frac{1}{sC_1}(i_s - i_{Rs} - i_{L2}) \qquad (2.24a)$$

$$i_{L2} = \frac{1}{sL_2}('i_{C1}' - 'i_{C3}') \qquad (2.24b)$$

$$'i_{C3}' = \frac{1}{sC_3}(i_{L2} - i_{L4}) \qquad (2.24c)$$

$$i_{L4} = \frac{1}{sL_4}('i_{C3}' - 'i_{C5}') \qquad (2.24d)$$

$$'i_{C5}' = \frac{1}{sC_5}(i_{L4} - i_o) \qquad (2.24e)$$

where $'i_{Ci}'$ represents current converted by voltage v_{Ci}

It is obvious from Fig.2.12(b) that the values of scaling current variable $'i_{C1}'$ and $'i_{C5}'$ are the same as those of i_{Rs} and i_o, respectively.

$$'i_{C1}' = i_{Rs} \qquad (2.25a) \qquad\qquad 'i_{C5}' = i_o \qquad (2.25b)$$

Taking into account of Eq.(2.25) and applying z-domain transformation to Eq.(2.24), the relations for the signal flow graph are obtained:

$$i_{Rs} = \frac{1}{\lambda \cdot C_1 \cdot f_s}(i_s - i_{Rs} - i_{L2}) = \frac{1}{\lambda \cdot \alpha_1}(i_s - i_{Rs} - i_{L2}) \qquad (2.26a)$$

$$i_{L2} = \frac{1}{\lambda \cdot L_2 \cdot f_s}(i_{Rs} - 'i_{C3}') = \frac{1}{\lambda \cdot \alpha_2}(i_{Rs} - 'i_{C3}') \qquad (2.26b)$$

$$'i_{C3}' = \frac{1}{\lambda \cdot C_3 \cdot f_s}(i_{L2} - i_{L4}) = \frac{1}{\lambda \cdot \alpha_3}(i_{L2} - i_{L4}) \qquad (2.26c)$$

$$i_{L4} = \frac{1}{\lambda \cdot L_4 \cdot f_s}('i_{C3}' - 'i_{C5}') = \frac{1}{\lambda \cdot \alpha_4}('i_{C3}' - i_o) \qquad (2.26d)$$

$$i_o = \frac{1}{\lambda \cdot C_5 \cdot f_s}(i_{L4} - i_o) = \frac{1}{\lambda \cdot \alpha_5}(i_{L4} - i_o) \qquad (2.26e)$$

where λ is z-domain integrator.

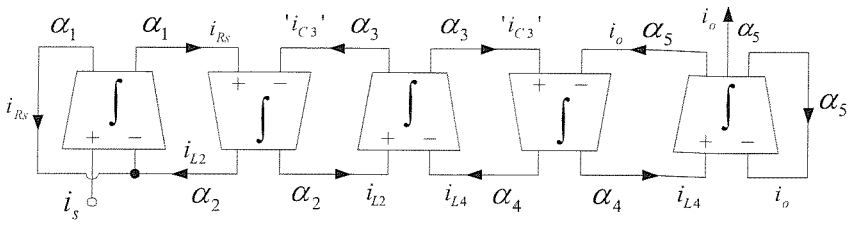


Fig.2.13 SGF of SI 5th-order lowpass filter

The signal graph flow (SGF) of the 5th-order lowpass SI ladder filter is shown in Fig.2.13. Currents are summed at the input of the integrators, and multiple output currents are generated for each output required. α_1 through α_5 represent the integrator scale factors obtained from Eq.(2.26). Early approaches to the realization of SI ladder filters relied on the use of Euler integrators (Fig.2.4 and Fig.2.5) [13]. However, these were restricted to the application in which the clock frequency was much higher than the cutoff frequency because of the errors inherent in Euler transformations [83,84]. Now bilinear integrators (Fig.2.7 and Fig.2.8) are often used to implement SI integrator-based filters with better sensitivities and low clock to cutoff frequency ratios [11,12,18].

2.4 Wave synthesis technique

Wave synthesis technique simulates passive LC networks through the use of wave quantities instead of node voltages and branch currents. The advantages of wave filters are their excellent passband sensitivity properties and bilinear relationship between continuous and discrete-time domains. The basic idea of this technique is reviewed as follows.

2.4.1 Wave models

The wave synthesis technique developed by Fettweis [24] is modelled after classical filters, preferably in lattice or ladder configurations. This technique simulates the behaviour of passive networks through the use of wave quantities instead of port voltages and currents, Fig.2.14. The wave variables A (incident wave) and B (reflected wave) are defined as linear combinations of the corresponding port current, i and voltage, v:

$$A = v + i \cdot R \qquad (2.27a) \qquad\qquad B = v - i \cdot R \qquad (2.27b)$$

where R is port resistance, and is chosen arbitrarily to simplify the wave model. For the passive components: R, L and C, their port resistances are R, $2L/T$ and $T/2C$, respectively (T is the sampling period).

Fig.2.14 Passive network and its wave block

Using this technique, the passive elements, such as capacitor C and inductor L, are first transformed into one-port wave models, and then these wave models are connected to form the wave filter.

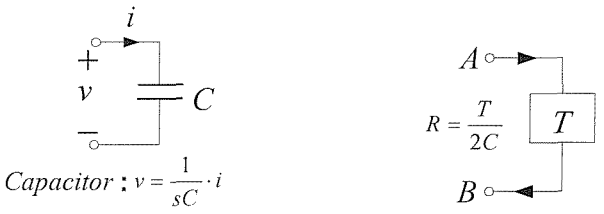


Fig.2.15 Capacitor and its wave model

For the passive component C, the $T/2C$ is selected as its port resistance, and its corresponding wave relationship can be derived from Eq.(2.27):

$$\frac{B}{A}=\frac{v-R\cdot i}{v+R\cdot i}=\frac{i\cdot(1/Cs)-i\cdot(T/2C)}{i\cdot(1/Cs)+i\cdot(T/2C)} \qquad (2.28)$$

Applying bilinear transformation $s \rightarrow z$ to Eq.(2.28), the wave relationship is given as:

$$B(z)=z^{-1}A(z) \qquad (2.29)$$

For the passive component L, the $2L/T$ is selected as its port resistance, and its corresponding wave relationship can be derived from Eq.(2.27):

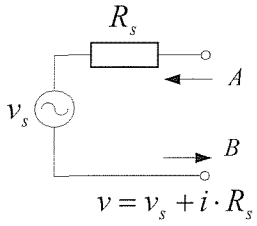
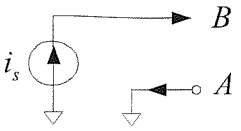
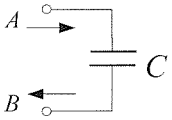
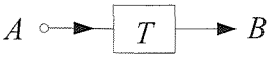
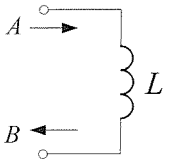
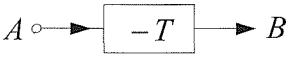
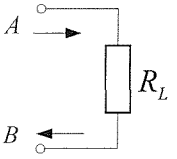
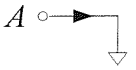
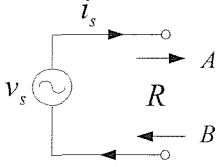
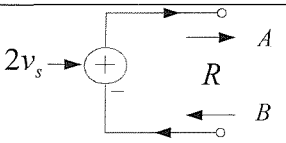
$$\frac{B}{A}=\frac{v-R\cdot i}{v+R\cdot i}=\frac{i\cdot(Ls)-i\cdot(2L/T)}{i\cdot(Ls)+i\cdot(2L/T)} \qquad (2.30)$$

Applying bilinear transformation $s \rightarrow z$ to Eq.(2.30), the wave relationship is given as:

$$B(z)=-z^{-1}A(z) \qquad (2.31)$$

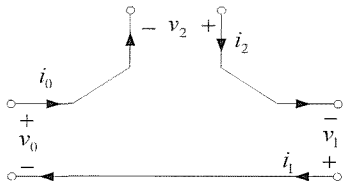
It is shown from Eq.(2.29) and Eq.(2.31) that using wave synthesis technique capacitor and inductor are converted into delay cell and negative delay cell, respectively. Similarly, other passive elements, which are used to design passive filter, can also be transformed into their corresponding wave models and given in Table 2.3.

Table 2.3 One-port passive elements and their wave models

Component	*Port Resistance*	*Wave Model*
Resistor Source  $v = v_s + i \cdot R_s$	R_s	 $B(n) = i_s(n) = v_s(n)$
Capacitor  $v = \frac{1}{sC} \cdot i$	$\frac{T}{2C}$	 $B(n) = A(n-1)$
Inductor  $v = sL \cdot i$	$\frac{2L}{T}$	 $B(n) = -A(n-1)$
Resistor  $v = i \cdot R_L$	R_L	 $A(n) = 2v = 2i \cdot R_L$ $B=0$
Voltage Source  	R	 $A(n) = 2v_s - B(n)$

2.4.2 Wave adaptors

In order to transform *LC* network into wave structure, wave synthesis technique models the connections in passive network as wave adaptors.



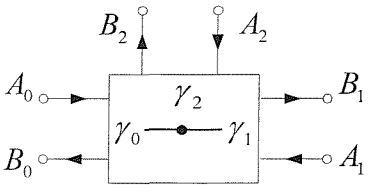


Fig.2.16 Series connection of *3-ports* and its equivalent wave series adaptor

The voltage-current relationships of *n-ports* series passive network connection, i.e. *3-port* series connection in Fig.2.16, are:

$$v_0 + v_1 + \cdots + v_{n-1} = 0\,,\ i_0 = i_1 = \cdots = i_{n-1} \tag{2.32}$$

The wave quantities of each port are given as:

$$A_i = v_i + R_i \cdot i_i\,, \qquad B_i = v_i - R_i \cdot i_i\,, \qquad i = 0,1,2\cdots(n-1) \tag{2.33}$$

According to the voltage-current relationships of series connection, Eq.(2.32), and the definition of wave quantities, Eq.(2.33), the following relations can be obtained:

$$A_0 + A_1 + \cdots + A_{n-1} = (R_0 + R_1 + \cdots + R_{n-1}) \cdot i_i \tag{2.34a}$$

$$B_i = A_i - 2R_i \cdot i_i \tag{2.34b}$$

$$\Rightarrow\ B_i = A_i - \frac{2R_i}{(R_0 + R_1 + \cdots + R_{n-1})} \cdot (A_0 + A_1 + \cdots + A_{n-1}) \tag{2.34c}$$

The term $\dfrac{2R_i}{(R_0 + R_1 + \cdots + R_{n-1})}$ in Eq.(2.34c) is defined as series wave adaptor coefficient γ_i :

$$\gamma_i = \frac{2R_i}{(R_0 + R_1 + \cdots + R_{n-1})} \tag{2.35}$$

According to this definition, the wave relationship of series wave adaptor can be rewritten as:

$$B_i = A_i - \gamma_i \cdot (A_0 + A_1 + \cdots + A_{n-1}) \tag{2.36}$$

And the relationships of wave quantities in *3-port* series wave adaptor are:

$$\begin{bmatrix} B_2 \\ B_1 \\ B_0 \end{bmatrix} = \begin{bmatrix} 1-\gamma_2 & -\gamma_2 & -\gamma_2 \\ -\gamma_1 & 1-\gamma_1 & -\gamma_1 \\ -\gamma_0 & -\gamma_0 & 1-\gamma_0 \end{bmatrix} \cdot \begin{bmatrix} A_2 \\ A_1 \\ A_0 \end{bmatrix} \tag{2.37}$$

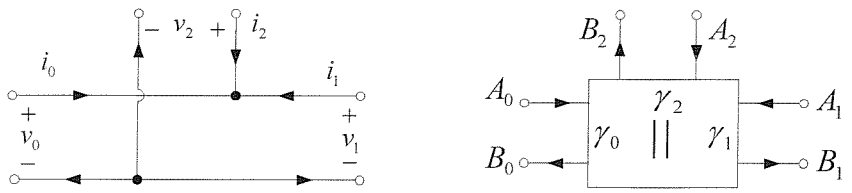


Fig.2.17 Parallel connection of *3-ports* and its equivalent wave parallel adaptor

The voltage-current relationships of *n-ports* parallel passive network connection, i.e. *3-port* parallel connection in Fig.2.17, are:

$$v_0 = v_1 = \cdots = v_{n-1},\ i_0 + i_1 + \cdots + i_{n-1} = 0 \tag{2.38}$$

According to the voltage-current relationships of parallel connection, Eq.(2.38), and the definition of wave quantities, Eq.(2.33), the following relations can be obtained:

$$G_0 \cdot A_0 + G_1 \cdot A_1 + \cdots + G_{n-1} \cdot A_{n-1} = (G_0 + G_1 + \cdots + G_{n-1}) \cdot v_i \tag{2.39a}$$

$$B_i = 2v_i - A_i, \text{ where } G_i = 1/R_i \tag{2.39b}$$

$$\Rightarrow B_i = \frac{2G_0}{(G_0 + G_1 + \cdots + G_{n-1})} \cdot A_0 + \cdots + \frac{2G_{n-1}}{(G_0 + G_1 + \cdots + G_{n-1})} \cdot A_{n-1} - A_i \tag{2.39c}$$

The term $\frac{2G_i}{(G_0 + G_1 + \cdots + G_{n-1})}$ in Eq.(2.39c) is defined as parallel wave adaptor coefficient γ_i:

$$\gamma_i = \frac{2G_i}{(G_0 + G_1 + \cdots + G_{n-1})} \tag{2.40}$$

According to this definition, the relationship of parallel wave adaptor can be rewritten as:

$$B_i = \gamma_0 \cdot A_0 + \cdots + \gamma_{n-1} A_{n-1} - A_i \tag{2.41}$$

And the relationships of wave quantities in *3-port* parallel wave adaptor are:

$$\begin{bmatrix} B_2 \\ B_1 \\ B_0 \end{bmatrix} = \begin{bmatrix} \gamma_2 - 1 & \gamma_1 & \gamma_0 \\ \gamma_2 & \gamma_1 - 1 & \gamma_0 \\ \gamma_2 & \gamma_1 & \gamma_0 - 1 \end{bmatrix} \cdot \begin{bmatrix} A_2 \\ A_1 \\ A_0 \end{bmatrix} \tag{2.42}$$

According to the definitions of wave adaptor coefficients, Eq.(2.35) and Eq.(2.40), the following relations should be satisfied:

For each *n*-port wave adaptor, the sum of wave adaptor coefficients is 2:

$$\sum_{k=0}^{n-1} \gamma_k = 2 \tag{2.43}$$

For series wave adaptor:

$$\frac{\gamma_0}{R_0} = \frac{\gamma_1}{R_1} = \cdots = \frac{\gamma_{n-1}}{R_{n-1}} \tag{2.44a}$$

For parallel wave adaptor:

$$\frac{\gamma_0}{G_0} = \frac{\gamma_1}{G_1} = \cdots = \frac{\gamma_{n-1}}{G_{n-1}} \tag{2.44b}$$

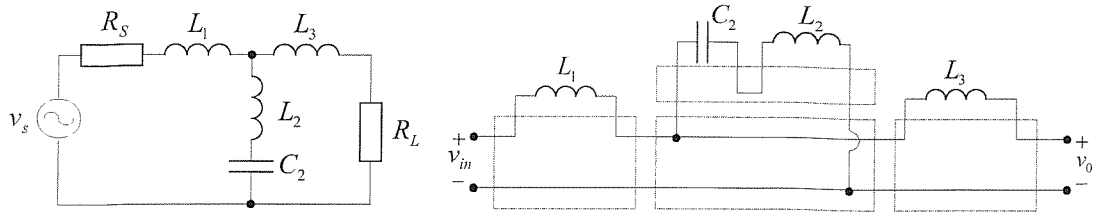


Fig.2.18 (a) 3rd-order elliptic filter (b) Passive circuit with identified series and parallel connections

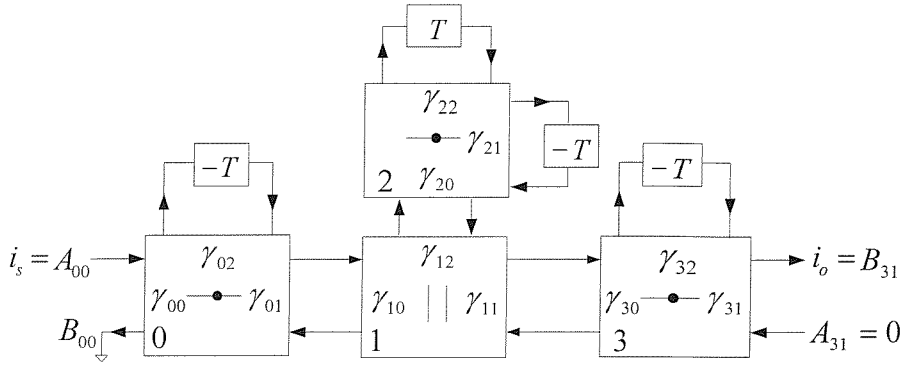


Fig.2.18 (c) Transformed wave filter structure

The conversion process from *LC* network to wave filter is illustrated through an example of 3rd-order *LC* elliptic filter, shown in Fig.2.18(a). It is redrawn in Fig.2.18(b) in order to make apparent the consecutive series and parallel connections (surrounded by dashed squares). The passive components are converted into their wave models according to Table 2.3, and these wave models are connected using wave adaptors, Fig.2.18(c). In this way, the 3rd-order wave filter is derived, where γ_{ij} is coefficient of port j in wave adaptor i. It should note that according to the Table 2.3 the input voltage resistor source in Fig.2.18(a) is transformed to current source i_s with the same value as voltage source v_s, while the resistor load is transformed to output current i_o with twice value of output voltage v_o. Therefore, the transfer function of 3rd-order *LC* elliptic filter is left unchanged through wave synthesis technique:

$$H(z) = i_o(z)/i_s(z) = 2 \cdot v_o(z)/v_s(z) \qquad (2.45)$$

2.5 SI wave filters

In section 2.4, wave synthesis technique is introduced and the design process of wave filters is described. The wave filters were originally implemented using digital

technology, but recently SI realization is proposed, where wave variables A_j and B_j are represented as current-mode signal [25]. It can be seen from Fig.2.18(c) that the resultant wave filter only consists of delay cells and wave adaptors, which will result in simple implementation.

SI implementation of delay cell

The delay cell in SI wave filter can be realized by cascading two SI memory cells. The 1st and 2nd-generation SI delay cell are shown in Fig.2.19. Compared with the 1st-generation SI delay cell, the basic 2nd-generation SI delay cell has large internal transient glitches that cause large linear and non-linear circuit errors [34]. The high performance 2nd-generation SI delay cell, S^2I, has been proposed to reduce these non-ideal characteristics [41]. The schemes of S^2I and its performance on SI wave filters will be analysed in Chapter 3.

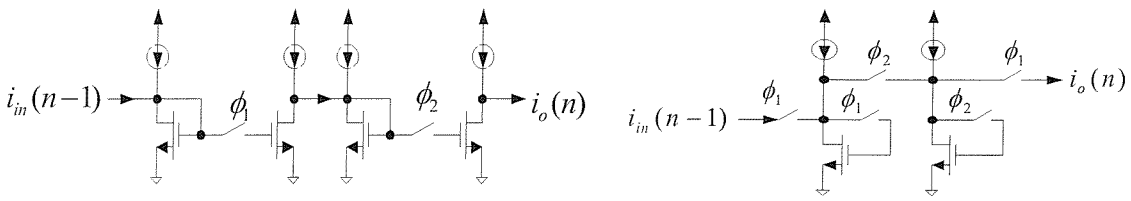


Fig.2.19 1st and 2nd-generation SI delay cell

SI implementation of wave adaptors

Wave adaptors are multi-port current-mode circuits implementing the algebraic relations between wave variables. Therefore, they only involve the use of summing current amplifiers with different gain factors. An efficient circuit implementation of *3-port* series and parallel wave adaptor was proposed in [28], shown in Fig.2.20. It establishes the direct correspondence between wave adaptor relations, Eq.(2.37) and Eq.(2.42), and SI transistor-level circuits. The wave adaptor coefficients in Fig.2.20 are implemented through the aspect ratio of the current mirror transistors.

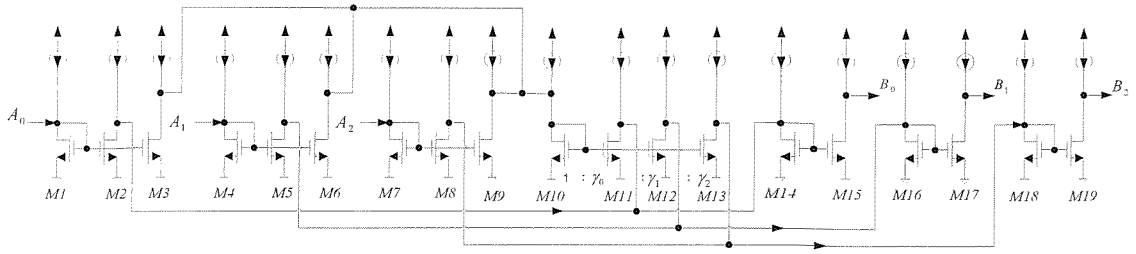


Fig.2.20 (a) SI circuit of *3-port* series wave adaptor [28]

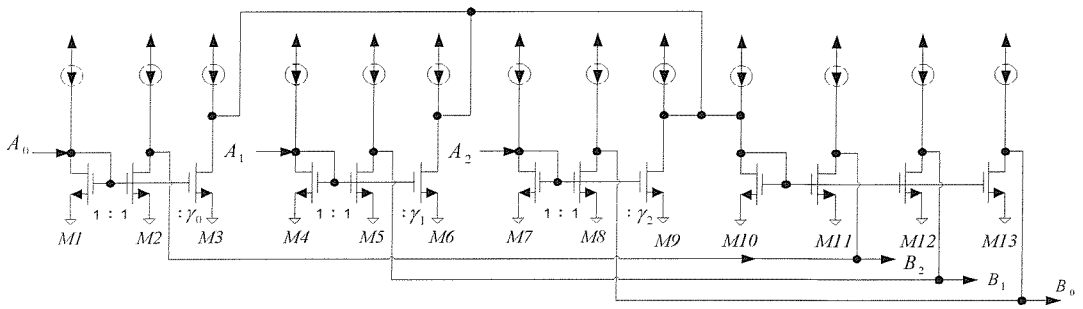


Fig.2.20 (b) SI circuit of *3-port* parallel wave adaptor [28]

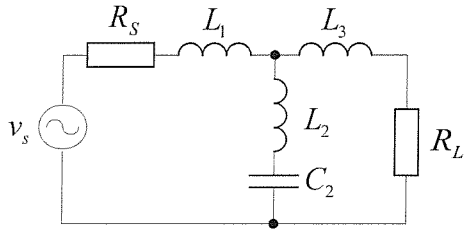


Fig.2.21 (a) 3[rd]-order *LC* elliptic filter

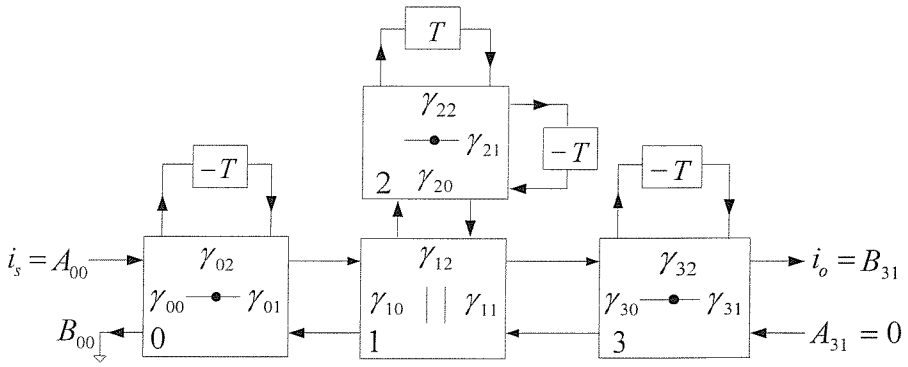


Fig.2.21 (b) Equivalent 3[rd]-order elliptic wave filter

To illustrate the design process and implementation, a design example of SI wave filter is presented. Given the discrete-time filter specification: sampling frequency f_{CLK} =*1MHz*, passband frequency f_p =*0.1MHz*, maximum passband ripple

$A_{max}=0.177dB$, minimum stopband ripple $A_{min} \geq 35dB$. According to these specifications, 3rd-order elliptic LC prototype, Fig.2.21(a), is chosen with normalized component values as follows [81]:

$$R_s = R_L = 1ohm,\ L_1 = L_3 = 1.1215H,\ L_2 = 0.0925H,\ C_2 = 1.0593F \qquad (2.46)$$

The normalized ($T=1$) passband frequency is $f_p / f_{CLK} = 0.1$. Prewarping of the passband frequency is performed according to the continuous-time, Ω, and discrete-time frequency, ω, transformation:

$$\Omega = \frac{2}{T} \cdot \tan(\frac{\omega T}{2}) \qquad (2.47)$$

The corresponding continuous-time passband frequency is:

$$\Omega = 2 \cdot \tan(0.1 \cdot \pi) = 0.65 \qquad (2.48)$$

The passive components in the LC prototype are calculated according to the continuous-time passband frequency:

$$L_1 = L_3 = 1.1215/0.65=1.725H,\quad L_2 = 0.0925/0.65=0.142H,$$
$$C_2 = 1.0593/0.65=1.63F \qquad (2.49)$$

Wave filter is constructed as outlined in section 2.4, Fig.2.21(b). The port resistance is calculated according to their definitions:

$$R_{00} = R_{31} = 1,\qquad R_{02} = R_{32} = 2L_1 / T = 3.45,$$
$$R_{21} = 2L_2 / T = 0.248,\qquad R_{22} = T / 2C_2 = 0.307 \qquad (2.50)$$

The wave adaptor coefficients are calculated as follows: for the *wave adaptor0*, the relationships of coefficients are:

$$\frac{\gamma_{00}}{R_{00}} = \frac{\gamma_{01}}{R_{01}} = \frac{\gamma_{02}}{R_{02}} \qquad (2.51a) \qquad \gamma_{00} + \gamma_{01} + \gamma_{02} = 2 \qquad (2.51b)$$

In order to simplify the circuit implementation, we set $\gamma_{01} = 1$, and according to Eq.(2.51), the other coefficients in *wave adaptor0* and port resistance R_{01} are calculated as:

$$\gamma_{00} = 0.225,\qquad \gamma_{02} = 0.775,\qquad R_{01} = 4.44 \qquad (2.52)$$

Similarly, setting $\gamma_{20} = 1$, the coefficients of *wave adaptor2* are calculated as:

$$\gamma_{21} = 0.447,\qquad \gamma_{22} = 0.553,\qquad R_{20} = 0.555 \qquad (2.53)$$

The relationships of coefficients in *wave adaptor1* are:

$$\frac{\gamma_{10}}{G_{10}} = \frac{\gamma_{11}}{G_{11}} = \frac{\gamma_{12}}{G_{12}} \qquad (2.54a) \qquad \gamma_{10} + \gamma_{11} + \gamma_{12} = 2 \qquad (2.54b)$$

It can be seen from Fig.2.21 that the port resistance $R_{10} = R_{01}$, $R_{12} = R_{20}$. Setting $\gamma_{11} = 1$, the other coefficients in *wave adaptor1* and port resistance R_{11} calculated as:

$$\gamma_{10} = 0.11, \qquad \gamma_{12} = 0.89, \qquad R_{11} = 0.493 \qquad (2.55)$$

Using the definition of series adaptor coefficient, Eq.(2.35), the coefficients in *wave adaptor3* are:

$$\gamma_{30} = 2R_{30}/(R_{30} + R_{31} + R_{32}) = 0.2, \quad \text{where } R_{30} = R_{11} \qquad (2.56a)$$

$$\gamma_{31} = 2R_{31}/(R_{30} + R_{31} + R_{32}) = 0.4 \qquad (2.56b)$$

$$\gamma_{32} = 2 - \gamma_{30} - \gamma_{31} = 1.4 \qquad (2.56c)$$

When the wave filter is built up, the transistor-level circuits described in this section can be employed to realize the current delay cell and current-mode wave adaptors.

2.6 SI wave filters based on Bruton transformation

In section 2.5, the wave filter structure is directly derived from the *LC* reference prototype. When Bruton transformation [81] is applied to suitably selected *LC* networks prior to their conversion to wave filter, it will yield less complicated SI circuits for a given filter response. Bruton transformation eliminates inductors in the *LC* circuit by multiplying impedance by 1/s. This converts resistors to capacitors, inductors to resistors and capacitors to FDNR (frequency dependent negative resistor) elements, Fig.2.22.

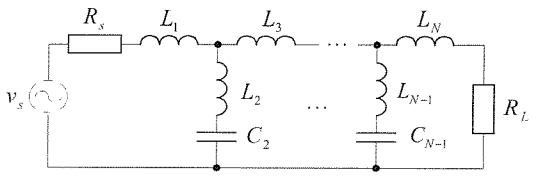


Fig.2.22 (a) *Nth*-order minimum-C elliptic *LC* reference prototype

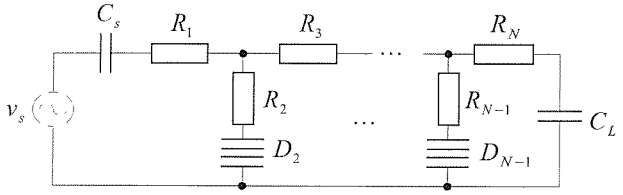


Fig.2.22 (b) *Nth*-order transformed prototype using Bruton transformation

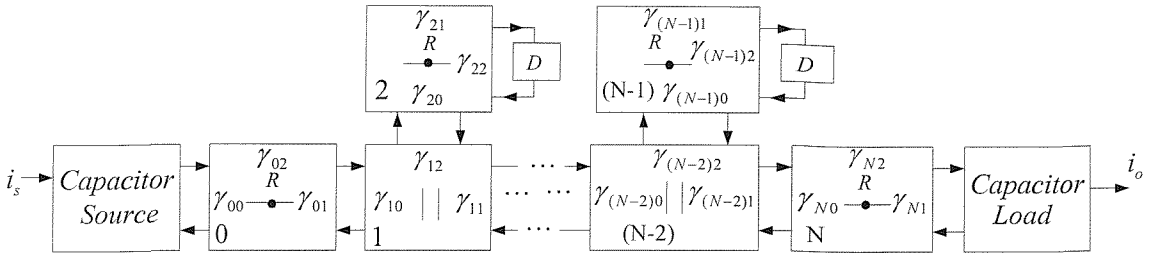
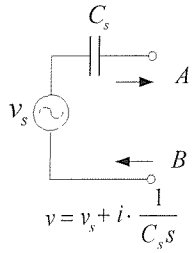
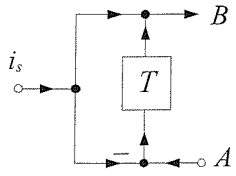
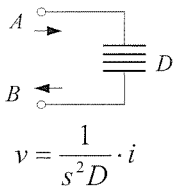
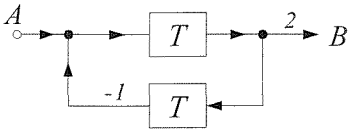
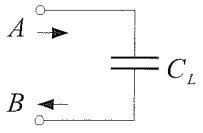
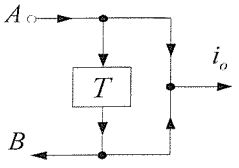


Fig.2.22 (c) *Nth*-order wave structure based on Bruton transformation

After making Bruton transformation, the complexity of wave adaptors is significantly reduced due to the presence of the resistors in Fig.2.22(b). These resistors effectively reduce the number of ports required in wave adaptors. Fig.2.22(c) shows the *Nth*-order transformed wave structure based on Bruton transformation. The element labelled 'D' denotes the FDNR components, while wave adaptors labelled 'R' are simplified to incorporate the resistance output. The new components as a result of applying Bruton transformation to reference prototype are: FDNR, capacitive source and load, Table 2.4.

Table 2.4 New wave models for Bruton transformation wave filters

Component	*Port Resistance*	*Wave Model*
Capacitive Source  $v = v_s + i \cdot \frac{1}{C_s s}$	$\frac{T}{2C_s}$	 $B(n) = i_s(n) - i_s(n-1) + A(n-1)$
FDNR  $v = \frac{1}{s^2 D} \cdot i$	$(\frac{T}{2})^2 \frac{1}{D}$	 $B(n) = 2A(n-1) - B(n-2)$
Capacitive Load  $v_o = i \cdot \frac{1}{C_L s}$	$\frac{T}{2C_L}$	 $B(n) = A(n-1)$ $i_o(n) = A(n) + B(n) = 2v_o(n)$

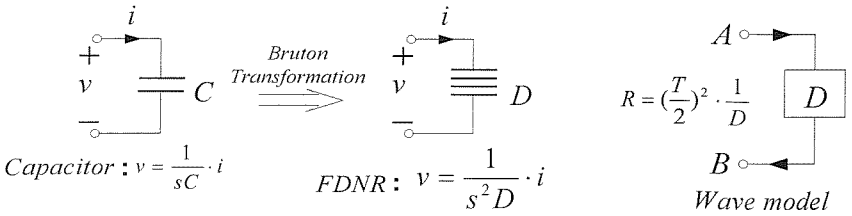


Fig.2.23 FDNR and its wave model

Fig.2.23 shows new component FDNR, which is obtained by multiplying 1/s on the capacitor. $(T/2)^2/D$ is selected as its port resistance, and its corresponding wave model can be derived as:

$$\frac{B}{A}=\frac{v-R\cdot i}{v+R\cdot i}=\frac{i\cdot(1/s^2D)-i\cdot(T/2)^2/D}{i\cdot(1/s^2D)+i\cdot(T/2)^2/D} \tag{2.57}$$

Applying bilinear transformation $s\rightarrow z$ to Eq.(2.52), it is given as:

$$B(z)=\frac{2z^{-1}}{1+z^{-2}}\cdot A(z) \tag{2.58}$$

For other new components, including capacitive source and load, new wave models can be derived in the same way and given in Table 2.4. It can be seen that the wave models needed to design the Bruton transformation wave filter are more complex than those required for the direct wave synthesis technique. However Bruton transformation produces a large number of resistors replacing inductances, and it not only simplifies the wave adaptors but also reduces the number of delays in the circuit. According to circuit theory [81], the transfer function of passive network is left unchanged after Bruton transformation is applied. Therefore, the transfer functions of Bruton transformation wave filters are the same as those of direct wave filters.

2.7 Comparison of design techniques

Several techniques for designing SI filters have been reviewed. The synthesis of cascade filter, which based on the biquadratic section, is relatively straightforward. The biquadratic sections are 2nd-order building blocks, which can be cascaded to form high order filters. The modularity and simplicity of this approach has led to its wide acceptance in active-RC, SC and SI filters design. The drawback of this technique is the relatively high sensitivity to the component variations, especially in high-order or high-Q filters. Therefore, to realize high-order or high-Q filters, *LC* simulation technique, which is less sensitive to manufacturing tolerances, is needed. The SFG (signal flow graph) synthesis of *LC* filter, which inherits the low component sensitivity

of ladder network, has proved to be particularly suited to the implementation of high-order and high-Q filters. Different integrators, the fundamental building block of this method, were investigated to improve the filter performance. However, the implementation of high-Q or lossless integrator is difficult [25,83]. Besides the difficulty of realizing high-Q integrators, integrators also impose a significant limitation on the filter performance, such as noise and limited dynamic range [1,25]. The wave technique is another design method to simulate the passive *LC* filters through wave variables. Unlike SFG simulation, the resultant SI circuit only consists of delay cell and wave adaptors, which are easily available in SI technology, and doesn't require integrators. Therefore, SI wave filter is a powerful alternative to the integrator-based SI filter. New efficient designing method for SI wave filter, Bruton transformation SI wave filter, has been proposed [2,3]. It not only inherits the advantages of SI wave filter, but also yields less complex SI circuits by applying Bruton transformation to suitably selected *LC* prototype prior to its conversion to wave filter. The saving achieved in SI elements can be expressed in terms of total transistor count, as shown in Table 2.5. It shows the total transistor count against filter order *N* for lowpass and highpass filters using the Bruton transformation and the direct SI wave filters.

Table 2.5 Complexity of SI lowpass and highpass elliptic wave filter [2]

SI element	*Lowpass (Direct Wave)*	*Lowpass (Bruton Wave)*	*Highpass (Direct Wave)*	*Highpass (Bruton Wave)*
Delay	*[3N/2]*	*2+2[N/2]*	*[3N/2]*	*2+2[N/2]*
CM_1	*4[N/2]*	*5[N/2]+3*	*N+3[N/2]*	*5[N/2]+3*
CM_2	*6[N/2]+3[N/2]*	*4[N/2]+ 3[N/2]+3*	*6[N/2]+3[N/2]*	*5[N/2]+ 3[N/2]+3*
CM_3	*N*	*[N/2]*	*N*	*[N/2]*
CM_4	*[N/2]*	*0*	*0*	*0*
Total transistor count	*12[3N/2]+8N +52[N/2] +18[N/2]*	*76[N/2]+ 18[N/2]+54*	*12[3N/2]+48[N/2] +18[N/2]+12N*	*82[N/2]+ 18[N/2]+54*

[] is the value rounded to the nearest integer, N=filter order, CM_n *is current mirror with n output.*

Table 2.5 shows Bruton transformation SI wave filter results in a lower transistor count, particularly for high-order filters, and this reduction improves with increasing order. For example, 7^{th}-order lowpass Bruton transformation SI wave filter requires 20% fewer delay elements, 36% fewer one-output current mirrors and 70% fewer three-output current mirrors, while 14^{th}-order highpass filter utilizes 15% fewer transistors. Reduction of transistor count in Burton transformation wave filter implies reduced silicon area, less power dissipation and noise, all of which are important performance parameters of mixed-signal ICs.

2.8 Concluding remarks

Design techniques of SI filters have been reviewed. The wave synthesis technique is introduced, and detailed design example of SI wave filter is included. It is shown SI wave filters only consists of delay cells and wave adaptors and have simple implementation. The recently reported Bruton transformation SI wave filters are presented. From the discussion in section 2.7, it shows Bruton transformation SI wave filters not only have low sensitivity and simplicity, but also yield significant reduction in SI circuits complexity compared with the direct wave filter. Therefore, further investigations of Bruton transformation wave filters, including the performance in the presence of non-ideal characteristics of SI circuits and transistor-level circuits design of such filters, are necessary to be made. In addition, SI group delay equalizers, which are used to improve the step response of the SI filters, are also required to be designed to realize the linear phase response of SI filters. These investigations will be carried out in order to better understanding of Bruton transformation SI wave filters and group delay equalizers.

Chapter 3

Non-ideal Performance of Bruton Transformation SI Wave Filters

3.1 Introduction

Chapter 2 has shown that the application of Bruton transformation in the design of wave filters can yield significant reduction in the SI circuit complexity. Despite their simplicity, SI cells suffer from fundamental sources of errors that produce deviations in terms of DC offset, gain and harmonic distortion. Although numerous enhanced SI cells have been proposed to improve performance [60-68], they do not eliminate the errors completely. Therefore, it is important to study the effects of these errors on the SI cells performance. Section 3.2 describes the two sources of errors: mismatch in current mirror and clock-feedthrough in SI delay cell. Taking account of these errors, the non-ideal input-output relations of new wave components in Bruton transformation SI wave filters are derived in section 3.3. These non-ideal relations are integrated with *MATLAB* to investigate the influence of errors, such as mismatch and clock-feedthrough, on the filter performance in section 3.4. Section 3.5 gives a detailed analysis of the speed limitation of Bruton transformation SI wave filters. Finally, section 3.6 concludes this chapter.

3.2 Non-ideal behaviour of current mirrors and SI delay cell

This section briefly discusses non-ideal characteristics in current mirrors and SI delay cells and shows how these non-ideal characteristics are represented using simple models. The discussion is a short summary of [37] and is included here since it is used in the development of the behavioural non-ideal models of Bruton transformation wave filter components, which have been given in Chapter 2.

3.2.1 Mismatch on current mirror

A simple current mirror with gain G is shown in Fig.3.1(a). The current mirror suffers from mismatch errors due to the fabrication process and finite precision of device with width and length. The small variations in the DC characteristics (threshold voltage V_T and current factor β) of MOS transistor are introduced due to mismatch errors. For the current mirror, the effect of mismatch is to produce DC offset, gain and non-linear errors on the output current i_o.

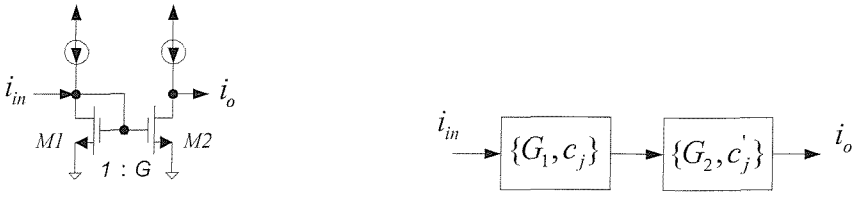


Fig.3.1 (a) Simple current mirror with gain G (b) Block diagram of cascaded current mirror

To deduce the non-ideal input-output relationship, which taking into account of the mismatch effect, we assume that the parameters β_1^o, β_2^o, V_{T1}^o, and V_{T2}^o ($G = \beta_2^o / \beta_1^o$ and $V_{T1}^o = V_{T2}^o$) are the nominal values of the current factors and threshold voltages of transistors *M1* and *M2*, respectively. Transistor mismatch errors are random in nature, and so these four mentioned parameters are affected by $\Delta\beta_1$, $\Delta\beta_2$, ΔV_{T1} and ΔV_{T2} which have normal distribution variations [38]. The drain currents of *M1* and *M2* are given in Eq.(3.1):

$$I_B + i_{in} = (\beta_1^o + \Delta\beta_1)[V_{GS} - (V_{T1}^o + \Delta V_{T1})]^2 \tag{3.1a}$$

$$GI_B - i_o = (\beta_2^o + \Delta\beta_2)[V_{GS} - (V_{T2}^o + \Delta V_{T2})]^2 \tag{3.1b}$$

From Eq.(3.1), the following relation can be derived:

$$G - \frac{i_o}{I_B} = \frac{\beta_2^o + \Delta\beta_2}{I_B} \cdot [\sqrt{\frac{i_{in} + I_B}{\beta_1^o + \Delta\beta_1}} + (V_{T1}^o + \Delta V_{T1}) - (V_{T2}^o + \Delta V_{T2})]^2$$

$$= \frac{\beta_2^o + \Delta\beta_2}{\beta_1^o + \Delta\beta_1} \cdot [\sqrt{1 + \frac{i_{in}}{I_B}} + \sqrt{\frac{\beta_1^o + \Delta\beta_1}{I_B}} \cdot (\Delta V_{T1} - \Delta V_{T2})]^2$$

$$\approx \frac{\beta_2^o + \Delta\beta_2}{\beta_1^o + \Delta\beta_1} \cdot [1 + \frac{i_{in}}{I_B} + 2 \cdot (\Delta V_{T1} - \Delta V_{T2}) \cdot \sqrt{\frac{\beta_1^o}{I_B}} \cdot \sqrt{1 + \frac{i_{in}}{I_B}}] \tag{3.2}$$

$$G = \beta_2^o / \beta_1^o \Rightarrow \frac{\beta_2^o + \Delta\beta_2}{\beta_1^o + \Delta\beta_1} \approx G \cdot (1 + \frac{\Delta\beta_2}{\beta_2^o} - \frac{\Delta\beta_1}{\beta_1^o}) \tag{3.3}$$

$$I_B = \beta_1^o (V_{GS} - V_{T1})_Q^2 \Rightarrow \sqrt{I_B \cdot \beta_1^o} = \frac{I_B}{(V_{GS} - V_{T1})_Q} \tag{3.4}$$

Taking Eqs.(3.3) and (3.4) into Eq.(3.2), Eq.(3.2) can be expressed as:

$$GI_B - i_o = G \cdot (1 + \frac{\Delta\beta_2}{\beta_2^o} - \frac{\Delta\beta_1}{\beta_1^o}) \cdot$$
$$[I_B + i_{in} + 2 \cdot (\Delta V_{T1} - \Delta V_{T2}) \cdot \frac{I_B}{(V_{GS} - V_{T1})_Q} \cdot \sqrt{1 + \frac{i_{in}}{I_B}}] \tag{3.5}$$

Since $i_{in} << I_B$, $\sqrt{1 + \frac{i_{in}}{I_B}}$ can be approximately expanded into the following 2[nd]-order series form:

$$\sqrt{1 + \frac{i_{in}}{I_B}} \approx 1 + \frac{i_{in}}{2I_B} - \frac{1}{8} \cdot (\frac{i_{in}}{I_B})^2 \tag{3.6}$$

Taking the above approximation into Eq.(3.5), $GI_B - i_o$ is expressed as:

$$GI_B - i_o = G \cdot (1 + \frac{\Delta\beta_2}{\beta_2^o} - \frac{\Delta\beta_1}{\beta_1^o}) \cdot$$
$$[I_B + i_{in} + 2 \cdot (\Delta V_{T1} - \Delta V_{T2}) \cdot \frac{I_B}{(V_{GS} - V_{T1})_Q} \cdot (1 + \frac{i_{in}}{2I_B} - \frac{1}{8} \cdot (\frac{i_{in}}{I_B})^2] \tag{3.7}$$

After some arrangements, the input-output current relationship is given as:

$$i_o \cong c_o + c_1 i_{in} + c_2 i_{in}^2 \tag{3.8}$$

where c_0, c_1, and c_2 are error mismatch coefficients given in Table 3.1 for the nominal and non-ideal cases.

Table 3.1 Error coefficients due to mismatch in simple current mirror [37]

coefficient	*nominal*	*error term*
c_0	0	$-GI_B(\frac{\Delta\beta_2}{\beta_2^0} - \frac{\Delta\beta_1}{\beta_1^0}) + GI_B \frac{2(\Delta V_{T2} - \Delta V_{T1})}{(V_{GS} - V_{T1}^0)_Q}$
c_1	$-G$	$G[(\frac{\Delta\beta_2}{\beta_2^0} - \frac{\Delta\beta_1}{\beta_1^0}) + \frac{(\Delta V_{T2} - \Delta V_{T1})}{(V_{GS} - V_{T1}^0)_Q}]$
c_2	0	$\frac{-G(\Delta V_{T2} - \Delta V_{T1})}{4I_B(V_{GS} - V_{T1}^0)_Q}$

Since mismatch errors have random origin, the coefficient c_j in Table 3.1 is taken as the random variable with normal distribution, whose mean value is nominal value and standard deviation is related to the error terms. Thus, the variation of c_j can be expressed as:

$$\sigma^2(c_j) = (\frac{\partial c_j}{\partial \beta_1})^2 \cdot \sigma^2(\beta_1) + (\frac{\partial c_j}{\partial \beta_2})^2 \cdot \sigma^2(\beta_2) + (\frac{\partial c_j}{\partial V_{T1}})^2 \cdot \sigma^2(V_{T1}) + (\frac{\partial c_j}{\partial V_{T2}})^2 \cdot \sigma^2(V_{T2}) \quad (3.9)$$

Using the statistical models proposed in [38], relationship between the variation of β_j, V_{Tj} and transistor area is given as:

$$\frac{\sigma^2(\beta_j)}{\beta_j^2} = \frac{K_\beta^2}{(WL)_j}, \qquad \sigma^2(V_{Tj}) = \frac{K_{vt}^2}{(WL)_j} \quad (3.10)$$

where K_β and K_{vt} are technology-dependent parameters [38], *(WL)* is transistor gate area. Thus, the variation of c_j for $G = \beta_2^o / \beta_1^o$ can be defined as:

$$\sigma^2(c_0) = \frac{G^2 \cdot I_B^2}{(WL)_1} \cdot (1 + \frac{1}{G}) \cdot [K_\beta^2 + \frac{4K_{vt}^2}{(V_{GS} - V_{T1})_Q^2}] \quad (3.11a)$$

$$\sigma^2(c_1) = \frac{G^2}{(WL)_1} \cdot (1 + \frac{1}{G}) \cdot [K_\beta^2 + \frac{K_{vt}^2}{(V_{GS} - V_{T1})_Q^2}] \quad (3.11b)$$

$$\sigma^2(c_2) = \frac{G^2}{(WL)_1} \cdot (1 + \frac{1}{G}) \cdot \frac{K_{vt}^2}{16 I_B^2 \cdot (V_{GS} - V_{T1})_Q^2} \quad (3.11c)$$

For instance, for the parameters $K_\beta = 0.02\mu m$, $K_{vt} = 20mV \cdot \mu m$, $W/L = 60\mu m / 10\mu m$, $G=1$, $(V_{GS} - V_T) = 0.6V$ and $I_B = 10\mu A$, the standard deviations in c_0, c_1 and c_2 are 40.18nA, 0.224% and 48.11 A^{-1}, respectively.

SI filters also contain cascaded current mirrors. Fig.3.1(b) shows a block diagram representation of a cascaded current mirror, which consists of two simple current mirrors with gains G_1 and G_2. The parameters c_j and $c_j^{'}$ are the error mismatch coefficients of the simple current mirror given in Table3.1. Since mismatch errors are random in nature, the three coefficients are different from one current mirror to the others. It can be derived from Eq.(3.8) that the non-ideal input-output relationship of the cascaded current-mirror due to mismatch is:

$$i_o = C_0 + C_1 i_{in} + C_2 i_{in}^2 \qquad (3.12)$$

where $C_0 = c_0' + c_1' c_0 + c_2' c_0^2$, $C_1 = c_1' c_1 + 2c_1 c_0 c_2'$, $C_2 = c_1' c_2 + c_2' c_1^2 + 2c_2 c_2' c_0$

The nominal values for C_0 and C_2 are zero, while the nominal value of C_1 is $G_1 \cdot G_2$. The variance of C_j coefficients are written as:

$$\sigma^2(C_0) = \sigma^2(c_0') + c_1'^2 \sigma^2(c_0) \qquad (3.13a)$$

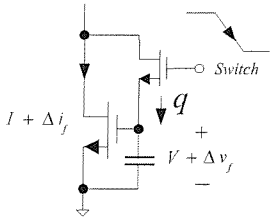
$$\sigma^2(C_1) = c_1'^2 \sigma^2(c_1) + c_1'^2 \sigma^2(c_1') \qquad (3.13b)$$

$$\sigma^2(C_1) = c_1'^2 \sigma^2(c_2) + c_1'^4 \sigma^2(c_2') \qquad (3.13c)$$

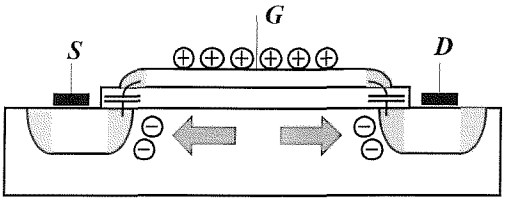
Using parameters $K_\beta = 0.02\mu m$, $K_{vt} = 20mV \cdot \mu m$, $W/L = 60\mu m/10\mu m$, $G=1$, $(V_{GS} - V_T) = 0.6V$ and $I_B = 10\mu A$, the standard deviations of C_0, C_1 and C_2 are calculated as 56.68nA, 0.317% and 68.04 A^{-1}, respectively.

3.2.2 Clock-feedthrough on SI delay cell

Clock-feedthrough is the main performance limitation in SI circuits and is inherent in any sampled-data systems using MOS switches [39,40].



(a) Switch turn-off in memory cell



(b) The clock-feedthrough in switch NMOS channel

Fig.3.2

When the sampling switch is turned off at the end of the sampling phase, Fig.3.2(a), the channel charge from the switch transistor is dissipated through its drain and source, and hence some of the charge is added onto the memory cell's hold capacitor. These charge transfers affect the gate voltage of the memory transistors and hence an error results in the memorized current. Approximate analysis was made to model clock-feedthrough errors in simple current memory cell as an error voltage on the data holding node.

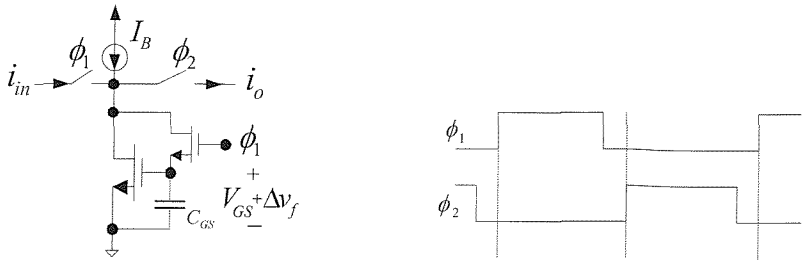


Fig.3.3 2nd-generation memory cell with voltage error at the holding node

For the 2nd-generation memory cell as illustrated in Fig.3.3, the absolute value of the voltage increment in the gate voltage is given in [1,37]:

$$|\Delta v_f| = k_1\sqrt{1+\frac{i_{in}}{I_B}} + k_2 \tag{3.14}$$

where k_1 and k_2 can be written as

$$k_1 = -\alpha\cdot\frac{C_{SW}}{C_{GS}}(1+\frac{\gamma}{3})\sqrt{\frac{I_B}{\beta_n}}, \qquad k_2 = \alpha\cdot\frac{C_{SW}}{C_{GS}}[V_H-(2+\frac{\gamma}{3})\cdot V_T]+\frac{C_{OL}}{C_{GS}}[V_H-V_L]$$

where C_{SW} and C_{OL} are the gate-to-source and gate-diffusion overlap capacitances of switch transistor, respectively, and C_{GS} is the memory transistor's gate-source capacitance. The coefficient α is proportional to the channel charge held in C_{GS} when the switch is closed ($\alpha \in [0.5,1]$). V_H and V_L are the high and low voltage clock levels, which are used to drive the switch, I_B is the bias current, γ and β_n are body factor and the current factor of an NMOS transistor, respectively. For the given NMOS transistor parameters:

$C_{ox} = 1.7\times10^{-3}\,pF/\mu m^2$, $C_{ol} = 310pF/m$, γ=0.76, $V_{T0} = 0.74V$,

$\beta_n = 221\mu A/V^2$, V_H=3.3V, V_L=0V, $I_B = 10\mu A$, $i_{in}/I_B = 0.5$

$(W/L)_{SW} = 2.4\mu m/1.2\mu m$, $(W/L) = 60\mu m/10\mu m$, $\alpha = 0.5$

$$\Rightarrow C_{SW} = (2/3)\times C_{ox}\times 2.4\times 1.2 = 3.264\times10^{-3}\,pF \tag{3.15a}$$

$$C_{OL} = C_{ol}\times 2.4\times10^{-6} = 7.44\times10^{-4}\,pF \tag{3.15b}$$

$$C_{GS} = (2/3)\times C_{ox}\times 60\times 10 = 0.68pF \tag{3.15c}$$

$$k_1 = -0.5\cdot\frac{0.003264}{0.68}\cdot(1+0.76/3)\cdot\sqrt{\frac{10}{224}} = -0.635mV \tag{3.15d}$$

$$k_2 = 0.5\cdot\frac{0.003264}{0.68}\cdot[3.3-(2+\frac{0.76}{3})\cdot0.74]+\frac{7.44\times10^{-4}}{0.68}\cdot5 = 6.6mV \tag{3.15e}$$

$$\left|\Delta v_f\right| = k_1\sqrt{1+\frac{i_{in}}{I_B}} + k_2 = 5.8mV \qquad (3.15f)$$

Due to the *N*-channel switch, the clock-feedthrough voltage Δv_f is $-5.8mV$. Taking into account of Δv_f, the input-output current relationship in memory cell of Fig.3.3 can be expressed as (phase ϕ_2):

$$\begin{aligned} i_o(n-\frac{1}{2}) &= I_B - \beta_n \cdot (V_{GS} - V_T + \Delta v_f)^2 \\ &= -i_{in}(n-1) - 2\Delta v_f\sqrt{I_B\beta_n}\cdot\sqrt{1+\frac{i_{in}(n-1)}{I_B}} - \Delta v_f^2\beta_n \end{aligned} \qquad (3.16)$$

Taylor series expansion is performed to approximate $\sqrt{1+\frac{i_{in}}{I_B}}$, and it leads to:

$$\sqrt{1+\frac{i_{in}}{I_B}} \approx 1+\frac{i_{in}}{2I_B} - \frac{1}{8}\cdot(\frac{i_{in}}{I_B})^2 \qquad (3.17)$$

The output current of 2[nd]-generation memory cell is:

$$i_o(n-\frac{1}{2}) = m_0 - (1+m_1)\cdot i_{in}(n-1) + m_2\cdot i_{in}^2(n-1) \qquad (3.18)$$

where the coefficients m_0, m_1 and m_2 are DC offset, gain and non-linear error terms respectively, and these parameters are given in Table3.2.

Table 3.2 Error coefficients due to clock-feedthrough [37]

	m_0-*DC offset*	m_1-*gain error*	m_2- *non-linear error*
2nd-generation	$-2\Delta v_f\sqrt{I_B\beta_n} - \Delta v_f^2\beta_n$	$\Delta v_f\sqrt{\frac{\beta_n}{I_B}}$	$\frac{\Delta v_f\sqrt{\beta_n I_B}}{4I_B^2}$
S^2I	$-2\Delta v_f\sqrt{I_B\beta_n} + \Delta v_f^2\beta_n$	$\Delta v_f^2\cdot\frac{\beta_n}{I_B}$	$-\Delta v_f^2\cdot\frac{\beta_n}{4I_B^2}$

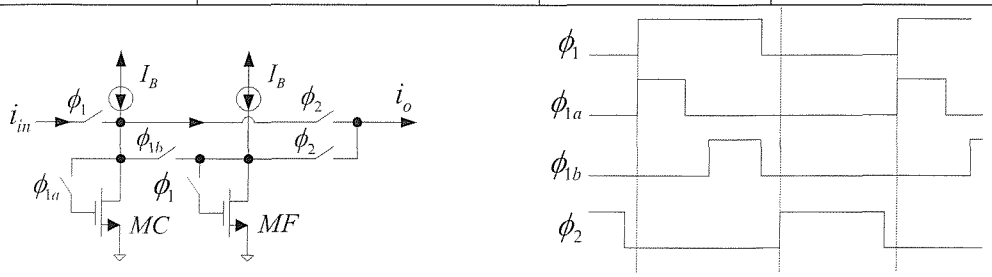


Fig.3.4 S^2I memory cell

Many circuit techniques have been proposed to reduce the clock-feedthrough errors, and the most effective method is S^2I memory cell [41], which cancels the 1st-order clock-feedthrough error without detriment to any other performance, Fig.3.4. The charge cancellation scheme of S^2I is analysed as follows: when switch ϕ_{1a} is off, from the above analysis, the output current of *MC*, i_{oc}, is same as the basic 2nd-generation SI memory cell:

$$i_{oc} = (-2\Delta v_f \cdot \sqrt{I_B \beta_n} - \Delta v_f^2 \cdot \beta_n) - \Delta v_f \cdot \sqrt{\frac{\beta_n}{I_B}} \cdot i_{in}(n-1)$$

$$+ \frac{\Delta v_f \sqrt{I_B \cdot \beta_n}}{4I_B^2} \cdot i_{in}^2(n-1) \qquad (3.19)$$

This current i_{oc} is sent to transistor *MF* during phase ϕ_{1b}. When switch ϕ_1 (ϕ_{1b}) is off, the output current of transistor *MF* is: (assuming the increment of the gate voltage Δv_f in *MF* is same to that of *MC*)

$$\begin{aligned} i_{of} &= I_B - \beta_n \cdot (V_{GS} - V_T + \Delta v_f)^2 \\ &= I_B - \beta_n \cdot (V_{GS} - V_T)^2 - 2\Delta v_f \cdot \beta_n \cdot (V_{GS} - V_T) - \beta_n \cdot \Delta v_f^2 \\ &= -i_{oc} - 2\Delta v_f \cdot \sqrt{I_B \beta_n} \cdot \sqrt{1 + \frac{i_{oc}}{I_B}} - \beta_n \cdot \Delta v_f^2 \end{aligned} \qquad (3.20)$$

When switch ϕ_2 is on, the output current i_o is the sum of output current of *MC* and *MF*:

$$\begin{aligned} i_o(n - \frac{1}{2}) &= [-i_{in}(n-1) + i_{oc}] + i_{of} \\ &= -i_{in}(n-1) - 2\Delta v_f \cdot \sqrt{I_B \beta_n} \cdot \sqrt{1 + \frac{i_{oc}}{I_B}} - \beta_n \cdot \Delta v_f^2 \end{aligned} \qquad (3.21)$$

Taylor series expansion is performed to approximate $\sqrt{1 + \frac{i_{oc}}{I_B}}$, and it leads to:

$$\sqrt{1 + \frac{i_{oc}}{I_B}} \approx 1 + \frac{i_{oc}}{2I_B}, \quad i_{oc} << I_B \qquad (3.22)$$

$$i_o(n-\frac{1}{2}) \approx -i_{in}(n-1) - 2\Delta v_f \cdot \sqrt{I_B \beta_n} \cdot [1+\frac{i_{oc}}{2I_B}] - \beta_n \cdot \Delta v_f^2$$

$$\approx -i_{in}(n-1) - 2\Delta v_f \cdot \sqrt{I_B \beta_n} - \Delta v_f \cdot \sqrt{I_B \beta_n} \cdot \frac{i_{oc}}{I_B} - \beta_n \cdot \Delta v_f^2$$

$$\approx m_o - (1+m_1) \cdot i_{in}(n-1) + m_2 \cdot i_{in}^2(n-1) \qquad (3.23)$$

where the coefficients m_0, m_1 and m_2 are DC offset, gain and non-linear error terms respectively, and also given in Table 3.2.

For a given NMOS memory transistor with $I_B = 10\mu A$, $\beta_n = 221\mu A/V^2$ and considering $\Delta v_f = 10mV$, the following values are result of the 2nd-generation memory cell: -0.962 μA DC current offset, 4.7% gain error. The total harmonic distortion (THD, we only take into account second harmonic here.), which caused by non-linear error term (m_2), is calculated for input signal $i_{in} = \hat{i} \sin \omega_0 t$ and $\hat{i} / I_B = 0.5$:

$$THD = \frac{m_2 \cdot \hat{i}^2/2}{(1+m_1)\cdot \hat{i}} = \frac{\Delta v_f \cdot \sqrt{I_B \beta_n} / 4I_B^2 \cdot \hat{i}^2/2}{(1+\Delta v_f \cdot \sqrt{\frac{\beta_n}{I_B}}) \cdot \hat{i}} = -50.638dB \qquad (3.24)$$

The corresponding values of DC current offset, gain error and THD for S^2I memory cell are: -0.918 μA, 0.22% and –77.19dB, respectively.

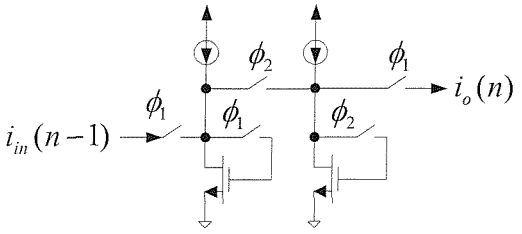


Fig.3.5 (a) 2nd-generation SI delay cell (b) Block diagram of a delay cell

The delay cell using 2nd-generation SI is shown in Fig.3.5(a), and its block diagram representation is given in Fig.3.5(b). This delay cell suffers from clock-feedthrough error due to the switches ϕ_1 and ϕ_2. The effect of the clock-feedthrough on the 2nd–generation delay cell is obtained by cascading the input-output current relationship of each memory cell, and is expressed in Eq.(3.25).

$$i_o(n) = M_0 + (1+M_1) i_{in}(n-1) + M_2 i_{in}^2(n-1) \qquad (3.25)$$

where $M_0 \approx -m_0 m_1$, $M_1 \approx 2m_1 + m_1^2 - 2m_0 m_2$, $M_2 \approx m_2 m_1$

Using the parameters $I_B = 10\mu A$, $\beta_n = 221\mu A/V^2$ and $\Delta v_f = 10mV$, the DC offset, gain error and THD are calculated as 0.045 μA, 9.4%, and -77.98dB, respectively. The corresponding values of DCcurrent offset, gain error and THD for S^2I current delay cell are -2.02 nA, 0.44% and -130.34dB, respectively.

3.3 Models of components in Bruton transformation SI wave filters

The effects of transistor mismatch and clock-feedthrough on the frequency response of SI direct wave filters were studied in [37]. As described in Chapter 2, Bruton transformation SI filters [2,3] are based on new wave components, such as capacitive source and load, FDNR, which are not used by the direct wave design method. This section develops behavioural models for these new wave components using the results outlined in section 3.2. Each non-ideal component model is developed in the form of a difference equation representing the input-output relationship of the wave component including mismatch and clock-feedthrough errors. The modelling process involves the following three main steps:

(i) Identify of the current signal path of each term in the wave component ideal difference equation from physical SI realization.

(ii) Obtain the input-output relationship of each current signal path of the wave component using the mismatch and/or clock-feedthrough error expressions given in Eqs.(3.8), (3.12) and (3.25).

(iii) Sum the contributions of all the component current signal paths to yield the non-ideal model of the wave component in the form of a difference equation.

To illustrate the modelling process, models for the main components of Bruton transformation filters including capacitive source and load, and FDNR are developed. Also, a model for non-ideal series adaptor is developed. Note the presented modelling process is general and can be applied to develop models of wave components implemented using different SI implementation techniques including 1st-generation, 2nd-generation and S^2I. In this section, component models based on 2nd-generation SI delay cells are developed as examples, and the effects of 2nd-generation and S^2I

implementation techniques on the filter frequency response are analysed and compared in section 3.4.

3.3.1 Capacitive source wave component

New wave model in Bruton transformation wave filter, capacitive source wave component, which have been given in Chapter 2, is shown in Fig.3.6. The difference equation of the ideal capacitive source is:

$$B(n) = i_s(n) - i_s(n-1) + A(n-1) \qquad (3.26)$$

where $i_s(n)$, $i_s(n-1)$ and $A(n-1)$ are the input, delayed input and filter feedback signals respectively, and $B(n)$ is the output signal of the capacitive source.

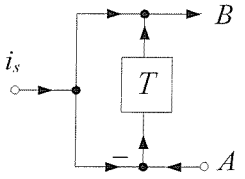


Fig.3.6 Capacitive source wave component

The capacitive source circuit using 2nd-generation SI realization is shown in Fig.3.7. It consists of one delay cell, *T*, and three current mirrors (*M1-M2*), (*M1-M3*), and (*M4-M5*). These current mirrors are marked as *CM1*, *CM2* and *CM3*. Following step.1 of the modelling process, the current signal paths of the ideal difference equation of the capacitive source, Eq.(3.26), are identified and presented in Fig.3.8.

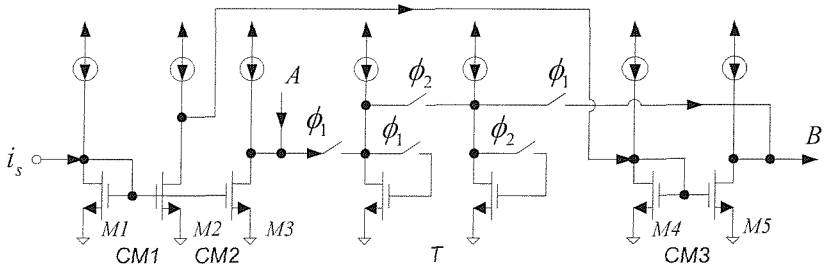


Fig.3.7 Capacitive source circuit using 2nd-generation SI delay cells

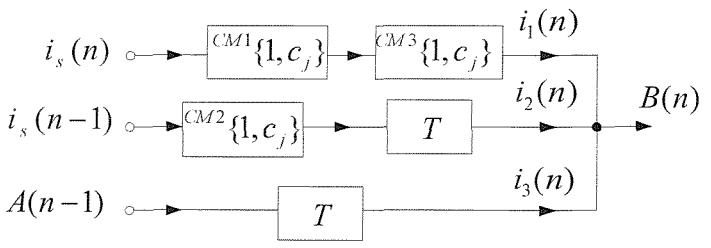


Fig.3.8 Block diagram model of non-ideal capacitive source wave component

The first term of the capacitive source difference equation, the signal current $i_{in}(n)$ flows through the current mirrors *CM1* and *CM3*. Hence it is affected by the mismatch of these two current mirrors as shown in Fig.3.8. The input-output relationship of non-ideal current mirror due to transistor mismatch has three coefficients: DC offset (c_0), gain (c_1) and non-linear coefficient (c_2), Eq.(3.8). Assume the mismatch coefficients of currents mirrors *CM1* and *CM3* are $\{c_{10}, c_{11}, c_{12}\}$ and $\{c_{30}, c_{31}, c_{32}\}$, respectively, and using the input-output relationship of non-ideal cascaded current mirror, Eq.(3.12), the input-output relationship of the first term of the ideal capacitive source difference equation is:

$$i_1(n) = C_0 + C_1 i_s(n) + C_2 i_s^2(n) \qquad (3.27a)$$

where $C_0 = c_{30} + c_{31}c_{10} + c_{32}c_{10}^2$, $C_1 = c_{31}c_{11} + 2c_{11}c_{32}$, $C_2 = c_{31}c_{12} + c_{32}c_{11}^2 + 2c_{10}c_{12}c_{32}$

Note the coefficient c_{ij} indicates the mismatch coefficient c_j (see Table 3.1) in current mirror i (*CMi*). For example, c_{30} denotes DC mismatch coefficient c_0 in current mirror three (*CM3*). Consider the second term of the difference equation of ideal capacitive source, $i_s(n-1)$. Fig.3.7 shows that this current flows through current mirror *CM2* and the delay cell. Hence, it is affected by both mismatch error due to the current mirror and clock-feedthrough error due to the delay element. Assume the mismatch coefficients in current mirror *CM2* are $\{c_{20}, c_{21}, c_{22}\}$, and the input-output relationship of non-ideal delay cell due to clock-feedthrough is given as Eq.(3.25), the input-output relationship of the second term of the ideal capacitive source difference equation is:

$$i_2(n) = M_0 + c_{20} + c_{20}M_1 + (c_{21} + c_{21}M_1)i_s(n-1) + (c_{22} + c_{22}M_1 + c_{21}^2 M_2)i_s^2(n-1) \qquad (3.27b)$$

Finally, the third term of capacitive source difference equation is considered, the feedback signal, $A(n-1)$. Fig.3.7 shows that this signal flows only through the delay cell, and hence it is affected by clock-feedthrough error. Using Eq.(3.25), the input-output relationship of this term is:

$$i_3(n) = M_0 + (1 + M_1)A(n-1) + M_2 A^2(n-1) \qquad (3.27c)$$

Having obtained the input-output relationship of the various terms of Eq.(3.12), the model for the non-ideal capacitive source wave component is obtained by summing up the expressions of Eqs.(3.27a), (3.27b) and (3.27c) to yield:

$$B(n) = i_1(n) + i_2(n) + i_3(n) \qquad (3.27d)$$

3.3.2 FDNR component wave component

The FDNR wave component is shown in Fig.3.9. The difference equation of the ideal FDNR component is:

$$B(n) = 2A(n-1) - B(n-2) \qquad (3.28)$$

where $A(n-1)$ is the delayed input signal and $B(n-2)$ is the delayed output signal.

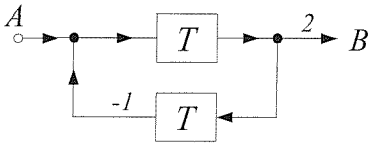


Fig.3.9 FDNR wave component

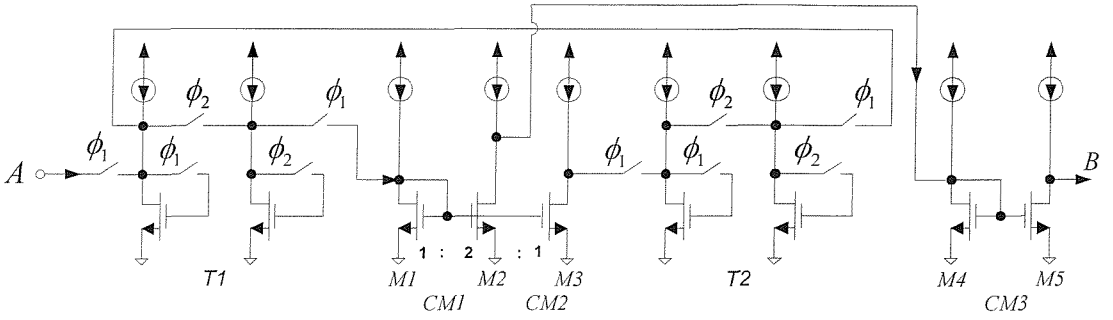


Fig.3.10 FDNR circuit using 2nd-generation SI delay cells

Fig.3.10 shows the FDNR component circuit using 2nd-generation SI circuit. This circuit consists of two delay cells, *T1* and *T2* for generating the necessary delays of Eq.(3.28), and three current mirrors: (*M1-M2*), (*M1-M3*) and (*M4-M5*). These current mirrors are marked as *CM1*, *CM2* and *CM3*, respectively. Note *CM1* is used to provide a gain of 2 for the first term of Eq.(3.28). Examining the circuit in Fig.3.10, the signal paths of the FDNR difference equation are identified and presented in Fig.3.11(a). The input signal, *A* flows through delay cell *T1*, current mirrors *CM1* and *CM3*. Therefore, signal *A* is affected by the clock-feedthrough of *T1* and the mismatch of *CM1* and *CM3*. The term *B(n-2)* of Eq.(3.28) is the output of the FDNR component two clock cycles earlier, and it flows through the entire FDNR component as shown in Fig.3.11(a) as the feedback and feed forward loops.

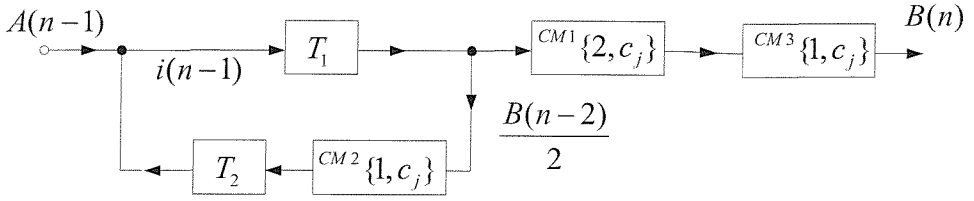


Fig.3.11 (a) Block diagram model of non-ideal FDNR wave component

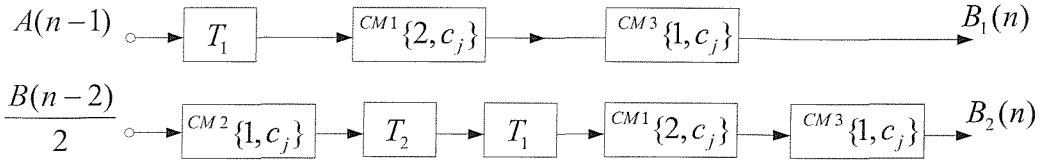


Fig.3.11 (b) Signal paths of the non-ideal FDNR component

To derive the behavioural model of the non-ideal FDNR component, the input-output relationship of each signal path of Fig.3.11(a) need to be obtained. To facilitate this, Fig.3.11(a) is redrawn as Fig.3.11(b) showing more clearly the signal paths of the FDNR component. The signal $B_1(n)$ is the output of the forward path of the FDNR component, and $B_2(n)$ is the combined feedback and feed forward paths signal. Assuming $\{c_{10}, c_{11}, c_{12}\}$, $\{c_{20}, c_{21}, c_{22}\}$ and $\{c_{30}, c_{31}, c_{32}\}$ are the mismatch coefficients in *CM1*, *CM2* and *CM3*, respectively, and the coefficients of the clock-feedthrough in *T1* and *T2* are (M_{10}, M_{11}, M_{12}) and (M_{20}, M_{21}, M_{22}), respectively, the input-output relationship of $B_1(n)$ is:

$$B_1(n) = a_0 + a_1 A(n-1) + a_2 A^2(n-1) \qquad (3.29a)$$

where $a_0 = C_0 + C_1 M_{10} + C_2 M_{10}^2$, $a_1 = C_1 + C_1 M_{11} + 2C_2 M_{10}$, $a_2 = C_1 M_{12} + C_2$

Similarly the input-output relationship of the $B_2(n)$ signal is:

$$B_2(n) = b_0 + b_1 B(n-2) + b_2 B^2(n-2) \qquad (3.29b)$$

where $b_0 = C_0 + M_{10} + (c_{20} + M_{20})(1 + M_{11})$,

$$b_1 = (1 + M_{11})(1 + M_{21})c_{21} + 2(M_{20} + c_{20})(1 + M_{21})c_{21} M_{12}$$

$$b_2 = M_{12} c_{21}^2 (1 + M_{21})^2 + (1 + M_{11})(c_{22}(1 + M_{21}) + c_{21}^2 M_{22})$$

$$+ C_2((1 + M_{11})(1 + M_{21})c_{21})^2 / C_1$$

The difference equation of the non-ideal FDNR component is given by summing up the contributions of the two signals: $B_1(n)$ and $B_2(n)$.

3.3.3 Capacitive load wave component

The capacitive load component is shown in Fig.3.12. The difference equation of the ideal capacitive load is:

$$B(n) = A(n-1) \qquad (3.30a) \qquad i_o(n) = A(n) + B(n) \qquad (3.30b)$$

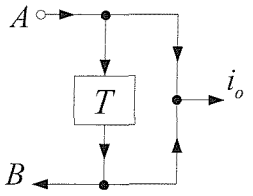


Fig.3.12 Capacitive load wave component

Fig.3.12 shows the capacitive load circuit using 2nd-generation SI delay cells. The circuit consists of one delay cell, *T*, and five current mirrors: *CM1*, *CM2*, *CM3*, *CM4*, and *CM5*.

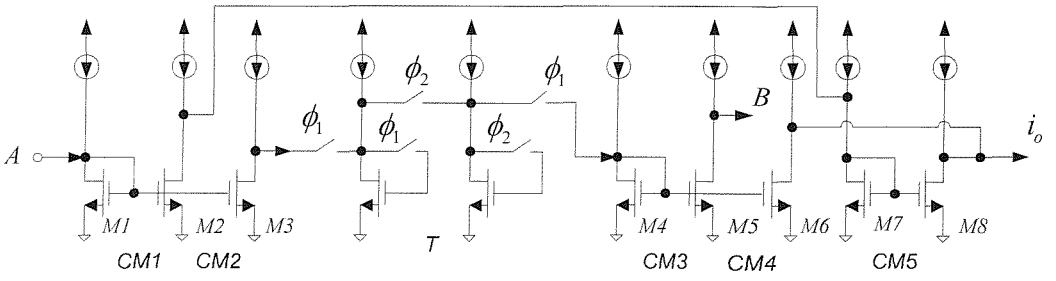


Fig.3.13 Capacitive load circuit using 2nd-generation SI delay cells

Using similar analysis to that used in identifying the current signal paths of the previous wave components, Fig.3.14 shows the block diagram model of the non-ideal capacitive load.

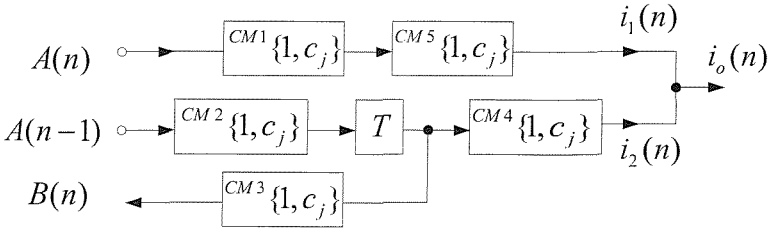


Fig.3.14 Block diagram model of non-ideal capacitive load component

Assume $\{C_0, C_1, C_2\}$ are the mismatch coefficients of the cascade current mirror: *CM1* and *CM5*, the signal $i_1(n)$ is:

$$i_1(n) = C_0 + C_1 A(n) + C_2 A^2(n) \qquad (3.31a)$$

Similarly, assume $\{c_{20}, c_{21}, c_{22}\}$ and $\{c_{40}, c_{41}, c_{42}\}$ are the mismatch coefficients of current mirrors *CM2* and *CM4*, and making use of Eq.(3.25), the signal $i_2(n)$ is:

$$i_2(n) = a_0 + a_1 A(n-1) + a_2 A^2(n-1) \qquad (3.31b)$$

where $a_0 = c_{40} + c_{41}M_0 + c_{41}c_{20}$, $a_1 = c_{41}c_{21} + 2c_{20}c_{21}c_{42} + 2c_{42}c_{21}M_0$,

$a_2 = c_{41}c_{22} + c_{21}^2 c_{42} + 2c_{42}c_{21}^2 M_1$

Clearly the output current, $i_0(n)$, of the capacitive load component is given by the summation of Eq.(3.31a) and (3.31b). Now the input-output relationship of the capacitive load feedback signal $B(n)$ should be obtained. As can be seen from Fig.3.14, this signal path consists of *CM2*, delay cell *T* and *CM3*. Assume $\{c_{30}, c_{31}, c_{32}\}$ is the mismatch coefficients of current mirror *CM3*, the $B(n)$ signal is:

$$B(n) = b_0 + b_1 A(n-1) + b_2 A^2(n-1) \qquad (3.31c)$$

where $b_0 = c_{30} + c_{31}M_0 + c_{31}c_{20}$, $b_1 = c_{31}c_{21} + 2c_{21}c_{20}c_{32} + 2c_{32}c_{21}M_0$,

$b_2 = c_{31}c_{22} + c_{21}^2 c_{32} + 2c_{32}c_{21}^2 M_1$

The model of the non-ideal capacitive load is given by Eqs.(3.31a), (3.31b) and (3.31c).

3.3.4 Wave adaptors

So far, behavioural models for non-ideal (mismatch and clock-feedthrough errors) wave components introduced by Bruton transformation have been developed. To complete the modelling of Bruton transformation wave filters' non-ideal characteristics, wave adaptors need to be considered. There are two types of wave adaptors, series and parallel, which are used to connect the various elements of wave filters. Wave adaptors affect the performance of direct wave filters as reported in [37], where model for non-ideal *3-port* parallel wave adaptor was proposed. It can be seen from Chapter 2 that only *2-port* series and *3-port* parallel wave adaptors are employed in Bruton transformation wave filters. Therefore, the non-ideal performance of *2-port* series wave adaptor is developed in this section. Both wave adaptors models will be used when analysing the non-ideal frequency response of Bruton transformation SI wave filters. Fig.3.15 shows the symbol of *2-port* series wave adaptor, where *A* denotes the incident variable and *B* denotes the reflected variable.

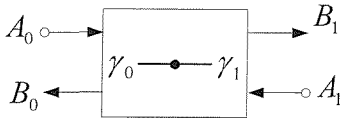


Fig.3.15 *2-port* series adaptor symbol

The input-output relationship of *2-port* serial wave adaptor in matrix form is:

$$\begin{bmatrix} B_1(n) \\ B_0(n) \end{bmatrix} = \begin{bmatrix} 1-\gamma_1 & -\gamma_1 \\ -\gamma_0 & 1-\gamma_0 \end{bmatrix} \begin{bmatrix} A_1(n) \\ A_0(n) \end{bmatrix} \qquad (3.32a)$$

where γ_0 and γ_1 are wave adaptor coefficients.

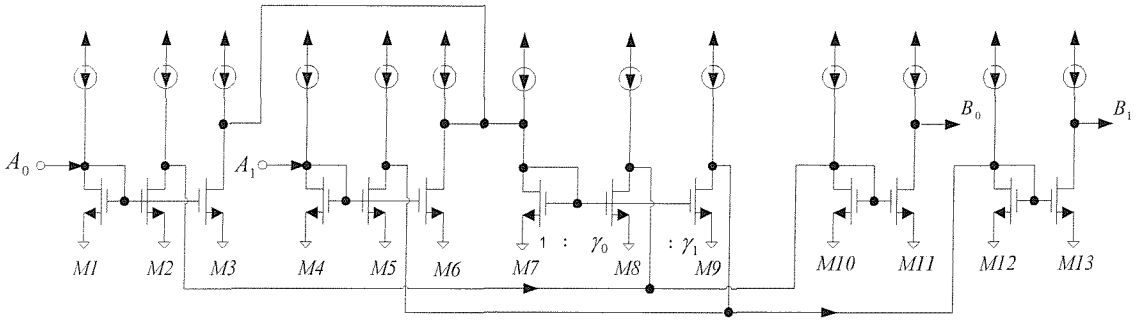


Fig.3.16 *2-port* series wave adaptor circuit [28]

The circuit of *2-port* series adaptor is shown in Fig.3.16. The SI circuit has current mirrors and no delay cell therefore the adaptor operation is only affected by mismatch errors. To obtain the input-output relationship of the non-ideal adaptor, consider the first entry of the matrix in Eq.3.32(a):

$$B_1(n) = A_1(n) - \gamma_1 A_1(n) - \gamma_1 A_0(n) \qquad (3.32b)$$

With reference to Fig.3.16, it can be seen that the current path of the first term in Eq.(3.32b) has two current mirrors: (*M4-M5*) and (*M12-M13*), and the second term current path has three current mirrors: (*M4-M6*), (*M7-M9*) and (*M12-M13*). The current path of the third term has three current mirrors: (*M1-M3*), (*M7-M9*) and (*M12-M13*). Similarly, the current paths of $B_0(n)$ are the same as that of $B_1(n)$. The general block diagram model of non-ideal *2-port* series adaptor due to mismatch is shown in Fig.3.17, where Fig.3.17(a) shows the current signal paths of the main diagonal elements of Eq.(3.32a), and Fig.3.17(b) shows the signal paths of the non-diagonal elements of Eq.(3.32a).

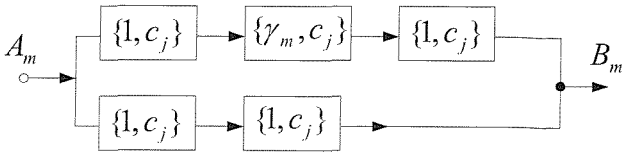


Fig.3.17 (a) Signal paths of main diagonal elements in input-output relationship of *2-port* series wave adaptor

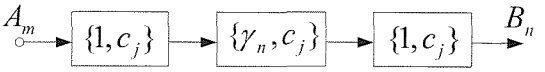


Fig.3.17 (b) Signal paths of non-diagonal elements in input-output relationship of *2-port* series wave adaptor

Assuming $\{C_{t0}, C_{t1}, C_{t2}, t = 0,1,2,3,4,5\}$ are mismatch coefficients of the cascaded current mirrors: (*M1-M2*, *M10-M11*), (*M1-M3*, *M7-M8*), (*M4-M6*, *M7-M8*), (*M4-M5*, *M12-M13*), (*M4-M6*, *M7-M9*) and (*M1-M3*, *M7-M9*), respectively. Also, assuming $\{c_{00}, c_{01}, c_{02}\}, \{c_{10}, c_{11}, c_{12}\}$ are mismatch coefficients of current mirrors: (*M10-M11*) and (*M7-M9*), respectively. From Fig.3.17, it can be shown that the input-output relationship of non-ideal *2-port* serial wave adaptor is:

$$B_0 = (C_{00} + C_{01}A_0 + C_{02}A_0^2) + c_{00} + c_{01}((C_{10} + C_{11}A_0 + C_{12}A_0^2) + (C_{20} + C_{21}A_1 + C_{22}A_1^2)) + c_{02}((C_{10} + C_{11}A_0 + C_{12}A_0^2) + (C_{20} + C_{21}A_1 + C_{22}A_1^2))^2 \quad (3.32c)$$

$$B_1 = (C_{30} + C_{31}A_1 + C_{32}A_1^2) + c_{10} + c_{11}((C_{40} + C_{41}A_1 + C_{42}A_1^2) + (C_{51} + C_{51}A_0 + C_{52}A_0^2)) + c_{12}((C_{40} + C_{41}A_1 + C_{42}A_1^2) + (C_{51} + C_{51}A_0 + C_{52}A_0^2))^2 \quad (3.32d)$$

3.4 Simulation results

In this section, the effects of mismatch in current mirrors and clock-feedthrough errors in delay cells on the frequency response of Bruton transformation SI wave filters will be investigated.

3.4.1 Computer program on Bruton transformation wave filters

To facilitate the investigation of non-ideal performance of Bruton transformation wave filters, a computer program was developed and interfaced with *MATLAB* [89]. The flow chart is shown in Fig.3.18, and its detailed *MATLAB* program is given in Appendix A.

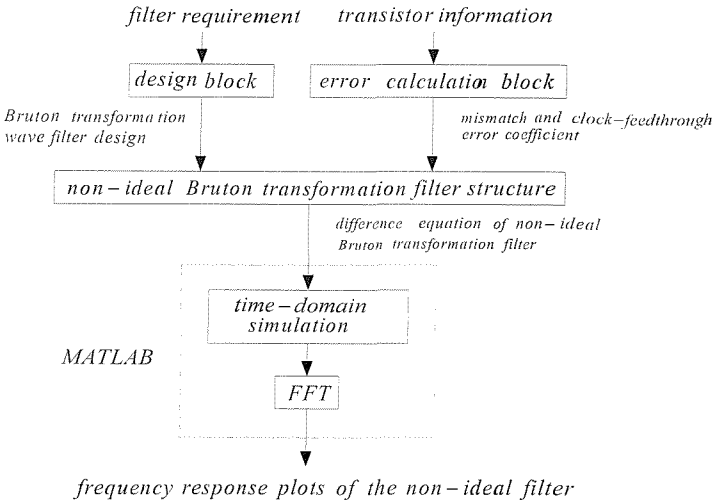


Fig.3.18 Flow chart for analysing non-ideal performance of Bruton transformation SI wave filter

The inputs to the design and error calculation blocks are filter requirements and transistor information, respectively. The filter requirements are filter type (*LP*, *HP*, *BP*, *BS*), frequency specification (cutoff frequency, passband ripple, stopband edge, and stopband attenuation). The filters are designed according to the Bruton transformation wave design method outlined in [2,3]. The output of the design block is a Bruton transformation wave filter with wave adaptors coefficients that meets the required specification. The inputs to error calculation block are: K_β, K_{vt} (technology-dependent parameters), W/L (aspect ratios), G (nominal gain), $(V_{GS}-V_T)$, I_B (bias current), β_n (current factor of NMOS transistor), Δv_f (incremental increase in gate voltage). The output of the error calculation block is values of the mismatch and clock-feedthrough coefficients given in Tables 3.1 and 3.2. The simulation results presented in this section were obtained using the following transistor information [37]: K_β=0.02 μm, K_{vt}=20 $mV.\mu m$, W/L=60 μm/10 μm, G=*1*(current mirror gain), $(V_{GS}-V_T)$=0.6 V, I_B=10 μA, β_n=221 $\mu A/V^2$ and different values of Δv_f as shown later when presenting the simulation results. Considering the random origin of matching errors, N times Monte Carlo simulations are used to simulate filter performance, which include mismatch effect. The outputs of the design and error calculation blocks are used with the behavioural models developed in section 3.3 to derive the difference equation of the non-ideal Bruton transformation wave filter in the presence of mismatch and clock-

feedthrough errors. Using *MATLAB*, time domain simulation is carried out on the non-ideal filter difference equation, from which frequency response plots of the filter are obtained following FFT analysis.

3.4.2 Simulation on 3rd-order lowpass Bruton transformation SI wave filter

To examine the effect of mismatch and clock-feedthrough errors on SI wave Bruton transformation filter, two examples are considered. The first example is 3rd-order elliptic lowpass filter, Fig.3.19.

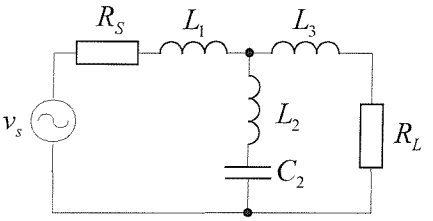


Fig.3.19 (a) 3rd-order elliptic lowpass LC filter

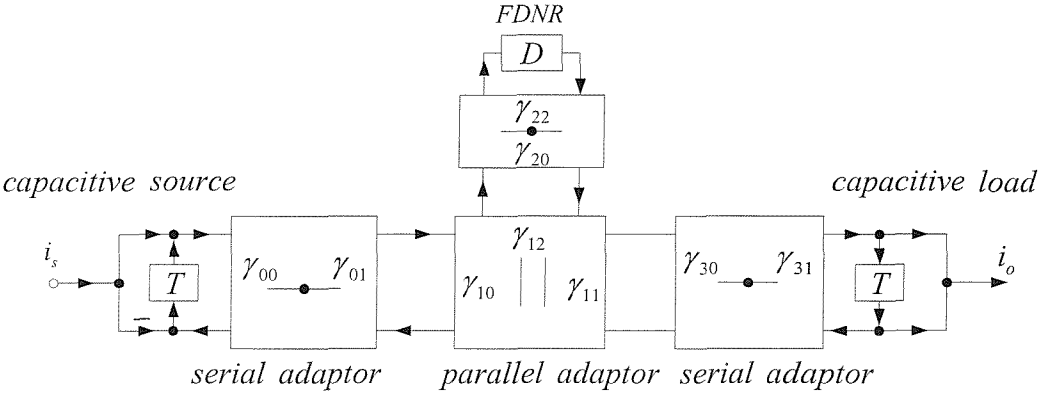


Fig.3.19 (b) 3rd-order lowpass Bruton transformation wave SI elliptic filter

The normalized lowpass filter specifications are: passband ripple ε=0.177dB, passband edge f_p=0.1, stopband edge f_s=0.229, stopband attenuation >36dB. The wave adaptor coefficients are:

γ_{00}=0.3282, γ_{01}=0.5, γ_{10}=0.1718, γ_{11}=0.5, γ_{12}=1.3282,

γ_{20}=0.5, γ_{22}=0.7527, γ_{30}=0.2055 γ_{31}=0.3927

Fig.3.20(a) shows the filter magnitude response when the filter suffers from clock-feedthrough error, assuming different values of Δv_f = 10mV, 4mV, 2mV, 0mv, -2mV, and –4mV. It shows that the filter passband ripple and stopband (notch position) responses are affected by this error. For example, the notch depth has reduced from

approximately 70dB in the ideal case to about 40dB when $\Delta v_f = 10\text{mV}$. To examine the effect of clock-feedthrough error on the filter passband in detail, Fig.3.20(b) shows the filter passband ripple is increased from 0.177dB in the ideal case to around 2.5dB when $\Delta v_f = 10\text{mV}$. A number of techniques, such as S^2I technique [41] have been proposed to reduce the effect of clock-feedthrough on SI circuits. Fig.3.21(a) shows the frequency response of the same filter with clock-feedthrough error when the filter is designed using S^2I delay cells. Clearly this shows that the filter performs better when S^2I delay cells are employed. Fig.3.21(b) shows the filter passband response in more details.

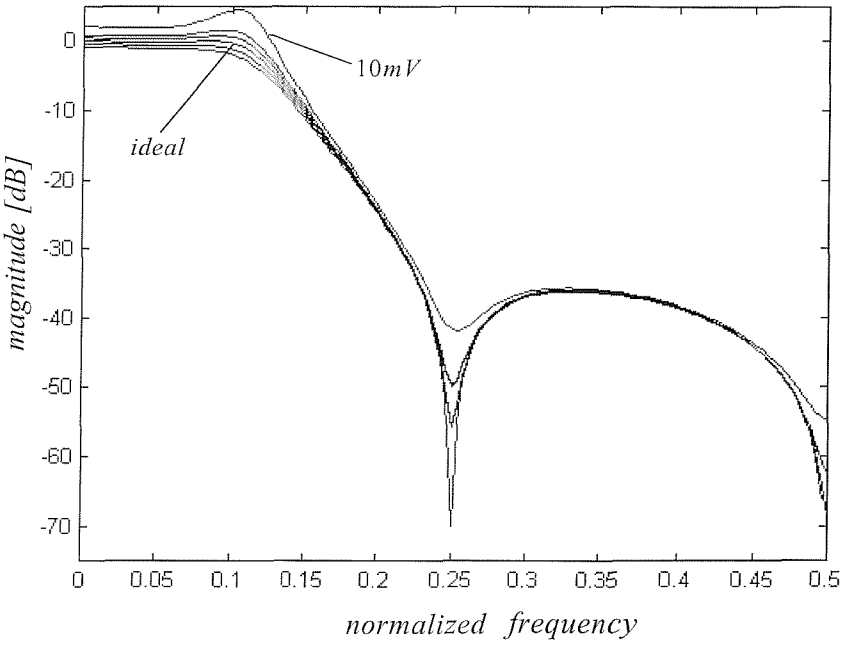


Fig.3.20 (a) Frequency response of 3rd-order lowpass Bruton transformation wave filter in the presence of clock-feedthrough error using 2nd-generation delay cells.

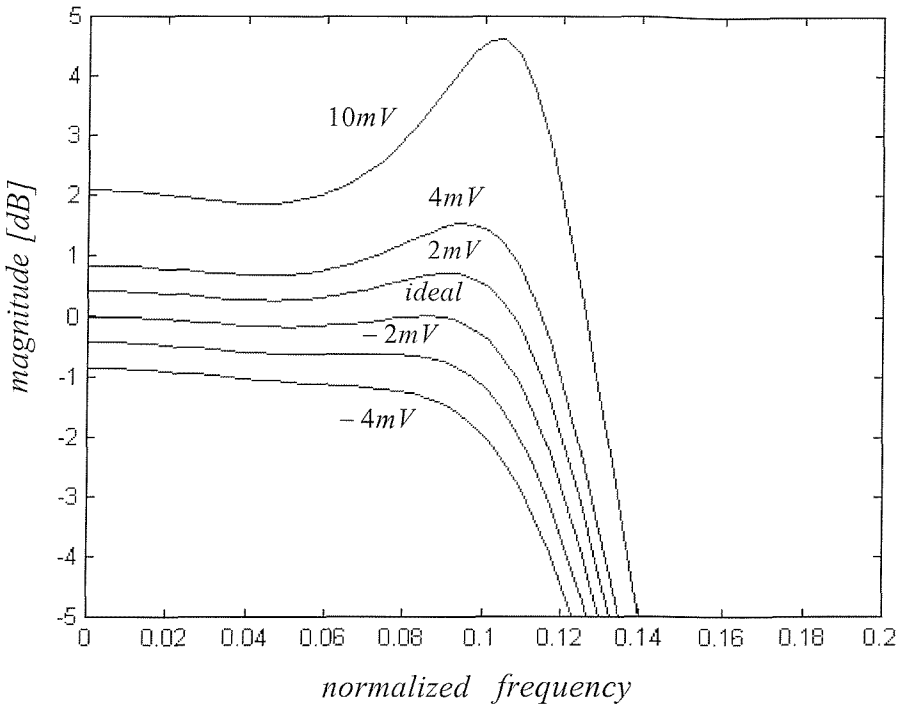


Fig.3.20 (b) Passband ripple response of filter in Fig.3.20(a)

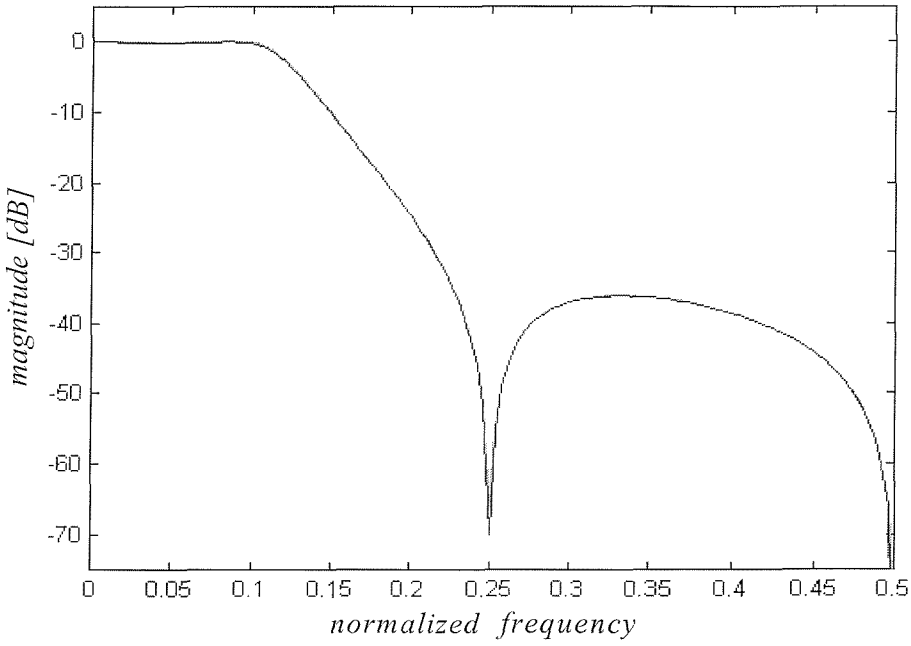


Fig.3.21 (a) Frequency response of 3rd-order lowpass Bruton transformation wave filter in the presence of clock-feedthrough error using S^2I delay cells

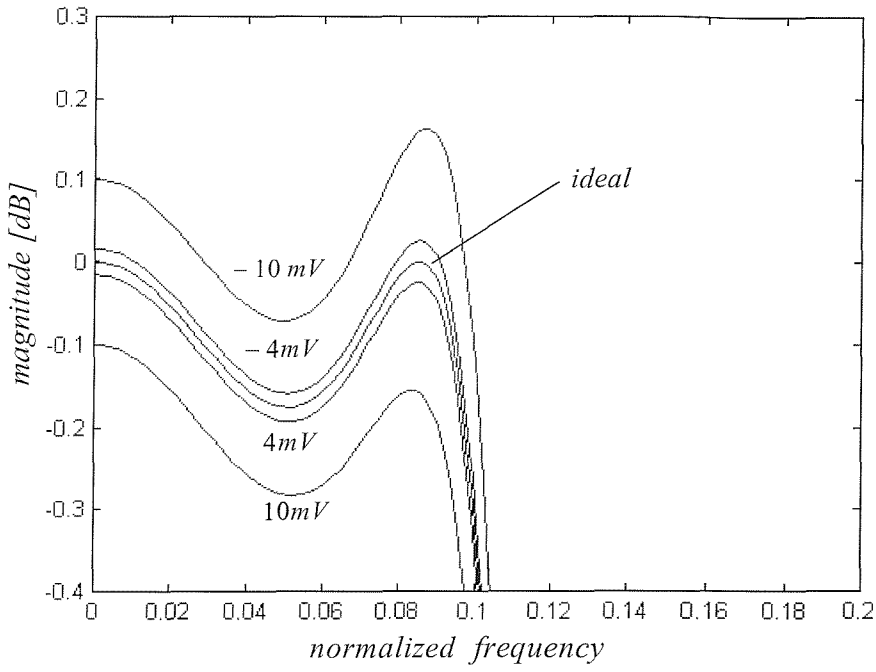


Fig.3.21 (b) Passband ripple response of filter in Fig.3.21(a)

So far, only the clock-feedthrough error effect on the filter performance has been considered. Now, the effects of mismatch error combined with clock-feedthrough are investigated. Table3.3 gives a summary of the filter performance parameters (passband ripple (ε), passband frequency (f_p), notch frequency (f_1), and DC gain *H(0)*), in the presence of only mismatch errors (i.e. when $\Delta v_f = 0$mV), and when the filter has both mismatch and clock-feedthrough errors (i.e. when $\Delta v_f = 2$mV, and 4mV) for 2nd-generation and S^2I delay cells. As can be seen from columns 2 and 3, the filter performance parameters are little affected by the mismatch error. For example the passband ripple is 0.1773dB in the case of SI implementation compared to the ideal passband ripple of 0.177dB. However, the error in filter performance parameters increases when mismatch and clock-feedthrough are combined and gets worse as Δv_f increases. For example, the passband ripple is 0.8484dB when $\Delta v_f = 4$mV. Table 3.3 shows as expected that S^2I delay cells based filters are less affected than 2nd-generation SI based filters by mismatch and clock-feedthrough errors.

Table 3.3 Summary of 3rd-order lowpass filter parameters performance in the presence of mismatch and clock-feedthrough errors.

Cell	*2nd*	S^2I	*2nd*	S^2I	*2nd*	S^2I
$\Delta v_f(mV)$	0	0	2	2	4	4
$\varepsilon[dB]$	0.1773	0.1774	0.4564	0.1793	0.8484	0.1858
ε *std%*	0.39	0.43	0.71	0.45	0.88	0.44
ε *error%*	0.19	0.25	157.85	1.32	379.3	4.95
f_p	0.0965	0.0965	0.1043	0.0966	0.1094	0.09675
f_p *std%*	0.045	0.0552	0.053	0.05	0.061	0.0472
f_p *error%*	0.4128	0.4128	7.637	0.31	12.9	0.155
f_1	0.25	0.251	0.251	0.251	0.252	0.251
f_1 *std%*	0.065	0.07	0.0478	0.052	0.12	0.078
f_1 *error%*	0.24	0.159	0.159	0.159	0.555	0.159
H(0) dB	0.0042	0.0036	0.431	-0.0069	0.8514	0.0158

std% represents the standard deviation and *error%* represents the difference between simulation results and required specification.

3.4.3 Simulation on 5th-order highpass Bruton transformation SI wave filter

The second example is 5th-order highpass elliptic filter, Fig.3.22. The normalized highpass filter specifications are: passband ripple ε=0.177dB, passband edge f_p=0.18, stopband edge f_s=0.1, stopband attenuation >60dB. The wave adaptor coefficients are:

γ_{00}=0.842, γ_{01}=0.5, γ_{10}=1.03, γ_{11}=0.5, γ_{12}=0.47, γ_{20}=1.928, γ_{50}=1.834,

γ_{30}=0.752, γ_{31}=0.5, γ_{40}=0.980, γ_{41}=0.5, γ_{42}=0.519, γ_{60}=0.965, γ_{61}=0.606

It has been shown that the filter frequency response is affected by mismatch and clock-feedthrough errors as shown in Fig.3.23(a) and (b). The filter frequency response improves when S^2I delay cells are used as shown in Fig.3.24(a) and (b). Table 3.4 gives a summary of the filter performance parameters (passband ripple (ε), passband frequency (f_p), notch frequency (f_1, f_2), 3dB frequency (*f(-3dB)*), magnitude in passband $|H(j\omega)|_p$ and magnitude in stopband $|H(j\omega)|_s$) in the presence of only

mismatch errors and when the filter has both mismatch and clock-feedthrough errors for 2[nd]-generation and S^2I delay cells. Again the filter frequency response is less affected by these two sources of errors when S^2I delay cells are used.

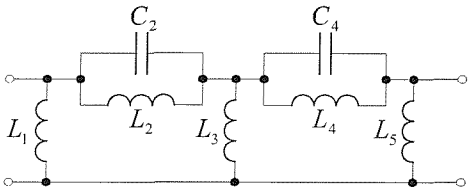


Fig.3.22 (a) 5[th]-order elliptic highpass LC filter

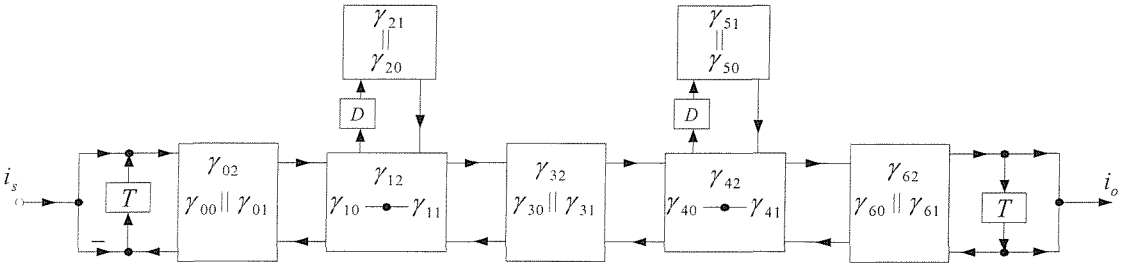


Fig.3.22 (b) 5[th]-order highpass Bruton transformation wave SI elliptic filter

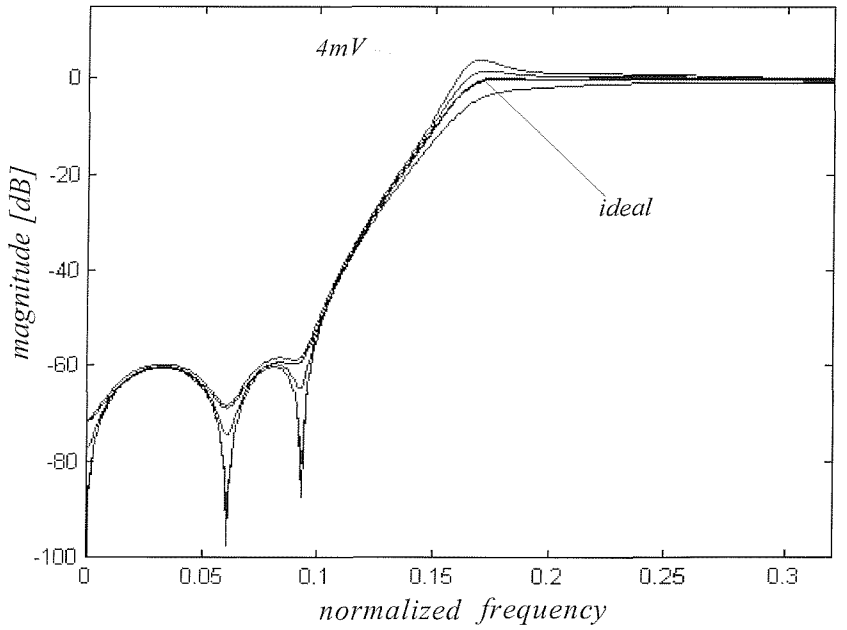


Fig.3.23 (a) Frequency response of the 5[th]-order highpass Bruton transformation wave filter in the presence of the clock-feedthrough error in 2[nd]-generation delay cells.

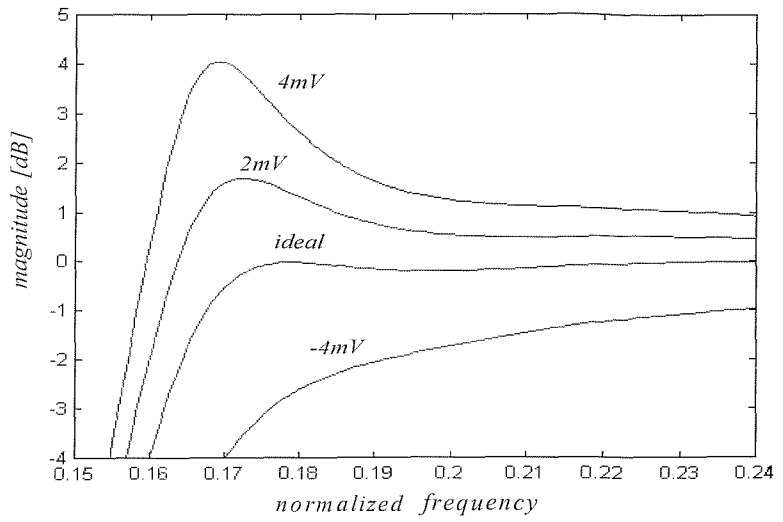


Fig.3.23 (b) Passband ripple response of filter in Fig.3.23 (a)

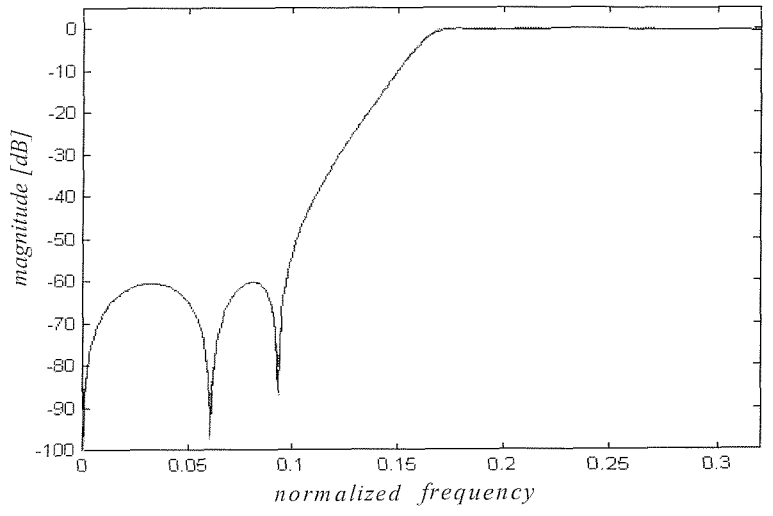


Fig.3.24 (a) Simulated frequency response of 5[th]-order highpass Bruton transformation wave filter in the presence of clock-feedthrough error in S^2I delay cells

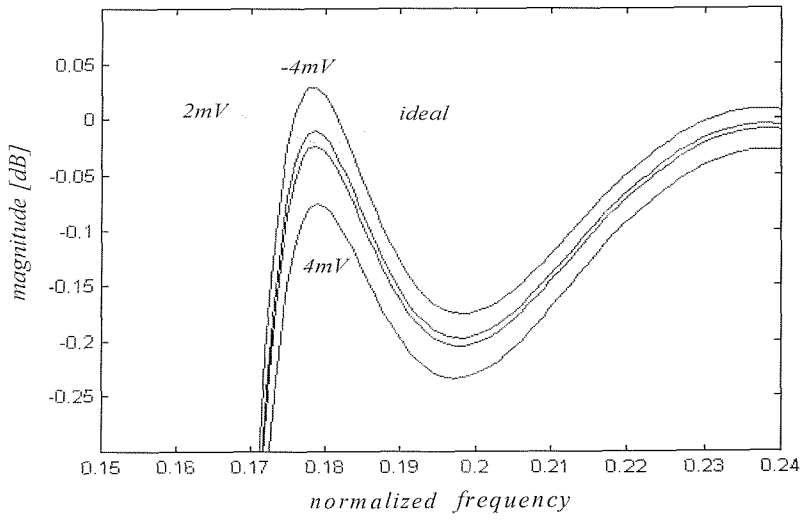


Fig.3.24 (b) Passband ripple response of filter in Fig.3.24 (a)

Table 3.4 Summary of the 5th-order highpass filter parameters performance in the presense of mismatch and clock feedthrough errors.

Cell	2^{nd}	S^2I	2^{nd}	S^2I	2^{nd}	S^2I
$\Delta v_f(mV)$	0	0	2	2	4	4
$\varepsilon[dB]$	0.1803	0.1779	1.1923	0.1856	4.0779	0.207
$\varepsilon\, std\%$	1.35	1.39	2.71	1.11	5.56	1.61
$\varepsilon\, error\%$	1.86	0.48	573.63	4.87	2204.3	16.95
f_p	0.1784	0.1786	0.1723	0.1786	0.1689	0.1781
f_p $std\%$	0.0714	0.0612	0.0617	0.0574	0.0478	0.0731
f_p $error\%$	0.0896	0.0224	3.51	0.0224	5.41	0.257
$f(-3dB)$	0.1619	0.1619	0.1583	0.1619	0.1557	0.1616
$f(-3dB)$ $std\%$	0.047	0.04877	0.0569	0.0581	0.0481	0.0488
f_1	0.0607	0.0608	0.0614	0.0607	0.0604	0.0602
f_1 $std\%$	0.17	0.17	0.14	0.16	0.16	0.19
$f_1\, error\%$	0.33	0.496	1.49	0.33	0.165	0.5
f_2	0.0932	0.0932	0.0924	0.0929	0.0901	0.0927
$f_2\, std\%$	0.092	0.0962	0.0952	0.11	0.11	0.12
$f_2\, error\%$	0.43	0.43	0.43	0.11	2.9	0.11
$\lvert H(j\omega)\rvert_p\, dB$	-0.0312	-0.0261	0.3937	-0.0377	0.8195	-0.014
$\lvert H(j\omega)\rvert_s\, dB$	-60.79	-61.53	-58.04	-62.887	-54.52	-61.177

std% represents the standard deviation and *error%* represents the difference between simulation results and required specification.

3.4.4 Comparison of non-ideal performance between direct and Bruton transformation SI wave filters

The two examples show the effectiveness of the behavioural models developed in studying the influence of different SI implementation techniques on the filters frequency response. To comment on how the non-ideal performance of Bruton

transformation SI wave filters compared with that of direct wave filters, these two filter examples were also designed using the direct wave method [1,25] and simulated. It has been shown that Bruton transformation wave filters and direct wave filters have similar non-ideal frequency response in the presence of mismatch and clock-feedthrough errors. To be able to compare the results with previous work in [37], non-ideal frequency response of 3rd-order lowpass Chebyschev wave filter is simulated with different values of clock-feedthrough voltages. Fig.3.25 shows a comparison between the non-ideal frequency response of the filter in [37] and that of an equivalent Bruton transformation wave filter when there is a clock-feedthrough error, for instance $\Delta v_f = 5\text{mV}$. As can be seen, both filters exhibit similar performance, despite the Bruton transformation wave filter having a smaller transistor count.

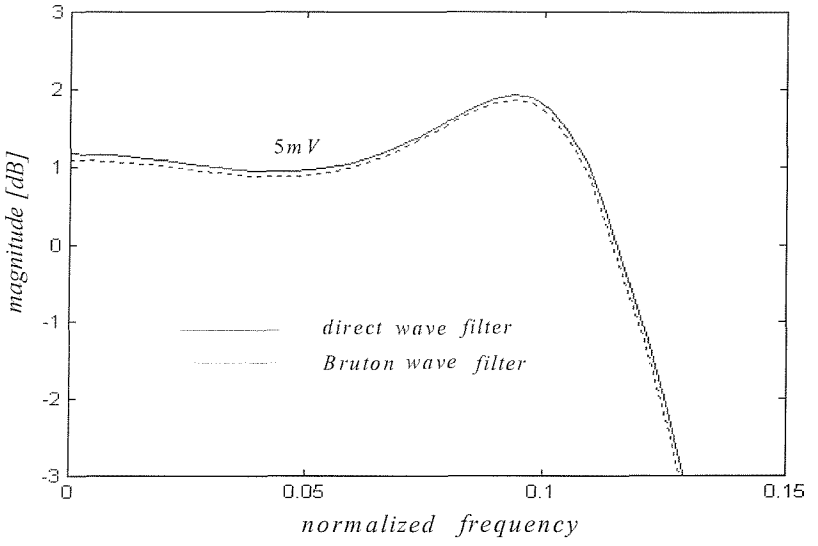


Fig.3.25 Non-ideal frequency response of 3rd-order Chebyshev lowpass filter designed using direct wave method [1,25] and Bruton transformation wave method [2]

3.5 Speed limitation of Bruton transformation SI wave filters

According to [1,36], wave adaptors impose the main speed limitation of SI wave filter. The bandwidth of wave adaptors is approximately studied using the small signal equivalent circuit. For the case of the lowpass Bruton transformation SI wave filter, following the analysis in [1,36], *3-port* parallel wave adaptor imposes main speed limitation of this filter. It shows in Fig.3.26 that for each input signal A_i, the path through two current mirrors is the most restrictive path in the *3-port* parallel wave adaptor.

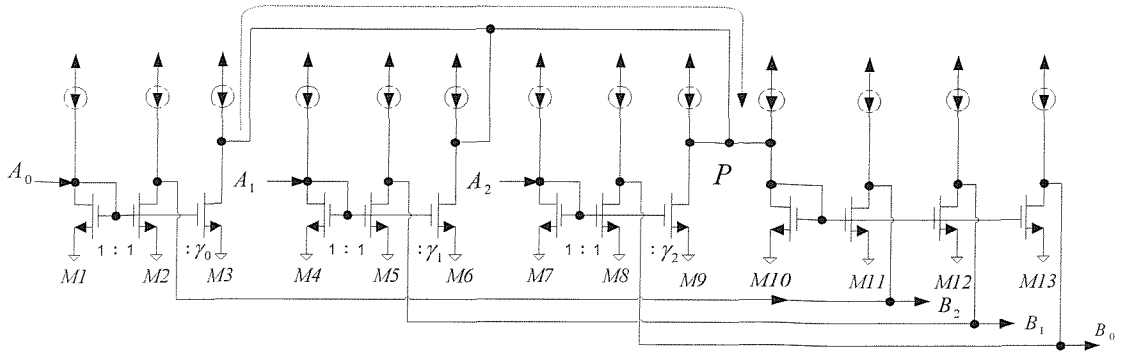


Fig.3.26 *3-port* parallel wave adaptor with most restrictive path identified

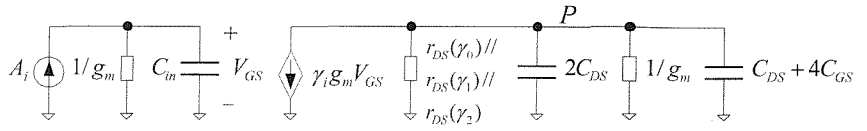


Fig.3.27 Small signal model of the restrictive path in *3-port* parallel wave adaptor

The small signal model of the most restrictive path is given in Fig.3.27, where $r_{DS}(\gamma_i)$ is output resistance of current mirror with wave adaptor coefficient γ_i. Since the combined output resistance of current mirror $r_{DS}(\gamma_0)//r_{DS}(\gamma_1)//r_{DS}(\gamma_2) >> 1/g_m$,

$$r_{DS}(\gamma_0)//r_{DS}(\gamma_1)//r_{DS}(\gamma_2)//(1/g_m) \approx 1/g_m \qquad (3.33)$$

The dominant pole is node *P*, and its time constant τ is:

$$\tau \approx (3C_{DS} + 4C_{GS})/g_m \qquad (3.34)$$

The bandwidth limitation of *3-port* parallel wave adaptor is:

$$f_{\max} \approx g_m/[2\pi \cdot (3C_{DS} + 4C_{GS})] \qquad (3.35)$$

Using the transistor information given in section 3.4: $g_m = 264\,\mu A/V$, $C_{DS} = 0.24pF$, $C_{GS} = 0.6pF$, the speed limitation of lowpass Bruton transformation SI wave filter is 13.47MHz.

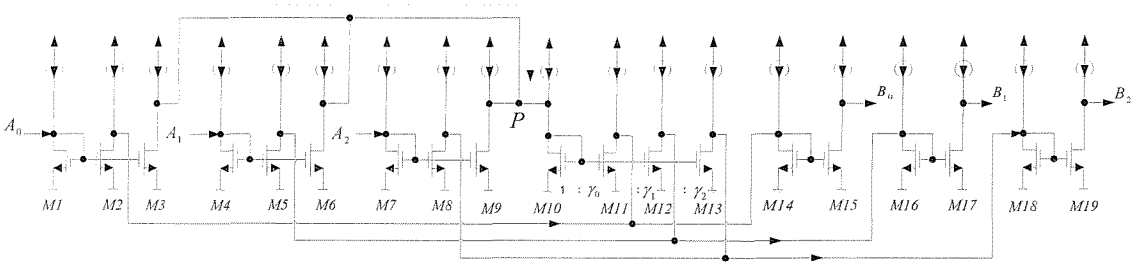


Fig.3.28 *3-port* series wave adaptor with most restrictive path identified

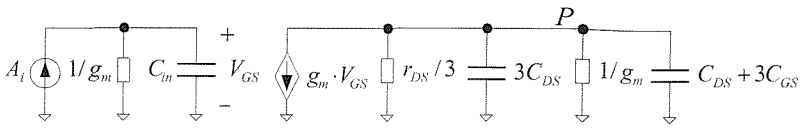


Fig.3.29 Small signal model of the restrictive path in *3-port* series wave adaptor

For the case of highpass Bruton transformation SI wave filter, *3-port* series wave adaptor imposes main speed limitation of this filter. Fig.3.28 shows the most restrictive path in *3-port* series wave adaptor, and its small signal model is shown in Fig.3.29. Since the combined output resistance of current mirror $r_{DS}/3$ is much larger than $1/g_m$,

$$(r_{DS}/3)//(1/g_m) \approx 1/g_m \tag{3.36}$$

The dominant pole is node *P*, and its time constant τ is:

$$\tau \approx (4C_{DS} + 3C_{GS})/g_m \tag{3.37}$$

The bandwidth limitation of *3-port* series wave adaptor:

$$f_{\max} \approx g_m/[2\pi \cdot (4C_{DS} + 3C_{GS})] \tag{3.38}$$

Using the transistor information given in section 3.4: $g_m = 264\,\mu A/V$, $C_{DS} = 0.24pF$, $C_{GS} = 0.6pF$, the speed limitation of highpass Bruton transformation SI wave filter is 15.2MHz.

3.6 Concluding remarks

This chapter has analysed and modelled the non-ideal performance of Bruton transformation SI wave filters in the presence of mismatch in current mirror and clock-feedthrough errors in delay cell. Non-ideal behavioural models of the filters' main components have been derived from analysing the physical realization of the Bruton transformation wave components. The developed models have been integrated with *MATLAB* and used to examine the effect of such errors on the filters frequency response. It has been shown that mismatch in current mirrors and clock-feedthrough in SI delay cells degrades the frequency response of the filters, and the level of degradation depends on the type of SI design technique. It has been found that filters designed using S^2I delay cells are little affected by theses errors and appears to be a practical choice when considering the transistor-level circuits design of Bruton transformation SI wave filters.

Chapter 4

SI Group Delay Wave Equalizers

4.1 Introduction

Video and high-frequency communication applications often call for filters with high attenuation in the stopband and linear phase or flat group delay (derivation of phase with respect to frequency) response in passband. Chapter 3 has shown that elliptic Bruton transformation SI wave filters can be used to design sharp filters with low component count. However, elliptic filters have non-linear phase or non-flat group delay response, which results in excessive overshoot in the filter's step response. An approach to improve the filter's step response (i.e. reduce the overshoot) is to cascade group delay equalizer (allpass filter) with the filter, where the equalizer's function is to compensate the filter's group delay without changing its magnitude characteristics. Although much research has been carried out on SI filters design [10-30], very little work has been reported on the important area of group delay equalization using SI technology. This chapter provides a new efficient design methodology for designing SI group delay equalizers. Section 4.2 introduces a new group delay equalizer architecture, which is based on wave synthesis technique. Section 4.3 describes the complete design process of SI wave group delay equalizer. The detailed design and simulation example of 7^{th}-order SI group delay equalizer is given in section 4.4, and the comparison among different order SI group delay equalizers is also included.

4.2 New group delay equalizer architecture

Allpass filters are defined as a system that has a constant magnitude response for all frequencies, that is:

$$|H(\omega)| = 1, \quad 0 \le \omega \le \pi \tag{4.1}$$

The genearal z-domain transfer function for describing allpass system is:

$$H(z) = \pm\frac{a_N + a_{N-1}z^{-1} + \cdots + a_1 z^{-(N-1)} + z^{-N}}{1 + a_1 z^{-1} + \cdots + a_{N-1}z^{-(N-1)} + a_N z^{-N}} = \pm\frac{\sum_{k=0}^{N} a_k z^{k-N}}{\sum_{k=0}^{N} a_k z^{-k}}, \quad a_0 = 1 \qquad (4.2)$$

(+ sign for $N=2m$, - sign for $N=2m+1$, and all the filter coefficients $\{a_k\}$ are real.)

If we define the polynomial $A(z)$ as:

$$A(z) = \sum_{k=0}^{N} a_k z^{N-k}, \quad a_0 = 1 \qquad (4.3)$$

then Eq.(4.2) can be expressed as: $$H(z) = z^N \frac{A(z^{-1})}{A(z)} \qquad (4.4)$$

Since $|H(\omega)|^2 = H(z)H(z^{-1})\big|_{z=e^{j\omega}} = 1$, the circuit given by Eq.(4.2) is verified to be allpass system. It is primarily to provide phase characteristics and any interference with an existing magnitude response should be avoided. However, in practical realizations, the magnitude response will inevitably be influenced by component variations. It is important therefore to use circuits with low magnitude sensitivity characteristics. A ladder-based design method for allpass digital filter has recently been proposed [55]. The allpass transfer function Eq.(4.4) can be rearranged as [56-58]:

$$H(z) = 1 - \frac{A(z) - z^N A(z^{-1})}{A(z)} = 1 - \frac{2}{1 + \dfrac{A(z) + z^N A(z^{-1})}{A(z) - z^N A(z^{-1})}} = 1 - \frac{2}{1 + Y(z)} \qquad (4.5)$$

where $Y(z) = \dfrac{A(z) + z^N A(z^{-1})}{A(z) - z^N A(z^{-1})}$, and we will show $Y(z)$ can be synthesized as the reactive driving point admittance of passive network.

In this way, the allpass transfer function is decomposed into two terms: a constant and a function realizable as the reactive driving point admittance of passive network. The magnitude response of allpass filter is:

$$|H(z)|_{z=e^{j\omega}} = \left|\frac{Y(z)-1}{Y(z)+1}\right|_{z=e^{j\omega}} = \left|\frac{Y(j\omega)-1}{Y(j\omega)+1}\right| \equiv 1 \qquad (4.6)$$

Since $Y(j\omega)$ is pure imaginary term, the magnitude response of ladder-based allpass filter has low sensitivity to the component variations in $Y(j\omega)$. Numerous implementations of Eq.(4.5) have been reported, including OTA-C [30] and SC realization [55]. In this chapter, SI implementation is proposed as shown in Fig.4.1.

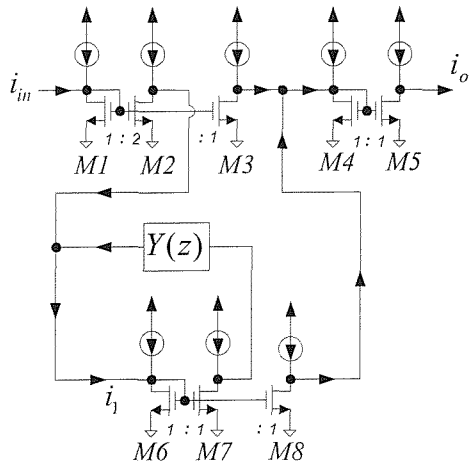


Fig.4.1 SI wave allpass circuit architecture

The circuit operates as follows: input current i_{in} is inverted and multiplied by a gain of 2 through current mirror *(M1~M2)*. This amplified current is summed with output of block *Y(z)* and fed into the current mirror *M6*, *M7* and *M8*. One inverted current copy of this current mirror is sent to the input of block *Y(z)*, whose output is fedback into current mirror *M6*, *M7* and *M8*. Another inverted current copy is summed with the inverted current copy of i_{in} and sent to current mirror (*M4~M5*), whose output is current i_o. The architecture operation can be summarized by the following equations:

$$-2i_{in} - i_1 Y(z) = i_1 \tag{4.7}$$

From which, we obtain:
$$i_1 = -2i_{in}/(1+Y(z)) \tag{4.8}$$

The output current is:
$$i_o = i_{in} + i_1 \tag{4.9}$$

Substituting Eq.(4.8) into Eq.(4.9) produce the allpass transfer function Eq.(4.5), confirming that Fig.4.1 realizes the allpass system, whose order and pole positions are determined by *Y(z)*. It was shown in [58,59], if the poles of allpass transfer functions are inside the unit circle, the continued fraction expansion of *Y(z)* can be achieved.

$$Y(z) = C_1 \cdot \lambda + \cfrac{1}{L_2 \cdot \lambda + \cfrac{1}{\vdots + \cfrac{1}{C_N \cdot \lambda}}} \tag{4.10}$$

where λ is bilinear transformation factor $\frac{2}{T} \cdot \frac{1-z^{-1}}{1+z^{-1}}$, C_i, $L_i > 0$ $i = 1,2,\cdots N$

It means if the allpass transfer function *H(z)* is stable, *Y(z)* is analogous to a reactive driving-point admittance, which can be synthesized from the LC ladder circuit, Fig.4.2.

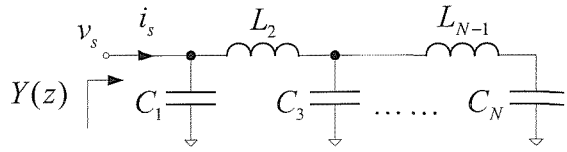


Fig.4.2 LC ladder network

There are several techniques for realizing LC ladder network, such as leapfrog method [79] and bilinear-LDI method [58], which was employed through various SI integrators. In this chapter, it is implemented using wave synthesis technique. The motivation for employing the wave synthesis technique is: it is based on the bilinear transformation between continuous and discrete time frequency domains and its resultant circuit do not require integrators as outlined in Chapter 2. More importantly, wave structure consists of elements, such as delay cells and wave adaptors, which are readily implemented in SI technology. The converted wave structure from Fig.4.2 is shown as following:

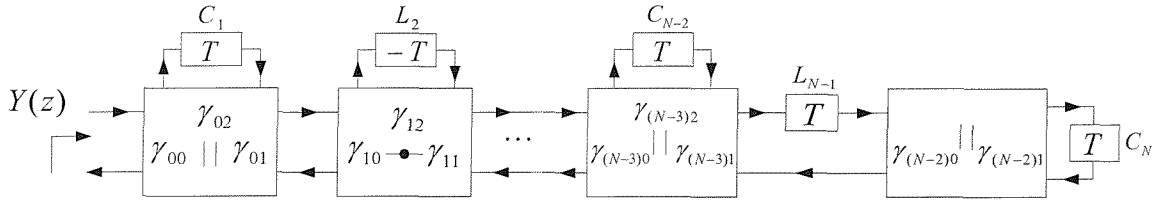


Fig.4.3 Wave structure of *LC* ladder network

Since the wave quantities (*A or B*) is processed in the wave block models, the conversion should be made between voltage-current relationship and wave quantities (*A or B*). From Table 2.1, the voltage source is transformed into wave models as follows:

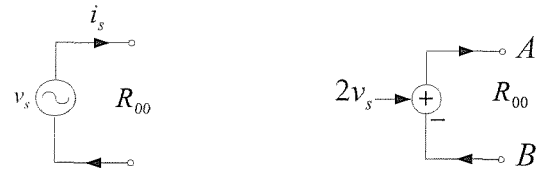


Fig.4.4 Voltage source and its wave models

It can be seen from the Fig.4.2 that voltage-current relationship is given as:

$$i_s = v_s \cdot Y(z) \qquad (4.11)$$

Using the definition of wave quantities Eq.(2.27), the input current i_s is expressed as:

$$i_s = (A - B)/2R_{00}, \text{ where } R_{00} \text{ is port resistance} \qquad (4.12)$$

Therefore, the converter, which performs Eq.(4.12) and outputs current signal equivalent of i_s, is added in front of wave structure, as shown in Fig.4.5.

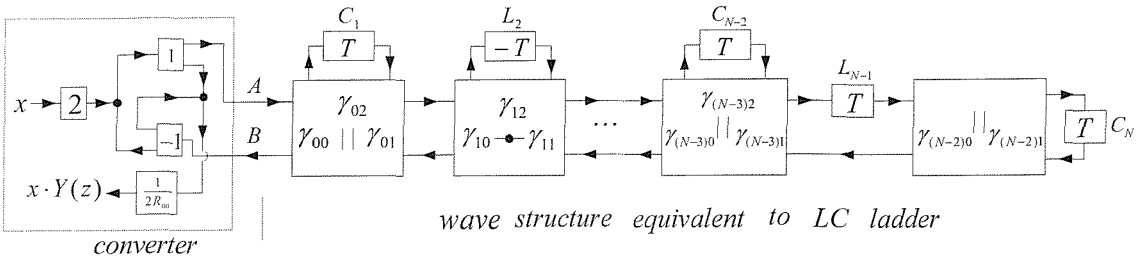


Fig.4.5 *Y(z)* realization using wave synthesis technique

4.3 Design of SI wave group delay equalizers

This section gives a detailed design process for SI wave group delay equalizer. First optimisation of allpass transfer function is described, and then design flow for the realization of SI wave group delay equalizer is presented.

4.3.1 Optimisation for z-domain allpass transfer function

The basic idea of optimisation is to find the coefficients of allpass transfer function so that the combined group delay of filter $\tau_F(\omega)$ and equalizer $\tau_E(\omega)$ is made more flat. One important property of allpass filter is that the filter, which is obtained by cascade connection of allpass sections, is also allpass filter. That means if $H_1(z)$, $H_2(z)$, ... $H_k(z)$ are allpass transfer function, then the following transfer function represents an allpass filter:

$$H(z) = H_1(z) \cdot H_2(z) \cdots H_k(z) \qquad (4.13)$$

This cascade structure is frequently used in optimisation because it reduces the problem of realizing the general transfer function of Eq.(4.2) to that of realizing a number of 2nd-order sections (biquads) plus perhaps 1st-order section.

To facilitate the optimisation process, the 2nd-order allpass section is expressed in terms of poles and zeros:

$$H_2(z) = \frac{(P - z^{-1})(\overline{P} - z^{-1})}{(1 - Pz^{-1})(1 - \overline{P}z^{-1})} \tag{4.14}$$

where P is pole and $\overline{P}$ is conjugate complex to P. The poles and zeros are harmonic conjugates, as shown in Fig.4.6

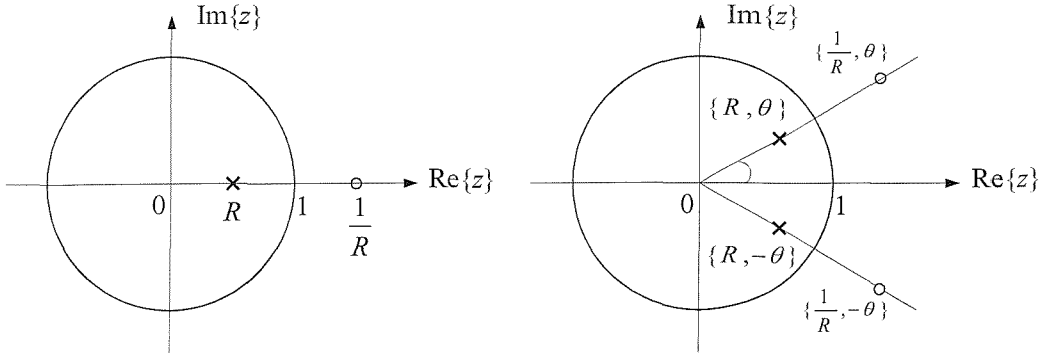


Fig.4.6 Pole-zero patterns of (a) first-order (b) second-order allpass filter

If the poles are expressed in terms of magnitude R and phase θ:

$$P = R \cdot e^{j\theta},\ \overline{P} = R \cdot e^{-j\theta} \qquad 0 < R < 1,\ 0 < \theta < \pi \tag{4.15}$$

The response of Eq.(4.14) is:

$$H_2(\omega)\Big|_{z=e^{j\omega}} = \frac{(e^{-j\omega T} - R \cdot e^{j\theta})(e^{-j\omega T} - R \cdot e^{-j\theta})}{(1 - R \cdot e^{j\theta} \cdot e^{-j\omega T})(1 - R \cdot e^{-j\theta} \cdot e^{-j\omega T})} \tag{4.16}$$

And the phase response can be obtained from Eq.(4.16):

$$\varphi(\omega) = -2\omega T - 2\arctan\left(\frac{\sin(\omega T + \theta) \cdot R}{1 - R \cdot \cos(\omega T + \theta)}\right) - 2\arctan\left(\frac{\sin(\omega T - \theta) \cdot R}{1 - R \cdot \cos(\omega T - \theta)}\right) \tag{4.17}$$

The group delay of 2nd-order section, $\tau_2(\omega)$, is defined as:

$$\tau_2(\omega) = -\frac{d\varphi(\omega)}{d\omega} = \frac{T(1 - R^2)}{1 - 2R \cdot \cos(\omega T - \theta) + R^2} + \frac{T(1 - R^2)}{1 - 2R \cdot \cos(\omega T + \theta) + R^2} \tag{4.18}$$

where T is sampling period, and when T=1, Eq.(4.18) is called normalized group delay of 2nd-order section $\tau_{2n}(\omega)$.

$$\tau_{2n}(\omega) = \tau_2(\omega) \cdot f_{CLK}\text{, where } f_{CLK} \text{ is sampling frequency} \tag{4.19}$$

Similarly, for the 1st-order section:

$$H_1(z) = \frac{z^{-1} - P}{1 - P \cdot z^{-1}}\text{, where } P = R \cdot e^{j\theta},\ \theta = 0 \text{ or } \pi,\ R<1 \tag{4.20}$$

The group delay is:

$$\tau_1(\omega) = \frac{T(1-R^2)}{1 \pm 2R \cdot \cos\omega T + R^2}, \text{ where '+' for } \theta = \pi \text{ and '-'for } \theta = 0 \qquad (4.21)$$

and the normalized group delay of 1st-order section is:

$$\tau_{1n}(\omega) = \tau_1(\omega) \cdot f_{CLK} \qquad (4.22)$$

The overall group delay of the allpass filter is the sum of the individual group delay in Eq.(4.18) and Eq.(4.21):

$$\tau_E(\omega) = \tau_1(\omega) + \sum_{i=1}^{k} \tau_{2i}(\omega), \text{ where the order of } H(z) \text{ is } N=2k+1 \qquad (4.23)$$

The input to the optimisation program is the group delay variation (group delay ripple) of the filter to be equalized specified in the form of data points (frequency, delay), equalizer order, N, and required final combined group delay ripple. The optimisation process aims to produce allpass transfer function, whose group delay $\tau_E(\omega)$ is approximately the inverse of that of filter $\tau_F(\omega)$ to be equalized. The optimisation procedure consists of minimizing the combined group delay ripple $\Delta\tau_{total}(\omega) = \Delta[\tau_E(\omega) + \tau_F(\omega)]$ by means of curve-matching approximation with following steps:

(i) An initial guess solution is generated for the order N and the magnitude R_i and phase θ_i of 1st and 2nd-order allpass section.

(ii) Given the order of N, the associated group delay for *kth* iteration $\tau_E(\omega, k)$ can be derived according to Eq(4.18), (4.21) and (4.23).

(iii) The combined group delay $\tau_{total}(\omega, k)$ is obtained within the desired frequency band ($0 < \omega < \omega_p$) for the *kth* iteration:

$$\tau_{total}(\omega, k) = \tau_E(\omega, k) + \tau_F(\omega, k) \qquad (4.24)$$

(iv) The variation of the group delay $\tau_{total}(\omega, k)$ is calculated using the cost function:

$$\Delta\tau_{total}(\omega) = \max(\tau_F(\omega) + \tau_E(\omega)) - \min(\tau_F(\omega) + \tau_E(\omega)) \qquad (4.25)$$

(v) If the desired minimal group delay variation is not achieved, the order N of group delay equalizer is increased and the algorithm continues from step(i).

Following this procedure, the required order N and coefficients a_i of allpass filter are determined. The group delay response of resultant equalizer $\tau_E(\omega)$ compensates the poor group delay characteristics of the filter and produces an overall flat combined group delay response. It should be noted that during the optimisation process, the normalized group delay is preferred for successful optimisation.

4.3.2 Design process of SI wave group delay equalizer

The second design process involves deriving *Y(z)* from the z-domain allpass transfer function, Eq.(4.2). Making continued fraction expansion on *Y(z)*, the LC ladder network, whose driving-point admittance is *Y(z)*, will be obtained. As discussed in section 4.2, the wave structure will be used to realize this LC network and wave adaptor coefficients are calculated using wave synthesis technique.

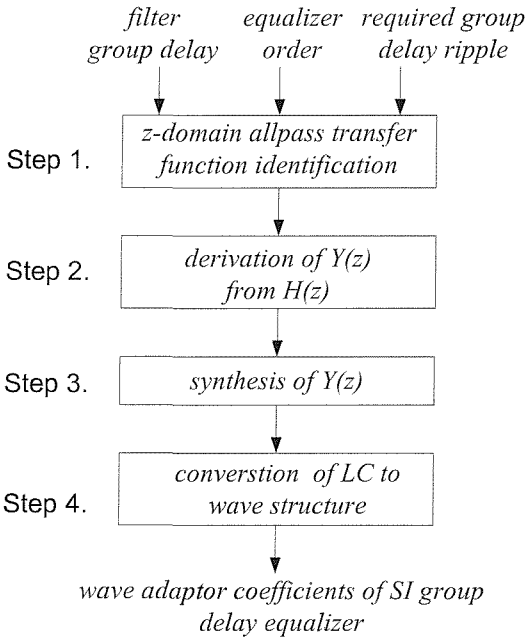


Fig.4.7 Design flow for SI wave equalizer

The overall design flow is shown in Fig.4.7. The input to the program is the group delay variation of the filter to be equalized specified in the form of data points (frequency, delay), equalizer order, *N*, and required final group delay ripple. To automate the SI wave equalizer design process, a computer program has been developed according to the design flow of Fig.4.7 and incorporated within *MATLAB*. It should be noted that optimisation process for z-domain transfer function is

implemented using *MATLAB* optimisation toolbox. The optimisation function *fmincon*, whose purpose is to find the minimum of constrained non-linear multivariable function, is used in the *MATLAB* program. The details of group delay design program are given in Appendix B.

4.4 Design and simulation examples

This section demonstrates the effectiveness of the proposed SI wave equalizer design flow through some design examples. For the 3rd-order lowpass SI elliptic filter circuit (Fig.2.1) with passband frequency 100kHz (f_p =*100kHz*) and sampling frequency 1MHz (f_{CLK} =*1MHz*), switched-circuit simulator, such as SCNAP4 [87], is used to derive its group delay response in the form of data points (frequency, delay). In SCNAP4, transistors are considered as ideal transconductors with parasitic effects ignored. For optimisation process, the group delay response is normalized using Eq.(4.19) and Eq.(4.22), and shown in Fig.4.8, where the sampling frequency is 1Hz and passband frequency is 0.1Hz. Using optimisation program discussed in section 4.3, it is found that the 7th-order group delay equalizer can be used to reduce the normalized group delay variation $\Delta\tau_n(\omega)$ from 2.294s to 0.162s when it is cascaded with the filter, Fig.4.8. An enlarged plot of the normalized group delay ripple of filter cascaded with 7th-order equalizer is also given in Fig.4.8.

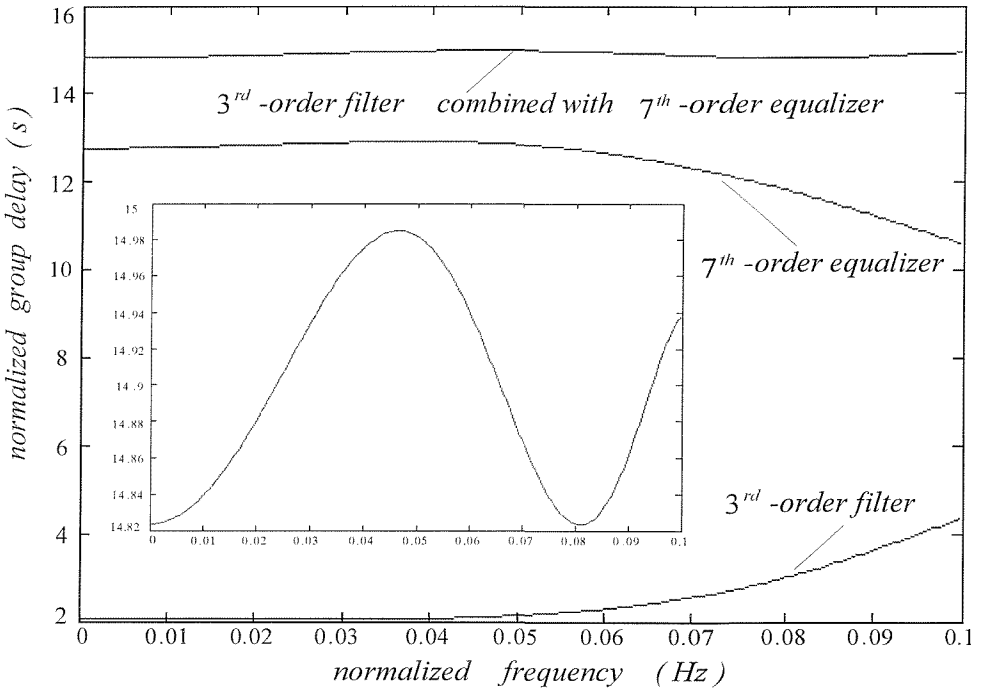


Fig.4.8 *MATLAB* optimisation of 7th-order allpass filter (equalizer)

The optimisation result for 7th-order allpass filter, which is expressed in term of magnitude (R_i) and phase (θ_i), is given in Table 4.1.

Table 4.1 Optimisation result of 7th–order allpass filter (equalizer)

$R_1 = 0.622$	$\theta_1\ (radian) = 0.39$
$R_2 = 0.487$	$\theta_2\ (radian) = 0.416$
$R_3 = 0.772$	$\theta_3\ (radian) = 1.43$
$R_4 = 0.441$	$\theta_4\ (radian) = 0$
combined normalized ripple $\Delta\tau_n(\omega)$	*0.162s*

Fig.4.9 shows the pole-zero plot of 7th-order allpass filter (group delay equalizer). As can be seen, the poles and zeros are reciprocal of one another, confirming the correct theoretical design of the group delay equalizer.

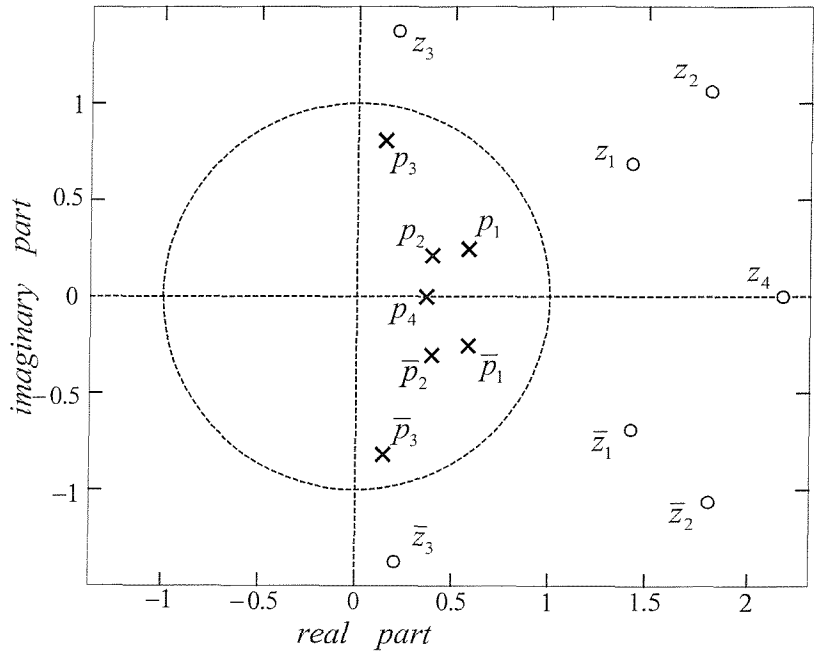


Fig.4.9 Pole-zero plot of 7th-order allpass filter (equalizer)

The resultant 7th-order allpass transfer function is:

$$H(z)=\frac{(P_1-z^{-1})(\overline{P}_1-z^{-1})}{(1-P_1z^{-1})(1-\overline{P}_1z^{-1})}\cdots\frac{(P_3-z^{-1})(\overline{P}_3-z^{-1})}{(1-P_3z^{-1})(1-\overline{P}_3z^{-1})}\cdot\frac{(z^{-1}-P_4)}{(1-P_4\cdot z^{-1})}$$

$$=-\frac{z^{-7}+a_1z^{-6}+a_2z^{-5}+a_3z^{-4}+a_4z^{-3}+a_5z^{-2}+a_6z^{-1}+a_7}{a_7z^{-7}+a_6z^{-6}+a_5z^{-5}+a_4z^{-4}+a_3z^{-3}+a_2z^{-2}+a_1z^{-1}+1} \qquad (4.26)$$

where $a_1=$-2.7, $a_2=3.684$, $a_3=$-3.378, $a_4=2.176$, $a_5=$-0.921, $a_6=0.226$, $a_7=$-0.024

From Eq.(4.5), the *Y(z)* is derived as:

$$Y(z)=\frac{(a_0+a_7)+(a_1+a_6)\cdot z^{-1}+\cdots(a_7+a_0)\cdot z^{-7}}{(a_0-a_7)+(a_1-a_6)\cdot z^{-1}+\cdots(a_7-a_0)\cdot z^{-7}}$$

$$=\frac{b_0+b_1z^{-1}+b_2z^{-2}+b_3z^{-3}+b_4z^{-4}+b_5z^{-5}+b_6z^{-6}+b_7z^{-7}}{c_0+c_1z^{-1}+c_2z^{-2}+c_3z^{-3}+c_4z^{-4}+c_5z^{-5}+c_6z^{-6}+c_7z^{-7}} \qquad (4.27)$$

where $b_0=0.976$, $b_1=$-2.474, $b_2=2.763$, $b_3=$-1.202, $b_4=$-1.202, $b_5=2.763$, $b_6=$-2.474, $b_7=0.976$, $c_0=1.024$, $c_1=$-2.926, $c_2=4.605$, $c_3=$-5.554, $c_4=5.554$, $c_5=$-4.605, $c_6=2.926$, $c_7=$-1.024

Using computer program, Eq.(4.27) can be expanded into the continuous-fraction form:

$$Y(z)=C_1\cdot\lambda+\cfrac{1}{L_2\cdot\lambda+\cfrac{1}{\vdots+\cfrac{1}{C_N\cdot\lambda}}} \qquad (4.28)$$

where λ is bilinear transformation factor $\frac{2}{T}\cdot\frac{1-z^{-1}}{1+z^{-1}}$, and $C_1=0.2459$, $L_2=0.6682$, $C_3=0.8741$, $L_4=0.9661$, $C_5=1.3913$, $L_6=2.3407$, $C_7=3.8691$

In this way, *Y(z)* is synthesized as 7th-order LC network shown in Fig.4.10.

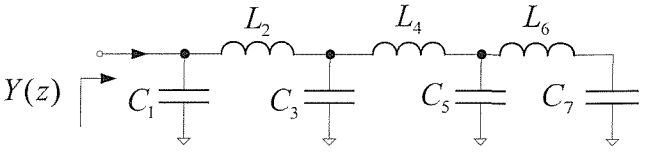


Fig.4.10 7th-order LC network

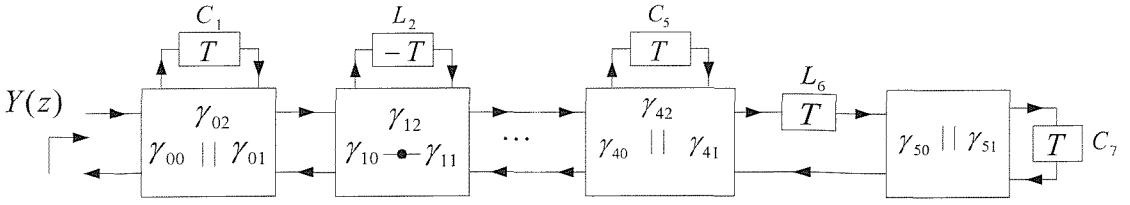


Fig.4.11 The wave structure for 7th-order LC network

The wave synthesis technique is used to implement the LC ladder network. The wave structure is given in Fig.4.11 and its wave adaptor coefficients are calculated as follows:

(1) Calculate the port resistance:

$R_{02} = T/2C_1 = 2.033,\ R_{12} = 2L_2/T = 1.3364,\ R_{22} = T/2C_3 = 0.572,\ R_{32} = 2L_4/T = 1.932,$

$R_{42} = T/2C_5 = 0.36,\ R_a = 2L_6/T = 4.6814,\ R_b = T/2C_7 = 0.13,\ R_{50} = R_a + R_b = 4.81,$

$R_{51} = (R_b/R_a)\cdot R_{50} = 0.1336$

(2) Calculate the coefficient of wave adaptor: $\gamma_{50} = 2G_{50}/(G_{50}+G_{51}) = 0.054,$ $\gamma_{51} = 2-\gamma_{50} = 1.946,$ *Setting* $R_{00} = R_{01} = R_{10} = R_{11} = R_{20} = R_{21} = R_{30} = R_{31} = R_{40} = 1$ *and using the definition of wave adaptor coefficients, Eq.(2.35) and Eq.(2.40)* $\Rightarrow \gamma_{00} = 0.8,\ \gamma_{01} = 0.8,\ \gamma_{02} = 0.4,\ \gamma_{10} = 0.6,\ \gamma_{11} = 0.6,\ \gamma_{12} = 0.8,\ \gamma_{20} = 0.533,$ $\gamma_{21} = 0.533, \gamma_{22} = 0.934, \gamma_{30} = 0.51, \gamma_{31} = 0.51, \gamma_{32} = 0.98, \gamma_{40} = 0.5, \gamma_{41} = 0.1, \gamma_{42} = 1.4$

SCNAP4 simulation is made on the 3rd-order 100kHz lowpass SI elliptic filter and filter cascaded with the resultant SI wave group delay circuit, respectively. The block *Y(z)* in SI wave group delay circuit, Fig.4.1, is represented by the 7th-order wave structure, and the sampling frequency of the SI circuit is set to 1MHz. Since the normalized passband frequency (f_p / f_{CLK}) is 0.1 as defined in the design process, the denormalized passband frequency of SI circuit is 100kHz. The detailed SCNAP4 program for 3rd-order SI wave filters and group delay equalizers are given in Appendix D. Fig.4.12 shows the 3rd-order SI elliptic filter has group delay ripple of almost 2.75 μs between DC and 100kHz. As can be seen, nearly flat group delay response has been obtained in the filter cascaded with the 7th-order wave group delay equalizer. An

enlarged plot of the group delay ripple is also included in Fig.4.12, which shows that the equalizer has reduced the group delay variation of the filter from 2.75 μs to nearly 0.165 μs over the entire filter bandwidth.

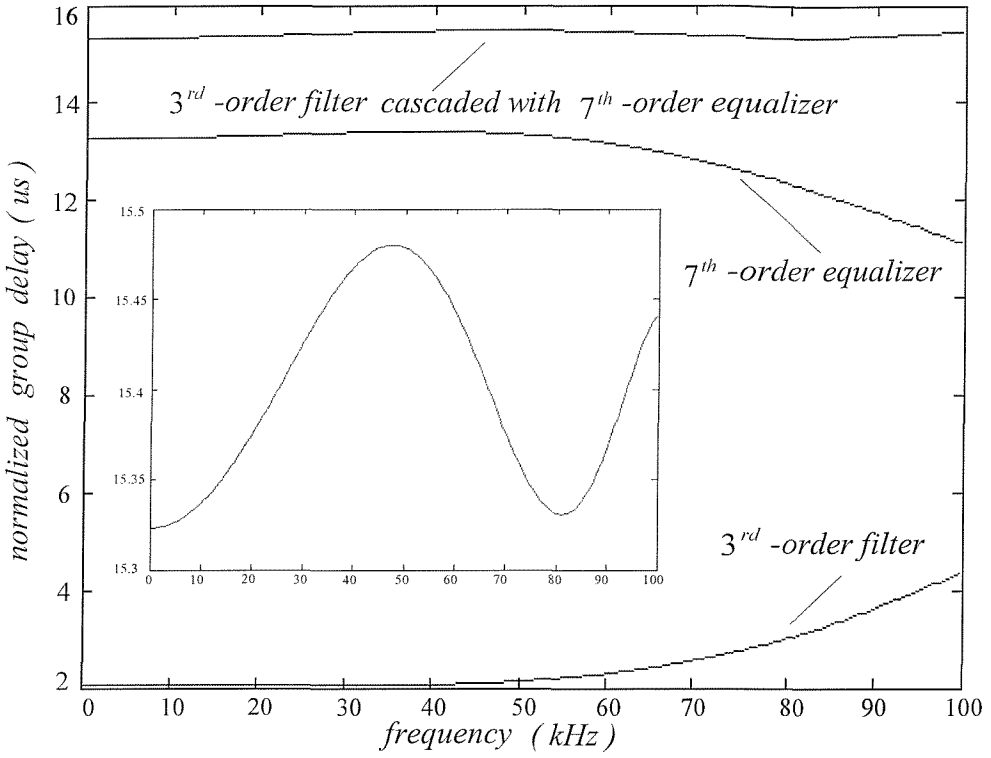


Fig.4.12 Group delay response of filter, equalizer and filter cascaded with equalizer

As discussed in Chapter 1, group delay is the derivation of phase with respect to frequency. To illustrate the effect of cascading an allpass circuit with the filter on the phase response, Fig.4.13 shows the phase response of the filter and filter cascaded with 7^{th}-order allpass circuit. It can be seen the phase response of the filter is not linear with frequency, while the phase response of the cascaded filter with allpass circuit is linear.

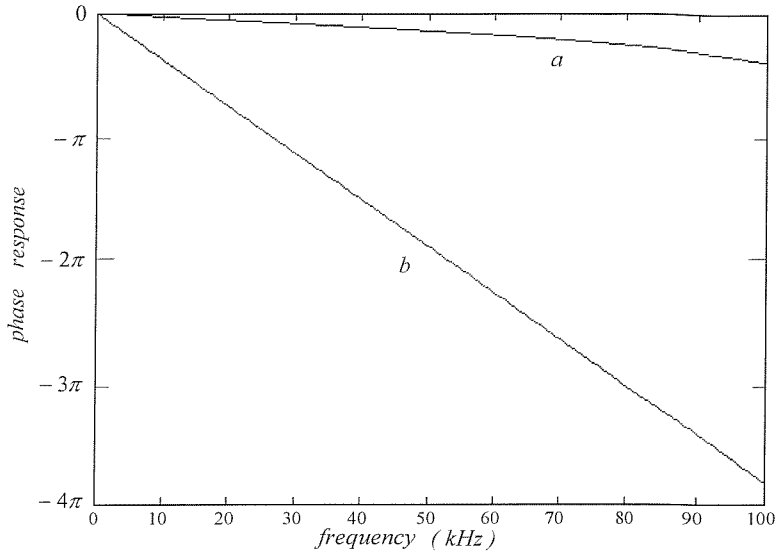


Fig.4.13 Phase response a) elliptic filter b) filter cascaded with 7th-order allpass circuit

To confirm the theoretical analysis of the proposed methodology, another two group delay equalizers with order three and five are designed using the computer program outlined to equalize the group delay response of 3rd-order 100kHz lowpass SI elliptic filter. To obtain the other order SI equalizers using the proposed allpass circuit architecture (Fig.4.1), it is only required to replace the driving-point admittance *Y(z)* of Fig.4.1 with the required order of wave structure generated from the design flow in Fig.4.7. The details of 3rd-order group delay wave equalizer are given in Chapter 5 as an example of practical implementation, and the 5th-order allpass transfer function is:

$$H(z) = -\frac{z^{-5} + a_1 z^{-4} + a_2 z^{-3} + a_3 z^{-2} + a_4 z^{-1} + a_5}{a_5 z^{-5} + a_4 z^{-4} + a_3 z^{-3} + a_2 z^{-2} + a_1 z^{-1} + 1} \qquad (4.29)$$

where $a_1 = 0.178$, $a_2 = -1.19$, $a_3 = -0.167$, $a_4 = 0.43$, $a_5 = -0.142$

Using wave synthesis technique, the wave adaptor coefficients are calculated as:

$\gamma_{00} = 0.95$, $\gamma_{01} = 0.95$, $\gamma_{02} = 0.1$, $\gamma_{10} = 0.9875$, $\gamma_{11} = 0.9875$, $\gamma_{12} = 0.025$, $\gamma_{20} = 0.285$, $\gamma_{21} = 0.29$, $\gamma_{22} = 1.425$, $\gamma_{30} = 0.075$, $\gamma_{31} = 1.925$

The circuits of 3rd and 5th-order SI wave equalizers are simulated using SCNAP4 and shown in Fig.4.14. It can be seen that the group delay ripple of cascaded filter and equalizer reduces as the equalizer order increases, as expected. For example, in case of the 7th-order equalizer, the ripple is nearly 0.165 μs, while the 3rd and 5th-order

equalizers reduce the group delay ripple of the filter to $0.23\,\mu$s and $0.19\,\mu$s, respectively.

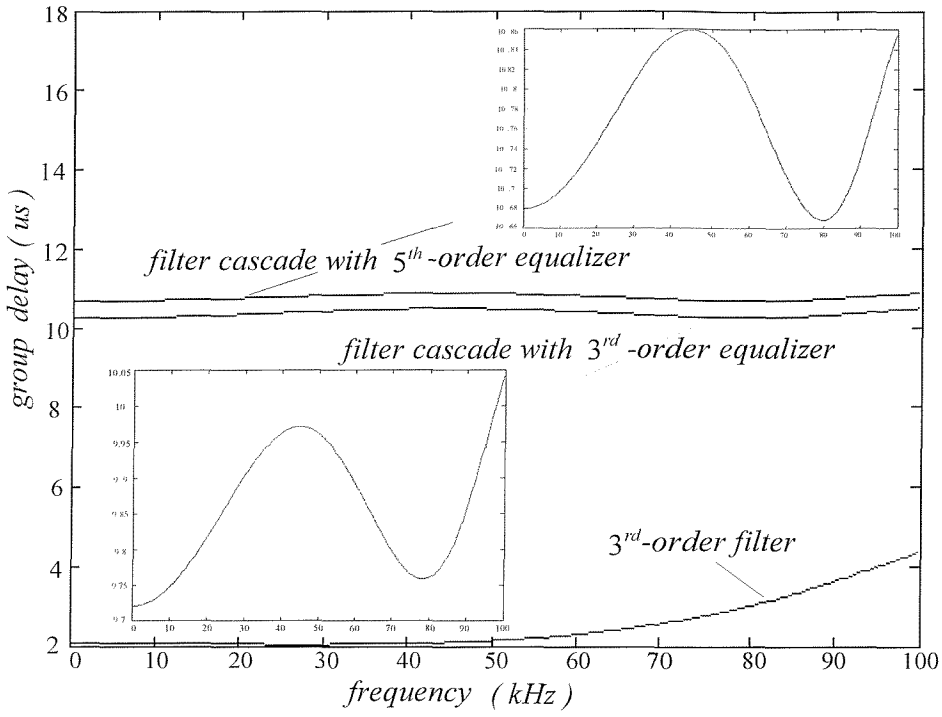


Fig.4.14 Group delay response of filter cascaded with 3rd and 5th-order equalizer

The details of *MATLAB* design and SCNAP4 simulation results are shown in Table 4.2. Note that the inclusion of group delay equalizer with filter increases the propagation delay of the filter, for example the filter propagation delay is approximately 15.5μs when 7th-order equalizer is connected (Fig.4.12) compared with 2.1μs when no equalizer is connected. The increase in propagation delay needs to be considered carefully in certain applications and may be reduced during step one of the design flow of Fig.4.7, if the propagation is input as a constraint in the optimisation process.

Table 4.2 Design and simulation result of 3rd-order SI elliptic lowpass filter (sampling frequency=*1MHz*, passband frequency =*100kHz*, group delay ripple =2.75 μs)

The order of equalizer	3rd	5th	7th
MATLAB Design: normalized group delay ripple of filter cascaded with equalizer	0.224	0.185	0.162
SCNAP4 Simulation: propagation of filter cascaded with equalizer	9.9 μs	10.75 μs	15.5 μs
SCNAP4 Simulation: group delay ripple of filter cascaded with equalizer	0.23 μs	0.19 μs	0.165 μs

As mentioned earlier, filters with large group delay variations or non-linear phase lead to waveform distortion in the form of overshoot in the step response. To demonstrate this point, Fig.4.15, trace (a) shows the step response of the 3rd-order elliptic lowpass filter without any group delay equalization, while trace (b) shows the step response of same filter cascaded with the 7th-order equalizer discussed earlier.

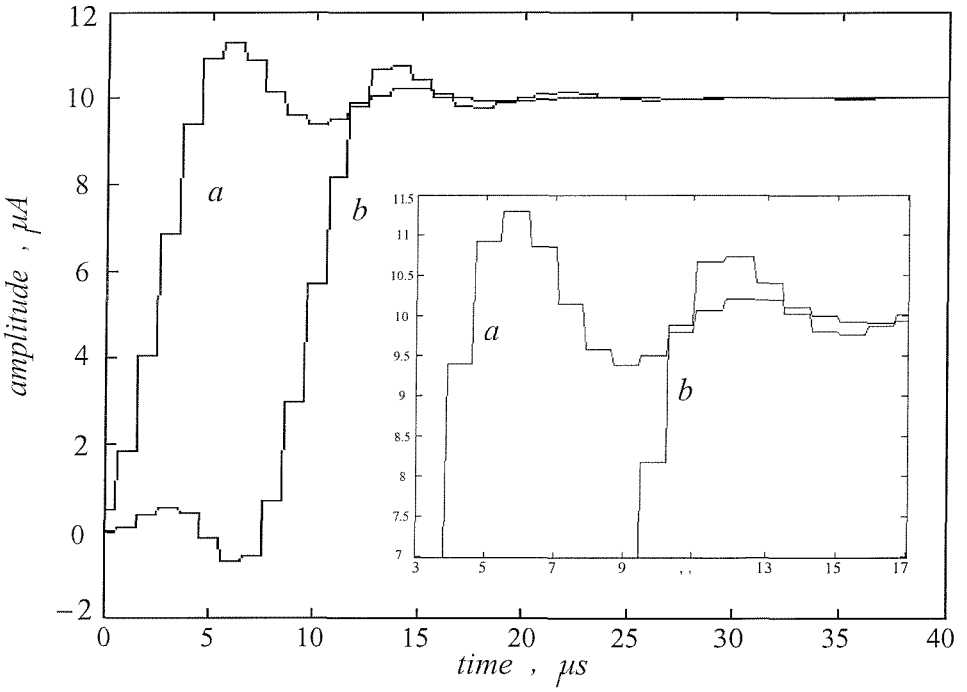


Fig.4.15 Step response of (a) 3rd-order elliptic filter (b) filter cascaded with 7th-order allpass circuit

As can be seen, the equalizer has resulted in reducing the amount of overshoot present in the filter step response by nearly 50%. Note all simulation results are obtained using 1st-generation delay cells in SI allpass filters.

4.5 Concluding remarks

This chapter presented new design methodology for *Nth*-order allpass SI circuits. This methodology combined wave synthesis technique, ladder-derived allpass equalizer design method and SI technology to produce the transistor-level realizations of group delay equalizer. The detailed design processes, including optimisation and synthesis of wave structure, are described and the resultant SI circuits can be implemented using SI technology. As a ladder-based design method, the resultant group delay wave equalizer has low magnitude sensitivity. In addition, this methodology has its simplicity to expand into high-order equalizers, because to obtain different order circuits only requires modifying a specific part, *Y(z)*, in the allpass circuit architecture. The complete design example of 7th-order group delay wave equalizer is presented, and the step response of 3rd-order elliptic SI filter cascaded with 7th-order group delay wave equalizer is simulated. It has been demonstrated that the overshoot in the step response is reduced by 50% when the filter is cascaded with group delay equalizer.

Chapter 5

Transistor-level design of SI Wave Filters and Group Delay Equalizers

5.1 Introduction

Chapter 2 and 3 have considered the design and non-ideal performance of Bruton transformation SI wave filters. Chapter 4 presents new design method of SI group delay wave equalizers. In this chapter, the transistor-level circuits of SI wave filters and equalizers have been designed. Section 5.2 introduces the basics of CMOS technology, and the non-ideal characteristics of SI technology, such as mismatch, clock-feedthrough, conductance ratio error and settling error, are discussed in section 5.3. Section 5.4 presents the practical circuit design of SI building blocks, and circuit design techniques are employed to minimize the influence of these non-ideal characteristics. Section 5.5 and 5.6 provide the overall transistor-level circuits of SI wave filters and group delay equalizers. In order to validate the investigation of SI wave filters and group delay equalizers (Chapter 3 and 4), the standard 1.2 μm p-well CMOS parameters and level-2 transistor models are used to simulate the resultant circuits. The clock-feedthrough effects on these transistor-level circuits are included in section 5.7.

5.2 Transistor models and characteristics

The design of analogue circuits relies on an understanding of the transistor models used. Models of transistors are derived from semiconductor physics. This section briefly reviewed the first-order model, which is used to evaluate circuit performance through hand-calculations. To obtain the second-order effects of circuit behaviour, such as precise gain, distortion and noise, depends on second-order transistor characteristics. The circuit simulator, such as SPICE, provides a full transistor model, which is used to verify the circuit's performance.

5.2.1 MOS transistor characteristics and circuit models

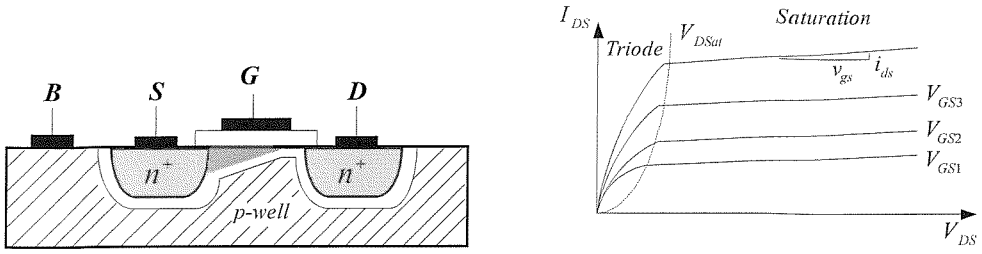


Fig.5.1 MOS transistor (MOST) and its characteristics

The ideal 'Long Channel' device characteristics, Fig.5.1, are modelled as simple quadratic expressions [83]:

For saturation region ($V_{DS} > V_{GS} - V_T$):

$$I_{DS} = \frac{\mu C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \qquad (5.1)$$

For triode region ($V_{DS} < V_{GS} - V_T$):

$$I_{DS} = \mu C_{ox}\frac{W}{L}(V_{GS} - V_T - \frac{V_{DS}}{2})V_{DS} \qquad (5.2)$$

where μ is surface mobility of the channel ($cm^2 / volt \cdot$ seconds)

$C_{ox} = \varepsilon_{ox} / t_{ox}$ is capacitance per unit area of the gate oxide (F / cm^2)

$\varepsilon_{ox} = 0.34 pF / cm$ is dielectric constant of silicon oxide

W is effective channel width and L is effective channel length

λ is channel length modulation.

The boundary between saturation and triode region is $V_{DSsat} = (V_{GS} - V_T)$.

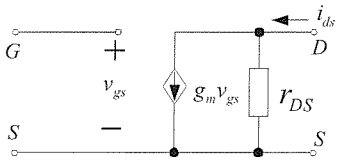


Fig.5.2 Small signal or AC equivalent circuit

In order to evaluate the response of gain stage to actual small signals, small-signal models need to be used, Fig.5.2. Small signals are considered to be small variations on DC or biasing voltages. In saturation region, the relation between small signal i_{ds} and v_{gs} is given by the slope of i_{ds} versus v_{gs} at static point Q, which yields:

$$g_m = \frac{\partial i_{ds}}{\partial v_{gs}} = \mu C_{ox} \frac{W}{L}(V_{GS} - V_T) = KP \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \qquad (5.3)$$

Alternative expressions are obtained by substitution, such as:

$$g_m = 2\sqrt{\mu C_{ox} \frac{W}{L} I_{DS}} \qquad \text{or} \qquad g_m = \frac{2I_{DS}}{V_{GSQ} - V_T} \qquad (5.4)$$

The output resistance r_{DS} or output conductance $g_{DS} = 1/r_{DS}$ is the result of the channel-shortening effect by v_{DS}. This effect causes the current to increase slowly for increasing values of v_{DS}. The value of parameter r_{DS} can be derived from Eq.(5.1) and is given by:

$$r_{DS} = \frac{1}{\lambda I_{DS}} \qquad (5.5)$$

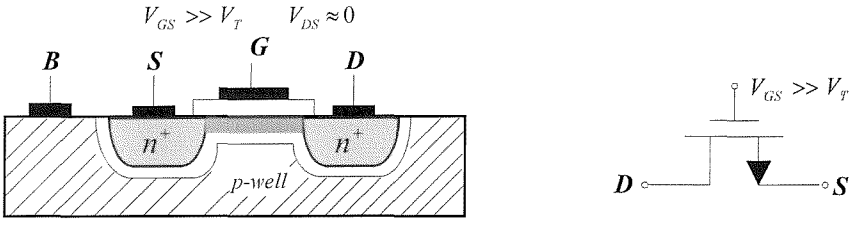


Fig.5.3 MOST switch and resistor

The triode region is often used to design analogue MOST switch and resistor, Fig.5.3. In these applications, a large value of V_{GS} is applied, and V_{DS} is kept at nearly zero. The channel consists of mobile electrons with charge Q_m. This mobile charge Q_m actually connects drain and source, and is given as $Q_m = C_{ox}(V_{GS} - V_T)$. It acts as a resistance connecting drain and source and is given by the sheet resistance under the gate. Its value is inversely proportional to this charge, as given as:

$$r_{DS\square} = \frac{1}{\mu Q_m} \qquad (5.6)$$

For the actual value of the resistance, its dimensions W and L must be considered. This yields:

$$r_{DS} = r_{DS\square} \frac{L}{W} = \frac{1}{\mu C_{ox} \frac{W}{L}(v_{GS} - V_T)} \qquad (5.7)$$

All of the above equations have been presented for n-channel transistors. In the case of p-channel transistors, a negative sign should be placed in front of every voltage

variable in the above equations. Thus, V_{GS} becomes V_{SG}, V_{DS} becomes V_{SD}, and so on. The condition required for p-channel conduction is $V_{SG} > -V_{tp}$, where V_{tp} is threshold voltage for p-channel transistor and is a negative value.

5.2.2 MOS transistor capacitors

At higher frequencies, parasitic capacitances in MOS transistors become important, and they must be added in the small signal model, as shown in Fig.5.4.

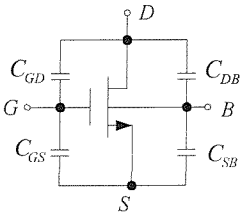


Fig.5.4 Terminal parasitic capacitances in MOST

Terminal capacitances C_{GS}, C_{GD}, C_{DB} and C_{SB}, as shown in Fig.5.4, are determined as listed in Table 5.1. And it is repeated for MOST in the regions of operation: saturation region and triode region.

Table 5.1 Terminal parasitic capacitances [83]

Saturation region	
$C_{GS} = C_{GS0} + 2/3C_{oxt}$	$C_{SB} = C_{jSBt} + 2/3C_{BCt}$
$C_{GD} = C_{GD0}$	$C_{DB} = C_{jDBt}$
Triode region	
$C_{GS} = C_{GS0} + 1/2C_{oxt}$	$C_{SB} = C_{jSBt} + 1/2C_{BCt}$
$C_{GD} = C_{GD0} + 1/2C_{oxt}$	$C_{DB} = C_{jDBt} + 1/2C_{BCt}$

MOS transistor parameters, which used in the derivation of small signal model, are obtained from measurements and provided by the silicon foundry. Representative values for the standard 1.2 μm *p-well* CMOS process are listed in Table 5.2.

Table 5.2 SPICE parameters for MOST (*p-well* CMOS)

Type	*n*MOS	*p*MOS	Dimension	Name
VT0	*0.74*	*-0.74*	*V*	*Zero bias threshold voltage*
KP	*8.0E-5*	*2.7E-5*	A/V^2	*Transconductance parameter*
LAMBDA	*0.037*	*0.061*	V^{-1}	*Channel length modulation parameter*
GAMMA	*0.54*	*0.58*	$V^{1/2}$	*Bulk threshold parameter*
CGS0	*4.3E-10*	*4.3E-10*	*F/m*	*GS overlap capacitance per meter channel width*
CGD0	*4.3E-10*	*4.3E-10*	*F/m*	*GD overlap capacitance per meter channel width*
TOX	*2.0E-8*	*2.0E-8*	*m*	*Oxide thickness*
LD	*1.5E-7*	*1.5E-7*	*m*	*Lateral diffusion*

According to the parameters given in Table 5.2, the parasitic capacitance in MOST can be evaluated as follows:

For example in saturation region:

$$C_{ox} = \varepsilon_{ox} / TOX = 1.7 \times 10^{-3}\, pF/\mu m^2 \tag{5.8}$$

$$C_{GS} = C_{GS0} + 2/3 C_{oxt}, \text{ where } C_{oxt} = C_{ox} W L_{eff},\ C_{GS0} = CGS0 \times W \tag{5.9}$$

$$C_{GD} = C_{GD0}, \text{ where } C_{GD0} = CGD0 \times W \tag{5.10}$$

5.3 Non-ideal characteristics in SI technology

The main advantages of SI technology are its high-speed, low-voltage potential and its compatibility with digital CMOS technology. There is however a set of non-ideal characteristics associated with practical current-mode circuits. In this section, these non-ideal characteristics are summarized. First, mismatch and clock-feedthrough, which have been described in Chapter 3, are briefly reviewed. Then the other two non-ideal characteristics, conductance ratio error and settling error, are introduced. These imperfections result in deviations from the ideal performance described in Chapter 2.

Mismatch errors

The mismatch is due to processing techniques and involves physical parameters such

as V_T and the geometry of devices, i.e., W and L. Considering the current mirrors, Fig.5.5, there are three types of mismatches listed as follows:

- $\mu C_{ox} \cdot W / L$ ($K = \mu C_{ox} \cdot W / L$) mismatch
- V_T (threshold voltage) mismatch
- λ (channel length modulation) mismatch

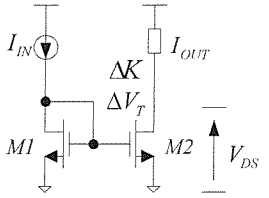


Fig.5.5 Current mismatch as a result of K, V_T and λ

Clock-feedthrough errors

Clock-feedthrough is a phenomenon in which some fraction of the charges stored in the channel of MOST switches are discharged onto associated capacitor as they turned *OFF*, Fig.5.6. A fraction of charge is injected into the memory capacitor, C_{GS2}, from the switch's gate-diffusion overlap capacitance, and it leaves an error voltage δV on capacitor C_{GS2}, resulting an error in the cell's output current, δI.

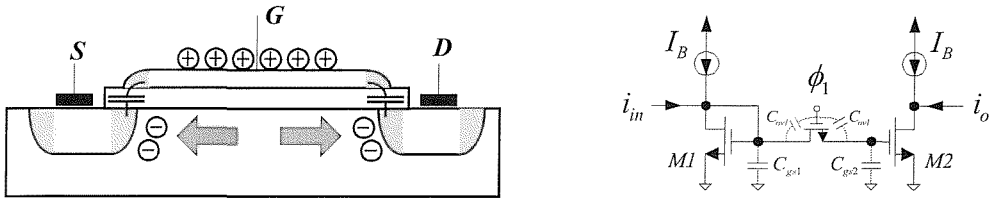


Fig.5.6 Clock-feedthrough in SI memory cell

Many clock-feedthrough compensation techniques have been put forward, which aim to reduce the error voltage or the amount of charge that is actually injected into the gate of the memory transistor [41-53]. The most obvious way to achieve this is to increase the capacitance at the storage node. Unfortunately, it will lead to large dominant attenuation, so this technique is only useful for low-speed applications. In this section, we combined the increment of memory capacitance with cancellation techniques, which using CMOS switches, to achieve the clock-feedthrough compensation in high-speed applications.

Conductance ratio errors

Ideal current mirror should have infinite output impedance and zero input impedance. In reality, the output impedance of simple current mirrors, Fig.5.7, is $1/g_{DS2}$ and the input impedance of next stage is $1/g_m$.

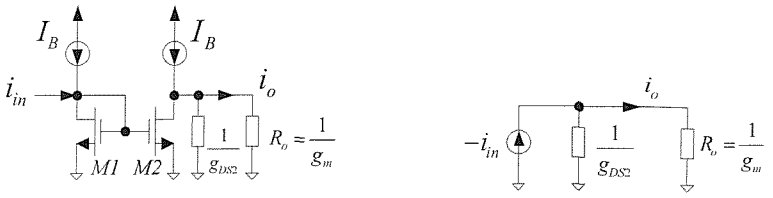


Fig.5.7 Conductance ratio errors

Thus, the resulting output is: $i_o = -\frac{g_m}{g_m + g_{DS2}} \cdot i_{in} \approx -(1 - \frac{g_{DS2}}{g_m}) \cdot i_{in}$ (5.11)

According to Eq.(5.11), the transfer from the output transistor to the input transistor of next stage is always less than unity. In SI filters, this will cause poles/zeros displacement. Therefore, SI circuits are usually implemented with some techniques that improve the conductance ratios. Cascode technique [1,14,61] is often used to increase output impedance. Thus, implementations presented in this chapter will use wide-swing cascode structures [80].

Settling errors

The operation of SI memory cell involves the charging of its gate capacitor to the gate-source voltage of diode-connected input transistor. If this charging is not completed during the time interval when switch ϕ_1 is on (time interval *T/2*), a residual error voltage results [1]. At the end of this interval, switch ϕ_1 is off, the error voltage is stored, and it results in an error in the memory cell's output current.

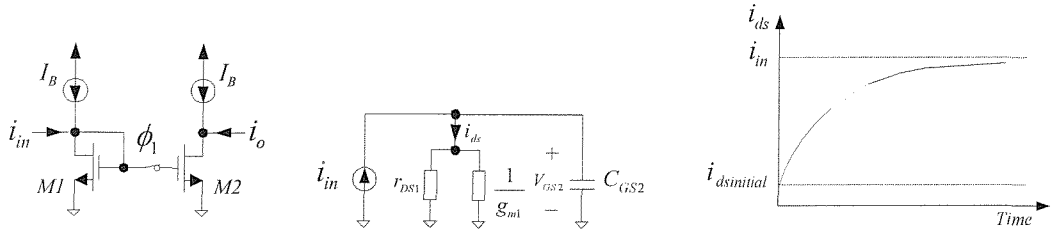


Fig.5.8 Settling errors

Fig.5.8 shows the small signal model for the 1st-generation memory cell during the phase ϕ_1. In this figure, we replace the diode-connected transistor by resistance $1/g_{m1}$

in parallel with the output resistance r_{DS1} and gate-source capacitance. The small signal drain current is found to be:

$$i_{ds}(t) = (i_{in} - i_{dsinitial})[1 - e^{-t/\tau}] + i_{dsinitial} \tag{5.12}$$

where $r_{DS1} >> 1/g_{m1}$ and τ can be approximately by C_{GS2}/g_{m1}

Thus, the small drain current is described as an exponentially decaying function. At the end of phase ϕ_1, the small signal drain current, denoted as $i_{dsfinal}$, will be:

$$i_{dsfinal}(t) = (i_{in} - i_{dsinitial})[1 - e^{-T/2\tau}] + i_{dsinitial} \tag{5.13}$$

We can rearrange the above equation and express the ratio of actual change in the drain current over the ideal change in the drain current:

$$\frac{i_{dsfinal} - i_{dsinitial}}{i_{in} - i_{dsinitial}} = [1 - e^{-T/2\tau}] \tag{5.14}$$

The ideal value of this ratio is one, and Eq.(5.14) indicates the effectiveness of the charge transfer process. The settling error ε is given as follows:

$$\varepsilon = e^{-T/2\tau} \tag{5.15}$$

It is obvious that in order to reduce the settling error either transconductance g_{m1} is made large or the gate-source capacitance is made small.

The main non-ideal characteristics in SI technologies have been summarized. These non-ideal characteristics limit the high accurate operations of SI circuits, and they also complicate the understanding and predictions of SI circuits' performance. Depending on the target system, these errors will have a different impact on the overall system performance. From a system designer's perspective, it is important to discern which errors are critical, analyse and compensate for these non-ideal characteristics.

5.4 Design of SI building blocks

SI building blocks of wave filters are current mirror, CMOS switches and delay cell. In this section, the practical designs of these building blocks are described.

5.4.1 Current mirror

Cascode technique [1,14,61] is often used to increase output impedance or lower the output conductance. Wide-swing cascode current mirrors are employed in the transistor-level implementation to reduce the conductance ratio errors, Fig.5.9.

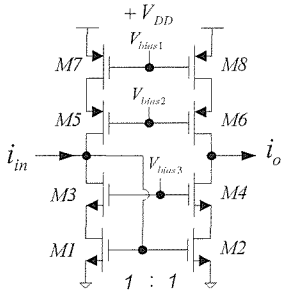


Fig.5.9 Wide-swing cascode current mirror [80]

The output resistance of wide-swing cascode current mirror is:

$$R_{out} = (g_{m4} \cdot r_{DS4} \cdot r_{DS2}) // (g_{m6} \cdot r_{DS6} \cdot r_{DS8}) \qquad (5.16)$$

In this circuit, transistor *M3* is included to lower the drain-source voltage of *M1* so that it is matched to drain-source voltage of *M2* and mismatch errors. The main advantage of this structure is the input signal voltage or current has larger dynamic range before making the transistors enter into triode region. In practical application, minimizing the lengths of *M1* and *M2* maximizes the frequency response, as their gate-source capacitances are the most significant capacitances contributing to high frequency poles. With the consideration of minimizing mismatch errors, a typical gate length of *M1* and *M2* is three times the minimum allowable channel length. *M3* and *M4* should be chosen to have shorter length to improve bandwidth. Due to the voltages across *M3* or *M4*, their typical size of length should be twice the minimum allowable channel length. This choice of gate lengths of *M3* and *M4* helps to eliminate short-channel effects.

5.4.2 MOS transistor switches

The circuit model for MOST as a switch is shown in Fig.5.10. Under the control of clock phase (i.e. ϕ_1 and ϕ_2), the MOST alternates between the cutoff and triode regions, which constitute the switch *OFF* and *ON* states, respectively.

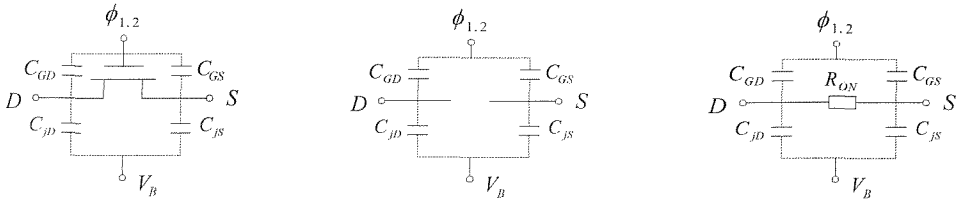


Fig.5.10 *P* or *NMOS* switch: (a) Switch circuit with bias V_B and control clock $\phi_{1,2}$
(b) Model for the *OFF* state (c) Model for the *ON* state

In its operation as a switch, MOST is a variable resistor with a very large resistance ($R_{OFF} \to \infty$) when the switch is *OFF*, and a very small resistor ($R_{ON} \to 0$) when the switch is *ON*. Expressions for the parasitic capacitances in the cutoff and triode regions are listed in Table 5.3.

Table 5.3 Parasitic capacitance in MOST switch [83]

Cutoff region	Triode region
$C_{GS} = C_{GS0}$	$C_{GS} = C_{GS0} + 1/2C_{oxt}$
$C_{GD} = C_{GD0}$	$C_{GD} = C_{GD0} + 1/2C_{oxt}$
$C_{jS} = C_{jSB}A_S$	$C_{jS} = C_{jSB}A_S + 1/2C_{BCt}$
$C_{jD} = C_{jDB}A_D$	$C_{jD} = C_{jDB}A_D + 1/2C_{BCt}$

According to Eq.(5.7), R_{ON} is expressed as:

$$R_{ON} = \frac{1}{\mu C_{ox} \cdot \frac{W}{L} \cdot (v_{GS} - V_T)} \qquad (5.17)$$

For SI filters, it is important that R_{ON} be small in order to not interfere with charge transfer. In addition, for a given switch, the designer must set $W \times L$ such that $R_{ON}C_T \le \eta T$, where C_T is the total capacitance connected to the switch's source and drain terminal, $\eta < 0.5$ is the duty cycle for the clock phase, and ηT is the time allowed for to C_T charge. In order to make R_{ON} small, W/L is required to be large. At the same time, we seek to make the parasitic capacitances in Fig.5.10 small, which requires the area of CMOS switch ($W \times L$) small. Therefore the minimum channel length is often chosen for transistor switches.

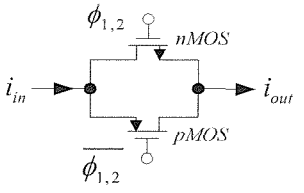


Fig.5.11 CMOS switch

In this circuit design, CMOS switch is used, Fig.5.11, where the designer can match the channel charges from the *P*- and *NMOS* switch transistors to cancel each other when CMOS switch is *OFF*. Besides the cancellation of clock-feedthrough effect, CMOS structure reduces R_{ON} and extends the input voltage range from $(V_{GS}-V_T)$ to V_{GS}.

5.4.3 Delay cell

The current delay is realized by cascading two SI memory cells, which are controlled by two non-overlap clock phases. According to Chapter 2, 2nd-generation memory cell has no mismatch problem theoretically, and are in some sense advantageous over 1st-generation memory cell. However, since two 2nd-generation memory cells are needed to provide the required isolation between input and output of delay cell, the mismatch errors between these two memory cells in delay cell are still evident. In addition, the basic 2nd-generation SI delay cell has large internal transient glitches that cause large linear and nonlinear errors, so it has higher THD than 1st-generation circuits [34]. Therefore, the 1st-generation SI circuits with improved clock-feedthrough cancellation are used in this transistor-level circuit design.

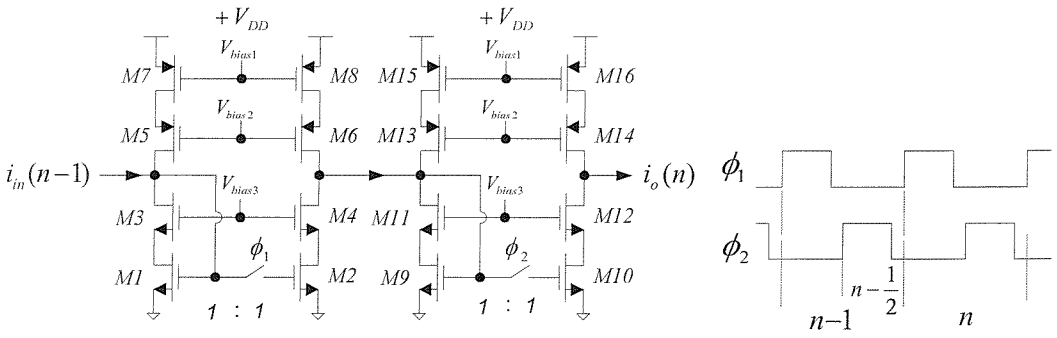


Fig.5.12 1st-generation cascode delay cell

As shown in Fig.5.12, the cascode current mirror memory cell is used to improve its performance, as well as to obtain error-free connection with wave adaptors, which are realized by the same cascode current mirrors.

5.5 Design and implementation of elliptic SI wave filters

In this section, the design of 3rd-order SI wave filter is described and its building blocks are realized using practical SI transistor-level circuits.

5.5.1 Design of SI elliptic wave filter

The chosen design example is 3rd-order elliptic lowpass filter, which is discussed in Chapter 2. Its specifications are: passband frequency $f_p = 0.1MHz$, passband ripple $A_{\max} = 0.177dB$, sampling frequency $f_{CLK} = 1MHz$. For convenience, its LC prototype and wave filter are repeated in Fig.5.13.

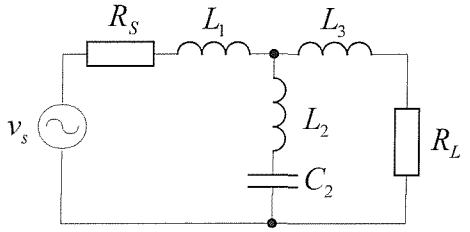


Fig.5.13 (a) The 3rd-order LC elliptic filter

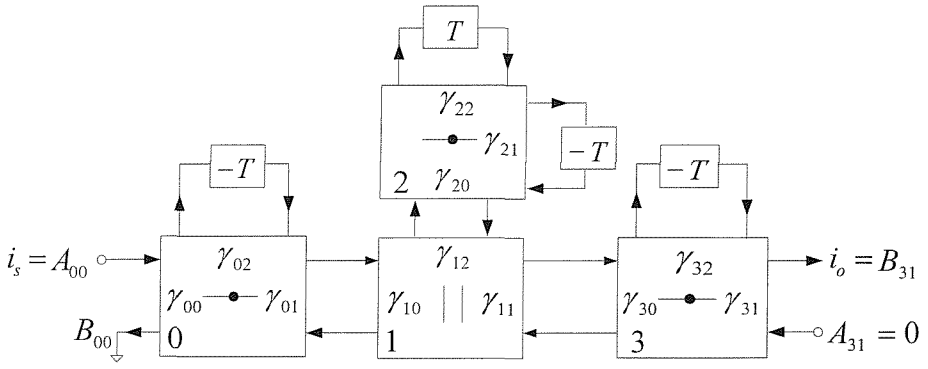


Fig.5.13 (b) Its equivalent 3rd-order elliptic SI wave filter

Using wave synthesis technique described in Chapter 2, wave adaptor coefficients are calculated as:

$\gamma_{00} = 0.225$, $\gamma_{01} = 1$, $\gamma_{02} = 0.775$, $\gamma_{10} = 0.11$, $\gamma_{11} = 1$, $\gamma_{12} = 0.89$,

$\gamma_{20} = 1$, $\gamma_{21} = 0.447$, $\gamma_{22} = 0.553$, $\gamma_{30} = 0.2$, $\gamma_{31} = 0.4$, $\gamma_{32} = 1.4$

Based on 1st-generation delay cells [14,86] and the wave adaptors of [28], Fig.5.14 gives SI implementation of the 3rd-order wave filter.

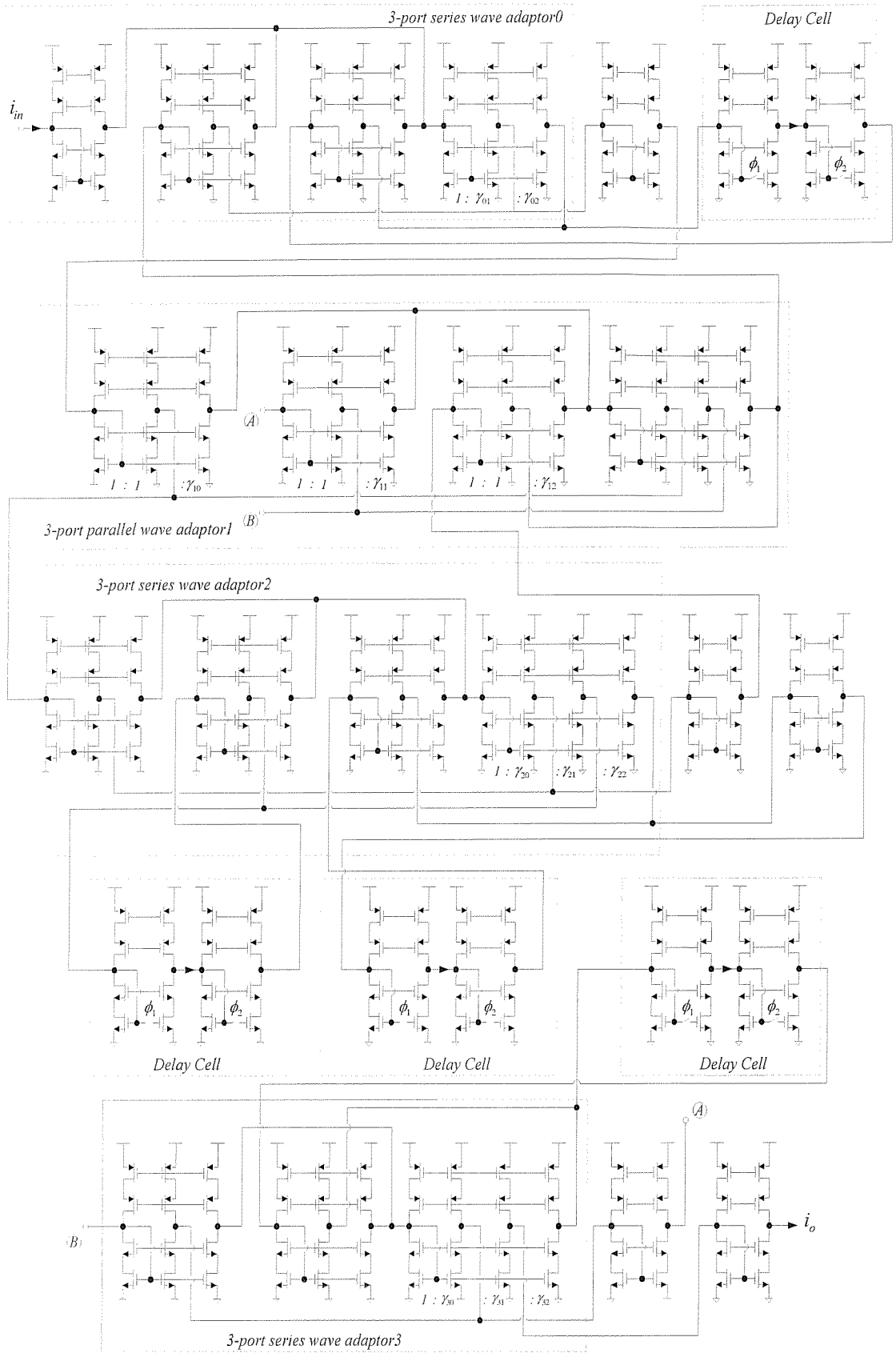


Fig.5.14 Transistor-level circuit of 3rd-order SI wave filter

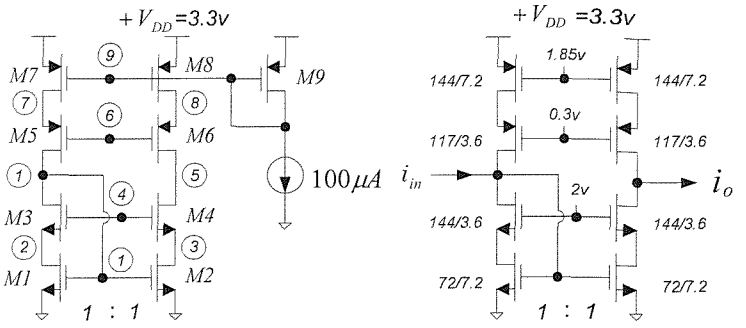


Fig.5.15 1st-generation cascode current mirror

5.5.2 Transistor-level design of SI elliptic wave filter

The task of this design phase is to size the transistors in current mirror, memory cells and switches and determine their operating bias to produce the specified filter performance. Considering the minimum value of wave adaptor coefficients is $\gamma_{10} = 0.11$, the aspect ratio of unit current mirror (W/L) is set to be 10 in order to reduce the mismatch errors in current mirrors with small gain factors. From Table5.2, the following transistor parameters are derived:

NMOS transistor: $\mu C_{ox} = 80\mu A/V^2$ $V_{T0} = 0.74V$

PMOS transistor: $\mu C_{ox} = 27\mu A/V^2$ $V_{T0} = -0.74V$

The transistor-level design of cascode current mirror with $3.3V$ voltage supply and $100\,\mu A$ bias current, Fig.5.15, is given as follows:

The first step is to calculate the gate-source voltage of $M1$ according to aspect ratio of unit current mirror.

$$M1:\ 100 = \frac{80}{2}\cdot(W/L)_1\cdot(V_{GS1}-0.74)^2,\ (W/L)_1=10 \Rightarrow V_{GS1} = 1.25V \quad (5.18)$$

To keep $M1$ in saturation region:

$$V_{DS1} > V_{GS1} - V_{T0} = 0.5V \Rightarrow V_2 > 0.5V \quad (5.19)$$

The next step is to decide aspect ratio of $M3$:

Setting the bias voltage at node ④ = $2V$ and $M3$ is often kept at the edge of triode region for large dynamic range.

$$M3:\ V_{DS3} \approx V_{DSsat} \approx 0.25 \Rightarrow V_2 = 1V \quad (5.20)$$

$$100 = \frac{80}{2}\cdot(W/L)_3\cdot(V_{GS3}-0.74)^2 \Rightarrow (W/L)_3 = 40 \quad (5.21)$$

Then the gate-source voltage of *M9* is calculated:

Setting $(W/L)_9$=20, the DC voltage of node ⑨ can be calculated from transistor *M9*:

$$M9:\ 100 = \frac{27}{2}\cdot(W/L)_9\cdot(V_{GS9}-0.74)^2 \Rightarrow V_9 = 1.95V \qquad (5.22)$$

To keep *M9*, *M7*, or *M8* in saturation region

$$V_{DS7} > V_{GS7} - V_{T0} = 0.6V \qquad (5.23)$$

In hand-calculation, DC voltage on node ⑦ is assumed to *1.95V*.

Finally the aspect ratio of *M5* is decided:

The drain voltage of *M5* is: $V_{DS5} = V_7 - V_1 \approx 0.7V.$ (5.24)

In order to keep *M5* in the saturation region, $V_{DS5} \geq (V_{GS5} - V_T)$, so the bias voltage at node ⑥ is set to be *0.3V*. For transistor *M5* considering its body effect ($V_T \approx 1\,V$):

$$100 = \frac{27}{2}\cdot(W/L)_5\cdot(V_{GS5}-V_T)^2 \Rightarrow (W/L)_3 = 17.5 \qquad (5.25)$$

According to discussion in section 5.4.1, the minimum length of mirror transistors (*M1, M2, M7* and *M8*) is set to be 7.2 μm for reducing mismatch errors. The minimum length of cascode transistors (*M3, M4, M5* and *M6*) is set to be 3.6 μm for higher bandwidth. Level-2 model, which represents 1.2 μm CMOS p-well process, is used to evaluate the circuit performance through PSPICE. The bias voltage and aspect ratio of cascode transistors (*M5* and *M6*) are adjusted to achieve the accurate current mirror. The complete cascode current mirror with the aspect ratios is also given in Fig.5.15, where the bias circuit should be designed to provide the bias voltages. The DC voltages of cascode current mirror, which obtained from PSPICE simulation, are listed as:

Table 5.4 DC voltage of cascode current mirror

Node	*1*	*2*	*3*	*4*	*5*	*6*	*7*	*8*	*9*
voltage	*1.32V*	*1V*	*1V*	*2V*	*1.32V*	*0.3V*	*1.9V*	*1.9V*	*1.85V*

The small signal or *AC* characteristics of cascode current mirror is analysed as follows:

For transistor *M1*: $g_{m1} = \frac{2I_{DS}}{(V_{GS1}-V_{T0})} = 345\,\mu A/V$ (5.26)

Drain-source resistance: $r_{DS1} = 1/\lambda I_{DS}$, $\lambda = 0.037\ V^{-1} \Rightarrow r_{DS1} = 27kohm$ (5.27)

Gate-source capacitance $C_{GS1} = C_{GS0} + 2/3C_{oxt} = 0.6pF$ (5.28)

where $C_{GS0} = CGS0 \times W = 4.3 \times 10^{-4} \times 72 = 0.031pF$

$$C_{oxt} = C_{ox} WL_{eff} = 1.7 \times 10^{-3} \times 72 \times (7.2 - 2 \times 0.15) = 0.845pF$$

The input resistance of cascode current mirror is like simple diode-connected transistor and given as:

$$R_{in} = 1/g_{m1} = 2.9kohm \quad (5.29)$$

In cascode current mirror, the dominant pole is created on the node ① and given as:

$$f_d = \frac{1}{2\pi \cdot R_{in} \cdot (C_{GS1} + C_{GS2})} = 45.7MHz \quad (5.30)$$

The output resistance of cascode current mirror is given as:

$$R_{out} \approx (g_{m4} \cdot r_{DS4} \cdot r_{DS2})/2 \approx 561kohm \quad (5.31)$$

where $g_{m4} = \frac{2I_{DS}}{(V_{GS4} - V_{T0})} = 1538\,\mu A/V$, and $r_{DS2} = r_{DS4} = 27kohm$

Since the input resistance is low, the dynamic range of cascode current mirror is large. For example, if voltage range on node ① is $0.1V$, the dynamic range of input current is $35\,\mu A$. PSPICE simulation on the cascode current mirror, which is fed with sinusoidal signal with amplitude of $10\,\mu A$, is shown in Fig.5.16. It clearly shows the performance of current mirrors.

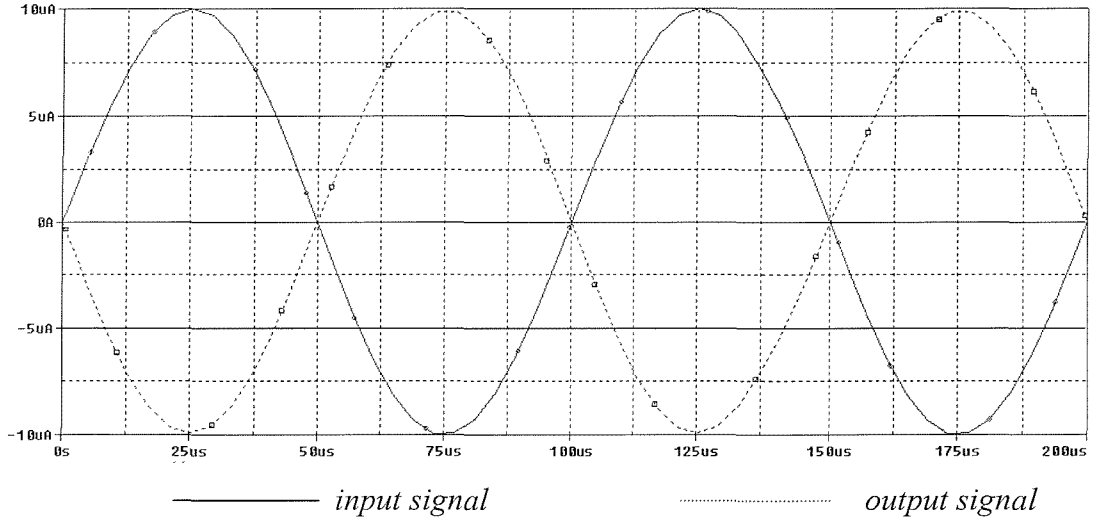


Fig.5.16 Simulation results of cascode current mirror with unity gain

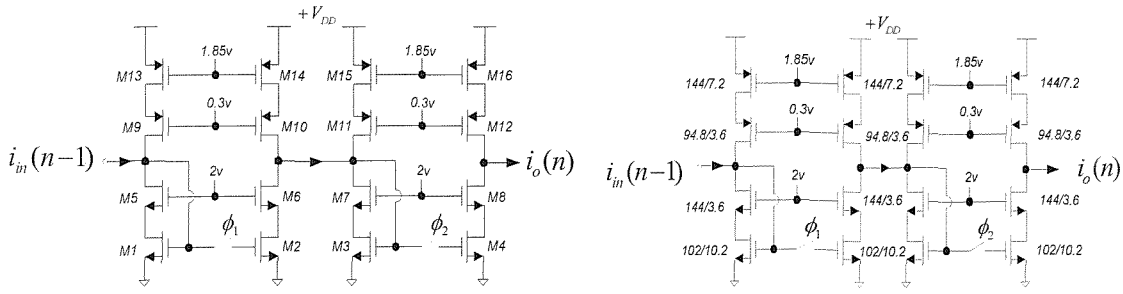


Fig.5.17 1st-order cascode delay cell

The transistor-level design procedure of delay cell is similar to cascode current mirror, and the dimensions of mirror transistors (*M1, M2, M3* and *M4*) are enlarged in order to hold voltage V_{GS} during the switch-off clock phase and reduce clock-feedthrough errors in the output current, $i_o(n)$. The transistor-level circuit of the 1st-order cascode delay cell is given in Fig.5.17.

The gate-source capacitance of mirror transistor (*M1, M2, M3* and *M4*) is:

$$C_{GS} = C_{GS0} + 2/3C_{oxt} = 1.6pF \qquad (5.32)$$

where $C_{GS0} = CGS0 \times W = 4.3 \times 10^{-4} \times 102 = 0.44pF$

$$C_{oxt} = C_{ox} WL_{eff} = 1.7 \times 10^{-3} \times 102 * (10.2 - 2 \times 0.15) = 1.72pF$$

The input resistance of delay cell is same with cascode current mirror: $R_{in} = 2.9kohm.$ According to Eq.(5.12), the constant $\tau \approx R_{in} \cdot C_{GS} \approx 4.64ns << 1/2f_{CLK} = 0.5\mu s$ and the settling error is negligible. As discussed in section 5.4, CMOS switch with minimum length is chosen, as shown in Fig.5.18.

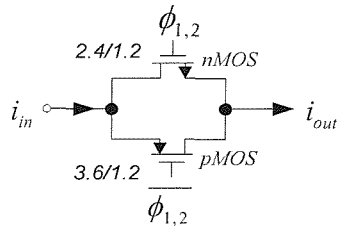


Fig.5.18 CMOS switch with aspect ratio

In order to reduce clock-feedthrough effect, *P-* and *NMOS* switch transistors are designed to match their channel charges. According to section 5.2, the mobile charge in switch transistor is:

$$Q_m = C_{ox} \cdot \frac{W}{L} \cdot (V_{GS} - V_T) \qquad (5.33)$$

Due to difference of C_{ox} in *P*- and *NMOS* switch transistors, different aspect ratios are set to match positive and negative charges, shown in Fig.5.18. The *ON*-resistance is calculated according to Eq.(5.6):

$$R_{ON} \approx R_{ONnmos} // R_{ONpmos}$$

$$\approx \frac{1}{2} \cdot \frac{1}{\mu C_{ox}(W/L) \cdot (V_{GS} - V_T)} \approx \frac{1}{2} \cdot \frac{1}{80 \cdot (2.4/1.2) \cdot (5 - 0.75)} \approx 0.74kohm \qquad (5.34)$$

The total capacitance connected to the switch's source and drain terminal, C_T, is often less than *5pF*, so the condition $R_{ON} C_T \leq \eta T = \eta / f_{CLK}$ ($\eta < 0.5$) can be satisfied. The PSPICE simulation on 1st-order cascode delay cell is shown in Fig.5.19. It is clear that the output signal is delayed by one clock period as predicted without much distortion.

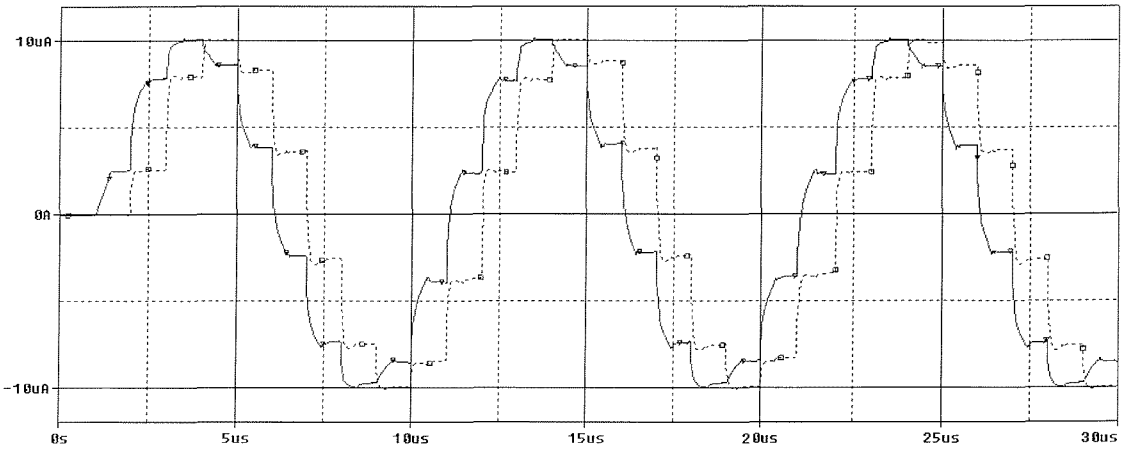


Fig.5.19 Simulation results on 1st-order cascode current mirror

So far, unit current mirror and delay cell have been designed. The wave adaptor coefficients are realized through aspect ratio of current mirrors, as listed in Table5.5.

Table 5.5 Coefficients and *W/L* of 3rd-order SI wave filter

Port	γ_{ij}	*W/L*
γ_{00}	*0.225*	*16.2/7.2*
γ_{01}	*1*	*72/7.2*
γ_{02}	*0.775*	*55.8/7.2*
γ_{10}	*0.11*	*7. 92/7.2*
γ_{11}	*1*	*72/7.2*
γ_{12}	*0.89*	*64.1/7.2*
γ_{20}	*1*	*72/7.2*
γ_{21}	*0.447*	*32.2/7.2*
γ_{22}	*0.553*	*39.8/7.2*
γ_{30}	*0.2*	*14.4/7.2*
γ_{31}	*0.4*	*28.8/7.2*
γ_{32}	*1.4*	*100.8/7.2*

Other transistors in current mirror have $W/L=72\mu m/7.2\mu m$

5.5.3 PSPICE simulation of SI wave filter

The overall transistor-level circuit of the 3rd-order SI wave filter is simulated through PSPICE. Time-domain and frequency-domain response can be obtained for continuous-time circuits using PSPICE. But for discrete-time systems like SI circuits, PSPICE simulation on transistor-level circuit can only be run in the time domain to produce transient analysis. The AC analysis can not be made because SI circuits generally exhibit periodic time-varying behaviour, which is related to its clock operation [83]. In this simulation, the frequency response is obtained through performing transient analysis with sinusoidal input signal of different frequencies and measuring the magnitude difference between input and output signal.

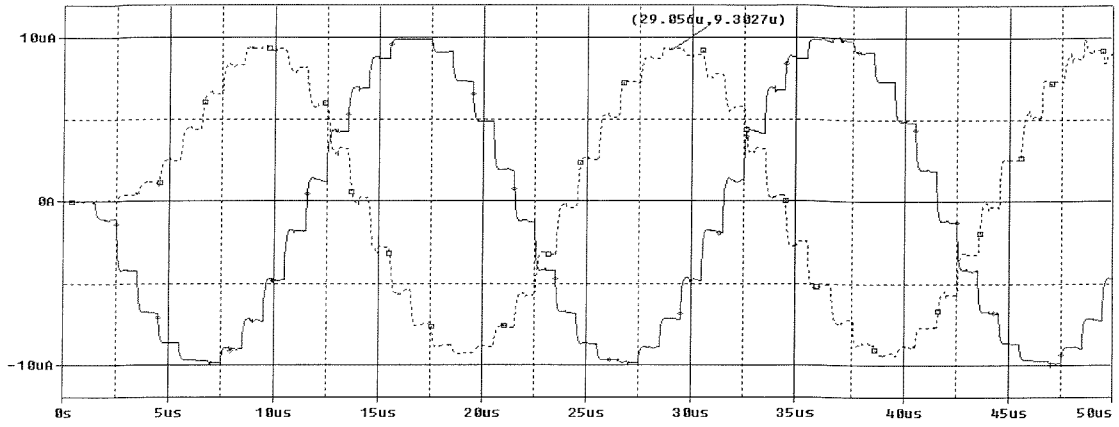


Fig.5.20 (a) Transient analysis on SI wave filter when fed with *50kHz* sinusoidal signal

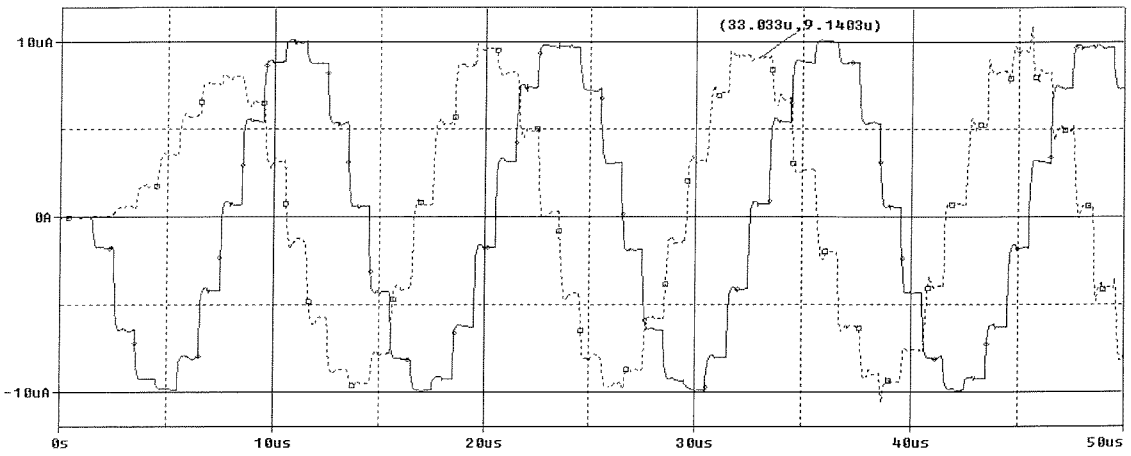


Fig.5.20 (b) Transient analysis on SI wave filter when fed with *80kHz* sinusoidal signal

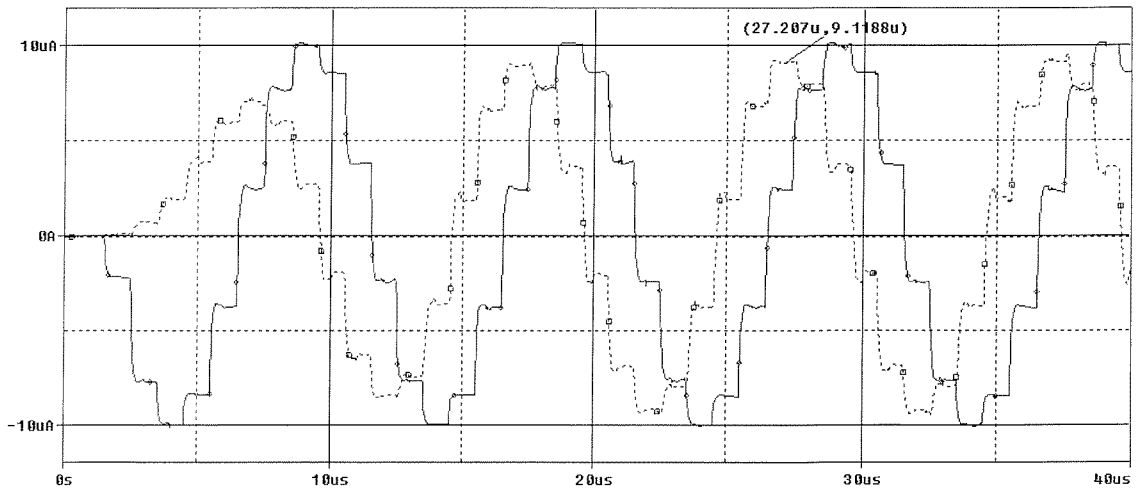


Fig.5.20 (c) Transient analysis on SI wave filter when fed with *100kHz* sinusoidal signal

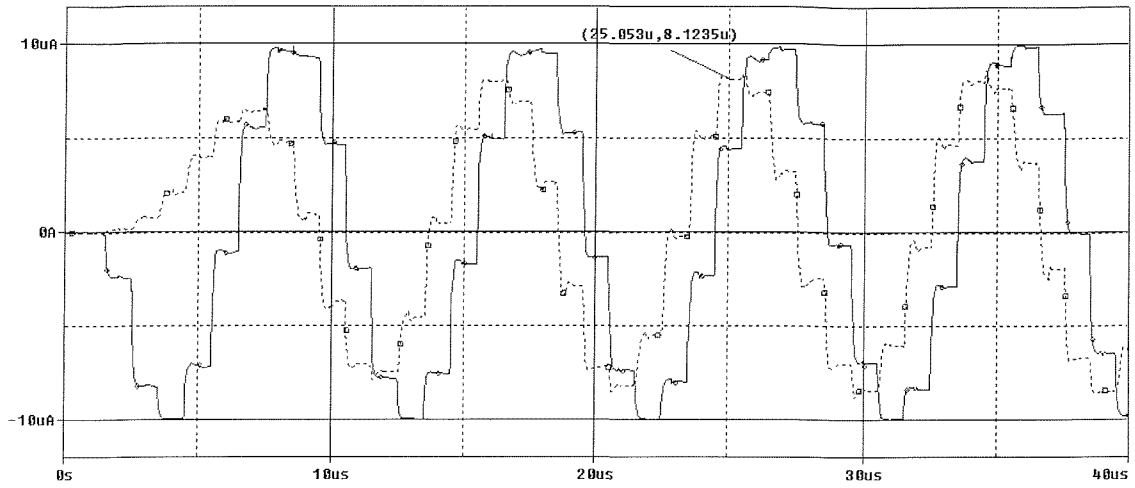


Fig.5.20 (d) Transient analysis on SI wave filter when fed with *110kHz* sinusoidal signal

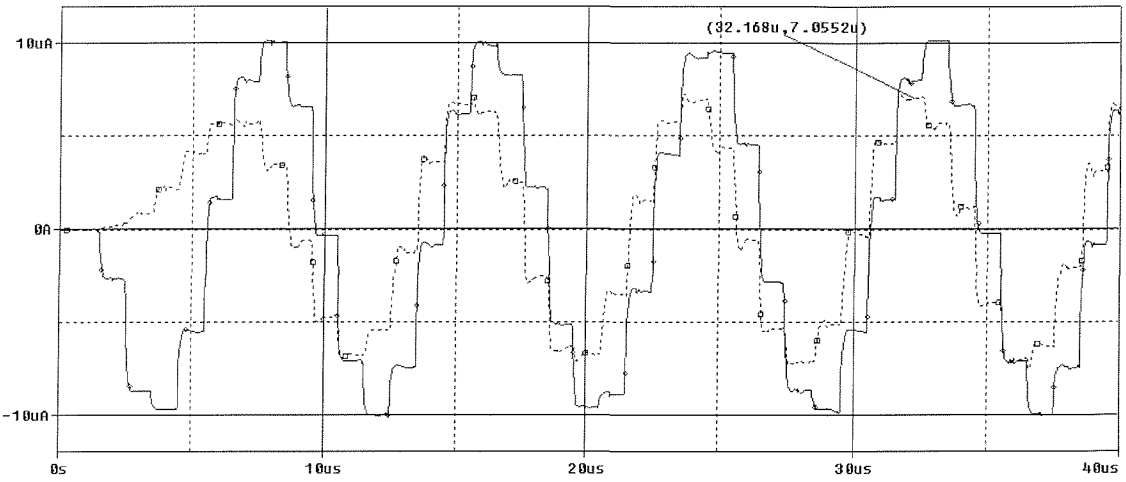


Fig.5.20 (e) Transient analysis on SI wave filter when fed with *120kHz* sinusoidal signal

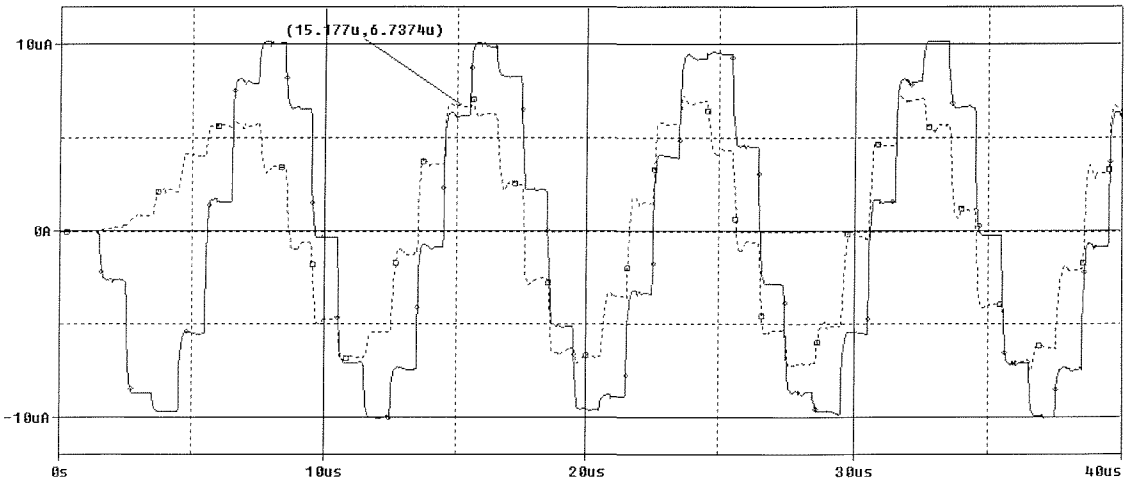


Fig.5.20 (f) Transient analysis on SI wave filter when fed with *150kHz* sinusoidal signal

Fig.5.20 shows the performance of SI wave filter, which is fed with *50kHz*, *80kHz*, *100kHz*, *110kHz*, *120kHz* and *150kHz* sinusoidal signals. The time-domain response of different frequency input signal is listed in Table5.6.

Table 5.6 The performance of 3rd-order elliptic SI wave filter

frequency	*50kHz*	*80kHz*	*100kHz*	*110kHz*	*120kHz*	*150kHz*
magnitude	*-0.63dB*	*- 0.78dB*	*-0.8dB*	*-1.8dB*	*-3dB*	*-3.43dB*

As expected, the magnitude of input signal with frequency higher than passband, $f_p = 100kHz$, is significantly reduced. This simulation frequency response of SI wave filter corresponds to the theoretical response, except that the simulation response exhibits level shift (*-0.63dB*) in the passband. The combination of non-ideal characteristics is responsible for the level shift in the passband. The performance of SI wave filter circuit is summarized in Table 5.7. It indicates the validity of transistor-level design of SI wave filter.

Table 5.7 Performance summary of SI wave filter

Performance characteristic	*Simulation value*	*Theoretical value*
Clock frequency	*1MHz*	*1MHz*
Passband edge	*102kHz*	*100kHz*
Stopband edge (-3dB)	*152kHz*	*142.5kHz*
Passband ripple	*0.2dB*	*0.177dB*
Power consumption	*36.8mW*	*24.1mW*

5.6 Design and implementation of SI group delay wave equalizers

Since the 3rd-order SI elliptic wave filters have non-linear phase or non-flat group delay response, which results in excessive overshoot in the filter's step response, the group delay equalizer (allpass filter) is required to cascade with elliptic filters for improving their time domain response. The design method for group delay wave equalizer was given in Chapter 4. First, the group delay response of 3rd-order SI elliptic wave filter is obtained through SCNAP4 simulation. Secondly, optimisation process, based on

MATLAB program, is made to derive the allpass transfer function, whose phase response (or group delay response) is used to compensate for the poor phase characteristics of SI elliptic wave filter. In this section, the 3rd-order group delay equalizer is chosen and its transfer function is:

$$H(z) = -\frac{z^{-3} + a_1 z^{-2} + a_2 z^{-1} + a_3}{a_3 z^{-3} + a_2 z^{-2} + a_1 z^{-1} + 1} \tag{5.35}$$

where a_1 = -0.3314, a_2 = -0.686, a_3 = 0.38

Thirdly, *LC* network is synthesized from the transfer function and implemented using wave structure, shown in Fig.5.21.

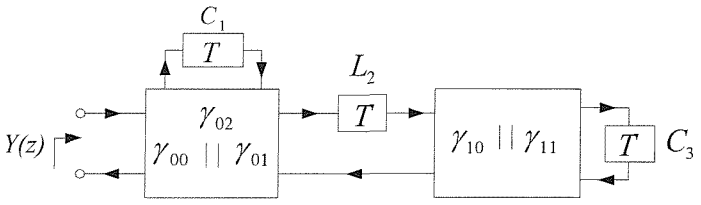


Fig.5.21 Wave structure of 3rd-order *LC* ladder network

The wave adaptor coefficients are calculated using wave synthesis technique:

γ_{00}=1.0536, γ_{01}=0.838, γ_{02}=0.1084, γ_{10}=0.1314, γ_{11}=1.8686

Finally, the overall SI wave equalizer circuit architecture is obtained. Its block diagram and transistor-level circuit, which employs 1st-generation current mirror and delay cells, are shown in Fig.5.22. The block '*CM(-1)/(-2)*' in Fig.5.22(a) means current mirror with two output: *(-1)* and *(-2)*, corresponding to Fig.4.1 .

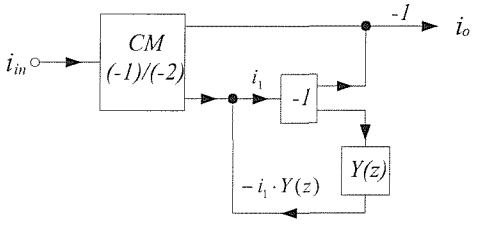


Fig.5.22 (a) Block diagram of 3rd-order SI wave equalizer

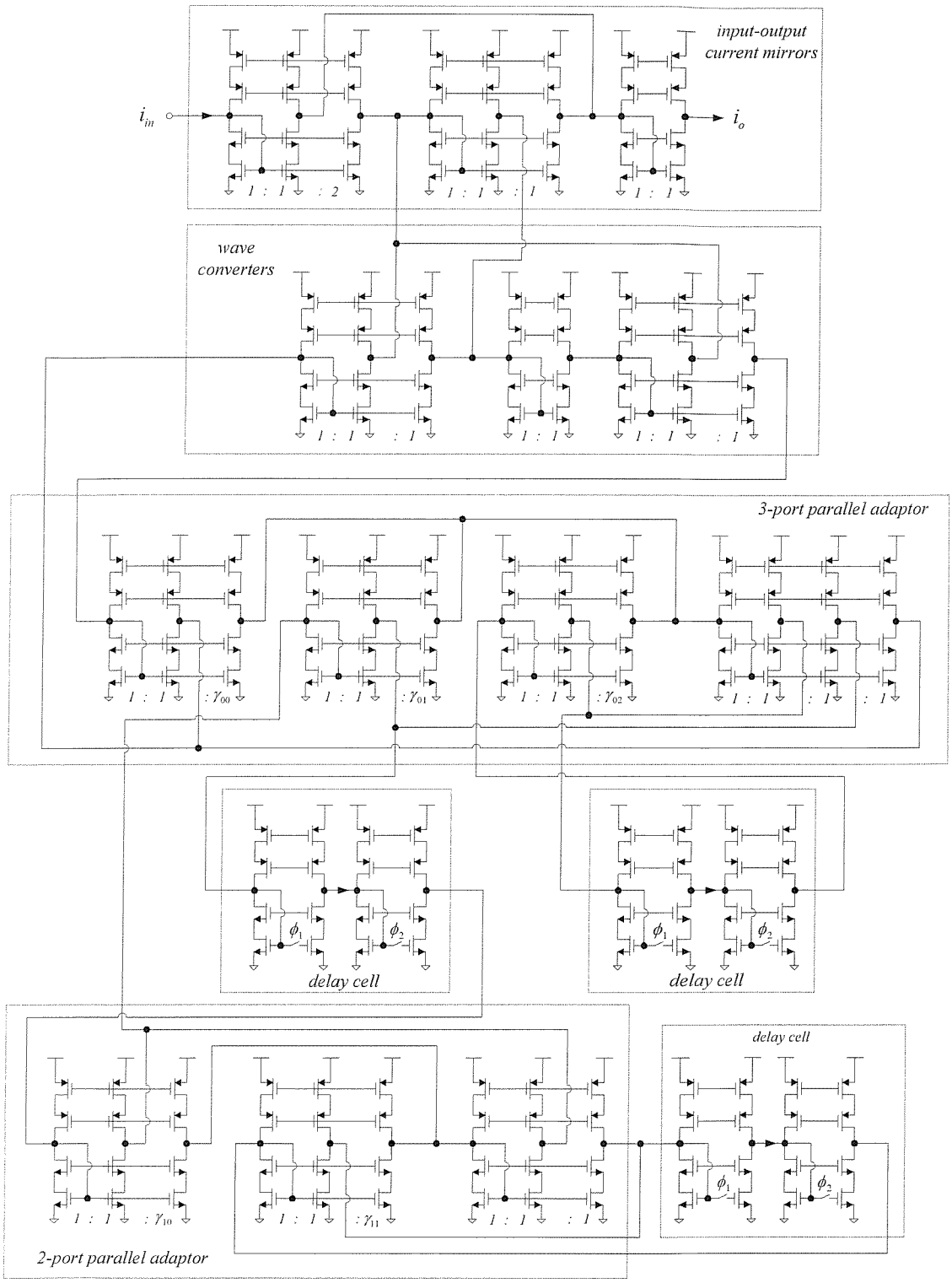


Fig.5.22 (b) Transistor level circuit of 3rd-order SI wave equalizer

Since the input to wave block *Y(z)* is characterized as wave quantities (*A* and *B*), wave converter is added into Fig.5.22(b) for converting current-mode signal in allpass circuit architecture into wave quantities of block *Y(z)*. Different aspect ratios of current

mirrors are used to realize wave adaptor coefficients in the 3rd-order SI wave equalizer, as listed in Table 5.8.

Table 5.8 Coefficients and *W/L* of 3rd-order SI wave equalizer

Port	γ_{ij}	*W/L*
γ_{00}	*1.0536*	*76/7.2*
γ_{01}	*0.838*	*60.3/7.2*
γ_{02}	*0.1084*	*7.8/7.2*
γ_{10}	*0.1314*	*9.5/7.2*
γ_{11}	*1.8686*	*134.5/7.2*

Other transistors in current mirror have *W/L=72μm/7.2μm*

Using typical 1.2μm CMOS process parameters, level 2 transistor models, bias current of 100μA, and V_{DD}=3.3V, Fig.5.23, trace (a) shows PSPICE step response of the 3rd-order elliptic SI wave filter when it is driven by $10\,\mu A$ input step signal. The response has almost 15% overshoot in this case. Trace (b) shows the same filter step response but in this case the 3rd-order SI wave equalizer circuit discussed earlier has been cascaded with the filter. It can be seen that the SI wave equalizer has resulted in reducing the amount of overshoot present in the filter step response by more than 50%. The details of PSPICE program on SI wave filters with group delay equalizers are given in Appendix E.

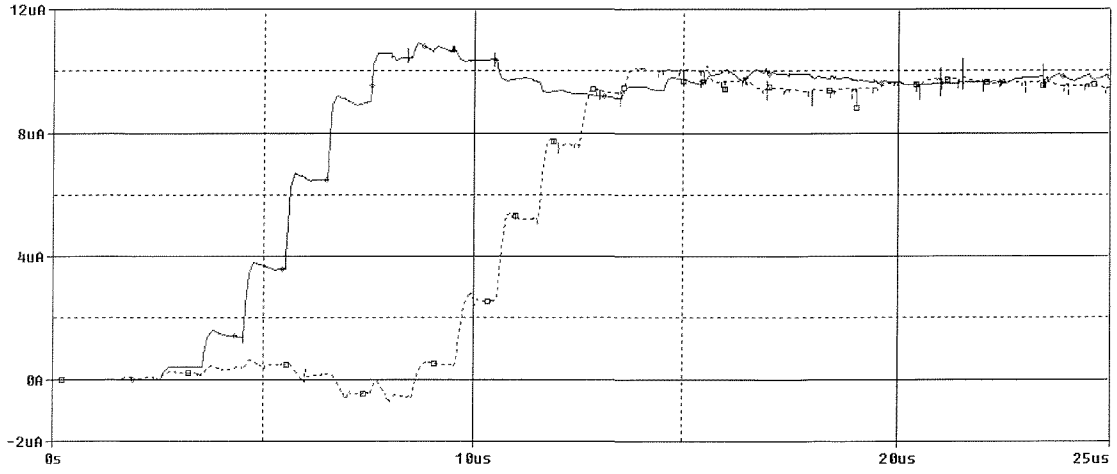


Fig.5.23 Step response of the filter and filter cascaded with 3rd-order SI wave equalizer

(trace *a*: ———— trace *b*: .....)

5.7 Clock-feedthrough effects on the performance of SI wave filters

In Chapter 3, the non-ideal performances of SI wave filters due to mismatch and clock-feedthrough have been analysed using *MATLAB*. It has been identified that clock-feedthrough is the main factor to degrade the frequency response of SI wave filters. The purpose of this section is to further validate the *MATLAB* simulation on clock-feedthrough voltages in Chapter 3. In order to investigate the effects of clock-feedthrough on the practical circuits of SI wave filters, NMOS switches are required to model the clock-feedthrough voltages, Fig.5.24.

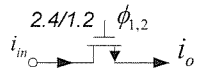


Fig.5.24 NMOS switch

The parameters of MOST in Table 5.2 is repeated as follows:

$C_{ox} = 1.7\times10^{-3}\,pF/\mu m^2$, $C_{ol} = 430pF/m$, γ=0.54, $V_{T0} = 0.74V$, $\alpha = 0.5$

$I_B = 100\mu A$, $\beta_n = 400\mu A/V^2$, V_H =5V, V_L =0V, $i_{in}/I_B = 0.1$,

$C_{SW} = 3.264\times10^{-3}\,pF$, C_{GS} =1.18pF, $C_{OL} = 7.44\times10^{-4}\,pF$

$(W/L)_{SW} = 2.4\mu m/1.2\mu m$, $(W/L) = 102\mu m/10.2\mu m$

According to Eq.(3.14), the clock-feedthrough voltage is calculated as:

$$|\Delta v_f| = k_1\sqrt{1+\frac{i_{in}}{I_B}} + k_2 = 4.68mV \qquad (5.36a)$$

where k_1 and k_2 can be written as:

$$k_1 = -\alpha\cdot\frac{C_{SW}}{C_{GS}}(1+\frac{\gamma}{3})\sqrt{\frac{I_B}{\beta_n}},$$

$$= -0.5\cdot\frac{0.003264}{1.18}\cdot(1+0.54/3)\cdot\sqrt{\frac{100}{400}} = -0.816mV \qquad (5.36b)$$

$$k_2 = \alpha\cdot\frac{C_{SW}}{C_{GS}}[V_H-(2+\frac{\gamma}{3})\cdot V_T]+\frac{C_{OL}}{C_{GS}}[V_H-V_L]$$

$$= 0.5\cdot\frac{0.003264}{1.18}\cdot[5-(2+\frac{0.54}{3})\cdot0.74]+\frac{7.44\times10^{-4}}{1.18}\cdot5 = 6.26mV \qquad (5.36c)$$

Due to the *N*-channel switch, the clock-feedthrough voltage Δv_f is $-4.68mV$. PSPICE simulations are made on the SI wave filter's transistor-level circuit (Fig.5.14) with NMOS switch, Fig.5.25.

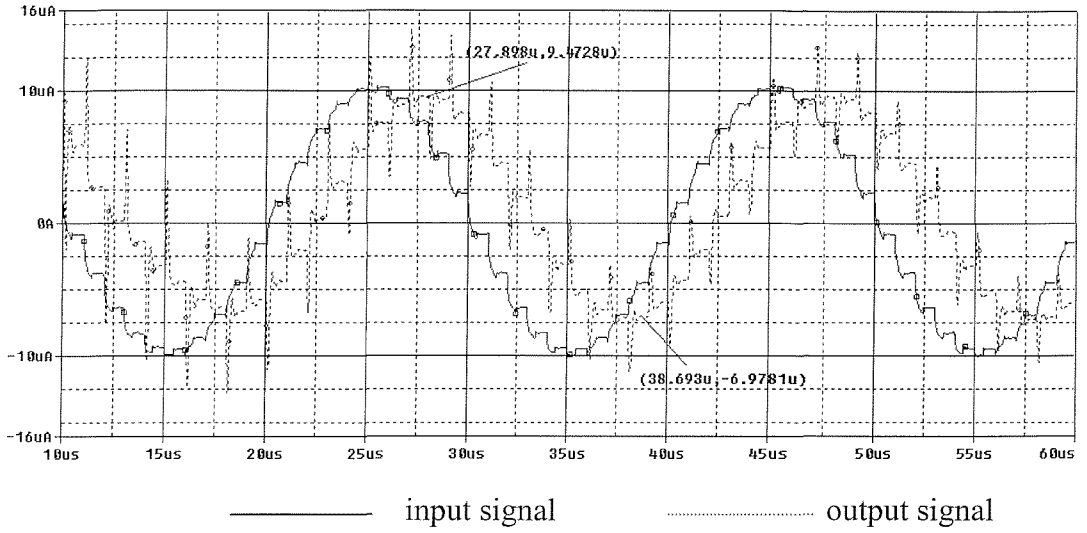


Fig.5.25 (a) Transient analysis on SI wave filter in the presence of clock-feedthrough when fed with *50kHz* sinusoidal signal

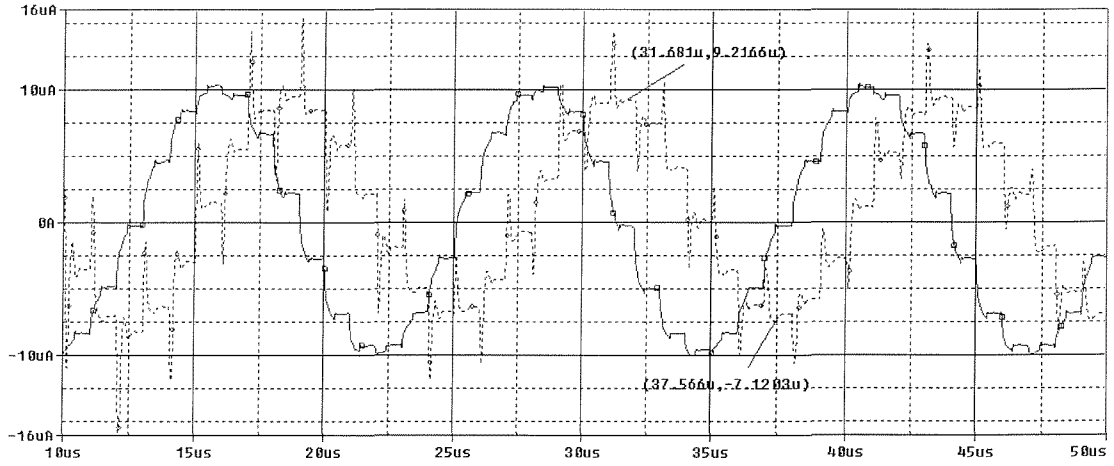


Fig.5.25 (b) Transient analysis on SI wave filter in the presence of clock-feedthrough when fed with *80kHz* sinusoidal signal

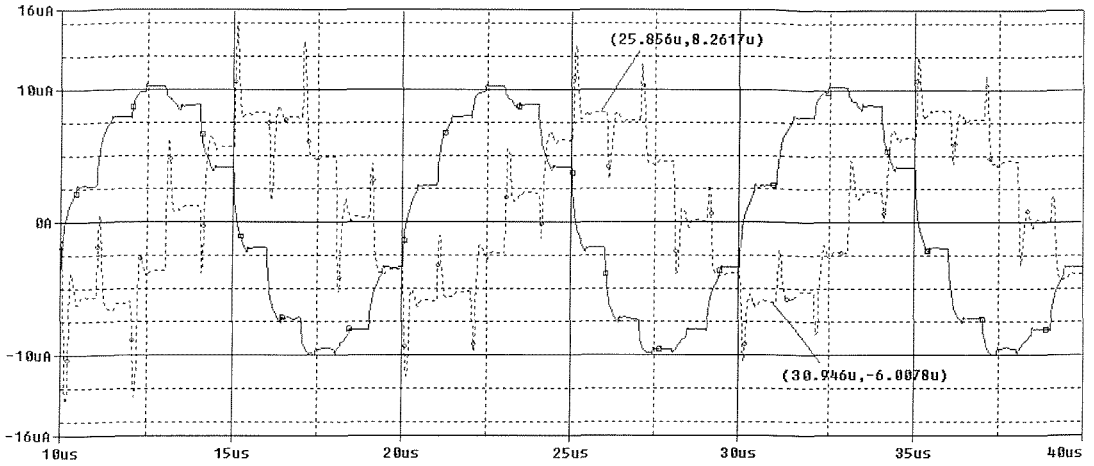


Fig.5.25 (c) Transient analysis on SI wave filter in the presence of clock-feedthrough when fed with *100kHz* sinusoidal signal

Compared with the simulation results on the circuits with CMOS switches (Fig.5.20), the magnitude response in the passband of this filter is reduced by 1.78dB due to the clock-feedthrough voltages. It agrees with the theoretical analysis of the clock-feedthrough effects on the performance of filters in the Chapter 3.

5.8 Concluding remarks

This chapter outlines the transistor-level circuits of SI wave filters and group delay equalizers. The non-ideal characteristics of SI technology are reviewed, and circuit design techniques, such as cascode circuit and CMOS switch, are used in transistor-level circuit design to reduce their influence on the performance of SI filters and group delay equalizers. Using current-mode signal rather than voltage-mode signal, wave filters and group delay equalizers are realized using SI building blocks. Detailed PSPICE simulation results based on 1st-order cascode SI delay cells and current mirrors have been included. The performance of these transistor-level circuits shows the agreement with the theoretical requirements on SI wave filters and effectiveness of SI wave equalizers in improving step response overshoot of lowpass elliptic SI filters. In addition, the clock-feedthrough effect on the transistor-level circuits of SI wave filters has been investigated. In this chapter, both non-ideal performance analysis of SI filter (Chapter 3) and design method of SI wave equalizer (Chapter 4) have been validated through transistor-level circuit simulations.

Chapter 6

SI Adaptive Wave Filters

6.1 Introduction

So far, the design of SI wave filters and group delay equalizers with fixed characteristics have been presented in Chapter 2,3,4 and 5. Whenever the filter's parameters are required to track time-varying conditions, adaptive filters are an attractive option. This chapter describes new SI adaptive filters based on wave synthesis technique. Section 6.2 gives a brief review on analogue adaptive filters. Section 6.3 proposes a new adaptive wave filter structure. The adaptive algorithm, which can be applied to adaptive wave filters, is described in section 6.4. *MATLAB* simulation and discussion of efficient hardware implementation are included in section 6.5. Section 6.6 provides some concluding remarks.

6.2 Analogue adaptive filters

Adaptive filters have been successfully employed in various applications including digital magnetic storage, seismic data analysis and echo cancellation, and it is likely they will continue to play an important role in future digital communication applications [70]. Although the vast majority of adaptive filters are implemented using digital techniques, analogue adaptive filters have the potential to operate at higher speeds, consume less power and occupy smaller silicon area. Two approaches have been proposed for designing analogue adaptive filters. The first approach is based on the FIR transversal filter structure and direct-form IIR filter structure [82], which are implemented using analogue SI [1,71,72] or SC technology [73]. The advantages of this approach are simplicity and computational efficiency. The second approach is based on filter structures, which are derived from LC ladder prototypes. The main advantages of this approach is that its resultant circuit has low sensitivity and capable of meeting sharp frequency response specifications. The most popular adaptive filter structure derived from LC ladder prototypes is the recursive state-space filter [74,75].

New adaptive wave filter structures, which are based on LC ladder prototypes, will be proposed in this chapter. The wave synthesis technique was originally developed to design digital filters with low sensitivity. It has been demonstrated that wave filter with fixed characteristics can be implemented using OTA-C and SI technology in [25,26,29,30], with [26] later being extended to include programmability in [27]. This research will investigate the explicit design of wave filters for analogue adaptive signal processing.

6.3 New adaptive wave filter structure

For the 3rd-order lowpass LC ladder prototype shown in Fig.6.1(a), wave synthesis technique is used to convert it into wave filter, shown in Fig.6.1(b).

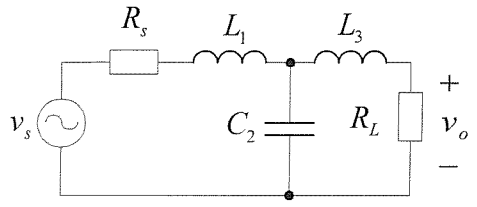


Fig.6.1 (a) 3rd-order *LC* low-pass ladder prototype

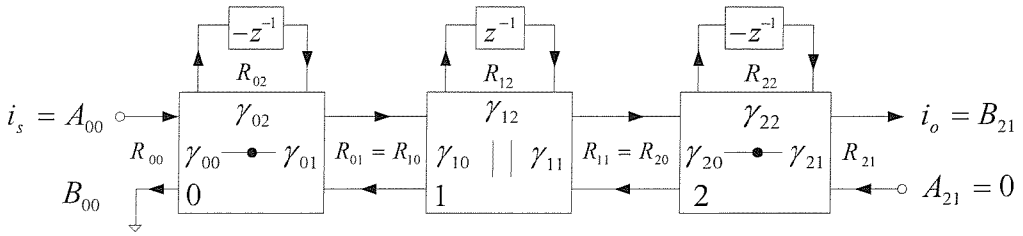


Fig.6.1 (b) Its equivalent wave structure

As discussed in Chapter 2, wave adaptor coefficients γ_{ij} are calculated using the following expressions, which must be satisfied for each *3-port* adaptor:

$$\sum_{j=0}^{2} \gamma_{ij} = 2, \text{ where } i = 0,1,2 \tag{6.1}$$

3-port series adaptors: $\frac{\gamma_{i0}}{R_{i0}} = \frac{\gamma_{i1}}{R_{i1}} = \frac{\gamma_{i2}}{R_{i2}}$, where $i = 0,2$ (6.2a)

3-port parallel adaptors: $\frac{\gamma_{i0}}{G_{i0}} = \frac{\gamma_{i1}}{G_{i1}} = \frac{\gamma_{i2}}{G_{i2}}$, where $i = 1$ (6.2b)

where R_{ij} and G_{ij} are the port resistance and conductance of port j. They are calculated from the LC prototype:

$$R_{00} = R_s = 1, \quad R_{02} = 2L_1 / T, \quad R_{12} = T / 2C_2, \quad R_{22} = 2L_3 / T, \quad R_{21} = R_L = 1$$

And other port resistances are decided by their corresponding wave adaptor coefficients γ_{ij}, which are often chosen to optimise the circuit of analogue wave filter [1,26]. From Eq.(6.2), it can be seen that each set of wave adaptor coefficients corresponds to the passive component (for example, the coefficients, γ_{0j}, j=*0,1,2,* in *wave adaptor0* corresponds to L_1, Fig.6.1).

The input-output relationship of *3-port* wave adaptor is:

$$\text{series adaptors: } \begin{bmatrix} B_{i2} \\ B_{i1} \\ B_{i0} \end{bmatrix} = \begin{bmatrix} 1-\gamma_{i2} & -\gamma_{i2} & -\gamma_{i2} \\ -\gamma_{i1} & 1-\gamma_{i1} & -\gamma_{i1} \\ -\gamma_{i0} & -\gamma_{i0} & 1-\gamma_{i0} \end{bmatrix} \cdot \begin{bmatrix} A_{i2} \\ A_{i1} \\ A_{i0} \end{bmatrix}, \text{ where } i = 0,2 \qquad (6.3a)$$

$$\text{parallel adaptors: } \begin{bmatrix} B_{i2} \\ B_{i1} \\ B_{i0} \end{bmatrix} = \begin{bmatrix} \gamma_{i2}-1 & \gamma_{i1} & \gamma_{i0} \\ \gamma_{i2} & \gamma_{i1}-1 & \gamma_{i0} \\ \gamma_{i2} & \gamma_{i1} & \gamma_{i0}-1 \end{bmatrix} \cdot \begin{bmatrix} A_{i2} \\ A_{i1} \\ A_{i0} \end{bmatrix}, \text{ where } i = 1 \qquad (6.3b)$$

The frequency response of wave filter is dependent on the value of wave adaptor coefficients γ_{ij}. Therefore, the wave filter structure can be made adaptive by updating each set of wave adaptor coefficients (γ_{ij}, *i=0,1,2*) toward their required values. However, when wave adaptor coefficients, for example γ_{00} and γ_{01} in *wave adaptor0*, are adapted, the port resistance R_{01} will change as well according to Eq.(6.4).

$$\frac{\gamma_{00}}{R_{00}} = \frac{\gamma_{01}}{R_{01}}, \text{ where } R_{00}=1 \qquad (6.4)$$

Since *port10* and *port01* are same port, Fig.6.1, this means port resistance R_{10} should be same as R_{01}. Consequently, R_{10} will change with R_{01}, which will result in the variation of *wave adaptor1* coefficients according to Eq.(6.5).

$$\frac{\gamma_{10}}{G_{10}} = \frac{\gamma_{11}}{G_{11}}, \text{ where } G_{10} \text{ is inverse of } R_{10} \qquad (6.5)$$

So if the coefficients in *wave adaptor0* are adapted, it will affect the values of the coefficients in *wave adaptor1*. This conflicts the design of adaptive wave filter, where wave adaptor coefficients are required to be varied independently towards their

required values. Therefore, in order to achieve adaptive wave filters, it is necessary to fix the value of interface port resistance (R_{01} and R_{11} in this example) during the adaptation process. According to Eq.(6.4) and Eq.(6.5), it can be achieved by keeping the corresponding coefficients in each wave adaptor at the fixed ratio during the adaptation process. For example, in order to fix the value of port resistance $R_{01} = m$, *(m=1,2,3...)* in *wave adaptor0*, the wave adaptor coefficients γ_{01} should be kept as $m \cdot \gamma_{00}$ during the *wave adaptor0*'s adaptation process. After making such modification, new series and parallel wave adaptors, which are suited to adaptive signal processing, are developed. Setting *m=1* (it will simplify the adaptive series and parallel wave adaptors) and substituting $R_{01} = R_{11} = m$ into Eq.(6.2), the following relationship is obtained:

$$\gamma_{i0} = \gamma_{i1}, \quad i=0,1,2 \tag{6.6}$$

And the input-output relationship of *3-port* wave adaptor, Eq.(6.3), is simplified as:

$$\text{series adaptors: } \begin{bmatrix} B_{i2} \\ B_{i1} \\ B_{i0} \end{bmatrix} = \begin{bmatrix} 2\gamma_{i0}-1 & 2\gamma_{i0}-2 & 2\gamma_{i0}-2 \\ -\gamma_{i0} & 1-\gamma_{i0} & -\gamma_{i0} \\ -\gamma_{i0} & -\gamma_{i0} & 1-\gamma_{i0} \end{bmatrix} \cdot \begin{bmatrix} A_{i2} \\ A_{i1} \\ A_{i0} \end{bmatrix}, \text{ where } i = 0,2 \tag{6.7a}$$

$$\text{parallel adaptors: } \begin{bmatrix} B_{i2} \\ B_{i1} \\ B_{i0} \end{bmatrix} = \begin{bmatrix} 1-2\gamma_{i0} & \gamma_{i0} & \gamma_{i0} \\ 2-2\gamma_{i0} & \gamma_{i0}-1 & \gamma_{i0} \\ 2-2\gamma_{i0} & \gamma_{i0} & \gamma_{i0}-1 \end{bmatrix} \cdot \begin{bmatrix} A_{i2} \\ A_{i1} \\ A_{i0} \end{bmatrix}, \text{ where } i = 1 \tag{6.7b}$$

According to above relationships, signal flow graphs (SFG) have been derived for the series and parallel wave adaptors, as shown in Fig.6.2.

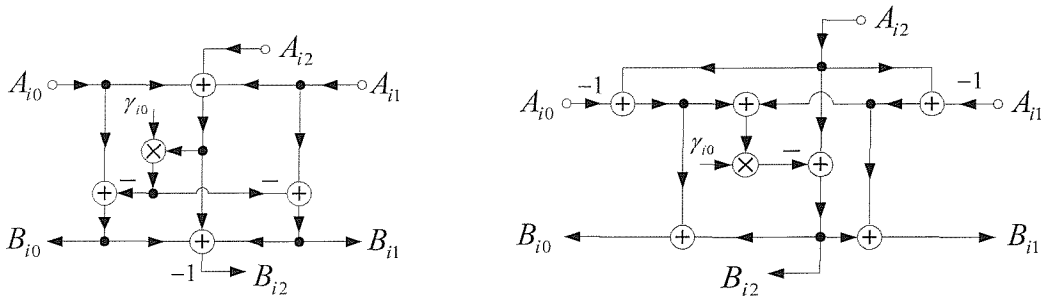


Fig.6.2 (a) SFG for series wave adaptor (b) SFG for parallel wave adaptor

Fig.6.2 shows each wave adaptor requires only one coefficient to be varied for the adaptive operation, for example γ_{00} for *wave adaptor0*. The hardware implementation

based directly on these SFGs would therefore have the advantage of requiring only one variable circuit structure for each wave adaptor.

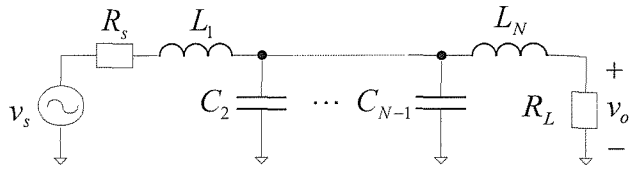


Fig.6.3 (a) *Nth*-order LC ladder filter structure

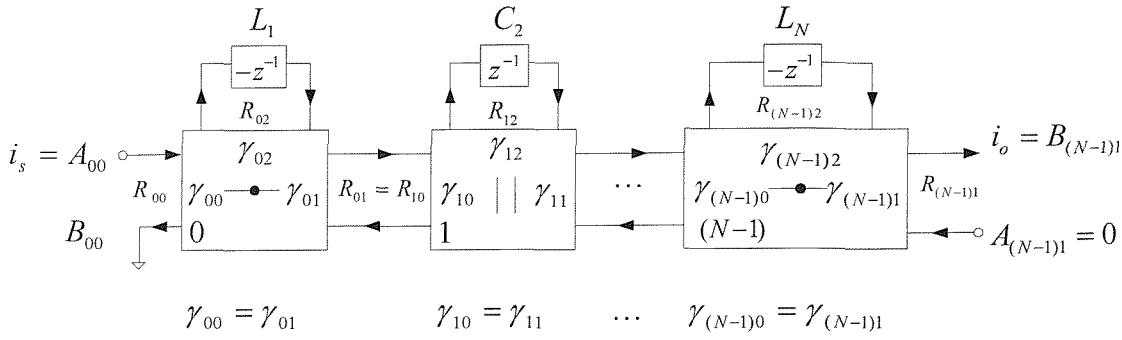


Fig.6.3 (b) *Nth*-order wave adaptive filter

In general, for the *Nth*-order LC ladder network, Fig.6.3, the port resistance and wave adaptor coefficients are given as:

$$R_{i1} = 1,\ \gamma_{i0} = \gamma_{i1},\ i=0,\ 1,\ldots(N\text{-}1) \qquad (6.8)$$

The wave adaptors coefficients in adaptive wave filters, Fig.6.3(b), should satisfy Eq.(6.8) in order to keep the interface port resistance fixed during adaptation process and update each coefficient independently toward its required value. Note this condition is unnecessary for wave filters with fixed characteristics, Fig.6.1(b).

From the definition of wave adaptor coefficients, Eq.(6.2), each set of wave adaptor coefficients corresponds to the passive component (for example, the coefficients, γ_{0j}, $j=0,1,2,$ in *wave adaptor0* corresponds to L_1, Fig.6.1). Therefore, varying wave adaptor coefficient in each wave adaptor corresponds to varying the passive component value in LC reference filter. By updating the adaptor coefficients during adaptation process, the wave adaptive filter behaves like an adaptive LC filter. Furthermore, due to this correspondence, the wave structure has simple stability checks. The stability of the wave structure can be easily guaranteed by ensuring the values of passive components L and C not to be negative. From Eq.(6.1) and (6.8), it

can be shown that the adaptive wave filter structure is stable, provided the wave adaptor coefficients satisfy the following conditions:

$$0<\gamma_{i0}<1,\ i=0,\ 1,\ldots(N-1) \tag{6.9}$$

6.4 Adaptive algorithm

In section 6.3, adaptive wave filter has been introduced. To implement such filters, adaptive algorithm is required to update the filter's wave adaptor coefficients. In this section, we will first explain why the well-known LMS (least-mean-square) algorithm [70,82] is not suitable to the adaptive wave filter, and then we propose a new approach to update the wave adaptor coefficients. The performance criteria used for adaptive filter is the mean-squared error (*MSE*):

$$\varepsilon(p) = E[(d-y)^2] = E[e^2] \tag{6.10}$$

where p is adaptive parameter, d is desired output, y is filter output and *E[]* denotes expectation.

The general iterative update rule is [70,82]:

$$p(k+1) = p(k) - \mu \cdot \nabla_{p(k)}\varepsilon(p(k)) \tag{6.11}$$

where μ is constant parameter determining the rate of adaptation, $p(k)$ is the value of adaptive parameter at *kth* iteration and $\nabla_{p(k)}\varepsilon(p(k))$ is gradient estimation.

Different approaches to obtaining the gradient estimation define different adaptive algorithm. The well-known LMS algorithm takes instantaneous squared error, $e^2(k)$, as its expected value, whose resulting gradient estimation is:

$$\nabla_{p(k)}\varepsilon(p(k)) = \nabla_{p(k)}(e^2(k)) = 2e(k)\cdot\nabla_{p(k)}(d(k)-y(k)) = -2e(k)\nabla_{p(k)}y(k) \tag{6.12}$$

where *d(k)* and *y(k)* are desired output and adaptive filter output at *kth* iteration, respectively.

For the adaptive direct-form IIR filter [82] and adaptive state-space filter [75], the gradient signal $\nabla_{p(k)}y(k)$ is obtained through the sensitivity formulas, and it is expressed in the form of intermediate transfer functions. Additional hardware is required to realize the intermediate transfer functions for producing gradient signal. For example, the 3rd-order transfer function of direct-form IIR filter:

$$H(z) = \frac{Y(z)}{U(z)} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3}}{1 - a_3 z^{-1} - a_2 z^{-2} - a_1 z^{-3}} \tag{6.13}$$

If a_3 is adapted, sensitivity formulas will be used to derive its gradient intermediate function:

$$g_3 = \frac{\partial Y(z)}{\partial a_3} = \frac{b_0 + b_1 z^{-1} + b_2 z^{-2} + b_3 z^{-3}}{(1 - a_3 z^{-1} - a_2 z^{-2} - a_1 z^{-3})^2} \cdot z^{-1} \cdot U(z)$$

$$= \frac{1}{1 - a_3 z^{-1} - a_2 z^{-2} - a_1 z^{-3}} \cdot z^{-1} \cdot Y(z) \qquad (6.14)$$

The direct-form IIR filter structure, where the coefficients a_1, a_2 and a_3 are adapted, are shown in Fig.6.4. Here the output signal g_1, g_2 and g_3 are the gradient signal for a_1, a_2 and a_3, respectively.

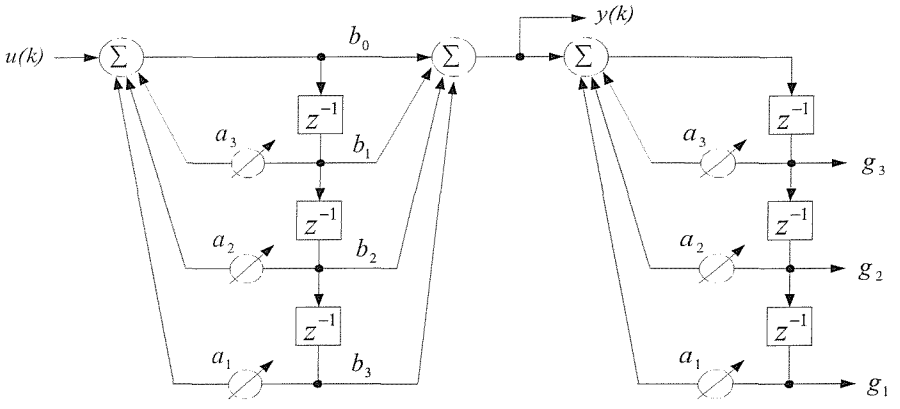


Fig.6.4 Direct-form IIR filter and gradient signal

In adaptive wave filter, the input-output transfer function, $H(z)=i_o(z)/i_s(z)$, is expressed with wave adaptor coefficients [1]. It can be seen from [1] that input-output transfer function, which is expressed with wave adaptor coefficients, contains a lot of complex terms. Therefore, its gradient intermediate transfer functions, which can be obtained through sensitivity formulas, will be complicated and difficult to implement. So an alternative approach should be used to estimate the gradient signal in adaptive wave filter. Recently, a new algorithm for filter adaptation, called the dithered linear search (DLS) technique, has been introduced [85]. The application of DLS algorithm to the adaptive wave filter is investigated now. The term 'dither' here refers to the action of perturbing the wave adaptor coefficients γ_{i0} by intentionally injecting small random (or pseudorandom) signal with zero mean, δ_i. The wave gradient signal is

given by measuring the change of squared-error function with respect to the dithered signal, Eq.(6.15).

$$\frac{\partial \varepsilon}{\partial \gamma_{i0}} = \frac{\varepsilon([\gamma_{00}, \gamma_{10} \cdots \gamma_{i0} + \Delta \cdots]^T) - \varepsilon([\gamma_{00}, \gamma_{10} \cdots \gamma_{i0} - \Delta \cdots]^T)}{2\Delta} \tag{6.15}$$

The binary dither signal δ_i with small amplitude Δ and zero mean is often used due to its simple hardware implementation. It is expressed as:

$$\delta_i(k) = \pm\Delta,\ E[\delta_i(k)] = 0,\ \text{the variation } \sigma^2 = E[\delta_i^2(k)] = \Delta^2 \tag{6.16}$$

From Eq.(6.15), the estimation equation for gradient signal is derived as follows:

$$\begin{aligned}
\frac{\partial \varepsilon}{\partial \gamma_{i0}} &= \frac{\varepsilon([\gamma_{00}, \gamma_{10} \cdots \gamma_{i0} + \Delta \cdots]^T) - \varepsilon([\gamma_{00}, \gamma_{10} \cdots \gamma_{i0} - \Delta \cdots]^T)}{2\Delta} \\
&= \frac{1}{2\Delta}(E[e^2(k)]\Big|_{\delta_i=+\Delta} - E[e^2(k)]\Big|_{\delta_i=-\Delta}) \\
&= \frac{1}{\Delta^2}[(\frac{\Delta}{2} \cdot E[e^2(k)]\Big|_{\delta_i=+\Delta}) + (\frac{-\Delta}{2} \cdot E[e^2(k)]\Big|_{\delta_i=-\Delta})] \\
&= \frac{1}{\Delta^2}[(\frac{1}{2} \cdot E[\delta_i(k) \cdot e^2(k)]\Big|_{\delta_i=+\Delta}) + (\frac{1}{2} \cdot E[\delta_i(k) \cdot e^2(k)]\Big|_{\delta_i=-\Delta})]
\end{aligned} \tag{6.17}$$

The binary dither signal has zero mean:

$$E[\delta_i(k)] = 0 \Rightarrow \begin{cases} \delta_i(k) = +\Delta & \textit{one-half of the time} \\ \delta_i(k) = -\Delta & \textit{one-half of the time} \end{cases}$$

$$\Rightarrow E[\delta_i(k) \cdot e^2(k)] = (\frac{1}{2} \cdot E[\delta_i(k) \cdot e^2(k)]\Big|_{\delta_i=+\Delta}) + (\frac{1}{2} \cdot E[\delta_i(k) \cdot e^2(k)]\Big|_{\delta_i=-\Delta}) \tag{6.18}$$

So the gradient estimate equation is:

$$\frac{\partial \varepsilon}{\partial \gamma_{i0}} = \frac{1}{\Delta^2} \cdot E[\delta_i(k) \cdot e^2(k)] \approx \frac{1}{\sigma^2} \cdot \delta_i(k) \cdot e^2(k) \tag{6.19}$$

From Eq.(6.11), the update operation for the wave adaptor coefficient is given as follows:

$$\gamma_{i0}(k+1) = \gamma_{i0}(k) - \frac{\mu}{\sigma^2} \cdot \delta_i(k) \cdot e^2(k) \tag{6.20}$$

The main advantage of this algorithm is that it does not require additional hardware to produce the gradient signals, and all filter parameters can be adapted independently by introducing uncorrelated dither signals to all of the parameters. A block diagram of adaptation operation of each series or parallel wave adaptor coefficient is shown in Fig.6.5.

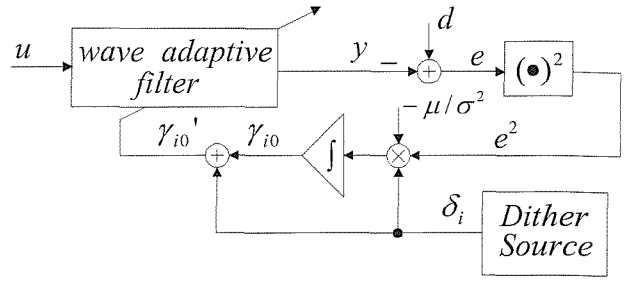


Fig.6.5 Adaptation process using DLS algorithm

6.5 Simulation and application

In this section, the theoretical analysis of the wave adaptive analogue filter structures is validated using *MATLAB* simulation and is used in a system identification application. In addition, comparison between proposed wave adaptive filter and previously reported adaptive IIR filter has been studied.

6.5.1 *MATLAB* simulation

In order to model the adaptation process in *MATLAB*, it is necessary to model the adaptive filter and DLS algorithm. The adaptive wave filter consists of the series and parallel wave adaptors, described by the SFGs of Fig.6.2, and delay cells. The model of the adaptive wave filter is derived by describing the wave adaptors using Eq.(6.7). The DLS update process, shown in Fig.6.5, is modelled and simulated by describing Eq.(6.20). A dither signal producer is implemented by a random binary function with zero mean and variance of σ^2 and the constraints of Eq.(6.9) are employed to ensure stability. Replication of the DLS block diagram is necessary for each coefficient. One common application of adaptive analogue filters is system identification, which is used to derive a guess of an unidentified system function. This is often used in communications where the characteristics of a channel are required for compensation. Fig.6.6 shows the block diagram of system identification model.

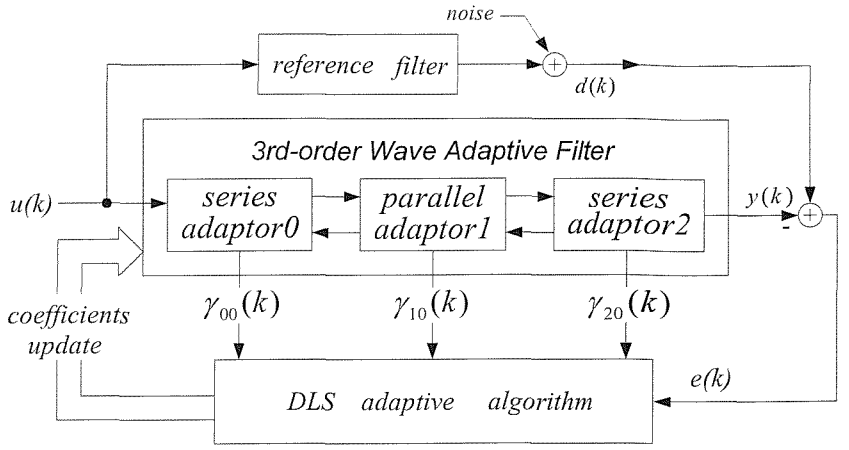


Fig.6.6 Block diagram of system identification

In this example, 3rd-order lowpass Chebyshev wave filter with 0.177dB ripple, and 0.2 normalized cutoff frequency has been chosen as reference filter. The normalized value of passive components in the prototype circuit, Fig.6.1(a), are calculated as: $L_1 = L_3 = 0.8183\text{H}$, $C_2 = 0.7943\text{F}$, and the z-domain transfer function, which is derived by bilinear transformation, is given as follows:

$$H(z) = \frac{0.1226 \times (1+z^{-1})^3}{1 - a_3 z^{-1} - a_2 z^{-2} - a_1 z^{-3}} \qquad (6.21)$$

where a_3=0.4353, a_2=-0.5334, and a_1=0.1175

Using the wave synthesis technique, the coefficients of the reference wave filter are:

$$\gamma_{00} = \gamma_{01} = 0.55, \quad \gamma_{02} = 0.9, \quad \gamma_{10} = \gamma_{11} = 0.5573,$$

$$\gamma_{12} = 0.8854, \quad \gamma_{20} = \gamma_{21} = 0.55, \quad \gamma_{22} = 0.9$$

To simplify the comparison with these theoretical values, it is assumed that the adaptive wave filter is also based on 3rd-order wave filter. According to adaptive theory [82], both the adaptive wave filter and the system to be identified are fed with an input white signal of variance 5. White noise of variance 0.1 is added to the output of the reference filter. Using the adaptive wave filter described in section 6.3 and DLS algorithm, only one coefficient of each adaptor of the filter is required to be updated, i.e. γ_{00} for *adaptor0*, γ_{10} for *adaptor1* and γ_{20} for *adaptor2*. The DLS algorithm converge factor μ used in this example is 4×10^{-4}. For each data sample k, $1<k<2000$, a dither signal with variance of 4×10^{-3} is inserted into the system, Fig.6.5. Mean-squared error (*MSE*) is used as the performance criteria for the DLS adaptation. An ideal

adaptation process would result in the adaptive wave filter being left with the same coefficients as the reference filter. The details of *MATLAB* program on the system identification are given in Appendix C.

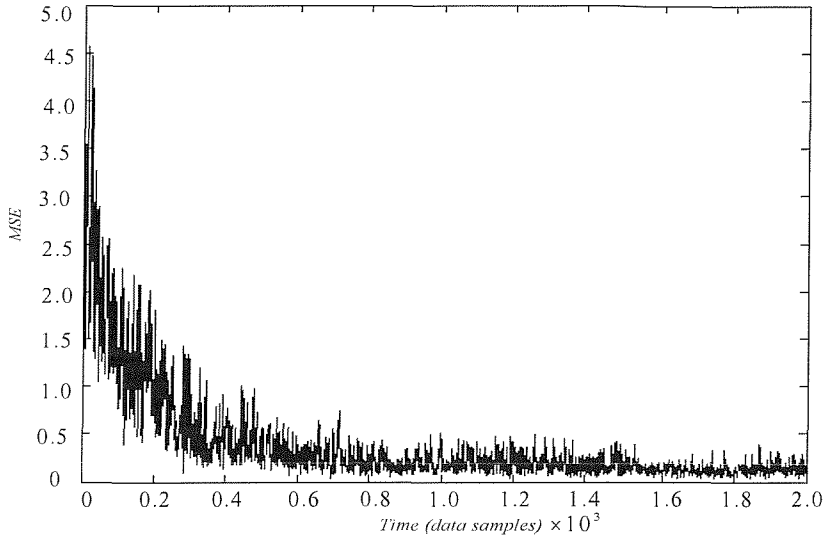


Fig.6.7 Learning curves for the 3rd-order wave adaptive filter

Results from an ensemble of 40 simulation runs are plotted in Fig.6.7. The simulated learning curve of *MSE* converges to its minimum value, which demonstrates the validity of the proposed structure. The steady values of wave adaptor coefficients, after 2000 samples, are:

$\gamma_{00}(2000) = \gamma_{01}(2000) = 0.5235,\ \gamma_{02}(2000) = 0.935,\ \gamma_{10}(2000) = \gamma_{11}(2000) = 0.5637,$

$\gamma_{12}(2000) = 0.8726,\ \gamma_{20}(2000) = \gamma_{21}(2000) = 0.5341,\ \gamma_{22}(2000) = 0.9318$

These coefficients compare well with that of the reference filter (within 3% difference with reference value), indicating that the wave adaptive filter is operating as expected. Note the coefficients $\gamma_{02}(2000)$, $\gamma_{12}(2000)$ and $\gamma_{22}(2000)$ are calculated and that all of the coefficients are within the stability constraints of Eq.(6.9). The frequency responses of the adaptive and reference filter are given in Fig.6.8 showing after the adaptation process, the adaptive wave filter exhibits similar performance to the ideal reference filter, indicating successful system identification.

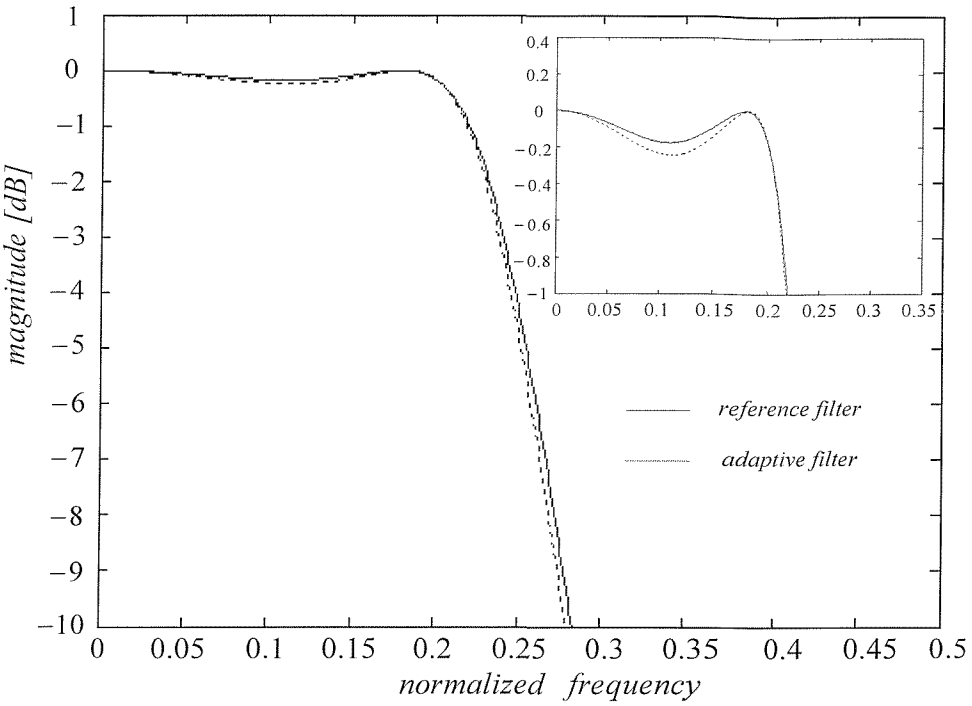


Fig.6.8 Frequency response of reference and wave adaptive filter

To see how the performance of the proposed adaptive filter based on wave structure and DLS algorithm compare with that of the other type of adaptive filters, the direct-form IIR adaptive filter [82] shown in Fig.6.4 is simulated in the system identification, Fig.6.9. Eq.(6.21) gives the transfer function for the direct-form IIR reference filter, and the ideal value of the coefficients are: a_1=0.1175 a_2=-0.5334 and a_3=0.4353. The steady values of transfer function coefficients in direct-form IIR adaptive filter, after 500 samples, are: $a_1(500)$ =0.1194, $a_2(500)$ =-0.5543, $a_3(500)$ =0.4562

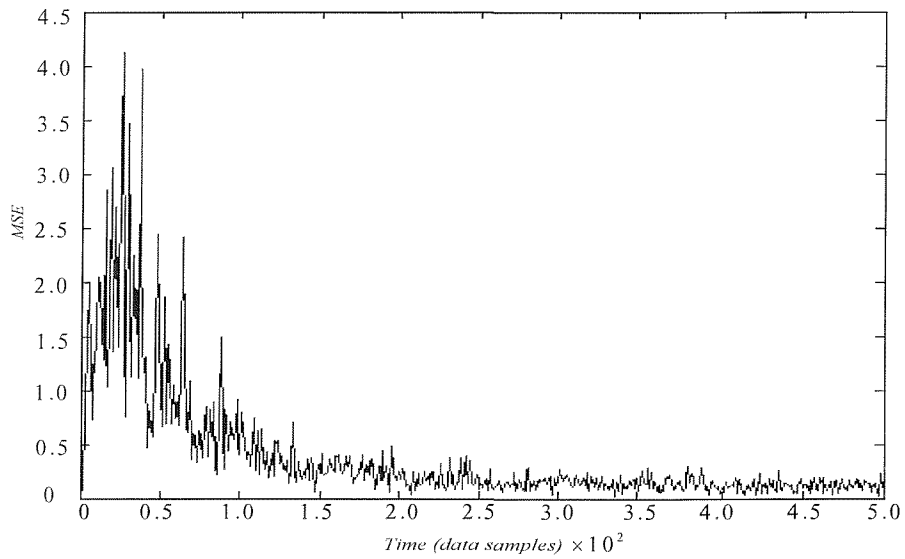


Fig.6.9 Learning curves for the 3rd-order direct-form IIR adaptive filter

It can be seen that the direct-form IIR adaptive filter, (Fig.6.9), which using LMS algorithm, converges faster than adaptive wave filter, because DLS algorithm, which is applied to the adaptive wave filter, averaged over more data samples for approaching the true value of gradient signal. The new trend in digital communication application is the signal bandwidths and data rate are increasing, while the required adaptation rates remain constant [70,85]. Therefore, it is reasonable to consider using analogue wave filter for high-speed signal processing while implementing the slower adaptive algorithm. In addition, although DLS adaptation algorithm requires a large number of iterations to converge, the sampling rate is so high that the process can converge quickly in absolute terms. The main advantages of the adaptive wave filters are their simpler hardware implementation and low sensitivity to the wave adaptor coefficients. The adaptive wave filter has simpler hardware implementation when compared with direct-form IIR adaptive filter, because the latter needs to adapt both feedback coefficients a_i and feedforward coefficients b_i, while the adaptive wave filter only adapt one coefficient γ_{0i} for each wave adaptor of the filter. In addition, the direct-form IIR adaptive filter requires additional hardware to realize the stability checks. Low sensitivity in adaptive wave filters is due to their derivation from LC ladder prototypes.

6.5.2 Circuit implementation

In section 6.5.1, the validity of adaptive wave filter has been demonstrated using *MATLAB*. In this section, its circuit implementation will be presented. The adaptive wave filter can be separated into two circuit parts, namely, the analogue wave filter part and the DLS adaptation part, Fig.6.10.

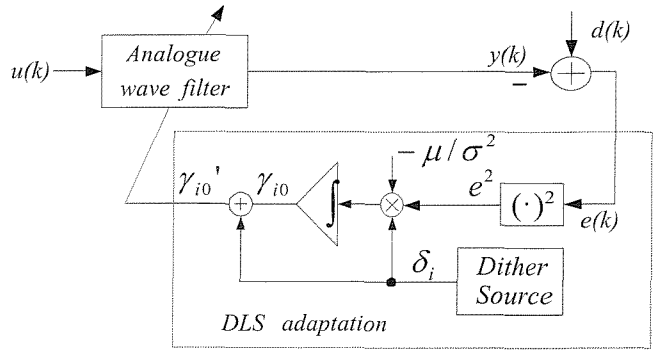


Fig.6.10 Configuration of analogue adaptive wave filter

It can be seen from Fig.6.10 that the elements of adaptive wave filter consist of delay cells, which are within the analogue wave filter, summing circuit (+), integrator ($\int$), and multipliers ($\times$). Different analogue technologies, such as switched-capacitor and switched-current, can be used to implement adaptive wave filter structure, which includes wave filter part and adaptation part. SI technology is more suitable for implementing the analogue wave filter part in Fig.6.10, because SI technology is easier than SC circuit for the wave filter design, where the values of wave adaptor coefficients depend only on the aspect ratio of the current mirror transistors. Previous research has shown that non-ideal characteristics, i.e. DC-offset, is introduced into the adaptive filter if using analogue implementation of adaptation part. It will lead to deterioration in the performance of analogue adaptive filters [70,73,85]. Recently there is indication that the digital implementation of gradient algorithm is more robust in the presence of DC-offset [70,85]. Therefore, the hardware-efficient method for digitally adapting analogue SI wave filter structure is considered here, Fig.6.11.

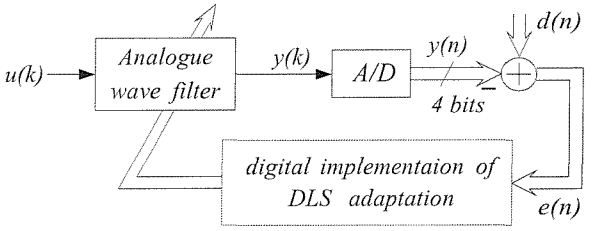


Fig.6.11 Analogue adaptive wave filter with digital implementation of adaptation

An A/D converter is used to converter discrete-time output signal *y(k)* to digital signal *y(n)*. The 4 bits digital signal is employed for parallel digital signal processing. The DLS algorithm is performed through digital implementation, which is free of non-ideal characteristics of analogue circuit. In this way, we can process the data at high speed and low power consumption, while maintaining the adaptation process free of analogue non-ideal characteristics.

The analogue wave filter with variable frequency response (Fig.6.11) can be realized through the implementation of series and parallel wave adaptor with adaptable wave adaptor coefficient γ_{i0}, Fig.6.2. The value of wave adaptor coefficient depends on the aspect ratio of the current mirror transistors. The variation of coefficient values in

series or parallel wave adaptors can be achieved with an array of unit-size transistors through a set of digitally controlled CMOS switches, Fig.6.12.

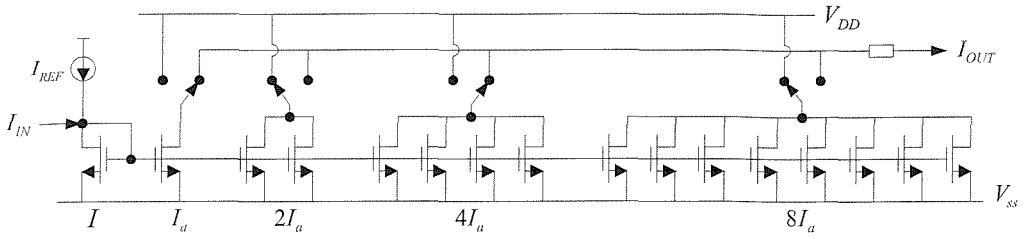


Fig.6.12 Current mirror with adaptable current output ($I = 16I_a$)

Quantization error can arise from this scaling current mirror, because the smallest updating step for wave adaptor coefficient γ_{i0} is limited to 2^{-4}, and it will affect the accuracy of the wave adaptor coefficients. Due to the low sensitivity of wave filters, the analogue adaptive wave filters are still able to meet sharp frequency response specifications in the presence of quantization error.

6.6 Concluding remarks

This chapter has demonstrated the feasibility of using wave synthesis technique for analogue adaptive signal processing. New analogue adaptive filters are obtained through the modification on the direct wave filters. These filters offer a number of advantages including low sensitivity since they are derived from LC ladder prototypes, simple adaptation process, as only one coefficient per adaptor needs to be updated, and simple stability checks. The simulation of 3rd-order analogue adaptive wave filter in a system identification application has been included, showing the effectiveness of the new filter structure in adaptive analogue signal processing applications. The hardware implementation has been discussed, showing an efficient method to realize the analogue adaptive wave filter.

Chapter 7

Conclusions and Further Research

7.1 Conclusions

The main aim of this thesis has been the investigation of the filters including adaptive and group delay equalizations using switched-current (SI) technology. With the increasing developments of mixed-signal chips in consumer electronics and communication applications, filters and group delay equalizers become important subsystem in analogue interfacing circuitry. Such analogue subsystem is required to be simple, low sensitivity and adaptive for time-varying conditions. Their fabrications using CMOS technology are required to be compatible with digital technology.

Based on these requirements, this thesis investigates the design of SI filters, group delay equalizers and SI adaptive filters using wave synthesis technique. Firstly, this thesis has identified Bruton transformation SI wave filters as an efficient design of SI filters and presented detailed analysis of their non-ideal performance using behaviour models. Secondly, a systemic design method of SI group delay wave equalizers has been proposed. Finally, SI adaptive filters, based on wave synthesis technique, are presented. The summary of contributions in this thesis is given next.

Chapter 3 provides a detailed analysis of Bruton transformation SI wave filters. The behaviour input-output models of new Bruton transformation wave components, which taking into account of mismatch and clock-feedthrough errors, have been developed according to the physical realization. Numerical simulations using these behaviour models have been performed on two different Bruton transformation SI wave filters. The results show that clock-feedthrough has stronger influence on the filter performances, and the filter passband sensitivities to mismatch are low. It is suggested that the effective circuit techniques, which are used to reduce clock-feedthrough errors, should be employed in practical design of Bruton transformation SI wave filters in order to improve the filters' performance.

Chapter 4 proposes new group delay wave equalizers, which are used to improve the time-domain response of elliptic SI filters. The whole design process, including optimisation of allpass transfer function and synthesis of wave structure, has been described, and new transistor-level circuit architecture, which can be implemented easily using SI technology, is presented. Different order of allpass circuits can be obtained through modifying block *Y(z)* in the architecture. SCNAP4 simulations are performed on the different order of SI group delay wave equalizers. It is shown that the nearly flat group delay response can be obtained when group delay equalizers are cascaded with SI filters, and the group delay variation of cascaded filters and equalizers reduces as the order of equalizers increases. The step response of SI filters cascaded with equalizers is also performed using SCNAP4 simulator, and these simulation results indicate the validity of design and the resultant circuit architecture of group delay wave equalizers.

Chapter 5 considers the transistor-level design of SI wave filters and group delay equalizers. Some design issues, such as non-ideal characteristics of SI circuits have been described. Practical SI building blocks are introduced to reduce the influence of non-ideal characteristics in SI technology. The complete design process of elliptic wave filter with group delay wave equalizer is presented. The overall transistor-level circuits, based on 1^{st}-order cascode SI delay cells and current mirrors, have been developed. PSPICE simulations are performed to demonstrate the validity of the non-ideal performance analysis of SI wave filters and design method of SI group delay equalizers.

Chapter 6 investigates SI adaptive wave filters, whose parameters can track time-varying conditions. The direct wave filter structure has been modified to perform adaptive signal processing. The DLS (Dither Linear Search) algorithm, which is suitable to adaptive wave filter, has been introduced to update the parameters of SI wave filters. These adaptive wave filters have a number of advantages, such as low sensitivity, simple adaptation process and easy stable checks. *MATLAB* simulation of system identification gives the satisfying learning curves of SI adaptive wave filters. Discussion of the efficient hardware implementation of such filters is also included.

In conclusion, the analysis methods, design techniques and transistor-level circuits of SI wave filters and group delay equalizers given in this thesis have contributed to the maturity of switched-current design as a potential alternate to

switched-capacitor in analogue IC design. The wave synthesis technique, which had been originally developed for digital filters, has been found to be a viable approach to the design of analogue filters and group delay equalizers based on the switched-current technology. Finally, this research has extended the application of wave synthesis technique into the area of adaptive analogue signal processing.

7.2 Further research

Based on research performed in this thesis, three relevant future research directions are identified and briefly outlined:

7.2.1 High-level simulations on the transistor-level circuits of SI wave filters and equalizers

In Chapter 5, transistor-level circuits of SI wave filter and group delay equalizer have been designed and simulated based on standard 1.2 μm *p-well* CMOS and level-2 transistor models. These simulations on transistor-level circuits have validated the non-ideal performance analysis of SI filters and design method of SI group delay wave equalizer. In order to implement and submit to manufacture, more transistor-level simulations based on sub-micron CMOS technology and BSIM3 models should be made. The detailed performances of transistor-level circuits, such as distortion and noise, are required to be investigated.

7.2.2 Low-power implementation of SI wave filters and equalizers

The emerging trends of portable analogue and mixed-signal applications require low-voltage, low-power and large dynamic range implementation. Bruton transformation wave filters have been identified as an efficient design method for high-order SI filters. Hence, further investigation is needed to focus on low-power building blocks, such as class-AB circuit [67] and adaptive bias current mirror [69], and fully differential CMOS implementation of high-order Bruton transformation SI wave filters and group delay equalizers.

7.2.3 High-speed SI adaptive wave filters

New SI adaptive wave filters have been proposed. As described in Chapter 6, adaptive algorithm is required to be realized using digital technology, while wave filters are preferred to be implemented using SI technology. This implementation has the benefit

of eliminating DC-offset in the adaptation circuitry. An important requirement in communication applications is high speed signal processing. Hence, it would be interesting to investigate the implementation of an adaptive algorithm through analogue SI technology. Differential implementation and circuit design techniques need to be considered to reduce DC-offset in SI building blocks, which will be used for development of high-speed analogue adaptation circuitry.

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Appendix

A. Analysis of non-ideal performance of Bruton transformation wave filters

This program analyses the non-ideal frequency response of Bruton transformation wave filters due to clock-feedthrough errors in delay cells. The Bruton transformation filters are simulated according to relations given in Chapter 2.

```
%3rd-order elliptic Bruton filter, fp is 0.1, fs is 0.2291, sample freq is 1.
k=256; In=zeros(1,k+1); IO=zeros(1,k); c=zeros(1,k+1);
A00=zeros(1,k+1); B00=zeros(1,k+1); A01=zeros(1,k+1); B01=zeros(1,k+1);
A02=zeros(1,k+1); B02=zeros(1,k+1);
A10=zeros(1,k+1); B10=zeros(1,k+1); A11=zeros(1,k+1); B11=zeros(1,k+1);
A12=zeros(1,k+1); B12=zeros(1,k+1);
A20=zeros(1,k+1); B20=zeros(1,k+1); A21=zeros(1,k+1); B21=zeros(1,k+1);
A22=zeros(1,k+1); B22=zeros(1,k+1);
A30=zeros(1,k+1); B30=zeros(1,k+1); A31=zeros(1,k+1); B31=zeros(1,k+1);
A32=zeros(1,k+1); B32=zeros(1,k+1);

y00=0.3282;   y01=0.5;    y10=0.1718;   y11=0.5;    y12=1.3282;
y20=0.5;      y22=0.7527;    y30=0.2055;   y31=0.3927;

vf=0.01;                  % clock-feedthrough error voltage
%e=2*vf*sqrt(22.1)+1;  % second  generation clock-feedthrough
e=2*22.1*vf*vf+1;         % adavanced second generation clock-feedthrough
In(2)=1;   t=0.000001;

for n=2:k+1

  s=1;   A00(n)=In(n)-e*In(n-1)+e*B00(n-1);
  A31(n)=e*B31(n-1);   A22(n)=c(n)*2;

  while s==1
  B01(n)=A01(n)-y01*(A00(n)+A01(n));
```

```
A10(n)=B01(n);
B10(n)=y10*A10(n)+y11*A11(n)+y12*A12(n)-A10(n);
B11(n)=y10*A10(n)+y11*A11(n)+y12*A12(n)-A11(n);
B12(n)=y10*A10(n)+y11*A11(n)+y12*A12(n)-A12(n);

A20(n)=B12(n);
B20(n)=A20(n)-y20*(A20(n)+A22(n));
A30(n)=B11(n);

B30(n)=A30(n)-y30*(A30(n)+A31(n));
B31(n)=A31(n)-y31*(A30(n)+A31(n));
%judge:
  p1=(abs(B10(n)-A01(n))<t);    p2=(abs(B20(n)-A12(n))<t);
  p3=(abs(B30(n)-A11(n))<t);    p=p1&p2&p3;
if p==1
  s=0;
end
%end of judge
A01(n)=B10(n); A12(n)=B20(n); A11(n)=B30(n);
end
B00(n)=A00(n)-y00*(A00(n)+A01(n)); B22(n)=A22(n)-y22*(A20(n)+A22(n));
c(n+1)=e*(B22(n)-c(n-1)*e);

IO(n-1)=A31(n)+B31(n);
end
s=20*log10(abs(fft(IO)));
f=(0:k-1)/k;
plot(f,s),axis([0,0.25,-1,1])
```

B. Optimisation of 7th-order SI group delay wave equalizer

This program uses optimisation function *fmincon* to find the allpass transfer function so that the combined group delay of 3rd-order elliptic filter and 7th-order group delay equalizer has minimum ripple. The optimisation process is described in Chapter 4.

```
format long e;
x0=[0.8,0.5,0.8,1,0.8,2,0.8];
lb=[0.1,0,0.1,0.1,0.1,0,0.1];
ub=[0.9,pi,0.9,pi,0.9,pi*9/10,0.9];

options=optimset('LargeScale','off');

[x,fval]=fmincon(@zrladder7,x0,[],[],[],[],lb,ub,[],options);
*********************************************************
% the function is 'zladder'
function ripple=zrladder7(x,ell3);
load C:\Matlab6\work\ell3.txt;

k=200;
for n=0:k-1
   t1=n*3+1;   p(n+1)=ell3(t1,1);
   t2=n*3+3;   q(n+1)=ell3(t2,2);
end

w=2*pi*p;              % passband freq. the unit is rad
fs=10^6;

%normalize  for run optimisation
w=w/fs;   T=1;
r1=x(1);     thea1=x(2);          r2=x(3);     thea2=x(4);
r3=x(5);     thea3=x(6);          r4=x(7);     thea4=0;

%normalized group delay tEni of equalizer
tEn1=gdc(r1,thea1,w,T);          tEn2=gdc(r2,thea2,w,T);
```

```
tEn3=gdc(r3,thea3,w,T);          tEn4=gdr(r4,thea4,w,T);

tFn=q*fs;  %normalized group delay of filter

for n=1:200
   % the normalized group-delay of the equalizer
      tEn(n)=tEn1(n)+tEn2(n)+tEn3(n)+tEn4(n);
   % the normalized group-delay of the combined filter and equalizer
     tFEn(n)=tFn(n)+tEn(n);
end
ripple=max(tFEn)-min(tFEn);

**********************************************************
% gdc---- the function to calculate the group delay of the complex pole

function [groupd]=gdc(r,theta,w,T)
 a1=w*T-theta;                    a2=w*T+theta;
 a3=1-2*r*cos(a1)+r*r;            a4=1-2*r*cos(a2)+r*r;

for n=1:200
    a5(n)=1/a3(n);       a6(n)=1/a4(n);
    groupd(n)=T*(1-r*r)*(a5(n)+a6(n));
end

**********************************************************
%the function to calculate the group-delay  of the real single pole
% since it is the real pole, theta is only 0 or pi
function [groupd]=gdr(r,theta,w,T)
a1=2*r*cos(w*T);        a2=T*(1-r*r);          a3=1-a1+r*r;
if theta==pi
    a3=1+a1+r*r;
end
for n=1:200
   groupd(n)=a2/a3(n);
end
```

C. System identification program

This program gives the adaptation process of 3rd-order SI adaptive wave filter in the application of system identification. The modelling of SI adaptive wave filter and adaptive algorithm is described in Chapter 6.

```
%normal 3rd Chebyschev filter with  cutoff freq. is 0.2
y02=0.9;     y00=0.5*(2-y02);     y01=y00;
y12=0.8854;  y10=0.5*(2-y12);     y11=y10;
y22=0.9;     y20=0.5*(2-y22);     y21=y20;
number=5000;    iteration=number+1;
u=zeros(1,iteration); d=zeros(1,number);
A00=zeros(1,iteration); A10=zeros(1,iteration); B10=zeros(1,iteration);
A20=zeros(1,iteration); B20=zeros(1,iteration); A01=zeros(1,iteration);
B01=zeros(1,iteration); A11=zeros(1,iteration); B11=zeros(1,iteration);
A21=zeros(1,iteration); B21=zeros(1,iteration); A02=zeros(1,iteration);
B02=zeros(1,iteration); A12=zeros(1,iteration); B12=zeros(1,iteration);
B22=zeros(1,iteration);
u=sqrt(10)*randn(1,iteration);    v=sqrt(0.01)*randn(1,iteration);    limit=10^(-5);

for n=2:iteration
  s=1;
  A00(n)=u(n);   A02(n)=-B02(n-1);   A12(n)=B12(n-1);   A22(n)=-B22(n-1);
 while s==1
   B01(n)=A01(n)-y01*(A00(n)+A01(n)+A02(n));
  A10(n)=B01(n);
  B10(n)=y10*A10(n)+y11*A11(n)+y12*A12(n)-A10(n);
  B11(n)=y10*A10(n)+y11*A11(n)+y12*A12(n)-A11(n);
 A20(n)=B11(n);   B20(n)=A20(n)-y20*(A20(n)+A22(n));
%judge:
  p1=(abs(B10(n)-A01(n))<limit);   p2=(abs(B20(n)-A11(n))<limit);   p=p1&p2;
  if p==1
    s=0;
  end
  %end of judge
```

```
   A01(n)=B10(n);A11(n)=B20(n);
   end

   B02(n)=A02(n)-y02*(A00(n)+A01(n)+A02(n));
   B12(n)=y10*A10(n)+y11*A11(n)+y12*A12(n)-A12(n);
   B22(n)=A22(n)-y22*(A20(n)+A22(n));  B21(n)=A21(n)-y21*(A20(n)+A22(n));
   d(n-1)=B21(n)+v(n);
end

% the program perform the DLS adaptive algorithm
times=5;     k=zeros(times,number);     y02=zeros(times,iteration);     pp=0;
y12=zeros(times,iteration);     y22=zeros(times,iteration);

for m=1:times
A00=zeros(1,iteration); A10=zeros(1,iteration); B10=zeros(1,iteration);
A20=zeros(1,iteration); B20=zeros(1,iteration); A01=zeros(1,iteration);
B01=zeros(1,iteration); A11=zeros(1,iteration); B11=zeros(1,iteration);
A21=zeros(1,iteration); B21=zeros(1,iteration); A02=zeros(1,iteration);
B02=zeros(1,iteration); A12=zeros(1,iteration); B12=zeros(1,iteration);
B22=zeros(1,iteration);
e=zeros(1,number);     Io=zeros(1,number);     c=zeros(1,number);

% dither signal are used to adapt taps with variance=10^(-5)
variance=10^(-5);
dither1=sqrt(variance)*randsrc(1,iteration);
dither2=sqrt(variance)*randsrc(1,iteration);
dither3=sqrt(variance)*randsrc(1,iteration);

t=2*10^(-5);        % t is step length
y02(m,1)=1;     y00=0.5*(2-y12(m,1));     y01=y00;
y12(m,1)=1;     y10=0.5*(2-y12(m,1));     y11=y10;
y22(m,1)=1;     y20=0.5*(2-y22(m,1));     y21=y20;

 for n=2:iteration
   s=1;
```

```
y02a=y02(m,n-1)+dither1(n-1);   y00=0.5*(2-y02a);   y01=y00;
y12a=y12(m,n-1)+dither2(n-1);   y10=0.5*(2-y12a);   y11=y10;
y22a=y22(m,n-1)+dither3(n-1);   y20=0.5*(2-y22a);   y21=y20;

A00(n)=u(n);  A02(n)=-B02(n-1);  A12(n)=B12(n-1);  A22(n)=-B22(n-1);
while s==1
count=count+1;    B01(n)=A01(n)-y01*(A00(n)+A01(n)+A02(n));

A10(n)=B01(n);   B10(n)=y10*A10(n)+y11*A11(n)+y12a*A12(n)-A10(n);
B11(n)=y10*A10(n)+y11*A11(n)+y12a*A12(n)-A11(n);

A20(n)=B11(n);   B20(n)=A20(n)-y20*(A20(n)+A22(n));

%judge:
  p1=(abs(B10(n)-A01(n))<limit);   p2=(abs(B20(n)-A11(n))<limit);   p=p1&p2;

if p==1
  s=0;
end
%end of judge

A01(n)=B10(n); A11(n)=B20(n);
end

B02(n)=A02(n)-y02a*(A00(n)+A01(n)+A02(n));
B12(n)=y10*A10(n)+y11*A11(n)+y12a*A12(n)-A12(n);
B22(n)=A22(n)-y22a*(A20(n)+A22(n));
B21(n)=A21(n)-y21*(A20(n)+A22(n));

Io(n-1)=B21(n);
e(n-1)=d(n-1)-Io(n-1);
y02(m,n)=y02(m,n-1)-t*dither1(n-1)*e(n-1)*e(n-1)/variance;
y12(m,n)=y12(m,n-1)-t*dither2(n-1)*e(n-1)*e(n-1)/variance;
y22(m,n)=y22(m,n-1)-t*dither3(n-1)*e(n-1)*e(n-1)/variance;
```

```
    if (y02(m,n)<0.1)
       y02(m,n)=0.1;
    end
    if (y12(m,n)<0.1)
       y12(m,n)=0.1;
    end
    if (y22(m,n)<0.1)
       y22(m,n)=0.1;
    end
    if (y02(m,n)>1.8)
       y02(m,n)=1.8;
    end
    if (y12(m,n)>1.8)
       y12(m,n)=1.8;
    end
    if (y22(m,n)>1.8)
       y22(m,n)=1.8;
    end
    k(m,n-1)=e(n-1)*e(n-1);
  end
 end

for n=1:number
   for m=1:times
      c(n)=k(m,n)+c(n);
   end
   c(n)=c(n)/times;
end
p=(1:number);
plot(p,c)
```

D. Group delay response of 3rd-order SI wave filter and equalizer

The program gives SCNAP4 simulation on 3rd-order SI wave filter and equalizer, which are outlined in Chapter 4. The advantage of this simulator is that it can analyse the frequency response of switched-current and switched-capacitor circuits. Transistors are considered as ideal transconductors in with parasitic effects ignored in SCNAP4.

```
*use first generation memory cell, the normal passband frequency is 0.1
*the denormalized passband freq. is 100kHz, the denormalized sample freq. is 1MHz
.option cont ron=1.0e-1 roff=1.0e+20
.subckt mos 1 2 (k)
c1 1 0 1.0e-15
g1 1 0 2 0 k
r2 2 0 1.0e+8
c2 2 0 1.0e-15
.ends mos
.subckt delay 1 5 (t1,t2)
xmos1 1 1 mos(1.0)
s1 1 2 t1
xmos2 2 3 mos(1.0)
xmos3 3 3 mos(1.0)
s2 3 4 t2
xmos4 4 5  mos(1.0)
.ends delay
.subckt mirror 1 2
xmos1 1 1 mos(1.0)
xmos2 1 2 mos(1.0)
.ends mirror
.subckt twomirror 1 2 3
xmos1 1 1 mos(1.0)
xmos2 1 2 mos(1.0)
xmos3 1 3 mos(1.0)
.ends twomirror

.subckt threemirror 1 2 3 4
xmos1 1 1 mos(1.0)
```

```
xmos2 1 2 mos(1.0)
xmos3 1 3 mos(1.0)
xmos4 1 4 mos(1.0)
.ends threemirror

vin 40 0 ac 1.0 0.0
g1 40 0 0 1 1

**************************************
*3-port series adaptor
xmirror1 1 2 mirror
xmirror2 3 4 2 twomirror
xmirror3 5 6 2 twomirror
xmos1 2 2 mos(1.0)
xmos2 2 4  mos(1.0)
xmos3 2 6  mos(0.775)
xmirror5 4 7 mirror
*delay cell
xdelay1 6 5  delay(t1,t2)
**************************************
*3-port parallel adaptor
xmos5 7 7 mos(1.0)
xmos6 7 8 mos(1.0)
xmos7 7 9  mos(0.11)
xmos8 10 10 mos(1.0)
xmos9 10 11 mos(1.0)
xmos10 10 9 mos(1.0)
xmos11 12 12 mos(1.0)
xmos12 12 13 mos(1.0)
xmox13 12 9 mos(0.89)
xmirror8 9 8 11 3  threemirror
**************************************
*3-port series adaptor
xmirror9 8 13 14 twomirror
xmirror10 15 16 14 twomirror
```

```
xmirror11 17 18 14 twomirror
xmos14 14 14 mos(1.0)
xmos15 14 13 mos(1.0)
xmos16 14 16 mos(0.447)
xmos17 14 18 mos(0.553)
xmirror12 13 12 mirror
xmirror13 18 19 mirror
*delay cell
xdelay2 16 15 delay(t1,t2)
xdelay3 19 17 delay(t1,t2)
**************************************
*3-port series adaptor
xmirror16 11 20 21 twomirror
xmirror17 22 23 21 twomirror
xmos18 21 21 mos(1.0)
xmos19 21 20 mos(0.2)
xmos20 21 24 mos(0.4)
xmos21 21 23 mos(1.4)
xmirror18 20 10 mirror
xmirror19 24 25 mirror
*delay cell
xdelay4 23 22 delay(t1,t2)
**************************************
*input signal for allpass
xmos24 25 25 mos(1.0)
xmos25 25 26 mos(1.0)
xmos26 25 27 mos(2.0)
xmirror20 27 28 26 twomirror
xmos27 26 29 mirror

xmirror21 30 27 28 twomirror
xmirror22 28 31 mirror
xmirror23 31 27 32 twomirror

*3-port parallel adaptor
```

```
xmos33 32 32 mos(1.0)
xmos34 32 30 mos(1.0)
xmos35 32 31 mos(1.0536)
xmos36 34 34 mos(1.0)
xmos37 34 35 mos(1.0)
xmos38 34 31 mos(0.838)
xmos39 36 36 mos(1.0)
xmos40 36 37 mos(1.0)
xmos41 36 31 mos(0.1084)
xmirror29 31 37 35 30 threemirror

*delay cell
xdelay5 35 38 delay(t1,t2)
xdelay6 37 36 delay(t1,t2)
xdelay7 41 40 delay(t1,t2)

*2-port parallel adaptor
xmos42 38 38 mos(1.0)
xmos43 38 34 mos(1.0)
xmos44 38 39 mos(0.1314)
xmos45 40 40 mos(1.0)
xmos46 40 41 mos(1.0)
xmos47 40 39 mos(1.8686)
xmirror30 39 34 41 threemirror
r1 29 0 1

*the clock frequency is 1MHz
.phase t1 pwl 0.0 1.0v 500ns 0v 1us 1.0v
.phase t2 pwl 0.0 0.0v 500ns 1v 1us 0.0v

.option groupd
.sens
.freq 10 0.1e+6 lin 200
.plot ac vi(29)
```

E. Implementation of 3rd-order SI wave filter and equalizer

The program uses standard 1.2um *p-well* CMOS process to simulate the transistor-level circuits of 3rd-order SI wave filter with group delay equalizer. The design process and overall transistor-level circuits are given in Chapter 5.

```
*p-well CMOS technology (the source and bulk of nmos transistor can be connected to
*remove body effect)
*CMOS 1.2um - level 2 model
 .model nmos NMOS LEVEL=2 LD=0.15U TOX=200E-10
 + NSUB=5.37E15 VTO=0.74 KP=8E-5 GAMMA=0.54
 + PHI=0.6 UO=656 UEXP=0.157 UCRIT=31444
 + DELTA=2.34 VMAX=55261 XJ=0.25U LAMBDA=0.037
 + NFS=1E12 NEFF=1.001 NSS=1E11 TPG=1 RSH=70
 + CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0003 MJ=0.66
 + CJSW=8E-10 MJSW=0.24 PB=0.58

 .model pmos PMOS LEVEL=2 LD=0.15U TOX=200E-10
 + NSUB=4.33E15 VTO=-0.74 KP=2.7E-5 GAMMA=0.58
 + PHI=0.6 UO=262 UEXP=0.324 UCRIT=65720
 + DELTA=1.79 VMAX=25694 XJ=0.25U LAMBDA=0.061
 + NFS=1E12 NEFF=1.001 NSS=1E11 TPG=1 RSH=121
 + CGDO=4.3E-10 CGSO=4.3E-10 CJ=0.0005 MJ=0.51
 + CJSW=1.35E-10 MJSW=0.24 PB=0.64
 .subckt switch 1 2 3 4 5 6
  * 1-input, 2-output, 3-nmos clock, 4-pmos clock, 5-nmos bulk, 6-pmos bulk
    mn 1 3 2 5 nmos W=2.4u L=1.2u
    mp 2 4 1 6 pmos W=3.6u L=1.2u
 .ends switch

.subckt memorycell 1 5 12 13 10 6 4 9
    *1-input, 5-output, 12-nmos clock, 13-pmos clock
    *10-dc voltage, 6-vpmos bias1, 4-vnmos bias, 9-vpmos bias2
   mp7 7 9 10 10 pmos W=144u L=7.2u
   mp8 8 9 10 10 pmos W=144u L=7.2u
   mp5 1 6 7 10 pmos W=94.8u L=3.6u
```

```
    mp6 5 6 8 10 pmos W=94.8u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=102u L=10.2u
    xs1 1 11 12 13 0 10 switch
    mn2 3 11 0 0 nmos W=102u L=10.2u
 .ends memorycell

.subckt delaycell 4 10 6 7 8 9 1 2 3 11
    *4-input, 10-output, 6,7-clock of the first memory cell
    *8,9-clock of the second memory cell
    *1-dc voltage, 2-vpmos bias1, 3-vnmos bias, 11-vpmos bias2
    xmemorycell1 4 5 6 7 1 2 3 11  memorycell
   xmemorycell2 5 10 8 9 1 2 3 11 memorycell
.ends delaycell

.subckt mirrorcell 1 5 10 6 4 9
   *1-input, 5-output, 10-dc voltage, 6-vpmos bias1, 4-vnmos bias, 9-vpmos bias2
    mp7 7 9 10 10 pmos W=144u L=7.2u
    mp8 8 9 10 10 pmos W=144u L=7.2u
    mp5 1 6 7 10 pmos W=117u L=3.6u
    mp6 5 6 8 10 pmos W=117u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=72u L=7.2u
    mn2 3 1 0 0 nmos W=72u L=7.2u
.ends mirrorcell

.subckt mirrorcell2  1 5  12 10 6 4 9
    *current mirror with two output
    *1-input, 5-output1, 12-output2, 10-dc voltage,
    *6-vpmos bias1, 4-vnmos bias, 9-vpmos bias2
    mp7 7 9 10 10 pmos W=144u L=7.2u
    mp8 8 9 10 10 pmos W=144u L=7.2u
    mp5 1 6 7 10 pmos W=117u L=3.6u
```

```
mp6 5 6 8 10 pmos W=117u L=3.6u
mn3 1 4 2 2 nmos W=144u L=3.6u
mn4 5 4 3 3 nmos W=144u L=3.6u
mn1 2 1 0 0 nmos W=72u L=7.2u
mn2 3 1 0 0 nmos W=72u L=7.2u

mp12 13 9 10 10 pmos W=144u L=7.2u
mp11 12 6 13 10 pmos W=117u L=3.6u
mn10 12 4 11 11 nmos W=144u L=3.6u
mn9 11 1 0 0 nmos W=72u L=7.2u
.ends mirrorcell2

.subckt mirrorcell3  1 5 12 15 10 6 4 9
*current mirror with three output, 1-input, 5-output1, 12-output2, 15-output3
*10-dc voltage, 6-vpmos bias1, 4-vnmos bias, 9-vpmos bias2
mp7 7 9 10 10 pmos W=144u L=7.2u
mp8 8 9 10 10 pmos W=144u L=7.2u
mp5 1 6 7 10 pmos W=117u L=3.6u
mp6 5 6 8 10 pmos W=117u L=3.6u
mn3 1 4 2 2 nmos W=144u L=3.6u
mn4 5 4 3 3 nmos W=144u L=3.6u
mn1 2 1 0 0 nmos W=72u L=7.2u
mn2 3 1 0 0 nmos W=72u L=7.2u

mp12 13 9 10 10 pmos W=144u L=7.2u
mp11 12 6 13 10 pmos W=117u L=3.6u
mn10 12 4 11 11 nmos W=144u L=3.6u
mn9 11 1 0 0 nmos W=72u L=7.2u

mp16 16 9 10 10 pmos W=144u L=7.2u
mp15 15 6 16 10 pmos W=117u L=3.6u
mn14 15 4 14 14 nmos W=144u L=3.6u
mn13 14 1 0 0 nmos W=72u L=7.2u
.ends mirrorcell3
```

```
*wave adaptor0 in elliptic SI wave filter
.subckt mirrorcofficient1  1 5  12 10 6 4 9
  mp7 7 9 10 10 pmos W=144u L=7.2u
  mp8 8 9 10 10 pmos W=144u L=7.2u
  mp5 1 6 7 10 pmos W=117u L=3.6u
  mp6 5 6 8 10 pmos W=117u L=3.6u
  mn3 1 4 2 2 nmos W=144u L=3.6u
  mn4 5 4 3 3 nmos W=144u L=3.6u
  mn1 2 1 0 0 nmos W=72u L=7.2u
  mn2 3 1 0 0 nmos W=72u L=7.2u

  mp12 13 9 10 10 pmos W=111.6u L=7.2u
  mp11 12 6 13 10 pmos W=90.7u L=3.6u
  mn10 12 4 11 11 nmos W=111.6u L=3.6u
  mn9 11 1 0 0 nmos W=55.8u L=7.2u
.ends mirrorcofficient1
.subckt adaptor0  1 3 4 5  6 7 8 9 10
*7~10 are DC bias voltages
xcm1 1 2 7 8 9 10  mirrorcell
xcm2 3 4 2 7 8 9 10  mirrorcell2
xcm3 5 6 2 7 8 9 10  mirrorcell2
xcm4 2 4 6 7 8 9 10  mirrorcofficient1
.ends adaptor0
************************************************
* wave adaptor1 in elliptic SI wave filter
.subckt mirrorcofficient2  1 5  12 10 6 4 9
  mp7 7 9 10 10 pmos W=144u L=7.2u
  mp8 8 9 10 10 pmos W=144u L=7.2u
  mp5 1 6 7 10 pmos W=117u L=3.6u
  mp6 5 6 8 10 pmos W=117u L=3.6u
  mn3 1 4 2 2 nmos W=144u L=3.6u
  mn4 5 4 3 3 nmos W=144u L=3.6u
  mn1 2 1 0 0 nmos W=72u L=7.2u
  mn2 3 1 0 0 nmos W=72u L=7.2u
```

```
    mp12 13 9 10 10 pmos W=15.8u L=7.2u
    mp11 12 6 13 10 pmos W=12.9u L=3.6u
    mn10 12 4 11 11 nmos W=15.8u L=3.6u
    mn9 11 1 0 0 nmos W=7.9u L=7.2u
 .ends mirrorcofficient2
.subckt mirrorcofficient3  1 5  12 10 6 4 9
    mp7 7 9 10 10 pmos W=144u L=7.2u
    mp8 8 9 10 10 pmos W=144u L=7.2u
    mp5 1 6 7 10 pmos W=117u L=3.6u
    mp6 5 6 8 10 pmos W=117u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=72u L=7.2u
    mn2 3 1 0 0 nmos W=72u L=7.2u

    mp12 13 9 10 10 pmos W=128.2u L=7.2u
    mp11 12 6 13 10 pmos W=104u L=3.6u
    mn10 12 4 11 11 nmos W=128.2u L=3.6u
    mn9 11 1 0 0 nmos W=64.1u L=7.2u
 .ends mirrorcofficient3
.subckt adaptor1  1 2 4 5  6 7 8 9 10 11
 *8~11 are DC bias voltages
xcm1 1 2 3 8 9 10 11  mirrorcofficient2
xcm2 4 5 3  8 9 10 11 mirrorcell2
xcm3 6 7 3 8 9 10 11  mirrorcofficient3
xcm4 3 2 5  7 8 9 10 11  mirrorcell3
.ends adaptor1
************************************************
* wave adaptor2 in elliptic SI wave filter
.subckt mirrorcofficient3  1 5 12 15 10 6 4 9
    mp7 7 9 10 10 pmos W=144u L=7.2u
    mp8 8 9 10 10 pmos W=144u L=7.2u
    mp5 1 6 7 10 pmos W=117u L=3.6u
    mp6 5 6 8 10 pmos W=117u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
```

```
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=72u L=7.2u
    mn2 3 1 0 0 nmos W=72u L=7.2u

    mp12 13 9 10 10 pmos W=64.4u L=7.2u
    mp11 12 6 13 10 pmos W=117u L=3.6u
    mn10 12 4 11 11 nmos W=52.3u L=3.6u
    mn9 11 1 0 0 nmos W=32.2u L=7.2u

    mp16 16 9 10 10 pmos W=79.6u L=7.2u
    mp15 15 6 16 10 pmos W=64.7u L=3.6u
    mn14 15 4 14 14 nmos W=79.6u L=3.6u
    mn13 14 1 0 0 nmos W=39.8u L=7.2u
 .ends mirrorcofficient3
.subckt adaptor2  1 2 4 5  6 7 8 9 10 11
 *8~11 are DC bias voltages
xcm1 1 2 3 8  9 10 11  mirrorcell2
xcm2 4 5 3 8  9 10 11  mirrorcell2
xcm3 6 7 3 8 9 10 11  mirrorcell2
xcm4 3 2 5  7 8 9 10 11  mirrorcofficient3
.ends adaptor2
*********************************************
* wave adaptor3 in elliptic SI wave filter
.subckt mirrorcofficient4  1 5 12 15 10 6 4 9
   mp7 7 9 10 10 pmos W=144u L=7.2u
   mp8 8 9 10 10 pmos W=28.8u L=7.2u
   mp5 1 6 7 10 pmos W=117u L=3.6u
   mp6 5 6 8 10 pmos W=23.4u L=3.6u
   mn3 1 4 2 2 nmos W=144u L=3.6u
   mn4 5 4 3 3 nmos W=28.8u L=3.6u
   mn1 2 1 0 0 nmos W=72u L=7.2u
   mn2 3 1 0 0 nmos W=14.4u L=7.2u

   mp12 13 9 10 10 pmos W=57.6u L=7.2u
   mp11 12 6 13 10 pmos W=46.8u L=3.6u
```

```
    mn10 12 4 11 11 nmos W=57.6u L=3.6u
    mn9 11 1 0 0 nmos W=28.8u L=7.2u

    mp16 16 9 10 10 pmos W=201.6u L=7.2u
    mp15 15 6 16 10 pmos W=163.8u L=3.6u
    mn14 15 4 14 14 nmos W=201.6u L=3.6u
    mn13 14 1 0 0 nmos W=100.8u L=7.2u
 .ends mirrorcofficient4
.subckt adaptor3  1 2 4 5  6 7 8 9 10
 * 7~10  are DC bias voltages
xcm1 1 2 3 7 8  9 10  mirrorcell2
xcm2 4 5 3 7 8  9 10  mirrorcell2
xcm3 3 2 6 5  7 8 9 10  mirrorcofficient4
.ends adaptor3
************************************************
*input-output circuit in SI group delay wave equalizer
.subckt mirrorcofficient5  1 5  12 10 6 4 9
   mp7 7 9 10 10 pmos W=144u L=7.2u
   mp8 8 9 10 10 pmos W=144u L=7.2u
   mp5 1 6 7 10 pmos W=117u L=3.6u
   mp6 5 6 8 10 pmos W=117u L=3.6u
   mn3 1 4 2 2 nmos W=144u L=3.6u
   mn4 5 4 3 3 nmos W=144u L=3.6u
   mn1 2 1 0 0 nmos W=72u L=7.2u
   mn2 3 1 0 0 nmos W=72u L=7.2u

   mp12 13 9 10 10 pmos W=288u L=7.2u
   mp11 12 6 13 10 pmos W=234u L=3.6u
   mn10 12 4 11 11 nmos W=288u L=3.6u
   mn9 11 1 0 0 nmos W=144u L=7.2u
.ends mirrorcofficient5
.subckt inputoutput  1 3 4 5  6 7 8 9
 *6~9  are DC bias voltages
xcm1 1 2 3 6 7 8 9  mirrorcofficient5
xcm2 3 4 2 6 7 8 9   mirrorcell2
```

```
xcm3 2 5 6 7 8 9  mirrorcell
.ends inputoutput
**********************************************
*wave converters in SI group delay equalizer
.subckt converter  1 2 3 5  6 7 8 9
 *6~9 are DC bias voltages
xcm1 1 2 3 6 7 8 9  mirrorcell2
xcm2 3 4  6 7 8 9  mirrorcell
xcm3 4 2 5 6 7 8 9  mirrorcell2
.ends converter
**********************************************
* wave adaptor4 in SI group delay equalizer
 .subckt  mirrorcofficient6 1 5 12 10 6 4 9
   mp7 7 9 10 10 pmos W=144u L=7.2u
   mp8 8 9 10 10 pmos W=144u L=7.2u
   mp5 1 6 7 10 pmos W=117u L=3.6u
   mp6 5 6 8 10 pmos W=117u L=3.6u
   mn3 1 4 2 2 nmos W=144u L=3.6u
   mn4 5 4 3 3 nmos W=144u L=3.6u
   mn1 2 1 0 0 nmos W=72u L=7.2u
   mn2 3 1 0 0 nmos W=72u L=7.2u

   mp12 13 9 10 10 pmos W=152u L=7.2u
   mp11 12 6 13 10 pmos W=123.3u L=3.6u
   mn10 12 4 11 11 nmos W=152u L=3.6u
   mn9 11 1 0 0 nmos W=76u L=7.2u
.ends mirrorcofficient6
.subckt  mirrorcofficient7 1 5 12 10 6 4 9
   mp7 7 9 10 10 pmos W=144u L=7.2u
   mp8 8 9 10 10 pmos W=144u L=7.2u
   mp5 1 6 7 10 pmos W=117u L=3.6u
   mp6 5 6 8 10 pmos W=117u L=3.6u
   mn3 1 4 2 2 nmos W=144u L=3.6u
   mn4 5 4 3 3 nmos W=144u L=3.6u
   mn1 2 1 0 0 nmos W=72u L=7.2u
```

```
    mn2 3 1 0 0 nmos W=72u L=7.2u

    mp12 13 9 10 10 pmos W=120.7u L=7.2u
    mp11 12 6 13 10 pmos W=98u L=3.6u
    mn10 12 4 11 11 nmos W=120.7u L=3.6u
    mn9 11 1 0 0 nmos W=60.3u L=7.2u
  .ends mirrorcofficient7
 .subckt  mirrorcofficient8 1 5 12 10 6 4 9
    mp7 7 9 10 10 pmos W=144u L=7.2u
    mp8 8 9 10 10 pmos W=144u L=7.2u
    mp5 1 6 7 10 pmos W=117u L=3.6u
    mp6 5 6 8 10 pmos W=117u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=72u L=7.2u
    mn2 3 1 0 0 nmos W=72u L=7.2u

    mp12 13 9 10 10 pmos W=15.6u L=7.2u
    mp11 12 6 13 10 pmos W=12.7u L=3.6u
    mn10 12 4 11 11 nmos W=15.6u L=3.6u
    mn9 11 1 0 0 nmos W=7.8u L=7.2u
 .ends mirrorcofficient8
.subckt adaptor4  1 2 4 5  6 7 8 9 10 11
 *8~11  are DC bias voltages
xcm1 1 2 3 8  9 10 11 mirrorcofficient6
xcm2 4 5 3 8  9 10 11  mirrorcofficient7
xcm3 6  7 3 8  9 10 11  mirrorcofficient8
xcm4 3 7 5 2 8 9 10 11 mirrorcell3
.ends adaptor4
*********************************************
* wave adaptor5 in SI group delay equalizer
 .subckt  mirrorcofficient9 1 5 12 10 6 4 9
   mp7 7 9 10 10 pmos W=144u L=7.2u
   mp8 8 9 10 10 pmos W=144u L=7.2u
   mp5 1 6 7 10 pmos W=117u L=3.6u
```

```
    mp6 5 6 8 10 pmos W=117u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=72u L=7.2u
    mn2 3 1 0 0 nmos W=72u L=7.2u

    mp12 13 9 10 10 pmos W=19u L=7.2u
    mp11 12 6 13 10 pmos W=15.4u L=3.6u
    mn10 12 4 11 11 nmos W=19u L=3.6u
    mn9 11 1 0 0 nmos W=9.5u L=7.2u
 .ends mirrorcofficient9
.subckt  mirrorcofficient10 1 5 12 10 6 4 9
    mp7 7 9 10 10 pmos W=144u L=7.2u
    mp8 8 9 10 10 pmos W=144u L=7.2u
    mp5 1 6 7 10 pmos W=117u L=3.6u
    mp6 5 6 8 10 pmos W=117u L=3.6u
    mn3 1 4 2 2 nmos W=144u L=3.6u
    mn4 5 4 3 3 nmos W=144u L=3.6u
    mn1 2 1 0 0 nmos W=72u L=7.2u
    mn2 3 1 0 0 nmos W=72u L=7.2u

    mp12 13 9 10 10 pmos W=269u L=7.2u
    mp11 12 6 13 10 pmos W=218.6u L=3.6u
    mn10 12 4 11 11 nmos W=269u L=3.6u
    mn9 11 1 0 0 nmos W=134.5u L=7.2u
 .ends mirrorcofficient10
.subckt adaptor5  1 2 4 5  6 7 8 9
 *1~5 are inputs and outputs of wave adaptor1, 6~9 are DC bias voltages
xcm1 1 2 3 6 7 8 9  mirrorcofficient9
xcm2 4 5 3 6 7 8 9  mirrorcofficient10
xcm3 3 2 5 6  7 8 9  mirrorcell2
.ends adaptor5
*****************************************
 vdd 1 0 dc 3.3
 vpmos1 2 0 dc 0.3
```

```
vnmos 3 0 dc 2
vpmos2 40  0 dc 1.85
iin 0 4 sin(0 10uA 10kHz 1us)
xdelay1 4 5 60 61 62 63 1 2 3 40 delaycell
xadaptor0 5 6 7 8 9 1 2 3 40 adaptor0
xcm1 7 10 1 2 3 40  mirrorcell
xdelay2 9 8 60 61 62 63 1 2 3 40 delaycell
xadaptor1 10 11 12 13 14 6 1 2 3 40 adaptor1
xadaptor2 11 15 16 17 18 19 1 2 3 40 adaptor2
xcm2 15 14 1 2 3 40 mirrorcell
xcm3 19 20 1 2 3 40  mirrorcell
xdelay3 17 16 60 61 62 63 1 2 3 40 delaycell
xdelay4 20 18 60 61 62 63 1 2 3 40 delaycell
xadaptor3 13 21 22 23 24 1 2 3 40 adaptor3
xdelay5 24 22 60 61 62 63 1 2 3 40 delaycell
xcm4 21 12 1 2 3 40 mirrorcell
xcm5 24 25 1 2 3 40 mirrorcell
xinout 25 26 27 28 1 2 3 40  inputoutput
xconverter 29 26 27 30 1 2 3 40  converter
xadaptor4 30 29 31 32 33 34 1 2 3 40  adaptor4
xdelay6 32 35 60 61 62 63 1 2 3 40  delaycell
xdelay7 34 33 60 61 62 63 1 2 3 40 delaycell
xadaptor5 35 31 36 37 1 2 3 40 adaptor5
xdelay8 37 36 60 61 62 63 1 2 3 40 delaycell
cl 28 38 10mf
rl 38 0 15k
*clock1
vclkn1 60 0 pulse (5V 0V 1.4us 0.025us 0.025us 0.55us 1us)
vclkp1 61 0 pulse (0V 5V 1.4us 0.025us 0.025us 0.55us 1us)
*clock2
vclkn2 62 0 pulse (5V 0V 0.9us 0.025us 0.025us 0.55us 1us)
vclkp2 63 0 pulse (0V 5V 0.9us 0.025us 0.025us 0.55us 1us)
.tran 0.1us 100us
.probe
.end
```