UNIVERSITY OF SOUTHAMPTON

Fabrication of Lateral Silicon Germanium Heterojunction Bipolar Transistors

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ABSTRACT

ELECTRONICS AND COMPUTER SCIENCE

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FABRICATION OF LATERAL SILICON GERMANIUM HETEROJUNCTION BIPOLAR TRANSISTORS

By Khairil Osman

The fabrication of lateral SiGe heterojunction bipolar transistors requires the development of new processing stages, device design and modelling. In this work, techniques for cavity fabrication, surface preparation and confined selective epitaxial growth are developed and a new design of lateral SiGe heterojunction transistor is proposed.

Two types of cavity were fabricated in this work, the open-sided cavity and the SOI cavity. The open-sided cavity allows confined growth to be carried out from a planar seed window, while the SOI cavity allows growth from a vertical (sidewall) seed. To ensure warp-free and rigid structures, the wall of the cavities has to be made from an LTO/nitride/LTO sandwich. For sacrificial etching, the use of dry (SF_6) and wet etch (KOH) processes were found to be suitable for the removal of polysilicon/silicon sacrificial layer, however, the use of wet processing meant a higher probability of stiction. It is also shown that the fabrication of SOI cavities should include a silicon sidewall rippling reduction step (using KOH), to create an epi-ready vertical seed.

Silane-only selective epitaxy is found to give good quality epitaxial layers, however the growth thickness that can be achieved before selectivity is lost is limited by an incubation period of ~30 minutes. In addition, the high growth temperature (980°C) is found to cause oxide pitting and etching at silicon/oxide sidewall areas. Furthermore, development for a selective silicon germanium process at low temperatures has so far led to non-selective growth.

A new $DCS/SiH_4/H_2$ epitaxy process has been established that provides good quality selective epitaxial layers at between 750°C – 930°C. At 850°C, uniformity was found to be +/- 5%, with a vertical and lateral growth rate (from a planar seed) of 38 nm/min and 11 nm/min, respectively. Confined and unconfined lateral growth from a vertical seed of up to 0.5 μm and 1 μm, respectively, has been demonstrated. The epitaxy process, which has an activation energy of 2.4eV, was found to be largely unaffected by any local loading effects. In addition, silicon germanium epitaxial layers have also been successfully grown. As with the silane-only process, $DCS/SiH_4/H_2$ growth, selectivity is found to be lost after an incubation period, which at 850°C is close to 90 minutes.

Based on the cavity and epitaxy processes that have been developed, a lateral SiGe heterojunction bipolar transistor has been proposed. From simulations, the design shows promise, with f_T and f_{max} figures of 2.0 and 8.0 GHz, respectively. With further development in the $DCS/SiH_4/H_2$ epitaxy process to allow *in situ* doping, the design may achieve an f_T and f_{max} figure of 6.3 and 15.8 GHz, respectively. Further scaling and design optimisation is likely to yield high performance devices.

Contents

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Chapter 1

Introduction

Over the last few years, the rapid growth in the communications and internet sector has spurred the development of circuits and devices that operate at higher frequencies (above 1GHz) while using less power and maintaining economic viability. The increasing demand for highly integrated wireless consumer and business products such as Personal Digital Assistants (PDAs), home and office networking, and mobile phones has been the main driving force behind this growth. One reason for this is the sheer high volume of the market, and the huge potential profitability. Gallium Arsenide and indium phosphide metal semiconductor field effect transistors (MESFETs) and heterojunction bipolar transistors (HBTs) are important high frequency devices [1-3], however, these technologies are expensive when compared to silicon based devices and not readily integrated with CMOS. SiGe based heterojunction bipolar transistors are rapidly gaining prominence as they can be integrated with CMOS and share many of the advantages of other commercial silicon technologies such as high yield, high output and low cost. They can also bring improvements in terms of higher gain and cut off frequency (f_T), better low noise figure, excellent linearity, more stable operation over a wide temperature range and higher resistance to radiation exposure [4].

Over the last 15 years, silicon bipolar technology has matured, and self-aligned transistors with abrupt doping profiles have brought about devices with high cut-off frequencies. So far, silicon bipolar transistors with cut-off frequencies (f_T) and

maximum frequencies (f_{max}) of 30 to 50 GHz have been manufactured [5, 6]. Over the same period, SiGe technology has also progressed and has pushed silicon based bipolar transistors to higher levels of performance. SiGe HBTs now readily attain f_{max} of over 100 GHz [7]. More impressively, modern SiGe HBTs produced on silicon-on-insulator (SOI) substrates have achieved cut-off frequencies of over 350 GHz [8]. This level of performance has allowed SiGe HBTs to begin to replace the traditional markets of III-V compound semiconductors such as GaAs and InP. SiGe technology has become the technology of choice to meet the current demand for high frequency low cost devices.

Many of the design aspects incorporated into SiGe heterojunction bipolar transistors, such as self-alignment, deep and shallow trench isolation and double polysilicon base contacting, have been taken from modern silicon homojunction bipolar transistor design. However, the use of SiGe has required considerable divergence from the standard methods used to fabricate bipolar junction transistors. For example, the use of ion implantation to define the base region has had to be replaced by epitaxial methods. The use of epitaxial growth technologies such as molecular beam epitaxy (MBE), ultra-high vacuum chemical vapour deposition (UHV/CVD) and low pressure chemical vapour deposition (LPCVD) are now employed to grow stable strained SiGe layers. It first appeared that expensive modifications would be required to adapt existing production lines (including both circuit design and device fabrication) to include SiGe layers. However, in practice, lines have adapted economically and with relative ease and SiGe technology has already been successfully incorporated into several commercial fabrication facilities [1, 9].

So far only vertical heterojunction bipolar transistors have been produced, however, the advancement of photolithographic techniques towards smaller feature size raises the prospect of high-frequency "lateral" bipolar transistors in which collector, base and emitter regions can be directly contacted [10-12]. A lateral structure should allow the fabrication of transistors with smaller parasitic resistances and capacitances, (particularly extrinsic base resistance and collector-base junction capacitance), than exist in vertical bipolar transistors. If properly exploited, this in turn should translate to improved frequency performance [13]. Lateral bipolar transistors also operate at lower operating currents, making them suitable for low power applications [14]. Furthermore, the lower vertical profiles of lateral transistors also make them more compatible with

complementary metal oxide semiconductor (CMOS) processing.

In the past, the performance of lateral bipolar transistors has been limited by large base widths, which have usually been determined by lithographic resolution. With the advent of deep sub-micron lithography, the base width can now be greatly reduced, and this can directly lead to increased f_T and f_{max}. In addition, the use of spacers, controlled dopant diffusion and novel etching techniques have also been used to further assist the formation of narrow base regions and align base contacts [14-18]. The progress in SOI technology has also contributed to the resurgence of interest in lateral bipolar transistors. The isolation of lateral devices from bulk silicon was always a difficulty and this is now readily solved by the use of SOI. Currently, lateral homojunction bipolar transistors on SOI can achieve an f_T of up to 20GHz [14]. This is considerably lower performance than typically obtained for vertical homojunction bipolar transistors however, if lateral device fabrication techniques were allowed to mature to a point where lithographic features are similar to those utilised by vertical devices then the fundamental advantages of lateral design should lead to faster devices.

As yet, SiGe has not been successfully incorporated into lateral bipolar junction transistors, however, simulations of lateral SiGe heterojunction bipolar transistors have been reported by Neudeck *et al.* and Tang *et al.* [15, 19]. One of the problems of applying SiGe technology to lateral bipolar transistors is finding a suitable method to incorporate germanium into the base. Unconfined SiGe growth proceeds uniformly in all directions. To fabricate a lateral bipolar transistor, epitaxial growth has to somehow be confined vertically in order to ensure growth occurs only in the lateral direction. One method that can be used to achieve this is confined lateral selective epitaxial growth (CLSEG) a technique pioneered by Neudeck *et al.* [20].

Tang *et al.* carried out a detailed comparison of a lateral SiGe HBT with a state-of-the-art vertical SiGe HBT. Simulations showed that by exploiting confined lateral selective epitaxial growth a lateral SiGe heterojunction bipolar transistor, using SOI and deep sub-micron lithography, could achieve an f_T and f_{max} of 33 GHz and 160 GHz, respectively [19]. With further design improvements it seems likely that f_{max} could be pushed to 220 GHz [19]. This shows that lateral SiGe HBTs can achieve performance levels similar to those of comparable vertical HBTs. Figure 1.1 below shows the f_{max}

trend of vertical HBTs over the years. It also marks the level of performance that can be achieved from lateral SiGe HBTs. It is worth noting that the value of 220 GHz quoted for the lateral SiGe HBT was based on fabrication technology in 2001.

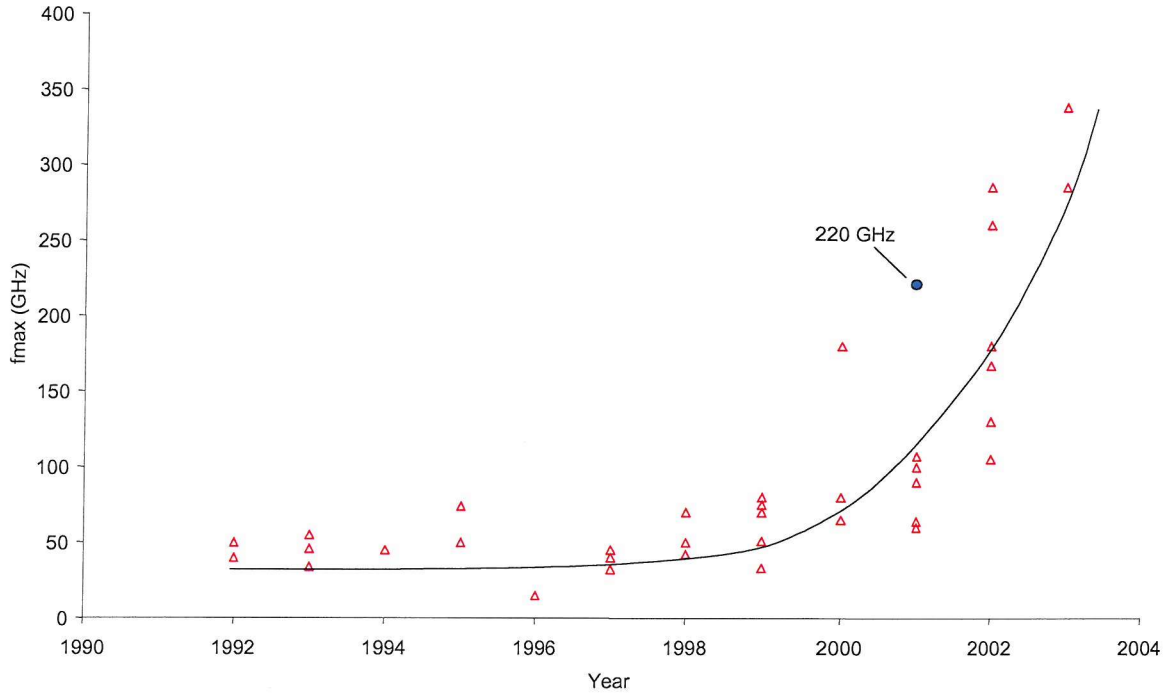


Fig. 1.1 f_{max} trend of vertical SiGe HBT over the years. The dashed line shows the possible f_{max} of a lateral SiGe HBT, as proposed by Tang [19]. The value of 220 GHz for the lateral SiGe HBT is based on fabrication technology circa 2001 (see appendix B for references).

The objective of this work is to examine the feasibility of fabricating a lateral heterojunction bipolar transistor by confined lateral selective epitaxial growth (CLSEG) using the extensive facilities available at Southampton University Microelectronics Centre.

This thesis is arranged as follows. In chapter 2, the theory of heterojunction bipolar transistors is presented. The chapter will look at the advantages of lateral bipolar transistors over vertical bipolar transistors, and present a method of fabricating a lateral SiGe heterojunction bipolar transistor. In chapter 3, an overview of chemical vapour deposition is presented. The chapter will particularly look at epitaxy growth, including

aspects that are related to it such as selectivity, faceting and epitaxy quality. In chapter 4, the work will look at cavity fabrication, which is an important requirement for the fabrication of a lateral SiGe heterojunction bipolar transistor. Developments of selective epitaxial growth techniques are described in Chapters 5 and 6. In chapter 7, simulations of lateral SiGe HBTs are presented. Finally, in chapter 8, conclusions and future work are presented.

Chapter 2

Bipolar Transistor Theory

This chapter will begin by looking at silicon homojunction bipolar theory and will serve as a foundation for the silicon germanium heterojunction bipolar theory which follows. Although, in theory the principal operations of the two transistors are the same, the addition of germane to form a strained silicon germanium base region greatly enhances the performance of heterojunction bipolar devices. So far, the majority of high frequency bipolar transistors have been vertical devices, even though lateral devices could theoretically have lower parasitics and hence, better performance. The limited usage of lateral devices is largely due to technological limitations (e.g. lithography, epitaxy). However, with recent developments in epitaxial growth techniques such as confined lateral selective epitaxial growth (CLSEG), low power, high frequency lateral silicon germanium devices could now be fabricated. In this chapter, the issues related to the design and fabrication of bipolar transistors will be examined.

2.1 Bipolar Transistor Theory

The operation of a silicon homojunction bipolar transistor can be understood by looking at the emitter-base junction, (figure 2.1). The band diagram in solid lines shows

the formation of the junction when unbiased. In this state, the diffusion and drift currents which result from the formation of the p-type and n-type junction are at equilibrium. V_0 is the natural built in voltage which results from the diffusion of electrons in the conduction band (E_C) from the n-type emitter to the p-type base, and holes in the valence band (E_V) from the p-type base to the n-type emitter regions. The built-in voltage that is formed prevents further net diffusion of carriers between the base and emitter regions. This results in zero net current. When the transistor is biased in the forward active region, the emitter-base region is forward biased, while the collector-base region is reverse biased. When the emitter-base junction is forward biased by a voltage, V_a, the potential barrier is reduced, as shown by the band diagram in dashed lines and electrons are injected from the emitter into the base region. Similarly, holes in the base are injected into the emitter. Electrons that are injected into the base, become minority carriers, which can diffuse across the base region before being swept into the collector by the reversed biased base-collector junction. Thus, the result of a forward biased emitter-base junction, should be a large flow of current between the collector and the emitter.

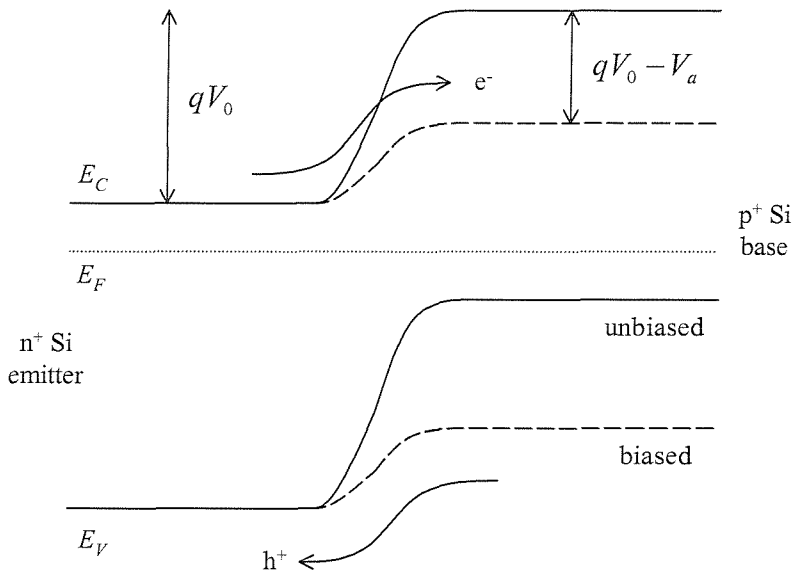


Fig. 2.1 Band diagram of emitter-base junction of a silicon homojunction bipolar transistor.

Figure 2.2 shows the main electron and hole current components of a transistor in the forward active mode of operation. The largest current component is the flow of electrons from emitter to base (I_{ne}). Holes will also cross the emitter-base depletion region giving rise to part of the base current, I_{pe}. Most electrons injected into the base will diffuse into the collector-base depletion region and will then be swept into the collector (I_{nc}). In a well designed transistor $I_{ne} \sim I_{nc}$, however some electrons will recombine with holes in the p-type base region giving rise to the second significant component of the base current (I_{rb}). Although the majority of holes and electrons drift across the emitter-base depletion region some recombination does occur (I_{rg}),

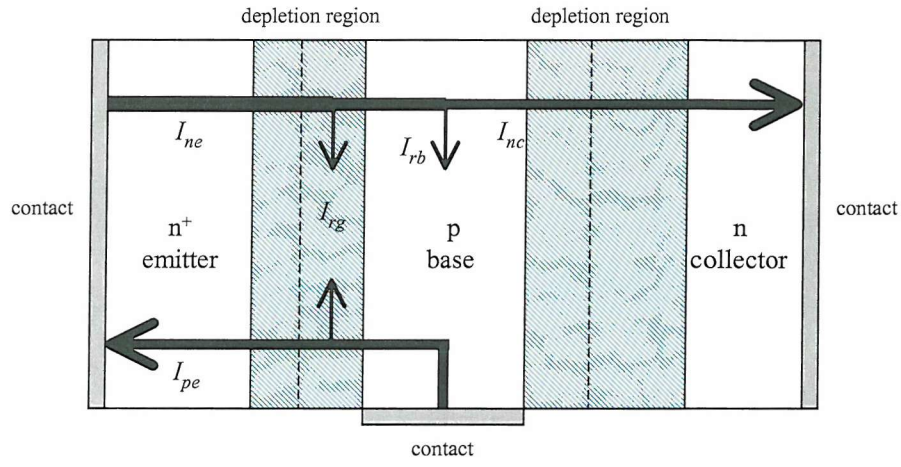


fig 2.2 Current components in an n^+pn bipolar transistor in the forward active mode of operation. After Ashburn [21].

A good, high gain, device requires the collector current to be much greater than the base current. Already, by examining the principle current components, we can see how this can be readily achieved by heavily doping the emitter (so that $I_{ne} >> I_{pe}$), and by making the base width narrow (so that I_{rb} is small).

So, in most modern bipolar transistors, the width of the base is narrow. This means that the amount of electron recombination that occurs in the base is often negligible ($I_{rb} << I_{pe}$). Based on this assumption, to a good first approximation, I_{nc}, which is effectively also the collector current, I_C, is be given by [21]

$$I_{nc} = I_C = -\frac{qAD_{nb}n_i^2}{W_B N_{ab}} \exp\frac{qV_{BE}}{\eta kT} \tag{2.1}$$

where q is electron charge, A is area, D_{nb} is the diffusivity of electrons in the base, n_i is the intrinsic silicon concentration, W_B is the width of the base, N_{ab} is base doping, V_{BE} is the base-emitter voltage, η is the ideality factor, k is Boltzmann's constant and T is the temperature. Based on figure 2.2, base current, I_B, is given by

$$I_B = I_{pe} + I_{rg} + I_{rb} \tag{2.2}$$

To a first approximation, I_{rg} and I_{rb}, can be neglected. This gives an equation for base current which is determined by hole injection into the emitter [21]

$$I_B = -\frac{qAD_{pe}n_i^2}{L_{pe}N_{de}} \exp\frac{qV_{BE}}{\eta kT} \tag{2.3}$$

where D_{pe} is the hole diffusivity in the emitter, L_{pe} is the diffusion length of holes in the emitter and N_{de} is the emitter doping concentration. Taking the ratio of collector current to base current gives the transistor common emitter current gain, β which is given by,

$$\beta = \frac{I_C}{I_B} = \frac{D_{nb}L_{pe}N_{de}}{D_{pe}W_B N_{ab}} \tag{2.4}$$

If the width of the emitter is smaller than the hole diffusion length then L_{pe} can be replaced by the emitter width, W_E. Although this equation shows that the common emitter current gain can be increased by increasing L_{pe} (or W_E) and N_{de} while reducing W_B and N_{ab}, in practice, it is necessary to take into account other aspects of the transistors performance. For example, as we will see in the following section, base resistance and collector-base junction capacitance affect a transistor's frequency performance. So, to obtain a low base resistance, high base doping is necessary. But according to equation 2.4, this increase in doping would result in a reduction in current gain. Hence, a trade-off is required and in practise, a current gain of ~100 is often chosen to be a good compromise [21].

2.2 Frequency Performance

The frequency performance of a bipolar transistor is often of paramount importance, and in this regard the cut-off frequency (f_T) is often used as a figure of merit. It is defined as the frequency at which the common emitter short circuit a.c. current gain is unity [21]. Physically, the cut off frequency relates to the delay experienced by a minority carrier crossing from emitter to collector. The cut off frequency is given by,

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{2.5}$$

where τ_{ec} is composed of several delay terms which are,

$$\tau_{ec} = \tau_e + \tau_{ebd} + \tau_b + \tau_{cbd} + \tau_{je} + \tau_c^{'} \tag{2.6}$$

where τ_e and τ_{ebd} are the delays due to excess minority carriers in the emitter and emitter-base depletion layers.

The base transit time τ_b is the delay due to excess minority carriers in the base and is given by,

$$\tau_b = \frac{W_b^2}{\alpha D_{nb}} \tag{2.7}$$

where W_b is the neutral base width, D_{nb} is the minority carrier diffusion coefficient and α is a constant that depends on the base doping profile ($\alpha = 2$ for a uniformly doped base). To reduce τ_b (and increase f_T) the width of the transistor, W_b has to be minimised.

τ_{cbd} is the collector depletion layer transit time. It represents the delay at the collector-base depletion region. τ_{cbd} is given by [22],

$$\tau_{cbd} = \frac{W_{jbc}}{2v_{scl}} \tag{2.8}$$

where W_{jbc} is the width of the collector base junction depletion layer and v_{scl} is the carrier scattering limited velocity, which is approximately equal to $1\times10^{7}\,\mathrm{cms}^{-1}$ [23]. For high speed devices, as the base width τ_b is reduced, τ_{cbd} becomes significant.

τ_{je} is the total emitter depletion layer charging time and is given by [24],

$$\tau_{je} \approx \frac{kT}{qI_c}(C_{jbe} + C_{jbc}) \tag{2.9}$$

where C_{jbe} and C_{jbc} are the emitter-base and collector-base junction capacitances.

τ'_c is the collector charging time and is given by [25],

$$\tau'_c = R_c C_{jbc} \tag{2.10}$$

where R_c and C_{jbc} are the collector resistance and collector base junction capacitance, respectively. The significance of τ'_c can be reduced by making R_c small, in modern devices this can be achieved by using and an epitaxial collector.

Substituting each delay term into the f_T equation gives ,

$$f_T = \frac{1}{2\pi}\left(\frac{kT}{qI_c}(C_{jbe} + C_{jbc}) + \frac{W_b^2}{\alpha D_{nb}} + \tau_e + \tau_{ebd} + \frac{W_{jbc}}{2v_{scl}} + R_c C_{jbc}\right)^{-1} \tag{2.11}$$

A curve of f_T versus collector current, shown below, shows that f_T increases with collector current. It peaks at a certain value of collector current and then rapidly falls. At low collector current, τ_{je} is the dominant delay term. However, at higher frequencies the effect of τ_{je} reduces drastically. At peak f_T, the dominant terms for an optimal transistor design are τ_{je}, τ_b and τ_{cbd} [21]. Hence, to increase f_T, these three delay terms must be minimised.

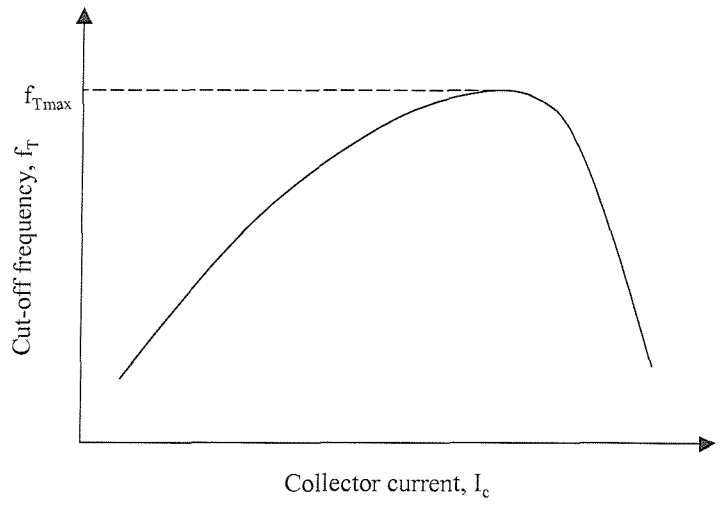


Figure 2.3 f_T versus collector current.

The value of f_T is based on a model in which the transistor's output is short-circuited, it is therefore, not an entirely realistic figure of merit to use. f_T also fails to take into account base resistance and the collector-base depletion capacitance, a time constant which affects high frequency performance.

A better figure of merit to use is f_{max}, which is defined as the frequency at which the unilateral power gain becomes unity. With f_{max}, the output of the transistor is isolated from the input by an external circuit with reactive and resistive components. The load is assumed to be conjugately matched to the transistor's output impedance. f_{max} is given by [26],

$$f_{\max} = \sqrt{\frac{f_T}{8\pi C_{jbc} R_b}} \tag{2.12}$$

where R_b is the total base resistance. Hence, to achieve high frequency operation, base resistance and collector-base capacitance have to be minimised. In modern bipolar transistors, the base width is made ever smaller to achieve lower base transit times and high f_T. As explained earlier, the reduction in base width increases base resistance, which from the equation above reduces f_{max}. To counter this, the base doping can be

increased. This has to be matched with a reduction in emitter doping to prevent emitter-base junction tunnelling, but this in turn will result in the reduction of gain.

However, with the introduction of germanium to form a SiGe base, current gain can be enhanced. In fact, the main advantage of the addition of germanium is that it gives extra freedom to heterojunction bipolar transistor designers, allowing unnecessary increases in transistor performance, principally gain, to be traded-off for alternative performance gains such as lower power operation at a given operational frequency.

2.3 Heterojunction Bipolar Transistors

The addition of silicon germanium into silicon epitaxial layers to form strained silicon germanium layers can allow large improvements in transistor performance. Before considering the impact of the use of a SiGe base region on transistor parameters we will first look at the important material properties of SiGe in order to understand how the alloy offers enormous advantages over traditional silicon BJTs.

Silicon and silicon germanium have different lattice constants. At 300K, they are 5.43Å and 5.66Å, respectively. When silicon germanium is grown on silicon the lattice mismatch will lead to a strained or a relaxed SiGe layer. A strained (or pseudomorphic) SiGe layer has a lattice constant that gradually changes from that of silicon to that of relaxed silicon germanium. The whole structure is strain compensated with compressive strain in the SiGe layer and tensile strain in the silicon layer [27]. In a relaxed structure the strain is released by the presence of misfit dislocations at the Si/SiGe interface. The presence of misfit dislocations, and associated recombination centres impairs the performance of devices and reduces yield. Figure 2.4 shows a schematic demonstrating the difference between strained and relaxed layers.

There are several factors which influence the formation of misfit dislocations, mainly layer thickness, germanium content and temperature. The thickness at which a strained SiGe layer relaxes as a result of the build up of stress beyond a certain threshold is

called the critical thickness. In a SiGe HBT the critical thickness determines the maximum possible basewidth, and in most cases to avoid device degradation it is wise to have a basewidth well below the critical thickness. With a silicon capping layer, the thickness of the SiGe can be almost double that of an uncapped layer. This is convenient in a SiGe HBT, as the capping layer would form the emitter of the transistor [28, 29]. Since the SiGe lattice constant changes with germanium content, the critical thickness is also dependent on germanium content, so lower germanium concentrations allows thicker layers. Besides thickness, the stability of layers is also dependent on temperature. Layers are often in a thermally metastable state whereby, after a high temperature process, such as annealing, the layer can relax. Figure 2.5 shows a plot of critical thickness for different germanium concentration for capped and uncapped SiGe layers.

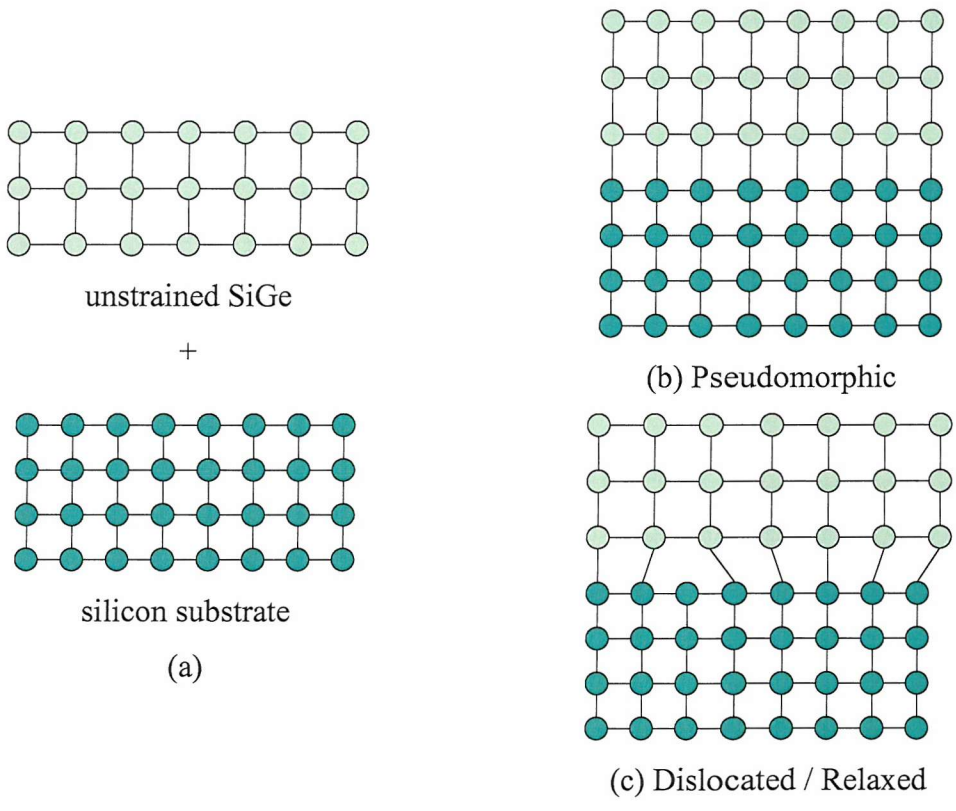


Fig. 2.4 A two dimensional crystal representation of Si and SiGe crystal structure (a) Growth of SiGe on a Si substrate (b) Pseudomorphic structure (c) Dislocated structure. After Iyer *et al.* [27].

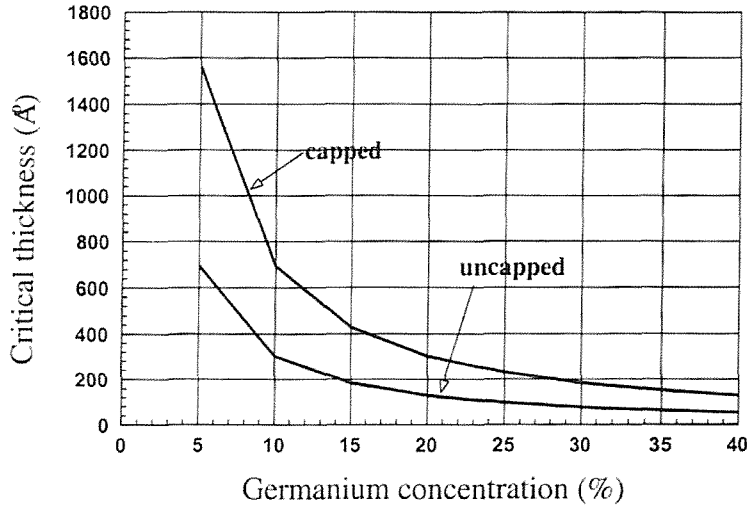


Fig. 2.5 Critical thickness of capped and uncapped SiGe layers with different germanium concentrations. After Hull *et al.* and Green *et al.* [30, 31].

The enhanced performance of a SiGe heterojunction bipolar transistor over silicon homojunction transistor is for the most part attributed to the ability to decrease the potential barrier presented to electrons at the emitter-base junction. In addition to bandgap engineering by changing the geramium concentration the presence of strain in the SiGe also causes valence and conduction band splitting [32], resulting in an even smaller bandgap (figure 2.6).

So, in a SiGe HBT the composition and thickness of the SiGe base are crucial parameters determining the electrical characteristics of the device. Practical limitations that result from the material properties of SiGe include a trade-off between composition and maximum basewidth, high germanium contents necessitate very thin base widths and in practice base compositions rarely exceed 25% germanium. Fortunately, as a result of strain this can still allow a considerable conduction band offset.

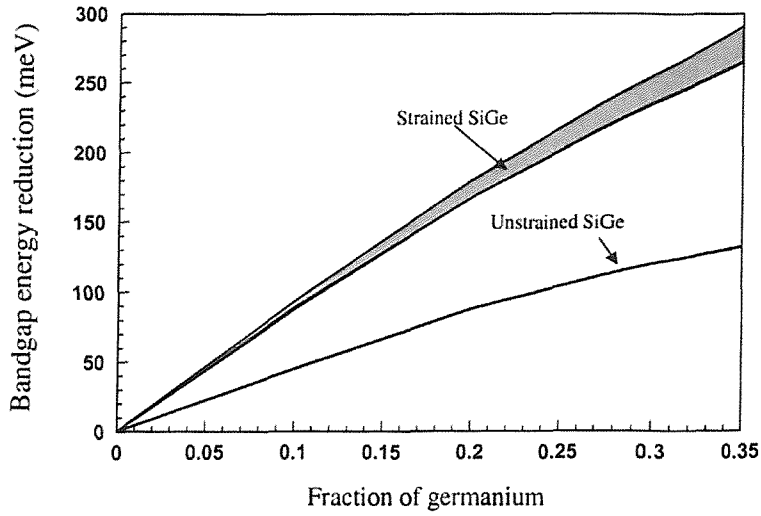


Fig. 2.6 Plot of bandgap reduction for various fraction of germanium at 90K. After People *et al.* [32].

2.4 Electrical Properties of $Si/Si_{1-x}Ge_x/Si$ HBTs

Figure 2.7 shows the band diagram of an Si/SiGe emitter base junction. In thermal equilibrium, the fermi level is constant across the base and emitter and the vacuum level remains continuous through the junction. These effects lead to discontinuities in the conduction and valence band (δE_c and δE_v respectively). As a result of the bandgap difference and the band alignment considerations the potential barrier in the conduction band is much smaller than that in the valence band. After the introduction of germanium, the bandgap of the emitter, $E_{g(Si)}$ remains the same whereas the bandgap of the base, $E_{g(SiGe)}$ is reduced. The difference between $E_{g(Si)}$ and $E_{g(SiGe)}$ is equal to $\delta E_c + \delta E_v$.

After the introduction of germanium into the base, the barrier to hole injection (Ψ_p) remains almost unaffected and as a result the base current, which is due to mainly holes injected from the emitter into the base, remains more or less the same as in a silicon homojunction bipolar transistor. However, the barrier to electron injection (Ψ_n) is significantly reduced. This results in a considerable increase in electron injection from the emitter to the base, corresponding to an increase in emitter current. It will be shown later that all of this results in an increase in collector current and current gain.

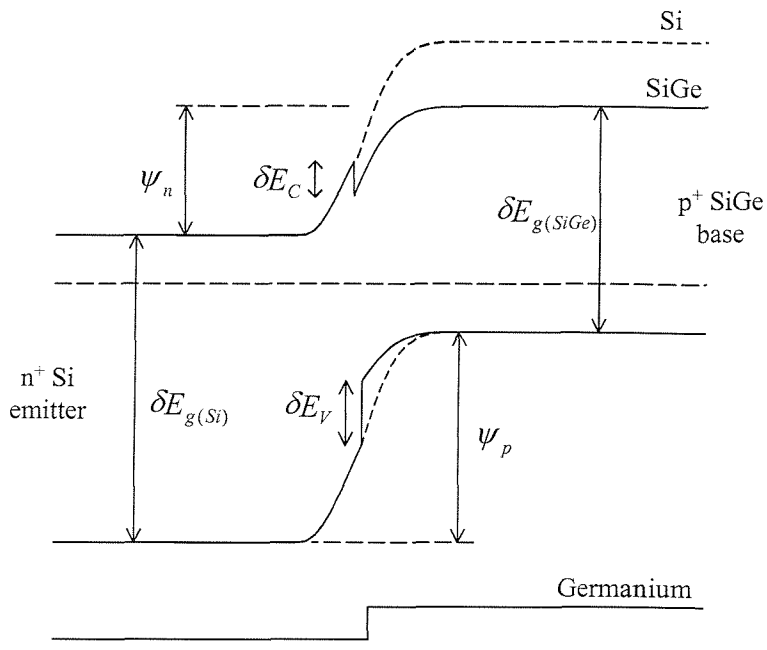


Fig. 2.7 The effect of a strained SiGe layer on the bandgap of an emitter base junction.

2.5 Current Gain and Early Voltage Enhancement

The introduction of germanium into the base region improves several aspects of the transistor. The following derivations will show how collector current and current gain is improved, and how this can be ultimately traded for lower power operation. The derivations are closely based on the work by Harame *et al.* [33]. For the derivation, we assume the geometry of the SiGe HBT and Si BJT to be identical. We also assume that the emitter, base and collector profiles of the two transistors to be the same except for the germanium in the base of the SiGe HBT. The germanium profile is assumed to be linearly graded between the emitter-base and collector base junctions, as shown in figure 2.8, this feature is readily obtained and helps to reduce the base transit time by providing for the drift of minority carriers in the base.

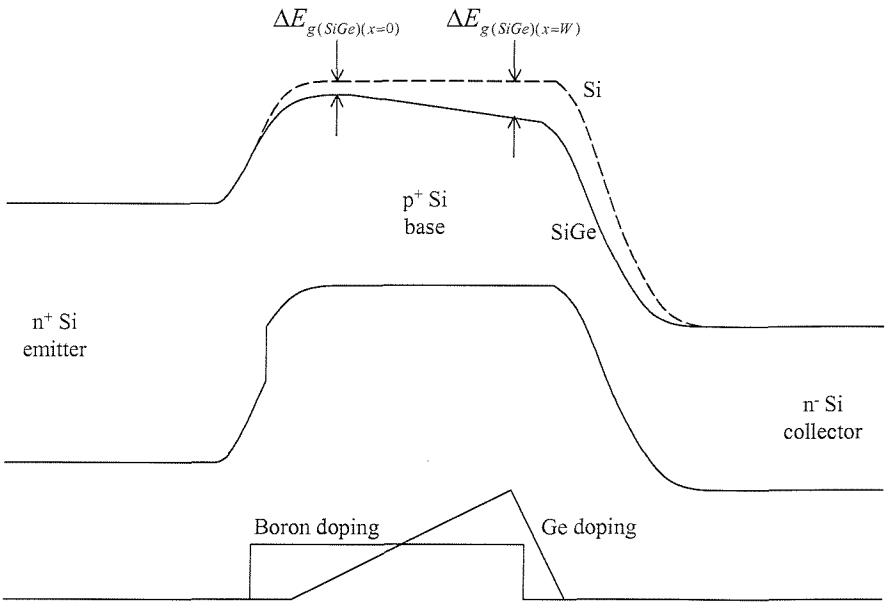


Fig. 2.8 Band diagram of Si (dotted line) and SiGe HBT (solid line) in forward active mode.

The major advantage of using a SiGe base is the inherent increase in current gain that allows additional design freedom. The improvement in current gain offered by SiGe HBTs compared to a Si BJT can be expressed by taking the ratio of the common emitter current gain of the SiGe HBT (β_{SiGe}) and the Si BJT (β_{Si}) to give

$$\frac{\beta_{SiGe}}{\beta_{Si}} \approx \tilde{\eta}\,\tilde{\gamma}\left(\frac{\Delta E_{g,Ge}(grade)}{kT}\right) \times \frac{\exp\left(\frac{\Delta E_{g,Ge}(0)}{kT}\right)}{1-\exp\left(-\frac{\Delta E_{g,Ge}(grade)}{kT}\right)} \qquad (2.13)$$

where,

$$\tilde{\gamma}=0.4,\ \tilde{\eta}>1,\ \frac{\exp\left(\frac{\Delta E_{g,Ge}(grade)}{kT}\right)}{1-\exp\left(-\frac{\Delta E_{g,Ge}(grade)}{kT}\right)}>1,\ \exp\left(\frac{\Delta E_{g,Ge}(0)}{kT}\right)>1$$

where $\Delta E_{g,SiGe}(grade)$ is the reduction in bandgap due to germanium grading in the base. Equation (2.13) shows that the SiGe HBT collector current increases exponentially for finite germanium content. For a SiGe HBT with a 3-8% Ge trapezoid

doping, base current remain generally the same but collector current density is increased 4.5 times compared to a Si BJT for a comparable base doping level.

This increase in current gain is advantageous as it can be traded for higher base doping. The increase in base doping reduces base resistance, which can then be used to increase the maximum frequency (f_{max}) of the transistor. Higher base doping also allows smaller basewidth, which reduces base transit time and further improves the frequency performance.

The improvement in the high frequency operation of a SiGe HBT can be considered by looking at the small-signal unity gain frequency (or cut-off frequency), which is given by,

$$f_T = \frac{1}{2\pi}\left(\frac{kT}{qI_C}(C_{jbe} + C_{jbc}) + \tau_b + \tau_e + \tau_{bc}\right)^{-1} \qquad (2.14)$$

where τ_b, τ_e and τ_{bc} are the base, emitter and emitter base transit times, respectively. Among these τ_b is typically the limiting delay time in bipolar transistors.

The ratio of $\tau_{b,SiGe} / \tau_{b,Si}$ is given by,

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,Ge}(grade)} \times \left[1 - \frac{kT}{\Delta E_{g,Ge}(grade)}\left(1 - \exp(-\frac{\Delta E_{g,Ge}(grade)}{kT})\right)\right] \qquad (2.15)$$

For a finite Ge grading, equation 2.15 above is less than unity. This shows how a SiGe HBT's f_T is enhanced, compared to a similar silicon devices, due to a reduction in base transit time.

Another beneficial effect of using a SiGe HBT is the enhancement of the early voltage, V_A, that brings about an improvement in the output conductance of the transistor. Output conductance is a measure of collector current variations with respect to the reverse biased collector-base voltage. Early voltage can be defined as,

$$V_A \approx \frac{J_C}{\left.\frac{dJ_C}{dV_{CB}}\right|_{V_{be}}} \tag{2.16}$$

which is the ratio of the collector current to the change in output conductance at V_{be}.

Thus, the improvement in the Early voltage between a Si and SiGe device can be found by,

$$\frac{V_{A,SiGe}}{V_{A,Si}} \approx \exp\left(\frac{\Delta E_{g,Ge}(grade)}{kT}\right) \times \left(\frac{1-\exp(-\Delta E_{g,Ge}(grade)/kT)}{\Delta E_{g,Ge}(grade)/kT}\right) \tag{2.17}$$

For finite germanium grading across the base, the ratio is larger than unity. Hence, the early voltage of a SiGe HBT is an improvement over a Si BJT. Furthermore, as both current gain and Early voltage are enhanced by the introduction of germanium, the βV_A product, which is an important figure of merit especially for high speed analogue applications, is also improved.

2.6 Issues Facing High Frequency Lateral Bipolar Transistors

Current high performance silicon based bipolar transistors are predominantly vertical devices and are used for a wide variety of analogue applications. In comparison, lateral bipolar devices have had little use in mainstream applications and are mainly used for low frequency or DC applications. This is because the vertical bipolar transistor has been the standard device for analogue applications and despite improvements in lateral bipolar design and the potential for better performance, vertical bipolar transistors are an established technology and currently outperform lateral devices. The investment required to develop the lateral bipolar transistors is a considerable barrier to mainstream interest in the technology.

A few technological difficulties have hindered the progress of high-frequency lateral bipolar transistors formed by implantation and diffusion. Isolating a lateral device from the substrate is the first such problem and is illustrated in figure 2.9. The parasitic transistors that are formed place restriction on the voltage range that can be used or else severely degrade the frequency performance of the lateral device. In addition to this, lateral transistors, which are commonly formed by diffusion in a CMOS process, tend to occupy a large area which contributes towards substantial parasitic capacitance that affects the transistors high frequency performance (increased C_{be} and C_{bc} in eqn 2.14). Another problem is the obvious practical difficulty that the base of the transistor has to be sufficiently wide to allow easy contact. A wide base region increases the base transit time and results in poor high frequency performance (equation 2.14), and lower gain.

Each of these difficulties are inherent to lateral bipolar transistors formed by implantation and diffusion, however, the advent of HBT technology has required the use of epitaxy to form transistor regions. The use of epitaxy to form regions of a lateral bipolar transistor has the potential to overcome all of these problems.

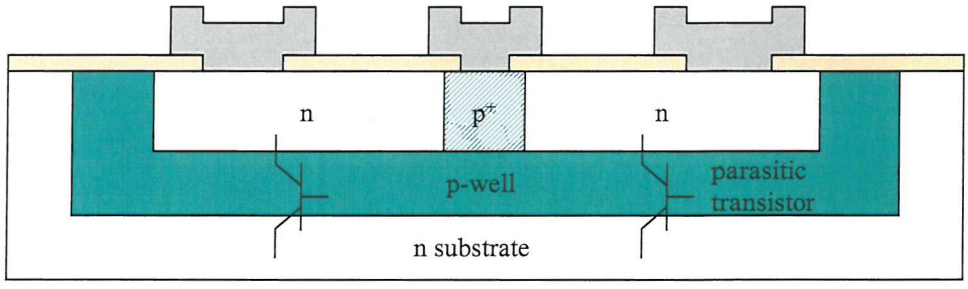


Fig. 2.9 The illustration above shows parasitic transistors inherent in a lateral bipolar transistor.

The prospect of solving these difficulties by the use of epitaxy, has encouraged a re-examination of the lateral BJT and its inherent advantages over the vertical BJT. Many potential advantages arise from the overall simplicity of the structure of the lateral BJT. This can be seen from figure 2.10 below, which shows schematic cross-sections of lateral and vertical bipolar transistors.

Figure 2.10 includes some of the important resistances and capacitances associated with the devices. R_{bi}, R_{bex} are the intrinsic and extrinsic base resistances, respectively. The intrinsic base resistance refers to resistance of the base area that is within the active area and is inherent in all bipolar transistors. R_{bex} refers to the parasitic resistance for the region of the base that is needed to allow the base contact at the surface of the device. Similarly, the collector resistance has components R_{ci}, R_{cb} and R_{cex} are the intrinsic collector, buried layer and extrinsic collector resistances, respectively. In figure 2.10, R_{cex} is shown as an n-type diffused layer, however, in practise this is more likely to be a deep metal contact. Since the emitter is directly accessible at the surface of the device, R_{ei}, the intrinsic emitter resistance is the only component of the emitter resistance and this is often small as the emitter area is usually highly doped. The capacitances, C_{jbc} and C_{jbe} are the base-collector and base-emitter junction capacitances, each of these capacitances also has associated parasitic capacitances, where depletion regions form between "extrinsic" regions of the device.

In a vertical bipolar transistor, an n^+ epitaxial buried layer is often grown to reduce the collector resistance. Without the buried layer, making contact to the collector from the surface would result in a high resistance path for the collector current and cause early current saturation. To ensure a low resistance contact, the buried layer is often contacted directly from the surface. This usually requires a deep anisotropic etch and the use of a polysilicon or tungsten plug to fill the etched via before metallization. Similar to the collector, the base of a vertical bipolar transistor cannot be easily contacted from the surface. Some form of low resistance contact method is needed to avoid high base resistance. Low base resistance is essential to avoid reduction in the maximum transistor operating frequency, as highlighted in equation 2.12 above. One method that is often used to reduce the overall base resistance is to employ highly doped double polysilicon extrinsic base contacts. Unlike the base and collector, the emitter of a vertical bipolar transistor is accessible directly from the surface and therefore, emitter contact problems are not an issue.

Lateral bipolar transistors allow the emitter, base and collector regions to be contacted directly to the device surface and the need for buried layers and complicated contact methods are removed. In addition to this, it minimises extrinsic base (R_{bex}), collector (R_{ci}) and emitter (R_{ei}) resistances, which should result in improved high frequency

performance. The lateral bipolar transistor also benefits from being more readily compatible with CMOS processes, albeit with some modification [15], due to its shallower structure (compared to vertical bipolar transistors).

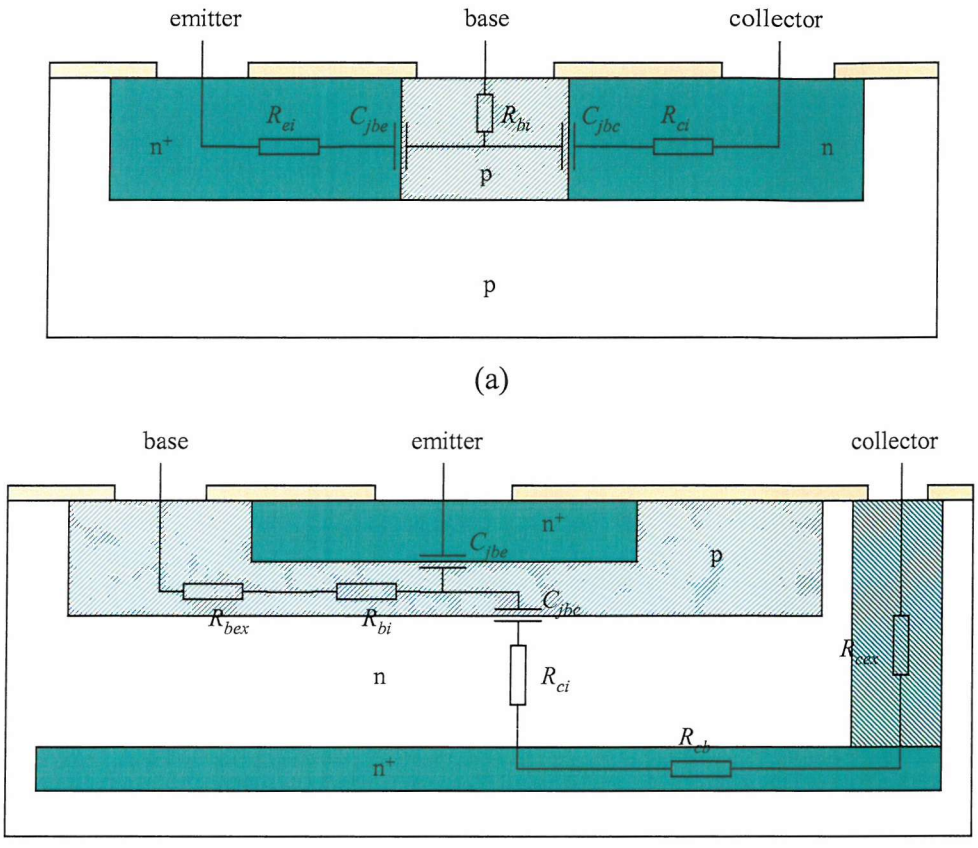


Fig. 2.10 General schematic of (a) lateral bipolar transistor and (b) vertical bipolar transistor showing parasitic resistances and capacitances that are associated with each device.

2.7 Current Lateral Bipolar Transistor Designs

Modern lateral bipolar transistors employ a number of common features utilised to push devices towards higher frequency operation. These features are designed to overcome the main difficulties we have already discussed, namely definition of a lateral thin base, definition of a fully aligned base contact and device isolation.

In modern lateral bipolar transistors, the formation of a thin base can be achieved by spacer techniques, dopant diffusion, and novel angled ion implantation [14-16]. A review of published material shows that among these, the first technique is the most commonly used [14, 16, 18]. Figure 2.11 below illustrates the spacer technique, as proposed by Nii *et al.* [16]. The technique involves the use of an oxide spacer to define the basewidth of the transistor. The process begins with the structure shown in figure 2.11(a). Ion implantation is used to dope the exposed SOI layer p-type (figure 2.11(b)). A thin spacer is then formed on the poly/SOI sidewall. This isolates the p-type base area during the n-type ion implantation step that defines the active area of the emitter (figure 2.11(c)). Contact is made to the thin base by the p^+ polysilicon layer above the base/collector area. The final device, before metallisation is shown in figure 2.11(d). Nii *et al.* found this device to have low base resistance (i.e. 270Ω) and low junction capacitances (i.e. C_{je}, C_{jc} and C_{jb} of 1.5fF, 2.4fF and 1.4fF respectively), and f_T and f_{max} of 12GHz and 67GHz respectively. Incidentally, the spacer technique shown here also allows a fully aligned base contact to be made to the intrinsic base (other researchers have also used similar spacer techniques to self align the external contact to the base) [14, 34].

For some time now SOI substrates have been used with vertical bipolar transistor technologies in order to isolate devices from the bulk substrate. SOI technology is readily adapted for use for lateral bipolar transistors and removes one of the principle difficulties faced by lateral bipolar technology.

All of the high frequency lateral BJTs that have been reported to date make use of SOI substrates. Traditionally, a lateral transistor would sit in a p-type or n-type well as shown in figure 2.9. However, this arrangement makes device isolation difficult and can cause latch-up. In addition, SOI substrates also minimises parasitic substrate capacitance, which has a detrimental effect on high frequency operation. Currently, the downside to using SOI substrates is cost, as they are generally more expensive than ordinary substrates, however, with the increased use of the substrate in industry along with further improvements in manufacturing, the cost of SOI substrates is expected to fall, making it more cost effective.

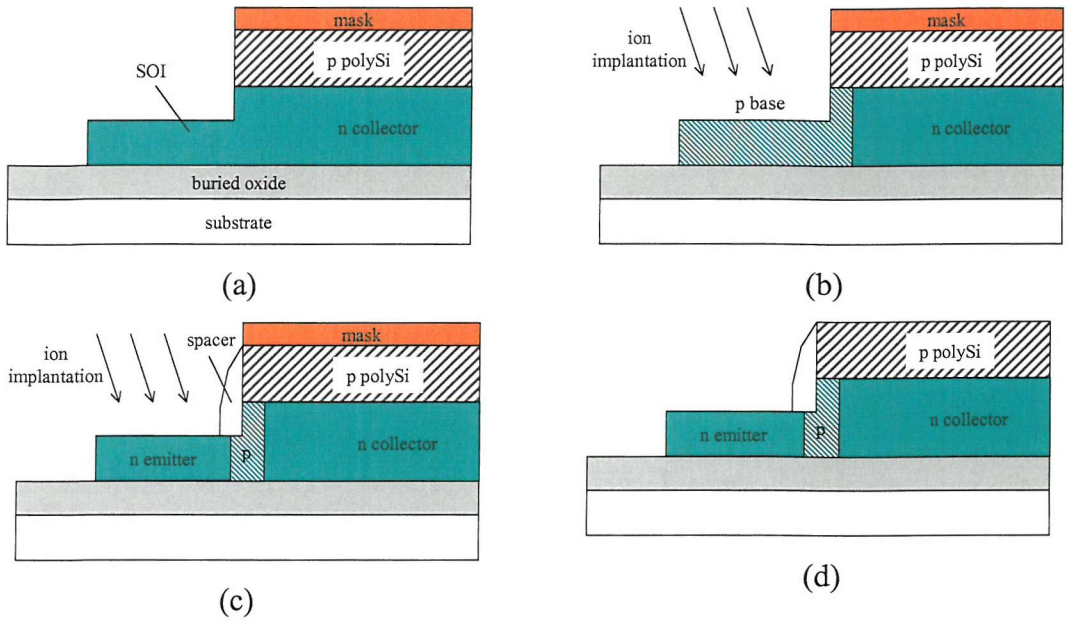


Fig. 2.11 Lateral bipolar transistor fabricated by spacer technique, after Nii *et al.* [16].

While the techniques discussed have been successful in producing high frequency lateral transistors, their potential can further be maximised through the use of SiGe alloy and epitaxy to form laterally grown HBTs [19]. We have already examined the benefits of heterojunction transistors, however, the need for SiGe layers adds difficulty since the layer has to be epitaxially grown (ion implantation of germanium into silicon can create strained SiGe layers, however layers usually have a high defect concentration, even after annealing [35, 36]). If lateral epitaxial growth can be achieved, epitaxy would also allow the formation of thin layers and sharp doping profiles. By combining the best features of vertical HBT and lateral bipolar technologies it should be possible to produce devices with excellent frequency performance.

In *vertical* heterojunction bipolar transistor design, SiGe layers are often grown by chemical vapour deposition (CVD), a technique which allows epitaxial growth to occur selectively on exposed silicon surfaces but not on oxides. In principle it should be possible to create structures and CVD conditions that could orientate a growth plane such that device epitaxy can proceed in parallel to a wafer surface, epitaxial lateral overgrowth (ELO) and confined lateral selective epitaxial growth (CLSEG), are two possible techniques. The main difficulty associated with ELO is the lack of

confinement in the vertical direction - in general vertical and lateral growth proceed simultaneously - and the loss of planarity is a difficult problem to overcome. Nevertheless, Shahidi *et al.* [14], have used ELO, along with chemical mechanical polishing (CMP) to obtain a thin silicon active layer for lateral transistor fabrication (implantation was used to define the transistor regions).

Confined lateral selective epitaxial growth (CLSEG) is a more difficult method to employ but is a more promising prospect for the fabrication of lateral strained SiGe layers (figure 2.12). In CLSEG vertical growth must be prevented by producing a growth front within some form of cavity. To date, CLSEG has only been used for silicon epitaxy growth. However, there is no reason why CLSEG cannot be used for SiGe growth. This technique should allow very thin lateral SiGe layers to be formed, enabling the fabrication of lateral heterojunction devices. Tang *et al.* have shown that an epitaxially defined SiGe base lateral bipolar transistor can potentially have a performance that is better than a vertical SiGe HBT [19] fabricated using similar lithographic resolution.

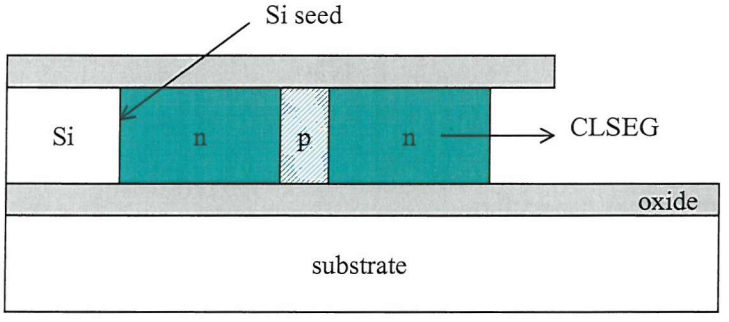


Fig. 2.12 Formation of lateral transistor by CLSEG.

2.8 Lateral Heterojunction Bipolar Transistor of Tang *et al.*

The lateral SiGe heterojunction bipolar transistor proposed by Tang *et al.*, shown in figure 2.13 makes use of confined lateral selective epitaxial growth by CVD to define the collector, base and emitter regions of the transistor. The doping of each region, including the SiGe base, is carried out *in situ* during epitaxial growth. The transistor is fabricated on an SOI substrate, which isolates it from the bulk substrate. The transistor

is also designed to have a self aligned external base contact, which makes direct contact to the intrinsic base. The general steps of the lateral bipolar fabrication process are illustrated in figure 2.13.

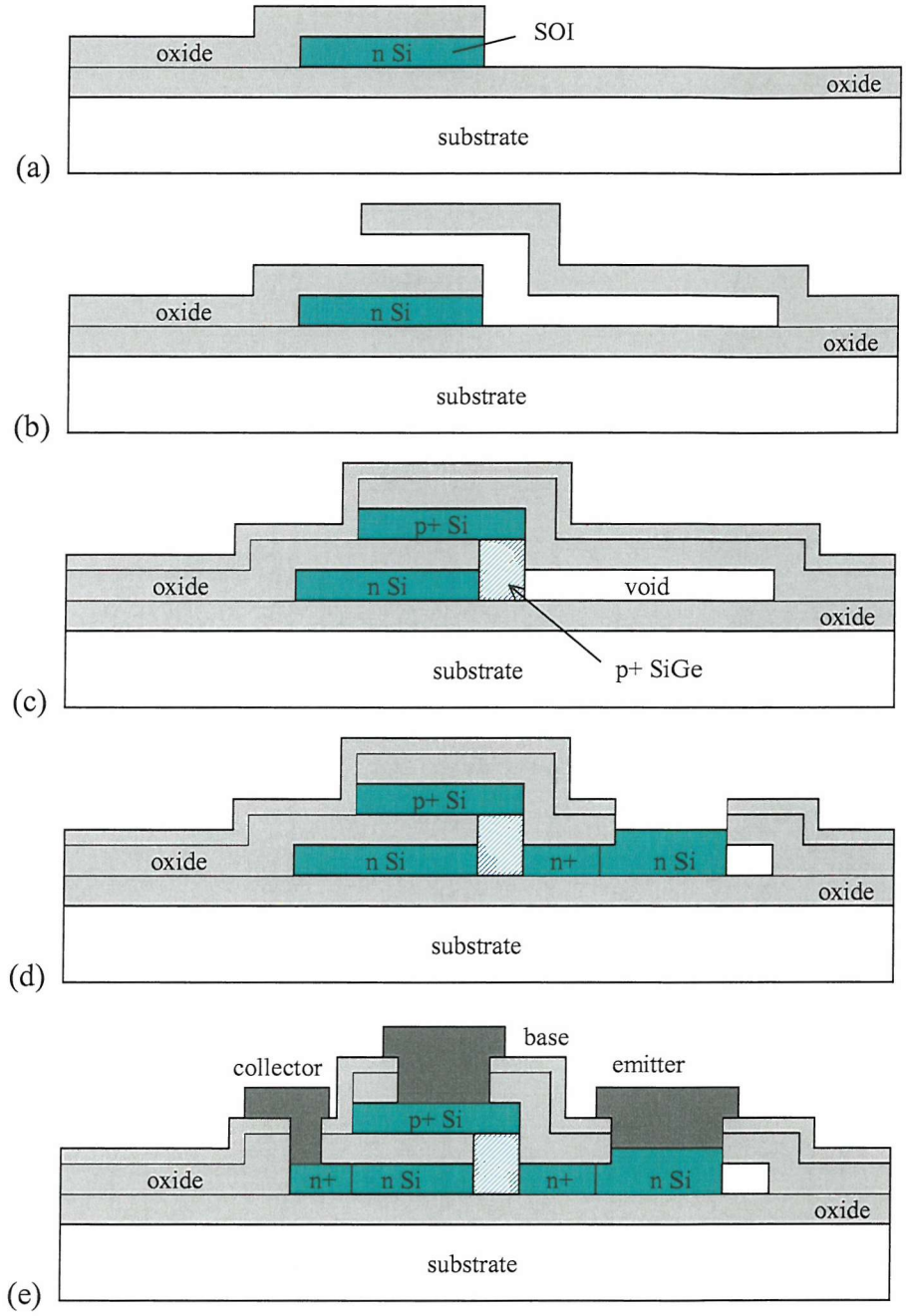


Fig. 2.13 Lateral SiGe HBT fabrication process proposed by Tang *et al.*[19]. (a) Initial preparation of the SOI wafer (b) formation of cavity by sacrificial etching techniques (c) growth of p^+ SiGe base and p^+ silicon extrinsic base by CLSEG, followed by oxide deposition (d) growth of n^+ epitaxy (e) contact to collector, base and emitter.

The fabrication process uses SOI wafers with a thin active layer (e.g. SIMOX). The use of a thin active layer minimizes the cross section of the device, which helps towards low power operation. The process begins by preparing a structure like that shown in figure 2.13(a). The sidewall of the n-type SOI layer will serve as the seed for the lateral epitaxy growth. This is followed by the formation of a cavity, which is created by sacrificial etching (figure 2.13(b)). The base of the transistor is then grown by CVD to form the SiGe base, followed by the p^+ silicon extrinsic base, as shown in figure 2.13(c). This is then followed by an oxide deposition process and an etch that opens the right hand side of the cavity. CLSEG is then carried out again to form the emitter area of the transistor (figure 2.13(d)). The process finishes with metallisation to the collector, base and emitter areas (figure 2.13(e)).

Simulations carried out by Tang *et al.* showed that with a germanium concentration of 10% and an overall base width of 100nm, the lateral SiGe HBT could have a peak f_T of 33 GHz and a peak f_{max} of 160 GHz. At peak f_T and f_{max}, the peak collector current was found to be 40 μA. As a reference, a vertical HBT with similar size, lithographic resolution and doping made by Kondo *et al.* produced an f_T and f_{max} of 40 GHz and 75 GHz, respectively at a peak collector current of 200 μA [37]. These results are shown in figure 2.14. The increase in performance (i.e. higher frequency and lower power) of the lateral device is attributed to its lower base contact resistance, R_b, and collector base junction capacitance, C_{jc}, and lower parasitics allowing for lower bias current for a given frequency of operation [38]. Tang *et al.* also showed that, with further improvement, the lateral transistor could potentially achieve an f_{max} of 220 GHz. These simulation results show the potential of the lateral heterojunction bipolar transistor and in particular, highlight its capability to operate at lower power and higher frequencies than vertical transistors.

One of that the most important aspect of the lateral HBT device is the CLSEG process, as it is the means by which a lateral strained SiGe can be formed. In order to achieve this, the CLSEG process has to be able to maintain complete selectivity throughout growth. In addition to this, the grown epitaxy has to be of high quality and defect free. The use of SiGe means a growth process with a low thermal budget is preferred to avoid relaxation of the material and to minimize the out diffusion of dopants. Part of

the requirement is the preparation of cavities that are suitable for CLSEG. In this work, these two aspects (i.e. CLSEG and cavity fabrication) will be examined in detail.

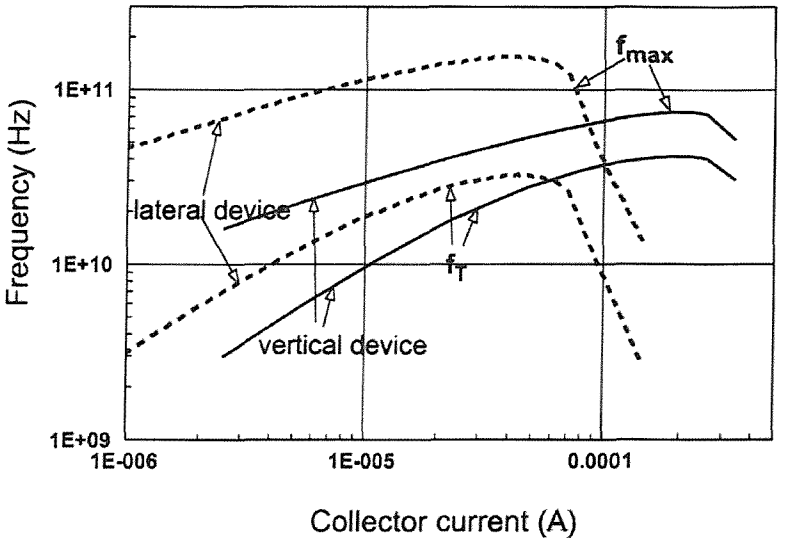


Fig. 2.14 f_T and f_{max} of lateral HBT by Tang et al and vertical HBT by Kondo et al. After Tang *et al.* [19]

Chapter 3

Chemical Vapour Deposition Theory

Selective chemical vapour deposition (CVD) is a key requirement for the fabrication of a lateral HBT. This chapter provides a detailed consideration of epitaxial growth in general and selective epitaxial growth by LPCVD in particular. The chapter begins with a general look at epitaxy. This is followed by a look at three systems that are commonly used for epitaxy growth, MBE, LPCVD and UHV/CVD. The Southampton University Microelectronic Centre LPCVD system is then introduced. The latter part of the chapter looks at chemical vapour deposition in general, highlighting important factors that influence deposition such as the effects of boundary layers, diffusion lengths and surface reaction processes. The section finishes by looking at issues pertaining to epitaxy growth such as selectivity, epitaxy quality and faceting. The final section describes the main types of epitaxial growth, which include non-selective epitaxy growth (NSEG), selective epitaxy growth (SEG), epitaxial lateral overgrowth (ELO) and confined lateral selective epitaxial growth (CLSEG).

3.1 Epitaxy

Epitaxy refers to the growth of single crystal material on a single crystal substrate. If the growth material is the same as the substrate, the process is called homoepitaxy. An

example of this is the growth of single crystal silicon on a silicon substrate. For brevity, homoepitaxy will be referred to in this work simple as epitaxy, unless otherwise stated. However, if the growth material is different from the substrate then the epitaxy growth is called heteroepitaxy. An example of this is the growth of silicon germanium on a silicon substrate.

Epitaxy is normally achieved by a chemical vapour deposition (CVD) process such as low pressure chemical vapour deposition (LPCVD) or by a physical vapour deposition process (PVD) such as molecular beam epitaxy (MBE). Although the two deposition methods are different, the basic requirements for epitaxial growth are similar. Both require a supply of silicon adatoms to the wafer surface in order for growth to occur. For epitaxial growth to occur the silicon adatoms must diffuse on the surface of the substrate and find suitable nucleation sites before being desorbed into the lattice. In general adatoms will stop diffusing, and form part of the growing crystal when they find locations that are energetically favourable. The most favourable nucleation sites are "kinks" on atomic growth planes. If conditions are such that adatoms can diffuse to such sites, then epitaxial growth will occur row by row and plane by plane to produce defect free epitaxial layers aligned to the underlying crystallographic plane.

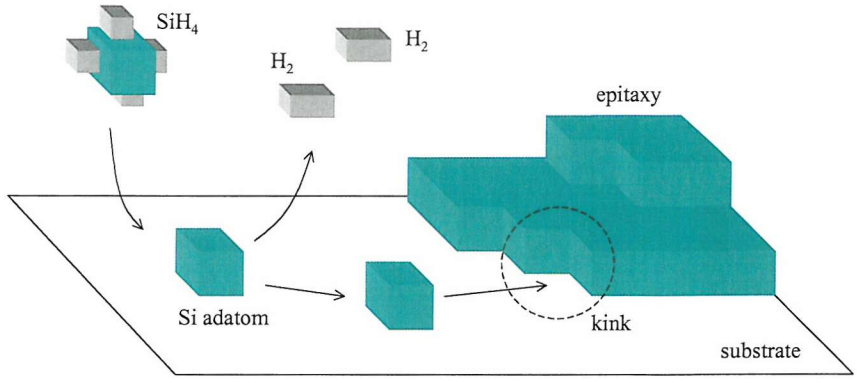


Fig. 2.1 Epitaxial growth by CVD using SiH_4 involves diffusion of the source gas through a boundary layer, decomposition of SiH_4, surface diffusion and incorporation of silicon adatoms at energetically favourable kink sites.

Impurities, defects or dust on the substrate surface, or the growth surface can offer alternative nucleation sites that prevent layer by layer growth, cause three-dimensional

growth islands to form and ultimately degrade the quality of the epitaxial layer. It is very important that the silicon substrate is well prepared prior to growth. The growth itself has to be carried out in a clean environment as gas and water vapour contaminants can also deteriorate epitaxy quality.

3.2 Epitaxy Systems: A Comparison

There are three common systems used for epitaxial growth, namely UHV/CVD, LPCVD and MBE systems. Each has advantages and disadvantages, and use tends to be very application specific.

3.2.1 Molecular Beam Epitaxy (MBE)

Molecular beam epitaxy (MBE) is a physical vapour deposition (PVD) process, unlike UHV/CVD and LPCVD systems, which are chemically based. The physical vapour deposition processes involve the evaporation of silicon and dopants either by electron beam evaporation or resistive heating. Evaporated species (in a flux) are transported to the wafer surface in a low vacuum where they are incorporated onto the surface [39]. Figure 3.2 below shows a schematic diagram of an MBE system. A more detailed working of an MBE system can be found elsewhere [39].

In comparison to CVD based systems, MBE has several features that are advantageous for certain applications. MBE typically operates at low temperatures, normally ranging from 400°C to 800°C [39], although growth at higher temperature (i.e. 900°C) is also carried out [40, 41]. Low temperature deposition brings the advantage of greatly reduced dopant out-diffusion and autodoping. Unlike CVD processes, MBE is not complicated by boundary layer effects nor by reaction kinetics at the wafer surface [39]. This allows MBE to be used to produce complex doping profiles that are difficult to achieve by CVD methods. The absence of intermediate reactions and diffusion effects, allows layer properties to be rapidly modulated. This allows fine control over growth rate to be achieved, with sharp doping profiles and material transitions. Growth rates as low as 0.1 nm/min [42] to as high as 300 nm/min [43] have been reported. This

fine control is especially beneficial for quantum devices such as quantum cascade lasers and quantum well infrared photodetectors. Although MBE growth rates are relatively slow MBE has been used for applications such as silicon and silicon germanium epitaxial growth for HBTs [44, 45]. MBE systems operate at ultra high vacuum pressures, in the region of 10^{-8} to 10^{-10} Torr. Operating at UHV pressures is advantageous as it reduces the partial pressures of water and oxygen, which are found to be detrimental to the quality of the grown film [46]. However, the disadvantages of working at very low pressure are long turn-around times and the need for expensive pumps that can achieve UHV pressures, and expensive maintenance.

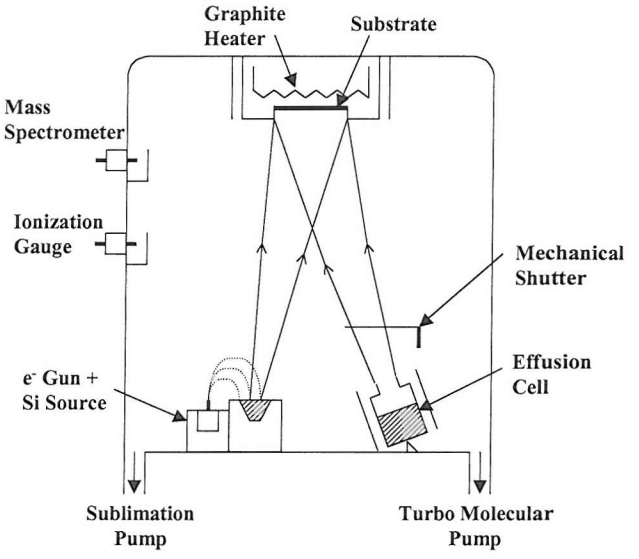


Fig. 3.2 Schematic of an MBE system, after Gruhle *et al.* [47]

One of the major drawbacks of MBE is its low throughput, as typical systems can only process a small number of wafers at a time. This makes MBE expensive and unsuitable for commercial use, where high throughput is demanded. MBE is also more complicated to clean than CVD systems, often requiring complex chamber cleaning processes [46]. Besides this, maintaining and replenishing the silicon and dopant sources requires opening the MBE reactor. This is detrimental to the system as it exposes the reactor chamber to air. To bring the system back to operational status would then require long bakes to desorb any atmospheric species from the systems walls, which results in a long downtime.

3.2.2 Chemical Vapour Deposition

During chemical vapour deposition (CVD) gases are used to transport growth materials to the substrate. These gases react or decompose at the growth temperature to allow atoms to be adsorbed. CVD reactors can be divided into two main types - hot wall and cold wall systems. In a hot wall system, the entire reaction chamber is heated to the growth temperature. This configuration is advantageous as it ensures a relatively constant temperature throughout the reaction chamber, which results in layers with good uniformity. However, the drawback of this is that during growth, materials will be deposited on the chamber walls. This will give a memory effect, where materials (such as dopants) on the walls can continue to be incorporated into the growth surface long after the gas supply has been cut off. In comparison, in cold wall systems only the substrate is heated to the growth temperature and the chamber walls are kept much cooler than the substrate (usually by water cooling). This minimises deposition on the chamber walls and also the need for regular cleaning. One of the biggest advantages of CVD based epitaxy over MBE is the ability to batch process many wafers in a single run. Commercial UHV/CVD systems are now available that can batch process up to 25 wafers at a time . Unlike MBE systems CVD does not require the reactor chamber to be opened in order to replace source materials. Therefore, CVD based systems have shorter downtime compared to MBE systems.

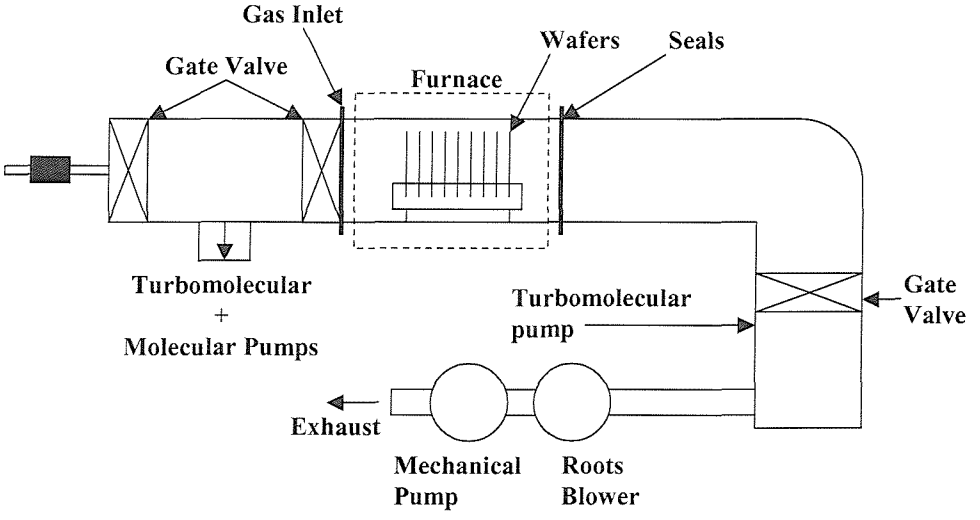


Fig. 3.3 Schematic of a UHV/CVD based epitaxy system, after Meyerson [48].

In terms of pressure, LPCVD systems normally operate in the 10^{-1} to 10^{2} Torr region [49-51], while UHV/CVD systems tend to operate at around 10^{-4} Torr [43]. As with MBE, one of the advantages of operating at UHV pressures is that it allows good quality epitaxy to be carried out a low temperatures (i.e. 500°C to 650°C) [52, 53]. This is a result of the UHV conditions, which minimise the presence contaminants such as water vapour or oxygen [54]. Although these are obvious benefits of UHV/CVD, growth at LPCVD pressures have also been found to give epitaxial layers of good quality [49, 55, 56], so UHV conditions are not necessary to obtain device quality epitaxial layers. LPCVD pressures are advantageous because they do not require expensive UHV-standard equipment. This fact is highlighted in this work where growths are carried out at around 1 Torr. With UHV/CVD systems, growth at very low pressures and temperature essentially means low growth rate. Although not as low as in MBE systems, the growth rate of UHV/CVD systems are typically in the 1 to 10 nm/min for silicon epitaxy. In comparison, silicon epitaxial growth by LPCVD has growth rates >10 nm/min [46, 57]. At higher pressures (i.e. 150 Torr), growth rates can be as high as ~100 nm/min [56]. The higher growth rate of LPCVD systems is advantageous especially when thick layers are required such as for epitaxial lateral overgrowth (ELO) and confined lateral selective epitaxial growth (CLSEG). Although thick layers are possible with UHV/CVD systems, the low growth rates requires long growth times making it less suitable compared to LPCVD systems, especially when layers several hundreds of nanometres to several microns thick are needed.

3.3 SUMC LPCVD Epitaxy System

This section describes the main design features of the SUMC LPCVD system. For reference, the schematic of the epitaxy system is shown in figure 3.4. The SUMC LPCVD system is a stainless steel system built to MBE standards. This makes the system expensive to build, however, the use of stainless steel chambers and metal seals offer the cleanest growth environment. Unlike the use of a quartz graphite chamber in UHV/CVD systems, the use of stainless steel minimises the safety risk from the danger of an implosion. The machine is water cooled (i.e. a cold walled system) and accepts

both 4-inch and 8-inch wafers. The machine has two growth chambers with a central load lock. The growth chambers can be pumped down to a base pressure of 1 mTorr using a Roots and dry pump. Growth can be carried out at a pressure of between 0.01 to 2 Torr. The load lock also has a turbo pump, which helps reduce the amount of water and oxygen vapour in the chamber. The pressure in the load lock is also lower than the growth chamber. This prevents any water, oxygen or other contaminants from transferring into the growth chamber from the load lock. The machine is fixed with a graphite heater, which can be used to heat wafer substrates up to 1100°C. The machine is connected to a range of source gasses such as silane, dichlorosilane, arsine, phosphine, diborane, germane and hydrogen. All of the gasses are purified and controlled using mass flow controllers. Doping p-type using diborane can be achieved to concentration levels between $2x10^{17}$ cm^{-3} to $6x10^{19}$ cm^{-3}. For n-type doping, phosphorus is used and concentrations between $2x10^{15}$ cm^{-3} to $2x10^{19}$ cm^{-3} can be achieved. The SUMC LPCVD machine used in this work can be fully controlled by computer but it can also be operated manually. The machine has been successfully used to fabricate various homojunction and heterojunction bipolar and MOS devices using selective and non-selective epitaxy processes based on silane [58]. More detailed information of the SUMC LPCVD system is covered by Bonar [46].

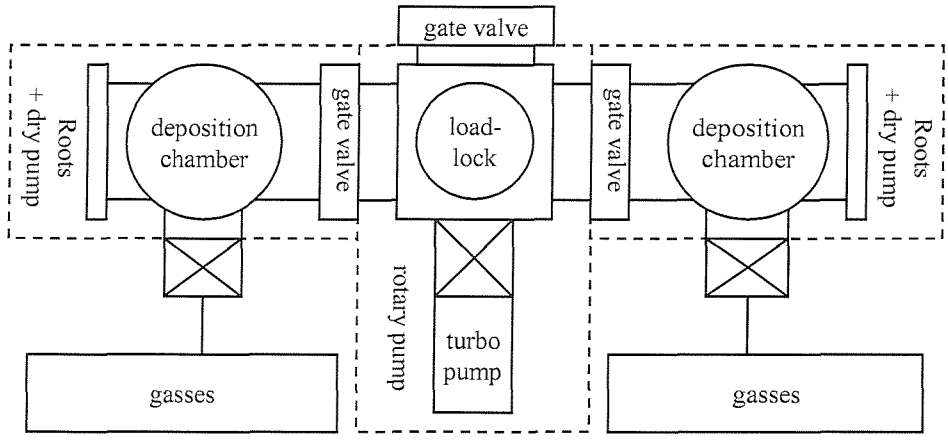


Fig. 3.4 Schematic of SUMC LPCVD system.

3.4 SUMC Epitaxial Growth Procedure

A typical procedure for epitaxial growth starts with an *ex-situ* cleaning of the silicon substrate, commonly known as an RCA clean. It is a two step process which involves initially cleaning the wafers in a solution of NH_4OH : H_2O_2 : H_2O (1:1:5) at 72°C for 10 minutes, followed by a rinse in purified water. The second step in the process is the immersion of the wafers in a solution of HCl : H_2O_2 : H_2O (1:1:6) at 72°C for 10 minutes, followed by another rinse in purified water. The wafers are then spun-dry in a warm nitrogen environment. At the end of the RCA cleaning stage a thin "RCA oxide" of around 1.5 nm thick is formed, which protects exposed silicon areas from contamination before subsequent growth.

Following the clean, the wafer is loaded into the epitaxy load lock which is then pumped down to base pressure. Once the base pressure is reached, a robotic arm transfers the wafer into one of the growth chambers. A hydrogen prebake is then carried out to remove the RCA oxide. This involves ramping the temperature up to 980°C and baking the wafer for 5 minutes. Following this, the wafer is then cooled to the growth temperature in a hydrogen atmosphere. When the growth temperature is reached, the growth gasses (SiH_4 or $DCS/SiH_4/H_2$) are turned on for the required growth period. When the growth period is over, the heater and gasses are turned off.

3.5 Chemical Vapour Deposition Process

Chemical vapour deposition consists of several steps, illustrated in figure 3.5. The first part of the deposition process is forced convection. This is the injection of reactant and carrier gasses into the growth chamber at high pressure. These gasses, enter the growth chamber and diffuse close to the wafer surface. They then diffuse through a boundary layer and are adsorbed onto the wafer surface. There, the gasses decompose to leave adatoms on the surface of the wafer. In a silicon epitaxial process, silicon adatoms which have resulted from the decomposition of silane, migrate until they find stable silicon sites to incorporate into the growing layer. These sites tend to be at steps formed by partially incomplete silicon layers. If a silicon atom fails to find a suitable site, it can nucleate on a dielectric surface or be desorbed from the wafer surface. Atoms or molecules that are desorbed from the wafer surface, along with unused reactant gasses

and by-products of chemical reactions are extracted out of the reactor chamber. All these steps occur concurrently and, provided controllable parameters are fixed, the system can be considered to be steady-state. Depending on the growth conditions, one particular step may rate-limit the overall process [42].

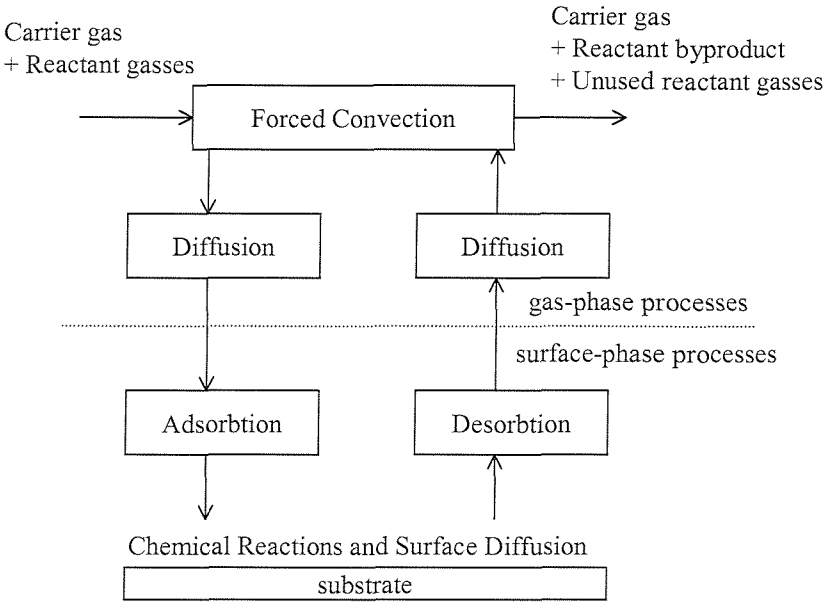


Fig. 3.5 Illustration of a chemical vapour deposition process, after Kamins [42].

3.5.1 Boundary Layer Diffusion

Gas diffusion through a boundary layer is often a rate limiting step in a deposition process [42]. The boundary layer is the thin layer of depleted reactant which separates the gas in the forced convection region from the surface of the substrate. Gas molecules that are forced into the reactor chamber have to diffuse through the boundary layer before being adsorbed onto the wafer surface. The flux of gas molecules diffusing through the boundary layer is weakly proportional to temperature and inversely proportional to pressure. This is highlighted in the equation [42],

$$D = D_0 \left(\frac{T}{T_0} \right)^{\alpha} \left(\frac{P_0}{P} \right) \qquad (3.1)$$

Where D is the gas phase diffusion coefficient across the boundary layer, D_0 is a between 0.1 and 0.2 m^2s^{-1}, T_0 is 273 K, P_0 is 760 Torr, and α is between 1.75 and 2 [42].

3.5.2 Surface Reaction

Surface reaction chemistry is a major factor influencing growth rate. Several processes occur when reactants approach the region close to the wafer surface. These processes include, decomposition of the source gas in the gas-phase, adsorption and decomposition of the source gas at the wafer surface, adsorption of atoms, the diffusion of silicon adatoms on the wafer, incorporation of adatoms into the growth front, the desorption of adatoms, and the desorption of reaction by-products [42].

Gasses can decompose either homogeneously (i.e. in the gas phase) or heterogeneously (i.e. at the surface). Of the two, heterogeneous decomposition is preferred because it results in layers that are low in defects [42]. Gas phase decomposition tends to create clusters of atoms in the near-surface region. These clusters can disrupt the formation of epitaxial layers and be a source of defects. The clusters may also have a poly-crystalline structure which can cause misalignment in the epitaxial layer, resulting in poor epitaxy quality. Although complete decomposition at the surface is preferred, some decomposition in the gas phase will always occur. In general low pressure systems will have less gas-phase reactions but other factors such as the type of reactor can also have an effect. For example, hot wall reactors have a hot ambient compared to cold wall reactors, where only the substrate is heated. As a result, homogeneous decomposition is more likely to occur in hot wall reactors than in cold wall reactors. The type of carrier gas also influences gas phase decomposition. The use of hydrogen is found to limit the amount of homogeneous decomposition because it is one of the reaction products.

During heterogeneous decomposition reactant molecules arrive at the wafer surface and are adsorbed. Once adsorbed, the reacting species will be temporarily bound to the

wafer surface. A surface phase reaction will then take place causing the growth atoms to be adsorbed. Although these adatoms are bound to the surface of the wafer they are free to diffuse until a suitable site is found. After decomposition, reaction by-products desorb from the surface region and are removed from the reactor by forced convection.

At the wafer surface, the diffusion length (L) of the adatoms is given by [42]

$$L \approx \sqrt{D_S \times t} \tag{3.2}$$

where D_S is the surface diffusion coefficient and t is time available for surface diffusion. This can be approximated to [42]

$$L \approx \frac{1}{\sqrt{R_D}} \exp\left(-\frac{E_a}{2kT}\right) P^{-n} \tag{3.3}$$

where R_D is deposition rate, E_a is activation energy, T is temperature, P is pressure and n is a number less than unity. Equation 3.3 above shows that the diffusion length of the adsorbed reactants on the wafer surface is dependent on temperature and inversely dependent on pressure. The diffusion length of adsorbed silicon atoms on the surface influences the quality of the layers formed. When diffusion length is long, the silicon atoms have a chance to travel further in search of a suitable silicon site. If a suitable silicon site is not found then the silicon atom may desorb from the wafer surface and extracted out of the epitaxy reactor. Alternatively, if the silicon adatom comes into contact with other silicon adatoms nucleation can occur and three-dimensional growth can result. This in turn can result in defected epitaxial or polycrystalline growth. With a shorter diffusion length, the chance of polysilicon island growth becomes more likely. In an epitaxy process, the choice of temperature and pressure is limited by the machine capability and fabrication process (e.g. thermal budget). Hence, a balance between temperature and pressure is often needed to obtain good quality epitaxy.

3.5.3 Growth from Silane and Dichlorosilane

Silane (SiH_4) is a silicon source gas that can be used for epitaxial growth. The deposition of silicon using silane is obtained by pyrolytic decomposition, such that

$$SiH_4(g) \rightarrow Si(s) + 2H_2(g) \qquad (3.4)$$

where silicon (Si) and hydrogen (H_2) are the reaction products. The reaction is irreversible, and for single-crystal layers, has to be carried out at high temperatures (>900°C). Although the equation above suggests a single-step reaction process, in practice, the growth of silicon from silane involves several intermediate steps. Lee *et al.* [59] suggests that silicon deposition from silane involves: (1) diffusion of silane from the bulk gas through the boundary layer, (2) dissociation of silane into SiH_2 and H_2 at the silicon surface, (3) adsorbtion of SiH_2 on the surfaces, (4) diffusion of SiH_2 adatoms to kink sites, and (5) incoroporation of Si into the crystal lattice.

As an illustration of surface chemistry, for silane (SiH_4), the following reaction mechanism occurs,

$$SiH_4 + \underline{s} \rightarrow \underline{H} + \underline{SiH_3} \qquad (3.5)$$

$$SiH_3 + \underline{s} \rightarrow \underline{H} + \underline{SiH_2} \qquad (3.6)$$

$$2SiH_2 \rightarrow H_2 + 2\underline{SiH} \qquad (3.7)$$

$$2SiH \rightarrow H_2 + 2\underline{s} + Si\ (film) \qquad (3.8)$$

$$2H \rightarrow H_2 + 2\underline{s} \qquad (3.9)$$

where $\underline{s}$ denotes a vacant site and an underline designates an adsorbed species.

As with silane, the deposition of silicon from dichlorosilane (SiH_2Cl_2) (DCS) consists of several intermediate steps. Claassen *et al.* have shown that the two rate limiting steps in a dichlorosilane deposition process are: (1) decomposition of SiH_2Cl_2 to $SiCl_2$ and H_2, and (2) the release of Cl from $SiCl_2$ by interaction with H_2 [60]. These reversible reactions occur such that

$$SiH_2Cl_2(g) \leftrightarrow SiCl_2(g) + H_2(g) \quad (3.10)$$

$$SiCl_2(g) + H_2(g) \leftrightarrow Si(s) + 2HCl \quad (3.11)$$

The $SiCl_2$ and H_2 molecules are both adsorbed on the surface after reaction. $SiCl_2$ then diffuses to the surface steps, where it incorporates to the crystal lattice after the chemical reaction with H_2. The chemical by-product of this reaction (HCl) is then removed from the surface. An important feature of the DCS deposition is the reversibility of the overall reaction mechanism, as this allows greater selectivity (section 3.6).

3.5.4 Mass Transport Limited and Surface Reaction Rate Limited Growth

The two largely independent processes of diffusion through the boundary layer, and reaction at the surface give rise to two distinct growth regions, the first process effectively determines the rate at which reactant species arrive at the wafer and the second process determines the rate at which adatoms are adsorbed onto the wafer surface. Either of these processes can determine the overall deposition rate. Depending on which is the rate-limiting step, growth can either be mass transport limited or surface reaction rate limited, as shown in figure 3.6. If the flux of reactant molecules arriving at the wafer surface (through the boundary layer), is defined as A_d, and the flux of reactant that is consumed (by surface reaction) at the surface is defined as R_d, then the mass transport limited region occurs when $A_d < R_d$. Whereas when $A_d > R_d$, growth is surface reaction limited. When $A_d \sim R_d$, the process is influenced by both mass transport and surface reaction rate processes. A process is generally mass transport limited at high growth temperatures, and surface reaction limited at low growth temperatures.

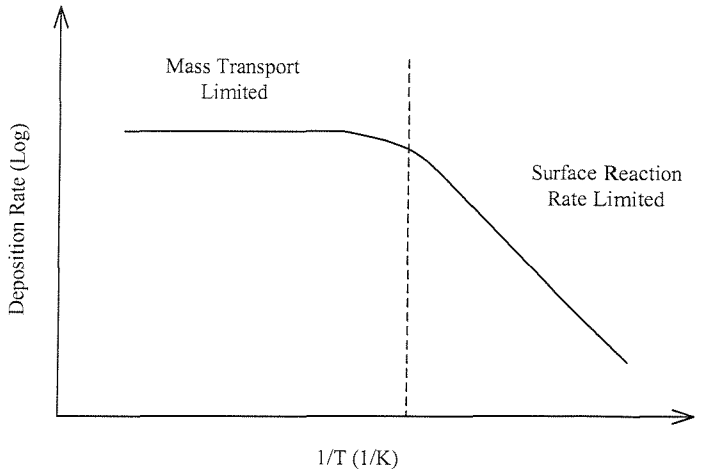


Fig. 3.6 Arrhenius plot showing surface reaction limited and mass diffusion limited region.

In a surface reaction rate limited process, the rate of reaction and hence adsorption is exponentially dependent on temperature, giving apparent activation energy, E_a. Growth in this region can be represented by,

$$G_r = A\exp\left(-\frac{E_a}{kT}\right) \tag{3.12}$$

Where G_r is growth rate, A is a constant, k is the Boltzmann constant and T is temperature. CVD systems designed to operate in the reaction rate limited region must be able to very accurately and uniformly control the wafer temperature to ensure that growth rates are reproducible and uniform across the wafer.

At high temperatures the supply of reactant to the wafer surface can not meet demand and the process becomes mass transport limited. As a result, growth rate remains relatively constant with increasing temperature. Epitaxy systems designed to operate in this region have high growth rates that are insensitive to significant changes in temperatures, heating uniformity and control is much less of an issue, but chamber design and gas flow become important.

Epitaxial growth systems are generally designed to operate in either mass transport limited or surface reaction rate limited regions [46, 55] to ensure uniform layers and

repeatability from growth to growth. At the Southampton University Microelectronics Centre, good epitaxy growth is obtained in both regions [46, 49, 57], though uniformity was found to best in the mass transport limited region. Growths can also be carried out at the knee of the characteristic between surface reaction limited and mass diffusion limited regions. In this transition region, temperature, pressure and flow rate will all influence growth rates, growth quality and uniformity.

3.6 Selectivity

In silicon epitaxial growth, a growth is termed selective if growth occurs only on areas of exposed silicon, and not on areas covered by an insulator (e.g. silicon dioxide or silicon nitride) as shown in figure 2.7(a). When silicon is also deposited on oxide to form polysilicon islands as shown in figure 2.7(b), growth is termed non-selective. Non-selective epitaxy growth may be partial, as shown in figure 2.7(b), where polysilicon islands partially cover parts of the oxide surface. However, in certain growth conditions, epitaxial growth may be completely non-selective resulting in a blanket polysilicon layer on the oxide surface.

Selective epitaxial growth can be achieved by balancing the rates of adsorption and desorption of silicon adatoms on the wafer surface. Adsorption and desorption rates are different for different surfaces (Si or SiO_2) by carrying out growths at conditions where the adsorption rate on silicon is greater than the desorption rate on silicon while, at the same time, the adsorption rate on oxide is smaller than the desorption rate on oxide, then selective growth can be obtained.

There are therefore, many factors that can affect selectivity, one is clearly temperature, since adsorption rates are a strong function of temperature. This is shown in epitaxial growths using silane, where selective growth is only achieved at high temperatures (i.e. >950°C) [46]. In silane-only selectivity the activation energy for adsorption on silicon is lower than that for adsorption on oxide, thus there is a finite temperature range where silicon adatoms are adsorbed and incorporated while on the oxide there is no adsorption. Other, secondary factors include pressure and flow rates, as these will also

influence adsorption rates. Reduced growth pressure can also have the additional benefit of reducing the amount of water vapour in the growth reactor, which have been found to affect selectivity [50]. For an epitaxy process which uses only silicon containing gases such as silane, correlations exist between selectivity and flow rate. At low flow rates and high temperatures, growth is selective with growth rate being some function of flow rate. However, at high flow rates, growth may become non-selective. as the high concentration of silicon species increases the likelihood of spontaneous nucleation as adatoms form stable silicon islands on the oxide surface.

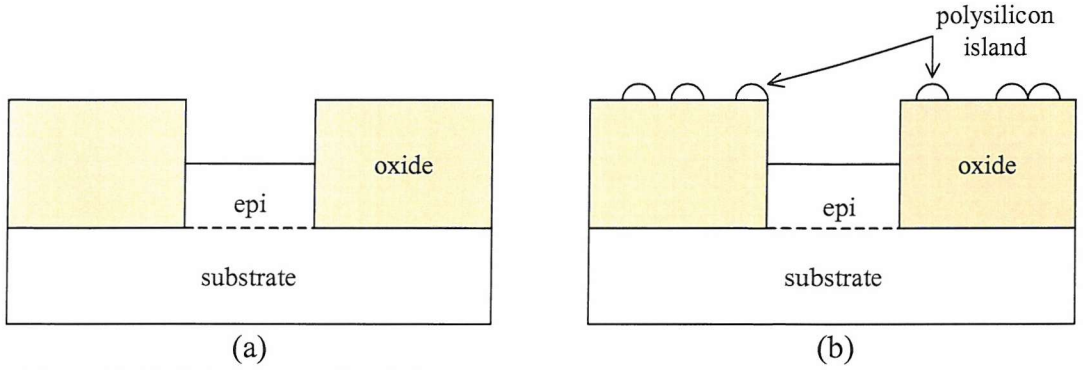


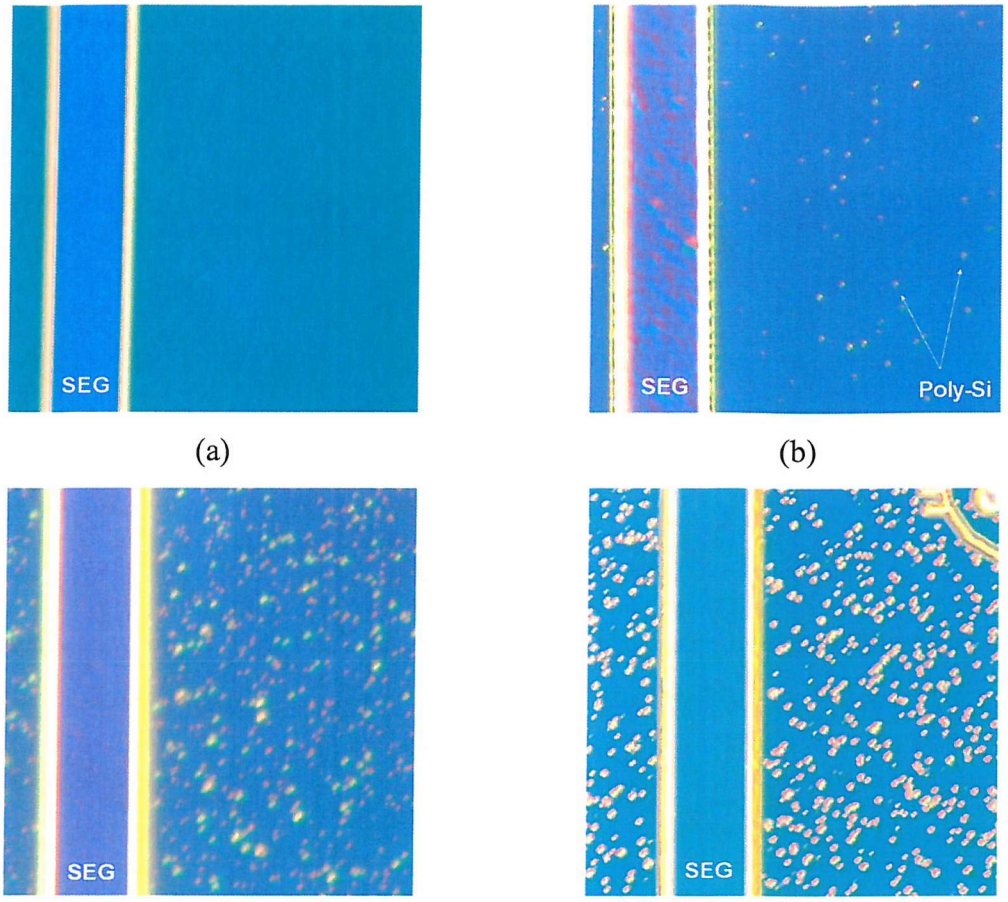
Fig. 2.7 (a) Selective epitaxial growth (b) Non-selective epitaxial growth due to polysilicon island deposition on the oxide.

In the silane-only selective regime adsorption and desorption rates can not be independently controlled. However, independent control can be established if chlorine based gasses are included in the gas chemistry, here, the silicon (deposition) to chlorine (etching) ratio becomes important. Extremes of silicon to chlorine ratio can lead, to etching or complete non-selective growth [61]. However, a point between the two extremes usually exists which can provide good selectivity[61].

Selectivity is useful when quantified as it allows ready comparison between growths with different conditions and also allows the engineer to determine a device tolerance to a loss in selectivity. The selectivity of a growth can be determined by optical inspection methods [62]. During inspection, a sign of a loss in selectivity is indicated by polysilicon island deposition on the insulator layer. A complete lost in selectivity, where the insulator is totally covered by polysilicon can often be observed by eye as the

wafer will look cloudy and not specular. However, if the polysilicon island density is low (e.g. ~10^6 islands/cm^2), then inspection by eye is often insufficient, as the wafer substrate will still look specular and similar to completely selective growth. A more consistent method of determining selectivity is by Nomarski optical microscopy (referred to after this as Normarski). Nomarski is a form of microscopy especially suited for the evaluation of surface quality and defects. The Nomarski method incorporates polarization and phase shift techniques that accentuate small variations on a surface. Using this method, polysilicon islands can clearly be observed and differentiated from other features on the mask. Figure 3.8 shows images of selective and non-selective epitaxial growth at various temperatures as viewed by Nomarski. From images such as these, the density of polysilicon islands deposited can be quantified. In this work, this is done by counting the number of polysilicon islands there are within a known surface area. To minimise measurement error, a large area should be taken. However, this may be impractical if counting is done manually for a high polysilicon density. If so, then taking a smaller area may be a more feasible approach. Alternatively, the task of counting can be automated using appropriate software (e.g. ImageTool [63]). However, the software is dependent on a good image, which has a high contrast between wafer surface and individual polysilicon islands on the surface.

A useful measure of selectivity is the incubation period, the period for which growth is completely selective. Once growth time surpasses the incubation period it becomes non-selective and stable polysilicon islands begin to nucleate on the oxide surface. Maximising "selectivity" is really concerned with maximising the incubation time. In fabrication, knowing the length of the incubation period is valuable as it sets the upper limit of epitaxy thickness that can be obtained. This can be found by systematically carrying out growth for various times. The growth time at which polysilicon deposition is detected on the wafer surface is the approximate value of incubation time. Another possible method is to obtain the incubation from interpolated polysilicon island density data, as will be discussed in section 6.4.3.



(a) (b)

(c) (d)

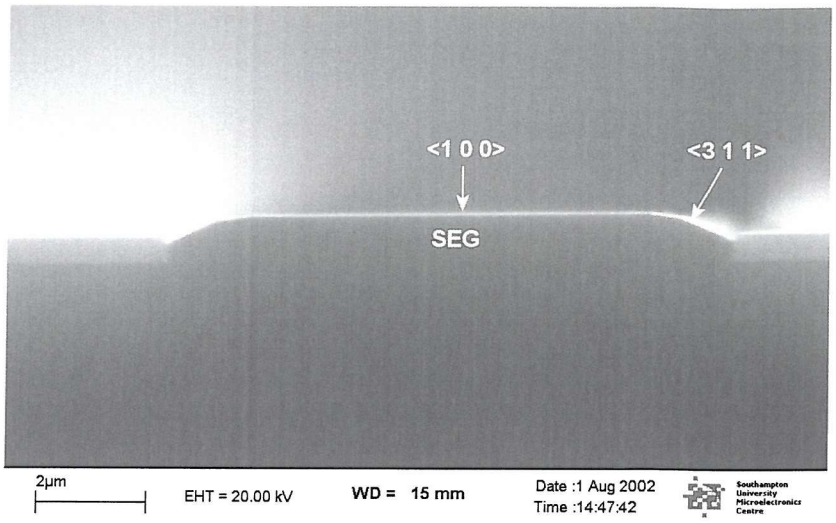
Fig. 3.8 Nomarski images of various wafer surfaces with polysilicon deposition (except (a)) after epitaxial growths at (a) 850°C, (b) 875°C, (c) 900°C and (d) 915°C.

3.7 Faceting

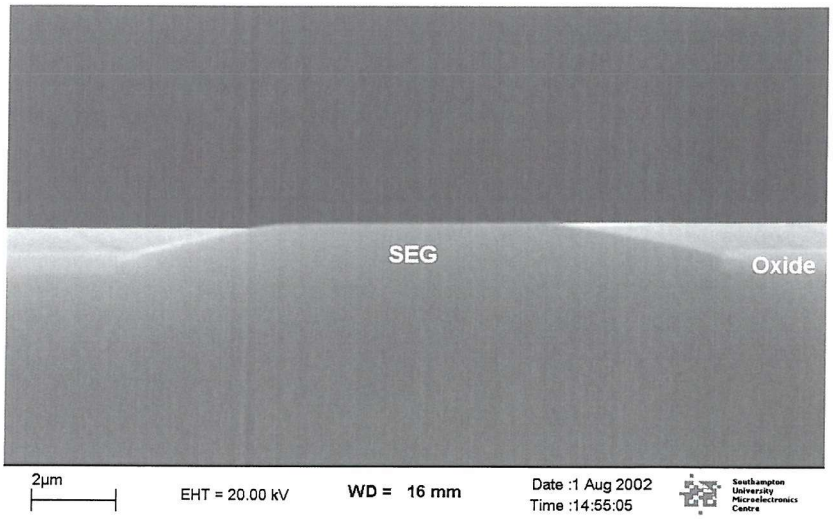
Faceting is a common occurrence in epitaxial growth by chemical vapour deposition. Facets develop as a result of silicon atoms incorporating on the most suitable silicon sites with the lowest free energy. The facets that develop during growth are dependent on several factors. Epitaxy growth carried out on standard (1 0 0) silicon wafers in <1 1 0> oriented seed windows often exhibit {1 0 0}, {3 1 1} and {1 1 1} facets. Each facet grows at different rates and typically the growth rate, GR_{hkl}, of the different planes are $GR_{100} > GR_{311} > GR_{111}$. The growth rates also reflect the atomic packing density of the different plane, which is highest for {1 1 1} plane, followed by the {3 1 1} and {1 0 0} planes. However, if the seed windows are oriented along the

<1 0 0> direction (i.e. angled 45 degrees to the wafer flat) then no distinct facets are observed. The growth rate ratio between the {1 0 0}, {3 1 1} and {1 1 1} are distinct but are dependent on gas chemistry [56, 64]. Figure 3.9 shows faceted and unfaceted epitaxial growth in <1 1 0> and <1 0 0> oriented features, respectively. Besides seed window orientation, the angle of the oxide sidewall also influences facet development as it can suppress the growth of certain facets. Drowley *et al.* found that during epitaxial growth in oxide seed windows, {1 1 1} facets generally do not appear until some lateral overgrowth has occurred (i.e. after epitaxy fills the seed window) [65]. This occurs because during the stage the epitaxy fills the oxide seed window, the oxide sidewall restricts silicon adatoms from silicon sites which forms the {1 1 1} plane. The {3 1 1} plane may also be suppressed to an extent at this stage of the growth. Once the epitaxy grows out of the window, the {1 1 1} plane is free to form. However, the {3 1 1} plane will often form prior to the {1 1 1} plane. As the {1 1 1} is the slowest growing plane compared to the {3 1 1} and {1 0 0}, the {1 1 1} becomes the dominant crystal plane once it forms. The way the facet forms can be influenced to an extent using chlorinated sources by tailoring the silicon to chlorine ratio [64]. Using this method, certain facets can be made preferential over others. This is especially useful for lateral epitaxy growth where a fast growing lateral growth front is desirable in order to achieve significant lateral overgrowth. Besides this, other variables such as temperature and pressure have also been found to influence faceting [66].

In relation to faceting, the orientation of the seed window also influences the defect densty. Epitaxial growth in seed windows oriented in the <1 0 0> direction produces less defected epitaxial layers than those oriented in the <1 1 0> direction [65, 67]. The reason for this is attributed to the stacking of silicon atoms, which in <1 1 0> seed windows, have a possibility of producing twin defects near the silicon / oxide interface. However, the amount of defects are less for <1 0 0> oriented windows.



(a)



(b)

Fig. 3.9 Epitaxial growth in (a) <1 1 0> and (b) <1 0 0> oriented seed windows. Growth in <1 0 0> seed windows do not show any distinct facets. Growth in <1 1 0> seed windows show {1 0 0} and {3 1 1} facets.

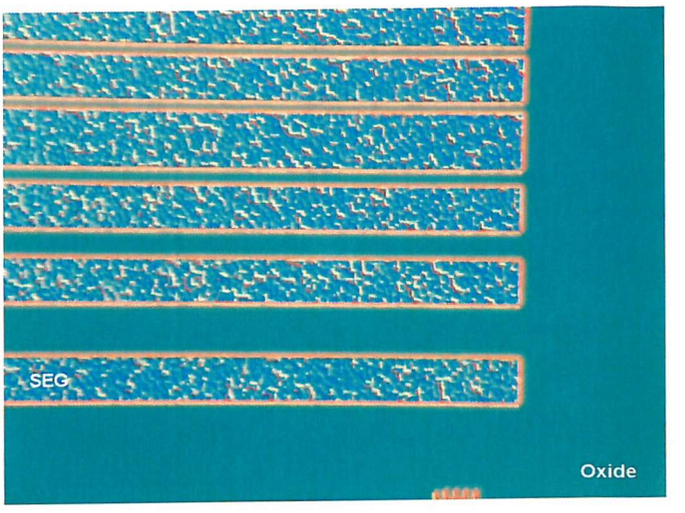
3.8 Epitaxial Quality

Good epitaxial quality is a prerequisite for device fabrication. The benchmark for good crystallinity is prime bulk silicon. There are several factors which influence epitaxial quality. This includes good preparation of the silicon seed surface. Prior to epitaxial growth, the wafer substrates should be thoroughly cleaned from metallic and organic

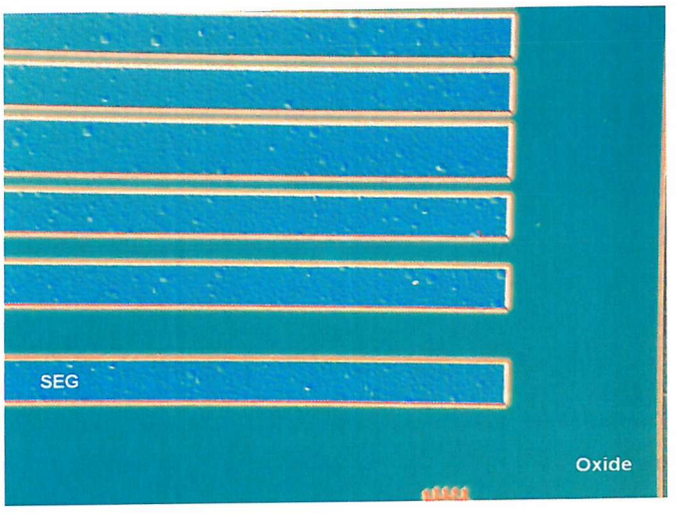
contaminants. This is done by carrying out an RCA clean. This also creates a thin layer of RCA oxide (~0.5 nm) on the surface, which protects the silicon surface from being contaminated when the wafer is transferred from the wet clean to the epitaxy machine. This thin oxide is removed by desorbtion at high temperatures (>900°C) before actual growth is carried out. However, the need for a high temperature bake step is undesirable in many fabrication processes. To minimise the thermal budget, the RCA oxide can be thinned down in a low concentration 100:1 BHF solution so that the bake can be shortened. Alternatively, a HF clean could be carried out instead of the RCA clean. The HF dip leaves the wafer surface hydrophobic, and the hydrogen terminated surface can be desorbed at a much lower temperature of 650°C and is therefore the preferred cleaning method if low thermal budget is important. Both cleaning methods have been used in epitaxial growth by LPCVD resulting in good epitaxy quality, indicating that both methods provide sufficient cleaning [49, 68, 69]. However, there are some indications by Bonar *et al.* that the RCA clean may be superior to the HF clean. Besides these two common cleaning methods, other methods such as low power plasma etching have also been found to give similar results [70, 71].

Epitaxy is often grown in oxide masked seed windows that have been prepared by dry etching. This can result in damage of the silicon surface, which affects epitaxy quality. To minimise this, an etch damage removal process should be carried out [72]. This consists of a thin oxidation step, which consumes the damage at the surface caused by the dry etching, followed by a wet etch in buffered HF to remove the grown oxide. The etch damage removal process has been found to give consistently better epitaxy quality than one that has not had the process. If the seed windows are wet etched, then an etch damage removal process is not needed.

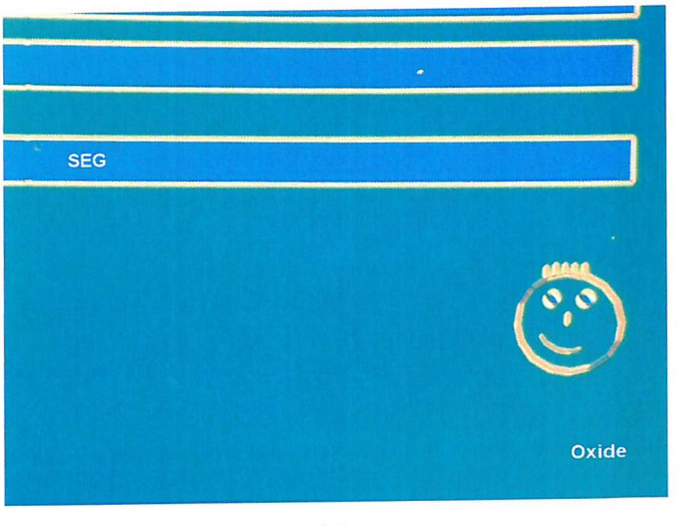
Epitaxy quality can be evaluated by several methods. The easiest method is by optical inspection using a Nomarski filter as it accentuates any non-uniformity on the epitaxy surface and allows surface defects to be clearly seen. As epitaxy quality can normally be inferred from the morphology of the epitaxy surface, this method allows quick determination of the quality of the grown layers. Figure 3.10 below shows several images of epitaxy surfaces as viewed under Normaski. Figure 3.10(a) is rough and rippled, which is an indication of poor epitaxial quality. The epitaxy surface in figure 3.10(b) is still somewhat rippled but much smoother than in Figure 3.10(a). The



(a)



(b)



(c)

Fig. 3.10 Nomarski images showing (a) defected epitaxy, (b) improved but defected epitaxy (c) good quality epitaxy.

smoother morphology is an indication that the epitaxy quality is better than the previous one. In figure 3.10(c), the epitaxy surface looks smooth and featureless. This is an indication of good epitaxy quality and is the reference for all growths. Although surface morphology is a good indication of epitaxy quality, defects may still exist below the epitaxial surface. This type of defect can be detected by electrical measurements (e.g. hall measurement, diode I-V curves). If diodes are used, defects in the epitaxy layer will result in a non-ideal ideality factor. Defects below the surface can also be detected by transmission electron microscopy (TEM), which allows high magnification (i.e. angstrom feature size) of the epitaxial layer.

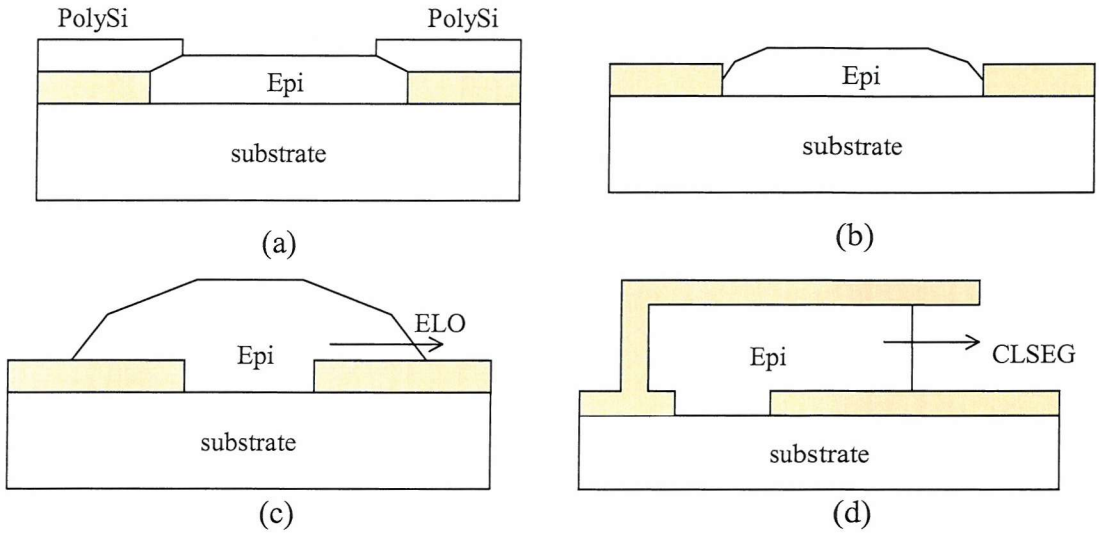


Fig. 3.11 Types of epitaxy growth (a) non-selective epitaxy growth (NSEG), (b) selective epitaxy growth (SEG), (c) epitaxy lateral overgrowth (ELO), and (d) confined lateral selective epitaxy growth (CLSEG).

3.9 Types of Epitaxial Growth

Silicon epitaxy refers to the growth of single crystal silicon on a silicon substrate. Epitaxial growth can be divided into two general types – non-selective epitaxial growth (NSEG) and selective epitaxial growth (SEG). The type of growth that is achieved is

dependent on several growth conditions such as temperature, pressure, gas and flow rates. Selective epitaxial growth can be further divided into several types – unconfined selective epitaxial growth, usually referred to as SEG, epitaxial lateral overgrowth (ELO) [56] and confined lateral selective epitaxial growth (CLSEG) [20]. These four types of epitaxy are illustrated in figure 3.11. The following subsections will look at each type in greater detail.

3.9.1 Non-Selective Epitaxy Growth (NSEG)

During non-selective epitaxial growth, silicon is deposited on the entire wafer surface. Epitaxy is obtained on areas where there is single crystal silicon exposed while on areas where there is an insulator (normally silicon dioxide or silicon nitride) amorphous silicon or polysilicon is obtained. In general, non-selective epitaxy is easier to achieve than selective growth, as conditions for selective growth are more stringent, non-selective epitaxial growth is generally obtained at lower temperatures than selective growth [61]. Good epitaxy quality can still be obtained even though growth is non-selective. This has been shown by Bonar *et al.*[58], who have successfully fabricated a silicon germanium HBT using a combination of SEG/NSEG processes indicating little correlation between epitaxy quality and selectivity [73].

Non-selective epitaxial growth has been used in several applications; the blanket growth of a n-type and p-type buried collector in bipolar junction transistors is one typical example [74]. One of the most advanced uses of a non-selective growth is during the fabrication of SiGe heterojunction bipolar transistors. In this process, where selectivity is not required, the epitaxial growth by LPCVD can be carried out at much lower temperatures (i.e. 700°C) than would be possible if a selective process with the same source gasses (i.e. silane) was required. The HBT fabrication sequence uses a non-selective/selective epitaxy process with *in situ* doping to define the intrinsic collector, heterojunction base and emitter regions, and the extrinsic base contact in a single growth run [75,76]. Besides the advantage of being able to define the transistor active regions in a single run, the low temperature growth minimises the thermal budget and allows thin layers with sharp doping profiles to be deposited.

3.9.2 Selective Epitaxial Growth (SEG)

Selective silicon epitaxial growth is the growth of epitaxial silicon on areas where there is exposed silicon, but not at areas that are masked by an insulator. Although non-selective epitaxy processes can be used to fabricate heterojunction devices, as shown by Schiz *et al.*[73], selective epitaxy processes add a number of useful design options to semiconductor device fabrication sequences. During selective epitaxial growth, silicon can be grown into predefined seed windows, these windows can be made small using sub-micron lithography and in this way small device active areas can be grown. With a non-selective process, the device active area has to be defined by lithography after growth and has to include alignment tolerance, and this will generally lead to larger active areas.

In general, the window for selective epitaxial growth is much smaller than for non-selective epitaxial growth. In the case of silane based CVD the selectivity window is very small, Bonar *et al.* found that selective growth using silane-only by LPCVD can only be achieved at temperatures above 900°C [46]. In comparison, non-selective epitaxy growth can be achieved down to 700°C [46]. Besides temperature, the pressure regime is also important in ensuring selective growth [77,78].

Although selective epitaxial growth can be achieved using silane-only, selectivity is much more readily achieved by the use of chlorinated gases such as HCl and dichlorosilane [51, 55, 68, 79]. In general, the gasses used for epitaxial growth usually include a silicon containing source gas such as silane or a chlorosilane and a chlorine containing gas such as HCl. The combination of the two types of gas along with a carrier gas such as hydrogen, allows independent control of growth and etching components of the overall chemistry, achieving a balance between silicon deposition in areas exposed by silicon and etching in areas masked by oxide.

The gas combination which are commonly used for selective growth are DCS/HCl/H_2 [51, 79-81] and to a lesser extent, SiH_4/HCl/H_2 [55]. To achieve good selectivity, the ratio between the silicon and chlorine containing gas has to be correctly balanced to achieve selective growth as a bias towards one type of gas could tip the growth

condition towards etching or non-selective growth. In epitaxy growth, growth temperature is often limited by the process' thermal budget, while pressure is limited, to an extent by the operational range of the epitaxy reactor. These two variables are often set prior to growth, although some leeway is possible. The addition of a chlorinated gas and varying the silane to chlorine ratio allows greater control to be put on growth so that selective growth can be achieved whilst maintaining the required temperature and pressure.

The development of selective epitaxy growth using advanced techniques based on LPCVD and UHV/CVD has led to the fabrication of high-performance HBT devices [8, 44, 45, 58]. This, along with other technological improvements such as the use of SOI substrates, shallow and deep trench isolation and smaller geometries has further improved the performance of current HBT devices. At the time of writing, the highest performing HBT that has been reported is by Rieh *et al.* (i.e. IBM), which has an f_T of 350 GHz [8]. This brings the HBT closer to the territory of GaAs and InP HBTs.

3.9.3 Epitaxial Lateral Overgrowth (ELO)

Epitaxial lateral overgrowth (ELO) is an extension to selective epitaxial growth. It refers to the situation in which epitaxial growth is allowed to extend laterally over the masking layer (i.e. oxide or nitride) [56]. Lateral overgrowth is achieved by prolonging growth times so that the growth front progresses, in vertical and lateral directions, beyond the area defined by the mask. If a substantial distance of lateral growth is required, an substantial thickness of vertical growth will also occur. The lateral growth rate is not necessarily equal to the vertical growth rate, as the lateral growth rate is determined by the lateral growth facet [64]. In selective epitaxial growth by LPCVD, the facets that commonly form are the {1 0 0}, {3 1 1} and {1 1 1}. Of these, the {3 1 1} and the {1 1 1} are the facets that contribute towards lateral overgrowth. As these facets are slow growing, the rate of lateral growth that can be achieved is low in comparison to the vertical growth (on the {1 0 0} plane). It is difficult but possible to control facet formation (a form of facet selectivity) by adjusting growth conditions [64].

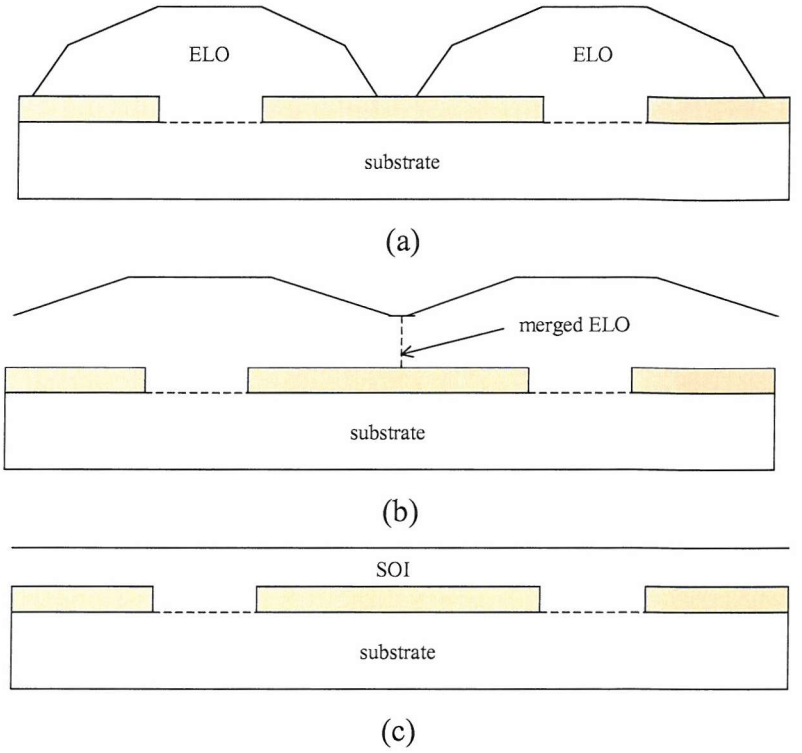


Fig. 3.12 Fabrication of SOI by ELO and CMP. (a) Epitaxial lateral overgrowth of silicon, (b) Merging of ELO islands, (c) ELO is thinned down by CMP to give an SOI layer.

With suitable growth conditions, significant epitaxial lateral overgrowth can be achieved. This was shown by Zingg *et al.* who achieved more than 8 μm of epitaxial lateral overgrowth with DCS / HCl / H_2 at 950°C at 150 Torr [56]. Similarly, Rathman *et al.* achieved lateral to vertical growth ratios of greater than unity using SiH_4/H_2 chemistry [79]. ELO has been used for a number of applications, of particular interest is the use of ELO to fabricate local SOI islands [82]. This consists of epitaxial lateral overgrowth, followed by a chemical mechanical polishing (CMP) stage to thin the epitaxy layer to the required thickness. The advantage of such a process is that it could reduce the need for expensive SOI wafers. An extension of this is the use of ELO to make SOI wafers, as shown in figure 3.12 below [83]. Here, the epitaxy is allowed to overgrow laterally and combine to form blanket silicon on insulator layer. Although this has been successfully carried out, the quality of the ELO layer is not as good as bulk silicon. ELO has also been used to fabricate bipolar transistors [84] with a good

performance in comparison to a similar device employing LOCOS isolation (i.e. $C_{cs} \times R_c$ product five times less than LOCOS device). All of these examples highlight the extra possibilities that ELO brings over standard selective epitaxy growth.

3.9.4 Confined Lateral Selective Epitaxial Growth (CLSEG)

Confined lateral selective epitaxial growth (CLSEG) is an extension of epitaxial lateral overgrowth. The main disadvantages of ELO is the vertical component of growth, which can lead to a thick layer of varying thickness [85]. Although this can be thinned down by CMP, it is an expensive extra process step and control over thickness uniformity by CMP can be difficult. A better approach is to limit vertical growth so that only lateral growth is obtained. This can be achieved by the CLSEG method and involves growing selective epitaxy in cavity structures prepared by micro-electromechanical systems (MEMS) processing techniques. The CLSEG method is illustrated in figure 3.13. As the figure shows, the cavity is fabricated prior to epitaxy growth (i.e. figures 3.13(a) to 3.13(c)). This involves growing a thin layer of oxide followed by an etch to open a seed window (figure 3.13(a)). A second thin layer of oxide is then deposited to protect the seed window. A sacrificial polysilicon layer is then deposited and patterned, before the deposition of another layer of oxide (figure 3.13(b)). A window is opened and the polysilicon sacrificial layer and thin oxide are etched (figure 3.13(c)). This then allows CLSEG to be carried out (figure 3.13(d)).

The advantage of the CLSEG method is it allows the thickness of the epitaxy to be specifically defined by the height of the cavity, which is determined by the thickness of the sacrificial layer. As the sacrificial layer is deposited by CVD, it allows layers with good uniformity to be deposited on the wafer, the results are generally better than the uniformity of the ELO + CMP technique described earlier. Furthermore, the use of CVD also allows very thin layers to be deposited, allowing thin cavities to be produced. Schubert *et al.* have fabricated cavities that are as thin as 500 nm [20]. With the vertical epitaxy growth confined, lateral growth progresses at a rate dependent on the lateral growing facet, as is the case with SEG and ELO. CLSEG by CVD opens up the prospect of the formation of strained SiGe layers within lateral SiGe heterojunction

bipolar transistors. CLSEG also brings other advantages associated with CVD such as the ability to grow thin doped layers with sharp doping profiles.

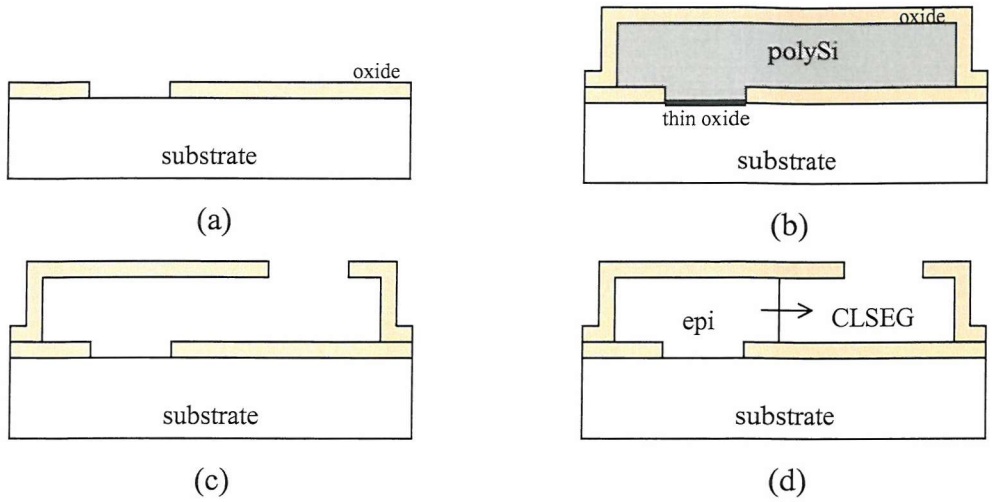


Fig. 3.13 Cavity fabrication process for CLSEG. (a) Deposition of thin oxide and opening of a seed window, (b) deposition of thin oxide and polysilicon, followed by another layer of oxide, (c) removal of sacrificial polysilicon layer by dry or wet etch techniques, (d) confined lateral epitaxial growth from prepared seed window.

So far, CSLEG has mainly been carried out using LPCVD epitaxy systems [20, 51, 86]. The growth pressure has been in the region of 100 to 150 Torr, and at a temperature of 900°C. DCS/HCl/H_2 has been the gas of choice, giving good epitaxy quality and good control over selectivity. Confined lateral epitaxy growth of over 3μm, with an estimated growth rate of 260 nm/min has been reported [87]. CLSEG has seen use in several applications. One of which is in the fabrication of local SOI [88]. It also shows potential for use in sensor applications, where devices are fabricated on the laterally grown epitaxial layer [89]. CLSEG has also been use to make a low resistance contact to the intrinsic base of a bipolar transistor [13]. The most novel use of CLSEG is in its use to fabricate a lateral heterojunction bipolar transistor [13]. Although, CLSEG has been used in a number of applications, it use has been limited as cavity preparation and suitable selective epitaxy processes are difficult to perform and represent considerable development challenges. The need to build a cavity for CLSEG requires several extra processing steps in comparison to the ELO + CMP method. It is therefore important to ensure that the advantages of CLSEG offset this extra processing need.

Chapter 4

Cavity Fabrication

Confined selective epitaxial growth requires the fabrication of cavity structures. In this research, three types of cavities have been designed and fabricated - test cavities, open-sided cavities and SOI cavities. The cavities have to fulfil several basic requirements in order to be suitable for confined growth. They have to be rigid and should not suffer from warping or collapse under stress. Any cavity must not be damaged or distorted by any fabrication processes that are required after it is made, this particularly applies to the epitaxial growth and (any pre-epitaxy cleaning stages), but also applies to any photolithographic, cleaning, deposition or etching. One of the important requirements of a cavity is it has to be compatible with the selective epitaxy process. As the epitaxy process developed at SUMC is designed to be selective to silicon dioxide, a cavity has to have its outer shell insulated by silicon dioxide. This is necessary as the use of materials such as silicon nitride can degrade selectivity. In addition, the cavity walls must be free from any silicon/polysilicon residues as these would create nucleation centres during selective epitaxial growth. The process must also provide a silicon seed that must be protected during cavity processing, to provide a smooth and flat, defect free surface suitable for epitaxial growth.

The first part of this work required a full consideration of the process stages and resources available at SUMC in order to establish the most effective overall process, the latter stages of the work required continued development of key stages in order to

optimise the process.

4.1 Processing Techniques

Cavity fabrication inevitably requires the deposition and etching of silicon compatible materials. In this section the processing techniques used for the deposition of silicon dioxide and silicon nitride, and the etching of silicon and polysilicon are introduced. Although there are a myriad of deposition and etching techniques, this section will look in detail at the processes that are available at the Southampton University Microelectronics Centre.

4.1.1 Dielectric Deposition

The deposition of insulating films such as silicon dioxide and silicon nitride is an important aspect of silicon fabrication. Silicon dioxide and silicon nitride, are normally deposited by chemical vapour deposition techniques. Atmospheric pressure CVD, low and medium temperature CVD (normally produce 'Low Temperature Oxide' - LTO) and plasma enhanced CVD (PECVD) [39] are the most common techniques. The choice of deposition technique depends on various factors such as thermal budget requirement, uniformity, step coverage and throughput, the type or quality of oxide produced is also an important factor.

4.1.1.1 Silicon Dioxide Deposition

Silicon dioxide is the most common dielectric material used in silicon fabrication. It can be grown *in situ* or deposited by chemical vapour deposition. High quality oxide layers are normally obtained from *in situ* thermal oxidation. This is usually carried out at temperatures above 900°C. For thick layers, 'wet' thermal oxidation is carried out, where steam is used as the growth source. For very thin layers (less than <100 nm),

'dry' thermal oxidation from a gas source is used. Although thermal oxidation gives layers with very good uniformity, high breakdown voltage, excellent thermal stability and good conformality, the process has a high thermal budget, can only produce layers on silicon and produces layers with high intrinsic stress (300 MPa compressive stress [90]). Alternatively, oxide layers may be deposited at low temperatures (around 450°C) at atmospheric pressure using conventional CVD techniques. The lower temperature is advantageous for situations that require low thermal budget (e.g. during post-metallisation processing). Layers deposited in this way generally have conformal step coverage and good uniformity but layers with high intrinsic stress (300 MPa compressive stress). However, the oxide layers tend to be more porous than thermally grown oxides, which results in higher oxide etch rates in buffered hydrofluoric acid (BHF). Low temperature oxides can however be densified by annealing to give less porous layers with lower etch rates, comparable to thermally grown oxide. The third oxide deposition method is by plasma enhanced CVD (PECVD) which allows growth to be carried at very low temperatures (200°C). This process can also be used to tailor the intrinsic stress of the oxide, between compressive and tensile stress (between 300 MPa compressive to 300 MPa tensile stress), by optimising the deposition conditions. PECVD deposited layers are non-conformal and have high etch rates.

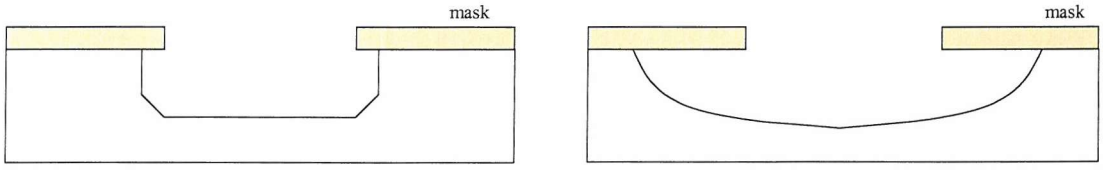
4.1.1.2 Silicon Nitride Deposition

Silicon nitride is normally used for the passivation of silicon devices and as a mask for the selective oxidation of silicon, the latter is possible due to the naturally slow oxide growth rate on silicon nitride. Silicon nitride is normally deposited by low pressure CVD at around 700°C using silane (SiH_4) and ammonia (NH_3). This deposition method gives good uniformity and high wafer throughput. However, deposited layers suffer from very high stress (1000 MPa), but this can be reduced by making the silicon nitride layer silicon-rich. Another method that can be used to deposit silicon nitride layers is plasma enhanced CVD (PECVD) in which silicon nitride layers are deposited at between 250°C and 350°C and can have an intrinsic stress ranging from 200 MPa (compressive) to 500 MPa (tensile) depending on the plasma drive frequency. Stress free layers can be obtained by using a switching plasma drive frequency technique [90].

4.1.2 Sacrificial Etching

During micro-electromechanical system (MEMS) microfabrication techniques silicon or polysilicon are often used as sacrificial materials to allows the formation of voids. Sacrificial layers can be removed using either wet or dry etching techniques. Several wet and dry silicon / polysilicon etching techniques are available within the facility.

Etching is an important part of semiconductor fabrication, and choosing a suitable etching process is important to achieve good results. There are many etching techniques that, in general, can be categorised into wet and dry methods. As in any fabrication process, the use of an etch method is dependent on the specific requirements of the process. The chosen method has to be evaluated based on several criteria, which include selectivity, uniformity, etch rate, etch profile, defect generation and layer damage. Other criteria such as stiction may also need to be considered depending on the application (for example, in MEMS processing).



(a) (b)

Fig. 4.1 (a) Anisotropic etch profile (b) Isotropic etch profile.

Wet etching methods have in the past been the primary method for etching. Wet etching is advantageous as it allows a large number of wafers to be batch-processed. It is also generally technologically simpler to carry out. However, with the push towards smaller feature sizes over recent years, dry etching has become the preferred option. This is due to its ability to etch various materials (e.g. silicon, silicon dioxide, silicon nitride, aluminium), allowing small features to be defined. In addition to this, dry etching methods create less wastage, minimising ecological impact to the environment.

A key issue with regard to etching is the etch profile. An etch is anisotropic if it etches

at different rates in different directions. However, if the etch rate is the same in all directions, the etch is called isotropic. In general, wet etching techniques tend to be isotropic whereas dry etching techniques are generally anisotropic. Figure 4.1 illustrates both anisotropic and isotropic etch profiles.

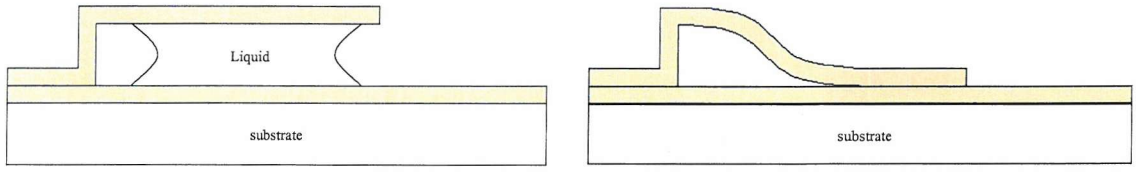
4.1.2.1 Wet Silicon Etching

There are a number of etchants that can be used to etch silicon or polysilicon. The most common are HF + HNO_3 + Acetic Acid (HNA) and alkali-OH based etchants such as KOH. Besides these, ethylenediaminepyrochatechol (EDP) and tetramethyl-ammonium hydroxide (TMAH) are also used, though they are less common. Among these etchants, KOH is readily available at the university fabrication facility. KOH is an anisotropic etch and etches different silicon crystallographic planes at different rates, with the {1 1 1} plane being the slowest. The etch rates of the individual planes (e.g. {1 0 0}, {1 1 0}) are highly dependent on various factors such as chemical composition, dopant concentration and temperature. However, the addition of other chemicals to the KOH solution can have an effect on the etch rate, as an example, the relative etch rate of the {1 0 0} and {1 1 1} plane can be changed from 8:1 to 34:1 by the addition of isopropyl alcohol (IPA) [91]. Another advantage of the KOH etch is that the facet dependence of the etch rate helps to minimise surface roughness. The etch is also highly selective to silicon in comparison to oxide, with an average selectivity of 100:1. In addition to this, KOH is low in cost and is easy to dispose of. At the Southampton University fabrication facility, the etch is normally carried out at 70°C giving a silicon etch rate of 100 nm/min. However, the etch rate increases dramatically, up to 3 times, when polysilicon is being etched.

4.1.2.2 Dry Silicon Etching

Dry etching is another method that can be used to remove bulk silicon or polysilicon. Most silicon dry etching processes use fluorine containing compounds as they readily

etch silicon and are highly selective to masking layers such as silicon dioxide. Dry etching can be done with or without a plasma. An example of a dry etchant without plasma is xenon diflouride (XeF_2). The XeF_2 dry etch process is generally highly selective to silicon relative to oxide, and is an isotropic etch. An example of a plasma dry etchant is SF_6. Similar to the XeF_2 etch process, the SF_6 etch process is also a highly selective silicon etchant relative to oxide. One of the advantages of SF_6 is the ability to change the isotropy of the etch from isotropic to anisotropic by changing the process conditions. Process conditions also have an effect on silicon roughening, and therefore, trade-offs between isotropy, silicon roughening and other criteria often have to be made. Another advantage of a dry etch process is the fact that etching does not occur in a wet solution, as the latter can cause stiction due to capillary effect, a significant problem in cantilever (and other similar structure) fabrication [92]. By avoiding the need to use a wet solution, this problem is prevented. At the Southampton University fabrication facility, the SF_6 dry etch process is readily available, and both isotropic and anisotropic etches can be made depending on the etch conditions.



(a) (b)

Fig. 4.2 The possible effect of wet etchants (liquid) on a cantilever. (a) Capillary action causes the cantilever to be pulled down to the surface, resulting in (b) stiction.

4.2 Test cavity

The first experiments were designed to examine issues related to the fundamental aspects of cavity fabrication. The "test" cavity would not allow confined vertical epitaxial growth, however, with a minimum of lithography stages fabrication of these structures allowed the assessment and development of the suitability of the cavity materials, deposition techniques and sacrificial etching methods. These structures also provide useful substrates with which to test selective epitaxial growth processes,

providing useful and early insight of selective growth on complex structures.

4.2.1 Fabrication Process

After full consideration of CLSEG cavity requirements and the fabrication processes available a fabrication process was developed that would provide the first "test" cavities (figure 4.3).

To begin, standard 100 mm, <100> oriented, p-type silicon wafers are subject to the growth of thermal oxide to a thickness of 200 nm. Next, undoped polysilicon is deposited and patterned. Next, either 200 nm of low temperature oxide (LTO) or a combination of LTO - nitride - LTO layers is deposited to form the outer shell of the cavity. Low temperature oxide (LTO) is used because it provides good conformal layers. Conformal deposition is important as it ensures the walls of the cavity are uniform in thickness and hence, have uniform stress [93]. However, the intrinsic stress of the oxide layer may cause parts of the cavity to deform [94]. To avoid this, an extra silicon nitride layer is deposited to strengthen the overall cavity structure. However, a dual LTO - nitride sandwich layer scheme leaves the silicon nitride exposed and as the selective epitaxy process is designed to be selective to oxide and not to nitride, this can be detrimental to the selectivity of the epitaxial growth. To overcome this problem, another layer of LTO is deposited on top of the silicon nitride layer, giving a tri-layer LTO - nitride - LTO sandwich structure. To ensure the deposited oxide layers are resistant to etching, which is especially important during the sacrificial etching stage, the wafer is densified in nitrogen at 950°C for 30 minutes (figure 4.3(a)). Section 4.2.2.1 will give a review of the densification methods used in this work.

After the outer LTO layer is deposited, a cavity window is then opened by dry etching. Part of the polysilicon is also removed using a dry anisotropic silicon etch process (figure 4.3(b)). Then the remainder of the polysilicon sacrificial layer needs to be removed. Both the isotropic SF_6 dry etch process and the KOH wet etch process were considered suitable. Both have good selectivity to oxide, but it was felt that SF_6 ought to minimise the chance of stiction, although KOH would be much easier to use.

After sacrificial layer removal the resist is stripped, and a standard etch-damage-removal process is carried out to remove any damage at the seed window caused by the dry etching (figure 4.3(c)). This consists of a short wet oxidation step at 950°C for 15 minutes, which forms a thin oxide layer, followed by a brief etch in buffered HF for 15 seconds to remove the grown oxide. Finally, the wafer is cleaned in an RCA solution after which the wafer is ready for epitaxial growth (figure 4.3(d)). A full process listing can be found in the appendix.

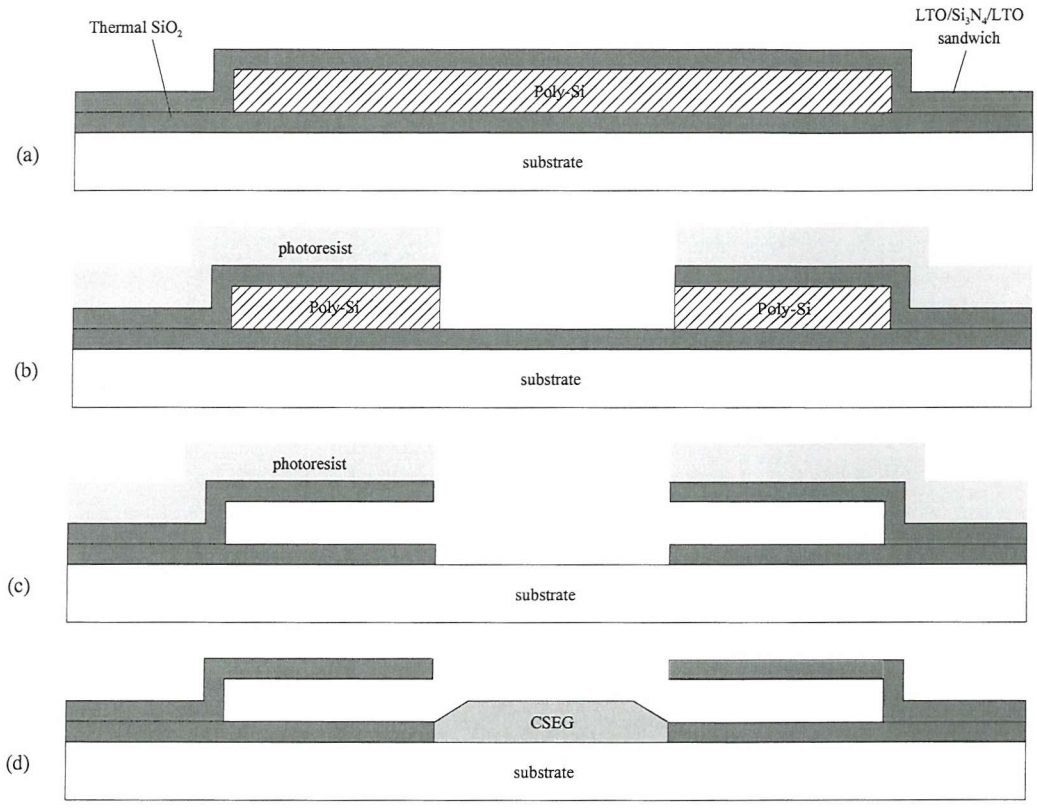


Fig. 4.3 Test cavity process (a) Deposition of thermal oxide, polysilicon and LTO/Si_3N_4/LTO sandwich layers, (b) Etching of sandwich and polysilicon layers, (c) Dry etching of sacrificial polysilicon and thermal oxide, (d) Cross section of cavity with confined selective epitaxial growth.

4.2.2 Results of Test Cavity Fabrication

4.2.2.1 Layer Densification

In the test cavity fabrication process, LTO and silicon nitride layers were used for the walls of the cavity. These layers were densified to improve the cavity's rigidity and strength. It is also necessary to minimise thinning during the sacrificial etch and minimise stress in the layers.

In this experiment, two densification methods were examined for use in the test cavity process. The first method involved a rapid thermal anneal (RTA) at 980°C for 20 seconds. The second method involved annealing the wafers at 850°C for 15 minutes in wet O_2. To determine the extent of the densification, these wafers were etched in buffered hydrofluoric (BHF) acid for 15 and 30 minutes. From this a plot of etch rate versus time was obtained. Thermally oxidised and undensified LTO deposited wafers were also etched for comparison. The wafers used in this experiment are summarised in table 4.4.1 below.

Wafer	Process
Wafer 1	Undensified LTO
Wafer 2	RTA, 980°C, 20 minutes
Wafer 3	Wet O_2, 850°C, 15 minutes
Wafer 4	Thermal Oxidation

Table 4.1 Wafers used in the densification experiment.

The results of the etch test, shown in figure 4.4, show the undensified LTO layer to have an etch rate of 360 nm/min. This is much higher compared to the other wafers in the test. The thermally oxidised wafer, along with the two densified wafers, has a much slower etch rate. The etch rate of the thermally oxidised wafer was found to be 115 nm/min. The etch rate of wafer 3, which was annealed in wet O_2 at 850°C, was also found to be similar at 115 nm/min. Wafer 2, which was rapid thermally annealed, was

found to have a slightly higher etch rate of 139 nm/min.

Low temperature oxide is used for the fabrication of the cavities because it allows oxide to be deposited uniformly over features. It also has less intrinsic stress compared to thermal oxide, even after densification. This is important in ensuring a rigid cavity structure. Undensified oxide layers also etch at a higher rate compared to thermal oxide. The ratio, as shown in the graph, is 3:1 (LTO:thermal oxide). The importance of densifying the LTO layer comes during the sacrificial layer stage. During this stage the oxide layer acts as a hard mask when the sacrificial layer is etched. Although the sacrificial etchant may be selective, the long etch time may severely thin the oxide layer. Densifying the oxide layer minimises this problem. Besides this, the densification process also redistributes the intrinsic stress of the LTO layer and ensures a level and rigid cavity ceiling.

From the results, it can be concluded that both densification methods have sufficiently densified the oxide layer. This is indicated by the similarity of etch rates to those for the thermal oxide. However, of the two methods, the Wet O_2 at 850°C for 15 minutes is found to be better as its etch rate is lower than the RTA at 980°C. The results of this experiment show that low temperature oxide, densified by either method, will have etch characteristics in buffered HF similar to thermally oxidised wafers. At SUMC, wafers RTA is carried out one wafer at a time, by contrast, the second anneal method can be used to batch-process up to 24 wafers at one time. Therefore, for a large number of wafers, the second anneal process would have an added advantage over the RTA process.

In this work, the test cavities were densified by RTA. This was partly due to the more readily available RTA machine over the oxide furnaces. Although the results show that the second densification method has a slight advantage over the RTA method, in practice, the difference between the two is small and has negligible effect in fabrication, especially if shallow etch backs of several microns are required. However, if long etch times are required then the second densification method is the preferred method.

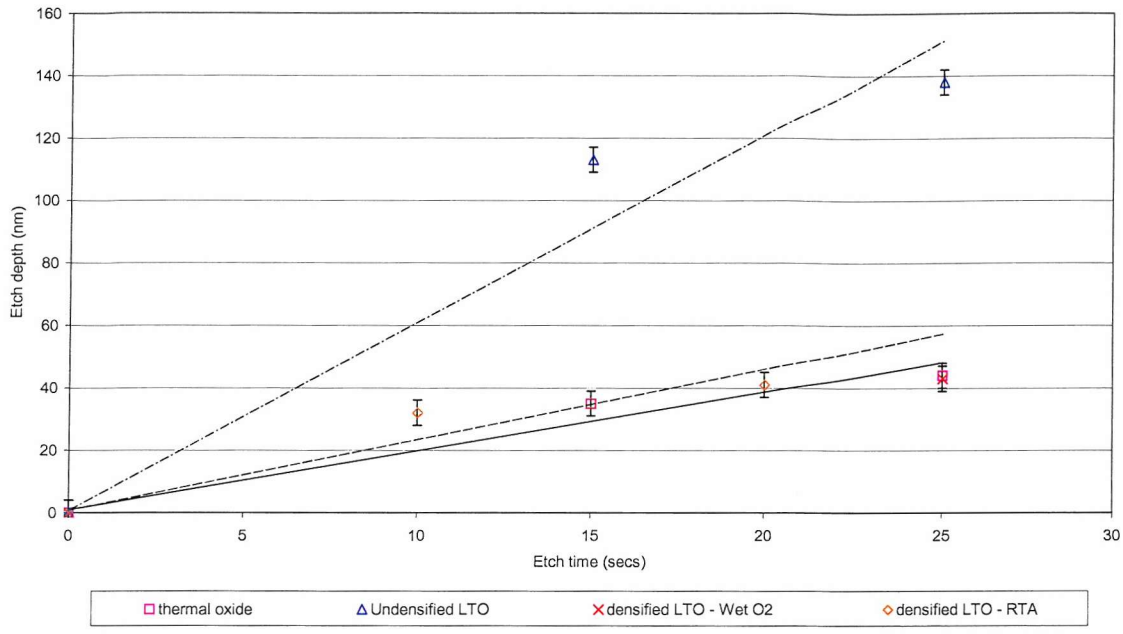


Fig. 4.4 Etch rate of thermal oxide, undensified and densified low temperature oxides.

4.2.2.2 Sacrificial Layer Etch

The sacrificial layer etch process is an important step in the cavity fabrication process. In the test cavity fabrication, two etchants were examined to find the one most suited for the process. They were, an isotropic SF_6 dry etch process and wet KOH etch. The main purpose of the sacrificial etch is to completely remove the sacrificial layer, which in the case of the test cavity, is polysilicon. The outcome of the sacrificial layer etch should be a rigid, freestanding hollow cavity, as shown in figure 4.3.

The SF_6 etch was carried out at a pressure of 150 mTorr, in a plasma energy of 80 Watt with an SF_6 flow rate of 50 sccm. The KOH etch was carried out 70°C in a KOH:H_2O_2 solution of 100:1. Prior to the KOH etch, wafers were briefly dipped in a buffered HF solution to remove any native oxide on silicon exposed areas.

The SF_6 etchant was found to be successful in removing the polysilicon sacrificial layer of the test cavities as shown in the SEM image in figure 4.19. The image shows a test cavity that is hollow and freestanding. However, some warping of the cavity ceiling can

be seen. This etch was carried out for 90 minutes, which corresponds to an etch-back distance of about 6 μm. Although the etch time is relatively long, the walls of the cavity have not been severely etched, confirming the high selectivity of the SF_6 etch.

As with SF_6, the use of the KOH wet etch was also found to completely remove the polysilicon sacrificial layer. Selectivity was found to be very good with minimal etching of the cavity walls. Warping of the cavity was also observed after the etch, similar to that seen after the SF_6 etch, indicating that warping is not dependent on the etch method but is due to non-uniform stress in the cavity walls, and this will be examined in more detail in the following section. Interestingly, although a wet etchant was used in the cavity process, no stiction was observed. As the size of the test cavities is small (less than 10×10 um^2), its susceptibility to stiction is reduced [95].

The results of the sacrificial layer etch show that the use of the dry SF_6 and wet KOH etch are both suitable for polysilicon sacrificial etching, giving cavity structures that are hollow and freestanding. In addition to this, epitaxial growth using the test cavity show no silicon deposition on the cavity walls, indicating that the etching is sufficient in removing the polysilicon sacrificial layer. If etching was incomplete, some silicon deposition is expected, especially on the inner walls of the cavity.

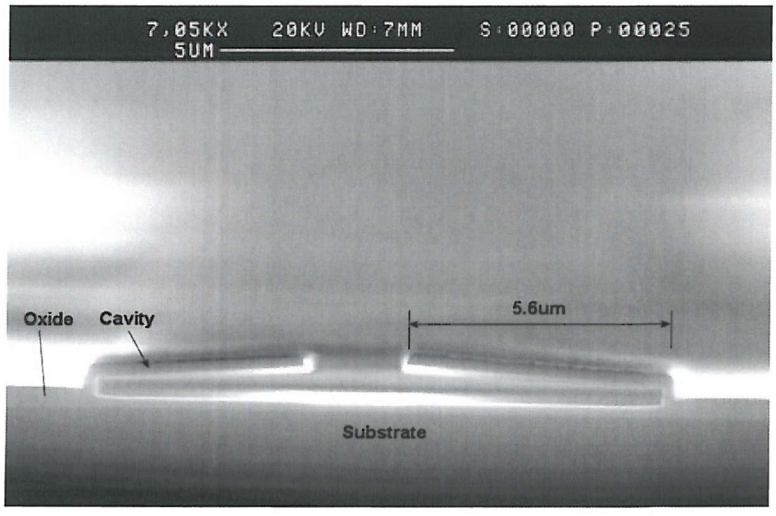


Fig. 4.5 A test cavity following an SF_6 polysilicon sacrificial layer etch.

4.2.2.3 Warping

Warping of the cavity ceiling was observed after every complete sacrificial etch step. Qualitative examination by SEM shows that the amount of warping is in general, dependent on the length of the cavity ceiling and the material used. All the cavities that were made from LTO were found to be warped and the amount of warping was found to be related to the ceiling length as shown in figure 4.6. The warping in the LTO test cavities is a result of non-uniform stress in the LTO layer, which may have formed as a result of the difference in thermal expansion coefficients between polysilicon and oxide after deposition [96]. Figure 4.6 shows that the ceiling deflects non-linearly with increasing length as indicated by the best-fit line. Figure 4.7 shows an external view of a test cavity made from LTO. The ripples on the cavity ceiling are an indication that the cavity is warped. These ripples are more visible when viewed by Normarski as shown in figure 4.9(a), where the interference patterns indicate the ripples seen under SEM. The warping or buckling of the cavity ceiling is an indication of residual stress within in the LTO layer, and is an indication of compressive stress [97, 98]. To alleviate this problem, cavities were also fabricated using a tri-layer combination of LTO – silicon nitride – LTO to form a stress-balanced structure, similar to that achieved by Choi *et al.*[99]. The basis of this idea is to make use of stress compensation (tensile in the nitride film, and compressive in the oxide film) by stacking multiple layers to approximate neutral stress. Although a simpler two layer LTO – silicon nitride scheme would give the same amount of rigidity, the outer LTO layer is needed because the selective epitaxial process is only selective to oxide. The result using this LTO/nitride/LTO sandwich is shown in figure 4.8. When compared to the LTO cavity in figure 4.7, it can be observed that the LTO/nitride/LTO cavity ceiling is free from any rippling. This shows that the use of LTO/nitride/LTO sandwich minimises rippling when compared the LTO cavity.

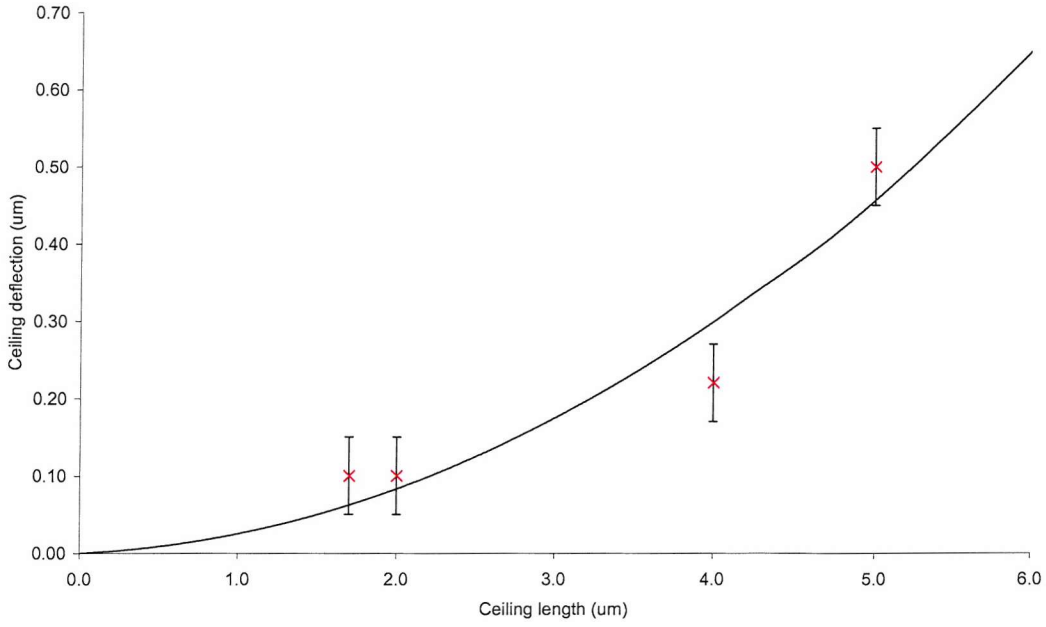


Fig. 4.6 Warping of test cavity ceiling made from LTO.

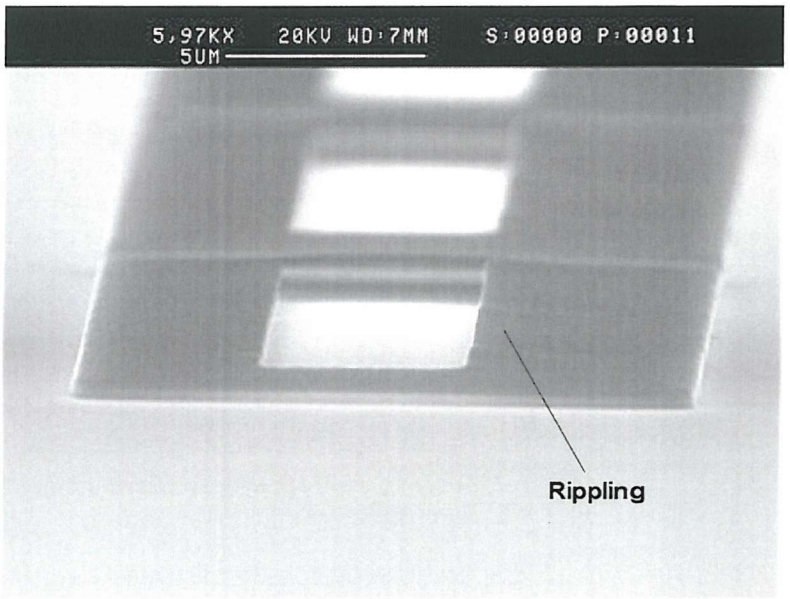


Fig. 4.7 Test cavities made from LTO only. Rippling on cavity ceiling is indicative of a warped ceiling.

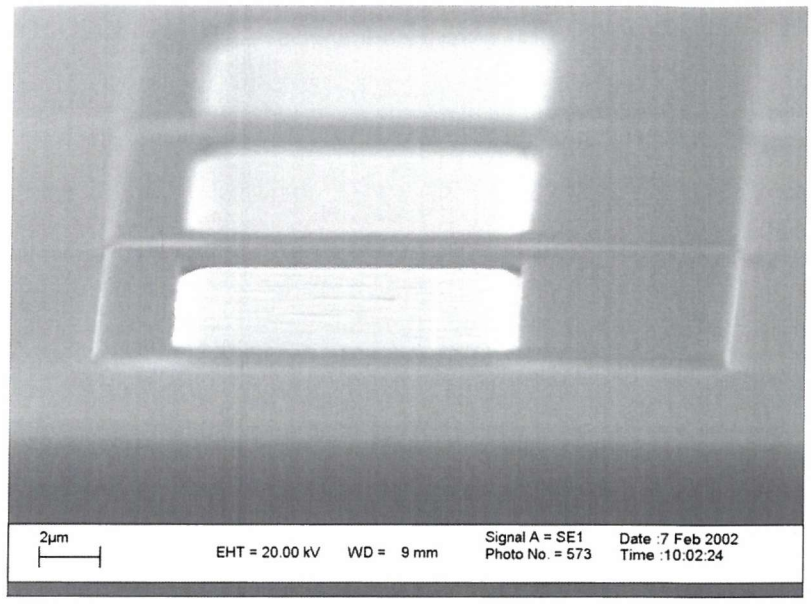
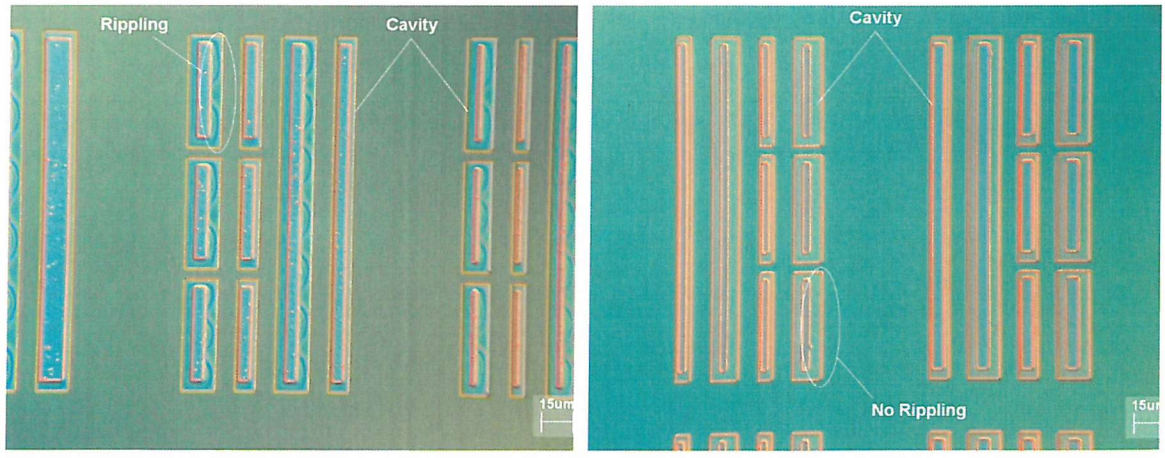


Fig. 4.8 Test cavity made from LTO/nitride/LTO sandwich. No rippling on the ceiling can be observed indicating the ceiling is not warped.



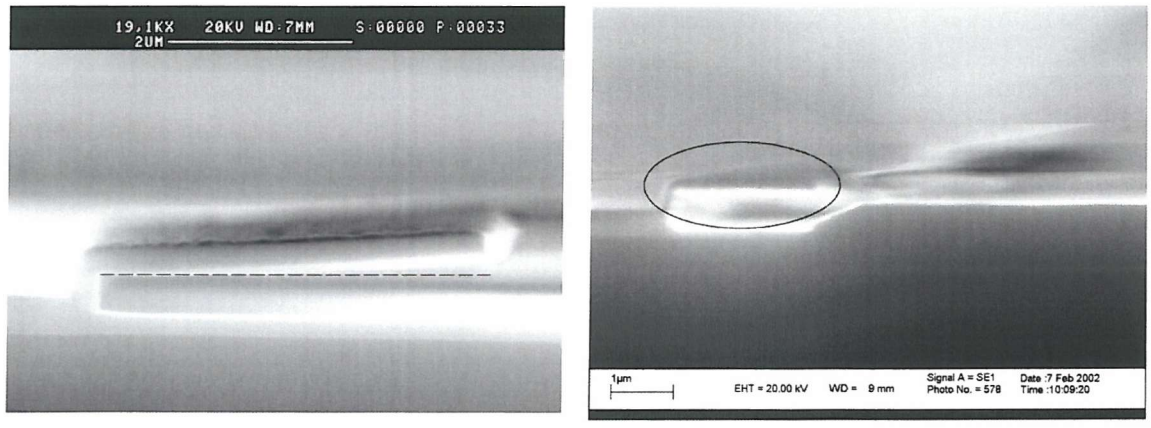
(a) (b)

Fig. 4.9 Nomarski image of (a) LTO cavity and (b) LTO/nitride/LTO cavity. The interference colours in (a) are indicative of a warped ceiling. This is not seen in the LTO/nitride/LTO cavities.

To examine the extent of warping, a cross section SEM was carried out on the LTO and LTO/nitride/LTO cavities. This meant that the cavity had to be cleaved through its cross section (it is likely that cleaving could redistribute the stresses in the cavity). Figure 4.10(a) and 4.10(b) are SEM images of an LTO cavity and LTO/nitride/LTO

cavity, respectively. Figure 4.10(a) shows the ceiling of the LTO cavity to be slightly warped. In comparison, the ceiling of the LTO/nitride/LTO cavity in Figure 4.10(b) is level with the wafer substrate. This shows that the tri-layer LTO/nitride/LTO combination is superior to the single layer LTO structure. LTO/nitride/LTO cavities measuring $10 \times 10\ \mu m^2$ with ceilings as long as 12 μm have been found to be free from warping. Such a cavity is shown in figure 4.11.

The results in this section shows that the LTO/nitride/LTO cavity is superior to LTO only cavity as it gives greater rigidity and is less effected by warping. The use of a tri-layer LTO – nitride – LTO structure does not add significant complexity to the overall cavity process as it needs only two extra process steps. Hence, subsequent cavities are fabricated using LTO/nitride/LTO sandwich layers.



(a) (b)

Fig. 4.10 (a) Warping of test cavity ceiling made from LTO. The dashed line shows the position of the ceiling if it was not warped. (b) Test cavity made from LTO/nitride/LTO sandwich. Not warping of the ceiling can be observed.

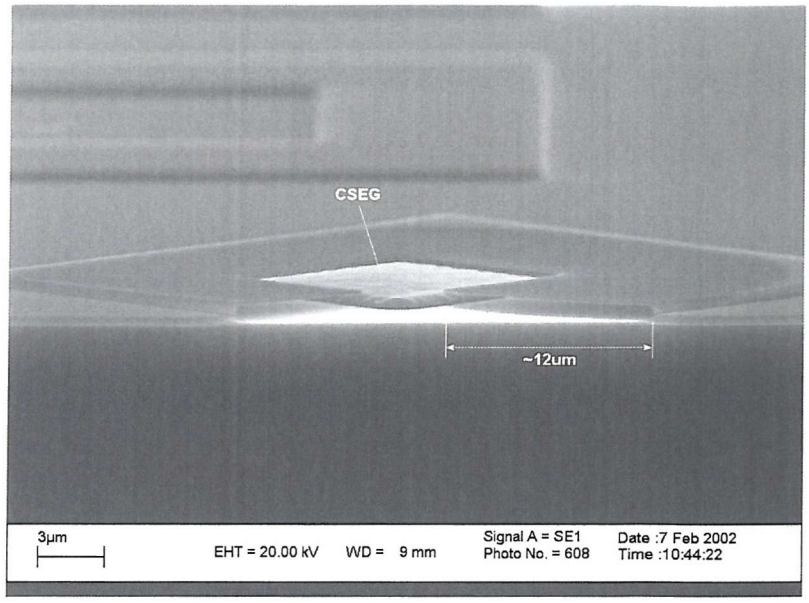


Fig. 4.11 A cavity made from an LTO/nitride/LTO sandwich with a ceiling of 12 µm. No warping of the ceiling is observed. Confined selective epitaxial growth (CSEG) can be seen in the center of the cavity.

4.2.3 Summary

The purpose of the test cavities was to examine the feasibility of the fabrication techniques, and then to apply successful techniques in subsequent cavity fabrication. The results in this section have shown that cavities should be fabricated using an LTO/nitride/LTO sandwich layer as it gives structures with good rigidity. It was also found to be compatible with the selective epitaxial growth process, which will be discussed in further detail later. The fabrication results also show that the sacrificial etching process can be carried out using either a dry SF_6 or wet KOH etch process without resulting in stiction problems. The methods highlighted here will be used in the following 'open sided cavity' process.

4.3 Open Sided Cavity

Fabrication of the open sided cavities was carried out to allow a study of confined lateral selective epitaxial growth. Unlike the test cavity, the open sided cavity has a

fully enclosed ceiling, which allows vertical growth to be confined. The sides of the cavity are designed to be open (hence, the term 'open sided') to provide a gas via and allow lateral epitaxial growth. When confined selective epitaxial growth is carried out, the epitaxy is expected to grow from the silicon seed situated at the centre of the cavity and overgrow laterally over the oxide and out of the side of the cavity. The open sided cavity will be fabricated using the techniques developed from the test cavity experiments. Figure 4.12 shows an illustration of the open sided cavity.

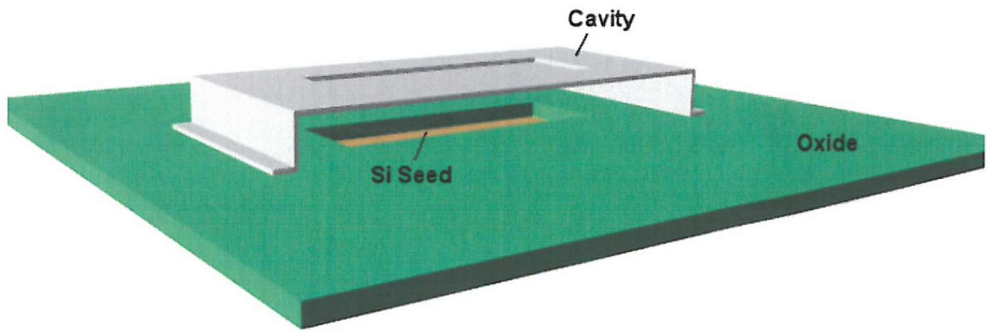


Fig. 4.12 3D view of an open sided cavity highlighting the opening on the sides of the cavity. The image also shows the silicon seed window in the centre, under the cavity.

4.3.1 Fabrication Process

The open sided cavity fabrication process begins with a thermal oxidation process which grows 200 nm of oxide. A seed window is then opened by dry etching. This is followed by a dry oxidation process which grows a thin oxide layer of about 30 nm (figure 4.13(a)). This dry oxidation step also consumes any surface damage that is caused by the dry etch process [100]. A layer of polysilicon, 500 nm thick, is then deposited. This forms the sacrificial layer, which is later etched. For the shell of the cavity, a triple layer consisting of LTO – silicon nitride – LTO is deposited (figure 4.13(b)), as used in the test cavity process. Next, the sides of the cavity are then dry etched. This is then followed by an isotropic SF_6 dry etch to remove the polysilicon sacrificial layer. As a comparison, a wet KOH etch was also carried out on a test wafer. Finally, the thin oxide protecting the seed window is removed using an isotropic dry

etch process (figure 4.13(c)) after which selective epitaxial growth is carried out. A full process listing can be found in the appendix.

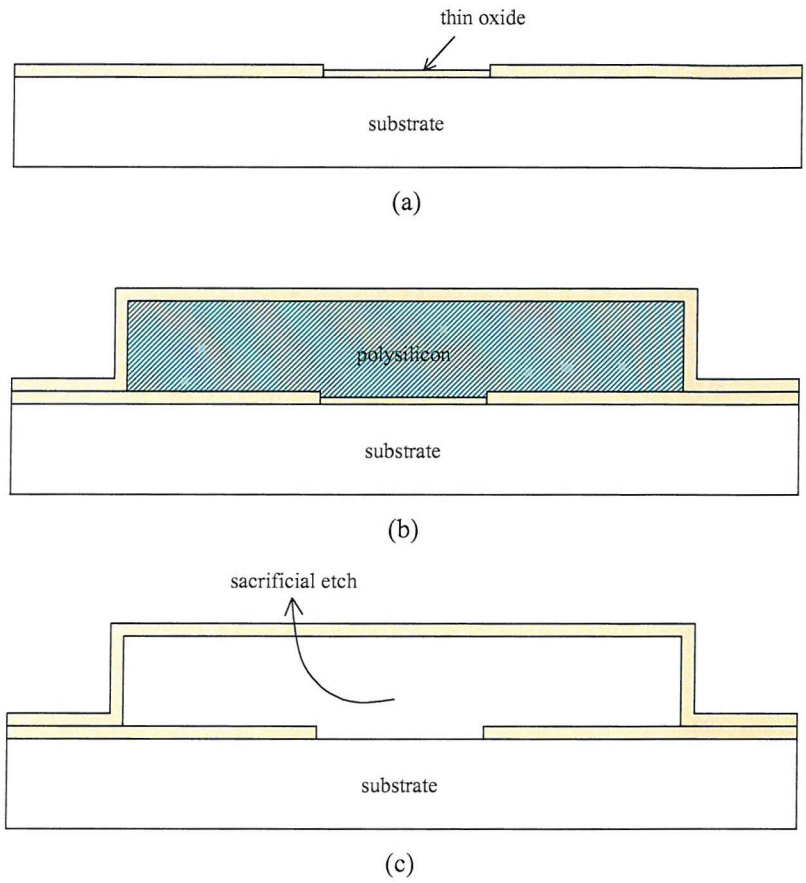


Fig. 4.13 Open sided cavity process. (a) Oxide deposition and patterning, followed by thin oxide growth. (b) Polysilicon followed by LTO deposition. (c) Polysilicon sacrificial layer etch followed by thin oxide removal.

4.3.2 Results of Open Sided Cavity Fabrication

4.3.2.1 Sacrificial Layer Etch

Figure 4.19 shows an open sided cavity after a polysilicon sacrificial layer etch, where the cavity structure can be seen to be hollow and freestanding. In the open sided cavity process, the sacrificial layer etch was carried out by dry etch (i.e. SF_6) and wet etch

methods (i.e. KOH). For the test cavities, the use of SF_6 resulted in the complete removal of the polysilicon sacrificial layer, as was the case with the test cavities. The use of KOH in the open sided cavity process also resulted in the complete removal of the polysilicon sacrificial layer. However, it was observed that once all of the polysilicon sacrificial layer has been etched, many of the cavities were found to suffer from stiction. The susceptibility of the cavity to stiction using KOH was found to be dependent on cavity size. Examination of the open sided cavities after etching show that the majority of the large cavities were affected by this problem. These are cavities measuring greater than 50 x 6 μm^2. However, smaller cavities, measuring smaller than 10 x 10 μm^2, were found to be unaffected. This indicates that the susceptibility of a cavity to stiction is to a great extent dependent on size. Figure 4.15 shows a cavity which suffers from the problem of stiction.

It is well known that wet processing methods, such as KOH, cause such problems and several techniques can be used to overcome this issue (e.g. phase-change release methods). However, these methods require special preparation of chemicals and apparatus. As a test to confirm that wet processing is indeed the cause of stiction, an SF_6-etched wafer with open sided cavities was dipped in deionised water for 3 minutes. The result of this was stiction similar to that after KOH etching. This highlights the unsuitability of the KOH as an etchant for the open cavity process. It also highlights a bigger problem, which is the inability to use wet processing (e.g. RCA clean) after the open sided cavity is fabricated. RCA clean is an important process, which is carried out prior to epitaxy growth to ensure good quality epitaxy. One method, which has been implemented to overcome this problem, is to carry out an RCA clean prior to the sacrificial layer etch, and to then immediately load the wafer into the epitaxy machine once the etched has been carried out. This is done to minimise the possibility of contamination.

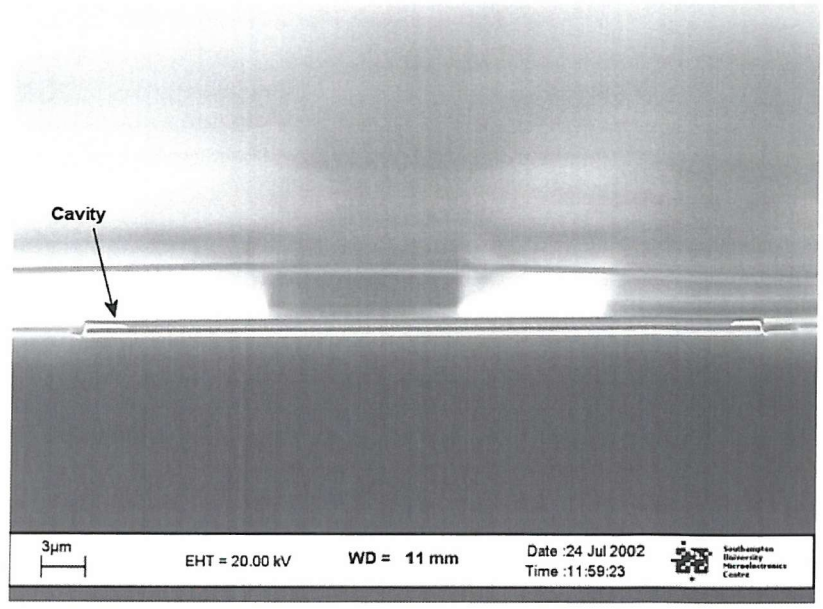


Fig. 4.14 An open sided cavity following an SF_6 sacrificial layer etch.

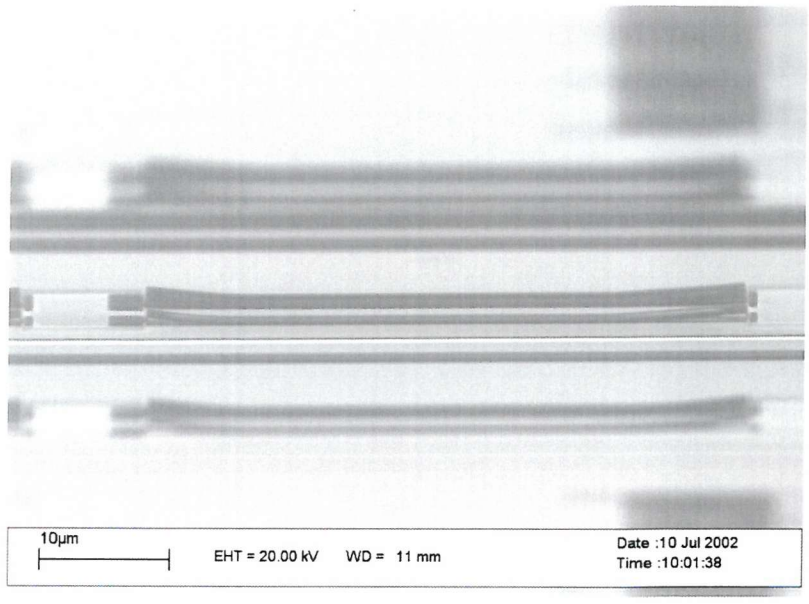


Fig. 4.15 Open sided cavity following a KOH etch. Larger cavities such as the one shown above were found to suffer from stiction.

4.3.3 Warping

The use of the LTO/nitride/LTO tri-layer sandwich in the open sided cavity process has been found to give both rigid and warped structures. The rigidity of the structures was found to be dependent on the size of the cavities. The open sided cavities can be divided by size into two groups – large cavities (measuring $\geq 6 \times 50\ \mu m^2$) and small

cavities (measuring $\leq 10x10\ \mu m^2$). All of the small open sided cavities were found to be free from warping. Of the large open sided cavities, a few were found to suffer from warping. This is despite the use of the LTO/nitride/LTO sandwich layer. Table 4.2 summarises this result. The table shows that the maximum open sided cavity that can be built without any indication of warping is $6\times160\ \mu m^2$. Some of the cavities that are $9\times160\mu m^2$ in size were found to be warped, however, others were found to be rigid. All of the cavities larger than $12\times160\ \mu m^2$ were found to be warped. This result shows that rigid freestanding open sided cavities can be successfully fabricated using the process above, but it is limited to a size of $6\times160\ \mu m^2$. Figure 4.16 shows an SEM image of a 45 μm long open sided cavity that is free from warping.

Type	Size (μm^2)	Warped
Large Cavities	6×50	No
	9×50	No
	12×50	No
	14×50	No
	15×50	No
	6×160	No
	9×160	Some
	12×160	Yes
	14×160	Yes
	15×160	Yes
Small Cavities	1×1	No
	2×2	No
	3×3	No
	5×5	No
	10×10	No

Table 4.2 Open sided cavities that are warped / not warped. $6\times160\ \mu m^2$ is the maximum cavity size that can be built without being effected by warping.

The reason for the warping is likely to be due to non-uniform stress distribution in the material. This is clearly shown in the case of the test cavities made from LTO only. In theory, the cavity ceiling can be represented as a cantilever beam fixed at one end. As the cavity is made from a single type of material, it should not exhibit any significant warping if its intrinsic stress is uniform as any expansion should occur in the

longitudinal direction. However, if the stress in the material is non-uniform then any material expansion will result in warping. In the case of the LTO cavity, the bending of the cavity ceiling is an indication that the intrinsic stress of the material is non-uniform. This is clearly visible in the SEM images and from optical inspection using a Nomarski filter.

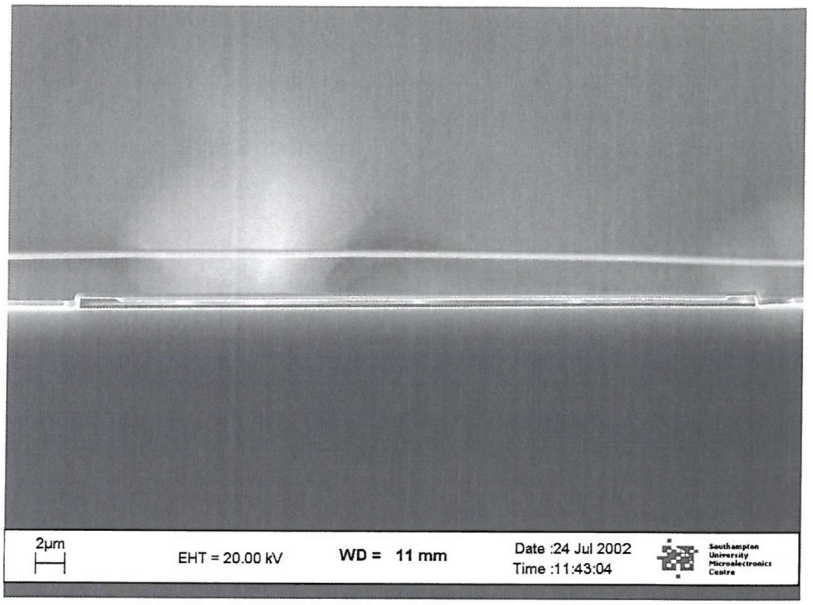


Fig. 4.16 Open sided cavity with level ceiling. Cavity length is 50 µm.

4.3.4 Summary

The results of the open sided cavity experiments show that the size of the open sided cavities (etched by SF_6) should be limited to a maximum of 6×160 µm^2, as cavities that are larger than this are susceptible to warping. The results also show that the use of a wet KOH sacrificial etch causes stiction problems and therefore, dry etch methods, such as SF_6 should be used instead. However, KOH can be used in the open sided cavity process if the cavities measure less than 10 x 10 µm^2. In addition to this, wet cleaning methods such as RCA also need to be avoided after a sacrificial etch is done in order to avoid stiction problems. Instead, dry cleaning methods should be used. Within the limits outlined in this summary, open sided cavities that are suitable for confined lateral epitaxial growth can be successfully fabricated.

4.4 Silicon on Insulator (SOI) Cavity

Confined lateral epitaxial growth is achieved using the open sided cavity by the overgrowth of silicon from a planar seed window over oxide. As it will be shown in chapter 6, the volume of lateral growth is dependent on the growth rates of the silicon facets that have a lateral growth component. To achieve a high lateral growth rate, a vertical {1 0 0} plane is highly desirable. However, when lateral epitaxial overgrowth develops from a planar seed window, the lateral growing plane that develops is not necessarily the {1 0 0} plane. Instead, slower growing planes such as the {3 1 1} or the {1 1 1} develop. An SOI cavity approach has been developed to try to overcome this "faceting" problem by providing a vertical rather than planar seed window. SOI substrates provide a possible route to cavity formation within which a silicon sidewall that, already in the <1 0 0> direction (i.e. {1 0 0} plane), can be placed. This should result in lateral growth on the {1 0 0} plane, with a growth rate that is similar to vertical epitaxial growth in the same experimental conditions. This is illustrated in figure 4.17.

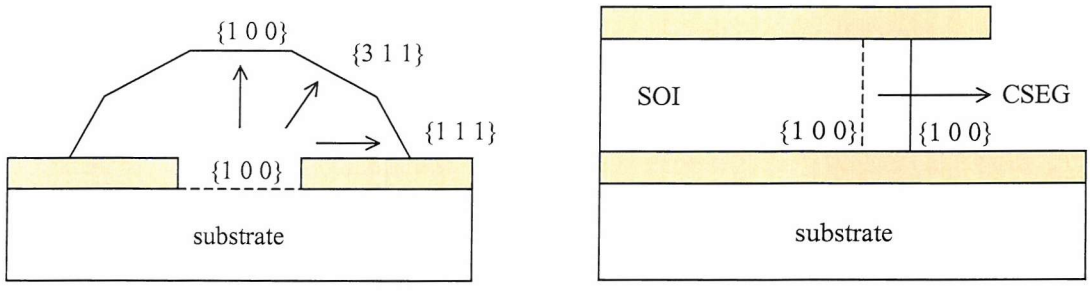


Fig. 4.17 Comparison of growth from a (a) planar seed, and (b) vertical seed. The {1 0 0} is the fastest growing plane and would be the preferred plane for lateral growth. Growth from a {1 0 0} sidewall ensures that the lateral growth rate (on the {1 0 0} plane) is maximised.

4.4.1 Fabrication Process

The wafers used in the SOI cavity fabrication process are n-type 100 mm silicon-on-insulator wafers. The SOI wafer has a silicon active layer thickness of 2 μm and a

buried oxide thickness of 460 nm. To fabricate the cavity, a layer of LTO is first deposited, followed by a layer of silicon nitride and another layer of LTO. This forms an LTO/nitride/LTO sandwich, as used in the open sided and test cavity processes (figure 4.18(a)). These layers are then densified by rapid thermal annealing at 980°C for 20 seconds. Next, the wafers are patterned and the LTO/nitride/LTO sandwich layer is dry etched. A deep silicon etch using trifluromethane (CHF_3) is then used to etch the SOI layer, which results in a vertical silicon sidewall (figure 4.18(b)). The SOI layer is then etched back using an isotropic SF_6 dry etch (figure 4.18(c)), several wafers were also etched using a wet KOH process. Unlike the test and open sided cavity processes, the SOI cavity process does not require the use of a polysilicon sacrificial layer, instead, the etch removes part of the SOI layer to provide a cavity and a single crystal seed. This process is then followed by an etch damage removal (EDR) to remove any defects caused by the dry etching [100], before epitaxial growth is carried out. Figure 4.18 illustrate the SOI cavity fabrication process.

Fig. 4.18 Cavity fabrication process using SOI. (a) Deposition of LTO/nitride/LTO sandwich layer. (b) Dry etch of sandwich and SOI layer. (c) Etch back of SOI layer by an SF_6 dry etch.

4.5 Results of SOI Cavity Fabrication

4.5.1 Sacrificial Layer Etch

In the test and open sided cavity processes, the SF_6 dry etch was successfully used to remove the sacrificial layer. In the SOI cavity process, a complete removal of the SOI layer is not required, instead the single crystal layer only has to be partially etched back to form a cavity. The use of the SF_6 isotropic dry etch back process was found to be suitable for the etch-back of the SOI layer, as shown in figure 4.19. This etch was carried out for 60 minutes, and corresponds to an etch-back distance of ~ 8 μm.

Although the SF_6 successfully removed silicon crystal silicon without damaging the cavity LTO, the surface of the sidewall after etching was found to be very rough and roughness of the sidewall seed is problematic to both device properties and the development of lateral epitaxial growth (see section 6.6). Inspection of the sidewall before the etch-back revealed that the surface of the silicon sidewall was already rough and rippled. The rippling on the sidewall is attributed to ripples that are present on the photoresist, a common problem in fabrication [101]. These ripples are translated onto the SOI sidewall during the deep silicon etch. The roughness that is observed on the sidewall is believed to be a characteristic of the deep silicon etch process (CHF_3). Qualitative comparison of the sidewall before and after the etch-back shows the sidewall to be rougher after the SF_6 etch, indicating that the SF_6 increases the roughness of the SOI sidewall. Section 4.5.2 will look at several possible solutions to this problem in more detail.

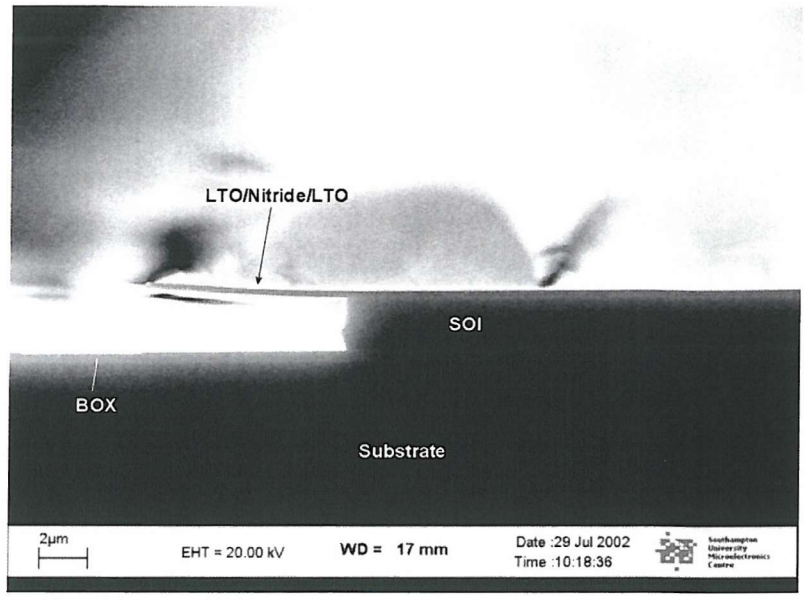


Fig. 4.19 SOI cavity following an SF_6 sacrificial layer etch.

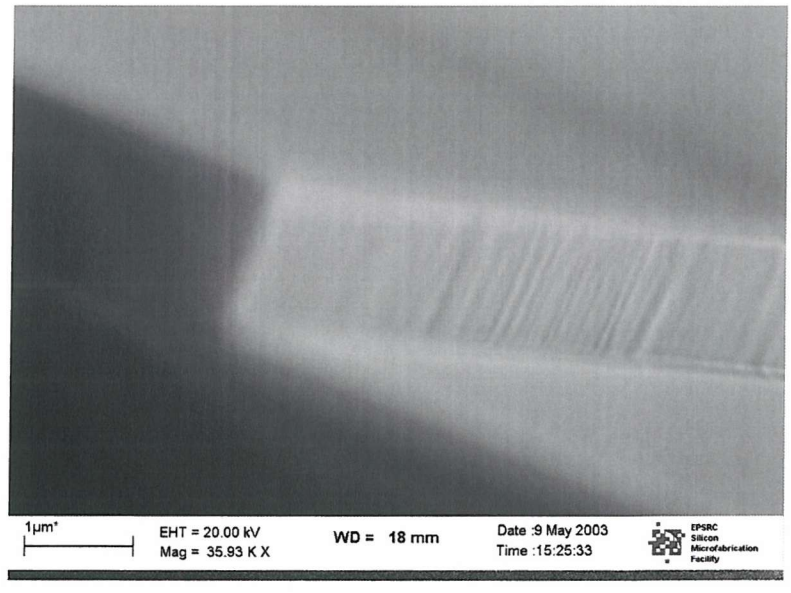


Fig. 4.20 SEM of SOI sidewall after 30 minute SF_6 etch back. The sidewall is visibly rippled.

When KOH was used to etch back the sacrificial layer in the SOI cavity process, the etch-back proceeded anisotropically along the crystal plane of the silicon on insulator layer. For features oriented along the <1 0 0> direction, the etch-back proceeded along the {1 0 0} plane, as shown in figure 4.21(a). However, for features oriented along the <1 1 0> direction, the etch-back proceeds along the {1 1 1} plane, resulting in an etch back profile such as that shown in figure 4.21(b).

Unlike with the open sided cavities none of the SOI cavities suffered from stiction problems. This is mainly due to the relatively short depth of the SOI cavities (i.e. < 8 μm) when compared to the length of the open sided cavity (i.e. up to 160 μm). In terms of roughness, the silicon sidewall which has been etched back was seen to be smoother than the original sidewall, indicating that the KOH etch has the effect of smoothing, or planarising, the silicon surface.

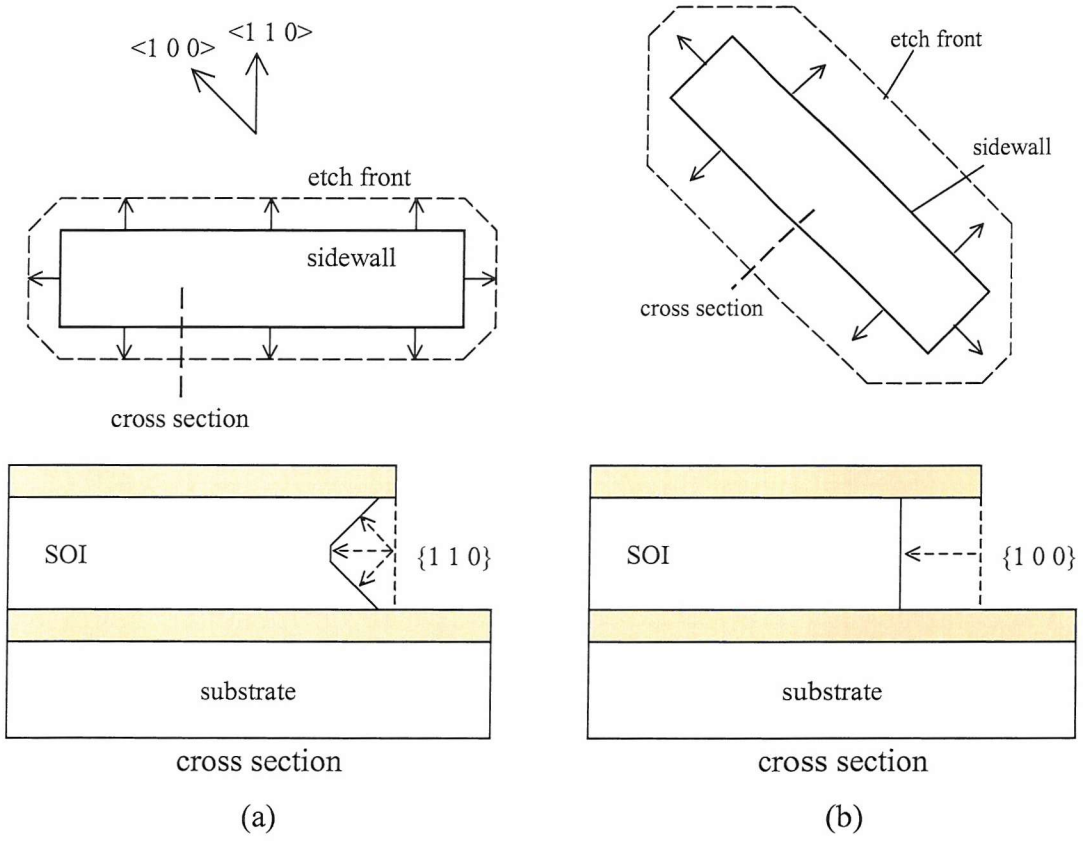


Fig. 4.21 KOH etch back from (a) a {1 1 0} sidewall results in a faceted sidewall whereas (b) etching a {1 0 0} sidewall results in a vertical sidewall.

4.5.1.1 Etch Back Uniformity

Etch-back uniformity was not an issue in either of the test or open-sided cavity processes because the sacrificial layer is completely removed in those processes. However, uniformity becomes an issue in the SOI cavity process as the etch-back

defines the depth of the cavity and this must be accurately known for device design.

In the lateral HBT fabrication process, the position of the transistor base has to be aligned accurately under the base contact window during selective epitaxial growth. One of the factors that determines the accuracy of the base placement is etch back accuracy. If the amount of etch back can be reliably known, then the base can be positioned provided the epitaxial growth rate is also accurately known. The precision of the etch back can be determined by looking at its uniformity. To do this, the amount of etch back, carried out using SF_6, of various cavities across the wafer was examined.

The results of these measurements are shown in figure 4.22. The results show that the amount of etch back is dependent on the thickness of the SOI layer. The relationship between the two features was found to be linear, as highlighted by the straight line of best-fit added to the figure. As there would be no etching if the thickness of the SOI is zero, the best fit line passes through zero of the x and y-intercepts. From the slope of the best fit, the etch rate dependence on SOI thickness was found to be 0.12 min^{-1}. The error bars indicate the accuracy of the etch-back measurement when examined by SEM. At 2μm feature size distance measurements have an error of +/- 60 nm.

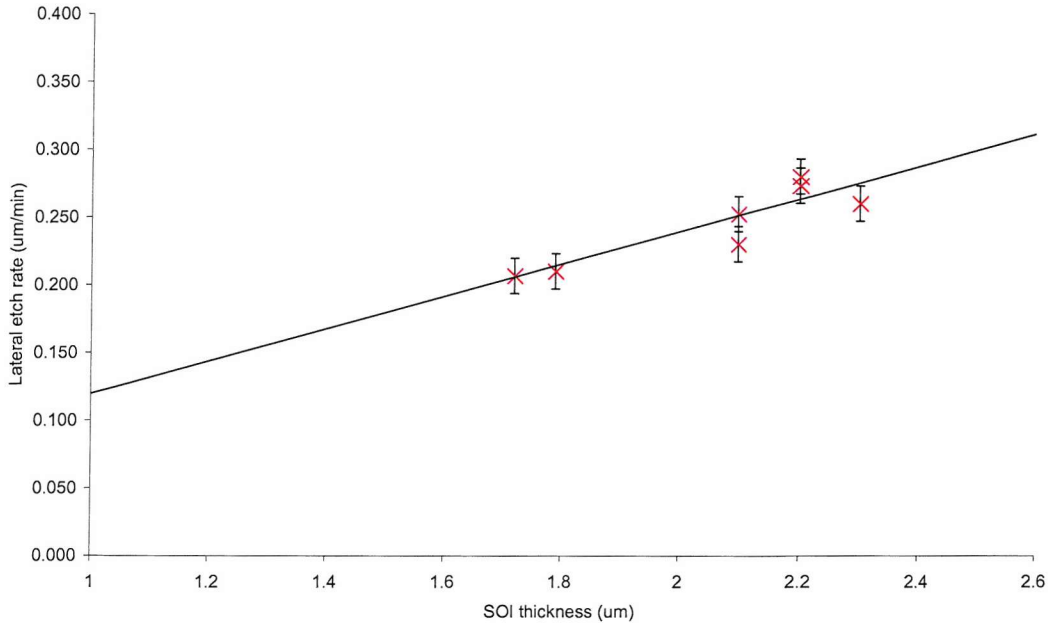


Fig. 4.22 Graph showing etch back dependence on SOI thickness.

The graph shows that there is a linear dependence between the etch rate and SOI thickness, which means that any variation in the thickness of the SOI layer will have an effect on the etch back. The thickness of the active layer of the SOI wafers used in this work varies +/- 250 nm around an average thickness of 2 μm. This means that the etch rate could vary by +/- 30 nm/min. In the lateral transistor design, the amount of etch back that is required is 0.5 μm. This corresponds to an etch time of 125 seconds for an average SOI thickness of 2 μm. With the uniformity stated above, carrying out an etch back for this amount of time will result in a variation of etch back between 440 nm and 560 nm. Hence, an extra tolerance of 120 nm has to be taken into account when deciding on the minimum basewidth that is acceptable in the lateral bipolar transistor design.

4.5.2 Silicon Sidewall Ripple Reduction

In the SOI cavity process, severe rippling was observed on the silicon sidewall after etch-back. The surface condition of a silicon seed is a factor which greatly affects the quality of epitaxial layers. The importance of surface quality is highlighted in section 6.7, where it is shown how epitaxial growth from a rough vertical seed results in rippled epitaxial layers with slow and unpredictable growth rates. In comparison, epitaxy on a smooth horizontal seed window is found to give good epitaxial quality with two dimensional growth and relatively fast and predicable growth rates. In order to achieve satisfactory lateral epitaxial growth from a vertical seed window, the roughness or ripples on the vertical silicon seed has to be reduced or eliminated. In fact, the vertical seed has to be "epi-ready". In this section, several silicon rippling reduction methods are examined.

Resist sidewall rippling is a problem that can occur in semiconductor processing. The irregular rippling, in both width and depth, on the resist sidewall often result in striations and roughness on the sidewall of the etched layer [101]. The seriousness of the problem is largely dependent on the device or structural requirements, and is often

only an issue if the quality of an etched sidewall is of importance (e.g. micro-mirrors, epitaxy, vertical MOS) [101, 102]. The reticulation on the resist sidewall is due to stress caused by the shrinking of the resist during post-exposure bake, a result of insufficient curing. In addition, reticulation can also occur due to interference fringes along the resist sidewalls in conventional lithography [102].

Four ripple reduction methods were examined in this work. The first, second and third methods involve carrying out specific processing steps after the silicon sidewall has been defined. The third method proposes a different method to fabricate the silicon sidewall.

The first method uses a combination of oxidation and wet etching to achieve smoother silicon sidewalls. The idea behind this method is that any protruding edges on the sidewall will oxidise at a faster rate than a flat surface, and this should have the effect of smoothing the rough surface. The process requires the wafer to be oxidised at 950°C in wet O_2 for 20 minutes. This process grows ~60 nm layer of oxide. This is then dipped in 7:1 buffered HF for approximately 45 seconds, which removes the grown oxide. Simulation results suggested that this process could reduce the magnitude of rippling by 50%, from 80 nm to 40 nm

The second rippling reduction method makes use of the anisotropic KOH wet etch. In this work, the silicon sidewall is orientated to the {1 0 0} plane and it ought to be possible to exploit anisotropic etching to reveal the {1 0 0} facet. During anisotropic etching etch fronts should progress to reveal facets belonging to the slowest etching planes. In the case of the silicon sidewall orientated to the {1 0 0} plane, surface roughness composed of higher-index facets can be etch more rapidly than the {1 0 0} plane. Provided the surface is not so rough as to cause the occurrence of other lower-order factes (e.g. {3 1 1} or {1 1 1}), anisotropic etching can, in principle, be used to produce a flat {1 0 0} vertical seed. Total etch time was 2 minutes in KOH at 70°C.

The third method used KOH with the addition of methanol. It is similar to the KOH wet etch process, and has been used at SUMC in NMOS processing to give smooth silicon etched layers. This etch was carried out for 2 hours at 28°C. The long etch time (in comparison to the KOH etch) is due to the low temperature of the KOH + methanol

etch, which was necessary due to safety reasons.

The fourth method makes use of a hard mask to reduce the rippling. The fabrication process of the mask, which is shown in figure 4.23, does not rely on dry etching to define its geometry. Instead, it is defined by wet etching. This is done to avoid translating the ripples in the photoresist sidewall onto the hard mask. The hard mask is prepared by first depositing a layer of oxide (300 nm). It is then patterned by wet etching using 7:1 buffered HF, which creates a sloped undercut below the photoresist. A blanket layer of nitride is then deposited and dry etched. This leaves a nitride fillet at the edge of the oxide hard mask. Using the hard mask, the exposed silicon layer is then dry etched to produce a silicon sidewall.

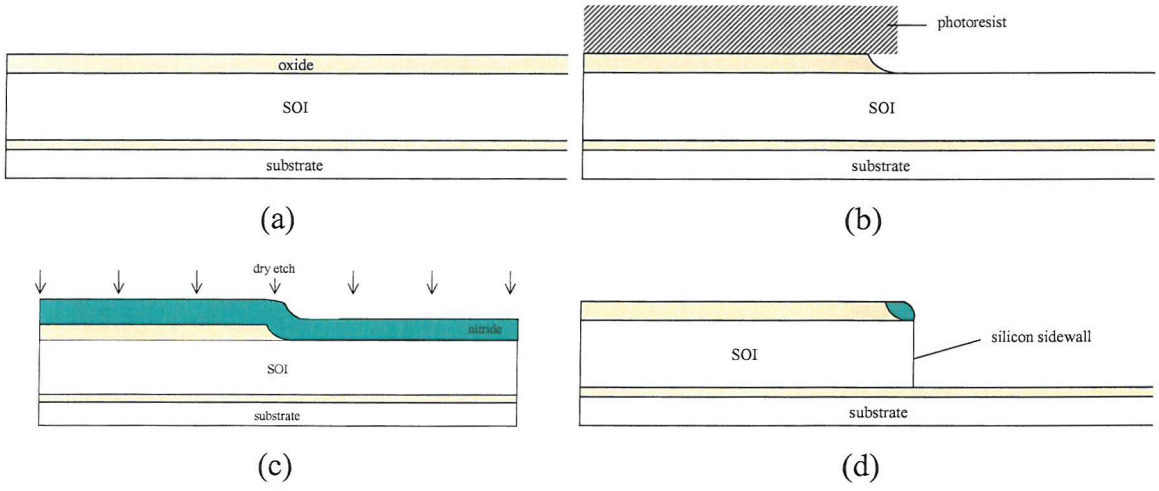


Fig. 4.23 Fabrication of silicon sidewall using hard mask. (a) Oxide deposition, (b) Wet oxide etch under photoresist, (c) Nitride deposition followed by blanket dry etch, (d) Silicon dry etch using oxide hard mask.

4.5.2.1 Results

Figure 4.24(a) shows an SEM image of a silicon sidewall before any rippling reduction is carried out, while figures 4.24(b) to 4.24(d) show the surfaces of silicon sidewalls after each rippling reduction experiment. Each image is typical of the quality of all silicon sidewalls after each process is carried out. All of the images show the <1 0 0>

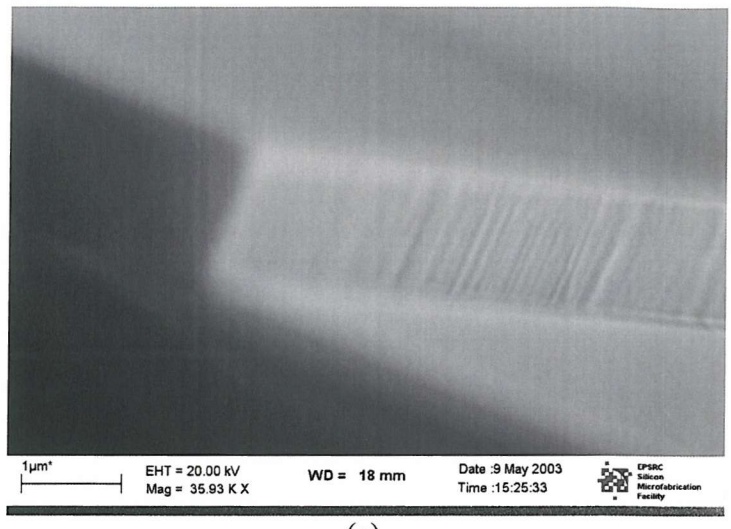
oriented sidewall as it is the plane of most interest in this work.

In this experiment, the silicon sidewall was evaluated qualitatively from SEM observations. Unfortunately, attempts to quantitatively measure the ripples by atomic force microscopy (AFM) have so far been unsuccessful as the AFM is unable to take an accurate profile of a silicon sidewall. Attempts to estimate the sidewall ripples from a surface profile have also been unsuccessful due to the large height differences between the top and bottom of the sidewall.

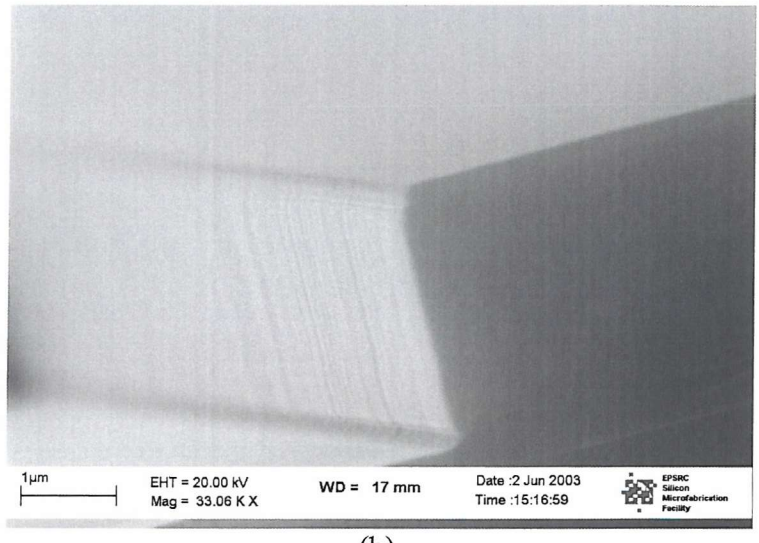
Figure 4.24(b) shows the surface of a silicon sidewall after a wet oxidation + buffered HF process. The magnitude of the ripples on the sidewall appear to be reduced when compared with those in figure 4.24(a) (i.e. before rippling), indicating that the roughness has been reduced. However, sharp linear features, can still be observed in the image which indicate that the wet oxidation + buffered HF process does not sufficiently remove the rippling on the sidewall.

In comparison, figure 4.24(c) shows how the rippling reduction experiment using KOH for 5 minutes results in silicon sidewalls that are very smooth with no signs of rippling. The depth of the etch back after 5 minutes was found to be ~500 nm. Similar results were also obtained using KOH + methanol, as show in figure 4.24(d). However, some striations on the silicon sidewall can be seen, indicating that some rippling is still present. The depth of the etch back after 2 hours was found to be ~200 nm, less than the KOH etch. Although not totally smooth, the result of the KOH + methanol etch is promising and further etching may remove the rippling entirely.

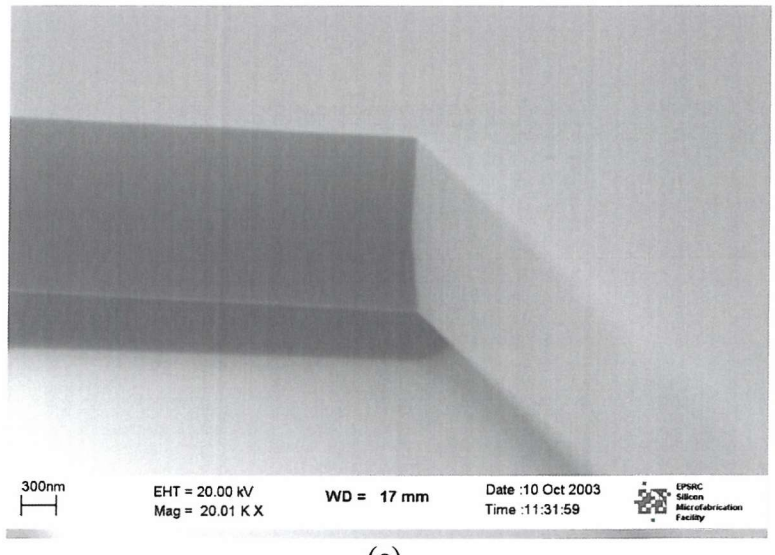
The result of the fourth rippling reduction experiment, which makes use of a hard mask to form ripple free SOI sidewalls, is shown in figure 4.24(e). The SEM image shows that the hard mask process was generally unsuccessful. The deep silicon etch was found to have completely remove the hard mask layer, which indicates that the thickness of the hard mask (300 nm) was insufficient in protecting the masked SOI layer from being etched. In addition to this, the rippling on the SOI sidewall shows that the process is unsuited to give rippled free layers. Further optimisation of the hard mask technique may give better results, however, due to the good result obtained using the KOH etch, this was not carried out.



(a)

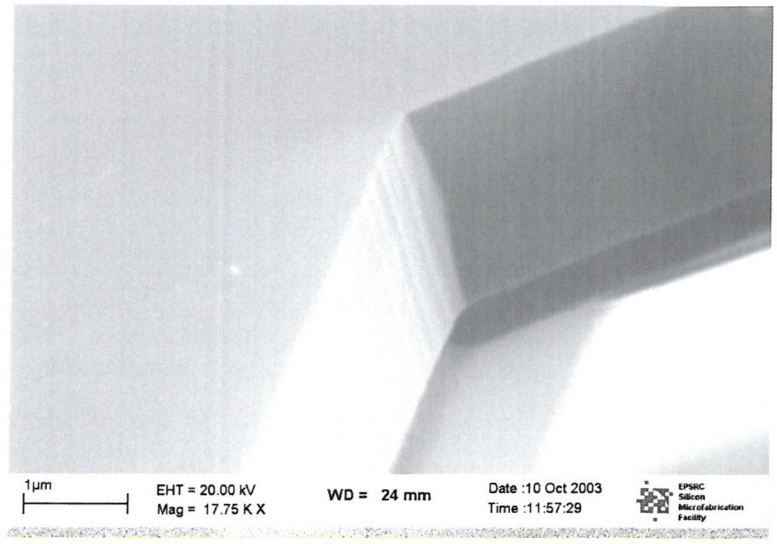


(b)

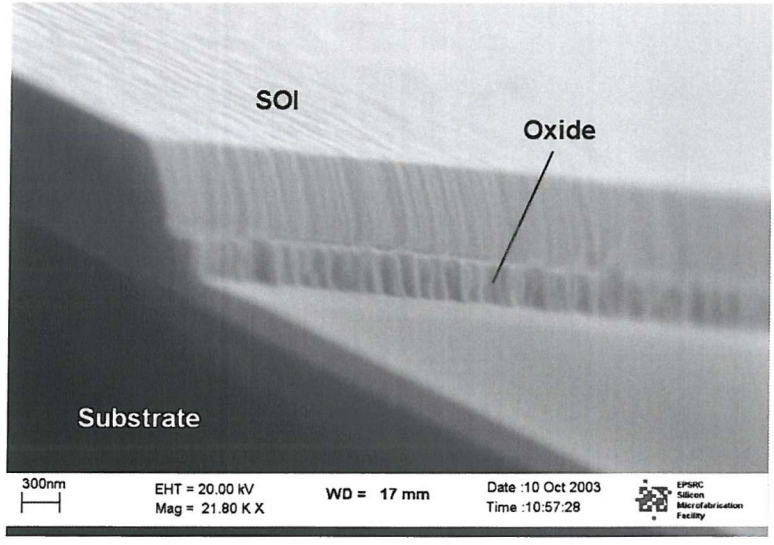


(c)

Fig. 4.24 Silicon sidewall (a) before rippling reduction, (b) after wet oxidation + buffered HF dip. (Figures continue following page)



(d)



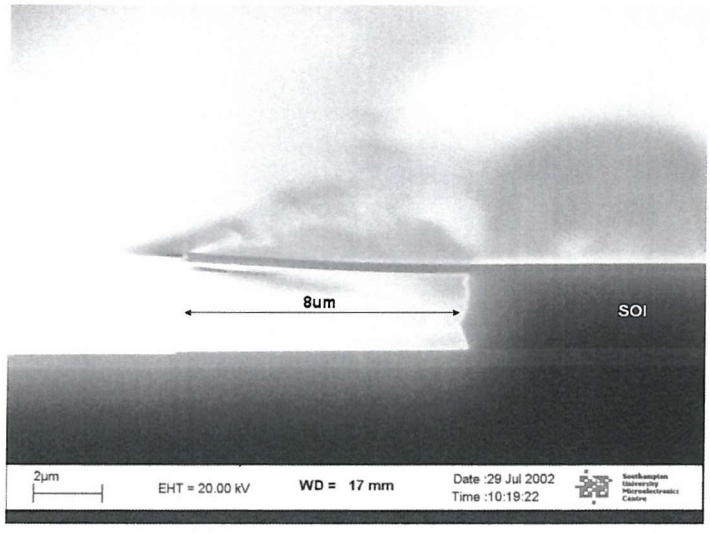
(e)

Fig. 4.24 Silicon sidewall (d) after KOH etch, (c) after KOH + methanol etch, (e) prepared by hard mask technique.

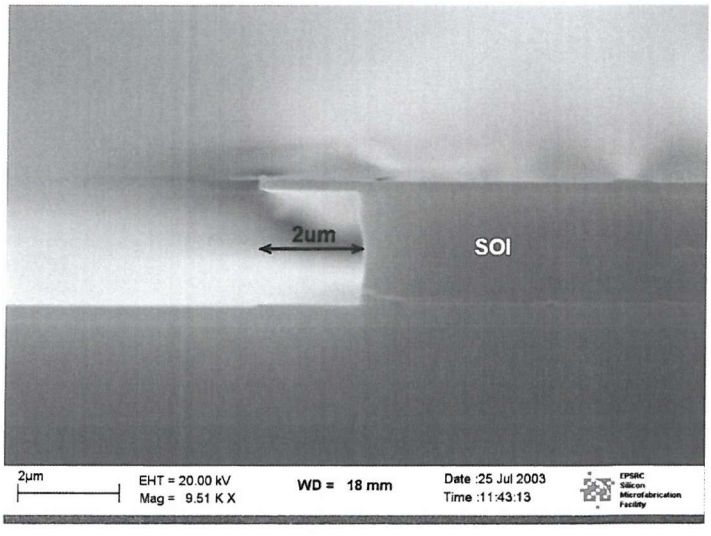
The results above show that the KOH etch process was found to be the best of the ripple reduction methods at removing the silicon ripples on the sidewall. In order to remove the ripples, the silicon sidewall has to be etched back by at least 500 nm. The etch rate of the KOH etch (i.e. 100 nm/min) is advantageous for this purpose as it allows a precise etch back to be carried out. As etch back is already required in the lateral transistor fabrication process the KOH etch can be used as a combined etch back, ripple reduction step. Although the other etch processes were not able to completely remove the sidewall rippling, each process was able to reduce rippling to some extent, with the exception of the hard mask technique.

4.5.3 Warping

Warping was in issue that affected the test and open sided cavities to varying degrees, it is also a problem for SOI cavities. Figure 4.25(a) shows an 8 μm deep SOI cavity with a ceiling that is warped by ~ 350 nm. The majority of SOI cavities have been found to be affected by this problem. However, the problem is minimised if a shallow etch-back is carried out, etch-backs of ~2 μm (figure 4.25(b)) result in no visible warping while providing cavities large enough to produce lateral HBT devices.



(a)



(b)

Fig. 4.25 (a) 8 μm SOI cavity with a slightly warped ceiling (b) A 2 μm SOI cavity with flat ceiling.

4.5.4 Summary

The SOI cavity process was established as an alternative route to confined lateral epitaxial growth. With the SOI cavity, the silicon sidewall serves as the seed for the growth, removing the need for lateral epitaxial overgrowth from a planar seed window, as is the case with the open sided cavities. The fabrication results presented in this section show that both SF_6 and KOH can be used in the etch-back process. However, the latter is preferred as it removes rippling on the silicon sidewall, an inherent problem with the photolithographic process. Shallow etch-backs of up to 2 μm have been found to give SOI cavity structures that do not suffer from stiction or warping problems, and this is well within the specification needed for a lateral device.

4.6 Conclusion

In this section, three types of cavities have been fabricated. They are the test cavity, open sided cavity and SOI cavity. Of the three, the two latter cavities can be used for fully confined lateral selective epitaxial growth. The differentiation between the open sided cavity and the SOI cavity is the former allows confined growth to be carried out from a planar seed window, while the latter allows growth from a vertical (sidewall) seed. In this work, several specific aspects of cavity fabrication were examined in detail, this includes sacrificial etching, warping and silicon sidewall rippling reduction. For sacrificial etching, the use of both SF_6 dry etch and wet KOH etch process were generally found to be suitable for the removal of the polysilicon or silicon sacrificial layer. However, the use of KOH was limited by stiction, and thus, should only be used in fabricating small sized cavities. Warping was a problem that affected all of the cavities. Initial use of densified low temperature oxide as the cavity material was found to be insufficient in providing warp free cavity structures. However, the use of an LTO/nitride/LTO sandwich layer greatly minimises this problem and hence, was implemented in all of the cavity designs. Silicon sidewall rippling was an issue that only concerns SOI cavities. Several rippling reduction methods were examined in this work, and out of these, the use of an anisotropic wet KOH etch process was able to significantly minimise the amount of rippling.

Chapter 5

Selective Epitaxial Growth using SiH_4

At Southampton University Microelectronics Centre, selective epitaxy growth has mainly been carried out by low pressure chemical vapour deposition with silane as the only source gas. This process has been used to grow high quality epitaxial layers with good selectivity. It has also been found reliable and reproducible, and has been used in many successful device fabrication processes [58, 103, 104]. In this work, the SUMC silane only epitaxy process is examined to determine its feasibility in meeting the requirements for confined selective epitaxial growth. These requirements are thick epitaxial lateral growth, good selectivity, low thermal budget, good uniformity and good epitaxial quality. Some of these requirements have already been examined to a certain extent by Bonar *et al.* [46, 49, 105], however, these earlier experiments with silane only selective epitaxial growth were mainly focused on the growth of thin layers for vertical devices (i.e. vertical BJTs and HBTs). In this chapter, the use of the silane process for thick epitaxial growth and lateral growth will be examined.

5.1 Epitaxial Growth

Several experiments were carried out to examine the feasibility of thick selective epitaxial growth using silane. All growths were carried out at 980°C at a pressure of

1 Torr. These growth conditions were chosen as previous growth studies have shown that epitaxial growth at these temperatures and pressures provide the best epitaxy quality and selectivity [46]. Growths were carried out for 5, 12, 20 and 30 minutes. All of the wafers were prepared for the epitaxial growth as described in section 3.4.

5.2 Results

In this work, the epitaxial layers were examined by Nomarski optical microscopy and scanning electron microscopy (SEM). Figure 5.1 and 5.2 show the surface of wafers, as viewed by the Nomarski, after 20 and 30 minutes of growth, respectively. In both growths, single crystal epitaxy was observed in the seed windows, identifiable by the smooth morphology of the grown layers (although not shown here, the epitaxial layers produced by the 5 and 12-minute growths were found to be of similar quality). Although generally smooth, epitaxial material situated close to oxide sidewalls is found to be rippled. These ripples are seen in all growths, and are a result of an interaction between the epitaxial growth front and the oxide sidewall; in particular the ripples in the epitaxy are seen to correspond to the rippling of the sidewall that is caused by pixilation of the photoresist.

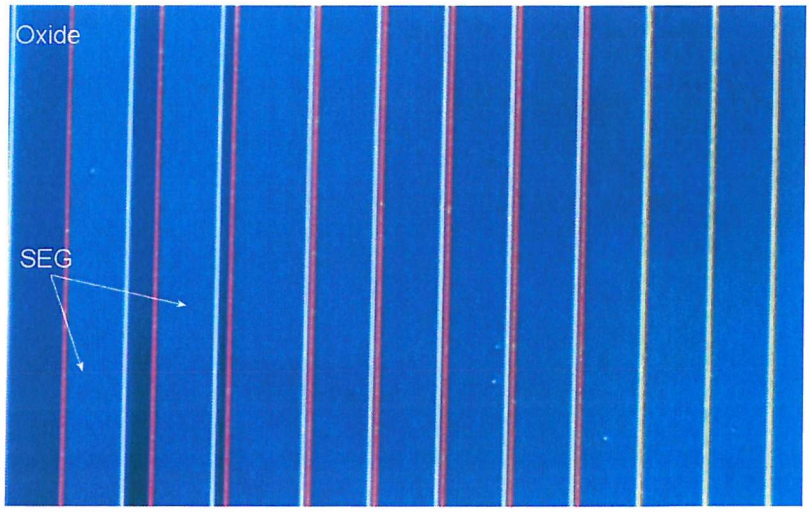


Fig. 5.1 Nomarski image of selective epitaxial growth using silane after 20 minutes at 980°C and 1Torr. Selectivity is excellent but defects in the epitaxial growth can be seen.

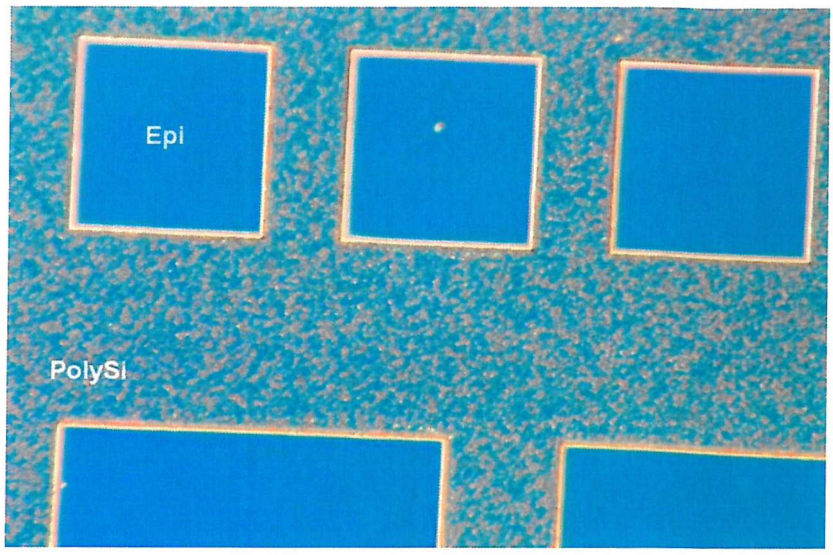


Fig. 5.2 Nomarski image of selective epitaxial growth using silane after 30 minutes at 980°C and 1 Torr. Selectivity is very poor and defects can clearly be seen in the epitaxial growth.

5.2.1 Selectivity

Examination of wafers after 5, 12 and 20-minutes of epitaxial growth confirmed the silane-only process to be completely selective. This is clearly evident, as all oxide covered areas are found to be free from any polysilicon deposition. This result concurs with the findings of Bonar [105], and indicates that the selectivity for the silane-only epitaxial growth process can be maintained for a minimum of 20 minutes. However, for the 30-minute growth, selectivity was found to have been lost, as indicated by the presence of a high density of polysilicon islands on the oxide. Closer examination of the oxide surface by SEM reveals that the features observed by Normarski actually consist of both polysilicon islands and oxide pits. The island density is seen to be very high, as can be observed from figure 5.2. The poor selectivity of the long epitaxial growth is to be expected, as the silane only process does not have an etching component to help maintain selectivity, unlike Si-Cl based epitaxy processes such as DCS/HCl/H_2.

The cause of the oxide pitting is due to the desorption of silicon dioxide. This commonly found to occur at temperatures greater than 950°C. This desorption feature

of silicon oxide is in many ways fortunate as it allows thin "RCA oxides" to be removed by heating prior to epitaxy. The desorption of oxide occurs by the reaction [106],

$$Si(s) + SiO_2(s) \rightarrow 2SiO(g) \qquad (5.1)$$

where Si is silicon, SiO_2 is silicon dioxide and SiO is silicon monoxide. The reaction of silicon with silicon dioxide forms silicon monoxide, a highly volatile gas, which is removed from the epitaxial reactor by convection. When this occurs, it leaves behind pits on the oxide and is exacerbated by long growth times.

The results here show that epitaxial growth using silane is selective up to 20 minutes. However, growth loses selectivity between 20 and 30 minutes which indicates that the incubation period of the growth on oxide, at the conditions used, lie between 20 and 30 minutes.

The existence of this incubation period limits the selective epitaxial growth duration, which in turn restricts the thickness of vertical or lateral growth. For certain applications where long growth times are not required, such as in the fabrication of vertical bipolar transistors [58], this limitation is not generally a problem. However, long epitaxial growths are often required and are particularly needed for the fabrication of lateral bipolar transistors (see section 7.2). The amount of lateral growth that can be achieved is therefore dependent upon the lateral growth rate and the incubation period, for long selective epitaxial lateral growths both incubation times and lateral growth rates need to be maximised.

The length of the incubation period depends on a number of factors including growth temperature, pressure and source gasses [105, 107, 108]. With the silane only epitaxy process, the variables that can be changed to influence the incubation time are pressure, temperature and flow rate. However, the epitaxy process used in this work is already highly optimised and hence, it is not possible (or at least, without considerable development time and resources) to significantly increase incubation time without causing adverse effects such as degradation in epitaxial quality.

5.2.2 Epitaxial Quality

Examination of the 20-minute growth by Nomarski shows the epitaxy to be of good quality. This was inferred from the morphology of the epitaxial surface, which was largely smooth and largely featureless. These are strong indications of good epitaxial quality. However, some defects can be seen on the epitaxy surface in the form of circular pits. Although defects can degrade device performance, the density of these defects is low ($<1\times10^5$ pits/cm^2) and should not prevent the fabrication of working devices. The epitaxial layer produced by the 30-minute growth was also found to be of good quality, despite its poor selectivity. If selectivity was not an issue, this result shows that good quality epitaxy can be provided for at least 30 minutes using the silane only process.

5.2.3 Vertical and Lateral Growth

An important factor determining the suitability of a process for lateral growth is the growth rate. In section 5.2.1, the silane only epitaxy process was found to be limited, in terms of selectivity, to window of less than 30 minutes. The incubation period limits the thickness of the growth that can be carried out, however, in order to determine the maximum growth that can be achieved before it loses selectivity, a figure for growth rate has to be obtained. In this section, vertical and lateral growth rates from seed windows are examined. To measure growth rate, the thickness of the epitaxial growth layer was measured by cross-sectional SEM. The thickness was measured from the base of the seed window to the top of the epitaxial surface. Vertical growth rate, G_V was calculated by the formula,

$$G_V = \frac{T}{t_V} \text{ nm/min} \qquad (5.2)$$

where T is the thickness of the epitaxy(in nm) and t_V is growth time (in minutes).

If lateral epitaxial growth is obtained, its growth rate, G_L is measured using the

formula,

$$G_L = \frac{L}{t_L} \text{ nm/min} \qquad (5.3)$$

Where L is the extent of lateral growth (in nm) and t_L is the lateral growth time (in minutes). Figure 5.4 shows how T and L are obtained. For consistency, all measurements were made at the central region of the wafer. As this growth was carried out at 980°C, clearly in the mass transport limited region [46], uniformity is expected to be within 3% across the wafer.

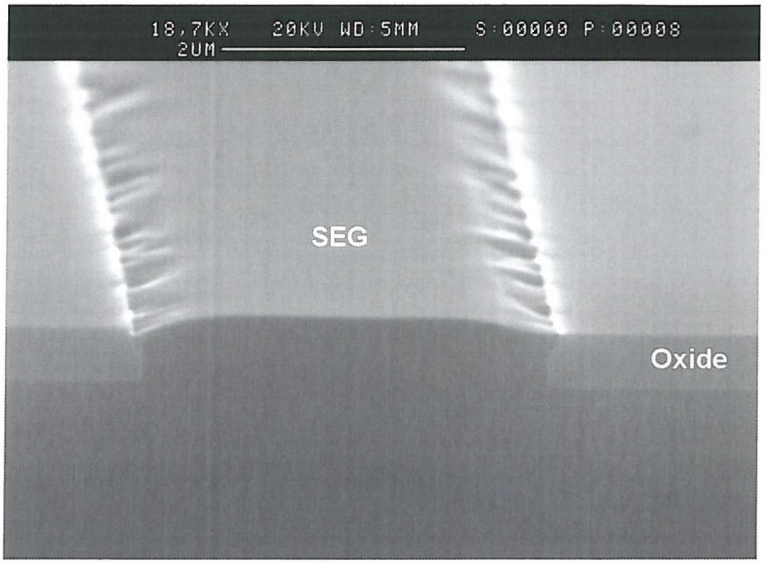


Fig. 5.3 Selective epitaxial growth using silane only after 20 minutes. Epitaxy thickness is 550 nm.

Figure 5.3 shows an oblique SEM image of selective epitaxy after 20 minutes of growth. The thickness of the epitaxial growth was found to be 550 nm. For the 5 and 12-minute growths, the thickness was found to be 150 nm and 350 nm, respectively. This gives the epitaxy process an average growth rate of 28 nm/min. For the 5 and 12-minute growths, no lateral growth was achieved as the thickness of the epitaxial layer was thinner than the 460 nm oxide layer. Lateral overgrowth was also not obtained with the 20-minute growth. Although the thickness of epitaxial growth was greater than the

oxide layer (i.e. 550 nm), the formation of the {3 1 1} plane has prevented the lateral growth. Epitaxial growth in both <1 1 0> and <1 0 0> oriented seed windows were found to be very similar in terms of thickness.

In order to achieve lateral growth, the fourth growth experiment was extended to a total time of 30 minutes. In addition to this, the thickness of the oxide layer was reduced from 460 nm to 200 nm to allow epitaxial growth to begin earlier in the growth process. The result of this growth is shown in figure 5.4 and figure 5.5. After 30 minutes, the thickness of the epitaxial growth, in a <1 1 0> oriented seed window, is 860 nm. The lateral growth, *l*, measured from the side of the oxide window is 500 +/- 50 nm, which gives a lateral growth rate of 11 nm/min. This calculation assumes that lateral growth only commences when epitaxy reaches the top of the seed window. This gives a vertical to lateral growth ratio of 2.5:1. The lateral growth rate is initially determined by the growth rate of the {3 1 1} plane, and then by the growth rate of the {1 1 1} plane. Different silicon planes will have different growth rates, dependent upon the atomic density of the plane, the nature of the surface bond reconstruction and the process conditions. The {1 1 1} plane has a higher atomic density than the {3 1 1} and {1 0 0} planes, and a consequence has the slowest growth rate of the three planes. As a result of the formation of slower growing facets, such as the {3 1 1} and {1 1 1}, the rate of lateral growth from a horizontal seed can be significantly reduced.

In theory, growth in <1 0 0> oriented seed windows should not form facets, and it is therefore interesting to determine the lateral growth rate of epitaxy grown in these seed windows. Figure 5.6 shows such a growth. The thickness of the epitaxial growth was found to be 860 nm, the same as the thickness in <1 1 0> oriented seed windows. Although no distinct facets are formed (other than the planar {1 0 0}), the amount of lateral growth was found to be similar to that from the <1 1 0> oriented seed windows at 530 +/- 50 nm. This result shows that the orientation of the seed window has only a small effect on the lateral growth rate of the epitaxy.

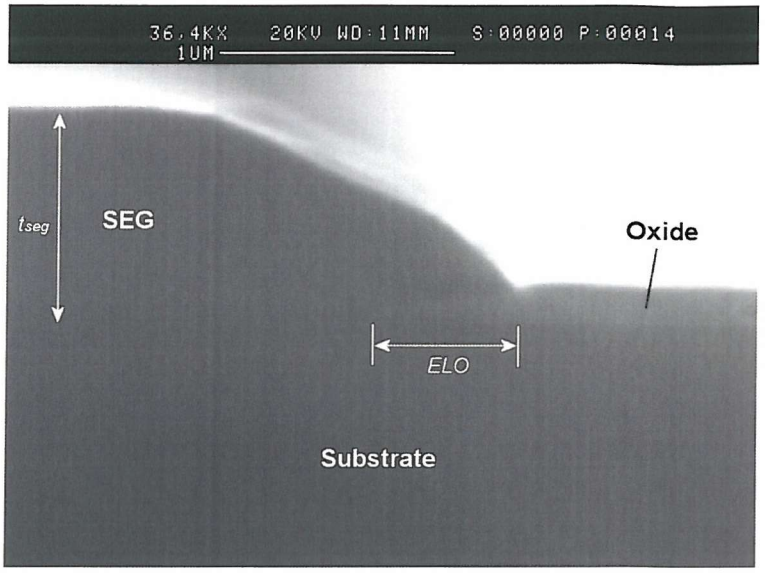


Fig. 5.4 SEM image showing 500 nm of epitaxial lateral overgrowth (*ELO*), and 860 nm of vertical growth (t_{seg}). The image also shows the severe oxide undercutting caused by the lateral epitaxial growth over the oxide.

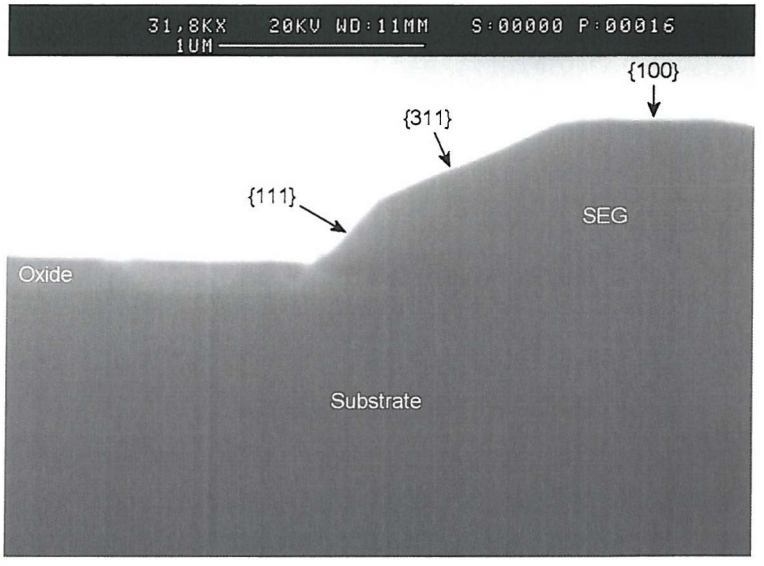


Fig. 5.5 Faceting of growth using silane only after 30 minutes. The fastest growing plane is the {1 0 0} followed by the {3 1 1} and {1 1 1}, the slowest growing plane.

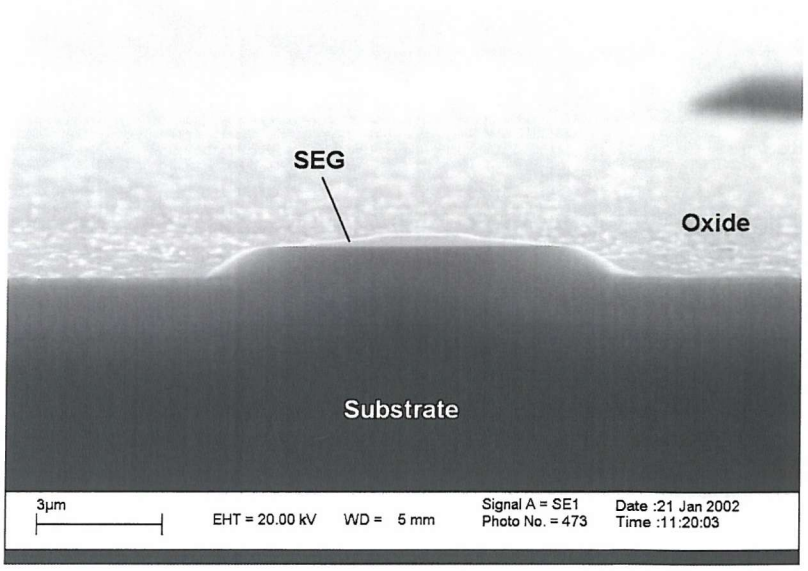


Fig. 5.6 Epitaxial growth after 30 minutes in a <1 0 0> oriented seed window. No distinct faceting other than the planar {1 0 0} is observed.

As the gas used in this process consists only of silane, control over the development of facets is limited to changes in other variables such as temperature and pressure. However, changes in temperature and pressure can lead to significant changes in epitaxial quality, selectivity and growth rate so these possible routes were not explored in this work. An alternative method with which to control the development of facets is by changing the silicon / chlorine gas ratio in chlorosilane systems [64]. This possibility and a number of other factors led to an exploration of chlorinated source gasses as this would not only allow some control over faceting but would also allow additional control over selectivity. Such a process is presented in the following chapter.

In addition to the problem of faceting, figure 5.4 also shows that the lateral epitaxial overgrowth process causes the loss of oxide in areas underneath the lateral growth, as is evidenced by the tapered oxide layer seen close to the seed window. The cause of this is believed to be similar to the problem of oxide pitting (described in section 5.2.1) due to the reaction between silicon and silicon dioxide at high temperatures (equation 5.1). As with oxide pitting, this problem can be minimised by a reduction in growth temperature. Similar 'etching' was also found in the 30-minute epitaxial growth sample. Etching is only observed in the Si/SiO_2 sidewall area as shown in figure 5.7. In this area, at least 80 nm of the oxide is found to be 'etched' on both sides of the

sidewall. This etching creates several problems, one of which is the enlarging of the silicon seed window. Although it is not a significant problem in this experiment, in fabrication processes that require growth in small windows or have tight alignment tolerances, this problem may not be tolerable. Oxide loss is likely to be significant for confined lateral epitaxial growths in cavities, where the walls of the cavities tend to be thin (~300nm). As this problem is directly related to temperature, carrying out epitaxial growth at lower temperatures would be highly beneficial. However, lowering the growth temperature of the silane-only epitaxy process degrades the quality of the epitaxial layers and makes it difficult to achieve selective growth [46].

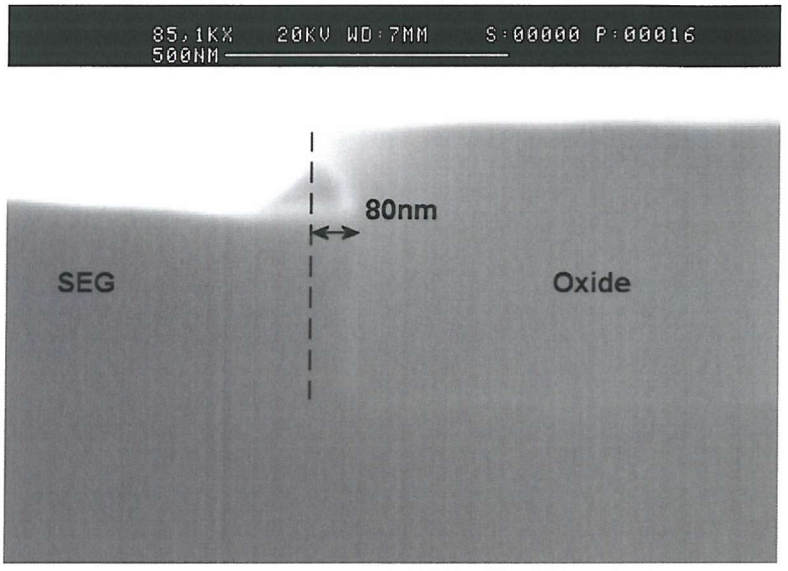


Fig. 5.7 80 nm of oxide sidewall is 'etched' during selective epitaxial growth. The dashed lines show the original oxide sidewall area.

5.2.4 Confined Selective Epitaxial Growth

So far, epitaxial growth using silane has been carried out without "confinement" and in ordinary seed windows. In order to determine the suitability of the epitaxy process for confined selective epitaxial growth, growth in one of the test cavity structures was attempted. The initial attempt at confined selective epitaxial growth was carried out using test cavities (see section 4.2) and although these do not confine vertical growth,

these "pseudo-confined" growths allowed the post-processing selectivity and epitaxial quality to be assessed. The methods used to define the cavities have to provide epi-ready seed layers and oxides that do not provide silicon nucleation sites.

The confined selective epitaxial growth was carried out using the same growth conditions as the unconfined selective epitaxial growths (i.e. 0.1 Torr, 980°C, 30 minutes using SiH_4). As with the unconfined growths the selectivity achieved from the epitaxial growth in test cavitites, as shown in figure 5.8, was found to be poor as indicated by the high density of polysilicon islands on the oxide surface. In addition to the poor selectivity, the oxide surface was also found to be pitted. The Nomarski image also shows the morphology of the epitaxial growth to be irregular and undulated, a sign of poor epitaxial quality.

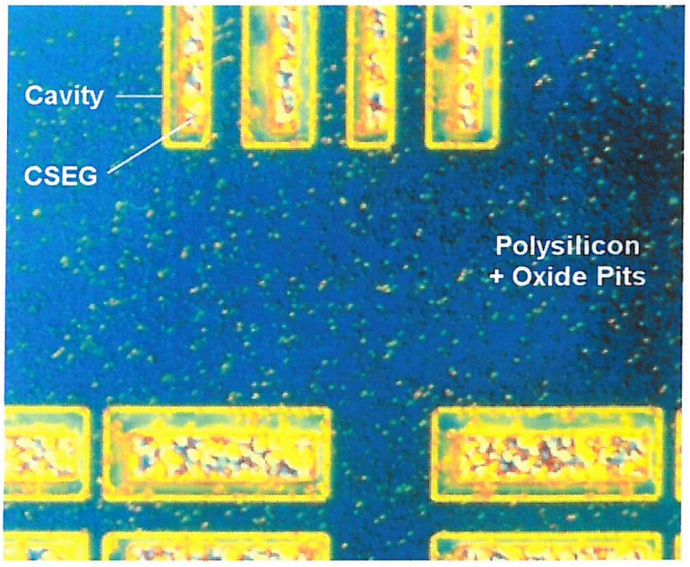
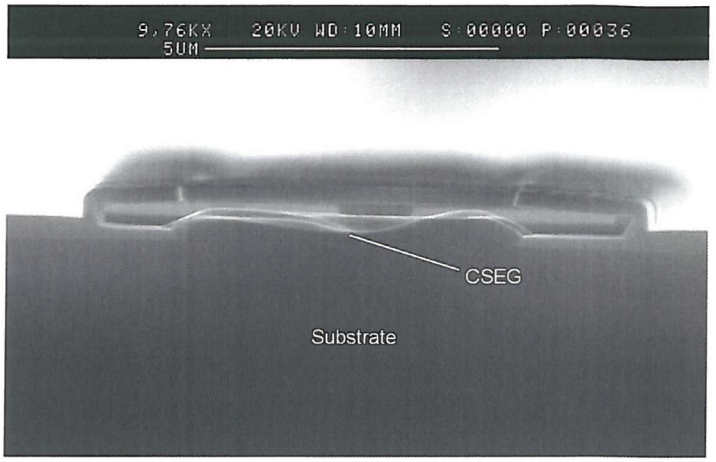


Fig. 5.8 Nomarski image after silane only growth on a wafer with test cavities. Selectivity is poor as indicated by the high density of polysilicon islands on the oxide.

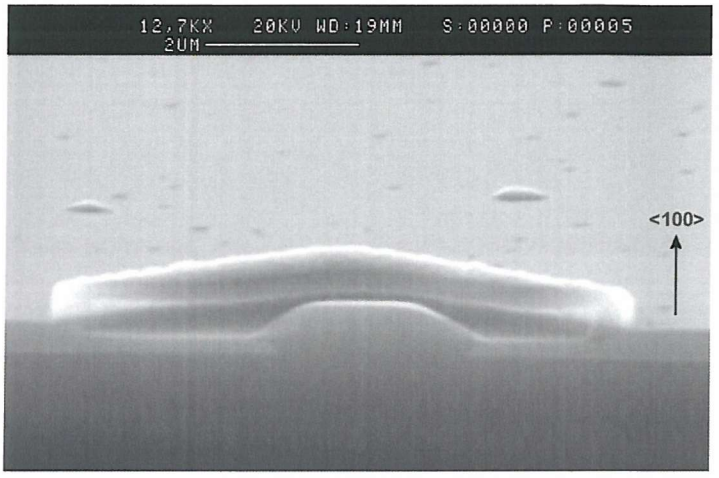
Figure 5.9 shows SEM images of confined epitaxial growth in test cavities oriented in the <1 1 0> and <1 0 0> directions. The epitaxial growth in the cavity oriented along the <1 1 0> direction (figure 5.9 (a)) can be seen to be non-uniform and irregular, features consistent with ideas inferred from the Normarski image in figure 5.8. Similar observations were also made of confined growth in cavities oriented along the <1 0 0>

direction, as shown in figure 5.9(b), although the cross-section image shown look to have more uniform growth.

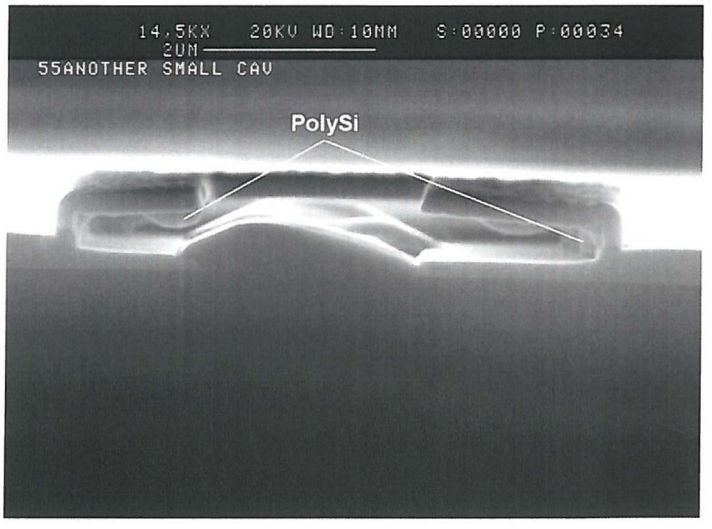
From the SEM images, the average thickness of the epitaxial growth of cavities oriented along the <1 1 0> direction was found to be ~340 nm, which corresponds to a growth rate of 11.3 nm/min. However, for cavities oriented along the <1 0 0> direction, the thickness of the epitaxy was found to be ~660 nm, corresponding to a growth rate of 22 nm/min. In comparison, *unconfined* selective epitaxial growth with the same growth conditions, was found to be 28 nm/min for both <1 1 0> and <1 0 0> oriented seed windows (section 5.2.3). This means that the confined growth has only a third of the growth rate of the unconfined growth. Due to the significantly reduced growth rate, no significant lateral overgrowth is observed in either cavity orientation. The reason for the difference in growth rates for confined and unconfined growth is difficult to determine given the small number of experiments allowed. However, the reduction in growth rate and irregularity of the epitaxial growth between cavities seems to indicate a local loading effect, where the silicon seed is starved of silicon. However, such growth non-uniformities between seed windows were not observed with unconfined growth, suggesting that the problem is specific only to confined growth. The confined growth differs from the unconfined growth in two important ways. The first, is the effect being tested, the confined growth is carried out in cavities. The second is the global silicon to oxide ratio. In unconfined growth, the silicon to oxide ratio is estimated to be 17%, however, in confined growth this is much higher at ~46%, almost three times greater. The dramatic increase in the silicon to oxide ratio is a result of the way in which the wafer used for confined growth was prepared. The large difference in silicon to oxide ratio seems to be the most likely reason for the reduction in growth as others have also reported similar observations [109]. With a large area of silicon exposed, the silicon acts as a sink for incoming silicon atoms diffusing through the boundary layer. When the silicon area is reduced, the amount of silicon adatoms that are 'collected' in seed windows increases, resulting in a higher growth rate.



(a)



(b)



(c)

Fig. 5.9 Confined epitaxy growth in test cavities made from LTO. (a) is a cavity oriented along the <110> direction. (b) is a cavity oriented along the <100> direction. (c) polysilicon deposition on the underside of the ceiling and ends of the cavity.

Besides epitaxial growth, polysilicon growth can also be observed inside the cavity. Looking at figure 5.9(c), polysilicon growth seems to be primarily concentrated at the ends of the cavity. Inspection of other cavities on the same wafer also show there to be polysilicon growth on the underside of the cavity ceiling. Interestingly, less polysilicon was found to nucleate on the cavity floor. There are two possible reasons for polysilicon growth – the polysilicon inside of the cavity could simply be non-selective growth similar to that observed on the oxide surface, or growth on polysilicon residues on the inner walls of the cavity, a result of incomplete etching during the fabrication process. The size and density distribution of the polysilicon areas within the cavitiy indicate that the most likely cause is incomplete polysilicon etching. The higher concentration of polysilicon islands on the underside of the ceiling could be a result of the rougher surface of the LTO layer (compared to the cavity floor which is thermally oxidised), which can act as nucleation sites for island growth. The rougher surface is probably due to the deposition of the oxide layer on polysilicon.

5.2.5 Selective Silicon Germanium Growth

At the Southampton University Microelectronics Centre (SUMC), heteroepitaxial growth of silicon germanium has been carried out at temperatures between 700°C and 800°C, at a growth pressure of 0.5 Torr. The gas flow rates used for silicon germanium growth are 120 sccm hydrogen and 30 sccm silane, with germane flows varying from 0.5 to 3.0 sccm. Germanium fractions of between 1.8% to 16% have been achieved, dependent on the germane flow rate. The SiGe process has been successfully used in HBT device fabrication with strained SiGe base widths of <100 nm, including intrinsic SiGe spacer layers, with sharp doping profiles and transitions. With the addition of diborane, SiGe layers can be doped p-type with doping concentrations of between 1.5×10^{18} cm^{-3} to 2×10^{19} cm^{-3}. The reader is asked to refer to Bonar [46] for more detailed information on the SiGe process.

Although device quality SiGe layers can be grown at SUMC, so far, the silicon germanium growth based on the silane process produces non-selective layers. The lack of selectivity is a direct result of the reduction in growth temperature, which is needed

in order to form stable strained silicon germanium layers, and at the same time ensure sharp doping profiles and minimise the out diffusion of dopants – all of which are necessary for the fabrication of heterojunction bipolar transistors.

Experiments exploring SiGe selectivity running concurrently to our own have shown that reducing temperature from 980°C does not allow selective growth while increasing the temperature causes germanium segregation [110]. This lack of a selective silicon germanium process renders the silane/germane only selective approaches unsuitable for lateral heterojunction bipolar transistor fabrication.

5.3 Conclusion

The SUMC silane-only epitaxy processes are proven epitaxial techniques which have, in the past, been successfully used to fabricate working devices. These includes vertical silicon homojunction bipolar transistors [111, 112] using a fully selective epitaxy process, and vertical silicon germanium heterojunction bipolar transistors [58, 103], using a combination of selective silicon and *non-selective* silicon germanium epitaxial growth. Although the silane only processes have been used to fabricate these devices, the requirements needed for the fabrication of lateral heterojunction bipolar devices are more stringent, as highlighted in section 2.8.

The results of the epitaxial growths show that the silane only process is able to produce high quality selective epitaxial layers, of up to 560 nm (28 nm/min). However, growth was only found to be selective within an incubation period of up to 20 - 30 minutes, beyond which the density of polysilicon islands increases dramatically. Epitaxial lateral growth up to 500 nm have also been achieved, however, lateral growth rates have been found to be limited by the formation of atomically compact facets such as the {3 1 1} and {1 1 1}. For lateral growth, the {1 0 0} is the preferred growing facet as it maximises the lateral growth rate. Further studies are required to determine if confinement or global loading causes the reduction in growth rate.

In this work, the silane only process was carried out at a high temperature (980°C), and

produced epitaxial layers of high quality. However, the high temperature encourages oxide pitting and causes severe oxide 'etching' at silicon/oxide sidewall areas. The high temperature process also makes it very difficult to grow strained silicon germanium layers without resulting in relaxed layers. So far, strained silicon germanium layers have only been successfully grown at lower temperatures *non-selectively*. This is a big problem as selective silicon germanium growth is essential for the fabrication of lateral heterojunction bipolar transistors.

Due to the limitations of the silane-only process (i.e. short incubation period, high growth temperature, oxide degradation and non-selective silicon germanium growth), the process was deemed unsuitable for the lateral heterojunction bipolar transistor process. As a result of this, a new process based on silane and dichlorosilane has had to be developed. The aim behind this process is to use the chlorine-based gas dichlorosilane as a means of controlling selectivity. With better control over selectivity, the silane + dichlorosilane process should allow growth to be carried out at a lower temperature while still retaining good selectivity for a longer period of time. The lower temperature is especially advantageous as it would allow strained SiGe growth. This novel DCS/SiH_4/H_2 selective epitaxy process is presented in the following section.

Chapter 6

Selective Epitaxy Growth using $DCS/SiH_4/H_2$

6.1 Introduction

This section looks at the selective epitaxial growth of silicon by dichlorosilane and silane in hydrogen (DCS / SiH_4). The addition of dichlorosilane into the silane based process is intended to provide a means of independently controlling the selectivity of the epitaxy growth by controlling the Si/Cl ratio. By adding this additional control it was hoped that the temperature range for suitable for selective growth could be reduced. To the best knowledge of the author, the use of DCS with silane for selective epitaxial growth has not been previously reported.

6.2 Epitaxial Growth using DCS / SiH4 / H_2

The section of work began with a series of exploratory growth experiments designed to determine the feasibility of selective epitaxial growth using dichlorosilane and silane in hydrogen. These experiments were intended primarily to explore the range of the available parameter space suitable for selective growth. The conditions used in the first

experiments were based on the silane-only processes developed in chapter 5, and published work on silicon epitaxy using chlorinated gas sources using similar conditions to those within the operational limits of the SUMC epitaxy reactor [46]. All growths were carried out at 850°C, significantly lower than the temperature used in the silane growth (980°C). This temperature reduction would reduce the process' thermal budget and increase the feasibility of satisfactory SiGe growth. Regolini *et al.* [55] explored selective growth using silane and HCl at base pressures of around 1 Torr and describe how the ratio between silicon and chlorine is an important factor which determines the selectivity of a growth [55]. Finding a balance between the two, by changing the silane or HCl flow rates, is required to obtain good selectivity. In this work DCS replaces the HCl, not necessarily to "reverse" the overall reaction, but to decrease the net adsorption of silicon adatoms onto the oxide.

In the first experiments a short series of growths were carried out for 30 minutes. Growths with a 1:2 DCS/silane ratio, with DCS only and with a 1:1 DCS/silane ratio were carried out as summarised in Table 6.1.

Process #	Growth Conditions
1	850°C, 1 Torr, 10 : 20 : 100 sccm DCS / SiH_4 / H_2
2	850°C, 2 Torr, 10 sccm DCS
3	850°C, 1 Torr, 10 : 10 : 100 sccm DCS / SiH_4 / H_2

Table 6.1 Epitaxial growth conditions using DCS / SiH_4.

6.2.1 Process #1: DCS / SiH_4 / H_2 at 10 : 20 : 100 sccm

The first attempt at selective epitaxial growth was carried out at 850°C, 1 Torr with a DCS : SiH_4 : H_2 ratio of 10 : 20 : 100 sccm. The results of this growth are shown in figure 6.1 and figure 6.2. The figures show the growth to be completely non-selective as indicated by the blanket layer of silicon on the entire wafer surface. Closer examination shows that epitaxial growth is obtained at areas where silicon is exposed

while polysilicon growth is observed on areas where there is oxide. These two areas are differentiated based upon the morphology of the surfaces, where polysilicon tend to have a grainier surface compared to that of epitaxial silicon, which is smoother when observed by Nomarski.

Epitaxial and polysilicon growths can also be distinguished by cross-sectional SEM where the formation of <3 1 1> and <1 1 1> facets on features oriented along the <1 1 0> direction indicate epitaxial growth. Cross-section examination of the growth shows that the thickness of the epitaxial growth is 1.5 μm, while the thickness of the polysilicon growth is 750 nm. This corresponds to a growth rate of 50 nm/min and 25 nm/min, respectively. The quality of the epitaxy, shown from figure 6.2, was found to be of poor quality. This was inferred from the morphology of the epitaxy surface, which was found to have square depressions of various sizes.

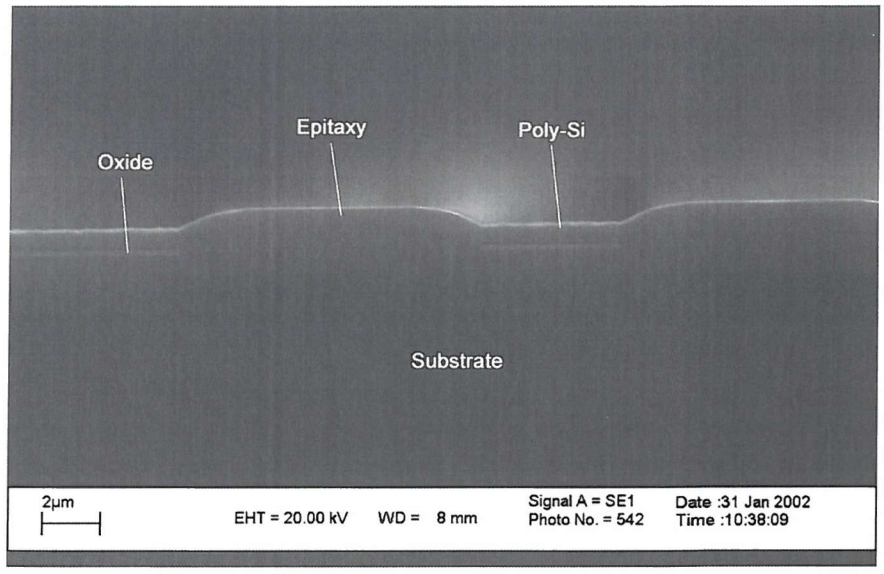


Fig. 6.1 Cross-section SEM image showing non-selective growth. Epitaxial growth is obtained on areas that are exposed to silicon while polysilicon is observed on areas that are covered by oxide.

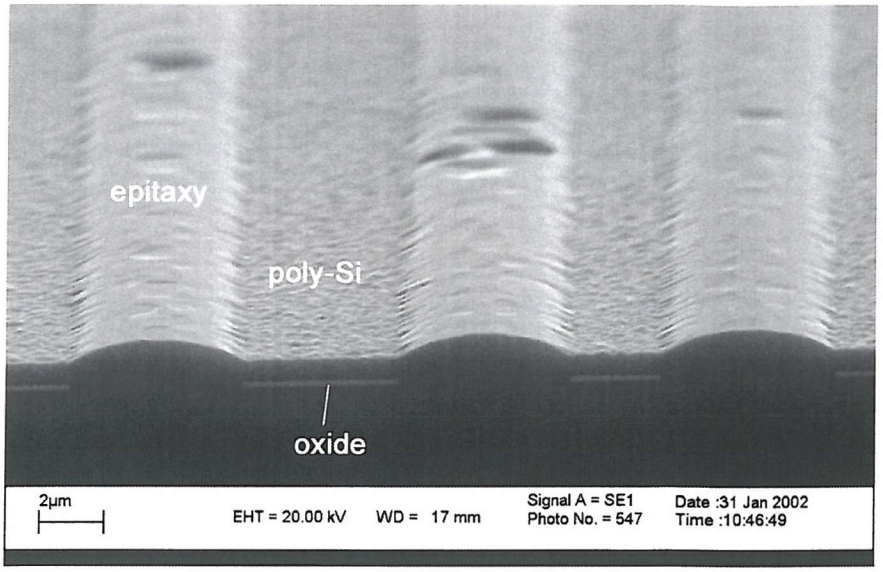


Fig. 6.2 Image of the wafer surface showing epitaxy and polysilicon growth over silicon and oxide, respectively.

6.2.2 Process #2: DCS / H_2 at 10 : 100 sccm

From the previous growth, it was clear that the flow rates used tipped growth too much towards deposition. In order to explore the opposite end of the scale, A second growth was carried out at 850°C at 2 Torr and with a DCS : H_2 ratio of 10 : 100 sccm (i.e. with no silane gas). Figure 6.3 is a cross sectional SEM image of a seed window after a 30 minute run. The image shows the process causes the etching of silicon. The depth of the etch is 420 nm, which corresponds to an etch rate of 14 nm/min. Figure 6.3 also shows the process etches along the crystallographic plane of silicon as evident by the distinct {1 0 0} and {3 1 1} planes, indicating the etch is anisotropic. Closer examination of the etched {1 0 0} surface shows the silicon to be roughened by the process. Measurements were also made to determine the selectivity of the etch to oxide by comparing the thickness of the oxide before and after the etch. The difference in thickness of the oxide before and after growth was found to be negligible indicating that the process is very selective.

The results show that the recipe and conditions that were used in this process causes etching instead of growth, and indicates one extreme of the DCS / SiH_4 regime.

Although, this experiment was manifestly unsuccessful in growing epitaxial layers, this process is shown to be a potentially useful single crystal silicon etching technique. This process could be useful in the cavity fabrication process where it can be used to etch back polysilicon or silicon during the sacrificial etch stage of the cavity process. The biggest advantage of this would be that the etch-back and epitaxial growth steps could be carried out consecutively in the clean environment of the epitaxy reactor. This would be superior to the more traditional process which involves removing the sacrificial layer by dry etching followed by a clean in RCA before the wafer is loaded into the epitaxy system. With the *in situ* etch and growth method, the need for an intermediate RCA clean step would be removed and the possibility of wafer contamination would be further minimised. The process' high silicon to oxide etch ratio is also helpful in that it ensures little oxide is removed during the etch-back. However, the anisotropic nature of the etch means careful consideration of the cavity design, primarily the orientation of the structures with respect to the crystallographic plane, has to be made.

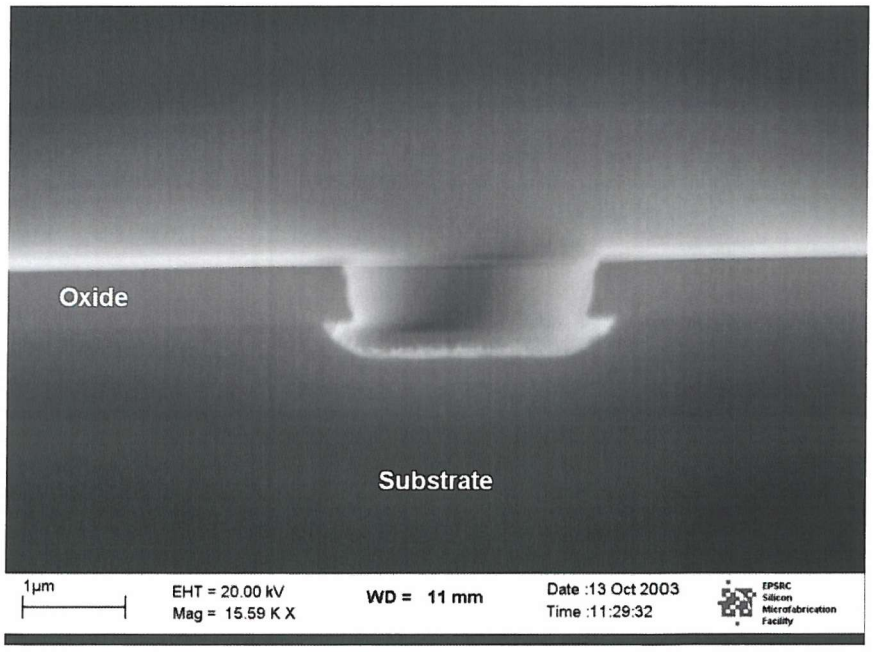


Fig. 6.3 SEM image of a seed window after a DCS / H_2 growth with 10 : 100 sccm gas ratio. The process results in anisotropic etching of the silicon substrate.

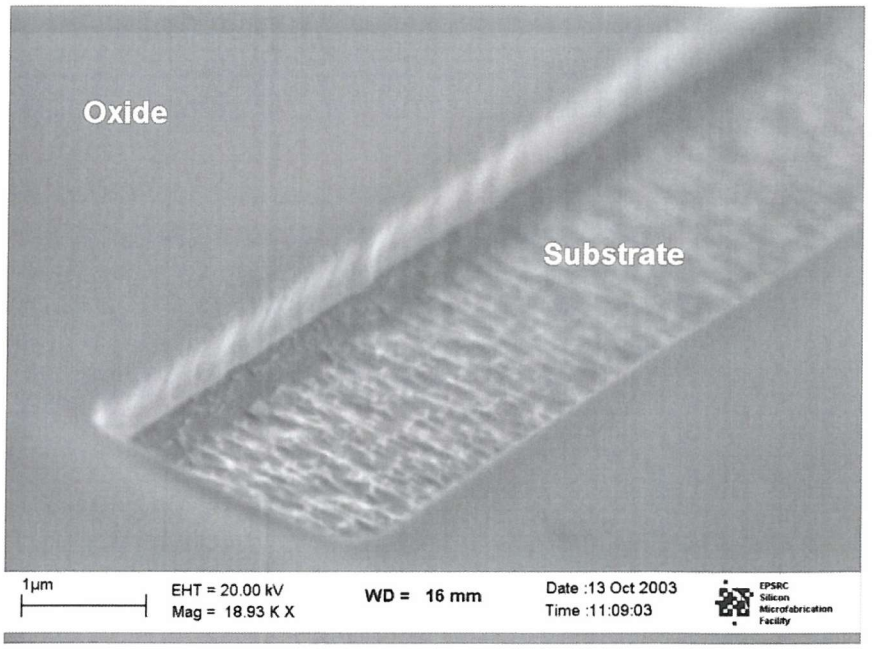


Fig. 6.4 SEM image showing a rough silicon surface after a DCS/H_2 "negative growth".

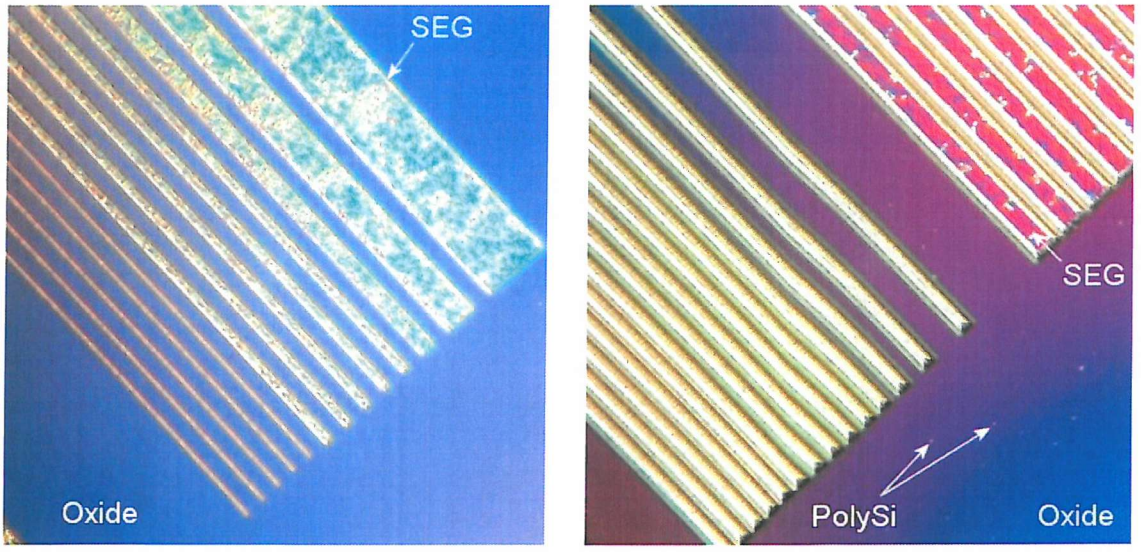
This experiment indicates the existence of an important and previously unreported, etching regime, with potential applications in device design and surface preparation, further studies of the regime, to determine the range and scope of the technique, would be valuable. Within the context of this work, however, the most important aspect of this etching regime is its applicability to selective growth. Combining both DCS and silane under the right conditions should provide etching and growth reactants that can be independently controlled. In this way DCS replaces HCl in the more traditional silane/HCl selective systems.

6.2.3 Process #3: DCS / SiH_4 / H_2 at 10 : 10 : 100 sccm

The third epitaxial growth was carried out at 850°C at 1 Torr with a DCS : SiH_4 : H_2 gas ratio of 10 : 10 : 100 sccm, the mid-point between the flow rates used in the first (blanket deposition) and second (etching) processes. Figure 6.1(a) below shows the result of the growth as viewed by Nomarksi. After 30 minutes of growth, the wafer surface was found to be free from any polysilicon island deposition, indicating that the

growth was completely selective. Although, selectivity was found to be excellent, epitaxy quality was found to be poor as indicated by the rough 'orange peel' like surface of the epitaxy. The thickness of the epitaxial layer was found to be 840 nm corresponding to a growth rate of 28 nm/min.

There are several factors that may lead to poor epitaxial quality, these include insufficient or poor pre-epitaxy cleaning, contamination in the growth reactor, gas-phase reactions or insufficient oxide removal [42, 46, 72]. In addition, surface roughness, adatom mobilities and adatom density can also strongly influence the quality of epitaxy, in extreme cases polysilicon or amorphous Si can be produced. In general epitaxy becomes more challenging with reducing growth temperature as this reduces adatom mobilities. Maintaining good epitaxial quality while decreasing temperature requires improved preparation and conditioning of the growth reactor. At this stage there was insufficient detail to establish any fundamental link between the selective process and degraded epitaxial quality. Although the need for improved preparation and conditioning as a result of temperature reduction is highlighted.



(a) (b)

Fig. 6.5 Nomarski images of DCS / SiH_4 growth after (a) 30 minute growth, (b) 90 minute growth. Growth is selective after 30 minutes of growth. After 90 minutes, selectivity is lost. The addition of DCS into the hydrogen prebake greatly improves epitaxial quality.

6.2.4 Extended DCS / SiH_4 / H_2 Growth

The 30 minute DCS / SiH_4 / H_2 growth with gas ratio of 10 : 10 : 100 sccm, was found to give epitaxial layers with good selectivity. To test the extent of the selectivity, the DCS / SiH_4 / H_2 growth (#3) was repeated with the same growth conditions but for 90 minutes. The result of the growth, shown in figure 6.1(b), shows the surface of the epitaxy to be bumpy and populated with square pits. These are clear signs of defects and are an indication that the epitaxy is of poor quality. The thickness of the epitaxy was found to be 2.6 μm, corresponding to a growth rate of 29 nm/min. An epitaxial lateral overgrowth of 0.5 μm was also observed in this growth, and as with the silane-only growth, the minimal lateral growth achieved is due to formation of slow growing {3 1 1} and {1 1 1} facets. Examination by Nomarksi shows there to be some polysilicon island deposition on the oxide surface. An estimation of the polysilicon density taken at the centre of the wafer is 1×10^6 islands/m^2.

In terms of selectivity, evidence of polysilicon islands on the oxide surface shows selectivity is certainly lost after 90 minutes of growth. As no polysilicon islands were detected after a 30 minute growth, it can be concluded that the DCS / SiH_4 process has an incubation period of between 30 to 90 minutes long. With the number of growths carried out, the exact incubation time cannot be determined. In figure 6.7 the small data set is fitted based on the assumption that polysilicon island density increases linearly after the incubation time has elapsed. In this way figure 6.7 assumes the shortest possible incubation time (30 minutes) and represents, therefore, the lower limit. Here it is perhaps useful to consider the definition of selectivity, it is acceptable to equate selectivity loss to the incubation time, however, this may be unnecessarily strict. In fact, the existence of one polysilicon island per 100×100 μm^2 area (i.e. 1×10^4 islands/cm^2) would be tolerable in a device process, most devices would have no islands incorporated and the loss of selectivity would only slightly degrade yield.

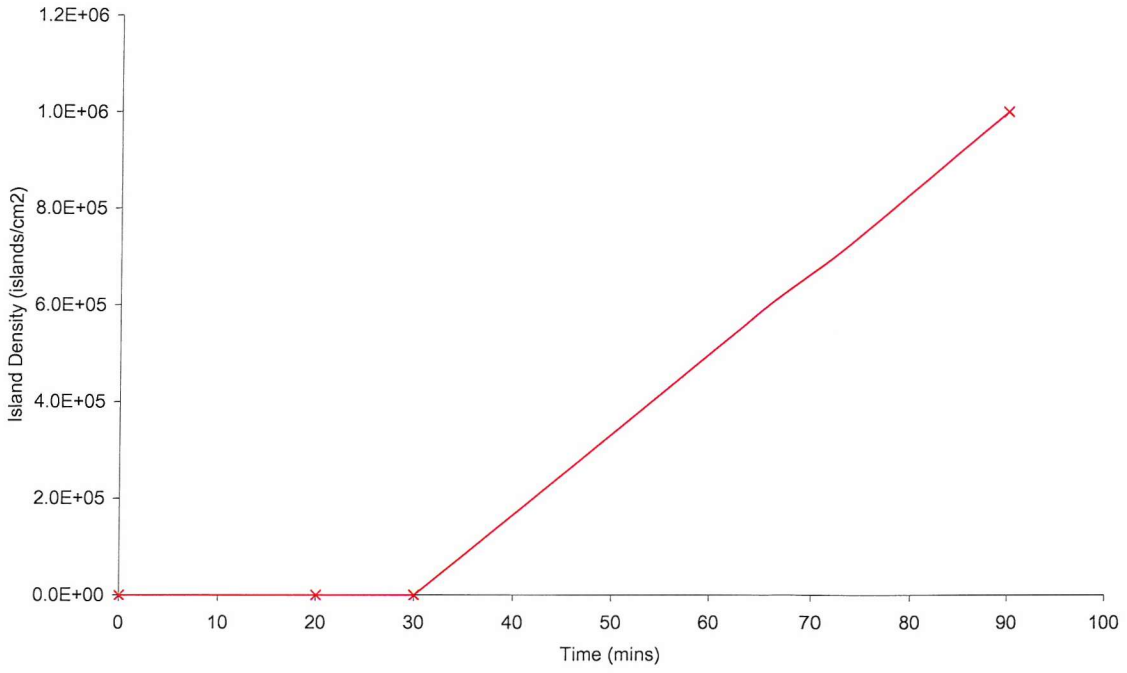


Fig. 6.6 Polysilicon island density with respect to growth time carried out at 850°C. The small data set is fitted based on the assumption that polysilicon island density increases linearly after the incubation time has elapsed. The fit represents, the lower limit of incubation time.

6.3 DCS / H_2 Prebake

The previous sections have shown the feasibility of using the DCS / SiH_4 / H_2 process for epitaxial growth. Although growth was selective, epitaxy quality was found to be generally poor. Compared to selective epitaxial growth using SiH_4, the surface of the epitaxy was found to be uneven with visible surface defects, indicative of defected epitaxy. As the DCS / SiH_4 processes are carried out at a much lower temperature (850°C) the process is less tolerant of surface defects, such as oxide islands/particulates [57]. In an attempt to improve epitaxial quality DCS was added to the prebake stage to help to prepare the silicon surface prior to growth. This was done by adding a small amount of DCS in the H_2 prebake cycle to aid surface cleanup [68].

The hydrogen prebake is normally carried out at 980°C for 5 mins at 100 sccm prior to epitaxial growth, and is designed to etch thin oxide layers on the silicon wafer. In the

new DCS / H_2 prebake process, 1 sccm of DCS is added to the hydrogen for the same time and temperature.

6.3.1 Results

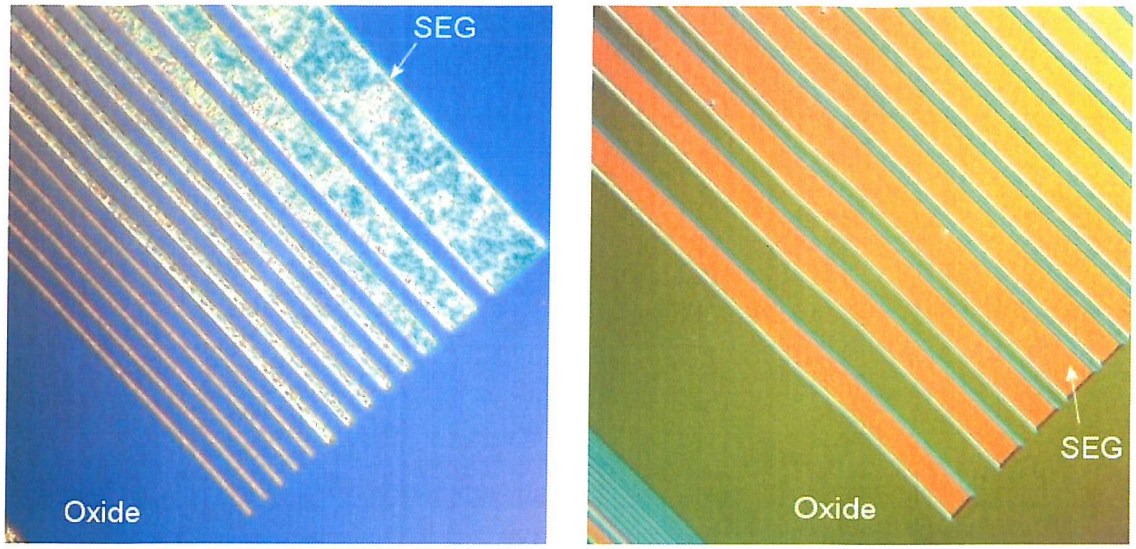
Figure 6.7 compares Normarski images of 30 minute DCS / SiH_4 / H_2 growths with and without DCS prebakes. After the standard prebake stage, the epitaxy surface is seen to be rough and grainy, as shown in figure 6.7(a). However, application of the DCS / H_2 prebake is seen to produce a dramatic improvement in epitaxial quality. This is indicated by the smoother epitaxial surface and the lack of obvious surface defects figure 6.7(b). Similar results with a similar process, have been reported by Chung *et al.* [68]. This improvement in epitaxy quality is believed to be due to either the removal of oxide residues at the seed interface which may have been insufficiently removed in the pre-epitaxial wafer preparation process, or due to the burial of the oxide residues by the DCS growth during the prebake. Of the two, the removal of oxide is the more likely cause as dichlorosilane-based epitaxy processes are known to severely degrade oxide [113, 114]. The has been suggested to occur by the reactions [114],

$$Si(s) + SiO_2(g) \rightarrow 2SiO(g) \qquad (6.1)$$

$$SiCl_2H_2(g) + SiO_2(g) \rightarrow 2SiO(g) + 2HCl(g) \qquad (6.2)$$

In addition to the removal of oxide, the use of DCS in the H_2 prebake may also cause etching of surface defects, leaving clean and damage-free surfaces suitable for epitaxial growth [74]. This hypothesis is supported by the DCS/H_2 etching results presented earlier in section 6.2.2.

As the addition of DCS in the hydrogen prebake was found to consistently provide good quality epitaxial layers, this pre-epitaxy growth process was included in all other DCS/SiH_4/H_2 growths.



(a) (b)

Fig. 6.7 Effect of adding DCS into the hydrogen prebake stage of the epitaxy process. (a) Without DCS, (b) with DCS. The addition of DCS results in a dramatic improvement in epitaxial quality.

6.4 Growth at Different Temperatures

The first few growth experiments, indicated that epitaxial growth using DCS / SiH_4 at 850°C and 1 Torr, combined with the use of DCS in the H_2 prebake offers selective epitaxial growth with good epitaxy quality and excellent selectivity. Growth rate is found to be reasonable at 38 nm/min, and allows fine control of epitaxy thickness features during growth. The following set of experiments were designed to characterise the DCS / SiH_4 system for a range of temperatures. Epitaxial quality, selectivity and growth rate were assessed.

Selective epitaxial growth was carried out at temperatures ranging from 750°C up to 930°C. All growths were carried out at 1 Torr with a DCS : SiH_4 : H_2 ratio at 10 : 10 : 100 sccm for 30 minutes.

6.4.1 Temperature Dependency on Growth

Figure 6.8 shows an Arrhenius plot for the DCS/SiH_4/H_2 process. As a comparison, the Arrhenius plot of the SiH_4 only epitaxy process is also shown in the graph [46]. The Arrhenius plot shows the existance of two linear regions, the flat mass transport limited region and the sloped surface reaction limited region. For the DCS/SiH_4/H_2 process, the growth rate is at a maximum above 900°C at 55 nm/min, and it is at a minimum at 800°C at 9 nm/min. The figure also shows that the DCS/SiH_4/H_2 process moves from being surface-reaction limited to mass-transport limited at around 870°C. From the slope of the low temperature part of the curve, the activation energy of the process was found to be 2.4 eV or 55.3 kcal/mol. In comparison, for the silane-only process, the maximum growth rate occurs above 800°C at 15 nm/min, and drops to 7 nm/min at 700°C. The activation energy of the silane only process is 1.9 eV. This value is a little less than the DCS/SiH_4/H_2 activation energy (E_a) of 2.4 eV. As a further comparison, other dichlorosilane based epitaxy processes carried out at this pressure region (1 to 10 Torr) also have similar activation energies. Regolini *et al.* has reported an E_a of 2.6eV for a DCS / H2 based process [55]. The similarity of the activation energies of the DCS based selective epitaxy processes indicate that the growth processes share the same rate determining reaction [42] and the DCS/Silane process has more in common with deposition using DCS only rather than silane only.

Figure 6.8 highlights the differences between the SUMC silane-only and DCS/SiH_4/H_2 processes. The DCS/SiH_4/H_2 process is able to achieve much higher growth rates at lower temperatures than the silane-only process. Selectivity can also be maintained at a much lower temperature (section 6.4.3). It is therefore a lower thermal budget process. In addition, growth using the silane-only process becomes non-selective below 930°C. Another characteristic of the DCS/SiH_4/H_2 process is that the transition from surface-reaction-limited to mass-transport limited growth occurs at a higher temperature (890°C) as compared to silane-only (790°C). This characteristic is typical of chlorinated sources where the reaction occurs more readily [42].

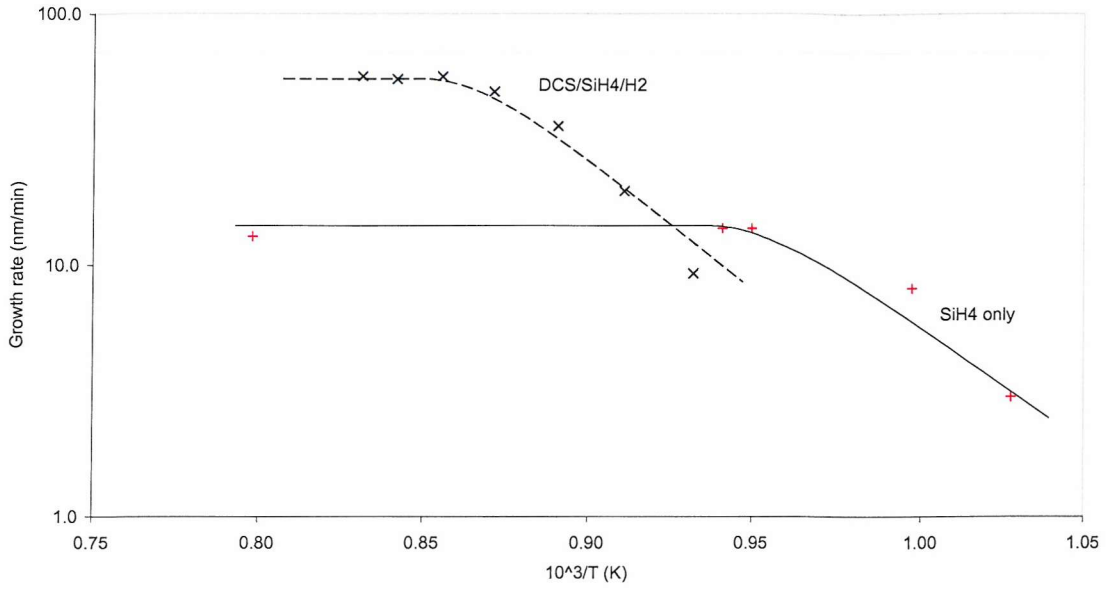


Fig. 6.8 Arrhenius plot of $DCS/SiH_4/H_2$ and silane only growth. The activation energy, E_a of the $DCS/SiH_4/H_2$ and silane only process is 2.4eV and 1.9eV, respectively.

6.4.2 Epitaxy Quality and Surface Morphology

Epitaxial quality is an important aspect in the fabrication of any semiconductor device, and temperature is one of the factors that directly impacts epitaxial quality. The Normarski images in figure 6.9 (a-c) show the morphology of the epitaxy and oxide surfaces of three growths, carried out at 825°C, 850°C and 915°C, respectively. The images show that the epitaxial quality improves with increasing temperature. At 825°C, the epitaxial layers look bumpy with visible hillocks and stacking fault defects. At 850°C, the surface of the epitaxial layers is smoother with no visible defects. When growth temperature is increased to 915°C, the epitaxial layers are largely smooth, although some very slight bumps can be seen on certain parts of the layers. Other types of surface defects such as those seen for the epitaxial layer produced at 825°C are not seen in layers grown at 915°C. This is highlighted in the SEM image in figure 6.10 which shows the smooth surface of the epitaxy.

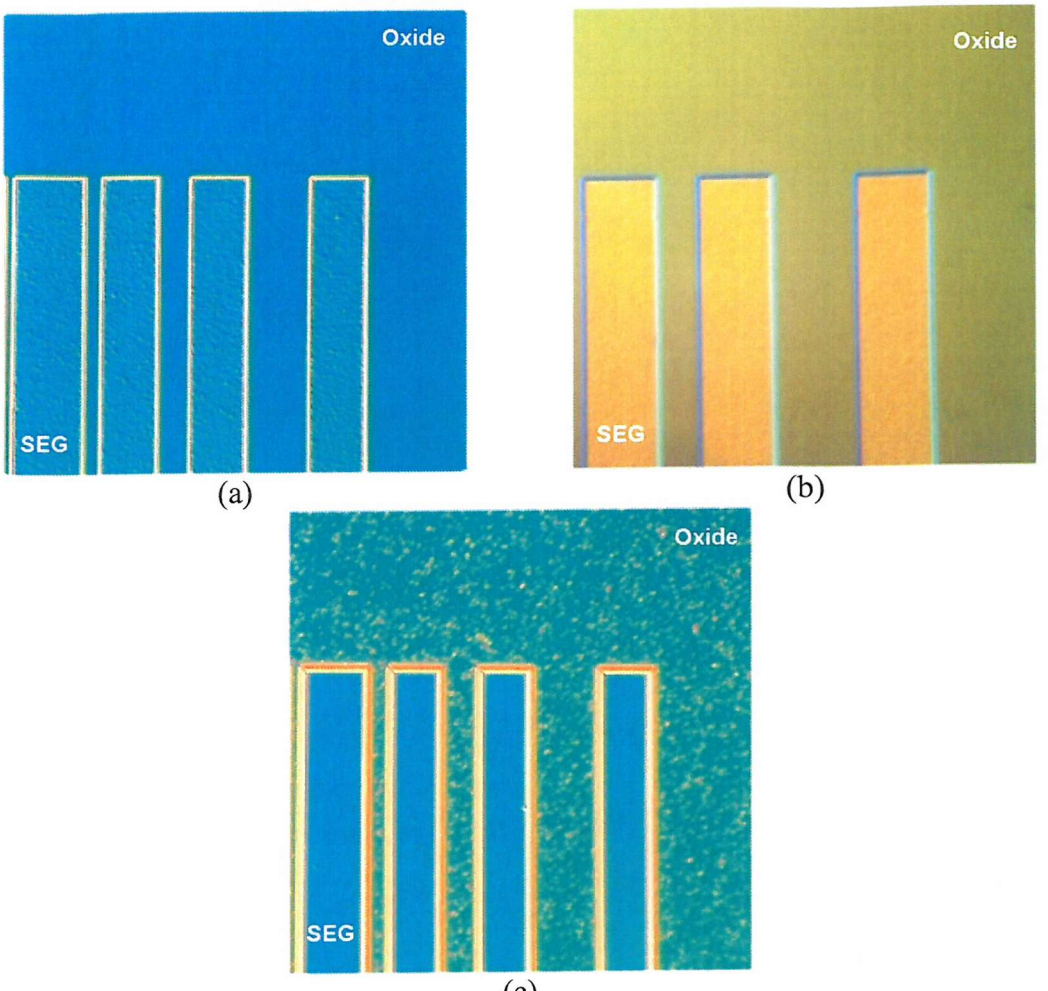


Fig. 6.9 Normarski images of epitaxial growths at (a) 825°C, (b) 850°C and (c) 915°C. Epitaxial quality improves with temperature.

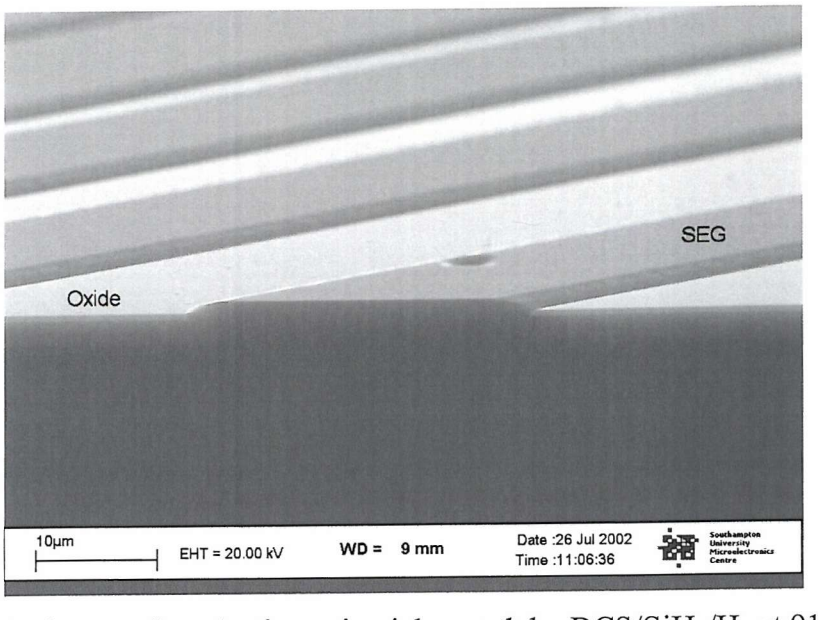


Fig. 6.10 SEM image of a selective epitaxial growth by DCS/SiH_4/H_2 at 915°C for 30 minutes, showing smooth epitaxial surface.

6.4.3 Selectivity

Although epitaxy was found to improve with increasing temperature, selectivity was found to degrade. Figures 6.11(a) to 6.11(d) show the density of the polysilicon islands on the oxide surface increases with increasing growth temperature. At 850°C and below, no polysilicon is observed on the oxide surface after 30 minutes of growth. However, polysilicon can be detected on the oxide surface for growths carried out at 875°C and above. The polysilicon island density at this temperature is 1.4×10^{6} islands/cm^2. At 900°C, the polysilicon island density increases sharply to 1.3×10^{7} islands/cm^2. This then drops to 5.2×10^{6} islands/cm^2 at 915°C. Examination of growth at 915°C shows that although the density of the polysilicon islands is reduced, the average size of the individual islands has increased. The estimated polysilicon island density at each growth temperature is shown in figure 6.12. The figure indicates that the increase in polysilicon island density with temperature after 30 minutes of growth is linear with temperature up to ~900°C. A linear approximation of the curve was made to estimate the maximum temperature at which growth can be maintained after 30 minutes. This was found to be around 875°C. To examine the length of incubation period at the highest growth temperature (930°C), growth after 15 minutes was found to be completely selective. As a comparison, at 850°C, growth became unselective after ~90 minutes. These results indicate that the incubation period shortens with increasing growth temperatures.

In summary, the results show that all DCS/SiH_4/H_2 growths at temperatures from 850°C through to 930°C are selective. Growths at 850°C and below have incubation periods greater than 30 minutes. Whereas growths above 850°C have incubation periods lower than 30 minutes. The polysilicon island density multiplied by polysilicon island size (the volume of silicon deposited on the oxide) can provide information on the incubation time and adsorption rates on oxide. In order to accurately assess these parameters a number of growths, over different time periods would be required at each temperature. Results for different growth times at 850°C (section 6.2.4) indicate the polysilicon islands grow rather slowly after incubation and, therefore, results here are likely to be a function of incubation time rather than growth rate.

The results of these epitaxial growths show that DCS/SiH_4/H_2 chemistry offers a wide selectivity window of from 750°C to 930°C, however, the incubation period shortens with increasing growth temperature. Even at 930°C incubation times of the order of ~15 minutes, allied to relatively high growth rates could be useful process conditions for thick layers (>500 nm). Further studies are required to fully characterise the system, however, within the context of this work, a process suitable for lateral HBT fabrication was found with this early set of experiments.

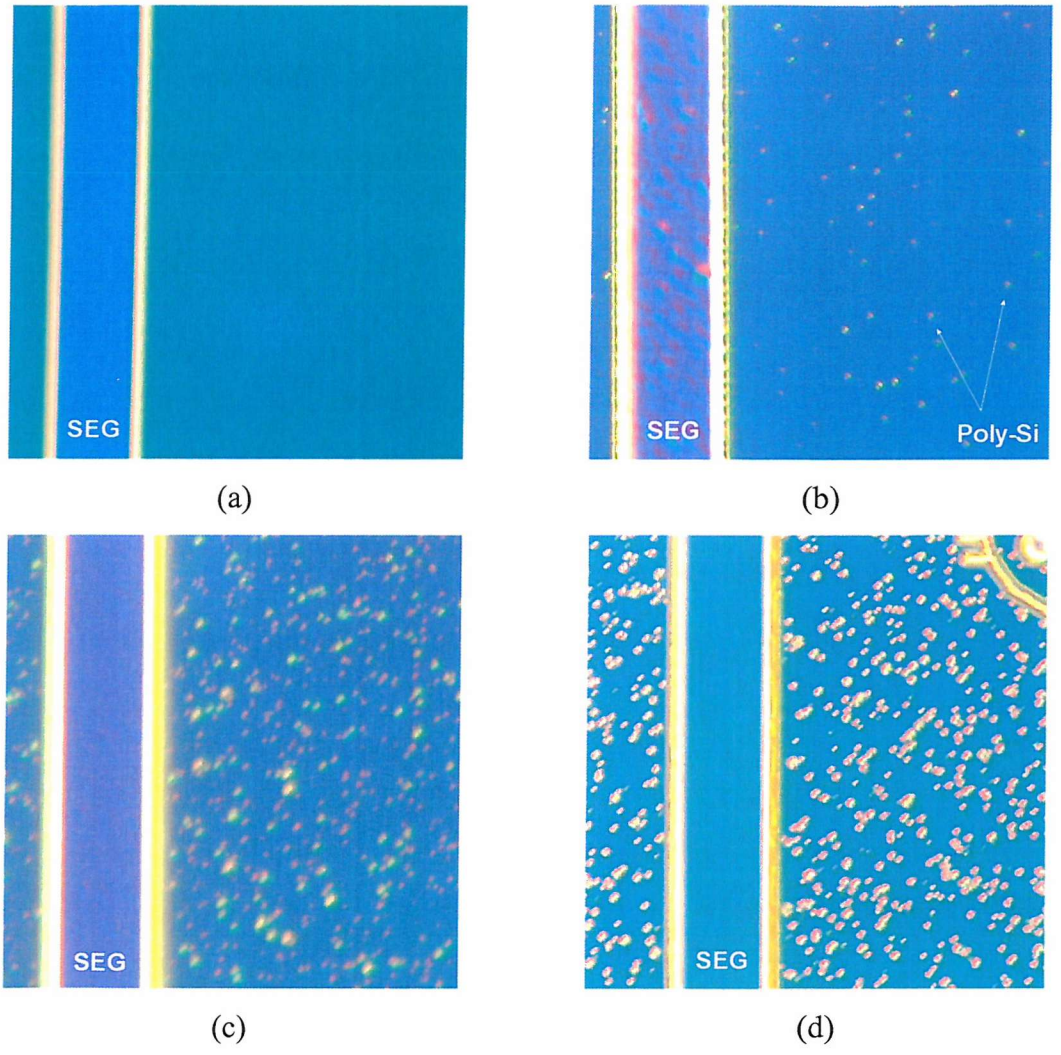


Fig. 6.11 Nomarski images of wafer surfaces with polysilicon deposition (except (a)) after epitaxial growths at (a) 850°C, (b) 875°C, (c) 900°C and (d) 915°C.

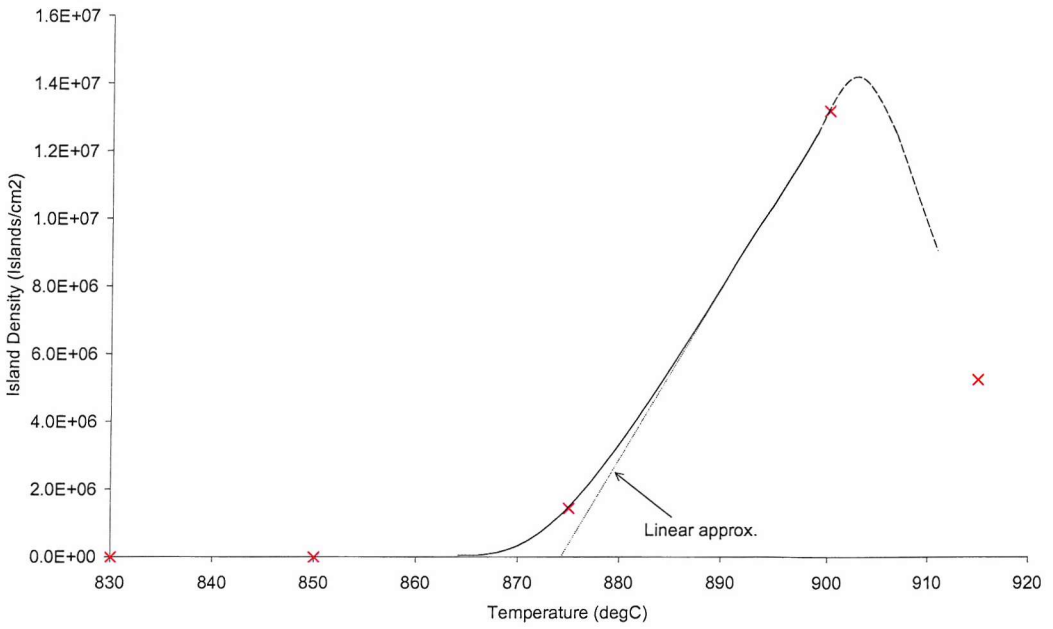


Fig. 6.12 Selectivity at 850°C, 875°C, 900°C and 915°C after 30 minutes of growth. Selectivity is excellent at 850°C but polysilicon islands are detected at the higher temperatures.

6.4.4 Growth Uniformity at Different Temperatures

Thickness uniformity across a wafer is an important consideration for epitaxial growth. Since thickness is strongly dependent on temperature in surface-reaction-limited regimes and position in mass-transport-limited regimes, thickness uniformity is potentially affected by all of these issues. Typical CVD epitaxy systems are designed to operate in either mass-transport or surface-reaction limited regimes, but not usually both. The SUMC reactors operate at the boundary of the two regimes and both gas-flow and temperature conditions need to be considered in order to achieve uniform growth. In general, to maintain device yield, growth thickness for all parts of a wafer should be the same and processes should be optimised to ensure this. In the SUMC reactors great care is taken to ensure that the wafers are uniformly heated, although the edges of wafers are inherently cooler. To assure uniform exposure to gas flow substrates are rotated and the gas-inlets are carefully positioned in relation to the substrate. Adjusting the height of the substrate is the most direct method with which uniformity can be gained in mass-transport regimes.

To determine the uniformity of deposition for the DCS/SiH_4/H_2 process, growths carried out at 825°C, 850°C and 930°C were examined in detail. The results of these measurements are shown in figure 6.13 . The epitaxy thickness measurements were taken from epitaxial growth in 10 μm seed windows at ten different chip sites across the wafer. These chip sites are denoted from 1 to 10 in the figure. The distance between chip sites is 10 mm, while the distance from the edge of the wafer to the first and tenth sites are 5 and 10 mm, respectively.

Figure 6.13 shows that the growth rates at 825°C, 850°C and 930°C, as measured at the central area of the wafer (area #6), are 20, 38 and 48 nm/min, respectively. The graph also shows that the growth rate reduces as growth moves away from the centre towards the edge of the wafer. For growth at 825°C, the difference in growth rate between the centre (area #6) and the edge (area #9) is 6 nm/min. For growth at 850°C, the difference is 5 nm/min, while at 930°C it is 3 nm/min. The graph also shows that at 930°C, the growth rate drops markedly at areas #1, #2 and #10. The drop between area nine and ten is 12 nm/min. This is much higher than the gradual drop seen between other sites, which is in the region of 0.5 nm/min.

Growth at sites close to the wafer edge is often atypical and are excluded from detailed analysis. To determine the uniformity of the growths, the values obtained from measurements were compared with the average growth rate across the wafer. Figure 6.14 shows the percentage difference between the average thickness and the actual thickness at different wafer positions for the three different temperatures. As in the previous figure, growths carried out at higher temperatures have better uniformity than at lower temperatures. At 825°C, the growth uniformity is +/- 10%, at 850°C it is +/- 5% and at 915°C it is only +/- 2%.

The SUMC epitaxy machines are generally operated for growth in the mass-transport limited region, an example of which is the silane-only growth presented in chapter 5, it is then unsurprising the best uniformity is obtained for the highest temperature growths (i.e. 915°C). The variation of +/- 10% for low temperature growth is due to temperature variations from the centre to the outside of the wafers. Improvements in uniformity may be achieved to some extent by an adjustment of the height of the substrate to

achieve higher flow rates at the edge of the wafer. However, this idea was not explored. Considering that the uniformity of growth at 850°C was considered to be good at +/- 5%, no further work on improving uniformity was carried out.

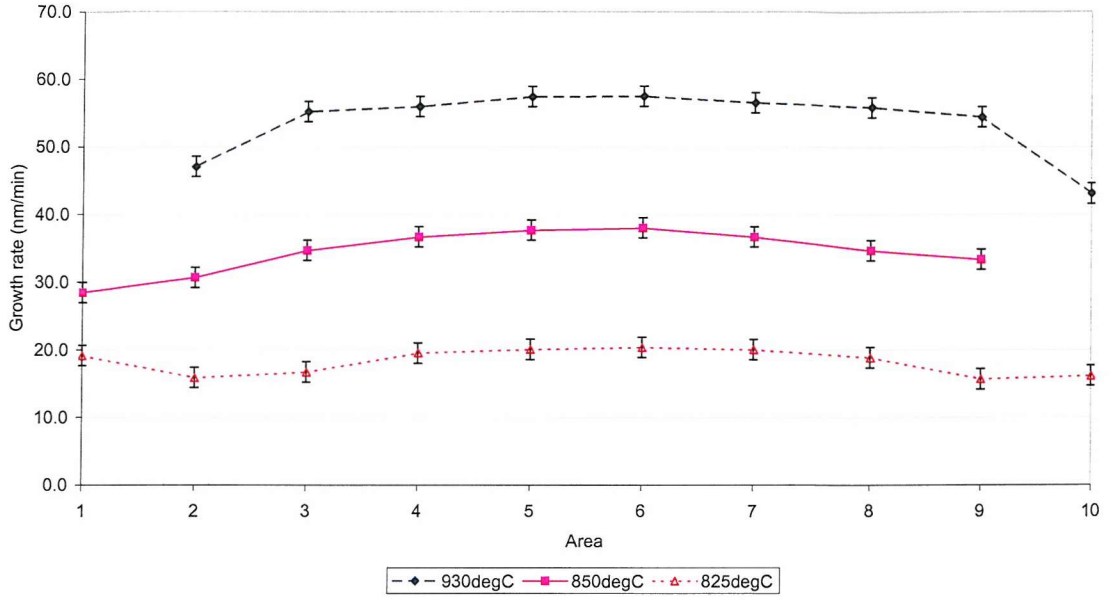


Fig. 6.13 Growth rate across the wafer for three different growth temperatures.

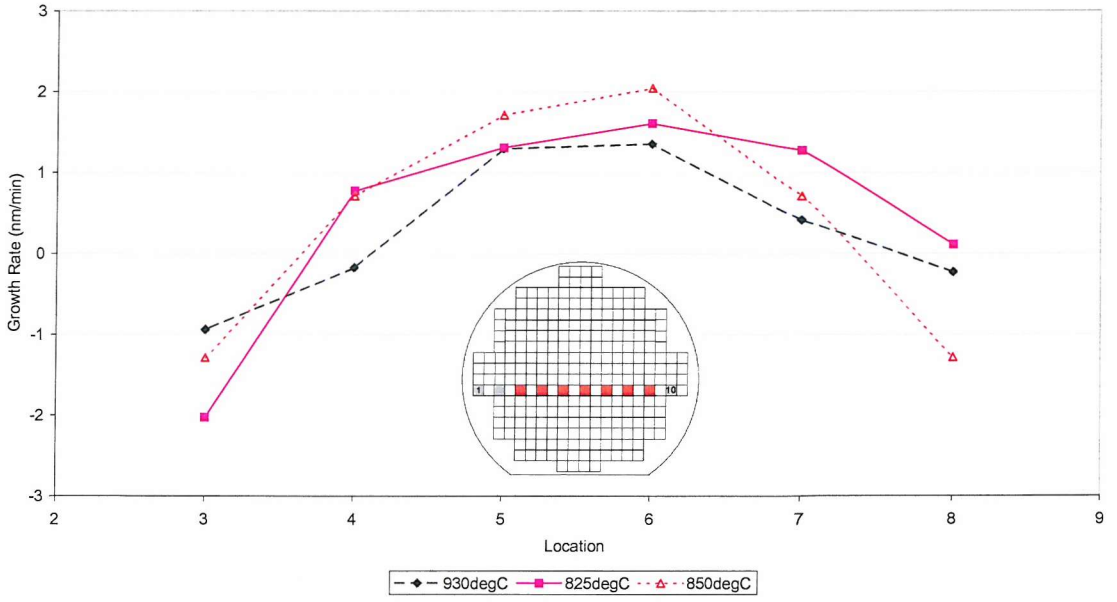


Fig. 6.14 Uniformity of selective epitaxial growths at 825°C, 850°C and 900°C. Uniformity improves with increasing temperatures.

6.4.5 Loading Effects

Section 6.4.4 looked at global uniformity issues, another important consideration are localised loading effects. It is easy to imagine that a small silicon seed window surrounded by a large area of oxide might experience a higher growth rate than a large area of silicon, if exposed silicon causes more gas depletion than an oxide mask then localised loading might be observed. In this section, the variation in growth rate due to local variations in the silicon to oxide ratio, or loading, is examined. To examine loading, the epitaxial growth by the DCS/SiH_4/H_2 process at 850°C in three different size seed windows, 3 μm, 6 μm and 10 μm, separated by 1 μm, 2 μm and 4 μm areas of oxide, were analysed. All of these measurements were carried out on the central areas of the wafer to ensure they were not influenced by uniformity issues discussed in the previous section.

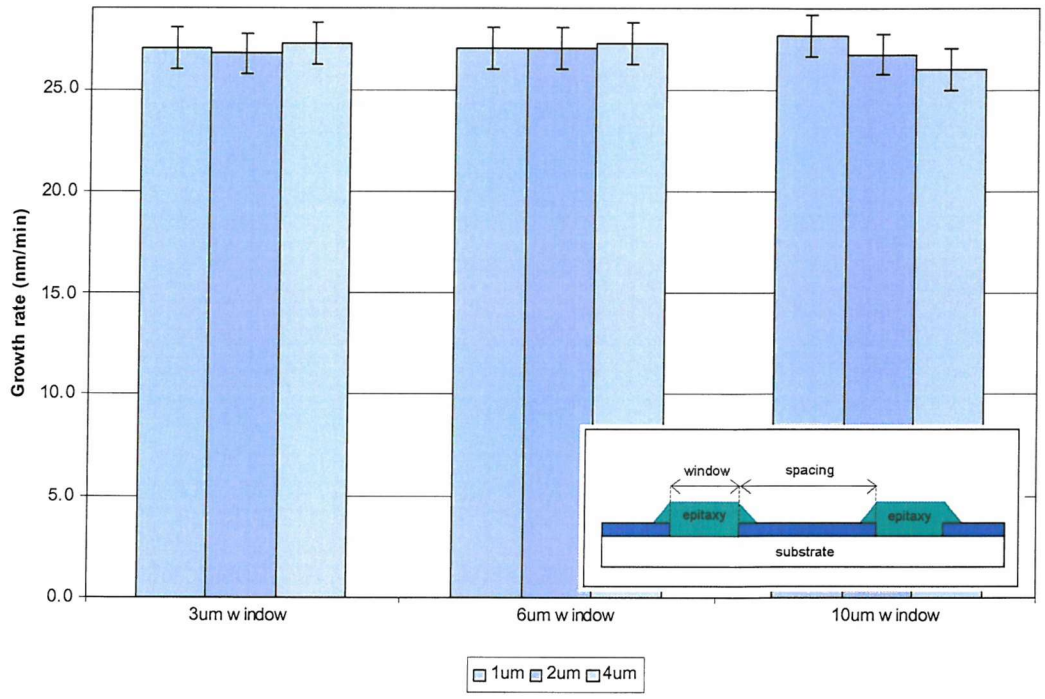


Fig. 6.15 Loading between windows, with error bars. No variation in growth (quantify) rate is seen.

The results of these measurements are shown in figure 6.15. The graph shows that the growth rates in all of the windows are very similar regardless of the silicon to oxide

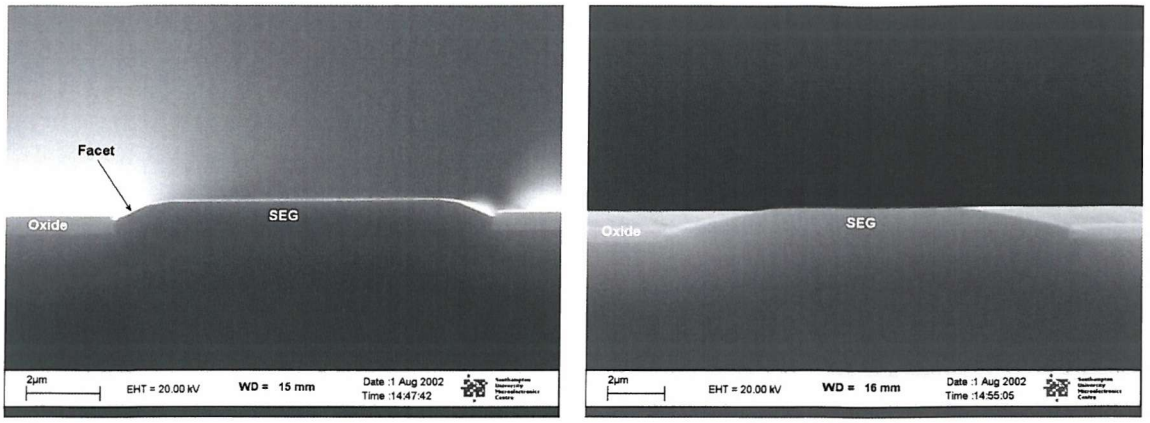
ratio in the immediate vicinity. This is a strong indication that silicon windows does not significantly deplete source gas concentrations close to the wafer surface. It is important to note that the measurements made here are representative of loading at a local scale and that global loading effects may still influence growth on the whole wafer.

6.4.6 Growth Uniformity in <1 0 0> and <1 1 0> Aligned Seed Windows

Devices fabricated by selective epitaxial growth are normally oriented to the <1 0 0> direction to minimise the generation of defects at the oxide sidewall area during epitaxial growth. The orientation of the device active area (i.e. seed window) has a direct impact on the quality of the epitaxial growth as it influences the development of the epitaxy. To examine the effect of seed window orientation on growth rate, epitaxial growth in <1 1 0> and <1 0 0> oriented seed windows were carried out at 850°C, 1 Torr for 30 minutes using DCS/SiH_4/H_2.

Results of epitaxial growth in <1 1 0> oriented seed windows were found to be faceted, forming the distinct {3 1 1} plane (figure 6.16(a)). In comparison, epitaxial growth in the <1 0 0> oriented seed windows were found to be free from faceting (figure 6.16(b)), although the corners of the seed window do develop facets. To compare the growth rates of the <1 1 0> and <1 0 0> seed windows, epitaxy thickness measurements were made on various chip sites across the wafer, which are shown in figure 6.17. As with previous measurements, chip sites that are close to the wafer edge (area #1 and #10) were omitted.

The results of the measurement show that any difference in vertical growth rate between seed windows oriented along the <1 1 0> and the <1 0 0> directions is small, and well within the error bars. The results also show that, for the process used, vertical growth rate is not a function of seed window orientation.



(a) (b)

Fig. 6.16 Growth in (a) <1 1 0> oriented seed window develops <3 1 1> facets after 30 minutes of growth. (b) <1 0 0> oriented seed window show no distinct facets.

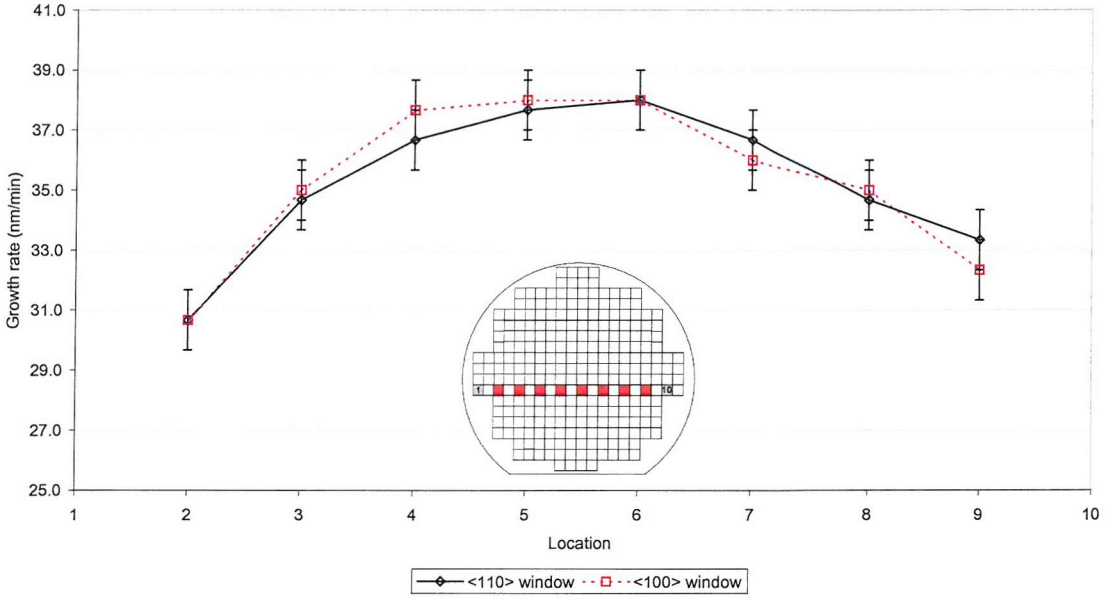


Fig. 6.17 Comparison of growth in <110> and <100> aligned seed windows, grown at 850°C using DCS/SiH_4/H_2. Little difference is seen between the growths.

6.5 Confined Selective Epitaxial Growth by DCS / SiH_4

So far, epitaxial growth using DCS / SiH_4 has been described for unconfined growth from ordinary seed windows. As with the silane-only process (section 5.2.4), selective epitaxial growth was attempted in test cavities in order to determine suitability for confined growth. The purpose of this experiment is to study the impact of the cavity on

epitaxial growth development and to compare with unconfined growth. Aspects such as growth rate and faceting are of particular interest in this study as growth in a confined structure like the cavity may have an effect on these aspects.

Figure 6.18 illustrates confined selective epitaxial growth in a test cavity. Ideally the CSEG region in figure 6.18(a) should have the same shape and dimensions as the SEG region in the unconfined window (fig.6.18(b)), as this would indicate that epitaxy conditions are such that mass-transport and loading effects are not affecting the epitaxy.

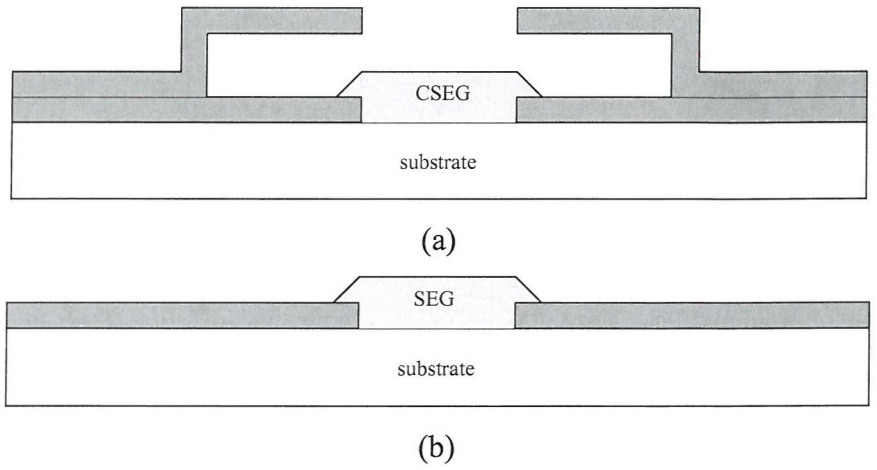


Fig. 6.18 (a) Cross section of test cavity with CSEG. (b) Cross section of unconfined window with SEG.

Indeed, confined selective epitaxy growth in test cavities using DCS/SiH_4/H_2 at 850°C, at 1 Torr and for 30 minutes were found to be similar to selective epitaxy growth in unconfined seed windows. The vertical growth rate of unconfined selective eptiaxy at the central area of the wafer was found to be 28 ± 2 nm/min. In comparison, the vertical growth of confined selective epitaxy was found to be 27 ± 2 nm/min. Inspection of the epitaxy thickness at the centre, middle and outer areas of the wafer shows that at all three areas, the epitaxy thickness of both confined and unconfined growths to be similar, as shown in figure 6.19 (the centre, middle and outer area refers to the area within 50 mm, 25 mm and 5 mm, respectively from the wafer edge). As seen in previous uniformity measurements, growth at the edges of the wafer are

reduced due to gas and temperature effects at the wafer edge effects. In this experiment, no epitaxial lateral overgrowth was observed, which is expected as the growth time was relatively short.

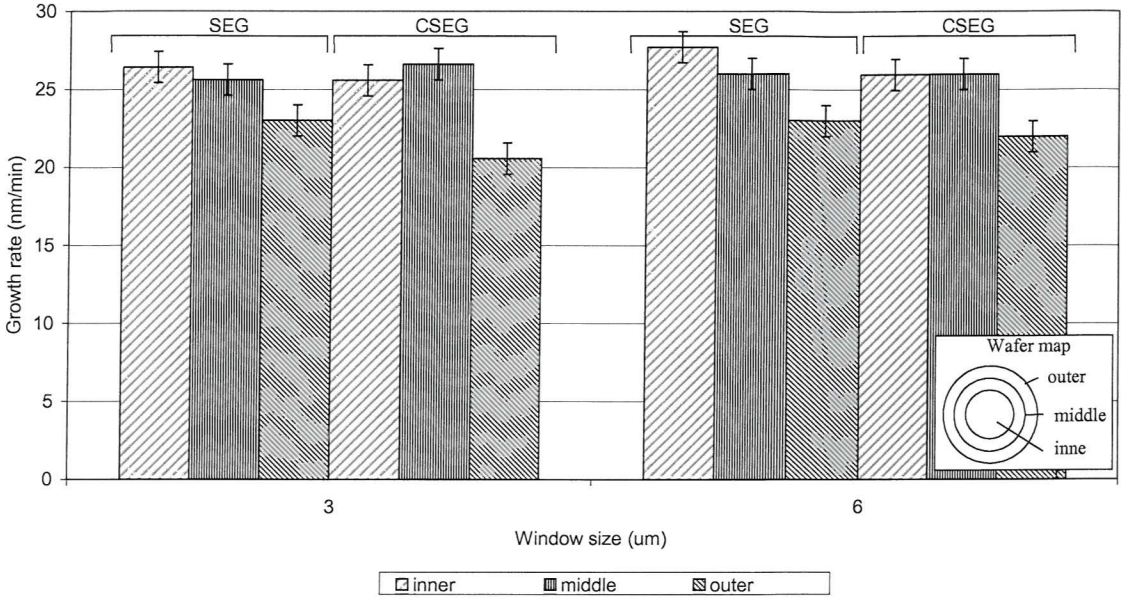
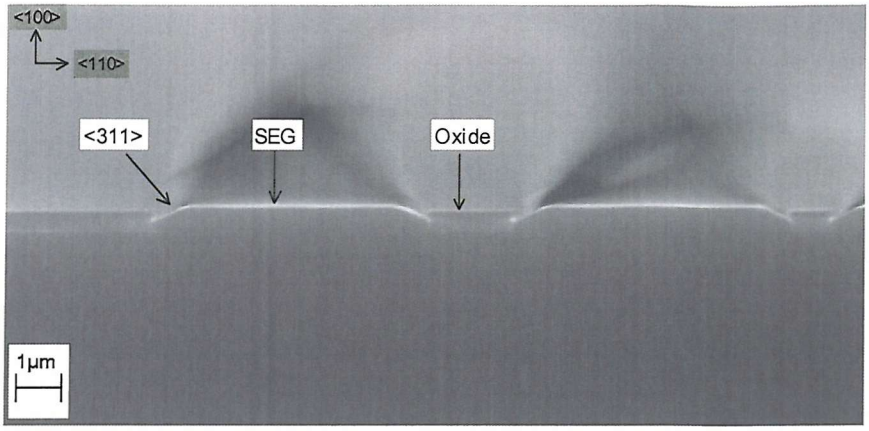
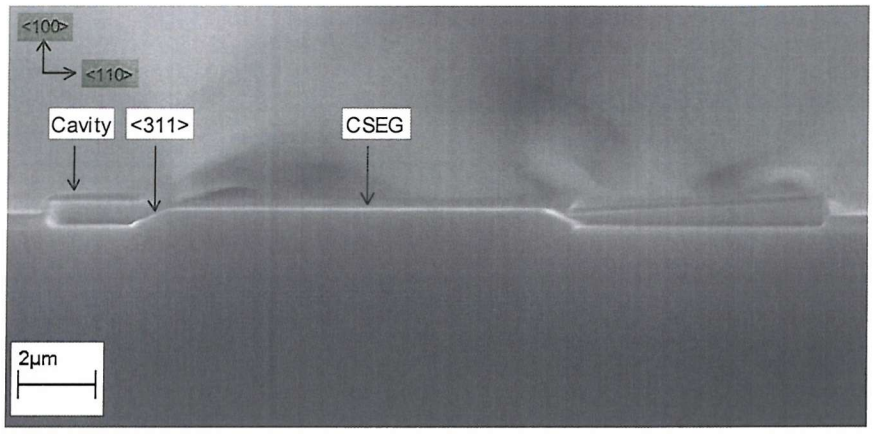


Fig. 6.19 Uniformity of unconfined selective epitaxial growth (SEG) and confined selective epitaxial growth (CSEG) in 3 μm and 6 μm window across a wafer.

Figure 6.20 shows epitaxy growth in unconfined seed windows and in a test cavity. From the SEM images, it can be observered that epitaxy growth in the cavity develops <3 1 1> facets in addition to the <1 0 0> facet. The same facets are also observed in unconfined growth. In terms of epitaxy quality, the surface of the epitaxial layers grown by confined selective epitaxial growth was found to be smooth, indicative of good epitaxial quality and similar to the sort of epitaxy quality seen in section 6.4.2 under the same growth conditions. In addition, growth in the test cavities was found to be confined to the exposed silicon areas with no evidence of selectivity loss either in the inner walls of the cavities or on outer walls or surfaces. This result indicates that the cavity preparation techniques provide suitable surfaces for selective growth, with no polysilicon residues or other nuleation centres and that with DCS/silane growth, the incubation period for growth on oxide remains above 30 minutes.



(a)



(b)

Fig. 6.20 Cross-sectional SEM of (a) SEG and (b) CSEG by DCS/SiH_4. Images show SEG and CSEG to be similar in terms of growth rate and facet formation. The substrate orientation is (1 0 0) the oxide sidewalls of the features are also in the <1 0 0> direction.

The similiarity between the confined and unconfined selective epitaxial growth in terms of growth rate, uniformity, facet development and epitaxy quality shows that confining structures do not significantly alter mass-transport phenomina in the areas imeadiately surrounding the growth front. This is despite the lower local silicon to oxide silicon ratio of the confined growth, due to the extra oxide area introduced by the cavity, as compared to unconfined growth. The similarity of the two growths is advantageous as it means that processing development for unconfined selective epitaxial growth can be

easily applied to confined selective epitaxial growth. An extension of this growth study would be to examine fully confined lateral selective epitaxial growth and how it compares with unconfined growth. A similar result from this study would further strengthen the theory of the similiarity between confined and unconfined growth at the epitaxy growth conditions which have been carried out. This following section examines this in detail.

6.6 Confined Lateral Selective Epitaxial Growth by DCS / SiH_4

In the previous section, growth in test cavities showed that pseudo-confined epitaxial growth is similar to unconfined epitaxial growth. In order to determine the feasibility of using the DCS / SiH_4 for lateral device fabrication, fully confined lateral epitaxial growths were carried out using SOI cavities. The use of the SOI cavities allows growth to be carried out directly from a vertical {1 0 0} seed, allowing lateral growth to be achieved immediately. In addition, growth from a {1 0 0} seed should theoretically result in epitaxial growth in the <1 0 0> direction, maximising the lateral growth rate that can be achieved. At this stage the vertical seed SOI cavity approach was considered more promising than the horizontal seed open-sided cavity approach. In the first instance SOI cavities are easier to prepare and provide a route to lateral growth that avoids the development of facets with slow lateral growth rates.

The growth conditions that were used for confined epitaxy growth was 900°C at a pressure of 1 Torr using DCS / SiH_4 / H_2 with a ratio of 10:10:100 sccm. The growth rate with these conditions, estimated from unconfined vertical growth experiments, is 56 nm/min (see section 6.4.1). Assuming the lateral growth rate will be similar to the vertical growth rate (both are on the (100) plane), the growth time was set at 60 minutes to give lateral epitaxial growth of over 3 μm. This was intended to allow epitaxy to grow laterally out of the cavity and be clearly visible for optical and SEM observations.

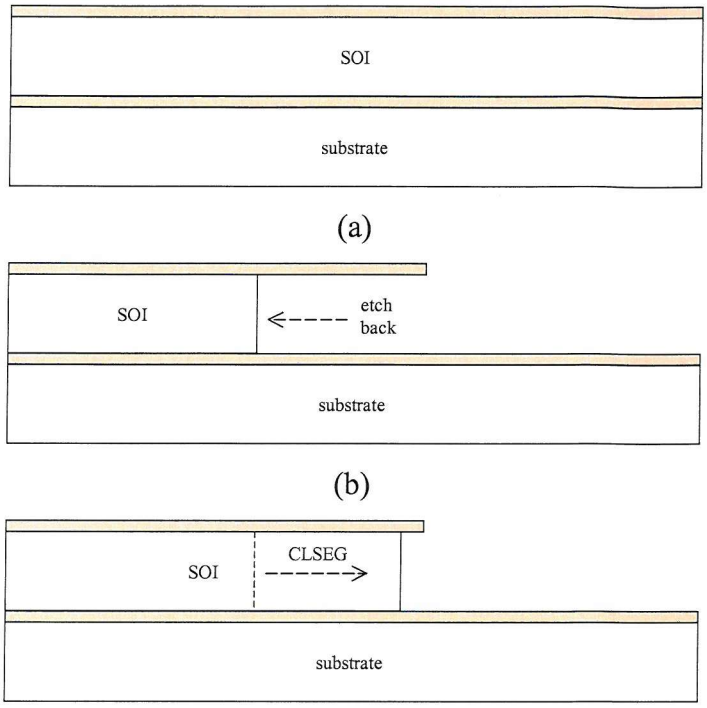


Fig. 6.21 Confined lateral epitaxy growth process, from wafer fabrication to growth. (a) Oxidation of SOI substrate. (b) Formation of silicon sidewall by dry etching. (c) Unconfined lateral growth by LPCVD.

6.6.1 Results

Figure 6.22 shows the results of the confined epitaxial growth experiment as observed by Nomarski optical microscopy. It shows that there is a high density of polysilicon islands on the wafer surface, indicating the epitaxial growth has lost selectivity. The figure also shows that there is little lateral epitaxial growth inside the cavities. Inspection by SEM revealed that some growth did occur in the <1 0 0> oriented cavities, as shown in figure 6.23. However, no significant growth can be measured in <1 1 0> oriented cavity (figure 6.24). The epitaxial growth in the <1 0 0> oriented cavity is estimated to be 500 +/- 50 nm. Closer examination of the confined epitaxial growth was made by SEM and figure 6.25 shows the morphology of the epitaxial growth front in a corner of a <1 1 0> oriented cavity. To determine that this growth is truly epitaxial, a sample was dipped into a silicon KOH etch for one minute. This etches away any polysilicon islands but leaves the epitaxy relatively intact. Inspection

of the sample after the etch shows that growth in the cavities are indeed epitaxial. Figure 6.25 also shows polysilicon island deposition on the surface of the oxide with the edge of the cavity in particular, being completely covered by polysilicon. The growth front of the epitaxy looks to have come almost to the edge of the over-etch mark, which confirms the optical observations of the extent of confined growth. Figure 6.26 shows clearly the morphology of the epitaxy growth front which is non-uniform and rippled with no distinct facets.

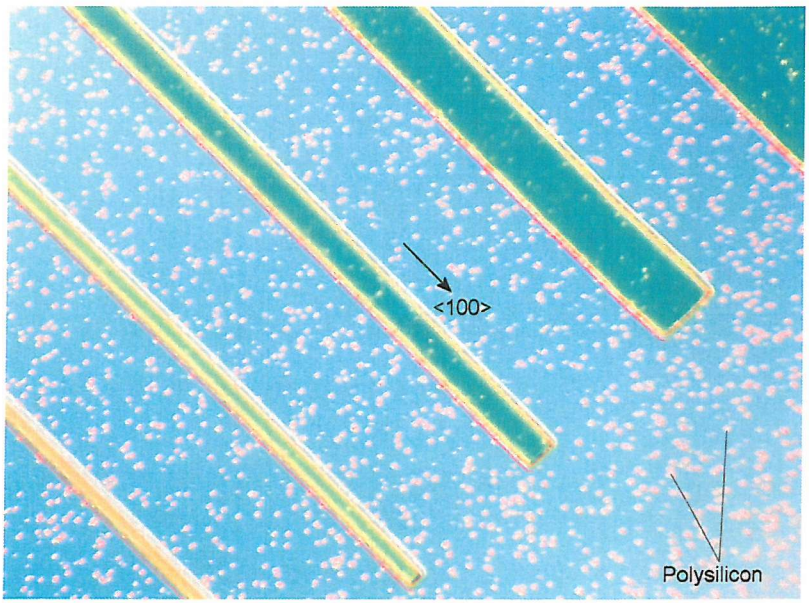


Fig. 6.22 Normarski image of confined epitaxy growth at 850°C for 90 minutes.

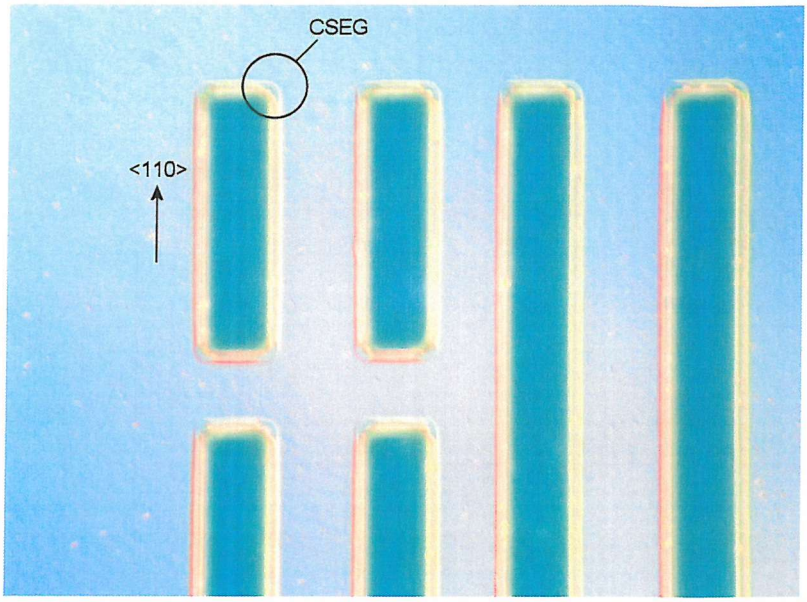


Fig. 6.23 Normarski image of epitaxial growth in SOI cavities oriented along the <1 1 0> direction. Confined growth can only be seen in the corners of the cavities.

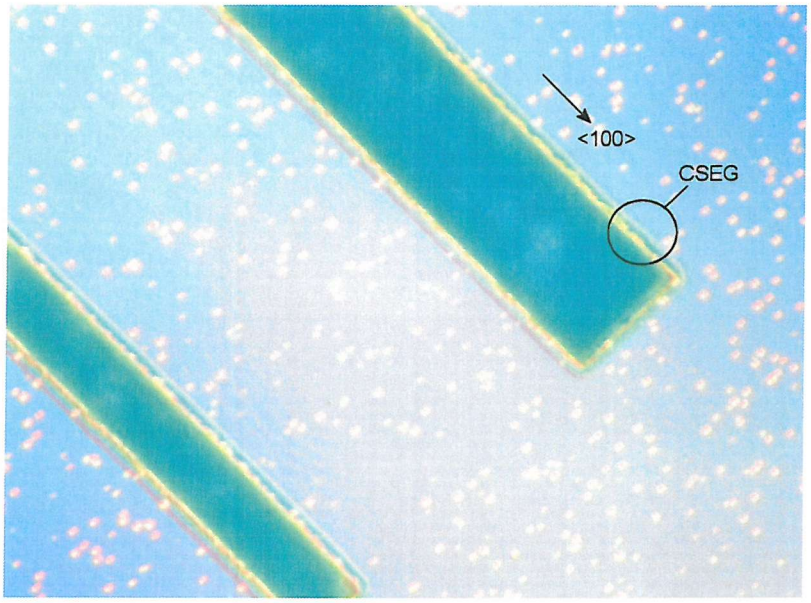


Fig. 6.24 Normarski image showing epitaxial growth in SOI cavities oriented along the <1 0 0> direction. Confined growth can be seen inside the cavities all along the cavity sidewall.

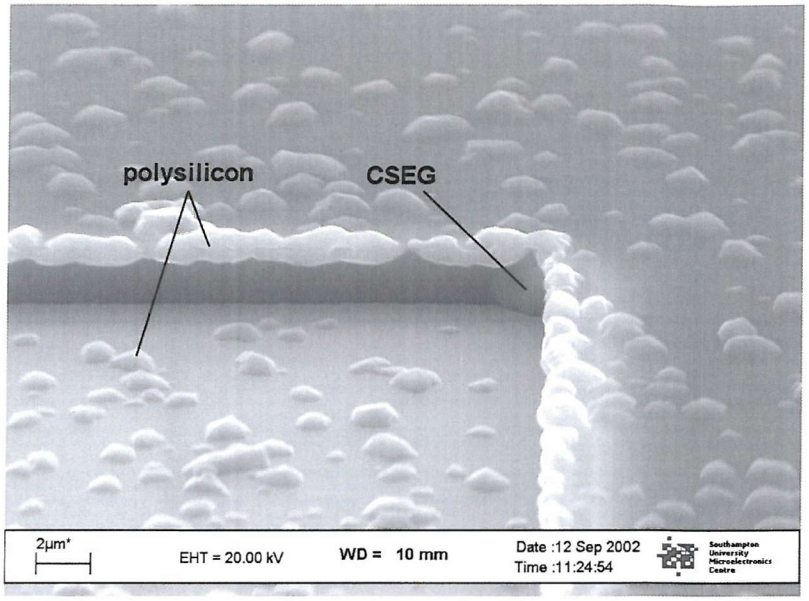


Fig. 6.25 SEM image of a <1 1 0> oriented cavity showing confined (100) epitaxial growth in the corners.

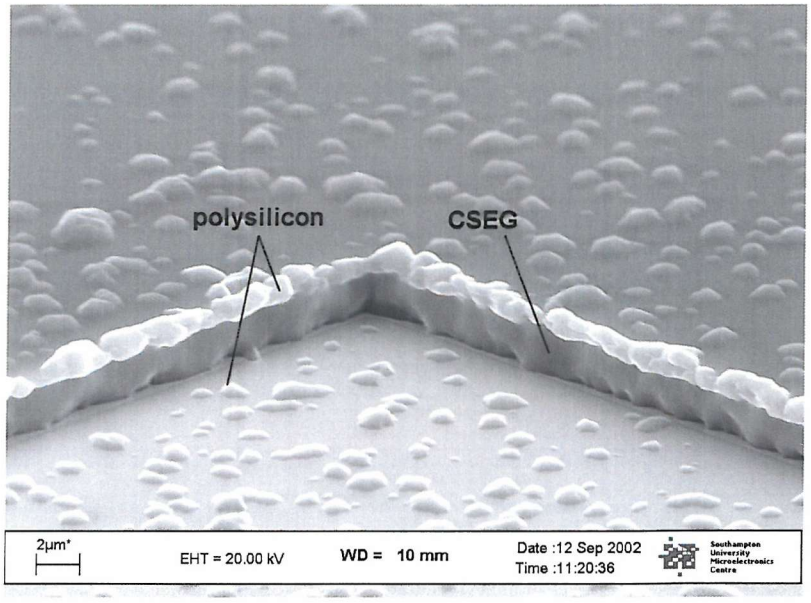


Fig. 6.26 SEM of <1 0 0> confined epitaxial growth showing growth inside the cavities.

6.7 Unconfined Lateral Selective Epitaxial Growth by DCS / SiH_4

Accurate knowledge of the rate of lateral growth is important for the fabrication of the lateral transistor as it impacts the accurate placement of the transistor's base region. One of the problems associated with confined epitaxial growth is determination of the exact extent of lateral growth. This problem stems from the difficulty in differentiating between the original silicon seed plane and the epitaxial layer, particularly if there is little growth. In order to determine the extent of growth more precisely, a 90 minutes growth was carried out at 900°C and 1 Torr using DCS / SiH_4 / H_2 with a ratio of 10:10:100 sccm., but this time with no etch-back of the SOI. The growth would therefore begin straight from the sidewall of the etched SOI layer. With this scheme, the edge of the oxide layer above the SOI acts as the reference point that will allow the start point of the epitaxial growth to be identified. Although this lateral growth is unconfined, the growth is expected to be similar to lateral confined growth.

6.7.1 Results

Figure 6.27 and figure 6.28 shows the result of the unconfined lateral growth from a {1 1 0} and {1 0 0} sidewall, respectively. The distance of lateral growth achieved from a {1 1 0} sidewall is 500 nm, while 1.5 μm of lateral growth emerges from a {1 0 0} sidewall. This corresponds to a growth rate of 5 nm/min and 17 nm/min, respectively. Selectivity is seen to be excellent and little polysilicon deposition is observed on the oxide surface. The surface of the epitaxial growth front, as can be observed from figure 6.27, is rippled and non-uniform. This result is similar to that observed after confined lateral epitaxial growth. It is believed that these ripples are a result of the ripples that are already present on the SOI sidewall prior to growth (section 4.5.2 looks at this problem in more detail). In comparison, the morphology of the lateral growth from a {1 0 0} sidewall (figure 6.28) is seen to be generally smooth, however, the epitaxy situated close to the buried layer of the SOI is very rippled. In addition, the thick lateral growth has also resulted in some overgrowth over the top oxide layer.

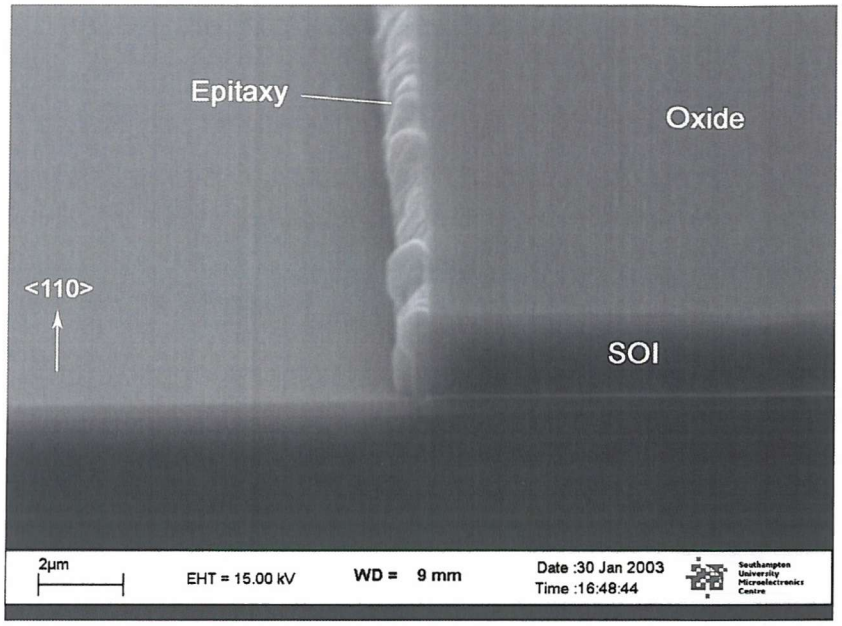


Fig. 6.27 Lateral epitaxial growth from a <1 1 0> silicon sidewall, the surface of the epitaxy is seen to be very rippled.

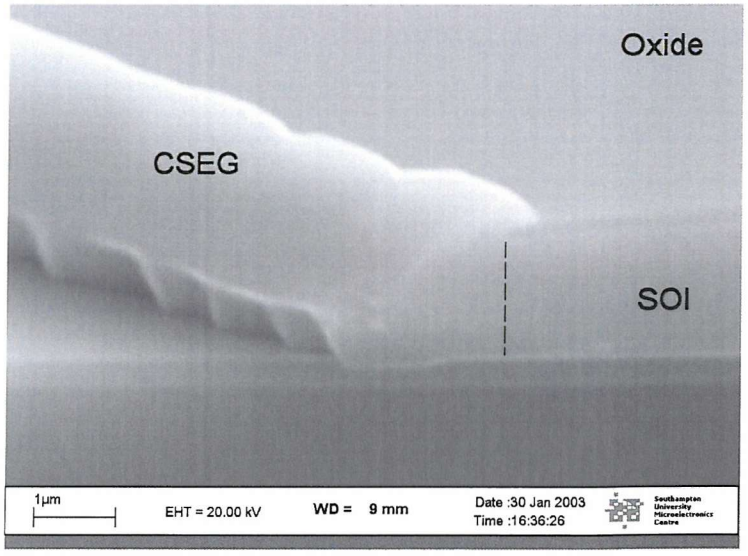


Fig. 6.28 Lateral growth showing epitaxial overgrowth over the top oxide and faceting of the epitaxy.

6.7.2 Discussion

The difference in the lateral growth rates for <1 0 0> and <1 1 0> oriented growths is due to the difference in growth rates of the two different crystal planes. From measurements, the average growth rate on the <1 1 0> sidewall was found to be 50% slower than average growth rate on a <1 0 0> sidewall. Interestingly, the lateral growth rate of the <1 0 0> sidewall is much slower than the vertical growth rate from the same crystal plane. The average vertical growth rate from a {1 0 0} plane was found to be 38 nm/min (see section 6.4.1), which is slightly more than three times the lateral growth rate on the same plane. In principle, in conditions where mass-transport and temperature variations are minimised the growth rates for vertical and horizontal <100> planes should be identical. Sections 6.4 and 6.6 have shown mass-transport and temperature effects to be minimised for the DCS/silane processes used in this work, this therefore, suggests that there is another reason for the reduction in growth.

Although vertical growth has been carried out on {1 0 0} wafer substrates, there has been no vertical growth carried out on {1 1 0} substrates. The later is being planned for future work. Therefore, the lateral growth rate on this particular plane cannot be compared to any vertical growth data. Table 6.2 below summarises the unconfined lateral and vertical growth rates results.

Growth Plane	Vertical Growth (nm/min)	Lateral Growth (nm/min)
{1 0 0}	55	17
{1 1 0}	n/a	5

Table 6.2 Unconfined lateral and vertical growth rate on {1 0 0} amd {1 1 0} crystal planes. Growth was carried out at 900°C at 1 Torr.

There could be several reasons for the reduction in lateral growth rate. The most likely reason is the roughness of the vertical seed surface, as first highlighted in section 4.5.2.

An important prerequisite for good quality epitaxial growth is an atomically smooth and defect free surface as this ensures monotonic growth of silicon adatoms on the crystal plane. If however, the surface of the seed is not atomically flat, as is the case with the SOI sidewall, defect free epitaxy will be more difficult to achieve. A very poor seed surface will lead to defected epitaxy, or polycrystalline growth. In less extreme cases a rippled surface will result in slower growth. A rippled surface is in fact a multi-faceted surface, and epitaxial growth will occur on each exposed facet with different growth rates. The fastest growing facets will rapidly form vertices and ultimately growth rate will be determined by the slower-growing facets. As a result of this, the overall growth rate will be significantly reduced. To ensure that epitaxial growth rates on vertical (100) seed windows is the same as horizontal (100) seed windows, the vertical walls need the same surface roughness as the epi-ready silicon substrate.

6.8 Selective Silicon Germanium Epitaxial Growth by DCS / SiH_4

Selective silicon germanium epitaxy growth is an essential requirement for the fabrication of heterojunction devices. In this section, preliminary results of undoped selective silicon germanium epitaxy growth are presented. The growth is based on the DCS / SiH_4 / H_2 selective epitaxy process. To obtain silicon germanium layers, germane (GeH_4) was added to the DCS / SiH_4 process. Growth was carried out at a temperature of 850°C at 1 Torr with a DCS / SiH_4 / H_2 flow rate ratio of 10 : 10 : 100 sccm. The GeH_4 flow rate was set at 10 sccm. Like the selective silicon epitaxy growth studies, growth was carried out in unconfined seed windows of various sizes and orientations. Growth time was 30 minutes.

The results of the growth are shown in figure 6.29. The figure is an image of the wafer surface as viewed by Normarksi and shows the growth is completely selective with no indication of polycrystalline island deposition on the surface of the oxide. The selectivity seen in this growth is similar to what would be expected from *silicon* epitaxial growth using the same growth conditions as discussed in section 6.4.3. The morphology of the silicon germanium epitaxy can be seen to be cross-hatched, which is a clear indication that the silicon germanium layer has relaxed. In addition to this,

pyramid defects can also be observed on the epitaxy surface. However, the defect density is low (i.e. ~$1x10^5$ pyramids/cm^{-2}) compared to the exposed silicon area.

Although the germanium content in the epitaxial layer has not been characterised, based on previous silicon germanium growths using silane-only, it is estimated to be in the region of 5% to 10%. With the thickness of the silicon germanium epitaxial layers obtained, along with the estimated germanium concentration, the grown layers are much thicker than the critical silicon germanium strained layer thickness [30, 31]. It is then not surprising that the layers are relaxed. With a reduction in thickness, the process is expected to produce strained silicon germanium layers.

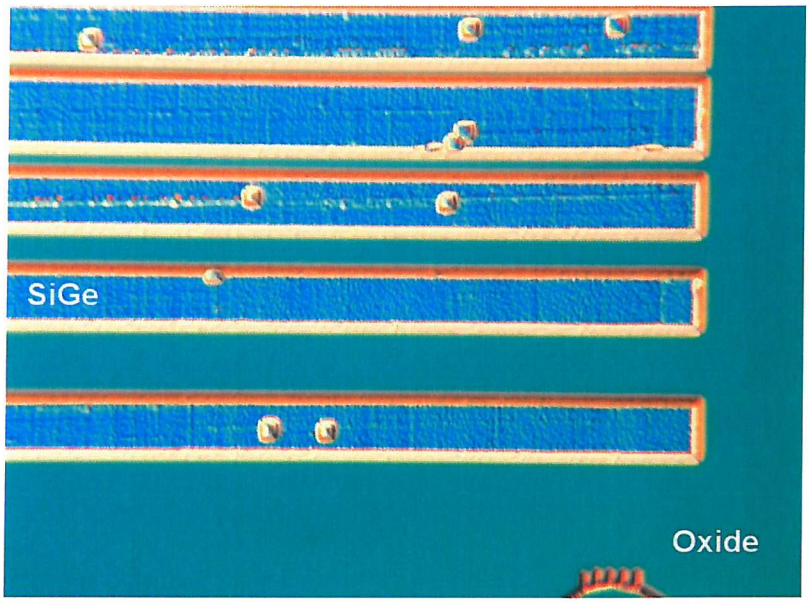


Fig. 6.29 Selective SiGe growth showing cross hatched surface and several pyramid shaped defects.

Although relaxed silicon germanium layers were obtained in this growth, the selective process that is used shows promise. In order for the process to be usable in a device process, further characterisation would be required. This would include an examination of the conditions that provide defect free strained silicon germanium layers, characterisation of the germanium concentration with respect to the conditions used, and the incorporation of boron doping.

6.9 Conclusions

In chapters 5 and 6, silane only and DCS/silane selective epitaxy processes have been examined. Both processes have been found to produce good quality epitaxial layers. The results described in section 6.4.3 show that the DCS / SiH_4 process achieves selective growth at a much lower temperature (down to 750°C) than silane (980°C). Results also show that both the DCS / SiH_4 and the silane-only processes lose selectivity after a finite incubation period. Silane-only growth has been found to have an incubation period of between 20 and 30 minutes, after which a dramatic increase in polysilicon island deposition is observed on oxide. With DCS / SiH_4, the incubation time is longer and is close to 90 minutes, even after 90 minutes of growth, polysilicon is observed but at a much lower density (1×10^6 islands/cm^2). The reason for the good selectivity and longer incubation time is attributed to the use of dichlorosilane, which allows selectivity to be controlled by providing a reversible reaction mechanism.

The DCS/SiH_4/H_2 process offers several significant advantages over the silane-only process. These are summarised in table 6.3.

.

Selectivity	Selective growth between 750°C to 930°C. Improved selectivity allows longer growths. Selective SiGe growth.
Low Temperature	Reduced thermal budget. Reduced diffusion / sharper junction profiles. Germanium incorporation. No oxide pitting.
General	Good uniformity >850°C (+/- 5%) No local loading effects.

Table 6.3 Advantages of the DCS / SiH_4/H_2 over the silane-only epitaxy process.

In addition to the above, results have shown that the use of a DCS / H_2 prebake prior to epitaxy growth leads to a significant improvement in the quality of epitaxial layers. The results presented in this chapter show that the DCS/SiH_4/H_2 process is a big improvement on the previous silane-only epitaxy processes, however, further development is necessary to fully optimise this process.

Chapter 7

Lateral SiGe Heterojunction Bipolar Transistor: Design & Simulation

This project has mainly been concerned with the development of techniques with which the lateral HBT described by Tang and Hamel *et al.*, [19, 115] (section 2.8) could be fabricated. In this chapter a new design of lateral heterojunction bipolar transistor is proposed. This new design takes into account all of the fabrication difficulties that have been discovered during this work and makes use of the new techniques that have been established.

The new design, is based on growth from an SOI cavity and employs the confined lateral selective epitaxial growth (CLSEG) technique developed in chapter 6. The design takes into account the lateral growth limitations and selectivity duration of the current CLSEG process that limits selective lateral confined growth to ~1 μm. It also takes into account the current inability to grow selective *in situ* doped silicon epitaxial layers. However, the design does assume that thin strained doped silicon germanium layers can be grown. This assumption is made based upon recent positive development in this area, and it is expected that a selective doped (p-type) silicon germanium process will be available in the near future.

Simulations are performed to assess the likely performance of the proposed lateral

device, fabricated with the technology that is currently available at the fabrication facility. Design optimisation and scaling could further improve performance to competitive levels.

There are several differences between the lateral device proposed in this work and the lateral device proposed by Tang and Hamel *et al.* The lateral HBT described by Tang and Hamel *et al.* uses sub-micron lithography and thin silicon-on-insulator substrates (i.e. 0.1 μm SOI active layer). Besides this, the device uses a self-aligned base process method which allows direct contact to be made by an external base contact. In addition, the epitaxial growth process used in the fabrication process employs *in situ* doping which allows the collector, base and emitter regions of the transistor to be formed during the confined epitaxial growth step.

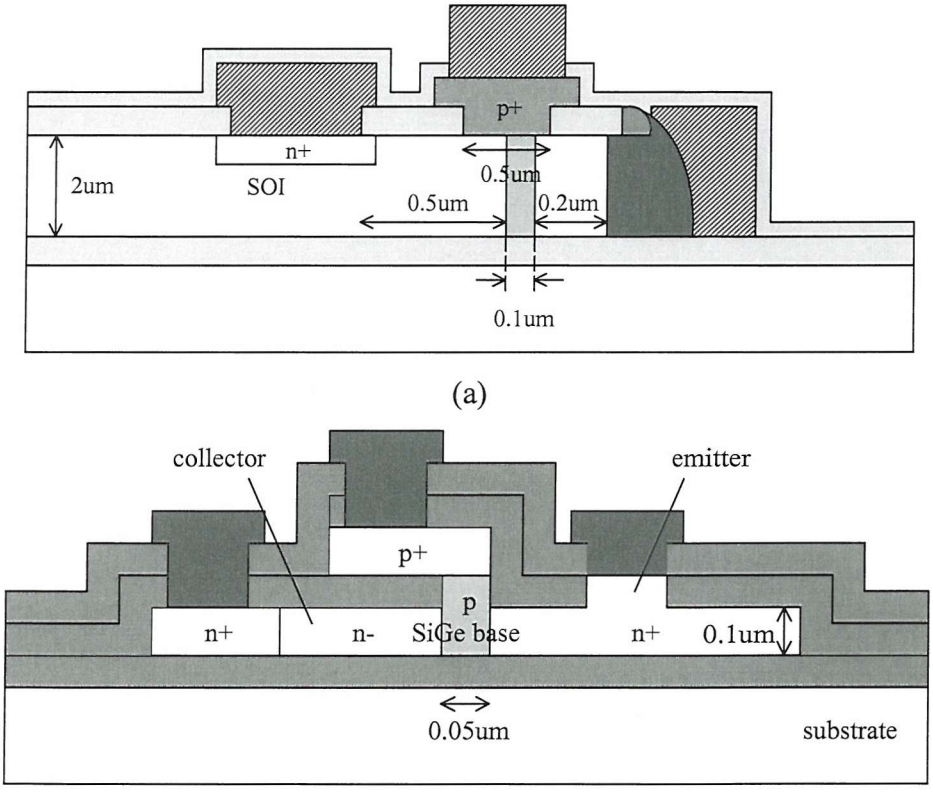


Fig. 7.1 Schematic of lateral SiGe heterojunctioin bipolar transistor (a) proposed in this work, (b) proposed by Tang and Hamel *et al.*

In comparison, the device proposed in this work assumes a lithographic resolution of

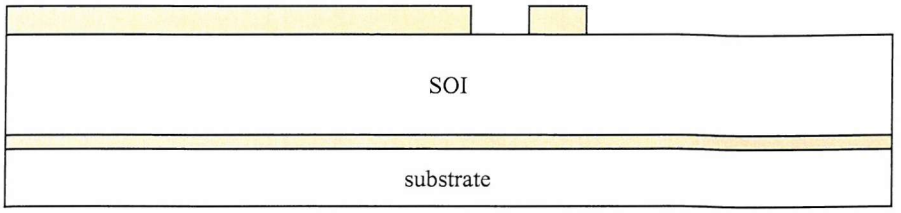
0.5 μm. The lateral devices are fabricated on SOI wafers with an active layer thickness of 2 μm. The collector, base and emitter regions of the transistor are grown by CLSEG (undoped), but doping is done *ex situ* by diffusion, with the exception of the base, which is doped *in situ* during epitaxial growth. In addition to this, contact to the base is not directly aligned to the intrinsic base, instead, it overlaps a small part of the emitter and collector. Figure 7.1 shows a schematic of the lateral SiGe HBT proposed in this work and that of Tang and Hamel *et al.* along with geometry of the active regions.

7.1 Fabrication Process

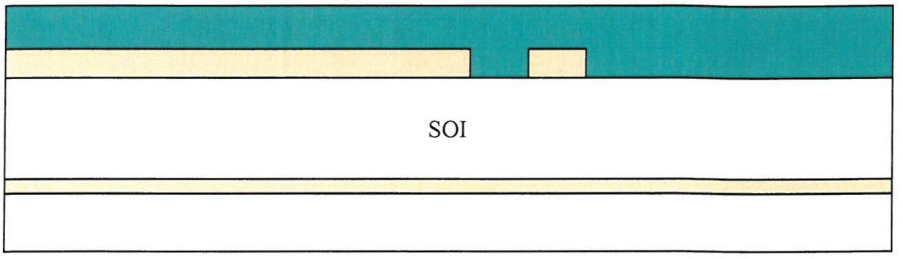
The lateral HBT fabrication process is illustrated in figure 7.2, and is based on the SOI cavity process desribed in section 4.4. The lateral HBT is fabricated on 100 mm silicon on insulator (SOI) wafers which has a buried oxide thickness of 400 nm and an active layer of 2 μm thick and is orientated to the {1 0 0} plane. The layer is p-type with a resistivity of ~15 $\Omega.cm^{-2}$. The fabrication begins with the deposition of a 300 nm thick LTO/nitride/LTO sandwich layer. This is then densified at 980°C for 20 minutes in nitrogen. Part of the oxide layer is then dry etched (figure 7.2(a)). This defines the base contact window and self-aligns it to the edge of the device cavity. A blanker layer of silicon nitride is then deposited (figure 7.2(b)) and dry etched leaving nitride fillets (figure 7.2(c)). The nitride fillets plug the base contact window and protects the epitaxial layer from being etched later in the process but are later removed prior to making base contact. With the oxide and nitride fillet acting as a hard mask, the exposed silicon layer is then dry etched, creating a vertical silicon sidewall. The silicon layer is then etched back 500 nm using a KOH solution (figure 7.2(d)). This will take approximately ~150 seconds at an etch rate of 20 nm/min. As the etch-back takes place, any ripples that are present on the silicon sidewall are removed leaving a silicon surface that is smooth (see section 4.5.2) and suitable for epitaxy growth. Selective epitaxial growth is then carried out using the DCS / SiH_4 / H_2 process.

Growth is carried out at 850°C, 1 Torr with a DCS : SiH_4 : H_2 gas ratio of 10 : 10 : 100 sccm. This is based on the process established in section 6.2.3. During epitaxial growth, the base and collector regions of the transistor are defined (figure 7.2(e)). The proposed

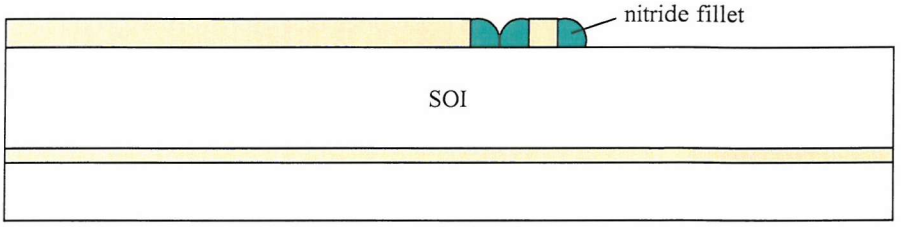
scheme for the SiGe base and collector region is illustrated in figure 7.3. The total width of the base is 100 nm. This consists of a p^+ SiGe base that is 60 nm wide, with intrinsic SiGe spacers that are each 20 nm wide. The spacers are put in to buffer any out diffusion of boron from the p^+ SiGe base. The base is to be doped *in situ* p-type to a concentration of $\sim 5\times10^{18}$ cm^{-3} with a germanium concentration of 10%. Unlike the base, the 100 nm wide collector region is doped *ex situ*. This is done by depositing a blanket layer of n^+ polysilicon with a concentration of $\sim 5\times10^{19}$ cm^{-3} and then annealing at 1000°C in N_2 for 20 minutes. This anneal causes out diffusion of phosphorus from the polysilicon into the intrinsic emitter region making it n-type and forming a junction with the boron doped base. The polysilicon layer is then patterned and dry etched (figure 7.2(f)). A selective nitride etch is carried out to remove the plug covering the base contact window. A layer of p^+ polysilicon is then deposited and patterned, and this becomes the extrinsic base contact (figure 7.2(g)). Next, the collector contact window is opened by dry etching and the exposed areas are implanted n^+ to a concentration of 1×10^{20} cm^{-3}. Metal (Al + 1% Si) is then deposited and patterned to allow contact to be made to the collector and emitter regions of the transistor. This is followed by a thin oxide deposition stage to isolate the collector and emitter contacts. Metal is again deposited and patterned to make contact to the base of the transistor. The final device structure is shown in figure 7.2(i).



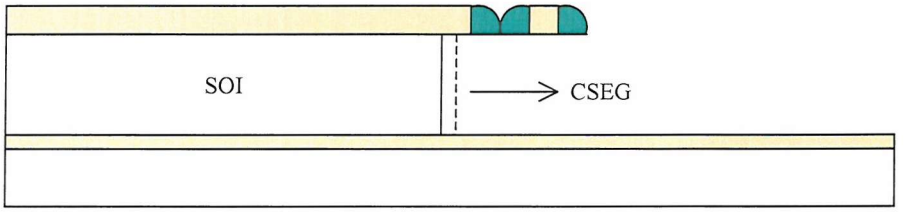
(a) LTO deposition and patterning.



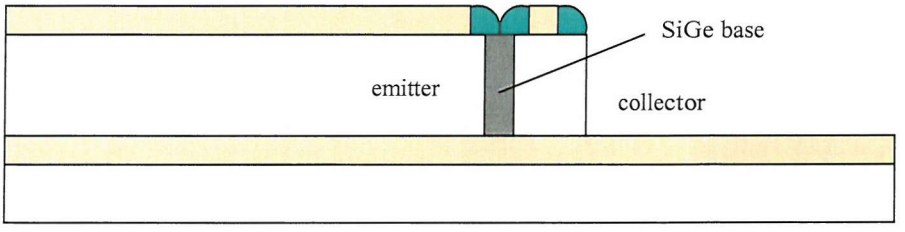
(b) Silicon nitride deposition



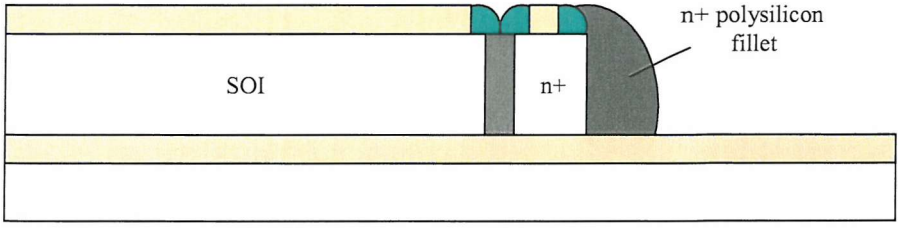
(c) Blanket dry etch of silicon nitride.



(d) Etch back of SOI by wet etch.

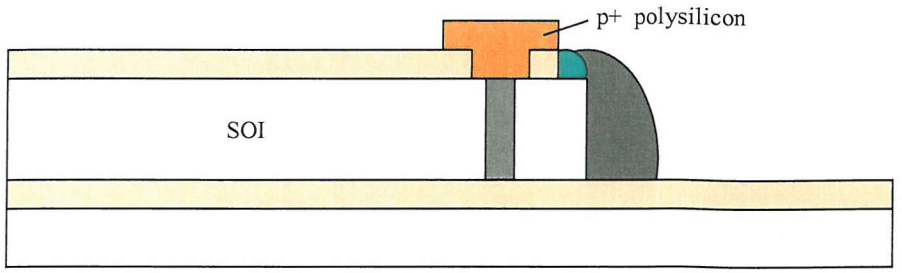


(e) Confined lateral selective epitaxial growth by DCS / SiH_4 / H_2.

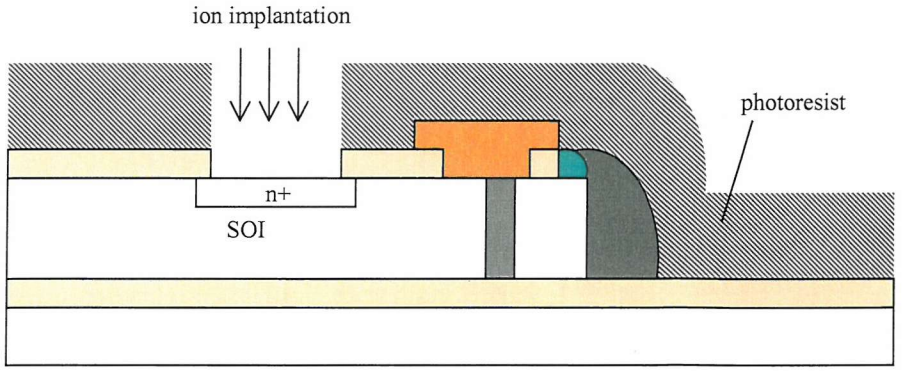


(f) n^+ polysilicon deposition followed by blanket dry etch.

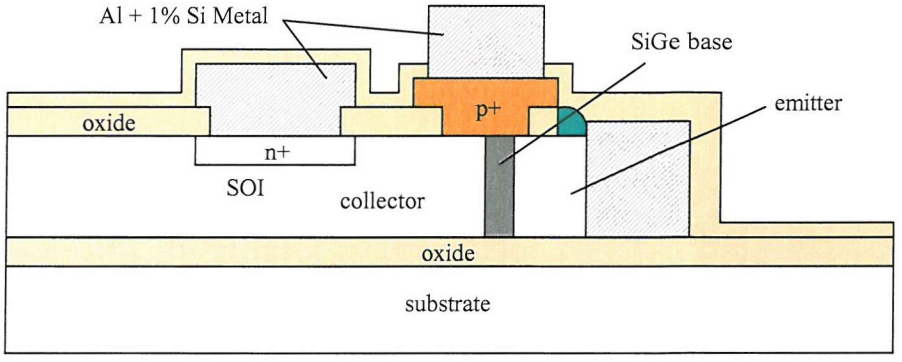
Fig. 7.2 Lateral HBT fabrication process. Continues following page.



(g) p^+ polysilicon deposition and patterning.



(h) n^+ implantation of collector area.



(i) Metallisation of collector, base and emitter.

Fig. 7.2 Lateral HBT fabrication process.

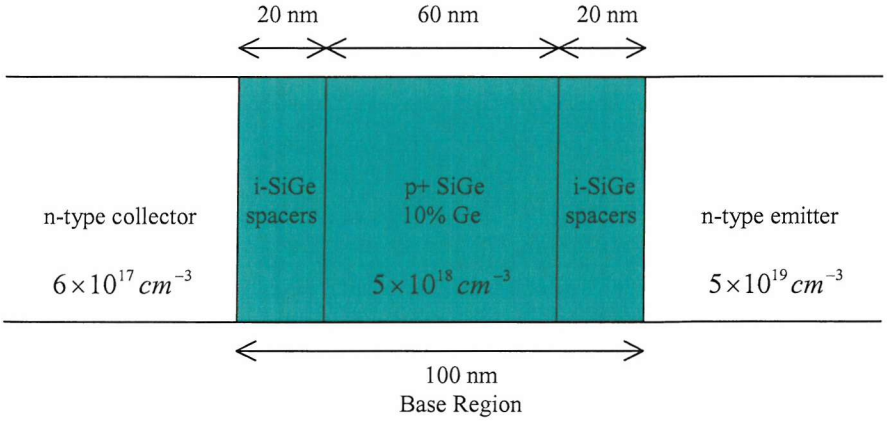


Fig. 7.3 Proposed base region of SUMC lateral HBT.

7.2 Issues concerning Lateral HBT Design

The new lateral HBT does not employ a self-aligned base contact scheme, which allows direct contact to be made to the thin lateral base. To achieve a fully self-aligned contact requires additional non-trivial processing steps and considerable development time. The first objective of this work is to demonstrate the feasibility of fabricating such a device, the next objective would be to optimise and scale device parameters.

A significant problem in lateral transistor fabrication is aligning the external base contact to the intrinsic base. The accuracy of the alignment is highly dependent upon lithography, the base resolution of which can be small (0.1 μm by e-beam direct-write), but the main limitation is the alignment tolerance (~0.5μm). This effectively means that direct contact to the thin base is very difficult. This problem can be overcome by enlarging the base contact window to take into account alignment tolerance, but, can lead to considerable degradation in transistor performance. In the transistor design proposed in this work, alignment tolerance of the external base contact is minimised by by defining both the base contact window and the cavity area on the same mask. With this scheme, emphasis is placed on accurately determining the position of base region during the epitaxial growth. The lateral epitaxial growth rate has been found to be ~17 nm/min, which is sufficiently slow to allow precise positioning of the base to be made. However, this can only be achieved if the etch back distance can also be determined accurately. As the etch-back rate using KOH is ~18 nm/min, it is also sufficiently controllable to allow precise etch-backs to be made.

One of the consequences of not using a self-aligned method for positioning the base contact is the need to have a base contact window that is larger than the actual base. In the design of the SiGe HBT, polysilicon is used to make contact to the base. By using an extrinsic p^+ polysilicon base contact, a retarding electric field to the minority carrier electrons is created, ensuring low base current. It also ensures that the collector and emitter regions are not in direct contact and allows transistor action to be maintained.

In the design of the lateral transistor, the base region is doped *in situ* while the collector region is doped *ex situ*. Ideally, both regions should be doped *in situ*. However, a

selective *in situ* n-type epitaxy process capable of ~1μm of lateral growth is still in development and not available at the time of writing. Therefore, the design of the transistor assumes the epitaxy growth of the emitter is carried out undoped. One of the drawbacks of *ex situ* doping is the need for annealing to drive in the dopants from the polysilicon in to the collector. These unfortunately will also cause the out diffusion of boron from the base region. This is further exacerbated by the fact that boron is a light dopant and diffuses easily. This is expected to degrade performance but will still maintain transistor action, as shown from simulation.

7.3 Lateral SiGe Heterojunction Bipolar Transistor Simulation

In this section, the performance of the proposed lateral bipolar transistor is evaluated through simulation. The simulation was carried out using Silvaco ATLAS, a semiconductor device simulation package. The simulation listing and device cross-section can be found in appendix C.

Figure 7.4 shows the doping profile of the device used in the simulation. An initial flat doping profile was used for the collector ($1.0\times10^{17}\,cm^{-3}$), base ($5\times10^{18}\,cm^{-3}$) and n^+ polysilicon emitter contact ($5\times10^{15}\,cm^{-3}$). An anneal was then carried out to simulate the diffusion of phosphorus from the polysilicon emitter contact to the intrinsic base. This was carried out at 950°C for 30 minutes. This time was found to be just sufficient to allow the dopants from the n^+ polysilicon emitter to diffuse towards the base and form a junction. Unfortunately, this anneal also causes the out diffusion of boron from the base. The effect of this anneal is the enlargement of the effective base from 100 nm (including spacers) to 250 nm.

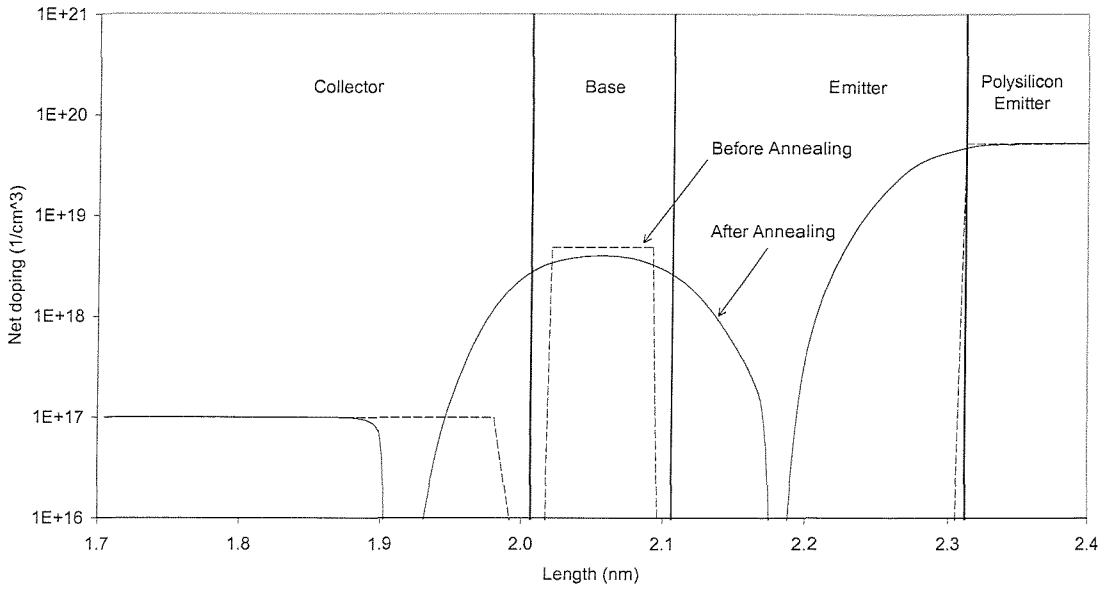


Fig. 7.4 Doping profile of the proposed lateral device before annealing and after annealing at 950°C for 30 minutes.

7.3.1 Results and Discussion

In this work, f_t and f_{max} are used as figures of merit to assess the performance of the device. In the simulation, these figures were extracted using y-parameters from which frequency admittance matrices can be calculated (i.e. Y_{11}, Y_{12}, Y_{21}, Y_{22}). From this, the device a.c. gain and power gain are calculated using [116],

$$\beta_{ac} = 20\log\left|\frac{Y_{21}}{Y_{11}}\right| \tag{7.1}$$

where β_{ac} is a.c. gain and using [116],

$$\text{a.c. power gain} = 10\log\left(\frac{\mathrm{Re}(Y_{21}-Y_{12})^2 + \mathrm{Im}(Y_{21}-Y_{12})^2}{4\left(\mathrm{Re}(Y_{11})\,\mathrm{Re}(Y_{22}) - \mathrm{Re}(Y_{12})(Y_{21})\right)}\right) \tag{7.2}$$

From these two equations, the device peak f_T and f_{max} are obtained at the point where a.c. gain and unity a.c. power gain are zero, respectively.

Figure 7.5(a) shows the simulation results of the proposed lateral heterojunction bipolar

transistor. The graph shows the variation in the device f_T and f_{max} with collector current. The plot shows that the device has a maximum f_T of 2.0 GHz and an f_{max} of 8.0 GHz, and this occurs at a peak collector current of 0.9 mA. Figure 7.6 shows a Gummel plot of the device. From this, the current gain of the device is found to be 16.6.

The simulation results show that the transistor design gives a functional device. However, the figures for f_T and f_{max} are somewhat low compared to other lateral homojunction devices, as current optimised lateral homojunction bipolar transistor can achieve an f_T of 20 GHz with collector currents of 15 mA [14]. On reason for this is the large base that is formed by the out diffusion of boron, which is in turn, a consequence of the long anneal step for the phosphorus drive-in. This anneal step can be removed if both the base and emitter region can be doped *in situ*. Although such a process is currently unavailable, it is hoped that a selective *in situ* doped process will be developed in the near future. To have an idea of the possible performance gain that can be achieved from a device with a similar physical structure but sharp doping profiles, the simulation was repeated but with a doping profile that is similar to that before the anneal (see figure 7.4).

Figure 7.5(b) below shows the simulation result of the *in situ* doped device. The graph shows that the device has a maximum f_T of 6.3 GHz and an f_{max} of 15.8 GHz, which is a 3.1× and 2× improvement, respectively, over the proposed device. The device also has a peak collector current of 0.86 mA at maximum f_{max}, which is similar to the proposed device. This improvement comes from the use of *in situ* doping, which minimises the out-diffusion of boron. From the doping profile shown in figure 7.4 the use of *ex situ* doping enlarges the base from ~100 nm to ~250 nm. From the simulation results, the devices' base resistance, R_b and collector base junction capacitance, C_{jbc} was extracted using the formula [117],

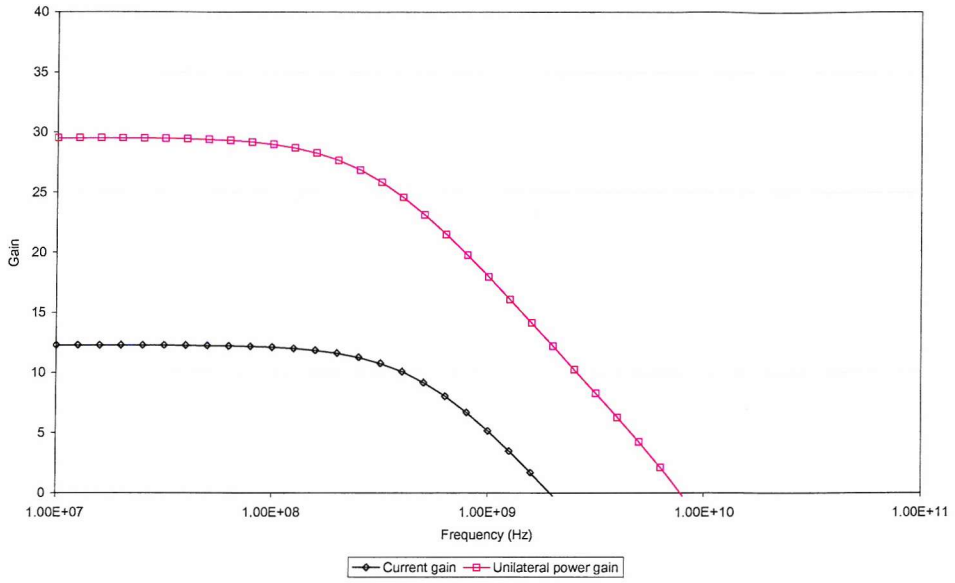
$$R_b = \mathrm{Re}(Z_{11} - Z_{12}) \tag{7.3}$$

and [117],

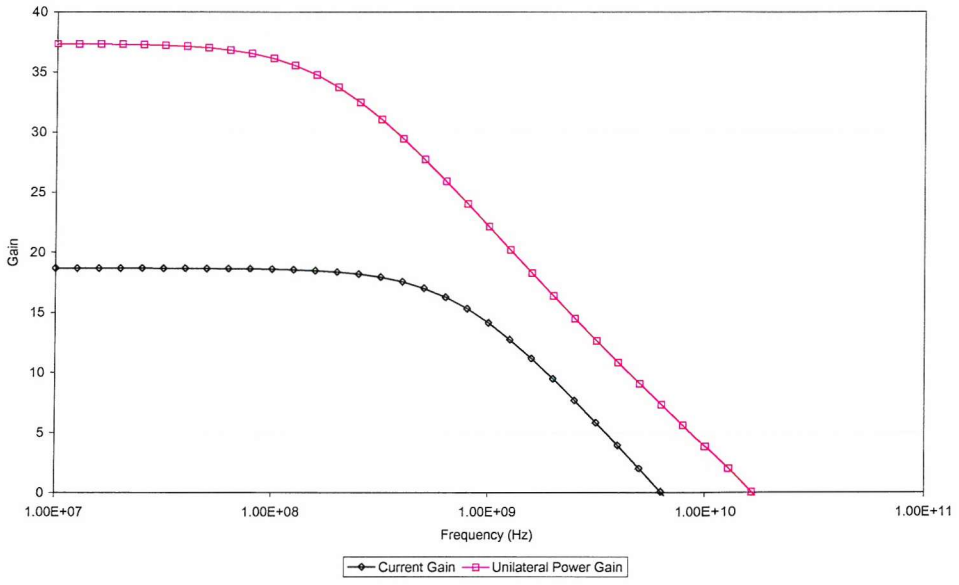
$$C_{jbc} = \frac{-1}{\omega\,\mathrm{Im}(Z_{22} - Z_{21})} \tag{7.4}$$

where Z_{11}, Z_{12}, Z_{21} and Z_{22} are two port Z-parameters. For the proposed device, R_b and C_{jbc} were found to be 600 Ω and 1.37 fF, respectively at peak f_{max}. In comparison, the improved design has an R_b and C_{jbc} of 490 Ω and 1.55 fF, respectively at peak f_{max} which means, R_b is reduced by 19% while C_{jbc} is increased by 13%. From this it can be concluded that one of the factors which contribute to the increase in f_{max} is the reduction in R_B. In addition, the increase in f_{max} also comes from a reduction in the base transit time due to the narrower base of the *in situ* doped device. From equation 2.7, the base transit time of the *in situ* doped device is reduced ~2.5× compared to the *ex situ* doped device due to the reduction in base width from 250 nm to 100 nm. It is therefore, not unexpected that the *in situ* doped device has a figure of f_{max} that is double of the *ex situ* doped device. In both of the devices, the value of C_{jbc} does not vary significantly, which is expected as the collector-base junction area of both devices remains largely the same regardless of the doping method.

Further improvement in device performance in the form of lower collector current and higher f_{max} can be found by reducing the thickness of SOI layer. A reduction in SOI thickness from the present 2.0 μm to 0.5 μm results in a device with an f_T of 9.8 GHz and f_{max} of 30 GHz, and a peak collector current of 0.66 mA. This reduction in collector current is due to smaller collector area (i.e. 2.0 ×0.5 μm^2) as compared to the proposed device (i.e. 2.0 × 2.0 μm^2), highlighting the advantages of thinner SOI.

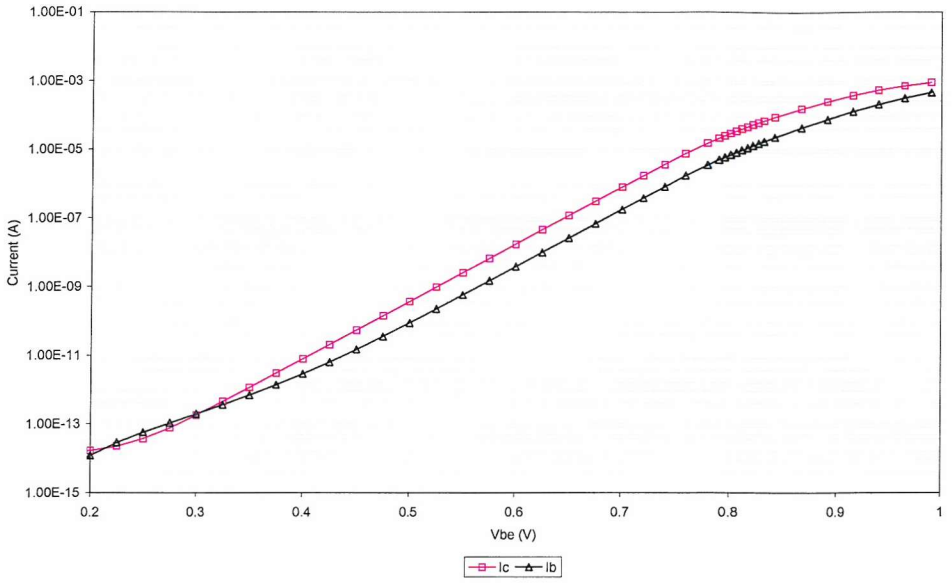


(a)

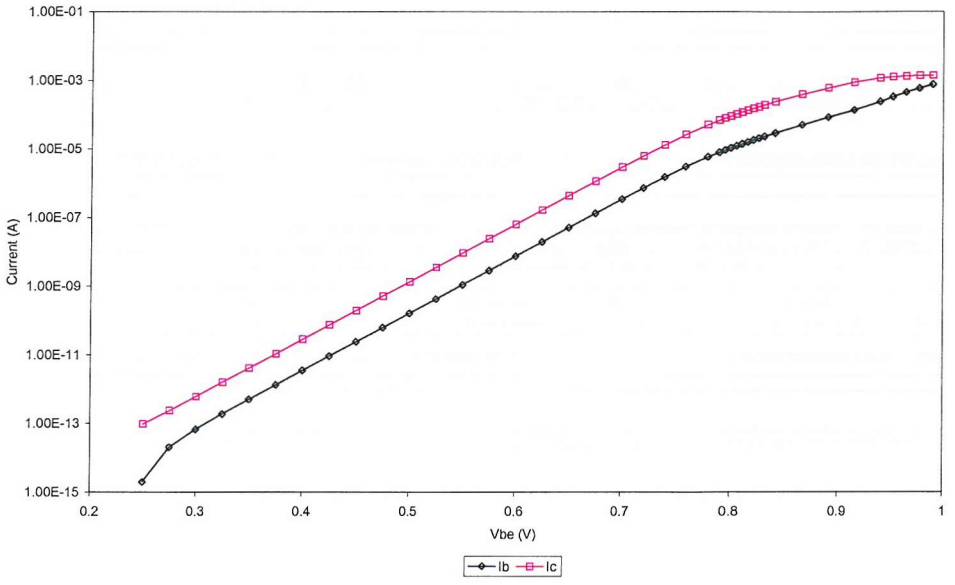


(b)

Fig. 7.5 Variation in f_T and f_{max} with collector current of lateral device with (a) *ex situ* collector, base and emitter doping (b) *in situ* collector, base and emitter doping.



(a)



(b)

Fig. 7.6 Gummel plot of lateral device with (a) *ex situ* collector, base and emitter doping (b) *in situ* collector, base and emitter doping.

7.4 Conclusion

In this section, a lateral SiGe heterojunction bipolar transistor is proposed, the design of which is based on the lateral selective epitaxial growth process using DCS / SiH_4 / H_2 developed at the fabrication facility. The design requires an *in situ* doped p-type SiGe

selective epitaxial growth process to be developed, which is needed to form the base region of the lateral transistor. For the emitter, the design employs an *ex situ* doping method which uses diffusion from a highly doped polysilicon emitter. The simulation results have shown that the proposed lateral SiGe heterojunction bipolar transistor gives a functional device with an f_T and f_{max} of 2.0 GHz and 8.0 GHz, respectively. In order to improve the performance of the device, an *in situ* doped selective epitaxial process has to be developed. From simulations, the use of *in situ* doping to form the active regions of the transistor has been found to result in an increase in device performance, with an f_T and f_{max} of 6.3 GHz and 15.8 GHz, respectively. Further improvement in device performance can be achieved by simply reducing the thickness of the SOI layer from 2.0 μm to 0.5 μm. This results in an enhancement in f_T and f_{max} to 9.6 GHz and 30 GHz, respectively. Currently, SOI wafers with silicon active layers of less than 50 nm are commercially available (SIMOX-SOI), and the use of such wafers could potentially improve the performance of the lateral HBT even further.

Chapter 8

Conclusion and Future Work

The objective of this work was to develop fabrication techniques and processes suitable for the fabrication of lateral heterojunction bipolar transistors by confined lateral selective epitaxial growth. The two most challenging fabrication aspects were the development of processes suitable for the fabrication of cavity structures and the development of selective epitaxy techniques suitable for the growth of devices.

In order to achieve lateral epitaxial growth vertical growth has to be restricted and this is best achieved by creating cavity structures. The first part of the work was primarily concerned with the design and process development required for cavity fabrication. This work has led to the successful fabrication of two types of cavity, the "open-sided cavity" and the "SOI cavity". Open-sided cavities allow confined lateral growth to be established from a planar silicon seed window, while the SOI cavity provides a vertical seed from which lateral growth can develop directly. Initial work using "test" cavity structures showed that rigid cavities could be fabricated if the walls of the cavity are made from an LTO/nitride/LTO sandwich layer. In addition, etching of the polysilicon or silicon sacrificial layers, which is required to form a cavity, can be carried out using both dry (SF_6) and wet (KOH) methods, however, the latter has a tendency to cause stiction for larger sized cavities. Similarly, warping of the cavity ceiling, a problem that affected most cavities, can be minimised by reducing the overall size of the cavity. For SOI cavities, a sidewall rippling reduction process using KOH is necessary to form a

smooth sidewall seed that is suitable for epitaxial growth. Open sided cavities of 50 μm in length and SOI cavities of 8 μm depth have been fabricated successfully. Although these large cavities can be fabricated by the processes developed in this work, smaller cavities <5 μm are preferred for lateral HBT fabrication as these are more robust to dry and wet fabrication processes and in any case large enough for good device performance.

The development of a confined lateral selective epitaxial growth process began with an examination of a selective silane-only epitaxy processes, which had been developed at the fabrication facility. Results showed growth at 980°C, at a pressure of 0.5 Torr with a silane ratio of 10 sccm, provided good quality epitaxial layers. Epitaxial growth was also found to be selective but limited to an incubation period of about 30 minutes. Growth carried out for this length of time gave vertical epitaxial growths of up to 840 nm (i.e. growth rate ~28 nm/min) but only a lateral epitaxial overgrowth of 500 nm (i.e. growth rate ~18 nm/min). Long growths using silane-only were also found to cause severe oxide undercutting and oxide pitting, a result of the high growth temperature. Due to the limitations of the silane-only process (i.e. short incubation period, high growth temperature and oxide degradation), along with the lack of a suitable selective silicon germanium epitaxial growth process resulted in the development of an alternative selective epitaxial process based on Si-Cl chemistry.

The new DCS/SiH_4/H_2 process uses the dichlorosilane as a means of controlling selectivity, allowing silicon and silicon germanium epitaxial layers to be grown at lower temperatures. By varying the silicon to chlorine ratio, growth can be moved between deposition and etching. The balance between silicon growth and etching of polysilicon on oxide, resulting in selective epitaxial growth, was found when the DCS : SiH_4 : H_2 gas ratio is 10 : 10 : 100 sccm. However, selectivity was found to be restricted by an incubation period, as in the silane only epitaxy process. Results show that the incubation period is ~90 minutes for growth at 850°C. The DCS / SiH_4 process was found to give good quality epitaxial layers at and above 850°C. However, a DCS / H_2 prebake stage is required prior to growth to ensure consistently good epitaxial layers. Arrhenius data show the process to have an activation energy of 2.4 eV, which is similar to other dichlorosilane based epitaxy process at similar pressures (i.e. ~1 Torr). Results show that growths that, at 850°C, produce layers with good uniformity (i.e. +/-

5%) and are insensitive to local loading effects. Selective vertical growth of 1.6 μm and lateral growth of 500 nm have been demonstrated from planar seed windows. The slow lateral growth rate is attributed to the slow growing {3 1 1} and {1 1 1} facets which develop during growth from a planar seed. Relatively slow growth on the {3 1 1} and {1 1 1} facets combined with selectivity loss after ~90 minutes will reduce device dimensions to less than 1 μm.

To overcome this problem, lateral growth was attempted from a {1 0 0} sidewall seed, prepared using SOI wafers. Theoretically this should result in growth similar to that from a horizontal seed. Using this scheme, confined lateral epitaxial growth of up to 1.5 μm has so far successfully been carried out in the SOI cavities. However, the lateral growth rate was found to be 17 nm/min, 50% less than the vertical growth rate. The reduction in growth rate has been attributed to the roughness of the sidewall surface, which is a result of the SOI preparation process. Fortunately, some development experiments have shown that ripples on the silicon sidewall can be removed using a KOH etch to provide a smooth surface that is suitable for epitaxial growth.

Besides silicon epitaxial growth, selective SiGe layers have also successfully been grown using a DCS / SiH_4 / GeH_4 / H_2 process at 850°C. The germanium content is estimated to be between 5% and 10%.

Based on the process developments outlined in this work, a realisable lateral SiGe bipolar transistor device has been proposed. The new device structure is based on processing and epitaxy techniques developed in this work (the only process that remains to be established is the p-type doping of the SiGe base). The proposed lateral device uses a non-self aligned base contact and an *ex situ* doped emitter region. With a germanium content of 10%, and a collector, base and emitter doping concentration of 1×10^{17} cm^{-3}, 5×10^{18} cm^{-3} and 5×10^{19} cm^{-3} simulation of the device predicts an f_T of 1.5 GHz and an f_{max} of 8.0 GHz at a peak collector current of 1.2 mA.

If, as expected, the base and emitter regions can be doped *in situ* during selective epitaxial growth, the lateral device proposed could achieve an f_T of 6.3 GHz and an f_{max} of 15.8 GHz. These simulations show levels of performance that can be achieved with relatively minor developments to the epitaxy growth processes developed in this work.

With further development in the epitaxy growth process and transistor design and scaling, significant gains in performance are expected.

8.1 Future Work

The results of the DCS / SiH_4 / H_2 selective epitaxial growth process indicate a very flexible and important new epitaxy regime, however there is still a great deal more to be learned about the system. Further, detailed growths and analysis would allow the development of processes with improved selectivity and better epitaxial quality to provide longer lateral growth at lower temperatures. These developments can be achieved by having a greater understanding of the effect of temperature, pressure and gas flow ratios on epitaxial growth. These three factors strongly influence epitaxial growth and optimising these factors should allow better layers to be grown.

Another important aspect of growth that requires development is *in situ* doping, including n-type doping of the silicon collector and emitter regions and p-type doping of the SiGe base. Of these the p-type doping of the SiGe is crucial to the overall device process, (n-type doping of the collector and emitter is not crucial but would be very beneficial). So far only undoped growth has been carried out. Recent experiments, not reported in this work, on *in situ* p-type doping have produced only non-selective growth. The parameter-space study outlined above, allowing optimisation of the process conditions should help to establish the most suitable process conditions for p-type SiGe doping. The advantages of having an *in situ* doped selective epitaxial process is advantages as it will simplify the lateral device fabrication process by allowing the collector, base and emitter transistor regions to be defined in one single growth. This will reduce the number of fabrication steps and also cost.

This work has also highlighted a disadvantage of carrying out lateral epitaxial growth from a vertical (i.e. sidewall) seed which is sidewall rippling. Although several methods have been proposed to reduce this rippling and create an epi-ready surface, it may be more feasible to achieve lateral growth from a traditional horizontal seed. It has been shown by Bradbury *et al.* [64] that an important factor in achieving this is finding

a suitable silicon to chlorine gas ratios which will give a fast lateral growing facet. Again, the parameter space study would help in giving an insight into this work. If lateral growth in this manner can be achieved, it would allow cheaper standard wafer substrates to be used instead of the more expensive silicon on insulator wafers.

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Appendix A

Publications

K. Osman, N. S. Lloyd, J. S. Hamel, J. M. Bonar, H. A. Kemhadjian, D. M. Bagnall, "Confined Epitaxial Growth using Silane by Low Pressure Chemical Vapour Deposition," The 4th International Conference on Materials for Microelectronics and Nanoengineering (MFMN 2002), 10 -12 June 2002, Hanaasari Cultural Centre, Espoo, Finland.

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Appendix B

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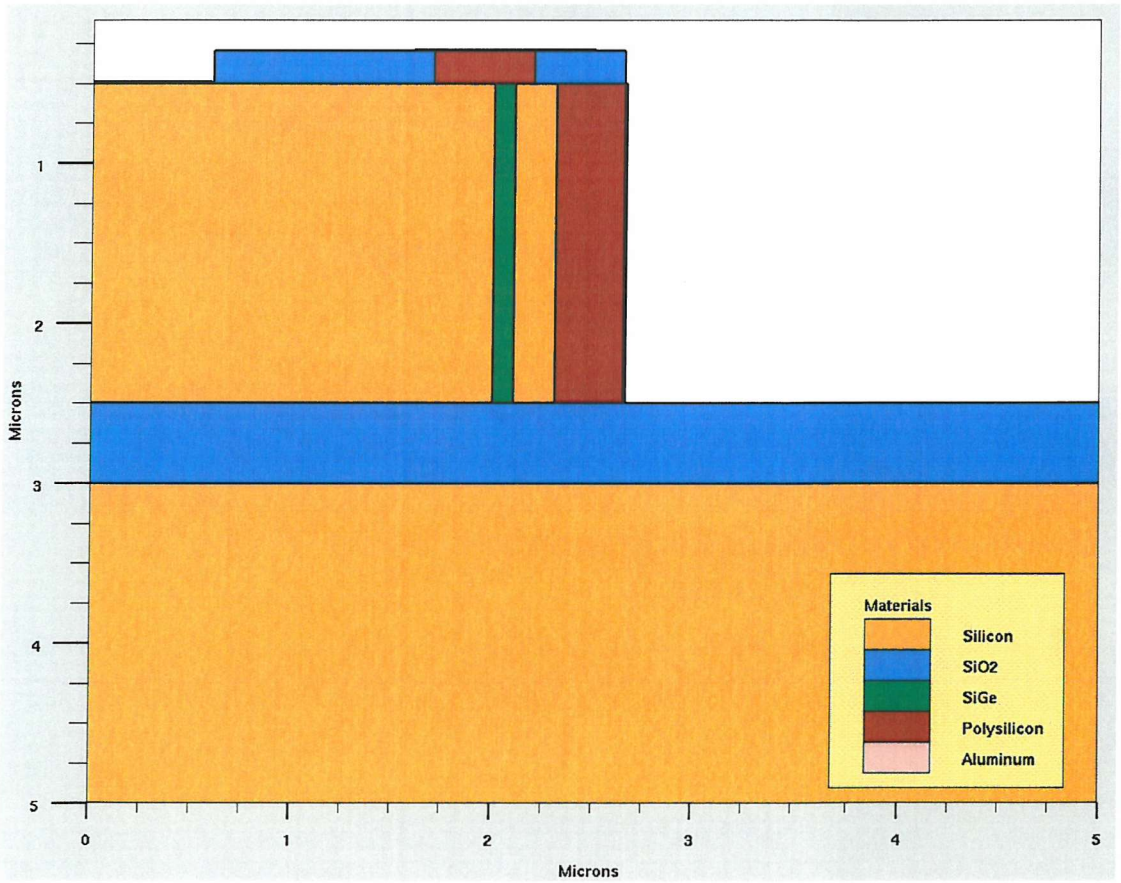
Appendix C

Simulation

Simulation input file and device cross-section.

```
go atlas
#
mesh infile=sige_hbt_3b.str

# Define model
material material=Si taun0=1e-7 taup0=1e-7
material material=SiGe taun0=1e-8 taup0=1e-8
models bipolar bgn print

# Initial solution
output con.band val.band
solve init

# Define method
method newton trap autonr

# Calculate Gummel Plot and AC parameters at 1MHz
solve prev

# 3 - collector  2 - base  1 - emitter
log outf=sige_hbt_3b_1.log

solve  vemitter=0  vbase=0.0  vcollector=0  vstep=0.1  vfinal=1.9
name=collector ac freq=1e6
solve  vemitter=0  vbase=0.0  vcollector=2  vstep=0.025  vfinal=0.7
name=base ac freq=1e6
save outf=sige_hbt_3b_2.str
solve  vemitter=0  vbase=0.72  vcollector=2  vstep=0.02  vfinal=0.78
name=base ac freq=1e6
solve  vemitter=0  vbase=0.79  vcollector=2  vstep=0.005  vfinal=0.83
name=base ac freq=1e6
solve  vemitter=0  vbase=0.84  vcollector=2  vstep=0.025  vfinal=1.0
name=base ac freq=1e6

# Frequency domain AC analysis up to 100 GHz
load inf=sige_hbt_3b_2.str master
log  outf=sige_hbt_3b_3.log  z.param  y.param  gains  inport=base
outport=collector

solve vemitter=0 vbase=0.8 vcollector=2 ac freq=1e7 fstep=1.258925412
mult.f nfstep=50

#  Extraction of parameters
extract init inf="sige_hbt_3b_1.log"

# Maximum cutoff frequency
extract name="Ft_max" max(g."collector""base"/(6.28*c."base""base"))

# Base bias at maximum cutoff frequency
```

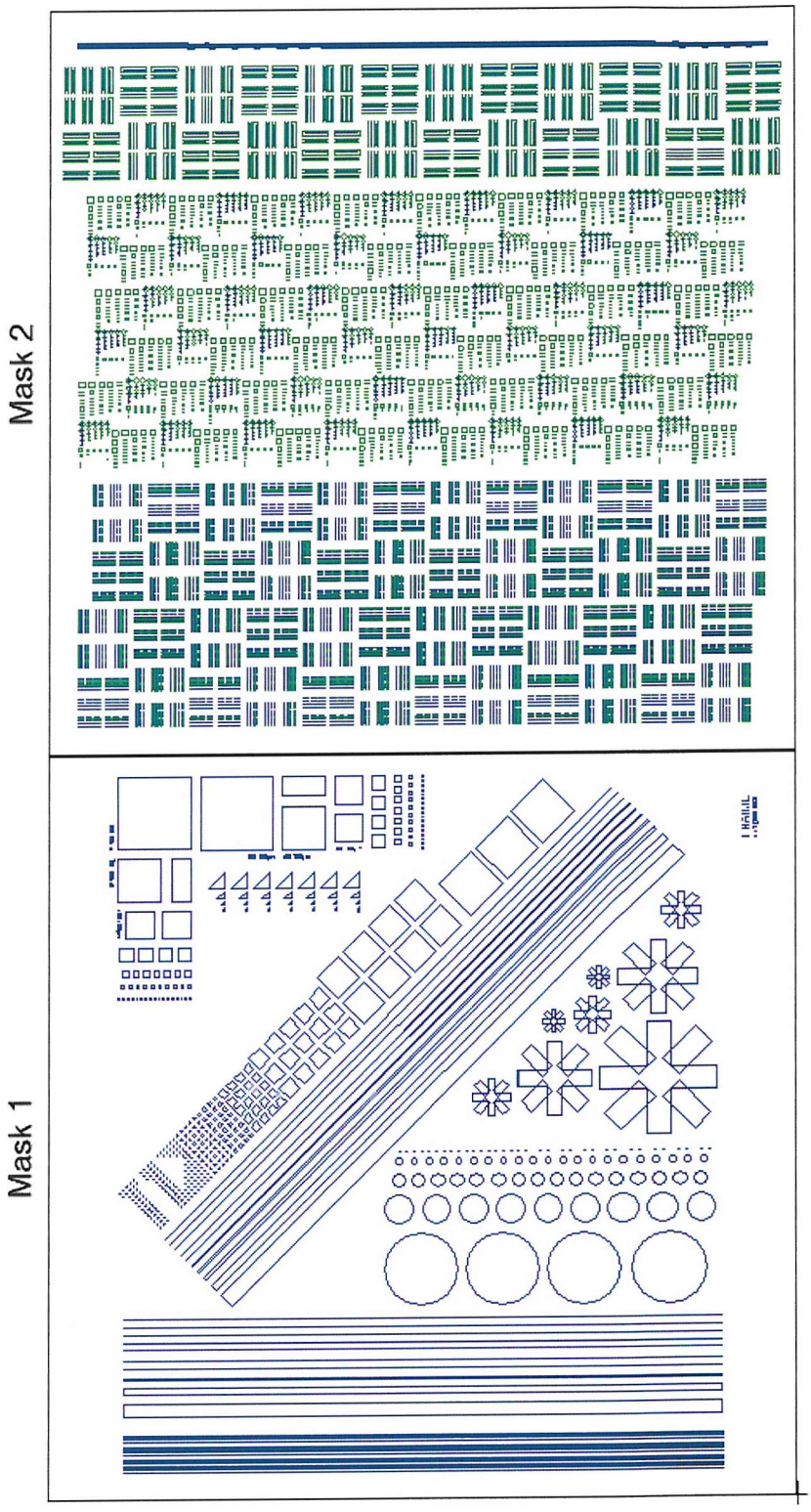
```
extract     name="Vbe@Ft_max"     x.val     from     curve     (v."base",
g."collector""base"/(6.28*c."base""base" )) where y.val=$"Ft_max"

# Input (base) capacitance at maximum cutoff frequency
extract     name="Cbb@Ft_max)"     y.val     from     curve     (v."base",
abs(c."base""base" )) where x.val=$"Vbe@Ft_max"

# Transconductance at maximum cutoff frequency
extract     name="Gm@Ft_max)"     y.val     from     curve     (v."base",
abs(g."collector""base" )) where x.val=$"Vbe@Ft_max"

# Peak other parameters
extract             name="peak             collector             current"
max(curve(abs(v."base"),abs(i."collector")))
extract name="peak gain" max(i."collector"/i."base")

# Gummel plot
tonyplot  sige_hbt_3b_1.log -set hbtex06_1_log.set

# AC current gain versus frequency
tonyplot  sige_hbt_3b_3.log -set hbtex06_4_log.set

quit
```



sige_hbt_3b.str

Appendix D

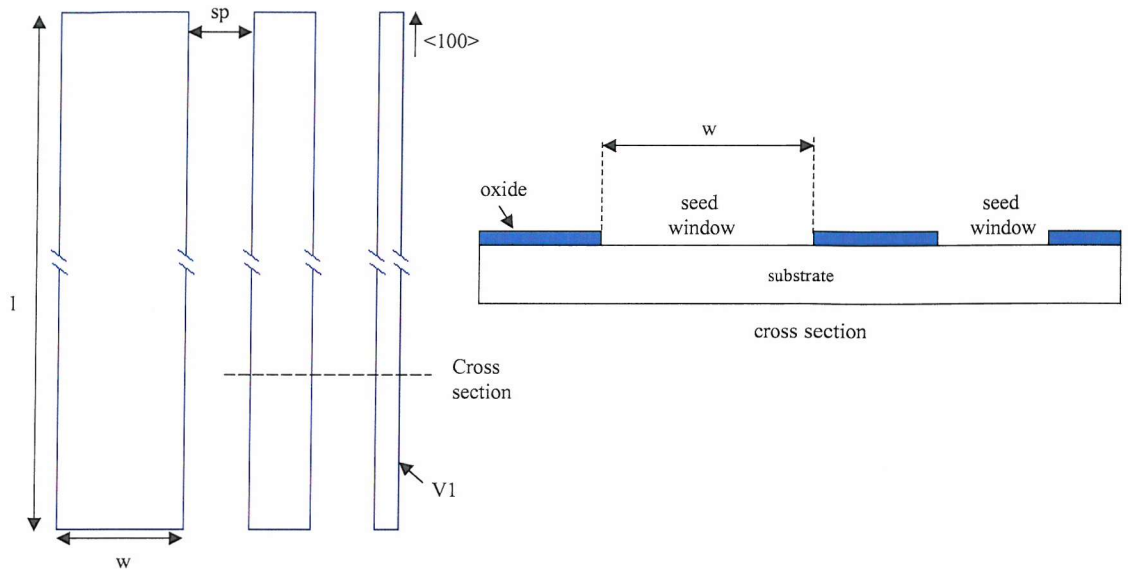
Cavity Mask and Design



Mask 1

Structure group 1A & 1B: Rectangular Seed Windows

These structures are oriented along the <110> direction.



Structure group 1A

w (um)	sp (um)
10	10, 5, 3, 2, 1, 0.5
5	as above
2	as above

l = 4000um

Structure group 1B

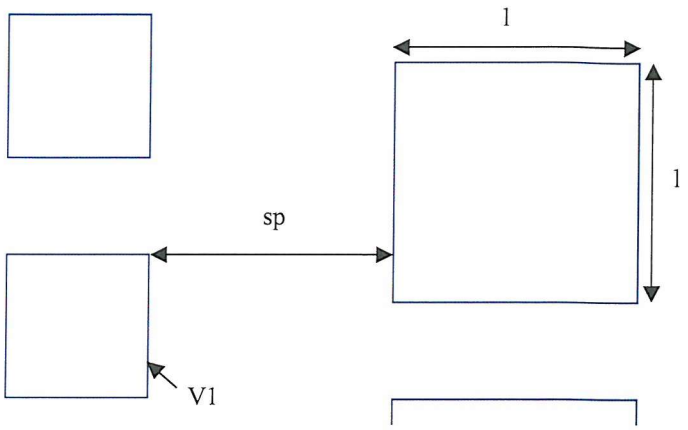
w (um)	sp (um)
100, 50, 20, 10, 5, 3, 2, 1, 0.75, 0.5	50

l = 4000um

Structure group 1C: Rectangular Seed Windows

These structures are similar to 1B but oriented along the <100> direction. Width, *w* and spacing, *sp* are similar to that of structure 1B.

Structure group 1D: Square Seed Windows

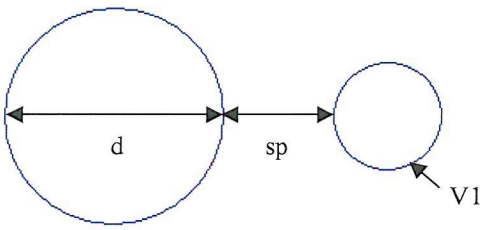


l (um)	sp (um)
500, 300, 200, 100, 50, 30, 20	40
10, 5, 2, 1, 0.75, 0.5	30

Structure group 1E: Square Seed Windows

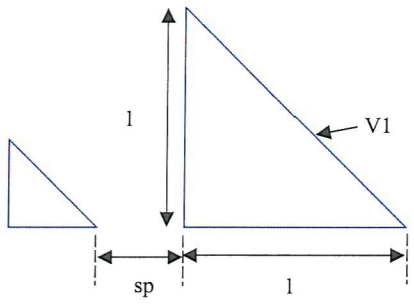
These structures are similar to 1B but oriented along the <100> direction. Width, *w* and spacing, *sp* are similar to that of structure 1B.

Structure group 1F: Circular Seed Windows



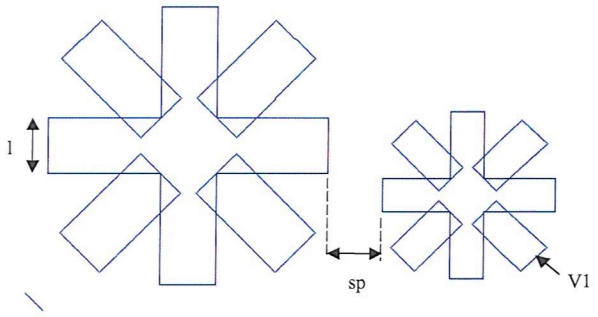
d (um)	sp (um)
500, 200	50
100, 50, 20, 10	30

Structure group 1G: Triangular Seed Windows



l (um)	sp(um)
100, 50, 20	20
10, 2 , 1	10

Structure group 1H: Star Seed Windows



l (um)	sp (um)
150, 50, 30	50 min.

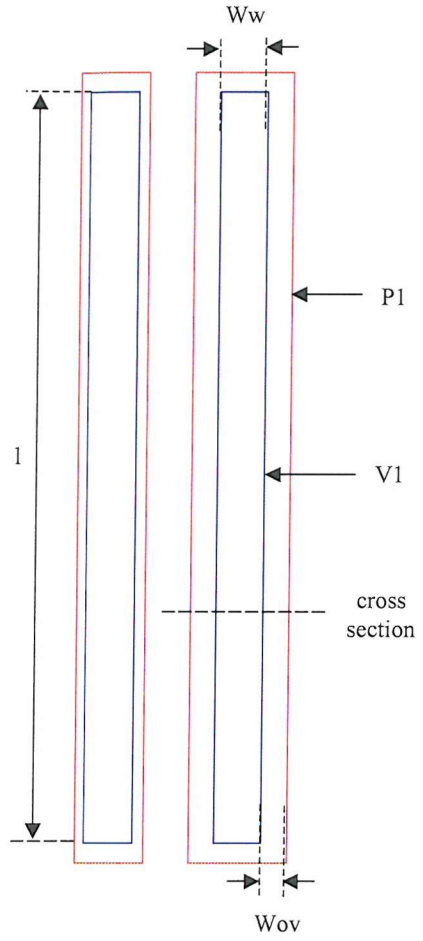
Mask 2

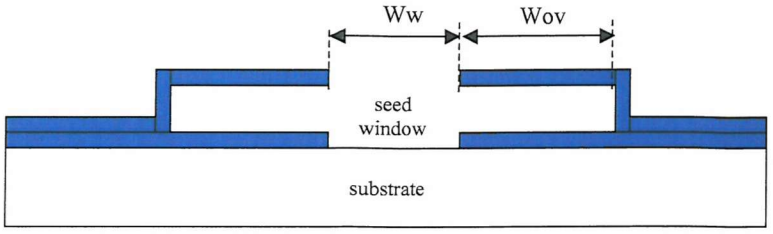
These structures will be used to look at:

- Unconfined selective epitaxial growth (SEG) – using oxide step structures.
- Confined selective epitaxial growth (CSEG) – using simple cavities.
- Epitaxial quality of CSEG at silicon/oxide interface of epitaxy/cavity.
- Mechanical strength of cavity.

Structure group 2A: Test Cavities

These structures are long rectangular cavities. These are oriented along the <110> direction.





Cross section

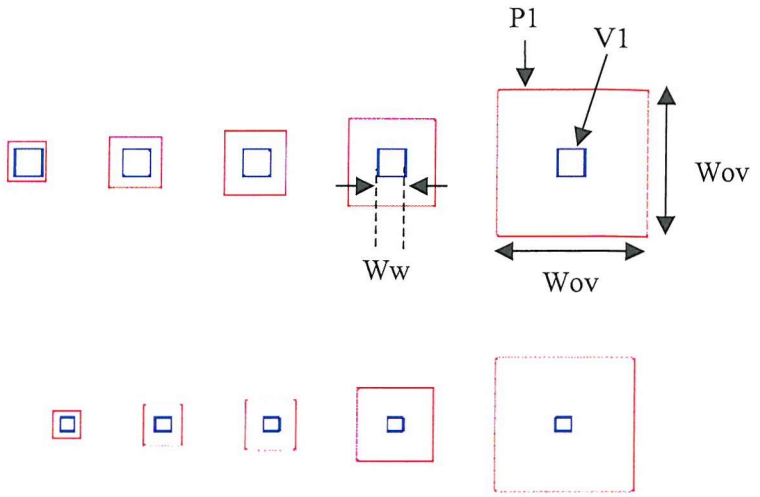
Legend:

P1 – polysilicon mask
V1 – seed window mask

w_{ov} (um)	l (um)	w_w (um)
2	50, 160	2
2	50, 160	5
2	50, 160	10
5	50, 160	2
5	50, 160	5
5	50, 160	10

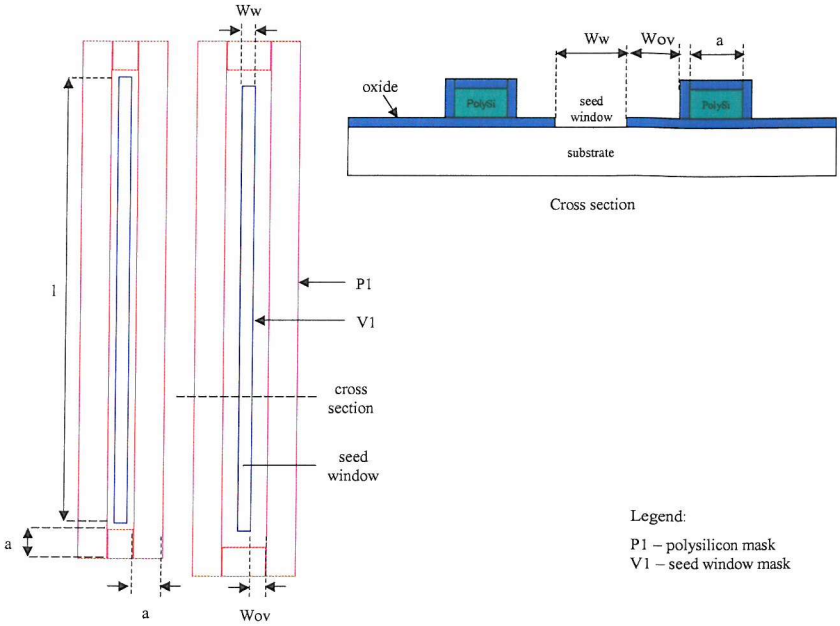
l = 152um and 42um

Structure group 2B: Square Simple Cavities (Small)



w_w (um)	w_{ov} (um)
1	1, 2, 3, 5, 10
2	as above
3	as above
5	as above
10	as above

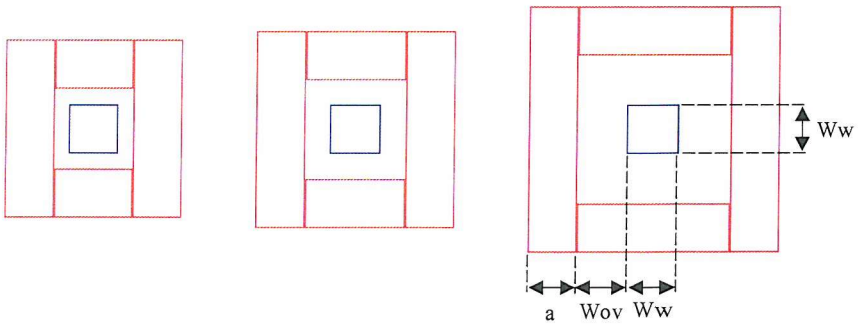
Structure group 2C: Oxide Step Structures



W_w (um)	W_{ov} (um)
2	2, 5
5	as above
10	as above

l = 152um, a = 10um

Structure group 2E: Oxide Step Structures (Small)



W_w (um)	W_{ov} (um)
10	10, 5, 3, 2, 1
5	as above
3	as above
2	as above
1	as above

Appendix E

Process Listings

See following pages for listings of each fabrication process.

K1963 – Selective epitaxy growth and epitaxial lateral overgrowth experiment

K1964 – Test cavity fabrication experiment

K2209 – Open sided cavity fabrication experiment

K2280 – SOI cavity fabrication experiment

K2484 – Silicon sidewall rippling reduction experiment

K2513 – Silicon sidewall rippling reduction using hard mask experiment

Running k1963s on 03-25-2004

	ID	Description	Count
1	G-S12	Title Page: 8 wafers, p-type, 10-30 ohm.cm	8
2	P-EM	E-BEAM Mask/Reticle Writing	2
3	G-1P	Lithography Notes	0
4	G-1	Notebook page	0
5	W-C1	* RCA clean	8
		INITIAL THERMAL OXIDATION	
6	F4-00	* Furnace 4: Load in O2: 200nm at 1000degC, 10' O2, 20' wetO2, 30' N2 WAFER 1 to 5	5
7	F4-W1	* Wet oxidation, 460+-10nm, 1100degC, 15'O2,44'wetO2,30'N2.(PNP Init ox) WAFER 6 TO 8	3
		GROW POLYSILICON AND THEN ETCH POLY (L/FIELD) ** split for wafers 4 and 5 only **	
8	W-C1	* RCA clean ** Only if A-Si deposition is not done immediately after oxidation ** WAFER 4 + 5	2
9	LP-A5	* Amorphous Si deposition: 500nm +-25nm at 560degC 10nm/min WAFER 4 + 5	2
10	P-GS1	* STEPPER Photolith: K991RW, P1, L/Field: nom. 1.1um resist STANDARD WAFER 4 + 5	2
11	G-2	* See Engineer: Inspect WAFER 4 + 5	0
12	P-RHE	* Hardbake for dry etch WAFER 4 + 5	2
13	D-SP2	Etch Poly/AmSi. Anisot. on oxides >15nm SYS90 HBr 2 step. (For LF patterns) WAFER 4 + 5	2
14	W-R2	* Resist strip, First pot Fuming Nitric acid only WAFER 4 + 5	2
15	P-RS	* Resist strip WAFER 4 + 5	2
16	X-I1	Inspect 2 wafers for residue after wet or dry etch. WAFER 4 + 5	2
		THERMAL OXIDATION (THIN LAYER)	
17	W-C1	* RCA clean WAFER 4 + 5	2
18	F4-D1	* Dry oxidation, 80nm, 1100degC. (BIPOLAR base area) WAFER 4 + 5	2
		ETCH OXIDE (All Wafers; 1 to 8)	
19	P-GS1	* STEPPER Photolith: K991RW, V1, D/Field: nom. 1.1um resist STANDARD WAFER 1 TO 8	6
20	G-2	* See Engineer: Inspect	0
21	P-RHE	* Hardbake for dry etch	6
22	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	6
23	P-RS	* Resist strip	8
24	X-I1	Inspect 12 wafers for residue after wet or dry etch.	8
		ETCH DAMAGE REMOVAL PROCESS	
25	W-C1	* RCA clean	8
26	F4-00	* Furnace 4: Load in O2: To be specified	8

Running k1963s on 03-25-2004

	1	2	3	4	5	6	ID	Description	Count
27							WH-7[	Dip etch, 7:1 BHF 25degC. To hydrophobic Si + 20secs. *see engineer*	1
28							X-0	General inspection stage	1
29							LE-0	Low Pressure Epitaxy; To be specified	1

Running k1964s on 03-25-2004

	ID	Description	Count
1	G-S12	Title Page: 8 wafers, p-type, 10-30 ohm.cm	8
2	P-EM	E-BEAM Mask/Reticle Writing	0
3	G-1P	Lithography Notes	0
4	G-1	Notebook page	0
5	W-C1	* RCA clean	8
		INITIAL THERMAL OXIDATION	
6	F4-00	* Furnace 4: Load in O2: 200nm at 1000degC, 10' O2, 20' wetO2, 30' N2	8
		GROW POLYSILICON AND THEN ETCH POLY (L/FIELD)	
7	W-C1	* RCA clean ?	8
8	LP-A5	* Amorphous Si deposition: 500nm +-25nm at 560degC 10nm/min	8
9	P-GS1	* STEPPER Photolith: K991RW, P1, L/Field: nom. 1.1um resist STANDARD ** resist thick enough? **	8
10	G-2	* See Engineer for instructions	0
11	P-RHE	* Hardbake for dry etch	8
12	D-SP2	Etch Poly/AmSi. Anisot. on oxides >15nm SYS90 HBr 2 step. (For LF patterns)	8
13	W-R2	* Resist strip, First pot Fuming Nitric acid only	8
14	P-RS	* Resist strip	8
15	X-I1	Inspect 12 wafers for residue after wet or dry etch.	12
		DEPOSIT OXIDE AND DRY ETCH OXIDE	
16	W-C1	* RCA clean	8
		CAVITY PROCESS SPLIT	
17	LO-20	* LTO deposition: 200nm +- 20nm at 400degC SiH4 and O2 WAFER 1 to 4	4
18	RA-0	AG RTA stage : 30secs at 1000degC * TO CHK RTA TIME * WAFER 5 to 8	0
19	LO-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2 WAFER 5 to 8	4
20	LN-13	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m. WAFER 5 to 8	4
21	LO-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2 WAFER 5 to 8	4
22	RA-0	AG RTA stage : 30secs at 1000degC ?	4
23	P-GS1	* STEPPER Photolith: K991RW, V1, D/Field: nom. 1.1um resist STANDARD ** resist thick enough **	4
24	G-2	* See Engineer for instructions	0
25	P-RHE	* Hardbake for dry etch	3
26	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFER 1 to 4	3
27	RA-0	AG RTA stage : 30secs at 1000degC ?	4
28	P-GS1	* STEPPER Photolith: K991RW, V1, D/Field: nom. 1.1um resist STANDARD ** resist thick enough **	4
29	G-2	* See Engineer for instructions	0
30	P-RHE	* Hardbake for dry etch	4
31	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFER 5 to 8	4
32	D-N1F	Etch Si3N4. Anisot. D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFER 5 to 8	0

Running k1964s on 03-25-2004

	1	2	3	4	5	6	ID	Description	Count
33							D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar WAFER 5 to 8	0
34							X-I1	Inspect wafers for residue after wet or dry etch.	4
35							X-I1	Inspect wafers for residue after wet or dry etch.	4
								POLY ETCH TEST	
36							D-SP3	Etch PolySi Isot. OPT 80+ SF6 ** Etch wafer 1-4	4
37							D-SP3	Etch PolySi Isot. OPT 80+ SF6 ** Etch wafer 5-,8 **	0
38							X-I1	Inspect wafers for residue after wet or dry etch.	4
39							X-I1	Inspect wafers for residue after wet or dry etch.	4
								ETCH OXIDE LAYER	
40							D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar ** Etch 200nm (bottom) oxide layer in cavities **	4
41							P-RS	* Resist strip	4
42							X-I1	Inspect 12 wafers for residue after wet or dry etch.	4
43							D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar ** Etch 200nm (bottom) oxide layer in cavities **	0
44							P-RS	* Resist strip	4
45							X-I1	Inspect 12 wafers for residue after wet or dry etch.	4
								ETCH DAMAGE REMOVAL PROCESS	
46							W-C1	* RCA clean	4
47							F4-00	* Furnace 4: Load in O2: To be specified	4
48							WH-7[	Dip etch, 7:1 BHF 25degC. To hydrophobic Si + 20secs.	4
49							X-0	General inspection stage	1
50							LE-0	Low Pressure Epitaxy; To be specified	2
51							W-C1	* RCA clean	4
52							F4-00	* Furnace 4: Load in O2: To be specified	4
53							WH-7[	Dip etch, 7:1 BHF 25degC. To hydrophobic Si + 20secs.	-2
54							X-0	General inspection stage	0
55							LE-0	Low Pressure Epitaxy; To be specified	0

Running k2209s on 03-25-2004

	ID	Description	Count
1	P-EM	E-BEAM Mask/Reticle Writing	1
2	G-S12	Title Page: 16 wafers, MATERIAL: p-type, 15ohm.cm <100> 16 wafers	16
3	G-1P	Lithography Notes	0
4	G-1	Notebook page	0
5	W-C1	* RCA clean	16
6	F4-00	* Furnace 4: 200nm, 10' O2, 20' wet O2 @ 1000degC, 30' N2	16
		DEFINE SEED WINDOWS	
7	P-GS1	* STEPPER Photolith: reticle k991rw, V1, D/Field: nom. 1.1um resist STANDARD	16
8	G-2	* See Engineer: Inspect	0
9	P-RHE	* Hardbake for dry etch	15
10	D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	15
11	P-RS	* Resist strip	15
12	X-I1	Inspect 16 wafers for residue after wet or dry etch.	15
13	W-C1	* RCA clean	15
		SEED WINDOW ISOLATION OXIDE GROWTH	
14	F5-90	* Pad oxidation: 900degC, 20nm+- 5nm, O2 + HCl ** Wafers 1-8 **	7
15	F5-95	* Pad oxidation: 950degC, 40nm+- 5nm, O2 + HCl ** Wafers 9-16 **	8
16	W-C1	* RCA clean	14
17	LP-A6	* Amorphous Si deposition: 600nm +-30nm at 560degC 10nm/min ** Wafers 1-4, 9-12 **	6
18	LP-A5	* Amorphous Si deposition: 500nm +-25nm at 560degC 10nm/min ** Wafers 5-8, 13-16 **	8
		POLYSILICON ETCH	
19	P-GS1	* STEPPER Photolith: reticle k991rw, T1, D/Field: nom. 1.1um resist STANDARD	14
20	P-RHE	* Hardbake for dry etch	14
21	G-2	* See Engineer for instructions ****DARK FIELD PATTERN - POOR END POINT AND ETCH SELECTIVITY, BUT STOPPING ON 200nm SiO2 - SHOULD BE OK****	0
22	D-SP2	Etch Poly/AmSi. Anisot. on oxides >15nm SYS90 HBr 2 step. (For LF patterns)	14
23	P-RS	* Resist strip	14
24	X-I1	Inspect 16 wafers for residue after wet or dry etch.	14
		DEFINE OXIDE CAVITY	
25	LO-30	* LTO deposition: 300nm +- 30nm at 400degC SiH4 and O2	14
26	LN-13	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m.	7
27	LO-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2	7
28	LO-15	* LTO deposition: 150nm +- 15nm at 400degC SiH4 and O2 wafers #13-16	2
29	RA-0	AG RTA stage : 30 secs @ 1000 degC	7
		** SPLIT FOR WAFERS 9 - 16 **	
30	W-C1	* RCA clean	8
31	F4-W8	* Wet oxidation: 15mins @ 850degC (PNP research)	8
32	X-0	General inspection stage: SEM wafer 9 by Engineer	8

Running k2209s on 03-25-2004

	1 2 3 4 5 6	ID	Description	Count
33		W-C2	* Fuming Nitric acid clean, 2nd pot only	8
34		P-GS1	* STEPPER Photolith: reticle k991rw, P1, L/Field: nom. 1.1um resist STANDARD	8
35		G-2	* See Engineer: Inspect	0
36		P-RHE	* Hardbake for dry etch	0
37		D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar	0
38		D-N1E	Etch Si3N4. Anisot. L/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	0
39		D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar	0
40		D-SP3	Etch PolySi Isot. OPT 80+ SF6 ** Wafers 9-16 **	0
41		P-RS	* Resist strip	0
42		X-I1	Inspect 16 wafers for residue after wet or dry etch.	0
43		X-0	General inspection stage: SEM wafers by Engineer	0
			REMOVE THIN OXIDE	
44		WH-7I	Dip etch, 7:1 BHF 25degC. 25 - 50 secs only	0
45		X-0	General inspection stage: SEM wafers 1 and 6 by Engineer	7
			ETCH OXIDE + POLYSILICON	
46		W-C2	* Fuming Nitric acid clean, 2nd pot only	14
47		P-GS1	* STEPPER Photolith: reticle k991rw, P1, L/Field: nom. 1.1um resist STANDARD	7
48		G-2	* See Engineer: Inspect	0
49		P-RHE	* Hardbake for dry etch	7
50		D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar	7
51		D-N1E	Etch Si3N4. Anisot. L/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	7
52		D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar	7
53		D-SP2	Etch Poly/AmSi. Anisot. on oxides >15nm SYS90 HBr 2 step. (For LF patterns)	0
54		D-SP3	Etch PolySi Isot. OPT 80+ SF6 ** Wafers 1-4, 9-12 **	4
55		WS-3	Etch silicon in KOH ** Wafers 5-8, 13-16 **	2
56		P-RS	* Resist strip	4
57		X-I1	Inspect 16 wafers for residue after wet or dry etch.	4
58		X-0	General inspection stage: SEM wafers by Engineer	0
			REMOVE THIN OXIDE	
59		WH-7I	Dip etch, 7:1 BHF 25degC. 25 - 50 secs only	0
			EPITAXY LPCVD	
60		W-C1	* RCA clean	-2
61		LE-0	Low Pressure Epitaxy; >1um SEG	-2

Running k2280s on 03-25-2004

	ID	Description	Count
1	P-EM	E-BEAM Mask/Reticle Writing	0
2	G-S12	Title Page: 15 wafers, MATERIAL: 12 wafers BCO SOI n-type, 2um active layer, <100> + 3 silicon check wafers <100>.	9
3	G-1P	Lithography Notes	0
4	G-1	Notebook page	0
5	W-C1	* RCA clean	9
		### Cavity Formation ###	
6	LO-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2	9
7	LN-0	* Deposit LPCVD Si3N4. 100nm @740degC	9
8	LO-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2	9
		#### Photolith + Etching Stages ####	
9	P-GS1	* STEPPER Photolith: reticle V1, D/Field: nom. 1.7um resist STANDARD	9
10	G-2	* See Engineer: Inspect	0
11	P-RHE	* Hardbake for dry etch	0
12	D-N1F	Etch **LTO-Si3N4-LTO sandwich** . Anisot. D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar (Si3N4 etch)	9
13	D-0	Dry deep Si anisot.etch (~2um) ICP HBr process 3 Si check wafers only	7
14	G-2	* See Engineer: Proceed only after SEM analysis of cleaved wafer	0
15	D-0	Dry deep Si anisot.etch (~2um) ICP HBr process SOI wafers 1 - 12	0
16	G-2	* Note for Engineer: Do test etch KOH and SF6	0
17	D-SP3	Etch PolySi Isot. OPT 80+ SF6 (etch back 5um) ** wafer 7-12 **	2
18	P-RS	* Resist strip ** wafer 7 - 12**	0
19	P-RS	* Resist strip ** test with wafer 1 only **	0
20	WS-3	Etch silicon in KOH (etch back 5um) ** test with wafer 1 only **	0
21	P-RS	* Resist strip ** Strip wafers 2 - 6 if test on wafer 1 ok **	5
22	WS-3	Etch silicon in KOH (etch back 5um) ** Etch wafers 2 - 6 if test on wafer 1 ok **	0
23	X-0	General inspection stage: SEM cavity (wafer 1,2,7)	5
		#### Etch Damage Removal Process + LP Epitaxy ####	
24	W-C1	* RCA clean	1
25	F4-00	* Furnace 4: Load in O2: dry O2, 950degC, 20 mins	0
26	WH-7[	Dip etch, 7:1 BHF 25degC. Etch for 25 seconds (chk hydrophobic)	0
27	LE-0	Low Pressure Epitaxy: 1 - 3 um by DCS/SiH4 + DCS/H2 etch back (wafer: see eng)	-2
28	LE-0	Low Pressure Epitaxy: 1 - 3 um by DCS/SIH4 + DCS/H2 prebake (wafer: see eng)	-2
29	X-0	General inspection stage: SEM cavities	-2

Running k2484s on 03-25-2004

	ID	Description	Count
1	P-EM	E-BEAM Mask/Reticle Writing	0
2	G-S12	Title Page: 7 wafers, 10-30 ohm.cm, p-type (wafers 1-4). 3 wafers, BCO SOI wafers (wafers 5-7)	7
3	G-1P	Lithography Notes	0
4	G-1	Notebook page	0
5	W-C1	* RCA clean	7
6	F4-W0	* Wet oxidation: 600nm, 1000degC: I,rO2,x'wO2,uN2 Wafers 1-4	4
7	LO-30	* LTO deposition: 300nm +- 30nm at 400degC SiH4 and O2 Wafers 5-7	3
8	F4-W8	* Wet oxidation: 15mins @ 850degC (PNP research) - LTO Densification	3
9	P-GS1	* STEPPER Photolith: V1, k991rw, D/Field: nom. 1.1um resist Wafers 1 - 7	7
10	G-2	* See Engineer: inspection	0
11	P-RHE	* Hardbake for dry etch	7
12	D-O1F	Etch SiO2 -600nm Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar Wafers 1 - 4	4
13	D-O1F	Etch SiO2 -300nm Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar Wafers 5 - 7	3
14	D-0	ICP Dry etch Anisotropic, HBr Process. 2um Si etch down to buried SiO2 (300nm)	3
15	P-RS	* Resist strip	3
16	X-I1	Inspect 7 wafers for residue after wet or dry etch.	7
17	W-C1	* RCA clean	7
		*** Oxide Rippling Reduction Experiment *** Wafers 1 - 3	
18	WH-7[	Dip etch, 7:1 BHF 25degC. 5 to 10 secs. Wafers 1 - 3	2
19	F4-W8	* Wet oxidation: 5mins @ 980degC (PNP research)	1
20	WH-7[	Dip etch, 7:1 BHF 25degC. 15 secs.	1
21	W-C1	* RCA clean Wafers 1 - 3	1
22	F4-W8	* Wet oxidation: 5mins @ 980degC (PNP research)	1
23	WH-7[	Dip etch, 7:1 BHF 25degC. 15 secs.	1
24	X-0	General inspection stage: SEM & AFM	1
		*** Silicon Rippling Reduction Experiment *** Wafers 5 - 7	
25	W-C1	* RCA clean Wafers 5 - 7	0
26	F4-0	*Furnace 4: 950degC 40mins wetO2	1
27	WH-7[	Dip etch, 7:1 BHF 25degC. 30secs	1
28	X-0	General inspection stage: SEM & AFM Wafer 5 only	1
29	W-C1	* RCA clean Wafers 6 and 7 only	1
30	F4-0	*Furnace 4: 950degC 40mins wetO2 - Carry out if needed	1
31	WH-7[	Dip etch, 7:1 BHF 25degC. 30secs - Carry out if needed	1
32	X-0	General inspection stage: SEM & AFM	1
		*** Etch Damage Removal EDR Process *** Wafer 4 only	
33	W-C1	* RCA clean	1
34	F4-0	*Furnace 4: 950degC 20mins DRY O2	1
35	WH-7[	Dip etch, 7:1 BHF 25degC. 25secs.	1

Running k2513s on 03-25-2004

	1	2	3	4	5	6	ID	Description	Count
1							P-EM	E-BEAM Mask/Reticle Writing	0
2							G-S6	* Title page: 4 wafers, MATERIAL: 2 SOIs No.1 and No.2, 2 n-type 15 ohm.cm <100> No.3 and No.4	4
3							G-1P	* Lithography information	0
4							G-1	*Notebook page	0
5							W-C1	* RCA clean	4
6							LO-40	* LTO deposition: 400nm +- 40nm at 400degC SiH4 and O2 Wafer No. 1 + 3	2
7							LO-30	* LTO deposition: 300nm +- 30nm at 400degC SiH4 and O2 Wafer No. 2 + 4	2
8							P-GS1	* STEPPER Photolith: reticle k989r, D Field: nom. 1.1um resist STANDARD	4
9							G-2	* See Engineer : Inspect	0
10							P-RHE	* Hardbake for wet etch	4
11							WH-2	Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs.	4
12							P-RS	* Resist strip	4
13							G-2	* See Engineer : SEM Inspec	0
14							W-C1	* RCA clean	4
15							LN-13	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m. Wafer No.1+3	2
16							D-0	Dry etch: Etch Si3N4. Anisot. (~130nm) OPT80+ CHF3+Ar Wafer No.1+3 Minimal over etch to retain Si3N4 fillet	2
17							LN-20	* Deposit Si3N4 200nm +- 20nm at 740degC DCS:NH4 1:4, 2.3nm/min. Wafer No.2+4	2
18							D-0	Dry etch: Etch Si3N4. Anisot. (~200nm) OPT80+ CHF3+Ar Wafer No.2+4 Minimal over etch to retain Si3N4 fillet	2
19							G-2	* See Engineer : Inspect	0
20							D-0	Dry Deep Si. anisot.etch (~2um) ICP HBr process	1
21							X-0	General inspection stage : SEM Sidewall	4