UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING, SCIENCE AND MATHEMATICS

SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

INVESTIGATION OF TiO_2 AS A POSSIBLE TUNNELING LAYER IN THE VERTICAL METAL INSULATOR SEMICONDUCTOR TUNNEL TRANSISTOR

by

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ABSTRACT

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INVESTIGATION OF TiO_2 AS A POSSIBLE TUNNELING LAYER IN THE VERTICAL METAL INSULATOR SEMICONDUCTOR TUNNEL TRANSISTOR

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In this thesis, a new field effect transistor, the vertical metal insulator semiconductor tunnel transistor (VMISTT) is proposed. It is a modified version of the metal oxide tunneling transistor (MOTT). The principle of operation of the device is based on the gate modulated Fowler Nordheim (F-N) tunneling of carriers through an insulating layer. The VMISTT is different from the MOTT in two important aspects. Firstly, the metallic source in the MOTT is replaced by doped silicon. The body of the transistor is an oxide, which functions as a tunnel barrier. By choosing a suitable tunnel barrier and metal drain, it is possible to make both n-type and p-type devices and hence complementary devices. Secondly, the vertical structure will allow better control of material growth and device processing. The tunnel barrier can be grown by a conventional scalable process such as evaporation of thin metal film followed by thermal oxidation. This will help to reduce the leakage current and hence enhance the performance of the device.

The SILVACO device simulator ATLAS is used to study the VMISTT performance. The barrier height between the tunnel barrier and the Si substrate is a critical device parameter. A low barrier is required for a large F-N tunneling current to occur. However, Schottky emission, which is one of the main sources of leakage current in the VMISTT, will also be huge for a low value of the barrier height. It is thus important to optimise the barrier height to minimize the effect of Schottky emission on the device performance. The simulation results show that with a barrier height of 0.6 V, an on/off current ratio of at least 4 orders of magnitude, and a subthreshold slope of 42 mV/dec can be obtained. Titanium dioxide TiO_2 is a promising candidate for the tunnel barrier due to its low barrier height to Si.

The fabrication and optimisation of the tunnel barrier of the VMISTT is the focus of the experimental chapters of this thesis. The observation of F-N tunneling current in the tunnel barrier is essential such that the modulation of the F-N tunneling current by the gate bias can be realised at room temperature. Electrical and structural analysis are performed on TiO_2 films grown from thermal oxidation of electron beam evaporated Ti thin film. TiO_2 MOS capacitors with different top metal electrodes (Al, Pt) and different Si substrate (n-type, p-type) were fabricated to analyse the electrical properties of the TiO_2 films. It is shown that the reactivity of Al top contact affects the electrical properties of the oxide layers. The current transport mechanism in the TiO_2 films is found to be Poole-Frenkel (P-F) emission at room temperature. At 84 K, F-N tunneling and trap-assisted tunneling are observed. By comparing the electrical characteristics of thermally grown TiO_2 films with the properties of those films grown by other techniques reported in the literature, it is suggested that irrespective of the deposition technique, annealing of as-deposited TiO_2 in O_2 is a similar process to thermal oxidation of Ti thin films. In conclusion, it is essential to reduce the defects density in the TiO_2 films, so that those trap-related mechanisms can be suppressed for the observation of the F-N tunneling at room temperature.

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Chapter 1

Introduction

1.1 Field Effect Transistor

The progress of the semiconductor industry has been very successful in the last few decades due to the continuing improvement in the system performance. This progress follows Moore's Law, which states that the transistor performance is to be doubled and the number of transistors on a chip is to be quadrupled every three years [1]. This is achieved by down-scaling the feature sizes of metal oxide semiconductor field effect transistors (MOSFETs), which improves the speed of the transistor and increases the density of the transistors on a chip. According to the International Technology Roadmap for Semiconductors (ITRS) [2], the down-scaling will continue and the gate length of a MOSFET is required to be around 10 nm in 2015. This continuous demand brings tremendous complications to the device design and fabrication due to the physical limitations of nano-scale devices. Quantum mechanical and short channel effects will become significant and deteriorate the device performance [3, 4] and in order to meet the down-scaling requirements, several new approaches have been introduced.

High-k dielectric material has been proposed to replace the SiO_2 as the gate oxide to reduce the gate to channel leakage current [5–7]. The gate oxide physical thickness is required to be below 1 nm at the 65 nm technology node [2]. As a result, the quantum mechanical tunneling of carriers will lead to a huge gate leakage current [2, 8]. A gate oxide with higher dielectric constant can achieve the same gate capacitance and a smaller equivalent oxide thickness (EOT) than SiO_2 but allow a thicker physical thickness. Therefore, the gate leakage current is reduced and there is more margin for continuing down-scaling.

However, there are strict requirements for the high-k material. A suitable candidate must have high stability and reliability on silicon as exhibited by SiO_2 [5]. It must also be thermally robust and have a good quality interface with silicon [5]. In addition, an effective surface electron and hole mobility similar to an SiO_2 interface is essential [9]. Recent experimental results showed that an EOT of less than 10 $\dot{A}$ is achieved using a hafnium nitride/hafnium dioxide (HfN/HfO_2) gate stack [10]. Nevertheless, issues such as carrier mobility degradation, instability in threshold voltage, and Fermi-level pinning effect with the gate electrode are to be addressed [7, 11–13]. It is believed these issues are caused by the charges and interface states in the high-k dielectric materials. Therefore, further investigation for a successful implementation of high-k dielectric materials is required.

Research on new device structures is also an approach that attracts much attention. Double gate FET (DGFET) is one of the promising structures which can enhance the device performance [3, 14, 15]. The double gate feature allows a better gate control of the channel, and improves the drive current by increasing the channel width. FinFET is a non-planar version of DGFET in which the silicon channel protrudes from the substrate surface like a fin [16, 17]. The drive current can be improved by increasing the device width through parallel connection of several fins. FinFETs with channel length less than 20 nm have been reported [17]. However, the drawbacks of FinFETs are the complexity in thin fin fabrication process, as well as the increase in source and drain resistances due to the thin silicon channel [3].

Another new device structure that has received considerable interest in recent years is vertical MOSFETs [18–25]. One of the major advantages of the vertical MOSFETs is that the channel length is not defined by photolithography techniques, which are difficult to downsize when approaching shorter channel length. Instead, the channel is grown vertically and its thickness is defined by the deposition and oxidation processes [26]. Hence, there is more control as the thickness of the channel can be precisely defined by the growth process. Also, a double or surround gate structure could be realised in the vertical transistor, which will increase the channel width per transistor area and thus increase the packing density compared to planar MOSFETs [27].

Many research groups have been working on replacing the MOSFETs with new devices, which have a principle of operation that is different from the MOSFETs, and which can meet the target of the ITRS roadmap after the scaling of the MOSFETs has become impossible. One of the popular candidates is Schottky barrier MOSFET (SBMOSFET) [28–33]. It has a structure similar as a MOSFET but with a metal silicide source and drain. The switching of the transistor can be achieved by modulating the Schottky barrier formed between the silicon substrate and the metal silicide source with the gate bias. The main advantage of the SBMOSFET is the low source and drain resistance due to the metal silicide source and drain. Also, owing to the abrupt interface between the metal silicide and the silicon substrate and channel, the SBMOSFET is scalable to sub-10 nm channel length regime. The SBMOSFET can realise complementary operation by choosing a low work function metal for n-FET (electrons as majority carriers) and a high work function metal for p-FET (holes as majority carriers). However, n-FET silicide material is not readily available due to the low barrier height requirement.

Another device of particular interest is metal oxide tunneling transistor (MOTT) [34–41]. The source and drain are metals, and the body of the transistor is an oxide. The body of the MOTT is also known as tunnel barrier. The principle of operation is similar to the SBMOSFET. It is based on the gate modulated Fowler Nordheim (F-N) tunneling of carriers through the oxide layer. The probability of the F-N tunneling is modulated by gate bias through a dielectric material. Single crystalline Si is not required in the MOTT and three-dimensional multi-layer circuits can be fabricated by stacking two-dimensional circuits. Other advantages of the MOTT include scalability to nano-scale, high speed, simple fabrication process, and alleviation of short channel effects. Transistor behaviour of the MOTT has been observed at low and room temperature. However, an efficient and reliable operation of the device requires further improvement in the device design and the quality of the tunnel barrier [41].

It is believed that the performance of the MOTT is limited by the quality of the tunnel barrier, which is determined by the fabrication technique. The fabrication technique is restricted by the lateral device structure. In addition, owing to the design of the MOTT, complementary operation cannot be realised. This is because the conduction current is due to the electrons from the metal source only.

1.2 Aim and Outline of this Thesis

In this thesis, a new nano-device, the vertical metal insulator semiconductor tunnel transistor (VMISTT) is proposed. The VMISTT is a modified version of the MOTT. It has a vertical structure and a semiconductor source. The VMISTT inherits the advantages offered by the MOTT. In addition, with its semiconductor source it is possible to realise complementary device operation. Its vertical structure will allow the growth of the channel by deposition techniques and an increase of the channel control by the surround gate structure. The proposed VMISTT also aims to reduce the leakage current at room temperature by optimising the quality and the barrier height of the tunnel barrier. With a vertical device structure, the tunnel barrier can be fabricated by a conventional thin film fabrication technique, which can produce tunnel barriers with better quality and which allows better control of the tunnel barrier thickness.

The fabrication and characterisation of the tunnel barrier are the focus of the experimental chapters of this thesis. The objective is to fabricate a tunnel barrier with F-N tunneling current as the dominant current transport mechanism at room temperature. The dielectric material and the fabrication technique to grow the tunnel barrier are two of the important factors for considerations. Titanium dioxide TiO_2 is expected to be a suitable material for the tunnel barrier because its barrier height to silicon Si is 1 V at both the conduction band and the valence band. Two fabrication methods are studied: thermal oxidation of electron beam (e-beam) evaporated titanium Ti thin films and molecular beam epitaxy (MBE) of Ti in an oxygen atmosphere. It is shown that TiO_2 films grown by thermal oxidation of e-beam evaporated Ti thin films are superior and these films are studied in detail.

The contents of this thesis is organized in the following order: Chapter 2 discusses the theory and the scaling limitation of MOSFETs, as well as various types of vertical MOSFETs and their fabrication processes. Chapter 3 focuses on the review of the MOTT and discusses its shortcomings.

Chapter 4 presents the simulation results of the newly proposed VMISTT. SILVACO device simulator ATLAS is used to perform the simulation. The device parameters that affect the performance of the VMISTT are also discussed in this chapter.

Chapter 5 focuses on the fabrication methods of TiO_2. An overview of TiO_2 is given and the fabrication techniques of TiO_2 films are discussed. The results of thermally grown TiO_2 layers and MBE grown TiO_2 layers are presented. It is shown that thermal oxidation of e-beam evaporated Ti thin films is superior. These thermally grown oxide samples are studied in detail in the following chapters.

Chapter 6 presents the structural analysis of thermally grown TiO_2 layers of different thicknesses. Scanning electron microscope (SEM), time-of-flight secondary ions mass spectrometry (TOF-SIMS), and X-ray diffraction (XRD) were used for structural analysis. Electrical characterisation were also performed on oxide layers with different thicknesses. A suitable oxide thickness is selected for further characterisation.

Chapter 7 focuses on the electrical characteristics of TiO_2 MOS capacitors on different Si substrates (n-type, p-type) and with different top metal electrodes (Al, Pt). This chapter discusses the current transport mechanisms in the TiO_2 layers at different temperatures and biases. Finally, this thesis is concluded with future work for the VMISTT project.

Chapter 2

Operation and Architecture of MOSFETs

2.1 Introduction

MOSFETs play an essential role in integrated-circuit (IC) technology since its invention in 1960. One of the important features of the MOSFET is the scalability. This has been a strong drive for the semiconductor industry to continue in down-scaling MOSFETs, as smaller device sizes will allow higher device density on an IC chip and also provide more functions. In addition, faster device switching speed can be achieved at smaller device size. However, as the feature sizes of the MOSFET are getting smaller, short channel effects and quantum mechanical tunneling is becoming more and more significant [3, 4]. This will degrade the device performance.

This chapter focuses on the theory of metal-oxide-semiconductor (MOS) capacitors and MOSFETs, which will be used for the interpretation of VMISTT concepts and the experimental results. Short channel effects in MOSFETs are addressed. The MOSFET theory presented here is based on the following books: *Solid State Electronic Devices* by B.G. Streetman [42], *The Physics of Semiconductor* by S.M. Sze [4] and *Fundamentals of Modern VLSI Devices* by Y. Taur and T.K. Ning [43]. Finally, the vertical MOSFET, a modified version of the planar MOSFET, is also discussed in this chapter.

2.2 MOS Capacitor: Two Terminal MOS Device

The MOS capacitor is the fundamental structure of a MOSFET. It has two terminal: the gate and the semiconductor substrate. Figure 2.1 shows the schematic and the energy band diagram of an ideal MOS capacitor with p-type Si (p-Si) at zero bias. When a negative bias is applied to the metal gate, positive charges will accumulate at the semiconductor surface and an equal amount of negative charges will appear on the gate. Due to the applied negative bias, the electrostatic potential of the metal relative to the semiconductor is lowered, which means the electron energy in the metal is raised relative to the semiconductor. Hence, the metal Fermi level will rise by qV, where q and V are the electronic charge and applied bias, respectively. This results in a tilt in the oxide energy band, as shown in Figure 2.2(a). The positive charges accumulated at the semiconductor surface imply an increase in $E_i - E_f$ at the semiconductor surface [42]. As there is no current flowing through the structure, there will be no change in the semiconductor Fermi energy level E_f. Hence, the intrinsic level E_i near the surface will move up in energy. The MOS capacitor is said to be in accumulation mode.

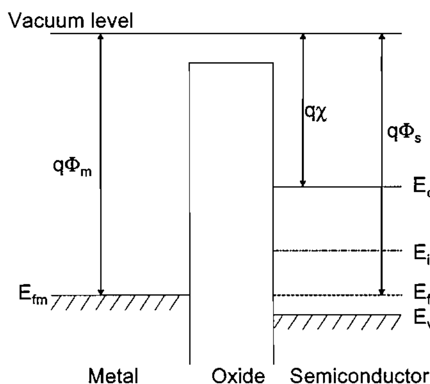

Figure 2.1: Energy Band Diagram for an ideal MOS capacitor at zero bias, $q\Phi_m$ and $q\Phi_s$ are the work function of the metal and the semiconductor, respectively, $q\chi$ is the electron affinity of the semiconductor. E_{fm} is the Fermi level of the metal, E_c, E_v, E_i and E_f are conduction band, valence band, intrinsic level and Fermi level of the semiconductor, respectively.

As shown in Figure 2.2(b), when a positive bias is applied to the gate, the metal Fermi level E_{fm} is lowered by qV due to the rise in the metal potential. At the semiconductor surface, the hole concentration will decrease as the holes are depleted away and left behind are the uncompensated ionized acceptors. As a result, E_i near the semiconductor surface will move down in energy. This indicates a decrease in E_i-E_f at the semiconductor surface. The MOS capacitor is said to be in depletion mode. If the positive bias is further increased,

E_i will bend below E_f (see Figure 2.2(c)), which means the region near the semiconductor surface has conduction properties of an n-type material. This n-type layer is created by the strong positive gate bias and consists of free electrons. This mode is called inversion as the free carriers in the semiconductor are now of opposite sign with respect to the situation without the applied bias. This inverted n-type layer is the conduction channel for the MOS transistor.

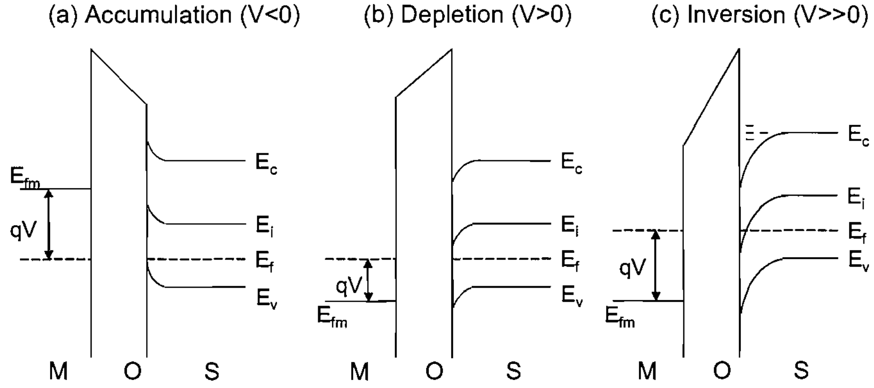

Figure 2.2: Three different operation modes of an ideal MOS capacitor:(a) accumulation, (b) depletion and (c) inversion.

Strong inversion occurs when the concentration of electrons in the inverted n-type layer is equal to the concentration of holes in the p-type substrate. The bias required to create strong inversion in the MOS capacitor is known as the threshold voltage V_T [42]:

$$V_T = -\frac{Q_d}{C_{ox}} + 2\Phi_f \tag{2.1}$$

where

$$Q_d = -\sqrt{2\epsilon_{ox} N_A (2\Phi_f)} \tag{2.2}$$

where C_{ox} is the oxide capacitance per unit area, Φ_f is the potential difference between E_f and E_i at the surface of the semiconductor, Q_d is the charge per unit area in the depletion region, N_A is the doping concentration of the p-type semiconductor substrate, and the permittivity of the oxide $\epsilon_{ox} = \epsilon_r \epsilon_0$, where ϵ_r is the dielectric constant of the oxide and ϵ_0 is the permittivity of free space.

2.2.1 Ideal Capacitance-Voltage Characteristic

The relationship between the MOS capacitance C and the applied gate bias V is shown in Figure 2.3(a). At high frequency, e.g 1 MHz, when V is negative, the MOS capacitor is in accumulation mode. A large number of holes is accumulated right below the oxide, forming the bottom plate of the capacitor. The effective maximum capacitance per unit area is

$$C_{ox} = \frac{\epsilon_r \epsilon_0}{d_{ox}} \tag{2.3}$$

where d_{ox} is the oxide thickness. When V becomes positive, the MOS capacitor is entering the depletion mode and the capacitance due to the depletion layer need to be accounted for. This depletion capacitance C_d is in series with C_{ox}, as shown in Figure 2.3(b), and the overall capacitance becomes [42]

$$C = \frac{C_{ox} C_d}{C_{ox} + C_d} \tag{2.4}$$

and

$$C_d = \frac{\epsilon_{Si} \epsilon_0}{W_{Si}} \tag{2.5}$$

$$W_{Si} = \sqrt{\frac{2\epsilon_{Si}\epsilon_0 \phi_s}{qN_A}} \tag{2.6}$$

W_{Si} and ϕ_s are the width of the depletion region and surface potential of the Si substrate, respectively, and ϵ_{Si} is the Si dielectric constant. As V keeps increasing, the width of depletion layer increases, which in turn causes the overall capacitance C to decrease. When $V \geq V_T$, an inversion layer forms beneath the oxide, the width of the depletion layer cannot be increased any further, and C reaches its minimum value, C_{min}.

When measuring the capacitance-voltage characteristics (C-V) of the MOS capacitor at very low frequency (*e.g.* 1 Hz), the capacitance at inversion will not stay at the minimum value. The capacitance will gradually increase when $V > V_T$, and eventually rise to the maximum value, C_{ox}. This is because at very low frequency, the gate bias is changing slowly by a small amount and a new equilibrium can be reached as the thermal generation and recombination of the carriers can response to the bias changes. A large number of electrons will appear right below the oxide, forming the bottom plate of the capacitor. Hence, the capacitance will go back to the maximum value C_{ox}. At high frequency, the inversion

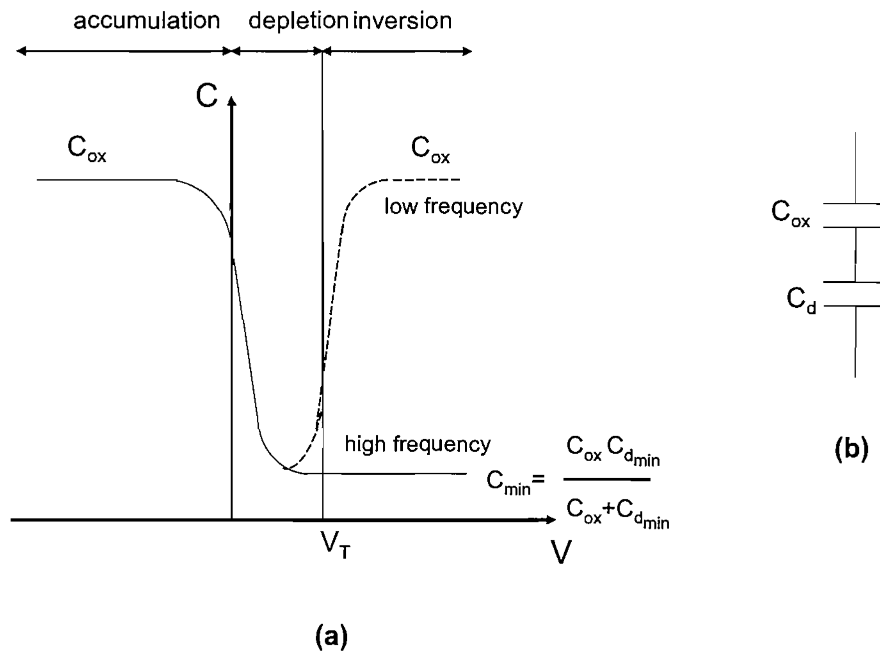

Figure 2.3: (a) Ideal capacitance-voltage characteristics for a MOS capacitor, $C_{d_{min}}$ is the depletion capacitance at maximum depletion width, (b) the model of the MOS capacitor.

layer charges cannot keep up with the fast changing gate voltage due to the slow thermal generation and recombination rate. The only change of charges is provided by covering and uncovering the acceptors at the interface of substrate and depletion region [44, 45], which results in the solid line shown in Figure 2.3(a).

2.2.2 Effect of Real Surfaces

The effect of real surfaces can affect the C-V characteristic of a MOS capacitor and must be accounted for when determining the value of V_T. Generally, the work function of the metal gate $q\Phi_m$ is not equal to that of the Si substrate $q\Phi_s$. Figure 2.4(a) illustrates the energy band diagram of a MOS capacitor with $q\Phi_m < q\Phi_s$. At equilibrium, both the Fermi level of the metal gate and the Si must align. This will result in a tilt in the energy band diagram, as shown in Figure 2.4(b). To obtain the flat band condition as pictured in Figure 2.4(c), a negative gate voltage V, which is equal to the work function potential difference between the metal and semiconductor Φ_{ms}, must be applied.

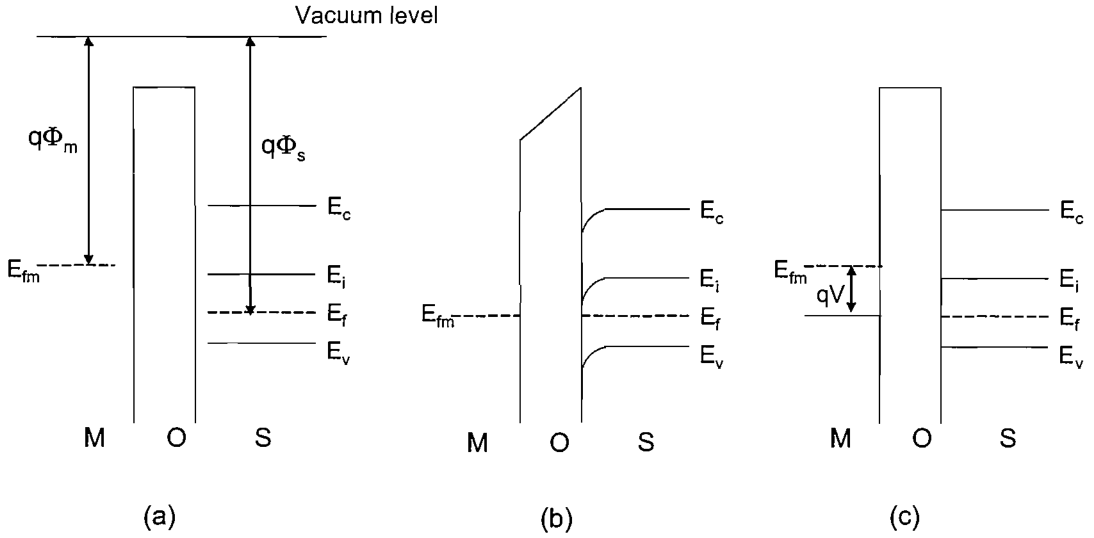

Figure 2.4: Illustration of the effect of work function difference between the metal gate and the Si substrate, with $q\Phi_m < q\Phi_s$: (a) The energy band diagram of a MOS capacitor before the materials come into contact, (b) The energy band diagram of the MOS capacitor at equilibrium, (c) The energy band diagram of the MOS capacitor when a negative gate voltage V is applied to achieve the flat band condition.

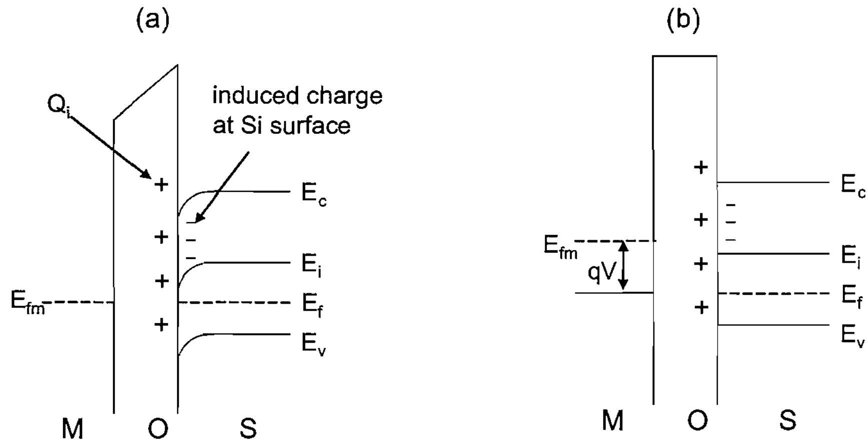

Figure 2.5: Illustration of the effect of oxide and interface charges on the energy band diagram of a MOS capacitor. (a) Q_i is the oxide and interface charges per unit area, and is represented by a sheet of positive charge at the oxide/Si interface. An equivalent negative charge is induced in the Si substrate. (b) a gate voltage V is applied to achieved the flat band condition.

Another real surface effect is the charges in the oxide as well as at the oxide/Si interface. These charges are associated with the defects created during the oxide fabrication process and are generally positive charges. Owing to that, an equivalent negative charge density is induced at the Si surface, as shown in Figure 2.5(a). To achieve flat band condition, a gate voltage with a value of -Q_i/C_{ox} must be applied, where Q_i is the oxide and interface charge per unit area of the MOS capacitor (see Figure 2.5(b)).

To account for the effect of a real surface, the voltage required to achieve the flat band condition of a MOS capacitor is [42]

$$V_{FB} = \Phi_{ms} - \frac{Q_i}{C_{ox}} = \Phi_m - \Phi_s - \frac{Q_i}{C_{ox}} \tag{2.7}$$

The flat band condition must be achieved before the strong inversion is created in the MOS capacitor. From Equations 2.1 and 2.7, the threshold voltage becomes [42]:

$$V_T = \Phi_{ms} - \frac{Q_i}{C_{ox}} - \frac{Q_d}{C_{ox}} + 2\Phi_f \tag{2.8}$$

The flat-band voltage V_{FB} can be determined by comparing the ideal and the measured C-V characteristic of the MOS capacitor, as shown in Figure 2.6. The oxide charge densities of the capacitors Q_i can be obtained using Equation 2.7. The Fermi level of the Si substrate Φ_s can be determined from Figure 2.7:

For n-Si,

$$\Phi_s = \chi + \frac{E_g}{2q} - \frac{E_f - E_i}{q} \tag{2.9}$$

For p-Si

$$\Phi_s = \chi + \frac{E_g}{2q} + \frac{E_i - E_f}{q} \tag{2.10}$$

where χ is the electron affinity of the Si, E_g is the bandgap of Si. $E_f - E_i$ and $E_i - E_f$ can be obtained using the following expressions [42]:

$$E_f - E_i = \frac{kT}{q} ln \frac{N_D}{n_i} \tag{2.11}$$

$$E_i - E_f = \frac{kT}{q} ln \frac{N_A}{n_i} \tag{2.12}$$

where N_D and N_A are the doping concentration of the n-Si and p-Si, respectively, and n_i is the intrinsic concentration of Si.

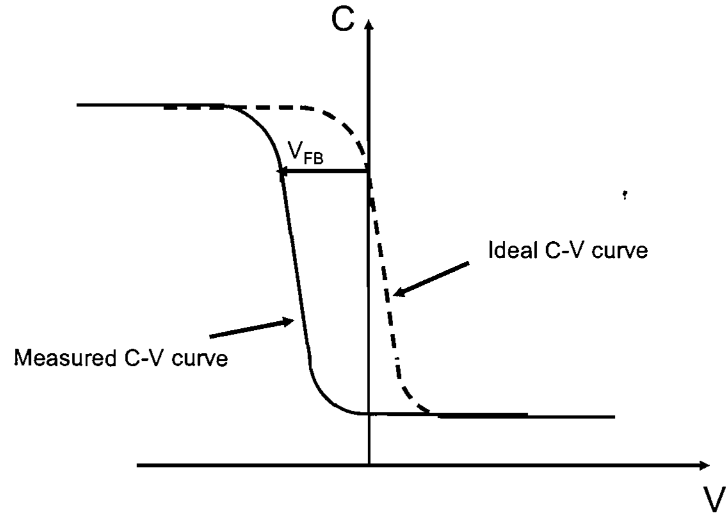

Figure 2.6: Comparison of the ideal and the measured C-V characteristic of a MOS capacitor. The device has a p-type Si substrate and positive Q_i. The value of the flat band voltage V_{FB} can be determined from the graph.

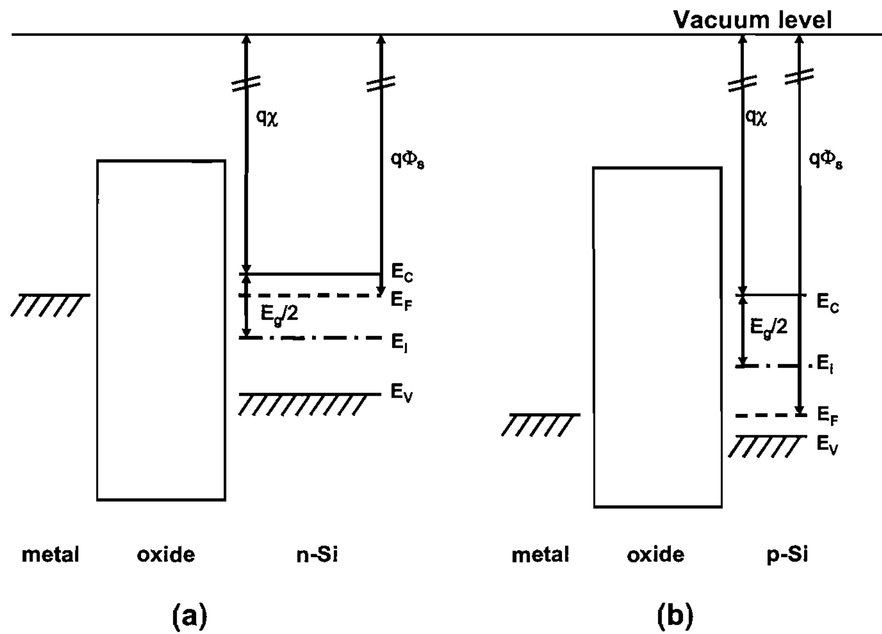

Figure 2.7: The energy band diagram of the MOS capacitors with (a) n-Si, (b) p-Si as substrate. E_g is the bandgap of Si.

2.3 MOSFET: Four Terminal MOS Device

The cross-sectional view of an n-channel MOSFET (nMOSFET) is shown in Figure 2.8. It has a p-type substrate, with two heavily doped n^+ regions, which form the source and drain of the device. The gate is on the top of the oxide (normally silicon dioxide) and the switching of the device is controlled by the gate bias. The discussion below is based on nMOSFET, but a similar idea is valid for p-channel MOSFETs (pMOSFET).

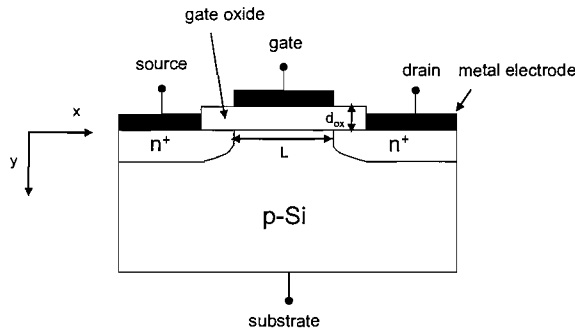

Figure 2.8: The cross-sectional view of a MOSFET. L and d_{ox} are the channel length and gate oxide thickness of the MOSFET, respectively.

The source of the device is normally grounded, and a positive voltage is applied to the drain. Without the gate bias V_G, there is no current flowing from drain to source. A positive V_G greater than the threshold voltage is required to create the inversion layer, which will be the channel for current conduction. As shown in Figure 2.9(a), when a small drain bias V_D is applied, a current will flow through the channel from the source to the drain and it will increase linearly with increasing V_D. This is the linear region of the MOSFET current-voltage (I-V) characteristic. In this region, $V_D << (V_G - V_T)$ and the drain current I_D can be expressed as [4]

$$I_D \approx \frac{W \mu_n C_{ox}}{L}(V_G - V_T)V_D \tag{2.13}$$

where W is the channel width, L is the channel length, μ_n is the electron mobility, and $C_{ox} = \epsilon_{ox}/d_{ox}$ is the gate oxide capacitance per unit area. When V_D is gradually increased, the depletion region under the drain increases. The width of the channel layer near the drain region will decrease, which in turn causes the channel resistance to increase. This leads to a slower current rate as shown in Figure 2.9(b). If V_D continues to increase, the width of the channel at the drain end will continue to decrease and eventually become

zero, this is known as pinch-off. The drain voltage required to create pinch-off is known as V_{Dsat}. At this point, the drain current will reach its maximum value, I_{Dsat}. Any further increased in V_D will only push the pinch-off point nearer to the source end, but will not increase the drain current, as illustrated in Figure 2.9(c). This is the saturation region of the MOSFET I-V characteristic and the drain current at saturation I_{Dsat} can be expressed as [4]

$$I_{Dsat} \approx \frac{W\mu_n C_{ox}}{2L}(V_G - V_T)^2 \tag{2.14}$$

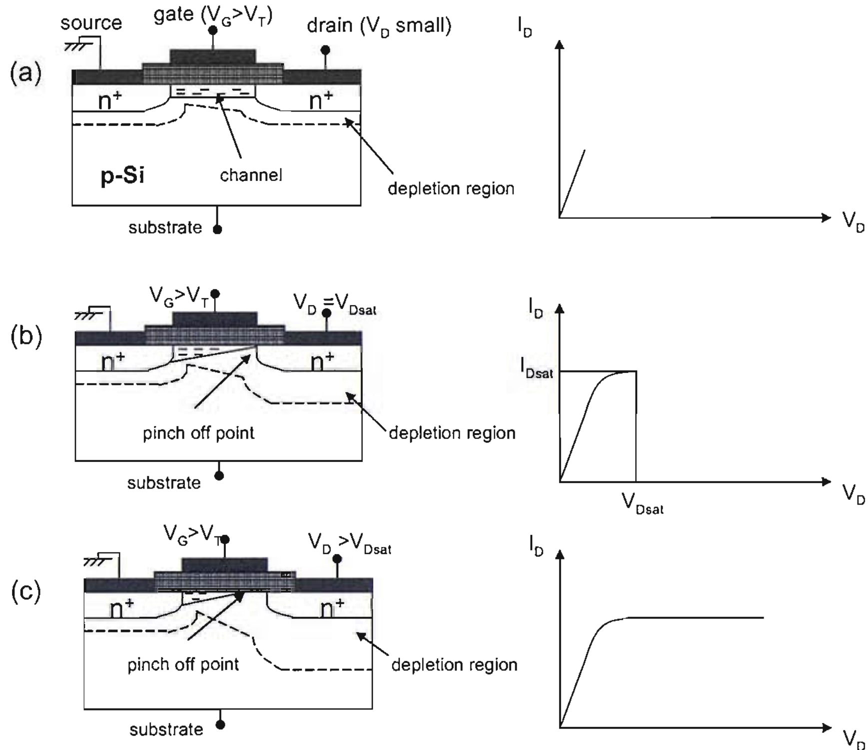

Figure 2.9: The operation of a MOSFET under different biased conditions:(a) small V_D, (b) $V_D = V_{Dsat}$ and (c) $V_D > V_{Dsat}$.

Figure 2.10 shows the I_D vs V_G characteristic of a MOSFET. The gate voltage swing required to increase the current by one decade is known as the subthreshold slope SVT [43]:

$$SVT = \frac{dV_G}{d(log_{10}I_D)} \tag{2.15}$$

SVT is determined from the maximum slope in the I_D vs V_G curve, as illustrated in Figure 2.10. The V_T of the MOSFET is defined as the V_G at the maximum subthreshold slope and can be determined from Figure 2.10. The lower the value of SVT, the smaller the gate voltage swing is required to switch the MOSFET on and off. As I_D is dependent on the carrier concentration at the Si surface n_s and $n_s = n_i exp(q\phi_s/kT)$ [42], it can be shown from Equation 2.15 that

$$SVT = \frac{kT}{q} ln10 \frac{dV_G}{d\phi_s} \approx 0.06 \frac{dV_G}{d\phi_s} \tag{2.16}$$

The gate voltage V_G is the sum of the voltage across the oxide V_{ox} and the surface potential of the Si substrate ϕ_s:

$$V_G = V_{ox} + \phi_s = \frac{Q}{C_{ox}} + \frac{Q}{C_d} \tag{2.17}$$

where Q is the charge induced by V_G. Rearranging Equation 2.17, the following expression can be obtained

$$\frac{V_G}{\phi_s} = 1 + \frac{C_d}{C_{ox}} \tag{2.18}$$

Using Equations 2.5, 2.6 and 2.18, SVT in Equation 2.16 becomes

$$SVT \approx 0.06 \left(1 + \frac{C_d}{C_{ox}}\right) \tag{2.19}$$

It can be seen from Equation 2.19 that the SVT of a MOSFET can never be lower than 60 mV/dec. The value of SVT of a MOSFET is typically 70 ~100 mV/dec [43].

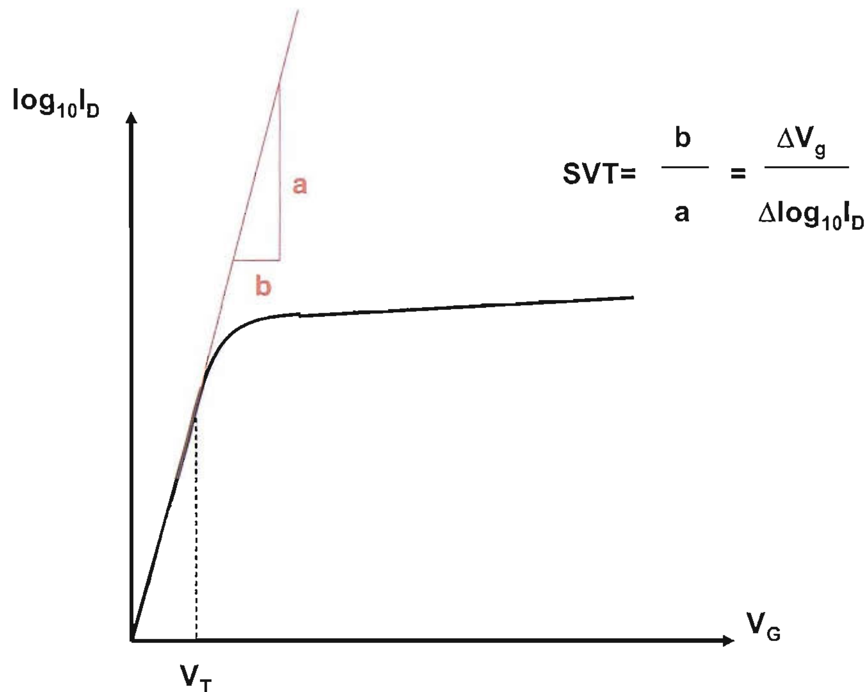

Figure 2.10: The I_D vs V_G characteristics of a MOSFET. The substhreshold slope SVT and the threshold voltage V_T of the MOSFET can be determined using this curve.

2.4 Complementary MOS

One of the major applications of MOSFETs is the implementation of complementary MOS (CMOS) in digital circuits. Figure 2.11 shows the most basic structure of a CMOS circuit: a CMOS inverter. It is a combination of an nMOSFET and a pMOSFET on the same substrate. The source of the pMOSFET is connected to the power supply V_{dd}, while the source of the nMOSFET is connected to the ground terminal. The gates of both transistors are connected together and known as the input. The drain of both transistors are connected together to the output. This digital circuit is named an inverter because the output signal is always the inverted value of the input signal: when the gate signal is low, the pMOSFET is switched on and the nMOSFET is switched off. The output signal is equal to V_{dd}. When the gate signal is high, the pMOSFET is switched off and the nMOSFET is switched on, and the output is pulled-down to ground. Only one transistor is switched on in either condition. As the transistors are connected in series, there is no current flowing except the charging or discharging current during the switching process. It has zero standby power and very little power dissipation during switching. As a result, CMOS circuits allow higher integration levels in very large scale integration (VLSI) applications [42, 43].

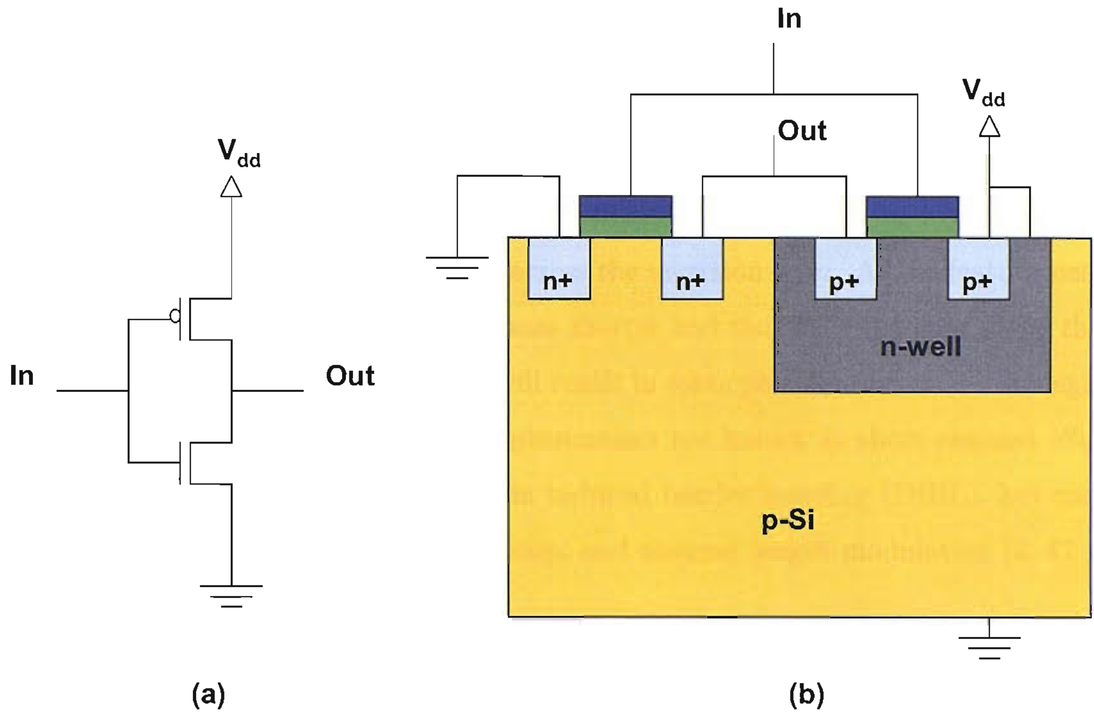

Figure 2.11: (a) Circuit of a CMOS inverter; (b) Schematic of a CMOS inverter.

The implementation of complementary operation is one of the main problems with proposed new devices to replace the MOSFET. Some of the proposed devices cannot realise complementary operation. One example is the metal oxide tunnel transistor (MOTT), since the carriers in this device are electrons coming from the metal source. Some of the proposed devices can realise complementary operation, but there are serious issues to be solved. The examples are Schottky barrier MOSFETs (SBMOSFETs) and carbon nanotube field effect transistors (CNTFETs). For SBMOSFETs, a low metal work function is required to create a low Schottky barrier height for the n-FET. This presents a problem because n-FET silicide material is not readily available and rare earth material such as erbium (Er) is generally attempted for n-FET silicide material [29, 32]. As for CNTFETs, the as-synthesized single-wall CNTFET is normally p-type. n-type CNTFETs can be fabricated using absorption doping [46, 47] or annealing [47]. However, the reproducibility, which is an important requirement in VLSI application, remains an issue in CNTFETs.

2.5 Short Channel Effects

In the previous section, the MOSFET is considered to have a sufficiently long channel so that the edge effect of the channel could be neglected. In the long channel model, the field pattern in the device is assumed to be one dimensional (y-direction in Figure 2.8), and there is no potential drop or band bending across the inversion layer. As the feature sizes of a MOSFET are reduced, the channel becomes shorter and thus the field lines along the x-direction should also be considered. This will result in some phenomena which can degrade the performance of the MOSFET. These phenomena are known as short channel effects. Some typical short channel effects are drain induced barrier lowering (DIBL), hot carrier effects, dopant fluctuation, velocity saturation, and channel length modulation [4, 42–44]:

(a) Drain Induced Barrier Lowering

In the short channel model, when the drain to source voltage V_{DS} is small, the channel depletion width is assumed to be constant. However, when V_{DS} is increased, the depletion width at the drain end becomes larger due to strong reverse bias at the drain pn junction. Owing to that, some charges in the depletion layer are controlled by the drain voltage instead of the gate voltage, which leads to a reduction in the threshold voltage. In addition, the drain depletion region will move towards the source depletion region, and more electric field will penetrate from drain to source, causing a lowering in potential barrier for the electrons in the source. As a result, more electrons in the source can be injected into the drain. Punch-through will occur when there is a large drain current flowing to the source even though the gate voltage is below the threshold voltage.

(b) Hot Carrier Effect

At short channel length, the electric field from drain to source is high. The electrons in the source region will gain high kinetic energy and cause impact ionization: these hot carriers have high energy and can break the lattice bond to create more electron-hole pairs. Some electrons can be absorbed by the drain, and cause a rise in drain current. Some electrons will be absorbed by the substrate and generate unwanted substrate current and may give rise to a parasitic transistor that leads to drain to source breakdown [4]. The hot carriers can also be injected into the gate and give rise to gate current. Besides, some of the hot carriers can be trapped in the oxide, and change the fixed oxide charge. The latter can pose a reliability problem to the device.

(c) Dopant Fluctuation

When the channel length and the oxide thickness of a MOSFET are being scaled down, the effect of the statistical fluctuation of dopant number in the channel depletion layer will become prominent [48, 49]. This dopant fluctuation is caused by the random fluctuation of incidental ion number in the p-well or the n-well formation and the random diffusion process of each ion. Dopant fluctuation will result in threshold voltage variation (see Equations 2.1 and 2.2 for the relationship between threshold voltage V_T and doping concentration N_A). This will be a problem for the chip design because it is critical that V_T can be reproduced from one transistor to another on a chip.

(d) Velocity Saturation

As the devices are reduced in size, the saturation of drain current will occur at lower voltage due to velocity saturation. This is because at shorter channel length, the longitudinal electric field (E_x, along the channel) is becoming more significant. As a result, the drift velocity will reach saturation at lower voltage. The saturation occurs near the mean thermal velocity of the carriers ($\sim 10^7$cm/s), where additional energy supplied by the field is transferred to the lattice instead of increasing the carrier velocity [42]. Due to this velocity saturation effect, the drain current in saturation is no longer following the square law as shown in Equation 2.14. Instead, it varies linearly with $V_G - V_T$ and is independent of the channel length L [43, 44]:

$$I_{Dsat} = W v_{sat} C_{ox}(V_G - V_T) \tag{2.20}$$

where W is the channel width, and v_{sat} is the saturation velocity.

(e) Channel Length Modulation

When the drain to source voltage V_{DS} increases beyond the saturation voltage V_{Dsat}, the pinch-off point will move towards the source. This is illustrated in Figure 2.12. ΔL is known as the channel length modulation by drain voltage. In this region, the carriers will be injected from the surface channel and travel towards the drain junction with saturation velocity. For the region between source and the pinch-off point, the one-dimensional MOSFET model is still valid. Hence, the device acts as if its channel length is shortened by ΔL. As a result, the drain current will be increased by a factor of $(1 - \Delta L/L)^{-1}$ [43]:

$$I_D = \frac{I_{Dsat}}{1 - (\Delta L/L)} \tag{2.21}$$

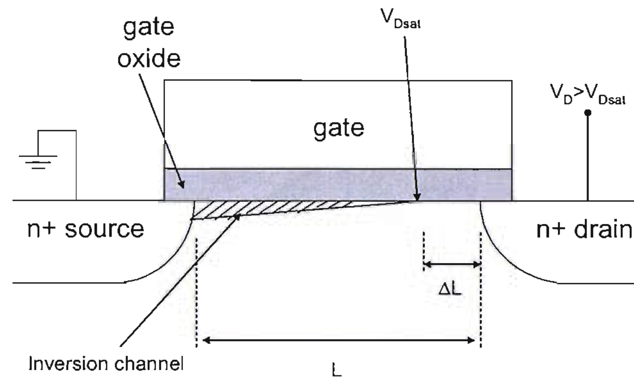

Figure 2.12: The schematic diagram of channel length modulation.

2.6 Vertical MOSFETs

The vertical MOSFET is a variant of the planar MOSFET which takes advantage of its geometrical structure [18–25]. The vertically grown structure will allow better control on the channel length and increase the channel width per transistor area and packing density. Various type of vertical MOSFET structures have been proposed and fabricated. The fabrication methods, advantages and disadvantages of each type of vertical MOSFET are discussed briefly in this section.

(a) Etched Pillar or Trench Structure

The etched pillar or trench structure (surround gate transistor) was first proposed by Takato *et al.* [27, 50]. The device schematic is shown in the Figure 2.13. The channel is along the sidewall of the etched pillar, and the gate length is defined by the timed-etched of a polysilicon spacer. The pillar height is the device parameter that determines the gate length. The source and drain regions are self-aligned to the gate and are formed by ion implantation. In addition to the advantages mentioned above, surround gate transistor (SGT) also allows better control of short-channel effects, ideal subthreshold slope and reduced substrate sensitivity in fully depleted operation [27, 50–52].

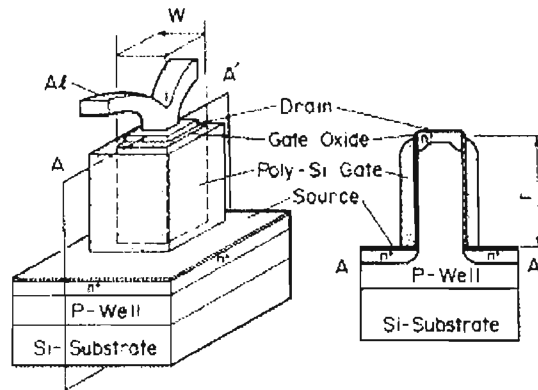

Figure 2.13: Schematic of the etched pillar or trench structure (after Takato *et al.* [27]).

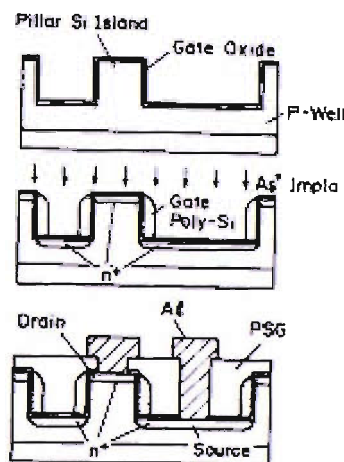

Figure 2.14: Fabrication process of the etched pillar or trench structure (after Takato *et al.* [27]).

The fabrication process of SGT is shown in Figure 2.14. First, the channel region is formed by ion implantation and subsequent diffusion. Then, vertical pillars are formed by lithography and anisotropic dry etch, followed by a sacrificial gate oxidation to remove etch damage on the vertical surface. After that, a thin layer of gate oxide is grown on the surface. Heavily doped polysilicon is then deposited and etched off by a reactive ion etching technique. Then, self-aligned source and drain are formed by ion implantation. Finally, the contact holes are formed, followed by the aluminium metallization.

One of the main disadvantages of this structure is the difficulty in gate length control, as the gate length is determined by a timed etch in the process. Thus, it is not easy to fabricate gate length of sub 0.1 μm by timed etch. It is also quite difficult to control a low

series resistance on the drain contact if the pillar is made very thin. In addition, it is not easy to make a contact to the gate. Furthermore, the overlap capacitances are consistently larger than those of the comparable lateral transistors [19].

(b) Vertical MOSFETs with Fillet Local Oxidation (FILOX) Process

The vertical MOSFETs with fillet local oxidation (FILOX) is similar to the etched pillar or trench structure [18, 19, 26]. Figure 2.15 compares the schematics of the vertical MOSFET with and without FILOX. It can be seen from Figure 2.15(a) that the gate to the top and to the bottom electrode overlap capacitance is huge due to the thin gate oxide. With the implementation of FILOX as shown in Figure 2.15(b), the oxide thickness between the gate track and the top and the bottom electrode increases. Therefore, the parasitic overlap capacitances are reduced significantly, and the device can be operated at higher frequency. In addition, the gate to the source and drain leakage current will be reduced due to FILOX.

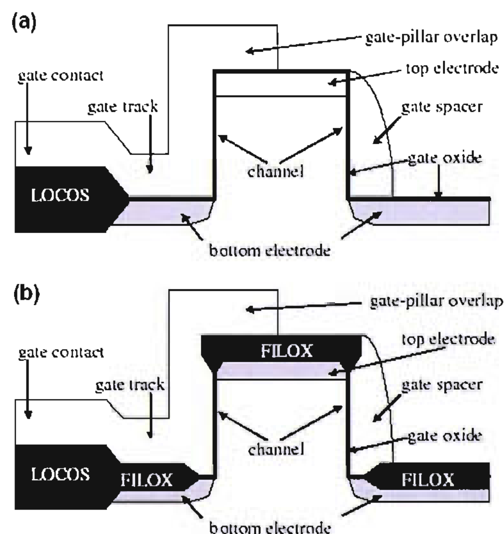

Figure 2.15: Schematics of the Vertical MOSFETs: (a)without FILOX process, (b)with FILOX process (after Gili *et al.* [19]).

Figure 2.16 shows the fabrication principle of the vertical MOSFETs with FILOX process. First, the vertical pillar is formed by etching. A thin layer of stress relief oxide is grown over the structure, followed by the deposition of a nitride layer. The nitride and the stress relief oxide on the horizontal plane are then removed by anisotropic etching. The layers only remain on the sidewall, which will serve as a protection layer for the vertical channel area. After that, a layer of oxide (FILOX) is grown over the exposed area by local oxidation.

This is followed by the removal of the nitride and the oxide on the sidewall by wet etching and the growth of the thin gate oxide on the sidewall. The major challenges in this design are the controllability and reproducibility of the FILOX oxidation.

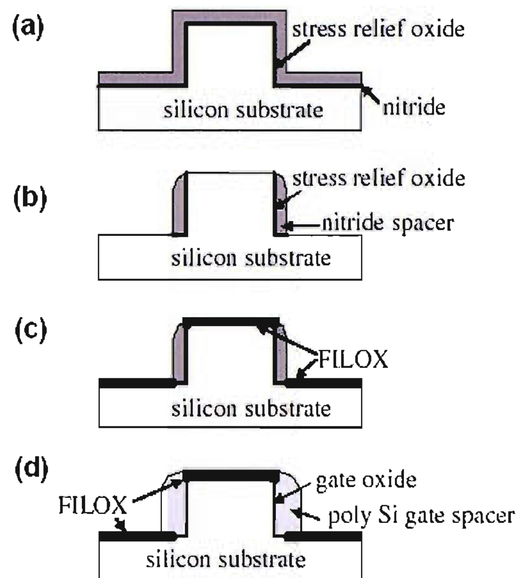

Figure 2.16: Fabrication principle of the Vertical MOSFET with FILOX process (after Gili *et al.* [19]).

(c) Molecular Beam Epitaxial (MBE) Growth Structure

Vertical MOSFET structures can be fabricated by using molecular beam epitaxial (MBE) techniques to grow the source, drain and channel of the device [20, 22, 53, 54]. The mesa structure is formed by dry etch. A schematic of the device is shown in Figure 2.17. The main advantage of this structure is that the channel is determined by the thickness of the epitaxial layer [53]. The device structure also allows very abrupt change in the doping, as the doping profile is formed by in-situ doping during the MBE growth of the channel [20, 54].

The process sequence of MBE growth structure is shown in Figure 2.18. The device is prepared by MBE growth of the source, channel and drain. After the mesa is etched, the gate oxide is grown on the vertical surface, followed by deposition of a polysilicon layer. The gate electrode is formed and passivation is performed on the device. Finally, contact holes are defined and the device fabrication is completed by metallization.

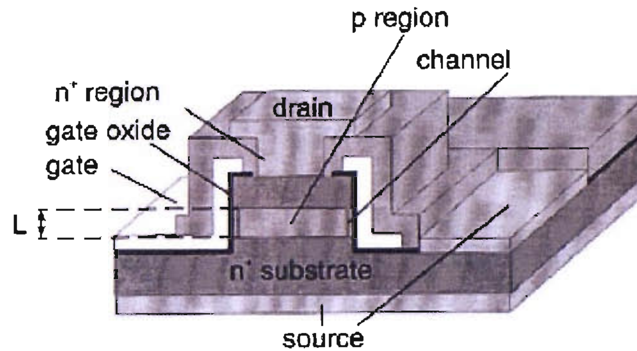

Figure 2.17: Schematic of the MBE growth structure (after Kaesen *et al.* [22]).

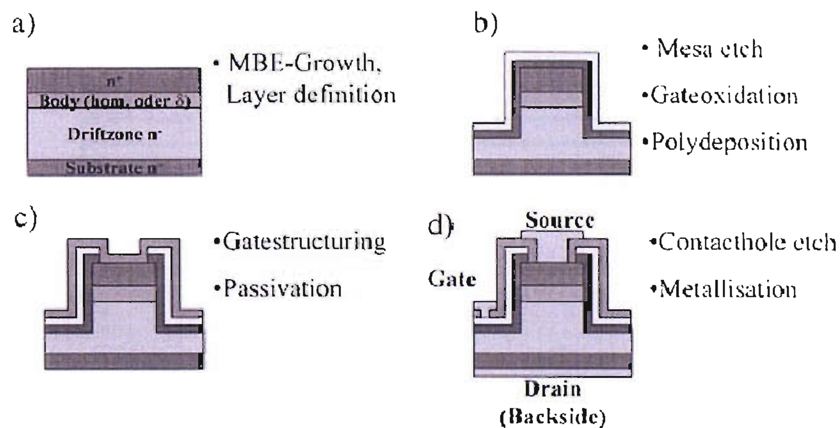

Figure 2.18: Fabrication process of the MBE growth structure (after Fink *et al.* [54]).

The drawback of this type of device is that there is a significant punch through path along the center of the structure. This could be prevented by using a high channel doping. However, this solution will result in a device with very high threshold voltage at shorter channel length [20, 22]. Large overlap capacitance between the substrate and gate is also a significant problem for this structure. This will degrade the performance of the device at high frequency.

(d) Selective Epitaxial Grown (SEG) Vertical Structure

The schematic of the selective epitaxial grown (SEG) vertical structure is shown in Figure 2.19(e). The channel length in the structure is defined by the SEG technique [55- 57]. The key feature of the SEG structure is that it has reduced gate to source and gate to drain overlap capacitances, which allows high speed applications.

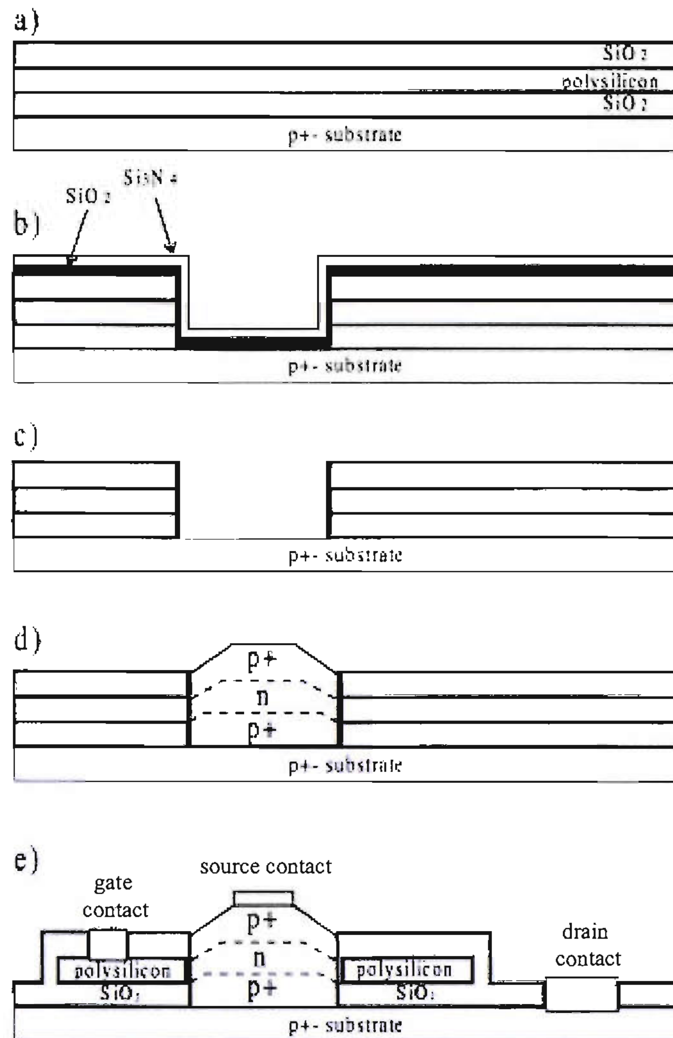

Figure 2.19: Fabrication process of the SEG grown structure(after Moers *et al.* [56]).

The fabrication process of the SEG structure is shown in Figure 2.19. First, layers of SiO_2/polysilicon/SiO_2 are deposited on the substrate. Package holes are etched by anisotropic reactive ion etching (RIE) to define the active transistor area. Gate oxide is then deposited by plasma enhanced chemistry vapour deposition (PECVD), followed by deposition of a gate oxide protective layer: silicon nitride. The gate oxide and the protective layer in the horizontal area is removed by anisotropic RIE, and the protective layer in the vertical wall is selectively removed to the gate oxide by wet chemical etching step in phosphoric acid (H_3PO_4). Then, the source and the drain region and the channel is formed by selective epitaxy performed by cold wall low pressure chemical vapour deposition (LPCVD). The upper oxide and polysilicon outside the transistor structure are removed by anisotropic RIE etching. Finally, contacts holes are defined, and the device is

completed after aluminium metallization. The main problem in SEG vertical MOSFET is the loss of source drain symmetry due to the channel to gate misalignment, which results in reduced transconductance [56].

2.7 Conclusion

The theory and operation of MOSFETs have been discussed in this chapter. Vertical MOSFETs have been introduced and different types of vertical MOSFETs have been described. By using a vertical architecture, the channel length can be better controlled and the packing density can be further increased. The scalability of MOSFETs has been a strong drive in the semiconductor industry. However, the short channel effects are increasingly significant as the features size of MOSFETs continue to scale down. This will affect the performance of MOSFETs. At one stage, the short channel effects will be overwhelming and the scaling of MOSFETs will fail. Although various methods have been used to reduce the short channel effects, these approaches can only extend the scalability of MOSFETs for a limited period. Eventually, a new type of device, with a new principle of operation, is required to replace MOSFETs in the future.

Chapter 3

Metal Oxide Tunneling Transistor

3.1 Introduction

As mentioned in previous chapters, the scaling of MOSFETs will reach its fundamental limitation due to short channel effects and quantum mechanical tunneling. It is thus important to research new types of switching logic devices so that MOSFETs can be replaced when the scaling fails. Many switching logic devices have been proposed of which the metal oxide tunneling transistor (MOTT) is one [34–41]. It was proposed in 1996 by Fujimaru *et al.* [36]. A schematic view of the MOTT is shown in Figure 3.1. The source, drain and gate are metals. The metal oxide in between the source and drain is the body of the transistor, which acts as the tunnel barrier. The principle of operation of the MOTT depends on the tunneling probability of electrons from the source to the drain through the tunnel barrier. This tunneling probability is modulated by the gate bias through the gate oxide, which is a high-k dielectric material.

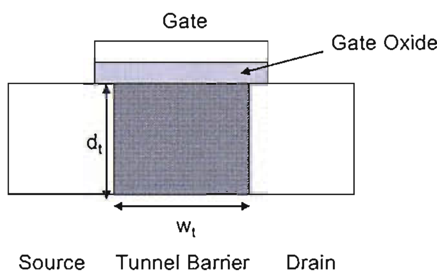

Figure 3.1: Schematic of the MOTT structure, d_t and w_t are the thickness and width of the tunnel barrier, respectively.

This chapter is a review of the MOTT. The principle of operation of the MOTT is explained, followed by an explanation of the advantages offered by the MOTT. After that, the design aspect and the experimental results of the MOTT are discussed. The fundamental problems in the MOTT are identified, and the approaches to improve the performance of the MOTT are suggested.

3.2 Principle of Operation of the MOTT

The current through the tunnel barrier is governed by Fowler Nordheim (F-N) tunneling modulated by the gate bias. As shown in Figure 3.2(a), F-N tunneling is the tunneling of electrons from the Fermi level of the electrode through the triangular barrier into the conduction band of the insulator [58–60]. The F-N tunneling current density J_{FN} can be expressed as [60]:

$$J_{FN} = \frac{q^3 E^2}{8\pi h m^* q\Phi_B} exp\left(\frac{-8\pi\sqrt{2m^* m_0 (q\Phi_B)^3}}{3qhE}\right) \tag{3.1}$$

where q is the electron charge, m_0 is the electron rest mass, m^* is the tunneling effective mass of the electron in the tunnel barrier, h is the Planck constant, E is the electric field across the tunnel barrier, and Φ_B is the barrier height with respect to the metal. It could be seen from Equation 3.1 that J_{FN} is exponentially dependent on Φ_B and E. In order to obtain a large F-N tunneling current, the tunnel barrier must have a low Φ_B and be thin enough for the drain bias to create a large electric field E across it.

Figure 3.2(a) shows a Metal-Oxide-Metal (MOM) energy band diagram without the effect of a gate electrode. When a positive drain bias V_D is applied, the effective potential thickness will decrease. Therefore, some electrons will be able to tunnel through the triangular barrier to the conduction band of the tunnel barrier. If a gate electrode is included in the structure, the potential profile of the tunnel barrier near the gate oxide and tunnel barrier interface can be modulated by the gate bias V_G. For positive V_G, the effective potential barrier will decrease further, as illustrated in Figure 3.2(b). More electrons will be able to tunnel to the conduction band of the tunnel barrier, and the F-N tunneling current will increase tremendously. Thus, the transistor is switched ON . For zero or negative V_G, the effective potential barrier will increase as shown in Figure 3.2(c). Few electrons will

be able to travel across the barrier, and the tunneling current is very low. Hence, the transistor is in the OFF state.

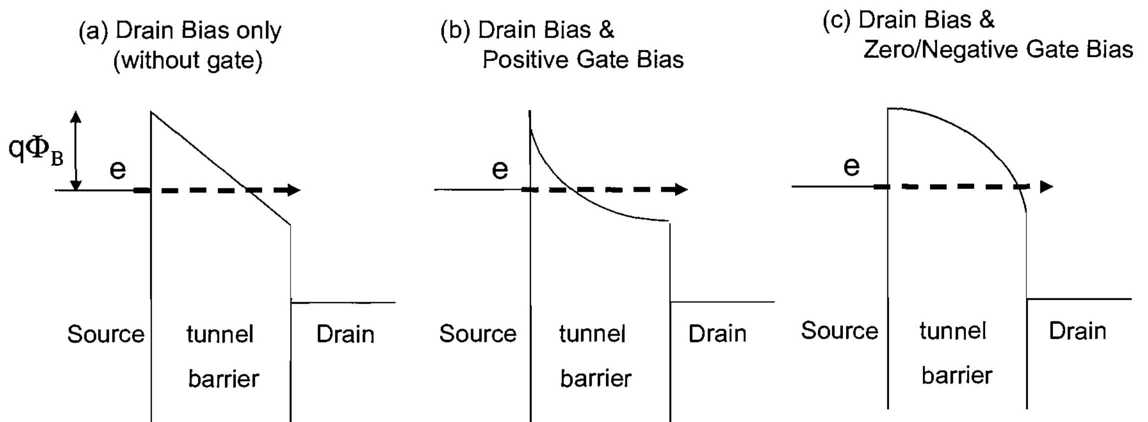

Figure 3.2: Energy band diagram of the MOTT: (a) with drain bias only (without gate bias), (b) with drain bias and positive gate bias, (c) with drain bias and zero or negative gate bias.

3.3 Carrier Transport Mode in the MOTT

For positive gate bias V_G, the MOTT is in the conduction mode. Rendell *et al.* [40] showed that there are three type of carrier transport modes in the MOTT. These carrier transport modes define the current-voltage characteristics of the MOTT, which is similar to those of the conventional semiconductor transistors [40]:

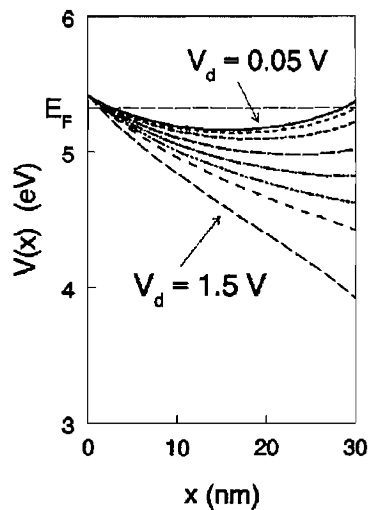

Figure 3.3: The potential barrier profiles near the gate oxide/tunnel barrier interface for different drain bias at positive gate bias [40].

(a) Shifting Double Barrier (SDB)

Shifting double barrier (SDB) is the transport mode occurs at a very low positive V_G, with a very small drain bias V_D (*e.g.* 0.05 V). In Figure 3.3, when a small V_D is applied to the device, the peak of the right barrier will be lowered, causing an asymmetrical double barrier in the potential well formed by the positive V_G. This is characterised by a rapid increase in the source-drain current, which varies linearly with V_D. In this mode of operation, the increase in the net tunneling current is the cause for the increase in the terminal current.

(b) Onset of the Single-Barrier Tunneling (OSBT)

Further increases in V_D will lead the device to go into the onset of the single-barrier tunneling (OSBT) mode. In this mode, the rate of increment of source-drain current decreases with increasing V_D. This is where the knee point of I-V characteristics is defined. Also, this is where the single-barrier tunneling becomes the dominant transport mechanism.

(c) Single-Barrier Tunneling (SBT)

At higher V_D, single barrier tunneling becomes the only carrier transport mode in the device. This is where the device exhibits saturation current, which is similar to the saturation regions in normal MOSFETs. The saturation is due to the resistance of the tunnel barrier, which will limit the current flow. In addition, after tunneling through the triangular barrier of the tunnel barrier, the electrons must travel through a low or negative electric field region of the amorphous tunnel barrier before reaching the drain electrode [38]. Charge-trapping effects and low electron mobility in that region will result in the build up of space charge in the tunnel barrier, which will limit the current flow.

3.4 Advantages of the MOTT

The MOTT offers many advantages that make it a potential candidate to replace conventional MOSFETs [34–41]:

(a) The transistor is non-crystalline

The MOTT can be fabricated with non-crystalline material. This allows arbitrary choice of substrates and possibility of development of multiple level circuits. These could be used for highly interconnected devices (*e.g.* neural network circuits) and for reducing the interconnect delays in ultra-high density integrated circuits.

(b) Small transistor active area

The size of the device can be minimised to nano-scale (about 15 nm). The metallic source and drain allow small contacts. In addition, the carriers are confined by the Schottky barrier formed between the silicon substrate and the metal electrodes [31, 38]. This will provide a built-in isolation between devices. Thus, the MOTT does not require large area for isolation.

(c) High speed performance

The source and drain of the MOTT are metallic and allows direct connection to the signal line. There will be no contact resistance between the source and drain and the signal line. Hence, the effective parasitic resistance is reduced and the RC charging times due to the parasitic components will be reduced. In addition, the drain current of the MOTT is due to the tunneling phenomena, which itself is a high speed process. Therefore, device speed in terms of pico-seconds can be achieved.

(d) Suppression of short channel effects

Short channel effects in the MOTT are suppressed because no minority carriers are involved in the current conduction. The current is contributed by the tunneling electrons. The operation of the MOTT only depends on its channel length. It is not influenced by the random location of dopant atoms in the channel, source and drain, which will create a fluctuation in threshold voltage of the MOSFETs.

(e) Similar operating characteristics as MOSFETs

There is no need for new circuit architecture to implement the MOTT, because it has similar operating characteristics as MOSFETs. Also, the cost of manufacturing is believed to be cheaper than MOSFETs due to the simpler device fabrication, as there is no PN junction formation during the process.

3.5 Design Aspect

In order to design a good device, the parameters that affect the performance of the device must be well understood so that the performance of the device can be optimised. The control of the gate over the source-drain F-N tunneling current is a major factor in the performance of the MOTT. It depends largely on the design and fabrication of a highly

efficient tunnel barrier and gate oxide.

(a) Tunnel Barrier

According to Equation 3.1, the F-N tunneling current is strongly suppressed with increases in the barrier height Φ_B of the tunnel barrier. Therefore, Φ_B should be carefully chosen to ensure a good device performance. For tunnel barrier with a low barrier height, the F-N tunneling current will be large, but Schottky emission is also likely to occur at room temperature. Schottky emission is the current transport mechanism caused by electrons overcoming the metal/oxide barrier at high temperature [4]. If the barrier height is high, Schottky emission can be effectively suppressed. However, a higher drain bias will be required to bring down the conduction band of the tunnel barrier for F-N tunneling to occur. This is undesirable because the drain bias for current CMOS technologies is typically 1 V [2]. Hence, it is important to choose a material with suitable barrier height.

(b) Gate Oxide

The thicker the gate oxide, the weaker the influence of gate field at the tunnel barrier [36]. As a result, the on state current will drop when the thickness of the gate oxide increases. Thus, a thinner gate oxide is required for a better transistor action. The simulation results by Rendell *et al.* [40] also showed that higher transconductance could be obtained from thinner gate oxide as the gate electric field can modulate the tunneling current effectively. The principles behind the scaling of the gate oxide are identical to those in MOSFETs. Also, the potential barrier between the gate electrode and both the source and drain electrode must be large enough to prevent gate leakage current to the source and drain electrodes. It has been shown that leakage current would be negligible if the gate barrier is greater than 2 eV [36].

(c) Dielectric Constant of the Tunnel Barrier and Gate Oxide

Ideally, the dielectric constant of the gate oxide ϵ_g should be greater than the dielectric constant of the tunnel barrier ϵ_t so that the gate bias could efficiently modulate the potential profile and control the F-N tunneling current. However, it is a general trend that the dielectric constant increases with a decrease in the barrier height of the oxide [5]. The device should be designed with a tunnel barrier with low barrier to allow large F-N tunneling current and a high barrier gate oxide to reduce the gate leakage current to source and drain. ϵ_g might be greater than ϵ_t in this case, and the gate bias would not be able

to modulate F-N tunneling current efficiently. Therefore, these two parameters must be considered carefully to optimise the performance of the MOTT.

3.6 Previous Experiments Result

The experimental results of the MOTT have been reported by two groups: the group of Fujimaru at Japan Advanced Institute of Science and Technology (JAIST) [34–37] and the group of Snow at Naval Research Laboratory in USA [38–41]. Their results are discussed in this section.

(a) Results of Fujimaru Group

A schematic of the device design of the Fujimaru group is shown in Figure 3.4(a) [35, 36]. Titanium oxide and silicon nitride were chosen as the tunnel barrier and the gate oxide, respectively. The tunnel barrier was grown laterally by anodic oxidation at the sidewall of a titanium film. The device dimensions used in the simulation are shown in Figure 3.4(a). In the simulation, the potential barrier height Φ_B between the tunnel barrier and metal electrodes was assumed to be 0.6 V, and the dielectric constants for the tunnel barrier and the gate oxide were assumed to be 5 and 3.9, respectively [35]. The simulation result in Figure 3.4(b) shows that for gate voltage between 0 to 2 V, the drain current will be in the range from 10^{-11} to 10^{-6} A [35].

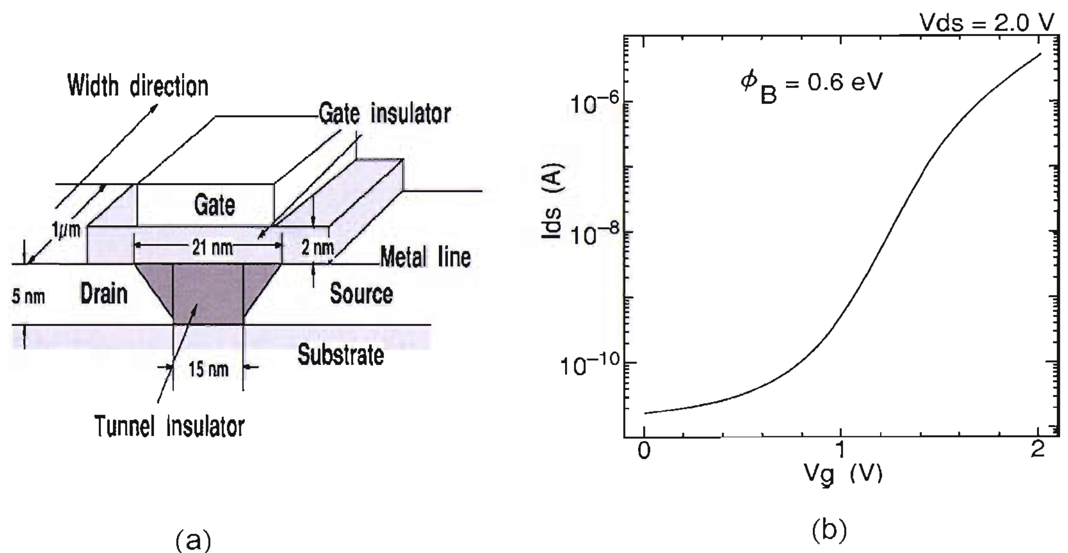

Figure 3.4: (a)Schematic of the MOTT structure designed by Fujimaru *et al.* [35]. (b) Simulated I-V characteristic of the MOTT design as shown in (a) (after Fujimaru *et al.* [35]).

Figure 3.5(a) and (b) show the I-V characteristics of the MOTT with different gate oxide thicknesses, fabricated by Fujimaru group. Transistor behaviour is reported at 90 K, but not at room temperature due to huge off-state current. One of the reasons that the device could not function properly at room temperature is due to the barrier height of the tunnel barrier. The barrier height was found to be 0.3 V [34, 35], that was only half of the expected value. The authors believed that if a barrier height of 0.6 V could be fabricated, then, the tunnel barrier would be effective in suppressing the Schottky current, and the device should be able to operate at room temperature [34]. Meanwhile, the gate oxide thickness of the MOTT can affect the I-V characteristics significantly. As shown in Figure 3.5(a), the MOTT with 38 nm gate oxide thickness exhibit poor on/off ratio. However, the MOTT with 10 nm gate oxide thickness gives an on/off ratio of five orders of magnitude, as shown in Figure 3.5(b). Therefore, the thickness of the gate oxide should be carefully controlled during the fabrication process.

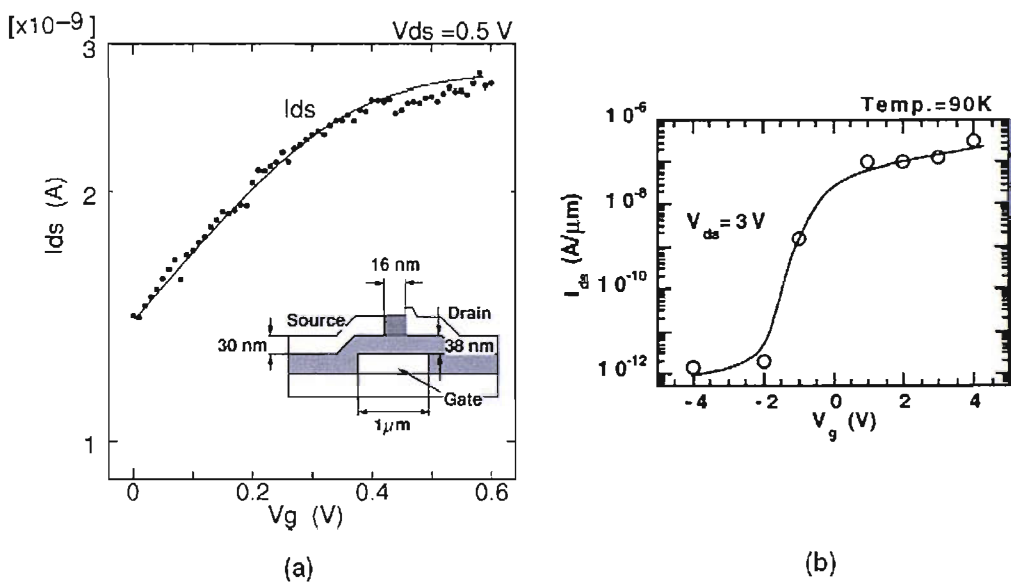

Figure 3.5: Experimental I-V characteristics of the MOTT at 90 K as designed by Fujimaru group: (a) gate oxide thickness=38nm [35], (b) gate oxide thickness=10nm [34].

(b) Results of Snow Group

A different device design for the MOTT was used by Snow *et al.* [38, 41], as shown in Figure 3.6. The tunnel barrier is fabricated using conducting tip atomic force microscope (AFM). Niobium oxide and aluminium oxide were used as the tunnel barrier and gate oxide, respectively. The aluminium oxide was chosen for the gate oxide because it has a high dielectric constant of approximately 10 and a large potential barrier of 2 V. However, there is one drawback in the device structure: a large parasitic gate capacitance is produced by the large buried gate metal finger. This is because the gate metal was defined by the optical photolithography, and that had resulted in a gate metal larger than the 40 nm tunnel barrier width. This leads to poor high frequency performance in the device operation. The group also used titanium oxide for the tunnel barrier in another experiment [41].

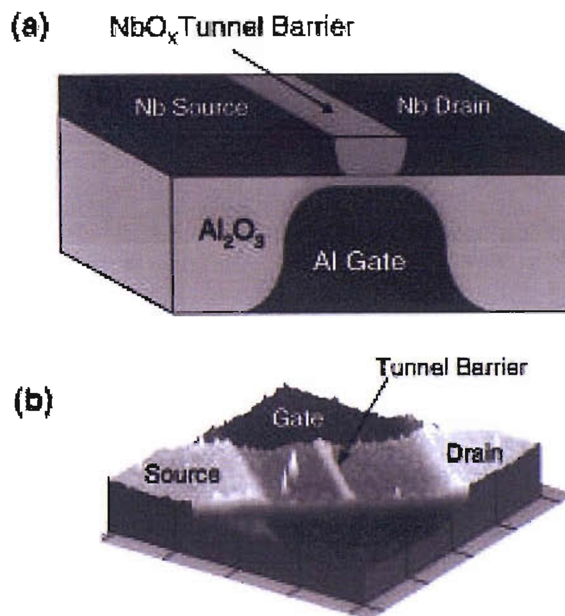

Figure 3.6: (a)Schematic of the MOTT structure designed by Snow *et al.* [38], (b)A $2\mu m \times 2\mu m$ AFM image of the tunnel junction region [38].

Figure 3.7 shows that the fabricated device (as shown in Figure 3.6) exhibits transistor behaviour at room temperature. However, it is still not efficient due to low on-state current. The group claimed that the performance of the device is limited by the transport properties of the amorphous oxide tunnel barrier. After tunneling through the barrier, the electron must travel across a low electric field region in the amorphous oxide layer. The charge-trapping effects and low electron-mobility will cause a buildup of space charge in the tunnel barrier, which will then limit the current flow. Therefore, further research is needed in order to improve the electron transport properties of amorphous oxide tunnel barrier. The authors have pointed out that large electron mobilities are shown in crystalline transition metal oxide at room temperature, and recent research had shown that the transition metal oxide could be crystallized by thermal annealing [38]. Therefore, crystallization on the metal oxide may improve the transport properties of the amorphous oxide tunnel junction.

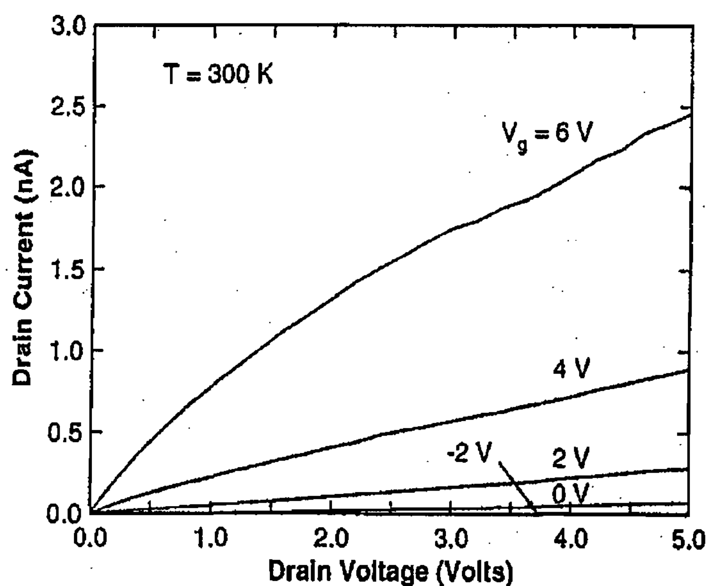

Figure 3.7: Experimental I-V characteristics of MOTT designed by Snow *et al.* [38] at room temperature.

3.7 Conclusion

The MOTT is a nanometer switching device with the conduction current controlled by the gate bias. The operating characteristics of the MOTT are similar to the MOSFET. The device performance is largely dependent on the properties of the transistor body, the tunnel barrier. The barrier height of the tunnel barrier relative to the metal electrode determines the magnitude of the MOTT conduction current, as F-N tunneling current is exponentially dependent on the barrier height. The advantages offered by the MOTT include non-crystalline device structure, suppression of short channel effects, high speed operation and small device active area.

The fabrication of the MOTT had been investigated by two different groups. The MOTT fabricated by the group of Fujimaru could only operate at low temperature, *e.g.* 90 K. At room temperature, the transistor cannot operate properly due to huge leakage current. Although the device fabricated by the group of Snow could exhibit transistor behaviour at room temperature, its on/off ratio is not good enough. Hence, it is very important to suppress the leakage current at room temperature. From Equation 3.1, it should be noted that F-N tunneling current is independent of the temperature. If the temperature dependent Schottky emission current can be reduced significantly, then the device should be able to show good transistor behaviour at room temperature. Moreover, a tunnel barrier fabricated by conducting tip AFM has problems in scalability and is not suitable for industry. It is essential to fabricate a scalable device that is industrially acceptable. Furthermore, due to the metal source, the MOTT can only exhibit electron F-N tunneling, which makes it impossible to realise complementary operation as in CMOS. In order to address the above stated issues, a new device design based on the MOTT design has been proposed and a suitable fabrication process has been investigated for the tunnel barrier in the following chapters.

Chapter 4

Vertical Metal Insulator Semiconductor Tunnel Transistor

4.1 Introduction

The vertical metal insulator semiconductor tunnel transistor (VMISTT) is a modified version of the MOTT. It is proposed to address the performance and fabrication issues in the MOTT. A schematic view of the VMISTT structure is shown in Figure 4.1. In this design, an oxide channel is sandwiched between the source and drain. The source/channel/drain columnar structure is fully surrounded by the gate oxide, covered by the gate metal. The principle of operation of a VMISTT is similar to that of a MOTT. However, it is different in two important aspects from the MOTT. First, by replacing the source by doped (single or poly crystalline) silicon and choosing an appropriate tunnel barrier and metal drain, it is possible to make both n-type and p-type devices for the complementary operations in the VMISTT, as will be discussed in more detail later in this chapter.

Secondly, the VMISTT has a vertical lay-out, which allows the metal oxide to be grown by controllable, scalable methods, such as evaporation or sputtering of a metal followed by thermal or plasma oxidation. This will lead to a better controlled oxide layer [39] and hence a strongly reduced leakage current as compared to the lateral MOTT. The thickness of tunnel barrier could be well defined to a precision of a single monolayer, unlike in conventional MOSFETs, which lateral features are defined lithographically. This will help to reduce the leakage current and hence enhance the performance of the VMISTT.

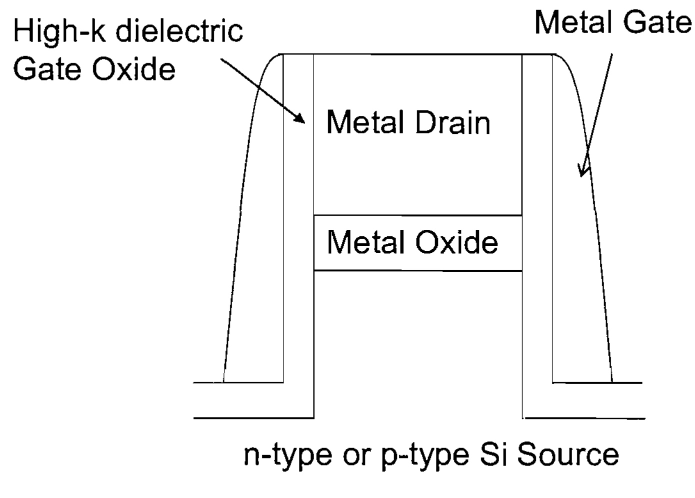

Figure 4.1: Cross-sectional view of the schematic diagram of a VMISTT.

It has been observed that double gate MOSFETs and vertical MOSFETs have more efficient gate control than their single gate counterparts [17, 27]. With a vertical structure, the gate electric field will be able to modulate the circumference region of the tunnel barrier, as can be seen in Figure 4.2(a). The inner region of the tunnel barrier will remain unmodulated, as the gate electric field cannot penetrate into this region. If an efficient tunnel barrier is fabricated such that other current transport mechanisms are suppressed, then the main leakage current will be the non-modulated F-N tunneling current. As a result, it is very important to have a small tunneling area to reduce the non-modulated F-N tunneling current. In Figure 4.2(b), with a smaller tunneling area, the gate-modulated F-N tunneling current will be the dominant current in the device. By advances in photolithography, the vertical design will allow the decrease in the tunneling area. The gate electric field will be able to modulate the whole tunnel barrier and possibly lead to complete gate control, which will result in an operation similar to a fully-depleted MOSFET, as illustrated in Figure 4.2(c). Therefore, it is believed that the proposed VMISTT will result in better performance at room temperature, as the surround gate structure will allow more efficient gate control than its single-gate counterparts [27].

Subsequent processing of the VMISTT can continue along the same lines as those for vertical MOSFETs, with the gate oxide replaced by a high-k dielectric [15, 19, 61]. There are intensive investigations underway on suitable high-k dielectrics in replacing SiO_2 as the gate oxide in conventional MOSFETs [5]. High-k dielectrics can achieve a smaller equiva-

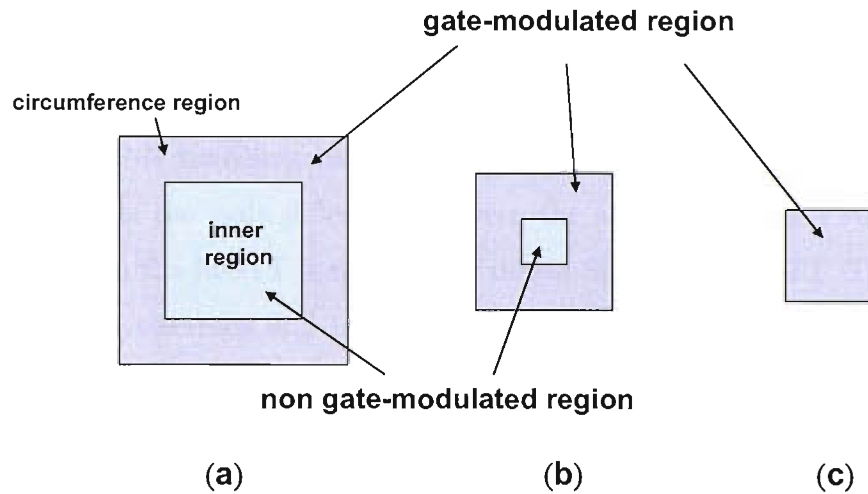

Figure 4.2: Schematics of the influence of the gate bias V_G on the VMISTT with different cross-sectional area: (a) the circumference of the columnar structure is modulated by V_G, the non gate-modulated region will contribute the non-modulated F-N tunneling current, (b) the non gate-modulated region decreases as the diameter of the columnar structure decreases, the magnitude of the non-modulated F-N tunneling current will decrease as well, (c) the diameter of the columnar structure is reduced such that V_G can effectively modulate all the region in the structure.

lent oxide thickness (EOT) than SiO_2 with a thicker physical thickness, which will result in a better gate modulation on the channel. These advantages are also applicable to the VMISTT. Gate oxide with higher dielectric constant than that of the tunnel barrier can enhance gate electric field penetration in the tunnel barrier, and hence allow better modulation of the tunnel barrier potential profile. Problems associated with electron mobility are not relevant to the VMISTT, easing the requirements for the high-k dielectric.

The structure and design aspects of the proposed VMISTT are discussed in this chapter, followed by studies on the effect of variation in the device parameters on the VMISTT performance. The results will include analytical solutions and simulations using the device simulation package ATLAS from SILVACO. The challenges in fabrication of the device are identified, and the problems related to the design of the VMISTT are addressed.

4.2 Principle of Operation of VMISTT

The principle of operation of the VMISTT is similar to that of the MOTT. It uses the gate modulation of F-N tunneling current from charge carriers in the source terminal of the transistor. One of the main difference between the MOTT and the VMISTT is that the metallic source in the MOTT is replaced by doped Si in the VMISTT. Therefore, the VMISTT can realise electrons and holes F-N tunneling through the selection of the Si source whilst the MOTT can only allow F-N tunneling of electrons to occur during the transistor operation. This feature of the MOTT makes it unable to perform complementary operations as in CMOS. However, as shown in Figure 4.3, a p-type VMISTT (p-VMISTT) can be realised by using a p-type Si (p-Si) for gate modulated hole F-N tunneling, and an n-type VMISTT (n-VMISTT) by using an n-type Si (n-Si) for gate modulated electron F-N tunneling. This feature of the VMISTT makes it possible to realise complementary operations as in CMOS.

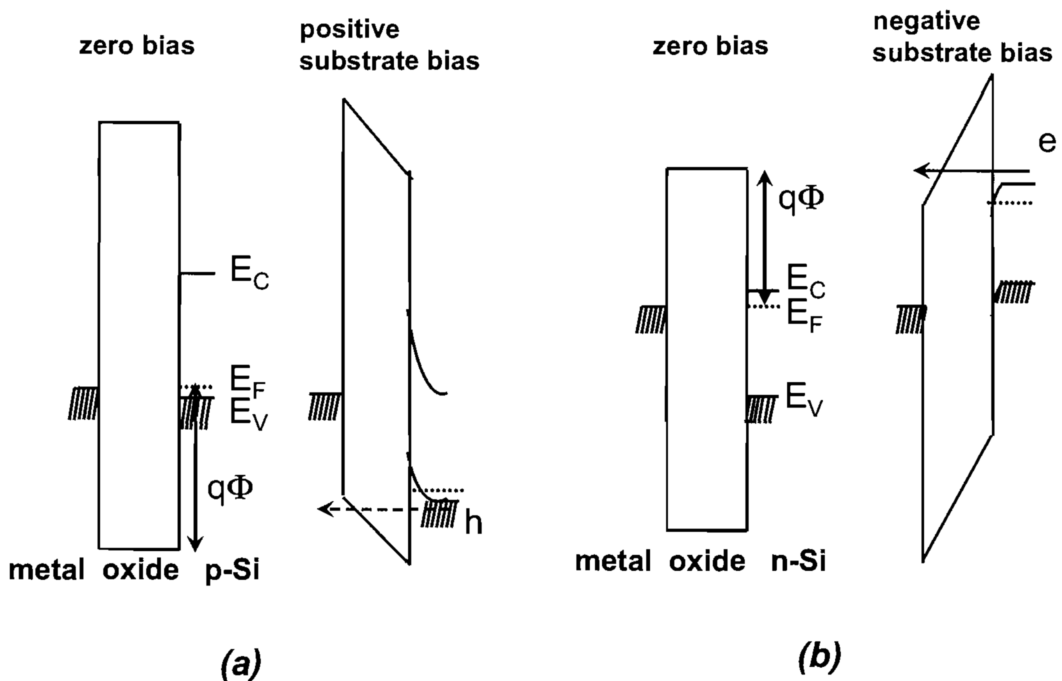

Figure 4.3: Schematic energy band diagrams of MOS capacitor with: (a) p-Si substrate at zero and positive substrate biases, (b) n-Si substrate at zero and negative substrate biases. e and h are the electrons and holes in the Si, respectively.

As the source is responsible for the supply of electrons or holes, it is essential to ensure that charge carriers tunnel only from the semiconductor to the drain electrode through the oxide channel and not from the metal drain to the semiconductor. This is possible

when metals with appropriate work function are selected for the drain terminal. The band diagrams in Figure 4.3 illustrate the situation. For a p-VMISTT in Figure 4.3(a), the holes tunnel from the p-Si through the triangular barrier at increased negative drain bias. A high work function of the drain metal ensures that the barrier for the electrons from the drain to the p-Si is large so that the electron current is minimized. In this case, platinum Pt is a suitable candidate for the metal drain in the p-VMISTT. It has a relatively high metal work function, which is 5.6 eV [4]. On the other hand, for an n-VMISTT shown in Figure 4.3(b), a low value of the metal work function ensures the electron tunneling from the n-Si to the metal drain and suppresses the hole current in the opposite direction. Therefore, aluminium Al with its relatively low work function of 4.1 eV [4] is a suitable candidate for the metal drain in the n-VMISTT.

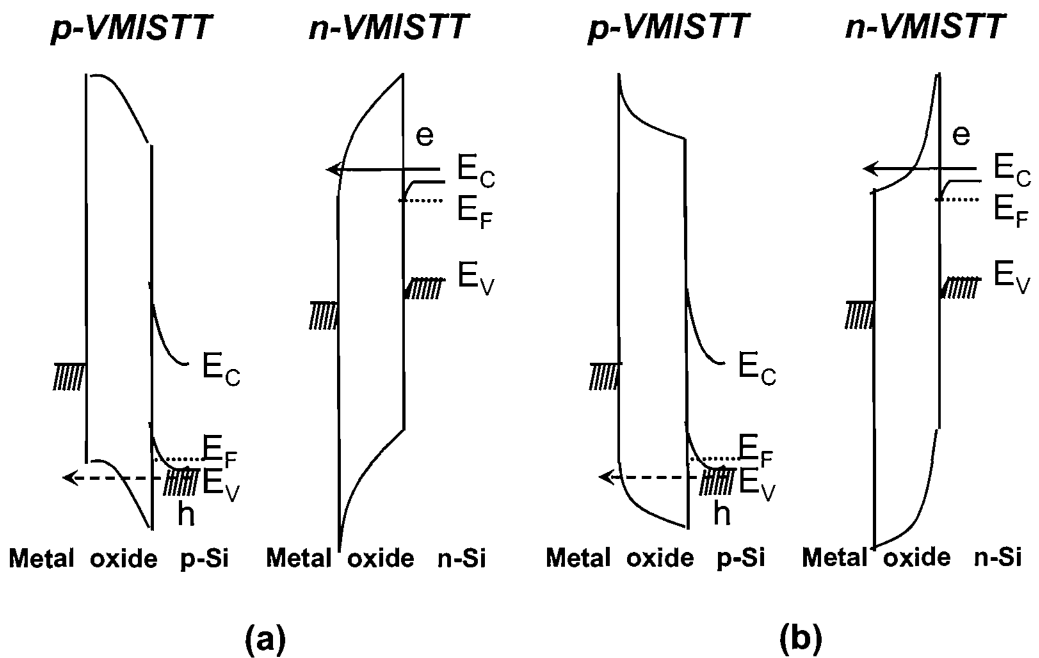

Figure 4.4: Schematic energy band diagrams of the complementary operations of VMISTT for (a) zero or negative gate bias (b) positive gate bias.

With the application of the gate bias, the complementary operations can be realised with the p-VMISTT and the n-VMISTT. As shown in Figure 4.4(a), at zero or negative gate bias, the F-N tunneling in the p-VMISTT will be enhanced, while the F-N tunneling in the n-VMISTT will be suppressed. On the other hand, Figure 4.4(b) shows that at positive gate bias, the F-N tunneling in the n-VMISTT will be enhanced, and the F-N tunneling in the p-VMISTT will be suppressed. This is similar to the operation of a CMOS inverter (refer to Section 2.4).

4.3 Simulation Method

To study the characteristics and performance of the VMISTT, the SILVACO device simulator ATLAS is used to simulate the tunnel barrier potential profile and the I-V characteristics of the VMISTT. ATLAS is a physically-based device simulator [62]. The user need to specify the physical structure and models of the device, as well as the bias conditions. The physical structure is divided into segments. Using a set of differential equations derived from Maxwell Equations, ATLAS can predict the electrical characteristics of the device on each segment, based on the models and the bias condition, and is hence able to simulate the electrical performance of the device [62].

Figure 4.5 shows the device structure used for the simulations of an n-VMISTT. For the ease of calculation, a two dimensional vertical device structure is considered. Based on the discussion in Chapter 3, a typical set of device parameters was selected for the VMISTT simulations. Unless otherwise stated, all the device parameters used in the simulation will be based on the values shown in Table 4.1. The effect of these parameters on device performance will be presented later.

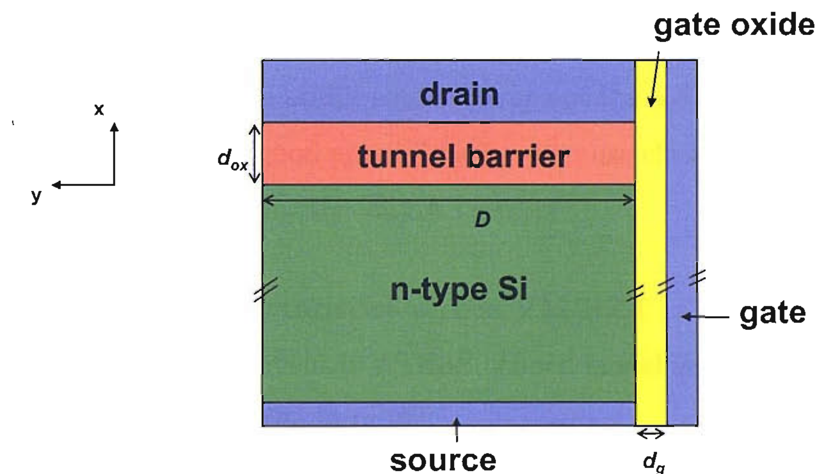

Figure 4.5: Schematic of an n-VMISTT used for ATLAS simulations.

Table 4.1: Device parameters used for ATLAS simulations.

device parameter	symbol [units]	default value
device depth	D [nm]	1000
tunnel barrier thickness	d_{ox} [nm]	10
gate oxide thickness	d_g [nm]	2
n-Si doping concentration	N_D [cm^{-3}]	10^{19}
barrier between oxide and n-Si	Φ_B [V]	0.6
dielectric constant of tunnel barrier	ϵ_r	30
dielectric constant of gate oxide	ϵ_g	100
effective mass constant of carrier	m^*	1

(a) Simulations of the Tunnel Barrier Potential Profile

In ATLAS, there is no discontinuity in the potential profile at an oxide/semiconductor interface. Hence, the potential profile of an n-VMISTT cannot be simulated using an n-Si source. This is because in the real case, there is a discontinuity in the potential profile due to the formation of the Schottky contact when the Si comes in contact with the oxide [63]. However, the potential profile can be simulated by replacing the Si source with a metallic source in the ATLAS program, as ATLAS assumes a Schottky contact between the oxide and the metal. Using a metallic source to replace the n-Si for the potential profile simulation of an n-VMISTT is a good approximation because electron is the charge carrier in both cases (see Appendix C.1 for the ATLAS script).

(b) Simulations of I-V Characteristics of the VMISTT

To simulate the F-N tunneling current in ATLAS, *fnord* model is triggered [62]. The F-N tunneling current in ATLAS has the form [62]:

$$J_{FN} = F_{AE} E^2 exp(-F_{BE}/E) \tag{4.1}$$

$$F_{AE} = \frac{q^3 m_0}{8\pi h m_e (q\Phi_B)} \tag{4.2}$$

$$F_{BE} = \frac{8\pi}{3qh}\sqrt{2m_e(q\Phi_B)^3} \tag{4.3}$$

where E is the electric field across the tunnel barrier; $m_e = m^* m_0$, m^* and m_0 being the

tunneling effective mass and electron rest mass, respectively; h is the Planck's constant and Φ_B is the barrier height between the oxide/Si interface. For a specified Φ_B, the parameters F_{AE} and F_{BE} can be determined from Equations 4.2 and 4.3. Based on the parameters given, ATLAS can simulate the F-N tunneling current at the oxide/Si interface (see Appendix C.2 for the ATLAS script).

(c) Leakage current in the VMISTT

Negligible gate leakage is assumed in the simulation. This is justifiable if the gate oxide energy gap and the band off-set are considerably higher than those of the tunnel barrier. In ATLAS, this is done by setting the *fnord* parameters of the gate oxide to zero.

Due to the low value of Φ_B, thermionic emission of carriers from the Si source into the conduction band of the oxide can occur at high temperatures [63]. This is known as Schottky emission [4]:

$$J = A_{SC}T^2 exp\left[-\frac{q}{kT}\left(\Phi_B - \sqrt{\frac{qV}{4\pi\epsilon_r\epsilon_0 d_{ox}}}\right)\right] \tag{4.4}$$

where A_{sc} is the effective Richardson constant, and has a value of 120 A/cm^2/K^2 [4]; T is the temperature and k is the Boltzman's constant. From the expression, it is noted that the Schottky current increases exponentially with the increase in temperature. The simulation results can only provide the F-N tunneling current. Thus, in the following analysis, Schottky current at a specified temperature will be added to the F-N tunneling current to account for the thermally activated leakage current.

4.4 Verification of ATLAS Model

To verify the I-V characteristics of an n-VMISTT simulated by ATLAS, the F-N tunneling current is manually calculated from the gate-modulated tunnel barrier potential profile simulated by ATLAS, using a metallic source as mentioned in Section 4.3. Firstly, the tunnel barrier potential profiles at different sets of gate and drain biases are obtained from ATLAS simulation based on the device parameters shown in Table 4.1. After that, for each set of gate and drain biases, the F-N tunneling current is manually calculated from the potential profiles. The following example describes the method used to calculate the

F-N tunneling current at $V_G = 3$ V and $V_D = 3$ V. The same procedure is applied to all the other sets of gate and drain biases.

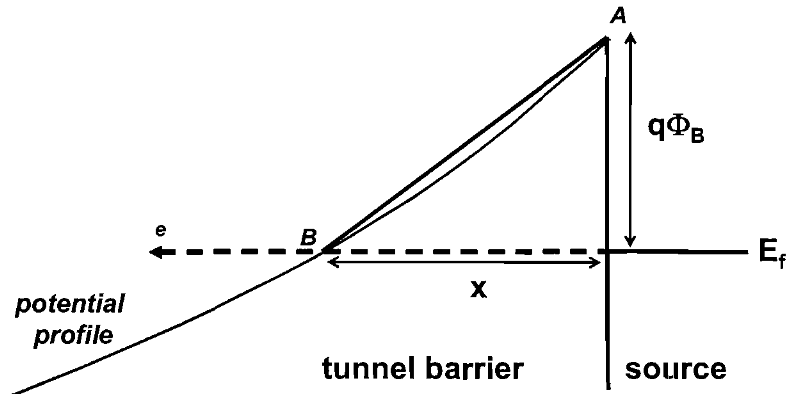

Figure 4.6: The estimation of electric field at the Fermi level. The plot shows a zoom-in potential profile near the source terminal at depth=0.1 nm. The slope of the line $AB = \Phi_B/x$ give an estimation of the electric field at the Fermi level.

Figure 4.6 shows the tunnel barrier potential profile at depth=0.1 nm below the gate oxide at $V_G = 3$ V and $V_D = 3$ V. The horizontal broken line drawn across the potential profile indicates the source Fermi level E_f. The effective electric field E can be approximated from the slope of the line AB, which is Φ_B/x. Then, using Equations 4.1 to 4.3, the F-N tunneling current at that specified depth can be determined. The same procedure is repeated for the potential profiles at different depths. The F-N tunneling current density of an n-VMISTT at different depth is shown in Figure 4.7. The total current can be obtained by performing an integration on the curve. However, as the curve cannot be expressed in a simple exponential function or a polynomial function, the total current is estimated by summing the area of rectangles under the curve as shown in Figure 4.7.

Figure 4.7 shows that the area under the curve is divided into 4 regions. Region A corresponds to the area under the curve for depth<0.4 nm. Due to the quantum mechanical reflection from the oxide/Si interface, the carriers cannot reside as close as possible to the interface. This is known as carrier quantum confinement effect [64, 65]. A 0.4 nm depletion region is generally estimated to account for this phenomenon [64]. Hence, it is required to exclude region A from the calculation of the total current. The total area under the curve in region B, C and D is estimated from the area of the rectangles. It is noted that the interval between two consecutive rectangles is 0.1 nm in region B and 1 nm in region C. A

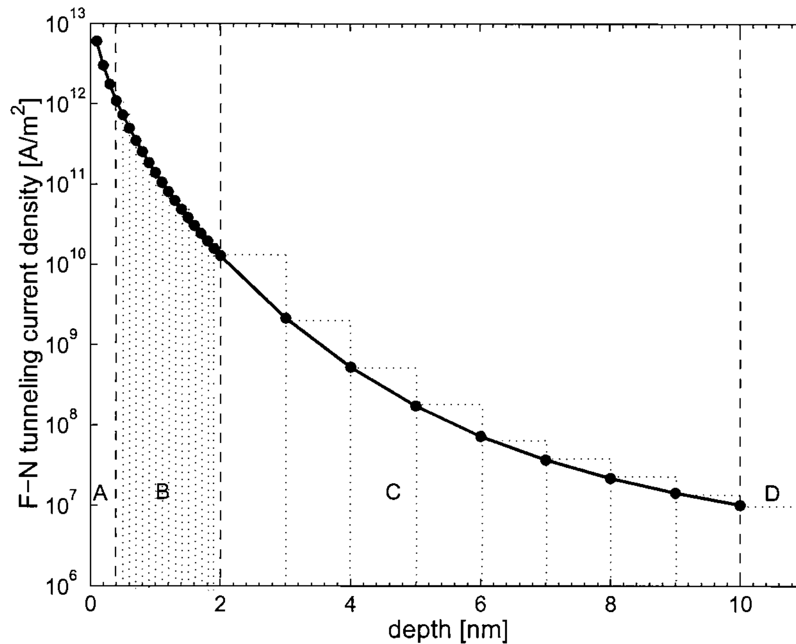

Figure 4.7: Estimated F-N tunneling current density at different depths. The graph is divided four regions: A, B, C, D, as explained in the text. The dotted line rectangles are visual aid for readers to understand the calculation method of the total current.

smaller interval is required in region B because the value of the tunneling current decreases sharply as the depth increases. Therefore, higher accuracy is required. In region C, the variation in current is not as significant as in region B, hence, a 1 nm interval between two consecutive rectangles is a good approximation.

Figure 4.8 shows the variation of the modulated potential profile along the depth of the tunnel barrier at V_D=1 V. It is observed that the potential profile near the gate oxide interface is strongly modulated by V_G, and the effect of the gate modulation decreases as the depth increases. At a depth of 10 nm, the potential profile is almost the same as the non-modulated potential profile. This suggests that the gate electric field can only effectively modulate the tunnel barrier potential profile up to a depth of 10 nm. Therefore, for depth>10 nm, the total non-modulated tunneling current can be estimated from the area of a rectangle of depth=990 nm, as the total depth is 1000 nm. The total current is the sum of the rectangles area in region B, C and D. Using the same procedure for other sets of V_G and V_D, the characteristics of drain current I_D versus V_G can be obtained.

Figure 4.9 compares the ATLAS simulated (see Appendix C.2 for the ATLAS script) and

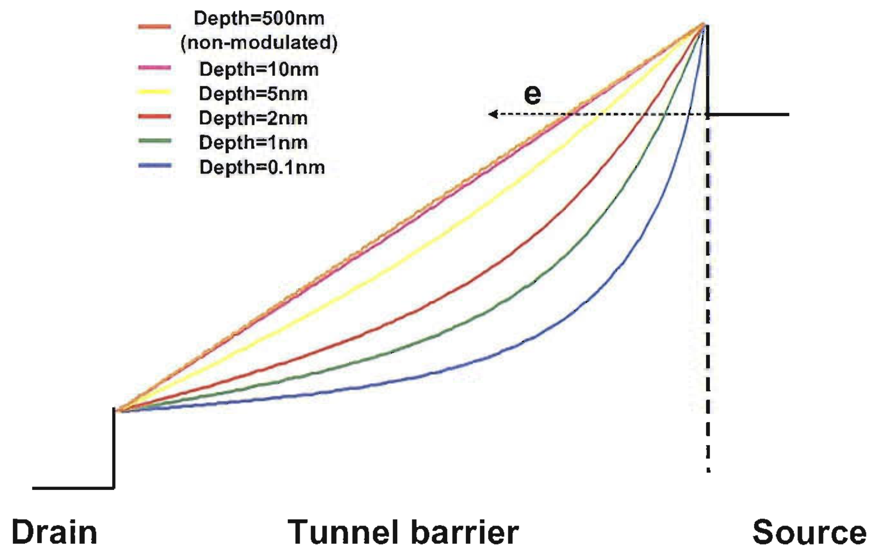

Figure 4.8: ATLAS simulated potential profiles of an n-VMISTT at V_D=3 V and V_G=3 V.

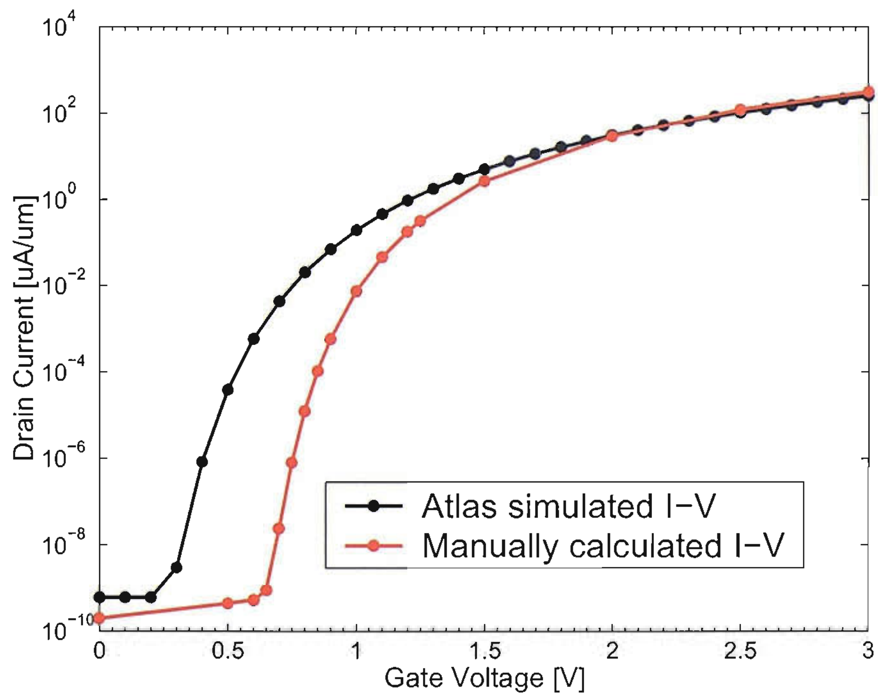

Figure 4.9: The comparison of the ATLAS simulated I-V characteristics and the manually calculated I-V characteristics from the tunnel barrier potential profile. Refer to Table 4.1 for the device parameters.

the manually calculated I-V characteristic of an n-VMISTT based on the device parameters in Table 4.1. It is noted that the I-V characteristics obtained from these two different methods are comparable. There is one major difference between the two curves: the onset of the current in the ATLAS simulated I-V characteristic occurs at a lower V_G. This can be explained by the method that ATLAS uses in the simulation. The F-N equation in Equation 4.1 used by ATLAS is only valid in a one dimensional model, where the electric field E is constant throughout the tunnel barrier length. But, the VMISTT with gate modulation is a two dimensional model, in which the electric field varies along the tunnel barrier length. This will lead to inaccuracy in the ATLAS simulation results.

Figure 4.10 shows the tunnel barrier potential profile for different V_G at depth=0.1 nm and V_D=1 V. In theory, the F-N tunneling current is determined by the effective electric field E_B at the source Fermi level E_f, indicated by point B in Figure 4.10. However, ATLAS does not take E_f into account: it uses the electric field E_A at the oxide/Si interface, i.e. point A in Figure 4.10, to calculate the F-N tunneling current. This approach is acceptable at low and at high V_G regions because E_A and E_B in the respective regions are similar. However, it will give inaccurate results in the intermediate V_G region (0.3 V $< V_G <$ 1.5 V).

In Figure 4.10(a), the effective electric field E_B is mainly due to the non-modulated potential profile, E_B at E_f is equal to E_A at the oxide/Si interface. At high V_G, E_B is due to the gate-modulated potential profile. As shown in Figure 4.10(c), E_A is similar to E_B. Hence, at low V_G and high V_G, the current density obtained by these two different methods should be of similar magnitude. For intermediate V_G, the position of E_f is important because it determines the V_T of the transistor. As shown in Figure 4.10(b), for $V_G = 0.5\ V$, ATLAS sees that E_A is due to the gate modulated potential profile, which corresponds to a huge current density in the ATLAS simulated I-V characteristic. Nonetheless, E_B at E_f is actually due to the non-modulated potential profile. Hence, the current density of the transistor remains low, and rises sharply only after $V_G >$ 0.65 V.

The above comparison shows the inaccuracy in ATLAS simulations in intermediate V_G region. Also, the onset of the current in ATLAS simulation is independent of the oxide/Si barrier height Φ_B. All these will affect the determination of subthreshold slope and V_T of the transistor. Therefore, in order to study the effect of Φ_B on the transistor performance,

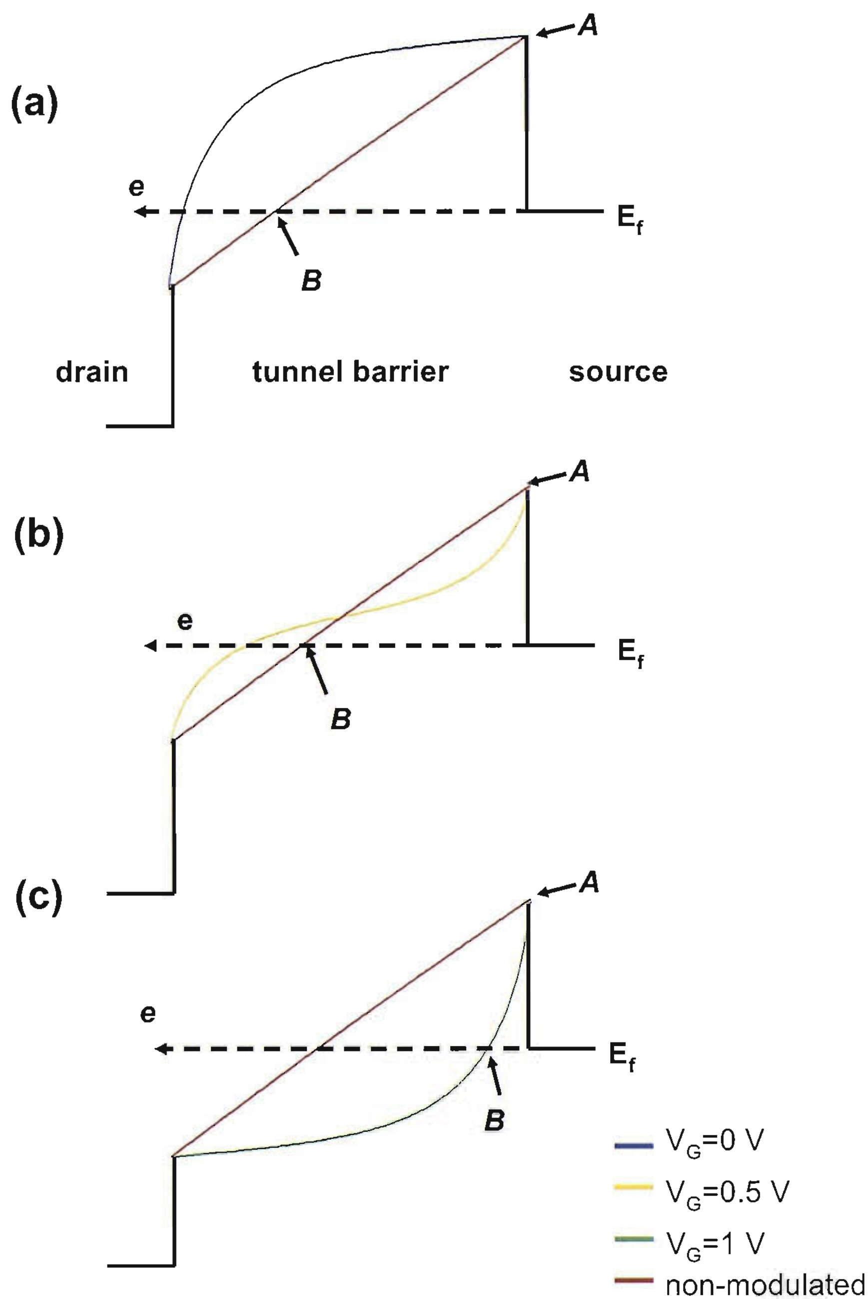

Figure 4.10: The simulated tunnel barrier potential profile for different V_G at depth=0.1 nm: (a) V_G=0 V at depth=0.1 nm and non-modulated potential profile, (b) V_G=0.5 V at depth=0.1 nm and non-modulated potential profile, (c) V_G=1 V at depth=0.1 nm and non-modulated potential profile. The non-modulated potential profile is taken at depth=500 nm. Refer to Table 4.1 for the device parameters.

the manually calculated I-V characteristics is used. On the other hand, as ATLAS simulations produce similar current density as that of the manually calculated I-V characteristic at high V_G, ATLAS is used to simulate the I-V characteristics of the VMISTT to investigate the effect of oxide dielectric constant and the tunnel barrier thickness on the current density at high V_G.

4.5 Simulation Results and Discussion

The effect of the device parameters on an n-VMISTT is studied in this section. Similar results are expected for a p-VMISTT. The performance parameters that are of interest are the off-state current I_{off}, the on-state current I_{on}, the on-off current ratio I_{on}/I_{off}, the subthreshold slope SVT, and the threshold voltage V_T. The typical values of these parameters for a MOSFET are shown in Table 4.2. For the analysis in this section, I_{off} and I_{on} are defined as the current density at $V_G = 0$ V and at $V_G = 1.5$ V, respectively. SVT can be determined from the maximum slope in the I-V characteristic. As discussed in Section 2.3, a steep subthreshold slope is essential because it indicates that the transistor can be switched off and on at a small variation of V_G. V_T of a VMISTT is the gate voltage at which the potential profile is sufficiently modulated to allow a large flow of F-N tunneling current. It is defined here as the V_G at the maximum subthreshold slope.

Table 4.2: Typical values of a MOSFET [2, 43].

performance parameter	**symbol [units]**	**value**
on-state current	I_{on} [μA/μm]	10^3
off-state current	I_{off} [μA/μm]	10^{-2}
on-off current ratio	I_{on}/I_{off}	$10^5 \sim 10^6$
subthreshold slope	SVT [mV/dec]	70~100
threshold voltage	V_T [V]	0.2

(a) Effect of Temperature

As the Schottky current is exponentially dependent on temperature, the device operating temperature T can have a great impact on the transistor performance. Figure 4.11 shows the effect of temperature on an n-VMISTT I-V characteristics. The effect of temperature on the performance parameters are summarized in Table 4.3. It is observed that the

temperature only affects the low V_G region. At 77 K, the performance parameters are the same as that with F-N tunneling only. This implies that Schottky emission can be neglected at 77 K and I_{off} is due to the non-modulated F-N tunneling current only. From 77 to 200 K, there is only a slight increment in I_{off}. It is due to the thermally activated Schottky current. However, it does not have significant effect on the performance parameters. At 300 K, I_{off} is sharply higher because of the Schottky current. This deteriorates all the performance parameters: I_{on}/I_{off} decreases by about five orders of magnitude, SVT increases from 14.21 to 40.51 mV/dec, and V_T increases from 0.75 to 0.95 V. From the analysis, it is shown that the VMISTT can be improved dramatically if is operated at lower temperature. It should be noted that the Schottky current has no effect on the high V_G region.

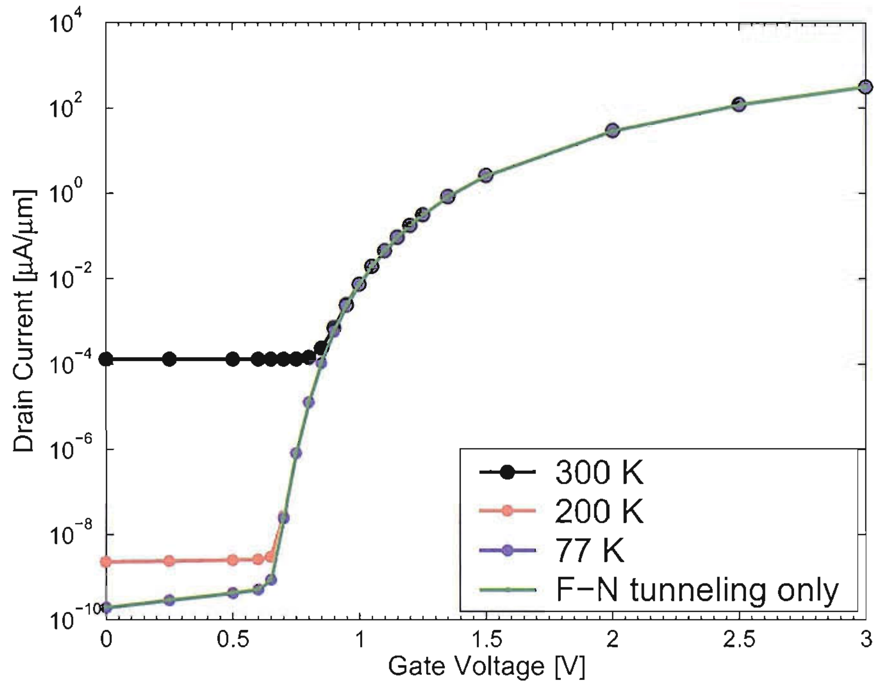

Figure 4.11: Manually calculated I-V characteristics of an n-VMISTT at $V_D = 1$ V, at different temperatures. Refer to Table 4.1 for device parameters used in the simulations.

Table 4.3: The performance parameters of an n-VMISTT at different temperatures.

Temperature [K]	I_{off} [μA/μm]	I_{on} [μA/μm]	I_{on}/I_{off}	SVT [mV/dec]	V_T [V]
300	1.33×10^{-4}	2.64×10^{0}	1.99×10^{4}	40.51	0.95
200	2.28×10^{-9}	2.64×10^{0}	1.16×10^{9}	14.21	0.75
77	2.00×10^{-10}	2.64×10^{0}	1.32×10^{10}	14.21	0.75
F-N tunneling only	2.00×10^{-10}	2.64×10^{0}	1.32×10^{10}	14.21	0.75

(b) Effect of Barrier Height

The oxide/Si barrier height Φ_B is an important parameter of a VMISTT. A low value of Φ_B is essential as this will ensure the onset of F-N tunneling current at low V_D so that it is comparable to conventional MOSFETs. Hence, due to its relatively high barrier, SiO_2 is not a suitable candidate for the tunnel barrier. However, if Φ_B is too low, the charge carriers will have enough energy to overcome the barrier through Schottky emission at high temperature. This leakage current can overwhelm the gate modulated F-N tunneling current, and affect the device performance, as shown in the previous section.

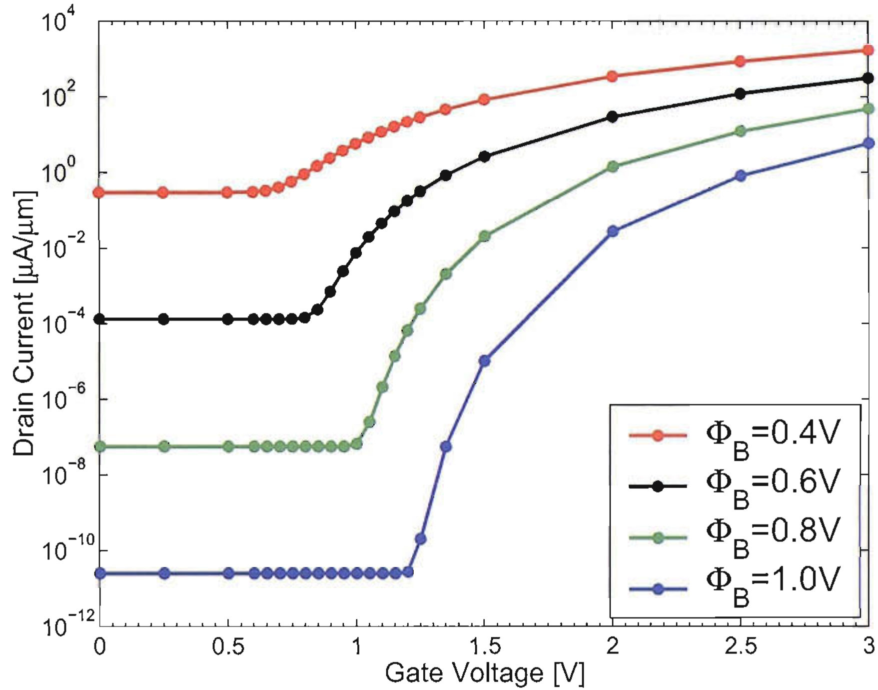

Figure 4.12: Manually calculated I-V characteristics of an n-VMISTT at V_D = 1 V and 300 K, for different Φ_B. Refer to Table 4.1 for device parameters used in the simulations.

Figure 4.12 shows the I-V characteristics of an n-VMISTT at V_D = 1 V and 300 K for different Φ_B. The effect of Φ_B on transistor performance is summarized in Table 4.4. The simulation results show that Φ_B has a significant effect on the device performance. The lower the Φ_B, the higher the I_{off} and I_{on}. However, I_{off} has a higher increment rate than I_{on} as Φ_B decreases. The I_{off} is mainly contributed by the Schottky current, and the I_{on} is due to the gate modulated F-N tunneling current. By comparing Equation 4.1 and 4.4, it can be seen that the Schottky current is more exponentially dependent on the variations of Φ_B than the gate modulated F-N tunneling current. This results in a decrease in I_{on}/I_{off} as Φ_B decreases, which is undesirable as a drain current swing of about 5 to 6 orders of

magnitude is required [2]. The increase of I_{off} at lower Φ_B also affects SVT. It is noted that SVT increases dramatically as Φ_B decreases. On the other hand, V_T increases as Φ_B increases. This is because the onset of drain current is dependent on Φ_B, as explained in Section 4.4.

From Table 4.4, it is suggested that $\Phi_B = 0.6$ V is a suitable oxide/Si barrier height for a n-VMISTT. Although the drain current swing is about four orders of magnitude only, it is higher than that of $\Phi_B = 0.4$ V, and it also has steeper subthreshold slope. For $\Phi_B > 0.6$ V, the I_{on}/I_{off} and SVT are superior to that at $\Phi_B = 0.6$ V, but the I_{on} values are much lower. In addition, the V_T at $\Phi_B = 0.6$ V is also lower than those with higher barrier.

Table 4.4: The effect of the oxide/Si barrier height Φ_B on n-VMISTT at 300 K.

Φ_B [V]	I_{off} [μA/μm]	I_{on} [μA/μm]	I_{on}/I_{off}	SVT [mV/dec]	V_T [V]
0.4	3.03×10^{-1}	8.51×10^{1}	2.81×10^{2}	102.05	0.85
0.6	1.33×10^{-4}	2.64×10^{0}	1.99×10^{4}	40.51	0.95
0.8	5.84×10^{-8}	2.08×10^{-2}	3.56×10^{5}	23.54	1.10
1.0	2.57×10^{-11}	1.07×10^{-5}	4.18×10^{5}	17.80	1.35

(c) Effect of Drain Bias

The magnitude of drain bias V_D determines the magnitude of the non-modulated F-N tunneling current. Figure 4.13 and Table 4.5 show the effect of V_D on the I-V characteristics of an n-VMISTT at different temperatures. It is observed that V_D only affects the I-V characteristics at low V_G. At high temperature, V_D has no significant impact on the I-V characteristics. This is because the magnitude of the Schottky current is so large at high temperature that it overwhelms the effect of V_D. However, at 77 K, the Schottky current is strongly suppressed. It is hence noted that a lower value of V_D can reduce I_{off} significantly and improve I_{on}/I_{off}, SVT, and V_T. This is because at low temperature, I_{off} is due to the non-modulated F-N tunneling current only. Lower V_D will increase the effective potential thickness of the non-modulated potential profile and thus reduce the non-modulated F-N tunneling current. Therefore, a lower V_D can be chosen to improve device performance if the transistor is operated at a lower temperature.

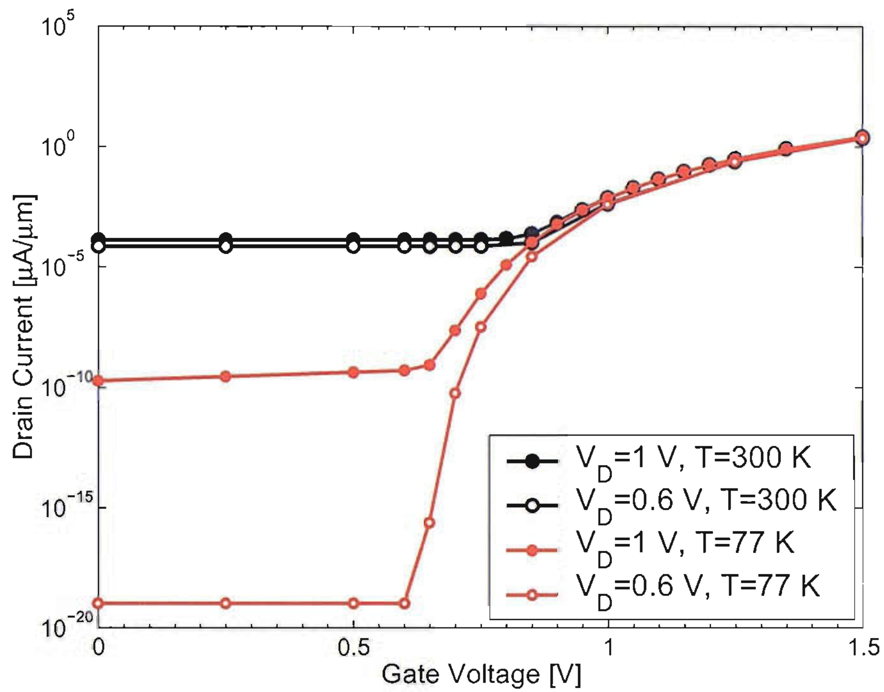

Figure 4.13: Manually calculated I-V characteristics of an n-VMISTT at $V_D = 0.6$ V and 1 V, at different temperatures T. Refer to Table 4.1 for device parameters used in the simulations.

Table 4.5: The effect of drain bias V_D on n-VMISTT at different temperatures.

Temperature [K]	V_D [V]	I_{off} [μA/μm]	I_{on} [μA/μm]	I_{on}/I_{off}	SVT [mV/dec]	V_T [V]
300	0.6	7.27×10^{-5}	2.28×10^{0}	3.14×10^{4}	36.07	0.90
	1	1.33×10^{-4}	2.64×10^{0}	1.99×10^{4}	40.51	0.95
77	0.6	1.06×10^{-19}	2.28×10^{0}	2.15×10^{19}	4.04	0.70
	1	2.00×10^{-10}	2.64×10^{0}	1.32×10^{10}	14.21	0.75

(d) Dielectric Constant

The ratio of the tunnel barrier dielectric constant over the gate oxide dielectric constant R heavily influences the gate modulation as the gate electric field can penetrate further in the channel for a higher gate dielectric constant. Figure 4.14 shows the effect of R on the I-V characteristics of an n-VMISTT. It is noted that I_{on} can be increased by one order of magnitude if R is reduced from unity to 0.1. Therefore, the VMISTT will have a better performance if a small value of R is realised through the choice of tunnel barrier and gate oxide.

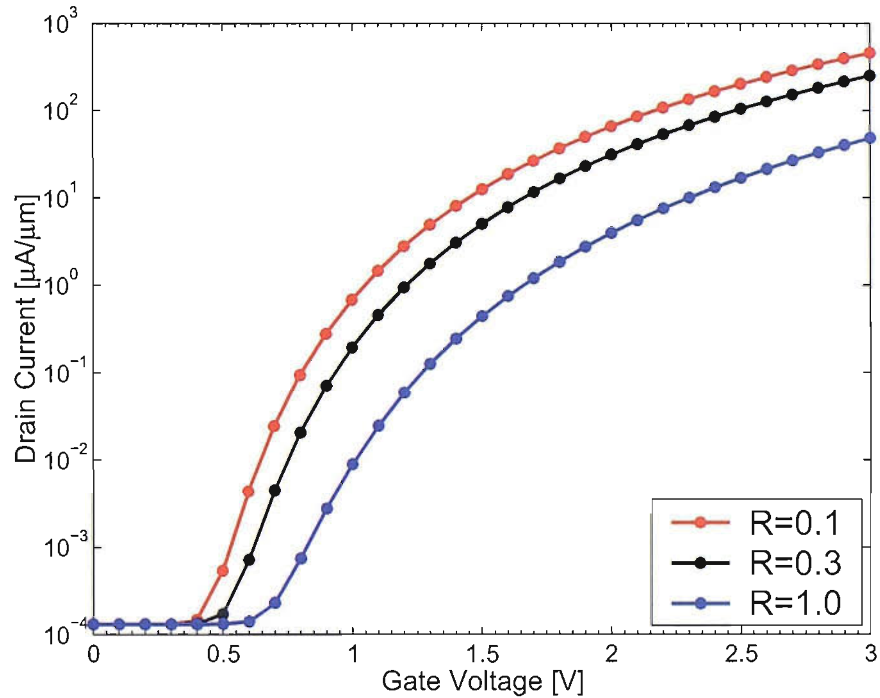

Figure 4.14: ATLAS simulated I-V characteristics of an n-VMISTT at $V_D = 1$ V and 300 K, for different dielectric constant ratio R. Refer to Table 4.1 for device parameters used in the simulations.

(e) Effect of Tunnel Barrier Thickness

Figure 4.15 shows the effect of tunnel barrier thickness d_{ox} on the I-V characteristics of an n-VMISTT at 300 K. At low V_G, d_{ox} has a significant effect on the current density: I_{off} decreases dramatically as d_{ox} increases. As explained before, at low V_G, the current density is due to the non-modulated potential profile. The effective potential thickness is directly related to d_{ox}. Therefore, as d_{ox} increases, the F-N tunneling current, which is exponentially dependent on the oxide thickness, will decrease sharply. On the other hand, at high V_G, there is not much difference in I_{on} for different d_{ox}. This can be explained with the aid of the gate modulated potential profile of different d_{ox} shown in Figure 4.16. It is noted that the effective potential thickness of the gate modulated potential profile are very similar, regardless of the value of d_{ox}. This suggests that at high V_G, the gate electric field has an overwhelming effect in controlling the effective potential thickness, and hence d_{ox} has little effect.

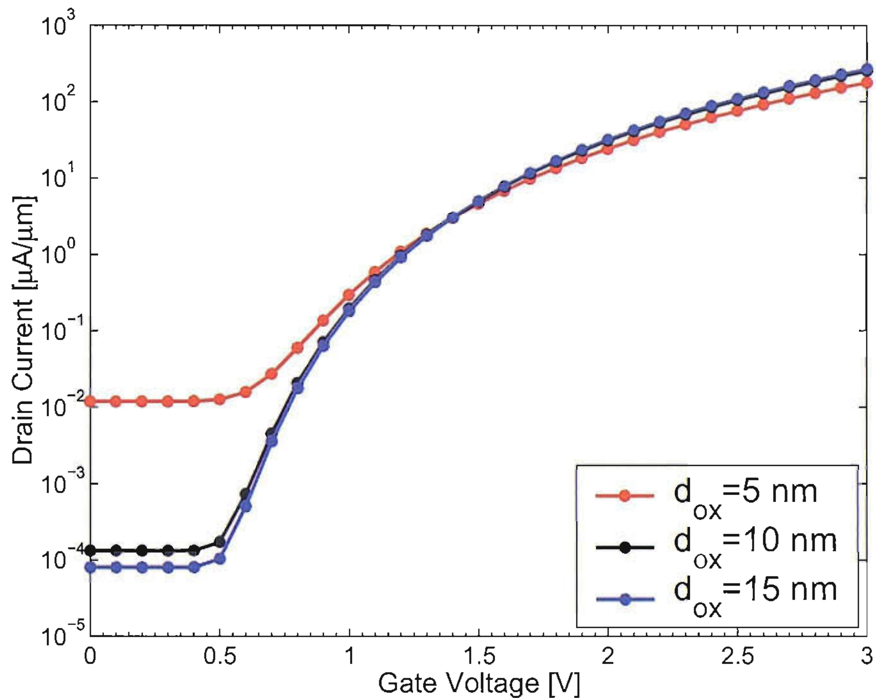

Figure 4.15: ATLAS simulated I-V characteristics of an n-VMISTT at V_D = 1 V and 300 K, for different tunnel barrier thickness d_{ox}. Refer to Table 4.1 for device parameters used in the simulations.

Figure 4.15 suggests that d_{ox} = 10 nm is a suitable value for the VMISTT because of the higher drain current swing than that with d_{ox} = 5 nm. Higher value of d_{ox} also seems suitable for the VMISTT as it will further reduce I_{off}. However, the resistance of tunnel barrier has to be taken into account because it will increase as d_{ox} increases. This will

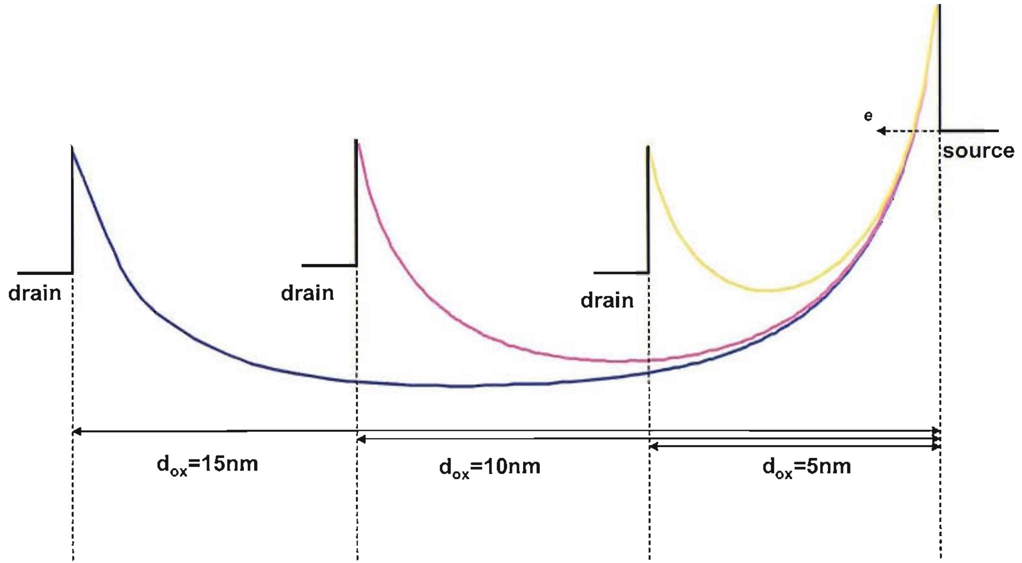

Figure 4.16: ATLAS simulated tunnel barrier potential profile at V_D = 1 V and 300 K, for different tunnel barrier thickness d_{ox}. Refer to Table 4.1 for device parameters used in the simulations.

further reduce I_{on}, which is a significant drawback as the I_{on} of an n-VMISTT is already lower than that of a typical MOSFET. It should also be noted that the resistance of tunnel barrier is not modelled in the simulations due to the difficulties in estimating its value.

(f) Effect of Device Depth

Figure 4.17 shows the effect of device depth D on the I-V characteristics at 300 K. It is observed that I_{off} will decrease as D decreases. This can help to improve I_{on}/I_{off} and V_T. This is because the Schottky current density is proportional to D. Thus, a reduction in D will reduce I_{off}. This has no effect on the gate-modulated F-N tunneling current because the penetration of the gate electric field into the tunnel barrier is about 10 nm (see Figure 4.8). However, it is extremely difficult to have a small value of D due to fabrication related issues. This will be discussed in Section 4.6.

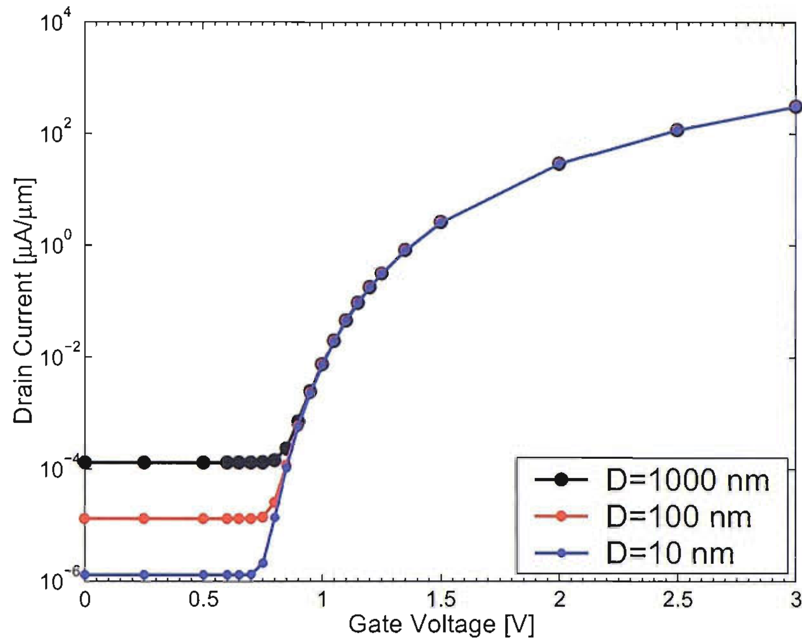

Figure 4.17: Manually calculated I-V characteristics of an n-VMISTT at V_D = 1 V and 300 K, for different depth D. Refer to Table 4.1 for device parameters used in the simulations.

(h) Summary of the Simulation Results

The simulations show the effect of the device parameters on the VMISTT performance. The most critical parameter is the oxide/Si barrier height Φ_B. A too low value of Φ_B will result in a huge off-state current I_{off} and a small subthreshold slope SVT. On the other hand, a too large value of Φ_B will lead to a low on-state current I_{on}. Another important parameter is the tunnel barrier thickness d_{ox}. A low d_{ox} will increase I_{off}, and a high d_{ox} will result in a low I_{on} due to the increase in the tunnel barrier resistance. It has been shown that Φ_B = 0.6 V and d_{ox} = 10 nm are suitable values for an n-VMISTT as this can give reasonably good I-V characteristics. A low value of the dielectric constants ratio R will also improve the gate modulation on the tunnel barrier potential profile. These parameters have to be taken into consideration when choosing the materials for the tunnel barrier and the gate oxide.

Table 4.6 compares the performance parameters of a MOSFET and an n-VMISTT. The n-VMISTT has a lower I_{off} and a steeper subthreshold slope. However, it also has a lower I_{on} and a higher V_T. Nonetheless, the simulation is based on a 2-dimensional n-VMISTT structure. A surround gate structure should result in a higher I_{on} due to the increase of the gate control [27]. A higher gate dielectric constant, which results in a higher dielectric

constant ratio R, and a thinner gate oxide can also enhance the gate modulation on the potential profile, and thus increase I_{on}. Furthermore, due to the metal drain and gate, the interconnect resistance will be lower so that a high value of I_{on} might not be required as in the MOSFET. Besides, I_{off} can be reduced with a smaller device depth, which can improve I_{on}/I_{off} as well. It is shown by the simulations that the performance of the VMISTT can be further improved if operated at a lower temperature and a lower V_D. Therefore, from the simulation results, the VMISTT is a promising candidate for replacing MOSFETs in some CMOS applications.

Table 4.6: Comparison of the performance parameters of a MOSFET [2, 43] and an n-VMISTT. The parameter values of n-VMISTT are obtained from ATLAS simulation based on Table 4.1 at V_D=1 V.

performance parameter	symbol [units]	MOSFET	2-dimensional n-VMISTT
on-state current	I_{on} [μA/μm]	10^3	10^0
off-state current	I_{off} [μA/μm]	10^{-2}	10^{-4}
on-off current ratio	I_{on}/I_{off}	$10^5 \sim 10^6$	10^4
inverse subthreshold slope	SVT [mV/dec]	70~100	40.51
threshold voltage	V_T [V]	0.2	0.95

4.6 Fabrication Challenges of the VMISTT

There are three main challenges for the fabrication of a VMISTT transistor: fabrication and optimisation of the tunnel barrier, fabrication of the vertical pillar, and deposition of the gate oxide over the vertical pillar. The experimental chapters of this thesis will focus on the fabrication and characterisation of the tunnel barrier. However, an overview of each fabrication challenges is briefly discussed.

(a) Fabrication and Optimisation of the Tunnel Barrier

From the simulation results, the oxide/Si barrier height is a critical parameter for the VMISTT. Therefore, it is crucial to identify a suitable material for the tunnel barrier. Besides Schottky current, there are other possible current transport mechanisms such as Poole-Frenkel emission, trap-assisted tunneling, and hopping conduction [4]. These mechanisms are undesirable and are classified as the leakage current in the VMISTT. It is important to suppress these mechanisms to allow F-N tunneling to be the dominant mech-

anism in the tunnel barrier. To achieve that, a suitable material and a suitable process must be chosen to fabricate the tunnel barrier. Further discussion on this will follow in the next chapter.

(b) Fabrication of Vertical Pillar

Fabrication of the vertical pillar is an important process because a vertical pillar with minimum roughness is essential to ensure a good interface between the tunnel barrier and the gate oxide. This will allow better gate modulation on the tunnel barrier potential profile. The diameter of the pillar, which is equivalent to the depth D of the VMISTT in the simulation section, is set to 1000 nm. This will present some process problems as the possible candidates for the metal electrodes are noble metals such as gold, silver, platinum, and copper etc. Reactive ion etching (RIE) on these metals is very difficult due to the hard nature of the materials. In addition, as the tunnel barrier thickness is very thin and about 10 nm, there is a possibility that during the etching process, metal may be deposited on the tunnel barrier surface. This is undesirable because it will create a leakage path in the device structure. The vertical MOSFETs fabrication techniques described in Chapter 2 can be used to fabricate the vertical pillar.

(c) Deposition of Gate oxide over the Vertical Pillar

The deposition technique of gate oxide must be able to provide a good interface between the gate oxide and the metal oxide, so that the gate bias can effectively modulate the tunnel barrier. As shown by the simulation results in previous sections, the gate oxide dielectric constant should be greater than the tunnel barrier dielectric constant to ensure efficient gate control. Also, the gate oxide must be as thin as possible so that most of the gate electric field will appear over the tunnel barrier for modulation. In addition, the barrier height of the gate oxide to the source and drain terminal and to the tunnel barrier must be relatively high to prevent gate leakage current to the source, drain or tunnel barrier. Deposition techniques such as atomic layer chemical vapour deposition (ALCVD) in the application in high-k dielectrics have received a lot of attention recently [66]. This technique can be employed for the gate oxide deposition in the VMISTT.

4.7 Conclusion

The VMISTT has been proposed as a candidate to replace the MOSFET. The VMISTT is a vertical version of the MOTT, with the source metal replaced by doped-Si. The vertical structure can improve the performance by increasing the channel width of the device, and allowing better gate control over the tunnel barrier. Most importantly, the Si source of the VMISTT makes it possible to realise complementary operation as in CMOS. ATLAS device simulations were used to study the effect of the device parameters on the I-V characteristics of the VMISTT. It has been shown that the oxide/Si barrier height and tunnel barrier thickness have significant effect on the VMISTT performance. In addition, the performance can be further improved if the device is operated at lower temperature and with a lower drain bias. The challenges in the design of the VMISTT have been identified. The next few chapters of this thesis will focus on the first stage of this project, which is the fabrication and optimisation of the tunnel barrier.

Chapter 5

Fabrication Methods of TiO_2

5.1 Introduction

The tunnel barrier is the body of the VMISTT and an essential part of the transistor. It is important to choose a suitable material for the tunnel barrier. The main criterion for the tunnel barrier is low barrier height Φ_B relative to the Si conduction band as well as the valence band. This is to ensure low turn-on voltage for the electron F-N tunneling current in the n-VMISTT and the hole F-N tunneling current in the p-VMISTT. However, Φ_B cannot be too low as Schottky emission will be significant and overwhelming the F-N tunneling current. TiO_2 appears to be a promising material for the tunnel barrier because its band off-set is around 1 eV for both electrons in the conduction band and holes in the valence band [5, 67]. As shown in the simulations in Chapter 4, a Φ_B of 1 V is high enough to suppress the Schottky emission current, and allow an on-off current ratio of 10^5 (refer to Section 4.5).

Up to this stage, only Schottky emission and non-modulated F-N tunneling current are identified as the main leakage currents in the VMISTT. Actually, there are other current transport mechanisms that could happen in an insulating thin film, such as Poole-Frenkel (P-F) emission, trap-assisted tunneling and hopping conduction [63, 68, 69]. All these mechanisms are also classified as leakage current in the VMISTT. These mechanisms are trap-related and are due to the defects and interface states in the tunnel barrier. Hence, a suitable thin film fabrication technique should be chosen to grow high quality tunnel barrier with high uniformity, minimum surface roughness and good interface with the substrate. In addition, it should be noted that the TiO_2 in the MOTT were fabri-

cated by non-industrial acceptable method such as anodic oxidation by AFM tips [38, 41]. Therefore, the chosen fabrication technique should also be industrial acceptable.

In this chapter, an overview of the properties of TiO_2 thin film is presented in the next section to provide a better understanding of this material. Several popular thin film fabrication techniques are discussed. Two fabrication methods were studied experimentally in details: thermal oxidation of electron beam (e-beam) evaporated Ti thin films and molecular beam epitaxy (MBE) of Ti in an oxygen atmosphere. It is shown that the thermally grown TiO_2 layers are superior to the MBE grown TiO_2 layers. Hence, further analysis will be presented on thermally grown TiO_2 layers in later chapters.

5.2 The Properties of TiO_2 Thin Film

TiO_2 is a popular material with many applications in electronics due to its high permittivity [5, 70]. It has been investigated for static random access memory (SRAM) applications [71, 72]. It is physically and chemically stable and titanium metal is generally accepted in most of the CMOS fabrication process [67]. Understanding the structural and electrical properties of the TiO_2 layers is critical for the successful implementation of this material as the tunnel barrier in the VMISTT.

TiO_2 has three different crystalline polymorphic forms: rutile, anatase, and brookite [67, 70]. However, only the rutile and anatase have major roles in the TiO_2 applications [70] and hence the discussion is focused on this two structures. Figures 5.1 and 5.2 shows the unit cells of rutile and anatase TiO_2, respectively. The lattice constants (a, b, and c) of the unit cell of the rutile and anatase are listed in Table 5.1. The bandgap E_g of TiO_2 is reported to be between 3 and 3.7 eV depending on the crystalline phase [67, 73]. Both the conduction band difference ΔE_C and the valence band difference ΔE_V of TiO_2 to Si are about 1 eV [5, 67], as illustrated in Figure 5.3. This makes TiO_2 a suitable material for the tunnel barrier in n-VMISTT as well as in p-VMISTT. Owing to different crystalline phases, TiO_2 has a range of dielectric constants [70, 74, 75]. The dielectric constant can be as low as 20 for an anatase phase TiO_2, and as high as 170 for a rutile phase TiO_2.

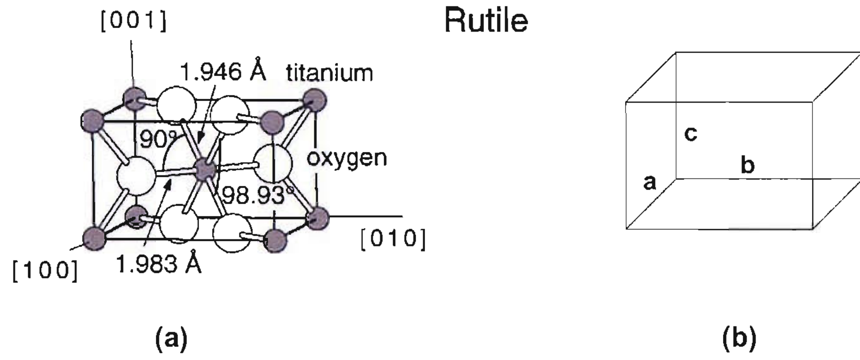

Figure 5.1: (a) Unit cell of the rutile phase TiO_2, (b) structure depicting the lattice constant of the unit cell a, b, and c. The values of the lattice constant are listed in Table 5.1. Figure based after [70].

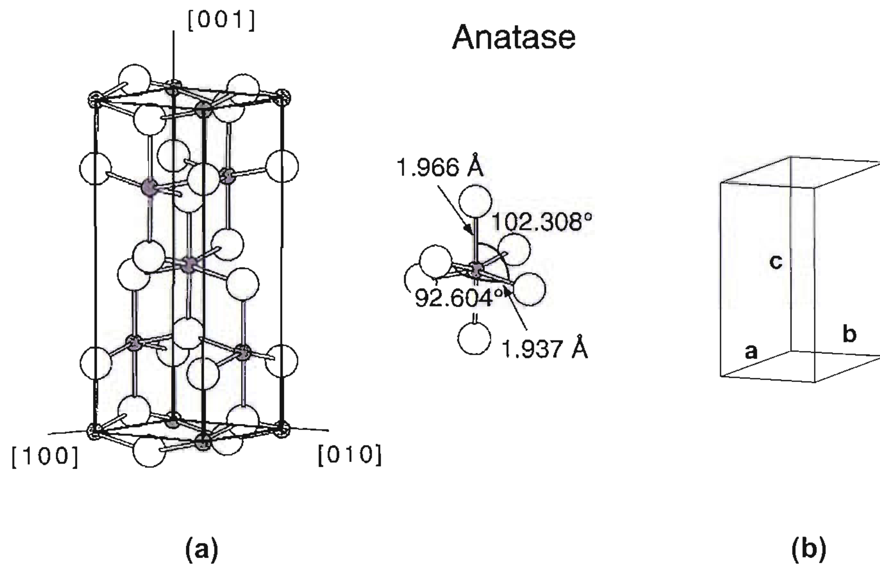

Figure 5.2: (a) Unit cell of the anatase phase TiO_2, (b) structure depicting the lattice constant of the unit cell a, b, and c. The values of the lattice constant are listed in Table 5.1. Figure based after [70].

Table 5.1: The crystal systems and lattice constants (a, b, c) of TiO_2 [70].

	Crystal system	a [$\AA$]	b [$\AA$]	c [$\AA$]
rutile	tetragonal	4.58	4.58	2.95
anatase	tetragonal	3.73	3.73	9.37

Temperature has a significant effect on the atomic structure of TiO_2. It has been shown that the anatase phase will be transformed to rutile phase for annealing temperature greater than 600°C [67, 74], this will increase the dielectric constant of TiO_2 but decrease the bandgap [67]. Therefore, the barrier height Φ_B between TiO_2 and Si substrate at the

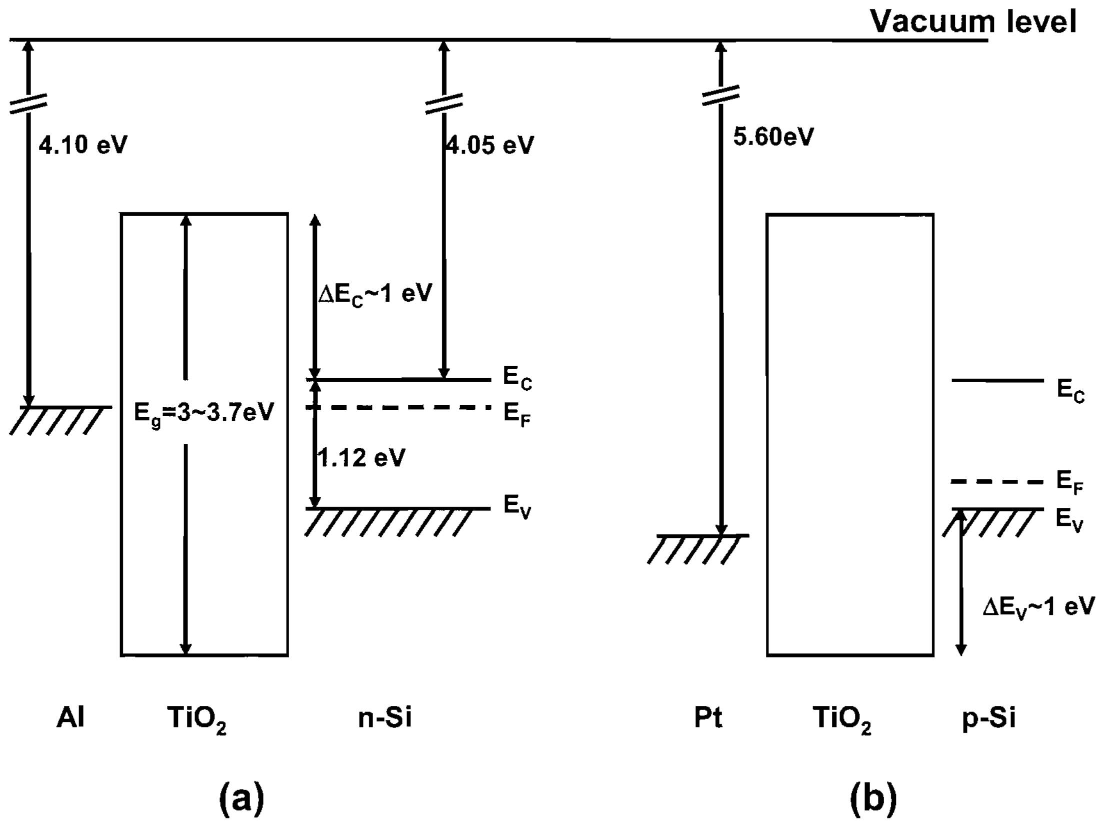

Figure 5.3: Energy band diagrams of (a) Al/TiO_2/n-Si (b) Pt/TiO_2/p-Si MOS capacitor.

conduction band as well as the valence band will decrease. As mentioned in Chapter 4, a high tunnel barrier dielectric constant will be a detriment to the maximization of the gate control over the drain current in the VMISTT. Therefore, a compromise between the dielectric constant and the barrier height is required to optimise the efficiency of the tunnel barrier for the VMISTT. However, as Φ_B has a more significant impact on the VMISTT performance than the tunnel barrier dielectric constant, the emphasis will be placed on Φ_B.

Oxygen deficiencies are expected in TiO_2 [76]. It is reported that the defect states of TiO_2 are 0.7 to 1 eV below the conduction band [77–80]. These defect states could enhance the trap-related mechanisms like P-F emission, trap-assisted tunneling and hopping conduction. A suitable fabrication technique could help to reduce the density of the defect states and furthermore ensure thin film uniformity and minimum surface roughness.

A metal oxide semiconductor (MOS) capacitor structure is generally used for the electrical characterisation of the oxide layers. However, the electrical properties of TiO_2 layer can be affected by the growth technique and the interfacial layer due to reactions at the TiO_2/Si interface [5, 70]. In addition, depending on the choice of the top metal electrode of the MOS capacitor, the interfacial layer at the metal/TiO_2 interface can also affect the electrical properties of TiO_2 [70]. Therefore, fabrication technique and top metal electrode are important to minimize the effect of interfacial layers.

5.3 Fabrication Techniques of TiO_2 Thin Film

The quality of the tunnel barrier depends largely on the fabrication process. There are various type of growth techniques for TiO_2, e.g. thermal oxidation [81–86], plasma oxidation [87], radio frequency (RF) sputtering [72, 74, 88, 89], plasma-enhanced chemical vapor deposition (PECVD) [90, 91], metal organic chemical vapor deposition (MOCVD) [67, 92–94] and reactive evaporation [95–97]. It is necessary to understand the principle of these growing techniques and be aware of the advantages and disadvantages of each technique so that a suitable deposition process can be chosen to fabricate TiO_2 layers.

(a) Thermal Oxidation of Ti Thin Film

Thermal oxidation is a simple process to fabricate TiO_2 thin films. Before thermal oxidation, a thin layer of Ti is deposited on the substrate. This can be done by RF sputtering [84, 85] or electron-beam (e-beam) evaporation [83, 86] of the Ti thin film. E-beam evaporation of Ti thin film is favoured to RF sputtering because the underlying substrate surface smoothness is preserved [98]. Also the e-beam evaporated Ti thin film is flat on a nano-scale level. Thus, a high quality tunnel barrier can be grown without making pinholes [35]. During the process, an electron beam is directed at a pure Ti source. This will produce a large flux of Ti vapour and deposit a thin layer of Ti film on the substrate. The substrate can be rotated during the process to ensure film uniformity. After that, the Ti thin film is oxidized at a specific temperature and pressure. Besides the simplicity of this process, it will also give a uniform metal layer with minimum roughness [99]. In addition, the chances of impurity incorporation is minimum and the oxide growth rate is low, which is suitable for thin layers. The drawback of this method is the uncertainty in the film thickness and the stoichiometry of the oxide formed during the oxidation process, which depend on the oxidation conditions and the Ti thin film thickness [83]. Besides TiO_2, there

are several oxide phases for titanium such as TiO, Ti_2O_3 and Ti_3O_5 [83, 100, 101]. These oxide phases could be formed during the oxidation process. In addition, inter-diffusion between Ti and Si atoms during the high temperature oxidation process can occur, and can even lead to the formation of silicide. Titanium silicide has been reported to be formed at temperatures above 400° C [102–106]. Also, titanium silicates could be formed due to the reaction among Ti, Si and O atoms.

(b) Plasma Oxidation of Ti Thin Film

Plasma oxidation is similar to thermal oxidation. The Ti thin film can be deposited by e-beam evaporation or RF-sputtering before being oxidized in oxygen plasma. Since the electron temperature of the ionized oxygen is about 10000 K, the oxidation process can be carried out at low temperature [107]. This can reduce the chance of inter-diffusion between the metal and the Si substrate and the formation of silicide. However, as there are high electric field present during the process, the as-deposited oxide layer may contain high interface traps density and have low electric field strength [107].

(c) RF Sputtering of TiO_2 Thin Film

In RF sputtering, the TiO_2 thin film is deposited on a substrate by bombardment of argon Ar ions on the target in an oxygen ambient or inert ambient. The main advantage of this technique is the replication of target composition in the deposited film [107]. It is suitable for low vapour pressure, high melting point material (e.g. tungsten, platinum), because high temperatures are not required for the source heater [108]. However, interface roughness and uniformity of the film will be a problem in the fabrication of the tunnel barrier since the substrate surface could be damaged by the active ions, which will result in poor interface quality [107]. In addition, the sputter gas must be very pure to ensure good adhesion of the oxide layer on the substrate [108].

(d) Chemical Vapour Deposition of TiO_2 Thin Film

In a chemical vapour deposition (CVD) process, the reactant species will be transported into the reactor. The reactions will take place at the substrate and an oxide layer will be deposited. The unwanted reaction products will be removed [107, 108]. The advantages of CVD includes high throughput and uniformity. However, contamination in the oxide layer is a main problem because most of the reactions are of the pyrolytic nature, which involves decomposition or transformation of a chemical compound as a result of heating [81, 107].

Plasma enhanced CVD (PECVD) is one type of CVD process that has the advantages offered by plasma oxidation. The high electron temperature in PECVD allows the oxide layer to be deposited at much lower temperature and the impact of energetic species can improve the adhesion of oxide layer to the substrate [107]. Nonetheless, the underlying substrate could be damaged and result in poor interface between the oxide and substrate. For metal organic CVD (MOCVD), a metal organic compound precursor is used in the reactor. MOCVD can provide a uniform layer [93] and be suitable for stoichiometric and micro-structural thin film deposition [92]. However, the carbon in the precursor may contaminate the thin film during the deposition process, and increase the leakage current [81].

(e) Reactive Evaporation of TiO_2 Thin Film

The TiO_2 thin film can be formed in-situ by a reaction between an oxygen containing reactive gas and a thermally evaporated Ti vapour [95–97]. The Ti vapour can be produced by molecular beam epitaxy (MBE) technique, which is a refined form of e-beam evaporation [107]. An MBE system requires ultra high vacuum to ensure no gas phase collisions occur before the beam atoms arrive at the substrate [109]. The main advantages offered by the MBE is the precise control of the film thickness and the excellent uniformity of the layer [109].

Summary

Each fabrication technique has its own advantages and disadvantages. It is believed that thermal oxidation of e-beam evaporated Ti thin film is a suitable technique due to the advantages that it can offer: minimum roughness at the TiO_2/Si interface and uniformity of the grown oxide layer. In addition, the as-grown layer will have minimum contamination. These will result in an improved and more consistent electrical properties of the tunnel barrier. The leakage current due to the surface roughness could also be suppressed. Also, this method is industrial acceptable. Reactive evaporation of the TiO_2 layer by the MBE technique will also be studied. The capability of precise control of the oxide thickness can allow better electrical characterisation of the oxide.

5.4 Thermal Oxidation of Electron-beam Evaporated Ti Thin Film

The oxidation temperature is the prime parameter for thermal oxidation. If the temperature is too low, the Ti thin film will not be fully oxidized, which will result in a huge leakage current due to the non-oxidized Ti atoms in the layer. Oxidation of Ti is generally performed at temperatures above 300° C [83, 86, 110]. On the other hand, if the temperature is too high, it is possible that a substantial interfacial SiO_2 layer will be grown at the TiO_2/Si interface. This is undesirable as it will reduce the F-N tunneling current due to the high barrier of SiO_2. Although the growth of an interfacial layer SiO_2 layer is inevitable, even at room temperature, a thin SiO_2 interfacial layer may be tolerated as the carriers can pass through the SiO_2 layer by direct tunneling.

Oxidation of Ti thin film can lead to the formation of different types of titanium oxide, depending on the experimental conditions [83, 100]. The expansion factor of different titanium oxides are listed in Table 5.2. These expansion factors are calculated by using the atomic mass and density of the oxides and Ti [70, 101]. It is shown that the thickness of titanium oxide increases with increased oxidation. According to the simulation results in Chapter 4, the tunnel barrier should have a thickness of about 10 to 15 nm to give a good device performance. Therefore, the thickness of the e-beam evaporated Ti thin film should be around 7 to 10 nm.

Table 5.2: The expansion factor for different titanium oxide phases.

Oxide Phase	Expansion Factor
TiO	1.21
Ti_2O_3	1.51
Ti_3O_5	1.66
TiO_2 (rutile)	1.78
TiO_2 (anatase)	1.96

TiO_2 MOS capacitors were fabricated to optimise the fabrication process and to characterise the oxide layer. Generally, to reduce leakage current in the as-deposited oxide, post oxidation annealing is used to repair the damage or defects in the oxide layer [67, 111]. Therefore, the effect of post oxidation annealing on the as-grown oxide layers in inert

atmosphere and at temperatures higher than the oxidation temperature were studied.

The back contact of the MOS capacitors is an Al layer on Si. Normally, an alloying process is performed at the final stage of the fabrication process to ensure the back contact is ohmic. However, as the alloying is performed at 450 °C, this can lead to the diffusion of Al top electrode into the TiO_2 layer and the formation of an Al_2O_3 interfacial layer at the Al/TiO_2 interface [70, 112]. In fact, if the substrate is highly doped ($> 10^{19}cm^{-3}$), the depletion region in the Si will be extremely narrow. Hence, alloying may not be necessary because the carriers will tunnel through the metal semiconductor barrier and the resulting I-V characteristics will be ohmic as well [107]. Therefore, it is necessary to investigate the effect of alloying of the Al back contact in the TiO_2 MOS capacitor.

5.4.1 Experimental Details & Instruments

(a) Experimental Details

Two batches of TiO_2 MOS capacitors were fabricated to optimise the oxidation conditions for TiO_2 layer. Figure 5.4 shows the process flow of the first batch. *p*-Si wafers with resistivity of 0.02 Ωcm were used. First, the wafers were cleaned in two solutions in sequence to remove contaminants on the wafer surface. This cleaning process was developed by Radio Corporation of America (RCA). The first solution consists of ammonia (NH_4OH), hydrogen peroxide (H_2O_2) and water (H_2O). It consists of a volume ratio of 1 : 1 : 5 of NH_4OH : H_2O_2 : H_2O. The NH_4OH is used to remove heavy metals by forming amino complexes with them, and the H_2O_2 is used to oxidize the organic contaminants on the wafer surface. The constituents of the second solution are hydrochloric acid (HCl), hydrogen peroxide and water. It consists of a volume ratio of 1 : 1 : 6 of HCl : H_2O_2 : H_2O. This solution is used to remove aluminum, magnesium and light alkali ions. During each cleaning step, the wafers were dipped in the solutions for 10 min at 73 °C. After the RCA cleaning, the wafers were cleaned with hydrofluoric acid (HF) solution. This will remove the native oxide formed on the wafer surface. The wafers were then sent for evaporation of Ti thin films immediately after the HF cleaning process. 10 nm Ti thin films were deposited by vacuum e-beam evaporation on the wafers without any substrate heating. The evaporation pressure was 2.25×10^{-6} torr, and the evaporation rate of Ti was 0.3 nm/s.

The samples were oxidized at three different temperatures: 300, 400 and 500 °C for 30 minutes. After the oxidation, the batch was split into half. One half was annealed at 700 °C in nitrogen ambient for 30 minutes. The other half was metallized without post oxidation annealing. In the metallization stage, a 1 μm thick Al top electrode was vacuum evaporated using a shadow mask to make various contact pad sizes and a 1 μm Al layer was evaporated on the back surface. Finally, all samples were alloyed in hydrogen and nitrogen ambient at 450 °C for 30 minutes to make the ohmic back contacts. The ratio of the gases in alloying is 60% hydrogen and 40% nitrogen. The process listing is shown in Appendix B.2. The results of this batch are discussed in Section 5.4.2 and 5.4.3.

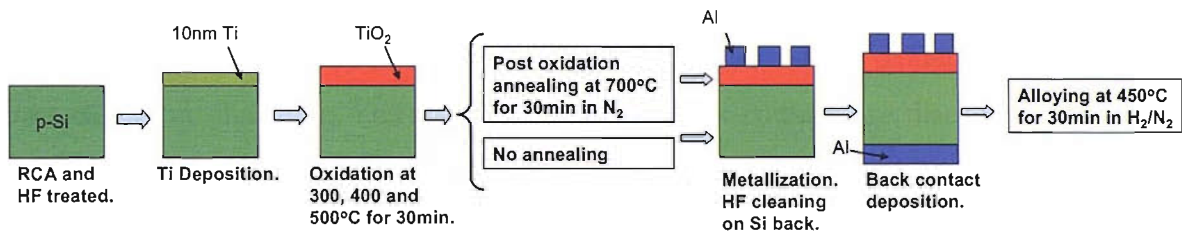

Figure 5.4: Process flow of the TiO_2 MOS capacitors fabricated by thermal oxidation of e-beam evaporated Ti thin films in the first batch.

The process flow of the second batch is shown in Figure 5.5. *p*-Si wafers with resistivity of 0.02 Ωcm were used. The wafers were RCA cleaned and HF treated before evaporation of the Ti thin films. The conditions of the evaporation were the same as the first experiment. After the evaporation of the Ti thin films, the samples were oxidized at 450, 500 and 550 °C for 30 minutes. Subsequently, the samples were metallized without post oxidation annealing. The metallization process was the same as the first experiment. Finally, each group was split into two parts, and one part was alloyed in hydrogen and nitrogen ambient at 450 °C for 30 minutes to make the ohmic back contacts. The process listing is shown in Appendix B.3. The structural characterisation presented in the next chapter will show that the films grown are indeed TiO_2. In order to study the effect of alloying of the Al back contacts, samples with different substrate resistivity (0.5 Ωcm and 17 Ωcm) were also fabricated.

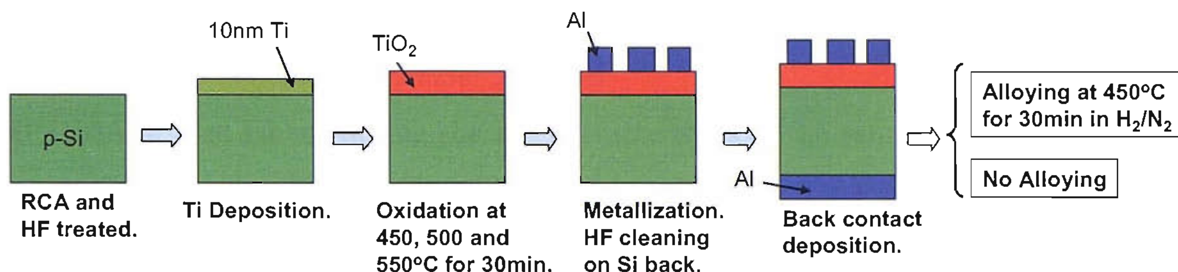

Figure 5.5: Process flow of the TiO_2 MOS capacitors fabricated by thermal oxidation of e-beam evaporated Ti thin films in the second experiment.

The conditions of thermal oxidation is optimised by studying the I-V and the C-V characteristics of the thermally grown TiO_2 layers. The effect of the oxidation temperatures, post oxidation annealing, and alloying of the Al back contact are discussed in the next few sections. The I-V characteristics of the samples were measured by a HP4155A parametric analyser at room temperature. The C-V measurements were done by a HP4280A capacitance-meter and a HP4192A impedance analyser. In all the measurements, the bias was applied to the substrate of the samples and the Al top electrode was kept at ground potential.

For the I-V measurements, the positive and negative bias sweeps were started from zero and for every bias sweep, the sample was kept at zero bias for 10 s to remove any possible charge storage effect. The voltage step was 20 mV, with a step delay time of 10 ms. For the C-V measurements, the voltage sweep was set such that the MOS capacitors were driven from inversion mode to accumulation mode. The voltage step was 50 mV, with a step delay of 10 ms. Measurements were done on pads at different locations on each of the wafers to ensure that the results obtained were typical for the particular sample. Nominal values of the top electrode area were used in the analysis. However, it is observed that for some wafers there is variation in the top electrode area due to the shifting of the shadow mask during the metal evaporation stage. This variation may affect the result of the electrical analysis.

(b) Experimental Instruments

HP4155A Semiconductor Parameter Analyzer

HP4155A is used for measuring the I-V characteristics of the samples [113]. It has four source monitor units (SMUs). Each SMU unit has three different modes: (1) voltage source and current monitor mode, (2) current source and voltage monitor mode, and (3) source common mode. Each SMU can force and measure up to ±100 V or ±100 mA. It can perform two types of measurements: sweep and sampling. In the experiment, the sweep measurement is used: one SMU (say SMU1) is set to voltage source and current monitor mode, and another SMU is set to source common mode. The device under test (DUT) is connected between these two SMUs. During each sweep measurement, SMU1 forces voltage and measures the current flowing across the DUT.

HP4280A 1MHz Capacitance Meter

HP4280A can measure capacitance up to 2 nF at a fixed 1 MHz frequency [114]. A parallel circuit model is used when measuring the capacitance and the conductance. To measure the capacitance, a constant amplitude sine wave is applied to the DUT. The resulting current is detected by an I-V converter, which then determines the admittance of the DUT. A vector voltage ratio detector can separate the real and imaginary components of the admittance, which are the conductance (real component) and the capacitance (imaginary component) of the DUT.

HP4192A LF Impedance Analyzer

HP4192A can measure the capacitance of the DUT for a range of frequencies from 5 Hz up to 13 MHz [115]. The maximum value of the measured capacitance could be up to 100 mF depending on the impedance or admittance range and the measuring frequency. The theory of operation is similar to HP4280A, and it can measure the capacitance in parallel or series mode.

5.4.2 Oxidation Temperature: 300, 400 and 500 °C

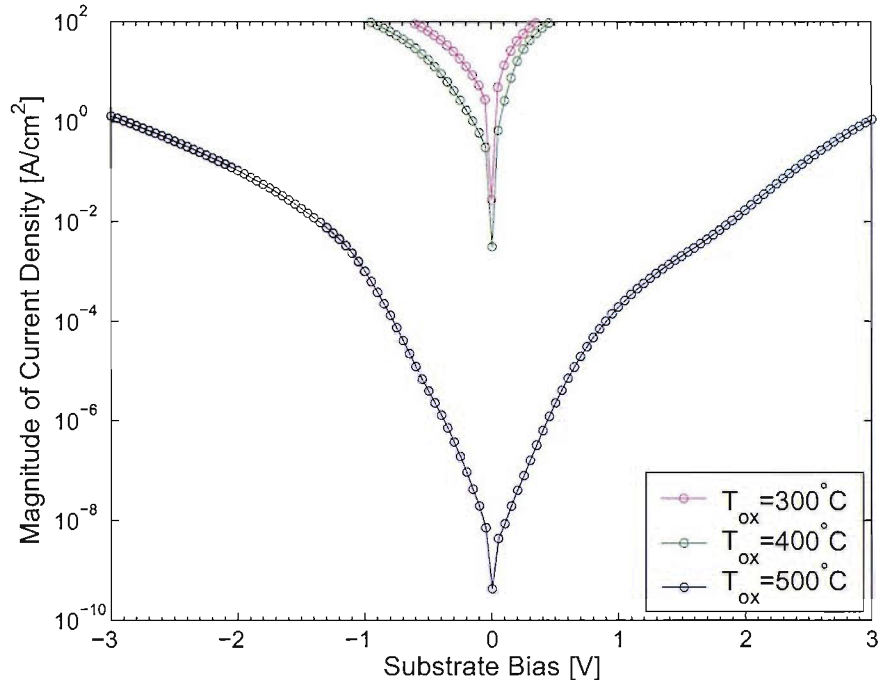

Figure 5.6: I-V characteristics of the TiO_2 layers grown at different oxidation temperatures T_{ox}. The oxide layers are not annealed, and the back contact of the samples are alloyed.

It is essential to optimise the oxidation temperature to grow TiO_2 layer from Ti thin film. The I-V characteristics of the TiO_2 layers grown at 300, 400 and 500 °C are shown in Figure 5.6. It can be observed that the leakage current decreases with increases in T_{ox}. This implies that the oxide quality improves as T_{ox} increases. For samples oxidized at 300 and 400 °C, the leakage current is so high that the I-V characteristics at high applied biases cannot be measured by the measurement instrument. For samples oxidized at 500 °C, the leakage current decreases sharply, which implies that an effective oxide layer is formed. The kinetics of titanium oxidation begins with a fast oxidation stage and followed by a slowing down stage due to the formation of a passivating film [83]. In addition, the diffusivity of oxygen in titanium layer and the titanium chemical reactivity will increase with temperature [83]. Thus, it is believed that at 300 and 400 °C, a thin passivating film is formed at the beginning of the oxidation phase. However, the temperatures were not high enough to lead to a complete oxidation of the Ti thin films. Hence, a very leaky oxide layer was formed. At 500 °C, the diffusivity of oxygen and titanium chemical reactivity has increased, and a better oxidation was achieved. Hence, it is suggested that TiO_2 layer can be grown from Ti thin film at 500 °C. The oxidation temperature will be optimised by

investigating the I-V and C-V characteristics of TiO_2 layers grown at 450, 500 and 550 °C, which will be discussed in Section 5.4.5.

5.4.3 Post Oxidation Annealing at 700 °C in N_2 Ambient

Annealing at high temperature is generally employed to repair the defects in the as-deposited and as-grown oxide layer [67, 74]. Figure 5.7 shows the effect of post oxidation annealing on the I-V characteristics of the TiO_2 layers. The samples were annealed at 700 °C in N_2 ambient for 30 mins. It is observed that the post oxidation annealing has reduced the leakage current of the samples by about four orders of magnitude when compared to the sample that was oxidized at 500 °C without annealing. As shown in Figure 5.7, the annealed samples show similar leakage current density regardless of the oxidation temperatures. This indicates that the annealing has significantly altered the characteristics of the as-grown TiO_2 layers.

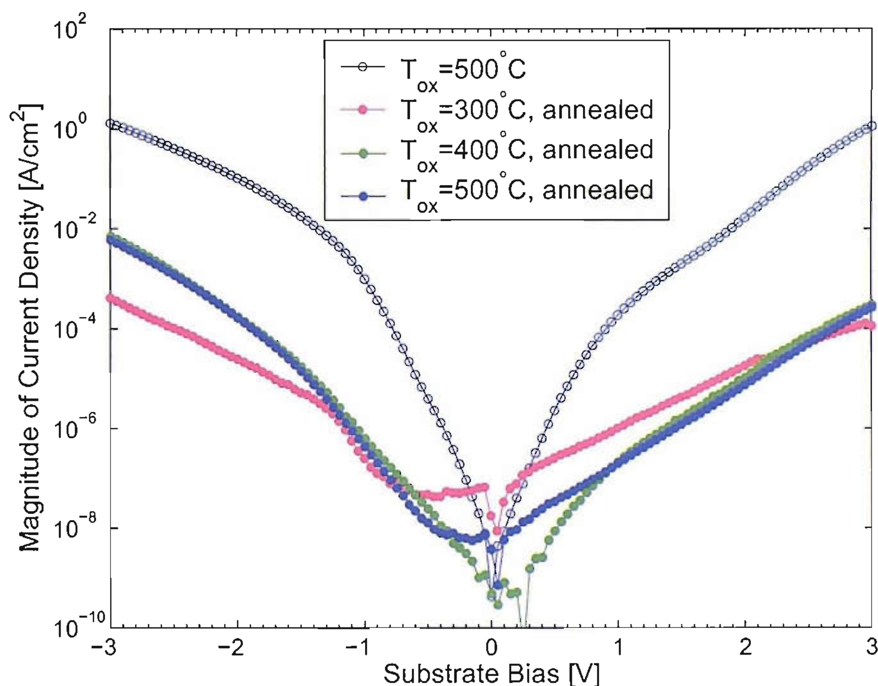

Figure 5.7: Comparison of the I-V characteristics of the non-annealed and annealed samples. The annealed samples were annealed at 700° C in N_2 ambient for 30 mins. The back contact of the samples were alloyed.

Figure 5.8 compares the C-V characteristics of the as-grown TiO_2 layer with those of the annealed TiO_2 layers. The maximum capacitance C_{ox} and the minimum capacitance C_{min} of the samples are summarized in Table 5.3. C_{ox} of the annealed samples are quite

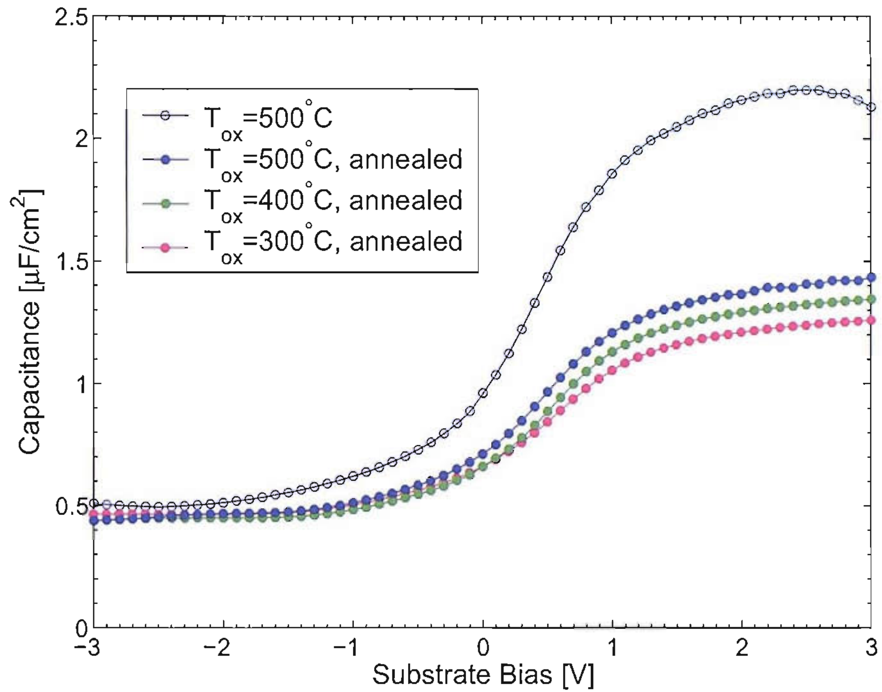

Figure 5.8: Comparison of the C-V characteristics of the non-annealed and annealed samples. The annealed samples were annealed at 700° C in N_2 ambient for 30 mins. The back contact of the samples were alloyed.

Table 5.3: The maximum capacitance C_{ox} and minimum capacitance C_{min} of the annealed and non-annealed samples grown under different oxidation temperatures, T_{ox}.

Sample	C_{ox} [$\times$**10**$^{-6}$ **F/cm**^{2}]	C_{min} [$\times$**10**$^{-7}$ **F/cm**^{2}]
T_{ox} = 500 °C, non-annealed	2.20	5.11
T_{ox} = 500 °C, annealed	1.44	4.40
T_{ox} = 400 °C, annealed	1.35	4.40
T_{ox} = 300 °C, annealed	1.26	4.66

similar and are lower than that of the non-annealed sample. The difference can be due to the interfacial layer grown in the annealed samples, which reduces the total effective C_{ox}. Although the annealing process was performed in N_2 ambient, at 700 °C, oxygen atoms in the oxide layer can become active and diffuse to the interface to form an interfacial SiO_2 layer [67, 74]. In addition, it is observed that C_{ox} of the annealed samples increases as T_{ox} increases. This could be due to the level of oxygen content in the TiO_2 layer. As mentioned before, the diffusivity of the oxygen atoms in the Ti thin films and the reactivity of the oxygen atoms with the Ti atoms increase with increasing T_{ox}. Hence, the oxygen content

in the as-grown oxide layers increases as T_{ox} increases. During the annealing process, the diffusivity and reactivity of the oxygen atoms increase. Some oxygen atoms will react with the Ti atoms and some will reach the substrate and react with the Si atoms to form silicon oxide. The formation of titanium silicates is also possible. Due to the diffusion of oxygen atoms towards the Si substrate, more oxygen vacancies will be created in the oxide layers. The stoichiometry of the TiO_2 layer will decrease, and the dielectric constant of the TiO_2 layer will decrease [116, 117]. Hence, C_{ox} of the annealed samples increases as T_{ox} increases.

It is believed that the significant reduction in the leakage current could be due to the growth of an interfacial SiO_2 layer between the TiO_2 layers and the Si substrate during the annealing process. This could reduce the F-N tunneling current due to the high barrier in the interfacial SiO_2 layer. Therefore, it is suggested that post oxidation annealing at high temperature is not beneficial for thermally grown TiO_2 layer.

5.4.4 Alloying of the Al Back Contact

As mentioned before, alloying is used to create an ohmic contact between the Al back contact and the Si substrate. However, this process is performed at 450 °C, and this may cause the diffusion of Al top electrode into the TiO_2 layer and the formation of an Al_2O_3 interfacial layer at Al/TiO_2 [70, 112]. As the Si substrates used in the experiment have a doping concentration of 10^{19} cm^{-3}, alloying may not be necessary.

I-V measurements were performed to investigate the effect of alloying of the Al back contact. The samples were cut and the Al back contacts scratched to form two isolated Al pads. Then, the I-V characteristics between the two Al pads were measured. Figure 5.9 shows the I-V characteristics of the Al back contacts. Some of the samples have TiO_2 deposited on the front surface, and others are just unprocessed samples with the Al back contact only. The lead resistance was measured to be 2.8 Ω. The I-V characteristics of all the measured samples are linear. The experimental resistances R_e and the calculated resistances R_c from the I-V plots are listed in Table 5.4. It is noted that the experimental resistances for 0.02 Ωcm and 0.5 Ωcm substrate are about 0.2 Ω and 2.5 Ω, respectively. This is either smaller than (for 0.02 Ωcm substrate) or similar to (for 0.5 Ωcm substrate) the lead resistance, which is about 2.8 Ω.

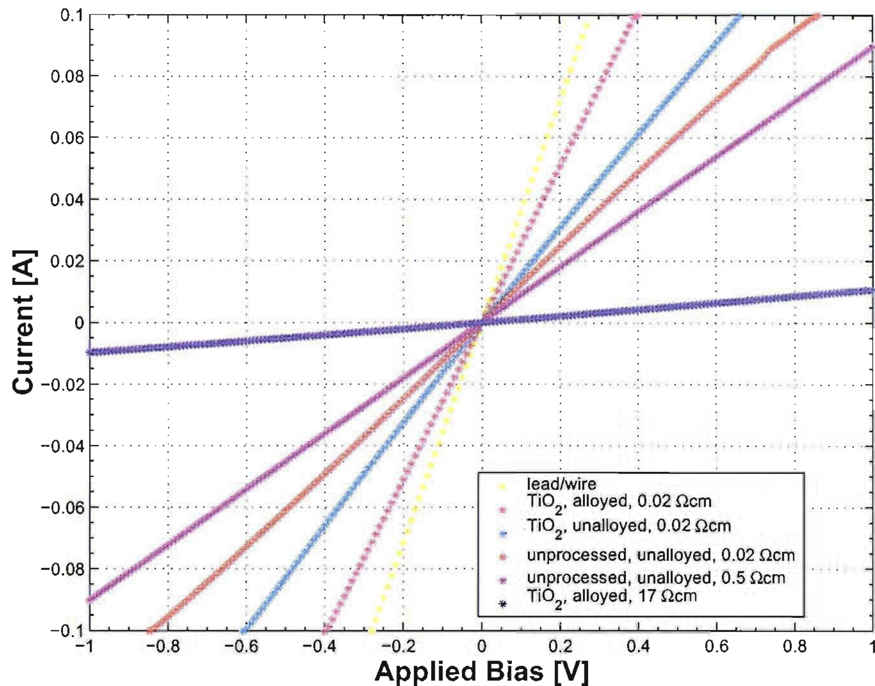

Figure 5.9: The I-V characteristics of the back contact of various samples. The current flow in the lead is also shown for comparison.

Table 5.4: The comparison between the experimental derived resistance R_e and the calculated resistance R_c of the samples. The area A is the estimated cross sectional area for current flow, and the length x is the estimated distance between two Al pads. The 'unprocessed' samples refer to the samples with Al back contacts but no TiO_2 layer.

Sample	**Resistivity** ρ [Ωcm]	**Area** A [$\times 10^{-6}$ m^2]	**length** x [mm]	R_e [Ω] (=$\rho x/A$)	R_c [Ω] **(Figure 5.9)**
TiO_2, alloyed	0.02	1.5	2.0	0.27	4.0
TiO_2, non-alloyed	0.02	2.5	2.0	0.16	6.6
unprocessed, non-alloyed	0.02	1.5	2.0	0.27	8.7
unprocessed, non-alloyed	0.5	2	1.0	2.5	11.2
TiO_2, alloyed	17	2.5	2.0	136	91.0

To ascertain that the measurement method is a correct indication for the ohmic behaviour of the back contact, the same measurement is performed on a 17 Ωcm alloyed substrate. The calculated resistance R_c from the I-V plot is about 91 Ω. This matches well to the resistance of 136 Ω calculated from the roughly estimated A (cross sectional area for current flow) and x (distance between two Al pads), assuming uniform current flow through the thickness of the wafer. Therefore, this measurement method can be used to check the

ohmic behavior of the back contact. From the above analysis, it can be concluded that alloying has no significant effect on the ohmic behaviour of the Al back contact on the 0.02 Ωcm and 0.5 Ωcm substrates. The I-V characteristics of the Al back contact on these two substrates are linear and the contact can be regarded as an ohmic contact.

Figures 5.10 and 5.11 show the I-V and C-V characteristics of both the alloyed and non-alloyed MOS capacitors, respectively. The C_{ox} and C_{min} of the alloyed and non-alloyed samples grown at 500 °C are summarized in Table 5.5. It is noted that the leakage current and the capacitance of the alloyed sample is higher than that of the non-alloyed sample. This observation can be explained if the alloyed sample has a thinner effective oxide thickness. As mentioned before, alloying at 450 °C can cause the diffusion of Al atoms from the top electrode into the TiO_2 layer. If the interfacial layer is very leaky, the total effective oxide thickness is reduced. The 'bump' feature in the non-alloyed sample will be discussed in Section 5.4.5.

In summary, alloying of the Al back contact is not required for the TiO_2 MOS capacitors fabricated on a highly doped Si substrate. In fact, the diffusion of Al atoms into the TiO_2 layer during the alloying process will deteriorate the electrical characteristics of the device. Therefore, the analysis presented later will be based on the TiO_2 MOS capacitors with non-alloyed back contact.

Table 5.5: The maximum capacitance C_{ox} and the minimum capacitance C_{min} of the alloyed and non-alloyed samples grown at 500 °C.

Sample	C_{ox} [$\times 10^{-6}$ F/cm^2]	C_{min} [$\times 10^{-7}$ F/cm^2]
T_{ox} = 500°C, non-alloyed	1.39	5.52
T_{ox} = 500°C, alloyed	2.20	5.11

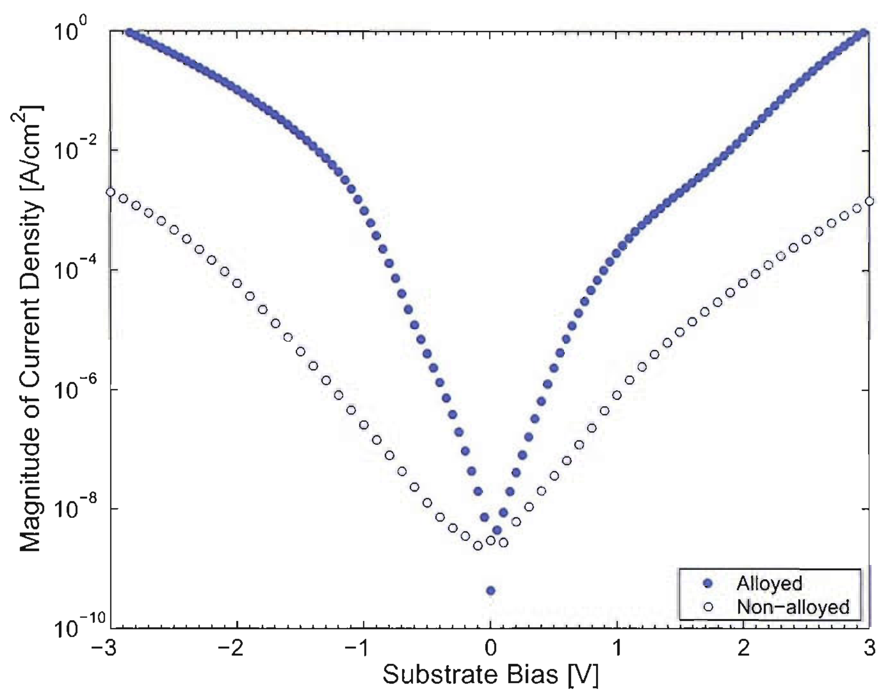

Figure 5.10: Comparison of the I-V characteristics of the alloyed and non-alloyed samples, with the TiO_2 layers grown at 500 °C.

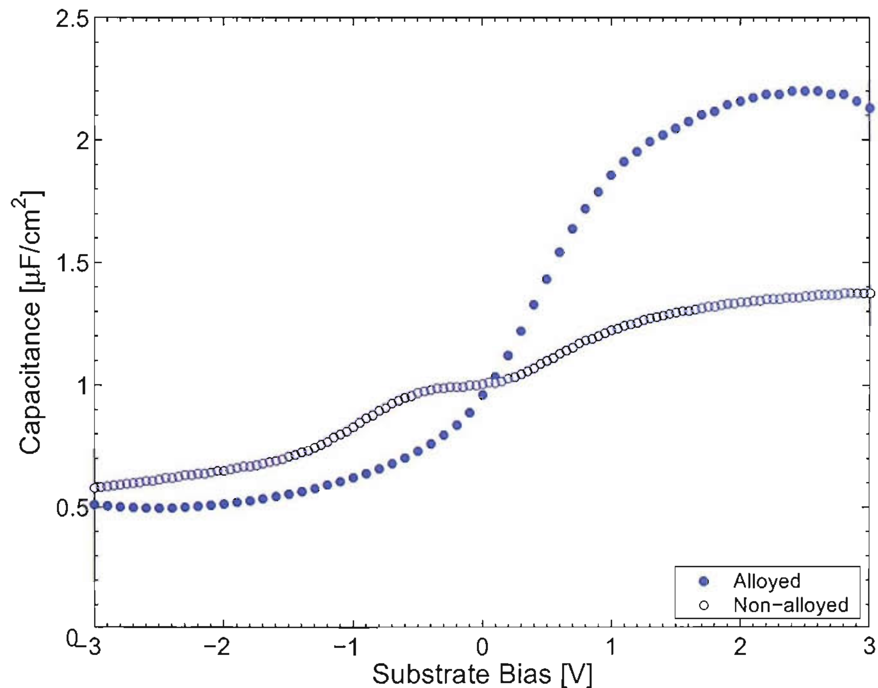

Figure 5.11: Comparison C-V characteristics of the alloyed and non-alloyed samples, with the TiO_2 layers grown at 500 °C.

5.4.5 Thermal Oxidation: 450, 500 and 550 °C

It has been shown in Section 5.4.2 that TiO_2 layer can be grown at 500 °C. It is therefore important to optimise the oxidation temperature by comparing the electrical characteristics of TiO_2 layers grown at temperature around 500 °C. Figure 5.12 shows the I-V characteristics of the TiO_2 layers grown at 450, 500 and 550 °C. It can be observed that the leakage current decreases with increases in T_{ox}. Comparing the I-V characteristics of TiO_2 layers grown at T_{ox} between 450 and 550 °C in Figure 5.12, it is believed that as the oxidation temperature increases, the oxide layer will be closer to TiO_2 stoichiometry. TiO_2 with better stoichiometry will have lower leakage current [117]. However, the formation of a SiO_2 interfacial layer at high temperature will also reduce the current. Figure 5.12 shows that the leakage current difference between 500 °C and 550 °C is relatively small. This indicates that there is not much change in the TiO_2 stoichiometry and in the interfacial layer thickness for the oxide layers grown at these two temperatures. A more detailed analysis of the I-V characteristics and the current transport mechanism will be presented in Chapter 7.

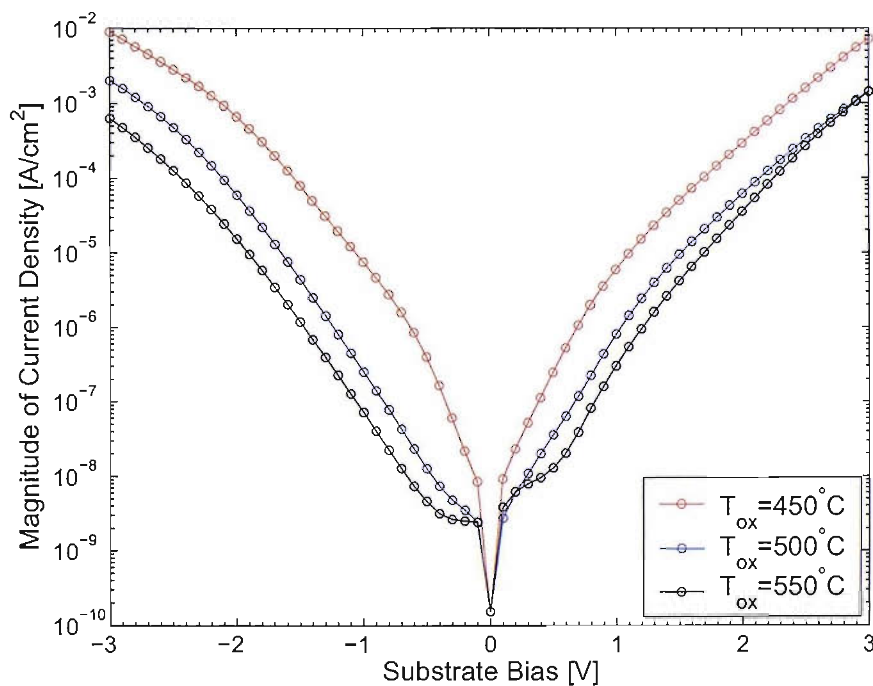

Figure 5.12: I-V characteristics of the TiO_2 layers grown at different oxidation temperatures T_{ox}.

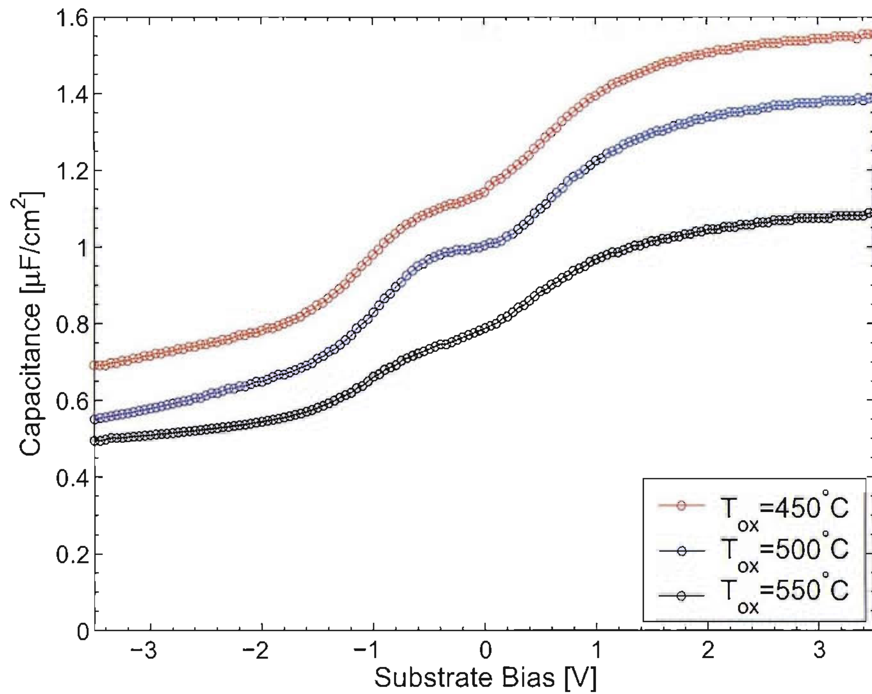

Figure 5.13: C-V characteristics of the TiO_2 layers grown at different oxidation temperatures T_{ox}.

The C-V characteristics of the TiO_2 layers grown at different T_{ox} are shown in Figure 5.13. It is noted that the C-V characteristic of the samples show a 'bump' feature around 0 V. This is most likely to be due to the non-equilibrium effects similar to those observed at high frequency C-V measurements of silicon carbide (SiC) MOS capacitors at room temperature [118] and at low temperatures C-V measurements in Si MOS capacitor [119, 120]. The charge exchange of the surface states is due to the emission or capture of a charge [119]. The emission time constant of the surface states depends on the energy difference between the surface state state energy and the band edges whilst the time constant of the capture of carriers by the surface state depends on the free carrier density at the surface [119]. When the device is in inversion mode, all the surface states are negatively charged. When changing the bias such that the device is driven into depletion, the capture time constant of the surface state is high because the hole concentration at the Si surface is low in the inversion or depletion region. The surface states very close to the conduction band edge are able to follow the changing bias and emit electrons because the emission time constants are very short. The other negatively charged surface states can only be discharged when the hole concentration at the surface are high enough for the holes capture to occur. When the capture of hole happens, the slope of C-V characteristic will change, which results in the 'bump' feature in Figure 5.13. The width of the 'bump' depends on the negatively

charged surface state density in non-equilibrium. It is noted from Figure 5.11 that the C-V characteristic of the alloyed sample has no 'bump' feature. This could be due to the reduction of the surface state density during the alloying process or the high leakage current in the alloyed sample.

Table 5.6: The maximum capacitance C_{ox} and the minimum capacitance C_{min} of the samples grown under different oxidation temperatures T_{ox}.

Sample	C_{ox} [$\times 10^{-6}$ F/cm^2]	C_{min} [$\times 10^{-7}$ F/cm^2]
$T_{ox} = 450°C$	1.56	6.91
$T_{ox} = 500°C$	1.39	5.52
$T_{ox} = 550°C$	1.09	4.95

Table 5.6 summarizes the values of C_{ox} and C_{min} of the samples. It is observed that the C_{ox} decreases with increasing oxidation temperature. There are three possible reasons. Firstly, the increase of the titanium oxide thickness with increased oxidation. Secondly, the increase of the interfacial layer thickness between the TiO_2 and the Si [82, 111]. Thirdly, the diffusion of Al from top metal electrode into the TiO_2 layer, which reduces the total effective oxide thickness. It will be shown in Chapter 7 that Al from the top electrode can diffuse into the TiO_2 layer even at room temperature. It is believed that the diffusivity of Al decreases with better stoichiometry in the TiO_2 layer. As better stoichiometry is expected for the TiO_2 layer formed at higher temperature, the diffusion of Al into the oxide layer is less significant and the total effective oxide thickness of the oxide grown at 550 °C will be thicker than those grown at lower temperatures, hence resulting in a lower C_{ox}. The minimum capacitance C_{min} of the samples also decreases as the oxidation temperature increases. This is likely to be due to the capacitance associated with the interface traps [45].

From the discussion above, it is believed that better stoichiometry can be achieved at 550 °C due to lower leakage current. It is noted that there is little difference between the leakage current of the oxides grown at 500 and 550 °C. Therefore, oxides grown at either 500 or 550 °C can be chosen for further analysis. However, the analysis of the current transport mechanisms is very difficult for under-oxidized TiO_2 as there is no good model for the effect of oxygen vacancies on the conduction. When the sample is slightly over-oxidized, a stoichiometric TiO_2 layer will form together with a thin interfacial layer. The

latter is easier to incorporate in the transport models. In addition, the effect of surface states in the oxide grown at 550 °C is lower compared to those formed at lower oxidation temperatures. Therefore, TiO_2 grown at 550 °C will be analysed in more details in the next chapters.

5.4.6 Summary

TiO_2 layers were grown by thermal oxidation of e-beam evaporated Ti thin films at temperatures between 300 and 550 °C for 30 mins. The thickness of the Ti thin films is 10 nm. For samples grown at 300 and 400 °C, there is a huge leakage current due to poor quality of the oxide layers. From the I-V characteristics of the samples, the optimised oxidation temperature for thermally grown TiO_2 is determined to be 550 °C. The TiO_2 layer grown at this temperature gives minimum leakage current and it is believed that this is due to better stoichiometry of the oxide.

It has been demonstrated that annealing the samples in N_2 ambient at 700 °C can reduce the leakage current sharply, regardless of the oxidation temperatures. However, this is likely to be due to the growth of an interfacial SiO_2 layer at the TiO_2/Si interface. This is undesirable because the F-N tunneling current will be reduced due to the high barrier of the SiO_2 layer. Therefore, post oxidation annealing is not beneficial for the thermally grown TiO_2 layer.

Alloying increases the leakage current and maximum capacitance of the samples. This is due to the diffusion of Al into the TiO_2 during the alloying process, which reduces the total effective oxide thickness and deteriorate the electrical properties of the TiO_2 layer. It has been shown that the Al back contact at low resistivity substrate (0.02 Ωcm) is ohmic. Hence, alloying is not required for the Al back contact.

In summary, TiO_2 layer can be grown from e-beam evaporated Ti thin film at 550 °C. No post oxidation annealing is required for the thermally grown oxide layer, and no alloying is required for the Al back contact on a highly doped Si substrate.

5.5 TiO_2 layer grown by Molecular Beam Epitaxy

A molecular beam epitaxy (MBE) deposition system is very useful for growing thin films. It can accurately control the thickness of the thin film. It can also deposit a vast varieties of compounds and mixtures by controlling the timing and flux of the molecular beams [107, 109]. Because of these advantages of the MBE system, the combinatorial methods for synthesis and screening of materials (also known as composition-spread) can be used [121, 122]. This method involves the growth of a continuous film of varying composition, which is then discretely characterised. The MBE system can be used to grow a huge amount of compounds and their mixtures. From there, the dielectric constant and interfacial properties of the thin film can be characterised. The systematic correlation between the chemical and structural properties and also the electrical properties can be shown. Therefore, the factors that influence the electrical properties of the thin film can be studied and understood.

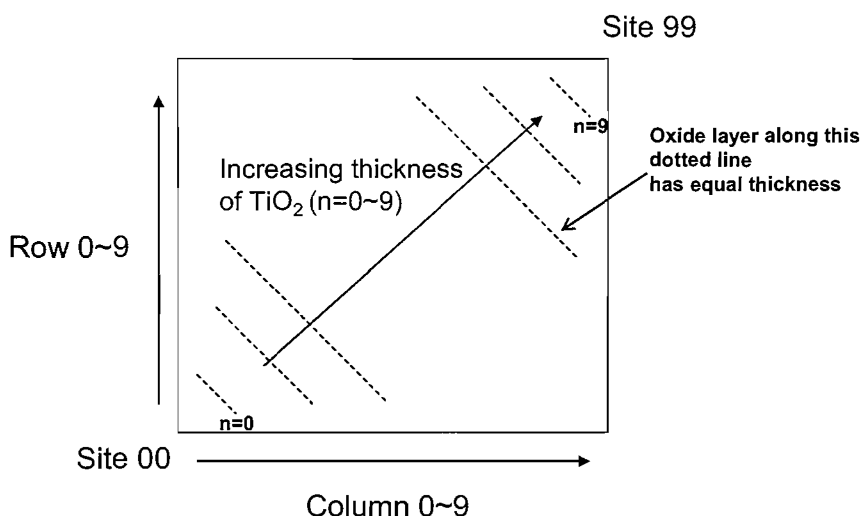

Figure 5.14: The MBE sample layout. Site 00 has the minimum TiO_2 thickness. The oxide thickness gradually increases to Site 99, which has the maximum thickness. For site 00, n=1; for site 01 and site 10, n=0.5, and so on.

An MBE deposition system was used to grow TiO_2 layer. The Ti atoms were evaporated at temperatures between 1750 and 1850 °C using an effusion cell. The evaporated Ti atoms can react with an oxygen flux near the substrate to form the oxide layer on the Si substrate. With the implementation of an oxygen cracker in the system, atomic oxygen with higher reactivity are produced. The oxygen cracker is used to produce a source of atomic oxygen. By passing the molecular oxygen through an electron bombardment heated fine tungsten

capillary, the molecular oxygen is cracked to atomic oxygen by bouncing along the hot walls [123]. This increases the reactivity between the oxygen and titanium atoms, and allows the growth of a better quality TiO_2 layer. Due to a special design in the system, the concentration of the TiO_2 layer will be the same but the oxide thickness will vary throughout the surface, as shown in Figure 5.14. This is useful for characterisation of the TiO_2 layer as the I-V and C-V characteristics will vary with the oxide thickness, and the electrical and interfacial properties of the TiO_2 layer can be studied.

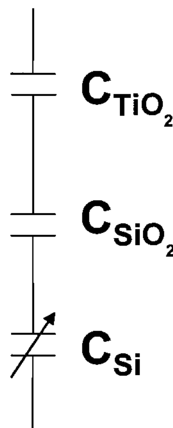

Figure 5.15: A simple capacitor model for the MBE sample, C_{TiO_2} and C_{SiO_2} are the capacitances of the TiO_2 and interfacial SiO_2 layers, respectively. The variable capacitance, C_{Si}, is the capacitance due to the depletion region in the silicon substrate.

The oxide layer deposited by the MBE system can always be modelled as three capacitors connected in series mode, as shown in Figure 5.15. C_{TiO_2}, C_{SiO_2} and C_{Si} are the capacitance per unit area due to the as-grown TiO_2 layer, the interfacial SiO_2 layer and the depletion region in the Si substrate, respectively. Therefore, the total capacitance per unit area can be expressed as

$$\frac{1}{C} = \frac{1}{C_{TiO_2}} + \frac{1}{C_{SiO_2}} + \frac{1}{C_{Si}} = \frac{d_{TiO_2}}{\epsilon_{TiO_2}\epsilon_0} + \frac{d_{SiO_2}}{\epsilon_{SiO_2}\epsilon_0} + \frac{d_{Si}}{\epsilon_{Si}\epsilon_0} \tag{5.1}$$

where d_{TiO_2} and ϵ_{TiO_2} are the thickness and dielectric constant of the TiO_2 layer, respectively, d_{SiO_2} and ϵ_{SiO_2} are the thickness and dielectric constant of the SiO_2 layer, respectively, and d_{Si} and ϵ_{Si} are the depletion width and dielectric constant of the silicon substrate, respectively. d_{Si} varies with the applied bias, and hence the capacitance due to the depletion region in the Si substrate will vary with the applied bias as well. The TiO_2 thickness d_{TiO_2} can be expressed as

$$d_{TiO_2} = n\Delta t + d_0 \tag{5.2}$$

where n is the index for different oxide thickness as shown in Figure 5.14, and n=[0, 0.5, 1, ..., 9]. The oxide thickness is minimum at n=0, and maximum at n=9. d_0 is the TiO_2 thickness at site 00 and Δt is the difference of the oxide thickness between n and $n+1$. Δt can be estimated because the maximum oxide thickness can be determined from the fabrication process, and the minimum oxide thickness can be assumed to be zero. Substituting Equation 5.2 into Equation 5.1, the following expression can be obtained:

$$\frac{1}{C} = \frac{\Delta t}{\epsilon_{TiO_2}\epsilon_0} n + \frac{d_0}{\epsilon_{TiO_2}\epsilon_0} + \frac{d_{SiO_2}}{\epsilon_{SiO_2}\epsilon_0} + \frac{d_{Si}}{\epsilon_{Si}\epsilon_0} \tag{5.3}$$

By plotting the graph of $1/C$ versus n, the slope S and the y-axis intercept $y_{intercept}$ of the linear line can be expressed as:

$$S = \frac{\Delta t}{\epsilon_{TiO_2}\epsilon_0} \tag{5.4}$$

$$y_{intercept} = \frac{d_0}{\epsilon_{TiO_2}\epsilon_0} + \frac{d_{SiO_2}}{\epsilon_{SiO_2}\epsilon_0} + \frac{d_{Si}}{\epsilon_{Si}\epsilon_0} \tag{5.5}$$

The values of S and $y_{intercept}$ can be extracted from the graph of $1/C$ versus n. Using Equation 5.4 and assuming a reasonable value for Δt, ϵ_{TiO_2} can be determined. Then, from Equation 5.1 and 5.5, as C_{Si} can be assumed to be negligible in the accumulation mode of the device at site 00, d_{SiO_2} can be determined by assuming a reasonable value for d_0, which is supposed to be closed to zero.

5.5.1 Experimental Details

The process flow of the TiO_2 MOS capacitors fabricated by the MBE technique is shown in Figure 5.16. *p*-Si substrate with resistivity of 0.02 Ωcm were used. First, the wafers were RCA cleaned and HF treated before a 1 μm Al layer was deposited at the back of the Si substrate. The front side of the Si substrates were etched with HF just before the growth of the TiO_2 layer. The Ti effusion temperature was 1800 °C, and the substrate temperature was 300 °C. The deposition time was 900 seconds. Two different setups were used to grow the TiO_2 layers: with and without an oxygen cracker. The partial pressure of the oxygen were 7×10^{-7} torr and 5×10^{-6} torr for setup with and without the oxygen cracker, respectively. For both cases, the TiO_2 layer thickness at site 99 is estimated to be 30 nm from previous calibration. After the growth of the oxide layers, a 300 nm thick gold electrode was deposited on the oxide layers through a shadow mask. The size of the gold pads is 1 mm×1 mm.

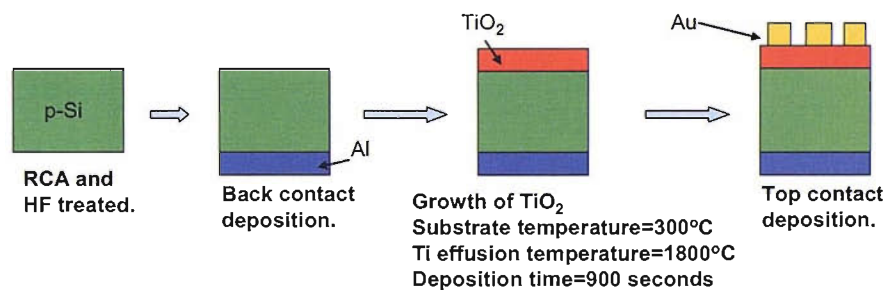

Figure 5.16: Process flow of the TiO_2 MOS capacitors fabricated by MBE.

Atomic force microscopy (AFM) and scanning electron microscopy (SEM) were used to inspect the surface roughness of the oxide layers. AFM measurements were performed using Topometrix Accurex 2 and the SEM measurements were done using a Leo 1450VP SEM. The I-V characteristics of the oxide layers were measured by HP4155A. The principle of operation of AFM and SEM are presented in Chapter 6.

5.5.2 Physical Observation

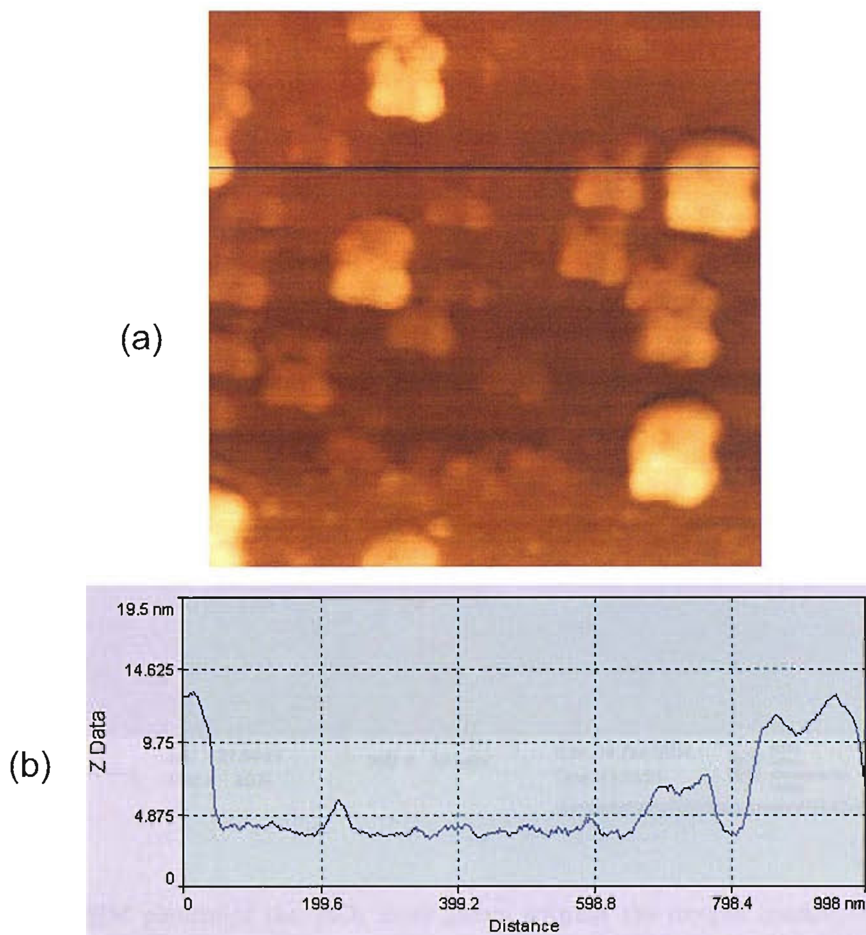

Figure 5.17: (a) The AFM picture of the TiO_2 layer grown without the oxygen cracker. (b) Line measurement refers to the blue line across the AFM picture (a). The pictures show that the surface is non-uniform and consists of extruding structures with about 14 nm height.

Unlike the thermally oxidized samples, the entire surface of the MBE sample grown without the oxygen cracker looks rough and grainy. There are bright spots visible throughout the surface when viewed under the microscope (in reflection mode). These bright spots could be due to the extruding structures or pits on the surface. The AFM scan of the sample in Figure 5.17 clearly show large features on the oxide. In addition, the SEM picture of the sample in Figure 5.18 shows that there are pits scattered on the oxide surface. One possible explanation is that not all the Ti atoms reacted fully with the oxygen molecules to form TiO_2 molecules on the Si substrate. Instead, some of the Ti atoms were deposited on the substrate directly, which results in the grainy structure and the pits on the oxide layer.

As for the sample grown with the implementation of the oxygen cracker, there are no bright spots visible under the microscope. This implies a better quality of oxide layer, as the Ti atoms have better reactivity with the oxygen atoms produced by the oxygen cracker.

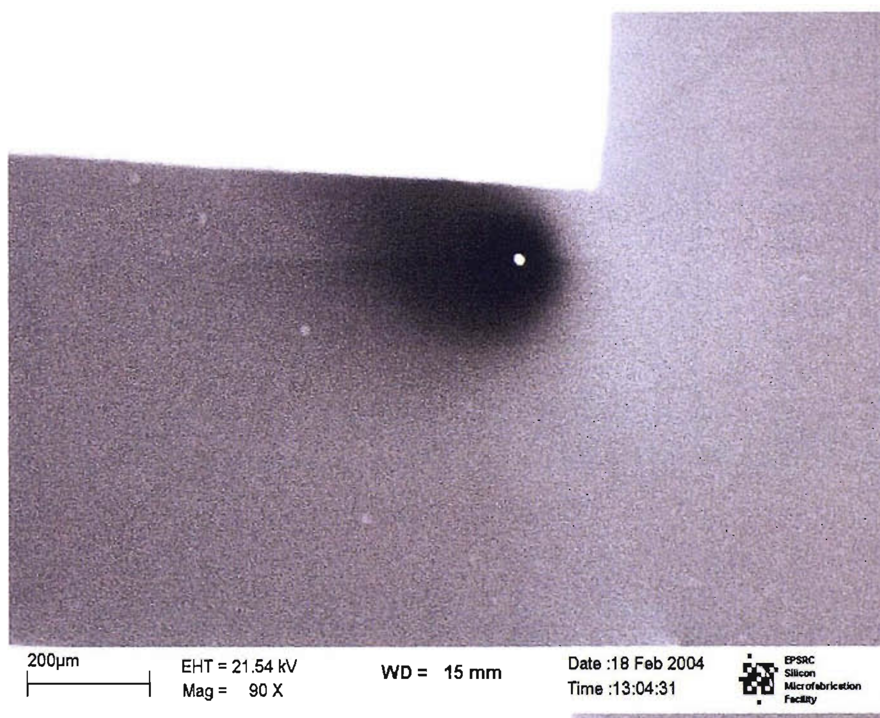

Figure 5.18: The SEM picture of the TiO_2 layer grown without the oxygen cracker. The pit is just beside the gold pad, which is showing white in the picture. The diameter of the pit is about 200 μm.

5.5.3 Electrical Analysis

As shown in Figure 5.14, the oxide thickness grown on the sample increases along the diagonal of the sample. The device at site 00 has minimum oxide thickness and the device at site 99 has maximum oxide thickness. Therefore, it is expected that the leakage current flowing through the devices will decrease along the diagonal as the oxide thickness increases. During the I-V measurements of the samples, it is observed that for the same device if the probe tip remains at the same location of the electrode, the leakage current will increase in a subsequent measurement. Therefore, unless some unusual characteristics showed up, the first measurement of the device was always recorded for the analysis.

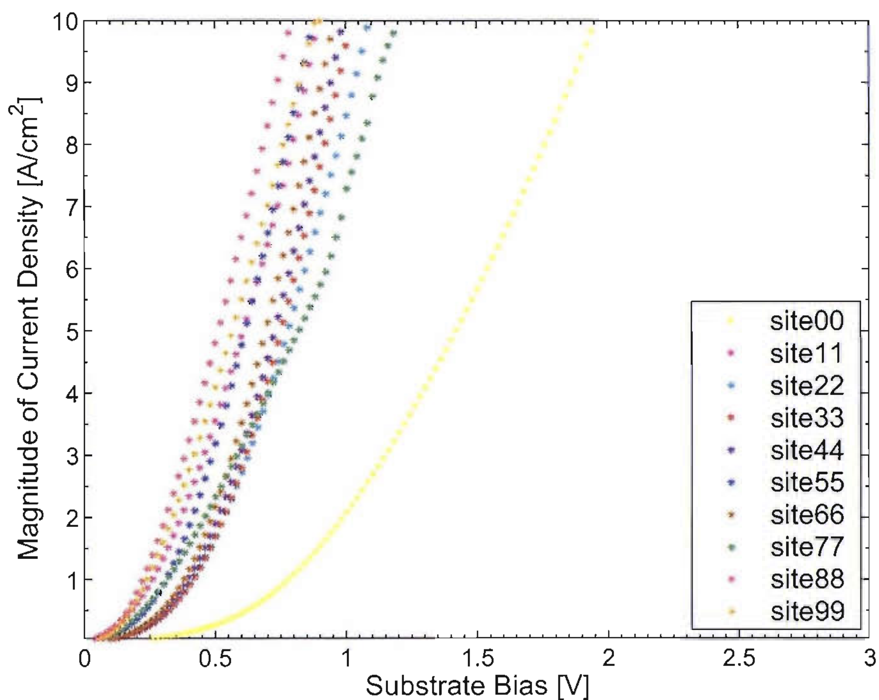

Figure 5.19: The I-V characteristics of the TiO_2 layers along the diagonal of the sample grown without the oxygen cracker.

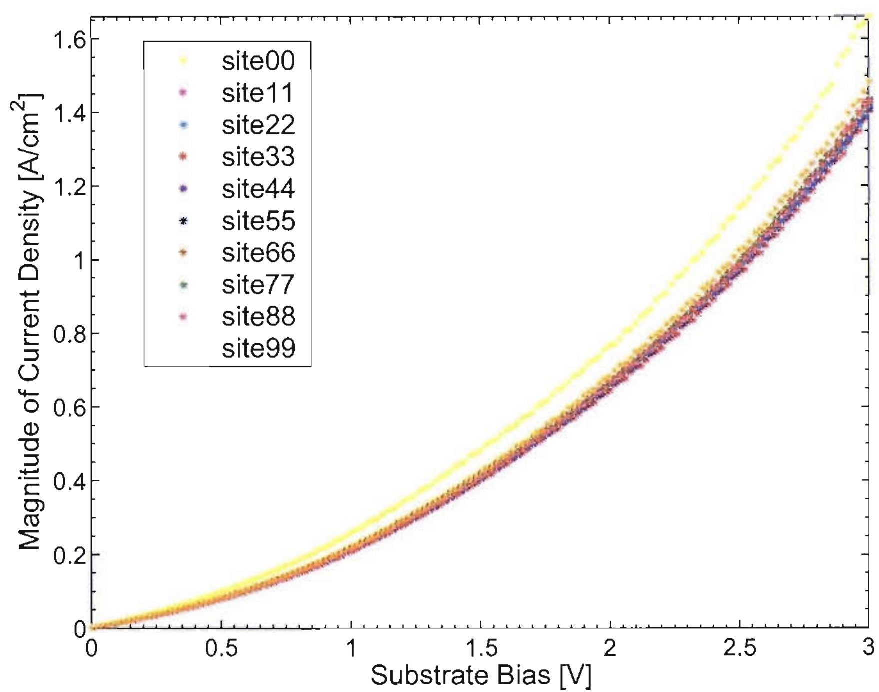

Figure 5.20: The I-V characteristics of the TiO_2 layers along the diagonal of the sample grown with the oxygen cracker.

Figure 5.19 and 5.20 shows the I-V characteristics of the MOS capacitors along the diagonal of the sample grown without and with the oxygen cracker, respectively. It is observed that the magnitude of the current density has no correlation to the oxide thickness in both cases. This indicates that the oxide layers were leaky and the increase in oxide thickness has no effect on reducing the magnitude of the leakage current. It is noted that the TiO_2 layer grown with the oxygen cracker shows lower current density than that grown without the oxygen cracker. This is expected because the TiO_2 layer grown without the oxygen cracker show grainy structures and pits. These features can become centers of high electric field, lead to oxide breakdown, and result in huge leakage current.

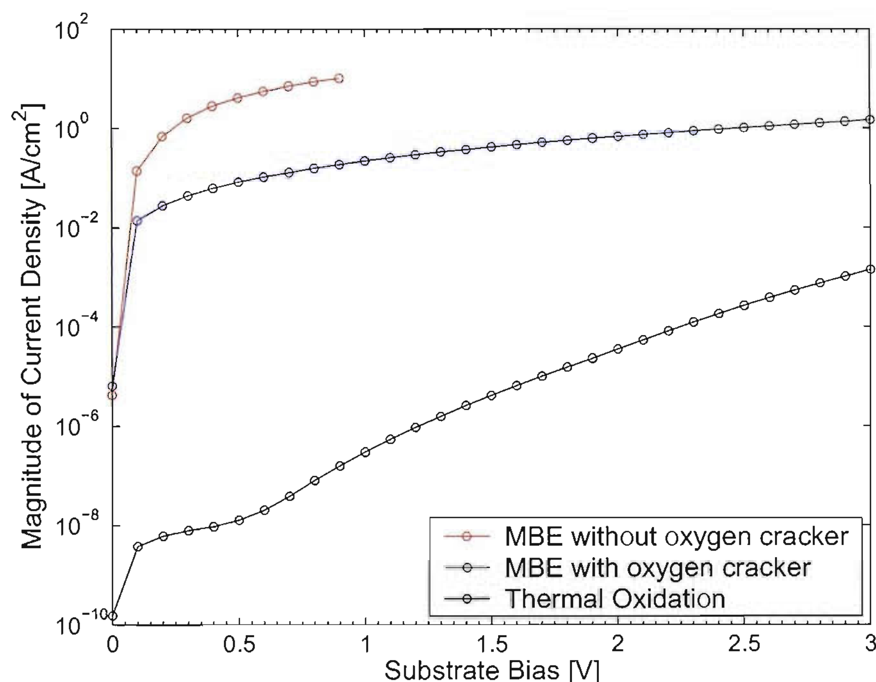

Figure 5.21: The I-V characteristics of the TiO_2 layers grown by MBE technique and thermal oxidation on e-beam evaporated Ti thin film. For samples grown by the MBE technique, I-V characteristic of device at site 99 was chosen. For thermal oxidation technique, the oxide layer was grown from 10 nm Ti thin film at 550 °C.

Figure 5.21 compares the I-V characteristics of the MBE grown TiO_2 layers and the thermally grown TiO_2 layer. For MBE grown TiO_2 layers, the I-V characteristic were based on the device at site 99, which has an oxide thickness of about 30 nm. For thermally grown TiO_2 layer, the oxide was grown from a 10 nm Ti thin film at 550 °C, which will result in a TiO_2 layer thickness of 18 nm as shown in Table 5.2. It is observed that the implementation of the oxygen cracker can help to reduce the leakage current by two orders of magnitude in the MBE grown samples. However, the thermally grown TiO_2 layer has a

much lower leakage current compare to those of the MBE grown TiO_2 layers, even though the thermally grown oxide layer is thinner than those of the MBE grown TiO_2 layers. This indicates that thermal oxidation of e-beam evaporated Ti thin film is a better technique as it produces oxide layers with lower leakage current.

5.5.4 Summary

An MBE technique was used to grow a continuous TiO_2 layer of varying thickness. The TiO_2 layer was formed on the Si substrate by the reaction with an oxygen flux. It is observed that the oxide layer grown without an oxygen cracker has grainy structures and pits on the surface, and exhibits huge leakage current. The oxide layer quality can be improved by growing the oxide layer with the implementation of an oxygen cracker, as the oxide layer shows a visually more uniform surface, and the devices exhibit lower leakage current than those fabricated without the oxygen cracker. However, the main objective of using the MBE technique is to characterise the dielectric constant and interfacial properties of the TiO_2 layers based on the varying oxide thickness. In both cases, i.e. in molecular oxygen or atomic oxygen environment, the magnitude of the current density of the TiO_2 MOS capacitors exhibit no correlation to the oxide thickness. This indicates that further optimisation is required to improve the oxide quality before the advantages offered by the MBE technique can be fully exploited.

Besides the reactivity of the gas in the reaction chamber (which is molecular oxygen and atomic oxygen in this case), the oxide quality is also determined by the titanium effusion temperature and the deposition time. The Ti vapour pressure varies with the effusion temperature. A 50°C difference in the effusion temperature will make one order of magnitude difference in Ti vapour pressure [4], which will affect the growth of TiO_2 significantly. Lower Ti effusion temperature will allow the Ti atom to react with oxygen and form TiO_2 at the substrate surface. Longer deposition time is necessary to grow the oxide to the required thickness because of the slow growing rate. Therefore, lower Ti effusion temperature and longer deposition time should result in a better quality oxide.

5.6 Conclusion

Various fabrication techniques for growing thin oxide layer have been reviewed. For thermal oxidation technique, TiO_2 layers were grown from e-beam evaporated Ti thin films at temperatures between 300 and 550 °C. It has been shown that the optimised oxidation temperature is 550 °C, as the oxide layer grown at that temperature gives minimum current. The effect of post oxidation annealing on the as-grown oxide layer has been investigated. It is shown that post oxidation annealing in nitrogen at 700 °C reduces the current by introducing an SiO_2 interfacial layer between the TiO_2 and Si substrate. This is undesirable because it will decrease the F-N tunneling current as well. Hence, post oxidation annealing is not beneficial for thermally grown TiO_2 layers. It has also been shown that no alloying is required as the Al back contact is ohmic due to the highly doped Si substrate. In addition, alloying can cause diffusion of Al atoms from the top electrode into the TiO_2 layer, which will reduce the oxide thickness and alter the oxide electrical properties.

For the MBE technique, TiO_2 layers were grown by reactions of evaporated Ti atoms with an oxygen flux. The oxide layers have a varying thickness to allow the characterisation of the dielectric constant and interfacial properties. It is observed that an oxide layer of better quality can be grown if the Ti atom are reacted with atomic oxygen instead of the molecular oxygen. However, the leakage current through the TiO_2 MOS capacitors shows no correlation with the oxide thickness. Further optimisation is required to improve the oxide quality.

By comparing I-V characteristics of the thermally grown and the MBE grown TiO_2 layers, it is observed that the thermally grown TiO_2 layer exhibits lower leakage current, even though the oxide thickness is thinner than those grown by the MBE technique. This suggests that thermal oxidation of e-beam evaporated Ti thin film can produce better oxide quality than the MBE technique. Therefore, more analysis will be performed on the thermally grown TiO_2 layer in later chapters.

Chapter 6

Structural Analysis of Thermally Grown TiO_2

6.1 Introduction

The optimised oxidation temperature for thermally grown TiO_2 layers is 550 °C, as determined in Chapter 5. Another important parameter is the thickness of the TiO_2 layer, as it will affect the I-V and C-V characteristics of the oxide. The TiO_2 layer thickness can be determined from the thickness of the Ti thin film, according to the expansion factors listed in Table 5.2. If the Ti thin film is fully oxidized, the resulting TiO_2 layer thickness will be 1.8 times that of the Ti thin film. The simulation results in Chapter 4 indicates that the tunnel barrier thickness should be around 15 nm to give a drain current swing of four orders of magnitude in VMISTT. Therefore, TiO_2 layers grown at 550 °C from 7 and 10 nm Ti thin films are studied and compared.

One of the drawbacks of thermal oxidation of Ti thin film is the uncertainty in the film thickness and the stoichiometry of oxide formed during oxidation, which depends on the oxidation conditions and the e-beam evaporated Ti thin film thickness [83]. As can be seen from Table 5.2, Ti has various oxide phases and each has different expansion factor. This will lead to the uncertainty in the oxide thickness if the oxide phase is unknown. In addition, the e-beam evaporated Ti thin film thickness is estimated from the evaporation rate and the evaporation time. This can also result in uncertainty in the oxide thickness even if the oxide phase is known. Hence, scanning electron microscope (SEM) was used to produce a microscopy view of the TiO_2 MOS capacitor structure so that the physical

thickness of the oxide layers can be determined.

Another issue related to thermal oxidation is the interfacial oxide layer at the TiO_2/Si substrate [81]. Titanium silicates can be grown at temperature above 400° C [124]. As the optimised oxidation temperature is 550° C, it is possible that silicates will be formed during the oxidation process. Time-of-flight secondary ions mass spectrometry (TOF-SIMS) was used to perform elemental analysis of the TiO_2 layers grown at 550° C from 7 and 10 nm of Ti thin films. It was used to analyse the composition and the depth profile of the thermally grown oxide on Si substrates.

As mentioned in previous chapter, TiO_2 has three different crystalline polymorphic forms: anatase, rutile and brookite [70]. Among these three different forms, anatase and rutile are the more commonly observed crystalline forms in TiO_2 [125]. The crystal structure of the thermally grown oxide layer is determined by x-ray diffraction (XRD).

In this chapter, the electrical characterisation of the TiO_2 layers of different thicknesses are presented. This is followed by the focus of this chapter, the structural analysis of the TiO_2 layers of different thicknesses. An oxide thickness is chosen for further characterisation of the tunnel barrier in the next chapter.

6.2 Experimental Details & Instruments

6.2.1 Experimental Details

TiO_2 MOS capacitors were fabricated to study the electrical and structural properties of the TiO_2 layers grown from 7 nm Ti thin films. The process flow is shown in Figure 6.1. The experimental details is similar to that described in Section 5.4.1. 7 nm Ti thin films were deposited by vacuum e-beam evaporation on p-Si (resistivity of 0.02 Ωcm) without any substrate heating. The wafers were RCA cleaned and HF treated before evaporation. The evaporation pressure was 2.25×10^{-6} Torr, and the evaporation rate of Ti was 0.3 nm/s. The samples were oxidized at 550 °C for 30 minutes. After that, a 1 μm thick Al top electrode was vacuum evaporated using a shadow mask to make various contact pad sizes and a 1 μm Al layer was evaporated on the back surface. The process listing is shown in Appendix B.3. The TiO_2 layers grown from 10 nm Ti thin films are from the second batch

described in Section 5.4.1.

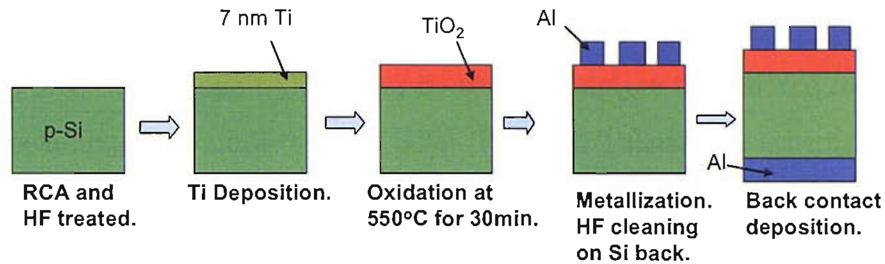

Figure 6.1: Process flow of the TiO_2 MOS capacitors.

The electrical measurement setup was same as that described in Section 5.4.1. Cross-sectional SEM was done using a Hitachi S-4800 microscope to visualise the oxide layers grown. TOF-SIMS measurements were performed with an ION-TOF TOF.SIMS 5 instrument. For erosion a 500 eV Cs^+ beam with a target current of 52 nA was applied to an area of 300×300 μm^2. A 25 keV Bi_3^+ beam, with a target current of 0.33 pA, was used for analysis. The analysed area was approximately 100×100 μm^2. During the TOF-SIMS experiment, the analysed intensity as a function of the sputtering time was stored. The final crater depth was determined by a mechanical profiler and this crater depth was transferred to a depth scale assuming a constant sputter rate. This assumption is not exactly correct because the sputtering rate varies with the chemical composition of the material.

XRD was performed with a Siemens D5000 X-ray diffractometer. As the diffracted beams from the 18 nm TiO_2 layers can be weak for XRD analysis, thicker oxide layers were grown from 100 and 500 nm vacuum e-beam evaporated Ti thin films without substrate heating. The wafers were RCA cleaned and HF treated before evaporation. The samples were oxidized at different temperatures (550 and 750 °C) for 2 hours. The process listing is shown in Appendix B.5.

6.2.2 Experimental Instruments

(a) Atomic Force Microscope

An Atomic Force Microscope (AFM) can be used to analyse the surface roughness of the samples by scanning the sample surface [126]. Figure 6.2 shows the schematic of an AFM machine. The laser beam is directed towards the end of the cantilever. As the probe tip (which is mounted at the end of the cantilever) scans across the sample surface, the topographic features will cause deflection of the tip and the cantilever, which reflects the laser beam towards a four segment photodetector. The difference in the light intensity on the sectors of the detector indicates the position of the laser spot on the detector. Thus, the amount of deflection of the cantilever can be calculated and the surface roughness can be analysed.

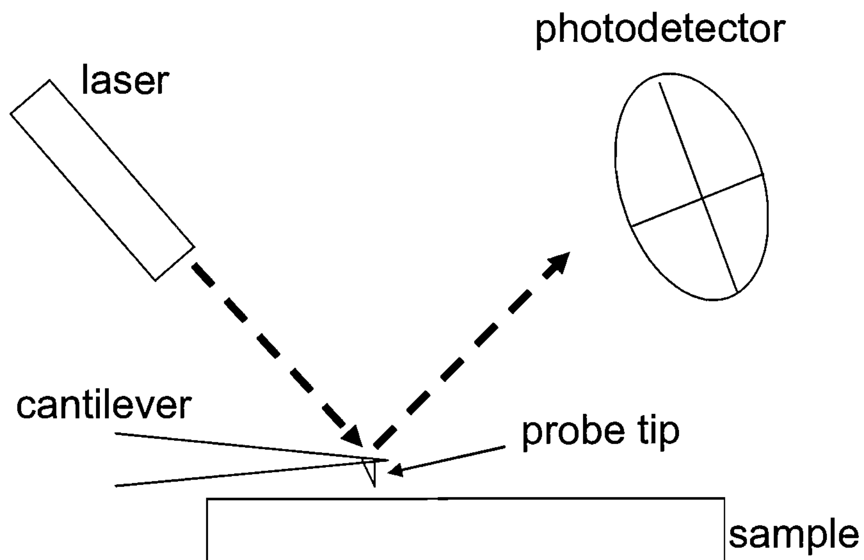

Figure 6.2: Schematic of an AFM machine.

(b) Scanning Electron Microscope

A Scanning Electron Microscope (SEM) can create images with magnification greater than 100,000 [127]. This is much higher than the normal light microscope magnification, which is less than 1000. This is because the wavelength of the electron is about 100,000 smaller than the wavelength of the light. Figure 6.3 shows the schematic of an SEM machine. The sample (target) is placed inside a vacuum chamber. An electron beam will be focused to a very fine spot through a series of magnetic lenses. The focused beam is moved back and forth across the target by a set of scanning coils. As the electron beam hits each spot on the sample, secondary electrons are knocked out from the sample surface. These secondary electrons are counted by a detector and its signal is sent to an amplifier. The final image is built up from the number of electrons emitted from each spot on the sample.

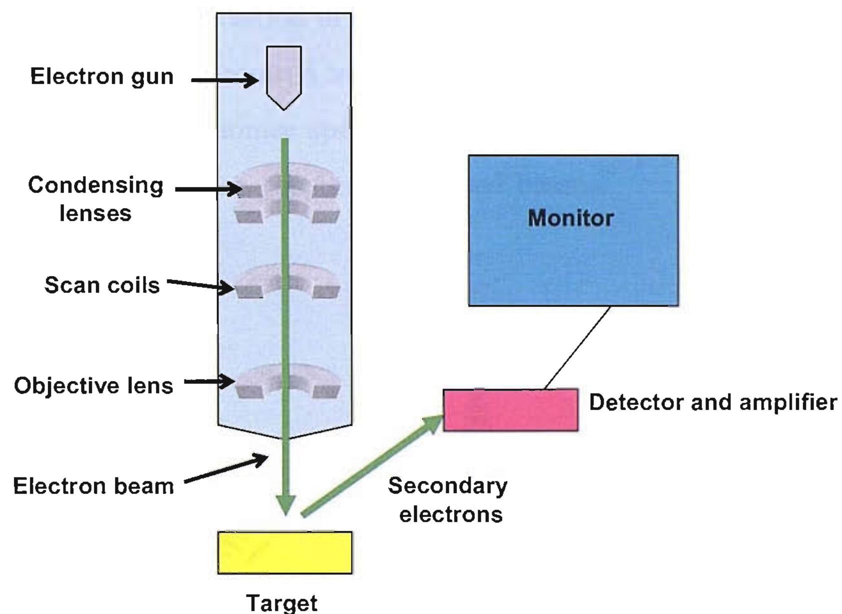

Figure 6.3: Schematic an SEM machine. Figure based upon [127].

(c) Time-of-flight secondary ion mass spectrometry (TOF-SIMS)

Time-of-flight secondary ion mass spectrometry (TOF-SIMS) is used to determine the composition of the sample surface constituents [128, 129]. It can also be used for depth profiling. Figure 6.4 illustrates the schematic of a TOF-SIMS machine. A pulsed primary ion beam is directed to the sample to desorb and ionize species from the sample surface. These ionized species are known as secondary ions, and are accelerated into a mass spectrometer. As the "time-of-flight" of an ion from the sample surface to the detector is proportional to the square root of its mass, the ions with different masses will arrive at the detector separately. The next pulse of primary ions will start after all the secondary ions have been analyzed so that the heavy ions in the first pulse will not be overtaken by the light ions in the second pulse. By measuring the "time-of-flight" of the ions, the masses can be analyzed and the composition of the sample can be studied. For the application in depth profiling, sputtering is required to remove a layer of the sample surface so that the pulsed primary ion beam can ionize species from the revealed surface. This can be done during the time interval between consecutive pulsed beams.

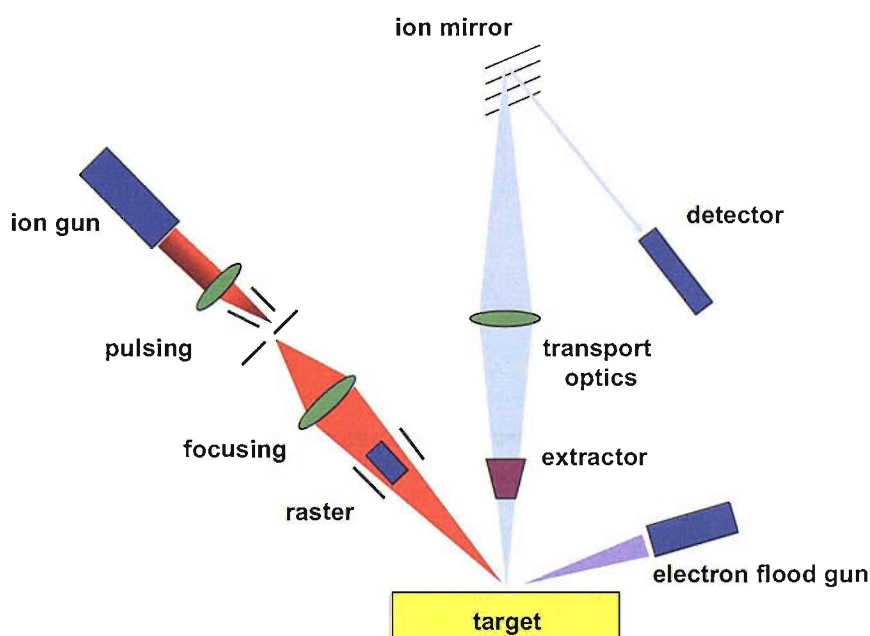

Figure 6.4: Schematic a TOF-SIMS machine. Figure based upon ref [130].

(d) X-ray diffraction (XRD)

X-ray diffraction (XRD) is a technique to investigate of the structure of the material [131, 132]. It can produce a spectrum of diffraction peak as a function of the x-ray diffraction angle. From the diffraction peaks, the crystal structure of a known material can be determined. Figure 6.5 illustrates the schematic of a x-ray diffractometer. The x-ray is directed towards the target, and the diffracted rays are collected at the detector. The detector and the sample holder are mechanically coupled with a goniometer so that the rotation of the detector relative to the rotation of the sample holder is fixed at 2:1 ratio. The divergent slits and the receiving slits help to reduce background noise, limit scattered radiation and collimate the radiation.

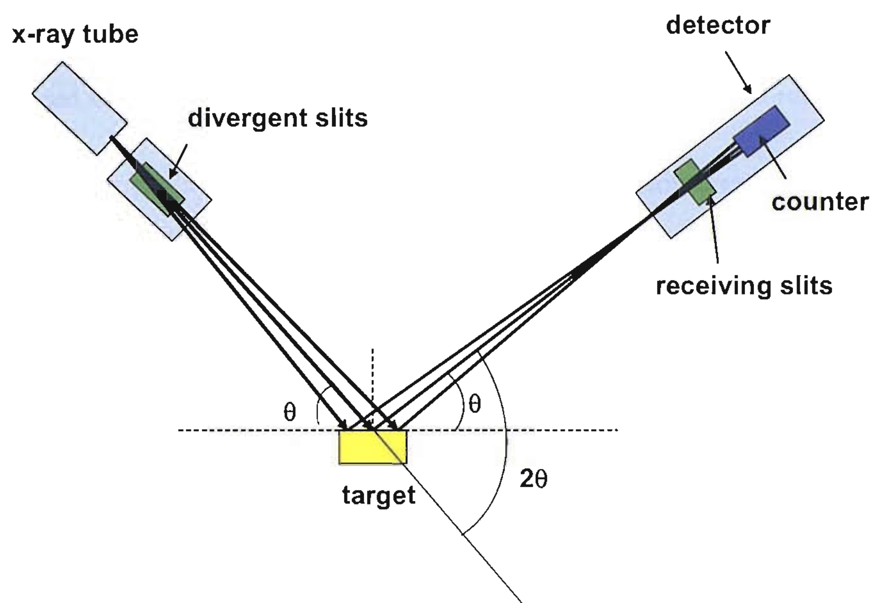

Figure 6.5: Schematic of a x-ray diffractometer. Figure based upon ref [131].

Theory of X-ray Diffraction

Diffraction is a phenomenon of waves interaction with a regular structure with a repeat distance similar to the wavelength of the waves. A material with crystalline structure has an orderly arrangement of atoms [131, 132]. The wavelength of x-rays is comparable to the interatomic distances in crystalline solids, which is on the order of a few angstroms. Therefore, diffraction can occur when x-ray beam is directed towards a crystalline solid. The diffracted waves will consist of sharp interference maxima, which can be used to determine the crystal structure of the solid.

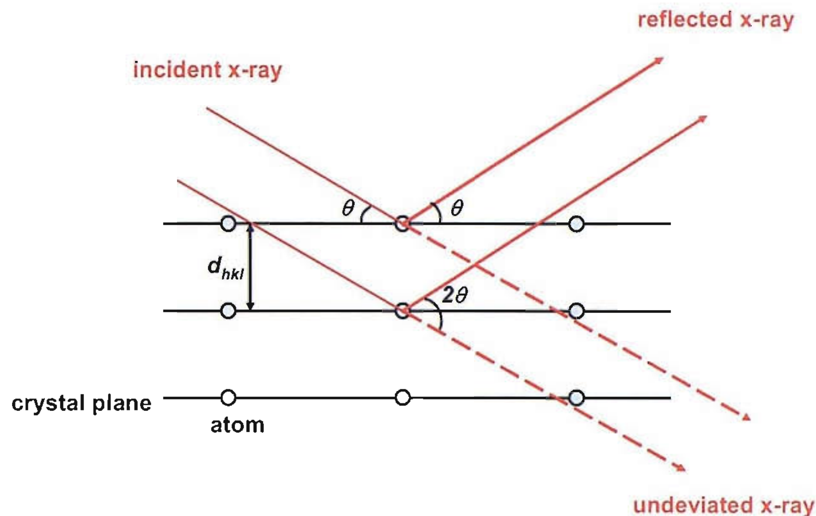

Figure 6.6: Schematic of x-ray diffraction on a crystal solid. The atoms and crystal plane of the crystal solid are represented by blue dots and black line, respectively. Figure based upon ref [132].

Figure 6.6 illustrates the x-ray diffraction from a two dimensional crystal structure. When the x-ray interacts with the atoms on a crystal plane, the x-ray will be reflected away. At a specific angle θ, the reflected rays will form a diffracted beam if the rays differ in phase by a whole number of wavelengths. Those reflected rays will reinforce each other and produce a maxima on the diffraction pattern. For diffraction to occur, the relationship between the interplanar spacing d_{hkl} and the x-ray diffraction angle θ can be expressed by Bragg's Law [131, 132]:

$$n\lambda = 2d_{hkl}sin\theta \tag{6.1}$$

where λ is the wavelength of the x-ray, which is 1.54 $\mathring{A}$ for a copper source, and n is 1,2,3, etc. From the x-ray diffraction angle, the interplanar spacing d_{hkl} of the unknown crystal solid can be determined. If the crystal solid is known, d_{hkl} can be determined from the lattice constant and the Miller indices of different crystal planes, as shown in Table 6.1. The diffraction angle θ can be calculated using Equation 6.1. The diffraction pattern can then be used to determine the crystal phase of the solid by matching the calculated diffraction angle θ with those of the peaks on the diffraction pattern. It should be noted that the peaks on the diffraction pattern will occur at an angle twice that of the diffraction angle. This is because the reflected x-rays will be at an angle of 2θ from the incident x-rays, as shown in Figure 6.5.

Table 6.1: The values of interplanar spacing d_{hkl} in some common crystal systems [132], a and c are the lattice constant of a crystal, h, k, l are the Miller indices of the crystal plane.

Crystal systems	d_{hkl} [$\AA$]
cubic	$[\frac{1}{a^2}(h^2+k^2+l^2)]^{-1/2}$
tetragonal	$[\frac{h^2+k^2}{a^2}+\frac{l^2}{c^2}]^{-1/2}$
hexagonal, hexagonal indexing	$[\frac{4}{3a^2}(h^2+hk+k^2)+\frac{l^2}{c^2})]^{-1/2}$

The full width half maximum (FWHM) of a XRD diffraction peak can be used to determine the grain size D of a crystalline material. Figure 6.7 shows the determination of the FWHM from a XRD diffraction peak. The grain size G of the material can be calculated from Debye-Scherrer's formula [131]

$$G = \frac{0.94\lambda}{\beta cos\theta} \tag{6.2}$$

where λ is the wavelength of the x-ray, β is the FWHM of the diffraction peak expressed in radian, and θ is the diffraction angle.

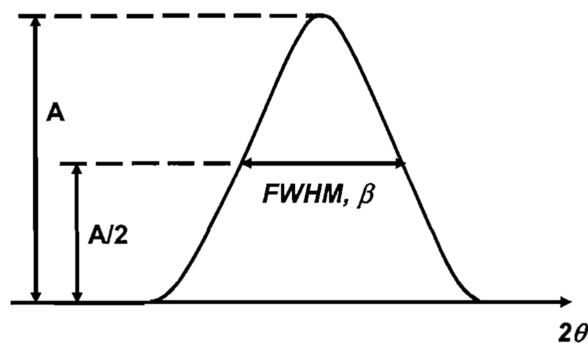

Figure 6.7: Illustration of the FWHM β of a x-ray diffraction peak with intensity A.

6.3 Electrical Characterisation

The I-V characteristics of the TiO_2 layers grown from 7 and 10 nm Ti thin films at 550° C are shown in Figure 6.8. It is noted that the leakage current through the TiO_2 layer decreases strongly as the oxide thickness increases. This is expected as most of the current transport mechanisms are exponentially dependent on the thickness of the sample [4]. The difference in the leakage current is more prominent at negative substrate bias than that at positive substrate bias. This is due to the depletion region created in the *p*-type substrate at negative substrate bias.

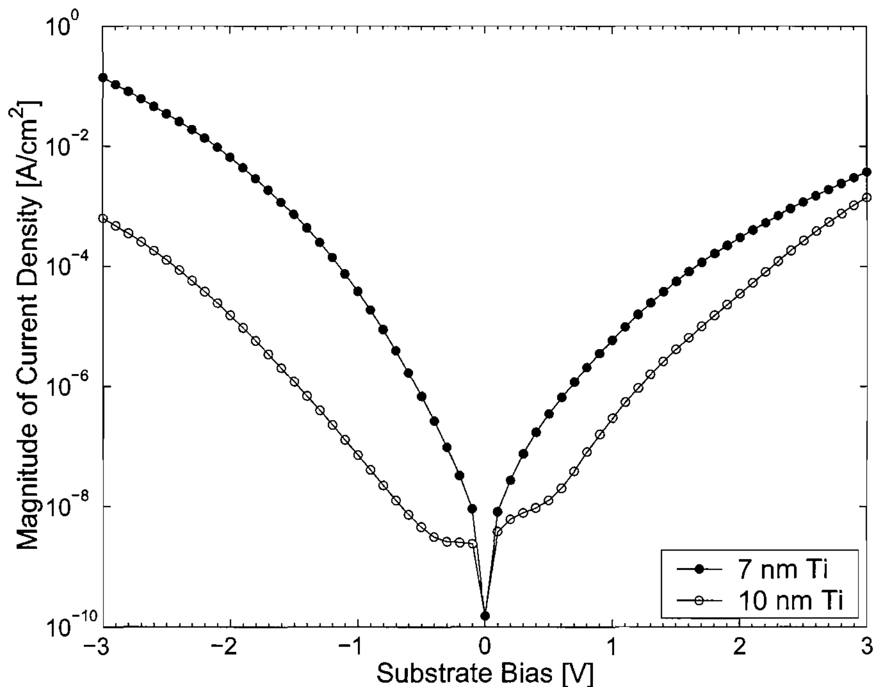

Figure 6.8: Comparison of I-V characteristics of the TiO_2 layers grown from 7 and 10 nm Ti thin films at 550° C.

The results of C-V measurements are shown in Figures 6.9. The maximum capacitance C_{ox} and minimum capacitance C_{min} of the samples are summarized in Table 6.2. C_{ox} decreases as the oxide thickness increases. This is expected because the capacitance is inversely proportional to the oxide thickness. It is noted that the C-V characteristics of the oxide layers show a 'bump' feature around zero bias, which has been discussed in Section 5.4.5. The 'bump' is more significant in the 13 nm TiO_2 layer than the 18 nm TiO_2 layer, which indicates higher surface states density in 13 nm TiO_2 sample [118]. There is also oscillation in the C-V characteristic of the 13 nm TiO_2 layer at the inversion region. This could be due to a poor interface quality and a strong influence of the surface states on the oxide electrical

properties. The structural characterisations of these two samples will be presented in the next section.

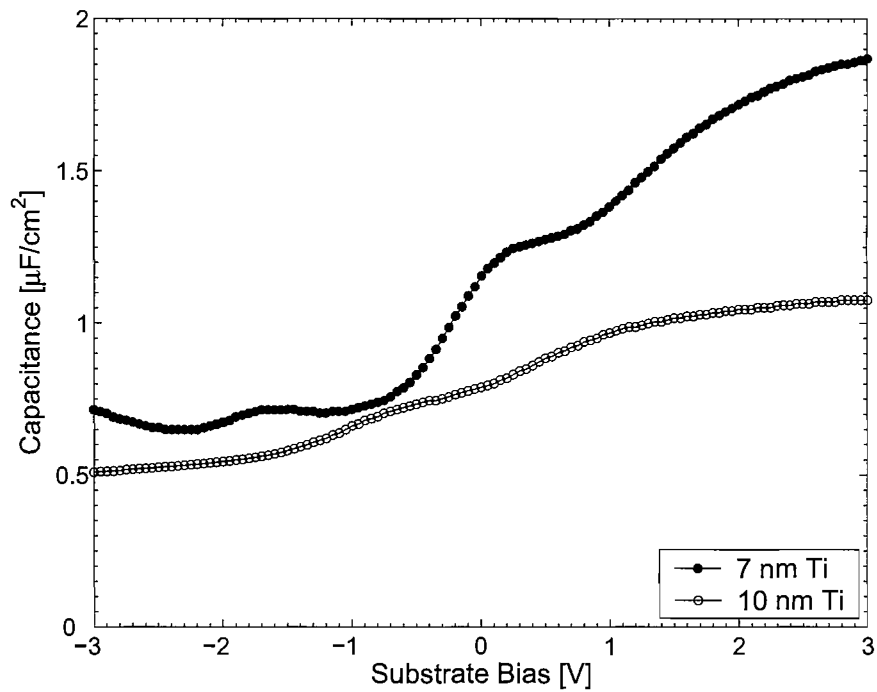

Figure 6.9: Comparison of C-V characteristics of the TiO_2 layers grown from 7 and 10 nm Ti thin films at 550° C.

Table 6.2: The maximum capacitance C_{ox} and the minimum capacitance C_{min} of the samples grown from the Ti thin films of different thicknesses.

TiO_2 thickness [nm]	C_{acc} [$\times 10^{-6}$ F/cm^2]	C_{min} [$\times 10^{-7}$ F/cm^2]
13	1.88	6.49
18	1.09	4.95

6.4 Structural Characterisation

6.4.1 SEM Analysis

Figure 6.10 show the cross-sectional SEM picture of the oxide layer grown from a 7 and 10 nm Ti film at 550 °C, respectively. It is observed that the thickness of the oxide layer is about 12 nm for a 7 nm Ti thin film and 19 nm for a 10 nm Ti thin film. This agrees well with the expected thickness-expansion factor of 1.8 when Ti is fully oxidized to TiO_2, as shown in Table 6.3. Therefore, the nominal thickness will be used for the thermally grown TiO_2 layer, i.e. 13 and 18 nm of TiO_2 layers can be grown from 7 and 10 nm of Ti thin films.

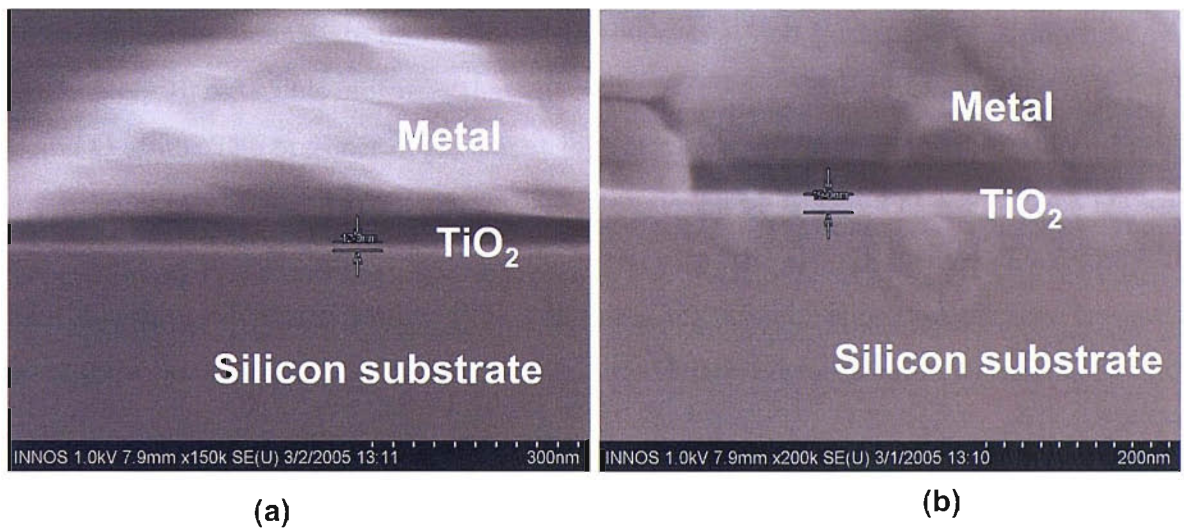

Figure 6.10: Cross-sectional field emission of SEM micrograph of the oxide grown from (a) 7 nm and (b) 10 nm Ti layer. The oxide layer appears as a bright band in the diagram.

Table 6.3: The comparison of the TiO_2 thicknesses grown from 7 and 10 nm Ti thin films. It is shown that TiO_2 thicknesses determined from the SEM micrograph match well to that determine from Table 5.2. A rutile TiO_2 is assumed to calculate the expected TiO_2 thickness from Table 5.2.

Ti thickness [nm]	TiO_2 thickness [nm] (from SEM)	TiO_2 thickness [nm] (from Table 5.2)
7	12	13
10	19	18

6.4.2 TOF-SIMS Analysis

Figure 6.11 shows the SIMS profile of the sample grown from a 7 nm thick Ti film. It is observed that the TiO_2 signal decays slowly from the surface and falls sharply after 10 nm and is only detected for depths < 12 nm. This value provides a good estimate for the oxide thickness and agrees with the nominal thickness of TiO_2 and the SEM picture. The Ti signal from the oxide region exhibits a long tail that extends into the Si substrate. This could be due to diffusion of Ti atoms into the Si as diffusivity of Ti in Si is $1.45\times10^{-2}\exp(-1.79\ eV/kT)$ cm^2s^{-1}, which is about one order of magnitude higher than that of O in Si [133] . Furthermore an increase of the CsTi ion formation efficiency in the Si compared to the TiO_2 matrix cannot be excluded [134]. Notably, SiO_2 and titanium silicate ($TiSiO_3$) signals are also detected in this region and both peak at a depth of approximately 10 nm. This indicates that the interfacial layer formed by reactions among Ti, Si and O atoms.The presence of oxygen at high temperature leads to the formation of SiO_2 and titanium silicate at the interface. The peak of the SiO_2 signal at the surface is most likely due to a polysiloxane (PDMS) contamination of the sample surface. Therefore, the SIMS depth profile of the sample grown from a 7 nm Ti thin film confirms that the total oxide thickness is about 12 nm and there is an interfacial layer of 4 nm titanium silicate.

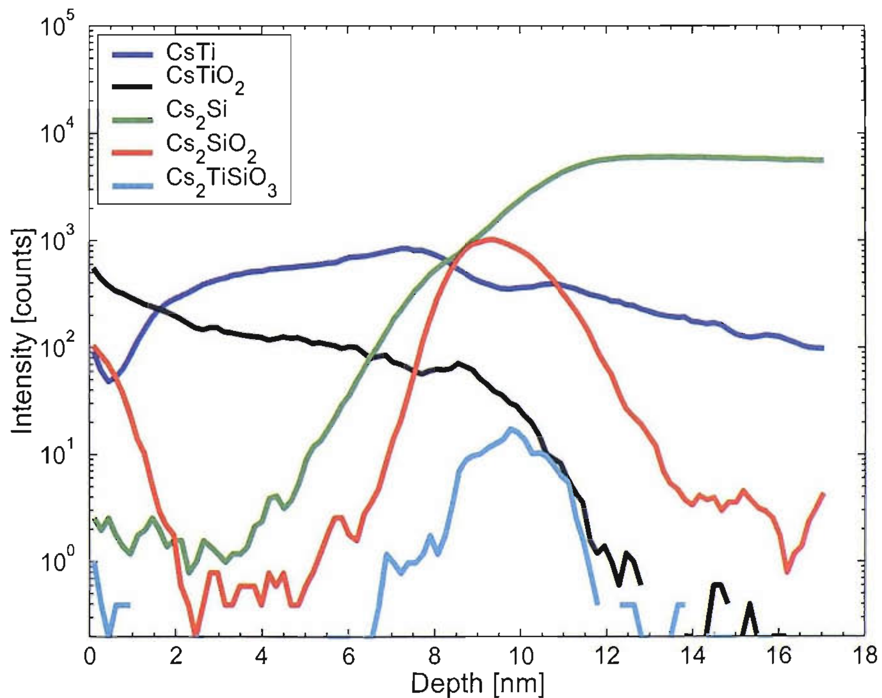

Figure 6.11: TOF-SIMS data of the oxide grown by thermal oxidation of 7 nm Ti layer at 550 °C.

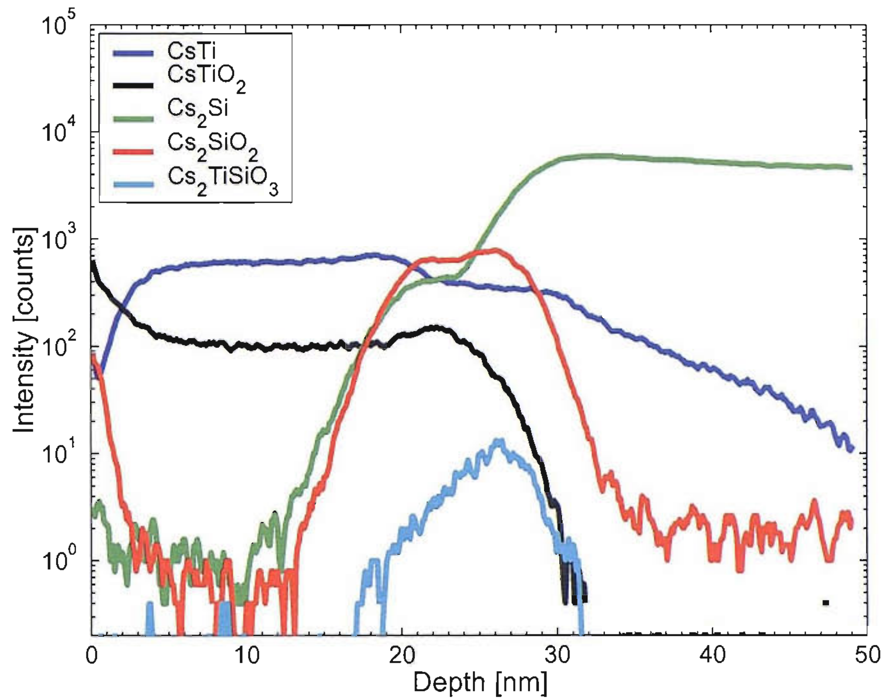

Figure 6.12: TOF-SIMS data of the oxide grown by thermal oxidation of 10 nm Ti layer at 550 °C.

The SIMS profile of the sample grown from a 10 nm Ti thin film is illustrated in Figure 6.12. It is observed that the signals show similar pattern to those in Figure 6.11. The TiO_2 signal decays sharply after 25 nm and is not detectable for depths $>$ 30 nm. This value is not in agreement with the nominal thickness or the oxide layer thickness observed in the SEM micrograph shown in Figure 6.10(b). The discrepancy is likely to be due to the assumption of constant sputtering rate used in determination of the crater depth. The assumption of constant sputtering rate is acceptable for the oxide layer because of the small variation in the chemical compositions in the oxide layer. Hence, this assumption can be used for the SIMS analysis of the oxide grown from a 7 nm Ti thin film because the sputtering process stops after the TiO_2 signal disappeared. However, for the SIMS analysis of the oxide grown from a 10 nm Ti thin film, the sputtering process continued even after the TiO_2 signal had disappeared. The sputtering yield of Si is higher than that of the TiO_2 [135] and hence the constant sputtering rate assumption is not valid for the depth scale. A more precise depth scale can be done by performing the sputtering rate on a reference materials (TiO_2 and Si). Therefore, the SIMS profile in Figure 6.12 cannot be used to determine the oxide thickness. However, it shows the evidence of the TiO_2 layer and the interfacial layer grown from the 10 nm Ti thin film.

6.4.3 XRD Analysis

In the XRD analysis, the diffraction peaks over a range of 2θ values were studied. The occurrence of the diffraction peaks depends on the crystal system and the crystal structure of the material. Table 6.4 lists out the crystal systems and respective lattice constants of Si, Ti and TiO_2. This can be used to determine the occurrence of the diffraction peaks of each material with the formulae in Table 6.1.

Table 6.4: The crystal systems and lattice constants (a, b, c) of Si [42], Ti [101] and TiO_2 [70].

	Crystal system	a [Å]	b [Å]	c [Å]
Si	cubic	5.43	5.43	5.43
Ti	hexagonal	2.95	2.95	4.69
TiO_2 (rutile)	tetragonal	4.58	4.58	2.95
TiO_2 (anatase)	tetragonal	3.73	3.73	9.37

Figure 6.13 shows the XRD result of a 500 nm Ti film oxidized at 550 °C for 2 hours. It can be seen that there is one significant diffraction peak at 69.2 °, which is due to Si(004). Another diffraction peak with relatively small intensity is observed at 32.9 °, which is due to Si(002). Although Si(002) is forbidden due to the vanishing structure factor in the diamond structure [131, 136], multiple diffractions of the beam in the crystal structure could result in the final diffracted beam appears to correspond to a forbidden reflection [137]. It is noted that there is a diffraction peak with very small intensity, which is due to the non-oxidized Ti atoms. It is observed that the diffraction from Ti in the sample is relatively weak compared to those from the Si substrate. This is due to the Ti thickness, which is much thinner compare with that of the Si substrate, as the diffracted beam will be weak if the specimen thickness is thin [131].

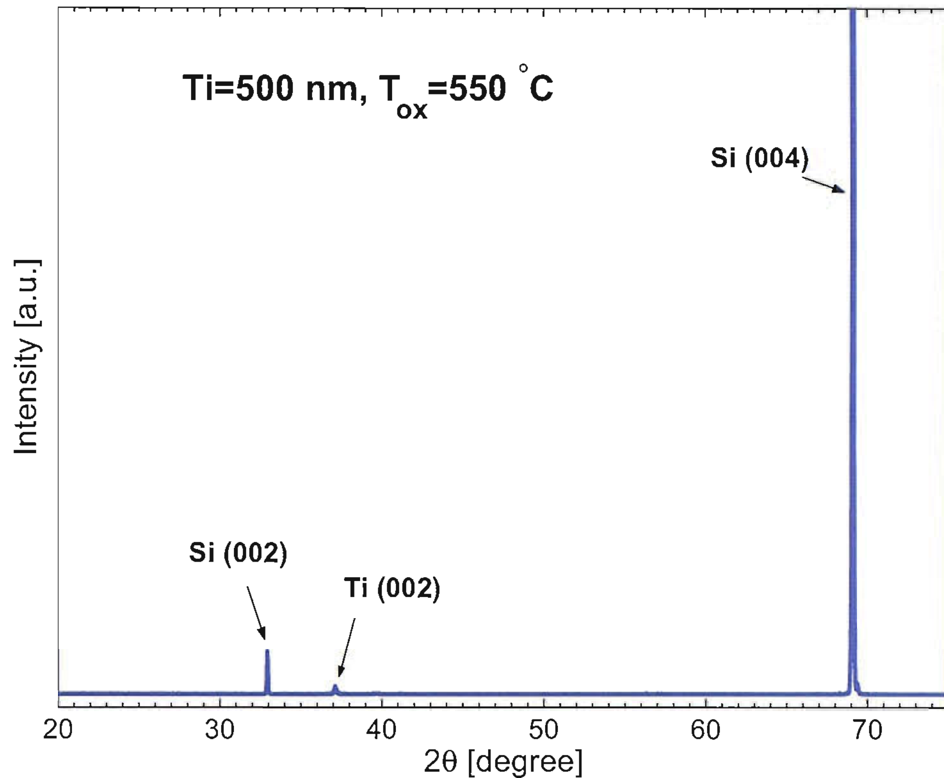

Figure 6.13: The XRD result for sample with 500 nm Ti thin film and oxidized at 550 °C.

The effect of the Ti thin film thicknesses and the oxidation temperatures on the crystal structure of the thermally grown oxide layer are shown in Figure 6.14. The diffraction peaks related to the oxide layers are observed between 35 and 45 °. It is noted that there is no diffraction peak for samples with 100 nm Ti thin films, regardless of the oxidation temperatures. For samples with 500 nm Ti thin film and oxidized at 550 °C, there is one relatively large diffraction peak at 37.16 ° and a small peak at 39.68 °C. This is due to Ti(002) and Ti(101), which has a peak at 38.37 ° and 40.14 °, respectively. The 2θ values of Ti(002) and Ti(101) were determined using Equation 6.1 and the formulae in Table 6.1. The low angle shift in the values of 2θ is due to the enlargement of the lattice volume via the incorporation of oxygen atoms during the oxidation process [85, 110]. This results in an increase in the lattice constant of the Ti crystal [110]. The interplanar spacing of Ti will increase according to the equation listed in Table 6.1, and hence the diffraction peaks will shift to a lower value of 2θ. The peaks of oxygen-enriched Ti(002) and Ti(101) indicate an incomplete oxidation in the 500 nm Ti thin film at 550 °C. As no diffraction peaks are observed in the layer oxidized from 100 nm Ti thin film at 550 °C, it is suggested that the oxide layer is fully oxidized and is amorphous.

For samples with 500 nm Ti thin film and oxidation temperature of 750 °C, the diffraction peak of Ti(002) and Ti(101) have disappeared. This implies that the Ti thin film is fully oxidized. Furthermore, a relatively small peak appears at 43.34 °. This is due to rutile crystal R(210), which has a diffraction peak at 2θ=44.12. The low angle shift is likely due to the insufficient oxidation time for the complete transformation from amorphous to rutile phase [125, 138]. In addition, the weak intensity of the R(210) peak indicates that the oxide layer is still largely amorphous. This is in agreement with the literature, as thermally oxidized Ti will only be transformed to rutile phase at longer oxidation time or at higher oxidation temperature [85]. It is noted that R(210) peak is not observed at sample with 100 nm Ti thin films and oxidized at 750 °C. This could be due to a thinner oxide layer formed by the 100 nm Ti thin film, which make the weak R(210) signal even difficult to be detected.

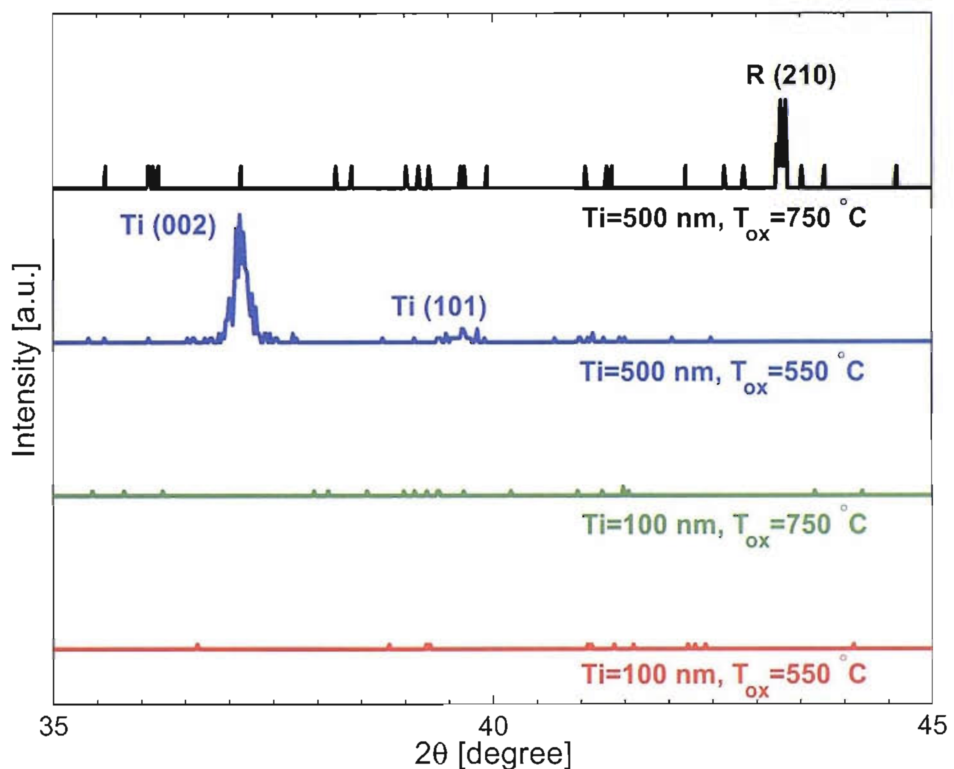

Figure 6.14: The comparison of the XRD data for samples with different Ti thickness and oxidation temperature T_{ox}.

Figure 6.15 shows the R(210) peak from the sample with 500 nm Ti thin film and oxidized at 750 °C. The FWHM of the R(210) peak is 0.11°. The R(210) peak occurs at 2θ=43.3°, hence, the diffraction angle θ is 21.7°. Using Equation 6.2, the grain size G of the oxide layer is determined to be 81.2 nm. It is reported that Ti thin films oxidized at 700 and 800 °C will result in TiO_2 layers with grain size of about 58 and 100 nm, respectively [85]. Hence, for Ti thin film oxidized at 750 °C, a TiO_2 grain size of 81.2 nm is reasonable.

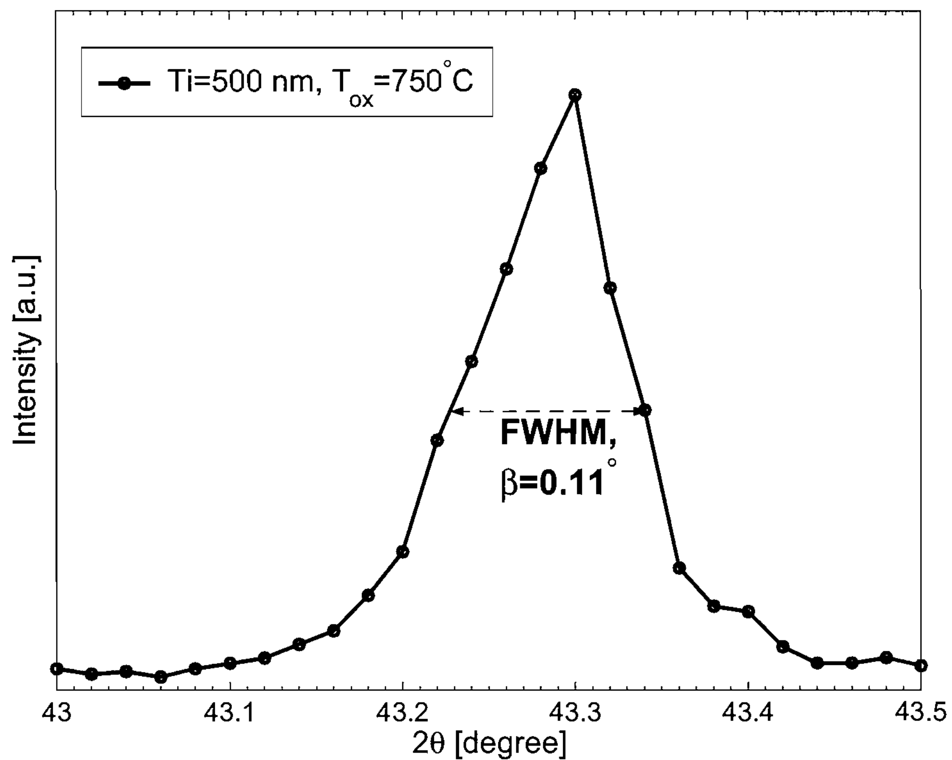

Figure 6.15: The FWHM β of diffraction peak R(210) of sample with 500 nm Ti thin film and oxidation temperature at 750 °C.

XRD on the 13 and 18 nm TiO_2 layers, which were oxidized at 550 °C for 30 mins, show no diffraction peak. One possible explanation is that the oxide layers are too thin for diffraction peak of strong intensity to be observed. However, as the XRD results show that thicker thermally oxidized Ti layers grown at 550 °C are amorphous, it is believed that thinner oxide layers oxidized at the same temperature but shorter oxidation time are amorphous as well.

6.5 Conclusion

Structural and electrical properties of the TiO_2 layers grown from 7 and 10 nm Ti thin films were studied. SEM pictures show that 13 and 18 nm TiO_2 layers can be grown from 7 and 10 nm Ti thin films, respectively. TOF-SIMS was used to perform elemental analysis of the thermally grown TiO_2 layers. It has been shown that Ti atoms will diffuse into Si substrate during the oxidation process. Also, an interfacial layer consist of Ti, Si, and O atoms is observed in the SIMS depth profile. X-ray diffraction was used to identify the crystal phase of thermally oxidized TiO_2 layers. The results show incomplete oxidation in the oxide layers grown from 500 nm Ti thin films with oxidation temperature at 550 °C. However, a weak rutile phase signal, R(210), was detected in the layers oxidized at 750 °C. This suggest that crystallization of thermally grown TiO_2 layers occurs at higher oxidation temperatures. In addition, there is no diffraction peaks on the XRD results of TiO_2 layers grown from 100 nm Ti thin films with oxidation temperature at 550 °C, which indicates that the TiO_2 layers grown at those conditions are amorphous. Therefore, it is believed that TiO_2 layers grown at 550 °C and with Ti thin film thickness thinner than 100 nm are amorphous also.

The I-V characteristics of the TiO_2 layers has shown that the leakage current through the oxide layer decreases as the oxide thickness increases. Comparison of the C-V characteristics of the TiO_2 layers indicates that the surface states have greater influence on thinner oxide. To minimize the influence of surface states on the electrical properties, TiO_2 layers grown from 10 nm of Ti thin films were used to study the electrical properties of the TiO_2 layers with different Si substrates and top metal electrodes.

Chapter 7

Current Transport Mechanism in Thermally Grown TiO_2

7.1 Introduction

One of the main advantages of VMISTT is the possibility of complementary operation as in CMOS. As mentioned in Chapter 4, to realise complementary operation, the choice of Si source and metal drain for VMISTT is important. The Si source will supply the charge carriers for conduction current. The requirement for the metal drain is such that it has a work function which suppresses the F-N tunneling of the electrons from the metal. For an n-VMISTT, the electron is the charge carrier. Thus, n-Si is chosen for F-N tunneling of electron to occur at the applied gate and drain bias. It is essential to have a low work function metal drain to suppress hole tunneling from the metal to the Si substrate. Therefore, Al with a work function of 4.2 eV [4], is chosen as the metal drain for the n-VMISTT. On the other hand, for p-VMISTT, the hole is the charge carrier. Therefore, p-Si should be used to supply holes for the F-N tunneling at the applied biases. A high work function metal drain is required to suppress the electron F-N tunneling from the metal to the Si substrate. Thus, Pt with a work function of 5.6 eV [4], is chosen as the metal drain for the p-VMISTT.

The MOS capacitor is used to characterise the tunnel barrier because a non-gated VMISTT is essentially a MOS capacitor. By choosing the appropriate Si substrate and the top metal electrode for the MOS capacitors, the current transport mechanism in the oxide layer can be studied. The observation of F-N tunneling through the oxide layer is important, as this

will allow the F-N tunneling current to be modulated by the gate bias in the VMISTT operation.

TiO_2 MOS capacitors with two kinds of top electrode (Al, Pt) and two Si substrate (n-type, p-type) were fabricated to characterise the TiO_2 layers through electrical measurements. The TiO_2 layers were grown from 10 nm Ti thin films at 550 °C. There are four types of different MOS capacitor structures: Al/TiO_2/n-Si, Al/TiO_2/p-Si, Pt/TiO_2/n-Si, and Pt/TiO_2/p-Si. This is to study the effect of the Si substrates and top metal electrodes on TiO_2 layers.

7.2 Current Transport Mechanisms in Tunnel Barrier

An ideal tunnel barrier for the VMISTT will exhibit F-N tunneling as the dominant current transport mechanism for the entire temperature range. This will not be the case for a real tunnel barrier, as there are other mechanisms which will be dominant at various temperatures and bias conditions. To design and fabricate a good tunnel barrier, it is important to understand the nature of these mechanisms so that the related leakage current can be suppressed. The following discussion is using the electron as the charge carrier. Similar arguments apply to holes.

(a) Fowler-Nordheim Tunneling

Fowler-Nordheim (F-N) tunneling is the field emission of electrons from a metal or semiconductor surface into the conduction band of an insulator through a triangular barrier, as illustrated in Figure 7.1. It occurs under the influence of a strong electric field. The current voltage (I-V) relationship of F-N tunneling can be expressed as [58–60]

$$J = A_{FN} V^2 exp\left(-\frac{B_{FN}}{V}\right) \tag{7.1}$$

where J is the current density, and A_{FN} and B_{FN} are constants, which can be expressed as

$$A_{FN} = \frac{q^3}{8\pi h m^*(q\Phi_B)} \tag{7.2}$$

$$B_{FN} = \frac{8\pi\sqrt{2m^*m_0}(q\Phi_B)^{3/2}d_{ox}}{3qh} \quad (7.3)$$

m* is the tunneling effective mass of the charge carrier in the tunnel barrier, m_0 is the free electron rest mass, d_{ox} is the thickness of the tunnel barrier, q is the electronic charge and h is Planck's constant. If the dominant current transport mechanism is F-N tunneling, then, the graph of $ln(J/V^2)$ versus $1/V$ will show a linear line of slope $-B_{FN}$. From the slope, the barrier height $q\Phi_B$ in eV can be determined,

$$q\Phi_B = 0.2778 \times \left(\frac{B_{FN}^2}{m^*d_{ox}^2}\right)^{1/3} \quad (7.4)$$

where d_{ox} is measured in nm.

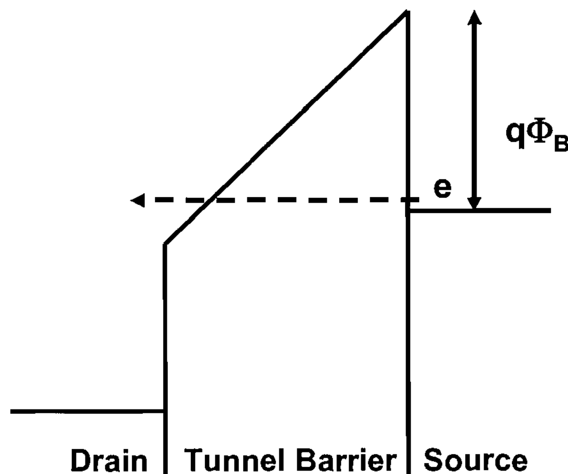

Figure 7.1: Band diagram of the drain/tunnel barrier/source structure showing F-N tunneling.

Theoretically, F-N tunneling is independent of the temperature. However, the number of electrons of a given energy incident on the barrier is temperature dependent, and the oxide/Si barrier height Φ_B is also temperature dependent [59, 139, 140]. These will results in small variation of tunneling current magnitude with temperature.

(b) Trap-assisted Tunneling

When there are traps or defects in the oxide, trap-assisted tunneling could occur through the traps [141, 142]. As shown in Figure 7.2, trap-assisted tunneling is a two step tunneling process: first, the electron from the source will tunnel into the traps, then, it will tunnel to the conduction band of the oxide. The I-V relationship for trap-assisted tunneling is quite similar to F-N tunneling except for the V^2 pre-factor, and is given by [141]

$$J = A_{TAT}exp\left(-\frac{4\sqrt{2m^*m_0}(q\Phi_T)^{3/2}d_{ox}}{3q\hbar V}\right) \tag{7.5}$$

where A_{TAT} is a constant, which can be expressed as

$$A_{TAT} = \frac{q^3}{8\pi hm^*(q\Phi_B)} \tag{7.6}$$

The traps energy level, $q\Phi_T$ in eV, can be determined from the slope B_{TAT} of the linear lnJ versus $1/V$:

$$q\Phi_T = 0.2778 \times \left(\frac{B_{TAT}^2}{m^*d_{ox}^2}\right)^{1/3} \tag{7.7}$$

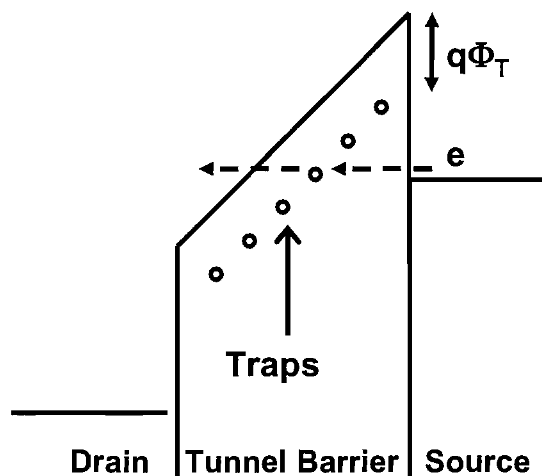

Figure 7.2: Band diagram of the drain/tunnel barrier/source structure showing the trap assisted tunneling.

(c) Schottky Emission

At high temperatures, thermionic emission of electrons from the source into the conduction band of oxide is expected to be the dominant carrier transport mechanism [4, 68, 69]. This is also known as Schottky emission, which is illustrated in Figure 7.3. The I-V expression of Schottky emission is as followed [4]:

$$J = A_{SC}T^2 exp\left[-\frac{q}{kT}\left(\Phi_B - \sqrt{\frac{qV}{4\pi\epsilon_r\epsilon_0 d_{ox}}}\right)\right] \tag{7.8}$$

where A_{sc} is the effective Richardson constant, T is the temperature and k is the Boltzman's constant. From the expression, it is seen that the Schottky current increases exponentially with an increase in temperature.

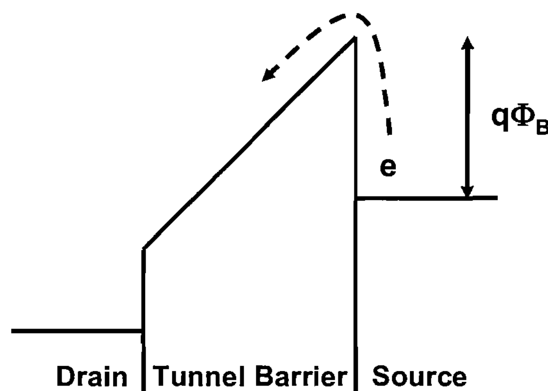

Figure 7.3: Band diagram of the drain/tunnel barrier/source structure showing Schottky emission.

At a given temperature, a linear lnJ versus $\sqrt{V}$ plot will indicate the possibility of the presence of Schottky emission. The slope of the linear portion in the plot, B_{SC}, can be used to determine the dielectric constant ϵ_r of the oxide provided the thickness of the oxide d_{ox} is known, or vice versa:

$$B_{SC} = \frac{q}{kT}\sqrt{\frac{q}{4\pi\epsilon_r\epsilon_0 d_{ox}}} \tag{7.9}$$

It is important to check if ϵ_r falls within the reported values. If that is true, then, Schottky emission is the dominant current transport mechanism in that voltage range [72]. If not, the current is due to some other mechanisms. On the other hand, at constant applied bias, the Schottky barrier height $q\Phi_B$ in eV can be extracted from the slope β_{SC} of the $ln(J/T^2)$ versus $1/T$ straight line plot using

$$q\Phi_B = -8.617 \times 10^{-5}\beta_{SC} \tag{7.10}$$

The $\sqrt{qV/(4\pi\epsilon_r\epsilon_0 d_{ox})}$ term in Equation 7.8 is due to the image-force-induced lowering effect [4], it is visualised as $\Delta\phi$ in Figure 7.4. When an electron is at a distance x from the source, a positive charge will be induced on the surface of the source. This is known as the image charge. The attractive force F between these two charges is called the image force, it is equivalent to the force between the electron and an equal positive image charge located at $-x$:

$$F = \frac{-q^2}{4\pi\epsilon_{ox}(2x)^2} = \frac{-q^2}{16\pi\epsilon_{ox}x^2} \tag{7.11}$$

The total potential energy of the electron with an applied electric field E is given by

$$P_{total}(x) = P_E(x) + P_e(x) \tag{7.12}$$

where $P_E(x) = qEx$ is the potential energy due to the applied electric field at a distance x from the metal surface. P_e is the potential energy of the electron and is equal to the work done on the electron by moving it from infinity to the point x:

$$P_e(x) = \int_{\infty}^{x} F dx = \frac{q^2}{16\pi\epsilon_{ox}x} \tag{7.13}$$

The maximum potential occurs when $d[P_{total}(x)]/dx = 0$. Therefore, the location of the top of the barrier x_m and the image-force-induced lowering $\Delta\phi$ can be determined:

$$x_m = \sqrt{\frac{q}{16\pi\epsilon_{ox}E}} \tag{7.14}$$

$$\Delta\phi = \sqrt{\frac{qE}{4\pi\epsilon_{ox}}} = \sqrt{\frac{qV}{4\pi\epsilon_r\epsilon_0 d_{ox}}} \tag{7.15}$$

The carriers in the source will see a lower barrier $(\Phi_B - \Delta\phi)$.

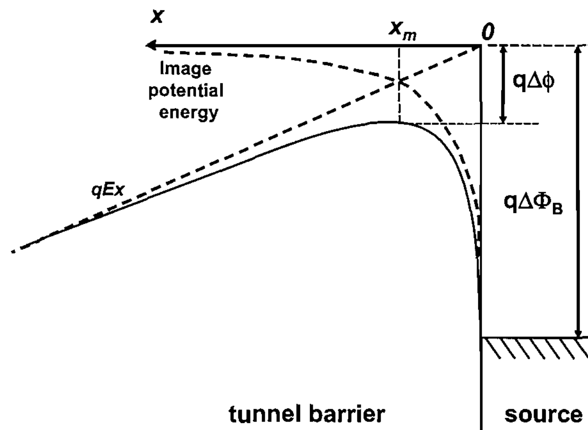

Figure 7.4: Band diagram between the source and tunnel barrier, showing the image barrier lowering effect. Figure based upon ref [4].

(d) Poole-Frenkel Emission

When there are traps in the bulk of the oxide, the Poole-Frenkel (P-F) effect may be significant [4, 68, 69, 143, 144]. It is very similar to Schottky emission, except that it is the field dependent thermionic emission from the traps instead of the source, as shown in Figure 7.5. It can be expressed as [4, 144]

$$J = A_{PF} V exp\left[-\frac{q}{kT}\left(\Phi_T - \sqrt{\frac{qV}{\pi\epsilon_r\epsilon_0 d_{ox}}}\right)\right] \tag{7.16}$$

and

$$A_{PF} = q\mu n_0 / d_{ox} \tag{7.17}$$

where μ and n_0 are the mobility of the charge carriers and the carrier density, respectively. The image force lowering term $\sqrt{qV/(\pi\epsilon_r\epsilon_0 d_{ox})}$ is twice that of the Schottky emission because of the immobility of the positive charge associated with the traps [4]. P-F emission is only effective for the traps which are neutral when filled and positively charged when empty. For traps which are neutral when empty and charged when filled, there is no P-F effect due to the lack of Coulomb interaction [145]. The oxide dielectric constant can be determined from the slope B_{PF} of a linear lnJ/V versus $\sqrt{V}$ plot:

$$B_{PF} = \frac{q}{kT}\sqrt{\frac{q}{\pi\epsilon_r\epsilon_0 d_{ox}}} \tag{7.18}$$

Similarly, the value of ϵ_r must fall within reported values for P-F emission to be the dominant mechanism [72].

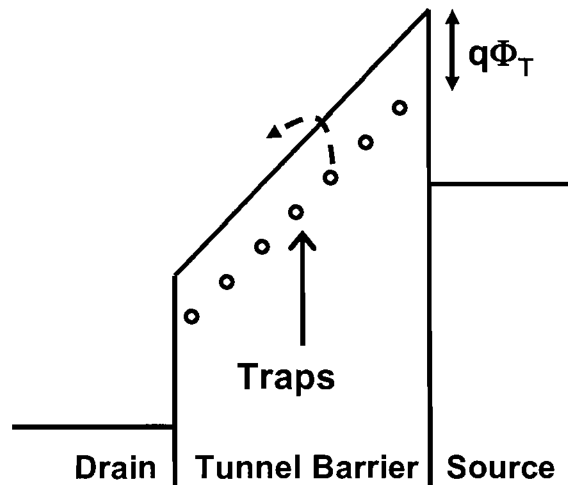

Figure 7.5: Band diagram of the drain/tunnel barrier/source structure showing Poole-Frenkel emission.

(e) Hopping Conduction

At low voltage, current conduction is possible due to the carrier hopping from one trap to another [63]. It is indistinguishable from ohmic conduction as it has a linear I-V characteristic. It can be expressed as [5, 67]:

$$J = \frac{q^2 l^2 n^* \Gamma V}{kT d_{ox}} \tag{7.19}$$

where l is the interval of separation between adjacent hopping sites, n^* is the density of free electrons in the oxide, and Γ is the mean hopping frequency.

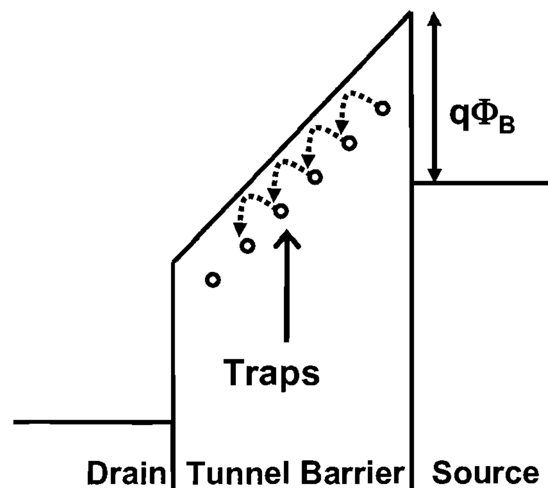

Figure 7.6: Band diagram of the drain/tunnel barrier/source structure showing hopping conduction.

7.3 Experimental details

10 nm Ti thin films were deposited on RCA-cleaned and HF-treated standard 4 inch diameter, low-resistivity (0.02 Ωcm) n-type and p-type Si substrates by vacuum e-beam evaporation without any substrate heating. The oxide was subsequently formed by thermal oxidation at 550 °C for 30 minutes. MOS capacitors were fabricated to characterise the TiO_2 layers. 300 nm Pt and 1000 nm Al top contacts were formed by vacuum evaporation using shadow masks. The back contacts consist of a 1000 nm thick Al layer, which was deposited by vacuum evaporation as well. High doping in Si ensured that the back contacts were ohmic. The process listing is shown in Appendix B.4.

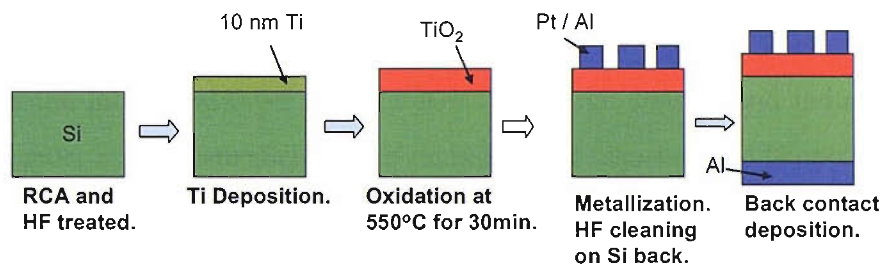

Figure 7.7: Process flow of TiO_2 MOS capacitors.

I-V characteristics were obtained at room temperature and low temperatures using the HP4155A parametric analyser. Low temperature measurements were performed by mounting the samples on a liquid nitrogen cryostat, controlled by a Biorad DL4960 temperature controller. The C-V characterization was done at room temperature at 1 MHz using a HP4280A capacitance meter and HP4192A impedance analyser. The measurement setup was same as that described in Section 5.4.1.

7.4 Results & Discussion

7.4.1 Current-Voltage Analysis

The I-V characteristics of the TiO_2 MOS capacitors are shown in Figure 7.8. It is noted that the leakage current is higher in the capacitors with Al top electrode, regardless of the type of substrate. It has been shown that the choice of the top electrode material can affect I-V and C-V characteristics due to reactivity of the metal with the underlying oxide at the metal/oxide interface [146]. Al is more reactive than Ti as the heat of formation of alumina is higher than that of the titania [147], it tends to react with oxygen of underlying TiO_2 and creates an interfacial layer of oxygen-deficient titanium oxide, which has a lower resistivity and allows more leakage current. This will bring adverse effect on VMISTT operation as the interfacial layer can increase the charge density and induce trap-related current transport mechanism such as P-F emission and trap-assisted tunneling. Therefore, metal with similar work function as Al but less reactive must be considered for the drain electrode of n-VMISTT.

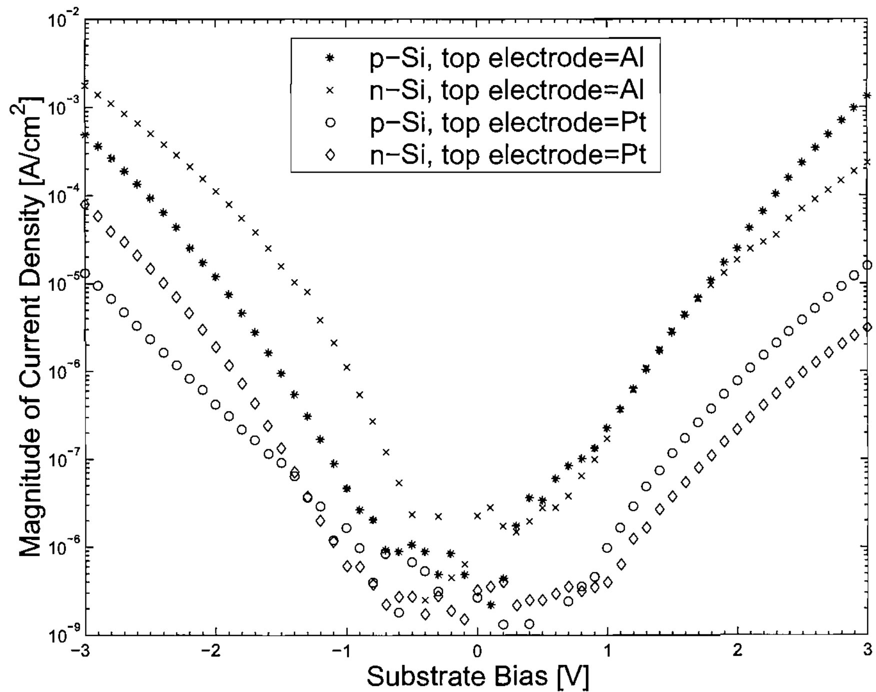

Figure 7.8: The room temperature current voltage characteristics of the 18 nm TiO_2 layers. The capacitors with Al top contact give higher leakage current than those with Pt top contact.

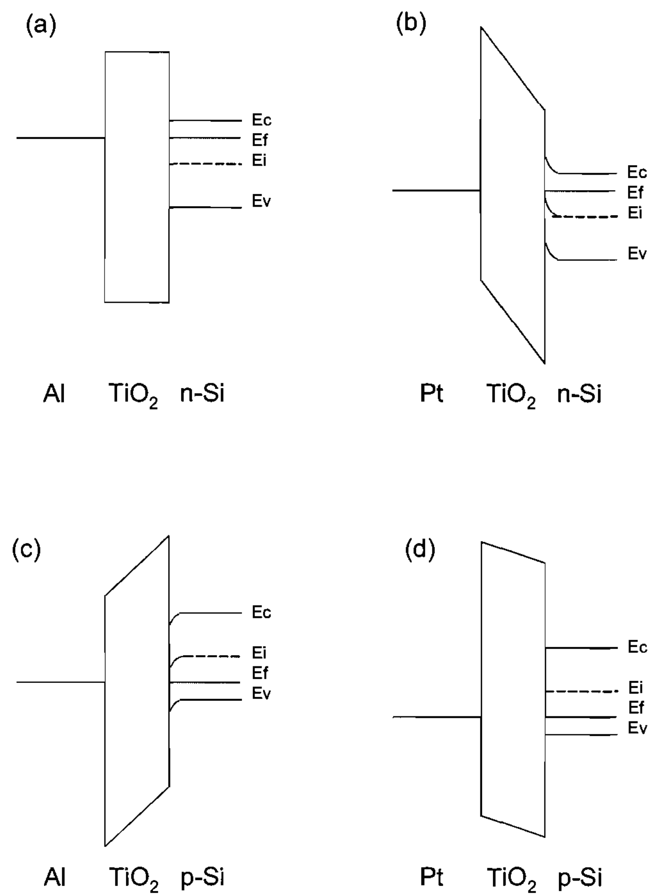

Figure 7.9: The energy band diagram of TiO_2 MOS capacitors with different metal electrodes and Si substrates.

It is interesting to observe in Figure 7.8 that at negative substrate bias, the capacitors with n-Si substrate exhibit higher current density than the capacitors with p-Si substrate. On the other hand, at positive substrate bias, the capacitors with p-Si substrate show higher current density than those with n-Si substrate. This can be explained with the aid of energy band diagram shown in Figure 7.9. At negative substrate bias, the energy level of the Si substrate will increase, and the band diagram will be tilted such that only carriers flow from the substrate is possible. The n-Si substrate will be biased into accumulation mode and the majority carriers (electrons) are responsible for the current flow in the capacitors. For capacitor with p-Si substrate, the substrate will be driven into inversion mode at negative substrate bias. The current is mainly due to the minority carriers (electrons) in the inversion layer. Therefore, for capacitors with the same metal electrode, the one with the n-Si substrate will exhibit higher current density at negative substrate bias than that of the p-Si substrate. This is because the whole n-Si substrate can supply the electrons for conduction at accumulation mode, whilst the electrons in p-Si substrate come only from the

inversion layer through generation and recombination process. At positive substrate bias, there are two possible sources for the current: the electrons in the metal electrode and the holes in Si substrate. For p-Si, the substrate will be in accumulation mode, the current is contributed by the electrons in the metal and the majority carriers in the substrate (holes). For n-Si, holes become the minority carriers as the substrate is driven into inversion mode, and the contribution of the minority carriers could be lower as only the inversion layer can provide the holes for current conduction. Thus, the current density of the capacitors with n-Si is lower than that of the p-Si at positive substrate bias.

7.4.2 Capacitance-Voltage Analysis

The results of C-V measurements are shown in Figure 7.10. Two distinct characteristics are observed. Firstly, the capacitors with Al top electrode have higher accumulation capacitance than the capacitors with Pt top electrode. If the oxide thickness is the same, the accumulation capacitance should be similar regardless of the top electrode. However, as mentioned before, the Al top electrode may react with TiO_2 and reduce the effective oxide thickness. As the capacitance is inversely proportional to the oxide thickness, the accumulation capacitance of the capacitors with Al top electrode will show higher value than those with the Pt top electrode. Secondly, the minimum capacitances C_{min} of the capacitors on n-Si substrate are lower than those on the p-Si. This is due to the fact that for the similar resistivity, the p-Si substrate has a higher doping concentration than the n-Si substrate [4]. As the capacitance due to the depletion region in the silicon substrate C_d is proportional to the square root of the doping density, as shown in Equation 2.6.

Table 7.1 summarizes the maximum capacitance C_{ox}, the minimum capacitance C_{min}, the oxide thickness d_{ox} and the dielectric constant ϵ_r of the capacitors. As there is minimal reaction between the Pt top electrode and the oxide, the dielectric constant is calculated from the accumulation capacitance of the capacitors with Pt top electrode assuming the nominal oxide thickness of 18 nm, as confirmed by SEM. The calculated dielectric constant is then used to calculate the effective thickness of the oxide in the capacitors with Al top electrode, by assuming that the dielectric constant of the thermally grown oxide is similar. This is likely as all the oxides are grown simultaneously under the same conditions. This analysis suggests that the top 3 nm of the TiO_2 layers is depleted in oxygen due to the Al top contact.

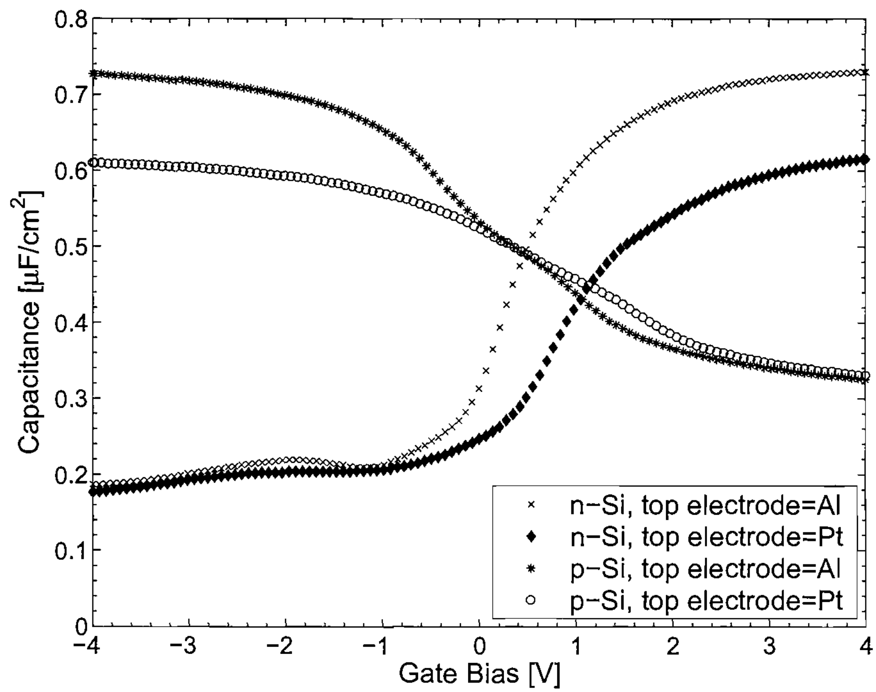

Figure 7.10: The capacitance voltage characteristics of the 18 nm TiO_2 layers at room temperature.The capacitors with Al top contact show higher accumulation capacitance than those with Pt top contact.

Table 7.1: Summary of the C-V analysis of the samples with TiO_2 grown from 10 nm of Ti thin film at 550°C. d_{ox} is fixed for the Pt contacts, while ϵ_r has been fixed to the Pt value for Al.

sample	C_{ox} [$\times$**10**$^{-7}$ **F/cm**^{2}]	C_{min} [$\times$**10**$^{-7}$ **F/cm**^{2}]	d_{ox} **[nm]**	ϵ_r
p-Si, top contact=Pt	6.16	3.31	18.0	12.5
p-Si, top contact=Al	7.30	3.26	15.2	12.5
n-Si, top contact=Pt	6.10	1.78	18.0	12.4
n-Si, top contact=Al	7.27	1.87	15.1	12.4

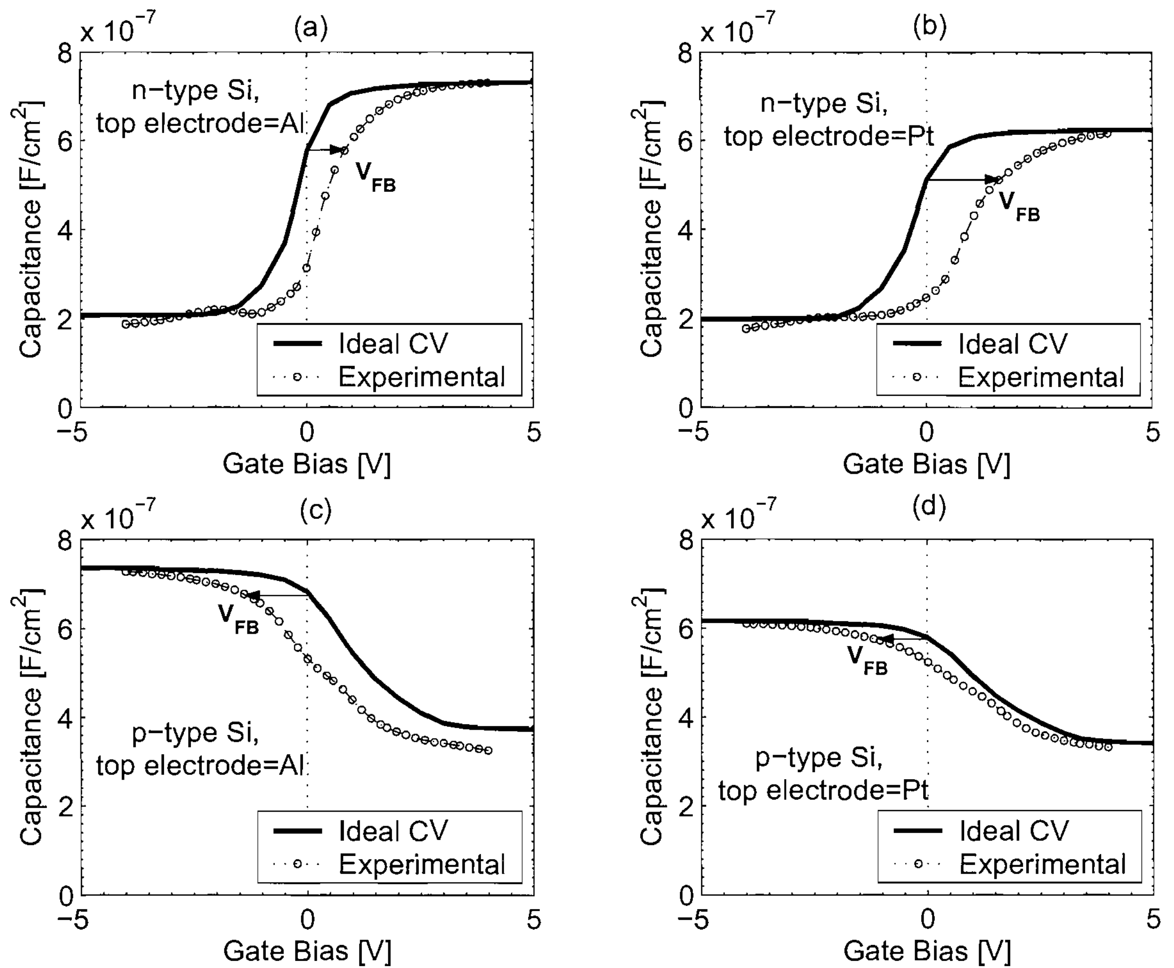

Figure 7.11: The comparison of the ATLAS simulated ideal C-V curve with the measured C-V characteristics of TiO_2 MOS capacitors with different type of Si substrate and top metal electrodes.

As mentioned in Section 2.2.2, by comparing the C-V characteristics of the capacitors with the ideal C-V curves, V_{FB} of the capacitors can be determined. Figure 7.11 shows the comparison of the ideal C-V curves with the experimental C-V characteristics for different type of Si substrates and metal top electrodes. The ideal C-V curves were simulated using ATLAS (see Appendix C.3 for the scripts) by assuming Φ_m equals Φ_s and Q_i is zero. Table 7.2 lists the values of V_{FB}, Φ_m, Φ_s, and Q_i of each samples. The values of V_{FB} are estimated from Figure 7.11. Φ_s of the Si substrates is obtained using Equations 2.9 to 2.12, with $q\chi$=4.17 eV, E_g=1.08 eV, and n_i=1.45 $\times$ 10^{10}cm^{-3}, respectively [148]. For a substrate resistivity of 0.02 Ωcm, N_D and N_A are 10^{18}cm^{-3} and 3 $\times$ 10^{18}cm^{-3}, respectively [4]. With the values of V_{FB}, Φ_m, and Φ_s, Q_i can be calculated from Equation 2.7.

Table 7.2: Summary of the oxide charge density (Q_i) analysis. V_{FB} are estimated from Figure 7.11. The values of Φ_m are based on ref [4]. Φ_s are calculated by using Equations 2.9 to 2.12.

sample	V_{FB} [V]	Φ_m [V]	Φ_s [V]	Q_i [cm^{-2}]
p-Si, top contact=Pt	-1.24	5.6	5.23	6.19×10^{12}
p-Si, top contact=Al	-1.62	4.1	5.23	2.23×10^{12}
n-Si, top contact=Pt	1.62	5.6	4.25	-1.03×10^{12}
n-Si, top contact=Al	0.86	4.1	4.25	-4.58×10^{12}

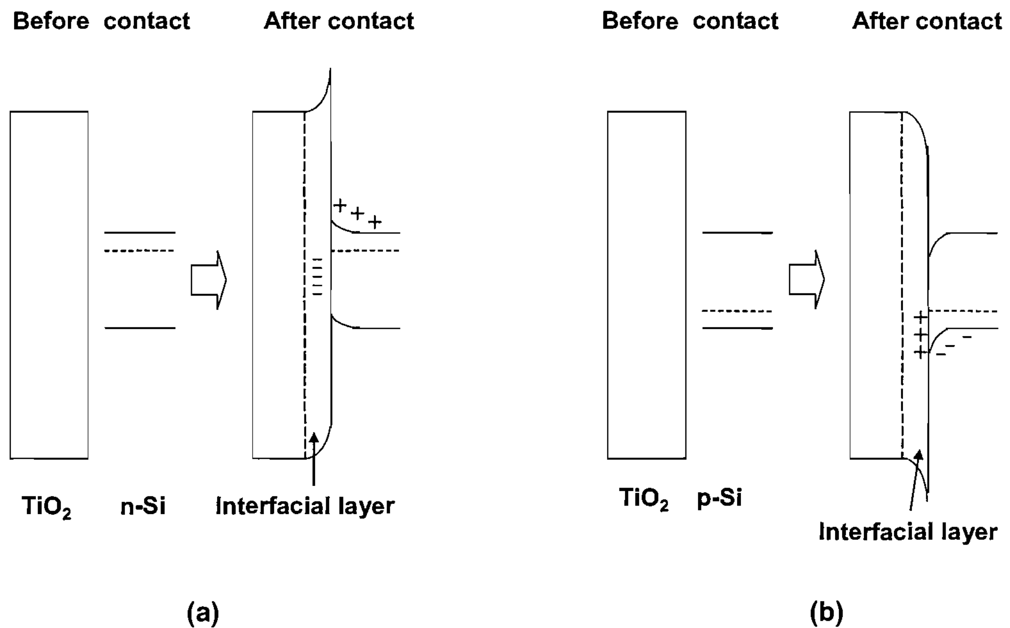

Figure 7.12: The energy band diagram to illustrate the interface charge when TiO_2 layer make contact to (a)n-Si, (b)p-Si.

As shown in Table 7.2, the values of the oxide charge density are all above 10^{12} cm^{-2}. These are similar to the values reported in literature [91, 111]. It is noted that the oxide charge is negative for n-Si and positive for p-Si. This indicates that Fermi-level pinning happens at the interface of the TiO_2 and Si, possibly due to the amphoteric nature of the metal-Si bonds [149, 150]. For n-Si substrate, the electrons will fill-in the unoccupied interface states located below the substrate Fermi level, which results in a net negative charges in the oxide. This is illustrated in Figure 7.12(a). On the other hand, for p-Si substrate, the interface state will act as electron-donor states and transfer the electrons to the substrate. This will results in a net positive charges in the oxide as illustrated in Figure 7.12(b).

7.4.3 Current Transport Mechanism

Owing to the reaction of Al on TiO_2, Pt/TiO_2/p-Si capacitor was chosen for in-depth analysis of the current transport mechanisms in the thermally grown TiO_2 thin films. Due to the large work function of the Pt, the current is expected to consist predominantly of electrons and holes from the Si substrate for negative and positive substrate bias, respectively. Observation of hole F-N tunneling from the Si substrate will be essential for the implementation of the complementary operation of the VMISTT.

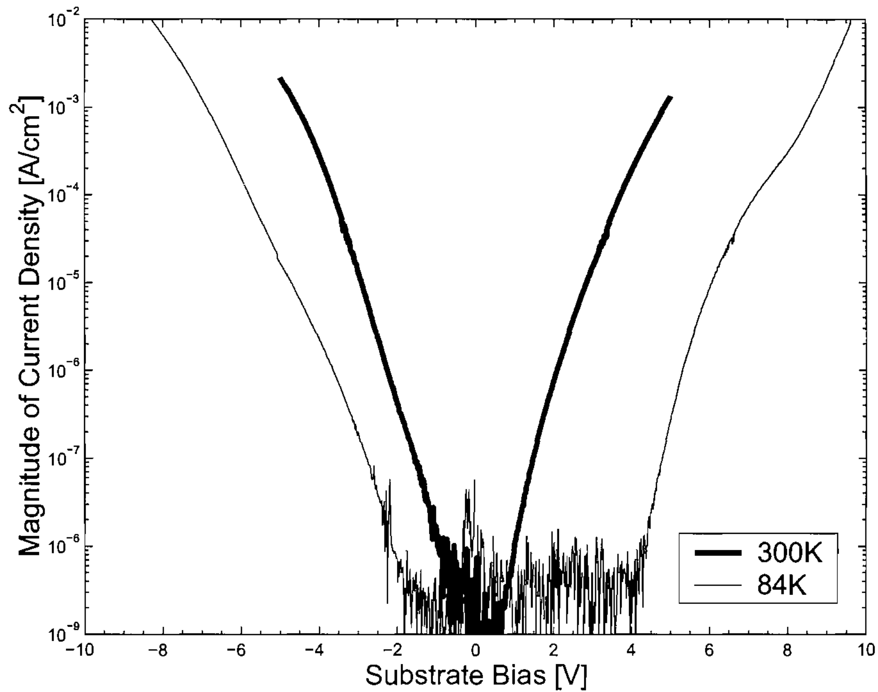

Figure 7.13: The comparison of the I-V characteristics of the 18 nm TiO_2 layers (p-Si and Pt top electrode only) at room temperature and at 84K.

Figure 7.13 compares the I-V characteristics of a Pt/TiO_2/p-Si capacitor at room temperature and at 84 K. It is shown that the current flowing through the device is strongly temperature dependent. As the thermally grown TiO_2 has high interface charge density as shown by C-V analysis, Poole-Frenkel (P-F) emission due to the traps or defects in the oxide is possible. The lnJ/V vs $\sqrt{V}$ P-F plot is shown in Figure 7.14. The slope of the straight line results in a dynamic dielectric constant ϵ_{dyn} of 7.89. As pointed out by O'Dwyer [151], only a self-consistent ϵ_{dyn} can ensure the current conduction is due to P-F emission. ϵ_{dyn} should be greater than the optical dielectric constant ϵ_{opt} and less than the static dielectric constant, ϵ_{static} to be self-consistent [152]. ϵ_{opt} can be determined from the refractive index of TiO_2, η=2.75 [153]. Hence, $\epsilon_{opt} = \eta^2 = 7.56$. ϵ_{static} is obtained from the

C-V measurement, which is 12.5. ϵ_{dyn} is within the expected range and P-F emission is the dominant current transport mechanism at room temperature.

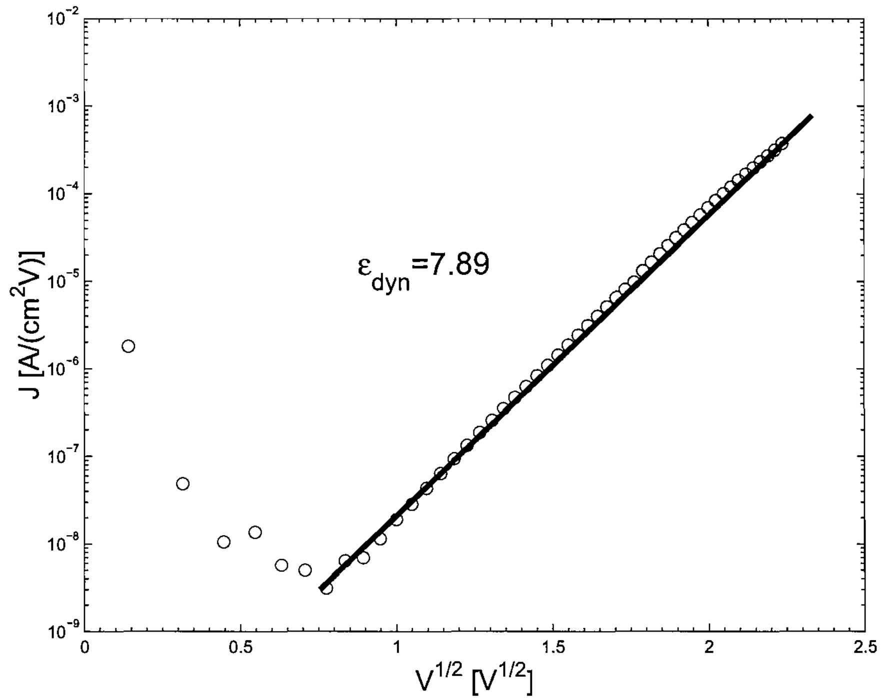

Figure 7.14: The Poole-Frenkel plot of the 18 nm TiO_2 layer at room temperature. The straight line is a fit to Equation 7.16.

At 84 K, the thermal activation mechanisms, such as P-F emission, will be suppressed. Therefore, tunneling processes, which are temperature independent, could be the dominant current transport mechanism at low temperature. At high bias, F-N tunneling of carriers through the triangular barrier to the conduction band of oxide will occur. When there are traps or defects in the oxide, trap-assisted tunneling could occur through the traps [141, 142].

The F-N plot of the Pt/TiO_2/*p*-Si capacitor at negative substrate bias is shown in Figure 7.15. There is a linearity of about three orders of magnitude at high bias. This is due to the F-N tunneling of electrons from the inversion layer of *p*-Si substrate. The TiO_2/Si potential barrier $\Phi_{TiO_2/Si}$ at the conduction band is determined from the slope of the straight line and Equation 7.3, which gives $\Phi_{TiO_2/Si} = 0.73$ V.

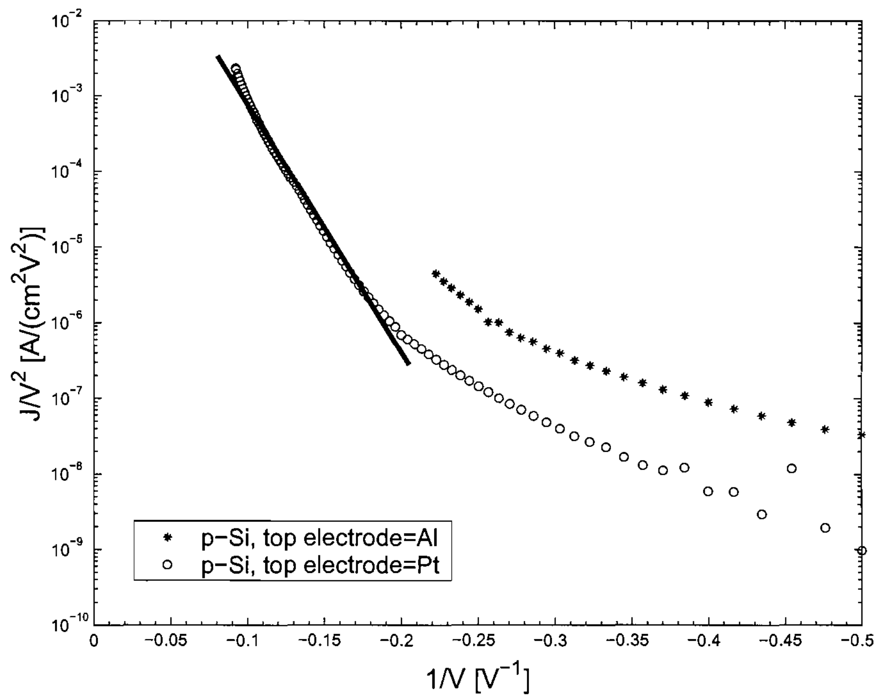

Figure 7.15: The Fowler-Nordheim plot of the 18 nm TiO_2 layers (with *p*-Si only) at 84 K, at negative substrate bias. The straight line is a fit to Equation 7.1.

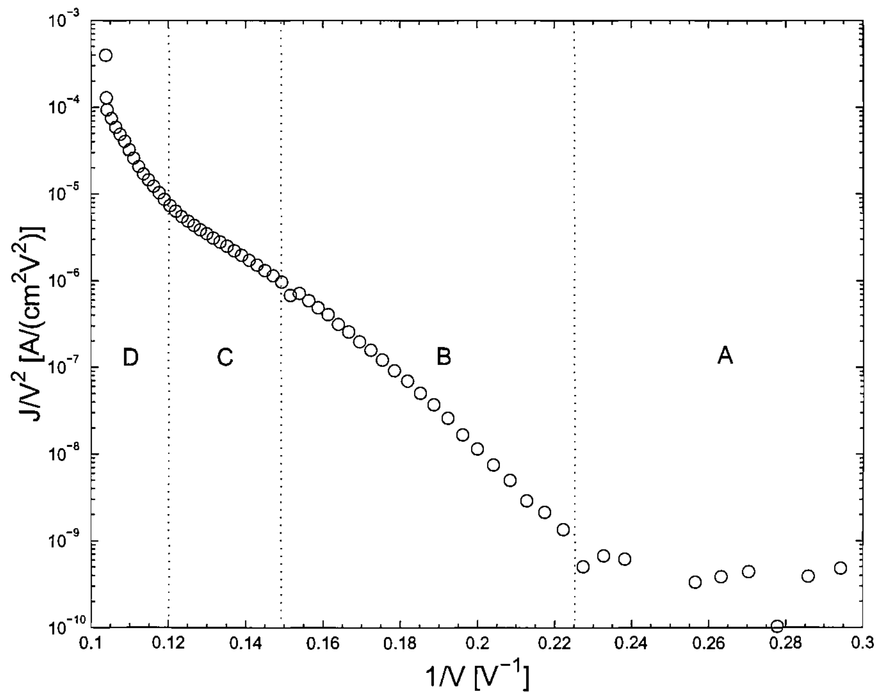

Figure 7.16: The Fowler-Nordheim plot of the 18 nm TiO_2 layer (Pt top electrode, *p*-Si substrate) at 84 K. The four different regimes indicate four different mechanisms in the oxide.

Figure 7.16 shows the F-N plot of a Pt/TiO_2/*p*-Si capacitor at positive substrate bias. It is noted that there are four significantly different regimes visible in the F-N plot. At low bias (regime A), hopping conduction is the dominant current transport mechanism, as shown by the J vs V hopping plot in Figure 7.17. The current increases sharply for a bias greater than 4.5 V, due to trap-assisted tunneling (regime B) as will be explained in the next paragraphs. This is followed by a quasi-saturation stage (regime C) for biases between 6.5 V and 8 V. A similar phenomenon was observed by Wong *et al.* [154] in thermally nitrided SiO_2. For bias above 8 V, F-N tunneling can occur (regime D).

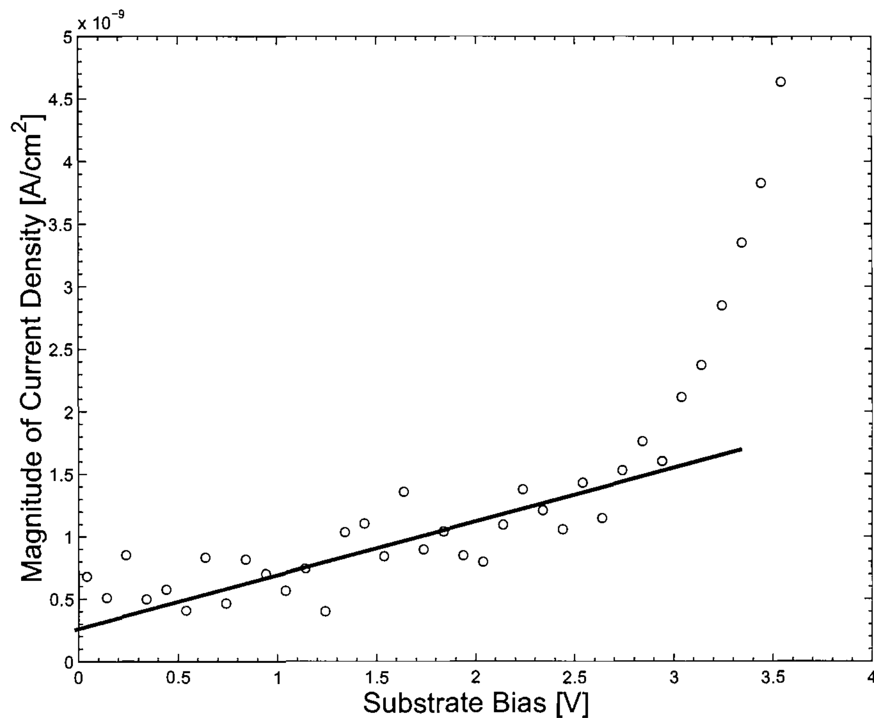

Figure 7.17: The hopping conduction plot of the 18 nm TiO_2 layer at 84 K and at low positive substrate bias. The straight line is a visual guide.

Figure 7.18 shows the $ln\ J$ versus $1/V$ trap-assisted tunneling plot. It is clear that for biases between 4.5 and 6 V, the current transport mechanism is due to trap-assisted tunneling of holes. Using Equation 7.7, the trap activation energy is found to be 0.90 eV above the valence band, which is similar to the trap level observed earlier by Klusek *et al.* [155] in heavily reduced TiO_2. The filling of this trap level by holes in our samples led to the saturation of current in regime C in Figure 7.16. The more well-known trap level at 0.7 eV below the conduction band [78, 79] was not observed here as the substrate is *p*-type and holes are the majority charge carriers.

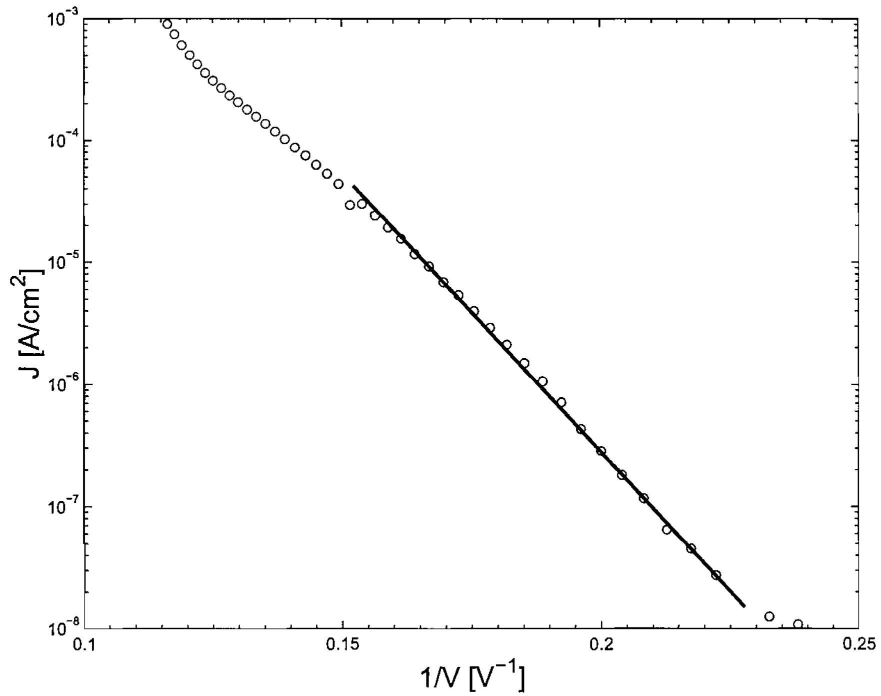

Figure 7.18: The trap-assisted tunneling plot of the 18 nm TiO_2 layer (Pt top electrode, *p*-Si substrate) at 84 K and positive substrate bias. The straight line is a fit to equation 7.5.

In conclusion, F-N tunneling of holes is not observed in thermally grown TiO_2 layer at room temperature due to P-F emission. At low temperature, such as 84 K, trap-assisted tunneling becomes the dominant current transport mechanism. The trap activation energy is 0.90 eV. It is these traps or defects in the oxide that enhance the trap-related current transport mechanisms. It is concluded that F-N tunneling is not the dominant current transport mechanism in TiO_2 layers grown by thermal oxidation on e-beam evaporated Ti thin films. Therefore, unless the trap density can be reduced significantly, F-N tunneling current cannot be observed in TiO_2.

7.4.4 Comparison of the Electrical Properties with Reported Literature

In this section, the electrical characteristics of our thermally grown TiO_2 thin films were compared with reported fabrication methods in literature. This is to investigate if a better quality of TiO_2 (in terms of leakage current) can be fabricated by other techniques. Figures 7.19 and 7.20 show leakage currents flowing through similar MOS capacitors where oxide layers of similar thicknesses were deposited by different techniques. The graphs show I-V characteristics of the capacitors under accumulation condition only to ensure that the leakage current is not influenced by the depletion region in the silicon substrate. Figure 7.19 compares the I-V characteristics of our thermally grown TiO_2 with those of as-deposited oxide layers grown by other techniques [87, 91, 111]. It is observed that the leakage current in the thermally grown TiO_2 is about three orders of magnitude lower than that in plasma-oxidized TiO_2 [87] and in e-beam deposited TiO_2 [111]. At low bias, thermally grown TiO_2 also has a lower leakage current than PECVD-grown TiO_2 [91]. As the leakage current in other techniques is unacceptably high, post deposition treatments are usually performed in oxygen. Leakage currents in capacitors using thermally grown TiO_2 are compared with those using annealed oxides grown by other techniques in Figure 7.20. The devices have similar structures and oxide thicknesses. The MOCVD-grown TiO_2 was post-annealed at 750 °C in O_2 [67] while the e-beam grown TiO_2 was annealed at 700 °C in O_2 for 60 mins [111]. From Figure 7.20, it is clear that leakage currents in our thermally grown TiO_2 thin films are very similar to those in the post-growth annealed oxide layers.

It is evident that as-deposited titanium oxide layers produced by plasma oxidation [87], PECVD [91], e-beam evaporated [111], MOCVD [67] often exhibit high leakage current and post-growth anneals at high temperatures help to reduce this [67, 111]. Interestingly, the annealed oxide layers exhibit I-V characteristics similar to those of thermally grown TiO_2. Hence, it is suggested that irrespective of the deposition technique, annealing of the as-deposited TiO_2 in O_2 is a similar process to thermal oxidation of e-beam evaporated Ti thin films. The leakage current could be due to high density of charges in the oxides, which is about $10^{12}cm^{-2}$ in thermally grown TiO_2. This is in agreement with values reported in literature for TiO_2 films fabrication by different methods [91, 111]. It is therefore suggested these TiO_2 fabrication processes will grow oxide layers with high density of charges. It is believed that the traps is related to the high density of charge in the oxide. Therefore,

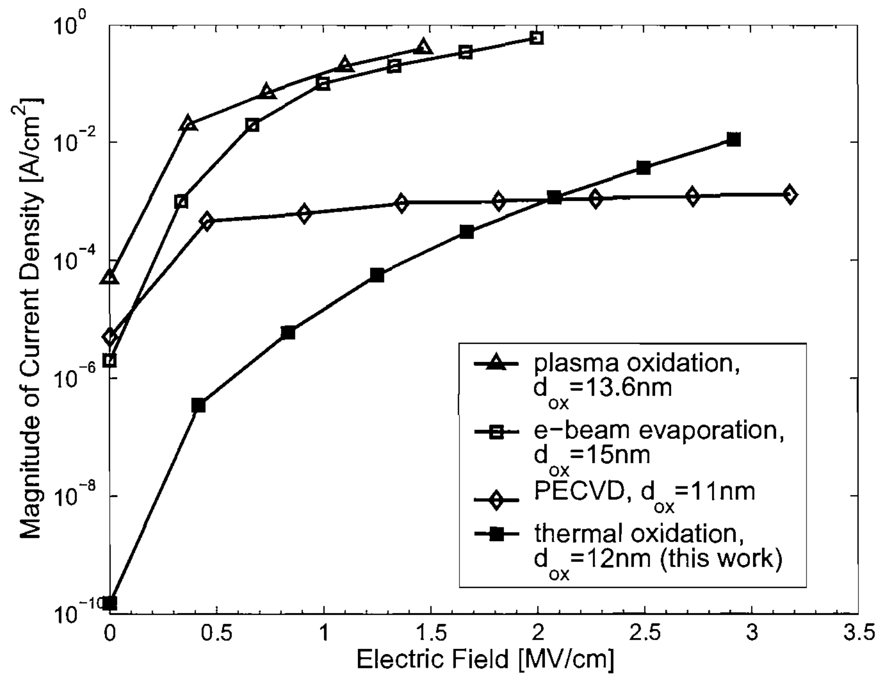

Figure 7.19: The comparison of the I-V characteristics of 12 nm TiO_2 grown by thermal oxidation with plasma oxidation[87], e-beam evaporation [111], and PECVD [91]. The thermally grown TiO_2 was fabricated by oxidizing 7 nm of Ti thin film at 550 °C.

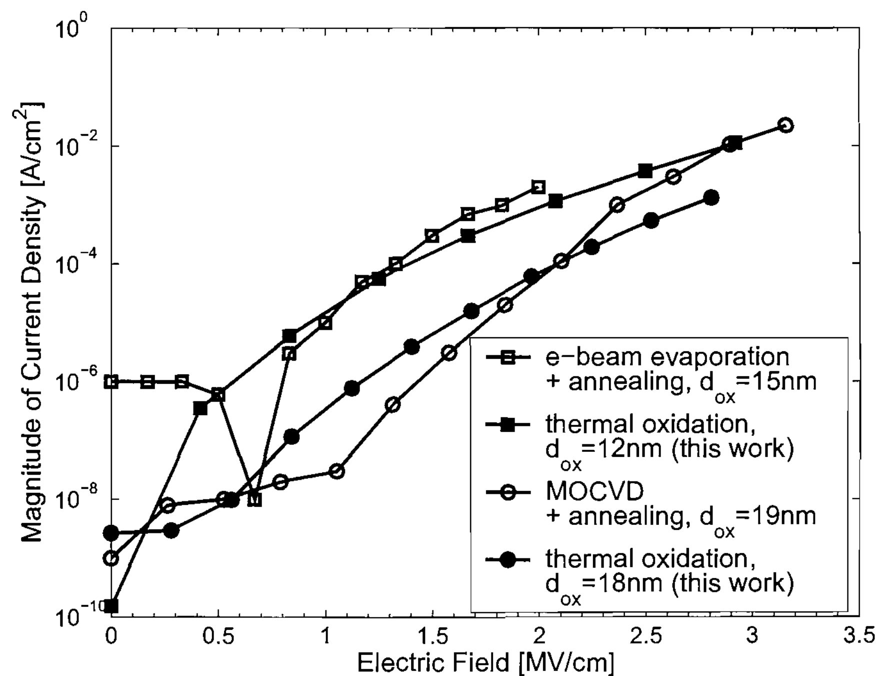

Figure 7.20: The comparison of the I-V characteristics of thermal oxidized TiO_2 with other fabrication methods with post deposition annealing: MOCVD [67] and e-beam evaporation [111].The 12 nm and 18 nm thermally grown TiO_2 were fabricated by oxidizing 7 nm and 10 nm Ti thin film at 550 °C, respectively.

for F-N tunneling to be the dominant mechanism in TiO_2 layer, a suitable technique is required to reduce the charge density in the oxide. Only then, TiO_2 can be a suitable tunnel barrier for VMISTT.

7.5 Conclusion

It is shown that TiO_2 layers grown at 550 °C have a dielectric constant of 12.5 and a charge density of $10^{12}cm^{-2}$. In addition, it is found that the top electrode in a MOS capacitor can affect the electrical characteristic of the oxide. Although Al has a suitable work function for n-VMISTT, it can react with TiO_2 to form an interfacial layer of about 3 nm. This may affect VMISTT operation as the interfacial layer can increase the charge density and induce trap-related current transport mechanism. Therefore, a metal with a similar work function as Al, but less reactive than Al should be considered for the drain electrode in n-VMISTT. Copper would seen to be a reasonable alternative.

The most important criteria for a tunnel barrier is the ability to exhibit F-N tunneling current at room temperature. However, F-N tunneling is not the dominant current transport mechanism in the thermally grown TiO_2 layer due to the trap-related mechanisms. It is observed that P-F emission is the dominant mechanism at room temperature, due to the traps or defects in the oxide. At low temperatures and low bias, the dominant mechanism is hopping conduction. F-N tunneling due to electrons is observed at low temperature and high negative substrate bias. The TiO_2/Si barrier at the conduction band is 0.73 eV. Quasi-saturation is observed in the I-V characteristic at low temperature and at positive substrate bias. It is believed that this is due to filling of defect-related traps above the valence band with holes during the trap-assisted tunneling process. The trap activation energy is 0.90 eV, identical to the values observed in the literature. F-N tunneling of holes is not observed due to the traps in the oxide.

The leakage current density of the thermally grown TiO_2 thin films was compared with as-deposited and annealed oxide layers grown by other techniques. Thermally grown TiO_2 thin films have lower leakage current densities than those of as-deposited oxides, and exhibit leakage current densities similar to those of annealed oxides. It is suggested that deposition of TiO_2 followed by annealing is equivalent to direct thermal oxidation of metallic Ti films and produce similar oxide quality in terms of leakage currents and interface states. The

comparison also suggests that the TiO_2 layers grown by those fabrication techniques all exhibit high leakage current due to high density of charges in the oxide, which is about $10^{12}cm^{-2}$. It is believed that it is this high charge density that masks the observation of F-N tunneling current in TiO_2 layers. A technique or process stage is required to reduce the charge density so that the trap-related mechanisms are suppressed. In that case, TiO_2 can be considered as the tunnel barrier in VMISTT.

Chapter 8

Conclusion

In this thesis, a new type of transistor, the vertical metal insulator semiconductor tunnel transistor (VMISTT) has been proposed. The VMISTT is a vertical modified version of the MOTT. It inherits the advantages offered by the MOTT, which includes high speed, simple fabrication process, and small transistor active area. Its operation is similar to the MOTT but with two different features. Firstly, the metallic source in the MOTT is replaced by a silicon source. By choosing appropriate types of silicon and proper metals for the drain, it is possible to realise complementary operation in the VMISTT. For an n-type VMISTT, the source is n-Si, and the drain metal should have a low value of work function. This is to allow electron F-N tunneling from Si at positive gate bias and prevent hole F-N tunneling from the drain. On the other hand, for a p-type VMISTT, the source is p-Si, and the drain metal should have a high value of work function. With that, hole F-N tunneling can occur from the Si at negative gate bias and the electron F-N tunneling can be prevented from the drain. Secondly, the vertical structure of the VMISTT can increase the channel width controlled by the gate bias, and also allow better material growth and device processing. These may help to improve the transistor performance at room temperature, which is one of the main drawback of the original MOTT.

Simulations of an n-VMISTT were performed to understand the effect of device parameters on the transistor performance. It has been shown that the barrier height Φ_B between the tunnel barrier and the Si source is an important device parameter which can affect the VMISTT performance significantly. The simulations results shows that F-N tunneling current is high for a low value of Φ_B. However, Schottky emission, which is the main source of leakage current, is significant at low Φ_B. For a high value of Φ_B, Schottky emission can

be suppressed. But, this also results in low F-N tunneling current. The tunnel barrier thickness d_{ox} is another important parameter. If d_{ox} is too small, the non-modulated F-N tunneling current will be too high, which results in huge off-state currents. If d_{ox} is too large, the resistance of the tunnel barrier will reduce the on-state current. Besides by optimisation of these two parameters, it has been shown from the simulation results that the device performance can also be improved by the ratio of tunnel barrier dielectric constant over the gate oxide dielectric constant R. A low value in R can improve the gate field modulation of the tunnel barrier potential profile and hence increase the on-state current. In addition, the device performance can be further improved by having a smaller device depth, lower operating temperature and lower drain bias. The 2-D simulations of an n-VMISTT with Φ_B=0.6 V and d_{ox}=10 nm shows an SVT of 42.56 mV/dec, which is superior to MOSFET. Although the drain current swing is only four orders of magnitude, a higher dielectric constant R and a thinner gate oxide can increase I_{on} by improving the gate modulation on the tunnel barrier potential profile.

The fabrication of the VMISTT can be divided into three main phase: firstly, the fabrication and optimisation of the tunnel barrier; secondly, the fabrication of the vertical pillar; thirdly, the deposition of gate oxide. The fabrication and optimisation of the tunnel barrier is the focus of the experimental chapters of this thesis. TiO_2 is a suitable material for the tunnel barrier because the barrier height to Si is 1 V at the conduction band as well as at the valence band. TiO_2 layers were fabricated by thermal oxidation of e-beam evaporated Ti thin film. This is because this technique can produce oxides with minimum roughness, while preserving the substrate smoothness. TiO_2 layers grown by an MBE deposition technique have also been studied. It has been shown that thermally grown TiO_2 layers are superior to the MBE grown oxide in terms of the leakage current. Hence, further characterisations were performed on the thermally grown TiO_2 layers.

MOS capacitors were fabricated to characterise the thermally grown TiO_2 thin film and optimise the fabrication process. It is determined that the optimised oxidation temperature for TiO_2 layers is 550 °C. Post oxidation annealing is not beneficial for the oxide. Annealing at temperature higher than oxidation temperature will cause the growth of an interfacial SiO_2 layer. This is undesired because it will reduce F-N tunneling current due to the high barrier of the SiO_2 layer. In addition, it has been shown that alloying of Al back

contact is not required for the MOS capacitors because the high doping concentration in the Si substrate ensures an ohmic back contact. Furthermore, it is observed that the alloyed sample exhibit higher leakage current due to the diffusion of Al atoms from the top electrode into the TiO_2 layers. This is undesired because it will affect the electrical properties of the oxide layer.

Structural analysis was performed on the thermally grown TiO_2 layer. It has been shown by SEM that 13 and 18 nm TiO_2 layers can be grown from 7 and 10 nm Ti thin film, respectively. The TOF-SIMS results indicate that inter-diffusion of Ti and Si atoms occur during the oxidation process. There is also evidence of SiO_2 and titanium silicates interfacial layers at the TiO_2/Si interface. XRD analysis shows that the oxide grown at 550 °C is amorphous. The rutile phase is only observed in thicker oxide grown at 750 °C for 2 hours.

To study the effect of top electrode and Si substrate on the oxide layer and current transport mechanisms, TiO_2 MOS capacitors with different top electrodes (Al, Pt) and Si substrates (*n*-type, *p*-type) were fabricated. The oxide were grown from 10 nm Ti at 550 °C. The I-V and C-V analysis indicate that even at room temperature Al top electrode can react with the oxygen in the TiO_2 thin films at the Al/TiO_2 interface, resulting in the top 3 nm of the TiO_2 being depleted in oxygen. It has been shown that the as-grown oxide have a dielectric constant of 12.5 and a charge density of about 10^{12} cm^{-2}.

The current transport mechanism in TiO_2 at room temperature is P-F emission, due to the traps or defects in the oxide. At low temperatures and low bias, the dominant mechanism is hopping conduction. F-N tunneling due to electrons is observed at low temperature and high bias. The TiO_2/Si barrier at the conduction band is 0.73 eV. Quasi-saturation is observed in the I-V characteristic at low temperature. It is believed that this is due to filling of defect-related traps above the valence band with holes during the trap-assisted tunneling process. The trap activation energy is shown to be 0.90 eV.

The leakage current density of the thermally grown TiO_2 thin films were compared with as-deposited and annealed oxide layers grown by other techniques. It has been shown that thermally grown TiO_2 thin films have lower leakage current densities than those of as-deposited oxides, and exhibit leakage current densities similar to those of annealed oxides.

It is suggested that deposition of TiO_2 followed by annealing is equivalent to direct thermal oxidation of metallic Ti films and produce similar oxide quality in terms of leakage currents and interfacial states.

It is suggested that the leakage current in thermally grown TiO_2 layer is mainly due to the high charge density, which is about 10^{12}cm^{-2} in both reported literature and the thermally grown TiO_2. A better technique is required to reduce the charge density. With that, trap-related mechanisms can be suppressed, and F-N tunneling current may arise as the dominant mechanism.

Future works on the VMISTT project can focus on the simulations of VMISTT complementary operation. Simulations have been performed on the n-VMISTT. Simulations on the p-VMISTT need to be performed so that the complementary operations of the VMISTT can be studied in details.

There are two directions to realise the observation of F-N tunneling in the tunnel barrier: using a new deposition technique and/or a new material for tunnel barrier. It is believed that MBE grown TiO_2 layer of varying thickness is useful for understanding and characterization of the oxide electrical properties. However, the as-grown oxide layer exhibit huge leakage current compared to the thermally grown TiO_2 layer. Further optimisation on the MBE system is required to allow characterisation of the oxide layer. Besides TiO_2, Ta_2O_5 is another material with relatively low barrier to the Si. Therefore, the electrical properties of Ta_2O_5 thin film can be studied. If F-N tunneling is observed in the tunnel barrier, then, the fabrication of VMISTT can proceed.

Appendix A

List of Symbols

A	-	cross-sectional area of the current flow [m^2]
A_{FN}	-	prefactor of Fowler-Nordheim tunneling current
A_{PF}	-	prefactor of Poole Frenkel emission
A_{SC}	-	prefactor of Schottky emission
A_{TAT}	-	prefactor of trap assisted tunneling current
B_{FN}	-	slope of the linear $ln(J/V^2)$ versus $1/V$ F-N plot
B_{PF}	-	slope of the linear $ln(J/V)$ versus $\sqrt{V}$ P-F plot
B_{SC}	-	slope of the linear lnJ versus $\sqrt{V}$ Schottky plot
B_{TAT}	-	slope of the linear lnJ versus $1/V$ trap-assisted tunneling plot
C	-	capacitance per unit area[F/m^2]
C_d	-	capacitance due to the depletion region per unit area [F/m^2]
C_{it}	-	capacitance per unit area due to interface traps [F/m^2]
C_{min}	-	minimum capacitance per unit area [F/m^2]
C_{ox}	-	oxide capacitance per unit area [F/m^2]
C_{Si}	-	Si capacitance per unit area [F/m^2]
C_{SiO_2}	-	SiO_2 capacitance per unit area [F/m^2]
C_{TiO_2}	-	TiO_2 capacitance per unit area [F/m^2]
d_0	-	oxide thickness of the MBE samples at site 00 [m]
d_{hkl}	-	interplanar spacing of a crystalline solid [m]

d_{ox}	-	oxide thickness [m]
d_{Si}	-	Depletion width in Si substrate [m]
d_{SiO_2}	-	SiO_2 thickness [m]
d_t	-	tunnel barrier thickness in MOTT [m]
d_{TiO_2}	-	TiO_2 thickness [m]
D	-	depth [m]
E	-	electric field [V/m]
E_c	-	conduction band energy level [eV]
E_f	-	Fermi energy level [eV]
E_g	-	bandgap [eV]
E_{fm}	-	metal Fermi energy level [eV]
E_i	-	intrinsic energy level [eV]
E_v	-	valence band energy level [eV]
F	-	attractive force between the two charges [N]
G	-	grain size [m]
h	-	Planck's constant [Js]
I	-	current [A]
I_D	-	drain current [A]
I_{DS}	-	drain to source current [A]
I_{Dsat}	-	drain current at saturation [A]
I_{off}	-	off-state current [μA/μm]
I_{on}	-	on-state current [μA/μm]
J	-	current density [A/m^2]
J_{FN}	-	Fowler-Nordheim current density [A/m^2]
k	-	Boltzman's constant [J/K]

l	-	interval of separation between adjacent hopping sites [m]
L	-	channel length of MOSFETs [m]
m^*	-	tunneling effective mass of electron
m_0	-	electron rest mass [kg]
n	-	number for indexing
n^*	-	density of free electron [cm^{-3}]
n_0	-	carrier density [cm^{-3}]
n_i	-	intrinsic carrier for Si [cm^{-3}]
n_s	-	carrier concentration at Si surface [cm^{-3}]
N_A	-	p-type semiconductor doping concentration [cm^{-3}]
N_D	-	n-type semiconductor doping concentration [cm^{-3}]
P_e	-	potential energy of an electron [J]
P_E	-	potential energy due to the applied electric field [J]
P_{total}	-	total potential energy [J]
q	-	magnitude of the electronic charge [C]
Q_d	-	depletion region charges per unit area [C/m^2]
Q_i	-	oxide and interface charges per unit area [C/m^2]
R	-	ratio of tunnel barrier dielectric constant over the gate oxide dielectric constant
R_c	-	calculated resistance [Ω]
R_e	-	experimental derived resistance [Ω]
R_{it}	-	resistance per unit area due to interface traps [Ω/m^2]
S	-	slope of a linear line
SVT	-	subthreshold slope [mV/dec]
T	-	temperature [K]
T_{ox}	-	oxidation temperature [°C]

v_{sat}	-	saturation velocity [m/s]
V	-	voltage [V]
V_{dd}	-	supply voltage [V]
V_D	-	drain voltage [V]
V_{DS}	-	drain to source voltage [V]
V_{Dsat}	-	drain voltage at saturation [V]
V_{FB}	-	flatband voltage [V]
V_G	-	gate voltage [V]
V_{ox}	-	voltage across the oxide [V]
V_T	-	threshold voltage [V]
w_t	-	tunnel barrier width in MOTT [m]
W	-	channel width in MOSFETs [m]
W_{Si}	-	width of the depletion region in Si [m]
x	-	a variable for length [m]
x_m	-	location of the image-force-induced lowering [m]
$y_{intercept}$	-	y-axis intercept of a linear line
Z_{out}	-	output impedance of the transistor [Ω]
β	-	full width half maximum [radian]
β_{SC}	-	slope of the linear $ln(J/T^2)$ versus $1/T$ Schottky plot
χ	-	electron affinity [V]
ΔE_C	-	difference in conduction band energy level [eV]
ΔE_T	-	activation energy [eV]
ΔE_V	-	difference in valence band energy level [eV]
ΔL	-	channel length modulation [m]
Δphi	-	image force induced lowering [V]

Δt - difference of TiO_2 thickness between two consecutive devices along the main diagonal of the MBE sample [m]

ϵ_0 - permittivity of free space [F/m]

ϵ_g - dielectric constant of the gate oxide

ϵ_{ox} - permittivity of the oxide [F/m]

ϵ_r - dielectric constant of the oxide

ϵ_{Si} - dielectric constant of Si

ϵ_{SiO_2} - dielectric constant of SiO_2

ϵ_t - dielectric constant of the tunnel barrier

ϵ_{TiO_2} - dielectric constant of TiO_2

Γ - mean hopping frequency [Hz]

λ - wavelength [m]

ϕ_s - surface potential of the Si substrate [V]

Φ_B - barrier height of tunnel barrier [V]

Φ_m - metal work function potential [V]

Φ_s - semiconductor work function potential [V]

Φ_{ms} - metal and semiconductor work function potential difference [V]

Φ_f - $(E_i - E_f)/q$ [V]

Φ_T - barrier height of the traps [V]

μ - mobility of carriers [m^2/Vs]

μ_n - electron mobility in channel [m^2/Vs]

ρ - resistivity [Ωm]

τ - interface trap time constant [s]

θ - diffraction angle

Appendix B

LMS Listing

B.1 Comparison of the Batches

Batch A	-	first batch described in Section 5.4.1
Batch B	-	second batch described in Section 5.4.1
		and the batch described in in Section 6.2
Batch C	-	batch described in Section 7.3
Batch D	-	samples fabricated for XRD, described in Section 6.2

Table B.1: Comparison of the wafer batches.

Batches	A	B	C	D
Devices	Al/TiO_2/p-Si	Al/TiO_2/p-Si	Al/TiO_2/n-Si Pt/TiO_2/p-Si	TiO_2/p-Si
Ti Thickness [nm]	10	7, 10	10	100, 500
Oxidation Temperature [°C]	300 400 500	450 500 550	550	550 750
Oxidation Time [min]	30	30	30	120
Post Oxidation Annealing	Batch Split: (1) 700 °C, N_2, 30 min (2) No	No	No	No
Alloying of Al back contact	450 °C, H_2/N_2, 30 min	Batch Split: (1) 450 °C, H_2/N_2, 30 min (2) No	No	No

B.2 LMS listing for Batch A

Refer to Section 5.4.1.

	LMS ID	Description
1	G-S12	6 wafers, *p*-Si, 0.02 Ωcm
2	W-C1	RCA clean (wafers 1-6).
3	WH-2D1	Dip etch, 20:1 BHF, 25 °C until just hydrophobic (wafers 1-6).
4	ME-0X	Evaporate 10 nm Ti thin films (wafers 1-6).
5	F7-0	Load O_2, 300 °C for 30 minutes (wafers 1, 4).
6	F7-0	Load O_2, 400 °C for 30 minutes (wafers 2, 5).
7	F7-0	Load O_2, 500 °C for 30 minutes (wafers 3, 6).
8	F7-0	Load N_2, 700 °C for 30 minutes (wafers 1, 2, 3).
9	ME-0	Evaporate 1000 nm Al on wafer front using shadow mask (wafers 1-6).
10	WH-0X	Remove oxide on wafer back using cotton bud in 7:1 BHF (wafers 1-6).
11	ME-0	Evaporate 1000 nm Al on wafer back (wafers 1-6).
12	F7-H45CX	Alloying in H_2/N_2 (60% of H_2 and 40% of N_2) at 450 °C for 30 mins (wafers 1-6).

B.3 LMS listing for Batch B

Refer to Section 5.4.1 and 6.2.

	LMS ID	Description
1	G-S12	6 wafers, *p*-Si, 0.02 Ωcm
2	W-C1	RCA clean (wafers 1-6).
3	WH-2D1	Dip etch, 20:1 BHF, 25 °C until just hydrophobic (wafers 1-6).
4	ME-0X	Evaporate 10 nm Ti thin films (wafers 1-3).
5	ME-0X	Evaporate 7 nm Ti thin films (wafers 4-6).
6	F7-0	Load O_2, 450 °C for 30 minutes (wafers 1, 4).
7	F7-0	Load O_2, 500 °C for 30 minutes (wafers 2, 5).
8	F7-0	Load O_2, 550 °C for 30 minutes (wafers 3, 6).
10	ME-0	Evaporate 1000 nm Al on wafer front using shadow mask (wafers 1-6).
11	WH-0X	Remove oxide on wafer back using cotton bud in 7:1 BHF (wafers 1-6).

12	ME-0	Evaporate 1000 nm Al on wafer back (wafers 1-6).
13	G-3	Cut all wafers into half (wafers 1-6). One half keep for comparison.
14	F7-H45CX	Alloying in H_2/N_2 (60% of H_2 and 40% of N_2) at 450 °C for 30 mins (wafers 1-6).

B.4 LMS listing for Batch C

Refer to Section 7.3.

	LMS ID	Description
1	G-S12	6 wafers, 0.02 Ωcm: 4 *n*-Si (wafers 1-4), 2 *p*-Si (wafers 5-6).
2	W-C1	RCA clean (wafers 1-6).
3	WH-2D1	Dip etch, 20:1 BHF, 25 °C until just hydrophobic (wafers 1-6).
4	ME-0X	Evaporate 10 nm Ti thin films (wafers 1-6).
5	F7-0	Load O_2, 550 °C for 30 minutes (wafers 1-6).
6	ME-0	Evaporate 1000 nm Al on wafer front using shadow mask (wafers 4,6).
7	ME-0	Evaporate 200 nm Pt on wafer front using shadow mask (wafers 1-3,5).
8	WH-0X	Remove oxide on wafer back using cotton bud in 7:1 BHF (wafers 1-6).
9	ME-0	Evaporate 1000 nm Al on wafer back (wafers 1-6).

B.5 LMS listing for Batch D

Refer to Section 6.2.

	LMS ID	Description
1	G-S12	4 wafers, *p*-Si, 0.02 Ωcm
2	W-C1	RCA clean (wafers 1-4).
3	WH-2D1	Dip etch, 20:1 BHF, 25 °C until just hydrophobic (wafers 1-4).
4	ME-0X	Evaporate 100 nm Ti thin films (wafers 1,3).
5	ME-0X	Evaporate 500 nm Ti thin films (wafers 2,4).
6	F7-0	Load O_2, 550 °C for 120 minutes (wafers 1,2).
7	F7-0	Load O_2, 750 °C for 120 minutes (wafers 3,4).

Appendix C

Atlas Codes

C.1 Simulation of the Tunnel Barrier Potential Profile in VMISTT

Refer to Section 4.3(a).

```
#The device is a 2D n-VMISTT, but with metallic source, as no barrier between the Si and oxide.
#Potential profile at different biases condition can be obtained by changing vgate and vdrain.
#nitride: gate oxide, thickness=2nm
#oxide: channel oxide, thickness=10nm

go atlas

mesh
x.mesh loc=0.00 spac=0.1
x.mesh loc=0.90 spac=0.01
x.mesh loc=0.98 spac=0.01
x.mesh loc=0.99 spac=0.0001
x.mesh loc=1.00 spac=0.0001
x.mesh loc=1.002 spac=0.001
x.mesh loc=1.01 spac=0.01
y.mesh loc=0.00 spac=0.01
y.mesh loc=0.008 spac=0.0001
y.mesh loc=0.01 spac=0.0001
y.mesh loc=0.02 spac=0.0001
y.mesh loc=0.022 spac=0.0001
y.mesh loc=0.03 spac=0.01
```

```
region num=1 oxide y.min=0.01 y.max=0.02 x.min=0.0 x.max=1.0
region num=2 nitride y.min=0.0 y.max=0.51 x.min=1.0 x.max=1.002

electrode name=drain y.min=0.00 y.max=0.01 x.min=0.00 x.max=1.0
electrode name=source y.min=0.02 y.max=0.20 x.min=0.00 x.max=1.0
electrode name=gate y.min=0.00 y.max=0.51 x.min=1.002 x.max=1.01

contact name=drain workfunction=1
contact name=gate workfunction=1
contact name=source workfunction=1

material material=oxide affinity=3.6 eg300=3.2 nc300=2.509e19 nv300=2.509e19 permittivity=30.0
material material=nitride affinity=0.9 eg300=9.0 nc300=1.0e19 nv300=1.0e19 permittivity=100.0

method carriers=2 newton trap maxtraps=8 autonr output efield con.band val.band

solve init
solve vgate=3 outf=solve_vgate
load infile=solve_vgate
solve vdrain=3
save outfile=vg3vd3_r03.str

quit
```

C.2 I_D vs V_G curve of VMISTT

Refer to Section 4.3(b).

```
#This code is used to generate the I_D vs V_G curve of the n-VMISTT
#The 0.6V potential barrier at oxide/Si interface is set by the f.ae and f.be of the fnord parameter.
#The I-V characteristic is obtained by setting Vdrain=1 V, and sweeping Vgate from 0 to 3 V
#oxide: channel, thickness=10nm
#nitride: gate oxide, thickness=2nm

go atlas

mesh
x.mesh loc=0.00 spac=0.01
x.mesh loc=0.01 spac=0.01
x.mesh loc=0.90 spac=0.01
```

```
x.mesh loc=1.00 spac=0.0001
x.mesh loc=1.002 spac=0.0001
x.mesh loc=1.01 spac=0.01
y.mesh loc=0.00 spac=0.01
y.mesh loc=0.01 spac=0.001
y.mesh loc=0.02 spac=0.001
y.mesh loc=0.20 spac=0.02
y.mesh loc=0.50 spac=0.01
y.mesh loc=0.51 spac=0.01

region num=1 silicon y.min=0.02 y.max=0.50 x.min=0.0 x.max=1.0
region num=2 oxide y.min=0.01 y.max=0.02 x.min=0.0 x.max=1.0
region num=3 nitride y.min=0.0 y.max=0.51 x.min=1.0 x.max=1.002

electrode name=drain y.min=0.00 y.max=0.01 x.min=0.00 x.max=1.0
electrode name=source y.min=0.50 y.max=0.51 x.min=0.00 x.max=1.0
electrode name=gate y.min=0.00 y.max=0.51 x.min=1.002 x.max=1.01

doping uniform conc=1e19 n.type region=1
contact name=drain workfunction=4.1
contact name=gate workfunction=4.1

material material=oxide affinity=3.6 eg300=3.2 nc300=2.509e19 nv300=2.509e19 permittivity=30.0
material material=nitride affinity=0.9 eg300=9.0 nc300=1.0e19 nv300=1.0e19 permittivity=100.0

models region=2 fnord f.ae=2.5606e-6 f.be=3.1696e7
models region=3 fnord f.ae=0.0 f.be=0.0
models print

method carriers=2 newton trap maxtraps=8 autonr output efield con.band val.band

solve vdrain=1 outf=Vd1Vg0
save outfile=Vd1Vg0.str

load infile=Vd1Vg0
log outfile=pVgId_eps_r01V.log
solve name=gate vgate=0.0 vstep=0.1 vfinal=3.0
tonyplot pVgId_eps_r01V.log -set current.set

quit
```

C.3 Ideal Capacitance-Voltage Curve

Refer to Section 7.4.2.

```
# This is the code for Al/TiO2/n-Si MOS capacitor.
# The C-V curve is obtained by sweeping the bias from -10V to 10V
# For device with Pt top electrode, replace Aluminum with Platinum in region 1.
# For device with p-Si:
# (1) set "doping region=3 p.type concentration=3e18 uniform",
# (2) set "contact name=gate workfunction=5.23",
# (3) change the sweeping from 10V to -10V

go atlas

mesh
x.mesh loc=0 spac=0.01
x.mesh loc=1 spac=0.01
y.mesh loc=0 spac=0.1
y.mesh loc=0.01 spac=0.001
y.mesh loc=0.03spac=0.001
y.mesh loc=0.04 spac=0.001
y.mesh loc=0.5 spac=0.1

region number=1 x.min=0 x.max=1 y.min=0 y.max=0.01 material=Aluminum
region number=2 x.min=0 x.max=1 y.min=0.01 y.max=0.0255 material=oxide
region number=3 x.min=0 x.max=1 y.min=0.0255 y.max=0.5 material=silicon

electrode x.min=0 x.max=1 y.min=0 y.max=0.01 name=gate
electrode bottom name=substrate

doping region=3 n.type concentration=1e18 uniform
contact name=gate workfunction=4.25
material material=oxide affinity=3.9 eg300=3.2 nc300=2.509e19 nv300=2.509e19 permittivity=13
interface x.min=0 x.max=1 y.min=0.01 y.max=0.04 qf=0
models mos print consrh method carriers=2 newton trap maxtraps=8 autonr

solve init
log outfile=CV_1MHz.log solve vgate=-10 vstep=0.5 vfinal=5.0 name=gate ac freq=1e6 previous
tonyplot CV_1MHz.log -set CV.set
quit
```

Appendix D

Publications

D.1 Journal Papers

- "The structural and electrical properties of thermally grown TiO_2", L.H. Chong, K. Mallik, C.H. de Groot, Reinhard Kersting, *Journal of Physics: Condensed Matter*, 18 (2006), p645-657

- "The vertical metal insulator semiconductor tunnel transistor: a proposed Fowler-Nordheim tunneling device", L.H. Chong, K. Mallik, C.H. de Groot, *Microelectronic Engineering*, 81 (2005), p171-180

D.2 Conference/Workshop

- "Design and material characterization of a complementary Fowler-Norhdeim tunneling transistor", L.H. Chong, K. Mallik and C.H. de Groot, MRS Spring Meeting, San Francisco, USA, March 2005

- "Design and material characterization of the vertical metal insulator semiconductor tunnel transistor (VMISTT)", L.H. Chong, K. Mallik and C.H. de Groot, Nanoelectronics Days, Julich, Germany February 2005

- "Vertical metal oxide tunneling transistor (VMOTT) and characterization of its tunnel oxide", L.H. Chong, K. Mallik, C.H. de Groot, Prep 2004, Hatfield, UK, April 2004

References

[1] G.Moore, "Progress in Digital Integrated Electronics," *IEDM Tech. Digest*, pp. 11–13, 1975.

[2] International Technology Roadmap, "International Technology Roadmap for Semiconductors," *http://public.itrs.net.*

[3] H.-S.P.Wong, "Beyond the conventional transistor," *IBM J. RES. & DEV.*, vol. 46, no. 2/3, pp. 133–168, March/May 2002.

[4] S.M.Sze, *Physics of Semiconductor Devices*, Wiley Inter-Science, 1981.

[5] G.D.Wilk, R.M.Wallace, and J.M.Anthony, "High-k dielectrics: current status and materials properties consideration," *J. Appl. Phys.*, vol. 89, pp. 5243–5275, 2001.

[6] D.A.Buchanan, "Scaling the gate dielectric: materials, integration, and reliability," *IBM J. RES. DEVELOP.*, vol. 43, no. 3, pp. 245–264, 1999.

[7] S.J.Rhee and J.C.Lee, "Threshold voltage instability characteristics of HfO_2 dielectrics n-MOSFETs," *Microelectronics Reliability*, vol. 45, pp. 1051–1060, 2005.

[8] M.LeRoy, E.Lheurette, O.Vanbesien, and D.Lippens, "Wave-mechanical calculations of leakage current through stacked dielectrics for nanotransistor metal-oxide-semiconductor design," *J. Appl. Phys.*, vol. 93, no. 5, pp. 2966–2971, March 2003.

[9] S.W. Huang and J.G. Hwu, "Electrical characterization and process control of cost-effective high-k aluminum oxide gate dielectrics prepared by anodization followed by furnace annealing," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1658–1664, July 2003.

[10] H.Y.Yu, J.F.Kang, J.D.Chen, C.Ren, Y.T.Hou, S.J.Whang, M.-F.Li, D.S.H.Chan, K.L.Bera, C.H.Tung, A.Du, and D.-L.Kwong, "Thermally robust high quality

HfN/HfO_2 gate stack for advanced CMOS devices," *IEDM*, pp. 4.5.1–4.5.4, Dec 2003.

[11] S.J.Rhee, C.Y.Kang, C. S.Kang, R.Choi, C.H.Choi, M.S.Akbar, and J.C.Lee, "Effects of varying interfacial oxide and high-k layer thicknesses for HfO_2 metal-oxide-semiconductor field effect transistor," *Appl. Phys. Lett.*, vol. 85, no. 7, pp. 1286–1288, 2004.

[12] C.C.Hobbs, L.R.C.Fonseca, A.Knizhnik, V.Dhandapani, S.B.Samavedam, W.J.Taylor, J.M. Grant, L.G. Dip, D.H.Triyoso, R.I.Hedge, D.C.Gilmer, R.Garcia, D.Roan, M.L.Lovejoy, R.S.Rai, E.A.Hebert, H.-H.Tseng, S.G.H.Anderson, B.E.White, and P.J.Tobin, "Fermi-level pinning at the polysilicon/metal oxide interface - part I," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 971–977, June 2004.

[13] C.C.Hobbs, L.R.C.Fonseca, A.Knizhnik, V.Dhandapani, S.B.Samavedam, W.J.Taylor, J.M.Grant, L.G.Dip, D.H.Triyoso, R.I.Hedge, D.C.Gilmer, R.Garcia, D.Roan, M.L.Lovejoy, R.S.Rai, E.A.Hebert, H.-H.Tseng, S.G.H.Anderson, B.E.White, and P.J.Tobin, "Fermi-level pinning at the polysilicon/metal oxide interface - part II," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 978–984, June 2004.

[14] L.Chang, Y.-K Choi, D.Ha, P.Ranade, S.Xiong, J.Bokor, C.M.Hu, and T.-J King, "Extremely scaled silicon nano CMOS devices," *Proceedings of The IEEE*, vol. 91, no. 11, pp. 1860–1873, Nov 2003.

[15] T.Schulz, W.Rosner, E.Landgraf, L.Risch, and U.Langmann, "Planar and vertical double gate concepts," *Solid-State Electronics*, vol. 46, pp. 985–989, 2002.

[16] X.J.Huang, W.C.Lee, C.Kuo, D.Hisamoto, L.Chang, J.Kedzierski, E.Anderson, H.Takeuchi, Y.K.Choi, K.Asano, V.Subramanian, T.J.King, J.Bokor, and C.M.Hu, "Sub-50nm p-channel FinFET," *IEEE Trans. Electron Devices*, vol. 48, no. 5, pp. 880–886, May 2001.

[17] Y.-K.Choi, N.Lindert, P.Xuan, S.Tang, D.Ha, E.Anderson, T.-J.King, J.Bokor, and C.M.Hu, "Sub 20nm CMOS FinFET technologies," *IEDM*, pp. 421–424, 2001.

[18] V.D.Kunz, T.Uchino, C.H.de Groot, P.Ashburn, D.C.Donaghy, S.Hall, Y.Wang, and P.L.F. Hemment, “Reduction of parasitic capacitance in vertical MOSFETs by spacer local oxidation,” *IEEE Trans. Electron Devices*, vol. 50, pp. 1487–1493, 2003.

[19] E.Gili, V.D.Kunz, C.H.de Groot, T.Uchino, P.Ashburn, D.C.Donaghy, S.Hall, Y.Wang, and P.L.F.Hemment, “Single, double and surround gate vertical MOSFETs with reduced parasitic capacitance,” *Solid-State Electronics*, vol. 48, pp. 511–519, 2004.

[20] H.Gossner, F.Wittmann, I.Eisele, T.Grabolla, and D.Behammer, “Vertical MOS technology with sub-0.1μm channel lengths,” *Electronics Lett.*, vol. 31, no. 16, pp. 1394–1396, August 1995.

[21] D.Behammer, M.Zeuner, T.Hackbarth, J.Herzog, M.Schafer, and T.Grabolla, “Comparison of lateral and vertical Si-MOSFETs with ultra short channels,” *Thin Solid Films*, vol. 336, pp. 313–318, 1998.

[22] F.Kaesen, C.Fink, K.G.Anil, W.Hansch, T.Doll, T.Grabolla, H.Schreiber, and I.Eisele, “Optimization of the channel doping profile of vertical sub-100 nm MOSFETs,” *Thin Solid Films*, vol. 336, pp. 309–312, 1998.

[23] C.Fink, K.G.Anil, W.Hansch, J.Schulz, and I.Eisele, “Vertical sub-100nm MOSFETs with local channel doping,” *ULSI'2000 Workshop 'Ultimate Integration of Silicon', Grenoble, France,*, pp. 59–62, January 2000.

[24] L.Risch, W.H.Krautschneider, F.Hofmann, H.Schaefer, T.Aeugle, and W.Roesner, “Vertical MOS Transistor with 70nm Channel Length,” *IEEE Trans. Electron Device*, vol. 43, no. 9, pp. 1495–1498, 1996.

[25] T.Schulz, W.Roesner, L.Risch, T.Aeugle, U.Langmann, and A.Korbel, “130nm vertical PMOS transistor with P+ poly-gate,” *ESSDERC*, pp. 168–171, 1998.

[26] D.Donaghy, S.Hall, C.H.de Groot, V.D.Kunz, and P.Ashburn, “Design of 50-nm vertical MOSFET incorporating a dielectric pocket,” *IEEE Trans. on Electron Devices*, vol. 51, pp. 158–161, 2004.

[27] H.Takato, K.Sunouchi, N.Okabe, A.Nitayama, K.Hieda, F.Horiguchi, and F.Masuoka, “Impact of surrounding gate transistor (SGT) for ultra-high-density LSI's,” *IEEE Trans. Electron Device*, vol. 38, no. 3, pp. 573–578, March 1991.

[28] C.Wang, J.P.Snyder, and J.R.Tucker, "Sub-40 nm PtSi Schottky source/drain metal-oxide-semiconductor field-effect transistors," *Appl. Phys. Lett.*, vol. 74, no. 8, pp. 1174–1176, Feb 1999.

[29] J.Larson and J.Snyder, "Schottky Barrier CMOS," *Technology overview of Spinnaker Semiconductor*, pp. 1–12, Sept 2004.

[30] C.-K.Huang, W.E.Zhang, and C.H.Yang, "Two-dimensional numerical simulation of Schottky barrier MOSFET with channel length to 10 nm," *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 842–848, Apr 1998.

[31] J.R.Tucker, C.Wang, and T.-C.Shen, "Metal silicide patterning: a new approach to silicon nanoelectronics," *Nanotechnology*, vol. 7, pp. 275–287, 1996.

[32] X.Tang, J.Katcki, E.Dubois, N.Reckinger, J.Ratajczak, G.Larrieu, P.Loumaye, O.Nisole, and V.Bayot, "Very low Schottky barrier to *n*-type silicon with PtEr-stack silicide," *Solid-State Electronics*, vol. 47, pp. 2105–2111, 2003.

[33] X.Baie, *SODAMOS Project IST-2000-27475*, http://www.iemn.univ-lille1.fr/sites_perso/baie/, 2000.

[34] R.Sasajima, K.Fujimaru, and H.Matsumura, "A metal/insulator tunnel transistor with 16 nm channel length," *Appl. Phys. Lett.*, vol. 74, pp. 3215–3217, 1999.

[35] K.Fujimaru, R.Sasajima, and H.Matsumura, "Nanoscale metal transistor control of Fowler-Nordheim tunneling currents through 16 nm insulating length," *J. Appl. Phys.*, vol. 85, pp. 6912–6916, 1999.

[36] K.Fujimaru and H.Matsumura, "Theoretical considerations of a new nanometer transistor using metal/insulator tunnel-junction," *Jap. J. Appl. Phys 1.*, vol. 35, pp. 2090–2094, 1996.

[37] K.Fukushima, R.Sasajima, K.Fujimaru, and H.Matsumura, "A novel nanoscale metal transistor fabricated by conventional photolithography," *Jap. J. Appl. Phys.*, vol. 38, pp. 7233–7236, 1999.

[38] E.S.Snow, P.M.Campbell, R.W.Rendell, F.A.Buot, D.Park, C.R.K.Marrian, and R.Magno, "A metal/oxide tunneling transistor," *Appl. Phys. Lett.*, vol. 72, pp. 3071–3073, 1998.

[39] F.A.Buot, R.W.Rendell, E.S.Snow, P.M.Campbell, D.Park, C.R.K.Marrian, and R.Magno, "Dependence of gate control on the aspect ratio in metal/metal-oxide/metal tunnel transistors," *J. Appl. Phys.*, vol. 84, pp. 1133–1139, 1998.

[40] R.W.Rendell, F.A.Buot, E.S.Snow, P.M.Campbell, D.Park, C.R.K.Marrian, and R.Magno, "Operation and design of metal-oxide tunnel transistors," *J. Appl. Phys.*, vol. 84, pp. 5021–5031, 1998.

[41] E.S.Snow, P.M.Campbell, R.W.Rendell, F.A.Buot, D.Park, C.R.K.Marrian, and R.Magno, "A metal/oxide tunneling transistor," *Semi. Sci. Tech.*, vol. 13, pp. A75–A78, 1998.

[42] B.G.Streetman, *Solid State Electronic Devices*, Prentice Hall International, Inc, 1995.

[43] Y.Taur and T.H.Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, 1998.

[44] Y.P.Tsividis, *Operation and Modelling of The MOS Transistor*, McGraw-Hill, 1987.

[45] E.H. Nicollian and J.R. Brews, *MOS(Metal Oxide Semiconductor) Physics and Technology*, John Wiley & Sons, 1982.

[46] M.Bockrath, J.Hone, A.Zettl, and P.L.McEuen, "Chemical doping of individual semiconducting carbon-nanotube ropes," *Physical Review B*, vol. 61, no. 16, 2000.

[47] P.Avouris, R.Martel, V.Derycke, and J.Appenzeller, "Carbon nanotube transistors and logic circuits," *Physica B*, vol. 323, pp. 6–14, 2002.

[48] T.Mizuno, J.Okamura, and A.Toriumi, "Experimental study of threshold voltage fluctuation due to statistical variation of channel dopant number in MOSFET's," *IEEE Trans. on Electron Devices*, vol. 41, no. 11, pp. 2216–2221, Nov 1994.

[49] A.Asenov, G.Slavcheva, A.R.Brown, J.H.Davies, and S.Saini, "Increase in the random dopand induced threshold fluctuations and lowering in sub-100nm MOSFETs due to quantum effects: A 3-D density-gradient simulation study," *IEEE Trans. on Electron Devices*, vol. 48, no. 4, pp. 722–729, APR 2001.

[50] H.Takato, K.Sunouchi, N.Okabe, A.Nitayama, K.Hieda, F.Horiguchi, and F.Masuoka, "High performance CMOS surrounding gate transistor (SGT) for ultra high density LSIs," *IEDM*, pp. 222–225, March 1988.

[51] C.P.Auth and J.D.Plummer, "Scaling theory for cylindrical, fully-depleted, surrounding-gate MOSFET's," *IEEE Trans. Electron Device*, vol. 18, no. 2, pp. 74–76, February 1997.

[52] M.Terauchi, N.Shigyo, A.Nitayama, and F.Horiguchi, "'Depletion isolation effect' of surrounding gate transistors," *IEEE Trans. Electron Device*, vol. 44, no. 12, pp. 2303–2305, December 1997.

[53] M.Yang, C.L.Chang, M.Carroll, and J.C.Sturm, "25-nm p-channel vertical MOSFET's with SiGeC sources-drains," *IEEE Trans. Electron Device Lett.*, vol. 20, no. 6, pp. 301–303, 1999.

[54] C. Fink, K.G. Anil, H. Geiger, W. Hansch, J. Schulze, T. Sulima, and I. Eisele, "Optimization of breakdown behaviour and short channel effects in MBE grown vertical MOS-devices with local channel doping," *Thin Solid Film*, vol. 369, pp. 383–386, 2000.

[55] D.Klaes, J.Moers, A.Toennesmann, S.Wickenhaeuser, L.Vescan, M.Marso, T.Grabolla, M.Grimm, and H.Lueth, "Selectively grown vertical Si MOS transistor with reduced overlap capacitances," *Thin Solid Films*, vol. 336, pp. 306–308, 1998.

[56] J.Moers, D.Klaes, A.Toennesmann, L.Vescan, S.Wickenhaeuser, T.Grabolla, M.Marso, P.Kordos, and H.Lueth, "Vertical p-MOSFETs with gate oxide deposition before selective epitaxial growth," *Solid-State Electronics*, vol. 43, pp. 529–535, 1999.

[57] D.Behammer, L.Vescan, R.Loo, J.Moers, A.Mueck, H.Lueth, and T.Grabolla, "Selectively grown vertical Si-p MOS transistor with short channel lengths," *Electronics Lett.*, vol. 32, no. 4, pp. 406–407, February 1996.

[58] R.H.Fowler and L.Nordheim, "Electron emission in intense electric fields," *Proceedings of the Royal Society of London, Series A*, vol. 119, no. 781, pp. 173–181, May 1928.

[59] M.Lenzlinger and E.H.Snow, "Fowler-Nordheim tunneling into thermally grown SiO_2," *J. Appl. Phys.*, vol. 40, no. 1, pp. 278–283, January 1969.

[60] A.A.Evtukh, V.G.Litovchenko, and A.Yu.Kizijak, "Investigation of tunneling current through thin dielectrics," *Int'l NonVolatile Memory Technology Conference*, pp. 111–114, 1998.

[61] K.Mori, A.K.Duong, and W.F.Richardson, "Sub 100 nm vertical MOSFET with threshold voltage implant," *IEEE Trans. Electron Device*, vol. 49, pp. 61, 2002.

[62] Silvaco International, *ATLAS User's Manual Device Simulation Software Volume 1*, Silvaco International Ltd, 2000.

[63] S.M.Sze, *Semiconductor Devices Physics and Technology*, John Wiley & Sons, 1985.

[64] G.Ghibaudo, R.Clerc, E.Vincent, S.Bruyere, and J.L.Autran, "Gate dielectrics for ultimate CMOS technologies-limitations and alternative solutions," *C. R. Acad. Sci. Paris*, pp. 911–927, 2000.

[65] Y.M.Li, J.W.Lee, T.W.Tang, T.S.Chao, T.F.Lei, and S.M.Sze, "Numerical simulation of quantum effects in high-k gate dielectric MOS structures using quantum mechanical models," *Computer Physics Communications*, vol. 147, pp. 214–217, 2002.

[66] W.F.A.Besling, E.Young, T.Conard, C.Zhao, R.Carter, W.Vandervorst, M.Caymax, S.de Gendt, M.Heyns, J.Maes, M.Tuominen, and S.Haukka, "Characterisation of ALCVD Al_2O_3-ZrO_2 nanolaminates, link between electrical and structural properties," *Journal of Non-Crystalline Solids*, vol. 303, pp. 123–133, 2002.

[67] S.A.Campbell, H.-S.Kim, D.C.Gilmer, B.He, T.Ma, and W.L.Gladfelter, "Titanium dioxide (TiO_2)-based gate insulators," *IBM J. RES. & DEV.*, vol. 43, no. 3, pp. 383–392, May 1999.

[68] D.R.Lamb, *Electrical Conduction Mechanisms in Thin Insulating Films*, Methuen and Co. Ltd., 1967.

[69] J.J.O'Dwyer, *The Theory of Electrical Conduction and Breakdown in Solid Dielectrics*, Clarendon Press, Oxford, 1973.

[70] U.Diebold, "The surface science of titanium dioxide," *Surface Science Reports*, vol. 48, pp. 53–229, 2003.

[71] N.Rausch and E.P.Burte, "Thin high-dielectric TiO_2 films prepared by low pressure MOCVD," *Microelectronic Engineering*, vol. 19, pp. 725–728, Sept 1992.

[72] S.-F.Chen and C.-W.Wang, "Effects of deposition temperature on the conduction mechanisms and reliability of radio frequency sputtered TiO_2 thin films," *Journal of Vacuum Science Technology B*, vol. 20, no. 1, pp. 263–270, Jan/Feb 2002.

[73] C.H.Chen, E.M.Kelder, and J.Schoonman, "Electrostatic sol-spray deposition (ESDD) and characterisation of nanostructured TiO_2 thin film," *Thin Solid Films*, vol. 342, pp. 35–41, 1999.

[74] M.Kadoshima, M.Hiratani, Y.Shimamoto, K.Torii, H.Miki, S.Kimura, and T.Nabatame, "Rutile-type TiO_2 thin film for high-k gate insulator," *Thin Solid Films*, vol. 424, pp. 224–228, 2003.

[75] D.Mardare, "Optical constants of heated-treated TiO_2 thin films," *Material Science and Engineering*, vol. 95, pp. 83–87, 2002.

[76] K.F.McCarty, "Growth regimes of the oxygen-deficient TiO_2(110) surface exposed to oxygen," *Surface Science*, vol. 543, pp. 185–206, 2003.

[77] S.Munnix and M.Schmeits, "Origin of defect states on the surface of TiO_2," *Physical Review B*, vol. 31, no. 6, pp. 3369–3371, Mar 1985.

[78] V.E.Henrich, G.Dresselhaus, and H.J.Zeiger, "Observation of two-dimensional phases associated with defect states on the surface of TiO_2," *Physical Review Letters*, vol. 36, no. 22, pp. 1335–1339, May 1976.

[79] M.Ramamoorthy, R.D.King Smith, and D.Vanderbilt, "Defects on TiO_2 surfaces," *Physical Review B*, vol. 49, no. 11, pp. 7709–7715, Mar 1994.

[80] R.H.Tait and R.V.Kasowski, "Ultraviolet photoemission and low-energy electron diffraction studies of TiO_2 (rutile)(001) and (110) surfaces," *Physical Review B*, vol. 20, no. 12, pp. 5178–5191, Dec 1979.

[81] C.Hobbs, R.Hedge, B.Maiti, H.Tseng, D.Gilmer, P.Tobin, O.Adetutu, F.Huang, D.Weddington, R.Nagabushnam, D.O'Meara, K.Reid, L.La, L.Grove, and M.Rossow,

"Sub-quarter micron CMOS process for TiN-gate MOSFETs with TiO_2 gate dielectric formed by titanium oixdation," *Symposium on VLSI Technology Digest of Technical Papers*, pp. 133–134, 1999.

[82] J.Unnam, R.Shenoy, and R.Clark, "Oxidation of commercial purity titanium," *Oxidation of Metals*, vol. 26, no. 3/4, pp. 231–252, 1986.

[83] L.I.Vergara, M.C.G.Passeggi Jr., and J.Ferron, "The role of passivation in titanium oxidation: thin films and temperature effects," *Applied Surface Science*, vol. 187, pp. 199–206, 2002.

[84] Y.L.Brama, Y.Sun, S.R.K.Dangeti, and M.Mujahid, "Response of sputtered titanium films on silicon to thermal oxidation," *Surface and Coating Technology*, vol. 195, pp. 189–197, 2005.

[85] C.-C.Ting and S.-Y.Chen, "Structural evolution and optical properties of TiO_2 thin films prepared by thermal oxidation of sputter Ti films," *J. Appl. Phys.*, vol. 88, no. 8, pp. 4628–4633, 2000.

[86] Z.Dai, H.Naramoto, K.Narumi, and S.Yamaoto, "Epitaxial growth of rutile films on Si(100) substrates by thermal oxidation of evaporated titanium films in argon flux," *J. Phys: Condens. Matter*, vol. 11, pp. 8511–8516, 1999.

[87] J.C.Tinoco, M.Estrada, and G.Romero, "Room temperature plasma oxidation mechanism to obtain ultrathin silicon oxide and titanium oxida layers," *Microelectronics Reliability*, vol. 43, pp. 895–903, 2003.

[88] M.Hiratani, M.Kadoshima, T.Hirano, Y.Shimamoto, Y.Matsui, T.Nabatame, K.Torii, and S.Kimura, "Ultra-thin titanium oxide film with a rutile-type structure," *Applied Surface Science*, vol. 207, pp. 13–19, 2003.

[89] M.D.Stamate, "On the dielectric properties of DC magnetron TiO_2 thin films," *Applied Surface Science*, vol. 218, pp. 317–322, 2003.

[90] G.K.Dalapati, S.Chatterjee, S.K.Samanta, and C.K.Maiti, "Electrical characterization of low temperature deposited TiO_2 films on strained-SiGe layers," *Applied Surface Science*, pp. 249–254, 2003.

[91] S.Chakraborty, M.K.Bera, S.Bhattacharya, and C.K.Maiti, "Current conduction mechanism in TiO_2 gate dielectrics," *Microelectronic Engineering*, vol. 81, pp. 188–193, 2005.

[92] B.C.Kang, S.B.Lee, and J.H.Boo, "Growth of TiO_2 thin films on Si(100) substrates using single molecular precursors by metal organic chemical vapor deposition," *Surface and Coatings Technology*, vol. 131, pp. 88–92, 2000.

[93] A.Sandell, M.P.Andersson, M.K.-J.Johansson, P.G.Karlsson, Y.Alfredsson, J.Schnadt, H.Siegbahn, and P.Uvdal, "Metalorganic chemical vapor deposition of antase titanium dioxide on Si: modifying the interface by pre-oxidation," *Surface Science*, vol. 530, pp. 63–70, 2003.

[94] P.Babelon, A.S.Dequiedt, H.Mostefa-Sba, S.Bourgeois, P.Sibillot, and M.Sacilotti, "SEM and XPS studies of titanium dioxide thin films grown by MOCVD," *Thin Solid Films*, vol. 322, pp. 63–67, 1998.

[95] H.Selhofer, E.Ritter, and R.Linsbod, "Properties of titanium dioxide films prepared by reactive electron-beam evaporation from various starting materials," *Applied Optics*, vol. 41, no. 4, pp. 756–762, 2002.

[96] H.K.Pulker, G.Paesold, and E.Ritter, "Refractive indices of TiO_2 films produced by reactive evaporation of various titanium-oxygen phases," *Applied Optics*, vol. 15, no. 12, pp. 2986–2991, 1976.

[97] H.Nozoye, N.Nishimiya, and H.Sato, "Reactive evaporation of titanium oxide films with controlled Ti/O ratio," *Appl. Phys. Lett.*, vol. 54, no. 3, pp. 231–232, 1989.

[98] K.Y.Ahn and L.Forbes, "Highly reliable amorphous high-k gate dielectric ZrOXNY," *United States Patent*, , no. 6767795, Jan 2002.

[99] L.Lai and E.A.Irene, "Si/SiO_2 interface roughness study using Fowler-Nordheim tunneling current oscillations," *J. Appl. Phys.*, vol. 87, no. 3, pp. 1159–1164, February 2000.

[100] I.Vaquila, Jr. M.C.G.Passeggi, and J.Ferron, "Oxidation process in titanium thin films," *Physical Review B*, vol. 55, no. 20, pp. 13925–13931, May 1997.

[101] M.Winter, "WebElements^{TM} Periodic table professional edition," *http://www.webelements.com/*.

[102] K.Holloway and R.Sinclair, "Amorphous Ti-Si alloy formed by interdiffusion of amorphous Si and crystalline Ti multilayers," *J. Appl. Phys.*, vol. 61, no. 4, pp. 1359–1364, Feb 1987.

[103] I.J.M.M.Raaijmakers, A.H.Reader, and P.H.Oosting, "The formation of an amorphous silicide by thermal reaction of sputter-deposited Ti and Si layers," *J. Appl. Phys.*, vol. 63, no. 8, pp. 2790–2795, Apr 1988.

[104] S.A.Chambers, D.M.Hill, F.Xu, and J.H.Weaver, "Silicide formation at the Ti/Si(111) Interface: diffusion parameters and behavior at elevated temperatures," *Physical Review B*, vol. 35, no. 2, pp. 634–640, Jan 1987.

[105] M.Berti, A.V.Drigo, C.Cohen, J.Siejka, G.G.Bentini, R.Nipoti, and S.Guerri, "Titanium silicide formation: effect of oxygen distribution in the metal film," *J. Appl. Phys.*, vol. 55, no. 10, pp. 3558–3565, May 1984.

[106] M.A.Taubenblatt and C.R.Helms, "Silicide and Schottky barrier formation in the Ti-Si and the Ti-SiO_x-Si Systems," *J. Appl. Phys.*, vol. 53, no. 9, pp. 6308–6315, Sept 1982.

[107] S.K.Ghandhi, *VLSI Fabrication PrinciplesSilicon and Gallium Arsenide*, Wiley Intersciences, 1994.

[108] W.R.Runyan and K.E.B.Runyan, *Semiconductor Integrated Circuit Processing Technology*, Addison-Wesley, 1990.

[109] J.R.Arthur, "Molecular beam epitaxy," *Surface Science*, vol. 500, pp. 189–217, 2002.

[110] C.-C.Ting, S.-Y.Chen, and D.-M.Liu, "Preferential growth of thin rutile TiO_2 films upon thermal oxidation of sputtered Ti films," *Thin Solid Films*, vol. 402, pp. 290–295, 2002.

[111] V.Mikhelashvili and G.Eisenstein, "Effects of annealing conditions on optical and electrical characteristics of titanium dioxide films deposited by electron beam evaporation," *J. Appl. Phys.*, vol. 89, no. 6, pp. 3256–3269, March 2001.

[112] Y.Zhu, L.Zhang, L.Wang, R.Tan, and L.Cao, "Interface diffusion and reaction between TiO_2 film photocatalyst and aluminium alloy substrate," *Surface and Interface Analysis*, vol. 32, pp. 218–223, 2001.

[113] Hewlett-Packard, *HP 4155A Semiconductor Parameter Analyzer User's Guide.*, 1998.

[114] Hewlett-Packard, *4280A 1MHz C Meter/C-V plotter: Operation and Service Manual*, 1985.

[115] Hewlett-Packard, *4192A LF Impedance Analyzer: Operation and Service Manual*, 1984.

[116] P.Barquinha, L.Pereira, H.Aguas, E.Fortunato, and R.Martins, "Influence of the deposition conditions on the properties of titanium oxide produced by R.F. magnetron sputtering," *Material Science in Semiconductor Processing*, vol. 7, pp. 243–257, 2004.

[117] A.M.Stoneham, "Why Model High-k dielectrics?," *Journal of Non-Crystalline Solids*, vol. 303, pp. 114–122, 2002.

[118] S.Berberich, P.Godignon, M.L.Locatelli, J.Millan, and H.L.Hartnagel, "High frequency CV measurements of SIC MOS capacitors," *Solid State Electronics*, vol. 42, no. 6, pp. 915–920, 1998.

[119] A.Goetzberger and J.C.Irvin, "Low-temperature hysterisis effects in metal-oxide-silicon capacitors caused by surface-state trapping," *IEEE Trans. Electron Devices*, vol. ED-15, no. 12, pp. 1009–1014, Dec 1968.

[120] M.Kuhn and E.H.Nicollian, "Nonequilibrium effects in quasi-static MOS measurements," *Journal of the Electrochemical Society: Solid State Science*, vol. 118, no. 2, pp. 370–373, Feb 1971.

[121] I.Ohkubo, H.M.Christen, P.Khalifah, S.Sathyamurthy, H.Y.Zhai, C.M.Rouleau, D.G.Mandrus, and D.H.Lowndes, "Continuous composition spread thin films of transition metal oxides by pulsed-laser deposition," *Applied Surface Science*, vol. 223, pp. 35–38, 2004.

[122] H.Chang, C.Gao, I.Takeuchi, Y.Yoo, J.Wang, P.G.Schultz, X.-D.Xiang, R.PSharma, M.Downes, and T.Venkatesan, "Combinatorial synthesis and high throughput evaluation of ferroelectric/dielectric thin-film libraries for microwave applications," *Appl. Phys. Lett.*, vol. 72, pp. 2185–2187, 1998.

[123] SPECS Scientific Instrucments Inc., "OS-Crack Thermal Gas Cracker from Oxford Scientific Atomic Hydrogen Source," *http://www.specs.com/products/MBE/Hydrogen-Cracker/Hcrack.htm.*

[124] Z.M.Wang, Q.Fang, J.-Y.Zhang, J.X.Wu, Y.Di, W.Chen, M.L.Chen, and I.W.Boyd, "Growth of titanium silicate thin films by photo-induced chemical vapor deposition," *Thin Solid Films*, vol. 453-454, pp. 167–171, 2004.

[125] A.M.Ruiz, G.Sakai, A.Cornet, K.Shimanoe, J.R.Morante, and N.Yamazoe, "Microstructure control of thermally stable TiO_2 obtained by hydrothermal process for gas sensors," *Sensors and Actuators B*, vol. 103, pp. 312–317, 2004.

[126] Topometrix, *Explorer Instrument Operation Manual*, 1985.

[127] Museum of Science, *Scanning Electron Microscope*, http://www.mos.org/sln/SEM, 1998.

[128] T.Grehl, R.Mollers, and E.Niehuis, "Low energy dual beam depth profiling: influence of sputter and analysis beam parameters on profile performance using TOF-SIMS," *Applied Surface Science*, vol. 203-204, pp. 277–280, 2003.

[129] A.Benninghoven, "Surface analysis by secondary ion mass spectrometry (SIMS)," *Surface Science*, vol. 299/300, pp. 246–260, 1994.

[130] Max Planck Institute for Solid State Research, *Interface Analysis*, http://www.fkf.mpg.de/ga/.

[131] B.D.Cullity, *Elements of X-ray Diffraction, 1st edn*, Addison-Wesley Publishing Company, Inc, USA, 1959.

[132] E.W.Nuffield, *X-ray Diffraction Methods*, Wiley, USA, 1966.

[133] H.Bracht and N.A.Stolwijk, "Diffusion in Si," *Landolt-Bornstein-Group III Condensed Matter*, vol. 33, pp. 196, Jan 1998.

[134] A.Benninghoven, F.G.Rudenauer, and H.W.Werner, *Secondary Ion Mass Spectrometry*, Wiley, Chichester, 1987.

[135] V.S.Smentkowski, "Trends in sputtering," *Progress in Surface Science*, vol. 64, pp. 1–58, 2000.

[136] C.Kittel, *Introduction to Solid State Physics, Sixth Edition*, Wiley, USA, 1986.

[137] B.-H.Hwang, "Calculation and measurement of all (002) multiple diffraction peaks from a (001) silicon wafer," *Journal of Physics D: Applied Physics*, vol. 34, pp. 2469–2474, 2001.

[138] C.Li, Z.Zheng, F.Zhang, S.Yang, H.Wang, L.Chen, F.Zhang, X.Wang, and X.Liu, "TiO_{2-x} films prepared by ion beam assisted deposition," *Nuclear Instruments and Methods in Physics Research B*, vol. 169, pp. 21–25, 2000.

[139] G.Pananakakis, G.Ghibaudo, and R.Kies, "Temperature dependence of the Fowler-Nordheim current in metal-oxide-degenerate semiconductor structures," *J. Appl. Phys.*, vol. 78, no. 4, pp. 2635–2641, Aug 1995.

[140] A.Hadjadj, G.Salace, and C.Petit, "Fowler-Nordheim conduction in polysilicon n+-oxide-siliconp structures: limit of the classical treatment in the barrier height determination," *J. Appl. Phys.*, vol. 89, no. 12, pp. 7994–8001, June 2001.

[141] M.P.Houng, Y.H.Wang, and W.J.Chang, "Current transport mechanism in trapped oxides: a generalized trap-assisted tunneling model," *J. Appl. Phys.*, vol. 86, no. 3, pp. 1488–1491, August 1999.

[142] R.Perera, A.Ikeda, R.Hattori, and Y.Kuroki, "Trap assisted leakage current conduction in thin silicon oxynitride films grown by rapid thermal oxidation combined microwave excited plasma nitridation," *Microelectronic Engineering*, vol. 65, pp. 357–370, 2003.

[143] J.Frenkel, "On pre-breakdown phenomena in insulators and electronic semiconductors," *Physical Review*, vol. 54, pp. 647–648, Dec 1938.

[144] J.R.Yeargan and H.L.Taylor, "The Poole-Frenkel effect with compensation present," *J. Appl. Phys.*, vol. 39, no. 12, pp. 5600–5604, Nov 1968.

[145] W.R.Harrell and J.Frey, "Observation of Poole-Frenkel effect saturation in SiO_2 and other insulating films," *Thin Solid Films*, vol. 352, pp. 195–204, 1999.

[146] R.M.Fleming, D.V.Lang, C.D.W.Jones, M.L.Steigerwald, D.W.Murphy, G.B.Alers, Y.-H.Wong, R.B.van Dover, J.R.Kwo, and A.M.Sergent, "Defect dominated charge transport in amorphous Ta_2O_5 thin films," *J. Appl. Phys.*, vol. 88, no. 2, pp. 850–862, July 2000.

[147] D.R.Lide (ed), *CRC Handbook of Chemistry and Physics 83rd edition*, CRC Press, 2002-2003.

[148] Silvaco International, *ATLAS User's Manual Device Simulation Software Volume 2*, Silvaco International Ltd, 2000.

[149] G.Pourtois, A.Lauwers, J.Kittl, L.Pantisano, B.Soree, S.De Gendt, W.Magnus, M.Heyns, and K.Maex, "First-principle calculations on gate/dielectric interfaces: on the origin of work function shifts," *Microelectronic Engineering*, vol. 80, pp. 272–279, 2005.

[150] L.Pantisano, P.J.Chen, V.Afanas'ev, L.-A.Ragnarsson, G.Pourtois, and G.Groeseneken, "Direct measurement of barrier height at the HfO_2/poly-Si interface," *Symposium on VLSI Technology Digest of Technical Papers*, pp. 122–123, 2004.

[151] J. J.O'Dwyer, "Current-voltage characteristics of dielectric films," *J. Appl. Phys.*, vol. 37, no. 2, pp. 599–601, Feb 1966.

[152] G.S.Oehrlein, "Oxidation temperature dependence of the dc electrical conduction characteristics and dielectric strength of thin Ta_2O_5 films on silion," *J. Appl. Phys.*, vol. 59, no. 5, pp. 1587–1595, March 1986.

[153] D.Luca and L.S.Hsu, "Structural evolution and optical properties of TiO_2 thin films prepared by thermal oxidation of PLD Ti films," *Journal of Optoelectronics and Advanced Materials*, vol. 5, no. 4, pp. 835–840, Dec 2003.

[154] H.Wong and Y.C.Cheng, "Electronic conduction mechanisms in thin oxynitride films," *J. Appl. Phys.*, vol. 70, no. 2, pp. 1078–1080, July 1991.

[155] Z.Klusek, S.Pierzgalski, and S.Datta, "Insluator-metal transition on heavily reduced TiO_2 110 surface studied by high temperature-scanning tunneling spectroscopy HT-STS," *Applied Surface Science*, vol. 221, pp. 120–128, 2004.