UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING, SCIENCE & MATHEMATICS

School of Electronics and Computer Science

Fabrication of Vertical MOSFETs with Reduced Parasitics and Incorporating a Dielectric Pocket

by

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This thesis is dedicated to

Katerina Gargaroni

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ABSTRACT

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SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

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FABRICATION OF VERTICAL MOSFETs WITH REDUCED PARASITICS AND INCORPORATING A DIELECTRIC POCKET

by Enrico Gili

The international technology roadmap for semiconductors predicts that in order to extend CMOS scaling beyond the 45nm node and to its physical limits new device architectures will have to be introduced. Vertical MOSFETs are a potential solution, since their channel length is independent from the device layout. CMOS compatible vertical MOSFETs, which do not require epitaxy or challenging processing, have been developed to simplify the integration of these devices in a mainstream planar process. A fully CMOS compatible, self-aligned second oxidation process, called spacer or fillet local oxidation (FILOX), is characterized, which reduces the gate/drain and the gate/source overlap capacitances of vertical MOSFETs. Furthermore, a novel dielectric pocket vertical MOSFET process is proposed and fabricated, which provides shallow source/drain junctions and hence gives better control of short channel effects.

Single, double and surround gate FILOX vertical nMOSFETs with reduced gate overlap capacitance have been fabricated. In these devices, a 40 nm thick FILOX oxide covers the horizontal silicon area, while the vertical sidewalls of the active pillar only contain the 3.3 nm thick gate oxide. Single and double gate transistors have been been successfully fabricated and characterized. The threshold voltage roll-off of surround gate vertical MOSFETs with channel length ranging between 90 nm and 140 nm has been investigated, showing that the FILOX process must be carefully tuned in order to minimize the short channel effects. The transfer characteristics of long channel FILOX vertical MOSFETs in drain on top and drain on bottom measurement configurations are found to be symmetric in on-state operation. On the other hand, the off-state drain leakage currents of the devices are found to be asymmetric when the source and the drain are interchanged, with gate induced drain leakage (GIDL) being higher in the drain on bottom configuration and body leakage being higher in the drain on top configuration.

Surround gate vertical nMOSFETs with shallow drain junctions and dielectric pockets have been fabricated using a novel approach. This process is fully compatible with conventional planar CMOS technology, does not require epitaxial growth and allows sub-100 nm vertical MOSFETs with shallow drain junctions to be fabricated without requiring advanced photolithography. Dielectric pocket vertical nMOSFETs with channel length down to 70 nm have been produced and display good electrical characteristics. The drain of the devices is connected to the channel by a polysilicon spacer with a minimum thickness of about 20 nm. During annealing, the drain dopants outdiffuse into the single-crystal silicon body, yielding a drain junction depth into the pillar sidewall of less than 50 nm. In a separate diffusion experiment, the benefits of a polysilicon drain are highlighted for the fabrication of both p- and n-type vertical MOSFETs. Polysilicon drains are found to yield shallow junctions in the single-crystal silicon substrate, and to reduce the transient enhanced diffusion in the underlying source.

Contents

Abstract i

Contents ii

List of figures vi

List of tables x

Declaration of authorship xi

Acknowledgements xii

List of symbols xiii

List of acronyms xvii

1 Introduction 1
- 1.1 Challenges related to state of the art CMOS scaling 1
- 1.2 Advanced double and surround gate CMOS technologies 2
- 1.3 Vertical MOSFETs 4

2 Theory of MOSFETs 10
- 2.1 Long-channel MOSFETs 10
  - 2.1.1 Threshold voltage of a long-channel nMOSFET 10
  - 2.1.2 Drain current in long-channel nMOSFETs 12
- 2.2 Short channel effect in MOSFETs 15
  - 2.2.1 Charge sharing model of the short channel effect 15
  - 2.2.2 Analytical expression of the threshold voltage in short channel MOSFETs 16
  - 2.2.3 Subthreshold slope of long channel and short channel MOSFETs 17
- 2.3 Drain leakage current in MOSFETs 18
  - 2.3.1 Body leakage current 20
  - 2.3.2 GIDL 21

3 Fabrication and characterization of single, double and surround gate, short channel vertical MOSFETs with FILOX: initial results 26
- 3.1 Introduction 26
- 3.2 Fabrication of vertical MOSFETs with FILOX 27
- 3.3 Experimental procedure 31
  - 3.3.1 Electrical characteristics 31

3.3.2 SIMS profiles . . . 32
3.3.3 SEM cross-sections . . . 32
3.4 Overlap capacitance reduction in vertical MOSFETs with FILOX . . 33
3.4.1 FILOX structural characterization . . . 33
3.4.2 Evaluation of capacitance reduction due to the FILOX process 34
3.5 Characterization of single, double and surround gate vertical MOSFETs 36
3.5.1 Structural characterization of the gate spacers removal process 36
3.5.2 Layout of the single, double and surround gate vertical MOSFETs fabricated with the FILOX process . . . 37
3.5.3 Electrical characteristics of single, double and surround gate vertical MOSFETs . . . 40
3.6 Electrical characterization of short channel FILOX vertical MOSFETs . . . 41
3.6.1 Extraction of the channel length of short channel, surround gate vertical MOSFETs . . . 41
3.6.2 Electrical characterization of the short-channel effect in surround gate vertical MOSFETs . . . 44
3.7 Discussion . . . 46
3.8 Summary . . . 50

4 Asymmetric Gate Induced Drain Leakage and Body Leakage in FILOX Vertical MOSFETs 51
4.1 Introduction . . . 51
4.2 Experimental procedure . . . 52
4.3 Results . . . 54
4.4 Discussion . . . 58
4.4.1 Leakage mechanisms . . . 58
4.4.2 Asymmetric body leakage . . . 60
4.4.3 Asymmetric gate induced drain leakage . . . 61
4.5 Summary . . . 64

5 Dielectric pocket vertical MOSFET process development 66
5.1 Introduction . . . 66
5.2 The concept of dielectric pocket in a vertical MOSFET . . . 66
5.3 Approaches to dielectric pocket vertical MOSFET fabrication . . . 69
5.3.1 Epitaxial channel approach . . . 69
5.3.2 Polysilicon spacer approach . . . 70
5.4 Fabrication process of CMOS compatible dielectric pocket vertical MOSFETs with the polysilicon spacer approach . . . 71
5.4.1 Drain deposition and patterning . . . 71
5.4.2 Formation of the drain sidewall spacers . . . 73
5.4.3 Source/drain ion implantation and gate stack formation . . . 75
5.4.4 Back end processing . . . 76
5.4.5 Process splits fabricated . . . 77
5.5 Summary . . . 78

6 Electrical and structural characterization of dielectric pocket vertical MOSFETs 79
6.1 Introduction . . . 79
6.2 Experimental procedure . . . 79
6.2.1 Characterization of the doping profiles . . . 79
6.2.2 SEM cross-sections . . . 82
6.2.3 Electrical characteristics . . . 82
6.2.4 Device simulation . . . 84
6.3 Doping profiles . . . 84
6.3.1 SIMS profiles of source and drain junctions . . . 84
6.3.2 Resistivity measurements . . . 86
6.4 SEM cross-sections of fabricated transistors . . . 87
6.5 Reproducibility of the fabrication process . . . 91
6.6 Effect of measurement configuration (drain on top and drain on bottom) on electrical characteristics . . . 94
6.7 Effect of process splits on transistor characteristics . . . 96
6.7.1 Effect of process splits on transfer characteristics . . . 96
6.7.2 Effect of process splits on output characteristics . . . 99
6.8 Effect of process splits on diode characteristics . . . 102
6.9 Discussion . . . 104
6.10 Summary . . . 110

7 Investigation of the role of a polysilicon drain on source and drain diffusion in short channel vertical MOSFETs 112
7.1 Introduction . . . 112
7.2 Experimental procedure . . . 113
7.2.1 Fabrication of arsenic-doped test structures with a polysilicon drain . . . 113
7.2.2 Fabrication of boron-doped test structures with a polysilicon drain . . . 115
7.2.3 Doping profile characterization . . . 116
7.3 Results . . . 117
7.3.1 Doping profiles of arsenic-doped structures . . . 117
7.3.2 Boron-doped samples . . . 119
7.4 Discussion . . . 119
7.5 Summary . . . 122

8 Conclusions 123

9 Suggestions for future work 126

A Batch listings 128
A.1 Batch listing for fabrication of FILOX vertical MOSFETs . . . 129
A.2 Batch listing for fabrication of dielectric pocket vertical MOSFETs . 132
A.3 Batch listing for fabrication of test structures to assess the role of a polysilicon drain on arsenic diffusion in vertical nMOSFETs. . . . 136
A.4 Batch listing for fabrication of test structures to assess the role of a polysilicon drain on boron diffusion in vertical pMOSFETs. . . . 137

B Simulation script files **138**
B.1 GIDL device simulations 138
B.2 Dielectric pocket device simulations 140

C Mask description **143**

D List of Publications **146**
D.1 Journal papers 146
D.2 Conference papers 147

References **148**

List of Figures

1.1 Operating principle of advanced double and surround gate CMOS technologies . . . 3
1.2 Simplified process flow of the FILOX process . . . 7

2.1 Cross-section and band diagram of a long-channel nMOSFET . . . 11
2.2 Cross-section of a MOSFET showing the depletion region configuration used in the charge sharing model of the short channel effect . . . 15
2.3 Components of the drain leakage current in a nMOSFET . . . 19
2.4 Cross-section of the drain/gate overlap region of a MOSFET in off-state 21
2.5 Band diagram of the drain-gate overlap region of a MOSFET . . . 22
2.6 Region of integration of the band-to-band tunneling rate in the drain-gate overlap region of a MOSFET . . . 24
2.7 Leakage current of a p^+-n gated diode at temperatures ranging from 50K to 400K . . . 25

3.1 Schematic cross-sections of CMOS compatible vertical MOSFETs . . 27
3.2 Schematic layout of the mask set used for fabrication of surround gate FILOX vertical MOSFETs . . . 28
3.3 Fabrication process of FILOX vertical MOSFETs: FILOX formation . 28
3.4 Fabrication process of FILOX vertical MOSFETs: gate formation . . 29
3.5 Fabrication process of FILOX vertical MOSFETs: partial removal of the gate spacers . . . 30
3.6 Layout of the Gate spacers removal mask used to fabricate surround, single and double gate vertical MOSFETs . . . 30
3.7 Schematic cross sections of the surround gate and of the single gate vertical MOSFETs fabricated . . . 30
3.8 SEM cross-section of the active area of a surround gate vertical nMOSFET fabricated with the FILOX process . . . 33
3.9 Cross-section and layout of the simplified planar nMOSFET model used in the overlap capacitance calculations . . . 34
3.10 Cross-section and layout of the conventional vertical nMOSFET model used in the overlap capacitance calculations . . . 34
3.11 Cross-section and layout of the FILOX vertical nMOSFET model used in the overlap capacitance calculations . . . 35
3.12 Gate/source and gate/drain overlap capacitance of the simplified MOSFET models . . . 35
3.13 SEM cross-section of the active area of a vertical MOSFET showing the pillar sidewall of the device after the gate spacers removal process 36

3.14 Schematic 3D view and top view of a surround gate vertical MOSFET 37
3.15 Schematic 3D view and top view of a double gate vertical MOSFET . 38
3.16 Schematic 3D view and top view of a single gate vertical MOSFET . 39
3.17 Transfer characteristics of a surround gate vertical nMOSFET 40
3.18 Transfer characteristics of a double gate vertical nMOSFET 40
3.19 Transfer characteristics of a single gate vertical nMOSFET 41
3.20 SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 90 nm channel length 42
3.21 SIMS profile of the drain/body junction of a FILOX vertical MOSFET 42
3.22 SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 100 nm channel length 43
3.23 SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 120 nm channel length 44
3.24 SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 140 nm channel length 44
3.25 Transfer characteristic of surround gate vertical MOSFETs with different channel lengths 45
3.26 Threshold voltage of surround gate FILOX vertical nMOS transistors as a function of the channel length 45
3.27 On-state drain current of surround gate vertical nMOS transistors as a function of the channel length 46
3.28 On-state drain current as a function of the channel width of single, double and surround gate FILOX vertical nMOSFETs 47
3.29 Threshold voltage of long-channel nMOSFETs plotted as a function of the gate oxide thickness 48

4.1 Schematic cross-section of a surround gate FILOX vertical MOSFET 52
4.2 SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 220 nm channel length. 52
4.3 Measurement configurations used for the electrical characterization of the vertical MOSFETs 53
4.4 Measured transfer characteristics of a typical surround gate vertical MOSFET in drain on top and drain on bottom configurations 54
4.5 Current-voltage characteristics of the top and bottom body-drain p-n junctions measured on the large area, ungated diodes 55
4.6 Gated diode and diode electrical characteristics measured at temperatures ranging between -50°C and 200°C 56
4.7 Reciprocal temperature dependence of the gated diode and diode characteristics 57
4.8 Schematic cross-section of the drain region of a MOSFET showing GIDL and body leakage 58
4.9 Schematic cross-section of the pillar sidewall of a vertical MOSFET, including a representation of the GIDL mechanism 59
4.10 SIMS profiles and capacitance-voltage characteristics of the top and bottom body-drain p-n junctions of a FILOX vertical MOSFET . . . 60
4.11 Model of the gated diodes implemented for the simulation of the GIDL 61
4.12 Comparison between the simulated gated diode characteristics and the experimental gated diode characteristics 62

4.13 Simulated total electric field and band to band tunneling generation rate 63

5.1 Schematic cross-sections of a dielectric pocket vertical nMOSFET . . 67
5.2 Schematic cross-sections of a conventional CMOS compatible vertical nMOSFET 68
5.3 Schematic cross-section of the active pillar of a dielectric pocket vertical MOSFET fabricated with the epitaxial channel approach 69
5.4 Process overview of the polysilicon spacer approach to fabrication of dielectric pocket vertical MOSFETs. 70
5.5 Mask layout of the fabricated dielectric pocket vertical MOSFETs. . . 72
5.6 Fabrication process of dielectric pocket vertical MOSFETs: deposition and patterning of the drain and of the dielectric pocket 72
5.7 Fabrication process of dielectric pocket vertical MOSFETs: deposition of the thin amorphous silicon layer 73
5.8 Fabrication process of dielectric pocket vertical MOSFETs: pillar dry etch 74
5.9 Process development of the pillar dry etch of dielectric pocket vertical MOSFETs 75
5.10 Fabrication process of dielectric pocket vertical MOSFETs: gate stack and back-end 76

6.1 Schematic representation of the devices analyzed by SIMS. 80
6.2 Schematic representation of the Van der Pauw structure used to measure sheet resistivity. 81
6.3 Measurement configurations of dielectric pocket vertical MOSFETs . 82
6.4 Wafer map of a device wafer with indicated the cells 83
6.5 SIMS doping profiles of the drain/body and source/body junctions of dielectric pocket vertical MOSFETs 85
6.6 SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 130 nm channel length 87
6.7 SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 150 nm channel length 88
6.8 SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 70 nm channel length 88
6.9 SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 90 nm channel length 89
6.10 SEM cross-section of the active area of a control vertical MOSFET with 250 nm channel length and without dielectric pocket 89
6.11 SEM cross-sections of the active area of dielectric pocket vertical MOSFETs showing the gate track 90
6.12 Transfer characteristics of surround gate, dielectric pocket vertical MOSFETs from process split 1 in table 5.2 at $V_D = 1V$ 91
6.13 Transfer characteristics of surround gate vertical MOSFETs from process split 2 in table 5.2 at $V_D = 1V$ 92
6.14 Transfer characteristics of surround gate vertical MOSFETs from process split 3 in table 5.2 at $V_D = 1V$ 92
6.15 Transfer characteristics of surround gate vertical MOSFETs from process split 4 in table 5.2 at $V_D = 1V$ 93

6.16 Transfer characteristics of surround gate vertical MOSFETs from process split 6 in table 5.2 at $V_D = 1V$ 93
6.17 Comparison of the threshold voltage (V_t) of devices from different process splits 94
6.18 On-state drain current of devices from different process splits 95
6.19 Maximum gate transconductance of devices from different process splits 96
6.20 Logarithmic transfer characteristics of dielectric pocket vertical MOSFETs and of a control device without dielectric pocket 97
6.21 Comparison of the transfer characteristics of vertical MOSFETs with drain bias increasing from 0.1V to 3V 98
6.22 Linear output characteristics of dielectric pocket vertical MOSFETs and of a control device at $V_G = 3V$ 100
6.23 Output characteristics of a dielectric pocket vertical MOSFET from process split 1 (table 5.2) in logarithmic scale 101
6.24 Output characteristics of a control device from process split 6 (table 5.2) in logarithmic scale 101
6.25 Shift from the origin of the $I_D(V_D)$ characteristics of devices with different channel length and different polySi spacer thickness 102
6.26 Current-voltage diode characteristics in logarithmic scale of vertical MOSFETs from different process splits 102
6.27 Comparison of the diode current dependence on reverse and forward bias of devices from different process splits 103
6.28 Schematic representation of the conduction mechanism of dielectric pocket vertical MOSFETs 107
6.29 Planar model of a dielectric pocket vertical MOSFET used to simulate the effect of a thin oxide layer between the drain and body 108
6.30 Simulated output characteristics based on the planar model of a dielectric pocket vertical MOSFET shown in figure 6.29 109

7.1 Schematic cross-section of the active pillar of a dielectric pocket vertical MOSFET 112
7.2 Schematic cross-sections of the arsenic-doped test structures fabricated to investigate the role of a polysilicon drain 114
7.3 Schematic cross-sections of the boron-doped test structures fabricated to investigate the role of a polysilicon drain 115
7.4 Example of extraction of dopant diffusion (or outdiffusion) and channel length 117
7.5 SIMS profiles of arsenic-doped test structures annealed with different thermal cycles. 118
7.6 SIMS profiles of boron-doped test structures annealed with different thermal cycles 119
7.7 Diffusion and outdiffusion of dopants in arsenic-doped test structures with and without polysilicon drain 120
7.8 Boron diffusion/outdiffusion in test structures with and without polysilicon drain after different anneal cycles 121

C.1 Layout of the mask set used for the fabrication of the vertical MOSFETs144

List of Tables

1.1 Current best estimates of introduction for specific technology requirements from the International Technology Roadmap for Semiconductors 1

3.1 Values of gate/source and gate/drain overlap capacitance calculated based on simplified MOSFET models 36
3.2 Comparison of single, double and surround gate FILOX vertical MOSFETs with state of the art vertical and planar MOSFETs 49

5.1 Advantages of a dielectric pocket vertical MOSFET in comparison with a conventional CMOS compatible vertical MOSFET 68
5.2 Process splits for fabrication of dielectric pocket vertical MOSFETs with the novel polysilicon spacer approach 77

6.1 Sheet resistance, junction depth and resistivity of a dielectric pocket vertical MOSFET 86
6.2 Structural parameters of dielectric pocket vertical MOSFETs and of a control device 90
6.3 Comparison of dielectric pocket vertical MOSFETs with state of the art vertical and planar MOSFETs 110

7.1 Process splits fabricated to investigate the role of a polysilicon drain on arsenic diffusion in vertical MOSFETs 114
7.2 Process splits fabricated to investigate the role of a polysilicon drain on boron diffusion in vertical MOSFETs 116
7.3 Channel length range of the structures fabricated to investigate the role of a polysilicon drain on arsenic diffusion in vertical MOSFETs . 118

C.1 Layout description of the devices included in the mask layout of the fabricated vertical MOSFETs 145
C.2 Layout description of the test structures included in the mask layout of the fabricated vertical MOSFETs 145

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List of Symbols

English symbols

A_{BBT}	-	effective area of band to band tunneling [m^2]
A_{diode}	-	area of a p-n junction [m^2]
C_{diode}	-	junction capacitance of a p-n junction [F m^{-2}]
C_{ox}	-	oxide capacitance per unit of area [F m^{-2}]
D_n	-	electron diffusion coefficient [$m^2 s^{-1}$]
E	-	energy [eV]
E_c	-	energy level of the conduction band [eV]
E_f	-	Fermi energy level [eV]
E_{Fn}	-	electrons quasi Fermi level [eV]
E_{Fp}	-	holes quasi Fermi level [eV]
E_g	-	semiconductor band gap = 1.12eV in Si
E_i	-	Fermi level in intrinsic silicon [eV]
E_v	-	energy level of the valence band [eV]
G_{BBT}	-	band to band tunneling generation rate [m^{-3} s^{-1}]
g_m	-	gate transconductance [A/V]
I_B	-	body current [A]
I_D	-	drain current [A]
I_{diode}	-	diode current of a p-n junction [A]
I_{DS}	-	drain-source current [A]
I_{Dsat}	-	saturation drain current [A]
I_G	-	gate current [A]
I_{off}	-	off-state drain current of a MOSFET [A]
I_{on}	-	on-state drain current of a MOSFET [A]
I_S	-	source current [A]
J_{BBT}	-	band to band tunneling current density [A m^{-2}]
J_{gen}	-	generation current density in a p-n junction depletion region [A m^{-2}]
J_n	-	electron current density [A m^{-2}]
J_S	-	reverse bias diffusion current density of a p-n diode [A m^{-2}]

k	-	Boltzmann constant [J K^{-1}]
L	-	channel length [m]
m	-	body-effect coefficient
n	-	electron concentration in silicon [m^{-3}]
N	-	doping concentration [m^{-3}]
N_A	-	acceptor doping concentration [m^{-3}]
N_C	-	effective densities of states in the Si conduction band [m^{-3}]
N_D	-	donor doping concentration [m^{-3}]
n_i	-	intrinsic carrier concentration [m^{-3}]
n_n	-	electron concentration in n-type silicon [m^{-3}]
n_p	-	electron concentration in p-type silicon [m^{-3}]
n_S	-	electron concentration at the oxide/silicon interface in nMOSFETs [m^{-3}]
N_V	-	effective densities of states in the Si valence band [m^{-3}]
p	-	hole concentration in silicon [m^{-3}]
P	-	band-to-band tunneling rate [m^{-3} s^{-1}]
p_n	-	hole concentration in n-type silicon [m^{-3}]
p_p	-	hole concentration in p-type silicon [m^{-3}]
q	-	electron charge [C]
Q_B	-	depletion charge per unit area in the body of a MOSFET [C cm^{-2}]
Q_{BTOT}	-	depletion charge per unit of channel width in the body of a MOSFET [C cm^{-1}]
Q_i	-	inversion charge per unit area [C cm^{-2}]
Q_{TOT}	-	total charge per unit area in the body of a MOSFET [C cm^{-2}]
s	-	second
S	-	subthreshold swing or inverse subthreshold slope [V]
S_L	-	inverse subthreshold slope of a long-channel MOSFET [V]
S_S	-	inverse subthreshold slope of a short-channel MOSFET [V]
T	-	temperature [K]
t_{a-Si}	-	thickness of an amorphous silicon layer [m]
t_{ox}	-	oxide thickness [m]
t_{spacer}	-	spacer thickness [m]
V_B	-	body voltage [V]
V_c	-	channel voltage [V]
V_D	-	drain voltage [V]
V_{DB}	-	drain/body voltage [V]
V_{DD}	-	high power supply voltage in an integrated circuit [V]
V_{diode}	-	bias applied to a p-n junction [V]
V_{DS}	-	drain/source voltage [V]

$V_{DS,sat}$	-	drain/source voltage at saturation [V]
V_{FB}	-	flat band voltage [V]
V_G	-	gate voltage [V]
V_{GB}	-	gate/body voltage [V]
V_{GD}	-	gate/drain voltage [V]
V_{GS}	-	gate/source voltage [V]
V_{on}	-	linearly extrapolated threshold voltage [V]
V_{ox}	-	oxide voltage [V]
$V_{ox,S}$	-	oxide voltage drop of a short-channel MOSFET [V]
V_R	-	reverse bias across a p-n junction [V]
V_S	-	source voltage [V]
V_{SB}	-	source/body voltage [V]
V_t	-	threshold voltage [V]
$V_{t,L}$	-	threshold voltage of a long-channel MOSFET [V]
$V_{t,S}$	-	threshold voltage of a short-channel MOSFET [V]
w	-	depletion region width [m]
W	-	channel width of a MOSFET [m]
$w_{max,L}$	-	maximum gate depletion region width of a long-channel MOSFET [m]
$w_{max,S}$	-	maximum gate depletion region width of a short-channel MOSFET [m]
w_n	-	depletion region width in an n-type region [m]
w_p	-	depletion region width in a p-type region [m]

Greek symbols

ε	-	electric field [V m^{-1}]
ε_{max}	-	maximum electric field in a p-n junction [V m^{-1}]
ε_{ox}	-	electric field in silicon dioxide [V m^{-1}]
ε_{Si}	-	electric field in silicon [V m^{-1}]
ϵ_0	-	vacuum permittivity [F/m]
ϵ_{ox}	-	dielectric constant of silicon dioxide = $\epsilon_{rox}\epsilon_0$ [F/m]
ϵ_{rox}	-	relative dielectric constant of silicon dioxide = 3.9
ϵ_{rSi}	-	relative dielectric constant of silicon = 12
ϵ_{Si}	-	dielectric constant of silicon = $\epsilon_{rSi}\epsilon_0$ [F/m]
μ_n	-	electron mobility [m^2 V^{-1} s^{-1}]
μ_{neff}	-	effective electron mobility [m^2 V^{-1} s^{-1}]
ρ	-	resistivity [Ω cm]
ρ_d	-	charge density [cm^{-3}]
ρ_{sh}	-	sheet resistance [Ω/square]
τ_n	-	electron lifetime [s]
Φ_F	-	Fermi potential [V]
ψ	-	potential [V]
ψ_{bi}	-	built-in voltage of a pn-junction [V]
ψ_S	-	surface potential [V]

List of Acronyms

a-Si - amorphous silicon
BPSG - Boron Phosphorous Silicate Glass

CMOS - Complementary Metal Oxide Semiconductor

DC - Direct Current
DIBL - Drain Induced Barrier Lowering effect
DP - Dielectric Pocket
DRAM - Dynamic Random Access Memory

FD - Fully Depleted
FEG-SEM - Field Emission Gun Scanning Electron Microscope
FILOX - Spacer or Fillet Local Oxidation
FinFET - Fin Field Effect Transistor

GAA MOSFET - Gate All Around Metal Oxide Semiconductor Field Effect Transistor
GIDL - Gate Induced Drain Leakage current

HDD - Highly Doped Drain

ITRS - International Technology Roadmap for Semiconductors

LOCOS - Localized Oxidation of Silicon
LPCVD - Low Pressure Chemical Vapor Deposition
LSTP MOSFET - Low Standby Power Metal Oxide Semiconductor Field Effect Transistor
LTO - Low Temperature Oxide

MOS - Metal Oxide Semiconductor
MOSFET - Metal Oxide Semiconductor Field Effect Transistor

NAND - logical NAND gate
Nitride - Silicon Nitride (Si_3N_4) insulator
nMOSFET - n-channel Metal Oxide Semiconductor Field Effect Transistor
NOR - logical NOR gate

PD - Partially Depleted
p-i-n - p-type silicon / intrinsic silicon / n-type silicon junction
p-n junction - p-type silicon / n-type silicon junction
pMOSFET - p-channel Metal Oxide Semiconductor Field Effect Transistor
polySi - polycrystalline silicon

RF - Radio Frequency
RTA - Rapid Thermal Annealing

SCE - Short Channel Effect
SEM - Scanning Electron Microscope
SIMS - Secondary Ion Mass Spectroscopy
SOI - Silicon On Insulator
STI - Shallow Trench Isolation

TEM - Transmission Electron Microscope

UTVC MOSFET - Ultra Thin Vertical Channel Metal Oxide Semiconductor Field Effect Transistor

VRG MOSFET - Vertical Replacement Gate vertical Metal Oxide Semiconductor Field Effect Transistor

Chapter 1

Introduction

1.1 Challenges related to state of the art CMOS scaling

Near-term years

Year of production	2006	2007	2008	2010	2012
Half Pitch [nm]	78	68	59	45	36
Printed Gate Length [nm]	48	42	38	30	24
Physical Gate Length [nm]	28	25	22	18	14
Equivalent Oxide Thickness [nm]	1.1	1.1	0.9	0.6	0.5
Power Supply Voltage (V_{DD}) [V]	1.1	1.1	1	1	0.9
Threshold voltage (V_t) [V]	0.17	0.16	0.16	0.15	0.15
nMOS drive current (I_{on}) [$\mu A/\mu m$]	1130	1200	1570	2050	2300

Table 1.1: Current best estimates of introduction for specific technology requirements from the International Technology Roadmap for Semiconductors (ITRS) 2005 [1]; the data presented are relative to a high-performance planar bulk logic technology and are presented in the Process Integration, Devices and Structures chapter of the ITRS; V_t is measured at $V_D = V_{DD}$; I_{on} is measured at $V_G = V_D = V_{DD}$.

As shown in table 1.1, from the International Technology Roadmap for Semiconductors [1], in 2006 CMOS scaling has reached the 78nm technology node. This is identified in table 1.1 by the half pitch of a high performance logic MOS technology, characterized by a 28 nm physical gate length, 1.1 nm equivalent gate oxide thickness, a threshold voltage of 0.17 V and a drive current of 1130 $\mu A/\mu m$. In order to keep scaling the dimensions of the devices and at the same time maintain the historic annual increase of intrinsic speed of high-performance Micro Processor Units (17% annual increase for digital applications), the industry will require by 2012 a 14 nm long channel, a 0.5 nm equivalent gate oxide thickness and a threshold voltage as low as 0.15 V.

In order to achieve these requirements, several front-end technological challenges will have to be overcome. First, the leakage currents and in particular the gate leakage due to exceedingly thin gate oxides will need to be controlled in order to limit the amount of power dissipated by the devices. Second, gate electrode depletion will have to be suppressed in order to allow device scaling. Third, the short channel effects of MOSFETs with ultra-short channels will have to be controlled by increasing the body doping, which will lead to reduced mobility and enhanced drain/body leakage. Fourth, excessive statistical variations of the threshold voltage due to fluctuation of the number of channel dopants will have to be avoided to achieve satisfactory device reliability.

Several solutions have been proposed in order to extend planar bulk technology as far as possible on the roadmap. In particular, the introduction of new materials and of ultra-thin-body, fully depleted SOI will address most of the technological issues. The introduction of high-k gate dielectrics will allow enhanced drive currents without exceeding the gate leakage requirements. Metal gate electrodes will prevent gate electrode depletion and will allow scaling of the equivalent gate oxide thickness. Carrier mobility in the channel will be improved by introducing local or globally induced strain in the channel of bulk or SOI MOSFETs [2]. Eventually, new channel materials like Ge, III-V compound semiconductors [3] or carbon nanotubes may be used to enhance channel transport. Finally, ultra-thin-body, fully depleted SOI MOSFETs with threshold voltage controlled by the workfunction of metal gate electrodes [4] will be introduced. These devices will suppress short-channel effects and leakage currents thanks to a silicon channel less than 10 nm thick on a SOI substrate. Moreover, they will allow very low channel doping without short-channel effect enhancement. Alternatively, the Silicon-On-Nothing structure [5] will combine the advantages of bulk and SOI MOSFETs without requiring an SOI substrate.

1.2 Advanced double and surround gate CMOS technologies

In order to extend CMOS scaling to its physical limits while maintaining the current rate of performance improvement, devices with a structure different from the conventional planar MOSFET will eventually have to be introduced. A promising concept in this direction is that of double or surround gate MOS structures (Figure 1.1). This is a class of devices based on the concept of adding additional gate electrodes around the body of a MOSFET. This approach has several advantages in comparison with conventional planar MOS technology. First, if perfect coupling between front and back gate is achieved in devices with a thin body, short channel effects can be suppressed and devices featuring an ideal subthreshold swing of 60mV/decade can

be fabricated. Second, due to the improved electrostatic coupling between gate and channel the body doping concentration of double and surround gate MOSFETs can be reduced without generating short channel effects, thus improving channel mobility. Third, the channel width per unit area is at least doubled, thus obtaining increased drive current per unit area of the transistors without requiring aggressive device scaling.

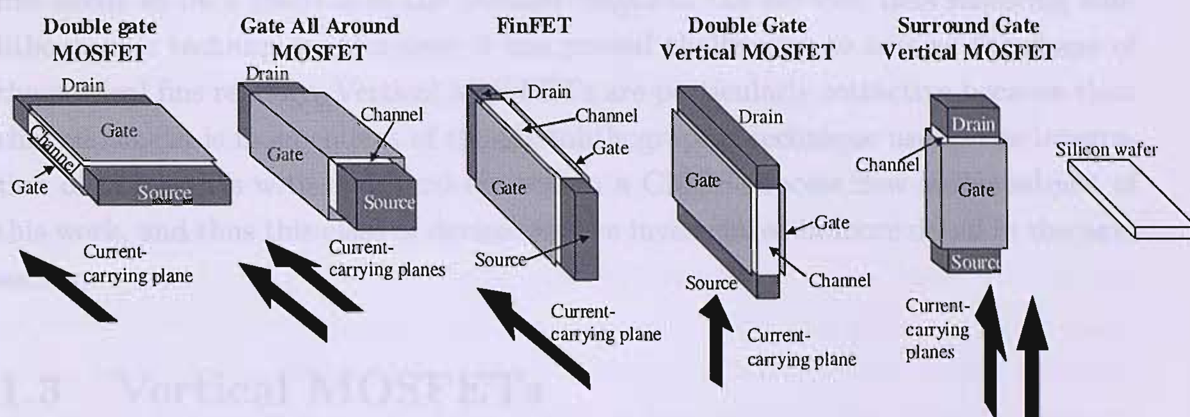

Figure 1.1: Operating principle of advanced double and surround gate CMOS technologies. The current-currying planes, relative to the orientation of the silicon wafer shown on the right of the image, are shown for each of the different structures.

Double and surround gate MOSFETs can be grouped in three classes, as shown in figure 1.1: planar double gate/Gate All Around (GAA) MOSFETs, FinFETs and double/surround gate vertical MOSFETs. In planar double gate MOSFETs a second gate is added underneath the body of the device. Both the current-carrying plane and the current flow are parallel to the wafer surface. GAA MOSFETs are based on the same concept, but the channel current can flow on planes perpendicular to the wafer surface as the gate wraps all around the body of the device. FinFETs are fabricated on SOI substrates with a process very similar to that used to fabricate SOI MOSFETs. Standalone silicon fins are etched on a SOI wafer and gate electrodes are patterned to define the channel of the devices. In FinFETs the current-carrying plane is perpendicular and the current flow parallel to the wafer surface. Finally, Double and Surround Gate Vertical MOSFETs are based on the use of non-lithographic methods to define the channel length. In these devices both the current-carrying planes and the current flow are perpendicular to the wafer surface.

Double and surround gate technologies are good candidates to succeed to planar CMOS technology. Until now their implementation has been hindered mainly by process integration considerations, as these structures generally require basic modifications of the standard CMOS process flow that has been so successful in the past. Both planar double gate [6–11] and GAA MOSFETs [12–15] require very complex fabrication processes. This limits their integration in a standard CMOS process flow.

In particular, the realization of planar double gate MOSFETs is difficult because, to obtain good performance, the top and bottom gates must be aligned. On the other hand, FinFETs seem the most likely candidates to extend the CMOS roadmap because of their remarkable CMOS compatibility [16–21]. This devices require SOI substrates, which are now increasingly being used in VLSI technology. One drawback is that to achieve good gate/channel electrostatic coupling, the width of the silicon fins needs to be a fraction of the channel length of the devices, thus requiring sub-lithographic techniques. Moreover it has proved challenging to control the shape of the vertical fins reliably. Vertical MOSFETs are particularly attractive because their channel length is independent of the photolithographic technique used. The integration of MOSFETs with a vertical channel in a CMOS process flow is the subject of this work, and thus this class of devices will be investigated in more detail in the next section.

1.3 Vertical MOSFETs

Vertical MOSFETs are different from the other double and surround gate CMOS technologies presented in figure 1.1 because the channel current flows perpendicularly to the silicon substrate. This has four main implications that make this technology particularly attractive for several post-planar CMOS applications. First, the channel length of the vertical MOSFETs is defined by non-lithographic methods, such as ion implantation or epitaxial deposition. All the other device concepts shown in figure 1.1 rely on advanced photolithography to define sub-100 nm long channels, while ultra-short channel vertical MOSFETs can be produced with relaxed lithography rules and, as a consequence, at a low cost. Second, in contrast to planar double gate and GAA MOSFETs, vertical MOS transistors are naturally predisposed to the fabrication of double or surround gate structures. This allows a remarkable increase of channel width per unit area in comparison with planar devices without requiring an exceedingly complex fabrication process. This feature of vertical MOSFETs is attractive for RF and power applications. Third, the gate length of the vertical MOSFETs is decoupled from the packing density. This allows low leakage, long channel devices to be integrated in a microprocessor or memory unit without reducing its packing density. This feature is very attractive for applications where low leakage and high packing density are key requirements, such as Dynamic Random Access Memory (DRAM). Fourth, vertical MOSFETs built on the sidewalls of pillars or ridges less than 50 nm wide exhibit an enhanced electrostatic coupling of gate and channel. This leads to suppression of the short channel effects of the devices, with a mechanism similar to that in ultra-thin-body SOI MOSFETs or FinFETs.

Although vertical MOSFETs have several advantages on conventional planar CMOS technology, their fabrication process requires considerable changes compared with a

mainstream CMOS process. This has slowed down considerably their introduction in the microelectronics industry. Five main processing challenges can be identified. First, vertical MOSFETs can only be fabricated with one channel length per wafer. For this reason, they need to be integrated with planar transistors in order to satisfy the range of requirements of a solid state circuit for analog or digital applications. Second, the precise control of the channel length of the devices is generally difficult by ion implantation though much easier by epitaxy. On the other hand, epitaxial growth is a low throughput, high cost process and has low CMOS compatibility. Third, vertical MOSFETs have additional sources of parasitic capacitance compared with planar transistors. In particular, gate/drain and gate/source parasitic capacitance is a serious concern as the source and drain electrodes of the vertical MOSFETs cannot be easily self-aligned to the gate as in planar MOSFETs. Fourth, the source and/or drain of the vertical MOSFETs usually extend across the whole width of the active ridge or pillar. The source and/or drain junction depth of the devices is equal to the width of the pillar or ridge. For this reason, it is difficult to control the short channel effects of devices with sub-100 nm channel length. The fifth challenge related to vertical MOSFET fabrication is the elimination of damage introduced in the sidewall of the active pillar or ridge when this is patterned by dry etch. The sidewall damage can be incorporated into the gate oxide of the device, affecting the quality of the channel/gate oxide interface.

In order to address the drawbacks associated with vertical MOSFET fabrication, a variety of devices and structures have been developed in the past. These can be divided in two groups. The first class of vertical MOSFETs is composed of devices with channel length defined by epitaxial deposition of a source/body/drain stack. The second group is composed of vertical MOSFETs with channel length determined by ion implantation of source and drain electrodes into a previously patterned silicon pillar.

Epitaxial deposition allows fabrication of ultra-short-channel devices, because the thickness of the body of the vertical MOSFETs can be controlled with precision during epitaxial growth [22–25]. Unfortunately, epitaxial deposition is expensive and has low throughput. These devices are difficult to integrate in a CMOS process flow because it is difficult to deposit both n-doped and p-doped channels on the same silicon wafer. Moreover, epitaxial vertical MOSFETs suffer of punchthrough and floating-body effects. In order to improve device performance, several advanced structures featuring a delta doped body [26–30], selective epitaxial growth of the active pillar [31–34], a p-i-n diode [35] or multiple vertical channels [36] have been proposed in the literature. The Vertical Replacement Gate (VRG) MOSFET [37–40] process is probably the most promising of these concepts. The gate overlap capacitance of the VRG MOSFET is suppressed by creating self-aligned source and drain regions outdiffused from deposited layers. A natural evolution of vertical MOSFETs based on epitaxy

has led to devices that exploit the strain introduced in source, drain or channel by SiGe layers in order to improve their electrical performance. Heterojunction vertical MOSFETs incorporating SiGe layers in the source and/or drain electrodes have been developed in order to suppress short-channel effects (in pMOSFETs) [41, 42], suppress the floating body effect [43, 44] or increase the breakdown drain current [44, 45]. A different research direction has led to the introduction of SiGe layers in the vertical channel of the devices to enhance mobility. The vertical structure allows integration of strained Si and SiGe layers to improve channel mobility without generating misfit dislocations [46, 47].

As discussed above, the main drawback of the epitaxial approach to vertical MOSFET fabrication is its low compatibility with mainstream CMOS planar technology. For this reason, in recent years research has focused on a different class of vertical MOSFETs. These devices are epitaxy-free and rely on ion implantation to define the source and drain electrodes on the top and on the bottom of a pillar/ridge etched in a silicon substrate. This has allowed the fabrication process to be considerably simplified and fully CMOS compatible devices to be developed [48–51]. Many of these device concepts feature a body contact which is successful in suppressing the floating body effect. One of the main challenges associated with CMOS compatible vertical MOSFETs is the development of strategies to control the short channel effects. In fact it is very challenging to fabricate devices with shallow drain junctions or to incorporate pockets next to source and drain as in planar MOSFETs. Parasitic gate overlap capacitance is another concern, as it may compromise device performance in a circuit environment. In order to suppress the short-channel effects, it has been proposed to reduce the width of the active silicon ridge of double gate MOSFETs to achieve fully depleted operation. This would provide enhanced electrostatic coupling of gate and channel of the devices. Different approaches have been proposed to fabricate double gate vertical MOSFETs with sub-50nm ridge thickness, such as advanced lithography techniques [13, 48, 52–56] or selective wet etching of the sidewalls of thin silicon ridges [57–60]. Alternatively, Liu et al. have proposed the deposition of an ultrathin vertical channel (UTVC) on the sidewall of an oxide pillar [61–63]. Nevertheless, both these approaches require challenging processing and/or advanced photolithography. In an attempt to reduce the gate overlap capacitance of CMOS compatible vertical MOSFETs, Jurckzak et al. proposed the growth of a thicker oxide layer between gate and source/drain by amorphizing the horizontal silicon surface with a high dose and low energy ion implantation, which selectively increases the oxidation rate on the planar surfaces [64]. However this process only yields a small increase in oxide thickness.

Vertical MOSFETs have been successfully used in the past for memory applications. They are particularly suitable for this purpose because of the specific requirements of the access transistors of DRAM cells, such as low leakage currents, low power

consumption and high integration density. A long channel vertical access transistor can be integrated on top of a storage capacitor without requiring any additional space compared to a short channel transistor. This has allowed the integration density of DRAM cells to be improved without compromising their performance [65–69].

In this work, two novel technological advances are investigated to provide solutions to the two main drawbacks of CMOS compatible vertical MOSFETs discussed above: parasitic gate overlap capacitance and deep drain junctions. A fully CMOS compatible, self-aligned second oxidation process to suppress gate overlap capacitance, called spacer or fillet local oxidation (FILOX), is investigated. The FILOX process was developed by V. D. Kunz, a previous Ph.D. student at Southampton University [70–77]. In a separate experiment, the incorporation of a dielectric pocket between drain and body of surround gate vertical MOSFETs is proposed and demonstrated to fabricate devices with shallow drain junctions [78–80]. The two strategies proposed are fully compatible with each other and with the conventional planar CMOS technology. They provide a viable solution for the integration of ultra-short channel, parasitics-free vertical MOSFETs within a conventional planar CMOS process.

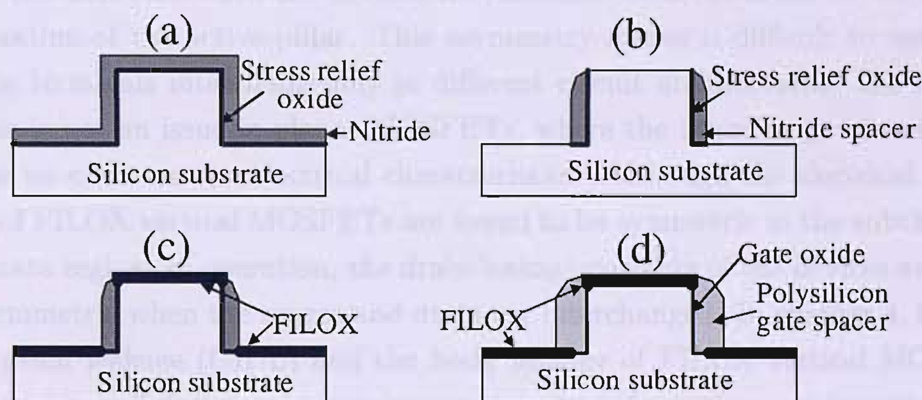

Figure 1.2: Simplified process flow of the FILOX process, after V. D. Kunz [70]. (a) Stress relief oxide and nitride deposition. (b) Nitride and oxide anisotropic etch to leave nitride spacers on the sidewalls of the pillar. (c) Growth of thick oxide on all planar surfaces. (d) Wet etch of nitride spacers and stress relief oxide, gate oxidation, gate polysilicon deposition and patterning.

Figure 1.2 shows a simplified process flow of the FILOX process, proposed and demonstrated by V. D. Kunz [70]. After etching the active pillar of the vertical MOSFET, a thin stress relief oxide is grown over the structure. A nitride layer is deposited over the pillar by chemical vapor deposition, as shown in figure 1.2(a). First the nitride layer and then the stress relief oxide are anisotropically etched to expose the silicon substrate on the horizontal surfaces, while leaving nitride fillets on the sidewalls of the pillar, as shown in figure 1.2(b). A subsequent local oxidation will result in the growth of an oxide layer on all exposed planar surfaces, except on the protected vertical channel area (figure 1.2(c)). After the removal of the nitride

fillets by wet etch, the grown oxide covers the active area, while the vertical sidewalls of the pillar only contain the thinner original stress relief oxide which doubles up as sacrificial oxide. After removal of the stress relief oxide by wet etch and growth of a thin gate oxide, the extra oxide in the trench and on top of the pillar will reduce the parasitic capacitance by a factor equal to the ratio of the gate oxide and the FILOX oxide. The final structure of the vertical MOSFET is shown in figure 1.2(d).

For convenience, the FILOX fabrication process has been described in detail in chapter 3. In order to complete the preliminary electrical characterization results presented by V. D. Kunz in his Ph.D. Thesis [70], in this work surround gate FILOX vertical MOSFETs with channel length down to 90 nm are structurally and electrically characterized. A comparison of gate overlap capacitance of a FILOX vertical MOSFET, a conventional vertical MOSFET and a planar MOSFET allows to estimate the gate overlap capacitance reduction obtained with the FILOX process. This is followed by electrical characterization of the single, double and surround gate vertical MOSFETs fabricated.

A further potential disadvantage of the vertical MOSFETs is the inherent asymmetry of the structure when the devices are measured with the drain on the top and on the bottom of the active pillar. This asymmetry makes it difficult to use source and drain terminals interchangeably in different circuit architectures. On the contrary, this is not an issue in planar MOSFETs, where the interchange of source and drain has no effect on the electrical characteristics. Although the electrical characteristics of FILOX vertical MOSFETs are found to be symmetric in the subthreshold and on-state regions of operation, the drain leakage currents of the devices are found to be asymmetric when the source and drain are interchanged. In chapter 4, the gate induced drain leakage (GIDL) and the body leakage of FILOX vertical MOSFETs in drain-on-top and drain-on-bottom measurement configurations are investigated to identify the effect of the asymmetric source/drain geometry on the off-state drain leakage of the devices.

A novel approach to the fabrication of dielectric pocket vertical MOSFETs, named the polysilicon spacer approach, is described in chapters 5 and 6. This novel, CMOS compatible process allows vertical MOSFETs with shallow drain junctions to be fabricated. This is achieved without adding complexity to the fabrication process and without requiring challenging photolithography. Surround gate dielectric pocket vertical MOSFETs with channel lengths down to 70 nm are structurally and electrically characterized. SIMS analysis and SEM cross-sections are used to estimate a drain junction depth into the pillar sidewall of less than 50 nm. Thus the novel dielectric pocket process is effective in controlling channel length and drain junction depth of vertical MOSFETs with sub-100 nm channel length.

The dielectric pocket process relies on drain dopants out-diffused from the polysilicon drain into the single-crystal silicon body of a vertical MOSFET to form shallow

drain junctions. In chapter 7, diffusion experiments are carried out to optimize the drain junction depth of dielectric pocket vertical MOSFETs. Moreover, the role of the polysilicon drain on the diffusion of the underlying source is investigated. The presence of a polysilicon drain is found to be effective in reducing source diffusion and hence facilitates the creation of n- and p-channel dielectric pocket vertical MOSFETs with very short channel lengths.

Chapter 2

Theory of MOSFETs

2.1 Long-channel MOSFETs

2.1.1 Threshold voltage of a long-channel nMOSFET

A long-channel MOSFET is a transistor with a channel long enough so that the source and drain depletion regions widths within the body are negligible compared with the channel length. The influence of the source and drain electric fields on the body can be neglected so that the transistor behaves like a MOS capacitor with two electrodes at the opposite ends of the channel. The following approximations apply to a long-channel nMOSFET:

- Gradual channel approximation: the variation of the electric field in the direction parallel to the gate oxide (y direction) is much less than the variation in the direction perpendicular to the gate oxide (x direction); this allows the Poisson equation to be reduced to a 1-dimensional form in the x direction (see figure 2.1).

- The hole current component of the drain current of a nMOSFET is negligible compared to the electron current component.

- The generation and recombination currents are negligible in the channel region.

- Charge-sheet approximation: the inversion charge is located at the Si/SiO_2 interface, so that it doesn't give rise to any potential drop within the silicon substrate.

Figure 2.1(a) shows the cross-section of a long-channel MOSFET. Figures 2.1(b) and (c) show the band diagrams of the device for $V_G > V_t$ along a cross-section perpendicular to the gate oxide in the channel region next to the source, with $V_B = 0$ V and $V_B < 0$ V respectively.

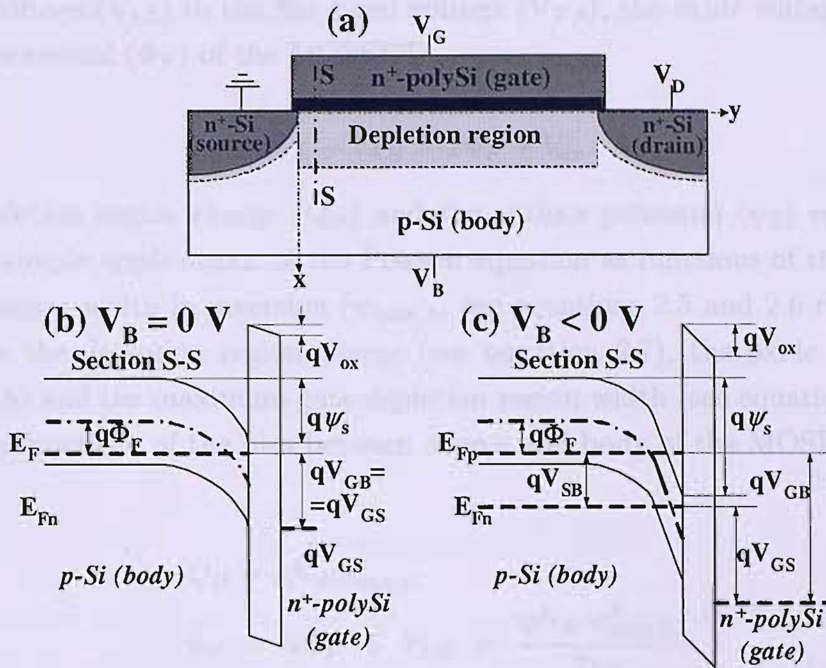

Figure 2.1: (a) Cross-section of a long-channel nMOSFET. (b) Band diagram of a long-channel nMOSFET with body grounded; cross-section perpendicular to the gate oxide (in the x direction) in the channel region next to the source. (c) Band diagram with $V_B < 0$ V.

$$n = N_C e^{-\frac{E_C - E_{Fn}}{kT}} \quad (2.1)$$

$$p = N_V e^{-\frac{E_{Fp} - E_V}{kT}} \quad (2.2)$$

Equations 2.1 and 2.2 show the relations between Fermi levels and carrier concentration in doped silicon. The channel of an nMOSFET is in strong inversion when the electron concentration at the silicon surface is equal to the hole concentration in the body ($n_S \approx p_p$). In the neutral region of the body the hole concentration is approximately equal to the acceptor doping concentration ($p_p \approx N_A$). At the oxide/silicon interface, at the onset of strong inversion, $n_S \approx p_p \approx N_A$. The Fermi level energy at the onset of inversion can be calculated from equations 2.1 and 2.2. The relationship between the electron Fermi level and the hole Fermi level in the channel of a nMOSFET in strong inversion can be expressed by equation 2.3.

$$E_C - E_{Fn} = E_{Fp} - E_V \quad (2.3)$$

At the onset of inversion ($V_G = V_{t,L}$), the inversion charge per unit area in the channel (Q_i) is negligible. Only the depletion region charge (Q_B) contributes to the total charge per unit area in the body (Q_{TOT}). Thus $Q_i \approx 0$ and $Q_{TOT} = Q_i + Q_B \approx Q_B$. In analogy with figure 2.1, equation 2.4 can be formulated, which relates the

threshold voltage ($V_{t,L}$) to the flat band voltage (V_{FB}), the oxide voltage (V_{ox}) and the Fermi potential (Φ_F) of the MOSFET.

$$V_{t,L} - V_{FB} = 2\Phi_F + V_{ox} \tag{2.4}$$

The depletion region charge (Q_B) and the surface potential (ψ_S) can be calculated from simple applications of the Poisson equation as functions of the maximum depletion region width in inversion ($w_{max,L}$; see equations 2.5 and 2.6 respectively). This allows the depletion region charge (see equation 2.7), the oxide voltage (see equation 2.8) and the maximum gate depletion region width (see equation 2.9) to be obtained as functions of the bias between source and body of the MOSFET (V_{SB}).

$$Q_B = qN_A w_{\max,L} \tag{2.5}$$

$$\psi_S = 2\Phi_F + V_{SB} = \frac{qN_A\, w_{max,L}^2}{2\epsilon_{Si}} \tag{2.6}$$

$$Q_B = -\sqrt{2\epsilon_{Si} q N_A \left(2\Phi_F + V_{SB}\right)} \tag{2.7}$$

$$V_{ox} = -\frac{Q_B}{C_{ox}} = \frac{\sqrt{2\epsilon_{Si} q N_A \left(2\Phi_F + V_{SB}\right)}}{C_{ox}} \tag{2.8}$$

$$w_{max,L} = \sqrt{\frac{2\epsilon_{Si}\left(2\Phi_F + V_{SB}\right)}{qN_A}} \tag{2.9}$$

The threshold voltage of a long-channel nMOSFET can be obtained from equations 2.4 and 2.8.

$$V_{t,L} = V_{FB} + 2\Phi_F + \frac{\sqrt{2\epsilon_{Si} q N_A \left(2\Phi_F + V_{SB}\right)}}{C_{ox}} \tag{2.10}$$

2.1.2 Drain current in long-channel nMOSFETs

As shown in equation 2.11, the total channel current density in a nMOSFET is the sum of the drift and diffusion currents in the y direction, parallel to the gate oxide (see figure 2.1).

$$J_n = qn\left(x,y\right)\mu_n \varepsilon_y\left(y\right) - qD_n \frac{\partial n\left(x,y\right)}{\partial y} \tag{2.11}$$

In a MOSFET in strong inversion the diffusion current can be neglected and the electric field in the y direction (ε_y) is given by the derivative of the surface potential in the y direction. If the body is grounded (V_{SB} = 0 V), the surface potential of a long-channel MOSFET at a distance y from the source end of the channel (see figure 2.1) can be written as $\psi_S = 2\Phi_F + V_c(y)$. The channel voltage V_c(y) varies from 0 V at the source end to V_{DS} at the drain end of the channel. With these

assumptions equation 2.11 reduces to:

$$J_n = -qn\left(x,y\right)\mu_n \frac{dV_c\left(y\right)}{dy} \tag{2.12}$$

The charge-sheet approximation allows equation 2.12 to be simplified by assuming that all the inversion layer charge is located at the silicon/oxide interface. In this condition, the inversion charge depends only on the y coordinate. Furthermore, the mobility can be considered constant by averaging it along the channel length, thus obtaining an effective electron mobility μ_{neff}. Equation 2.13 shows the expression of the drain current per unit of channel width as a function of the inversion charge per unit area (Q_i).

$$\frac{I_{DS}}{W} = -\mu_{neff} Q_i\left(y\right)\frac{dV_c\left(y\right)}{dy} \tag{2.13}$$

The depletion charge per unit area (Q_B(y)) can be obtained with a simple application of the Poisson equation, in analogy with equation 2.7 (see equation2.14).

$$Q_B(y) = -\sqrt{2\epsilon_{Si} q N_A\left(2\Phi_F + V_c(y)\right)} \tag{2.14}$$

Another application of the Poisson equation on a cross-section perpendicular to the gate oxide yields equation 2.15, where Q_{TOT} is the total charge per unit area in the body of the MOSFET.

$$V_G - V_{FB} = \psi_S - \frac{Q_{TOT}}{C_{ox}}\ , \tag{2.15}$$

In equation 2.15, Q_{TOT} is the sum of the inversion and depletion charge. From equations 2.14 and 2.15 the expression of the inversion charge as a function of the channel potential V_c(y) can be obtained (equation 2.17).

$$\begin{aligned} Q_i\left(V\right) &= Q_{TOT} - Q_B && (2.16)\\ &= -C_{ox}\left(V_G - V_{FB} - 2\Phi_F - V_c\right) + \sqrt{2\epsilon_{Si} q N_A\left(2\Phi_F + V_c\right)} && (2.17)\end{aligned}$$

Q_i can be integrated as a function of the channel potential, as shown in equation 2.18.

$$\frac{I_{DS}}{W}\int_0^L dy = -\mu_{neff}\int_0^{V_{DS}} Q_i\left(V_c\right) dV_c \tag{2.18}$$

By carrying out the integration, the expression of the drain current of a long channel MOSFET is obtained as shown in equation 2.19.

$$\frac{I_{DS}}{W} = \frac{\mu_{neff} C_{ox}}{L} \left\{ \left(V_G - V_{FB} - 2\Phi_F - \frac{V_{DS}}{2} \right) V_{DS} - \frac{2\sqrt{2q\epsilon_{Si}N_A}}{3C_{ox}} \left[(2\Phi_F + V_{DS})^{\frac{3}{2}} - (2\Phi_F)^{\frac{3}{2}} \right] \right\} \tag{2.19}$$

In order to remove the power 3/2 in equation 2.19, it can be simplified with a Taylor expansion around $V_{DS} = 0$ V. From equations 2.9, 2.10 and 2.19 it is possible to obtain a simple expression of the drain current. In the linear (or triode) region, at low drain bias, only the first-order term of the Taylor expansion is taken in account (equation 2.20). On the other hand, for higher V_{DS} values it is necessary to take in account the second-order term as well (equation 2.21).

$$\frac{I_{DS}}{W} = \frac{\mu_{neff} C_{ox}}{L} (V_G - V_{t,L}) V_{DS} \tag{2.20}$$

$$\frac{I_{DS}}{W} = \frac{\mu_{neff} C_{ox}}{L} \left[(V_G - V_{t,L}) V_{DS} - \frac{m}{2} V_{DS}^2 \right] \tag{2.21}$$

$$m = \left(1 + \frac{t_{ox}}{\epsilon_{ox}} \frac{\epsilon_{Si}}{w_{max,L}} \right) \tag{2.22}$$

The coefficient m in equation 2.22 is the body-effect coefficient. The value of m is proportional to the gate oxide thickness and inversely proportional to the maximum gate depletion layer width in the body of the device. The value of m is inversely proportional to the electrostatic coupling between the gate and the body and thus its value increases with the threshold voltage of the MOSFET.

The I_D (V_{DS}) relationship in equation 2.21 follows a parabolic curve up to a maximum saturation value (I_{Dsat}), at $V_{DS} = V_{DS,sat}$ (equation 2.23). This is is called pinch-off point. For this drain voltage the channel disappears at its drain end. Beyond the pinch-off point the saturation drain current is constant (equation 2.24) because the voltage at the drain end of the channel is pinned to $V_{DS,sat}$ even if V_{DS} increases.

$$V_{DS,sat} = \frac{(V_G - V_{t,L})}{m} \tag{2.23}$$

$$\frac{I_{Dsat}}{W} = \frac{\mu_{neff} C_{ox}}{L} \frac{(V_G - V_{t,L})^2}{2m} \tag{2.24}$$

2.2 Short channel effect in MOSFETs

2.2.1 Charge sharing model of the short channel effect

Figure 2.2 shows a MOS transistor and its depletion regions. The gate induced depletion region of a long channel MOSFET has constant width, because the source and drain depletion region widths are negligible compared to the channel length of the device. The gate induced depletion region charge per unit of channel width of a long channel MOSFET is labeled "$Q_{BTOT,L}$" in figure 2.2. On the contrary, if the channel is short, this approximation is not valid. In this situation the model detailed in section 2.1.1 is not accurate and the threshold voltage has a value lower than the one obtained from equation 2.10. This phenomenon is called short channel effect.

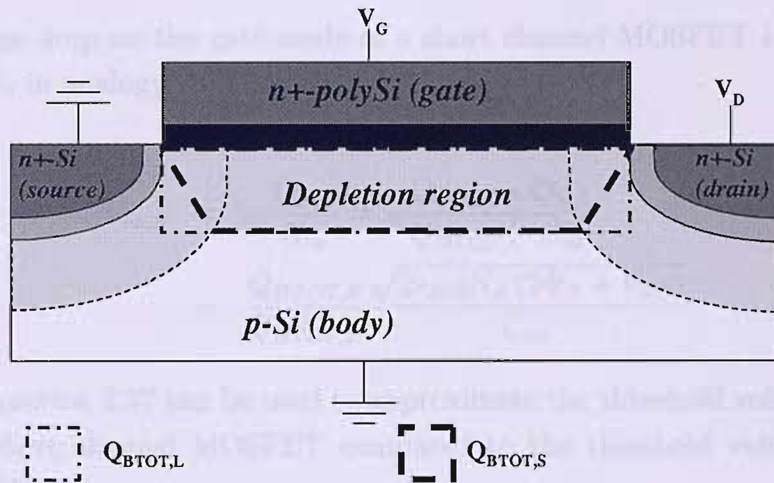

Figure 2.2: Cross-section of a MOSFET showing the depletion region configuration used in the charge sharing model of the short channel effect; $Q_{BTOT,L}$ = gate induced depletion region charge per unit of channel width of a long channel MOSFET; $Q_{BTOT,S}$ = effective gate induced depletion region charge per unit of channel width of a short channel MOSFET.

An intuitive representation of the relationship between the channel length and the short channel effect in MOS transistors is provided by the charge sharing model [81]. Figure 2.2 shows the cross-section of a short channel MOSFET. The charge sharing model is based on the assumption that in short channel MOSFETs the gate induced body depletion region width is not constant throughout the channel. The body depletion region charge per unit of channel width controlled by the gate is labeled "$Q_{BTOT,S}$" in figure 2.2. The depletion region is nonuniform because at the extremities of the channel it is controlled by the source and drain rather than by the gate. If the effect of the source and drain fields is neglected, the depletion region is uniform and the charge per unit of channel width is equal to the long-channel case ($Q_{BTOT,L}$). In this case, the depletion charge per unit area is $Q_{B,L} = Q_{BTOT,L}/L$ (equivalent to the model of a long channel MOSFET). The charge sharing model

is based on the assumption that a short-channel MOSFET can be modeled with a uniform gate depletion region such as that of a long channel MOSFET, but with effective depletion region charge per unit of channel width equal to $Q_{BTOT,S}$. Consequently, if the short channel effect is taken in consideration but the gate induced body depletion region is considered uniform, the depletion charge per unit area of the device is $Q_{B,S} = Q_{BTOT,S}/L$. As shown in figure 2.2, the only difference between the two situations is the shape of the gate induced depletion region, and the channel length (L) does not change. For this reason, $Q_{B,L}/Q_{B,S} = Q_{BTOT,L}/Q_{BTOT,S}$, and the threshold voltage of the short-channel device ($V_{t,S}$) can be obtained from equation 2.25, in analogy with equation 2.4.

$$V_{t,S} - V_{FB} = 2\Phi_F + V_{ox,S} \tag{2.25}$$

The voltage drop on the gate oxide of a short channel MOSFET is expressed by equation 2.26, in analogy with equation 2.8.

$$\begin{aligned} V_{ox,S} &= -\frac{Q_{B,S}}{C_{ox}} = -\frac{Q_{BTOT,S}}{Q_{BTOT,L}}\frac{Q_{B,L}}{C_{ox}} \\ &= \frac{Q_{BTOT,S}}{Q_{BTOT,L}}\frac{\sqrt{2\epsilon_{Si}qN_A\left(2\Phi_F + V_{SB}\right)}}{C_{ox}} \end{aligned} \tag{2.26}$$

Finally, equation 2.27 can be used to approximate the threshold voltage reduction (ΔV_t) of a short channel MOSFET compared to the threshold voltage of a long channel MOSFET.

$$\Delta V_t = V_{t,L} - V_{t,S} = \left(1 - \frac{Q_{BTOT,S}}{Q_{BTOT,L}}\right)\frac{\sqrt{2\epsilon_{Si}qN_A\left(2\Phi_F + V_{SB}\right)}}{C_{ox}} \tag{2.27}$$

2.2.2 Analytical expression of the threshold voltage in short channel MOSFETs

The calculation of an accurate expression of the threshold voltage of a short channel MOSFET is a very complex mathematical problem involving the solution of an irregular 2-D boundary-value problem. To obtain accurate results it is advisable to run numerical simulations on a finite-element program. Nevertheless Taur et al. [82] propose an approximate analytical solution, based on a two-dimensional form of Poisson's equation (equation 2.28). The solution proposed assumes a uniform body doping concentration concentration.

$$\frac{\partial^2\psi\left(x,y\right)}{\partial x^2} + \frac{\partial^2\psi\left(x,y\right)}{\partial y^2} = \frac{q\rho_d\left(x,y\right)}{\epsilon_{Si}} \tag{2.28}$$

To eliminate the electric field discontinuity across the silicon-oxide boundary the

oxide is replaced by an equivalent region with the same dielectric constant as silicon, but with a thickness equal to 3 times the gate oxide thickness ($3t_{ox}$). This is approximately the ration of the dielectric constants of silicon and silicon dioxide ($\epsilon_{Si}/\epsilon_{ox} \approx 3$). With this approximation, equation 2.28 is solved by assuming a simplified set of boundary conditions (see Taur et al. [82], Appendix A6). In a short channel MOSFET the point of the channel region in which the surface potential is highest determines the maximum depletion region width of the device and the threshold voltage. Due to the interaction of the surface potential with the source/drain electric fields the short channel maximum depletion region ($w_{max,S}$) is wider that its long-channel counterpart ($w_{max,L}$; see equation 2.9). In order to to find a solution for $w_{max,S}$, equation 2.29 [82] needs to be solved iteratively.

$$\frac{w_{\max,S}}{w_{\max,L}} = 1 + 4\left(\frac{w_{\max,L}}{w_{\max,S} + 3t_{ox}}\right) \times \times \left(\frac{\sqrt{\left(\frac{E_g}{2q} + \Phi_F + V_{SB}\right)\left(\frac{E_g}{2q} + \Phi_F + V_{SB} + V_{DS}\right)}}{2\Phi_F + V_{SB}}\right) e^{-\frac{\pi L}{2\left(w_{\max,S}+3t_{ox}\right)}} \tag{2.29}$$

Once the maximum depletion region width of the short channel MOSFET has been calculated, an accurate expression of the threshold voltage reduction of the device can be obtained (equation 2.30).

$$\Delta V_t = \frac{24t_{ox}}{w_{\max,S}} \sqrt{\left(\frac{E_g}{2q} + \Phi_F + V_{SB}\right)\left(\frac{E_g}{2q} + \Phi_F + V_{SB} + V_{DS}\right)} \; e^{\frac{-\pi L}{2\left(w_{\max,S}+3t_{ox}\right)}} \tag{2.30}$$

2.2.3 Subthreshold slope of long channel and short channel MOSFETs

The inverse subthreshold slope or subthreshold swing of a MOSFET is defined as the inverse slope of the logarithm of the drain current in the subthreshold region of operation (equation 2.31).

$$S = \left(\frac{d\left(\log_{10} I_{DS}\right)}{dV_G}\right)^{-1} \tag{2.31}$$

In the subthreshold region of operation the body of a MOSFET is in depletion and its channel is not inverted. The surface potential, in a long-channel transistor, is approximately constant throughout the channel and thus is a function of V_G only. As a result the lateral electric field (parallel to the gate oxide) is small and the drift

current is negligible. Once V_{DS} becomes larger than a few kT/q, there is a difference in charge density between the source and the drain end of the channel. This gives rise to a diffusion-dominated current which increases exponentially with the surface potential and the gate voltage of the MOSFET. The subthreshold drain current of a MOSFET can be expressed by equation 2.32.

$$I_{DS} = f\left(V_{DS}\right) e^{\frac{q(V_G - V_t)}{kT} \frac{1}{1+\frac{\epsilon_{Si} t_{ox}}{\epsilon_{ox} w_{\max,L}}}} \tag{2.32}$$

The subthreshold slope of a long channel MOSFET can be calculated from equation 2.32, as shown in equation 2.33.

$$S = 2.3\frac{kT}{q}\left(1 + \frac{\epsilon_{Si} t_{ox}}{\epsilon_{ox} w_{\max,L}}\right) \approx 2.3\frac{kT}{q}\left(1 + \frac{3t_{ox}}{w_{\max,L}}\right) \tag{2.33}$$

On the other hand, an accurate expression of the subthreshold slope of a short channel MOSFET is proposed by Taur et al. [82] (equation 2.34), based on the analytical model described in section 2.2.2.

$$S \approx 2.3\frac{kT}{q}\left(1 + \frac{3t_{ox}}{w_{\max,L}}\right)\left(1 + \frac{11t_{ox}}{w_{\max,S}} \quad e^{-\frac{\pi L}{2\left(w_{\max,S}+3t_{ox}\right)}}\right) \tag{2.34}$$

2.3 Drain leakage current in MOSFETs

The channel length of the MOS transistors is continuously scaled down in order to improve the performance and reduce the dimensions of the devices. In the meantime, in order to minimize the subthreshold slope while maximizing the drive current of the MOSFETs, the gate oxide thickness is scaled to the minimum value permitted by oxide reliability constraints. On the contrary, the body doping has to be increased to keep Poisson's equation invariant with respect to scaling [82] and suppress short channel effects and DIBL (Drain Induced Barrier Lowering). However, there are several factors that do not scale with the physical dimensions of the devices. One of these non-scaling factors is drain leakage current. This is composed of four main contributions (figure 2.3):

- Gate leakage due to carriers tunneling through the gate oxide (I_1).
- Subthreshold conduction between source and drain (I_2).
- Body leakage current due to the reverse-biased drain/body junction (I_3).
- Surface leakage current or GIDL (I_4; GIDL stands for Gate Induced Drain Leakage).

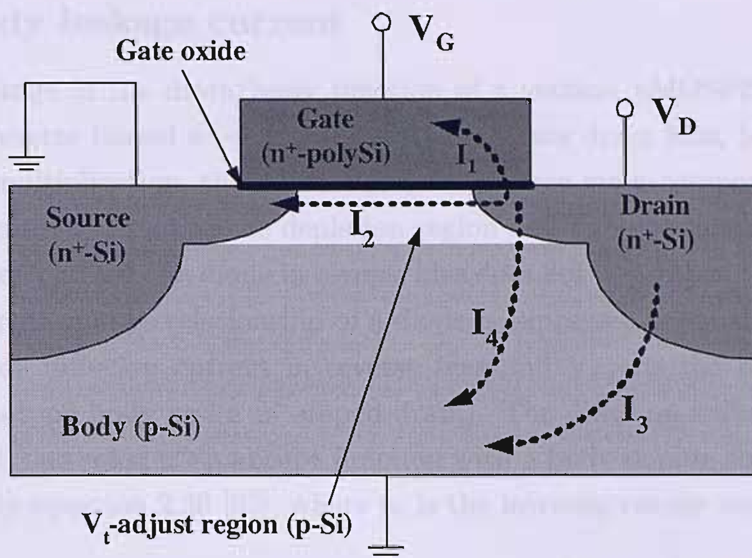

Figure 2.3: Cross-section of a nMOSFET showing the four main components of the drain leakage current: I_1 = gate leakage, I_2 = subthreshold conduction, I_3 = body leakage, I_4 = GIDL.

Gate leakage current depends on the gate oxide thickness and on the oxide quality. For thick gate oxides, the main mechanism involved in gate leakage is Fowler-Nordheim tunneling. On the other hand, when the gate oxide is scaled down in short channel devices, direct tunneling and hot-carrier injection become the predominant phenomena [82].

Subthreshold conduction is the transistor drain current in weak inversion, which increases exponentially with the gate voltage (see section 2.2.3). When a MOSFET is scaled down, the supply voltage (V_{DD}) and the threshold voltage are reduced to keep the electric field in the channel constant. As shown in equation 2.32, the off current of a MOSFET (defined as the subthreshold drain current of the transistor at V_G = 0 V) has an exponential dependence on the threshold voltage. The threshold voltage cannot be scaled down significantly without causing a substantial increase in the off current. As a result, the subthreshold conduction of the device in off-state operation increases when the physical dimensions of a MOSFET are scaled down [82].

Body leakage is the diode leakage of the reverse-biased drain/body n^+-p junction in a nMOSFET. It is independent of the gate voltage and depends only on the drain to body voltage. The body leakage will be analyzed in detail in section 2.3.1.

Gate Induced Drain Leakage (GIDL) is a current between drain and body which increases with V_{DG} in nMOSFETs. It is mainly due to band-to-band tunneling of carriers in the drain depletion region near the gate oxide. GIDL will be analyzed in detail in section 2.3.2.

2.3.1 Body leakage current

The body leakage of the drain/body junction of a vertical nMOSFET is the diode leakage of a reverse biased n^+-p junction. At moderate drain bias, before the onset of avalanche multiplication, the diode leakage has three main components: diffusion current, generation current in the depletion region and band-to-band tunneling.

The diffusion current of a diode in reverse bias does not depend on the bias applied. The ideal current-voltage relationship of a diode is expressed in equation 2.35, where J_S is the diode diffusion current in reverse bias and V_{BD} is the body/drain bias (assuming a p-type body and a n^+-doped drain). The diffusion leakage current of a reverse-biased, one-sided n^+-p abrupt junction with a body doping concentration N_A is expressed by equation 2.36 [83], where n_i is the intrinsic carrier concentration.

$$J = J_S\,(e^{\frac{qV_{BD}}{kT}} - 1) \tag{2.35}$$

$$J_S = q\sqrt{\frac{D_n}{\tau_n}}\frac{n_i^2}{N_A} \tag{2.36}$$

The second component of the body leakage current is due to the generation of carriers in the depletion region of the p-n junction. This can be expressed by equation 2.37, where n_i is the intrinsic carrier concentration, w is the width of the depletion region and τ is the carrier lifetime [83]. At a given temperature, J_{gen} depends on the width of the depletion layer, and thus increases with the applied reverse bias between the drain and the body of the MOSFET (V_{DB}). As the lifetime is a slowly varying function of temperature, the generation current has the same temperature dependence as n_i [84].

$$J_{gen} = \frac{qn_i}{\tau}w \tag{2.37}$$

High values of body doping concentration in the proximity of the drain are required in short channel MOSFET technologies to suppress the short channel effects. In this condition, the maximum electric field in the depletion region of the drain/body junction increases. When the reverse bias applied on the p-n junction is high enough, the electric field can induce direct tunneling of electrons from the body valence band to the drain conduction band. As this phenomenon depends mainly on the maximum electric field in the depletion region (ε_{max}), it has a weak temperature dependence. The band-to-band tunneling leakage current can be expressed by equation 2.38, where c_{BBT} and F_0 are constants [85]. Alternatively, the tunneling of electrons from the body valence to the drain conduction band can be mediated by traps in the depletion region. In this mechanism, called trap-assisted tunneling, the existence of an electric field in the depletion region gives rise to two nonthermal transitions: tunneling of electrons from the valence band to the traps followed by tunneling from the traps to

the conduction band.

$$J_{BBT} = c_{BBT}\, V_{DB}\, \varepsilon_{max}^{\frac{3}{2}}\, e^{\frac{-F_0}{\varepsilon_{max}}} \tag{2.38}$$

In MOSFETs with a low-doped body, or at low reverse bias, the diffusion and generation currents are dominant. In semiconductors with large values of n_i, such as germanium, the diode leakage follows the diffusion equation (2.36). In silicon, n_i is much smaller, and thus the generation current dominates (equation 2.37). However, in MOSFETs with high body doping concentration and at high reverse bias (V_{DB}), the drain leakage current is dominated by band-to-band tunneling (equation 2.38).

2.3.2 GIDL

Concept of band-to-band tunneling GIDL

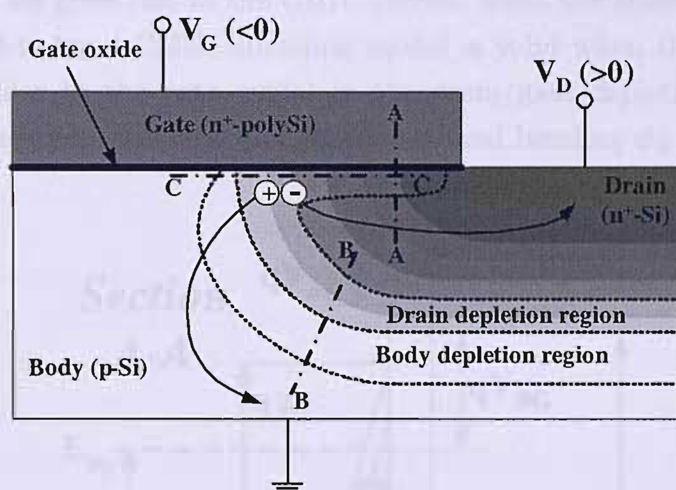

Figure 2.4: Cross-section of the drain/gate overlap region of a MOSFET in off-state ($V_G < 0$); the drain and body depletion regions and the mechanism of GIDL are shown in figure.

Gate induced drain leakage current is due to the formation of a depletion region under the gate oxide in the gate/drain overlap region of a MOSFET. Figure 2.4 shows the gate/drain overlap region of a nMOSFET in off-state operation ($V_G < 0$). In short channel MOSFETs, increased drain doping concentration and reduced gate oxide thickness both contribute to a high vertical electric field (perpendicular to the gate oxide) in the gate/drain overlap region, which increases with V_{DG}. The high electric field induces GIDL leakage currents due to band-to-band tunneling of carriers in the drain. When V_{DG} is increased, initially the drain surface is in depletion. Equation 2.39 shows the general relation between the drain surface potential (ψ_S) and V_{DG} in depletion, where $V_{FBdrain}$ is the drain flat band voltage. When the drain surface reaches inversion, the drain surface potential and the drain depletion region

cannot increase further and equation 2.39 takes the form of equation 2.40.

$$V_{DG} - |V_{FBdrain}| = \psi_S + V_{ox} \tag{2.39}$$

$$V_{DG} - |V_{FBdrain}| = V_{DB} + 2\Phi_F + V_{ox} \tag{2.40}$$

By increasing V_{DB}, the drain depletion region extends farther into the drain, following equation 2.40. At the same time, the drain surface potential and band banding increase. Due to the V_{DB} term in equation 2.40, the drain band bending increases in excess of $2\Phi_F$ and eventually exceeds the silicon bandgap, as shown in figure 2.5. When $\psi_S > E_g$, in the presence of a high electric field, electrons can tunnel from the drain valence band to the drain conduction band, thus creating an electron/hole pair. Both carriers are then swept away by the body-drain p-n junction electric field. The holes are collected at the body contact and the electrons at the drain contact. This gives rise to the GIDL current when the transistor is in the off-state. The band-to-band GIDL tunneling model is valid when the vertical electric field (perpendicular to the gate oxide) in the drain/gate depletion region is high enough for tunneling of electrons and when the band bending ψ_S is larger than the silicon bandgap.

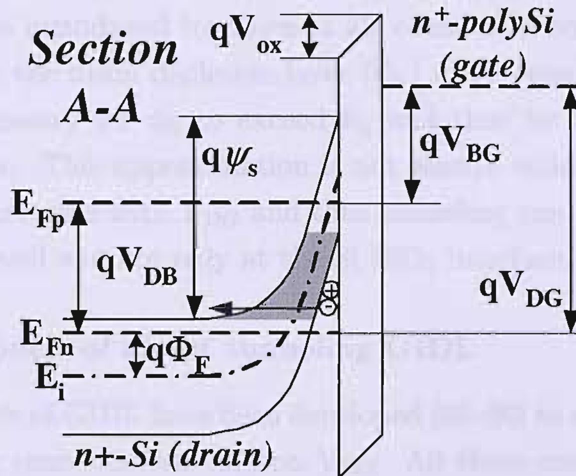

Figure 2.5: Band diagram in the drain-gate overlap region of a MOSFET corresponding to section A-A in figure 2.4.

Dependence of the band-to-band tunneling GIDL on the vertical electric field: constant surface potential model

The direct tunneling GIDL model is based on the assumption that in deep depletion electrons can tunnel from the valence band to the conduction band at the drain surface without changing their energy (see figure 2.5). Electrons have a finite probability of

tunneling through the energy barrier. The tunneling probability increases with the vertical electric field, proportional to V_{DG}.

Many models have been proposed to quantify the tunneling current. The first model proposed [86, 87] is based upon equation 2.41, where A and B are constants depending on the bandgap, w is the width of the gate induced depletion layer in the drain and $\varepsilon_{Si}(w)$ is the maximum vertical electric field at the Si/SiO_2 interface.

$$I_D = A\varepsilon_{Si}(w)e^{-\frac{B}{\varepsilon_{Si}(w)}} \tag{2.41}$$

In order to calculate $\varepsilon_{Si}(w)$, it is necessary to apply the continuity equation for electric displacement at the Si/SiO_2 interface, as displayed in equation 2.42, where $V_{FBdrain}$ is the drain flat band voltage.

$$\epsilon_{Si}\varepsilon_{Si}(w) = \epsilon_{ox}\varepsilon_{ox} = \epsilon_{ox}\frac{V_{DG} - |V_{FBdrain}| - \psi_S}{t_{ox}} \tag{2.42}$$

If any interface states or fixed charges in the oxide are neglected, the electric field in the oxide can be considered constant ($V_{ox} = \varepsilon_{ox}t_{ox}$). The vertical electric field in the drain can then be obtained from equation 2.42, yielding equation 2.43.

$$\varepsilon_{Si}(w) = \frac{V_{DG} - |V_{FBdrain}| - \psi_S}{\frac{\epsilon_{Si}}{\epsilon_{ox}}t_{ox}} \tag{2.43}$$

The simplification introduced by Chen et al. consists in considering the value of the band bending in the drain depletion layer (ψ_S) to be equal to 1.2 V. This is the minimum value necessary for ψ_S to exceed E_g and thus for tunneling to occur at the Si/SiO_2 interface. This approximation is not always valid, as in deep depletion the band bending increases with V_{DG} and thus tunneling can occur inside the drain depletion region as well and not only at the Si/SiO_2 interface.

Advanced 1-D models of direct tunneling GIDL

More accurate models of GIDL have been developed [88–90] to explain its dependence on the drain doping concentration and on V_{DG}. All these models are based on the band-to-band tunneling probability as a function of the electric field in Si. This leads to equation 2.44, where A and B are constants depending on the material bandgap. $P(\varepsilon_{Si}(z))$ is the band-to-band tunneling rate. The coordinate z is defined in figure 2.6.

$$P(\varepsilon_{Si}(z)) = A\varepsilon_{Si}^2(z)e^{-\frac{B}{\varepsilon_{Si}(z)}} \tag{2.44}$$

By applying the Poisson equation for a semiconductor with constant doping, it is possible to calculate the space charge layer width (w) and the electric field in the drain ($\epsilon_{Si}(z)$) at the Si/SiO_2 interface (z=w). This is shown in equations 2.45 and 2.47, where N_D is the drain doping concentration.

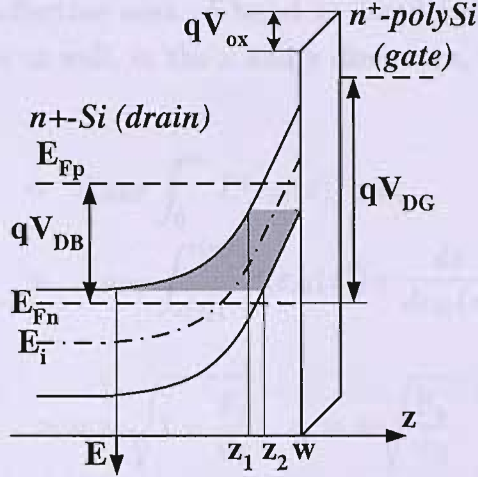

Figure 2.6: Band diagram showing the region of integration of the band-to-band tunneling rate P(ε_{Si}) in the drain-gate overlap region of a MOSFET; diagram along section A-A shown in figure 2.4.

$$w = \sqrt{\frac{2\epsilon_{Si}}{qN_D}\psi_S} \tag{2.45}$$

$$\varepsilon_{Si}(z) = \frac{qN_D}{\epsilon_{Si}}z \tag{2.46}$$

$$\varepsilon_{Si}(w) = \sqrt{\frac{2qN_D}{\epsilon_{Si}}\psi_S} \tag{2.47}$$

Equations 2.43 and 2.47 allow the band bending at the Si/SiO$_2$ interface ψ_S to be calculated, as shown in equation 2.48.

$$\begin{aligned}\psi_S(V_{DG}, N_D, t_{ox}) &= (V_{DG} - |V_{FBdrain}|) + \psi_0(N_D, t_{ox}) \\ &\quad - \sqrt{\psi_0^2(N_D, t_{ox}) + 2\psi_0(N_D, t_{ox})\,(V_{DG} - |V_{FBdrain}|)} \\ \psi_0(N_D, t_{ox}) &= \frac{qN_D\varepsilon_{Si}t_{ox}^2}{\varepsilon_{ox}^2}\end{aligned} \tag{2.48}$$

Equation 2.48 summarizes the dependence of the surface potential, and thus of the GIDL, on drain doping concentration and on gate oxide thickness. It is worth pointing out that the drain doping contribution was neglected in the simplified model by Chen et al., described in the previous section, because the surface potential was assumed to be fixed at 1.2 V. In this model, instead, the band-to-band tunneling rate can be integrated over the grey area in figure 2.6 in the z direction, which represents the region where the drain band bending is high enough for tunneling to occur. In order to obtain the value of GIDL current, the band-to-band tunneling rate has to

be integrated over the effective area of band to band tunneling (A_{BBT}) near the gate/drain overlap region as well, in the x and y directions, leading to equation 2.49.

$$\begin{aligned} I_D(x,y) &= A_{BBT} \int_0^{z_1} P(\varepsilon_{Si}(z))\, q\, dz \\ &= A_{BBT} \int_{\varepsilon(z_2)}^{\varepsilon(w)} P(\varepsilon_{Si}(z))\, q \, \frac{dz}{d\varepsilon_{Si}(z)} d\varepsilon_{Si}(z) \end{aligned} \tag{2.49}$$

$$z_1 = w\sqrt{1 - \frac{E_g}{\psi_S}}; \;\; z_2 = w\sqrt{\frac{E_g}{\psi_S}} \tag{2.50}$$

Physical models and temperature dependence of GIDL

Nobel et al. [91] characterized gated diodes as a function of the measurement temperature in order to investigate the GIDL leakage mechanisms (see figure 2.7). At low gate voltage the tunneling mechanism can be distinguished for its lack of temperature dependence, as shown in figure 2.7 for measurement temperatures lower than 200 K. At temperatures higher than 200K and at low gate voltage, the low electric field in the drain gives rise to transport-limited thermal generation, yielding a leakage current slowly increasing with V_{DG}. For higher vertical electric fields (high gate voltage) the predominant phenomenon becomes band-to-band tunneling, as soon as the drain band bending exceeds the silicon bandgap. Figure 2.7 shows that the tunneling mechanism has a weak temperature dependence.

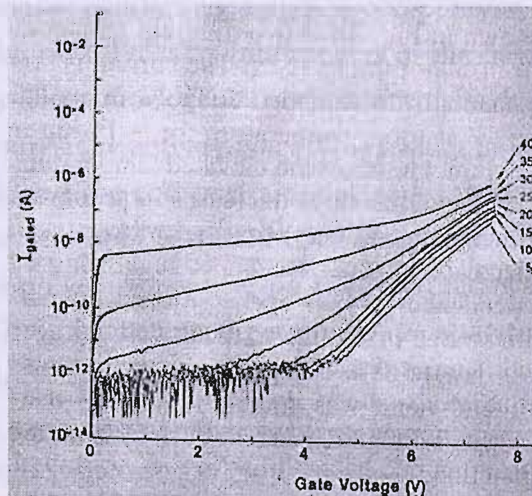

Figure 2.7: Leakage current (I_{gated}) of a p^+-n gated diode (corresponding to the drain-body junction of a pMOSFET) versus the gate voltage at temperatures ranging from 50K to 400K; after Nobel et al. [91].

Chapter 3

Fabrication and characterization of single, double and surround gate, short channel vertical MOSFETs with FILOX: initial results

3.1 Introduction

CMOS compatible vertical MOSFET fabrication processes have been developed to reduce the process complexity associated with vertical MOSFET technology. Nevertheless, the conventional vertical MOSFET layout [48] shown in figure 3.1(a) introduces gate/drain and gate/source overlap capacitance components which are considerably higher than in planar MOSFETs. The gate spacers of the device are connected to the gate contact via a polysilicon track that overlaps onto the drain on the top and onto the source on the bottom of the active pillar. This results in large overlap capacitance between the gate track and the source-drain electrodes, which are only separated by a thin gate oxide in conventional vertical MOSFETs (figure 3.1(a)). In addition, the gate itself consists of a polysilicon spacer on the pillar sidewall. The spacer overlaps source and drain, resulting in increased gate overlap capacitance.

In this chapter a fully CMOS compatible, self-aligned second oxidation process, called spacer or fillet local oxidation (FILOX), is described. The FILOX process allows gate overlap capacitance to be reduced in ion implanted vertical MOS transistors [70–77]. This is achieved by growing a thicker oxide layer between the drain and the gate on the pillar top and between the source and the gate on the pillar bottom, as shown in figure 3.1(b). In the following, a comparison of gate overlap capacitance of a FILOX vertical MOSFET, a conventional vertical MOSFET and a planar MOSFET is attempted.

In this chapter, electrical characteristics of vertical MOSFETs fabricated with the

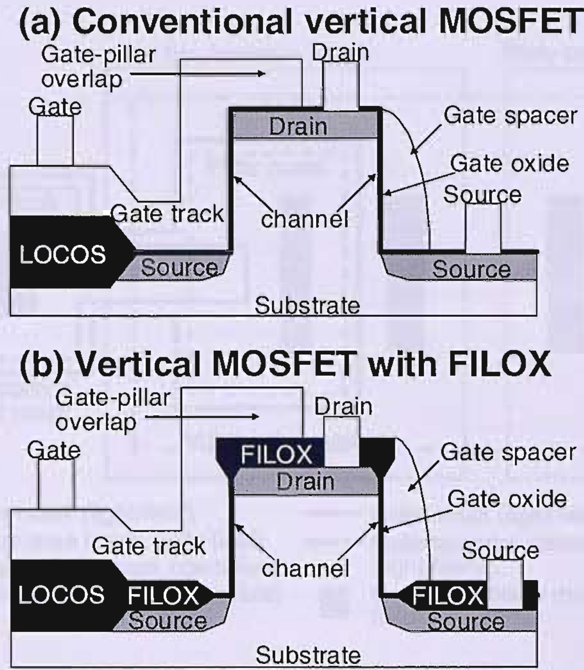

Figure 3.1: Schematic cross-sections of CMOS compatible vertical MOSFETs. (a) The overlap between the gate track and the source/drain electrodes gives rise to parasitic gate overlap capacitance in conventional ion implanted vertical MOSFETs. (b) The FILOX process allows to reduce the gate overlap capacitance.

FILOX process are presented. Devices with single, double and surround gate layout have been successfully fabricated on the same wafer with the FILOX process. Surround gate vertical MOSFETs have been structurally and electrically characterized. Devices with channel length down to 90nm are found to yield good electrical characteristics.

3.2 Fabrication of vertical MOSFETs with FILOX

Single, double and surround gate vertical nMOS transistors with reduced gate parasitic capacitance were successfully fabricated with the FILOX process by V. D. Kunz, a previous Ph.D. student at Southampton University [70, 71, 73]. For convenience, a detailed description of the fabrication process has been included in this section. The batch listing of the fabrication process is reported in appendix A.1. Figure 3.2 shows a schematic layout of the mask set used (for a detailed description of the mask set, see appendix C). A detailed description of the process flow is given below.

Boron-doped silicon wafers with resistivity 17-33 Ωcm and <100> crystallographic orientation served as the starting material. The p-type body was doped by boron ion implantation (dose: 5×10^{14} cm^{-2}; energy: 50 keV), followed by a drive-in anneal. An initial anneal at 1100°C in oxygen for 10 minutes, performed to prevent pitting of the silicon substrate, was followed by a 30 minutes anneal at the same temperature in

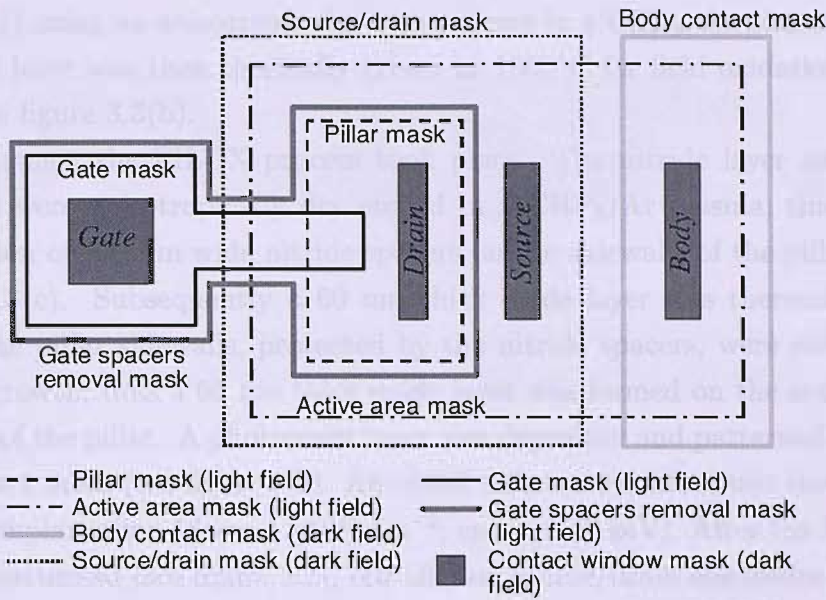

Figure 3.2: Schematic layout of the mask set used for fabrication of FILOX vertical MOSFETs. For reasons of clarity, the Metal mask has been excluded from the schematic layout.

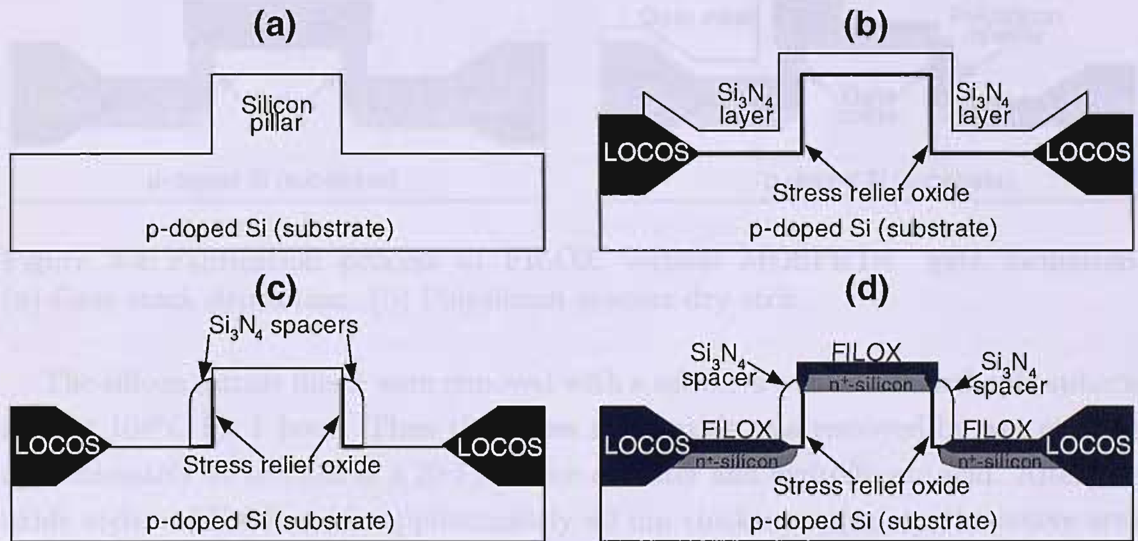

Figure 3.3: Fabrication process of FILOX vertical MOSFETs: FILOX formation. (a) Silicon pillar dry etch. (b) LOCOS formation. (c) Patterning of silicon nitride spacers. (d) FILOX oxidation and source / drain ion implantation.

nitrogen atmosphere. This yielded a body doping concentration in the channel region between 2×10^{18} cm^{-3} and 3×10^{18} cm^{-3}. After photoresist deposition and patterning by using the Pillar mask (see figure 3.2), the silicon pillars were dry etched in a HBr plasma, as shown in figure 3.3(a). A 20 nm stress relief oxide was thermally grown at 900°C to relieve the stress between the ensuing nitride layer and the silicon substrate. Silicon nitride was deposited by LPCVD to a thickness of 130 nm at 740°C. The active area was defined by patterning the nitride layer (Active area mask, shown

in figure 3.2) using an anisotropic dry etch process in a CHF_3/Ar plasma. A 600 nm thick oxide layer was then thermally grown at 1000°C for field oxidation (LOCOS), as shown in figure 3.3(b).

At this stage, the FILOX process took place. The nitride layer and the stress relief oxide were anisotropically dry etched in a CHF_3/Ar plasma; this resulted in the formation of 130 nm wide nitride spacers on the sidewalls of the pillar, as shown in figure 3.3(c). Subsequently a 60 nm thick oxide layer was thermally grown at 1000°C. The pillar sidewalls, protected by the nitride spacers, were not affected by the oxide growth; thus a 60 nm thick oxide layer was formed on the active area and on the top of the pillar. A photoresist layer was deposited and patterned by using the Body contact mask (see figure 3.2). An ohmic substrate contact was then created by boron ion implantation (dose: 1×10^{15} cm^{-2}; energy: 47 keV). After the Source/drain mask was patterned (see figure 3.2), self-aligned source/drain electrodes were formed by arsenic ion implantation (dose: 6×10^{15} cm^{-2}; energy: 120 keV), as shown in figure 3.3(d).

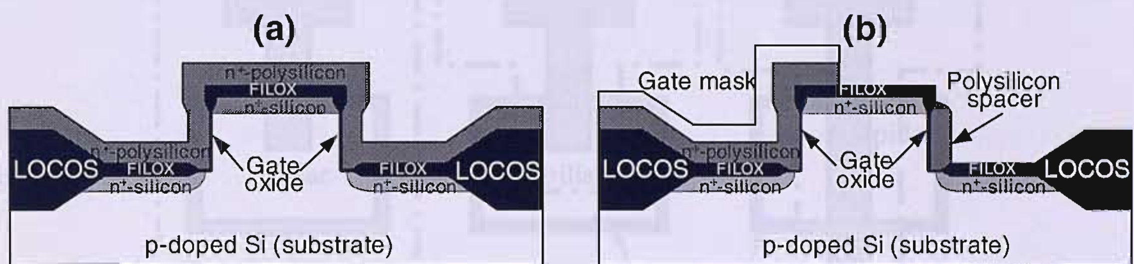

Figure 3.4: Fabrication process of FILOX vertical MOSFETs: gate formation. (a) Gate stack deposition. (b) Polysilicon spacers dry etch.

The silicon nitride fillets were removed with a selective wet etch in orthophosphoric acid at 160°C for 1 hour. Then the stress relief oxide was removed by wet etch for approximately 40 seconds in a 20:1 solution of water and hydrofluoric acid. After this oxide etch, a FILOX oxide approximately 40 nm thick remained on the active area and on the top of the pillar. A gate oxide was thermally grown on the sidewall of the pillar at 800°C. A 3.3 nm oxide thickness was measured on the flat <100> surface of silicon check wafers. The gate oxide grown on the pillar sidewalls of the vertical MOSFETs was likely to be about 40% thicker due to the <110> crystallographic orientation of the sidewalls [92]. A 200 nm in-situ phosphorus doped polysilicon layer with 5×10^{19} cm^{-3} doping concentration was deposited by LPCVD, as shown in figure 3.4(a). Then photoresist was deposited and patterned by using the Gate mask (see figure 3.2). The gate was patterned by anisotropic dry etch in a HBr/O_2 plasma, selective to the gate oxide. In this way polysilicon spacers were created all around the pillar. The polysilicon track connecting the polysilicon spacers to the gate contact was protected from the etch by the Gate mask, as shown in figure 3.4(b).

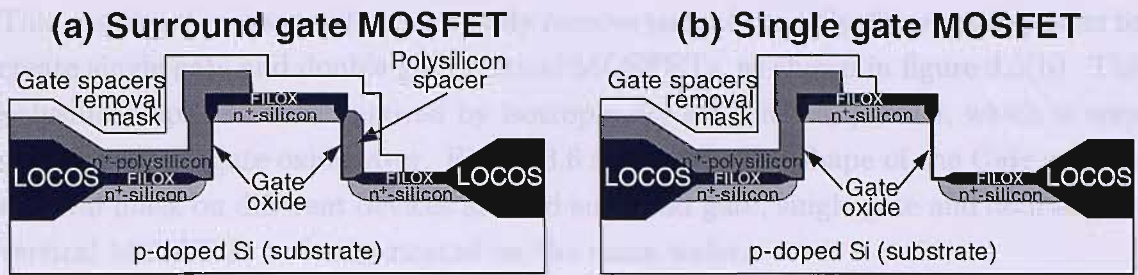

Figure 3.5: Fabrication process of FILOX vertical MOSFETs: partial removal of the gate spacers for fabrication of (a) surround gate and (b) single gate vertical MOSFETs.

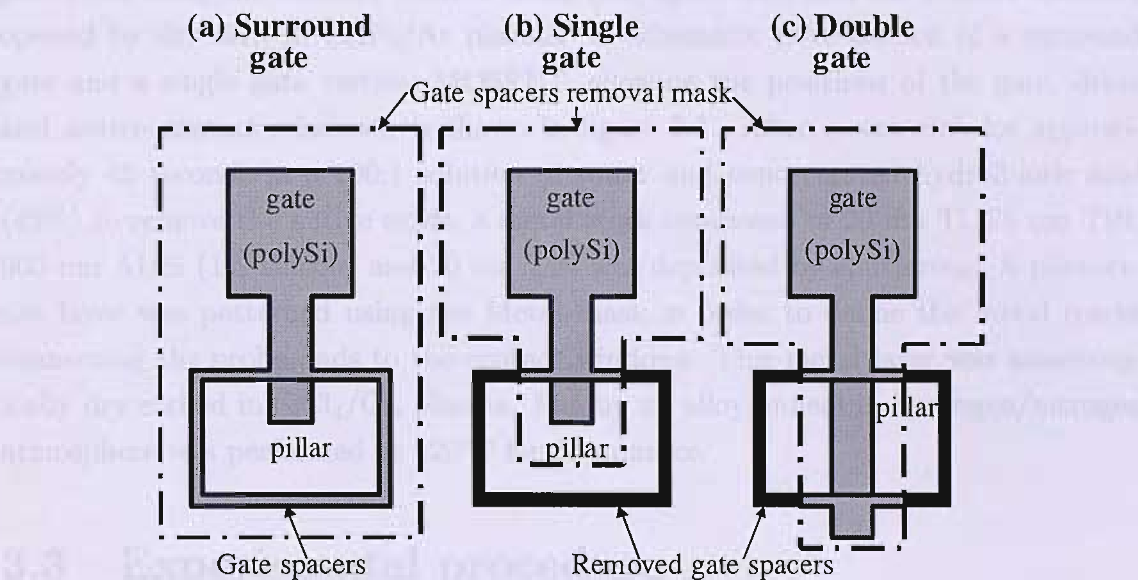

Figure 3.6: Schematic top view showing the layout of the Gate spacers removal mask used to fabricate (a) surround gate, (b) single gate and (c) double gate vertical MOSFETs.

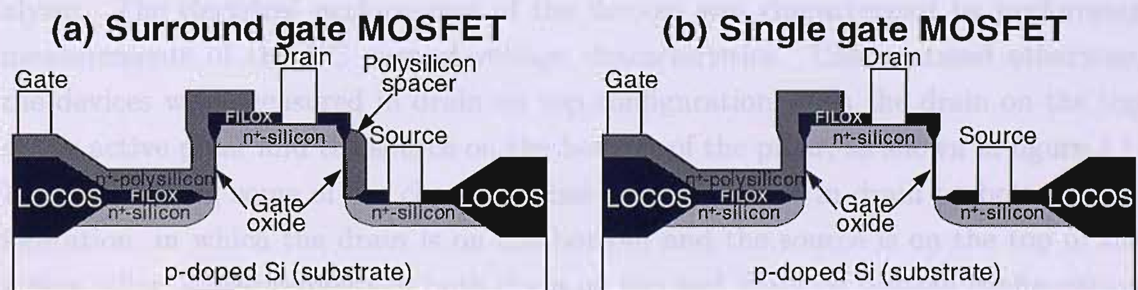

Figure 3.7: Fabrication process of FILOX vertical MOSFETs: schematic cross sections (a) of the surround gate and (b) of the single gate vertical MOSFETs fabricated. The figure shows the positions of gate, drain and source vias.

A photoresist layer was patterned using the Gate spacers removal mask (see figure 3.2) to protect the polysilicon gate track and the polysilicon spacers of the surround gate vertical MOSFETs from the subsequent polysilicon etch (see figure 3.5(a)).

This process step was used to selectively remove part of the polysilicon gate spacers to create single gate and double gate vertical MOSFETs, as shown in figure 3.5(b). The polysilicon spacers were removed by isotropic dry etch in SF_6 plasma, which is very selective to the gate oxide layer. Figure 3.6 shows how the shape of the Gate spacers removal mask on different devices allowed surround gate, single gate and double gate vertical MOSFETs to be fabricated on the same wafer.

A 100 nm thick undoped oxide diffusion barrier layer was then deposited, followed by a 500 nm thick Boron Phosphorous Silicate Glass (BPSG) layer. An RTA at 1100°C for 10sec was performed for dopant activation. A photoresist layer was patterned using the Contact window mask (see figure 3.2), and the contact windows opened by dry etch in CHF_3/Ar plasma. A schematic cross-section of a surround gate and a single gate vertical MOSFET, showing the positions of the gate, drain and source contact windows, is shown in figure 3.7. After a wet etch for approximately 45 seconds in a 100:1 solution of water and concentrated hydrofluoric acid (49%) to remove the native oxide, a metal stack composed of 20 nm Ti, 75 nm TiN, 900 nm Al/Si (1% silicon) and 20 nm TiN was deposited by sputtering. A photoresist layer was patterned using the Metal mask in order to define the metal tracks connecting the probe pads to the contact windows. This metal layer was anisotropically dry etched in $SiCl_4/Cl_2$ plasma. Finally an alloy anneal in hydrogen/nitrogen atmosphere was performed at 420°C for 30 minutes.

3.3 Experimental procedure

3.3.1 Electrical characteristics

The transistors fabricated were characterized using a HP4155A semiconductor analyzer. The electrical performance of the devices was characterized by performing measurements of the DC current-voltage characteristics. Unless stated otherwise, the devices were measured in drain on top configuration, with the drain on the top of the active pillar and the source on the bottom of the pillar, as shown in figure 3.1. For comparison, some of the characteristics were measured in drain on bottom configuration, in which the drain is on the bottom and the source is on the top of the active pillar. Measurements in both drain on top and drain on bottom configuration were required to assess the asymmetry of the electrical characteristics of the vertical MOSFETs. On the contrary, this is not an issue in planar MOSFETs, where the interchange of source and drain has no effect on the electrical characteristics.

In order to assess the performance of the devices, the following parameters were extracted, in drain on top configuration: threshold voltage, subthreshold slope, on-state drain current, off-state drain current and DIBL. The linearly extrapolated threshold voltage (V_{on}) was extracted by linear extrapolation from $I_D(V_G)$ characteristics at

V_D = 0.025 V. For a second order correction in V_D, the threshold voltage (V_t) was calculated as $V_t = V_{on} - V_D/2$. This expression is derived from equation 2.21 with m = 1. The subthreshold slope of the transistors was extracted as the inverse of the slope of the logarithmic transfer characteristics (Log I_D (V_G)) in the subthreshold region (equation 2.31). The on-state drain current was extracted at $V_G - V_t = 1$ V from $I_D(V_G)$ characteristics measured at $V_D = 1$ V. This allowed a comparison of the drain current of the devices at constant total inversion charge density in the channel ($V_G - V_t$ = constant; see equations 2.20 and 2.21). The off-state drain current of the transistors was extracted at $V_G = 0$ V and $V_D = 1$ V. The DIBL was calculated as the subthreshold slope shift between the logarithmic transfer characteristics (Log I_D (V_G)) at high drain bias ($V_D = 1$ V) and low drain bias ($V_D = 0.025$ V).

3.3.2 SIMS profiles

The doping profiles of the fabricated devices were characterized by Secondary Ion Mass Spectroscopy (SIMS). This technique employs a primary ion beam to sputter a sample. The impurity concentration in the substrate is quantified by detecting the secondary ions emitted during sputtering. The samples were analyzed using O_2^+ primary ion bombardment and positive secondary ion detection. These conditions combined good depth resolution with good sensitivity to boron and reasonable sensitivity to arsenic. The data were quantified using implanted reference materials and the depth scales were determined by measuring the sputtered crater depths by interference microscopy, yielding results accurate to $\pm$5 nm.

3.3.3 SEM cross-sections

SEM cross-sections of the active pillars of vertical MOSFETs were taken during process development and after completion of the fabrication process using a JSM 6500F thermal field emission scanning electron microscope. The samples were prepared by cleaving the substrates through SEM bars with the same structure of the active pillar of the vertical MOSFETs (except the metal contacts). The outlines of highly doped silicon regions (e. g. source and drain of the MOSFETs) and thin oxide layers were enhanced by stain etching the samples in a 400:1 solution of nitric acid and concentrated hydrofluoric acid (49%). High resolution SEM images were mostly obtained with a beam energy of 10 keV.

The channel length of the devices was estimated from SEM cross-sections by measuring the distance between the source/body junction on the bottom of the pillar and the drain/body junction on the pillar sidewall. The channel length value extracted by SEM was then adjusted by measuring the difference between the depth of the drain/body junction measured by SIMS and the drain junction depth observed by SEM. This procedure will be discussed in more detail in section 3.6.1.

3.4 Overlap capacitance reduction in vertical MOSFETs with FILOX

3.4.1 FILOX structural characterization

The FILOX process provides a gate overlap capacitance that is lower than in the standard process. The reduction in overlap capacitance is achieved by the approximately 40 nm thick FILOX oxide layer that is grown on all planar surfaces instead of the 3.3 nm thick gate oxide. The SEM image in Figure 3.8 shows a cross-section of a fabricated surround gate vertical MOSFET.

Several factors contribute to reduce the gate overlap capacitance. First, the thick FILOX oxide reduces the gate/source overlap capacitance between the gate track and the active area at the bottom of the pillar. Second, the nitride spacer used in the FILOX process was much thinner than the gate spacer, which allows the FILOX oxide to extend beneath the gate and reduce the gate/source overlap capacitance. Third, the FILOX oxide on top of the pillar reduces the gate/drain overlap capacitance where the gate track overlaps onto the top of the pillar. Fourth, both the nitride spacer and the polysilicon gate spacer were over-etched, which reduces the gate/drain overlap capacitance on the side of the pillar. Finally, the FILOX bird's beaks reduce the gate/drain overlap capacitance on the pillar sidewall and the gate/source overlap capacitance on the bottom of the pillar.

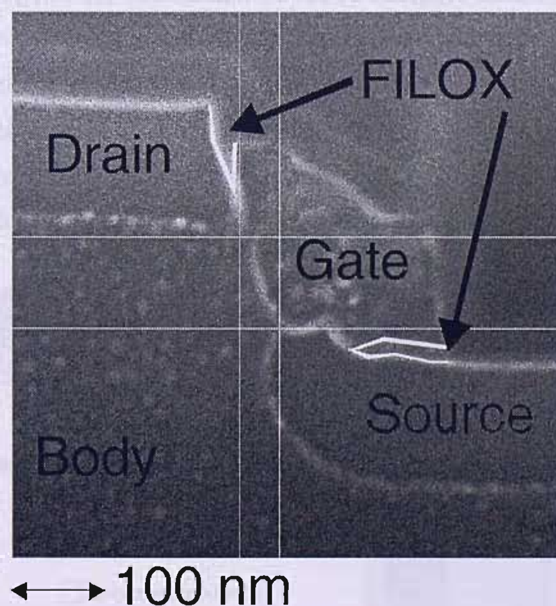

Figure 3.8: SEM cross-section of the active pillar of a surround gate vertical nMOSFET fabricated with the FILOX process. Both pillar top and bottom show the thick FILOX oxide, accentuated in the picture.

3.4.2 Evaluation of capacitance reduction due to the FILOX process

Although direct probing of the intrinsic capacitance of FILOX vertical MOSFETs is difficult due to their small size, calculations based on SEM cross-sections have been used to give an estimate of the expected capacitance reduction. This takes place both below the gate track and below the gate spacers and is strongly dependent on the nitride spacer thickness and on the lithography node.

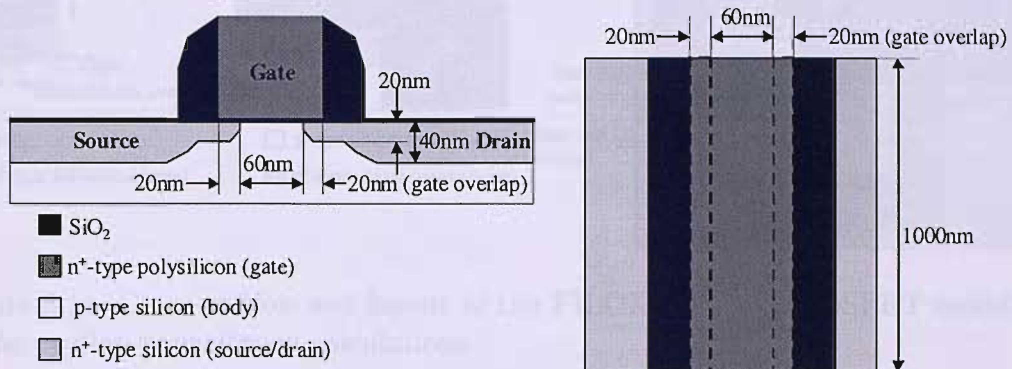

Figure 3.9: Cross-section and layout of the simplified planar nMOSFET model with 100 nm gate length and 60 nm channel length used in the overlap capacitance calculations.

A quantitative comparison was made of three simplified transistor: a planar MOSFET, a conventional vertical MOSFET and a FILOX vertical MOSFET. To compare the results, all devices had channels 1 μm wide. The comparison was done for a state of the art industrial planar MOSFET technology with 20 nm source/drain extensions junction depth, 40 nm HDD junction depth, 2 nm gate oxide, 60 nm channel length, 100 nm minimum feature size and 50 nm alignment tolerance, as shown in figure 3.9.

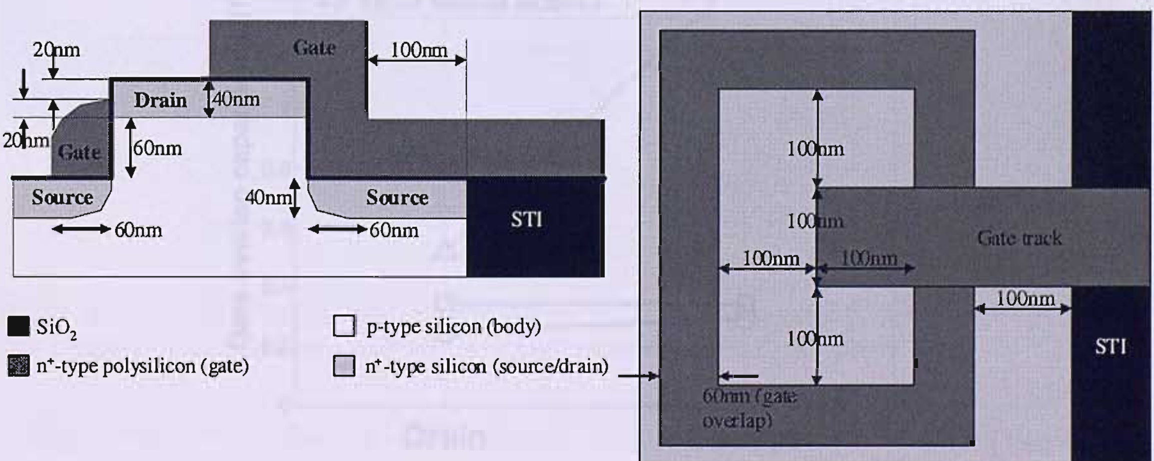

Figure 3.10: Cross-section and layout of the conventional vertical nMOSFET model used in the overlap capacitance calculations.

The model of the conventional vertical MOSFET is shown in figure 3.10. The same design rules were used as in the planar MOSFET. The gate spacers were scaled to 60 nm width. The gate spacers overetch was 20 nm from the top of the pillar. An STI field oxide was used for consistency with the 100 nm planar technology.

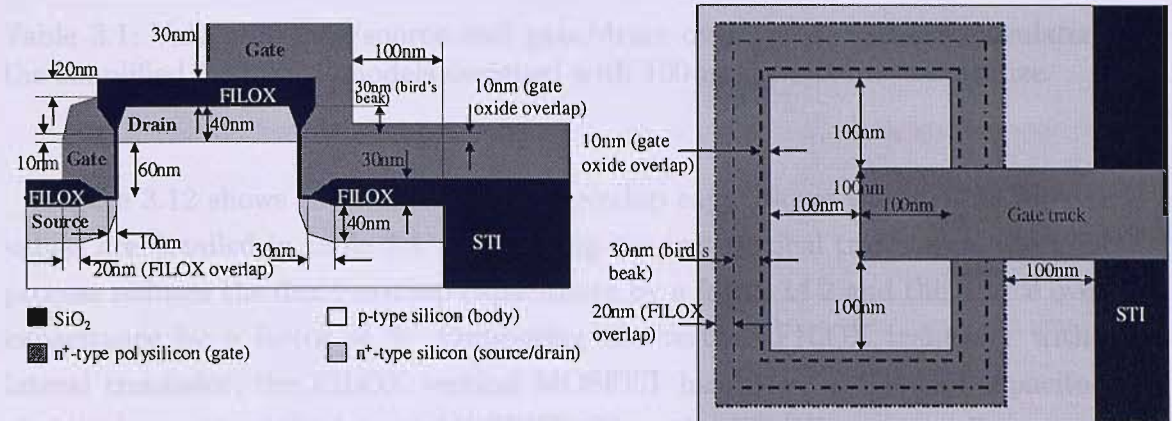

Figure 3.11: Cross-section and layout of the FILOX vertical nMOSFET model used in the overlap capacitance calculations.

Figure 3.11 shows the simplified model used for the gate overlap capacitance calculations of the FILOX vertical MOSFET. The bird's beaks length (30 nm) and FILOX thickness (30 nm) were extrapolated from figure 3.8. The nitride spacer thickness was scaled down to 40 nm and the polysilicon gate thickness to 60 nm. In the calculations the bird's beaks were modelled as homogeneous oxide layers and their thickness was assumed to be 16 nm (the average of the gate oxide thickness and of the FILOX oxide thickness).

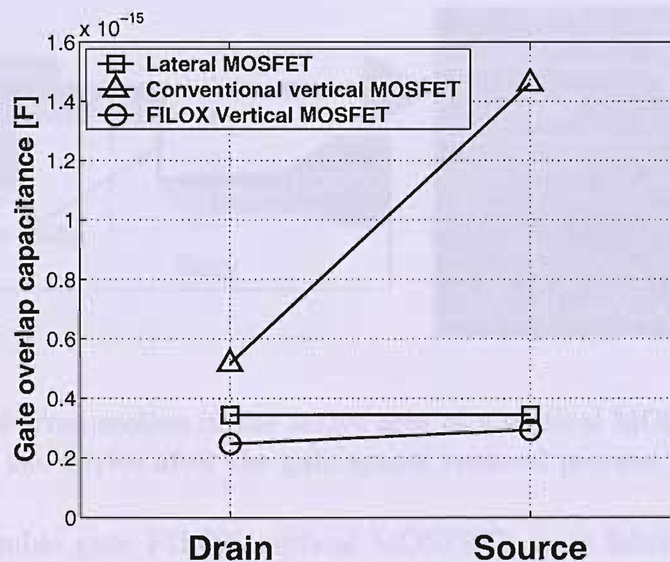

Figure 3.12: Gate/source and gate/drain overlap capacitance of the simplified MOSFET models designed with a 100 nm industrial technology design rules.

	Gate overlap capacitance [F]		
	Planar MOSFET	Conventional vertical MOSFET	Vertical MOSFET with FILOX
Drain	3.45×10^{-16}	5.17×10^{-16}	2.48×10^{-16}
Source	3.45×10^{-16}	1.46×10^{-15}	2.94×10^{-16}

Table 3.1: Values of gate/source and gate/drain overlap capacitance calculated on the simplified MOSFET models designed with 100 nm minimum feature size.

Figure 3.12 shows the calculated gate overlap capacitance values. The numerical values are detailed in table 3.1. Comparing the two vertical transistors, the FILOX process reduces the drain overlap capacitance by a factor of 2 and the source overlap capacitance by a factor of 5. Comparing the vertical FILOX transistor with the lateral transistor, the FILOX vertical MOSFET has drain and source capacitances slightly lower than the lateral MOSFET. Thus the FILOX process allows vertical MOSFETs to be fabricated with overlap capacitance values much lower than the traditional vertical devices and similar to those achieved in planar MOSFETs.

3.5 Characterization of single, double and surround gate vertical MOSFETs

3.5.1 Structural characterization of the gate spacers removal process

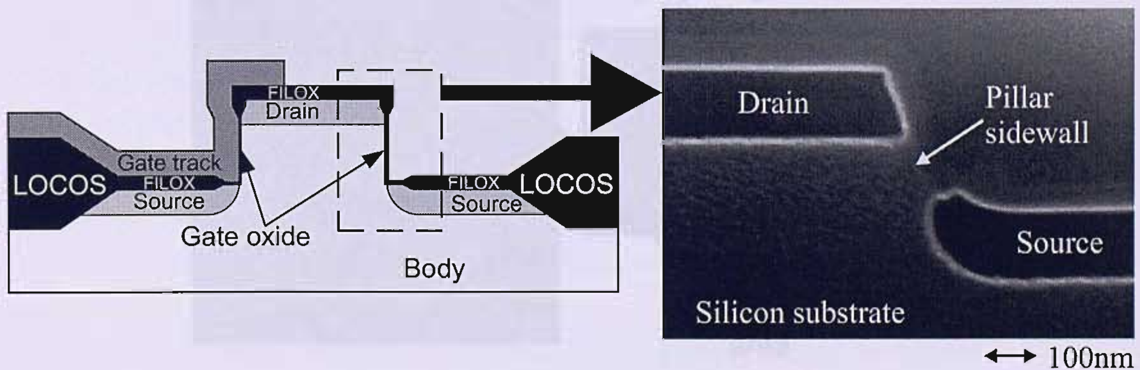

Figure 3.13: SEM cross-section of the active area of a vertical MOSFET showing the pillar sidewall of the device after the gate spacer removal process.

Single and double gate FILOX vertical MOSFETs were fabricated by partially removing the polysilicon gate spacers from the sidewalls of a ridge or pillar etched in silicon. The process used for the selective etch of the gate spacers is described in detail in section 3.2. A Gate spacers removal mask was used to protect the polysilicon gate

track connecting the gate spacers to the gate contact from the plasma used for the etch process. Moreover, the mask protected from the etch the gate spacers of the single and double gate MOSFETs. Figure 3.13 shows a cross-section of the pillar sidewall of a single gate vertical MOSFET which was exposed to the polysilicon etch. The pillar sidewall does not present any irregularities. This confirms that the selectivity to the gate oxide of the etch process was high enough and that the gate oxide was sufficient to protect the pillar sidewall from the plasma used to etch the polysilicon spacers. No residue of the polysilicon spacers is visible in the picture. This confirms that the spacers were completely removed from the portion of the pillar sidewalls exposed to the plasma.

3.5.2 Layout of the single, double and surround gate vertical MOSFETs fabricated with the FILOX process

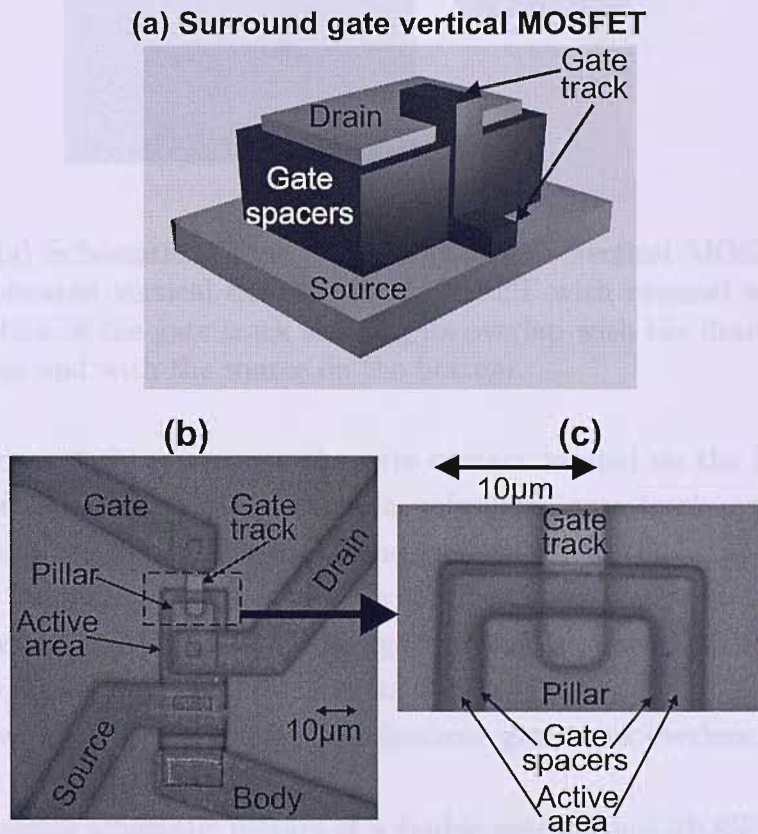

Figure 3.14: (a) Schematic 3D view of a surround gate vertical MOSFET. (b) Top-view of a fabricated vertical surround gate MOSFET with channel width of $52\mu m$. (c) Magnification of the gate track showing its overlap with the drain on the top of the active pillar and with the source on the bottom.

Figure 3.14(a) shows a schematic 3-dimensional view of a surround gate vertical MOSFET. The polysilicon gate spacers wrap around the active pillar of the device.

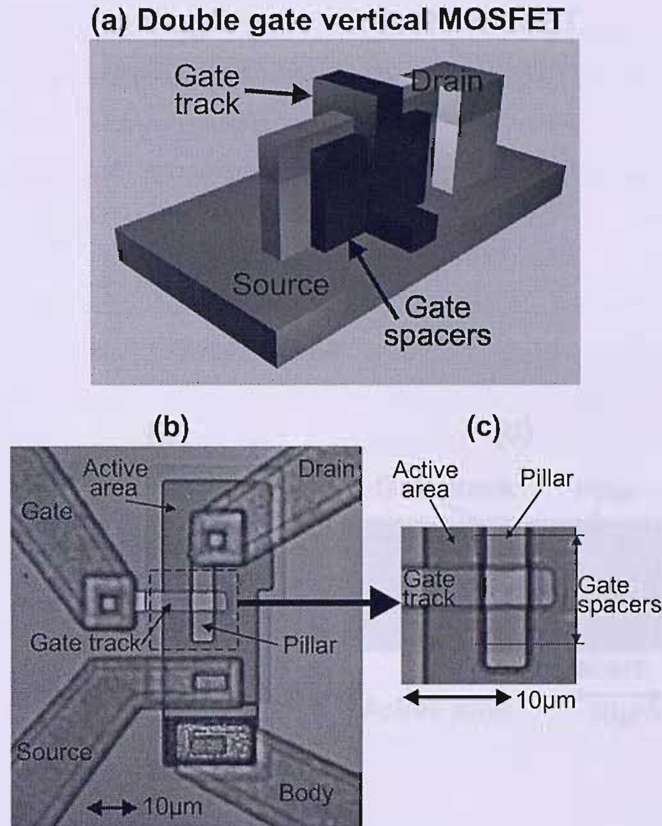

Figure 3.15: (a) Schematic 3D view of a double gate vertical MOSFET. (b) Top-view of a fabricated vertical double gate MOSFET with channel width of $20\mu m$. (c) Magnification of the gate track showing its overlap with the drain on the top of the active ridge and with the source on the bottom.

In order to connect the spacers to the gate contact located on the field oxide that surrounds the active area of the device, a polysilicon gate track overlaps both the drain and the source of the MOSFET. The gate oxide and the FILOX oxide are not shown in the 3-dimensional view. Figure 3.14(b) shows a top-view of a fabricated surround gate vertical MOSFET. The figure shows the metal tracks that connect the contact windows to the electrode contact pads. Finally, figure 3.14(c) displays a magnified view of the region where the polysilicon gate track overlaps the active area and the pillar of the device.

A 3-dimensional schematic picture of a double gate vertical MOSFET is shown in figure 3.15(a). The polysilicon gate track overlaps a thin active ridge and connects the polysilicon spacers on both sides of the ridge to a gate contact on the field oxide. The drain contact is located at the far end of the ridge, where it widens in order to allow the drain contact window to be aligned to the active ridge, as shown in figure 3.15(b). The selective polysilicon etch process, described in section 3.2, allows to remove the gate spacers from the drain contact area. If the active ridge of the double gate vertical MOSFET is thin enough (about 30-70 nm), the channel of the

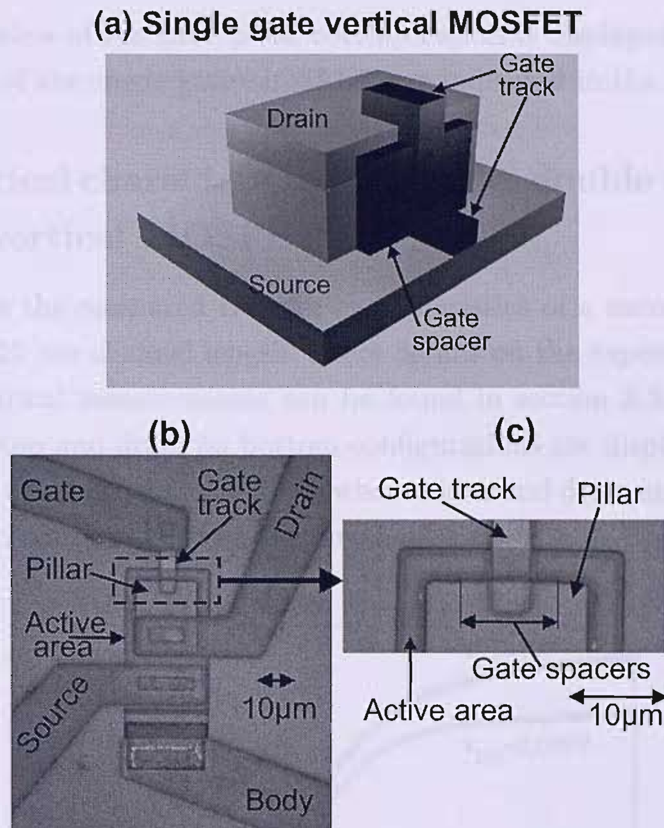

Figure 3.16: (a) Schematic 3D view of a single gate vertical MOSFET. (b) Top-view of a fabricated vertical single gate MOSFET with channel width of $10\mu m$. (c) Magnification of the gate track showing its overlap with the drain on the top of the active pillar and with the source on the bottom.

device in strong inversion can be fully depleted [53, 54]. Figure 3.15(b) shows a top-view of a fabricated double gate vertical MOSFET. The active ridge of this device is not thin enough to achieve fully depleted operation. Nevertheless, this device demonstrates that the FILOX process can be used to fabricate double gate, thin body vertical MOSFETs with reduced gate overlap capacitance. A magnification of the region where the polysilicon gate track overlaps the active ridge is shown in figure 3.15(c). The gate spacers of the double gate MOSFET are indicated in the figure.

A schematic 3-dimensional view of a single gate vertical MOSFET is shown in figure 3.16(a). The polysilicon gate spacers have been removed from all around the active pillar except from one of its sides and the drain contact is positioned on the top of the pillar. Independently biased gates could be fabricated on each of the four sides of the active pillar of the device, with a common drain contact on the top of the pillar. This process allows the integration of logic gates with reduced parasitic capacitance within a single active area incorporating one (NOR gate) or two (NAND gate) active pillars. Figure 3.16(b) shows a top-view of a fabricated single gate vertical MOSFET.

A magnified top-view of the gate/pillar overlap region is displayed in figure 3.16(c). The gate spacers of the single gate MOSFET are indicated in the figure.

3.5.3 Electrical characteristics of single, double and surround gate vertical MOSFETs

Figure 3.17 shows the measured transfer characteristics of a surround gate vertical MOSFET with 125 nm channel length. More details on the experimental procedure used for the electrical measurements can be found in section 3.3.1. Measurements in both drain on top and drain on bottom configurations are displayed to assess the asymmetry of the electrical characteristics when source and drain are exchanged. Very little asymmetry is observed in the subthreshold and on-state regions of operation,

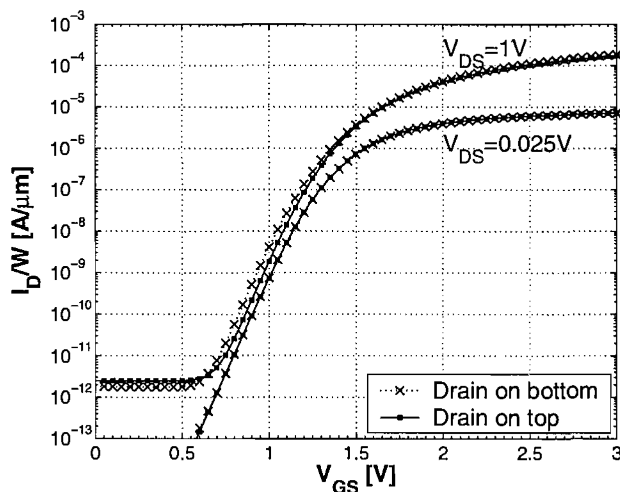

Figure 3.17: Measured transfer characteristics of a surround gate vertical nMOS transistor with channel width = 24 μm and channel length = 125 nm; V_S=V_B=0 V.

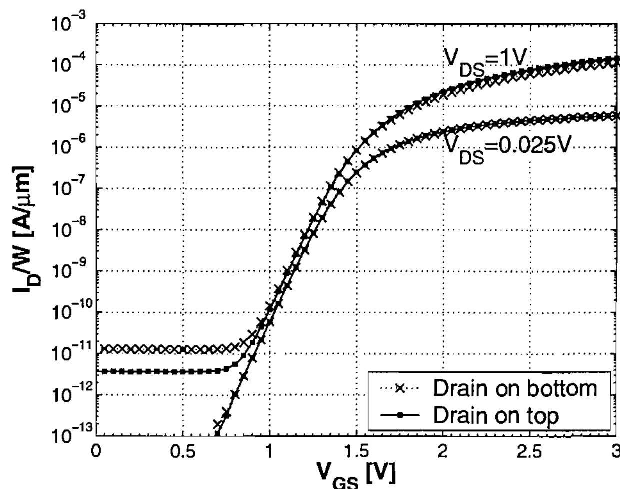

Figure 3.18: Measured transfer characteristics of a double gate vertical NMOS transistor with channel width = 9 μm and channel length = 125 nm; V_S=V_B=0 V.

due to the low series resistances of both electrodes. Van der Pauw sheet resistance measurements [93] have been performed on test structures with the same doping concentration as the source/drain electrodes. A source/drain sheet resistance value of 49 Ω has been measured, which constitutes an acceptable value for MOSFETs [82]. It can be observed that in the off-state region of operation the characteristics of the devices are not perfectly symmetric. The off-state behavior of the devices will be analyzed in detail in chapter 4.

The measured transfer characteristics of a double gate vertical MOSFET are shown in figure 3.18. The device shows reasonably symmetrical electrical characteristics in drain on top and drain on bottom configurations both in the subthreshold and in the on-state regions of operation.

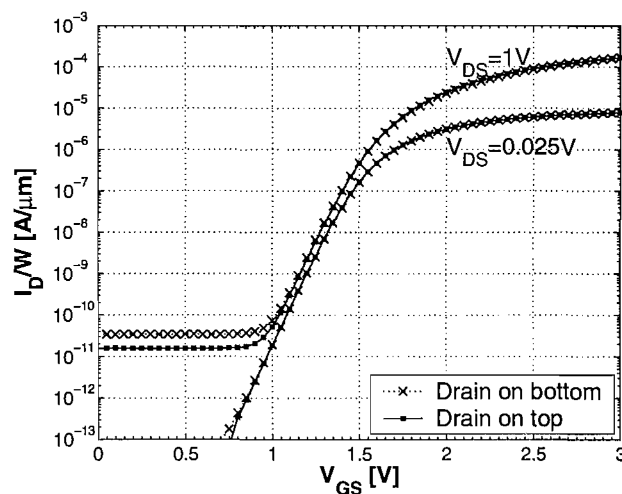

Figure 3.19: Measured transfer characteristics of a single gate vertical NMOS transistor with channel width = 4.5 μm and channel length = 125 nm; V_S=V_B=0 V.

Figure 3.19 shows the measured transfer characteristics of a single gate vertical MOSFET with 125 channel length. In the on-state and in the subthreshold regions of operation, the device again shows symmetrical characteristics both in drain on top and in drain on bottom configurations.

3.6 Electrical characterization of short channel FILOX vertical MOSFETs

3.6.1 Extraction of the channel length of short channel, surround gate vertical MOSFETs

As described in section 3.2, the active pillar of the short channel vertical MOSFETs was dry etched in the silicon substrate using an HBr plasma. Due to the nonuniformity of the dry etch process, a distribution of pillar heights was obtained on the

same silicon wafer. Profilometer measurements allowed the pillar height to be probed throughout the wafer. The pillar height was found to be lower close to the left edge and higher close to the right edge of the wafer (relative to the flat of the silicon wafer). This was confirmed by SEM cross-sections of devices from different sites on the wafer, which allowed the quantification of the channel length of the transistors. A distribution of vertical MOSFETs with channel lengths between 90 nm and 140 nm was found. As all the devices characterized were on the same wafer, it was reasonable to assume that the transistors were identical except for the channel length. This variation provided an ideal way of probing the effect of channel length variation on the electrical characteristics of surround gate vertical MOSFETs with FILOX.

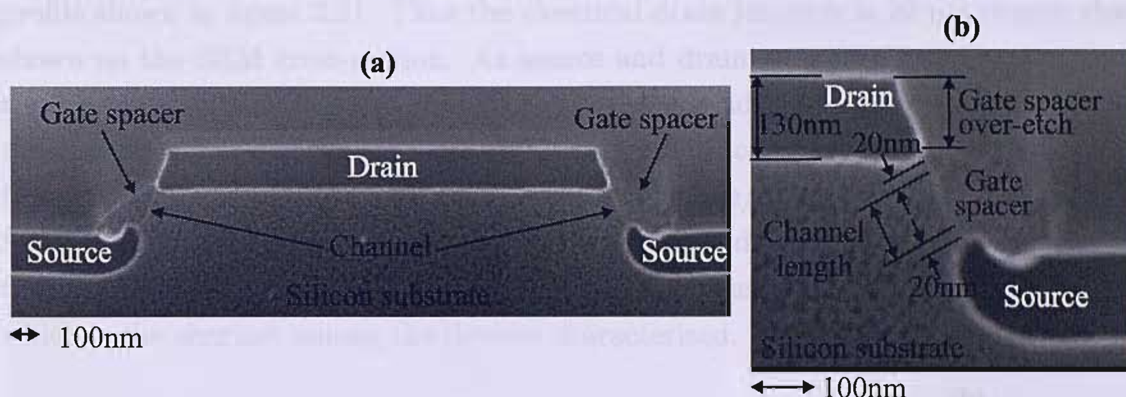

Figure 3.20: SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 90 nm channel length. The device was located close to the left edge of the wafer.

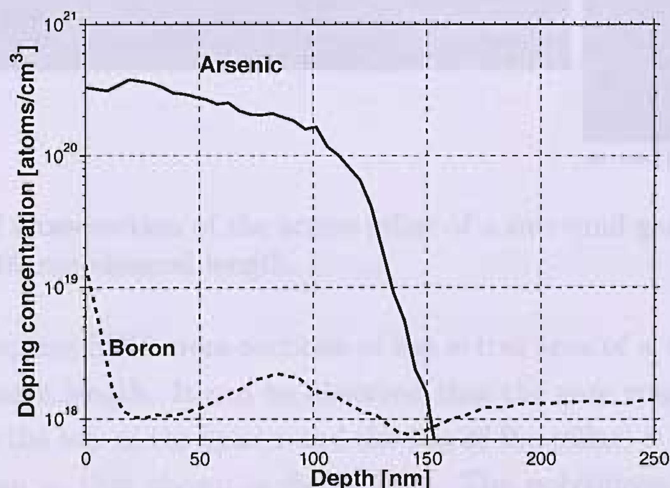

Figure 3.21: SIMS profile of the drain/body junction of a vertical MOSFET; the junction is 150 nm deep.

Figure 3.20 shows the SEM cross-section of a test structure showing the active pillar of a surround gate FILOX vertical MOSFET. The outlines of highly doped silicon regions (source and drain of the MOSFETs) are enhanced by stain etching.

This allows the distance between the drain/body and source/body junctions to be measured. The stain etching technique allows the contrast of highly doped silicon regions to be enhanced, as described in section 3.3.3. If the drain/body junction is gradual, the junctions shown on the SEM cross-sections do not correspond to the electrical junctions of the devices, which are defined as the depth at which the drain and body doping concentrations have the same value. For this reason, the drain junction depth measured on the SEM cross-sections is compared with the value extracted from the SIMS doping profile of a device from the same wafer. The drain junction depth of the vertical MOSFET shown in the SEM cross-section in figure 3.20(b) is 130 nm. On the other hand, a 150 nm junction depth is extracted from the SIMS profile shown in figure 3.21. Thus the electrical drain junction is 20 nm deeper than shown on the SEM cross-section. As source and drain were implanted at the same time, it is reasonable to estimate a 20 nm lateral spread of the source junction under the gate spacer. As shown in figure 3.20(b), a 40 nm correction factor is subtracted from the distance between the drain/body and source/body junctions extracted by SEM in order to compensate for the extra source and drain junction depth shown in the SIMS results. The device shown in figure 3.20 has a channel length of 90 nm, which is the shortest among the devices characterized.

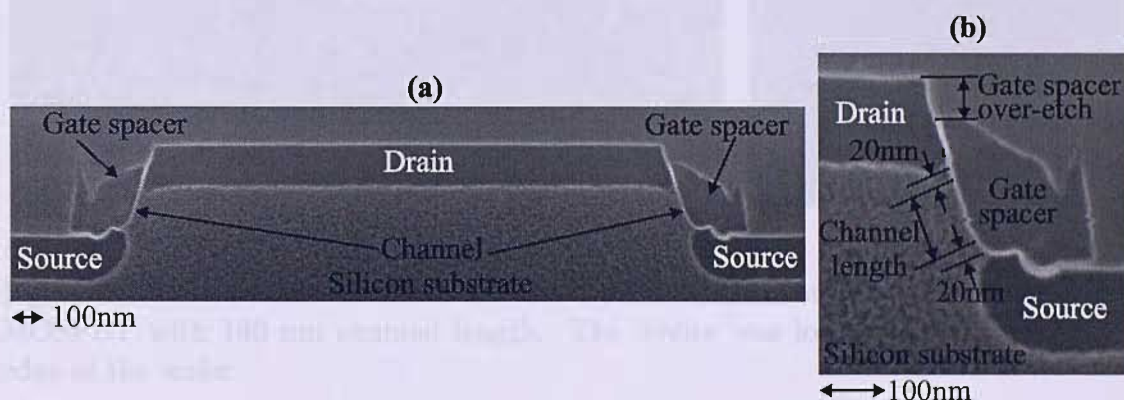

Figure 3.22: SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 100 nm channel length.

Figure 3.22 displays SEM cross-sections of the active area of a vertical MOSFET with 100 nm channel length. It can be observed that the gate spacer over-etch (the distance between the top of the spacer and the top of the pillar) is more pronounced in this device than in that shown in figure 3.20. The polysilicon layer was etched in HBr/O_2 plasma, as described in section 3.2, to leave gate spacers on the pillar sidewalls of the MOSFETs. The polysilicon etch rate was higher in the cells closer to the edge of the wafer (figure 3.20) than in those at the center of the wafer (figure 3.22). This is due to loading effect, a well known dry etch phenomenon due to faster depletion of reactive species from the plasma in the central area of the wafer.

An SEM cross-section of the active area of a vertical MOSFET with 120 nm

channel length is shown in figure 3.23. Finally, the cross-section of a vertical MOSFET with 140 nm channel length is shown in figure 3.24. This is the device with the longest channel measured on the wafer.

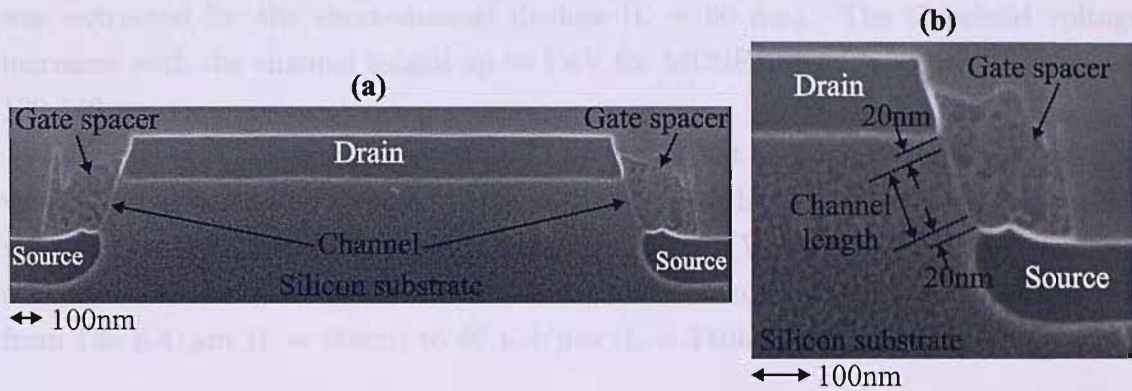

Figure 3.23: SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 120 nm channel length.

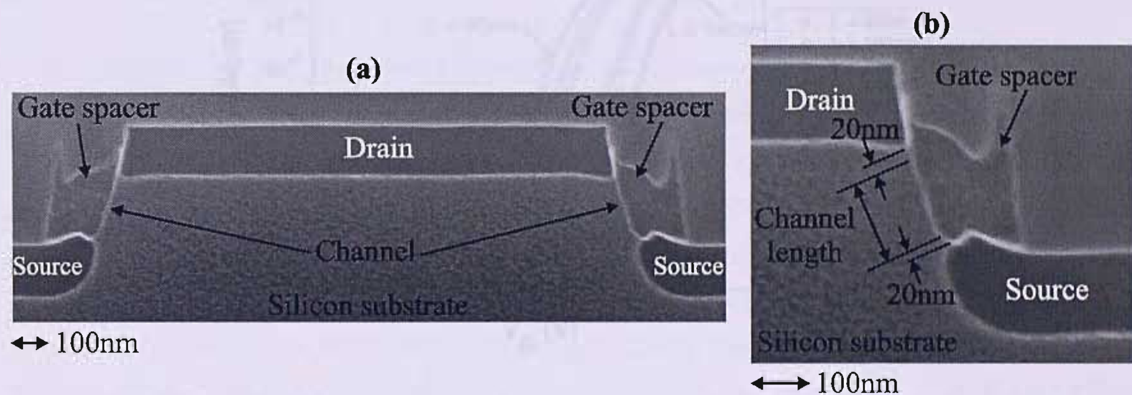

Figure 3.24: SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 140 nm channel length. The device was located close to the right edge of the wafer.

3.6.2 Electrical characterization of the short-channel effect in surround gate vertical MOSFETs

Transfer characteristics of surround gate FILOX vertical nMOSFETs with channel lengths ranging between 90nm and 140nm at a drain bias of 1 V are shown on the same graph in figure 3.25. The procedure used to extract the channel length of the devices is described in section 3.6.1. It can be observed that the subthreshold slope of the devices is approximately constant, and a subthreshold shift of about 1.2 V is observed between the characteristic of the device with L = 90 nm and that with L = 140 nm. The on-state drain currents decrease with increasing channel length. At V_G = 3 V, the drain current decreases from 300 $\mu A/\mu m$ (L = 90nm) to 60 $\mu A/\mu m$ (L = 140nm).

Figure 3.26 shows the channel length dependence of the threshold voltage of surround gate FILOX vertical MOSFETs. The results show a decrease in the value of the threshold voltage with decreasing channel length. A threshold voltage of 0.8V was extracted for the short-channel devices (L = 90 nm). The threshold voltage increases with the channel length up to 1.6V for MOSFETs with a channel length of 130-140 nm.

In Figure 3.27 the measured on-state drain current of the surround gate FILOX vertical nMOS transistors is plotted as a function of the channel length. The values were measured with a constant gate voltage overdrive (V_{GS} - V_t = 1 V). As expected, a decrease of the on-state drain current with increasing channel length is observed, from 135 $\mu A/\mu m$ (L = 90nm) to 40 $\mu A/\mu m$ (L = 140nm).

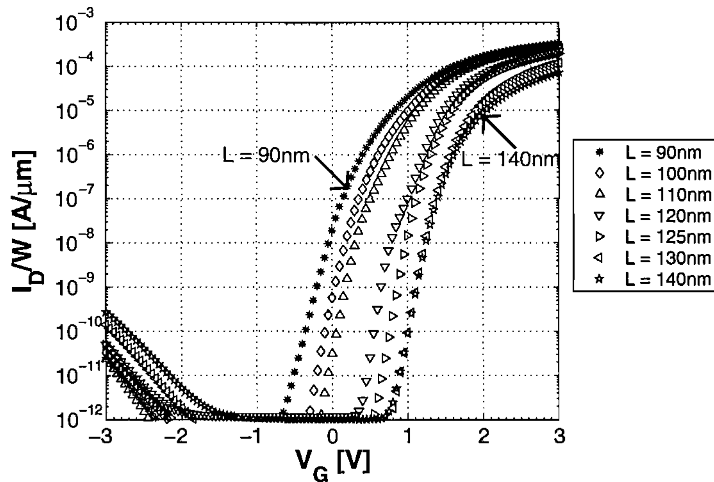

Figure 3.25: Transfer characteristic of surround gate vertical MOSFETs with different channel lengths at V_{DS} = 1 V; W = 24 μm; V_S = V_B = 0 V.

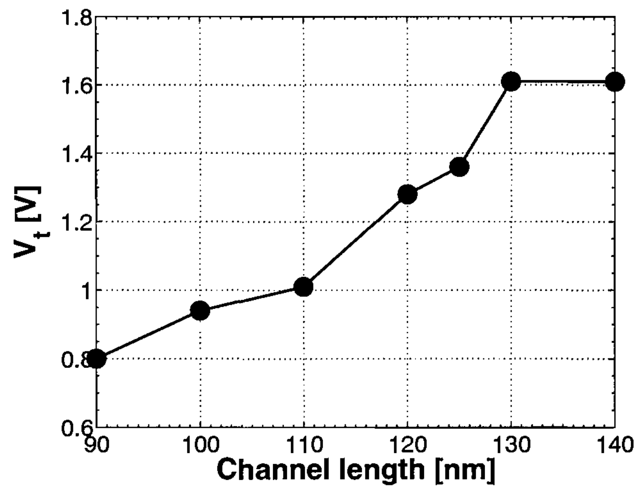

Figure 3.26: Threshold voltage of surround gate FILOX vertical nMOS transistors as a function of the channel length; W = 24 μm; V_S=V_B=0 V.

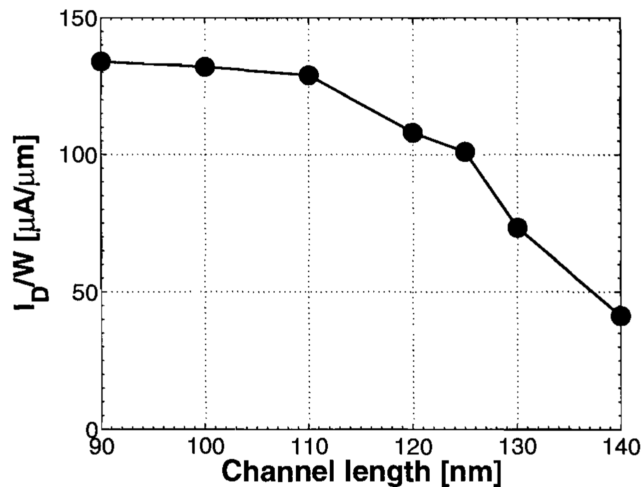

Figure 3.27: On-state drain current (measured at V_G - V_t = 1V) of surround gate vertical nMOS transistors as a function of the channel length; W = 24μm; V_S=V_B=0V.

3.7 Discussion

In this chapter a novel, fully CMOS compatible self-aligned second oxidation process, called spacer or fillet local oxidation (FILOX), is described and characterized. The FILOX process allows the gate overlap capacitance of CMOS compatible vertical MOS transistors to be reduced. Single, double and surround gate FILOX vertical MOSFETs have been fabricated and characterized successfully. The surround gate layout allows the drain current per unit of silicon surface to be maximized. The single gate layout allows the fabrication of independently biased gates on each side of the active pillar of the device, with a common drain contact on the top of the pillar. Finally, the double gate layout could be used to achieve fully depleted operation of the devices. Good electrical characteristics of devices with channel length down to 90nm have been demonstrated.

The gate overlap capacitance reduction ensuing from the FILOX process was quantified with a structural characterization of SEM cross-sections of the pillar sidewall of the vertical MOSFETs fabricated. Then the gate overlap capacitance of vertical MOSFETs with and without FILOX was compared with that of a planar MOSFET. In order to make a quantitative comparison, the same design rules were applied for the layout of the three structures. Comparing the two vertical transistors, the FILOX process was found to reduce the drain overlap capacitance by a factor of 2 and the source overlap capacitance by a factor of 5. Comparing the vertical FILOX transistor with the lateral transistor, the two transistors were found to have similar gate overlap capacitance. Thus the FILOX process eliminates one of the main disadvantages of vertical MOSFETs in comparison with planar MOSFETs with a CMOS compatible fabrication process.

Single, double and surround gate vertical MOSFETs have been fabricated with

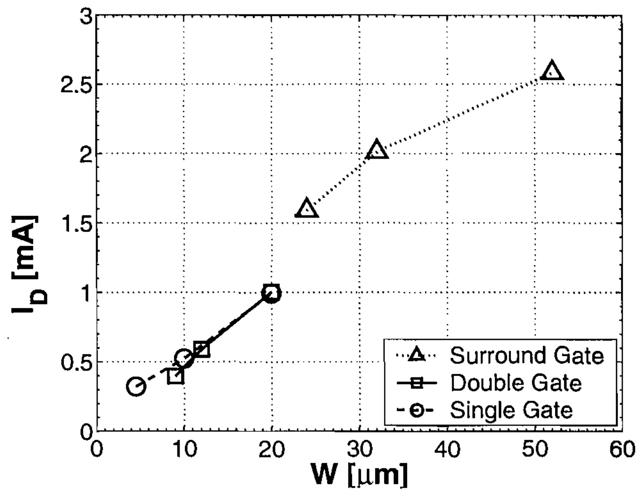

Figure 3.28: On-state drain current as a function of the channel width of single, double and surround gate FILOX vertical nMOSFETs with estimated channel length of 130nm; V_{DS} = 1V; V_G - V_t = 1V; V_S = V_B=0V.

the FILOX process and yielded good electrical characteristics. Transistors with different channel widths have been fabricated for each of the three layouts. Electrical measurements were performed in order to evaluate the precision of the transfer of the channel width drawn on the mask on the real devices fabricated. With this objective the on-state drain current, extracted with constant gate voltage overdrive (V_{GS} - V_t = 1 V, V_{DS} = 1 V), has been measured and plotted as a function of the channel width of surround, single and double gate FILOX vertical MOSFETs in figure 3.28. The on-state drain current increases with the channel width, as expected. Within transistors with the same structure, the on-current is approximately proportional to the channel width. Single and double gate MOSFETs lie approximately on the same I_D(W) line. On the other hand, the surround gate devices lie on a I_D(W) line which is slightly shifted to higher drain currents compared with the trend found for single and double gate devices. This may be due to two different factors. First, the gate spacer removal process described in section 3.2 affected single and double gate MOSFETs but not surround gate MOSFETs. Due to the isotropy of the etch process, the portion of the gate spacers of single and double gate MOSFETs protected by the Gate spacers removal mask may have been partially etched, yielding a channel width lower than expected. Second, the gate of the surround gate vertical MOSFETs wraps around the rectangular pillar. At the corners of the pillar, the electrostatic coupling between the gate and the channel of the device is enhanced due to the corner effect [94], boosting the drive current of the devices.

Due to the nonuniformity of the active pillar dry etch, a distribution of pillar heights was obtained on the same silicon wafer. The resulting range of channel lengths was quantified by means of SEM cross-sections and SIMS analysis. The channel lengths of the devices were found to range between 90 nm and 140 nm, and the effect

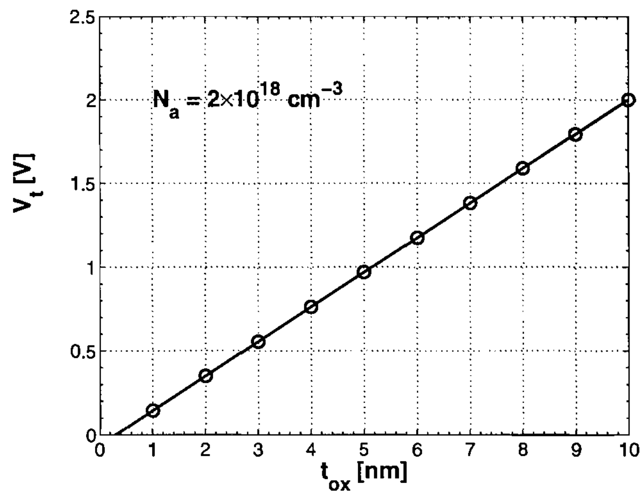

Figure 3.29: Threshold voltage of long-channel nMOSFETs (obtained from equation 2.10) plotted as a function of the gate oxide thickness for a channel doping concentration of 2×10^{18} cm^{-3}.

of channel length variation on the performance of surround gate vertical MOSFETs fabricated with the FILOX process could be assessed. The threshold voltage of the devices was found to decrease from 1.6V for MOSFETs with 140 nm channel length to 0.8V for 90nm devices. All the devices have a 3.3 nm thick gate oxide, measured on the horizontal <100> surface of test wafers. In vertical MOSFETs, the gate oxide is grown on the vertical pillar sidewall which has <110> crystallographic orientation. A 40% difference between the oxide thickness on <100> and <110> surfaces has been reported in the literature [92], yielding an oxide 4.6 nm thick on the vertical sidewalls of the devices. Figure 3.29 shows a plot of the theoretical threshold voltage (calculated from equation 2.10) of long channel MOSFETs with the same body doping concentration as the vertical MOSFETs fabricated (2×10^{18} cm^{-3}). The figure shows that a threshold voltage of 1.6 V is expected from long channel MOSFETs with a gate oxide 8 nm thick. This value is considerably higher than the 4.6 nm oxide thickness expected on the pillar sidewall. A thicker than expected gate oxide could be due to partial or incomplete removal of the 20 nm thick stress relief oxide layer grown on the pillar sidewall to relieve the stress between the ensuing nitride layer and the silicon substrate. As described in section 3.2, the stress relief oxide was removed in a solution of hydrofluoric acid and water immediately before growth of the gate oxide. The etch time had to be optimized in order to completely remove the stress relief oxide while leaving an approximately 40 nm thick FILOX oxide on the active area and on the top of the pillar. In fact an etch longer than needed would remove the FILOX as well as the stress relief oxide. On the other hand, an etch shorter than necessary would result in partial or incomplete removal of the stress relief oxide, leaving a thin oxide layer on the pillar sidewall that would add to the gate oxide grown immediately afterwards.

Type of MOSFET	LSTP [95]	**Sidewall** [48]	**VRG** [37]	FILOX (surround)	FILOX (double)	FILOX (single)
L [nm]	75	100	50	125	125	125
t_{ox} [nm]	2.2	3	2.8	3.3	3.3	3.3
N_A [10^{18} cm^{-3}]	-	2	3.5	2	2	2
V_{DD} [V]	1.2	1.5	1.5	1	1	1
I_{on} [$\mu A/\mu m$]	410	240	100	92	82	100
I_{off} [$A/\mu m$]	1×10^{-5}	5×10^{-12}	3×10^{-11}	2.5×10^{-12}	3.7×10^{-12}	1.6×10^{-11}
V_t [V]	0.5	0.6	0.73	1.41	1.52	1.58
S [mV]	-	102	105	103	108	110
DIBL [mV]	-	70	90	50	50	50

Table 3.2: Comparison of structural and electrical parameters of single, double and surround gate FILOX vertical MOSFETs with state of the art vertical and planar MOSFETs (data from the literature); Planar LSTP = Low Standby Power planar MOSFET [95]; Sidewall = conventional CMOS compatible vertical MOSFET [48]; VRG = Vertical Replacement Gate vertical MOSFET [37]; FILOX (surround) = surround gate vertical MOSFET with FILOX; FILOX (double) = double gate vertical MOSFET with FILOX; FILOX (single) = single gate vertical MOSFET with FILOX; L = channel length; t_{ox} = gate oxide thickness; N_A = body doping concentration; I_{on} = on current (calculated at V_G - V_t = 1V, V_D = V_{DD}; for LSTP [95] calculated at V_G = V_D = V_{DD}); I_{off} = off current (calculated at V_D = V_{DD}, V_G = 0V); V_t = threshold voltage; S = subthreshold slope (calculated at V_D = V_{DD}); DIBL = drain induced barrier lowering (calculated at V_D = V_{DD}).

A comparison of the performance of FILOX vertical MOSFETs with vertical and planar MOSFETs from the literature is attempted in table 3.2. Electrical parameters of single, double and surround gate FILOX vertical MOSFETs are extracted from the transfer characteristics shown in section 3.5.3 in the drain on top measurement configuration. The reference devices from the literature are a Low Standby Power (LSTP) planar technology [95], a conventional CMOS compatible vertical MOSFET (Sidewall VMOS) [48] and a Vertical Replacement Gate (VRG) MOSFET [37]. The highest on-current among FILOX vertical MOSFETs was measured on the single gate device. The measured value of 100 $\mu A/\mu m$ is the same as reported for the VRG MOSFET. On the other hand, the on-current of FILOX vertical MOSFETs is considerably lower than both Sidewall VMOS and LSTP MOSFET. This is due to the thicker gate oxide and to the longer channel of the FILOX devices. On the other hand, the FILOX vertical MOSFETs exhibit lower values of off-state drain current, subthreshold slope and DIBL than the other technologies compared. In particular, the surround gate device exhibits the lowest values of subthreshold slope and off-state drain current among the FILOX MOSFETs.

3.8 Summary

In this chapter the fabrication process of surround, single and double gate vertical MOSFETs has been described. For the first time, transistors with the three different structures have been fabricated on a single wafer using a new spacer or fillet local oxidation (FILOX) process. The devices fabricated have channel lengths down to 90 nm and a gate oxide 3.3 nm thick measured a horizontal <100> surface. The fabrication process is epitaxy free and CMOS-compatible.

A quantitative comparison has been made of the overlap capacitance of the FILOX vertical MOSFET and a conventional lateral MOSFET using a 100 nm baseline technology. The gate/drain overlap capacitance of the FILOX vertical MOSFET is found to be 1.4 times lower and the gate/source overlap capacitance 1.2 times lower than the lateral MOSFET. These results demonstrate the effectiveness of the FILOX process in reducing gate overlap capacitance in vertical MOSFETs.

Electrical characteristics of single, double and surround gate transistors have been presented. The gate spacer removal process has been found to successfully and selectively remove excess gate spacers to fabricate single and double gate MOSFETs. The transfer characteristics measured with the drain on top or the drain on bottom of the active pillar are remarkably symmetrical. Drive currents up to 100 $\mu A/\mu m$, off-state drain leakage currents of the order of 10^{-11} $A/\mu m$, subthreshold slopes down to 103 mV/dec and 50 mV DIBL have been achieved for FILOX vertical MOSFETs with 125 nm channel length.

The dependence of the threshold voltage of short channel, surround gate FILOX vertical MOSFETs on the channel length has been investigated. A threshold voltage roll off between 1.6 V and 0.8 V has been measured on devices with 140 nm and 90 nm long channels. In order to minimize the threshold voltage roll off of the devices, it is necessary to optimize process parameters to ensure that the stress relief oxide layer grown on the pillar sidewall in the early stages of the fabrication process is completely removed before growing the gate oxide.

Chapter 4

Asymmetric Gate Induced Drain Leakage and Body Leakage in FILOX Vertical MOSFETs

4.1 Introduction

CMOS compatible vertical MOSFETs are easier to integrate in conventional CMOS technologies, but they are affected by a considerable parasitic gate overlap capacitance. In chapter 3, a novel process developed to reduce gate/drain and gate/source overlap capacitance in CMOS compatible vertical MOSFETs, called the Fillet Local Oxidation (FILOX) process [70–77], has been described. The structure of a FILOX vertical MOSFET is illustrated schematically in figure 4.1, where it can be seen that the FILOX oxide reduces the overlap capacitance between the gate and the source-drain electrodes. A further potential disadvantage of vertical MOSFETs is the inherent asymmetry of the structure in drain on top and drain on bottom configurations, which might make it difficult to use source and drain terminals interchangeably in different circuit architectures. On the contrary, this is not an issue in planar MOSFETs, where the interchange of source and drain has no effect on the electrical characteristics. The asymmetry of vertical MOSFETs is potentially exacerbated in the FILOX process, because any bird's beak arising from the FILOX oxidation will be different at the top and bottom of the pillar. Further study of the asymmetry of the electrical characteristics of vertical MOSFETs is essential to determine whether this is an issue, and if so, to identify the physical mechanisms responsible for asymmetric behavior.

In this chapter the gate induced drain leakage (GIDL) and the body leakage of FILOX vertical MOSFETs are investigated in drain on top and drain on bottom configurations to identify the effect of the asymmetric source/drain geometry on the off-state drain leakage. The temperature dependence of the leakage currents is also studied to identify the physical mechanisms responsible for the leakage in the two

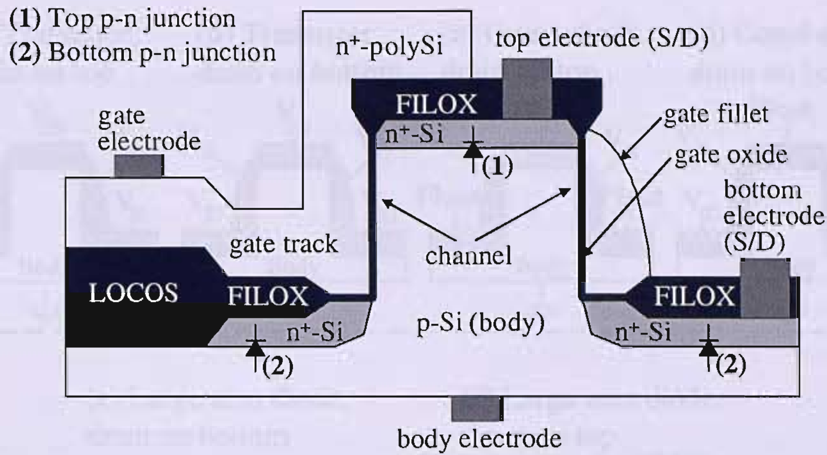

Figure 4.1: Schematic cross-section of a surround gate FILOX vertical MOSFET (see chapter 3); S/D = source-drain. The figure shows the asymmetric top and bottom structure of the body-drain p-n junctions.

configurations, and simulations are performed to confirm the mechanisms. It is shown that both the gate induced drain leakage and the body leakage of vertical MOSFETs are asymmetric when the source and drain are interchanged, GIDL being higher in the drain on bottom configuration and body leakage being higher in the drain on top configuration.

4.2 Experimental procedure

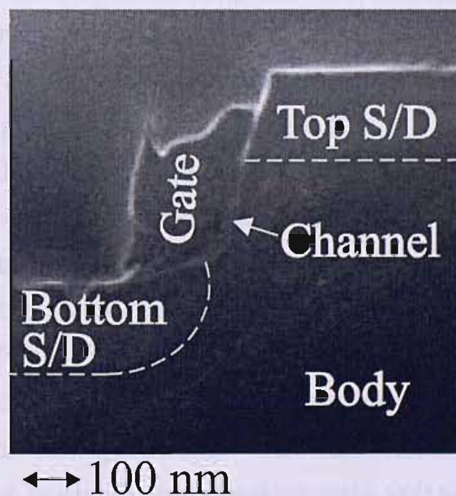

Figure 4.2: SEM cross-section of the active pillar of a surround gate FILOX vertical MOSFET with 220 nm channel length.

Surround gate, CMOS compatible vertical nMOSFETs with reduced gate overlap capacitance were fabricated with the FILOX process, described in chapter 3. The devices had a 220 nm channel length and a 3.3 nm thick gate oxide was measured

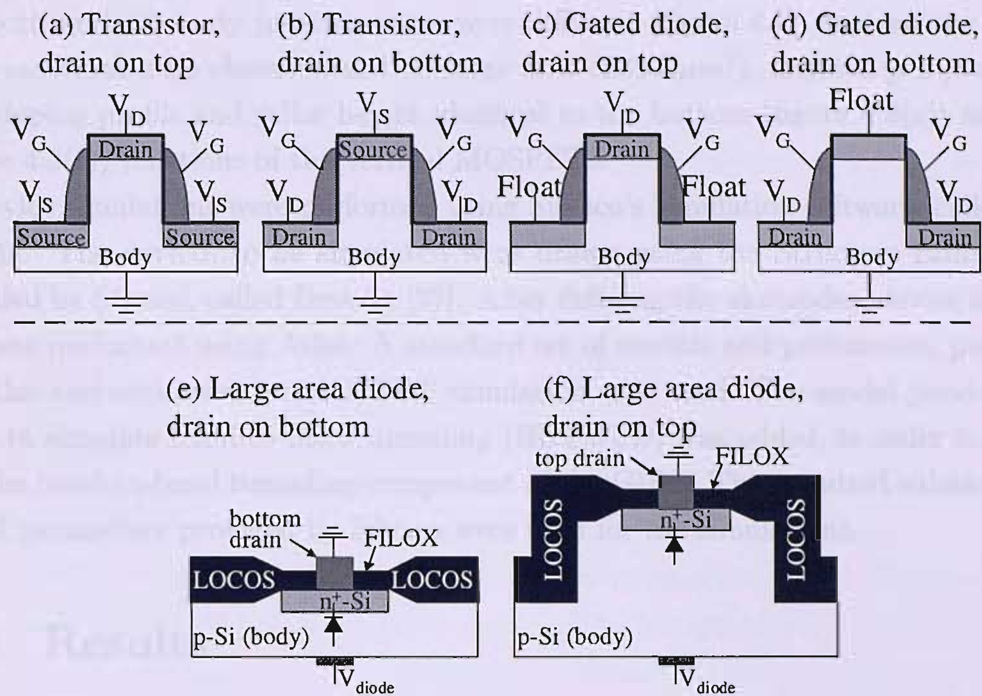

Figure 4.3: Measurement configurations used for the electrical characterization of the vertical MOSFETs. (a)-(b) Transistor measurement configuration. (c)-(d) Gated diode measurement configuration. (e)-(f) Large area, ungated diodes measurement configuration. The large area diodes characterized had an area (A_{diode}) of 22200 μm^2 and the same doping profile of the top and bottom body-drain junctions of the vertical MOSFETs (see figure 4.1).

on the horizontal <100> surface. The long channel vertical MOSFETs characterized in this chapter were fabricated on a different wafer from the short channel devices characterized in chapter 3. An SEM cross-section of a completed vertical MOSFET with 220 nm channel length is shown in figure 4.2.

Transistor electrical characterization was performed on a temperature controlled chuck linked to a Semiconductor Parameter analyzer. Initial measurements were taken at room temperature and then detailed measurements were made at different temperatures, ranging from -50°C to 200°C. Vertical MOSFETs with channel width (W) ranging between 32 and 52 μm and channel length (L) of 220 nm were characterized. Three types of electrical measurement were made, all in both drain on top and drain on bottom configurations. The first measurement was of transistor transfer characteristics for positive and negative gate voltages, with the body contact grounded (figure 4.3(a) and (b)). The second measurement was of gated diode characteristics. This measurement was made on the transistors with the source floating, the body grounded and bias applied to the gate and drain (figure 4.3(c) and (d)). The final measurement was of diode current/voltage characteristics, with the objective of investigating the characteristics of the top and bottom body-drain p-n junctions. These measurements were not performed directly on the transistors, because the top

and bottom drain-body junction areas were different (figure 4.1). Instead the drain-body junctions were characterized on large area ($22200 \mu m^2$), ungated p-n junctions with doping profile and pillar height identical to the bottom (figure 4.3(e)) and top (figure 4.3(f)) junctions of the vertical MOSFETs.

Device simulations were performed using Silvaco's simulation software, called Atlas [96]. The devices to be simulated were drawn using the Structure Editor tool provided by Silvaco, called Devedit [97]. After defining the electrodes, device simulation was performed using Atlas. A standard set of models and parameters, provided by Atlas and optimized for MOSFET simulation, was used. The model provided by Atlas to simulate band-to-band tunneling (BBT.STD) was added, in order to simulate the band-to-band tunneling component of the GIDL. The standard values of the model parameters provided by Silvaco were used for the simulations.

4.3 Results

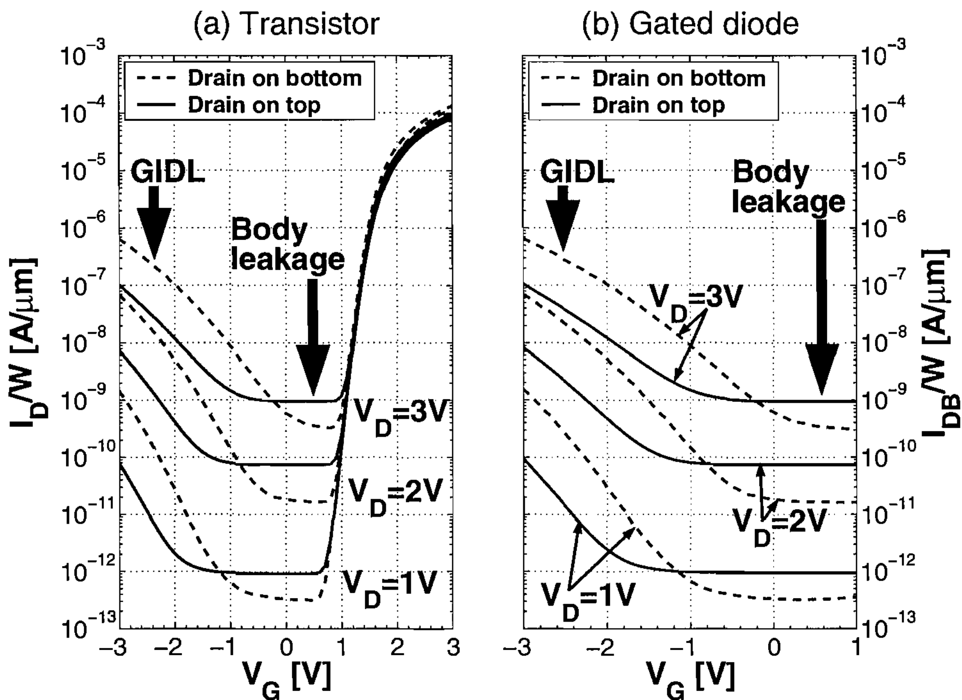

Figure 4.4: (a) Measured transfer characteristics of a typical surround gate vertical MOSFET with 32 μm channel width (W) and 220 nm channel length (L) in drain on top and drain on bottom configurations; $V_S = V_B = 0$ V. (b) Measured gated diode characteristics in drain on top and drain on bottom configurations for the same device; $V_B = 0$ V; source floating; I_{DB} = drain-body current.

Figure 4.4(a) shows typical measured transfer characteristics of the surround gate vertical MOSFETs in drain on top and drain on bottom configurations. The devices have a threshold voltage of 1.7 V in both configurations and only a small difference

in the on-state currents is observed. In contrast in the off-state region of operation a large difference (about a factor of ten) in the drain leakage currents is observed when source and drain are interchanged. Two different regions of the characteristics can be distinguished in the off-state region of operation (figure 4.4(a)). At low gate bias (V_G) the drain current is independent of V_G. This indicates a body leakage mechanism in which the current depends only on the drain-body bias. In contrast, at higher negative gate bias the drain current is strongly dependent on V_G. This indicates the presence of gate induced drain leakage, which varies with both gate bias and drain bias (V_D). The gate induced drain leakage at high negative gate bias is a factor of approximately ten higher in the drain on bottom configuration than the drain on top configuration. In contrast, the body leakage at low gate bias is lower in the drain on bottom configuration than the drain on top configuration.

To further investigate the asymmetric off-state leakage, figure 4.4(b) shows the gated diode characteristics in which the source of the vertical MOSFET is left floating. The off-state leakage can be more easily distinguished in this measurement mode, since both the subthreshold and the on-state currents are suppressed. It can be seen that the values of body leakage obtained from the gated diode measurement are similar to those obtained at low gate bias in the off-state region of the transfer characteristic. This confirms that the gate bias-independent current seen at low gate bias in figure 4.4(a) is due to body leakage. Furthermore the same asymmetry in the characteristics is observed for drain on bottom and drain on top configurations in figure 4.4(a) and figure 4.4(b). The body leakage is lower in the drain on bottom configuration, whereas the gate induced drain leakage is about a decade higher.

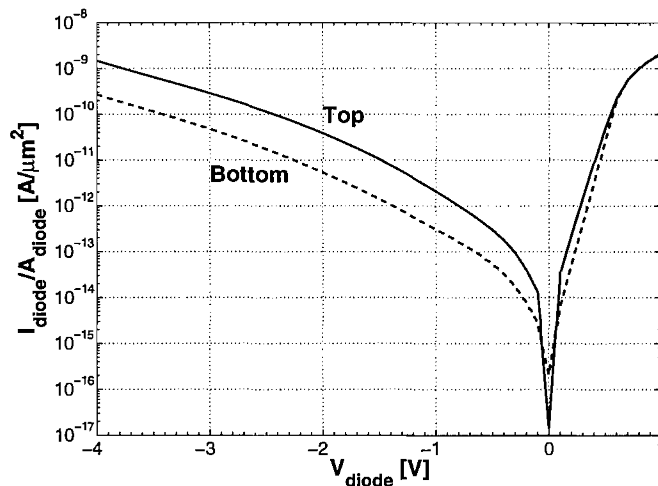

Figure 4.5: Current-voltage (I_{diode}-V_{diode}) characteristics of the top and bottom body-drain p-n junctions measured on the large area, ungated diodes shown in figure 4.3(e) and (f).

To further confirm the asymmetry in the body leakage, figure 4.5 shows the results of measurements of the current-voltage characteristics of large area, ungated diodes

(figure 4.3(e) and (f)), with the same drain-body doping profile as the transistors. The data from the top and bottom drain-body junctions are directly comparable as the diodes have the same area. In reverse bias the leakage current is a decade higher for the top (solid line) than for the bottom drain-body junction (dashed line). This result confirms the asymmetry in the body leakage, with the top junction giving higher values of body leakage than the bottom junction.

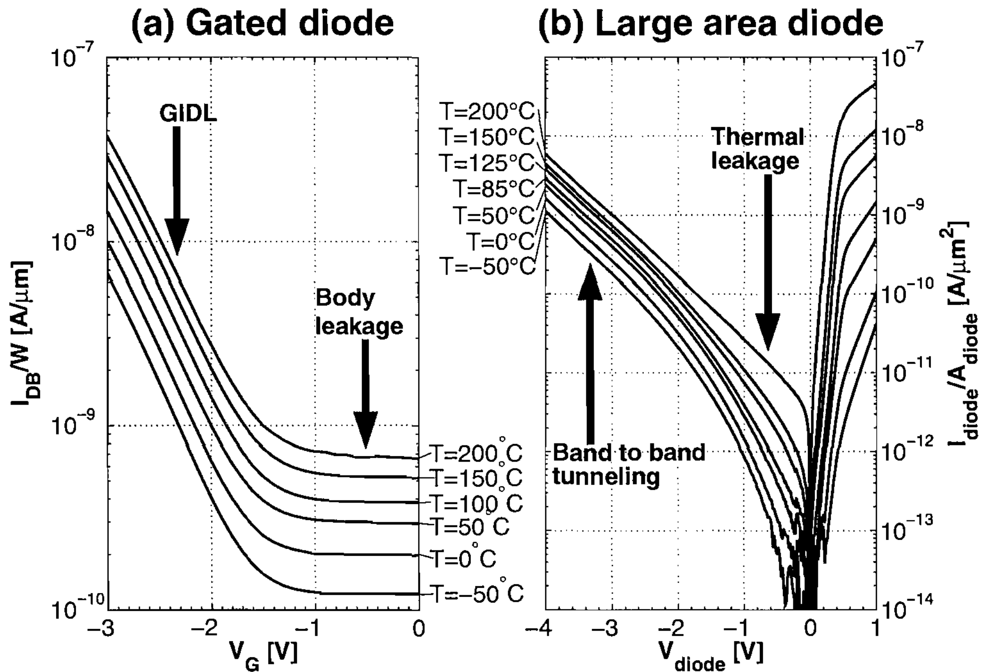

Figure 4.6: (a) Gated diode electrical characteristics measured at temperatures ranging between -50°C and 200°C on surround gate vertical MOSFETs in drain on top configuration; L=220 nm and W=52 μm; source floating; V_B = 0V; V_D = 2V. (b) Measured current-voltage diode characteristics of the bottom body-drain p-n junction at temperatures ranging between -50°C and 200°C, measured on the large area, ungated diode shown in figure 4.3(e).

In order to investigate the leakage mechanisms, figure 4.6 shows measurements of the gated diode characteristics (figure 4.6(a)) and the large area diode current-voltage characteristics (figure 4.6(b)) at different temperatures. The gated diode characteristics were measured for the drain on top configuration at a drain bias of 2V. The gated diode characteristics in figure 4.6(a) show a similar temperature dependence in the gate induced drain leakage and body leakage regions of the characteristic, indicating that a similar mechanism controls the leakage current in the two regions. The large area diode current-voltage characteristics in figure 4.6(b) show a different temperature dependence at low reverse voltages than at high. At low reverse voltages (V_{diode} around -0.5 V), a strong temperature dependence is seen at high temperatures (T > 50°C), whereas at high reverse voltages a weak temperature dependence is observed. This result indicates that different mechanisms dominate the characteristics at low

and high reverse bias.

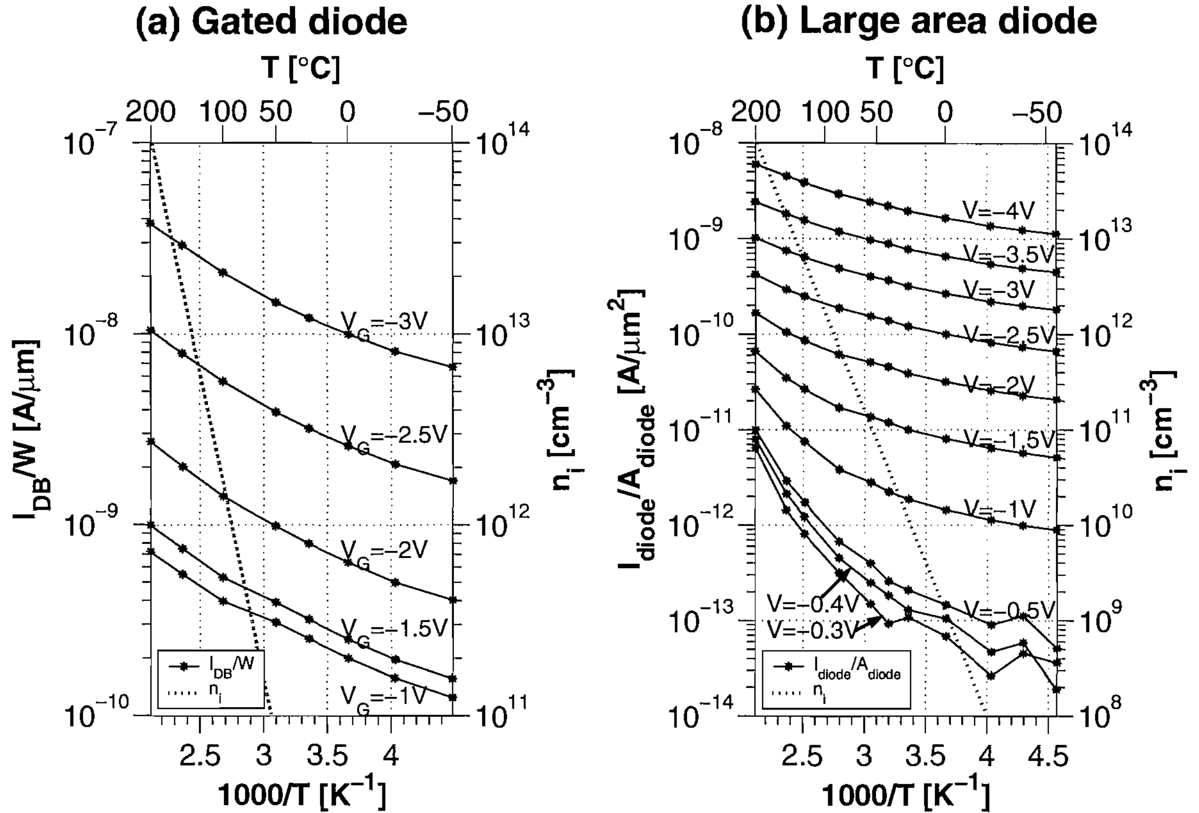

Figure 4.7: (a) Reciprocal temperature dependence of the gated diode characteristics (figure 4.6(a)), for different values of gate bias. (b) Reciprocal temperature dependence of the large area diode leakage (figure 4.6(b)), for different values of reverse bias (V = V_{diode}). The experimental data are compared with the temperature dependence of the intrinsic carrier concentration in Si (n_i) [84].

Figure 4.7 shows measurements of the reciprocal temperature dependence of the gated diode characteristics and the large area diode current-voltage characteristics. In figure 4.7(a) the gated diode current is plotted as a function of reciprocal temperature for different values of gate voltage. It can be seen that the gated diode current has a weak temperature dependence over the whole temperature range and for all values of gate voltage. In figure 4.7(b), the diode leakage is plotted as a function of reciprocal temperature for different values of reverse bias. At high reverse bias, the leakage has a weak temperature dependence, which suggests that the mechanism controlling the large area diode leakage at high bias is the same as that controlling the gated diode current. However, at low reverse bias, the temperature dependence of the diode leakage current shows a stronger temperature dependence at high temperatures (T>50°C).

4.4 Discussion

4.4.1 Leakage mechanisms

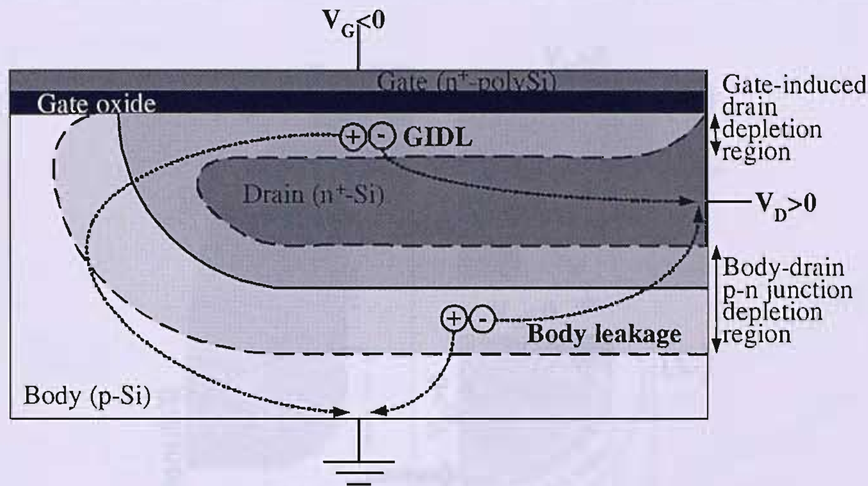

Figure 4.8: Schematic cross-section of the gate/drain overlap region of a MOSFET showing a representation of the gate induced drain leakage (GIDL) and of the body leakage.

In the off-state region of operation of a conventional lateral MOSFET, the drain leakage current is generally due to two main contributions: gate induced drain leakage and body leakage [86, 98]. An overview of the drain leakage mechanisms in MOS transistors is provided in section 2.3. A schematic representation of the two leakage mechanisms is shown in figure 4.8, which shows a cross-section of the drain region of a MOSFET. This Figure shows the depletion regions induced by a negative gate voltage and a positive drain voltage. The body-drain depletion region is due to the reverse biased body-drain p-n junction. An additional gate-induced depletion region is formed at the surface for V_{DG} >0, where the gate overlaps the drain extensions of the MOSFET. The gate-induced depletion region gives rise to band bending in the drain extensions. When the band bending exceeds the silicon bandgap, electrons can tunnel into the drain from the valence to the conduction band [86]. The generated electron-hole pairs are then collected by the drain and body contacts respectively, giving rise to gate induced drain leakage (see section 2.3.2). Band to band tunneling can also occur in the body-drain depletion region at high reverse biases, giving rise to body leakage [98]. This type of leakage is very sensitive to the body doping concentration, because an increased doping gives rise to a higher electric field and enhanced band to band tunneling. On the other hand, both gate induced drain leakage and body leakage can arise from thermal generation of carriers in the depletion regions [84, 91, 98]. This mechanism is dominant in devices with low body and drain doping concentrations. It has been demonstrated that the reciprocal temperature dependence of the thermal generation current within the depletion region is the same as

that of the intrinsic carrier concentration (n_i; see section 2.3.1). However, in the vertical MOSFETs that are investigated here, the drain and body doping concentrations are higher in order to control short channel effects and source/drain series resistance, and hence the main leakage mechanism is band to band tunneling of electrons.

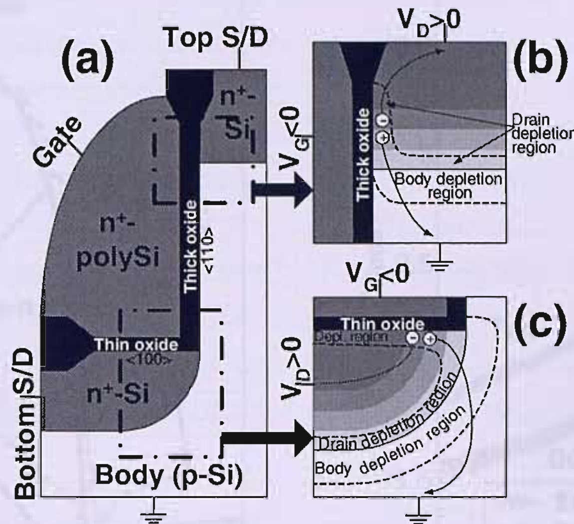

Figure 4.9: (a) Schematic cross-section of the pillar sidewall of a vertical MOSFET, including a representation of the gate induced drain leakage mechanism (b) in the top and (c) in the bottom gate/drain overlap regions. The < 100 > horizontal surface and the < 110 > vertical sidewall are indicated. The grey scale in (b) and (c) represents the area where the As doping concentration decreases rapidly. The dashed lines show the locations of the depletion regions.

In the current work, the leakage current mechanisms can be identified from the temperature dependence of the currents shown in figure 4.6 and 4.7. The results in figure 4.7(a) show that the gate induced drain leakage has a much weaker temperature dependence than the intrinsic carrier concentration, which is shown as a dotted line. A weak temperature dependence of this type is typical of band to band tunneling [91], and hence it can be inferred that this mechanism is responsible for the gate induced drain leakage seen in this work. For the drain on top configuration this gate induced drain leakage occurs where the gate spacer overlaps the n^+-doped drain at the top of the pillar, as shown schematically in figure 4.9(b). For the drain on bottom configuration, the gate induced drain leakage occurs where the gate spacer overlaps the n^+ drain at the bottom corner of the pillar, as shown in figure 4.9(c). A similar weak temperature dependence is seen at high reverse bias in figure 4.7(b) for the diode reverse leakage, and hence this leakage can also be attributed to band to band tunneling. At low reverse bias and high temperatures, the temperature dependence is much stronger and approaches the slope of the intrinsic carrier concentration. At these temperatures the leakage current is dominated by thermal generation of carriers within the depletion region [84].

4.4.2 Asymmetric body leakage

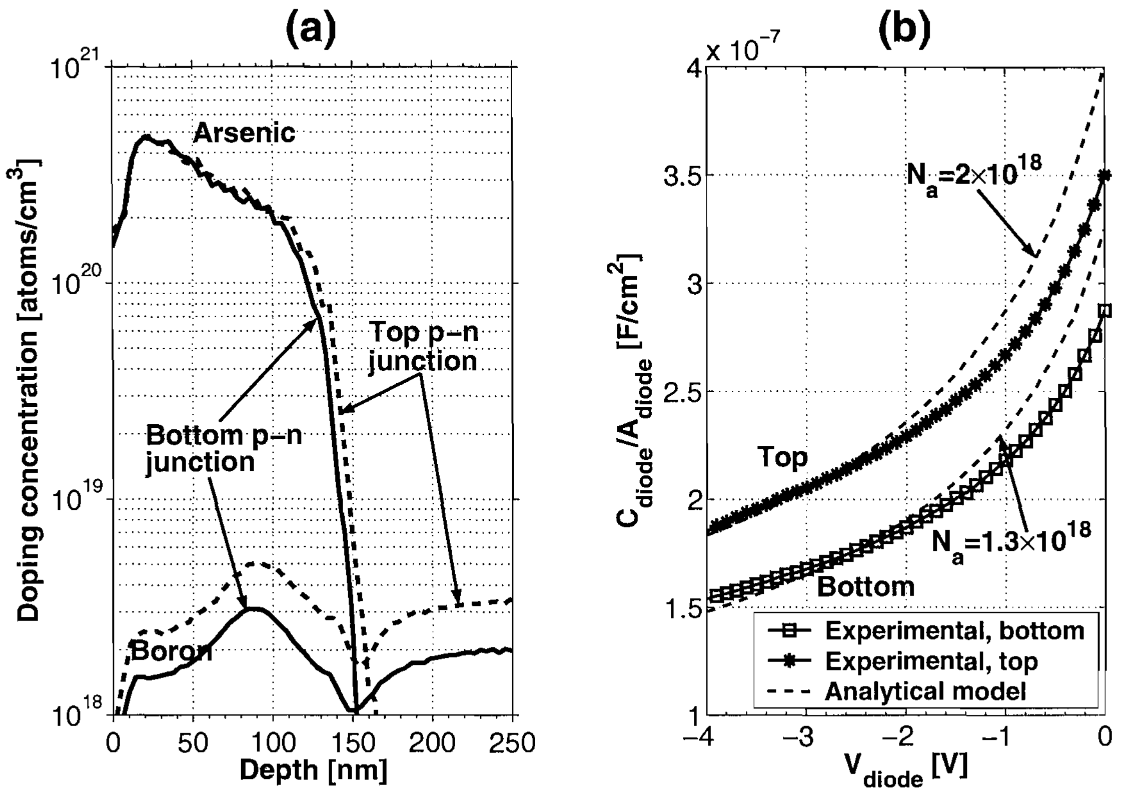

Figure 4.10: (a) SIMS (secondary ion mass spectroscopy) measurements of the doping profiles of the top and bottom body-drain p-n junctions (indicated in figure 4.1) of a FILOX vertical MOSFET. (b) Capacitance-voltage (C_{diode}-V_{diode}) characteristics of the top and bottom body-drain p-n junctions, measured on the large area, ungated diodes shown in figure 4.3(e) and (f); the measurement frequency was 1MHz; N_a = acceptor doping concentration. The experimental results are compared with the prediction of an analytical model for an abrupt n^+-p junction.

As shown in figure 4.5, the body leakage is a factor of approximately ten higher in the drain on top configuration than the drain on bottom. The dominant body leakage mechanism at room temperature is band to band tunneling, as demonstrated in figure 4.7(b). Thus the body doping has to be considered as a source of the asymmetry because the band to band tunneling current is very sensitive to the doping concentration. A high doping enhances the band bending and the electric field across the reverse biased body-drain junction. To investigate the role of the body doping, SIMS (secondary ion mass spectroscopy) profiles were measured for the top and bottom body-drain p-n junctions, and the results are presented in figure 4.10(a). These profiles show that the average body doping at the top p-n junction ($N_a \approx 3 \times 10^{18} cm^{-3}$) is higher than that at the bottom p-n junction ($N_a \approx 2 \times 10^{18} cm^{-3}$), which is consistent with the higher body leakage in the drain on top configuration. This interpretation is confirmed by the body-drain p-n junction capacitance-voltage plots shown in figure 4.10(b). The capacitance is lower for the bottom body-drain

junction, indicating a lower body doping concentration. Using an analytical model of an abrupt, one-sided n+-p junction to fit the capacitance-voltage characteristics gives body doping concentrations of $2\times10^{18}cm^{-3}$ and $1.3\times10^{18}cm^{-3}$ for the top and bottom body-drain p-n junctions respectively. These values of body doping concentration are in reasonable agreement with the SIMS profiles given the assumption of an abrupt p-n junction and uncertainties in the absolute values of SIMS doping concentrations.

The asymmetric doping profiles at the top and bottom of the pillar are caused by the use of a p-type well ion implantation and high temperature drive-in to dope the body at the beginning of the fabrication process (see section 3.2). After the p-well drive-in a photoresist mask was used to define the pillar and the exposed Si substrate was dry etched to create the vertical channel. During the pillar dry etch, boron impurities were removed from the area not covered by the pillar photoresist mask. The subsequent LOCOS and FILOX high temperature anneals gave rise to a higher body doping concentration on the top of the pillar than on the bottom, as shown in figure 4.10(a).

4.4.3 Asymmetric gate induced drain leakage

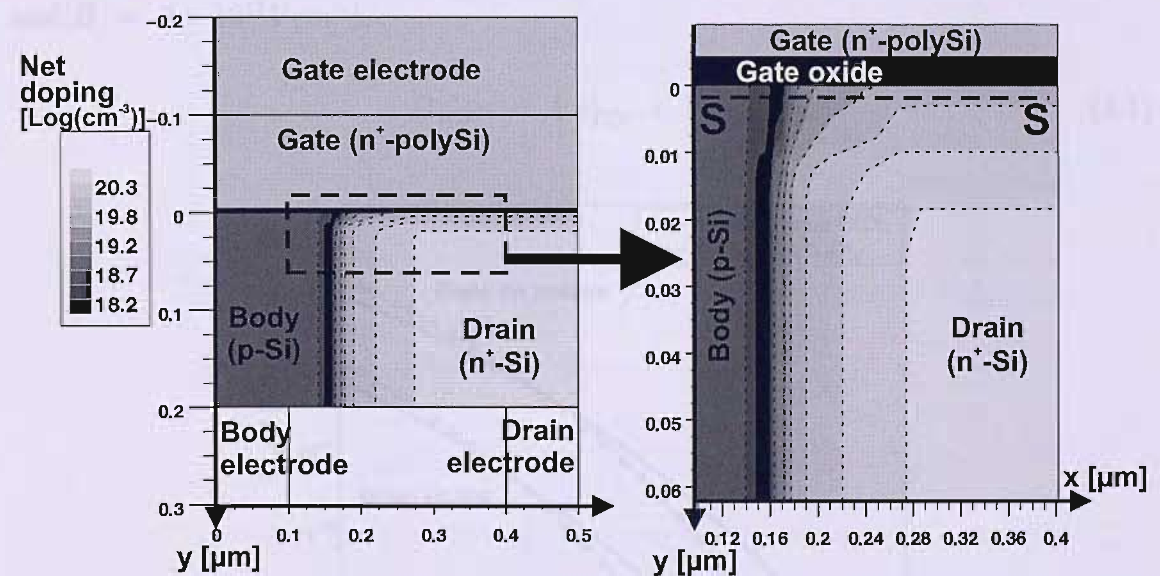

Figure 4.11: Model of the gated diodes implemented for the simulation of the gate induced drain leakage. The gate oxide thickness was used as a fitting parameter in the simulations.

As shown in figure 4.4, the gate induced drain leakage is a factor of approximately ten higher in the drain on bottom configuration than the drain on top. To investigate the origin of this asymmetry, device simulations were performed using the simplified model of the gated diodes shown in figure 4.11. Simple planar gated diodes with different gate oxide thickness were drawn using a Structure Editor software in order

to simplify the simulations as much as possible. The drain doping profile was obtained from the structural characterization of the fabricated devices. The gate oxide thickness was used as a fitting parameter in the simulations. This allowed to assess the effect of the gate oxide thickness on the band-to-band tunneling GIDL in the drain region of the devices.

The script files used for the simulations are presented in appendix B.1. Measured SIMS doping profiles (figure 4.10(a)), calibrated to measured sheet resistance values, were used in the simulations to set the drain doping profile. The body doping profile was assumed, for simplicity, to be constant throughout the structure, as its effect on gate induced drain leakage is negligible. In order to simplify the simulated structure, body and drain electrodes were placed on the back of the structure. The simulations were based on a 2-D gate induced drain leakage model [88], in which the band to band tunneling generation rate (G_{BBT}) of hole-electron pairs is a function of the total electric field ($\varepsilon_{TOT} = \sqrt{\varepsilon_x^2 + \varepsilon_y^2}$) in the gate-induced drain depletion region. This generation mechanism is implemented into the right-hand of the continuity equation [96]. The relation between G_{BBT} and ε_{TOT} implemented by the device simulator [96] is displayed in equation 4.1. The following standard values provided by the device simulator for the model parameters were used: $A = 9.66 \times 10^{18} V^{-2} s^{-1} cm^{-1}$ and $B = 3 \times 10^{17} V cm^{-1}$.

$$G_{BBT} = A\, \varepsilon_{TOT}^2\, e^{-\frac{B}{\varepsilon_{TOT}}}, \tag{4.1}$$

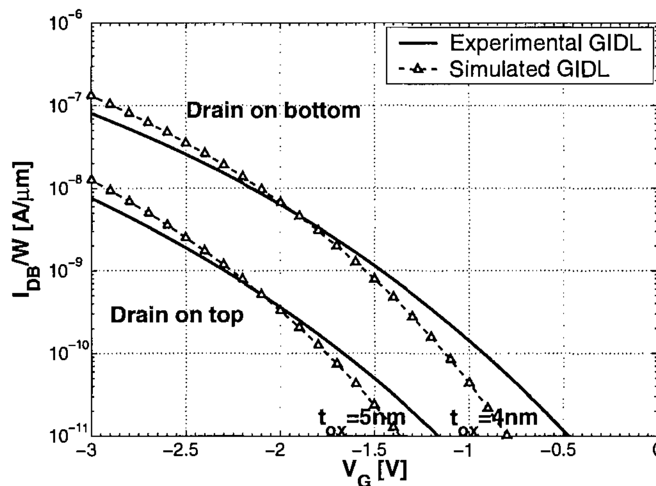

Figure 4.12: Comparison between the simulated gated diode characteristics and the experimental gated diode characteristics of a surround gate vertical MOSFET with W = 52μm and L = 220 nm; V_D=2V; V_B=0V; source floating. The experimental gate induced drain leakage curves are obtained by subtracting the body leakage component from the $I_{DB}(V_G)$ experimental characteristics of the gated diode.

Figure 4.12 shows the simulated gated diode characteristics for drain on bottom

and drain on top configurations, and also for comparison the measured data. To separate the gate induced drain leakage component of the off-state current, the body leakage current was subtracted from the measured data. Figure 4.12 shows that a reasonable fit to the measured gate induced drain leakage is obtained for a gate oxide thickness of 5 nm for the drain on top configuration and 4 nm for the drain on bottom. For the drain on bottom configuration, the gate oxide is on the horizontal <100> surface, as shown in figure 4.9, and hence the fitted value of 4 nm can be compared with a measured value of 3.3 nm obtained from <100> test wafers. The measured and fitted values of gate oxide thickness are in excellent agreement. For the drain on top configuration, the gate oxide is on the vertical <110> sidewall, as shown in figure 4.9, and the fitted gate oxide thickness is 25% higher (5 nm) than obtained in the drain on bottom configuration. This 25% difference in fitted oxide thickness compares with a measured difference of 40% between <100> and <110> surfaces reported in the literature [92]. This agreement is reasonable, given that the pillars are not completely vertical, as shown in figure 4.2.

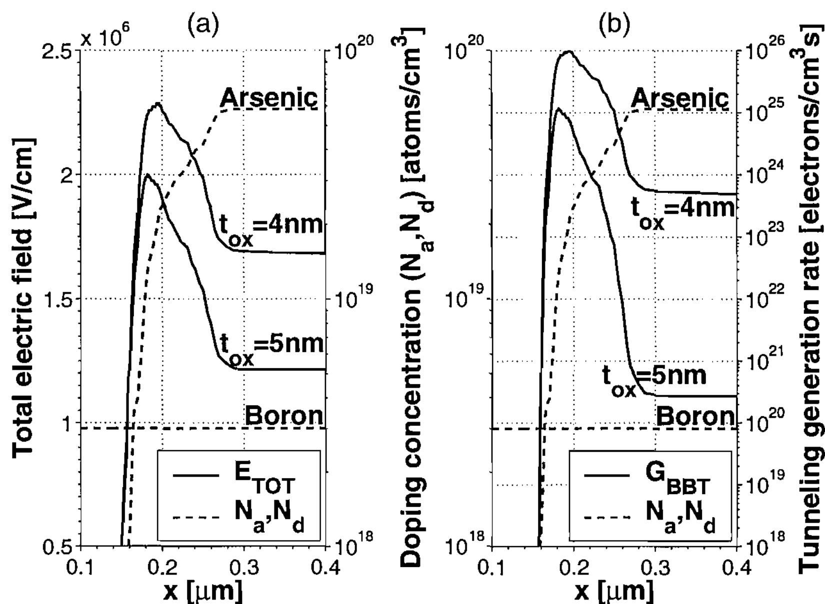

Figure 4.13: (a) Simulated total electric field (E_{TOT}) and (b) simulated band to band tunneling generation rate (G_{BBT}) along a cross-section parallel to the gate oxide in the gate-induced drain depletion region (section S-S in figure 4.11); V_D=2V, V_G=-3V, V_B=0V; N_a = acceptor doping concentration; N_d = donor doping concentration. The figures show for comparison the doping profile along the cross-section.

Figure 4.13 shows the simulated total electric field (E_{TOT}) and the band to band tunneling generation rate (G_{BBT}) on a cross-section parallel to the gate oxide in the gate-induced drain depletion region (section S-S in figure 4.11). The 4 nm gate oxide yields a higher electric field (figure 4.13(a)) and, as a consequence, boosts the band to band tunneling generation rate (figure 4.13(b)) and the gate induced drain leakage. The arsenic doping profiles are also plotted in figure 4.13, and it can be seen that the

electric field has a maximum in the portion of the gate-induced drain depletion region close to the drain-body junction, where the arsenic doping concentration decreases rapidly. This sharp peak in the electric field gives a similar sharp peak in the band to band tunneling generation rate in the same physical location. In fact, the band to band tunneling generation rate at this location is more than two decades higher than that at the peak of the arsenic profile. This result indicates that the gate induced drain leakage is highly localised, and therefore it is not influenced by the area of the gate/drain overlap. The asymmetry in the gate overlaps at the top and bottom of the pillar can therefore be discounted as an explanation for the asymmetric gate induced drain leakage. The presence of asymmetric bird's beaks from the fillet local oxidation process (FILOX), which would give rise to further asymmetry in the gate overlaps at the top and bottom of the pillar, can also be discounted as an explanation for the asymmetry. It can therefore be concluded that the asymmetric gate induced drain leakage can be explained solely in terms of the different gate oxide thicknesses on the horizontal <100> and vertical <110> surfaces.

The asymmetry in the drain leakage currents of vertical MOSFETs could be used to advantage if the transistors were fabricated on <110> wafers instead of <100> wafers. For this arrangement a thin gate oxide would be obtained on the vertical <100> pillar sidewall, whereas a thicker oxide would be obtained on the horizontal <110> surface. Both the gate induced drain leakage and the body leakage would then be lower in the drain on bottom configuration. In this situation, vertical MOSFETs operating in the drain on bottom configuration would provide lower off-state leakage than conventional planar MOSFETs, which could prove useful in applications that require low standby power.

4.5 Summary

In this chapter experimental evidence of asymmetric leakage currents in surround gate FILOX vertical MOSFETs with reduced gate overlap capacitance is presented. The asymmetry is observed in the transfer characteristics of the devices when the source and the drain are interchanged, with gate induced drain leakage (GIDL) being higher in the drain on bottom configuration and body leakage being higher in the drain on top configuration. The temperature dependence of the leakage currents has been analysed and band to band tunneling of electrons from the valence band to the conduction band identified as the dominant leakage mechanism. The asymmetric body leakage is process induced, and arises from a slightly larger body doping concentration on the top of the pillar than on the bottom due to the use of a well implant for the body doping. On the other hand, the asymmetric gate induced drain leakage is explained by a thicker gate oxide on the vertical <110> pillar sidewall than on the horizontal <100> wafer surface. The thinner gate oxide at the bottom of the

pillar increases the electric field and enhances the band to band tunneling, which is the cause of the gate induced drain leakage. The good agreement between the simulated and measured leakage characteristics of the devices is a strong indication that the fillet local oxidation process (FILOX) has a negligible impact on the asymmetric drain leakage currents of the long channel (220 nm) FILOX vertical MOSFETs characterized in this chapter.

Chapter 5

Dielectric pocket vertical MOSFET process development

5.1 Introduction

The dielectric pocket concept was first introduced by Jurczak et al. [99] as an alternative to pocket ion implantation in order to suppress the short channel effects in conventional lateral MOSFETs. Collaborative research between the Universities of Liverpool and Southampton later extended the concept to vertical MOSFETs [75, 100, 101]. Device simulations showed that the incorporation of a dielectric pocket between drain and body of a vertical MOSFET gave enhanced control over the short channel effects together with lower off currents. The simulations were based on an epitaxial channel approach to the fabrication of the device [75, 100–102]. In this chapter, a simple CMOS-compatible dielectric pocket fabrication process is proposed that delivers the above benefits without the requirement for epitaxy. This novel fabrication process is based on a polysilicon spacer approach [78–80]. A detailed description of the process development performed to optimize device fabrication is provided in this chapter. The novel process allows vertical MOSFETs with shallow drain junctions to be fabricated. This is achieved without adding complexity to the process flow and without requiring challenging photolithography.

5.2 The concept of dielectric pocket in a vertical MOSFET

Figure 5.1 shows the cross-section of a dielectric pocket vertical MOSFET. An oxide layer, called the dielectric pocket, is inserted between the drain and the body of the device to confine the drain region to the perimeter of the pillar. In vertical MOSFETs the introduction of an insulating layer between drain and body is simpler than in

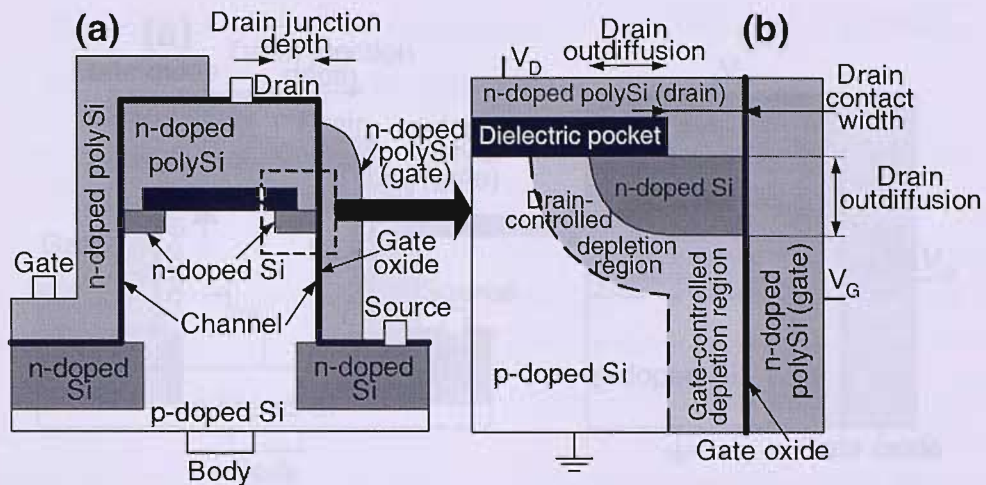

Figure 5.1: (a) Schematic cross-sections of a dielectric pocket vertical nMOSFET. (b) Magnification of the drain/channel junction of the device, showing the gate-controlled and the drain-controlled depletion regions in the body, assuming on-state operation ($V_D > 0$ and $V_G > V_t$).

planar MOSFETs because the oxide layer and the polysilicon drain of the device can be stacked on top of each other in the early stages of the device fabrication. The drain dopants outdiffuse from the contact region between the dielectric pocket and the gate oxide (labeled "Drain contact width" in figure 5.1) to form a shallow drain junction. Figure 5.1(a) shows that the drain junction depth is given by the drain contact width plus the lateral outdiffusion beneath the dielectric pocket (labeled "Drain outdiffusion" in figure 5.1). This approach allows short channel effects to be suppressed in vertical MOSFETs with sub-100nm channel length without requiring any challenging photolithography. Devices with ultra-short channel length can be integrated in a technology with relaxed photolithography (e.g. 0.35 μm technology), thereby reducing processing costs compared to the corresponding planar technology node. Figure 5.1(b) shows the role of the dielectric pocket in suppressing short channel effects. The dielectric pocket insulates the body of the device from the drain except for the contact region around the perimeter of the pillar. The shallow drain junction suppresses the short channel effects and this allows the threshold voltage of the vertical MOSFET to be tuned by reducing the body doping concentration. The dielectric pocket moreover reduces significantly the area of the body/drain p-n junction and the junction capacitance of the devices.

As a comparison, figure 5.2 shows a schematic cross-section of a conventional, CMOS compatible vertical MOSFET [48]. The main drawback of this structure is that the drain junction depth, shown in figure 5.2(a), is equal to half the width of the active pillar. Moreover it is not possible to ion implant pockets to suppress the short channel effects. Figure 5.2(b)) shows that in the center of the transistor pillar, the drain-body depletion region is controlled only by the drain and is independent

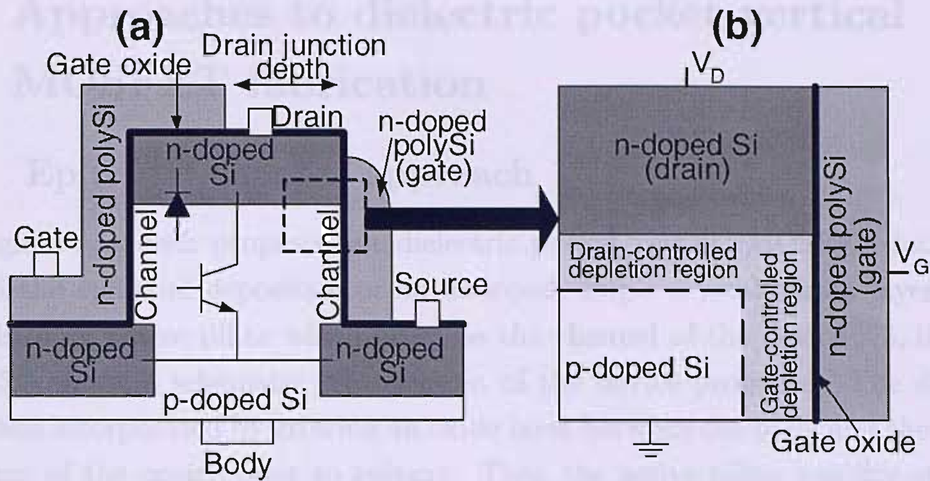

Figure 5.2: (a) Schematic cross-sections of a conventional CMOS compatible vertical nMOSFET. (b) Magnification of the drain/channel junction of the device, showing the gate-controlled and the drain-controlled depletion regions in the body, assuming on-state operation ($V_D > 0$ and $V_G > V_t$).

Dielectric pocket vertical MOSFET	Conventional vertical MOSFET
Shallow drain junction	Deep drain junction
Dielectric pocket suppresses SCEs	SCEs due to absence of pockets
Body doping can be optimized	High body doping necessary
Dielectric pocket screens drain and body	Body punchtrough path in the center of the pillar
Dielectric pocket reduces the drain/body junction capacitance	Large drain/body overlap area and high parasitic capacitance

Table 5.1: Advantages of a dielectric pocket vertical MOSFET in comparison with a conventional CMOS compatible vertical MOSFET.

of the gate bias. This gives rise to DIBL, subthreshold current degradation, bulk punchthrough and parasitic bipolar effects. A high dose body doping concentration is required to counteract these effects, leading to several drawbacks, such as high threshold voltage values, increased body factor, junction capacitance and junction leakage current. Table 5.1 summarizes the advantages introduced by dielectric pocket vertical MOSFETs in comparison with the conventional device structure.

5.3 Approaches to dielectric pocket vertical MOSFET fabrication

5.3.1 Epitaxial channel approach

The original approach proposed for dielectric pocket vertical MOSFET fabrication required the epitaxial deposition of an undoped, single crystal silicon layer on the sidewalls of an active pillar which acted as the channel of the device [75, 100–102]. Figure 5.3 shows a schematic cross-section of the device proposed. The dielectric pocket was incorporated by growing an oxide layer between the body and the polysilicon drain of the device prior to epitaxy. Then the active pillar was dry etched in the silicon substrate. A time-controlled oxide overetch provided a recessed dielectric pocket which permitted seeding of the epitaxial channel, deposited by epitaxial growth.

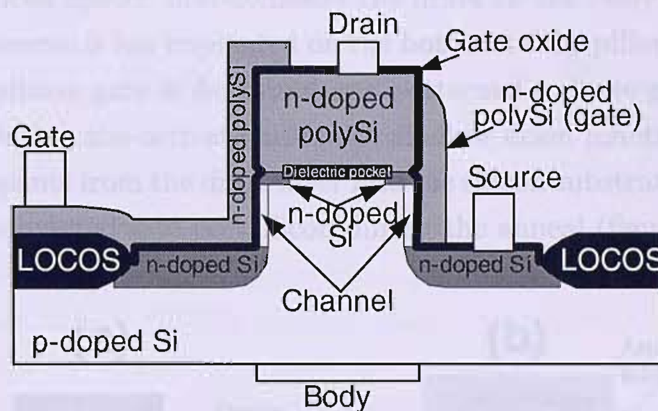

Figure 5.3: Schematic cross-section of the active pillar of a dielectric pocket vertical MOSFET fabricated with the epitaxial channel approach.

This approach is very promising but introduces a high level of complexity in the fabrication process. The most challenging step is the epitaxial growth of the channel of the device. Due to the different orientation of the silicon substrate and of the vertical pillar sidewalls, the control of growth rate and uniformity of the epitaxial layer is very challenging. Moreover, epitaxial growth is a low-throughput process. Finally, the junction depth of the device is set by the time-controlled overetch of the dielectric pocket and by the thickness of the epitaxial channel, which are difficult to control.

5.3.2 Polysilicon spacer approach

Overview of the fabrication process

Figure 5.4 shows an overview of the key process steps in the polysilicon spacer approach to the fabrication of dielectric pocket vertical MOSFETs. In this case, the connection between the polysilicon drain and the body of the device is created by an anisotropic silicon etch to form a polysilicon spacer on the sidewall of the pillar.

The process begins with the deposition of the drain stack comprising a thin oxide layer and an arsenic-doped amorphous silicon layer. Then an oxide mask is patterned and the two layers are etched down to the silicon substrate (figure 5.4(a)). A thin amorphous silicon layer is deposited in order to connect the drain and the body of the device. The thin oxide layer is completely encapsulated between the amorphous silicon and the silicon substrate, forming a dielectric pocket (figure 5.4(b)). The amorphous silicon layer and the silicon substrate are then anisotropically etched, leaving an amorphous silicon spacer that connects the drain to the body of the device (figure 5.4(c)). The source is ion implanted on the bottom of the pillar, then a gate oxide is grown. A polysilicon gate is deposited and patterned to leave gate spacers on the pillar sidewall. During the activation anneal, shallow drain junctions are formed by outdiffusion of dopants from the drain layer into the silicon substrate. The amorphous silicon spacer is converted into polysilicon during the anneal (figure 5.4(d)).

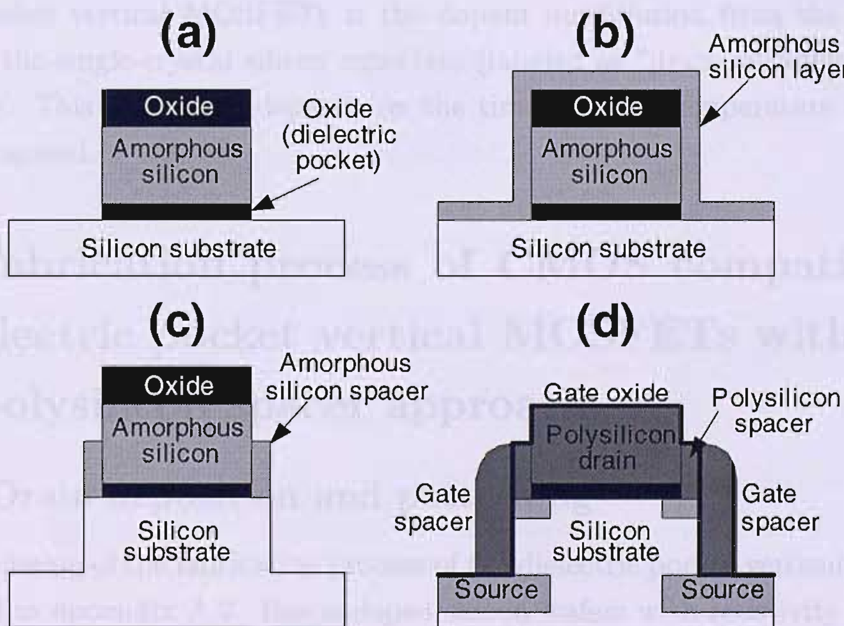

Figure 5.4: Process overview of the polysilicon spacer approach to the fabrication of dielectric pocket vertical MOSFETs.

CMOS compatibility

The novel fabrication process described provides several benefits from a process integration point of view. First, it is epitaxy-free, as the thin amorphous silicon layer can be deposited in a high throughput LPCVD furnace. Second, it allows integration of devices with ultra-short channel length in a planar CMOS technology with relaxed photolithography rules. Third, it is CMOS compatible, as it allows integration of both p-type and n-type vertical MOSFETs with planar CMOS transistors by adding only two extra masks. The first mask is needed to protect the active area of the planar MOSFETs from ion implantation or etch damage and the second mask is used to pattern the vertical pillars of the surround gate vertical MOSFETs.

Control of the critical dimensions of the device

Control of the drain contact width between the gate oxide and the dielectric pocket (see figure 5.1(b)) is essential to set the drain junction depth and to ensure the connection of drain and body around the pillar perimeter. In the novel concept proposed, the drain is connected to the channel of the device by a polysilicon spacer. The width of this spacer is proportional to the thickness of the thin amorphous silicon layer deposited by LPCVD before channel dry etch. This provides a simple and reliable method to control the drain contact width.

The other critical parameter in order to optimize the drain junction depth of dielectric pocket vertical MOSFETs is the dopant outdiffusion from the polysilicon drain into the single-crystal silicon substrate (labeled as "drain outdiffusion" in figure 5.1(b)). This parameter depends on the time and the temperature of the final activation anneal.

5.4 Fabrication process of CMOS compatible dielectric pocket vertical MOSFETs with the polysilicon spacer approach

5.4.1 Drain deposition and patterning

The batch listing of the fabrication process of the dielectric pocket vertical MOSFETs is reported in appendix A.2. Boron-doped silicon wafers with resistivity 17-33 Ωcm and <100> crystallographic orientation served as the starting material. A p-type body was formed by boron ion implantation (dose: 5×10^{14} cm^{-2}; energy: 50 keV), followed by a drive-in anneal. An initial anneal at 1100°C in oxygen for 10 minutes, performed to avoid pitting of the silicon substrate, was followed by a 30 minutes anneal at the same temperature in nitrogen, to achieve a body doping concentration

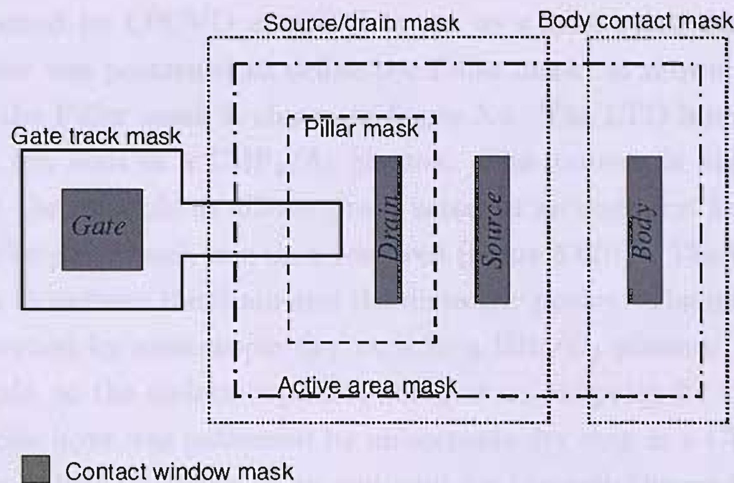

Figure 5.5: Mask layout of the fabricated dielectric pocket vertical MOSFETs. For a detailed description of the mask set, see appendix C.

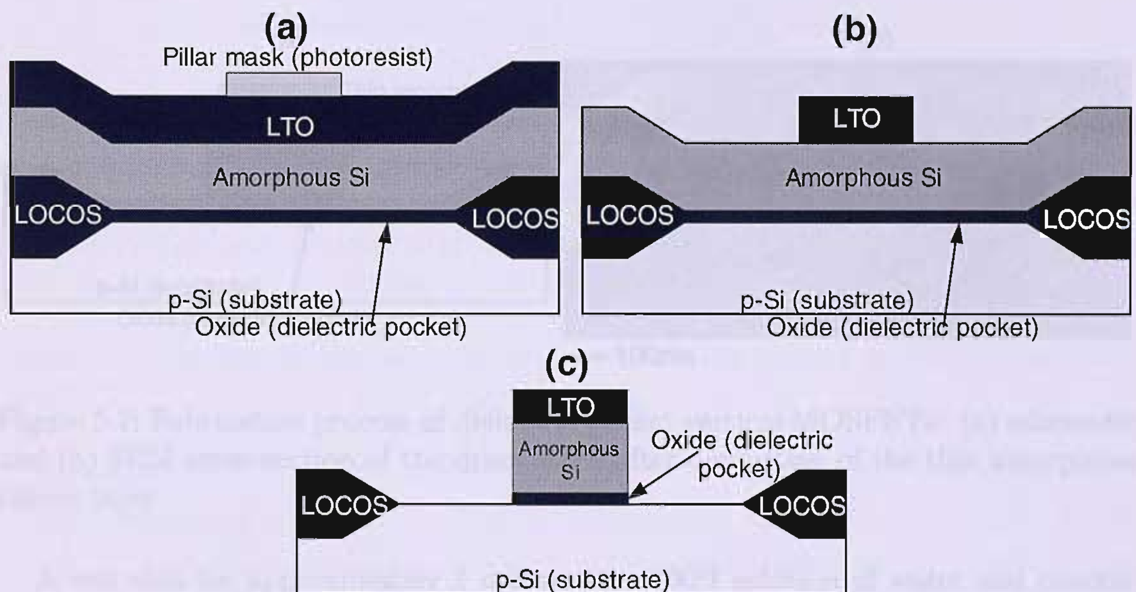

Figure 5.6: Fabrication process of dielectric pocket vertical MOSFETs: deposition and patterning of the drain and of the dielectric pocket. (a) Drain stack deposition. (b) Hard mask patterning. (c) Drain and dielectric pocket dry etch.

of about 3×10^{18} cm^{-3}. A 600 nm thick LOCOS oxide, thermally grown at 1000°C, acted as the field oxide and defined the active area of the devices. The layout of the Active area mask is shown in figure 5.5. Then the dielectric pocket layer was grown at 900°C by dry thermal oxidation to a thickness of 20 nm. Thermal oxidation was chosen to grow the dielectric pocket oxide in order to control the thickness of the layer accurately and to achieve good uniformity across the wafer. A 300 nm thick undoped amorphous silicon layer was deposited in an LPCVD (Low Pressure Chemical Vapour Deposition) furnace at 560°C and ion implanted with arsenic (dose: 5×10^{15} cm^{-2}; energy: 80 keV). A 250 nm thick LTO (Low Temperature Oxide) layer

was then deposited by LPCVD at 400°C to act as a hard mask during pillar etch. Then photoresist was patterned to define the Pillar mask, as shown in figure 5.6(a). The layout of the Pillar mask is shown in figure 5.5. The LTO layer was patterned by anisotropic dry etch in a CHF_3/Ar plasma. This process is highly selective to silicon, so that the amorphous silicon drain acted as an endpoint for the etch. The photoresist of the pillar mask was then removed (figure 5.6(b)). The LTO layer acted as a hard mask to pattern the drain and the dielectric pocket. The amorphous silicon layer was patterned by anisotropic dry etch in a HBr/O_2 plasma. This process is selective to oxide, so the dielectric pocket acted as an endpoint for the etch. Finally the thermal oxide layer was patterned by anisotropic dry etch in a CHF_3/Ar plasma, with the silicon substrate acting as an endpoint for the etch (figure 5.6(c)).

5.4.2 Formation of the drain sidewall spacers

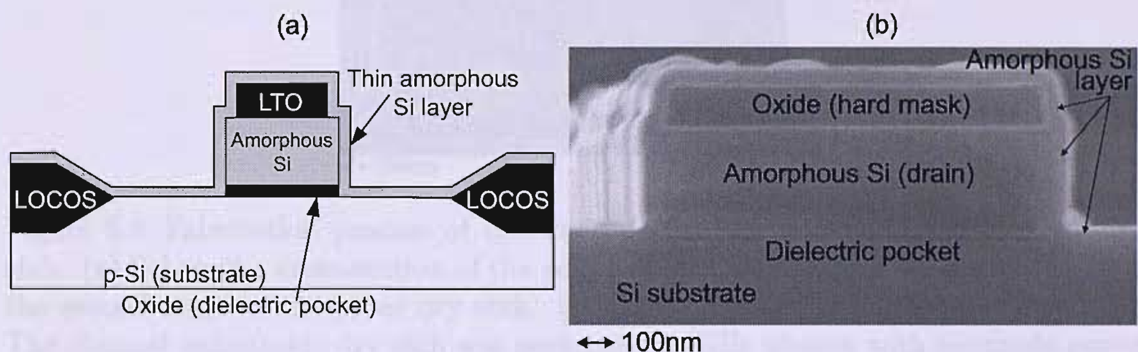

Figure 5.7: Fabrication process of dielectric pocket vertical MOSFETs: (a) schematic and (b) SEM cross-section of the drain stack after deposition of the thin amorphous silicon layer.

A wet etch for approximately 1 minute in a 100:1 solution of water and concentrated hydrofluoric acid (49%) was performed in order to remove the native oxide from the pillar sidewall and from the horizontal silicon surface. As a consequence the LTO hard mask was thinned down and laterally shrunk, leaving a step in the pillar profile, as shown in figure 5.7(a). Due to the low density of the LTO oxide, its etch rate is higher than that of the thermal oxide in the dielectric pocket. Consequently in our experiment the dielectric pocket was recessed by only 4 nm, whereas 25 nm of the LTO hard mask were removed during wet etch. Subsequently, an undoped amorphous silicon layer was deposited in a furnace by LPCVD at 560°C to a thickness of 30 or 50 nm for different process splits (figure 5.7(a)). It is worth pointing out that this is a high throughput, standard CMOS process step performed in a LPCVD furnace, which allows processing of up to 25 wafers at the same time. An SEM cross section of the drain stack at this stage of the fabrication process is shown in figure 5.7(b). The picture shows that the drain sidewall is perfectly vertical and

that the thin amorphous silicon layer is very uniform and conformal. This allowed precise control of the drain contact width between the dielectric pocket and the gate oxide, shown in figure 5.1(b), which is proportional to the thickness of the amorphous silicon layer.

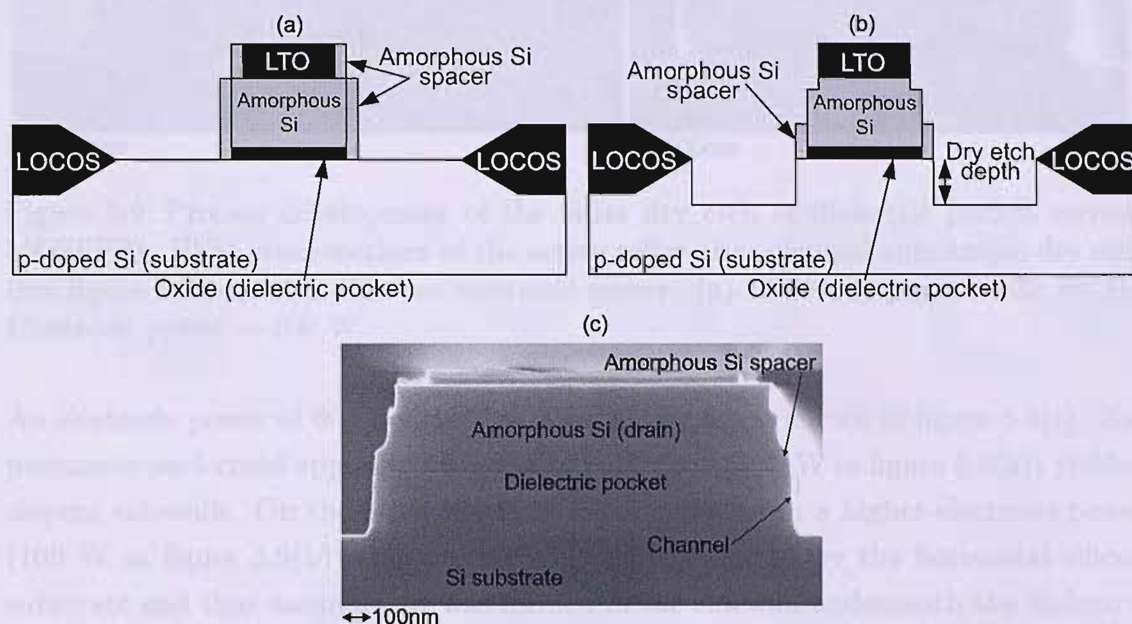

Figure 5.8: Fabrication process of dielectric pocket vertical MOSFETs: pillar dry etch. (a) Schematic cross-section of the active pillar after the first stage and (b) after the second stage of the pillar dry etch. (c) SEM cross-section after pillar dry etch. The channel anisotropic dry etch was performed in HBr plasma with electrode power = 60W.

The channel of the device was patterned by anisotropic dry etch in a HBr plasma, leaving amorphous silicon sidewall spacers connecting the drain to the body of the device, as shown in figure 5.8. This etch process was divided into 2 stages. In the first stage the thin amorphous silicon layer was dry etched (figure 5.8(a)). When this layer was completely removed, the LOCOS field oxide and the silicon substrate in the active area were exposed to the plasma. This yielded a change in the concentration of the reaction products ($SiBr_4$) in the plasma, and provided a first endpoint in the etch process, that could be detected by monitoring the optical emission of the plasma. During the second stage of the process, the channel of the device was etched in the silicon substrate (figure 5.8(b)). The channel length of the device could then be controlled by timing this second etch stage. Etch times of 18 seconds and 26 seconds were used for different process splits. The silicon etch process used was selective to oxide, and thus neither the LTO pillar hard mask nor the field oxide (LOCOS) were removed. Figure 5.8(c) shows an SEM cross-section of the active pillar after channel dry etch.

The electrode power in the etching chamber determined the energy of the ions incident on the silicon surface. This set the etch rate and the shape of the pillar sidewall.

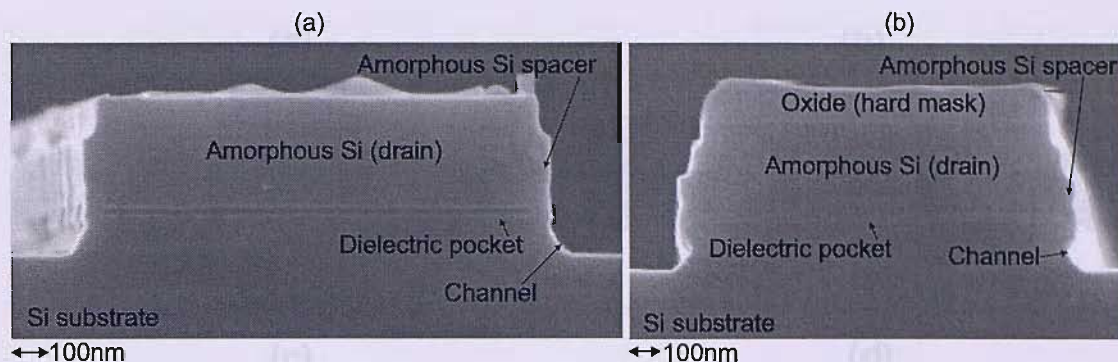

Figure 5.9: Process development of the pillar dry etch of dielectric pocket vertical MOSFETs: SEM cross-sections of the active pillar after channel anisotropic dry etch (see figure 5.8(b)) with different electrode power. (a) Electrode power = 30 W. (b) Electrode power = 100 W.

An electrode power of 60 W yielded vertical sidewalls, as shown in figure 5.8(c). Experiments performed applying a lower electrode power (30 W in figure 5.9(a)) yielded sloping sidewalls. On the other hand, in experiments with a higher electrode power (100 W in figure 5.9(b)) the ions were partially reflected by the horizontal silicon substrate and thus an undercut was formed in the sidewall underneath the dielectric pocket.

5.4.3 Source/drain ion implantation and gate stack formation

After pillar etch, a 50 nm thick sacrificial oxide layer was deposited by LPCVD at 400°C (see figure 5.10(a)). A photoresist layer was patterned in order to define the portion of the active area undergoing source/drain ion implantation. The layout of the Source/drain mask is shown in figure 5.5. The 50 nm thick oxide layer protected the channel of the device on the pillar sidewall during source/drain ion implantation with arsenic (dose: 8×10^{15} cm^{-2}; energy: 70 keV). Then the sacrificial oxide layer was removed, together with the residual oxide of the pillar hard mask, by wet etch for approximately 2 minutes in a 20:1 solution of water and concentrated hydrofluoric acid (49%).

A 3nm gate oxide was thermally grown at 800°C, followed by deposition of a 100 nm thick polysilicon layer, which was doped by tilted (45°) phosphorus ion implantation (dose: 4×10^{15} cm^{-2}; energy: 20 keV)), and annealed at 850°C for 30 minutes in nitrogen (see figure 5.10(b)). The polysilicon layer was then anisotropically dry etched in a HBr/O_2 plasma, to pattern gate spacers all around the pillar. The polysilicon track connecting the polysilicon spacers to the gate contact was protected from the etch by a photoresist mask (see figure 5.10(c)), named the Gate mask. The layout of the Gate mask is shown in figure 5.5. The polysilicon dry etch process

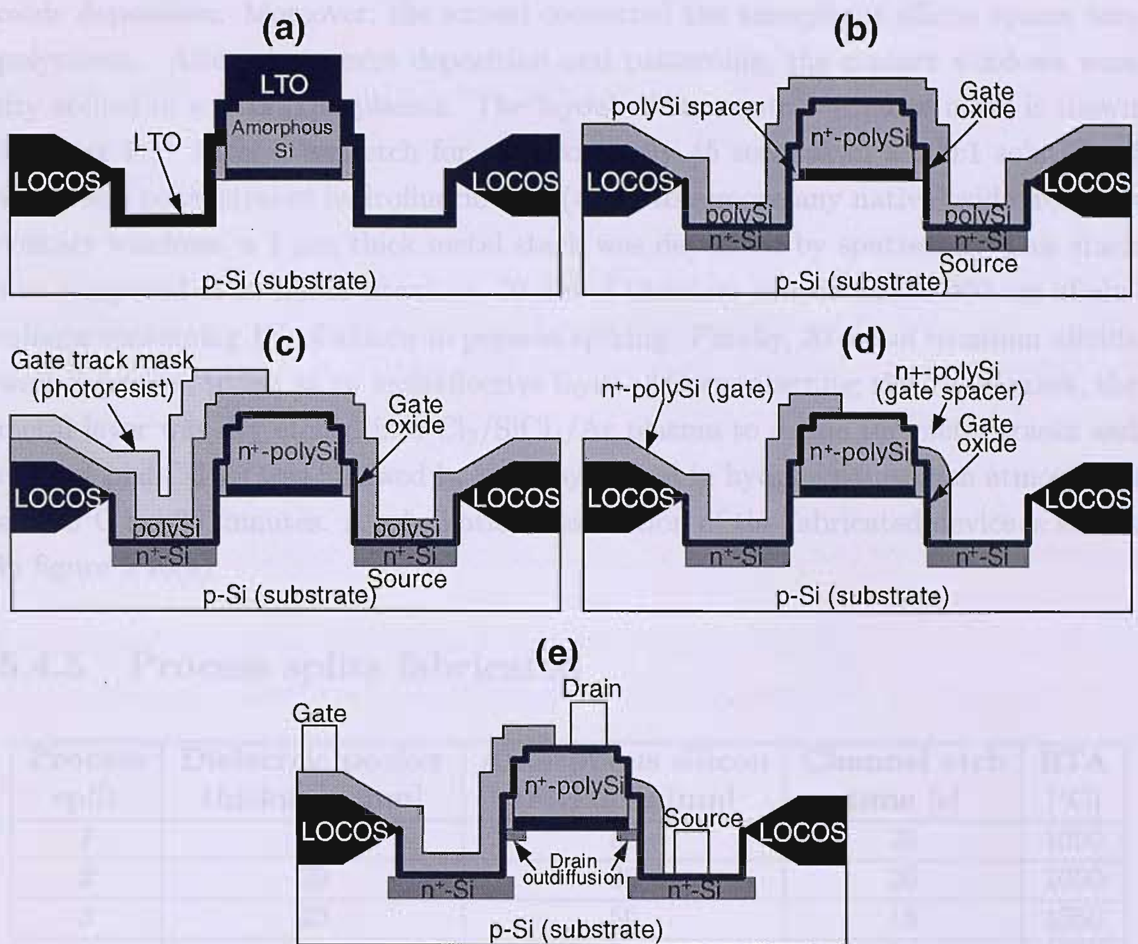

Figure 5.10: Fabrication process of dielectric pocket vertical MOSFETs: (a) source/drain ion implantation; (b) gate stack deposition; (c) - (d) gate patterning; (e) RTA (Rapid Thermal Annealing) and back-end processing.

was very selective to oxide and thus the gate oxide provided an endpoint for the dry etch. A suitable overetch was performed in order to remove any parasitic gate spacers remaining at the edge of the active area (see figure 5.10(d)).

Photoresist was patterned to define the portion of active area to be implanted in order to create an ohmic body contact for the device. The layout of the Body contact mask is shown in figure 5.5. For this purpose, boron difluoride was ion implanted in the silicon substrate (dose: 3×10^{15} cm^{-2}; energy: 25 keV).

5.4.4 Back end processing

A 100 nm thick undoped oxide layer was then deposited to act as diffusion barrier layer, followed by a 500 nm thick Boron Phosphorous Silicate Glass (BPSG) passivation layer. RTA (Rapid Thermal Annealing) was performed for 20 seconds at 1000°C or 1050°C for different process splits. The thermal treatment activated the dopants and reflowed the passivation layer, in order to fill any voids formed during

oxide deposition. Moreover, the anneal converted the amorphous silicon spacer into polysilicon. After photoresist deposition and patterning, the contact windows were dry etched in a CHF_3/Ar plasma. The layout of the contact window mask is shown in figure 5.5. After a wet etch for approximately 45 seconds in a 100:1 solution of water and concentrated hydrofluoric acid (49%) to remove any native oxide from the contact windows, a 1 μm thick metal stack was deposited by sputtering. This stack was composed of 20 nm of titanium, 20 nm of titanium nitride and of 960 nm of aluminum containing 1% of silicon to prevent spiking. Finally, 20 nm of titanium nitride were deposited to act as an antireflective layer. After patterning the Metal mask, the metal layer was dry etched in a Cl_2/$SiCl_4$/Ar plasma to define the metal tracks and contact pads. This was followed by an alloy anneal in hydrogen/nitrogen atmosphere at 420°C for 30 minutes. A schematic cross-section of the fabricated device is shown in figure 5.10(e).

5.4.5 Process splits fabricated

Process split	**Dielectric pocket thickness [nm]**	**Amorphous silicon thickness [nm]**	**Channel etch time [s]**	**RTA [°C]**
1	20	50	26	1050
2	20	30	26	1050
3	20	50	18	1050
4	20	30	18	1050
5	20	50	26	1000
6	No dielectric pocket	No amorphous Si	26	1050

Table 5.2: Process splits for fabrication of dielectric pocket vertical MOSFETs with the novel polysilicon spacer approach. The column labeled "Amorphous silicon thickness" reports the thickness of the thin amorphous silicon layer as deposited, before dry etch. The column labeled "Channel etch time" reports the time of the channel etch (second stage of the pillar dry etch). RTA = Rapid Thermal Annealing.

Table 5.2 reports the process splits fabricated. Four different process parameters were investigated: dielectric pocket, polysilicon spacer thickness, channel length and rapid thermal annealing temperature. A control device (process split 6 in table 5.2) was fabricated in order to compare the performance of vertical MOSFETs with and without a dielectric pocket. Devices with different drain contact width (see figure 5.1(b)) were fabricated by reducing the thickness of the deposited amorphous silicon layer from 50nm to 30nm in process splits 2 and 4 in table 5.2. In order to fabricate devices with shorter channels, the channel dry etch time was reduced from 26 seconds to 18 seconds in process splits 3 and 4. Finally, the effect of the thermal budget of the RTA was evaluated by reducing the anneal temperature of process split 5 from 1050°C to 1000°C.

5.5 Summary

In this chapter a novel polysilicon spacer approach to the fabrication of dielectric pocket vertical MOSFETs has been described. Vertical n-channel MOSFETs featuring shallow drain junctions on the pillar sidewall were fabricated using a novel two step pillar etch process. The key feature of this process is the deposition of a polysilicon spacer around the perimeter of the pillar to connect the channel to a polysilicon drain contact on the top of the pillar. The process development carried out to optimize the pillar etch conditions for this novel approach has been described in detail in this chapter. The polysilicon spacer approach involves only standard CMOS fabrication process steps and it is easy to integrate in a standard planar CMOS process flow. The process does not require epitaxial growth and thus can provide high throughput at low fabrication costs. Moreover it can be implemented without challenging lithography and thus allows sub-100 nm vertical MOSFETs to be integrated in a mature CMOS technology with relaxed lithography rules. Finally, the novel polysilicon spacer approach allows the drain junction depth to be controlled with precision, as it is proportional to the thickness of the polysilicon spacer connecting the drain to the body of the vertical MOSFETs.

Chapter 6

Electrical and structural characterization of dielectric pocket vertical MOSFETs

6.1 Introduction

In chapter 5, a novel polysilicon spacer approach to fabricate dielectric pocket vertical MOSFETs was described. Surround gate dielectric pocket vertical MOSFETs down to a channel length of 70 nm were successfully fabricated for the first time and are characterized in this chapter. The doping profiles of source and drain junctions are extracted by means of secondary ion mass spectroscopy and sheet resistance measurements. SEM cross-sections are employed to measure the channel length of the devices and to investigate the shape of the pillar sidewalls. The results of detailed DC electrical characterization are presented to gain a better understanding of issues associated with the dielectric pocket. The reproducibility of the electrical characteristics is investigated to assess the reliability of the novel fabrication process. The effect of process splits on transistor and diode electrical characteristics is analyzed in detail to provide further insight into the novel process flow.

6.2 Experimental procedure

6.2.1 Characterization of the doping profiles

Secondary Ion Mass Spectroscopy

The source and drain doping profiles of the dielectric pocket vertical MOSFETs were characterized by Secondary Ion Mass Spectroscopy (SIMS). This technique employs a primary ion beam to sputter the surface to be analyzed. The impurity concentration in the substrate is quantified by detecting the secondary ions emitted during

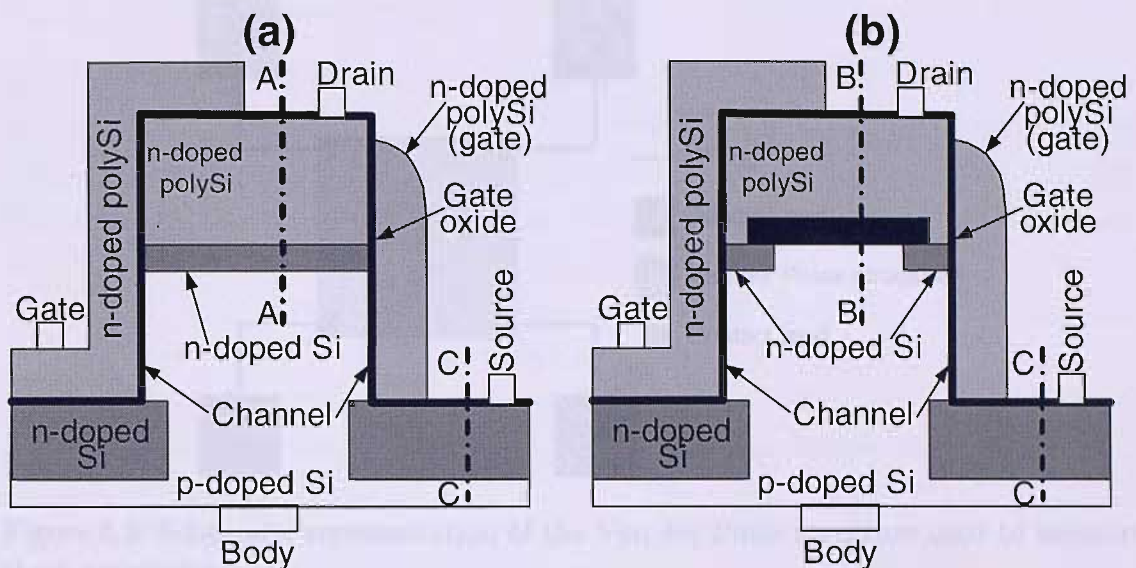

Figure 6.1: Schematic representation of the dielectric pocket vertical MOSFETs analyzed by SIMS. (a) Schematic cross-section of a control vertical MOSFET with polysilicon drain and without dielectric pocket (process split 6 in Table 5.2); section A-A = drain/body junction. (b) Schematic cross-section of a vertical MOSFET incorporating a dielectric pocket; section B-B = drain/body junction; section C-C = source/body junction.

sputtering. The samples were analyzed using O_2^+ primary ion bombardment and positive secondary ion detection. These conditions combined good depth resolution with good sensitivity to boron and reasonable sensitivity to arsenic. The data were quantified using implanted reference materials and the depth scales were determined by measuring the sputtered crater depths by interference microscopy, yielding results accurate to ±5 nm. The diameter of the circular spot of the primary beam was 125 μm, and the secondary ions were collected from a 30 μm spot in the center. For this reason, the profiles could not be measured directly on the transistors, but were obtained on a test structure 200 μm wide, with the same doping profile as the vertical MOSFETs. Figure 6.1 shows the cross-sections that were profiled by SIMS. Doping profiles were measured in three different regions: the drain/body junction of control vertical MOSFETs (section A-A), the drain/body junction of dielectric pocket vertical MOSFETs (section B-B) and the source/body junction of dielectric pocket vertical MOSFETs (section C-C). Due to the spot size, it was not possible to probe directly the composition of the polysilicon spacer that connects the drain and the body of the devices, which is only 30 nm wide.

Sheet resistivity characterization

The doping profile characterization was completed by extracting the sheet resistance and the resistivity of the source and drain regions of the vertical MOSFETs. Fig-

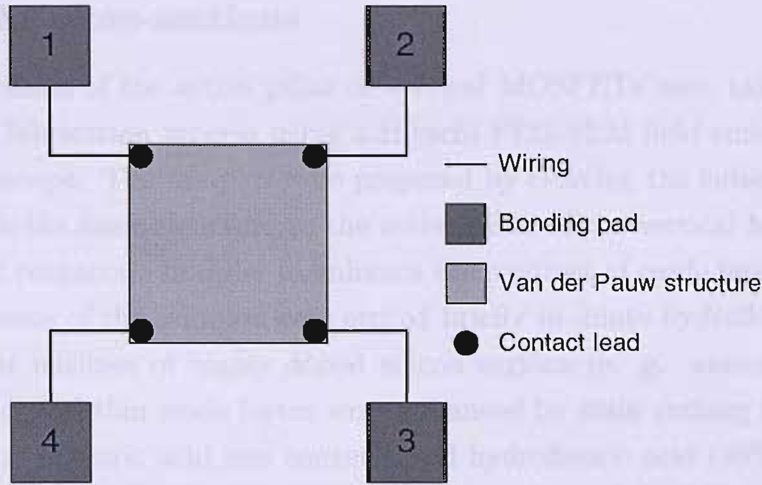

Figure 6.2: Schematic representation of the Van der Pauw structure used to measure sheet resistivity.

ure 6.2 shows a schematic representation of the so-called Van der Pauw structure, used to determine the sheet resistance of a conducting region. The Van der Pauw structure is a flat and homogeneous square-shaped 100 μm by 100 μm area with the same doping profile as the conducting layer to be characterized, i. e. the source or drain of the vertical MOSFET. The structure is symmetrically connected to bonding pads at each corner. The sheet resistance (ρ_{sh}) is calculated from the resistance of the Van der Pauw structure according to the Van der Pauw theorem [93]. The sheet resistance is extracted using equation 6.1, where V_{mn} is the bias measured between contacts m and n and I_{xy} is the current applied at contact x and taken off at contact y.

$$\rho_{sh} = \frac{\pi}{ln2}\frac{R_{12,34}+R_{23,14}}{2} \quad (6.1)$$
$$R_{12,34} = \frac{V_{12}}{I_{34}}$$
$$R_{23,14} = \frac{V_{23}}{I_{14}}$$

The thickness (t) of the conducting layer characterized is approximated as the junction depth of the layer (i. e. source or drain of the vertical MOSFET), extracted from the SIMS profiles. This approximation is reasonable because both layers have steep junctions. The average resistivity (ρ) of the conducting layer is then calculated using equation 6.2.

$$\rho = \rho_{sh}t \quad (6.2)$$

6.2.2 SEM cross-sections

SEM cross-sections of the active pillar of vertical MOSFETs were taken after completion of the fabrication process using a Hitachi FEG-SEM field emission scanning electron microscope. The samples were prepared by cleaving the substrates through SEM bars with the same structure as the active pillar of the vertical MOSFETs (except the metal contacts). In order to enhance the contrast of oxide layers on a silicon background, some of the samples were etched briefly in dilute hydrofluoric acid. Alternatively, the outlines of highly doped silicon regions (e. g. source and drain of the MOSFETs) and thin oxide layers were enhanced by stain etching the samples in a 400:1 solution of nitric acid and concentrated hydrofluoric acid (49%). In some of the pictures reported in the following sections, the edges of the highly doped silicon regions were only barely visible in the high resolution SEM cross-sections (10 keV beam energy) and have been enhanced for clarity.

6.2.3 Electrical characteristics

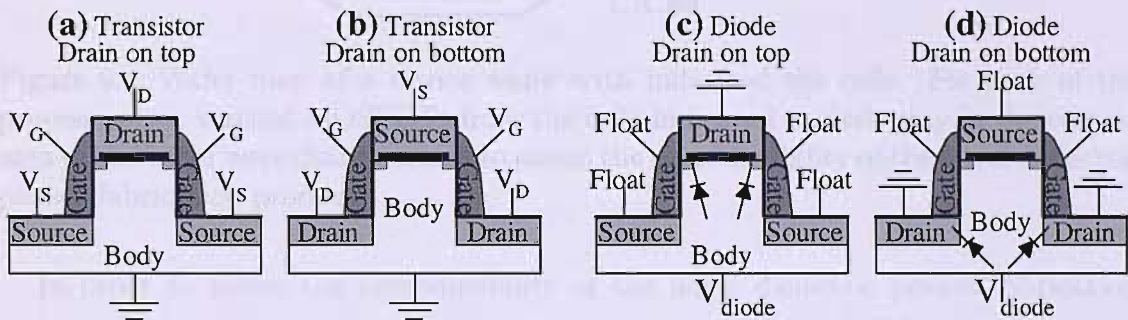

Figure 6.3: Measurement configurations of dielectric pocket vertical MOSFETs: (a)-(b) transistor measurement configuration; (c)-(d) diode measurement configuration.

Surround gate dielectric pocket vertical MOSFETs with channel widths ranging between 24 μm and 52 μm were characterized using a HP4155A semiconductor analyzer. The electrical performance of the devices was characterized using DC current-voltage characteristics.

The vertical MOSFETs were measured in two different configurations: a transistor configuration (figure 6.3(a)-(b)), in which gate and drain were biased with source and body grounded, and a diode configuration (figure 6.3(c)-(d)), in which a body-drain bias was applied with gate and source floating. The measurements in diode configuration allowed the body leakage component of the drain current to be decoupled from the other contributions (see section 2.3).

The electrical characteristics were measured both with the drain on the top and on the bottom of the transistor pillar. Figure 6.3(a) shows a dielectric pocket vertical MOSFET in drain on top measurement configuration and figure 6.3(c) shows

the correspondent diode configuration. Figure 6.3(b) shows the transistor in drain on bottom measurement configuration and figure 6.3(d) shows the correspondent diode configuration. These measurements were performed to investigate the inherent asymmetry of dielectric pocket vertical MOSFETs when the drain was on the top or on the bottom of the transistor pillar. It is important to understand this asymmetry when the vertical MOSFETs are introduced in circuit architectures. On the contrary, this is not an issue in planar MOSFETs, where the interchange of source and drain has no effect on the electrical characteristics.

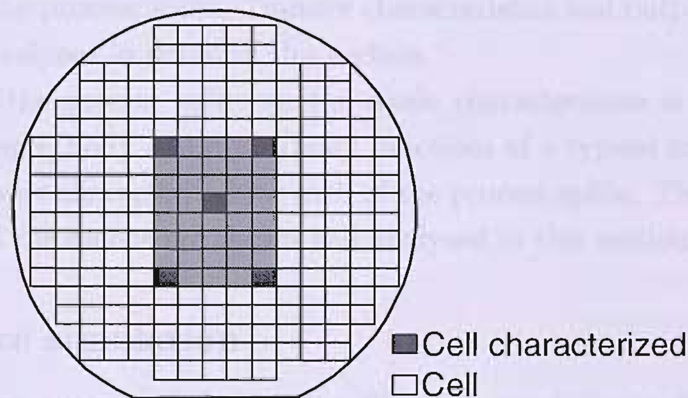

Figure 6.4: Wafer map of a device wafer with indicated the cells. For each of the process splits, vertical MOSFETs from the cells indicated in dark grey in the central area of the wafer were characterized to assess the reproducibility of the novel dielectric pocket fabrication process.

In order to assess the reproducibility of the novel dielectric pocket fabrication process, transfer characteristics of surround gate vertical MOSFETs were measured for each process split on cells in different locations on the silicon wafers. Figure 6.4 shows the cell map of a wafer. Five devices on five different cells were characterized for each process split. The locations of the cells are indicated in dark grey in figure 6.4. Devices with the same layout were characterized in each cell, allowing an assessment of the process-induced variation of the electrical characteristics on each of the wafers fabricated. All the devices measured were located in the central part of the wafer (light grey area in figure 6.4), one in the middle and the others at the corners, to avoid the possibly damaged area close to the edge of the wafer.

In section 6.6 a comparison of the characteristics of the devices in drain on top and drain on bottom measurement configurations is attempted. Electrical parameters were extracted from the transfer characteristics of five devices for each process split (see figure 6.4) and their average and standard deviation were calculated. The following parameters were investigated: threshold voltage, on-state drain current and maximum gate transconductance. The linearly extrapolated threshold voltage (V_{on}) was extracted by linear extrapolation from $I_D(V_G)$ characteristics at $V_D = 0.1$ V. For a second order correction in V_D, the threshold voltage (V_t) was calculated as

$V_t = V_{on} - V_D/2$. This expression is derived from equation 2.21 with m = 1. The on-state drain current was extracted from $I_D(V_G)$ characteristics at V_D = 1 V and $V_G - V_t$ = 1 V. This allowed a comparison of the drain current of the devices at constant inversion charge density in the channel ($V_G - V_t$ = constant; see equations 2.20 and 2.21). The maximum gate transconductance ($g_m = \frac{dI_D}{dV_G}$) was extracted as the maximum slope of the linear $I_D(V_G)$ characteristics at V_D = 1 V.

The effect of the process splits on the transistor characteristics is assessed in section 6.7. A typical surround gate vertical MOSFET was chosen and fully characterized for each of the process splits. Transfer characteristics and output characteristics are shown and analyzed in detail in this section.

The effect of the process splits on the diode characteristics is analyzed in section 6.8. The source/body and drain/body junctions of a typical surround gate vertical MOSFET were characterized for each of the process splits. The current-voltage characteristics of the diodes are shown and analyzed in this section.

6.2.4 Device simulation

Device simulations were performed using Silvaco's simulation software, called Atlas [96]. The devices to be simulated were drawn using the Structure Editor tool provided by Silvaco, called Devedit [97]. After defining the electrodes, device simulation was performed using Atlas. A standard set of models and parameters, provided by Atlas and optimized for MOSFET simulation, was used. In order to simulate carrier tunneling through a thin parasitic oxide layer between the drain and the body of a MOSFET, the standard model provided by Atlas to simulate Fowler-Nordheim tunneling of electrons through insulators (FNORD) was incorporated in the simulations.

6.3 Doping profiles

6.3.1 SIMS profiles of source and drain junctions

In order to assess the effect of the presence of the dielectric pocket on the drain doping profile of the vertical MOSFETs, the doping profiles of control and dielectric pocket devices were characterized by SIMS. Figure 6.5 shows the doping profiles measured on the cross-sections defined in figure 6.1. Figure 6.5(a) shows the doping profile of the drain/body junction of a control device with polysilicon drain and without dielectric pocket from process split 6 in Table 5.2 (section A-A in figure 6.1(a)). A magnification of the drain doping profile is shown in figure 6.5(b). As expected, the control device shows outdiffusion of drain dopants into the body of the device, yielding a junction depth of 30 nm. Arsenic pile up is observed at the interface between the polysilicon

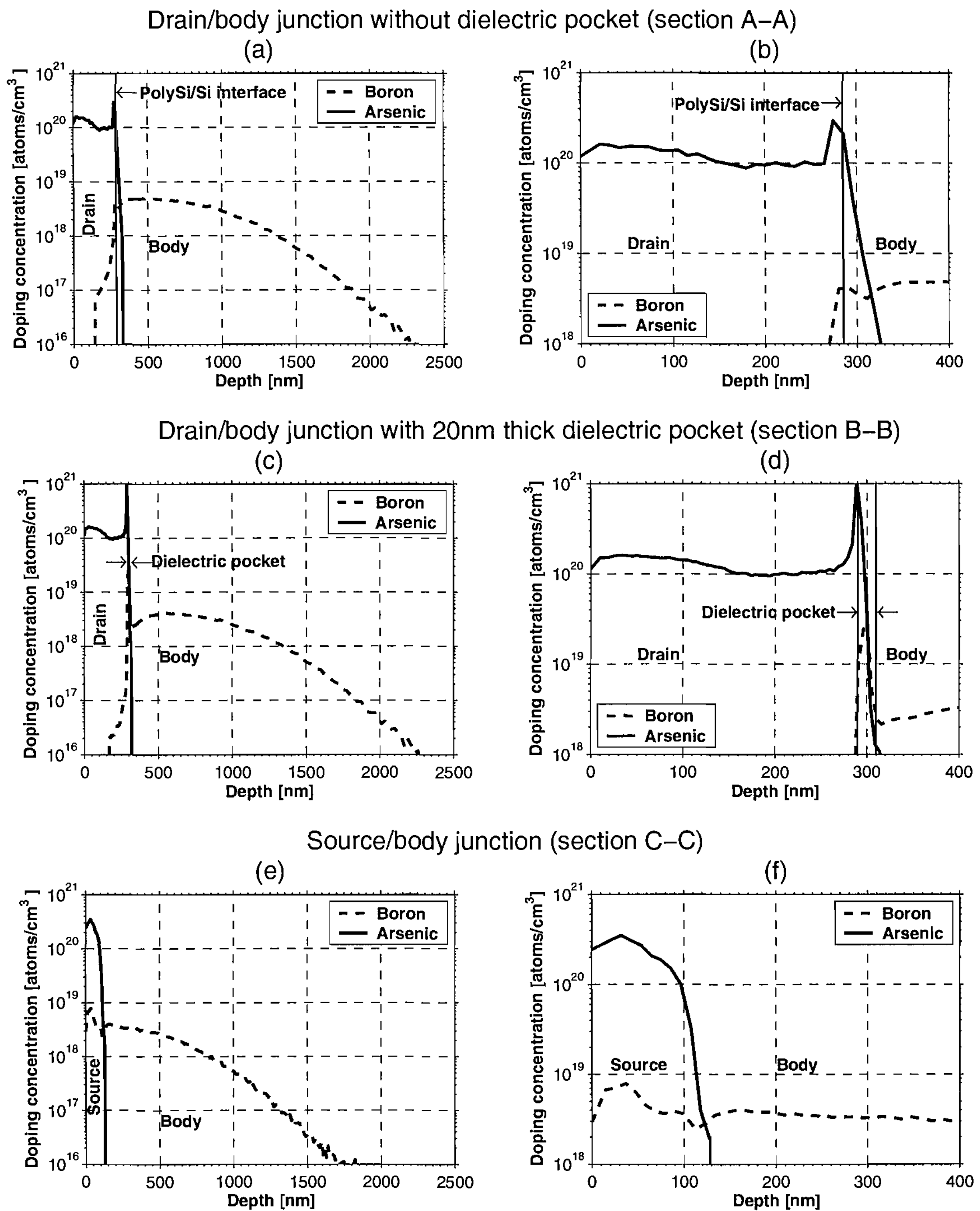

Figure 6.5: Secondary Ion Mass Spectroscopy (SIMS) doping profiles of the drain/body junctions (a-b) of a control device without dielectric pocket (process split 6 in Table 5.2) and (c-d) of a vertical MOSFET with a 20 nm thick dielectric pocket (process split 1 in Table 5.2). (e-f) SIMS profile of the source/body junction of a dielectric pocket vertical MOSFET (process split 1 in Table 5.2). Figures a, c and e show the entire profiles; figures b, d and f show a magnification of the profiles close to the surface.

drain and the single-crystal silicon substrate. This can be explained by segregated arsenic at the large grain boundary between the polysilicon drain and the single-crystal silicon substrate [103]. This phenomenon will be analyzed in more detail in chapter 7. The approximately flat arsenic profile in the polysilicon drain is caused by the high arsenic grain boundary diffusion coefficient, which is several orders of magnitude higher than the arsenic diffusion coefficient in single-crystal silicon.

Figure 6.5(c) shows the doping profile of the drain/body junction of a dielectric pocket vertical MOSFET from process split 1 in Table 5.2 (section B-B in figure 6.1(b)). A magnification of the drain doping profile is shown in figure 6.5(d). The dielectric pocket of the device was 20 nm thick. The oxide layer appears to be effective in suppressing the outdiffusion of drain dopant (arsenic) into the single-crystal silicon body of the device. An arsenic pile up is observed at the interface between the polysilicon drain and the silicon dioxide.

Figure 6.5(e) shows the doping profile of the source/body junction of a dielectric pocket vertical MOSFET (section C-C in figure 6.1(b)). A magnification of the drain doping profile is shown in figure 6.5(f). As the arsenic is ion implanted directly into the single-crystal silicon substrate, the doping profile has the characteristic bell shape ensuing from ion implantation with a junction depth of 120 nm.

6.3.2 Resistivity measurements

	Polysilicon drain	**Silicon source**
Sheet resistance [Ω/square]	75.6	63.4
Junction depth [nm]	290	120
Resistivity [Ω cm]	2.2×10^{-3}	7.6×10^{-4}

Table 6.1: Sheet resistance, junction depth and resistivity of a dielectric pocket vertical MOSFET (process split 1 in Table 5.2). The sheet resistance was measured on Van der Pauw test structures [93]. The junction depth values were extracted from SIMS profiles (figure 6.5).

Table 6.1 shows the values of sheet resistance and resistivity of the polysilicon drain and of the single-crystal silicon source of a dielectric pocket vertical MOSFET (process split 1 in Table 5.2) measured on Van der Pauw test structures (see section 6.2.1). The resistivity of the polysilicon drain is about three times higher than that of the single-crystal silicon source. This is due to the fact that arsenic which is segregated at the grain boundaries in polysilicon is generally electrically inactive [103]. The grain boundaries must become saturated with arsenic before significant diffusion can occur into the interior of the grains.

6.4 SEM cross-sections of fabricated transistors

This section presents SEM cross-sections of the active pillar of dielectric pocket vertical MOSFETs from different process splits. The SEM images are used to characterize the pillar sidewall and to extract the channel length of the devices. Figure 6.6 shows SEM cross-sections of a dielectric pocket vertical MOSFET from process split 1 in table 5.2, with 130 nm channel length. The channel length was calculated by subtracting the dopant outdiffusion from the drain, estimated as 30 nm from the SIMS profiles (see section 6.3), from the distance between the source/body junction at the bottom of the pillar and the polysilicon spacer/single-crystal silicon interface on the pillar sidewall. This distance was measured on the SEM cross-section. Figure 6.6 shows an undercut in the pillar sidewall, just underneath the dielectric pocket. This irregularity of the pillar sidewall is likely to be due to the dry etch process used. As explained in detail in section 5.4.2, the dry etch of the active pillar was performed in two stages. The second stage was a silicon dry etch in a HBr plasma. The position of the undercut underneath the dielectric pocket suggests that it formed during the HBr etch of the single-crystal silicon substrate. To suppress the sidewall undercut a possible approach would be to increase the anisotropy of the etch process. This can be achieved by modifying the chemistry of the plasma used for dry etch. The addition of oxygen to the HBr plasma, for example, is known to enhance the selectivity of the dry etch process by building up a passivation layer on the pillar sidewall.

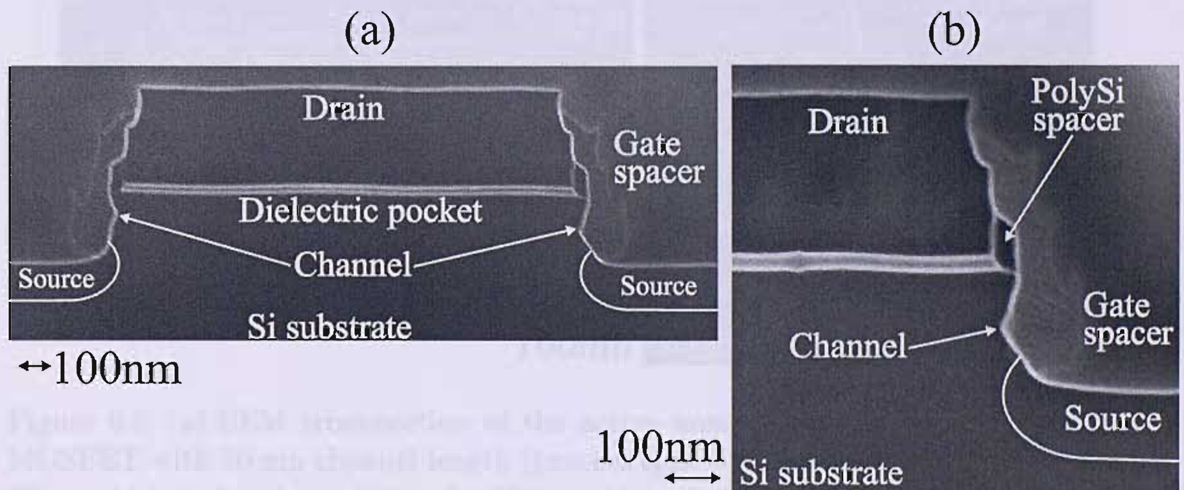

Figure 6.6: (a) SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 130 nm channel length (process split 1 in table 5.2). The device has a 20 nm thick dielectric pocket and a 30 nm wide polysilicon spacer. (b) Magnification of the pillar sidewall of the device.

Figure 6.7 shows SEM cross-sections of a dielectric pocket vertical MOSFET from process split 2 in table 5.2. A channel length of 150 nm was extracted from the SEM images. The polysilicon spacer was 20 nm wide. It can be noticed that the

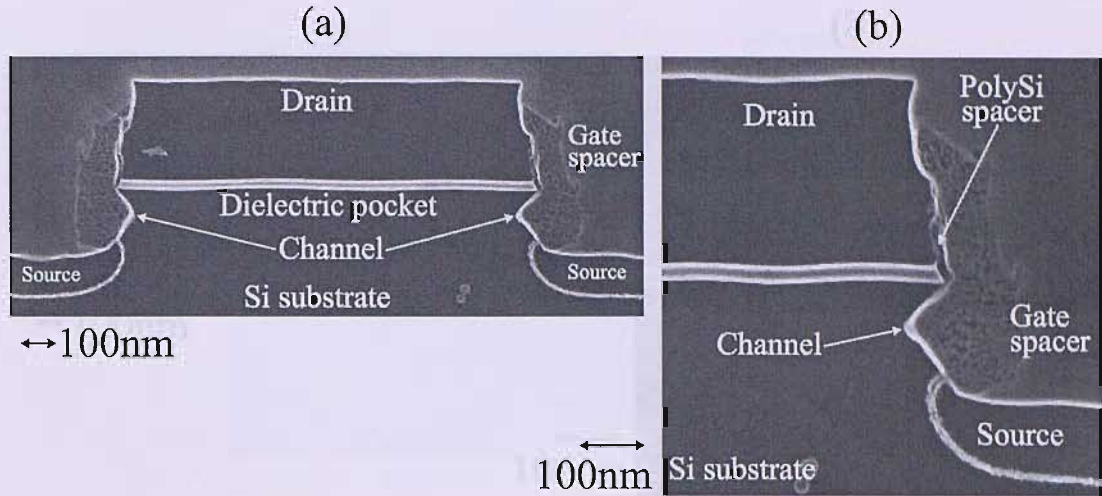

Figure 6.7: (a) SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 150 nm channel length (process split 2 in table 5.2). The device has a 20 nm thick dielectric pocket and a 20 nm wide polysilicon spacer. (b) Magnification of the pillar sidewall of the device.

undercut in the pillar sidewall is less pronounced in this device than in process split 1 (figure 6.6).

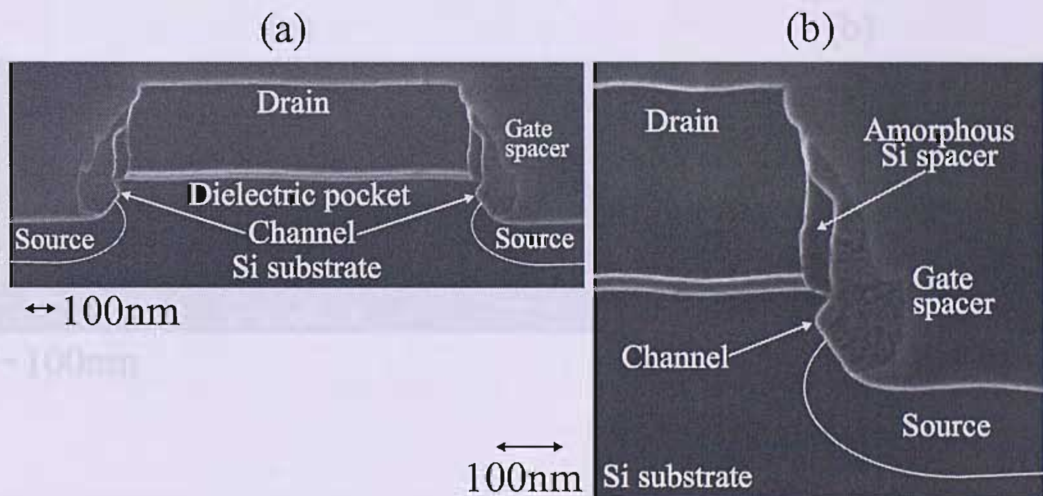

Figure 6.8: (a) SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 70 nm channel length (process split 3 in table 5.2). The device has a 20 nm thick dielectric pocket and a 35 nm wide polysilicon spacer. (b) Magnification of the pillar sidewall of the device.

SEM cross-sections of a dielectric pocket vertical MOSFET from process split 3 in table 5.2 are shown in figure 6.8. This device had a shorter channel length of 70 nm, because the channel was dry etched for a shorter time compared to process splits 1 and 2 (see table 5.2). The spacer connecting drain and body of the vertical MOSFET was 35 nm wide.

Figure 6.9 shows SEM cross-sections of a dielectric pocket vertical MOSFET from

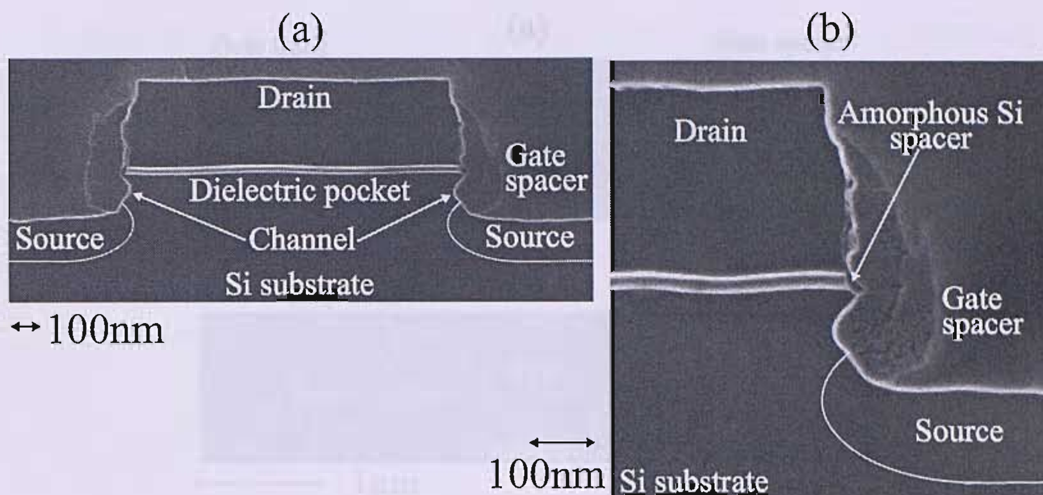

Figure 6.9: (a) SEM cross-section of the active area of a dielectric pocket vertical MOSFET with 90 nm channel length (process split 4 in table 5.2). The device has a 20 nm thick dielectric pocket and a 15 nm wide polysilicon spacer. (b) Magnification of the pillar sidewall of the device.

process split 4 in table 5.2. This device had a channel length of 90 nm and a polysilicon spacer 15 nm wide. The undercut in the pillar sidewall is very pronounced.

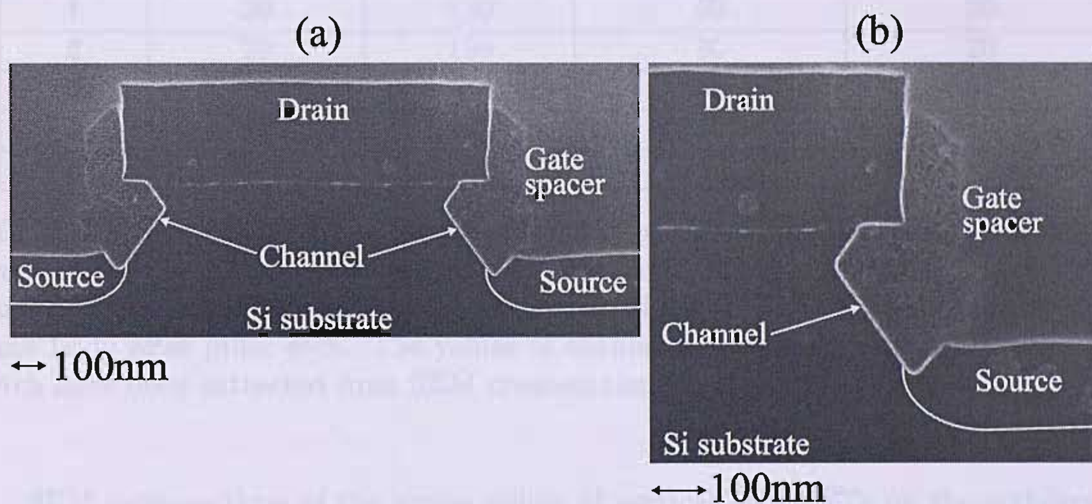

Figure 6.10: (a) SEM cross-section of the active area of a control vertical MOSFET with 250 nm channel length and without dielectric pocket (process split 6 in table 5.2). (b) Magnification of the pillar sidewall of the device.

SEM cross-sections of a control vertical MOSFET without dielectric pocket are shown in figure 6.10. The channel of this device was etched for the same time as process splits 1 and 3 (see table 5.2), but unexpectedly a longer channel (250 nm) was measured. A deep undercut of about 80 nm at the interface between the polysilicon drain and the single-crystal silicon substrate was observed. The existence of the pillar sidewall undercut in the control device suggests that the undercut is not due to the presence of the dielectric pocket, but is induced by the dry etch process.

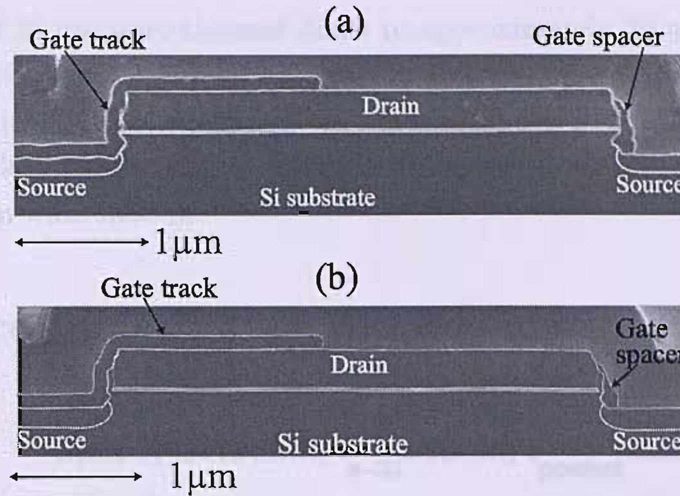

Figure 6.11: SEM cross-sections of the active area of dielectric pocket vertical MOSFETs, showing the gate track which connects the gate spacers to the gate contact on one side of the pillar, and the gate spacer on the opposite side. (a) Vertical MOSFET with a 35 nm thick polysilicon spacer (process split 3 in table 5.2). (b) Vertical MOSFET with a 15 nm thick polysilicon spacer (process split 4 in table 5.2).

Process split	Dielectric pocket [nm]	Channel length [nm]	t_{a-Si} before pillar etch [nm]	t_{spacer} after pillar etch [nm]
1	20	130	50	30
2	20	150	30	20
3	20	70	50	35
4	20	90	30	15
6	-	250	-	-

Table 6.2: Structural parameters of dielectric pocket vertical MOSFETs and of a control device. t_{a-Si} = thickness of the amorphous silicon layer that connects drain and body before pillar etch. t_{spacer} = thickness of the thin spacer that connects drain and body after pillar etch. The values of channel length and spacer thickness after etch have been extracted from SEM cross-sections.

SEM cross-sections of the active pillars of vertical MOSFETs on the orthogonal direction are shown in figure 6.11. On the left of the images the gate track that connects the gate spacers to the gate contact (shown in figure 5.10(e)) can be seen. On the right of the images the polysilicon gate spacer is visible.

Table 6.2 summarizes the values of channel length and spacer thickness extracted from the SEM cross-sections and from the SIMS profiles. The table shows that the spacer connecting the drain to the body of the devices was thinner after dry etch than after amorphous silicon deposition. This was due to a slight lateral etch of the spacer, which occurred during the channel etch. The amorphous silicon layers which were 50 nm thick after deposition yielded polysilicon spacers approximately 30 nm wide after dry etch (process splits 1 and 3). On the other hand the layers deposited

to a thickness of 30 nm were thinned down to approximately 20 nm after pillar dry etch (process splits 2 and 4). Deeper sidewall undercuts were observed in the devices from process splits 2 and 4, which had 20 nm wide spacers. On the other hand, the undercuts were less visible on the sidewalls of devices from process splits 1 and 3, which had 30 nm wide spacers.

6.5 Reproducibility of the fabrication process

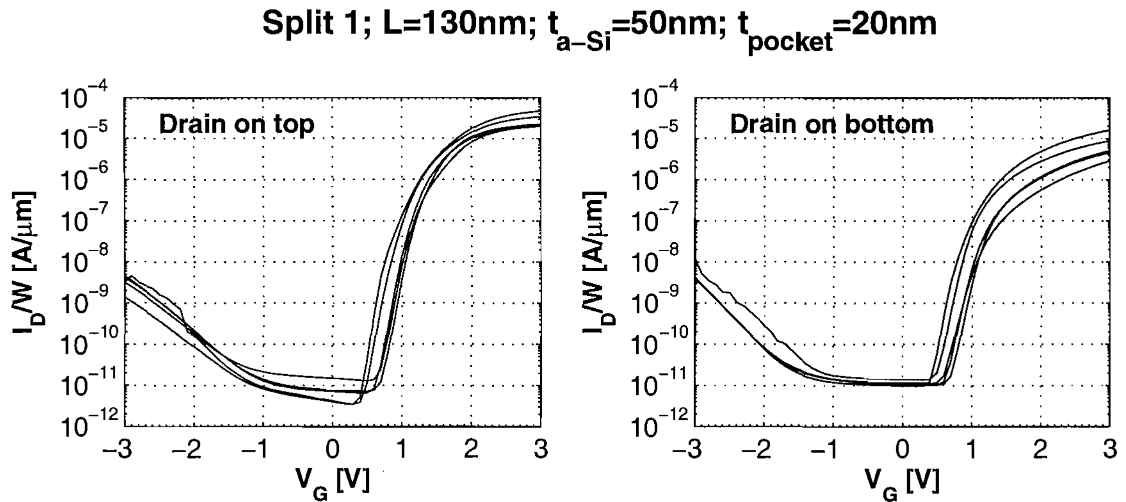

Figure 6.12: Transfer characteristics of surround gate, dielectric pocket vertical MOSFETs from process split 1 in table 5.2, measured at $V_D = 1V$; $V_S = V_B = 0V$; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition; t_{pocket} = thickness of the dielectric pocket.

In this section the reproducibility of the electrical characteristics of the dielectric pocket vertical MOSFETs is assessed. Transfer characteristics of surround gate vertical MOSFETs with the same layout from different parts of the wafer are shown on a single graph. The reproducibility of the devices from process split 5 in table 5.2, which had a low activation anneal temperature, is not investigated because the electrical characteristics are non-ideal. Measurements performed in drain on bottom and drain on top measurement configuration are displayed separately. More details on the experimental procedure can be found in section 6.2.3.

Figure 6.12 shows transfer characteristics of dielectric pocket vertical MOSFETs from process split 1 in table 5.2. These are long channel devices (L = 130 nm) with a thick spacer connecting drain and body (amorphous silicon layer 50 nm thick after deposition). The electrical characteristics show reasonable reproducibility in the drain on top measurement configuration. However, they are not very reproducible in the drain on bottom configuration, where a spread of about a decade is observed in the on-state currents.

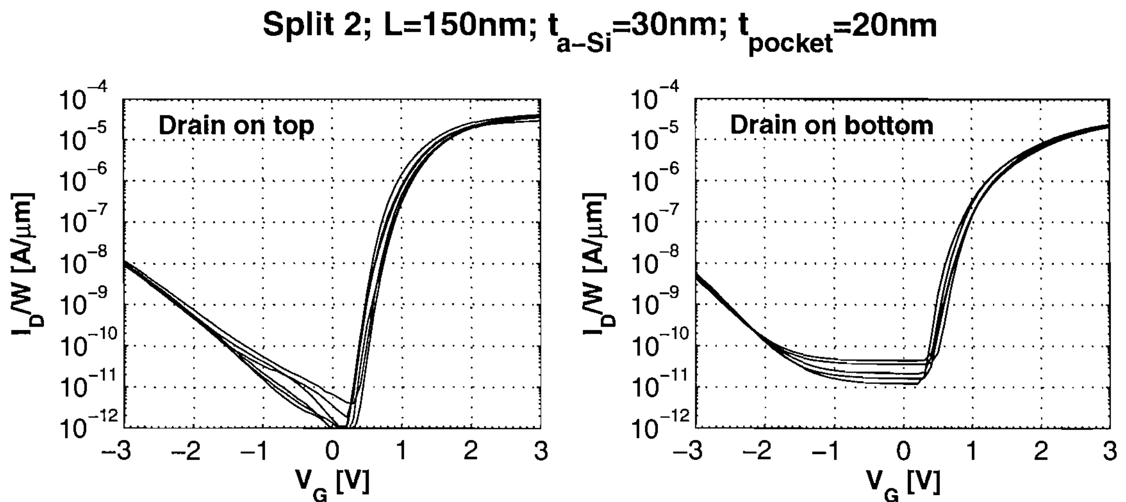

Figure 6.13: Transfer characteristics of surround gate, dielectric pocket vertical MOSFETs from process split 2 in table 5.2, measured at V_D = 1V; V_S = V_B = 0V; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition; t_{pocket} = thickness of the dielectric pocket.

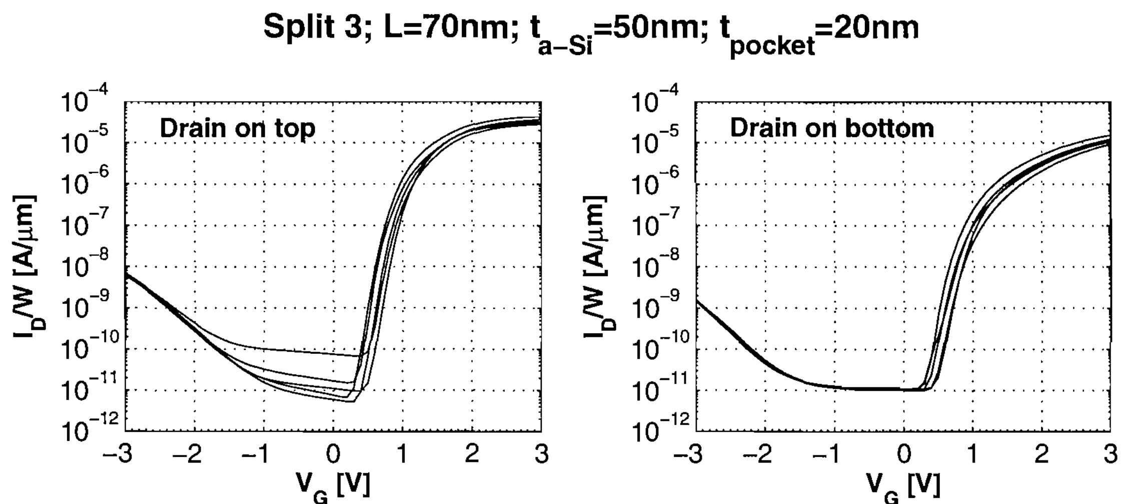

Figure 6.14: Transfer characteristics of surround gate, dielectric pocket vertical MOSFETs from process split 3 in table 5.2, measured at V_D = 1V; V_S = V_B = 0V; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition; t_{pocket} = thickness of the dielectric pocket.

Transfer characteristics of long channel (L = 150 nm) dielectric pocket vertical MOSFETs with a thin spacer connecting drain and body (amorphous silicon layer 30 nm thick after deposition) are shown in figure 6.13. These characteristics are remarkably reproducible, both in drain on top and in drain on bottom configurations.

Figure 6.14 displays characteristics of dielectric pocket vertical MOSFETs with 70 nm channel length. This is the shortest channel length achieved among the process splits fabricated. These devices have a thick spacer connecting drain and body

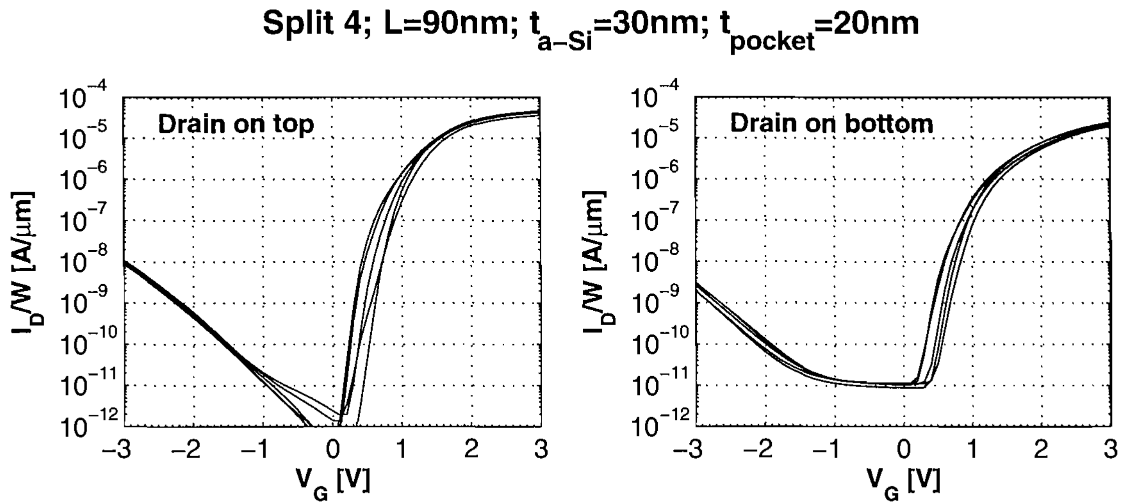

Figure 6.15: Transfer characteristics of surround gate, dielectric pocket vertical MOSFETs from process split 4 in table 5.2, measured at V_D = 1V; V_S = V_B = 0V; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition; t_{pocket} = thickness of the dielectric pocket.

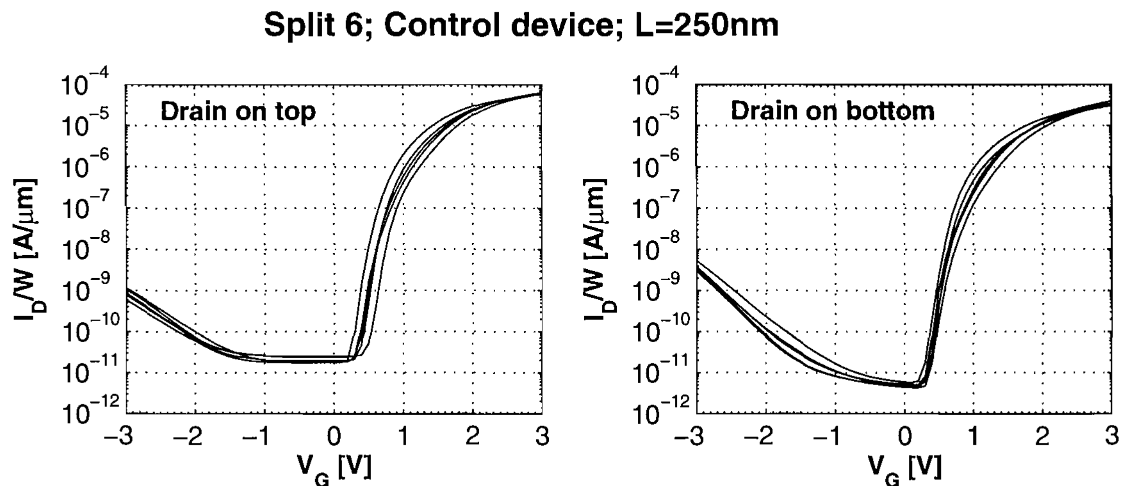

Figure 6.16: Transfer characteristics of surround gate vertical MOSFETs without dielectric pocket and with polysilicon drain from process split 6 in table 5.2, measured at V_D = 1V; V_S = V_B = 0V; L = channel length.

(amorphous silicon layer 50 nm thick after deposition). Their electrical characteristics show good reproducibility.

Figure 6.15 shows transfer characteristics of short-channel devices (L = 150 nm) with a thin spacer ensuring connection of drain and body (amorphous silicon layer 30 nm thick after deposition). Their electrical characteristics again show good reproducibility, both in on-state and off-state operation.

Finally, figure 6.16 shows characteristics of control devices without a dielectric pocket. These devices have a 250 nm channel length. Their transfer characteristics

show good reproducibility, both in on-state and off-state.

6.6 Effect of measurement configuration (drain on top and drain on bottom) on electrical characteristics

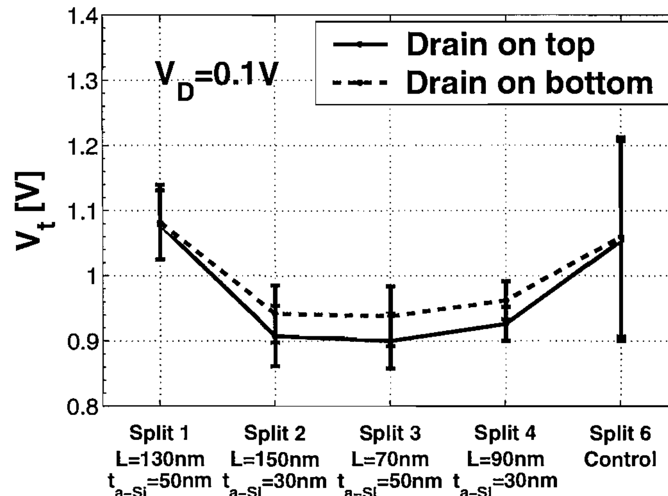

Figure 6.17: Comparison of the threshold voltage (V_t) of devices from different process splits, listed in table 5.2, in drain on top and drain on bottom measurement configuration; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition.

In this section the effect of the measurement configuration (drain on top or drain on bottom) on the electrical characteristics of dielectric pocket vertical MOSFETs is evaluated. This is achieved by performing an analysis of electrical parameters extracted from the transfer characteristics shown in section 6.5 for each of the process splits. The average and standard deviation of the parameters extracted is plotted on the same graph for drain on top and drain on bottom measurement configurations. A detailed description of the experimental procedure used to extract the parameters can be found in section 6.2.3.

Figure 6.17 shows the threshold voltage (V_t) of devices from different process splits. The average values lie between 0.9V and 1.1V. No significant difference is observed in the threshold voltage in drain on top and drain on bottom configurations. Furthermore no significant trend is seen in the threshold voltage among the different process splits.

The on-state drain current of devices from different process splits, measured at V_D = 1V and V_G - V_t = 1V, is shown in figure 6.18(a). It can be observed that the on-state drain current is strongly asymmetrical, with higher currents measured in

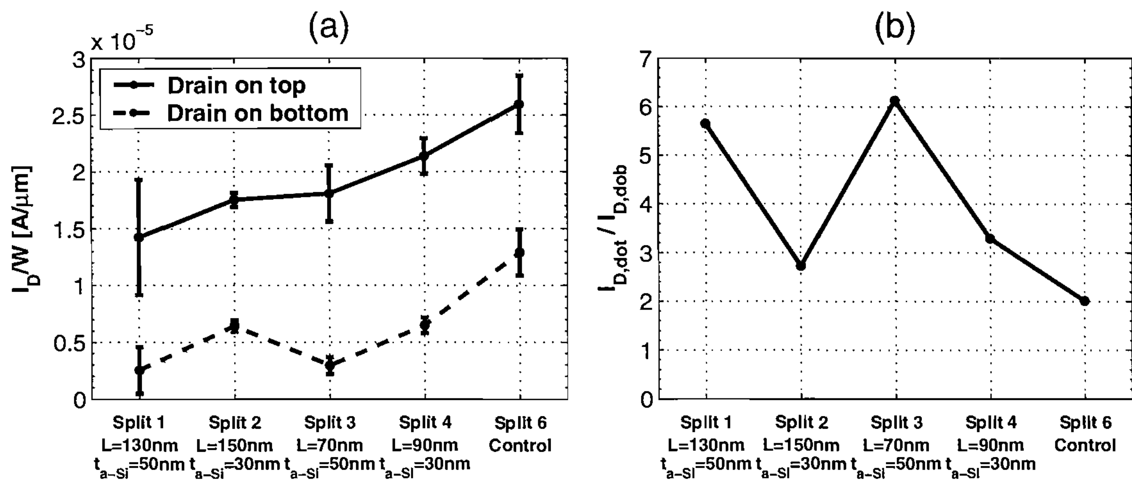

Figure 6.18: (a) On-state drain current of devices from different process splits, listed in table 5.2, in drain on top and drain on bottom configuration; V_G - V_t = 1V, V_D = 1V, V_S = V_B = 0V; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition. (b) Ratio of the average on-state drain current in drain on top and drain on bottom configurations.

the drain on top configuration for all the process splits. The control devices without a dielectric pocket display a higher on-current than the dielectric pocket vertical MOSFETs, both in drain on top and in drain on bottom configurations. The effect of the process splits on the asymmetry of the on-state drain current is investigated in figure 6.18(b). For each process split, the ratio of the average drain current in drain on top and drain on bottom configurations is displayed. The dielectric pocket devices with a thick spacer (50 nm thick after amorphous silicon deposition) show a higher asymmetry than the dielectric pocket MOSFETs with a thinner spacer (30 nm thick after amorphous silicon deposition). The vertical MOSFETs without dielectric pocket show the lowest ratio between drain on top and drain on bottom configurations.

Figure 6.19(a) shows the values of maximum gate transconductance, measured at V_D = 1V, for different process splits. The trends observed are in agreement with those highlighted in figure 6.18(a). A strong asymmetry between drain on top and drain on bottom configurations is observed, with higher values measured in drain on top. The control device without a dielectric pocket shows the highest value of transconductance for both configurations. The ratio of the average gate transconductance in drain on top and drain on bottom configurations is displayed in figure 6.19(b). The devices with a thicker spacer connecting drain and body (50 nm thick after amorphous silicon deposition) show a more marked asymmetry than the other process splits. This confirms the trends observed in figure 6.18(b).

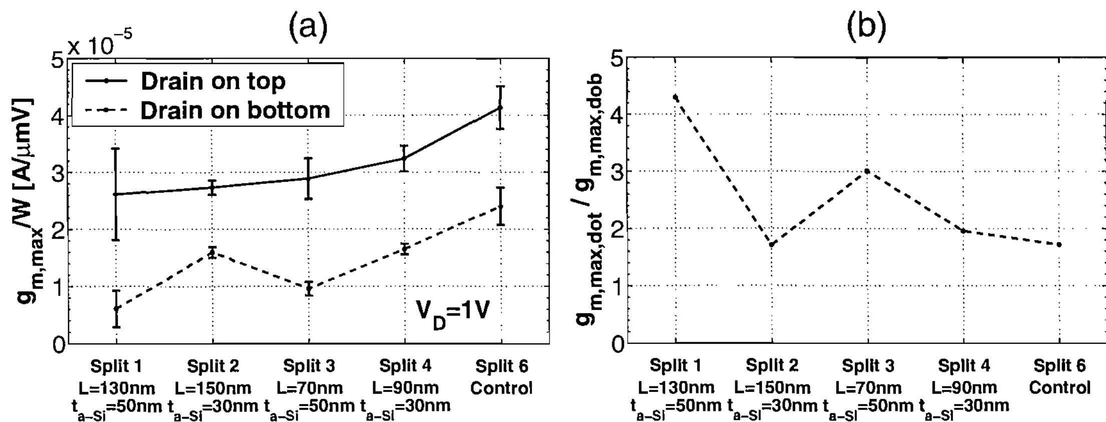

Figure 6.19: (a) Maximum gate transconductance ($g_m = \frac{dI_D}{dV_G}$) at $V_D = 1V$ of devices from different process splits, listed in table 5.2, in drain on top and drain on bottom configuration; $V_S = V_B = 0V$; L = channel length; t_{a-Si} = thickness of the deposited amorphous silicon layer. (b) Ratio of the average gate transconductance in drain on top and drain on bottom configurations.

6.7 Effect of process splits on transistor characteristics

6.7.1 Effect of process splits on transfer characteristics

Figure 6.20 shows the transfer characteristics of a typical vertical MOSFET for each of the process splits listed in table 5.2. For each process split, transfer characteristics in drain on top and drain on bottom measurement configurations are shown on the same graph. Characteristics measured at low and high drain bias (V_D = 0.1 V V_D = 1 V respectively) are displayed. A strong effect of the Rapid Thermal Annealing temperature (T_{RTA}) can be identified in figure 6.20. The dielectric pocket MOSFETs from process splits 1-4 and the control device (process split 6) were annealed at 1050°C for 20 seconds. These devices exhibit a subthreshold slope ranging between 85 mV/decade and 95 mV/decade and a DIBL of 50 mV in the drain on top configuration. In contrast, the dielectric pocket vertical MOSFET from process split 5 whose transfer characteristics are shown in figure 6.20(e) was annealed at a lower temperature of 1000°C for 20 seconds. The lower anneal temperature had a remarkable effect on the on-current of the device, giving a value two orders of magnitude lower than the other process splits. The subthreshold slope is also degraded and the DIBL in the drain on top configuration is about ten times higher than in the other process splits.

Figure 6.21 investigates the effect of the dielectric pocket and of the channel length on the transfer characteristics of the vertical MOSFETs at different drain voltages. Transfer characteristics with drain bias ranging from 0.1 V to 3 V are superposed for

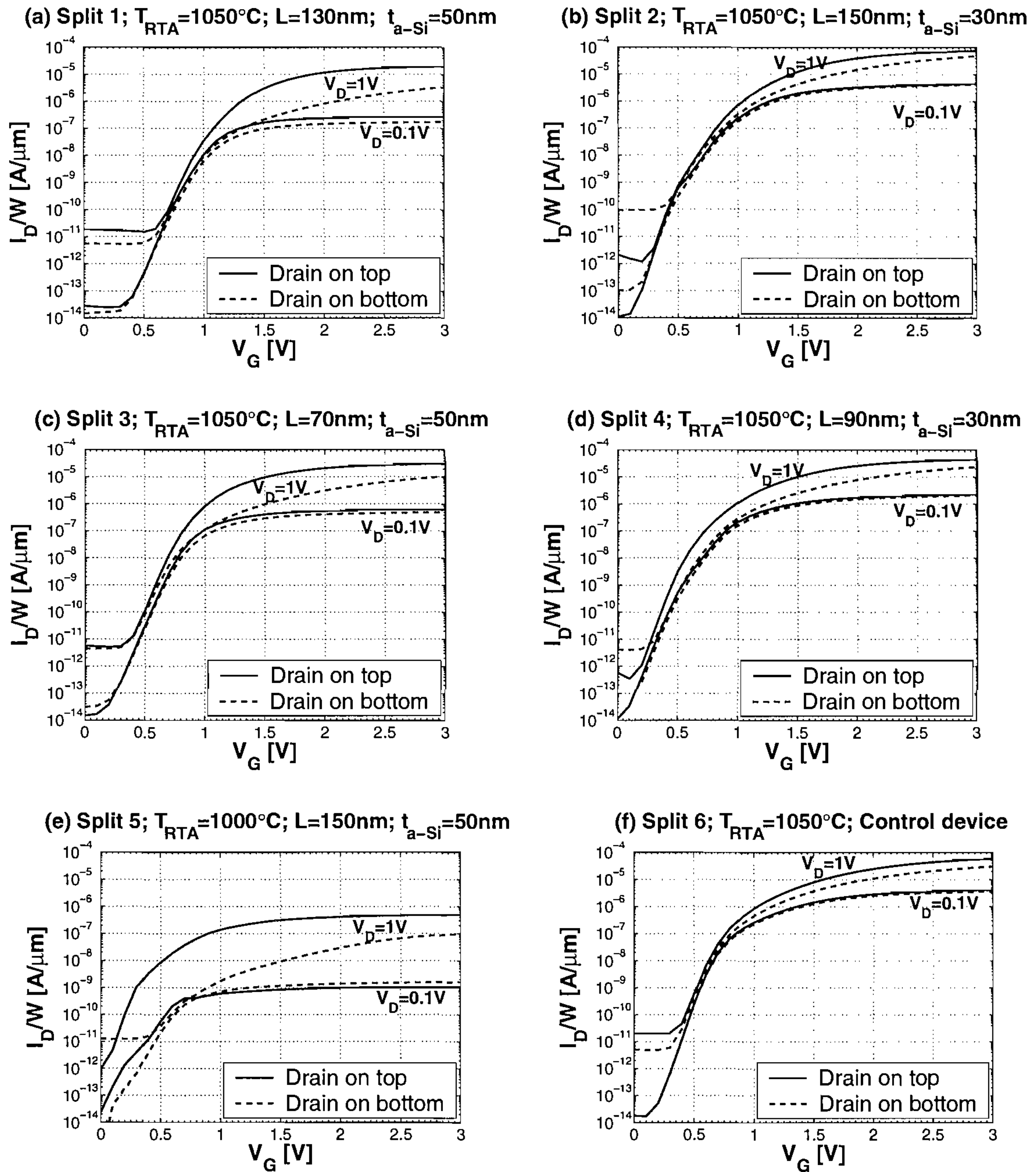

Figure 6.20: Logarithmic transfer characteristics of dielectric pocket vertical MOSFETs (figures a-e) and of a control device without dielectric pocket (figure f); the process splits are listed in table 5.2; T_{RTA} = Rapid Thermal Anneal Temperature; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition; $V_S = V_B = 0$V.

each process split investigated. Figure 6.21(a) shows the transfer characteristics of a dielectric pocket vertical MOSFET with a thin spacer connecting drain and body and with a long channel (L = 150 nm). Figure 6.21(b) displays the characteristics of a short channel dielectric pocket vertical MOSFET (L = 90 nm) with a thin spacer. Finally the transfer characteristics of a control vertical MOSFET without dielectric pocket are shown in figure 6.21(c). An increased subthreshold slope is observed at

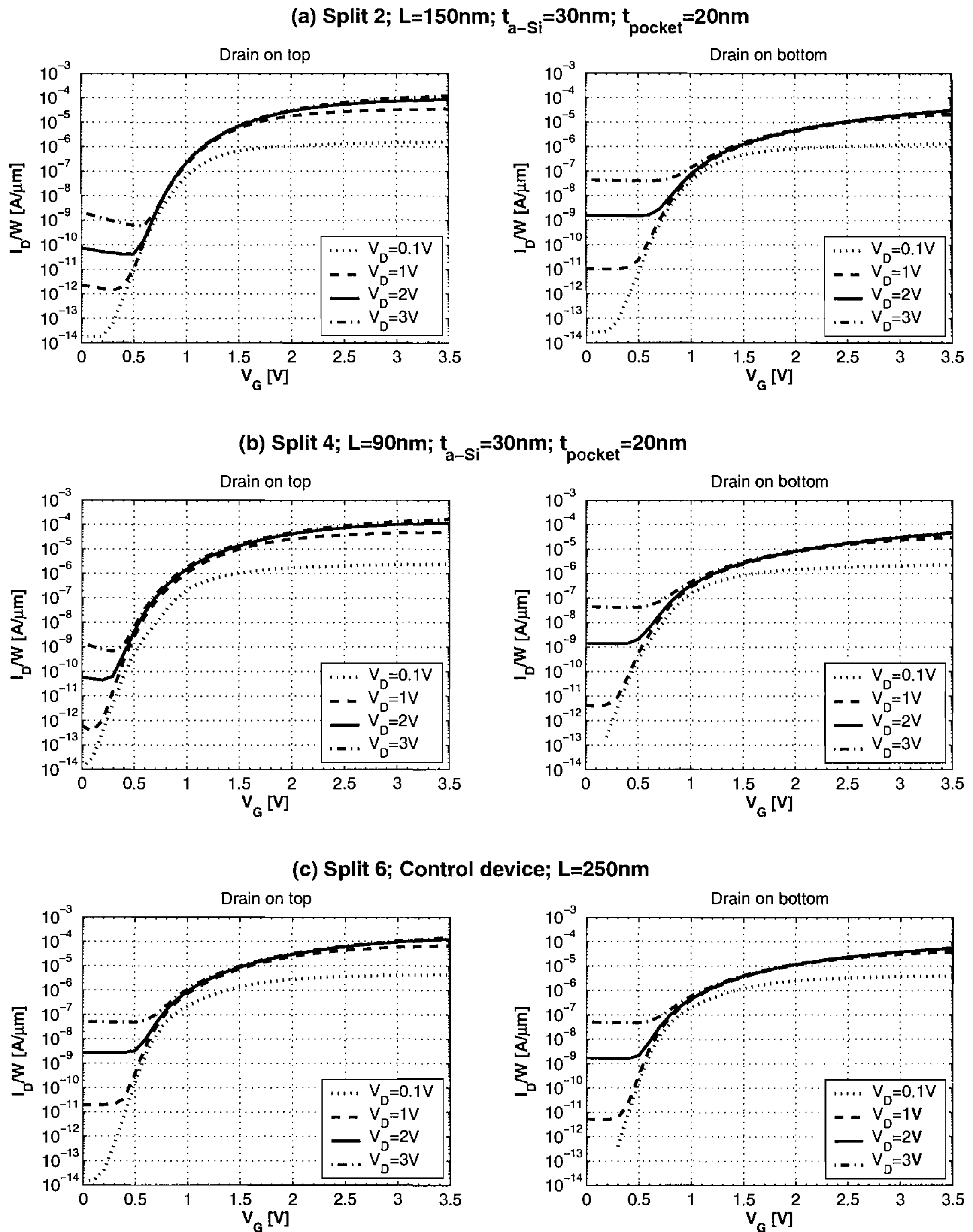

Figure 6.21: Comparison of the transfer characteristics of vertical MOSFETs with drain bias increasing from 0.1V to 3V; devices incorporating a dielectric pocket and a narrow polysilicon spacer (figures a-b) are compared with a control device (figure c); the process splits are listed in table 5.2; L = channel length; t_{a-Si} = thickness of the amorphous silicon layer after deposition; t_{pocket} = dielectric pocket thickness; $V_S = V_B = 0$ V.

V_D = 2 V and V_D = 3 V for dielectric pocket MOSFETs in the drain on bottom configuration. This is associated with a higher off-state drain leakage in the drain on

bottom than the drain on top configuration. This trend is not observed in the control devices without a dielectric pocket, where a subthreshold slope degradation and high off currents at $V_D = 2$ V and $V_D = 3$ V are observed in both configurations. No significant effect of the channel length on DIBL is observed in the dielectric pocket devices. The low impact of DIBL on sub-100 nm vertical MOSFETs can be attributed to the high body doping concentration, of the order of 3×10^{18} cm^{-3}.

6.7.2 Effect of process splits on output characteristics

Figure 6.22 shows the output characteristics of the fabricated vertical MOSFETs at $V_G = 3$ V. The characteristics displayed are strongly asymmetric between drain on top and drain on bottom measurement configurations. The asymmetry of the electrical characteristics has been investigated in section 6.6. The output characteristics in drain on bottom configuration show the beginning of breakdown, indicated by an upwards inflection of the $I_D(V_D)$ curve, at a drain bias of about 3.5 V. This is not observed in the characteristics of the dielectric pocket vertical MOSFETs in the drain on top configuration (figure 6.22(a)-(d)). On the other hand, a small inflection of the $I_D(V_D)$ characteristics of the control device is observed in both the drain on top and the drain on bottom configurations (figure 6.22(e)). Another feature of the curves presented in figure 6.22 is the non-ideal, diode-like behavior of the output characteristics in the linear region of operation, at low drain bias. This behavior is more marked in the characteristics of the dielectric pocket vertical MOSFETs rather than in those of the control device.

Figure 6.23 shows the output characteristics of a dielectric pocket vertical MOSFET from process split 1 plotted on a logarithmic scale. Drain, source and body currents are shown. The source current (I_{source}) is the current flowing in the channel of the device. The body current (I_{body}) is the leakage current of the reverse biased drain/body junction. The drain current (I_{drain}) is the sum of the channel current (I_{source}) and of the leakage current (I_{body}). In the drain on top configuration (figure 6.23(a)), at $V_D = 4.5$V, the leakage current (I_{body}) is about two orders of magnitude lower than the channel current (I_{source}). In contrast, in the drain on bottom configuration (figure 6.23(b)), at $V_D = 4.5$V, the leakage current (I_{body}) is higher than the channel current (I_{source}). Consequently, in the output characteristics (figure 6.22(a)) the beginning of breakdown is observed in the drain on bottom configuration but not in the drain on top configuration. This is due to enhanced leakage current of the reverse biased drain/body junction in the drain on bottom configuration.

Figure 6.24 shows the output characteristics of a control device from process split 8 plotted on a logarithmic scale. In the drain on top configuration (figure 6.24(a)), at $V_D = 4.5$V, the leakage current (I_{body}) is only about one order of magnitude lower

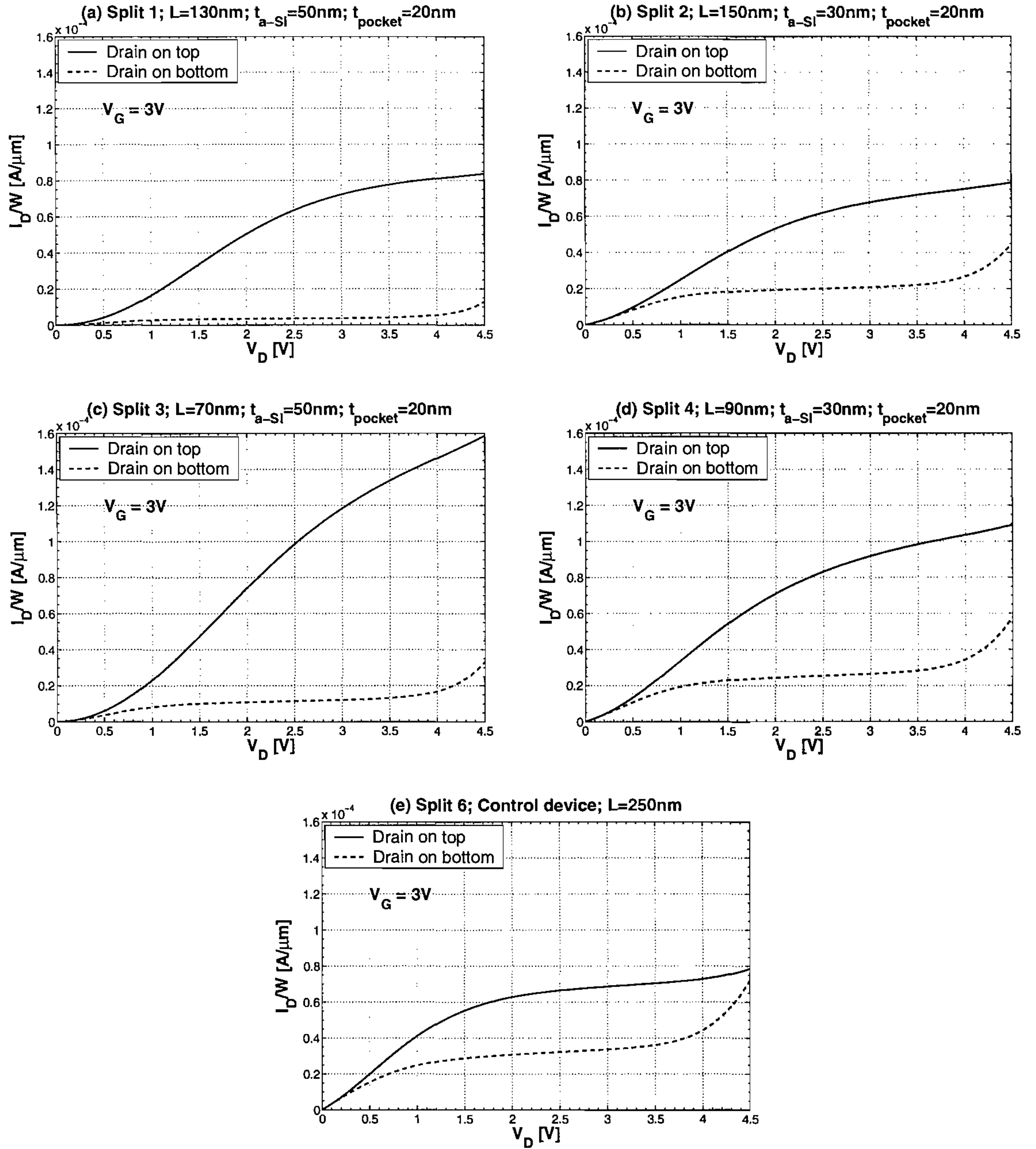

Figure 6.22: Linear output characteristics of dielectric pocket vertical MOSFETs (figures (a)-(d)) and of a control device (figure (e)) at V_G = 3V; the process splits are listed in table 5.2; L = channel length; t_{a-Si} = thickness of the amorphous silicon spacer after deposition; t_{pocket} = dielectric pocket thickness; V_S = V_B = 0V.

than the channel current (I_{source}). Consequently, the beginning of breakdown can also be observed in the drain on top output characteristic of the control device, shown in figure 6.22(e). This is not the case for the devices with a dielectric pocket, which have a lower drain leakage current (I_{body}) in the drain on top configuration.

In order to quantify the diode-like operation of the devices observed at low drain bias (figure 6.22), the shift of the $I_D(V_D)$ characteristics from the origin ($\Delta I_D(V_D)$) is calculated, as shown in figure 6.25, at V_G = 3 V. The $\Delta I_D(V_D)$ of an output

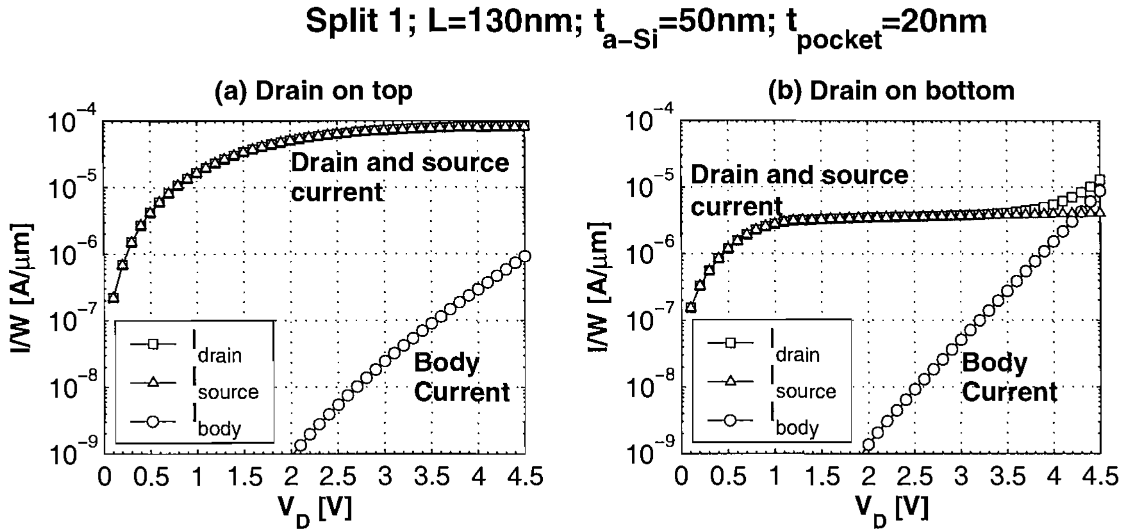

Figure 6.23: Output characteristics at V_G = 3V of a dielectric pocket vertical MOSFET from process split 1 (table 5.2) in logarithmic scale; I_{drain} = drain current; I_{source} = source current; I_{body} = body current; $V_S = V_B = 0$ V.

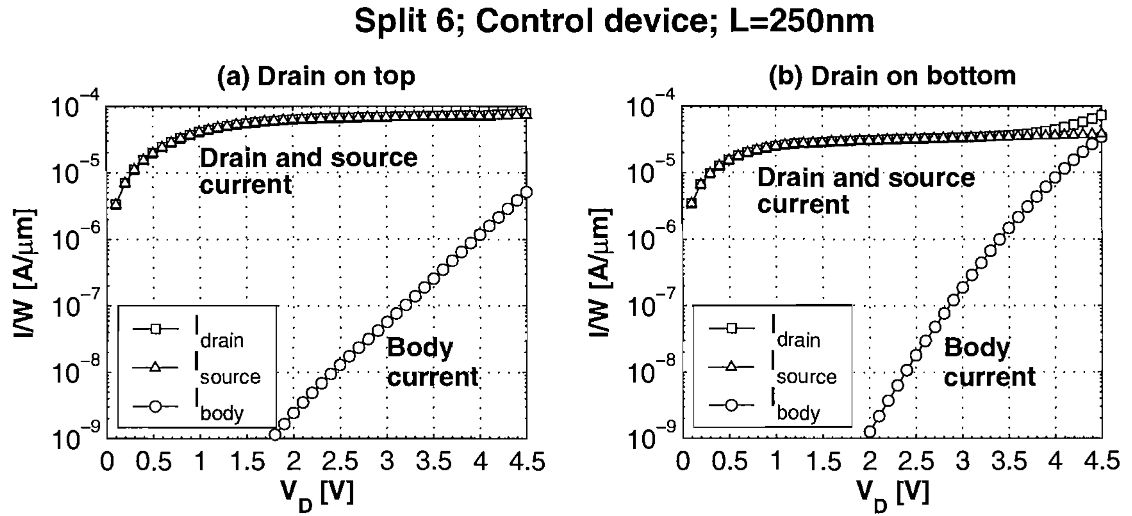

Figure 6.24: Output characteristics at V_G = 3V of a control device from process split 6 (table 5.2) in logarithmic scale; I_{drain} = drain current; I_{source} = source current; I_{body} = body current; $V_S = V_B = 0$ V.

characteristic is defined as the intercept with the x-axis of a line tangential to the linear region of the $I_D(V_D)$ curve, as shown in figure 6.25(a). Figure 6.25(b) shows the value of $\Delta I_D(V_D)$ for different process splits. Higher values of $\Delta I_D(V_D)$ are seen in the drain on top than in the drain on bottom configuration. The devices with a thicker spacer connecting drain and body (process splits 1 and 3) show a higher $\Delta I_D(V_D)$ than the devices with a thinner spacer (process splits 2 and 4). The control device shows the lowest value of $\Delta I_D(V_D)$ in the drain on top configuration and an ideal output characteristic ($\Delta I_D(V_D) = 0$ V) in the drain on bottom configuration.

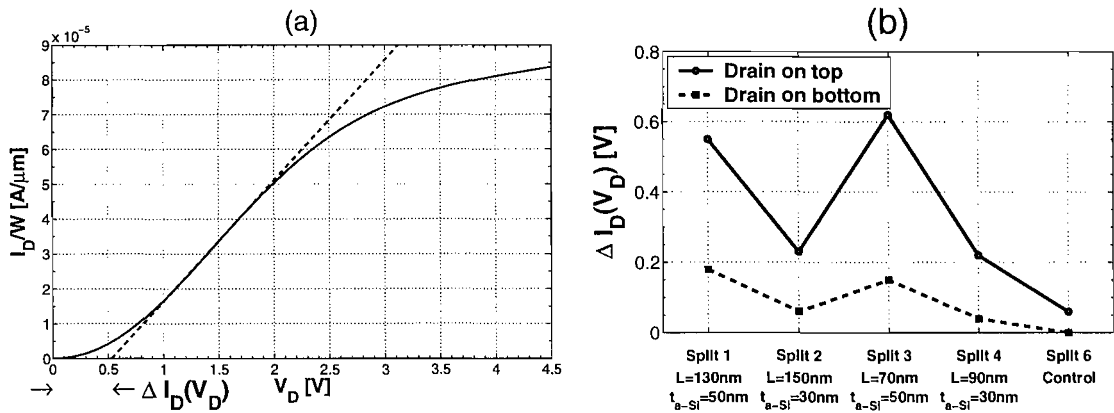

Figure 6.25: (a) Method used for the calculation of the shift from the origin ($\Delta I_D(V_D)$) of output characteristics. (b) Shift from the origin of the $I_D(V_D)$ characteristics of devices from different process splits, listed in table 5.2, in drain on top and drain on bottom configuration; L = channel length; t_{a-Si} = thickness of the amorphous silicon spacer after deposition; $V_S = V_B = 0V$; $V_G = 3$ V.

6.8 Effect of process splits on diode characteristics

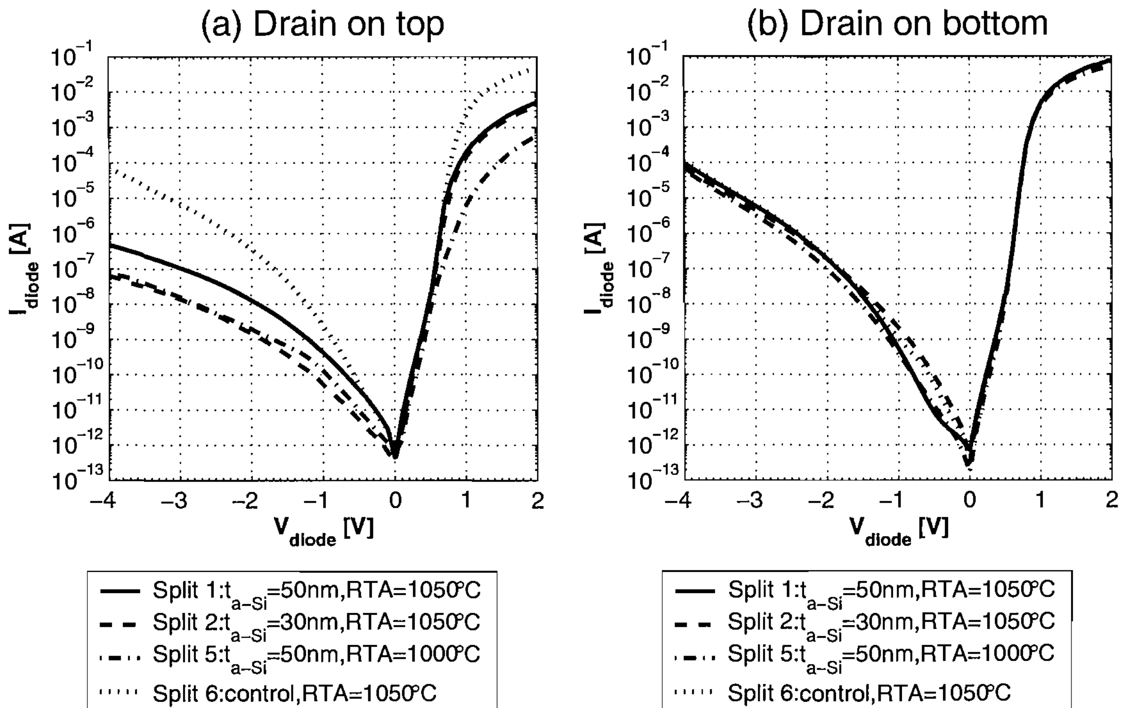

Figure 6.26: Current-voltage diode characteristics in logarithmic scale of vertical MOSFETs from different process splits, listed in table 5.2, in drain on top and drain on bottom configurations; t_{a-Si} = thickness of the amorphous silicon layer after deposition; RTA = Rapid Thermal Annealing temperature; the process splits are listed in table 5.2.

To gain a better understanding of the electrical characteristics of the source/body and of the drain/body junctions of dielectric pocket vertical MOSFETs, each junc-

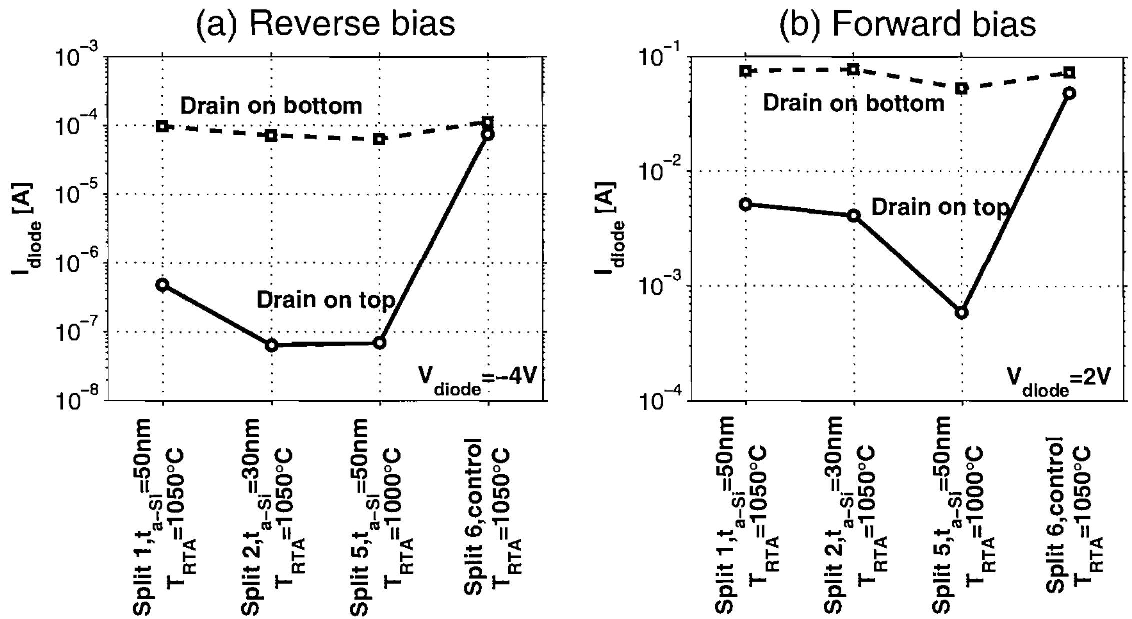

Figure 6.27: Comparison of the diode current dependence in (a) reverse and (b) forward bias of devices from different process splits, listed in table 5.2, in drain on top and drain on bottom configuration; t_{a-Si} = thickness of the amorphous silicon layer after deposition; T_{RTA} = Rapid Thermal Annealing temperature.

tion has been characterized independently by diode current-voltage measurements, as shown in figure 6.26. In the drain on top configuration (figure 6.26(a)), an effect of the Rapid Thermal Annealing (RTA) temperature on the diode current can be observed in forward bias ($V_{diode} > 0V$). Devices annealed at a low RTA temperature (1000°C, process split 5) have a forward bias diode current which is a decade lower than that of dielectric pocket MOSFETs annealed at 1050°C. Furthermore, a comparison of devices annealed at 1050°C shows that the control device without a dielectric pocket has a forward bias current a decade higher than the dielectric pocket devices. When the junction is reverse biased ($V_{diode} < 0V$), in the drain on top configuration (figure 6.26(a)) the control device has a diode current more than two decades higher than the dielectric pocket MOSFETs. In the drain on bottom configuration (figure 6.26(b)) no significant difference is observed between the diode characteristics of control devices and dielectric pocket devices annealed at 1050°C. However, a small diode current reduction in the drain on bottom configuration is observed for the dielectric pocket vertical MOSFET annealed at lower temperature (1000°C, process split 5), presumably due to reduced dopant activation.

A quantitative evaluation of the effect of process splits on the asymmetry between the diode characteristics in drain on top and drain on bottom configurations is presented in figure 6.27. The value of the reverse bias diode current at V_{diode} = -4 V is shown in figure 6.27(a). The dielectric pocket MOSFETs have a reverse bias diode current 2-3 decades lower in drain on top configuration than in drain on bottom.

On the other hand, the control device shows no significant difference in the value of reverse bias diode current of the top and bottom junctions. Figure 6.27(b) presents a comparison of the forward bias diode current of different process splits, measured at V_{diode} = 2V. The dielectric pocket MOSFETs annealed at 1050°C have a forward bias diode current about one decade lower in the drain on top than in the drain on bottom configuration. This asymmetry is enhanced in the case of the dielectric pocket MOSFET annealed at 1000°C, where the forward bias diode current in drain on top is about 2 decades lower than in drain on bottom. On the other hand, no significant asymmetry of the diode characteristic in forward bias is observed in the case of the control device.

6.9 Discussion

Surround gate dielectric pocket vertical MOSFETs were fabricated for the first time with a novel polysilicon spacer process. Devices with channel lengths down to 70nm were fabricated with a low cost and CMOS compatible process. This is comparable with state of the art vertical nMOSFETs with channel length down to 50nm fabricated in the past by Schulz et al. [48] and Hergenrother et al. [37]. The fabricated devices were structurally characterized by SIMS profiling and SEM microscopy, allowing the extraction of doping concentration, drain junction depth and channel length. SIMS analysis on wafers containing only the drain polysilicon layer gave a vertical penetration depth of the drain junction into the single-crystal silicon of around 30nm. The polysilicon spacer thickness was measured by SEM cross-sections of fabricated devices, yielding a minimum spacer thickness of about 20nm. This yields an upper limit for the drain junction depth into the pillar sidewall of 50nm. However, in the dielectric pocket vertical MOSFETs, the drain dopant also has to diffuse through the polysilicon spacer layer and through the interfaces between the polysilicon drain, the spacer and the single-crystal silicon substrate. These considerations lead us to suppose that the drain junction depth into the pillar sidewall is considerably less than 50nm.

The reproducibility of the fabrication process across the wafers was investigated by measuring the transfer characteristics of surround gate MOSFETs across the wafer surface. All the process splits, except one (process split 1) showed good reproducibility of the transfer characteristics both in drain on top and drain on bottom configurations.

The dielectric pocket and the control vertical MOSFETs had threshold voltage values between 0.9 V and 1.1 V, as shown in section 6.6. All the devices had a 3 nm thick gate oxide, measured on the horizontal <100> surface of test wafers. The gate oxide was grown on the vertical pillar sidewall which had <110> crystallographic orientation. A 40% difference between the oxide thickness on <100> and <110>

surfaces has been reported in the literature [92], yielding an oxide 4.2 nm thick on the vertical sidewalls of the devices. A threshold voltage of 1 V can be calculated using equation 2.10 for a long channel MOSFET with a 4.2 nm thick gate oxide and a channel doping concentration of 3×10^{18} cm^{-3}, extracted from the SIMS profiles of the fabricated devices (see section 6.3). The calculated value is in good agreement with the experimental value of 0.9 - 1.1 V.

All the devices showed asymmetric electrical characteristics when their source and drain were exchanged, with better performance when the drain was on the top of the active pillar. An analysis of process parameters confirmed that, even though the threshold voltage of the vertical MOSFETs was symmetric, the devices had higher on-state drain current and gate transconductance in the drain on top than in the drain on bottom configuration. The output characteristics of the devices were also asymmetric. An early beginning of breakdown was observed in the drain on bottom configuration, which was not observed in the drain on top configuration. This was due to enhanced drain/body junction leakage when the drain was at the bottom of the pillar. The output characteristics showed a rectifying behavior at low drain bias which was more pronounced in the drain on top measurement configuration. The asymmetry was further investigated by diode measurements that allowed the separate characterization of the top and bottom drain/body junctions. The bottom junction of the dielectric pocket devices showed higher diode current in forward bias and enhanced diode leakage in reverse bias compared with the top drain/body junction.

The effect of process splits on the asymmetry of the transistor electrical characteristics in drain on top and drain on bottom configurations was investigated. Dielectric pocket vertical MOSFETs with a thick spacer connecting drain and body (50 nm thick after amorphous silicon deposition) were found to have more asymmetric electrical characteristics than the devices with a thin spacer. Control devices without dielectric pocket displayed the least asymmetry. Diode measurements showed that the forward bias diode current of the top drain/body junction was lower in dielectric pocket devices than in control devices. On the contrary, no significant difference was found between the diode characteristics of the bottom drain/body junctions of devices with and without a dielectric pocket. This can be explained by the larger area of the top drain/body junction of the control devices compared with the dielectric pocket devices. The area of the top drain/body junctions of the control devices can be estimated to be about 30 times larger than that of dielectric pocket devices. This value is comparable with a measured ratio of 10 between the forward bias diode currents of the control devices and of the dielectric pocket devices (see figure 6.26). The difference in the two values is due to the different doping profile of the top junctions in the control devices and in the dielectric pocket devices, and by the imprecision in the estimation of the area of the junctions, which cannot be measured directly.

The effect of the activation anneal temperature on the electrical characteristics of

the devices was also investigated. A lower anneal temperature was found to degrade considerably the transfer characteristics of the devices. For example, the on-state drain currents of devices annealed at 1000°C were found to be two orders of magnitude lower than those of devices annealed at 1050°C. A lower annealing temperature yielded a considerable reduction of the forward bias diode current in the drain on top configuration. On the other hand, the effect of the annealing temperature on the bottom junction was much smaller, causing only a small reduction of the forward bias diode current. The low values of on-current and diode current measured in figures 6.20(e) and 6.26 on the device annealed at 1000°C point to the importance of series resistance in the dielectric pocket. In this device, a lower anneal temperature would be expected to increase both the polysilicon spacer resistance and the interface resistance. The spacer resistance would be higher because there would be less diffusion of arsenic into the polysilicon spacer. Moreover, at a lower activation temperature a lower proportion of the arsenic in the polysilicon spacer would be electrically active. The interface resistance between the drain, the polysilicon spacer and the body would also be higher because there would be less break-up of the native oxide which is likely to be located at these interfaces during the low temperature RTA [104].

The asymmetry of the electrical characteristics between drain on top and drain on bottom configurations can be explained by the presence of two insulating layers at the drain/polysilicon spacer interface and at the polysilicon spacer/drain interface. As discussed above, the asymmetry of the electrical characteristics is more marked in the devices with a thicker spacer and is lowest in the control devices without a dielectric pocket. As explained in section 5.4.2, the amorphous silicon spacer was deposited in a furnace by LPCVD. The deposition was timed in order to obtain the thickness required. For this reason, different thicknesses required separate depositions. Thus the devices with a thick spacer (process splits 1 and 3, with an amorphous silicon layer 50 nm thick after deposition) had the amorphous silicon deposited in a separate run from the devices with a thin spacer (process splits 2 and 4, with an amorphous silicon layer 30 nm thick after deposition). Although before deposition the wafers were briefly etched in hydrofluoric acid to remove any native interfacial oxide, a native oxide layer could grow on exposed surfaces during the transfer to the furnace and during the loading. The lower asymmetry in devices with the thinner spacer than those with thicker spacer suggests that the native oxide layer is thinner in the devices with the thin spacer. Moreover, in the case of the devices incorporating a dielectric pocket, two interfaces are present (drain/spacer and spacer/body), whereas in the case of the control devices only one interface is present (between drain and body). This explains the lower asymmetry in the control devices than the dielectric pocket devices.

The above arguments have shown that the origin of the asymmetric electrical char-

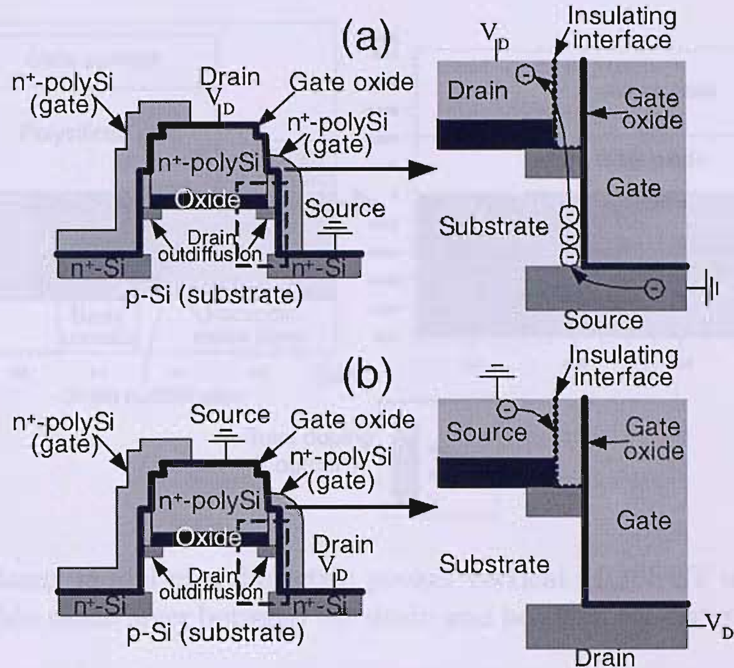

Figure 6.28: Schematic representation of the conduction mechanism of dielectric pocket vertical MOSFETs in different measurements configurations. (a) Drain on top configuration. (b) Drain on bottom configuration.

acteristics is the presence of two insulating layers between the drain, the thin polysilicon spacer and the body of the dielectric pocket vertical MOSFETs. These layers are labeled "insulating interface" in figure 6.28, which shows a schematic cross-section of a dielectric pocket vertical MOSFET in the drain on top and drain on bottom configurations. When the transistor is biased with the drain on the top of the pillar (figure 6.28(a)), the channel forms next to the source, on the bottom of the pillar. The electrons flow in the channel from the source and tunnel through the insulating interface between the drain and the channel thanks to the drain/source bias. On the contrary, when the transistor is biased with the drain on the bottom of the pillar (figure 6.28(b)), the insulating layer initially prevents the flow of electrons from the source in the channel of the device. A considerable tunneling of electrons from the source to the channel of the device is possible only when the gate voltage is high enough to form an inversion layer throughout the channel, and the drain/source bias is applied at the source/channel interface. In the drain on bottom configuration the devices therefore have a lower drive current. This model, summarized in figure 6.28, also explains the non ideal, diode-like behavior of the output characteristics. In drain on top configuration and at low drain bias, the characteristics are dominated by the tunneling of electrons through the two insulating regions. This causes the rectifying behavior observed in the output characteristics at low drain bias. At higher drain bias, enough electrons are able to tunnel through the interface and the output characteristics are dominated by the transistor action.

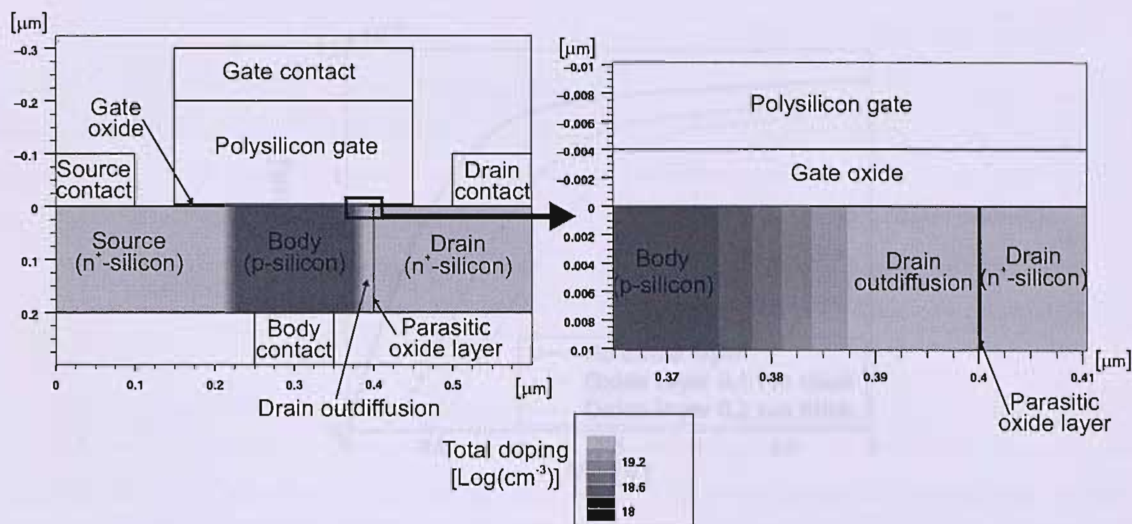

Figure 6.29: Planar model of a dielectric pocket vertical MOSFET used to simulate the effect of a thin oxide layer between the drain and body on the output characteristic of the device.

Device simulations were performed, in order to assess qualitatively the effect of introducing a parasitic insulating layer between the drain and body of a MOSFET. For this purpose, the simplified model of a planar MOSFET shown in figure 6.29 was drawn, using a Structure Editor software in order to simplify the simulations as much as possible. The structures simulated consisted of planar MOSFETs with a 4 nm thick gate oxide and 150 nm channel length. Device simulations were performed on three different structures: the first was a conventional planar MOSFET, while the second and the third had parasitic oxide layers, 0.1 nm and 0.2 nm thick respectively, separating the drain from the body, as shown in figure 6.29. The purpose of the simulations was to check qualitatively if the introduction of a thin oxide layer between the drain and the body of a MOSFET gives rise to a rectifying behavior in the output characteristics of the device. This would confirm the hypothesis that the rectifying behavior in the output characteristics of dielectric pocket vertical MOSFETs is due to the presence of parasitic insulating layers at the drain / polysilicon spacer interface and at the polysilicon spacer / body interface. Moreover, an increased shift of the output characteristics from the origin would be expected when the thickness of the parasitic interfacial layer is increased.

The script files used for the simulations are reported in appendix B.2. More details on the experimental procedure can be found in chapter 6.2.4. Figure 6.30 shows the simulated output characteristics. Tunneling of electrons through the thin parasitic oxide layer was simulated by activating the Fowler-Nordheim tunneling model [96] during the simulations. The model quantifies the tunneling of electrons from the drain conduction band into the insulator conduction band. The electrons are then swept into the drain extension by the electric field. Figure 6.30 shows that an ideal

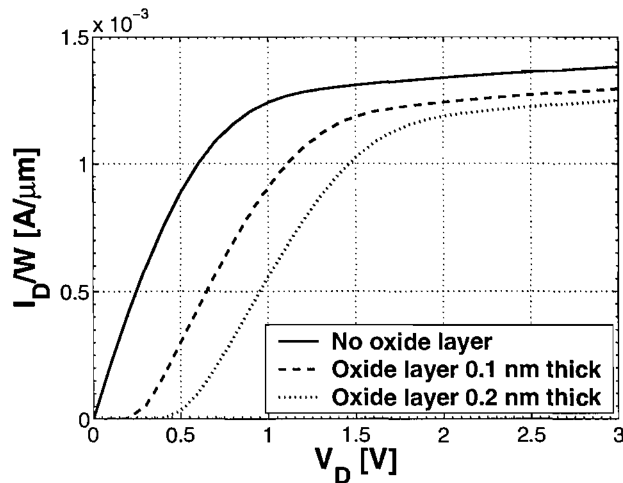

Figure 6.30: Simulated output characteristics based on the planar model of a dielectric pocket vertical MOSFET shown in figure 6.29; $V_G = 3$ V; $V_S = V_B = 0$ V.

$I_D(V_D)$ characteristic is obtained from the simulation of the structure without the parasitic oxide layer. On the other hand, when a thin oxide layer is present, the output characteristic shows rectifying behavior at low drain bias. The linear region of the $I_D(V_D)$ characteristic is shifted from the origin. The shift increases when the thickness of the parasitic oxide increases from 0.1 to 0.2nm. This behavior reproduces the experimental results discussed in the previous sections.

Table 6.3 shows a comparison of the performance of a 70 nm dielectric pocket vertical MOSFET, a Low Standby Power planar MOSFET [95], a conventional vertical MOSFET with ion implanted source and drain [48], a Vertical Replacement Gate (VRG) vertical MOSFET [37] and a surround gate FILOX vertical MOSFET (see chapter 3). It can be observed that the dielectric pocket vertical MOSFET is comparable or outperforms the other technologies on most performance indicators. In particular, the dielectric pocket device has lower off-state drain leakage, DIBL and subthreshold slope than the VRG, the sidewall and the planar MOSFETs. On the other hand, the drive current of the dielectric pocket vertical MOSFET is about one order of magnitude lower than that of the other technologies. This is likely to be due to the presence of parasitic interface layers, probably composed of silicon dioxide, between the drain, the thin polysilicon spacer and the channel on the drain sidewall. Two possible solutions can be implemented to suppress these parasitic interfaces. The amorphous silicon spacer could be deposited by LPCVD in a cluster tool. The native oxide could then be removed prior to amorphous silicon deposition by an in-situ surface clean [105]. Another approach could be a high dose silicon ion implantation with a large tilt angle to break up the native oxide layers after deposition of the amorphous silicon spacer in a conventional LPCVD furnace [63].

Type of MOSFET	LSTP [95]	Sidewall [48]	Sidewall [48]	VRG [37]	FILOX [73]	DP
L [nm]	75	100	50	50	125	70
t_{ox} [nm]	2.2	3	3	2.8	3.3	3
N_A [10^{18} cm^{-3}]	-	2	7	3.5	2	3
V_{DD} [V]	1.2	1.5	1.5	1.5	1	1
I_{on} [$\mu A/\mu m$]	410	240	80	100	92	18
I_{off} [$A/\mu m$]	1×10^{-5}	5×10^{-12}	2×10^{-8}	3×10^{-11}	2.5×10^{-12}	5×10^{-12}
V_t [V]	0.5	0.6	1.5	0.73	1.4	0.9
S [mV]	-	102	166	105	103	92
DIBL [mV]	-	70	300	90	50	50

Table 6.3: Comparison of structural and electrical parameters of dielectric pocket vertical MOSFETs with state of the art vertical and planar MOSFETs (data from the literature); Planar LSTP = Low Standby Power planar MOSFET [95]; Sidewall = conventional CMOS compatible vertical MOSFET [48]; VRG = Vertical Replacement Gate vertical MOSFET [37]; FILOX = surround gate FILOX vertical MOSFET (see chapter 3); DP = dielectric pocket vertical MOSFET, process split 3 in table 5.2; L = channel length; t_{ox} = gate oxide thickness; N_A = body doping concentration; I_{on} = on current (extracted at V_G - V_t = 1 V, V_D = V_{DD}; for LSTP [95] extracted at V_G = V_D = V_{DD}); I_{off} = off current at V_D = V_{DD}, V_G = 0 V; V_t = threshold voltage; S = subthreshold slope at V_D = V_{DD}; DIBL = drain induced barrier lowering at V_D = V_{DD}.

6.10 Summary

In this chapter experimental characteristics of dielectric pocket vertical nMOSFETs fabricated with a novel process have been presented. Surround gate dielectric pocket vertical MOSFETs with channel lengths down to 70 nm were fabricated and characterized. SIMS analysis and SEM cross-sections gave a drain outdiffusion depth into the single-crystal silicon of 30 nm and a polysilicon spacer thickness of about 20 nm, yielding a drain junction depth into the pillar sidewall of less than 50 nm. Electrical characteristics performed to assess the reliability of the fabrication process confirmed that the device characteristics were reproducible across the silicon wafers. The vertical MOSFETs showed asymmetric output and transfer characteristics, with higher drive currents measured with the drain on the top than the drain on the bottom of the active pillar. Moreover, a considerable degradation of the electrical characteristics was observed at a lower anneal temperature of 1000°C. The 70 nm dielectric pocket vertical MOSFETs showed excellent values of subthreshold slope (92 mV), off-state drain current (5×10^{-12} $A/\mu m$) and had a threshold voltage of 0.9 V. The on-current varied strongly with RTA temperature and was 18 μA/μm for an RTA of 20 seconds at 1050 °C. The low value of drive current is caused by parasitic drain series resistance due to the presence of native oxide layers at the two interfaces of

the polysilicon spacer with the polysilicon drain and with the single-crystal silicon substrate. This problem can be overcome by minor process modifications, such as depositing the spacer layer in a cluster tool after an in-situ surface clean [105] or using a high dose silicon implant with a large tilt angle to break up the native oxide layers [63].

Chapter 7

Investigation of the role of a polysilicon drain on source and drain diffusion in short channel vertical MOSFETs

7.1 Introduction

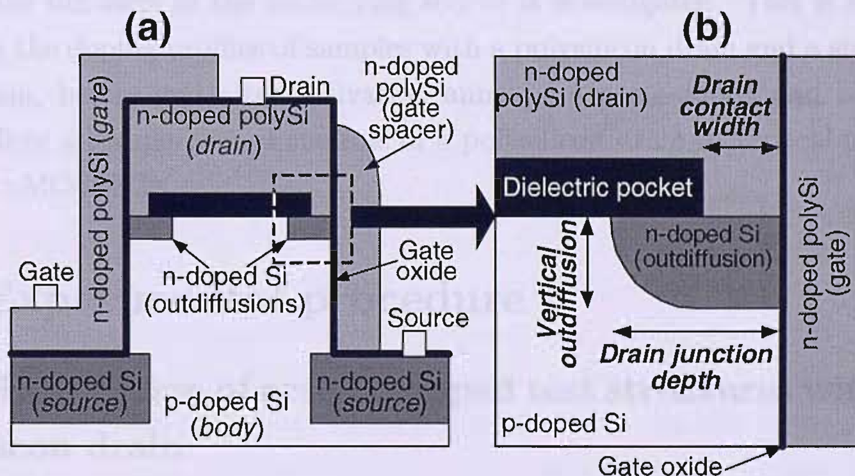

Figure 7.1: (a) Schematic cross-section of the active pillar of a dielectric pocket vertical MOSFET. (b) Magnification of the shallow drain/body junction of a dielectric pocket vertical MOSFET.

The incorporation of a dielectric pocket between the drain and body allows CMOS compatible vertical MOSFETs to be fabricated with shallow drain junctions, as shown in figure 7.1. During the activation anneal, drain dopants outdiffuse from the polysilicon drain into the single-crystal silicon body of the vertical MOSFET along the perimeter of the pillar. The dielectric pocket prevents the outdiffusion of

drain dopants in the center of the active pillar. This generates drain outdiffusion regions around the perimeter of the pillar. The drain junction depth is indicated in figure 7.1(b). This is the sum of the drain contact width (defined as the distance between the edge of the dielectric pocket and the gate oxide) and of the lateral outdiffusion of the drain dopants. This second component is approximately equal to the vertical outdiffusion of dopants from the drain, shown in figure 7.1(b). In order to minimize the drain junction depth it is necessary to minimize both the drain contact width and the vertical outdiffusion of the drain dopants into the single-crystal silicon body.

The drain contact width can be tuned by choosing the thickness of the amorphous silicon spacer that is deposited in order to connect the drain to the body of the device, as discussed in section 5.4.2. On the other hand, the vertical outdiffusion of the drain dopants depends on the annealing conditions chosen for dopant activation. It is worth pointing out that, as the drain of the devices is made of polysilicon, an insufficient outdiffusion of drain dopants into the single-crystal silicon body could compromise the electrical performance. The thermal budget of the fabrication process must be optimized in order to fabricate shallow drain junctions and at the same time ensure good electrical performance.

In this chapter diffusion experiments are carried out to optimize the drain junction depth of dielectric pocket vertical MOSFETs. Moreover, the role of the polysilicon drain on the diffusion of the underlying source is investigated. This is achieved by comparing the doping profiles of samples with a polysilicon drain and a single-crystal silicon drain, before and after activation anneal. Arsenic-doped and boron-doped samples allow a comparison of the role of a polysilicon drain in vertical pMOSFETs as well as nMOSFETs.

7.2 Experimental procedure

7.2.1 Fabrication of arsenic-doped test structures with a polysilicon drain

Figure 7.2 shows a schematic layout of the test structures fabricated to investigate the role of a polysilicon drain on arsenic diffusion in vertical MOSFETs. The test structures reproduce the source, body and drain regions of a vertical n-type MOSFET with a polysilicon drain (figure 7.2(a)) and with a single-crystal silicon drain (figure 7.2(b)). The test structures with a polysilicon drain had a lightly doped silicon layer, reproducing the body of a vertical MOSFET, sandwiched between a highly doped single-crystal silicon source and a highly doped polysilicon drain (figure 7.2(a)). The second type of test structure instead had both source and drain ion implanted in single-crystal silicon (figure 7.2(b)). Arsenic was used as the source and drain dopant

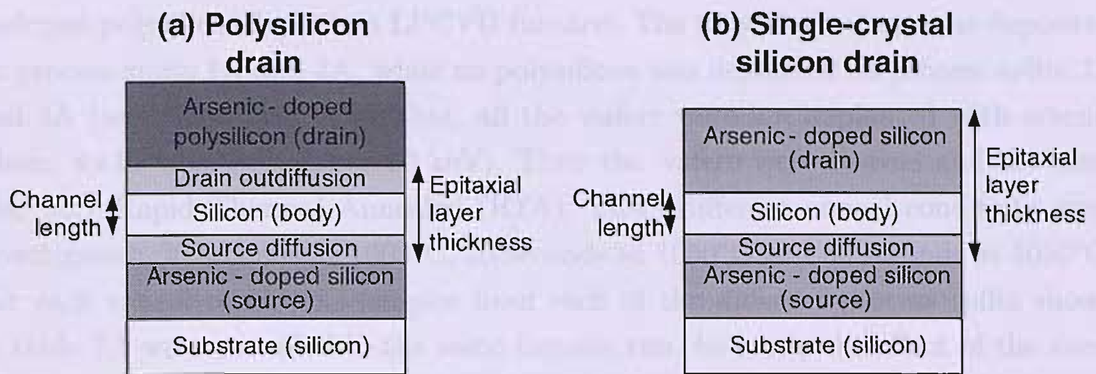

Figure 7.2: Schematic cross-sections of the arsenic-doped test structures fabricated to investigate the role of a polysilicon drain on arsenic diffusion in vertical MOSFETs.

Process split	Source/drain dopant	Drain material	Epitaxial layer thickness [nm]
1A	Arsenic	Polysilicon	180
2A	Arsenic	Polysilicon	350
3A	Arsenic	Silicon	300
4A	Arsenic	Silicon	440

Table 7.1: Process splits fabricated to investigate the role of a polysilicon drain on arsenic diffusion in vertical MOSFETs. The column labeled "Epitaxial layer thickness" reports the thickness of the epitaxial silicon layer after deposition.

in this experiment.

Four arsenic-doped process splits were fabricated, as shown in table 7.1. The batch listing of the fabrication process is reported in appendix A.3. Boron-doped silicon wafers with resistivity 17-33 Ωcm and <100> crystallographic orientation served as the starting material for the arsenic-doped structures. A 20 nm thick sacrificial oxide layer was grown on the silicon substrate in order to screen the surface from ion implantation damage. Arsenic was ion implanted into the silicon substrate (dose: 2×10^{15} cm^{-2}; energy: 40 keV) to form the source of the structure. This was followed by a drive-in and recrystallization anneal at 1100°C (10 minutes in oxygen followed by 30 minutes in nitrogen). The first stage of the anneal was performed in oxygen to prevent pitting on the silicon substrate, which would have compromised the ensuing epitaxial growth. After anneal, all the oxide was removed by wet etch in hydrofluoric acid.

A monocristalline, lowly doped p-type silicon layer (boron concentration: 2×10^{17} cm^{-3}) was grown by epitaxy in an LPCVD reactor at 800°C on top of the arsenic-implanted substrate. The native oxide was removed prior to amorphous silicon deposition by an in-situ surface clean [105]. Table 7.1 reports the thickness of the epitaxial layers grown in different process splits. A short wet etch in hydrofluoric acid was performed in order to remove the native oxide, followed by deposition of a 200 nm thick

undoped polysilicon layer in a LPCVD furnace. The polysilicon drain was deposited on process splits 1A and 2A, while no polysilicon was deposited on process splits 3A and 4A (see table 7.1). After that, all the wafers were ion implanted with arsenic (dose: 4×10^{15} cm^{-2}; energy: 50 keV). Then the wafers were cleaved and the samples were Rapid Thermal Annealed (RTA). Three different anneal conditions were investigated: 20 seconds at 1000°C, 20 seconds at 1050°C and 60 seconds at 1050°C. For each anneal condition, samples from each of the different process splits shown in table 7.1 were annealed in the same furnace run, to assess the effect of the same thermal cycle on samples with different structures.

7.2.2 Fabrication of boron-doped test structures with a polysilicon drain

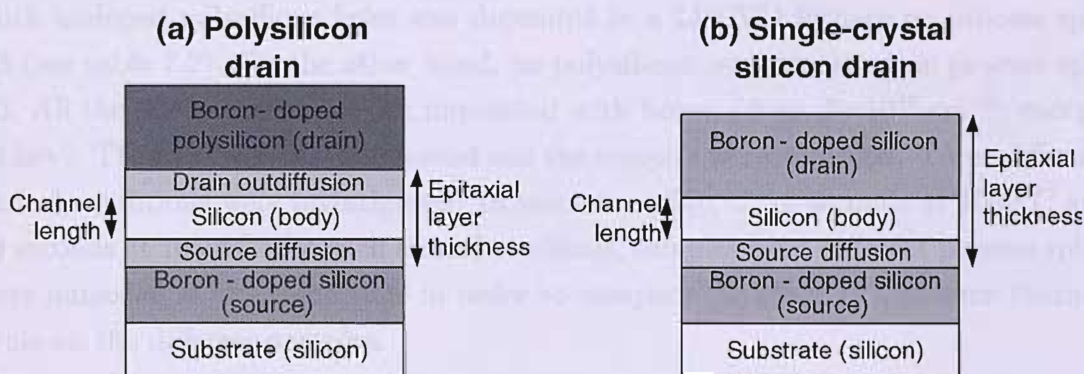

Figure 7.3: Schematic cross-sections of the boron-doped test structures fabricated to investigate the role of a polysilicon drain on boron diffusion in vertical MOSFETs.

Figure 7.3 shows a schematic layout of the test structures fabricated to investigate the role of a polysilicon drain on boron diffusion in vertical MOSFETs. The test structures reproduce the source, body and drain regions of vertical pMOSFETs with a polysilicon drain (figure 7.3(a)) and with a single-crystal silicon drain (figure 7.3(b)). In the first case, a lowly doped n-type silicon layer, reproducing the body of a vertical pMOSFET, was sandwiched between a boron-doped single-crystal source and a boron-doped polysilicon drain (figure 7.3(a)). In the second structure, both source and drain were made of boron-doped single-crystal silicon (figure 7.3(b)).

Two boron-doped process splits were fabricated, as shown in table 7.2. The batch listing of the fabrication process is reported in appendix A.4. Boron-doped silicon wafers with resistivity 17-33 Ωcm and <100> crystallographic orientation served as the starting material. After growing a 20 nm thick sacrificial oxide layer, boron was ion implanted into the silicon substrate (dose: 2×10^{15} cm^{-2}; energy: 20 keV) to form the source of the structure. After a drive-in and recrystallization anneal at 1100°C (10 minutes in oxygen followed by 30 minutes in nitrogen) the sacrificial oxide layer

Process split	Source/drain dopant	Drain material	Epitaxial layer thickness [nm]
1B	Boron	Polysilicon	280
2B	Boron	Silicon	470

Table 7.2: Process splits fabricated to investigate the role of a polysilicon drain on boron diffusion in vertical MOSFETs. The column labeled "Epitaxial layer thickness" reports the thickness of the epitaxial silicon layer after deposition.

was removed by wet etch in hydrofluoric acid.

After in-situ removal of the native oxide, a monocristalline, lightly doped n-type silicon layer (phosphorus concentration: 1×10^{18} cm^{-3}) was grown by epitaxy at 800°C on top of the boron-implanted substrate. Table 7.2 reports the thickness of the layers grown in the two process splits. After a short wet etch in hydrofluoric acid, a 200 nm thick undoped polysilicon layer was deposited in a LPCVD furnace on process split 1B (see table 7.2). On the other hand, no polysilicon was deposited on process split 2B. All the wafers were then ion implanted with boron (dose: 2×10^{15} cm^{-2}; energy: 20 keV). Then the wafers were cleaved and the samples were annealed. Three different anneal conditions were investigated: 10 seconds at 950°C, 10 seconds at 1000°C and 10 seconds at 1050°C. For each anneal condition, samples from different process splits were annealed at the same time in order to compare the effect of the same thermal cycle on the different samples.

7.2.3 Doping profile characterization

The doping profiles were characterized by Secondary Ion Mass Spectroscopy (SIMS). This technique employs a primary ion beam to sputter the silicon surface. A crater with depth proportional to the sputtering time is created in the substrate to be analyzed. The impurity concentration in the substrate is quantified by analyzing the secondary ions emitted during sputtering. The samples were analyzed using O_2^+ primary ion bombardment and positive secondary ion detection. These conditions combined good depth resolution with good sensitivity to boron and reasonable sensitivity to arsenic. The data were quantified using implanted reference materials and the depth scales were determined by measuring the sputtered crater depths by interference microscopy, yielding results accurate to ±5nm.

In order to compare quantitatively different samples and annealing conditions, the diffusion of dopant induced by the anneal was extracted from the measured doping profiles. The dopant diffusion was calculated as the linear distance between the doping profile before and after anneal at a reference doping concentration of 1×10^{18} cm^{-3}. An example is shown in figure 7.4, where figure (a) shows the doping profile of a sample with polysilicon drain and figure (b) shows the profile of a sample with

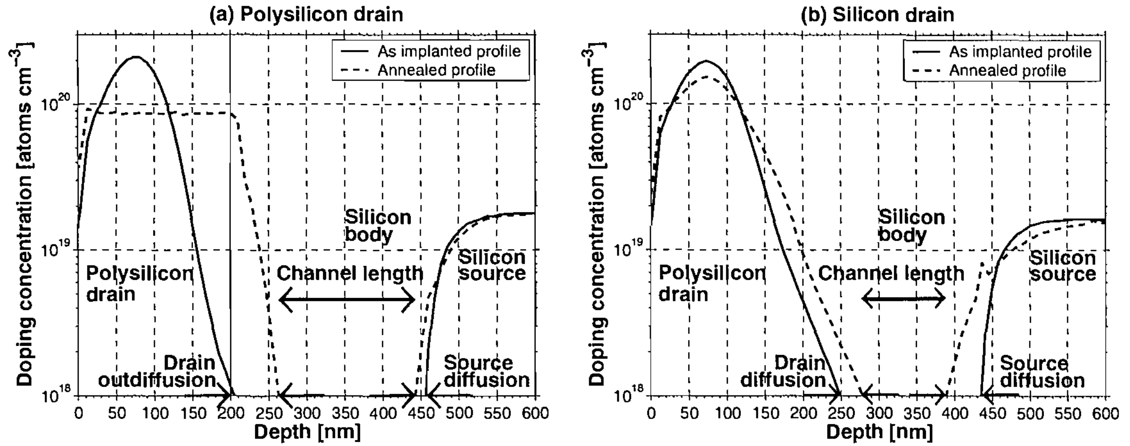

Figure 7.4: Example of extraction of dopant diffusion (or outdiffusion) and channel length from typical doping profiles of (a) a sample with polysilicon drain and (b) a sample with single-crystal silicon drain.

single-crystal silicon drain. In the case of the samples with polysilicon drain, the outdiffusion of dopants from the drain was calculated as the distance between the polysilicon/silicon junction and the annealed profile at a doping concentration of 1×10^{18} cm^{-3}, as shown in figure 7.4(a). The channel length was extracted as the linear distance between the doping profiles at a reference doping concentration of 1×10^{18} cm^{-3}.

7.3 Results

7.3.1 Doping profiles of arsenic-doped structures

Figure 7.5 shows the arsenic doping profiles measured by SIMS. It can be observed that the drain doping profiles after anneal are very different in samples with and without polysilicon drain. Figures 7.5(a) and (c) show that the arsenic doping profile in polysilicon is flat, with a concentration of approximately 2×10^{20} cm^{-3}, independent of the anneal temperature. A large peak in the arsenic concentration is observed at the polysilicon/silicon interface. Arsenic outdiffusion in the silicon substrate is observed, yielding a steep drain junction. Figures 7.5(b) and (d), on the other hand, show the profiles of structures with single-crystal silicon drain. The arsenic doping profile in these samples has the typical bell shaped dopant distribution ensuing from ion implantation.

Table 7.3 reports the channel lengths obtained from different arsenic-implanted process splits at the anneal temperatures investigated. The thickness of the deposited epitaxial layers was calibrated to obtain two short channel and two long channel structures. Process splits 1A and 2A allow an investigation of the effect of

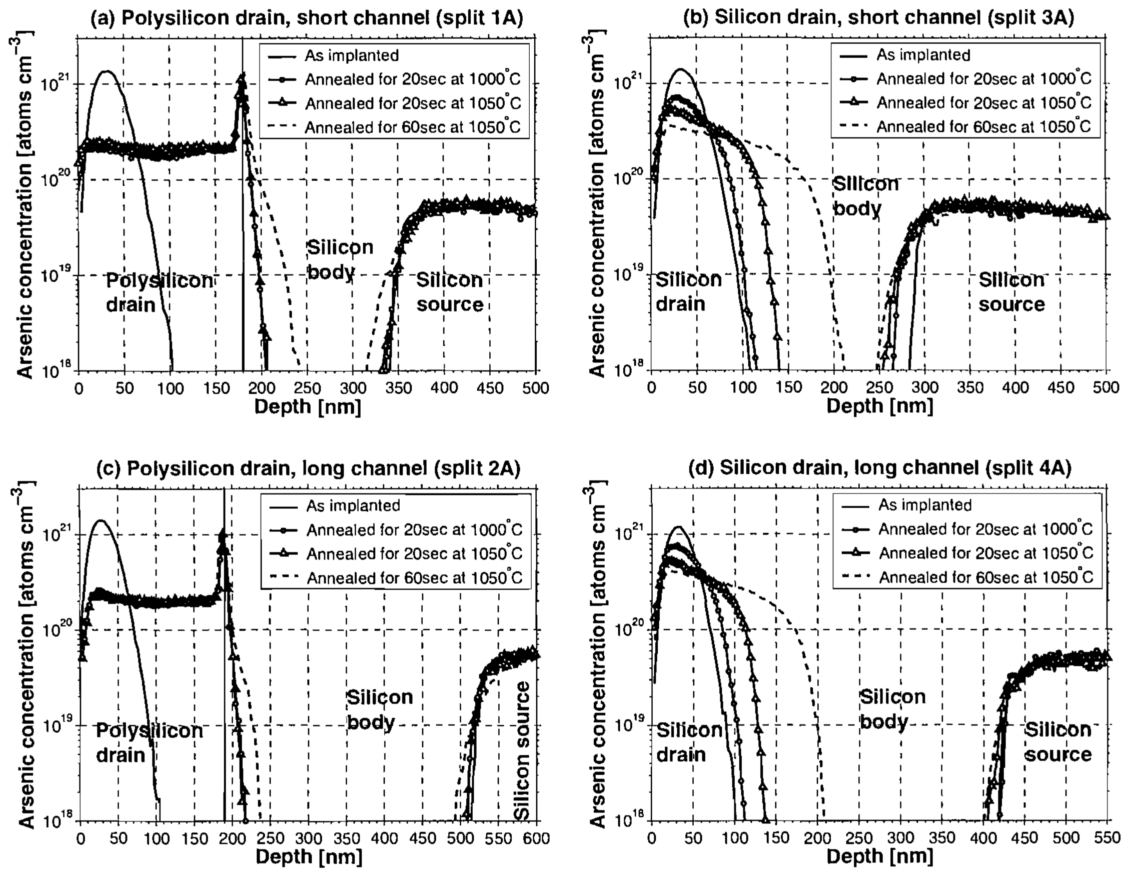

Figure 7.5: SIMS profiles of arsenic-doped test structures (see table 7.1) annealed with different thermal cycles. (a)-(c) Samples with polysilicon drain. (b)-(d) Samples with single-crystal silicon drain.

Process split	Source/drain dopant	Drain material	Channel length range [nm]
1A	Arsenic	Polysilicon	60-130
2A	Arsenic	Polysilicon	250-300
3A	Arsenic	Silicon	40-150
4A	Arsenic	Silicon	190-310

Table 7.3: Channel length range of the structures fabricated to investigate the role of a polysilicon drain on arsenic diffusion in vertical MOSFETs. The column labeled "Channel length range" reports the maximum and minimum channel length obtained with different anneals, extracted at an arsenic doping concentration of 10^{18} cm^{-3}.

a polysilicon drain on arsenic diffusion in short and long channel vertical MOSFETs respectively. On the other hand, process splits 3A and 4A allow a comparison of these results with single-crystal silicon drains.

7.3.2 Boron-doped samples

The doping profiles of the boron-doped test structures are shown in figure 7.6. Figure 7.6(a) shows that the boron doping profile in polysilicon after anneal is flat, with a doping concentration of approximately 9×10^{19} cm^{-3}. The doping concentration in the polysilicon is independent of the anneal conditions. No peak is observed in the boron concentration at the polysilicon/silicon interface. The boron outdiffuses into the single-crystal silicon body yielding steep drain junctions. The doping profiles of devices with a single-crystal silicon drain are shown in figure 7.6(b). It can be observed that these junctions are less steep than those outdiffused from a polysilicon drain, shown in figure 7.6(a).

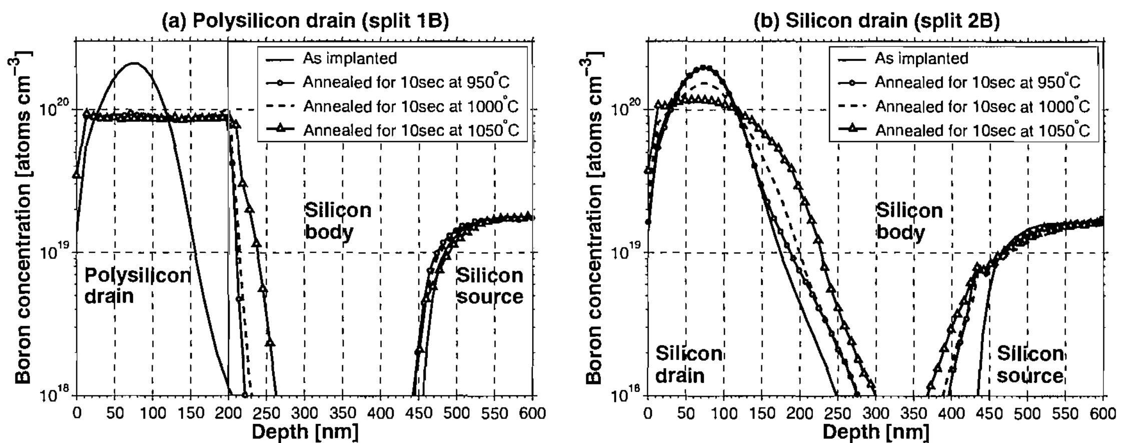

Figure 7.6: SIMS profiles of boron-doped test structures (see table 7.2) annealed with different thermal cycles. (a) Structures with polysilicon drain. (b) Structures with single-crystal silicon drain.

7.4 Discussion

The arsenic-doped structures were fabricated to investigate the role of a polysilicon drain on dopant diffusion in n-channel vertical MOSFETs. Steep outdiffusions less than 30 nm deep (at a reference doping concentration of 1×10^{18}cm^{-3}) were obtained from polysilicon drains for anneals at 1000°C and 1050°C. The diffusion of arsenic in polysilicon occurs in two stages. In the first few seconds of the anneal, the arsenic diffuses rapidly down the grain boundaries to the polysilicon/silicon interface, yielding an approximately flat doping profile in polysilicon. In fact, the grain boundary diffusion coefficient in polysilicon is several orders of magnitude higher than that in bulk silicon. The arsenic segregates at the grain boundaries and the center of the grains is left undoped. The large arsenic concentration peak observed at the polysilicon/silicon interface is caused by segregated arsenic at the pseudo-grain boundary

between the polysilicon drain and the silicon body [103]. In the remainder of the activation anneal, the arsenic diffuses from the grain boundaries into the bulk of the grains and from the polysilicon/silicon interface into the single-crystal body, yielding shallow drain outdiffusions.

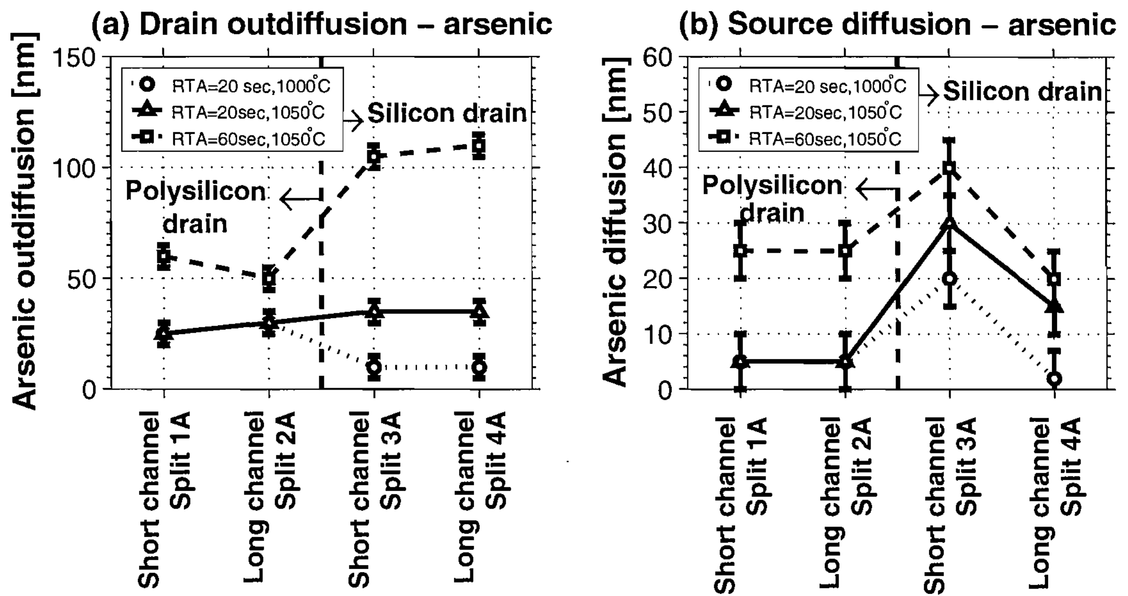

Figure 7.7: Arsenic diffusion/outdiffusion in test structures with and without polysilicon drain after different anneal cycles. (a) Arsenic diffusion/outdiffusion from the drain. (b) Arsenic diffusion from the source.

Figure 7.7(a) shows the values of drain outdiffusion/diffusion measured for different arsenic-doped process splits with and without a polysilicon drain. Short channel (process splits 1A and 3A) and long channel structures (process splits 2A and 4A) are compared in the figure. No significant dependence of the drain outdiffusion on the channel length of the structures is observed.

The source diffusion is investigated in figure 7.7(b). No dependence of the source diffusion on the channel length can be observed in structures with a polysilicon drain. However, enhanced source diffusion is observed in the short channel test structures with a silicon drain (process split 4A). This phenomenon is due to transient enhanced diffusion of the source dopants due to point defects created by the drain implant. When the impurities are implanted in a polysilicon layer, point defects arising from the ion implantation are mostly contained within the polysilicon layer and hence do not affect the diffusion of the underlying source. On the other hand, in short channel structures with a silicon drain, the point defects are injected directly into the silicon substrate, and thus enhance the source diffusion during the activation anneal. This effect is negligible in long channel structures, as the point defects are injected further from the source layer.

For the boron-doped structures, the boron profile in the polysilicon layer is flat.

This is due to the high grain boundary diffusion coefficient of boron in polysilicon, in analogy with the observation made for the arsenic-doped structures. However, no peak is observed in the boron concentration profile at the polysilicon/silicon interface. This is because boron atoms, unlike arsenic, do not segregate at the grain boundaries [106]. Once the boron atoms reach the polysilicon/silicon interface, they outdiffuse into the single-crystal silicon body, yielding steep drain junctions. Shallow drain outdiffusions 20-30 nm deep were obtained with 10 seconds anneals at 950°C and 1000°C. Moreover, figure 7.6 shows that steeper drain junctions were obtained in structures with a polysilicon drain than in those with a single-crystal silicon drain.

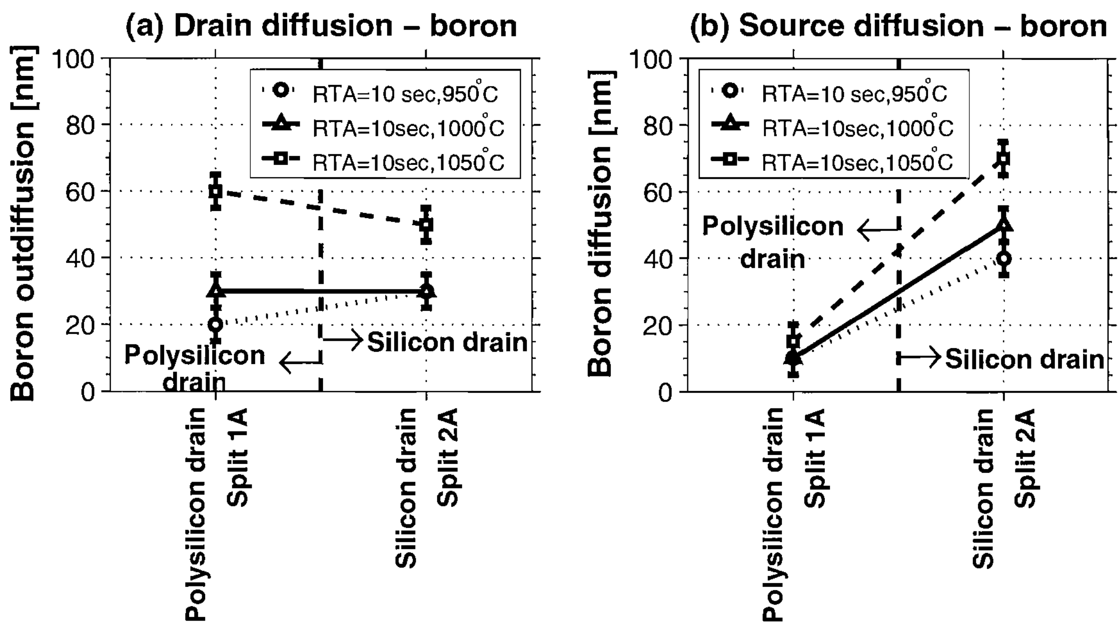

Figure 7.8: Boron diffusion/outdiffusion in test structures with and without polysilicon drain after different anneal cycles. (a) Boron diffusion/outdiffusion from the drain of the test structures. (b) Boron diffusion from the source of the test structures.

Figure 7.8(a) shows drain outdiffusion/diffusion measured on boron-doped structures with polysilicon and silicon drains. No significant difference is observed between boron outdiffusion from a polysilicon drain and boron diffusion in a single-crystal silicon drain.

The source diffusion of boron in test structures with and without a polysilicon drain is analyzed in figure 7.8(b) for different anneal conditions. For each of the anneal cycles performed, the source diffusion in the test structure with a polysilicon drain is significantly less than that in the structure with a single-crystal silicon drain. In analogy with arsenic results, the enhanced boron diffusion in the single-crystal silicon drain can be explained by transient enhanced diffusion of the source dopant due to point defects created by the drain implant. When the boron atoms are implanted into a polysilicon drain, point defects arising from the ion implantation are mostly contained within the polysilicon layer and hence do not affect the diffusion of the

underlying source. On the other hand, during ion implantation of boron in single-crystal silicon, point defects are created in the silicon body. These defects enhance the diffusion of boron atoms in the single-crystal silicon source.

The greater amount of source diffusion seen for boron than arsenic in structures with a single-crystal silicon drain arises because the diffusion coefficient of boron is larger than that of arsenic. Furthermore, boron is more susceptible to transient enhanced diffusion than arsenic, because its diffusion is mediated predominantly by self-interstitials [107]. This explains the enhanced boron source diffusion in structures with silicon drain compared with structures with polysilicon drain, as observed in figure 7.8(b).

7.5 Summary

In this chapter the diffusion of dopants in vertical MOSFETs with polysilicon drains has been investigated and compared with diffusion in conventional ion implanted silicon drains. Boron and arsenic diffusion has been quantified for different anneal conditions. Arsenic implanted test structures with a polysilicon drain are found to yield shallow outdiffusions less than 30 nm deep for anneals at 1000°C and 1050°C for 20 seconds. Boron-doped test structures are found to yield junctions less than 30 nm deep for anneals at 950°C and 1000°C for 10 seconds. These annealing conditions are suitable for the fabrication of dielectric pocket vertical MOSFETs with shallow drain junctions.

The role of a polysilicon drain on the diffusion of the underlying source has also been assessed. In samples with a single-crystal silicon drain, considerable diffusion of the underlying source is observed after anneal. On the other hand, in the presence of a polysilicon drain very little source diffusion is observed. The phenomenon is more evident in boron-doped than in arsenic-doped test structures. The enhanced source diffusion is due to the creation of point defects during drain ion implantation into the single-crystal silicon body, which enhances the diffusion of dopants in the source. In contrast, when the drain dopants are implanted into polysilicon, the point defects are retained in the polysilicon layer and have less effect on the diffusion of the underlying source. Thus the presence of a polysilicon drain is found to be effective in reducing source diffusion and hence facilitates the creation of n- and p-channel dielectric pocket vertical MOSFETs with very short channel lengths.

Chapter 8

Conclusions

In this thesis two technological solutions have been investigated for reducing parasitics in CMOS compatible vertical MOSFETs. First, a fully CMOS compatible, self-aligned second oxidation process, called spacer or fillet local oxidation (FILOX), has been characterized, which reduces the gate overlap capacitance in vertical MOSFETs. Second, a novel dielectric pocket process has been proposed and vertical MOSFETs fabricated. This process allows shallow drain junctions to be produced by incorporating a dielectric pocket between the drain and body. Although dielectric pocket and FILOX devices were fabricated in two separate experiments, the two processes are fully compatible and can be integrated to provide vertical MOSFETs with both shallow drain junctions and reduced overlap capacitance.

Single, double and surround gate vertical nMOSFETs with reduced gate overlap capacitance have been fabricated with the FILOX process. In these devices, a 40 nm thick FILOX oxide covers the horizontal silicon area, while the vertical sidewalls of the active pillar only contain the 3.3 nm thick gate oxide. The extra oxide in the trench and on top of the pillar reduces the parasitic capacitance by a factor approximately equal to the ratio of the gate oxide and the FILOX oxide. The fabrication process is epitaxy free and CMOS compatible. A quantitative comparison has shown that the gate/drain overlap capacitance of a FILOX vertical MOSFET is 1.4 times lower and the gate/source overlap capacitance 1.2 times lower than that of a lateral MOSFET. Single, double and surround gate transistors have been successfully fabricated and characterized. FILOX vertical MOSFETs with 125 nm channel length display drive currents up to 100 $\mu A/\mu m$, off-state drain leakage currents of the order of 10^{-11} $A/\mu m$, subthreshold slopes down to 103 mV/dec and 50 mV DIBL. The threshold voltage roll-off of surround gate vertical MOSFETs with channel lengths ranging between 90 nm and 140 nm has been investigated. The results show that the FILOX process must be carefully tuned in order to avoid short channel effects due to gate oxide thickness nonuniformity along the channel.

The transfer characteristics of surround gate FILOX vertical MOSFETs in the

drain on top and drain on bottom configurations are symmetric in the on-state. However, the off-state drain leakage currents are asymmetric when the source and the drain are interchanged, with gate induced drain leakage (GIDL) being higher in the drain on bottom configuration and body leakage being higher in the drain on top configuration. The asymmetric body leakage arises from a slightly larger body doping concentration on the top of the pillar than on the bottom. On the other hand, the asymmetric gate induced drain leakage is due to a thicker gate oxide on the vertical <110> pillar sidewall than on the horizontal <100> wafer surface.

Surround gate vertical nMOSFETs with a shallow drain junction and a dielectric pocket have been fabricated using a novel polysilicon spacer process. The key feature of this process is the deposition of a polysilicon spacer around the perimeter of the active pillar to connect the polysilicon drain contact on the top of the pillar to the channel of the transistor. The novel process is fully compatible with a conventional planar CMOS technology, and does not require epitaxial growth. Short-channel MOSFETs can be fabricated without challenging photolithography, so that sub-100 nm vertical MOSFETs can be integrated in a mature CMOS technology with relaxed lithography rules. As a result, the novel process is a high throughput and low cost solution for the fabrication of CMOS compatible vertical MOSFETs.

Dielectric pocket vertical nMOSFETs with channel length down to 70 nm have been structurally and electrically characterized. The polysilicon drain is connected to the channel by a polysilicon spacer with a minimum thickness of about 20 nm. The drain dopants outdiffuse into the single-crystal silicon body, yielding a drain junction depth into the pillar sidewall of less than 50 nm. Moreover the dielectric pocket screens the drain and the body of the device, contributing to suppressed short channel effects. The fabricated devices show good electrical characteristics, with a subthreshold slope of 92 mV, an off-state drain current of 5×10^{-12} A/μm and a threshold voltage of 0.9 V. On the other hand, the devices have a low on-state drain current of 18 μA/μm and asymmetric transfer characteristics when the source and the drain are interchanged. This is caused by parasitic drain series resistance due to the presence of native oxide layers at the two interfaces between the polysilicon drain, the polysilicon spacer and the single-crystal silicon substrate. The parasitic interfaces can be removed by introducing minor process modifications, such as depositing the polysilicon spacer layer in a cluster tool after an in-situ surface clean or using a high dose silicon ion implantation with a large tilt angle to break up the native oxide layers after spacer deposition.

The suitability of polysilicon drains for the fabrication of short-channel vertical MOSFETs has been investigated. By optimizing the thermal budget of the RTA anneal, both boron-doped and arsenic-doped drain layers are found to yield outdiffusions in the single-crystal silicon substrate of less than 30 nm. Furthermore, the presence of a polysilicon drain is found to be effective in reducing transient enhanced

diffusion in the underlying source. The polysilicon drain therefore facilitates channel length scaling to smaller dimensions.

Chapter 9

Suggestions for future work

From the material presented in this thesis, there are a number of areas where work might be carried out in the near future. These are summarized below.

- On both FILOX and dielectric pocket vertical MOSFETs, further measurements on the fabricated logic gates could be carried out and their potential for high speed applications could be investigated. Moreover, the functional ring oscillators could be measured and compared with simulated results. RF measurements to extract the maximum oscillation frequency and the cutoff frequency of the devices could be performed since special probe pads are included in the layout for this purpose.

- The first dielectric pocket vertical MOSFETs fabricated with the novel polysilicon spacer process suffer from low on-state drain current. This is due to parasitic drain series resistance induced by two native oxide layers at the two interfaces between the polysilicon spacer, the polysilicon drain and the single-crystal silicon substrate. In order to improve the performance of the devices, a modified fabrication process could be implemented. One possibility would be to remove the parasitic oxide layers with an in-situ surface clean before depositing the spacer layer in a cluster tool. Alternatively, the native oxide layer could be broken up after spacer deposition with a high dose silicon ion implantation with a large tilt angle.

- The dielectric pocket vertical MOSFETs fabricated have a high channel doping concentration of about 2×10^{18} cm^{-3}. Devices with lower channel doping, to achieve threshold voltage values compatible with the state of the art CMOS technology, could be fabricated. Moreover, this would allow the carrier mobility to be boosted in the channel of the devices.

In the longer term, further work could be carried out to advance the state of the art of CMOS compatible vertical MOSFETs. A few suggestions are summarized below.

- The FILOX process and the dielectric pocket process could be integrated to fabricate CMOS compatible vertical MOSFETs with shallow drain junctions and reduced gate overlap capacitance.

- Work is currently underway to fabricate vertical surround gate MOS capacitors with sub-100 nm wide pillars using the FILOX process. This work is intended to demonstrate the suitability of the FILOX process for the fabrication of thin pillar vertical MOSFETs with fully depleted channels to suppress the short channel effects.

- The suitability of vertical MOSFETs for the fabrication of high performance thin film transistors is currently being assessed. Experiments have been performed to induce the formation in amorphous silicon layers of large silicon crystals elongated in the vertical direction. A germanium-seeded crystallization process has been developed to ensure compatibility with CMOS fabrication. In the future, this process could be used to fabricate thin film, high performance vertical MOSFETs for application in the display industry.

Appendix A

Batch listings

A.1 Batch listing for fabrication of FILOX vertical MOSFETs

In this section is reported the batch listing for fabrication of FILOX vertical MOSFETs. A detailed description of the fabrication process can be found in chapter 3.

G	No	1	2	3	4	5	6	ID	Description
								k2101dt	DK - some ultracool vmos'
								r1	Front
								g1	HEADER
	1	☑						G-S12	Title Page: 12 wafers, p-type, <100>, 10-33ohm.cm + 4 check wafers of the same
	2	☑						P-EM	Reticle Writing
	3	☑						G-1P	Lithography Notes: optic litho, 1u
	4	☑						G-1	batch splits... wafer 1..3: 50nm channel length; tox = 3/6/9nm (VLOCOS) wafer 4..6: 100nm channel length; tox = 3/6/9nm (VLOCOS) wafer 7..9: 150nm channel length; tox = 3/6/9nm (VLOCOS) wafer 10..12: 150nm channel length; tox = 3/6/9nm (no VLOCOS)
	5	☑						G-1	wafer 13: test wafer to test pad oxide thickness for nitride spacers wafer 14..16: test wafer for silicon pillar etch
								com00	P-well implantation
	6	☑						W-C1	* RCA clean (WAFER 1..12) + test wafers #14-16
	7	☑						IB-5045	* Implant Boron: 5E14 B+ 50 KeV (BIPOLAR Base Implant) (WAFER 1..12,14-16)
	8	☑						W-C1	* RCA clean (WAFER 1..12,14-16)
	9	☑						F4-N10DI	* General Boron Drive-in 1100degC 10'dryO2,30'N2 (WAFER 1..12,14-16)
	10	☑						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic remove all oxide from the boron diffusion stage (WAFER 1..12,14-16)
								com1	Pillar definition and etch
	11	☑						P-GS1	* STEPPER Photolith: reticle KA14R PL Light Field: nom. 1.1um resist STANDARD
	12	☑						G-2	* See Engineer for instructions
	13	☑						P-RHBD	* Hardbake for dry etch (WAFER 1..12,14-16)
	14	☑						D-SP2S	testwafers (WAFER 14..16): Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 300nm deethis is a <si> etch not a poly etch!!!
	15	☑						G-2	* See Engineer for instructions
	16	☑						D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 250nm deep (WAFER 1..3) this is a <si> etch not a poly etch!!!
	17		☑					D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 300nm deep (WAFER 4..6) this is a <si> etch not a poly etch!!!
	18			☑				D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 350nm deep (WAFER 7..9) this is a <si> etch not a poly etch!!!
	19				☑			D-SP2S	Etch Poly/AmSi. Anisot. SYS90 HBr 2 step. (For LF patterns) ETCH 350nm deep (WAFER 10..12) this is a <si> etch not a poly etch!!!
	20	☑						P-RS	* Resist strip (WAFER 1..12)
								com1a	Active area definition
	21	☑						W-C1	* RCA clean (WAFER 1..12,13,14)
	22	☑						F5-9002P	* Pad oxidation: 900degC, 20nm+-5nm, O2 + HCl (WAFER 1..12) and check wafer 13,14 !!!
	23	☑						LN-130	* Deposit Si3N4 130nm+-20nm @ 740degC DCS:NH4 1:4, 2.3nm/m. (WAFER 1..12,14)
	24	☑						P-GS1	* STEPPER Photolith: reticle KA14R AA Light Field: nom. 1.1um resist STANDARD Wafers 1-12,14
	25	☑						G-2	* See Engineer for instructions
	26	☑						P-RHBD	* Hardbake for dry etch (WAFER 1..12,14)
	27	☑						D-NO1E	Etch Si3N4+PadSiO2. Anisot. L/F EBMF/OPTICAL resist OPT80+CHF3+Ar (WAFER 1..12,14)
	28	☑						P-RS	* Resist strip (WAFER 1..12,14)
	29	☑						W-C1	* RCA clean (WAFER 1..12,14)
	30	☑						F6-W0060	* Hydrox oxidation: 1000degC, 600nm+-20nm, H2 + O2 (WAFER 1..12,14)
								com3b	FILOX process
	31	☑						WH-2D2	Dip etch, 20:1 BHF 25degC. 30 seconds to remove any oxide on nitride (WAFER 1..12,14)
	32	☑						D-0	Dry Etch Si3N4 + pad oxide OPT80+CHF3+Ar TO LEAVE SIDEWALL SPACERS (WAFER 1..12,14) 5-10% overetch
	33	☑						D-D60	* Descum: 3 min. SRS barrel O2 (WAFER 1..12,14)
	34	☑						W-C1	* RCA clean (WAFER 1..12,14)
	35	☑						F6-0	* Furnace 6: Load in N2: 60nm @ 1000degC wafers #1-9,14
	36		☑					W-C2	* Fuming Nitric acid clean, 2nd pot only wafers #10-12

G	No	1	2	3	4	5	6	ID	Description
								com3c	Body contact implantation
	37	☑						P-GS1	* STEPPER Photolith: reticle KA14R, PP Dark Field: nom. 1.1um resist STANDARD (WAFER 1..12)
	38	☑						G-2	* See Engineer for instructions
	39	☑						P-RHBI	* Hardbake for implant (WAFER 1..12)
	40	☑						IB-0	* Implant B+: 1E15 47keV (WAFER 1..9)
	41		☑					IB-0	* Implant B+: 1E15 25keV (WAFER 10..12)
	42	☑						P-RS	* Resist strip (WAFER 1..12)
	43	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER 1..12)
								com3dd	Source and drain ion implantation for Gate After Implant MOSFETs
	44	☑						P-GS1	* STEPPER Photolith: reticle KA14R, NGA Dark Field: nom. 1.1um resist STANDARD (WAFER 1..12)
	45	☑						G-2	* See Engineer for instructions
	46	☑						P-RHBI	* Hardbake for implant (WAFER 1..12)
	47	☑						IA-0	* Implant As+: 3e15 120keV implant direction: west (WAFER 1..9)
	48	☑						IA-0	* Implant As+: 3e15 120keV impant direction: east (WAFER 1..9)
	49		☑					IA-0	* Implant As+: 3e15 50keV implant direction: west (WAFER 10..12)
	50		☑					IA-0	* Implant As+: 3e15 50keV impant direction: east (WAFER 10..12)
	51	☑						P-RS	* Resist strip (WAFER 1..12)
	52	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER 1..12)
								com3	Nitride fillets and stress relief oxide removal
	53	☑						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> to remove any access oxide on the nitride (WAFER 1..12) max 5 sec
	54	☑						WN-1	+ Strip/Wet etch Si3N4, Orthophosphoric acid 160degC this is to remove the fillets and the nitride on top of the pillar (WAFER 1..12)
								com4aa	Gate stack deposition
	55	☑						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> about 40sec for 20nm stress relief oxide... (WAFER 1,4,7,10) + check wafer 13!!!!!!!!!!!!!!!!!!!!!!!!!!!!!!
	56	☑						W-C1	* RCA clean (WAFER 1,4,7,10 + check 13)
	57	☑						F12-G0	* Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl) 3nm SiO2 on Si, O2 (WAFER 1, 4, 7, 10 + check13) at 800degC BEST EFFORT !!!
	58	☑						LE-0	Low Pressure Epitaxy -> deposit 200nm poly 5e19 at 650..670degC (WAFERS 1,4,7,10) and check wafer13!!!
	59		☑					WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> about 40sec for 20nm stress relief oxide... (WAFER 2,5,8,11)
	60		☑					W-C1	* RCA clean (WAFER2,5,8,11)
	61		☑					F12-G0	* Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl) 6nm SiO2 on Si, O2 (WAFER 2,5,8,11) at 800degC BEST EFFORT !!!
	62		☑					LE-0	Low Pressure Epitaxy -> deposit 200nm poly 5e19 at 650..670degC (WAFERS 2,5,8,11)
	63			☑				WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic --> about 40sec for 20nm stress relief oxide... (WAFER 3,6,9,12)
	64			☑				W-C1	* RCA clean (WAFER3,6,9,12)
	65			☑				F12-G0	* Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl) 9nm SiO2 on Si, O2 (WAFER 3,6,9,12) at 800degC BEST EFFORT !!!
	66			☑				LE-0	Low Pressure Epitaxy -> deposit 200nm poly 5e19 at 650..670degC (WAFERS 3,6,9,12)
								com4aaa	Polysilicon spacers etch
	67	☑						P-GS1	* STEPPER Photolith: reticle KA14R, P1 Light Field: nom. 1.1um resist STANDARD
	68	☑						G-2	* See Engineer: INSPECT

G	No	1	2	3	4	5	6	ID	Description
	69	☑						P-RHBD	* Hardbake for dry etch
	70	☑						D-SP2V	Etch Poly/AmSi. Anisot. on THIN gate ox, <15nm SYS90 HBr 3 step. (For LF patterns) WAFER1..12 Use ICP etcher ***** leave poly fillets - stop on 2nm oxide*****
	71	☑						P-RS	* Resist strip (WAFER 1..12)
	72	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only
								com0	Source and drain ion implantation for Gate Before Implant MOSFETs
	73	☑						P-GS1	* STEPPER Photolith: reticle KA14R, NGB Dark Field: nom. 1.1um resist STANDARD (WAFER1..12)
	74	☑						G-2	* See Engineer: INSPECT
	75	☑						P-RHBI	* Hardbake for implant (WAFER1..12) please, please, please, hardbake the wafers foor 2h !!!!
	76	☑						IA-0	* Implant As+: 3e15 90keV implant direction: west (WAFER1..9)
	77	☑						IA-0	* Implant As+: 3e15 90keV implant direction: east (WAFER1..9)
	78		☑					IA-0	* Implant As+: 3e15 50keV implant direction: west (WAFER10..12)
	79		☑					IA-0	* Implant As+: 3e15 50keV implant direction: east (WAFER10..12)
	80	☑						P-RS	* Resist strip (WAFER1..12)
	81	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only (WAFER1..12)
								comu	Polysilicon spacers removal for single/double gate MOSFETs
	82	☑						P-GS1	* STEPPER Photolith: reticle KA14R, PR Light Field: nom. 1.1um resist STANDARD
	83	☑						G-2	* See Engineer for instructions See Tony about next dry etch stage
	84	☑						P-RHBD	* Hardbake for dry etch
	85	☑						D-0	Dry etch: Use isotropic SF6 polySi etch in the OPT80+ To remove 200nm polysilicon fillets. No visible end point *****See engineer for nonstandard process - best effort***** please remember to stop in the thin gate oxide if possible
	86	☑						P-RS	* Resist strip
								backend	Back end - passivation
	87	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only
	88	☑						LS-BO1	BPSG: Deposit 100nm undoped Silox + 500nm BPSG (4%P/"10%"B approx)
	89	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only
	90	☑						RA-1	RTA implant activation 10secs 1100degC (Std.CMOS S D) - this is for annealing and reflow
	91	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only
	92	☑						P-GS1	* STEPPER Photolith: reticle KA14R,CW Dark Field: nom. 1.1um resist STANDARD
	93	☑						G-2	* See Engineer for instructions
	94	☑						P-RHBD	* Hardbake for dry etch (WAFER1..12)
	95	☑						D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar
	96	☑						P-RS	* Resist strip (WAFER 1..12)
	97	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only
								metaldepo	Back end - metal
	98	☑						WH-2D2	Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation)
	99	☑						MS-TA10	Sputter 1000nm Ti-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED
	100	☑						P-GS2	* STEPPER Photolith: reticle KA14r; M1,Light Field: nom. 2.2um resist (For Si etch>1um or metal)
	101	☑						G-2	* See Engineer for instructions
	102	☑						P-RHBD	* Hardbake for dry etch
	103	☑						X-0	General inspection stage
								metaletch	Back end - metal etch
	104	☑						D-MAT1	+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar (WHOLE 4" wfrs) WAFERS #1,4
	105		☑					P-RS	* Resist strip
	106		☑					MS-0	Add ARC to wafers #2,3,5-10,12
	107		☑					P-GS2	* STEPPER Photolith: reticle KA14r; M1,Light Field: nom. 2.2um resist (For Si etch>1um or metal)
	108		☑					G-2	* See Engineer for instructions
	109		☑					P-RHBD	* Hardbake for dry etch
	110		☑					D-MAT1	+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar (WHOLE 4" wfrs)
	111	☑						X-0	General inspection stage CHECK DENSITY OF Si GRAINYNESS
	112	☑						P-RS	* Resist strip
	113	☑						W-C3	* Fuming Nitric Acid clean, metallised wafers
	114	☑						F9-H42	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.

A.2 Batch listing for fabrication of dielectric pocket vertical MOSFETs

In this section is reported the batch listing for fabrication of dielectric pocket vertical MOSFETs. A detailed description of the fabrication process can be found in chapter 5.

G	No	1	2	3	4	5	6	ID	Description
								k2732s	EG - Vertical MOSFET with new dielectric pocket process
								r1	
								g0	
	1	☑						P-EM	E-BEAM Mask/Reticle Writing
	2	☑						G-S12	Title Page: 18 wafers, MATERIAL: p-type, <100>, 10-33 ohm.cm
	3	☑						G-1P	Lithography Notes: optic lithography ***SOME CRITICAL ALIGNMENTS - USE DEFAS ON G2***
	4	☑						G-1	Splits: wafers 1-12 = devices; wafer C1-C6 = pillar dry etch process development
								pwell	################p-well ion implantation
	5	☑						W-C1	* RCA clean; wafers 1-12 and C1-2
	6	☑						F5-9002P	* Pad oxidation: 900degC, 20nm+-5nm, O2 + HCl; wafers 1-12 and C1-2
	7	☑						IB-5045	* Implant Boron: 5E14 B+ 50 KeV (BIPOLAR Base Implant); wafers 1-12 and C1-2
	8	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-12 and C1-2
	9	☑						W-C1	* RCA clean; wafers 1-12 and C1-2
	10	☑						F4-N10DI	* General Boron Drive-in; 1100degC; 10'dryO2,30'N2; wafers 1-12 and C1-2
	11	☑						WH-2D6	Dip etch, 20:1 BHF 25degC. For specified time to remove 20nm pad oxide + oxide grown during anneal; wafers 1-12 and C1-2
								com2	################Active area definition
	12	☑						W-C1	* RCA clean; wafers 1-12 and C1-2
	13	☑						F5-9002P	* Pad oxidation: 900degC, 20nm+-5nm, O2 + HCl; wafers 1-12 and C1-2
	14	☑						LN-130	* Deposit Si3N4 130nm+-20nm @ 740degC; DCS:NH4 1:4, 2.3nm/m.; wafers 1-12 and C1-2
	15	☑						P-GS1	* STEPPER Photolith: reticle KA14R AA, Light Field: nom. 1.1um resist STANDARD; wafers 1-12 and C1-2
	16	☑						P-RHBD	* Hardbake for dry etch; wafers 1-12 and C1-2
	17	☑						D-N1E	Etch Si3N4. Anisot. L/F EBMF/OPTICAL resist OPT80+ CHF3+Ar; wafers 1-12 and C1-2
	18	☑						P-RS	* Resist strip; wafers 1-12 and C1-2
	19	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-12 and C1-2
	20	☑						W-C1	* RCA clean; wafers 1-12 and C1-2
	21	☑						F6-W0060	* Hydrox oxidation: 1000degC, 600nm+-20nm, H2 + O2; wafers 1-12 and C1-2
	22	☑						WH-2D2	Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metallisation) Used to remove SiO2 on Si3N4; wafers 1-12 and C1-2
	23	☑						WN-1	* Strip/Wet etch Si3N4, Orthophosphoric acid 160degC; wafers 1-12 and C1-2
	24	☑						WH-2D6	Dip etch, 20:1 BHF 25degC. For specified time to remove 20nm pad oxide; wafers 1-12 and C1-2
								com3a	################Drain and dielectric pocket deposition
	25	☑						W-C1	* RCA clean; wafers 1-12 and C1-3
	26	☑						F12-G0	* Gate oxidation 2: Temp = 800degC, thickness 10nm, O2 (+ HCl); wafers 2 + 4
	27		☑					F5-9002P	* Pad oxidation: 900degC, 20nm+-5nm, O2 + HCl; wafers 1,3,5-7,12,C1-C6
	28			☑				WH-2D5	Dip etch, 20:1 BHF 25degC. For specified time to remove native oxide; PERFORM JUST BEFORE a-Si DEPOSITION; wafers 8-11
	29	☑						LPV-0	* Blank sheet for LPCVD Amorphous Si; in KOYO vertical furnace; deposit 300nm undoped Amorphous Si; wafers 1-12 and C1-3
	30		☑					IA-8055	* Implant Arsenic: 5E15 As+ 80KeV (C/NMOS Source and Drain); wafers 1-6,8,10-12 and C1-2
	31	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-12 and C1-3
	32	☑						W-C1	* RCA clean; wafers 1-12 and C1-3
	33	☑						LO-0	* Blank sheet for LPCVD LTO; deposit 250nm LTO; wafers 1-12 and C1-3
								com4	################Drain and dielectric pocket dry etch
	34	☑						P-GS1	* STEPPER Photolith: reticle KA14R PL, Light Field: nom. 1.1um resist STANDARD; wafers 1-12, C1-3
	35	☑						G-2	* Alignment check; wafers 1-12, C1-3
	36	☑						P-RHBD	* Hardbake for dry etch; wafers 1-12, C1-3
	37	☑						D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar Etch 250nm SiO2; possible overetch on a-Si; wafers 1-12, C1-3
	38	☑						P-RS	* Resist strip; wafers 1-12, C1-3
	39	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-12, C1-3
	40		☑					D-0	Etch 300nm a-Si down to 20nm oxide layer; Anisotropic; use process 3STEPEXP first 2 steps only Wafers 1,3,5-7,12,C1-6

G	No	1	2	3	4	5	6	ID	Description
	41							D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar; etch 20nm oxide; 90 seconds; wafers 1,3,5-7,12,C1-6
	42							D-0	Etch 300nm a-Si down to 10nm oxide layer; Anisotropic; use process 3STEPEXP first 2 steps only Wafers 2,4
	43							D-O1E	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar; etch 10nm oxide; 60 seconds; wafers 2,4
								proctr34	################Process development for trench Silicon dry etch - wafers C3-C4
	44							W-C1	* RCA clean; wafers C3-4
	45							WH-0	* Wet etch oxide, 100:1 HF 25degC; etch 5-10nm oxide in order to remove native oxide; calibrate etch time with check wafer from dielectric pocket growth; PERFORM JUST BEFORE a-Si DEPOSITION; wafer C3-4
	46							LPV-0	* Blank sheet for LPCVD Amorphous Si; in KOYO vertical furnace; deposit 50nm undoped Amorphous Si; wafers C3-4
	47							P-GS1	* STEPPER Photolith: reticle KA14R, nom. 1.1um resist STANDARD; deposit 4 resist patches on 4 cells scattered throughout the wafers; wafers C3-4
	48							P-RHBD	* Hardbake for dry etch; wafers C3-4
	49							D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 50nm Amorphous Si (etch stop = LOCOS) + 150nm Si; wafers C3-4
	50							G-2	* SEM inspection: check effect of dielectric pocket wet etch and a-Si uniformity on covered cells; check effect of RCA and HF dip before gate oxidation; wafers C3-4
								proctr56	################Process development for trench Silicon dry etch - wafers C5-C6
	51							W-C1	* RCA clean; wafers C5-6
	52							WH-0	* Wet etch oxide, 100:1 HF 25degC; etch 5-10nm oxide in order to remove native oxide; calibrate etch time with check wafer from dielectric pocket growth; PERFORM JUST BEFORE a-Si DEPOSITION; wafer C5-6
	53							LPV-0	* Blank sheet for LPCVD Amorphous Si; in KOYO vertical furnace; deposit 50nm undoped Amorphous Si; wafers C5-6
	54							P-GS1	* STEPPER Photolith: reticle KA14R, nom. 1.1um resist STANDARD; deposit 4 resist patches on 4 cells scattered throughout the wafers; wafers C5-6
	55							P-RHBD	* Hardbake for dry etch; wafers C5-6
	56							D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 50nm Amorphous Si (etch stop = LOCOS) + 150nm Si; wafers C5-6
	57							G-2	* SEM inspection: check effect of dielectric pocket wet etch and a-Si uniformity on covered cells; check effect of RCA and HF dip before gate oxidation; wafers C5-6
								proctrench	################Process development for trench Silicon dry etch - wafers C1-C2
	58							W-C1	* RCA clean; wafers C1-2
	59							WH-0	* Wet etch oxide, 100:1 HF 25degC; etch 5-10nm oxide in order to remove native oxide; calibrate etch time with check wafer from dielectric pocket growth; PERFORM JUST BEFORE a-Si DEPOSITION; wafer C1-2
	60							LPV-0	* Blank sheet for LPCVD Amorphous Si; in KOYO vertical furnace; deposit 50nm undoped Amorphous Si; wafers C1-2
	61							P-GS1	* STEPPER Photolith: reticle KA14R, nom. 1.1um resist STANDARD; deposit 4 resist patches on 4 cells scattered throughout the wafers; wafers C1-2
	62							P-RHBD	* Hardbake for dry etch; wafers C1-2
	63							D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 50nm Amorphous Si (etch stop = LOCOS) + 150nm Si; wafer C1
	64							D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 50nm Amorphous Si (etch stop = LOCOS) + 50nm Si; wafer C2
	65							G-2	* SEM inspection: check effect of dielectric pocket wet etch and a-Si uniformity on covered cells; check effect of RCA and HF dip before gate oxidation; wafers C1-2
								trench	################Trench Silicon dry etch
	66							W-C1	* RCA clean; wafers 1-12
	67							WH-0	* Wet etch oxide, 100:1 HF 25degC; etch 5-10nm oxide in order to remove native oxide; calibrate etch time with check wafer from dielectric pocket growth; PERFORM JUST BEFORE a-Si DEPOSITION; wafers 3,4,6
	68							LPV-0	* Blank sheet for LPCVD Amorphous Si; in KOYO vertical furnace; deposit 30nm undoped Amorphous Si; wafers 3,4,6
	69							WH-0	* Wet etch oxide, 100:1 HF 25degC; etch 5-10nm oxide in order to remove native oxide; calibrate etch time with check wafer from dielectric pocket growth; PERFORM JUST BEFORE a-Si DEPOSITION; wafers 1,2,5,7,10,12
	70							LPV-0	* Blank sheet for LPCVD Amorphous Si; in KOYO vertical furnace; deposit 50nm undoped Amorphous Si; wafers 1,2,5,7,10,12
									***********Devices with dielectric pocket***********

G	No	1	2	3	4	5	6	ID	Description
	71	☑						D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 30nm Amorphous Si (etch stop = LOCOS) + 50nm Si; wafer 6
	72		☑					D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 50nm Amorphous Si (etch stop = LOCOS) + 50nm Si; wafer 5
	73			☑				D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 30nm Amorphous Si (etch stop = LOCOS) + 150nm Si; wafers 3,4
	74				☑			D-0	Trench etch Si; Anisotropic; HBr process TROXMASK without initiation; Use ICP etcher; Etch 50nm Amorphous Si (etch stop = LOCOS) + 150nm Si; wafers 1,2,7,12
									***********Devices without dielectric pocket***********
	75					☑		D-0	Trench etch Si; Anisotropic; HBr process TROXMASK normal; Use ICP etcher; Etch 300nm Amorphous Si (etch stop = LOCOS) + 150nm Si; wafers 8-10
	76						☑	D-0	Trench etch Si; Anisotropic; HBr process TROXMASK normal; Use ICP etcher; Etch 300nm Amorphous Si (etch stop = LOCOS) + 50nm Si; wafer 11
								sacrox	################Sacrificial oxidation and LTO removal
	77		☑					W-C1	* RCA clean; wafers 7+9
	78		☑					F14-0	Furnace 14 - KOYO VERTICAL FURNACE (OXIDATION); tox=6nm @ 800degC; wafers 7+9
	79		☑					WH-0	* Wet etch oxide, 20:1 BHF 25degC; etch LTO layer and sacrificial oxide layer; calibrate etch time with check wafer from LTO deposition; wafers 7+9
								gal	Gate After Implant ion implantation
	80	☑						W-C1	* RCA clean; wafers 1-9 and 11-12
	81	☑						LO-0	* LPCVD LTO; deposit 50nm LTO oxide; wafers 1-9 and 11-12
	82	☑						P-GS1	* STEPPER Photolith: reticle KA14R NGA, Dark Field: nom. 1.1um resist STANDARD; wafers 1-9 and 11-12
	83	☑						G-2	* Alignment check; ATTENTION: necessary 1µm structures definition; wafers 1-9 and 11-12
	84	☑						P-RHBI	* Hardbake for implant; wafers 1-9 and 11-12
	85	☑						IA-0	* Implant As+; 8e15, 70keV; tilt 0 degrees; wafers 1-9 and 11-12
	86	☑						P-RS	* Resist strip; wafers 1-9 and 11-12
	87	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
	88		☑					WH-0	* Wet etch oxide, 20:1 BHF 25degC; etch 50nm LTO layer; calibrate etch time with check wafer from LTO deposition; wafers 7+9
	89		☑					WH-0	* Wet etch oxide, 20:1 BHF 25degC; etch 50nm LTO layer and LTO hard mask; calibrate etch time with check wafer from LTO deposition; wafers 1-6, 8 and 11-12
	90	☑						G-2	* Measure pillar height at profilometer; wafers 1-9 and 11-12
								com7	################Gate oxidation
	91	☑						W-C1	* RCA clean; wafers 1-9 and 11-12
	92	☑						WH-0	Dip etch in HF 1:100 to remove native oxide; proceed this and the next three steps in the same day; wafers 1-9 and 11-12
	93	☑						F14-0	Furnace 14 - KOYO VERTICAL FURNACE (OXIDATION); tox=3nm grown at 800degC; wafers 1-9 and 11-12
	94	☑						LPV-A10	*Amorphous Si Deposition:100nm+-10nm @ 560degC 1.7nm/min; wafers 1-9 and 11-12
	95	☑						IP-0	* Implant PHOS; 1e15, 20keV; tilt=45 deg; implant direction: north; wafers 1-9 and 11-12
	96	☑						IP-0	* Implant PHOS; 1e15, 20keV; tilt=45 deg; implant direction: south; wafers 1-9 and 11-12
	97	☑						IP-0	* Implant PHOS; 1e15, 20keV; tilt=45 deg; implant direction: east; wafers 1-9 and 11-12
	98	☑						IP-0	* Implant PHOS; 1e15, 20keV; tilt=45 deg; implant direction: west; wafers 1-9 and 11-12
	99	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
	100	☑						W-C1	* RCA clean; wafers 1-9 and 11-12
	101	☑						F10-0	* Furnace 10: Load in N2; 850degC for 30 min; wafers 1-9 and 11-12
								com8	################Gate patterning
	102	☑						P-GS1	* STEPPER Photolith: reticle KA14R P1, Light Field: nom. 1.1um resist STANDARD; wafers 1-9 and 11-12
	103	☑						G-2	* Alignment check; ATTENTION: necessary 1µm structures definition; wafers 1-9 and 11-12
	104	☑						P-RHBD	* Hardbake for dry etch; wafers 1-9 and 11-12

G	No	1	2	3	4	5	6	ID	Description
	105	☑						D-SP2V	Etch Poly/AmSi. Anisot. on THIN gate ox, <15nm Stop on 3nm gate oxide USE ICP POLYSs ETCHER - VERY SHORT OVER ETCH ATTENTION: LEAVE POLYSILICON FILLETS; wafers 1-9 and 11-12
	106	☑						P-RS	* Resist strip; wafers 1-9 and 11-12
	107	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
								body	################Body contact ion implantation
	108	☑						P-GS1	* STEPPER Photolith: reticle KA14R PP, Dark Field: nom. 1.1um resist STANDARD; wafers 1-9 and 11-12
	109	☑						G-2	* Alignment check; wafers 1-9 and 11-12
	110	☑						P-RHBI	* Hardbake for implant; wafers 1-9 and 11-12
	111	☑						IBF-0	* Implant BF2+: 3e15, 35keV; wafers 1-9 and 11-12
	112	☑						P-RS	* Resist strip; wafers 1-9 and 11-12
	113	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
								com9	################Source ion implantation
	114	☑						P-GS1	* STEPPER Photolith: reticle KA14R NGB, Dark Field: nom. 1.1um resist STANDARD; wafers 1-9 and 11-12
	115	☑						G-2	* Alignment check; wafers 1-9 and 11-12
	116	☑						P-RHBI	* Hardbake for implant; wafers 1-9 and 11-12
	117	☑						IA-0	* Implant As+; 2e15, 50keV; tilt=45 deg; implant direction: south; wafers 1-9 and 11-12
	118	☑						IA-0	* Implant As+; 2e15, 50keV; tilt=45 deg; implant direction: north; wafers 1-9 and 11-12
	119	☑						IA-0	* Implant As+; 2e15, 50keV; tilt=45 deg; implant direction: west; wafers 1-9 and 11-12
	120	☑						IA-0	* Implant As+; 2e15, 50keV; tilt=45 deg; implant direction: east; wafers 1-9 and 11-12
	121	☑						P-RS	* Resist strip; wafers 1-9 and 11-12
	122	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
								com11	################Back-end processing
	123	☑						LS-BO1	BPSG: Deposit 100nm undoped Silox + 500nm BPSG (4%P/"10%"B approx); wafers 1-9 and 11-12
	124	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
	125		☑					RA-0	AG RTA stage; 20sec, 1050degC; wafers 1-9 and 11; DON'T PROCESS WAFER 12
	126		☑					RA-0	AG RTA stage; 20sec, 1000degC; wafer 12
	127	☑						P-GS1	* STEPPER Photolith: reticle KA14R CW, Dark Field: nom. 1.1um resist STANDARD; wafers 1-9 and 11-12
	128	☑						G-2	* Alignment check; ATTENTION: necessary 1µm structures definition; wafers 1-9 and 11-12
	129	☑						P-RHBD	* Hardbake for dry etch; wafers 1-9 and 11-12
	130	☑						D-O1F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar; wafers 1-9 and 11-12
	131	☑						P-RS	* Resist strip; wafers 1-9 and 11-12
	132	☑						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-9 and 11-12
	133	☑						WH-0	Dip etch, ****100:1**** BHF 25degC. 30 seconds. (Pre-metalisation); wafers 1-9 and 11-12
	134	☑						MS-TNA10	Sputter 1000nm (total) Ti-TiN-Al/Si 1% + TiN ARC in TRIKON SIGMA RESIST PROHIBITED; wafers 1-9 and 11-12
	135	☑						P-GS1	* STEPPER Photolith: reticle KA14R M1 Light Field: nom. 1.1um resist STANDARD; wafers 1-9 and 11-12
	136	☑						G-2	* Alignment check; wafers 1-9 and 11-12
	137	☑						P-RHBD	* Hardbake for dry etch; wafers 1-9 and 11-12
	138	☑						D-MAT1	+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar (WHOLE 4" wfrs); NECESSARY QUITE A LOT OF OVERETCH to make sure that metal fillets due to bad BPSG flow are removed; wafers 1-9 and 11-12
	139	☑						P-RS	* Resist strip (use asher in main wet etch area); wafers 1-9 and 11-12
	140	☑						W-C3	* Fuming Nitric Acid clean, metallised wafers
	141	☑						F9-H42	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.; wafers 1-9 and 11-12

A.3 Batch listing for fabrication of test structures to assess the role of a polysilicon drain on arsenic diffusion in vertical nMOSFETs.

In this section is reported the batch listing for fabrication of test structures to assess the role of a polysilicon drain on arsenic diffusion in vertical nMOSFETs. A detailed description of the fabrication process can be found in chapter 7.

G	No	1	2	3	4	5	6	ID	Description
								k2600s	EG - Re-start (k2567s) Trial batch for epitaxial vertical MOS
								r1	
								g0	
	1	☑						P-EM	E-BEAM Mask/Reticle Writing
	2	☑						G-S12	Title Page: 6 wafers, MATERIAL: p-type, <100>, 10-33ohm.cm; all wafers with half surface oxidized from LPEPI stock for epitaxial thickness and non-selective epitaxy thickness on oxide evaluation
	3	☑						G-1P	Lithography Notes
	4	☑						G-1	Objectives of the batch: - Channel length calibration for epitaxial vertical MOS with polysilicon drain - Comparison between polysilicon drain and implanted epitaxial drain with various RTA anneals; possible observation of TED for no-poly wafers
	5	☑						G-1	- Evaluation of polysilicon deposition on thick oxide during non-selective body epitaxy for developement of a new vertical MOSFET structure
	6	☑						G-1	Wafer 2: 150nm p-Si + 200nm polySi; target L=100nm Wafer 4: 300nm p-Si + 200nm polySi; target L=250nm Wafer 5: 250nm p-Si + implantation; target L=100nm Wafer 6: 400nm p-Si + implantation; target L=250nm
								com1	Source implantation and anneal
	7	☑						W-C1	" RCA clean (wafers 1-6)
	8	☑						F5-9002P	" Pad oxidation: 900degC, 20nm+- 5nm, O2 + HCl (wafers 1-6)
	9	☑						IA-0	" Implant As+: 2E15 As+ 40 KeV (wafers 1-6)
	10	☑						W-C2	" Fuming Nitric acid clean, 2nd pot only (wafers 1-6)
	11	☑						W-C1	" RCA clean (wafers 1-6)
	12	☑						F4-0	"Furnace 4: Load in N2; 30' Dry N2 @ 1100degC (wafers 1-6)
								com3	Epitaxial layer deposition
	13	☑						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic (wafers 1-6)
	14				☑			W-C6	" Pre-epitaxy clean (wafer 6)
	15				☑			LE-0	Low Pressure Epitaxy; non-selective; deposit B, 5e17cm-3; thickness: 400nm (wafer 6); thickness value is approximate
	16	☑						W-C6	" Pre-epitaxy clean (wafer 2)
	17	☑						LE-0	Low Pressure Epitaxy; non-selective; deposit B, 5e17cm-3; thickness: 150nm (wafer 2); thickness value is approximate
	18		☑					W-C6	" Pre-epitaxy clean (wafer 4)
	19		☑					LE-0	Low Pressure Epitaxy; non-selective; deposit B, 5e17cm-3; thickness: 300nm (wafer 4); thickness value is approximate
	20			☑				W-C6	" Pre-epitaxy clean (wafer 5)
	21			☑				LE-0	Low Pressure Epitaxy; non-selective; deposit B, 5e17cm-3; thickness: 250nm (wafer 5); thickness value is approximate
	22	☑						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic (wafers 2,4)
	23	☑						W-C1	" RCA ##2## clean; PLEASE DON'T PROCEED RCA1; (wafers 2,4)
	24	☑						LP-P20	" PolySi deposition: 200nm +-10nm at 610degC SiH4 10nm/min (wafers 2,4)
								com4	Drain doping and anneals
	25	☑						IA-5054	" Implant Arsenic: 4E15 As+ 50Kev (BICMOS Poly implant) (wafers 2,4,5,6)
	26	☑						W-C2	" Fuming Nitric acid clean, 2nd pot only (wafers 2,4,5,6)
	27	☑						G-1	" At this stage cleave a part of each wafer for SIMS (doping profile before oxidation and RTA) (wafers 2,4,5,6, part 0)
	28	☑						G-1	" Cleave wafers in 2 parts: part 1 for Oxidation and RTA and part 2 for RTA without oxidation (wafers 2,4,5,5)
	29		☑					W-C1	" RCA clean (wafers 2,4,5,6, parts 1)
	30		☑					F12-G0	" Gate oxidation 2: Temp = 900degC or less, < 10nm, O2 (+ HCl); tox = 3nm, grown at 800degC (wafers 2,4,5,6, parts 1)
	31	☑						G-1	" At this stage cleave both part 1 and part 2 in 5 pieces (wafers 2,4,5,6): - Piece A for SIMS (doping profile after oxidation and RTA 1000degC 30sec) - Piece B for SIMS (doping profile after oxidation and RTA 1025degC 30sec)
	32	☑						G-1	- Piece C for SIMS (doping profile after oxidation and RTA 1050degC 20sec) - Piece D for SIMS (doping profile after oxidation and RTA 1050degC 30sec)
	33	☑						G-1	- Piece E left for further anneals, for SEM (to check epitaxial deposition selectivity on thick oxide) and SIMS (doping profile after oxidation and before RTA)
	34	☑						W-C2	" Fuming Nitric acid clean, 2nd pot only (wafers 2,4,5,6, parts 1 and 2)
	35	☑						RA-0	AG RTA stage : implant activation 30secs 1000degC (wafers 2,4,5,6, pieces A1 and A2)
	36		☑					RA-0	AG RTA stage : implant activation 30secs 1025degC (wafers 2,4,5,6, pieces B1 and B2)
	37			☑				RA-2	RTA implant activation 20secs 1050degC ("0.5um"CMOS S_D) (wafers 2,4,5,6, pieces C1 and C2)
	38				☑			RA-0	AG RTA stage : implant activation 30secs 1050degC (wafers 2,4,5,6, pieces D1 and D2)

A.4 Batch listing for fabrication of test structures to assess the role of a polysilicon drain on boron diffusion in vertical pMOSFETs.

In this section is reported the batch listing for fabrication of test structures to assess the role of a polysilicon drain on boron diffusion in vertical pMOSFETs. A detailed description of the fabrication process can be found in chapter 7.

G	No	1	2	3	4	5	6	ID	Description
								k2801s	EG - Trial batch for vertical MOSFET with n channel
								r1	
								g0	
	1	✓						G-S12	Title Page: 4 wafers, MATERIAL: p-type, <100>, 10-33ohm.cm
	2	✓						G-1P	Lithography Notes: no lithography required
	3	✓						G-1	#1 -> Ltarget = 100nm (epi + implant) #2 -> Ltarget = 250nm (epi + implant) #3 -> Ltarget = 100nm (epi + poly) #4 -> Ltarget = 250nm (epi + poly)
								source	#################Source implantation and anneal
	4	✓						W-C1	* RCA clean; wafers 1-4
	5	✓						F5-9002P	* Pad oxidation: 900degC, 20nm+- 5nm, O2 + HCl; wafers 1-4
	6	✓						IB-0	* Implant B+; 2E15cm-3, 20KeV; wafers 1-4
	7	✓						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-4
	8	✓						W-C1	* RCA clean; wafers 1-4
	9	✓						F4-N10DI	* General Boron Drive-in 1100degC 10'dryO2,30'N2; wafers 1-4
	10	✓						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic; wafers 1-4
								epibody	#################Body epitaxial deposition
	11	✓						W-C6	* Pre-epitaxy clean; wafer 1
	12	✓						LE-0	Low Pressure Epitaxy; 750degC; N-doped Si, phosphorus, 1e18cm-3, thickness about 360nm; wafer 1
	13		✓					W-C6	* Pre-epitaxy clean; wafer 2
	14		✓					LE-0	Low Pressure Epitaxy; 750degC; N-doped Si, phosphorus, 1e18cm-3, thickness about 510nm; wafer 2
	15			✓				W-C6	* Pre-epitaxy clean; wafer 3
	16			✓				LE-0	Low Pressure Epitaxy; 750degC; N-doped Si, phosphorus, 1e18cm-3, thickness about 130nm; wafer 3
	17				✓			W-C6	* Pre-epitaxy clean; wafer 4
	18				✓			LE-0	Low Pressure Epitaxy; 750degC; N-doped Si, phosphorus, 1e18cm-3, thickness about 280nm; wafer 4
								polydep	#################Polysilicon drain deposition
	19	✓						W-C1	* RCA clean; wafers 3 and 4
	20	✓						WH-2D1	Dip etch, 20:1 BHF 25degC. Until just hydrophobic; wafers 3 and 4
	21	✓						F15-PSID	LPCVD POLYSILICON DEPOSITION; in Koyo vertical furnace; deposit 200nm polySi; wafers 3 and 4
								draindop	#################Drain doping and RTA
	22	✓						IB-0	* Implant B+; 2E15cm-3, 20KeV; wafers 1-4
	23	✓						G-1	Cleave samples for RTA; wafers 1-4
	24	✓						W-C2	* Fuming Nitric acid clean, 2nd pot only; wafers 1-4
	25	✓						RA-0	AG RTA stage : 20sec, 1000degC; 1 run with part wafers from wafers 1-4
	26		✓					RA-0	AG RTA stage : 20sec, 950degC; 1 run with part wafers from wafers 1-4
	27			✓				RA-0	AG RTA stage : 20sec, 900degC; 1 run with part wafers from wafers 1-4

Appendix B

Simulation script files

The device simulations presented in this thesis have been performed using Silvaco's device simulation software, called Atlas. A detailed description of the syntax and models used can be found in reference [96]. The Atlas script files used for the simulations are reported in the following. The structures simulated have been designed using Silvaco's device structure editor, called Devedit [97]. In the following are reported the Devedit command files relative to the structures simulated.

B.1 GIDL device simulations

In the following is reported the Atlas simulation script file used for device simulation of a gated diode. The results of the simulations are reported and discussed in chapter 4.

```
# Process simulation for GIDL on Gated Diode with 4.3 nm gate oxide thickness

go atlas

mesh infile=GatedDiodeGIDL02um43nm.str

# Models used for the simulation
models srh conmob fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \
        fermi print temperature=300 bbt.std numcarr=2

# Parameters used for the simulation
mobility  bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200 \
       taun.cvt=0.125 taup.cvt=0.0317 gamn.cvt=2.5 gamp.cvt=2.2 \
        mu0n.cvt=52.2 mu0p.cvt=44.9 mu1n.cvt=43.4 mu1p.cvt=29 mumaxn.cvt=1417 \
        mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 csn.cvt=3.43e+20 \
        csp.cvt=6.1e+20 alphn.cvt=0.68 alphp.cvt=0.71 betan.cvt=2 betap.cvt=2 \
        pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 delp.cvt=2.0546e+14

# Numerical methods
method newton trap

# Set all voltages to zero
solve initial

# Output the electric field
Output e.field
```

```
# Ramp the drain bias from 0 V to 2 V
solve Vdrain=0.0 Vstep=0.1 Vfinal=2 name=drain

# Ramp the gate bias from 0 V to 3 V
log outf=GatedDiode02um43nmIVg.log master
solve Vgate=0.0 Vstep=-0.1 Vfinal=-3 name=gate
save outf=GatedDiode02um43nmIVg.str
log outf=tmp
tonyplot GatedDiode02um43nmIVg.str
tonyplot GatedDiode02um43nmIVg.log

quit
```

The gated diode simulations were performed on a structure designed using the Devedit software. The Devedit command file used to design the gated diode with 4.3 nm thick gate oxide is reported in the following.

```
# Devedit command file for design of a gated diode with 4.3 nm thick gate oxide

# Work area definition
work.area x1=-0 y1=-0.2 x2=0.5 y2=0.3

# User defined 1D doping profiles
"profile name=""NewProfile001"""
"profile name=""NewProfile002"""

# Regions definitions
region reg=1 mat=Silicon color=0xffcc00 pattern=0x4 \
"polygon=""0,0 0.5,0 0.5,0.2 0.4,0.2 0.1,0.2 0,0.2"""
impurity id=1 region.id=1 imp=Boron \
peak.value=3e+18 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=1 default max.height=0.05
region reg=2 mat=SiO~2 color=0xff pattern=0x2 \
"polygon=""0,0 0,-0.0043 0.5,-0.0043 0.5,0"""
constr.mesh region=2 default max.height=0.0005
region reg=3 name=gate mat=Polysilicon color=0xffff00 pattern=0x5 \
"polygon=""0,-0.1 0.5,-0.1 0.5,-0.0043 0,-0.0043"""
impurity id=1 region.id=3 imp=Arsenic \
peak.value=6e+19 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=3 default
region reg=4 name=gate mat=Aluminum elec.id=1 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0,-0.2 0.5,-0.2 0.5,-0.1 0,-0.1"""
constr.mesh region=4 default max.height=1 max.width=1 \
min.height=0.1 min.width=0.4
region reg=5 name=bulk mat=Aluminum elec.id=2 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0.1,0.2 0.1,0.3 0,0.3 0,0.2"""
constr.mesh region=5 default max.height=1 max.width=1 \
min.height=0.1 min.width=0.1
region reg=6 name=drain mat=Aluminum elec.id=3 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0.4,0.2 0.5,0.2 0.5,0.3 0.4,0.3"""
constr.mesh region=6 default max.height=1 max.width=1 \
min.height=0.1 min.width=0.1

# Impurity doping profiles
impurity id=1 imp=Arsenic color=0x8c5d00 \
peak.value=2.07e+20 ref.value=5e+19 comb.func=Multiply \
y1=0.02 y2=0.2 rolloff.y=step \
x1=0.3 x2=0.5 rolloff.x=step
```

```
impurity id=2 imp=Arsenic color=0x8c5d00 \
peak.value=2.07e+20 ref.value=5e+19 comb.func=Multiply \
"y1=0.02 y2=0.02 rolloff.y=low conc.func.y=NewProfile002 conc.param.y=""Linear Interpolate"" \"
"x1=0.3 x2=0.5 rolloff.x=low conc.func.x=NewProfile001 conc.param.x=""Linear Interpolate"""
impurity id=3 imp=Arsenic color=0x8c5d00 \
peak.value=2.07e+20 ref.value=5e+19 comb.func=Multiply \
y1=0.02 y2=0.2 rolloff.y=step \
"x1=0.3 x2=0.3 rolloff.x=low conc.func.x=NewProfile001 conc.param.x=""Linear Interpolate"""

# Meshing Parameters
base.mesh height=10 width=10
bound.cond !apply max.slope=30 max.ratio=100 rnd.unit=0.0001 line.straightening=1
align.points when=automatic
imp.refine imp=Arsenic scale=log sensitivity=0.1 transition=1e+10
imp.refine min.spacing=0.002
constr.mesh max.angle=90 max.ratio=300 max.height=0.02 \
max.width=0.02 min.height=0.0001 min.width=0.0001
constr.mesh type=Semiconductor default
constr.mesh type=Insulator default
constr.mesh type=Metal default
constr.mesh type=Other default
constr.mesh region=1 default max.height=0.05
constr.mesh region=2 default max.height=0.0005
constr.mesh region=3 default
constr.mesh region=4 default max.height=1 max.width=1 \
min.height=0.1 min.width=0.4
constr.mesh region=5 default max.height=1 max.width=1 \
min.height=0.1 min.width=0.1
constr.mesh region=6 default max.height=1 max.width=1 \
min.height=0.1 min.width=0.1
Mesh Mode=MeshBuild

# Mesh refine
refine mode=y x1=0 y1=0.0001 x2=0.14 y2=0.02
refine mode=y x1=0 y1=0.0001 x2=0.14 y2=0.015
refine mode=y x1=0 y1=0.0001 x2=0.5 y2=0.01
refine mode=y x1=0 y1=-0.0044 x2=0.5 y2=-0.015
refine mode=y x1=0 y1=-0.0044 x2=0.5 y2=-0.015
```

B.2 Dielectric pocket device simulations

In the following is reported the Atlas simulation script file used for device simulation of a planar MOSFET with a parasitic oxide layer between drain and body. The results of the simulations are reported and discussed in chapter 6.

```
# Simulation of a planar MOSFET with a dielectric pocket
go atlas
mesh infile=MOSdpTunnTox2A.str

# Atlas models used for the simulation
models fnord srh conmob fldmob b.electrons=2 b.holes=1 evsatmod=0 hvsatmod=0 cvt \
        boltzman print temperature=300

# Models parameters
mobility  bn.cvt=4.75e+07 bp.cvt=9.925e+06 cn.cvt=174000 cp.cvt=884200 \
        taun.cvt=0.125 taup.cvt=0.0317 gamn.cvt=2.5 gamp.cvt=2.2 \
        mu0n.cvt=52.2 mu0p.cvt=44.9 mu1n.cvt=43.4 mu1p.cvt=29 mumaxn.cvt=1417 \
```

```
        mumaxp.cvt=470.5 crn.cvt=9.68e+16 crp.cvt=2.23e+17 csn.cvt=3.43e+20 \
        csp.cvt=6.1e+20 alphn.cvt=0.68 alphp.cvt=0.71 betan.cvt=2 betap.cvt=2 \
        pcn.cvt=0 pcp.cvt=2.3e+15 deln.cvt=5.82e+14 delp.cvt=2.0546e+14

# Numerical methods used
method newton trap

# Set all voltages to zero
solve initial

# Ramp the gate voltage from 0 V to 3 V
solve Vgate=0.0 Vstep=0.1 Vfinal=3 name=gate

# Ramp the drain voltage from 0 V to 3 V
log outf=IdVdVg3Tox2AYesOut.log master
solve Vdrain=0 Vstep=0.1 Vfinal=3 name=drain
save outf=StructVd3Vg3Tox2AYesOut.str
log outf=tmp
tonyplot StructVd3Vg3Tox2AYesOut.str
tonyplot StructVd3Vg3Tox2AYesOut.str -set Current.set
tonyplot IdVdVg3Tox2AYesOut.log
quit
```

The dielectric pocket MOSFET simulations were performed on a structure designed using the Devedit software. The command file used to design the planar MOSFET with a 2 Å thick parasitic oxide layer between drain and body is reported in the following.

```
# Devedit command file used to design the structure of a planar dielectric pocket
# MOSFET with a 2 Angstrom thick parasitic oxide between drain and body

# Work area definition
work.area x1=0 y1=-0.3 x2=0.6 y2=0.3

# Regions definitions
region reg=1 mat=Silicon color=0xffcc00 pattern=0x4 \
"polygon=""0.4,0 0.4,0.2 0.35,0.2 0.25,0.2 0,0.2 0,0 0.1,0 0.15,0"""
impurity id=1 region.id=1 imp=Boron \
peak.value=1e+18 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=1 default
region reg=2 mat=SiO~2 color=0xff pattern=0x2 \
"polygon=""0.4002,0 0.4002,0.2 0.4,0.2 0.4,0"""
constr.mesh region=2 default max.width=0.0001
region reg=3 mat=Silicon color=0xffcc00 pattern=0x4 \
"polygon=""0.6,0 0.6,0.2 0.4002,0.2 0.4002,0 0.45,0 0.5,0"""
impurity id=1 region.id=3 imp=Arsenic \
peak.value=1e+20 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=3 default
region reg=4 mat=SiO~2 color=0xff pattern=0x2 \
"polygon=""0.15,0 0.15,-0.004 0.45,-0.004 0.45,0 0.4002,0 0.4,0"""
constr.mesh region=4 default max.height=0.0005
region reg=5 mat=Polysilicon color=0xffff00 pattern=0x5 \
"polygon=""0.15,-0.2 0.45,-0.2 0.45,-0.004 0.15,-0.004"""
impurity id=1 region.id=5 imp=Arsenic \
peak.value=1e+20 ref.value=1000000000000 comb.func=Multiply
constr.mesh region=5 default
region reg=6 name=gate mat=Aluminum elec.id=1 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0.15,-0.3 0.45,-0.3 0.45,-0.2 0.15,-0.2"""
constr.mesh region=6 default
```

```
region reg=7 name=bulk mat=Aluminum elec.id=2 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0.25,0.2 0.35,0.2 0.35,0.3 0.25,0.3"""
constr.mesh region=7 default
region reg=8 name=source mat=Aluminum elec.id=3 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0,-0.1 0.1,-0.1 0.1,0 0,0"""
constr.mesh region=8 default
region reg=9 name=drain mat=Aluminum elec.id=4 work.func=0 color=0xffc8c8 pattern=0x7 \
"polygon=""0.5,-0.1 0.6,-0.1 0.6,0 0.5,0"""
constr.mesh region=9 default

# Impurity profiles
impurity id=1 imp=Arsenic color=0x8c5d00 \
peak.value=1e+20 ref.value=1e+18 comb.func=Multiply \
y1=0 y2=0.2 rolloff.y=step \
"x1=0 x2=0.2 rolloff.x=high conc.func.x=""Gaussian (Dist)"" conc.param.x=0.025"
impurity id=2 imp=Arsenic color=0x8c5d00 \
peak.value=1e+20 ref.value=1e+18 comb.func=Multiply \
y1=0 y2=0.2 rolloff.y=step \
"x1=0.4 x2=0.4 rolloff.x=low conc.func.x=""Gaussian (Dist)"" conc.param.x=0.025"

# Meshing Parameters
base.mesh height=10 width=10
bound.cond !apply max.slope=28 max.ratio=300 rnd.unit=0.0001 line.straightening=1
align.points when=automatic
imp.refine imp=Arsenic scale=log transition=1e+10
imp.refine min.spacing=0.005
constr.mesh max.angle=90 max.ratio=300 max.height=0.05 \
max.width=0.05 min.height=0.0001 min.width=0.0001
constr.mesh type=Semiconductor default
constr.mesh type=Insulator default
constr.mesh type=Metal default
constr.mesh type=Other default
constr.mesh region=1 default
constr.mesh region=2 default max.width=0.0001
constr.mesh region=3 default
constr.mesh region=4 default max.height=0.0005
constr.mesh region=5 default
constr.mesh region=6 default
constr.mesh region=7 default
constr.mesh region=8 default
constr.mesh region=9 default
Mesh Mode=MeshBuild

# Mesh refine
refine mode=x x1=0.1281 y1=0.0147 x2=0.3954 y2=0.0759
refine mode=x x1=0.423 y1=0.0119 x2=0.4698 y2=0.0726
refine mode=x x1=0.1788 y1=-0.0452 x2=0.4247 y2=-0.0129
refine mode=y x1=0.1613 y1=-0.0416 x2=0.4388 y2=-0.0115
refine mode=y x1=0.114 y1=0.0061 x2=0.3976 y2=0.0422
refine mode=y x1=0.4117 y1=0.0047 x2=0.4862 y2=0.0428
refine mode=y x1=0.1602 y1=-0.0228 x2=0.4371 y2=-0.0088
refine mode=y x1=0.1111 y1=0.0028 x2=0.3937 y2=0.0185
refine mode=y x1=0.4089 y1=0.0028 x2=0.4851 y2=0.0215
refine mode=y x1=0.1616 y1=0.00175 x2=0.3933 y2=0.01008
refine mode=y x1=0.412 y1=0.00146 x2=0.4414 y2=0.01008
refine mode=y x1=0.162 y1=-0.01263 x2=0.4349 y2=-0.00669
refine mode=both x1=0.3896 y1=0.0009 x2=0.4443 y2=0.0232
refine mode=x x1=0.4064 y1=0.00073 x2=0.4419 y2=0.0116
refine mode=x x1=0.4039 y1=0.00072 x2=0.43007 y2=0.01166
```

Appendix C

Mask description

In this appendix is described the layout of the mask set used for vertical MOSFET fabrication. Figure C.1 shows the mask layout used to fabricate both FILOX and dielectric pocket vertical MOSFETs. The devices are grouped in blocks in the figure. Table C.1 lists the blocks with a short description of the devices contained. Single and double gate vertical MOSFETs were only fabricated within the FILOX experiment. On the other hand, the dielectric pocket experiment included only surround gate vertical MOSFETs. Finally, table C.2 lists the test structures included in the mask design to characterize the devices fabricated.

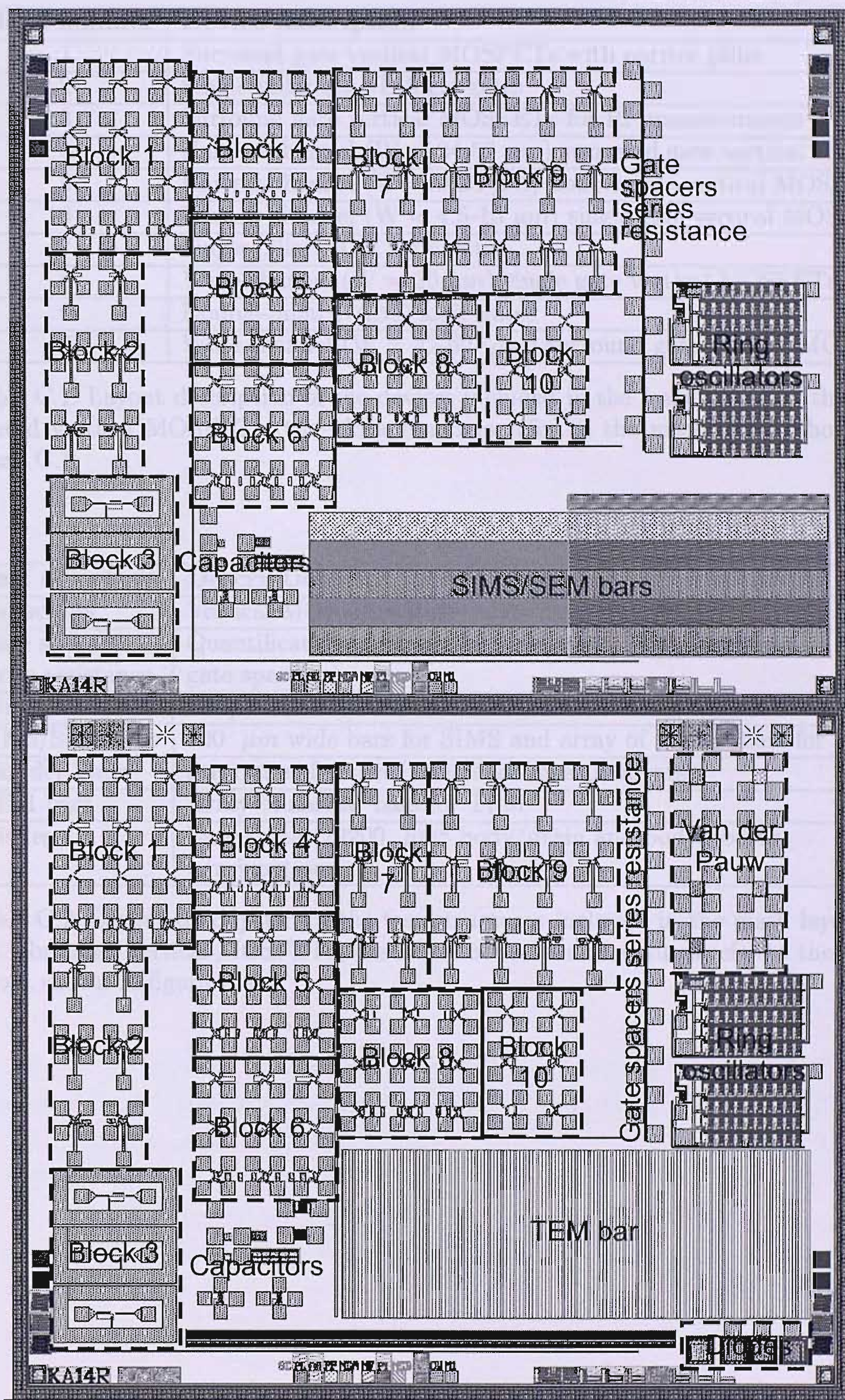

Figure C.1: Layout of the mask set used for the fabrication of the vertical MOSFETs; the labels of the device blocks refer to table C.1; the labels of the test structures refer to table C.2.

Block number	Device description
1	Surround gate vertical MOSFETs with narrow pillar
2	Single-pillar NAND logic gates
3	Surround gate vertical MOSFETs for RF measurements
4	Narrow-channel (W = 24-52 μm) surround gate vertical MOSFETs
5	Narrow-channel (W = 9-20 μm) double gate vertical MOSFETs
6	Narrow-channel (W = 4.5-10 μm) single gate vertical MOSFETs
7	Single-pillar NOR logic gates
8	Wide-channel (W = 20 μm) single gate vertical MOSFETs
9	Double-pillar NAND logic gates
10	Wide-channel (W = 42-62 μm) surround gate vertical MOSFETs

Table C.1: Layout description of the devices included in the mask layout of the fabricated vertical MOSFETs; the block numbers refer to the mask layout shown in figure C.1.

Test structure	Description
Capacitors	Vertical MOS capacitors
Gate spacers series resistance	Quantification of the series resistance of the polysilicon gate spacers
Ring oscillators	Simple circuit for RF characterization of the devices
SIMS/SEM bars	200 μm wide bars for SIMS and array of narrow bars for SEM
Van der Pauw	Structures for sheet resistance measurements
TEM bars	Array of narrow bars for TEM
Diodes	Large area (22200 μm^2 body/drain and body/source p/n junctions

Table C.2: Layout description of the test structures included in the mask layout of the fabricated vertical MOSFETs; the labels of the test structures refer to the mask layout shown in figure C.1.

Appendix D

List of Publications

D.1 Journal papers

Gili, E., Uchino, T., Hakim, M. M. A., De Groot, C. H., Buiu, O., Hall, S. and Ashburn, P. "Shallow Junctions on Pillar Sidewalls for Sub-100-nm Vertical MOSFETs". *IEEE Electron Device Letters*, 27 (8), pp. 692-695, August 2006.

Gili, E., Kunz, V. D., Uchino, T., Hakim, M. M. A., De Groot, C. H., Ashburn, P. and Hall, S. "Asymmetric Gate Induced Drain Leakage and Body Leakage in Vertical MOSFETs with reduced parasitic capacitance". *IEEE Transactions on Electron Devices*, 53 (5), pp. 1080-1087, May 2006.

Hakim, M. M. A., De Groot, C. H., Gili, E., Uchino, T., Hall, S., and Ashburn, P. "Depletion-Isolation Effect in Vertical MOSFETs During the Transition From Partial to Fully Depleted Operation". *IEEE Transactions on Electron Devices*, 53 (4), pp. 929-933, April 2006.

E. Gili, V.D. Kunz, C.H. de Groot, T. Uchino, P. Ashburn, D.C. Donaghy, S. Hall, Y. Wang, and P.L.F. Hemment. "Single, Double and Surround Gate Vertical MOSFETs with Reduced Parasitic Capacitance". *Solid-State Electronics*, 48 (4), pp. 511-519, April 2004.

S. Hall, D. Donaghy, O. Buiu, E. Gili, T. Uchino, V.D. Kunz, C.H. de Groot, and P. Ashburn. "Recent Developments in Deca-nanometer Vertical MOSFETs". *Microelectronic Engineering* (72), pp. 230-235, April 2004.

D.2 Conference papers

Tan, L., Buiu, O., Hall, S., Gili, E. and Ashburn, P. "A Technology for Building Shallow Junction MOSFETs on Vertical Pillar Walls". *Proceedings of 8th International Conference on Solid-State and Integrated-Circuit Technology*, Shanghai, China, October 2006.

Gili, E., Uchino, T., Hakim, M. M. A., De Groot, C. H., Ashburn, P. and Hall, S. "A New Approach to the Fabrication of CMOS Compatible Vertical MOSFETs Incorporating a Dielectric Pocket". *Proceedings of 6th International Conference on ULtimate Integration of Silicon (ULIS)*, pp. 127-130, Bologna, Italy, April 2005.

Hakim, M. M. A., De Groot, C. H., Gili, E., Uchino, T., Hall, S. and Ashburn, P. "Effect of Transition from PD to FD Operation on the Depletion Isolation Effect in Vertical MOSFETs". *Proceedings of 6th International Conference on ULtimate Integration of Silicon (ULIS)*, pp. 131-134, Bologna, Italy, April 2005

Hakim, M. M. A., Ashburn, P., De Groot, C. H., Gili, E., Uchino, T. and Hall, S. "Germanium Seeded Crystallisation of a-Si for Application in 3D Integration". *Proceedings of PREP*, Lancaster, UK, April 2005

V. D. Kunz, C. H. de Groot, E. Gili, T. Uchino, S. Hall, P. Ashburn. "CMOS-compatible Vertical MOSFETs and Logic Gates with Reduced Parasitic Capacitance". *Proceedings of the 34th European Solid-State Device Research Conference (ESSDERC)*, pp. 221-224, Leuven, Belgium, September 2004.

E. Gili, V. D. Kunz, C. H. de Groot, T. Uchino, D. Donaghy, S. Hall, and P.Ashburn. "Electrical Characteristics of Single, Double & Surround Gate Vertical MOSFETs with Reduced Overlap Capacitance". *Proceedings of 33rd European Solid-State Device Research Conference (ESSDERC)*, pages 533-536, September 2003.

S. Hall, D. Donaghy, O. Buiu, E. Gili, T. Uchino, V. D. Kunz, C. H. de Groot and P. Ashburn. "Recent Developments in Deca-nanometer Vertical MOSFETs". *Proceedings of the 13th Insulating Films on Semiconductors Conference*, June 2003.

Gili, E., Kunz, V. D., Uchino, T., De Groot, C. H. and Ashburn, P. "Realization and Characterization of Vertical MOSFETs with Reduced Parasitic Capacitance". *Proceedings of PREP*, pp. 81-82, Exeter, UK, April 2003.

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