UNIVERSITY OF SOUTHAMPTON

Near-infrared photodetectors based on Si\SiGe quantum nanostructures

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A thesis submitted for the degree of Doctor of Philosophy

Electronics and Computer Science

March 2006

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UNIVERSITY OF SOUTHAMPTON <u>ABSTRACT</u> ELECTRONICS AND COMPUTER SCIENCE <u>Doctor of Philosophy</u>

Near-infrared photodetectors based on Si\SiGe quantum nanostructures By Phansak Iamraksa

Si/Si_{1-x}Ge_x multiple quantum well structures are grown by low pressure chemical vapour deposition (LPCVD). The LPCVD systems used were built in-house and are used to produce epitaxial layers at relatively high growth rates. Typically, 10 periods of Si/Si_{1-x}Ge_x quantum wells are grown on <100> silicon substrates at 800°C and at 0.5 Torr. SiGe quantum wells of around 10, 20 or 30 nm are produced with Ge content in the range 6% to 20%. Increasing germane flow is shown to increase the incorporation rate of germanium atoms and at high germanium incorporation levels the Si/Si_{1-x}Ge_x layers are shown to form lens-shaped quantum dots of relatively high germanium content.

Absorption and photoluminescence (PL) measurements are performed to investigate the optical properties and the band structure of the quantum structures. Extended absorption in the near-infrared is observed for the $Si/Si_{1-x}Ge_x$ quantum well samples, with a wavelength cut-off around 1300nm. Doped multi-layer samples indicate additional absorption in the 2µm to 5µm spectral range, due to a free carrier absorption mechanism. Photoluminescence spectra indicate bandgap narrowing due to both increasing germanium composition and strain effects, furthermore, free exciton radiative transitions are observed up to 100K indicating quantum confinement.

p-*i*-n photodiodes are constructed to form photodetectors incorporating $Si/Si_{1-x}Ge_x$ epilayers. The epitaxial layers grown at 820°C and at 0.5 Torr, consisted sets of ten periods of $Si/Si_{1-x}Ge_x$ layers with nominal 6% or 20% germanium content and 10, 20 or 30nm SiGe thickness providing six main device sets. The I-V characteristics of all devices indicate reliable diode performance. Device photoresponses were studied with a range of bias voltages for wavelengths from 900 to 1500 nm at room temperature. The quantum efficiency in all devices indicates good photodetection extending to 1350 nm in the near-infrared beyond the energy corresponding to the bandgap of silicon.

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Acknowledgements

I would like to thank my supervisor Dr. Darren Bagnall for his support, guidance and patience throughout this project. I would like to thank especially Dr. Neil Lloyd and Dr. Janet M. Bonar for epitaxy growths advises and suggestions. I would like to thank Dr. Shuncai Wang, Dr. Takeshi Ushino, and Dr. Claudia Cerina for helping and teaching with TEM sample preparation and operation, and to Dr Wen Zhang for her help with mask design. My appreciation also spread out to all clean room staff particular Tony Blackburn, Mike Josey, Mohamad R Hadrun, Richard Bayly, Jean Humphries, and Corry Kratochvila for their help and consultation with fabrication processing.

My love and gratitude especially goes to my parent, Aueay, friends and past teachers for support during the hard time of my PhD and never giving up on me. I would like to thank to my family for raising and polishing, which make me as me today.

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Chapter 1

Introduction

Two important technologies currently dominate the optoelectronics industry; silicon based microectronics and silica based fibre-optics. Microelectronics enables information processing, while fibre-optics enable rapid long-distance communications. If these two technologies could be fully integrated a *global information super-highway* could be realised that could, among other things, enable real-time video, sound and perhaps *virtual reality* information to flow from every system user to any other system users.

The minimum absorption band for fibre-optics is in the near-infrared, just a little beyond the range that can be detected by silicon based photodetectors. This simple mismatch is a very effective barrier to the monolithic integration of optical components such as modulators and detectors, and microelectronics components. This mismatch is one of the factors that currently prevent the large scale realisation of the global information superhighway.

The silicon bandgap of 1.12eV ensures that only photons with wavelength below 1109 nm have sufficient energy to generate an electron-hole pair [1, 2]. As a result, silicon cannot provide efficient photodetectors, operating in the technologically important 1100-1600nm wavelength range. However, another group *IV* semiconductor, germanium, has a bandgap of 0.66eV and can allow the fabrication of photodetectors with detection up to 1882nm.

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The *Si-Ge binary* alloy system can, in principle, provide *bandgap engineering* in the form of *quantum wells* within silicon-based devices in order to move the detection limits of photodetectors (diodes or *CCDs*) from 1109nm (pure silicon) through to 1882nm (pure germanium) [3]. In practise, the defect-free epitaxial growth of *SiGe* layers on silicon can only be produced within relatively confined ranges of compositions and thicknesses. Layers with high germanium compositions can only be realised for very thin layers (a few nanometers) due to the crystal lattice mismatch that exists between silicon and germanium (4%) [4]. This lattice mismatch always produces strain in *Si/SiGe* systems that must be accounted for in device design. This makes *Si/SiGe* epitaxial growth challenging and leads to complex modifications to band structures and optical properties. These complications and difficulties, combined with the usual challenges associated with semiconductor epitaxy, make the realisation of controlled *SiGe* epitaxial growth the most crucial challenge during the manufacture of *SiGe* optoelectronic devices, and in spite of, the potential benefits of such advances. These problems have not yet been adequately solved.

Si/SiGe epitaxial growth can only be realised with the use of either molecular beam epitaxy (*MBE*) or chemical vapour deposition (*CVD*) techniques. In general, *MBE* is the preferred technique for multi-layered, optical semiconductor devices where slow growth rates. Additionally, *in-situ* monitoring and ultra-high vacuum cleanliness allow the best control of composition and thickness, and low-defect low-impurity deposition. On the other hand, *CVD* is associated with fast, large-area and multiple-wafer deposition. *CVD* does not readily lend itself to quantum well growth but it is the technique preferred by industry because it has a large throughput and lower maintenance costs.

The main categories of silicon based photodetectors currently, in commercial use, are p-i-n photodiodes, avalanche photodiodes and single photon avalanche detectors (SPADs). The wavelength ranges of each of these devices, having the potential to be extended into the infrared by placing *SiGe* quantum wells within the absorption region of the devices. Many reports consider designs of *Si/SiGe* strained quantum well photodetectors [5-9]. However, the main challenges relate to the deposition techniques, processes and *Si/SiGe* quality. The primary aim of this work is to use *CVD* to produce *Si/SiGe* quantum well structures for near-infrared photodetectors.

The development of near-infrared photodetectors for integrated fibre-optic devices is in itself a good justification for continued research into Si/SiGe devices and Si/SiGe epitaxial growth. However, there are important opportunities across the entire infrared spectral range that might benefit from increased research in this area. The very near infrared (700nm-1100nm) is readily absorbed and detected by silicon and commonly used. As discussed previously, the range is just beyond the limits of silicon (but potentially within reach of SiGe) from 1100nm to 1.8µm remains important for spectroscopy, imaging and photovoltaics but is perhaps an order of magnitude more expensive because technologies require more than purely silicon devices. The remainder of the near-, mid- and far-infrared (much of which is now considered as the *THz* regime) are becoming increasingly important and under-utilised spectral regions. Applications include thermal imaging systems, sensors for medical diagnosis and environmental monitoring, night-vision enhancement, space-based surveillance, fire and combustion control [10]. These applications often require high sensitivity and selectivity with photon energies so small that phonon energies and carrier thermal energies are always important considerations.

Recently, the realisation of *GaAlAs* and *InGaP* based quantum cascade lasers and quantum well infrared photodetectors have opened up new technological fields [11]. These new devices are based upon the exploitation of *intersubband transitions* rather than *interband transitions* [11]. During interband transitions, there are the familiar movements of electrons between conduction and valence bands. However, during intersubband transitions carriers move between energy sub-levels, existing within the valence or conduction bands. These transitions are accompanied by the absorption or emission of infrared photons. To date, most of the successful works on intersubband devices have been carried out using *III-V* semiconductors rather than group *IV* semiconductors, but where the *III-V* materials have a clear scientific advantage in the realisation of interband devices (where direct bandgaps are hugely advantageous). There are strong scientific, technological and economic arguments that actually favour group *VI* materials in the case of intersubband devices.

With intersubband, devices the disadvantages of group *IV* semiconductors are largely to do with the difficulties, associated with producing high quality epitaxial layers of

Si/SiGe, and the inconvenience of lattice mismatch, allied to the need for very precise thickness and composition control, not only to define energy levels but to also to obtain high quantum efficiency and low dark current [12-14]. Precise tuning of intersubband transitions requires precise design of the thickness of silicon barrier layers and the thickness of doped *SiGe* layers.

For a number of years Southampton University has developed a number of unique low pressure chemical vapour deposition (*LPCVD*) systems, and established a range of silicon growth processes. Southampton has also researched *SiGe* deposition for several years but mainly in the context of heterojunction bipolar transistors (*HBTs*) [15] and *BiCMOS* applications. *Si/SiGe* layers for optoelectronic applications have not been researched at Southampton before this work. Given the unique nature of the *LPCVD* equipment available, this work represents an exciting new research opportunity in which interband and eventually intersubband devices might be investigated.

This thesis contains a further 6 chapters. Chapter 2 contains a detailed consideration of epitaxy in general and *SiGe* epitaxy in particular. In chapter 3, the *Si/SiGe* epitaxial growth experiments and layer characterisations are detailed. Chapter 4 details an exploration of the photoluminescence properties of the *LPCVD Si/SiGe* structures. The fifth and sixth chapter detail device fabrication and characterisations. The seventh chapter provides some conclusions and suggestions for future work.

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Chapter 2

Literature Survey

This chapter presents a detailed overview of the epitaxial growth of silicon germanium structures and the fundamental structural, electronic and optical properties of silicon germanium. This chapter also considers *SiGe* technology and explores the fabrication and operation of some silicon germanium photodetectors.

2.1 Chemical Vapour Deposition

Chemical vapour deposition (CVD) is one of the most important deposition technologies and is widely used in industry for a large range of materials. Whereas, physical deposition techniques require low pressure systems to deliver atomic species to a substrate. Chemical vapour deposition techniques can take place in chambers at atmospheric pressure, and gas molecules (precursors) are delivered to a heated substrate. These molecules decompose at the surface of the substrate, the useful atoms are adsorbed into the growth plane, and the gaseous by-products are expelled from the system. It is convenient to visualise CVD as a complex system at equilibrium with a large number of parameters, governing the rate of atom adsorption to the growth surface.

2.1.1 Chemical Vapour Deposition Discussion

CVD epitaxy can be carried out on a heated substrate at temperatures substantially below the material melting point (typically 30 to 50% lower). There are three common types of susceptors: horizontal, pancake and barrel (Fig. 2.1), most are made of graphite [16]. These susceptors serve as the crucible of growth, supporting the wafer, and providing thermal energy for the deposition reaction.





CVD systems can be divided into hot-wall and cold-wall systems. The hot wall has the advantage that a constant temperature profile is assured through the process, resulting in good layer uniformity. However, the material can deposit on the wall of the system and might be subsequently re-deposited on the surface of the substrate. This problem is not found in cold-wall (water-cooled) systems where only the heated substrate is maintained at a high temperature.

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The growth pressure of CVD can also define many characteristics of a system Lowpressure CVD (LPCVD) system operates in the range 10^{-1} to 10^{-2} Torr. Ultra-highvacuum CVD (UHVCVD) operates at 10^{-4} Torr.

The gas kinetics between substrate and the reactant species can be considered as shown in figure 2.2.



Figure 2.2: The model of the epitaxial-growth process [16].

 C_g is the concentration of the reactant species in gas stream far away from the gas substrate interface (C_s). The flux of reactant species from the gas stream to the growth interface is F_1 , while F_2 is the flux corresponding to the gas consumed in the reactions. In the steady state, F_1 is equal F_2 ($F_1 = F_2 = F$), then

$$F_{I} = h_{g} \left(C_{g} - C_{s} \right) \tag{21}$$

$$F_2 = k_s C_s \tag{2.2}$$

where, h_g and k_s are vapour phase mass transfer coefficient (*cm/s*) and the surface reaction rate constant (*cm/s*) respectively. At steady state, the gas at the interface (C_s) becomes

$$C_s = \frac{C_g}{1 + \left(k_s / h_g\right)} \tag{2.3}$$

The growth rate (R) is calculated by steady-state flux divided by number of atoms incorporated into a unit volume of the layer (C_a)

$$R = \frac{F}{C_a} = \frac{k_s h_g}{k_s + h_g} \left[\frac{C_g}{C_a} \right]$$
(2.4)

The value of C_a is 5×10^{22} atom/cm³ for silicon and 4.4×10^{22} atom/cm³ for gallium arsenide [16]. The growth rate (*R*) can be divided into two regimes: firstly, if k_s is smaller than h_g , then *R* depends on how fast the surface reaction is acheived. However, if h_g is smaller than k_s , then *R* depends on how fast the reaction species are transported to the surface. The first case occurs at low growth temperature, while the latter occurs at high growth temperatures (Fig. 2.3).



Figure 2.3: The Arrhenius plot of growth temperature dependence of growth rate.

In an Arrhenius plot (Fig. 2.3), the two growth regimes can be readily observed. At low growth temperature regime, the growth rate obeys an exponential law, $R \sim exp(-E_a/kT)$, where E_a is the activation energy. At high temperature, the growth rate is independent of temperature. This high growth temperature regime is *mass transportcontrolled*, while the low temperature regime is surface-reaction (or temperature) controlled [1, 16]. Growth rate is not the only issue, in general high quality epitaxial layer are most likely to be obtained at relatively high growth temperatures. Furthermore, when thickness uniformity is an important issue growth should be performed where the growth rate is relatively insensitive to small growth temperature variations, and this is more likely in the mass transport regime.

Just as in equilibrium is established in the gas phase, an equally complex equilibrium is established on the growth surface. Adsorbed atoms, *adatoms*, arrive at the growth surface and then diffuse about the surface until they are absorbed into the growing layer, where the gas-phase processes, described above, largely determine the growth rate it is the surface *adatom* dynamics that determine the crystalline quality of the material and determine amorphous, polycrystalline or epitaxial growth (Fig. 2.4).

At the start of the process, adatoms are adsorbed (deposited) onto the growth surface. These adatoms then diffuse until they find an absorption site. Adatoms might nucleate with other adatoms, be integrated at kinks on steps of the growth plane or integrated at other existing nucleation sites [17]. Surface defects can trap adatoms and lead to the construction of growth islands. Adatoms that do not absorb or nucleate will be desorbed from surface.



Figure 2.4: Growth kinetics of adatoms on the growth surface [17].

For most of a deposition procedure, the growth equilibrium is established. However, the start of the deposition is slightly different. The detail of nucleation has to be considered. This effect leads to a concept of an incubation time (t_i) that represents the time delay for actual nucleation/deposition during the initial stages of a deposition process. For the majority of processes, incubation delays occur as a result of a different sticking probability of adatoms or precursors for the substrate and the material being deposited [17], and the deposition only becomes steady state when the material being deposited has more or less complete coverage of the substrate. Only in the case of pure epitaxial growth (silicon on silicon for example) might, we expect that there is no incubation time, but even then it is often difficult to prepare a surface adequately.

For perfect epitaxy, growth has to progress atomically, step-by-step and row-by-row, and adatoms need to be deposited within an *adatom diffusion length* of an atomic step to contribute to the growth. As a result of these requirements, epitaxial growth is difficult to achieve, and any number of non-ideal effects can produce threedimensional growth effects and defective crystallinity. Perfect epitaxial growth should produce atomically flat surfaces and perfect single crystals. To achieve this, it is necessary to ensure that the silicon wafer substrate is atomically flat, well cleaned, defect (and oxide) free, and the growth conditions must ensure that contaminants are not adsorbed onto the growth surface. The surface temperature must be such that the adatom diffusion length is long enough, or else amorphous growth will take place. The adsorption rate must also be low enough to ensure that adatoms do not spontaneously nucleate and form growth islands (and polycrystalline material), and the precursor density and temperature must be such that particulates are not formed in the gas-phase as this will also lead to defective growth.

As challenging as epitaxial growth may seem, it is often reliably achieved by experienced growth technicians operating suitable equipment, the temperatures, pressures and flow rates are well known and wafer preparation techniques to provide a suitably prepared surface are also well known. Epitaxy becomes increasingly challenging when multilayered strained heterostructures are required, especially when different lattice constants, alloy compositions and thicknesses are needed. In such systems, there is an increasing likelihood of defect formation and three-dimensional growth and control of these undesired effects remains a challenge. In this context, it is interesting to consider that the emerging desire to use self-assembling techniques to enhance semiconductor device performance, it causes scientists to actively seek three-dimensional growth to form quantum dots.

2.1.2 Growth Modes

Three different growth modes have been well described, Van de Merwe, Volmer-Weber and Stranski-Krastanov. These different modes are dependent on the freeenergy associated with the two materials, involved in growth. Three macroscopic free-energies are introduced, γ_0 is the free energy per unit area at the layer-vacuum interface, γ_i is the free energy per unit area at the layer-substrate interface and γ_s is the free energy per unit area at the substrate-vacuum interface [18] (Fig. 2.5).



Figure 2.5: Free energy consideration for growth mode determination. *FM* is *Van der Merwe* growth and *VW* is *Volmer-Weber* growth [18].

Perfect crystal epitaxy can be realized when these components meet the condition:

$$\gamma_{0(n)} + \gamma_{i(n)} \le \gamma_s \tag{2.5}$$

Where, n represents a film composed of n layers. This relation implies that the system gains energy when the substrate is entirely covered by the growth layer and allows the *Van der Merwe (FM)* growth mode (2D) layer by layer growth. This condition is likely to be acheived for homoepitaxial growth, and growth is, otherwise, closed to thermodynamic equilibrium.

In the heteroepitaxial case, the condition for FM growth mode is

$$\gamma_{0(n)} << \gamma_s.$$

If $\gamma_{0(n)} > \gamma_s$ then *Volmer-Weber* growth will prevail and three-dimensional islands will form on the substrate.

The structural mismatch between a pseudomorphic layer and the substrate can lead to a monotonic increase of strain energy during *Van der Merwe* growth as film thickness is increased. This will eventually begin to affect the balance of equation 2.5 and this can lead to an unstable situation at a critical thickness (h_c). At this point the growth mode will switch from 2D to 3D. This is known as the *Stranski-Krastanov* (SK) growth mode and is the mode most commonly exploited to create "self-organised" quantum dots [18, 19].

2.2 Silicon and silicon germanium growth reactions

Growth reactions usually described in terms of the chemical reaction between gaseous species and the surface of the wafer. These acknowledges, that the substrate surface and the substrate temperature, are integral parts of the process, and the chemical reactions necessary can only occur at the surface of the substrate.

For silicon growth, silane is the most commonly used precursor for silicon, while germane is most commonly used for germanium. Silicon and germanium growth can be described by the following reactionsl [20]:

$$SiH_4 \leftrightarrow SiH_2 + H_2$$
 (2.6A)

$$H_2 + 2S \leftrightarrow 2(H - S) \tag{2.6B}$$

 $SiH_2 + S \leftrightarrow (SiH_2 - S) \rightarrow Si_{(S)} + H_2 + S$ (2.6C)

Where S is an empty active site on the substrate surface, and quantities in brackets represent the gaseous species, occupying the vacant site [20].

Chemical reaction (Eq. 2.6A) is silane decomposition. This is accompanied by the hydrogen desorption reaction (Eq. 2.6B). Equation 2.6C is the beginning of the Si nucleation process between the gas products of equation 2.6A and empty sites at the substrate surface. These reactions are just a few examples of possible growth mechanisms that may occur inside the deposition chamber. Pressure, temperature and flow rate control will change the equilibrium and determine the dominated reaction. The actual growth mechanism, that operates, depends on all the conditions and equipment, used. Similar reaction also exists for *Ge* as:

$$GeH_4 \leftrightarrow GeH_2 + H_2$$
 (2.6D)

2.3 The Si/Si_{1-x}Ge_x system

Successive layers of silicon and silicon-germanium $(Si/Si_{1-x}Ge_x)$ can be grown by epitaxial processes. These types of structure are classified as a heterostructures because they are formed by different materials. Both silicon and germanium are group IV indirect band-gap semiconductors, the bandgap of silicon is 1.12eV at 300K, while the germanium bandgap is 0.66eV at 300K [21]. By using molecular beam epitaxy or epitaxial chemical vapour deposition, $Si/Si_{1-x}Ge_x$ heterostructures can be realized that modify the band structure and allow specific applications. In any heterostructure system, the lattice mismatch between layers must be considered. A key advantage of the III-V compound semiconductor system based on GaAs and AlAs is that the lattice mismatch is as low as 0.04%. This means that complex III-V semiconductor heterostructures can be grown with almost no lattice mismatch and very low defect levels. This is not the case for the Si/SiGe system where the lattice constants of silicon and germanium (5.43095 and 5.64613A°), amount to a lattice mismatch of 4% [21]. This mismatch limits the range of SiGe alloy compositions and thicknesses that can be combined. When one layer of material grows on another layer of material with built-in strain, so that there is a coherent alignment of atoms. It is called *pseudomorphic growth*, since the growth layers take on the morphology of the substrate. When germanium is grown epitaxially on silicon, the lattice constant of the epitaxial layer in the direction parallel to the interface is forced to be equal to the lattice constant of the substrate by *compressive strain*. At the same time the perpendicular lattice constant of the germanium will increase. Conversely, if a silicon epitaxial layer is grown on a relaxed germanium layer, the silicon layer experiences tensile strain in the direction parallel to the interface and there is a shrinkage of the lattice constant perpendicular to the interface [22].

In fact, with a mismatch of 4%, psuedomorphic growth of pure germanium on pure silicon is impossible for all but very thin germanium layers. Generally, after just a few monolayers of growth the strain build-up is such that misfit dislocations occur. This understanding of strain build-up leads to the concept of a *critical thickness*. Relatively thick layers of $Si_{0.9}Ge_{0.1}$ can be grown on silicon, but for high germanium compositions, the strain energy is increased and the critical thickness is much reduced. In general, with increasing germanium content (thickness or composition), structures are more prone to suffer from imperfect epitaxial growth.

The strain in the $Si_{1-x}Ge_x$ system is elastic and to relieve excessive strain in a $Si_{1-x}Ge_x$ layer, misfit dislocation arrays become incorporated at the interfaces. The geometry of misfit dislocations can be observed using an inspection technique such as transmission electron microscopy (*TEM*). $Si_{1-x}Ge_x$ dislocations propagate primarily by gliding on <111> planes from the interface so the dislocation geometry is defined by the intersection of these glide planes with the interface [22]. These intersections produce orthogonal, uniaxial, and hexagonal misfit dislocation arrays and, in the case of very high lattice-mismatch, dislocation glide occurs on other inclined planes, in so-called second slip processes [22]. For example, interfacial dislocation arrays with line directions along <010> have been observed at high strain *Si/Si_{1-x}Ge_x* <100> interface, corresponding to slippage on a <011> planes [22].

Matthews and *Blakeslee* have introduced a model for critical thickness by applying the concept of force balance to the propagation of misfit/threading dislocations [22]. The critical thickness can be calculated by combining linear elasticity theory and dislocation theory. The critical thickness for an uncapped strained layer is

$$2Gbh\varepsilon\cos\lambda\frac{(1+\nu)}{(1-\nu)} = Gb^2\frac{(1-\nu\cos^2\theta)}{4\pi(1-\nu)}ln\frac{\alpha h}{b}$$
(2.7)

where h is the epilayer thickness, G is the epilayer shear modulus, v is the epilayer Poisson ratio, ε is the lattice mismatch strain between the epitaxial layer and substrate, λ is the angle between the misfit dislocation Burgers vector magnitude b and a line in the interface drawn perpendicular to the dislocation line direction, and α is a factor which describes the energy of the dislocation core, where linear elasticity theory does not apply.

The left handed side of equation 2.7 is equal to F_{σ} and the right handed side is equal to F_T . The critical thickness (h_C) can be determined by finding the intersection of F_{σ} and F_T versus h plots [22]. Results from this analysis are shown in figure 2.6.

To obtain a dislocation-free $Si_{1-x}Ge_x$ layer, the critical thickness (h_c) and germanium compositions have to be considered carefully. The $Si_{1-x}Ge_x$ layer can be divided into three regimes: the first regime is characterized by strained layers with defects at large thicknesses. The second features non-equilibrium *metastable* states without defects at intermediate thickness. The last regime is characterized by using equilibrium layer that is strained and defect free at small thicknesses (no more than $10A^\circ$). For quantum-well infrared detectors, the metastable regime has to be used and the germanium composition, the thickness and the strain are chosen to control the band structure within devices [6, 22-25].



Figure 2.6: The critical thickness (h_c) versus Ge composition (x) in $Si_{l-x}Ge_x$. Matthews and Blakeslee [22].

2.4 Physical properties of Si_{1-x}Ge_x

Use of $Si_{1-x}Ge_x$ heterostructures widens the range of silicon based device applications and advances in thin film growth technology have led to the introduction of a variety of forms of $Si_{1-x}Ge_x$ in semiconductor devices. These devices include high-frequency heterojunction bipolar transistors (HBTs), Metal oxide semiconductor field effect transistors (MOSFETs) with high transconductance, high-mobility MODFETs and multiple quantum well photodetectors [15].

There are three important forms of $Si_{1-x}Ge_x$: unstrained $Si_{1-x}Ge_x$ bulk alloy grown by vertical pulling or horizontal boat methods [26, 27], strained-layer $Si_{1-x}Ge_x$ (where the $Si_{1-x}Ge_x$ layer is grown pseudomorphically on an Si substrate [3, 28, 29]), and relaxed-layer $Si_{1-x}Ge_x$, grown on Si substrate, much thicker than the critical thickness but with a dislocation structure embedded within the crystal [22] (Fig. 2.7).



Figure 2.7: Schematic representations of strained $Si_{1-x}Ge_x$ and relaxed $Si_{1-x}Ge_x$.

The bandgap of $Si_{1-x}Ge_x$ is between those of silicon and germanium and is dependant on the relative compositions of germanium and silicon. Measurement of the bandgap of $Si_{1-x}Ge_x$ has been carried out using several techniques including photoluminescence (*PL*) [24, 27, 30-33], photocurrent [34] and absorption [26, 35].

2.4.1 Unstrained Si_{1-x}Ge_x

The essential information for $Si_{1-x}Ge_x$ alloys is the bandgap energy. and this can be calculated (semi-empirically) [36] or measured by a range of techniques. Of these, photoluminescence and optical absorption measurements are most commonly used to determine the bandgaps of $Si_{1-x}Ge_x$ for different germanium contents.

The bandgap energy of unstrained $Si_{l-x}Ge_x$ for a range of germanium compositions from 28K through to room temperature have been determined by *Braunstein et al* [26]. By analysis of intrinsic absorption spectra, values were obtained for two extreme cases: the *Ge*-rich case and the *Si*-rich case. The *Si*-rich case is the most relevant to the samples which we have studied in this work. The ranges of bandgap energies for a series of $Si_{l-x}Ge_x$ alloys, according to *Braunstein*, are shown in figure 2.8.



Figure 2.8: The temperature dependence of bandgap energy for different *germanium* contents in $Si_{1-x}Ge_x$ alloys [26].

Another study of bandgap energies of $Si_{1-x}Ge_x$ alloys has been carried out using a photoluminescence technique [27]. For $Si_{1-x}Ge_x$ alloys, this technique provides not only the alloy bandgap energy but also a number of other crystal lattices activities such as the different modes of phonon-associated transitions. The unstrained approximation of the $Si_{1-x}Ge_x$ bandgap energy is determined by the energy of the peak corresponding to the *no-phonon transition* (NP) in the photoluminescence spectra (Fig. 2.9).



Figure 2.9: Near-bandgap photoluminescence spectra for bulk $Si_{1-x}Ge_x$ samples [27].

The photoluminescence spectra of $Si_{1-x}Ge_x$ alloys demonstrate the shift toward to lower energies with increasing germanium composition. The labels 'X' represent *excitonic transition processes*, and the superscripts represent characteristic transition details: NP, TO, TA and LA representing *no-phonon*, *transverse optical phonon*, *transverse acoustic phonon* and *longitudinal acoustic phonon*, respectively [37]. The subscripts express the distinguishable phonon bonds (*Ge-Ge*, *Si-Ge* or *Si-Si*). These photoluminescence measurements were performed at low temperatures so that the optical recombination, due to bound excitons, could be observed.

Excitons, the stable quasi-particles that are created as a result of the Coulombic attraction between electrons and holes, are commonly observed. Excitons can travel through the crystal as stable entities analogous to a hydrogen atom, and since they are charge-neutral, they can not directly contribute to current flow or photocurrent [38]. The annihilation of *free-excitons* can produce photons that can be observed as free-exciton features in photoluminescence spectra. *Bound-excitonic* features result from

recombination transitions between either the valence band or the conduction band and neutral donor or neutral acceptor energy levels respectively.

The no-phonon (*NP*) peaks, observed in figure 2.10, originate from bound-exciton recombinations, and the bandgap energy derived by this measurement, is known as the excitonic bandgap. The bandgap energy approximation for $Si_{1-x}Ge_x$ alloys can be considered for two distinct regions: the first is called the silicon-like region where silicon features of the energy band dominate, here the bandgap energy is measured for the X conduction band minimum. The second region is where the germanium features dominate, here the bandgap energy is measured for the L conduction band minimum. The excitonic band gap determined by photoluminescence data of *Weber et. al.* [27] is shown in figure 2.10.



Figure 2.10: The excitonic band gap (square) vs *Ge* composition of $Si_{1-x}Ge_x$ alloys [27]. The cross sign represents the experimental $Si_{1-x}Ge_x$ energy gap [26]. The solid lines are the excitonic band gap, obtained by least square procedure from equation 2.8 and 2.9.

In figure 2.10, the solid lines are plotted according to an analytical expression obtained by a least square fit of excitonic energy against germanium composition obtained by near-bandgap photoluminescence measurements at 4.2K [27]:

$$E_{\rm ex}^{(X)}(x) = 1.155 - 0.43x + 0.206x^2 \ eV \tag{2.8}$$

$$E_{gx}^{(L)}(x) = 2.010 - 1.270x \ eV \tag{2.9}$$

The bandgap energy, $E_{gx}^{(x)}$ in the silicon dominated region ($0 \le x < 0.85$) is provided by equation 2.8. While the bandgap energy, $E_{gx}^{(L)}$ in the germanium dominated region ($0.85 < x \le 1$) is provided by equation 2.9.

In both equation 2.8 and 2.9 the compositional dependence is only valid for bulk crystals. They cannot be directly applied to strained epitaxial layers. However, the bandgap energies serve as a useful reference point during material characterizations.

2.4.2 Excitonic behavior in Si and Si_{1-x}Ge_x

An exciton is an electron-hole pair, mutually bound by Coulombic attraction. The exciton can freely move through semiconductor crystals without contributing to the conductivity, and its electronic structure resembles that of a hydrogen atom or a quantized hydrogen state. Excitons are formed in very pure semiconductors at low temperatures. They are often found in epitaxial layers since epitaxy techniques commonly enable the growth of very pure crystals [39]. The excitonic behaviour in semiconductors can be observed by absorption measurement as a narrow peak in the absorption spectrum for direct bandgap materials and as steps at the absorption edge of indirect-gap semiconductors. The exciton level in band diagram can be illustrated as in figure 2.11.



Figure 2.11: The exciton levels within energy band diagram of semiconductors. The upward arrows represent the formation of electron-hole pairs into different exciton levels. The downward arrows represent exciton annihilation from the lowest free exciton level and bound state due to an impurity (E_{Bex}).

The many exciton levels represent ground and excited states of the exciton, and n_{∞} represents the continuum state and n_1 the ground state.

Then the emitted photon energy, is given by

$$h\upsilon = E_g - E_{ex} \tag{2.10}$$

for direct transitions and

$$h\upsilon = E_g - E_{ex} - E_p \tag{2.11}$$

for indirect transitions [38, 40].

Where E_{g} , is the bandgap energy, E_{ex} is the exciton binding energy, and E_{p} is the phonon energy.

The direct transition can be observed high energy as high intensity emission peak in SiGe alloy (excitonic energy gap) although it is forbidden in indirect semiconductors because the perfect translation symmetries of SiGe system are broken due to alloy disorder [30, 41, 42]. The indirect emission case can also be found as less intense peaks, which have smaller transition probability than the direct emission corresponding to different phonon energies.

In less pure material, bound exciton (*BE*) recombination dominates free exciton recombination. The bound exciton can be acceptor bound or donor bound. In case of the donor bound exciton, the hole is bound to a neutral donor, producing a positively charged excitonic ion. Therefore, the hole moves within the electrostatic field of this fixed dipole, travelling around this donor. An analogous system is created by acceptor bound electron. In *Si* and *SiGe* epitaxy, the *BE* emission is reported at very low temperature *PL* (2 – 6K), while the *free exciton* (*FE*) emission is observed at slight higher energies as the temperature is increased [23, 24, 27, 30, 31, 42, 43].

2.4.3 Strained Si/Si_{1-x}Ge_x layers

For the $Si/Si_{1-x}Ge_x$ system below the critical thickness, the built-in strain generates interesting modifications to the whole band energy structure. The heterostructure band alignment has been studied theoretically by several authors [36, 44]. The simplest derivations can be considered for the *Si/Ge* interface (Fig. 2.12)





In figure 2.12, a_{Si} and a_{Ge} are the lattice constants of Si and Ge, and the subscripts denote directions parallel (||) and perpendicular (\bot) to the interface, d is the average layer spacing between the two bulk materials. The two extreme cases are considered as: unstrained Si with strained Ge and strained Si with unstrained Ge. Alloys results can be obtained by interpolation, as shown in table 2.1.

<001>		$a_{\parallel}(A^{\circ})$	$a_{Si\perp}$ (A°)	a _{Ge⊥} (A°)
	unstrained. Si and strained Ge	5.43	5.43	5.82
	strained Si and strained Ge alloy	5.52	5.36	5.75
	strained Si and unstrained Ge	5.65	5.26	5.65

Table 2.1: Calculated lattice constants for the "super cell" [44].

From the table, the a_{\parallel} and a_{\perp} at the *Si/Ge* interface are compressed, compared with pure *Ge*. This directly affects the lattice potential at the interface. The band allignment is found, using *abinitio* calculations of the psedopotential (the "super cell") [44, 45]. The average potential wavefunctions for separated germainum and silicon atoms are resolved, and the shifted potential at the interface is shown in figure. 2.13.



Figure 2.13: The energy interface between unstrained Si and strained Ge [44].

The band calculation of unstrained *Si* and strained *Ge* is derived with l = 1 (l is angular momentum), as the reference potential. The crystal direction is <001>. The valence maximum of *Si* and *Ge* are found at 11.19eV and 10.88eV at $\Gamma_{25'}$ above average Si(\overline{V}_{Si}) and $Ge(\overline{V}_{Ge})$ potentials respectively. The potential difference $\Delta \overline{V}$ is 0.85eV. The discontinuity in the highest valence band ∇E_v is 0.84eV, or $\nabla E_{v,av} = 0.54eV$ for average valence band energy. In the conduction band, the discontinuity in the lowest is $\Delta E_c = 0.28eV$ and $\Delta E_{c,av} = 0.51eV$ for the average conduction band energy (going from *Si* to *Ge*). The energy gap difference is left undefined because this calculation does not agree with experiment [44].

The splitting of the valence and conduction bands in strained germanium is known as spin-orbit splitting. The valence electron levels of pure germanium and silicon located at p quantum number, having three-fold degeneration, and with spin included so six states become available.

Pure unstrained bulk silicon and germanium have small spin-orbit splitting of the valence band at Γ and is small enough to be neglected. With uniaxial strain, the spin -orbit splitting is 3/2:3/2, 3/2:1/2 and 1/2:1/2 (representing the total angular momentum quantum number $-j:m_j$). The conduction band is also affected by the same strain mechanism. The band splitting occurs at Δ (along the <100> and <010> directions) due to <001> or <110> strain. Strain along <111> does not result in splitting at Δ conduction band minima. These effects occur in *SiGe* alloy at germanium compositions from 0 to 85%. For high germanium content (>85%), the minimum in the conduction band occurs at *L*, which is more of a germanium-like band structure.

The splitting, created by $\langle 111 \rangle$ or $\langle 110 \rangle$ uniaxial strain, are shown in figure 2.14. The energy gap (indirect) is affected by the hydrostatic component of strain, which depends on the strain tensor and the potential deformation [34, 44, 46]. The hydrostatic strain can briefly be explained as: the unit cells have the fractional volume changing due to strain at both || and \perp direction to interface. The band gap narrowing for various Ge contents in strained $Si_{l-x}Ge_x$ alloy on Si < 001> substrates has been studied by People et al [28, 46] (Fig. 2.15)



Figure 2.14: The valence and conduction band splitting in strained $Si_{1-x}Ge_x$ on a Si < 001> substrate. The average valence and conduction band (at \triangle point) are represented by dashed line. The *L* represents the germanium-like conduction band when x > 0.85 [44]. The valence band spin-orbit splitting at various quantum numbers are represented by three lines with $(j:m_j)$ description.

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Figure 2.15: Comparison of fundamental (lowest energy) indirect energy gap of strained $Si_{1-x}Ge_x$ on Si <001> substrate with unstrained $Si_{1-x}Ge_x$ alloy [28, 46]. The two lines of the strained plots represent the possible range of energies that might result from valence band spin-orbit splitting.

In addition to the work of *People et al* [28] and *Van de Walle et al* [44], more recent work has proposed the energy band structure of strained *p*-type $Si_{1-x}Ge_x$ on Si < 001> substrates, calculated by solving 6×6 Hamiltonians [47]. This article describes the formation of the heavy-hole, light-hole and spin-off bands, and largely agreeing with *People et al* [28]. In addition, a 14-band *k.p*-formalism model has been presented by *El kurd, et al* [48], which provides a detailed understanding of both intersubband transitions and energy band formation.

Strained $Si/Si_{1-x}Ge_x$ layer energy gaps have been experimentally determined by several different methods. These include photoluminescence [49] and Raman spectroscopy [50]. The near-band gap photoluminescence of single strained pseudomorphic $Si_{1-x}Ge_x$ layers, sandwiched between layers of silicon, have been reported for the composition range 0.12 < x < 0.24 [30]. The excitonic bandgap at 4.2K is determined by the energy position of the no-phonon radiative recombination peak

in a manner similar to Weber et al [27] (Fig. 2.8 and 2.9). The empirical formula are obtained by a least-square fit for the excitonic bandgap (E_x^{S}) within strained $Si_{1-x}Ge_x$ on Si with x<0.24 [30];

$$E_X^{s}(x) = 1.155 - 0.874x + 0.376x^2$$
 eV (2.12)

Bandgap energy measurements can also be performed by photocurrent measurement techniques. These measurements reveal the optical absorption and the indirect bandgap features for strained $Si_{1-x}Ge_x$ layers, which has been presented by *Lang et al* [34] for germanium compositions in the range $0 \le x \le 0.7$, at 90K [34]. The variations of the bandgap of strained $Si_{1-x}Ge_x$ layers with ranges of germanium compositions and for different growth techniques have been experimentally and theoretically studied by several authors [33, 45, 51-54]. Here relatively small variations in values for different techniques and processing conditions acknowledges the fact that interfaces are rarely abrupt, compositions are rarely uniform and defect and impurity levels vary for different techniques and a precise measure of any of these quantities is not possible.

2.5 Optical Processes in Si/Si_{1-x}Ge_x

Silicon and germanium have indirect bandgaps so carrier transitions require phonons in order to conserve momentum as shown in figure 2.16. Furthermore, the diamond crystal structure of both elements also defines the optical process preferences through the space group selection rules [55]. The addition of germanium to silicon modifies the energy bands as described in the previous section. For the relaxed (unstrained) regime, the ordered crystal is disrupted due to the replacement of a large number of silicon atoms with germanium atoms within the silicon lattice. The wave functions of the electrons form into non-localized (band) states rather than localized (impurity) states. In addition, the disorder produces overlapping states in k-space, expanding the Bloch function in plane waves. Therefore, the initial and final states in the optical matrix are altered due to wave intermixing. This favors absorption and helps to overcome selection rule restrictions. This assumption leads to a temperatureindependent component of the absorption spectrum near the band edge. Although *Braunstein et al* [26] showed absorption spectra that are strongly temperaturedependent and concluded that the theory of phonon-assisted indirect transitions in disordered silicon germanium alloys is the same as pure germanium, and silicon evidence, supporting the overlapping effect, is demonstrated in other photoluminescence measurements [27, 56].



Figure 2.16: The indirect absorption diagram indicates the simple valence (E_v) and conduction (E_c) energy bands plotted against k-space. E_{ph} and E_{pn} are photon and phonon energies, respectively. The phonon-absorption and phonon-emission processes are represented by $E_{ph}-E_g+E_{pn}$ and $E_{ph}-E_g-E_{pn}$ respectively [39].

We have already discussed how bandgap reduction is observed in a strained layer due to the splitting of the valence and conduction bands (Fig 2.13 and 2.14). Now, if strain exists in both the $Si_{1-x}Ge_x$ and the silicon layers, *superlattices* are formed, leading to dramatic changes in both the electrical and the optical properties. The advantage of such a structure is that it can result in the broadening of the detectable wavelength range. Another possibility is the exploitation of the intraband absorptions in split bands to produce mid- and far-infrared devices [8, 10, 13, 57-62].
The indirect band structure requires phonon participation for the photo-excited vertical transition from valence to conduction bands. The general form of the *MacFarlane* 's one-phonon absorption model is:

$$\alpha_{abs} = A \left[\frac{(h\nu - E_g - \overline{E}_{pn})^2}{1 - exp(-\overline{E}_{pn} / kT)} + \frac{(h\nu - E_g + \overline{E}_{pn})^2}{exp(\overline{E}_{pn} / kT) - 1} \right]$$
(2.13)

Where \overline{E}_{pn} is the average energy of all participating phonons and A is an average weighting factor of the absorption coefficients of each phonon. The two square terms in represent the phonon emission probabilities with the phonon-generation-assisted process represented by the left-handed component of the bracketed term, and the phonon-absorption-assisted process is the term on the right. At low temperatures, the phonon density is small so the predominant effect is the phonon-emission process [40], while at room temperature both processes take place. This model has also been used for $Si_{l-x}Ge_x$ alloy [26]. The phonon energy is averaged from the most important phonon contributors seen in bulk silicon as well as $Si_{l-x}Ge_x$. These include *TA*, *LA*, *TO* and *LO* phonons [27, 30, 37, 41].

To derive absorption spectra, least-mean-square fitting techniques are applied to photocurrent spectra. Attention is focused on careful determination of the average phonon energy so that good agreement is found over the whole temperature range of interest. The typical value of the silicon bandgap is found to be in the range 1.08 to 1.12eV, while average phonon energies are in the range 40-60meV at room temperature [63]. More precise values for bandgap are often required, and have been described by:

$$E_{gSi} = E_{g(T=0K)} - \frac{\alpha_T \cdot T^2}{(T+\beta_T)} = E_{g(T=300K)} + \alpha_T \cdot \left[\frac{300^2}{(300+\beta_T)} - \frac{T^2}{(T+\beta_T)}\right]$$
(2.14)

Where, α_T and β_T are provided in table 2.2, the average phonon energy is given as 50meV [63]. The *A* parameter is 3200, and the best-fit E_{g300} of silicon is found to be 1.09eV when Eq. 2.13 is used for absorption modeling.

	Silicon	Germanium
$\alpha_T (meV/K)$	0.473	0.477
$\beta_T(K)$	636	235

Table 2.2: Coefficients for the temperature dependent bandgap model for both silicon and germanium [63].

Equation 2.14 can also be used to find the temperature dependence of the bandgap of a strained layer. In this case, linear interpolation can be used to supply parameters, α_r and β_r for compositions between pure silicon and pure germanium, although this is only accurate for $Si_{1-x}Ge_x$ if x is below 0.4 [63]. Thus, the dependence of the bandgap energy of strained $Si_{1-x}Ge_x$ on composition (x) and temperature is given by:

$$E_{g}(x) = E_{gSi-300K} + \alpha_{T} \cdot \left[\frac{300^{2}}{300 + \beta_{T}} - \frac{T^{2}}{T + \beta_{T}}\right] - 0.740 \cdot x$$
(2.15)

Values for the absorption coefficients for strained $Si_{l-x}Ge_x$ devices can be extracted using equation 2.13 and 2.15. The critical parameters such as the average phonon energy can be obtained by fitting to experimental data. Information covering the entire composition range (x) is not available so estimated values are made although this leads to errors, which can be reduced using certain correction procedures. *Polleux et al* [63] suggest that 9.2meV should be added to the E_{pn} fitting parameter to prevent discrepancies between the experimental determination of phonon energy and those provided by the preceding silicon analysis [63]. The example of this model is shown in figure 2.17.



Figure 2.17: The absorption coefficient of Si (inset) and $Si_{0.9}Ge_{0.1}$ at 300 and 77K obtained by the model described by equations 2.13-2.14.

2.6 Free-Carrier Absorption

Free-carriers are located at the conduction and valence band energies. These carriers can transfer to higher energy levels in the same valley by photon excitation. This transition can also conserve momentum by optical or acoustic phonon interactions or by impurity scattering [39]. Free-carrier absorption is observed at longer wavelengths as a monotonic increase in absorption with a wavelength dependence of the form λ^p , where *p* ranges from 1.5 to 3.5. The value *p* depends on the nature of the momentumconserving scattering. The free-carrier absorption can be expressed as

$$\alpha = \frac{Nq^2\lambda^2}{4\pi^2 m^* n_r c^3 \varepsilon_0} \left\langle \frac{l}{\tau} \right\rangle$$
(2.16)

where N is the free carrier concentration, n_r is the refractive index of the semiconductor, and $\left\langle \frac{l}{\tau} \right\rangle$ is the average value of the inverse of the relaxation time of the scattering process.

2.7 Si/SiGe Quantum Structures

The quantum well is an energy level surrounded by potential walls in either two or three dimensions. Compound systems such as *SiGe*, *InGaAs* and *AlGaAs* can readily realise quantum well structures using discontinuities provided by bandgap differences and strain effects. The *Si/SiGe* quantum well can be formed as single quantum well (*SQW*) or multiple quantum wells (*MQW*) (Fig. 2.18).

If the silicon germanium is strained then a *type-one* band structure is formed in which the conduction band minima exist in the same region as the valence band maxima (or *vice versa*). If both the silicon and the silicon germanium are strained, then the band alignment will be a *type-two* structure in which the maxima and minima do not align. To achieve quantum confinement, the size of the well (thickness) should be in a few angstrom A° (1×10⁻¹⁰m), while the barrier layer should be thick at (≥ 100 A°) for type one and a few monolayers thick for both well width and barrier for type two [64].



(a)

33



Figure 2.18: Types of *Si/SiGe* quantum well band structures (a) a double quantum well, type-one structure, (b) a multi-quantum well type two structure.

2.7.1 Quantum subbands

Two types of $Si_{1-x}Ge_x$ quantum structure are considered in this report: the quantum well and the quantum dot. Quantum wells can be created by growing thin epitxial layers of strained $Si_{1-x}Ge_x$ between layers of silicon. Quantum dots can be formed by exploiting self-assembly mechanisms by applying appropriate conditions during the deposition of small volumes of germanium on silicon. Schematic diagrams of these quantum structures are presented in figure 2.19.



Figure 2.19: Schematic representations of quantum structues (a) quantum well, and (b) quantum dots [64].

The Schrödinger equation is used to solve the eigenfunctions and eigenvalues within quantum structures. The difference between quantum well and quantum dot structures concern electron motion inside the structure. The boundary conditions of well and dot structures are presented as equation 2.17.

$$V(z) = \begin{cases} 0 & for |z| \leq L/2 \\ V_b & for |z| \geq L/2 \end{cases}$$
(2.17a)

$$V(x, y, z) = \begin{cases} 0 & inside & the box \\ +\infty & outside & the box \end{cases}$$
(2.17b)

Equation 2.17a represents the boundary conditions for the quantum well for the potential in the z direction. The quantum dot boundary conditions are presented in equation 2.17b. Full descriptions of the electron wave functions and energy levels of both regimes are essential for the understanding of quantum structure problems. The wave function and energy levels of a quantum well are presented in equation 2.18a and 2.18b.

$$\psi(z) = \begin{cases} C\cos k_{\omega} z & for|z| \leq L/2\\ Ae^{\mp k_b(z \mp L/2)} & for|z| \geq L/2 \end{cases}$$
(2.18a)

$$E_n = \frac{\hbar^2 \pi^2 n^2}{2m^* L^2}, \quad n = 1, 2, 3....$$
 (2.18b)

Where $k_{\omega} = \sqrt{2m^* \varepsilon / \hbar^2}$ is the wave-vector inside the well, A and C are arbitrary constants, and $k_b = \sqrt{-2m^*(\varepsilon - V_b)/\hbar^2}$ is the wave-vector outside the well. The first condition of equation 2.18a is the case where the electron wave function is inside the well, while the second condition is for the wavefunction outside the well. Equation 2.18b is the energy level relating to an infinitely deep well.

The first energy level of a shallow well, which may have only one level, is $E_1 \approx m^* L^2 V_b^2 / 2\hbar^2$, where m^* is an effective mass, L is the well width, and V_b is the well potential, and is alternatively called the well depth.

The solution to the Schrodinger equation with the quantum dot boundary conditions (described in equation 2.17b), that confines electrons into a box described by $0 \le x \le L_x$, $0 \le y \le L_y$, and $0 \le z \le L_z$, is given by:

$$\psi_{nl,n2,n3}(x,y,z) = \sqrt{\frac{8}{L_x L_y L_z}} \cdot \sin \frac{\pi x n_l}{L_x} \cdot \sin \frac{\pi y n_2}{L_y} \cdot \sin \frac{\pi z n_3}{L_z}$$
(2.19a)

$$E_{nl,n2,n3} = \frac{\hbar^2 \pi^2}{2m^*} \cdot \left(\frac{n_l^2}{L_x^2} + \frac{n_2^2}{L_y^2} + \frac{n_3^2}{L_z^2}\right)$$
(2.19b)

where n_1 , n_2 , $n_3 = 1$, 2, 3 are three discrete quantum numbers, resulting directly from the existence of three directions of quantization. Therefore, for a quantum dot, there are discrete-energy levels and wave functions localized in all three dimensions. All energies are generally different (or non-degenerate). However, if two or all dimensions are equal, degeneracy will occur: twofold degeneracy if two dimensions are equal or six-fold degeneracy for a cube [64]. The discrete spectrum and the lack of free-electron propagation distinguishes the quantum dot from the quantum well [61].

The essential parameters for these quantum structure models are effective mass and the structure dimensions. The electron and hole effective masses of $Si_{1-x}Ge_x$ have been reported in several publications [65-68], which generally both heavy-hole and light-hole effective masses are reported.

The number of dimensions in the quantum structure is also important as this affects the bound state approximation. The dimensional dependence of quantum structure bound states involves the vertical shift of bound state with size. In the simplest case, a quantum well with only one bound state, the bound state will shift closer to the silicon valence band with a very thin well width. The state shifts closer to the germanium or silicon germanium valence band as the well width increases. The electronic properties of real quantum structures are theoretically studied by several authors [52, 53, 61, 69-73].

2.7.2 Quantum well absorption

The absorption mechanisms in discrete quantum structures have two basic differences: firstly, material non-uniformities (compositions and widths) can cause specific changes in the features of the interaction of light, including light propagation, emission and absorption. Secondly, as we have seen, the electrons in quantum structures have different energy spectra, compared to bulk materials [64]. Quantum well absorption features demonstrate peaks, corresponding to excitons confined at different subbands in the quantum well [39]. The sharp peaks or steps are observed in absorption spectra close to the band-edge and shifted towards shorter wavelength (Fig. 2.20). The interband absorption transition within quantum wells are from hole subbands in valence band quantum wells to the electron subbands in the conduction band quantum wells (Fig.2.20)



Figure 2.20: The interband absorption of different subbands, in a type one lattice matched *InGaAs/InAlAs MQW* at 300K [39]. The inset exhibits the band diagram with the observed transitions, represented by arrows. The *lh* and *hh* represent the light-hole

and heavy-hole non-degenerate states, while c is a subband in the conduction band. The number description represents the wavevector numbers of each energy level.

The interband phototransitions have to obey the "selection rules": the transition of electrons or holes must conserve energy and momentum, which means that the wavevector (\vec{k}) of initial state (\vec{k}_i) and final state (\vec{k}_f) must be such that $\vec{k}_i = \vec{k}_f$; the energy difference between these states must equal to the external excitation energy [64]. Therefore, the transition will only occur if these two conditions are met. However, the transition can occur at different wave vector position but another particle such as a phonon must participate in order to conserve momentum. For quantum structures, the same concept is applied (Fig. 2.21) each subband number in a well serves as the wave vector of a subband eigenfunction. From the selection rule, the photo-transition is allowed as transitions between the same subband numbers (but different functions) are allowed, while the transition is forbidden for different subband numbers.



Figure 2.21: The subband dispersions in type one quantum well conduction and valence bands. The subband number $(E_{cl, 2...} \text{ and } E_{vl, 2...})$ represent the wavevector of a subband at various k space. The inset shows band diagram of type one quantum well.

In *Si/SiGe* type one structures, quantum wells are not generally formed in the conduction band [22, 29, 69, 74].

Intersubband transitions within quantum structures are unlikely to occur, due to the selection rules. However, they can be induced with the assistence of particles such as phonons, impurities and other crystal imperfections. There are two types of these transitions: the transition between subbands in a well and the transition from a subband to extended electron states (continuum states) (Fig. 2.22).



Figure 2.22: The intersubband transition. (a) is the transition between subbands in a well in-plane of the quantum well structure. (b) is the transition between subband and unconfined extended states [64].

If the x-y axis is the plane of the quantum well layer, a carrier is not characterized by the z component of the momentum in the heterostructure. Therefore, an in-plane wavevector $(\vec{k}_{||} = \{k_x k_y\})$ of initial and final states can be $(\vec{k}_{||i} - \vec{k}_{||f} \approx 0)$. The energy and momentum conservation are maintained and can occur without other particles, when the excitation energy corresponds to $\hbar\omega = E_f(\vec{k}_{||f}) - E_i(\vec{k}_{||i})$. In the case of transition to electron unconfined extended state, the same concept as the intersubband case is applied.

The major contribution to intersubband absorption is the subband population in quantum wells. Population of the lowest subband can be achieved by impurity doping

and selective doping with doped quantum wells and undoped barriers are used in many photodetector designs [22, 29, 69, 74]. The energy difference between subband in the well and unconfined extended state out of the well is small. It can be ranged from few hundred to a few tens of meV, corresponding to the far infrared range ($10\mu m$ and above).

2.8 Si/Si_{1-x}Ge_x Devices

 $Si/Si_{1-x}Ge_x$ photodetectors can detect 1.3 and 1.55µm, depending on the Ge content [5, 6, 9]. The major limitation of the $Si/Si_{1-x}Ge_x$ device is the quality of $Si_{1-x}Ge_x$ epitaxy, which is a direct consequence of the issues of critical thickness and stress driven morphological issues. Operating within these limitations, two types of $Si_{1-x}Ge_x$ device are commonly discussed, those based on quantum well structures, and those based on quantum dot structures. These structures are typically fabricated within the intrinsic layers of *p-i-n* photodiodes and related devices, forming quantum well infrared photodetectors (*QWIPs*) and quantum dot infrared photodetectors (*QDIPs*) (Fig. 2.23). The quantum dot structure can allow high concentrations of pure germanium nanostructures in detectors, extending sensitivity to wavelengths of upto 2µm.



Figure 2.23: (a) a *QWIP* device and (b) a *QDIP* device.

Several types of SiGe photodetector have been reported, p-i-n photodetectors (PDs), Avalanche photodiodes (APDs), wave-guide detectors and Single photon avalanche diodes (SPADs) (Fig. 2.24). The performance of these devices is generally much less than III-V based detectors because of the indirect silicon bandgap. However, some silicon-based designs can perform better than III-V devices, single photon detection for example uses a photon to trigger an avalanche breakdown of a diode biased just above breakdown voltage [11], though this success is more to do with the reliability of silicon device technology rather than the optical properties of silicon.



Figure 2.24: (a) waveguide and (b) avalanche detectors.

A few state-of-the-art devices are important to consider in the context of this work. A waveguide photodetector with *Ge/Si* self-assembled islands, has been described by *El Kurdi et al* [75] in which 20 layers of undoped *Ge/Si* islands were grown by high-pressure *CVD*, and within the *i*-region of *p-i-n* junction diode similar to the device depicted in figure 2.24b. The device was found to detect upto wavelengths of 1.5 μ m at 300K (Fig. 2.25).



Figure 2.25: The extended responsivity of a quantum dot *p-i-n* photodetector, *El Kurdi et al* [75].

Wang et Al [76] have also produced quantum dots in the *i*-region a p-*i*-n junction. Ten layers of undoped *Si/Ge* were produced by *MBE*. The photocurrent at 300K shows two distinct peaks at around 1100 and 1400nm wavelengths (Fig. 2.26).



Figure 2.26: The extended photocurrent, of a quantum dot *p-i-n* photodetector, showing two distinct features (*Wang et al* [76])

The *Daimler-Benz Research Centre* have produced active *Si/SiGe* regions that seek to maximise the germanium content of thick quantum wells (*Presting et al* [8]). These devices were fabricated using *MBE* techniques to achieve this high germanium content (Fig. 2.27).



Figure 2.27: The epitaxial configurations of *Presting et al* [8].

Devices numbered (B2804 and B2805) were waveguide detectors containing strain symmetrized $Si_{6nm}Ge_{4nm}$ superlattices. B2804 has a $Si_{0.5}Ge_{0.5}$ surfactant buffer, while B2805 has a step-graded buffer. The waveguide channel is p-type $Si_{0.6}Ge_{0.4}$ of 400 and 250nm thickness, respectively. B2817 has double quantum well structures on silicon consisting of Ge/Si/Ge with a 380nm thick n-type SiGe_{0.05} layer on top. The photocurrent spectra for these devices are shown in figure 2.28.



Figure 2.28: The normalized photocurrent of the photodetectors of *Presting et al* [8].

It is clear that Si/Ge quantum well and quantum dot structures can be used within silicon photodetectors to extend sensitivity into the near-infrared and the *communications wavelengths*. However, reproducible and reliable fabrication of these devices remains a significant challenge. The *LPCVD* sytems, in Southampton have been found to produce high quality $Si_{1-x}Ge_x$ epitaxy for use in Heterostructure Bipolar Transistors (*HBTs*) and vertical *MOSFET* for several years [15]. This work aims to investigate if these unique *LPCVD* systems can produce *Si/SiGe* photodetectors with extended infra-red sensitivity by exploiting new growth regimes.

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Chapter 3

The Si/SiGe epitaxy experiment

From the information gathered in the literature survey (chapter 2), it is clear that we can use chemical vapour deposition to create Si/SiGe quantum well and quantum dot structures, and these structures can be used to enhance the infrared absorption of photodetectors. The first objective of our experiments is to characterise the *CVD* growth of *SiGe* layers and calibrate growth for *SiGe* layer and quantum dot thickness (*W*) and composition (*x*) (Fig.3.1).



Figure 3.1: Features to be controlled and optimised by $Si/Si_{1-x}Ge_x$ growth experiments.

This chapter details the Si and SiGe low-pressure chemical vapour deposition (*LPCVD*) epitaxial growth, carried out during this work. These include experiments designed to optimise, characterise and calibrate both Si and SiGe growth regimes and includes the deposition of pure silicon, and undoped and doped $Si_{1-x}Ge_x$ quantum well structures. Physical characterization of materials has been performed using transmission electron microscopy (*TEM*), scanning electron microscopy (*SEM*) and

Secondary ion mass spectrometry (SIMS). In chapter 4 we describe the optical properties of the materials based on characterisations by photoluminescence (PL) and absorption spectroscopy.

3.1 The LPCVD System

For a number of years Southampton University has built expertise in the deposition of silicon and silicon germanium using low-pressure chemical vapour deposition (LPCVD) [77]. The epitaxy systems and processes have been in continual development to allow a broad range of capabilities including undoped growth at a range of temperatures [77], in-situ silicon doping [78], the growth of *Si/SiGe* heterostructures [77], germanium quantum dots [79, 80], *SiGe* virtual substrates and a number of selective growth regimes [77]. These epitaxy systems have provided a number of innovative electronic devices and fabrication processes including heterojunction bipolar transistors (HBTS) [81-83], high electron mobility *CMOS* [15, 84], vertical *CMOS* [15, 85], and lateral *HBTs* [86]. These applications indicated that the epitaxy systems could be exploited to produce silicon germanium quantum structures. The challenge of this work was the development of the Southampton *LPCVD* systems to produce *Si/SiGe* quantum well devices to rival those, produce elsewhere by molecular beam epitaxy techniques.

The LPCVD system used consists of three chambers, the *load-lock* and two *deposition chambers*. These chambers are connected by *gate valves*, with two knife-edge copper gaskets, providing vacuum seals between the chambers. The deposition chambers are surrounded by water cooled walls and contain graphite heaters mounted at the top of each chamber. All uncooled internal components are made out of ultra-high vacuum (*UHV*) compatible materials such as quartz or molybdenum. The vacuum pumping in the growth chambers and the load-lock is of the roots/dry-pump combination and can provide a base pressure of 1 mTorr. The typical growth pressure ranges from 30mTorr to 1Torr and is controlled by a throttle valve, placed downstream of the chamber and operated in a closed-loop configuration by a capacitance meter. This allows pressure and flow to be adjusted independently within the limits of the gas delivery and the pumping systems.



Wafer Platen carrier and rotate

Figure 3.2: Schematic diagram of the *LPCVD* system [87]. The inset figure represents a birds-eye view of the system.

The load-lock is primarily used to reduce the transfer of contaminants, especially water and oxygen, into the growth chamber after opening the system to the environment (typically to load a wafer substrate). By using a load-lock, the deposition chambers are never directly exposed to atmospheric pressure. This is an essential feature of silicon *CVD* systems as water or oxygen contamination in the growth chamber greatly reduces the quality of epitaxial growth [87]. The load-lock plays a significant role in successful epitaxy even then machine *conditioning* is always an important issue. In general, after any period of downtime (due to machine maintenance or a weekend) a number of high temperature growths are required to "*condition*" the chamber. If during extensive maintenance a growth chamber has been exposed to the atmosphere for an extended period then machine conditioning can take a number of weeks. These types of concerns extend to the use of dopants and

germanium. Auto-doping [87] is a common difficulty in silicon CVD after any *in-situ* doped growth or alloy growth. Therefore, re-conditioning will be required in order to return a chamber to low intrinsic silicon growth. This is because chamber surfaces will be contaminated with doping atoms and gases. For this reason, there are often two chambers placed around a single load-lock. This allows transfer of wafers from *n*-type to intrinsic or *p*-type chambers without the need to expose the load-lock or the growth wafer to atmosphere.

Given these complex issues and the expensive equipment, the maintenance and operation of *LPCVD* equipment is the responsibility of dedicated and experienced engineers. Even then, the deposition of a consistent series of epitaxial structures is a considerable challenge, and success will largely depend on the condition of the apparatus, the proximity to maintenance work and the recent growth history. In a facility involving many types of epitaxy requirements, the skilful engineer will seek to optimise the order in which they carry out work. Calibration runs can also be conditioning runs, while low specification batches (such as polysilicon growth) could be quickly performed after maintenance, and more complex or challenging batches have to wait for often elusive periods of high performance conditions.

Prior to any deposition, a wafer is loaded into the deposition chamber. The load-lock is *vented* to atmosphere (often after a purging cycle), and then the load-gate can be safely opened. The wafer, held by a platen, is placed onto a transfer mechanism (the *robot*), and the gate valve is closed (sealed by a built-in O-ring). The load-lock is then pumped by a turbomolecular pump that is supported by a rotary pump. Operation of the load-lock pumping system begins with the rotary pump, being used until the pressure in the load-lock is reduced to 1mTorr and then the turbo pump takes over. After around twenty minutes, the pressure in the load-lock is lower than the growth chamber can be opened. The higher pressure of the chamber minimizes any possible transfer of residual water and oxygen from load-lock to chamber during the loading process but adds a additional safety concern: given a small likelihood of deposition gases reaching the load-lock. Once, the chamber gate-valve has been

opened the wafer transfer *robot*, allowing the substrate wafer and platen to be transferred, under vacuum, from the load-lock to the growth chamber.

The substrate and platen is heated by a 10 inches diameter graphite meander, mounted on the top flange of the chamber. The robot can easily place the wafer and the platen into a suspended position within the heater assembly. Various sizes of wafer can be accommodated (up to 8 inch diameter) by changing the quartz platen upon which the wafers are carried. The substrate and platen are held in a rotation stage and routinely rotated during growth to enhance deposition uniformity. To minimize possible carbon contamination from the graphite heater, a new heater element is coated with silicon at high temperature before any device layer is grown.

The gas sources most commonly used are silane, germane, arsine, phosphine, diborane and hydrogen. These gas species are filtered and purified close to the point of entry into the deposition chamber. The source gas concentrations are 100% hydrogen, 100% silane, 10% germane in hydrogen, 100 volumes per million (vpm) arsine in argon, 1000 vpm phosphine in argon, and 1000 vpm diborane in argon. The gas flow rate for each gas is independently determined using *mass flow controllers* (*MFCs*). The gas supply manifold is designed to minimize dead volume and contain identical lengthed gas lines for each supply. This allows fast switching of composition and facilitates sharp transitions in doping and composition.

All the growth elements in our system are fully controlled by computer with specialist interface software. This provides huge advantage for reproduction, and all of the growth parameters for each growth are recorded as growth recipes and the growth recipes can govern epitaxy sequences from start to finish. There is no *in-situ* monitoring, however, all growth parameters such as substrate temperature, gas precursor flow, chamber pressure and electronic system are monitored and displayed on control panels. In the case of abnormal measurements, warning indicators allow for automatically or manually activated emergency stops under conditions that allow the pressure and substrate temperature to safely return to ambient.

3.2 Growth Procedures

The condition of surface is essential for epitaxy success, and both *ex* and *in-situ* cleaning procedures are used in this work. *RCA* cleaning [87] is used to remove contaminated particles such as native oxide, metallics and organics. First, wafers are immersed in the solution of $NH_4OH:H_2O_2:H_2O$ 1:1:5 at 72°C for 10mins, and then rinsed in *DI* water. Then, wafers are immersed in a solution of $HCL:H_2O_2:H_2O$ 1:1:6 for 10mins at 72°C, and then rinsed in *DI* water for 15 mins. Then, they are spun dry in a warm nitrogen atmosphere.

The *in-situ* wafer preparation in the growth chamber consists of substrate heating at 900° C for 5 to 10 minutes in order to desorb the thin native oxide, produced after the *RCA* clean. The heater current is then decreased to the growth temperature. The time it takes the substrate to cool down to a given temperature from the oxide desorption temperature has been measured using the optical pyrometer in order to minimize the time between oxide desorption and the initiation of epitaxial growth.

3.3 Characterisation equipment

The growth characterization, used in this work for impurities and defect investigation, consists of three main techniques, secondary ion mass spectroscopy (*SIMS*), tunnelling electron microscopy (*TEM*) and scanning electron microscopy (*SEM*).

3.3.1 SIMS

This technique is one of the most powerful and versatile techniques for measuring concentrations of impurities in solids. It has good detection sensitivity for many elements. It is not as sensitive as some electrical or optical methods, but it can provide composition and impurity distributions as a function of depth from the surface. As such it is ideal for ion implantation doping profile investigation and epitaxial growth characterisations.



Figure 3.3: Schematic of the SIMS technique [38].

During a *SIMS* measurement a primary ion is accelerated by a field and impinges the sample and atoms from the sample are sputtered. The ejected ions, *secondary* ions, are detected by a mass spectrometer, and they are recorded as a mass spectrum, count, or profile, according to the secondary ion mass/charge ratio (Fig.3.3). The incident ions lose their energy by momentum transfer as they land within solid, and they displace atoms within the sample. An atom near the sample surface must receive sufficient energy from incident ions to be ejected, which requires around 10 to 20keV accelerating voltage, and values in this range are typically used in *SIMS*. The *sputtering yield* is the average number of atoms sputtered per incident primary ion. This yield depends on the sample material, its crystallographic orientation, and the nature, energy and incidence angle of the primary ions. Different sputtering yields occur for different elements in the sample. The primary ion species commonly used in *SIMS*, are Cs^+ , O_2^+ , O_- and Ar^+ , which give yields ranging from 1 to 20 at 1 to 20keV.

SIMS measures the total impurity concentration, not the active impurity concentration. Therefore, sometime *SIMS* results may not be consistent with electrical and optical techniques. Additionally, *secondary* ion scattering can be affected by the surface roughness of the sample, and this can affect the accuracy.

3.3.2 TEM

TEM provides highly magnified sample microscopy. The magnification of *TEM* is higher than *SEM* by up to 1000 times, but based on a similar concept. Its resolution is typically in the range 1.8 to $2A^{\circ}$, and this is enough to inspect nanostructure details. Additionally, there are some improvements that allow increases in machine functionality such as electron energy loss detectors and light and *X*-ray detectors. In principle, *TEM* arrangements are similar to those of an optical microscope. They consist of a series of lens, with very high resolution and magnification as shown in figure 3.4.

If we consider an amorphous sample consisting of atoms A and atoms B, where $Z_B > Z_A$ (Z is atomic number). Electrons have stronger scattering in atoms B than atoms A. Strongly scattered electrons are not transmitted by the image-forming lens and do not reach the fluorescent screen, while the more weakly scattered electrons do. Therefore, the heavier elements do not appear on the screen. This implies that image brightness is determined by the intensity of electrons transmitted through the sample that pass into the image forming lenses. As a consequence, for example, the *TEM* image of a region of silicon is brighter than a region of germanium.

The *TEM* technique has very high resolution and provides a very highly magnified image. It is a very important tool for inspection of the uniformity of crystalline or amorphous thin layers. The contrast of images identifies different material in compound layers and structural defects. The main difficulty with *TEM* is the requirement for thin sample preparation and this is a time-consuming process.

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Figure 3.4: The schematic of a transmission electron microscope [38].

3.3.3 SEM

The scanning electron microscope is widely used for device inspection in order to monitor the topographies and connections obtained by deposition or etching processes or lithographic patterning. Magnification of the *Joule JSM-6500-F*, used in this work, can reach up to 500000X with 1.5nm resolution with an acceleration energy of 15kV. The *SEM* needs no extra sample preparation compared with the *TEM* technique.

During scanning electron microscopy the primary electron beams from an electron gun impinge on the sample, causing a secondary electron to be emitted from the sample. This secondary electron can be detected in the microscope chamber. The detector signal can be correlated with the electron beam raster to generate an intensity image on a monitor. The scattering between electrons and atoms is crucial for image sensitivity. For low atomic number (Z) samples, most electrons penetrate deep into the sample and are absorbed, while for large atomic number samples, the electron scattering occurs near to the surface and a large fraction of the incident electrons are backscattered [38]. Therefore, for a *Si/SiGe* sample an *SEM* image is inverted compared to the *TEM* technique and silicon is dark, while *SiGe* layers are brighter. Auxiliary detectors can be proved inside an *SEM* sample chamber for additional material analysis such as *X-ray* and back-scattering detectors.

3.4 Epitaxial growth experiments

At the beginning of this project, the epitaxial system was well understood, and operating conditions were well understood for a range of temperatures, pressures and gas flows. In particular, the most appropriate operating *windows* were well established for the growth of *Si/SiGe HBT* structures. The first objective of this work was to establish the optimum operating conditions for the deposition of *Si/SiGe* quantum well structures. In particular, it was felt that this new challenge would require relatively slow deposition rates as this would allow the maximum control of both composition and well thickness, and it would also allow for sharper junctions.

As we have seen in chapter 2, *CVD* machines generally operate in either a temperature controlled or a mass-transport controlled regime. Temperature controlled *CVD* systems are usually low pressure systems, and it is the substrate temperature that determines the growth rate. Mass-transport systems are usually operated at a higher pressure (often atmospheric), and it is the pressure of reactant species at the substrate that determines the growth rate. Interestingly, the *LPCVD* systems, used in Southampton, can operate in both regimes depending on the substrate temperature. At high temperatures, the mass transport is important, flow-rates and chamber pressure can be used to modify growth rates, but growth uniformity becomes increasingly challenging. At low temperatures, it is the temperature that can be most readily used to modify growth rate although maintaining epitaxial growth temperatures, the chamber pressure, hydrogen dilution, flow-rates and temperature can influence the growth rate and composition.

To achieve the lowest practical growth rates, it is clear that chamber pressure, flowrates and temperature could be reduced, but attention has to be paid to uniformity, epitaxial quality, and the operating ranges of the mass-flow controllers and the pressure control. While, it is easy to think that the obvious starting point for any new experiments might be a thorough study of all of the available parameter space, cost and time implications, dictating that a minimum number of calibration growths should be used. Thus, since temperature is the key parameter, the first experiment was designed to examine growth in the relatively low temperature range 650°C through to 800°C.

3.5 Growth Rate as a function of temperature

Five <100> p-type 17-33cm² silicon *half-masks* were prepared. These oxide half-masks were fabricated by wet oxidation at 1000°C to produce 600nm thickness across a whole wafer. Then, wet etching is performed using *HF* at 25°C in order to remove half of the oxide layer.

During growth the growth pressure was fixed at 0.5 Torr. The substrate temperature was set to 650, 700, 750, 800 and 800°C for wafers 1, 2, 3, 4 and 5 respectively; wafers 4 and 5 were grown at the same temperature but different target thickness. The target epitaxial layer thickness was 300nm, except for wafer no.4, for which the target thickness was 20nm. This would allow us to look at any possible starting transients during growth. The flow rate of silane with hydrogen carrier gas was 120:40sccm.

The oxide half-masks were used to facilitate surface and thickness inspection (Fig. 3.5). The step feature appears in *SEM* images; the higher step is the polysilicon, deposited during growth and appearing as a rough surface. The smoother surface occurs on the exposed silicon, representing homogeneous silicon epitaxy. The oxide layer has contrast image comparing with the silicon material in *SEM*. Therefore, the mark at the bottom of oxide mask is the substrate surface which the *Si* epitaxy can be measured. The poly-*Si* layer can also be measured. The height between top and bottom is measured (Δh), and by subtracting the oxide thickness (600nm) include poly *Si*. The epitaxial thickness can be approximated. The surface features of the 5 deposition wafers are shown in figure 3.6.



Figure 3.5: The profile of the half-mask, used to determine deposition thickness





Figure 3.6: The surface of silicon epitaxial layers

Surface roughness is seen to reduce with increasing growth temperature, and very smooth surfaces are seen from 750°C and upwards. The silicon growth rate at various growth temperatures was calculated from the thickness and growth time (Fig. 3.7).





Figure 3.7 indicates a similar trend to earlier work at Southampton [87]. The error bars represent the uncertainty in the growth rate determination, which is about

 \pm 10%. The experimental growth rate (*GR*) is lower than ref [87, 88], this may reflect slightly different machine geometry.

At temperatures below 750°C, the deposition is in a temperature controlled (surface reaction) regime, where the growth rate obeys exponential law: $GR \sim exp[-E_a/kT]$ which E_a is activation energy, k is boltzmann constant and T is growth temperature [16]. The activation energy, derived from figure 3.7, is about 1.8eV, which is slightly higher than the published vwlue of 1.5eV [16]. At temperatures above 750°C the growth rate is reasonably constant with temperature, which is the mass-flow controlled regime.

The single point at 800° C is the growth rate obtained from the thin silicon sample (k2517-4). The data indicates a slightly higher rate than the thick sample, and does not provide conclusive evidence of a significant growth transient at the beginning of a deposition.

The silicon growth rates also provide the basic growth data for the $Si_{1-x}Ge_x$ epitaxy layer designs. From previous experience in Southampton, we know that for the same conditions, the growth rate for *SiGe* will be similar to the growth rate of *Si* as long as the fraction of *Ge* is less than 30% [87]. However, when considering the growth of *SiGe* quantum wells, we have to consider how different conditions will affect the composition and how the very short growth times required for quantum wells (of the order of a few seconds), which might be more sensitive to any switching transients. Rather than carrying out extensive calibration runs for *SiGe* composition and thickness, it was decided that the most sensible approach would be to directly produce quantum well structures.

3.6 The first generation of Si/Si_{1-x}Ge_x multilayer structures

The first attempts to grow $Si/Si_{1-x}Ge_x$ were in a two wafer batch (k2452). The wafers were <100> p-type 17-33cm² silicon. The 100nm thick undoped silicon buffer was conventionally grown before any SiGe growth, and then ten repeated layers of

undoped Si (50nm thick) and undoped $Si_{l-x}Ge_x$ (5nm thick) with a 100nm thick undoped silicon capping layer, as shown in figure 3.8.

The germanium contents were designed to be x=0.06 and x=0.2 for wafers k2452-1and -2, respectively. These germanium compositions were selected to investigate the lower and upper boundaries of germanium incorporation. A substrate temperature of 810C and 0.5Torr pressure was used. The hydrogen:silane gas ratio for Si epitaxy was 120:40sccm, and the silane:germane ratio for SiGe layer was 40:6 and 40:20sccm for k2452-1 and -2 respectively. The growth time was 5 sec for each SiGe layer in both samples.



Figure 3.8: The Si/Si_{1-x}Ge_x multi-layer configuration.

After growth the compositions and thicknesses were measured by secondary ion mass spectrometry (*SIMS*), the cross-section tunnelling electron microscope (*XTEM*) is shown in figure 3.9 and 3.10.



Figure 3.9: SIMS data for sample k2452-1.

The *SIMS* data present the *Ge* concentration versus depth from the surface of the sample. Therefore, the thickness and concentration can be estimated. The *Ge* concentration of *SiGe* layer is determined by the peak in *SIMS* data. For thickness, *FWHM* are preferred as this can readily provide a *SiGe* thickness in a reliable manner. However, this thickness can only be approximate. For more accuracy *TEM* is required.

Figure 3.9 clearly shows the ten distinct $Si_{l-x}Ge_x$ peaks with maximum germanium content (x) of 0.05. At the surface of the sample, they appear to be an additional germanium peak. This is likely to be an effect of residual *Ge* ions detection in instrument vacuum chamber. In-between the first two quantum well peaks, the germanium content drops to less that 0.01%, indicating excellent *SIMS* resolution. We note that this level increases as we move deeper into the sample, which is most likely due to reducing *SIMS* resolution rather than increased diffusion since the first deposited quantum wells do not experience significantly longer anneal times. The excellent Ge consistency is observed at $4.5\pm1.6\%$, while the quantum well thickness (*FWHM*) is found to be 10.5 ± 0.71 nm. In general, the uniformity of the quantum well widths, maximum germanium contents and minimum germanium contents are greatly

encouraging. The stability and reproducibility of the deposition rates for silicon and germanium within the structure is much better than might have been expected.



Figure 3.10: XTEM data for sample k2452-1.

Figure 3.10 shows 7 (or perhaps 8) of the ten SiGe quantum wells. The silicon germanium is darker on *TEM* micrographs because strong electron scattering occurs in heavy material. We see sharp transitions from SiGe to Si, perhaps, even sharper than is indicated by *SIMS*. Additionally, there are no network dislocations, occurring at the interface of the different materials. Although the resolution of this *XTEM* is insufficient to provide an accurate measure of thickness, which is observed as 10 ± 0.71 nm, we can see that the quantum well is reasonably agreed with those determined by *SIMS*.



Figure 3.11: SIMS data for sample k2452-2.

Many of the features, seen in figure 3.9 (sample k2452-1), are repeated in figure 3.11 (sample k2452-2), and once again we see ten distinct peaks. This time the peak germanium content (x) is potentially increased as $14.5\pm0.4\%$, and the excellent *Ge* consistency is observed in every layer. The quantum well thickness (*FWHM*) is slightly narrower at 7.95 ± 0.7 nm since the quantum well growth times are equal for both structures, while the *SiGe* thickness obtained by *XTEM* (Fig. 3.12) occur as 9 ± 1.2 nm. This small thickness deviation suggests that the widths that we have inferred from the *FWHMs* of the *SIMS* measurements are accurate and the measurement is not heavily influenced by the germanium content of the quantum wells. Once again, the reproducibility of the quantum well features is greatly encouraging.



Figure 3.12: XTEM data for sample k2452-2.

The conclusion of physical measurement of k2452 batch is presented in table 3.1. Figure 3.12 shows a *XTEM* micrograph of sample k2452-2. This clearly shows 8 SiGe quantum wells and shows no evidence of misfit dislocations.

Sample Ge x	$Si_{I-x}Ge_x$ layer				
	Gax composition obtained by SIMS	The thickness (nm)			
	Ge x composition obtained by Shus	SIMS	XTEM		
k2452-1	0.045±0.016	10.5±0.71	10±0.71		
k2452-2	0.145±0.004	7.95±0.7	9±1.2		

 Table 3.1: Summary of physical properties of samples k2452-1 and -2.

The first two quantum structure growths demonstrated a number of important, and in many ways, encouraging features: excellent epitaxial quality free of misfit dislocations, excellent uniformity of deposition rate within a single growth run and reasonably good reproducibility from growth run to growth run (at least for these two consecutive growth runs). The *SIMS* profiles show that the germanium contents are lower than expected. Sample k2452-2 should have had a germanium content of x = 0.2, but the *SIMS* data indicate that the actual content is 0.1. This factor of two decreases might be due to transient effects (as a result of the time taken for the germane content to reach the necessary levels within the deposition chamber) or may be due to a more fundamental feature of the epitaxy of the strained-layer.

Encouragingly, the *Ge* contents are constant and the interfaces between the *Si* and *Si*₁. $_xGe_x$ are distinguishable on the *XTEM* micrographs. The absence of any misfit dislocations, extending from the quantum wells, indicates that they are below the critical thickness as we would expect considering the thicknesses and compositions, obtained.

In general, these initial results vindicate the decision to proceed to the deposition of quantum well structures without detailed calibrations for stand-alone *SiGe* layers as it seems that the growth of strained quantum well structures might require its own distinct calibrations. These results also demonstrate the difficulties of fully defining the shape of these thin quantum features. It is not sufficient to simply define a thickness and a composition for each quantum well. The electronic band structures within quantum structures are functions of the shape of the well [42, 89-92], and full modelling of band structure can only be obtained if composition profiles (*x* as a function of distance) are accurately measured. Even after accurate *SIMS* and *XTEM* measurements, it is still not possible to accurately quantify these features, and therefore, it would not be possible to accurately describe the band structure. It is, in general, better to infer band structure from optical characterisations as we shall see in chapter 4.

3.7 The second generation of Si/Si_{1-x}Ge_x multi-layer structures

The primary aim of the second generation of depositions was to improve on the relatively low maximum germanium contents found in the first generation structures. A second set of $Si/Si_{1-x}Ge_x$ multilayer structures were designed (k2680). The growth temperature and chamber pressure were 820° C and 400mTorr respectively, slightly modified from the previous experiment because equipment was recalibrated and conditioned, and routine *Si* growths, before this experiment, had indicated good epitaxy at this temperature and pressure. Three growths were carried out, each aimed to produce twenty layers of undoped *Si* barrier layers of 50nm and undoped *Si*_{1-x}*Ge*_x quantum wells of 5nm. The *Ge* concentrations of k2680-1 and k2680-2 were designed to be x=0.1, x=0.2 and x=0.3, respectively. The silane and germane ratios were 100:15, 100:25, and 100:50 for k2680-1, -2 and -3 respectively.



(a)




(c)

Figure 3.13: SIMS data showing the germanium contents of (a) k2680-1, (b) k2680-2, and k2680-3.

Figure 3.13 shows the *SIMS* data for the second generation of quantum structures (batch k2680). The germanium content profiles indicate that the peak germanium concentration in the $Si_{1-x}Ge_x$ layers gradually increases with growth time, while the background germanium content between the germanium peaks increases closer to substrate. This may indicate the different *Ge* content in different nanostructure (will explain later), while the detection of residual ion in instrument responds for background *Ge* profile. The mean peak germanium contents of k2680-1, -2 and -3 are $4\pm1\%$, $7\pm1.4\%$ and $9\pm1.4\%$ respectively, and the *FWHMs* are estimated as 11.7 ± 3.1 nm, 11.9 ± 3.9 nm and 10.1 ± 0.9 nm, again, for samples k2680-1, -2 and -3 respectively. The germanium peaks, seen at around 1.6μ m, indicate contamination at the surface of the original wafer.

 Trough
 Crest

 J
 SEI
 9.0kV
 X100,000
 100nm
 WD 5.4mm

(a)



(b)



Figure 3.14: SEM cross-section images of second generation of $Si/Si_{1-x}Ge_x$ multilayer structures. (a), (b) and (c) are SEM images of k2680-1, -2 and -3.



Figure 3.15: The *XTEM* of sample *k2680-2*. The magnified image in the inset allows a clear picture of the nanostructure.

Figure 3.14 shows two *SEM* images of three dimensional growth features within the $Si_{l-x}Ge_x$ layers (white band). Crests and troughs feature in all samples. These features are best seen at high resolution using *XTEM* (Fig. 3.15). The $Si_{l-x}Ge_x$ multilayer close to the substrate are observed as continuous, but slightly undulating layers, with increasing distance from the substrate these undulations intensify until relatively strong crest and trough features are observed. Interestingly, smaller $Si_{l-x}Ge_x$ structures, appear at the base of the $Si_{l-x}Ge_x$ crests (figure 3.15 inset). It appears that the strain conditions caused by the regions of high germanium contents increase the likelihood of the *SK* growth mode in the regions above. After many multilayers this mechanism gradually increase the three dimensional nature of the surface. The thicknesses. The trough thickness is around 10nm in all samples (Table 3.2). The crest structure seems to increase in thickness with higher germanium content.

		Si	i _{1-x} Ge _x layer				
Sample	Ge x composition	The thickness (<i>nm</i>)					
	obtained by SIMS	SIMS	SEM		XTEM		
			Crest	Trough	Crest	Trough	
k2680-1	0.04±0.01	11.7±3.1	22.5±2.3	10±1.9	*		
k2680-2	0.07±0.014	11.9±3.9	14.4±2.8	10±0.5	19±3.4	8 ±2	
k2680-2	0.09±0.014	10.1±0.9	14.5±2.7	10±0.4	-	-	

Table 3.2: Summary of physical of samples *k2680-1*, *-2* and *-3*.

3.8 The third generation Si/Si_{1-x}Ge_x multilayer structures

Batch k2833 consisted of two wafers growths and was designed to increase the maximum germanium content of the structure. Two <100> *p*-type wafers were used, and the layers on the first wafer was grown at 820°C, while the second was grown at a reduced temperature of 750°C. With a view to future requirements, boron was introduced into the growth chamber during the growth of the $Si_{1-x}Ge_x$ layers in order to dope the quantum wells *p*-type, the silicon layers were left with no intentional doping.

The growth sequence was as follows:

- 1) an undoped silicon buffer layer 100nm thick,
- 2) an undoped silicon spacer layer 40nm thick,
- 3) a heavily boron doped (target 1×10^{19} cm⁻³) Si_{1-x}Ge_x layer 10nm thick,
- 4) repeat steps 2 and 3 nine more times, and
- 5) an undoped silicon capping layer 100nm thick.

The stacks of $Si/Si_{1-x}Ge_x$ structure were grown at different silane flow rates. For the first five layers 40sccm of silane was used, and 10sccm of silane was used for the next five layers. The germanium and boron contents were evaluated by the *SIMS* technique, and the structures were studied by *XTEM*.



(a)



(b)

Figure 3.16: The Ge content and boron concentration SIMS profiles of samples k_{2833-1} and -2 represented in (a) and (b) respectively.

In the sample grown at 820° C, k2833-1, the change in silane flow does not lead to a significant enhancement of the germanium content. In fact, the germanium profile is consistent with the fraction of germanium, x being 0.125 ± 0.006 . The linewidth of each germanium line is sharp and narrow, which indicates that the layers are thin.

In the sample grown at 750°C, k2833-2, the effect of the silane flow reduction can be observed as two sets of germanium peak heights (Fig. 3.16b), The germanium content is enhanced when the silane flow is decreased; the first 5 layers have $x = 0.05\pm0.005$, while the top 5 layers have $x = 0.09\pm0.016$. The line widths are wider than those in the k2833-1 sample.

The peak concentration of boron (B) in these samples is high at 1×10^{19} cm⁻³, and each boron peak is within a $Si_{1-x}Ge_x$ layer as designed. However, boron interdiffusion and autodoping is clearly seen in both samples, and the background level in the epitaxial layer does not go below 1×10^{19} cm⁻³. The background impurity concentration in the low temperature growth sample is higher than in the sample grown at high temperature. The alignment of *SiGe* multilayer and boron multilayer seems to exhibit consistency in both growth temperature regimes. Additionally, the linewidth of *SiGe* and boron profile are also consistent with each other. This implies that the *SiGe* and boron multilayer growth recipes produce well-doped confinement in *SiGe* multilayer, sandwiched by undoped *Si* spacers. Although the boron concentration may not low enough to claim undoped status $(1 \times 10^{15} \text{ cm}^{-3} \text{ or less})$, the abruptness between so-called doped and undoped layer is distinct. However, the growth calibration is still needed to continuously carry out in order to improve this issue.





(b)

Figure 3.17: *XTEM* images of the $Si/Si_{1-x}Ge_x$ multi-layer. (a) and (b) show k2833-1 grown at the standard temperature (820°C) and k2833-2 grown at a lower temperature (750°C) respectively.

Figure 3.17 obviously indicates the *S-K* growth mode, leading to the three dimensional SiGe nanostructures. The dislocations are not observed in *XTEM* images (Fig 3.17), suggesting a good quality *SiGe* epitaxy. The thicknesses of nanostructures, obtained by *XTEM*, are 20 and 28nm, while the widths of the base of structures are 130 and 220nm (k2833-1 and -2) respectively as shown in table 3.3. The thicknesses of nanostructures are also extimated by *FWHM* method as preceding experiments, and they are 11.5±1.9 and 30.5±6.8nm of k2833-1 and -2 respectively. Note that the thickness, approximated by *XTEM* and *SIMS*, in k2833-1 sample exhibits difference upto around 50% because of the thick determination difficulty in *XTEM* due to dim *SiGe/Si* interface, comparing with k2833-2 image (Fig. 3.17b). However, in this report, the *FWHM* method for *SiGe* thickness determination in *SIMS* profile is still believed that it gives reliable thickness information. The alignments of nanostructure between each layer are inspected in figure 3.17, which agree to the multilayer of SiGe nanodot, published by elsewhere [93-97].

	Dot dimension measured by				
Sample	XTE	SIMS			
	Thickness (nm)	Width (nm)	Thickness (nm)		
Si _{0.85} Ge _{0.15} (k2833-1)	20	130	11.5±1.9		
Si _{0.89} Ge _{0.11} (k2833-2)	28	220	30.5±6.8		

Table 3.3: The dot dimension of *k2833-1* and *-2*.

3.9 Analysis

The strong three-dimensional features, observed in many of the $Si_{1-x}Ge_x$ layers, are due to a strain related mechanism. Lens-like shapes are connected by thin $Si_{1-x}Ge_x$ layers (inset of figure 3.15), which have been reported by a number of authors, using the *CVD* growth technique [93-97]. They appear to be two types of island formation, small lens features, occurring in the Si spacer layer close to the large lens feature. Their thickness at the crest is about 8nm, while thicknesses of larger features are around 20nm. The width of large lens is 170nm, while the width of small lens is from 100-170nm. It is likely that the smaller features represent the first stage of nucleation. Whereas, the uniformity of the larger features might represent either a maximum feature size or simply the size of germanium features that begin nucleation immediately. The growth characteristics of all the $Si/Si_{1-x}Ge_x$ multi-layer experiment are shown in Table 3.4.

				Silicon spacer			Si _{1-x} Ge _x layer			
Sample	T(C)	P(Torr)	^{SiH} 4 flow (sccm)	Growth Time (sec)	Thickness (<i>nm</i>)	SiH ₄ :GeH ₄ (sccm:sccm)	Growth Time (sec)	Ge content (x)	Thickness (<i>nm</i>)	
k2452-1	810	0.5	40	30	49	40:6	5	0.045±0.016	10±1.5	
k2452-2	810	0.5	40	30	48	40:20	5	0.145±0.004	9±1.2	
k2680-1	820	0.4	40	40	50 ± 6	40:15	3	0.04±0.01	10±1.9	
k2680-2	820	0,4	40	40	58±2	40:25	3	0.07±0.014	10±0.5	
k2680-3	820	0.4	40	40	55±5	40:50	3	0.09±0.014	10±0.4	
k2833-1	820	0.4	40	32	40 ± 6	40:50	. 5	0.125±0.006	20	
k2833-2 75						40:50		0.05±0.005	28	
	750	0.4	40	45	32 ± 2	10:50	. 8	0.09±0.016		

Table 3.4: The growth parameters and characteristics of the $Si/Si_{1-x}Ge_x$ growth experiments.

For all the experiments, the maximum germanium content is $x \approx 0.15$, agreeing with ref. [87]. The germanium concentration is dependant on the flow rate ratio and the growth temperature. At the same growth temperature, the germanium content increases with the flow rate ratio, as indicated by the k2680 samples in table 3.4. The germanium concentration is less at lower growth temperatures (750C), and the dependence of the germanium incorporation on silane flow rate seems to decrease at higher temperatures (k2833-1).

• .



Figure 3.18: Germanium composition versus the germane flow fraction (%) of the samples fabricated at various growth temperatures.

Other reports on *CVD* growth, show that the relationship between germane flow fraction and germanium content is linear [88, 98, 99]. The data of growth at 820°C in this work also suggests a linear relationship. The slope at 810°C is greater than at 820°C in accordance with [88]. However, the dependence at 750°C is the shallowest, this is surprisingly different from other reports. As discussed earlier, the Southampton *LPCVD* machines are relatively unique in that they operate at the cross-over between temperature- controlled and transport-controlled regimes. The relative growth rates of both silicon and germanium will be very sensitive to temperature at 750°C,

3.10 Conclusion

The growth experiments have produced a number of interesting samples that will be examined by optical techniques in chapter 4. In general, we have found that for all samples, there is significant germanium content. The *SiGe* thickness is always below the critical thickness, and the quality of the epitaxy is high with little evidence of

strain-relaxation defects. Intriguingly, the samples have revealed a tendency for threedimensional quantum-dot features that might greatly assist in the fabrication of near infra-red photodetectors. The sample sets are summarized in figure 3.19.





(b)







Chapter 4

Si/SiGe Optical Properties

As discussed in chapter 3, it is almost impossible to determine the composition profiles of Si/SiGe quantum structures with sufficient accuracy to determine features of the band-structure. Fortunately, a large range of optical characterisation techniques can allow determination of features such as bandgap energy and the energies of quantized levels and impurity levels. Optical characterisations can also help to determine the nature of quantum features (quantum well or quantum dot). Optical studies not only allow an understanding of the structure and composition of the Si/SiGe samples, they also allow us to understand the suitability for use in near-infrared photodiodes. This chapter will consider both photoluminescence and absorption spectra of a selection of samples described in chapter 3 (Fig.4.1)





Figure 4.1: Summary of device structures.

4.1 Photoluminescence apparatus

A schematic diagram of the photoluminescence system is shown in figure 4.2. Excitation can be provided by using an *Argon* ion laser (488-514nm) or a heliumneon (*HeNe*) laser (632.8nm), and the excitation power density can be varied up to 1.4 Wcm^{-2} . Samples are mounted on a metallic (*Al* or *Cu*) base plate and placed in a closed-cycle helium cryostat that could vary the temperature from 8K up to 300K. The luminescence from the sample was focussed into a *Jobin Vyon THR 1000 (1m* focal length) monochromator (1800 lines/mm grating) and detected using an *Edinburgh EI-L* germanium detector cooled by liquid nitrogen. The signal from the photodetector was amplified by a standard lock-in amplifier and collected on a standard *PC* using in-house software.



Figure 4.2: Schematic of the photoluminescence experiment. The neutral density and interference filters are used to reduce laser light and remove unwanted plasma lines.

4.2 Photoluminescence studies of Si/Si_{1-x}Ge_x samples

4.2.1 Photoluminescence from quantum wells

Figure 4.3 shows photoluminescence (*PL*) spectra for the first generation Si/SiGe quantum structures (k2452-1 and k2452-2) (Table 4.1) obtained at 16K.

	$Si_{l-x}Ge_x$ layer			
Sample	Ge content	Thickness		
	(x)	(<i>nm</i>)		
k2452-1	0.045±0.016	10±1.5		
k2452-2	0.145±0.004	9±1.2		

Table 4.1: The Ge content and SiGe layer thickness summary of samples k2452.



Figure 4.3: *PL* spectra of 10*nm* thick $Si/Si_{0.945}Ge_{0.055}$ (k2452-1) and 9nm thick $Si/Si_{0.855}Ge_{0.145}$ (k2452-2).

Many of the features seen in figure 4.3 are similar to those seen in spectra from similar samples under similar conditions [27, 30, 31, 41, 42]. The no-phonon (*NP*) line of the $Si_{1-x}Ge_x$ alloy structure [30, 31] and *momentum-conserving* (*MC*) phonon radiation are clearly observed.

In indirect bandgap material, *NP* transitions are forbidden due to the translational symmetry of the lattice, but with germanium incorporation, the requirement of *momentum conservation* is relaxed because of alloy disorder, which causes an overlap

of the wavefunctions in k-space [41, 42]. The position of the SiGe no-phonon transition (NP_{SiGe}) is seen to shift to a smaller energy with increasing germanium composition (1.12 and 1.06eV for k2452-1 and -2 respectively).

The silicon capping and barrier layers emitt at 1.1eV in both samples, as a result of transitions, attributed to the radiative recombination of local excitons at acceptor (boron) atoms with momentum-conserving transverse optical phonons (Si_{TO}). The full width at half maximum (*FWHM*) of the *NP* lines is 12meV, this is higher than reported in other work, and probably a result of inhomogeneous broadening [27].

The momentum-conserving phonon-radiative recombination of the $Si_{1-x}Ge_x$ alloy is found at lower energies than the *NP* line. Two types of phonon contribute to the *MC* transitions, *transverse-optical* (*TO*) phonons and *transverse-acoustic* (*TA*) phonons. There are *TO* phonons for each bond type in *SiGe*; *Si-Si* bonds (*TO*_{*Si-Si*}), *Si-Ge* bonds (*TO*_{*Si-Ge*}) and *Ge-Ge* bonds (*TO*_{*Ge-Ge*}) have energies 58, 49 and 35meV respectively. The silicon tranverse-acoustic phonons (*TA*_{*Si-Si*}) are also important and occur at 17meV [27, 31, 42]. An encouraging feature of the spectra is the lack of luminescence features due to dislocation networks, which are commonly observed at around 800-900meV [100-103].

Photoluminescence spectra obtained for the second generation of samples (k2680-1, - 2 and -3) (Table 4.2) measured at 16K are shown in figure 4.4.

	$Si_{l-x}Ge_x$ layer			
Sample	Ge content	Thickness		
	<i>(x)</i>	(<i>nm</i>)		
k2680-1	0.04±0.01	10±1.9		
k2680-2	0.07±0.014	10±0.5		
k2680-3	0.09±0.014	10±0.4		



As shown in table 4.2, the quantum well thickness for these samples is constant while the germanium content of the quantum wells increases from k2680-1 (x = 0.06) to k2680-3 (x = 0.11).



Figure 4.4: Near band-edge photoluminescence spectra of 10nm thick $Si_{0.94}Ge_{0.06}$ (k2680-1), 10nm thick $Si_{0.91}Ge_{0.09}$ (k2680 -2) and 10nm thick $Si_{0.89}Ge_{0.11}$ (k2680-3).

The momentum-conserving transverse-optical emission line from the silicon matrix is seen at 1.09eV for each sample, agreeing with ref. [30] value (1.092eV). The next most energetic feature for each spectra is the *NP* transition from the $Si_{1-x}Ge_x$ quantum wells. This *NP* line is seen to move to lower energies as the germanium content increases. Beyond the *NP* line, there are series of phonon replicas, the most dominant of which are the TA_{Si-Si} and the TO_{Si-Si} replicas. The expected positions of TO_{Si-Ge} and Si_{Ge-Ge} are marked in figure 4.4, where the shape of the spectra provides some relatively weak evidence of these less transition probability.

The *FWHMs* of the *NP* lines are all around 10-12meV except k2680-3 which at 23 meV is also higher than published data [27]. Broadening of this line width is most likely due to compositional disorder [27, 56].

Unfortunately, the third generation samples (k2833-1 and -2), showed no SiGe PL emission. This is perhaps a result of the boron doping. The non radiative transition probability is high in highly doped semiconductor via *Auger* recombination process: the photon energy, emitted from electrons (or holes) transition process, immediately transfers to other electrons (or holes). Consequently, excited electrons (or holes), then, travel to higher energy state in the energy band valley and emit a phonon. Such processes involve three-body collisions: two electrons and one hole or vice vesa as shown in figure 4.5. Additionally, the dislocation networks in epitaxial layers also suppress *PL* although they are not observed in *XTEM*, it is possibile that dislocations, which are low density, occur at outside the inspection area.



Figure 4.5: The diagram of *Auger* recombination indicates a band-to-band transition; the second electron (or hole) transforms the energy, released in the recombination of the first electron (or hole), into kinetic energy by being excited deep into the conduction band in n-type material or from deep in the valence band in p-type material.

From the *PL* results and our understanding of the physical $Si/Si_{1-x}Ge_x$ structures it is possible to construct a model of the main electronic features of the samples (Fig. 4.6). The *NP* transition, yielded by alloy disorder, is represented as the arrow from the

alloy exciton energy level (dashed line) in SiGe layer, while the *MC* transition (*TO* or *TA*) is represented by the two-line arrow from the conduction band minimum to valence band maximum (black solid line) of the SiGe alloy. The energy of the *NP* lines and its transition in the band energy for the five k2452 and k2680 samples, reflecting the energy gap of material, are shown against germanium composition in figure 4.7, which indicates that the *Ge* content and strained effect are major components for energy gap reduction. This mechanism is essential for *Si*-based opto-device realisation.



Figure 4.6: The excitonic transition in discontinuity energy band of Si/SiGe strained layer. The dashed dispersed curves represent the exciton level. The black solid curves represent solid state energy band of the SiGe strained layer, which has different position in k-space according to the E-k diagram. NP represents the transition between exciton levels in the valence and conduction bands, which occurs in the SiGe as a result of alloy disorder. TO and TA represent the momentum-conserved transition with phonon participation (diagonal line).



Figure 4.7: The fitted transition model from PL measurement of samples k2452 and k2680.

4.2.2 Si_{1-x}Ge_x indirect energy gap determination

The quantum well transition energies can be readily determined by comparing the silicon luminescence peak position from the *SiGe* peak position assuming that the difference between the energy of high-temperature *BE* peak alloy photoluminescence is equal to the difference in band-gap energies for *Si* and *SiGe*. This condition is valid for the silicon-rich $Si_{1-x}Ge_x$ layer. The published undoped silicon luminescence energies, E_g , and BE_{Si} , are 1.16938 and 1.15011eV respectively [56]. For k2452-1 and -2, NP_{BE} peaks are found at 1.12 and 1.063eV from the *NP PL*-peak in figure 4.3. Subtracting these from BE_{Si} gives 30 and 87meV, and the difference between these and E_g indicate that the approximate energy gaps of k2452-1 and -2 are 1.14 and 1.082eV respectively as demonstrated in figure 4.8. The energy gaps of the k2680 experiment can be estimated in the same way, and these are 1.11, 1.072 and 0.987eV, obtained from *NP PL*-peaks in figure 4.4, for k2680-1, -2 and -3 respectively. These results correspond to the $Si_{1-x}Ge_x$ strained energy gaps for x<0.05 for k2452-1 and -2, and x=0.09 and x=0.11 for k2680-2 and -3, respectively [28].

k2452-1



Figure 4.8: The approximation of undoped *SiGe* energy gap from *BE* peak *PL* energy comparison with undoped *Si*.

Another comparison is made with the excitonic gap study of *J. Weber et al.*[27], although the *PL* temperature in our report is slightly higher. According to the *SIMS* measurements, the germanium contents of k2452-1 and -2 suggest that the nominal energy gaps should be 1.14 and 1.13eV, respectively. The energy gaps for the k2680 samples can also be calculated, and these are 1.14, 1.12 and 1.11eV for k2680-1, -2 and -3 respectively. These energies are obviously higher than the experimental data of both sets of samples. The same trend is also found in other work [26, 36]. Similar sample configurations as those in this report are also studied by *D. J. Robin et al.*[30] in which the *PL* of a series of single strained $Si_{1-x}Ge_x$ embedded layers with a silicon cap are measured. They also introduced a formula for finding the excitonic band gap for x<0.24 created by a least-squares fit to their experimental data as shown in Eq. 2.12 in chapter 2.

Table 4.3 presents the energies of the no-phonon line luminescence of k2452 and k2680, compared with several values provided in the literature for strained layers [30, 31] and a set of values for bulk samples [56]. All of the germanium compositions of the selected samples are close to the composition of the structures, produced in this work.

The excitonic energy gap for x=0.14 exhibits a higher energy gap than ref. [30]. This is, perhaps, attributed to quantum confinement within the thin strained layer. Surprisingly, the sample with $x = 0.09 \pm 0.02$ presents the lowest energy gap although this compares with the energy gap for x = 0.203 of ref. [30]. This result might be due to exciton localisation in the inhomogeneously broadened $Si_{1-x}Ge_x$ layer. In the lens-shaped islands germanium atoms are likely to accumulate at the top of the structure, and these sites provide the lowest energy transition in the band structure, and this will be the dominant *PL* feature. The linear fits of the experimental data compared to *Weber et al.*[27] and *Robbins et al.*[30] are shown in figure 4.9. The samples k2680 indicate that the energy gaps are lower than the strained and relaxed cases, while those for the k2452 samples are close to those of ref.[30]. These results demonstrate that our samples demonstrate strain effects.

	Thickness (nm)		Composition x		NP energy	Cal.
Sample	Nominal	XTEM	Nominal	SIMS	(eV)	Eg (eV)
k2452-1	10	10 ± 1	0.06	0.045 ± 0.01	1.12	1.14
k2452-2	10	9	0.2	0.14 ± 0.005	1.063	1.082
k2680-1	10	10 ± 2	0.1	0.04 ± 0.02	1.097	1.11
k2680-2	10	10 ± 3	0.2	0.07 ± 0.02	1.053	1.072
k2680-3	10	10 ± 1	>0.2	0.09 ± 0.02	0.967	0.987
Ref[30]	50		0.126	•••••	1.051	•••••
Ref[30]	50		0.203	•••••	0.993	•••••
Ref[56]	Bulk		0.11	•••••	1.109	1.129
Ref[104]	8.3		0.2		0.985	
Ref[34]	7.5		0.25		0.98	•••••
Ref[42]	10		0.16		1.02	
Ref[31]	2.5		0.19 ± 0.03		1.037	

Table 4.3: Data from structures including the thickness of the $Si_{1-x}Ge_x$ layer, the germanium composition, the no-phonon energy and the calculated energy gap compared with several references.



Figure 4.9: Comparison of linear fits of the experimental excitonic energy gap data (dotted line) with the results of *Weber et al.*[27] (solid line) and *Robbins et al.*[30] (dashed line).

From figure 4.9, the results of experiment k2452 exhibit well-resolved linear Ge content dependence of strained SiGe energy gap, according to Robbins's model. This agreement is plausibly believed because the cross section of this experiment indicates the smooth continuous SiGe multilayer, which is similar to Robbins's experiment. Therefore, the samples in experiment k2452 are perfectly represented as two-dimensional strained SiGe quantum well multilayer. In k2680 results, the linear Ge content dependence of energy gap reduction indicates lower than k2452 experiment. These reflect the Ge content fluctuation due to crest and trough features as shoen in figure 3.14 and 3.15. The high Ge content at crest features, which may not be detected by SIMS, contribute exceed below the Robbins's model. To obtain more accurate exact Ge contents, alternative measurement techniques are required such as X-ray diffraction or raman spectroscopy. Comparing with Weber's model, both k2452 and k2680 results show obvious lower energy gaps, comprehensively indicating strained SiGe layer.

4.2.3 Photoluminescene of quantum dots.



Figure 4.10: The low energy emission due to $3D Si_{0.91}Ge_{0.09}$ nanostructures (k2680-2).

Figure 4.10 shows two extra emission bands between 0.85 and 0.95eV. These peaks can be attributed to emission from germanium-rich quantum dots. This pair of lines, due to emission from the quantum dot (0.931eV) and wetting layer emissions (1.053eV) is reported by ref. [105, 106], and this also accords with the *XTEM* image in figure 3.15. Additionally, TA_{Si-Si} and TO_{Ge-Ge} luminescences are also observed, which is generally expected in *SiGe PL*. The *X1* and *X2* would probably be the luminescence due to dislocation in the sample. The simple model of the *PL* emission is shown in figure 4.11. The energetic position of the germanium dot luminescence in k2680-2 is higher than in other published work [25, 105, 107-110]. This reflects a lower *Ge* content ($x \cong 0.25$), within the features [106, 111-113].



Figure 4.11: PL emission model of k2680-2. The dashed curves represent the exciton energy level, and the solid curves represent the material energy level.

4.2.4 The relative intensity NP/TO ratio

The relative intensity of the *PL* peaks provides the atomic composition of the alloy by considering the *NP/TO* ratio [27, 30]. The intensity of momentum-conserved phonon transitions is higher than the *NP* intensity in *Si*-rich $Si_{1-x}Ge_x$ material, and the *NP* peak will develop until it is greater than the phonon participating peak as the *Ge* composition is increased. This trend is seen in both alloy and strained layer cases. The evolution of the *NP/TO* ratio reaches a peak at a composition of 50% *Ge* (*x*=0.5), while the minima are at *x*=0 and *x*=1[27, 30]. This ratio represents the probability of finding a *Si-Ge* pair causing short-range potential fluctuations in alloys at various compositions. The *NP/TO* ratio of both experimental sets was observed to be between 0.5 and 1.5 as shown in figure 4.12, and it increases along with the composition, which agrees well with other work [27, 30].



Figure 4.12: Intensity ratio of the no-phonon transition, *NP*, to the *Si-Ge* phonon replica for various compositions of the investigated samples. The dashed line is proportional to the probability of finding a *Si-Ge* pair in the layer [27, 30].

4.2.5 PL temperature dependence measurement

Photoluminescence measurements were performed on the sample with the brightest photoluminescence, k2680-3 with the temperature range 8K to 150K, at 10K intervals (Fig. 4.13).



Figure 4.13: The temperature dependence of photoluminescence of k2680-3 excited by 633nm *HeNe* laser at 20mW/mm².

At temperatures above 18K, the *TO* and *NP* peaks thermalise and two different peaks emerge at 0.915eV and 0.967eV. These two lines maintain the same energy position, but broaden and reduce in magnitude with increasing temperature before becoming undetectable at around 150K. These two emission lines of fixed energy position, with increasing temperature, are consistent with other photoluminescence temperature dependent reports [90-92]. As has already been discussed, the bound exciton (*BE*) transitions (*NP*) are commonly observed at temperatures below 10K [27, 30]. However, as the temperature increases, the *free-exciton* (*FE*) no-phonon radiative recombination is more commonly observed. These free-exciton lines are at higher energy than the low temperature (*BE*) lines. It is clear that with increasing temperature. We are seeing the thermalisation of the bound excitons from the binding center (boron, phosphorous or arsenic) [27, 31, 41, 56]. Here, the *FE* line is first observed at 18K, however, this line and *BE* are also observed in low-doped $Si_{1-x}Ge_x$ at low temperatures down to 1.9K as reported by *Mitchard and McGill* [56]. *FE* recombination can be identified by fitting experimental data with the well-known Eq. 4.1 [27]

$$I(E) \propto \sqrt{E - E_0} \exp\left[\frac{E - E_0}{k_B T}\right]$$
(4.1)

Where I(E) is the luminescence intensity at photon energy E, E_0 is the FE recombination threshold energy, and T is the temperature in Kelvin. This expression explains the line shape and luminescence intensity at various temperatures, and not only the FE feature of the NP line but also TA-, LA-, TO-phonon replicas depending upon the composition.

The *FE* radiative recombination of Si_{TO} peak of $Si_{0.89}Ge_{0.11}$ is similar to *FE* thermal behaviour from other reports [27, 56]. The fitting data using equation 4.1 was performed as shown in figure 4.14. The fit temperature is about 20K, which is agreed with the cryostat temperature, and the line shape of the fitted data partially coincides with the experimental data. The expression for the fitted *FE* data is a little inadequate for fully resolving *FE* due to the weak *PL* intensity, high impurity, poor heat transfer in sample cryostat and composition inconsistency. These parameters may cause the experimental *FE* line shape to be broader, and they make *FE* identification at *NP* and *TO* difficult. The energy spacing of *NP* and *TO* at different cryostat temperature is about 3meV, which is close to the exciton binding energy at the *boron* and *phosphorous* impurity energies in *Si*. These binding energies are found to be large when a large number of excitons are bound in a complex are 9.9 and 13.1meV respectively [114]. Therefore, the large energy spacing would be attributable to many excitons.



Figure 4.14: Free-exciton luminescence from the undoped sample, k2680-3, and a least-squares fit of the theoretical line shape (Eq. 4.1). The sample temperature is given as T_{cryo} , while the temperature resulting from the fit is T_{fit} .

4.2.6 The quantum confinement effect

The survival of the *NP* line at high temperature can be attributed to quantum confinement. In principle, a strong *NP* line occurs due to the breaking of the *k*-selection rule of the $Si_{1-x}Ge_x$ system due to alloy disorder [27, 31, 42, 89, 115, 116], and furthermore, generated carriers (holes) can be trapped inside small potential structures formed by the $Si/Si_{1-x}Ge_x$ system [91]. In the case of bulk silicon, the *PL* peak signal (TO_{si}) decays at 20-60K [89-92] because the probability of a momentum conserving phonon is high only at very low temperatures, and the deactivation energy of *Si* emission is comparable to the activation of non-radiative pathways (~ 10meV)[40]. However, some authors have found that the silicon emission can survive up to room temperature in $Si/Si_{1-x}Ge_x$ samples, and claim that this is due to *TO*-phonon assistance of the silicon barrier layer [89]. In the quantum well case, the carrier population, created from the barriers, swiftly diffuses and thermalises to the

lowest bound state in the discontinuous band potential instead of the bulk band energy. This process is enhanced as the temperature is increased because more carriers will be collected in the well, and with the breaking of the translational symmetry of the $Si_{I-x}Ge_x$ lattice. The indirect transition rule is relieved [41, 43, 90]. The NP signal of the investigated sample is quenched at about 150K, which agrees with other authors for small Ge content (<30%) [89, 90], and the maximum intensity also occurs at 20K. The temperature dependence of the photoluminescence intensity is shown in figure 4.15. Table 4.4 presents the activation energy, calculated from the intensity reduction threshold of each sample. At this part, the plot is obeyed $I \propto exp(-E_a/kT)$, which I is intensity, k is boltzmann constant, T is temperature in Kelvin and E_a is activation energy. The E_a is high in high Ge content quantum well structure, reflecting high hole confinement energy.



Figure 4.15: The arrhenius plot of integrated intensity of the MQWs of the investigated samples k2452 and k2680.

Sample	Activation energy (meV)
$k2452-1$ (10nm $Si_{0.945}Ge_{0.055}$)	40.2
k2452-2 (9nm Si _{0.855} Ge _{0.145})	130.8
$k2680-1$ (10nm $Si_{0.94}Ge_{0.06}$)	74.4
$k2680-2 (10 \text{nm } Si_{0.91}Ge_{0.09})$	66.8
$k2680-3 (10 \text{nm } Si_{0.89}Ge_{0.11})$	162

Table 4.4: The activation energy of sample *k2452* and *k2680*.

4.2.7 Power dependence of Si/Si_{1-x}Ge_x PL

BE and *FE* emission can also be identified by the power dependence behaviour. In figure 4.16, at low power excitation, the *FWHM* and intensity are narrow and weak respectively. The *FWHMs* of the *PL* peaks widen when the excitation power is increased. Additionally, there is a shifted peak, occurring toward smaller energy at high-power; the energy shift, the difference between *M* and *TO*, is as much as $\approx 4-5$ meV. If the pump power is further increased, the shoulder at the low energy side of both *NP* and *TO* peak increase and give rise to a peak (*M*) at lower energy. In figure 4.16, a shifted peak (*M*) is clearly observed in the *TO* peak. This result can be attributed to bound multi-exciton complexes (*BMEC*) [27, 56]. The shift, due to *BMEC*, is found to be 2.2meV for *B* and 3.6meV for *P* [56]. In pure silicon or germanium crystals, *BMECs* are also formed at increased exciton densities. Conclusively, the *BMEC* decays give rise to *M* luminescence on the low-energy side of the bound-exciton recombination. However, no sharp *M* at *NP* line can be resolved in the *Si*_{1-x}*Ge*_x alloy because the linewidth increases due to alloy fluctuations.



Figure 4.16: Power dependent *PL* of *k2452-1* (10nm *Si_{0.945}Ge_{0.055}*)

4.3 Absorption study of Si/Si_{1-x}Ge_x samples

Near band edge absorption measurements were used in order to investigate the optical sensitivity of the samples. The data was obtained using a *PerkinElmer* Spectrum *GX FT-IR* spectrometer. The experiments were carried out at room temperature and the spectral range is from the near to the medium infrared: $0.9 - 5\mu$ m. All experimental data were acquired by using data acquisition software on a computer, interfaced to the *PerkinElmer* system. The absorption data are presented as absorbance (*A*), which converts from the transmittance data (%*T*) as: A = log(100/%T). In order to optimise the measurement, a specific beam splitter and detector were selected: a calcium fluoride (*CaF*₂) beam splitter and a triglycine sulphate (*TGS*) based pyroelectric infrared detector. The spectral ranges of each are 15600-1200 wavenumbers (cm⁻¹) respectively. A near-*IR* internal light source (15000-1200 wavenumber) generates the optical beam. The light is unpolarized and

projected on to the sample at normal incidence. The FT-IR spectroscopy diagram is shown in figure 4.17.



Figure 4.17: Schematic diagram of the FT-IR spectroscopy set up [38].

Briefly, the operation can be described as follows: the light source, which is a heated element or glowbar, generates the beam which is passed through the beam splitter. The beam splitter reflects 50% of the incident light and transmits the rest. Consequently, two different light paths are created, shown by L1 and L2 in the figure. The transmitted path (L2) is reflected back to the splitter by a fixed mirror (M2), while the reflected path (L1) impinges on the movable mirror (M1). The movable mirror translates back and forth, which is maintained parallel to the original plane. The two beams return coherently to the splitter. These two beams are summed and transmitted through the sample, and then reach the detector. With L1=L2, the two beams are inphase and reinforce each other, but as M1 is moved, L1 and L2 are no longer equal. The phase of the two beams changes according to the displacement of M1 (in x axis). The output of the detector consists of a series of maxima and minima due to the in phase and out of phase situations, and it reads like an interferogram. The detector signal is transformed using *Fourier* transformation.

4.3.1 Near bandedge absorption of k2452



Figure 4.18: The near-band edge absorption of the $Si/Si_{1-x}Ge_x$ multi-layer samples, k2452-1 and -2, at room temperature.

The absorbance signals are normalised by multiplying each spectral point by a factor derived from a selected ordinate value. Zero baseline correction is performed in order to adjust all spectral data to the same level and enhance the signal comparison. The absorbance, plotted in figure 4.18, indicates the cut off wavelength of the $Si_{1-x}Ge_x$ samples to be 1.3µm, which is greater than the silicon reference. The corresponding energy (minimum band-to-band transition energy) is 0.95eV.





Figure 4.19: The near-bandedge absorption of the $Si/Si_{1-x}Ge_x$ multi-layer sample, k2680, at room temperature.

Again, the normalization procedure was performed as in the preceding experiment. The figure indicates long wavelength sensitivity extending from silicon due to the associated *Ge* atoms. The k2680-1 and -2 *Ge* samples have the same cut off, which is at a wavelength of 1.386µm, while the sample with the maximum *Ge* percentage only reached 1.26µm, which is less than for the silicon substrate. The calculated minimum transition energy from this experiment is 0.89eV for samples no.1 and no.2, while 0.98eV belongs to sample no.3. The absorption data presented in figure 4.19 shows that absorption is greatly enhanced (by and order of magnitude) at 1.3µm for the *Si/SiGe* layers and although the *Si* samples are seen to absorb up to 1.5µm, it is important to remember that most of that absorption does not generate electron-hole pairs and can not be readily utilised for photodetection.
4.3.3 Near band edge absorption of k2833



Figure 4.20: The near-bandgap absorption of the $Si/Si_{1-x}Ge_x$ multi-layer sample, k2833, at room temperature.

The normalization procedure is also performed in this experiment as in the two previous ones. The near-bandedge cut off wavelength for both samples appears lower than the silicon reference, and are 1.11 and 1.13 μ m for samples *k2833-1* and *-2*, respectively. However, strong absorption is exhibited from 1.5 to 5 μ m. This effect may be attribute to either the intersubband transition or free carrier absorption in the doped quantum structure [95, 117]. The highest peaks are at 3.31 and 3.43 μ m for samples *k2833-1* and *-2*, respectively, giving energies of 375 and 362meV.

4.3.4 Discussion

Sample lots k2452 and k2680 indicate a long-wavelength shift compared to the silicon reference. Similar experiments have carried out by others [35, 95-97, 117], and they are in agreement with those measurements although the cut-offs appear at longer wavelengths due to the higher germanium content. Self-assembled islands were realized by a germanium atom segregation mechanism during the growth process. This phenomenon causes a large amount of germanium to be located at the peak and centre of islands, while less resides at the base [93, 118].

k2833 provides interesting signals. The selection rule prohibits the intersubband transition at normal incidence, but the rule is not valid in the case of free carrier absorption [95, 117]. From the boron distribution obtained by *SIMS* in figure 3.16a and b, the large boron concentration diffuses with both the $Si_{1-x}Ge_x$ layers and the *Si* spacers. Therefore, free carrier absorption is likely to become the dominant mechanism. These results indicate the possibility of building mid-infrared $Si_{1-x}Ge_x$ nanostructured photodetectors relying on free carrier absorption.

Transmission spectroscopy mainly relies on the refractive index, absorption coefficient, reflection coefficient, and thickness of the specimen. The deep-level impurities do not respond well to optical transmission measurements [38]. In compound materials, these parameters can be altered by the composition, resulting in different interference signals in the measurement. Additionally, multi-layers or stacks of different material, i.e. $Si/Si_{1-x}Ge_x$ multi-layers, can also change the intensity or line-shape of the reflection and transmission spectra [117].

4.4 Summary

The physical, electrical and optical measurement in chapter 4 and 5 provide essential parameters for epitaxial samples, which are the energy gap and absorption. The table 4.5 exhibits summary of all epitaxial samples. For the photodetector design, the absorption edge is important.

		SiGe layer nanostructure			Excitonic	Cal.	Absorption
Sample	2D	Thickness	3D	Thickness	gan 16K	Energy	adga (um)
	(trough)	(<i>nm</i>)	(crest)	(nm)	gap TOK	gap 8K	euge (µm)
k2452-1	0.0945	10	-	-	1.12	1.14	1.3
k2452-2	0.145	9	-	-	1.063	1.082	1.3
k2680-1	0.06	10	-		1.097	1.11	1.39
k2680-2	0.09	10	0.25	20	1.053	1.072	1 39
			0.20	20	(0.931)	1.072	
k2680-3	0.11	10	0.11	20	0.967	0.987	1.26
k2833-1	-	-	0.15	22	-	-	From 1.25-5
k2833-2	-	-	0.11	33	-	-	From 1.25-5

Table 4.5: The summary of all samples.

Samples k2452 is a 2D strained SiGe multiple quantum well according to temperature dependence PL measurement and XTEM. These undoped samples have smaller energy gap than Si because of Ge association (x=0.945 and 0.145 for k2452-1 and -2). The Ge content dependence of SiGe energy gap agrees with the Robbin's work [30]. The extension of absorption edge is found in both samples at around 1.3µm.

Samples k2680 exhibit more interesting structure and energy gap. The gap reduction of this set is smaller than samples k2452 even the *Ge* compositions obtained from *SIMS* are lower than k2452 (x=0.06, 0.09 and 0.11 for k2680-1, -2 and -3). The *Ge* content dependence of excitonic gap exhibits lower than *Robbin*'s work [30]. The absorption edge is also found at 1.3µm. Three dimensional features related to the strained *SiGe* structure is found in all samples in the set, and this increases with higher *Ge* composition. The quantum dot behaviour occurs in *PL* measurement of k2680-2(0.931eV), and the *Ge* content in the *3D* structure is estimated as x=0.25. *Ge* content at the crest of undulating layer is likely to be higher than the trough. Unfortunately, the dot *PL* cannot be observed in k2680-1 and-2.

The doped strained samples k2833 exhibit large undulating feature to be dot structures, but the *PL* of *SiGe* features cannot be identified due to low signal.

Chapter 5

Si/SiGe photodetectors

The epitaxial growth developments described in chapters 3 and 4 have been used to define the fabrication sequences to produce *Si/SiGe p-i-n* photodetectors. By the incorporation of germanium, the devices have been designed to demonstrate enhanced absorption in the near-infrared spectral range. It was hoped that the formation of quantum dots regions with high germanium content could extend photoresponses deep into the communications wavelengths. This chapter focuses on the device design and the fabrication processes utilised. Structural characterisations of the *Si/SiGe* layers and device cross-sections are considered.

5.1 Device design

It is clear that p-*i*-n structure with epitaxial *Si/SiGe* quantum well structures , occupying the intrinsic region, is the most appropriate overall device strategy. Beyond this, it was decided that mesa-structures would be constructed to define and isolate individual devices and allow contacting to the p-region at the base of the device. This p-region would be embedded into an n-well that would form a guard-ring to electronically isolate individual devices from the substrate and other devices (Fig. 5.1).





The overall device construction sequence with appropriate lithographic stages starts with a p-type substrate. The n-well is implanted and then a highly doped p-type region. The next stage is the epitaxy stage, involving a range of *Si/SiGe* thicknesses and compositions. After epitaxy, the heavily doped n-type region is implanted. The remaining stages are the creation of the mesa-structures then contacting. Fabrication recipes, without the epitaxy detail, were simulated by *Silvaco* software as part of the design process until optimum electrical characteristics were obtained.

5.2 Mask design

The overall wafer design consists of 66 repeats of a basic *chip* design (Fig. 5.2). The device geometries consist of square and circular devices with areas ranging from $625\mu m^2$ to $4\times 10^6 \mu m^2$. Some test structures are added to each chip. These include contacts to allow measurements of sheet resistances for the different doped regions and areas suitable for *SEM* and *TEM* cross-sections.

The mask set has 6 layers defining the *n*-well layer (*NW*), the active area (*AA*), the mesa definition (*CR*), the bottom ohmic contact area (*AR*), the contact window (*CW*) and the metal pad (*MI*) as shown in figure 5.3.



Figure 5.2: The overall device mask.





Figure 5.3: The sequence of mask layers that define a representative device.

5.3 Device fabrication

The fabrication sequence (k2675) begins with <100> p-type wafers, which have 17-33 Ω /cm², and are polished on one side. The first stage is to define the *n*-well (Fig.5.4). After an *RCA* clean, a wet oxidation produces a 600nm oxide layer. Then a layer of photoresist is deposited, and the *NW* mask is applied to open implantation windows. The resist prevents implantation in the resist, covered regions, while the oxide layer within the windows protects the wafer surface from the worst of the implantation damage. In addition, the thickness of oxide layer is such that the peak of the implantation distribution corresponds to the wafer surface (Fig. 5.4 inset). After implantation at phosphorous dose 1.8E12 with 80KeV energy, annealing is carried out to activate and drive-in the implanted impurities. An annealing time of 8 hours at 1150°C is used to ensure a deep and low doping profile in the substrate. The cross section of device at this step is shown in figure 5.4.



Figure 5.4: Cross-section and planar view of the *n*-well. (Inset: the oxide thickness is designed so that the impurity distribution peaks at the surface of the wafer)

The oxide layer is removed, and the wafer RCA clean is performed. A second oxide layer is, then, grown so that a similar set of procedures can be carried out for the boron implantation that defines the device active area, through the AA window. This oxide and film resist are removed, and another RCA clean performed.

Another *RCA* clean is carried out imeadiately prior to the deposition of the undoped *Si/SiGe* multilayers. After *RCA* cleaning, another oxide deposition and phosphorous ion implantation are performed for the whole wafer area (Fig. 5.5).





Figure 5.5: The cross-section after the active area is defined by p^+ implantation, *Si/SiGe* epitaxy deposited and n^+ ion implantation completes the *p-i-n* structure.

Next, the *CR* lithography stage is used to define the device mesa. Then, plasma etching, without a built-in etch stop, removes unwanted sections of the epitaxial layers. *In-situ* laser measurements are used to monitor the etch depth and end the etch at 800nm. Then the resist is removed, and the wafers are cleaned (Fig.5.6).



Figure 5.6: The cross-section of the devices after the plasma dry etching.

Next, another oxide layer is deposited for ion implantation. The AR mask is use to pattern a resist and open a window onto the p-type region at the wafer level. Boron implantation with dose 8E15 at 50KeV energy is performed through the window to create p^+ regions, forming adequate ohmic contacts (Fig. 5.7). The resist and oxide layer are removed and 500nm of borophosphosilicate glass (BPSG) and 100nm of undoped Silox are deposited, forming a passivation layer (Fig.5.8).



Figure 5.7: The cross section of device after AR mask was applied, and the ohmic contact process at p^+ layer was done.

Another lithographic stage, using the CW mask, is used to open windows in the BPSG. The film resist and oxide are removed, and the wafers are cleaned by fumic nitric acid. Then 1000nm of titanium-aluminium (*Ti-Al*) is deposited by sputtering (*TRIKON SIGMA*). The final lithographic stage uses the *M1* mask to expose unwanted metal to be removed by dry etching (Fig.5.8). Cleaning and annealing complete the fabrication procedure, and detailed fabrication listings are provided in the appendix D.



Figure 5.8: The complete device after metal sputtering, *M1* mask layer and metal etching were applied.

5.4. Si/SiGe Epitaxial layers

Epitaxial layers, consisting of ten repeated $Si/Si_{1-x}Ge_x$ multi-layers, were grown by low-pressure chemical vapour deposition, based on the results of the development batches described an analysed in chapters 4 and 5. The layers were deposited with no intentional doping.

Two germanium contents and three different *SiGe* thicknesses defined the 6 wafers. The first set consists of 3 wafers, aimed for a germanium content of x = 0.06 and thicknesses of 10, 20 and 30nm. The second set of 3 wafers, aimed for germanium content of x = 0.20 and the same three thicknesses (Table 5.1).

Device	SiGe thickness (nm)	Si spacer thickness (nm)	Target Ge %
k2975-1	10	40	6
k2675-2	20	40	6
k2675-3	30	30	6
k2675-4	10	40	20
k2675-5	20	40	20
k2675-6	30	30	20

Table 5.1: The $Si/Si_{1-x}Ge_x$ epitaxy designs of six different wafers.

The lithographic layout and device construction for each wafer was the same. The growths were carried out at 820° C and at a pressure of 0.4Torr. *SiH*₄ and *GeH*₄ gas were used for the silicon and silicon germanium deposition. The flow rate, growth times and epitaxial layer information are shown in table 5.2.

Device	GeH_4 flowrate (sccm)	Si growth time (sec)	SiGe growth time (sec)
k2975-1	50	32	3
k2675-2	50	32	5
k2675-3	50	24	8
k2675-4	100	32	3
k2675-5	100	32	5
k2675-6	100	24	8

Table 5.2: $Si/Si_{1-x}Ge_x$ epitaxy machine details for the six device wafers.

5.5 Physical Characteristics of the Devices

Both devices and epitaxy surfaces have been extensively studied using thermal field emission scanning electron microscopy (*Jeol JSM-6500F*) and a Normaski microscope. The surfaces of devices and device cross-sections have been inspected. These inspections have mainly aimed to ensure correct device formation and contacting. In general, the majority of devices were correctly formed.

5.5.1 Device inspection

The surface of fabricated devices were inspected both visually and using a Normaski microscope. For all wafers, some cloud-like features could be seen on the surface using the naked eye. These cloudy areas could be seen at differnet locations on each wafer. These features are, sometimes, seen as a result of defective epitaxial growth. Wafer preparation is a key aspect to epitaxy, and it seems likely that the processing prior to epitxy, especially the implantation and cleaning stage, might have left some residual surface roughness or contamination, and this may have caused regions of relatively poor epitaxy. Other than these features, microscope inspection of the lithographic details of the wafer surface indicate fine and sharp features, reflecting accurate photolithography and mesa definition with successful alignment realised (Fig.5.9).



Figure 5.9: Inspection images of the device, obtaining by Normaski microscope. The cloudy features seen in some locations on the wafer are similar to defective epitaxial growth features.

High magnification inspection was performed, using *SEM* (Fig.5.10). The device images indicate well-resolved mesas (Fig.5.10a). The high magnification of device surface and surrounding areas allow a better understanding of the rough features. The square-pitted features (Fig.5.10b and 5.10c) are seen on some of the mesa surfaces. This pattern is a typical of defective epitaxial growth [119].

Device cross-sections are shown in figure 5.10d, e and f. These cross-sections can just about resolve the germanium bands in the device mesa. The images indicate the presence of three-dimensional epitaxial growth similar to those detailed in chapter 3. With increasing nominal thickness and increasing germanium composition, the magnitude of these corrugations seems to increase. Furthermore, the effect increases with proximity to the device surface. In addition to these stress-driven relaxation mechanisms, lens shaped germanium features reminiscent of those seen in the *TEMS* of chapter 3 (Fig. 3.15) can be seen in some layers.





Figure 5.10: *SEM* inspection images of wafers and devices (a) is a view of three devices showing successful metallisation onto device mesa (b) shows a perspective image of a rough epitaxial surface of a device mesa. (c) A planar view of a rough device mesa, (d, e and f) show cross-sections of device mesas.

The three-dimensional features can be attributed to surface segregation of Ge during formation of the $Si/Si_{1-x}Ge_x$ multilayer [22]. Self-assembled $Si_{1-x}Ge_x$ quantum dots are distinctly found in the thick devices (k2675-3 and -6), exhibiting an impressive vertical alignment that has been reported by a number of authors studying germanium quantum dots devices [109-111, 120-123].

Growth temperature has a large influence on the outcome of the epitaxial growth. With increased temperature, germanium adatoms have a higher probability of bonding to the same species because they have greater mobility on the surface and a greater density, making layer-by-layer epitaxial growth less likely. This situation enhances the probability of obtaining a layer-cluster growth mode, and this is likely to happen in lattice mismatched growth.

Figure 5.10 (b and c) demonstrate relatively poor epitaxial surfaces to the devices. The square trenches on the surface indicate surface damage that is likely to have originated from the ion-plantation prior to the epitaxial growth stages. The surface condition is very important for the epitaxial processes, as any surface imperfections can lead to three-dimensional growth, and this might further induce germanium segregation, as seen in figure 5.10(e,,f). These results highlight the difficulties associated with incorporating *Si/SiGe* epitaxy into any device process as growth surface imperfections will lead to poor device performance.

5.5.2 SiGe SIMS profiles

SIMS has been used to assess the germanium distributions in the devices (Fig. 5.11). These SIMS plots are characterised by much poorer resolution than those presented in chapter 3. Although for most samples, it is possible to resolve all ten germanium bands, while the deepest bands are most difficult to resolve. Although this lack of resolution might be a result of germanium diffusion, originated by rapid thermal activation (RTA) at 1100°C for 10secs, this is not supported by the SEM images that still indicate the existence of distinct germanium rich bands. However, the expansion of crest height into Si spacers (Fig 5.10e and f) may cause less Ge peak profiling in

the *SIMS* instrument. It results high *Ge* sputterings where the primeary ion impinge the *Si* spacer; this makes high *Ge* reading in the *Si* spacer. Therefore, the abrupt *Ge* profile is lost. Furthermore, it is most likely to be the surface roughness (of the epitaxial layers and the *BPSG* glass) that is leading to loss of resolution, and this issue becomes worse with increasing depth. In this context, it is best to use the first germanium peaks as an indication of the germanium concentration and quantum well width. Table 5.3 summarizes these findings.



(a)



(b)

Figure 5.11: The germanium SIMS profiles of devices.

Samplas	Ge contents (%)	Mean Si barrier	Mean SiGe layer	
Samples	(maximum)	L_b (nm)	L_{w} (nm)	
k2675-1	5.6	25±8	22.4 ± 4	
k2675-2	6	27.1±8	22.4 ± 7	
k2675-3	7.6	20.3 ± 10	27.5±3	
k2675-4	7	25.5 ± 4	25.8±3	
k2675-5	8.4	25.3±8	25.3±5	
k2675-6	11.5	20 ± 5	20.5 ± 6	

Table 5.3: The thicknesses of the silicon barrier and the thicknesses and germanium contents of the $Si_{1-x}Ge_x$ layers.

5.6 Electrical characterization of devices

Each of the 66 chip sites on each wafer was provided with test structures to allow steps in the fabrication process to be monitored. These test structures are designed to allow engineers to carry out preliminary evaluations of devices and fabrication processes. Two test structures were placed on each chip to allow impurity concentration measurements. It is known that high impurity concentrations are required for ohmic contacts and to provide low series resistance in a *p-i-n* diode. The test structures, used to assess carrier concentration measurements, consist of four large contact squares at each corner of a square region, containing the impurity concentration of interest. In these experiments, these resistivity test structures were included to allow measurement of the p^+ and n^+ regions of the *p-i-n* diode. Current-voltage measurements can be readily obtained and the resistivity, retrieved from $\rho=1/qn\mu_n$ or $\rho=1/qn\mu_p$, where ρ is the resistivity, and q, n, p, μ_n and μ_p are the electron charge, the *n* or *p*-type concentration, and the mobility of the electrons (1450 cm²/V-s) in silicon [16] respectively.

All regions were found to have high carrier concentrations with the centre of each wafer, having the largest carrier concentrations for both *n*- and *p*-type. High concentration *p*-type layers in the range 3×10^{19} cm⁻³ to 7×10^{20} cm⁻³ were obtained on every wafer. Meanwhile, slightly lower than expected *n*-type layers were found in the range 1×10^{19} cm⁻³ to 9×10^{19} cm⁻³. Variations are most likely due to non-uniformity in the silicon surfaces and oxide layers, particularly for the *n*-type region. Overall, the high concentrations for all wafers and in all areas are expected to produce diodes with good electrical behaviour.

5.6.1 Diode characteristic

Current-voltage measurements for the diode structures are taken using an HP4155Semiconductor device analyser, and some measurements are taken by using a probe station, and others were taken after wafer dicing and wire-bonding in a dual in-line (*DIL*) package. Figure 5.12 and 5.13 shows a number of *I-V* measurements for forward bias and reversed bias a number of chip sites, distributed around the wafer are represented.



Figure 5.12: The forward bias I/V characterisites of diodes for a distribution of chip sites on k2675-3.



Figure 5.13: The forward bias I/V characterisites of diodes for a distribution of chip sites on k2675-3.

Most of the devices that have been examined have exhibited diode behaviour, and the overall device design has been successfully implemented. This includes the fundamental p-i-n part of the structure as well as the formation of ohmic contacts, and inclusion of the guard-ring structure (appendix B). These achievements alone represent a great degree of success, as such promising results can not be assured at the start of new, long and complicated device batches. Nevertheless, the inconsistency of the *I*-*V* characteristic turn-on voltage from device to device is marked, and interesting.

In the first instance, it is interesting to consider a 2V turn-on voltage in silicon device since basic p-n junction theory would suggest that the built-in voltage should not exceed the band-gap. However, the basic theory does not generally incorporate a detailed consideration of carrier densities in the depletion region of a p-n junction. In these devices, the large and complex intrinsic regions will be regions of high carrier recombination, and this can add to the turn-on voltage.

The inconsistency of the turn-on voltage itself is, perhaps, due to the non-uniform epitaxial quality of the wafer. To investigate the influence of epitaxial quality on the I-V behaviour, the magnitude of the reverse current, or so called dark current, can be used as an indicator. For an ideal device the reverse saturation current should be low. However, defects or dislocations within the layer are likely to increase carrier generation. Therefore, high dark-current is likely to be found where there is defective epitaxy. Thus, studying the variations in the reverse biased I-V characteristic for different parts of the wafer surface can be used to probe the uniformity of the epitaxial layer.

In general, the best devices, with the lowest dark-current and the lowest turn-on voltage have been found at the centre of the wafer. Therefore, the centre-middle has been routinely used as a representative of each wafer for further electrical analysis.

5.6.2 Forward and reverse characteristics

The forward bias I/V characteristics for representative samples from all six wafers are shown in figure 5.14.



Figure 5.14: The forward current of fabricated devices.

Most of the devices have been found to have turn-on voltages in the 1.5 to 2.0V range. The two exceptions to this are the k2675-1 that turns on slowly from 2 to 2.5V and k2675-6 that turns-on remarkably early at around 0.2V.

Most devices demonstrate significant recombination at small forward bias (0-1.5V). This generally occurs in *p-i-n* diodes due to the large volume of the *i*-layer. Furthermore, a deposited intrinsic-layer is likely to add to the likelihood of recombination and generation centres in the device energy band if imperfect crystal structure is introduced. In *Si/SiGe*, such centres are readily created by miss-match dislocations.

Information, regarding the forward bias region of a p-*i*-n diode, can be analysed by considering the ideality factor (n) as this indicates the deviation of the device from the ideal diode behaviour. The ideality factor can be obtained from a plot of log(I) versus V. The slope obtained from the straight-line portion of the graph is represented by

 $S = d \log(1) / dV$, and it is used in the formula $n = \frac{1}{2.3SkT/q}$ [38] where the factor

2.3 accounts for the conversion from ln(I) to log(I), and kT/q is the thermal voltage. The quantities on the y-axis are derived from taking the logarithm of the measured current in the forward region, and they are plotted on a linear scale. The ideality factors (n) of the investigated devices are shown in table 5.4.

The *I/V* characteristics of the devices under reverse bias are shown in figure 5.15. The reversed currents saturate from about 5V, and are in range from 1×10^{-6} to 1×10^{-5} A. Again, *k2675-6* provides the most unusual devices with an early breakdown. The saturation currents (dark current) (*I_s*) at 1V are included in table 5.4.



Figure 5.15: The reversed current of fabricated devices.

Devices at 10 Si/SiGe layers	Saturation current	Ideality factor (n)
	(I_s) (mA) at 6V	
$Si_{0.944}Ge_{0.056}$ 22.4 nm ($k2675-1$)	0.99	1.98
$Si_{0.94}Ge_{0.06}$ 22.4 nm ($k2675-2$)	4.8	2
$Si_{0.924}Ge_{0.076}$ 27.5 nm ($k2675-3$)	3.0	5.7
$Si_{0.93}Ge_{0.07}$ 25.8 nm ($k2675-4$)	1.5	1.88
<i>Si_{0.916}Ge</i> _{0.084} 25.3 nm (<i>k</i> 2675-5)	1.6	4.82
<i>Si_{0.885}Ge_{0.115}</i> 20.5 nm (<i>k</i> 2675-6)	2.7	0.2

Table 5.4: Ideality factors of photodiodes.

The ideality factors (*n*) of the $Si/Si_{1-x}Ge_x$ devices are similar to those of typical silicon *p-i-n* devices where the value of the ideality factor is between 1 and 2. The actual value shows the influence of generation and recombination in the depletion region. Recombination current is indicated by n>2 and generation currents are represented by values n<1. From table 5.4, it seems that although there are some anomalous results (k2675-6), the ideality factor of the devices seems to increase with the thickness of the SiGe layer, indicating that recombination currents dominate the forward behaviour, and this increases with epitaxy thickness and epitaxial disorder.

The saturation currents (I_s) , all large seem to systematically increase as the SiGe thickness increases. This indicates that the Si/SiGe multilayer epitaxy in *i*-region of devices can give rise to the high saturation current, and this can be attributed to either defects or high carrier concentrations.

5.7 Summary

This chapter has described the fabrication and electrical characterisation of six photodetector wafers containing many devices. The demonstration of working devices from every wafer represents a success given the complexity of the fabrication sequence. Nevertheless, electrical characterisations also show tremendous unpredictability in the results. This is largely due to the inconsistency of the epitaxy growth from wafer to wafer and within different regions of the same wafer. In chapter 6, the best devices are assessed as photodetectors.

Chapter 6

Optical Characterisation of Photodetectors

This chapter examines the optical response of the photodetectors that have been fabricated. Chapter 6 highlighted significant variations in the electrical characteristics from device to device on the same wafer. In this chapter, the results obtained for the best performing devices are presented. At the end of the chapter, the results are evaluated in comparison to similar device reported by other authors.

6.1 Spectral Response

Equipment was designed to measure the photoconductivity of the devices (Fig. 6.1). A tungsten lamp serves as the light source. The light, then, passes through a chopper to provide an alternating optical signal. A grating monochromator placed next to the chopper produces a monochromatic beam that is directed onto the photodetector under test. The photodetector produces an AC electrical signal which is then fed into a preamplifier, amplified and then fed to a lock-in amplifier. The signal from the lock-in amplifier is fed to an analogue to digital converter, and the digital data is acquired by a computer.



Figure 6.1: Schematic diagram of the photoconductivity equipment.

Photodetector operation can be divided into three modes: the basic photovoltaic mode, the zero-bias mode, and the photoconductor mode. In the basic photovoltaic mode (Fig 6.2a), the photocurrent is generated flows through the diode, and causing the voltage across the device to be forward biased. The diode resistance decreases exponentially as the illumination increases.

In the zero-bias mode (Fig. 6.2b), the photocurrent flows through resistor (R_L). The operational amplifier is included in the configuration in order to decrease the load resistance and amplify the output signal. This circuit has a linear response and low noise due to the nearly complete elimination of leakage current.

In the photoconductive mode (Fig. 6.2c), a load resistor is placed parallel to a shunt resistance. With a fixed reverse bias, the diode resistance is largely constant. A large value of R_L can be used, and there is a linear response between the output and the applied radiation intensity. This is the most responsive configuration for photodetection and is required for high speed of devices. The disadvantage of this configuration is the increased leakage current due to the bias voltage as this produces higher noise than the other modes of operation.



Figure 6.2: The operational modes of p-*i*-n photodiode (a) photovoltaic mode, (b) zero-bias mode, and (c) photoconductive mode.

6.2 Photoresponse

Photocurrent spectra were measured for devices with 0.042 and 0.0025cm^2 areas under reversed biases of 1V. The spectral range was from 1000 to 1500nm, and the experiments were performed for devices at room temperature. There was no polarization control of the light, and the incident direction of the light was perpendicular to the substrate (normal incidence). The light beam was focused by a lens in order to focus all of the available light onto a single device on the chip. Preliminary spectra of representative devices from each of the 6 device wafers at 1V reverse bias are shown in figure 6.3 and 6.4. Figure 6.3 shows the 0.042cm^2 devices, and figure 6.4 shows 0.0025 cm² devices. Plots of the response of a similar all-silicon detector are shown for comparison.



Figure 6.3: Photocurrent spectra at 1V reverse bias of 0.042cm² devices.



Figure 6.4: Photocurrent spectra at 1V reversed bias of 0.0025cm² devices.

At room temperature, the long wavelength detection for all of the *Si/SiGe* devices reaches 1.3μ m. This is at least 50nm beyond the silicon device. The best devices demonstrate sensitivity up to 1360nm. Beyond 1.3μ m, the signals drop to a flat response as the sensitivity falls to zero, and the current at this point represents the dark current of the device. The device with the highest germanium content, k2675-6 (*Si_{0.885}Ge_{0.115}*) has the longest wavelength detection amongst the fabricated devices. The large and small detector areas show similar results. The indirect energy gap and phonon energy of the *Si_{1-x}Ge_x* multi-layers in each sample can be analysed using the *Macfarlane*'s model to fit the photocurrent spectra [124-127]. This approximation is

valid for very thin absorbing layers $\alpha d << 1$ with a condition that applies for these samples [125-127]. Figure 6.5 and 6.6 depicts the square-root of the measured photoresponse for devices from each wafer having areas of 0.042 and 0.0025cm².



Figure 6.5: The $(I_{ph} x h v)^{-1/2}$ spectra of some large device (0.042cm²) with -1V bias.



Figure 6.6: The $(I_{ph} x hv)^{-1/2}$ spectra of some devices (0.0025cm²) with -0.5V.

The photocurrent is related to the absorption coefficient by:

$$I_{ph} \propto (l - exp(-\alpha d)) / hv$$

for the devices under investigation, $d << l/\alpha$, so $I_{ph} \cdot hv$ is proportional to α . For indirect transitions, particularly at room temperature, both phonon absorption and phonon emission transitions are seen. At small photon energies, phonon absorption dominates the absorption coefficient, whereas both phonon processes are present at high photon energies. This condition, discussed in section 2.5 can be written mathematically as:

$$\alpha(h\nu) = \begin{cases} A_{l}(h\nu - E_{G} + E_{ph})^{2} at & E_{G} - E_{ph} \leq h\nu < E_{G} + E_{ph} \\ A_{l}(h\nu - E_{G} + E_{ph})^{2} + A_{2}(h\nu - E_{G} - E_{ph})^{2} at & h\nu \geq E_{G} + E_{ph} \end{cases}$$
(6.1)

Thus, plotting the square-root of $I_{ph} \cdot hv$, against energy produces two slopes (Fig. 6.7) [40] and E_G and E_{ph} can be estimated using the two energy intercepts. The intercept at low energy represents $E_G - E_{ph}$, while $E_G + E_{ph}$ is represented by the high photon energy intercept [124-128]. The energy gaps and phonon energies obtained from the data shown in figure 6.5 and 6.6 are shown in table 6.1.



Figure 6.7: A schematic of the experimental data fitting according to equation 6.1. Line 1 and line 2 represent the phonon absorption and phonon emission lines respectively.

Devices	Large	e device	Small device	
Devices	$E_g(eV)$	E _{ph} (meV)	E _g (eV)	E _{ph} (meV)
k2675-1 (Si _{0.944} Ge _{0.056} 22.4nm)	0.92	60	0.92	51.5
k2675-2 (Si _{0.94} Ge _{0.06} 22.4nm)	0.92	60	0.9	33.5
k2675-3 (Si _{0.927} Ge _{0.076} 27.5nm)	0.902	42.5	0.912	36.5
k2675-4 (Si _{0.93} Ge _{0.07} 25.8nm)	0.96	28	0.93	32
k2675-5 (Si _{0.916} Ge _{0.084} 25.3nm)	0.93	35	0.928	28
k2675-6 (Si _{0.885} Ge _{0.115} 20.5nm)	0.94	60	0.923	22.5

Table 6.1: Energy gap and phonon energy of devices.

The data from the large and small devices exhibit slight differences as a result of the different output currents and the inherent sensitivity of the fitting processes. In addition, if the photocurrent of the measured devices has a poor signal quality due to high noise, errors in the interpretation are likely to appear. In order to improve the accuracy of the interpretation, low temperature measurements would be helpful.

Nevertheless, the data is sufficient to draw a number of conclusions and to observe a number of interesting features.

The effective bandgaps of all of the devices are less than the silicon bandgap, indicating that the addition of germanium has reduced the effective bandgap of the overall structure. There is reasonably agreement between the large and small devices, giving some confidence in the fitting technique and device fabrication consistency. The obtained phonon energies are in the expected range of *Si-Si* and *Si-Ge* phonon energies although the data are a little different from the published values [27].

The modelled energy gap can be obtain from equation 2.15, suggesting the energy gap of available germanium content in samples as 1.049, 1.046, 1.034, 1.038, 1.026 and 1eV for k2675-1, -2, -3, -4, -5 and -6 respectively. These values are higher than those, determined by *SIMS* experiment (Table 6.2) and suggests that regions within the quantum dot nanostructures perhaps reach germanium compositions in the range x=0.2 to 0.25.

Daviana	Large device	Small device	Derived from the SIMS by Eq. 2.15
Devices	E _g (eV)	$E_{g}\left(eV ight)$	E _g (eV)
<i>k2675-1 (Si_{0.944}Ge_{0.056} 22.4nm)</i>	0.92	0.92	1.049
<i>k2675-2 (Si_{0.94}Ge_{0.06} 22.4nm)</i>	0.92	0.9	1.046
<i>k2675-3 (Si_{0.927}Ge_{0.076}</i> 27.5nm)	0.902	0.912	1.034
k2675-4 (Si _{0.93} Ge _{0.07} 25.8nm)	0.96	0.93	1.038
<i>k2675-5 (Si_{0.916}Ge_{0.084}</i> 25.3nm)	0.93	0.928	1.026
k2675-6 (Si _{0.885} Ge _{0.115} 20.5nm)	0.94	0.923	1

 Table 6.2: The comparison between the experimental fitted energy gap and approximation by using equation 2.15, applied with the SIMS profile.

The consistency of the final energy gap determination for all devices is intriguing. The bandgaps for all the devices are surprisingly low and surprisingly consistent regardless of the targeted thickness and compositional variations. This consistency seems to indicate the presence of a fundamental maximum limit to the germanium composition in all samples, or else a maximum limit to the "useful" germanium composition in all samples.

The phonon energies estimated from our devices provide a range of values. These energies can be used to indicate the relative distributions the *Si-Si*, *Si-Ge* and *Ge-Ge* atomic pairs within the structures according to the descriptions provided by *J. Weber* et al [27]. In our devices the phonon values are found to be close to those of *Si-Si* atomic pairs for thin $Si_{1-x}Ge_x$ layers, and found to be close to *Si-Ge* and *Ge-Ge* atomic pairs for the thick $Si_{1-x}Ge_x$ layers. This is mostly consistent with the device cross sections shown in figure 5.10. The data set here is not reliable enough to make strong conclusions, but seem supportive of the likelihood that the near-band edge absorptions are most likely to take place in localised areas where there are relatively large *Si-Ge* bond concentrations.

6.3 Quantum efficiency

The external quantum efficiency (η_{ext}) is obtained from the photocurrent spectral measurement, divided by the power of incident light at given wavelength as shown in equation 6.2. The quantum efficiency of the largest (0.042 cm^2) devices have been calculated at a wavelength of 1.3µm at room temperature for reverse bias of 0, 0.5, 1 and 2V (Fig. 6.8.)

$$\eta_{ext} = \frac{\left| J / q \right|}{P_{inc} / Ahv} \tag{6.2}$$

Where, J is photocurrent (A), q is electron charge (C), P_{inc} is power of incident light at given wavelength (W), A is the detector area (cm²), h is Planck constant (J-s) and v is wavelength (μ m). The ideal of external quantum efficiency is equal to unity.



(a)



(b)



The quantum efficiency increases most with reverse bias for devices with the highest germanium contents. The maximum efficiency at maximum bias of all the samples is an impressive 12%. Several mechanisms can add to this effect. Increasing the reversed bias can improve the quantum efficiency simply by extending the depletion region and increasing the field across the junction.

However, there is some evidence that the applied electric field raises the quantum efficiency because the band bending as a result of the electric field leads to a reduction in the energy gap [129, 130]. The energy gap reduction is inversely proportional to the applied electric field, and a tunnelling process can commence by photon assistance, known as the *Franz-Keldysh effect* [130].

The electroabsorption (*Franz-Keldysh* effect) is the enhanced absorption in a semiconductor as a result of an applied electric field. The band energy is bent as a result of electric field as shown in figure 6.9. The electrons from maximum valence band can tunnel to the conduction band minimum through tunnelling states. Initially, the electrons in the valence band occupy *tunnel states* when a strong electric field is applied to normal indirect transitions occurs and, thereby, enhance absorption.



Figure 6.9: The band energy diagram and the indirect transition through tunnelling states under strong electric field [130].
6.4 Responsivity

To provide deeper insight into the device performance, it is possible to consider the *responsivity* of the devices. Normalised responsivity is derived by scaling the whole photoresponse relative to the photoresponse at a wavelength of 1 μ m, thus the *responsivity* at 1 μ m becomes 1 and the relative efficiency of the longer wavelengths can be considered. In this way, some unwanted detection range is removed from the analysis, and the device performance can be directly compared to a silicon-only detector, and in this case, the quantum dot detectors reported by *Elkurdi et al*[94]. Plots of the normalised, responsivity of the large devices (0.042cm²), with a reverse bias of 1V under room temperature, are shown in figure 6.10 and 6.11. Responsivity values for each device at 1300nm are shown in table 6.3.







Figure 6.11: Normalised responsivity of devices k2675, -4, -5 and -6.

Device	Responsivity (A/W) at 1300nm
k2675-1	0.013
k2675-2	0.01
k2675-3	0.09
k2675-4	0.01
k2675-5	0.02
k2675-6	0.07
Si	0.00117
<i>Qdot</i> detector ref[94]	0.2

Table 6	.3:]	Raw	responsivity	value	at	1300nm	for	0.042 cm ²	devices	at	1V	reversed
bias.												

The responsivity data provide strong evidence that the performance of our *Si/SiGe* devices is better than standard silicon devices in the long wavelength regime. However, the performance is, so far, not as good as germanium quantum dot devices that have been reported [121, 131, 132].

6.5 Comparison with other published works

It is interesting as this stage to perform a number of comparative studies with published work that details alternative approaches to enhanced *IR*-absorbtion in silicon based devices. This allows a critical assessment of our *LPCVD* quantum well processes in comparison with other structures and techniques, which will allow a consideration of future work.

6.5.1 Devices based on virtual substrates.

Presting et al [8] at the *Daimler-Benz Research Centre* have used *MBE* to produce complex waveguide structures, which use $Si_{0.5}Ge_{0.5}$ buffer layers to provide high germanium content (Fig.6.12).



Figure 6.12: The epitaxial configurations of *Presting et al* [8].

The devices numbered B2804 and B2805 are waveguide detectors. Strain symmetrized Si (6nm thick) /Ge (4nm thick) superlattices were fabricated within both devices. B2804 has a $Si_{0.5}Ge_{0.5}$ surfactant buffer, while B2805 has a step-graded buffer. The waveguide channels are p-type $Si_{0.6}Ge_{0.4}$ of 400nm and 250nm thickness respectively. Normalised responses for k2675-3, k2675-4, a similar all-silicon device, and devices B2804 and B2805 of ref. [8] are compared by scaling the device data so that the noise levels of each are equal to unity (Fig. 6.13).



Figure 6.13: Comparison the normalised photocurrent between some of fabricated devices with some published data of *Presting et al* [8].

Device B2804 and B2805 shows the best performance, in terms of the longest wavelength sensitivity, with detection as far as 1400nm. This cut-off wavelength is 1400nm because of the $Si_{0.6}Ge_{0.4}$, a structure that can only be achieved with the use of strain symmetric growth on virtual substrates. However, we can see that the detection is already relatively weak at even 1300nm. This perhaps indicates that quantum well/dot structures show enhanced detection sensitivity because of the better interaction between light and confined states.

6.5.2 Devices based on quantum dots.

Wang et al [76] have reported on devices incorporating germanium quantum dots. In many ways reminiscent of the quantum dots, observed in the cross-section images, observed in chapter 2 (Fig. 2.23). This reference device consists of ten periods of Ge dot/Si multilayer, grown by *MBE* technique, in *i*-region of *p-i-n* junction. The device cross-section of device is shown in figure 6.14. A comparison plot is shown in figure 6.15.



Figure 6.14: The Ge dot cross-section of Ge dot device, captured from ref. [76].



Figure 6.15: Comparisons between devices and a published quantum dot device [76].

The data of Wang et al show a clear distinction between absorption that we can attribute to silicon and absorption, which can be attributed to the quantum dots. This quantum dot peak centred on 1400nm but homogenously broadened to allow detection upto 1500nm has been observed by other researchers [76, 133]. This is not observed as a strong feature in our devices. Though there is perhaps a little evidence of some signal for sample k_{2675-5} and -3. In the wavelength range 1200 to 1300nm, our quantum well samples show better relative sensitivity than the reference device. It seems that the quantum dot device structure is very well optimised to ensure that all of the germanium content is contained within self-organised germanium islands and perhaps a thin wetting layer that might explain the slight wavelength extension, compared to the silicon device. Perhaps the most impressive feature of the quantum dot device is the strength of the response at 1400nm, which is relatively large when the relative Si: Ge atomic ratio in the structure as a whole, and the signal is perhaps 3 orders of magnitude less and yet the total germanium must be the equivalent of less than 100 monolayers (10nm) within a micron. This is perhaps further evidence of enhanced interaction as a result of the presence of quantum confined energy states.

6.6 Summary

Our results and comparison with published work show that *LPCVD SiGe* quantum wells can be used to enhance the detection of silicon based photodetectors into the near infrared. However, it seems clear that quantum dot devices provide the best performance at long wavelengths because of the pure germanium regions, incorporated within the overall structure, and the enhanced interaction between light and quantum features, confined in three dimensions. Intriguingly, our structural characterisations have shown a strong natural tendency to form germanium islands though it is not clear if these islands are purely germanium or if they are germanium rich silicon-germanium. This evidence is corraborated by the presence of strong photoluminescence features in some samples and weak photodetection features in one or two devices.

We have also seen that our three dimensional growth features have potentially led to the formation of structural defects that potentially act to inhibit carrier collection in the regions of high carrier concentration as a result of recombination. Our devices seem to be dominated by quantum-well rather than quantum-dot behaviour and it seems likely that this is self-limiting and our growth conditions have a maximum germanium content that can be achieved within a quantum well. At germanium contents beyond these maximum regions, the three-dimensional growth appear. The final results are quantum well detectors that have extended responsivity to a consistent limit of around 1300nm and relatively poor and non-uniform device performance.

In spite of these difficulties, this work shows that *LPCVD* can be used to produce near-infrared photodetectors, and with further optimisation of the epitaxial growth stages, it is likely that both quantum well and quantum dot structures could be deposited without the formation of defects as a result of strain relaxation.

Chapter 7

Conclusion and Future Work

This project represents the first attempt to fabricate Si/SiGe quantum well and quantum dot infrared photodetectors, using Southampton's unique LPCVD epitaxial growth apparatus. Although Southampton has a successful track record in the fabrication of Si/SiGe based electronic devices, the fabrication of quantum well based optoelectronic devices was always going to represent a major challenge certain to test the limits of the LPCVD systems in terms of thickness, composition and reproducibility. In addition to this, the realisation of efficient devices would require optical-quality epitaxy that would in turn require structural perfection and compositional purity. Beyond epitaxy, this project required the design of new device fabrication sequences and the commissioning of new characterisation apparatus. At the end of this project it is clear that each of these issues has proven challenging and although much has been achieved, much work is still required in order to understand and fully optimise the fabrication of efficient near-IR devices. It has not, as had been initially hoped, been possible to attempt the fabrication of quantum well or quantum dot infrared photodetectors based on intersubband transitions or quantum cascade lasers. To achieve success in these greater challenges, much more access to epitaxial growth equipment would be required, which is hard to achieve in a busy facility making many types of different devices. Even then, this project would certainly have made much greater progress, but for a very serious fire that destroyed a near-complete second generation of quantum dot photodetectors and all of the epitaxy and characterisation equipment that was being used.

This project has successfully demonstrated the epitaxial growth of defect free Si/SiGe pseudomorphic quantum well structures with excellent reproduction of features of ~20nm features and germanium compositions between 6 and 12%. Attempts to maximise germanium content have shown an unexpected tendency for germanium to form islands of material with high germanium content. TEM studies indicate that these islands are likely to be quantum dots formed by the Stranski-Krastanov growth mode. Photoluminescence measurements have demonstrated that excellent optical quality material can be produced by cold-wall LPCVD systems. The photoluminescence studies have shown features that can be attributed to excitonic emission from both quantum wells and quantum dots. The epitaxial developments have allowed the fabrication of Si/SiGe p-i-n photodetectors with detection sensitivity extending significantly beyond the normal detection range of silicon. The band-edge is seen to be extended by quantum well absorption to 1350nm. There is even weak evidence of photodetection as a result of quantum dot absorption at around 1500nm.

A number of aspects of the work could have been improved, and it had been possible to re-examine some devices or some growth features, or if some additional equipment had been available. For more accurate compositional analysis and strain measurement, X-ray diffraction and Raman spectroscopy could be used in conjunction with SIMS. Obtaining high quality *TEM* images has remained a difficult task, sample preparation in particular has posed many difficulties. This matter could be significantly improved with improved preparation techniques and focussed ion beam milling process. Photoluminescence excitation spectroscopy (*PLE*) could have allowed analysis of alloy inhomogeneties in $Si_{1-x}Ge_x$ system and could provide greater insight into both intentional and unintentional impurity concentration. It would also be interesting to use deep infrared light sources in conjunction with photoconductivity measurements at low temperature to explore intersubband transitions. Low temperature photodetection (77K) and/or more intense light sources would have allowed a greater insight into the devices fabricated.

Looking at the broader perspective, it is clear that the wider research community around the world finds *Si/SiGe* epitaxy of quantum features with optical quality a challenging issue. *SiGe* quantum well photodetectors are not routinely placed on *VLSI* devices, and although many theoretical works have proposed interesting devices, comparatively, little progress has been made. It is possible to predict theoretical devices based on ideal silicon, and yet in reality, silicon is complicated, and it is hard to make ideal silicon. Silicon epitaxy is destroyed by relatively small quantities of oxygen or water vapour, and this is costly in that machine maintenance and conditioning become time consuming issues. In addition, the epitaxial growth of silicon requires high growth temperatures, and this places particular demands on epitaxial growth apparatus. The heating that allows epitaxy also causes the release of impurities such as carbon and iron that are often sufficient to prevent defect free epitaxial growth and nearly always sufficient to impact optical properties. Often, it is preferable to grow silicon quickly so that impurities are diluted, and this in itself makes the deposition of thin features difficult. Finally, with a large difference between the lattice constants of silicon and germanium, band-engineering is much more difficult than it is within other semiconductor systems, although this miss-match can actually help by providing strain that allows self-forming quantum dots. Overall, silicon germanium optoelectronic devices will continue to be of interest to the research community. However, it will perhaps take a significant investment in a new generation of high-specification deposition tools and a sustained research effort.

References

- Sze, S.M., Semiconductor Devices Physics and Technology. 2 ed. 2002: John Wiley & Sons, Inc.
- 2. Wilson, J. and J. Hawkes, *Optoelectronics an Introduction* 1998, Prentice-Hall Europe. p. 2.
- Paul, D.J., Silicon-Germanium Strained Layer Materials in Microelectronics. Advanced Materials, 1999. 11(3): p. 191-203.
- 4. Nijs, J.F.A., Advanced Silicon & Semiconducting Silicon-Alloy Based Materials & Devices, in Advanced Silicon & Semiconducting Silicon-Alloy Based Materials & Devices. 1994, Institute of Physics Publishing p. 185.
- Herbert, D.C., Theory of SiGe Waveguide Avalanche Detectors Operation Operation at λ=1.3μm IEEE Transaction on Electron Devices, 1998. 45(4): p. 791-796.
- Li, B., Monolothic Integration of a SiGe/Si modulator and multiple quantum well photodetector for 1.55μm operation Appl. Phys. Lett., 1998. 73(24): p. 3504-3505.
- 7. Loudon, A.Y., Enhancement of the infrared detection efficiency of Silicon photon-counting avalanche photodiodes by use of Silicon Germanium absorbing layers. Optics Letters, 2002. 27(4): p. 219-221.
- Presting, H., Near and mid infrared silicon/germanium based photodetection. Thin Solid films, 1998. 321: p. 186-195.
- Lafontaine, H., Growth of undulating Si_{0.5}Ge_{0.5} layers for photodetectors at 1.55 µm J. Appl. Phys., 1999. 86(3): p. 1287-1291.
- Presting, H., Novel mid-infrared silicon/germanium detector concepts. Opt. Eng., 2000. 39(10): p. 2624-2641.
- 11. Ribordy, G., *Performance of InGaAs/InP avalanche photodiodes as gatedmode photon counters*. Applied Optics, 1998. **12**: p. 2272-2277.
- 12. Etteh, N.E.I. and P. Harrison, the role of sequential tunnelling in the dark current of quantum well infrared photodetectors (QWIPs) Superlattices and Microstructures, 2001. **30**(5).
- 13. Harrison, P. The physics of THz QWIPs. in ninth International Conference on Terahertz Electronics. 2000.

- Ettrh, N.E.I. and P. Harrison, Carrier Scattering Approach to the Origins of Dark current in Mid- and Far-Infrared (Terahertz) Quantum-Well Intersubband Photodetectors (QWIPs). IEEE Journal of Quantum Electronics, 2001. 37(5): p. 672-675.
- Ashburn, P., Materials and technology issues for SiGe heterojunction bipolar transistors. Material Science in Semiconductor Processing, 2001. 4: p. 521-527.
- SZE, S.M., Semiconductor Devices Physics and Technology. 1985, John Wileys & Sons. p. 301-304.
- 17. Kajikawa, Y. and S. Noda, Growth mode during initial stage of chemical vapor deposition. Applied Surface Science 2004. 245: p. 281-289.
- Brune, H., Encyclopedia of Materials: Science and Technology. 2001: Elsevier Science Ltd. pp. 3683-3693
- 19. Nakajima, K., et al., *Phase diagram of growth mode for the SiGe/Si* heterostructure system with misfit dislocations. Journal of Crystal Growth, 2004. **260**: p. 372-383.
- Lee, I.M., Kinetics and Modelling of Low Pressure Chemical Vapour Deposition of Si_{1-x}Ge_x Epitaxial Thin films Chemical Engineering Science, 1996. 51(11): p. 2681-2686.
- SZE, S.M., *Physics of Semiconductor Devices*. 1981, John Wileys & sons. p. 850-851.
- 22. Kasper, E., Properties of Strained and Relaxed Silicon Germanium 1995, INSPEC publication. p. 17-26.
- Forster, M., et al., *Electroluminescence, photoluminescence, and photocurrent studies of Si/SiGe p-i-n heterostructures.* J. Appl. Phys., 1996. 80(5): p. 3017-3023.
- Nayak, D.K., et al., Band-edge photoluminescence of SiGe/strained-Si/SiGe type II quantum wells on Si(100). Appl. Phys. Lett., 1993. 63(25): p. 3509-3511.
- Konle, J., et al., Enhanced performance of silicon based photodetectors using silicon/germanium nanostructures. Solid-State Electronics, 2001. 45: p. 1921-1925.
- 26. Braunstein, R., A.R. Moore, and F. Herman, *Intrinsic Optical Absorption in Germanium-Silicon Alloys*. Physical Review, 1958. **109**(3): p. 695-710.

- Weber, J. and M.I. Alonso, Near-band-gap photoluminescence of Si-Ge alloys. Physical Review B, 1989. 40(8): p. 5683-5693.
- People, R., Physics and Application of Ge_xSi_{1-x}/Si Strained Layer Heterostructures. IEEE Journal of Quantum Electronics, 1986. QE-22(9): p. 1696-1710.
- 29. Bean, J.C., Silicon-Based Semiconductor Heterostructures: Column IV Bandgap Engineering. Proceedings of the IEEE, 1992. 80(4): p. 571-587.
- 30. Robbins, D.J., et al., Near-band-gap photoluminescence from pseudomrphic Si_{1-x}Ge_x single layers on silicon. J. Appl. Phys., 1991. **71**(3): p. 1407-1414.
- Sturm, J.C., et al., Well-Resoleved Band-Edge Photoluminescence of Excitons Confined in Strained Si_{1-x}Ge_x Quantum Wells. Physical Review Letters, 1991.
 66(10): p. 1362-1365.
- 32. Sturm, J.C., et al., High Temperature (77-300K) Photo- and Electroluminescense in Si/Si_{1-x}Ge_x Heterostructures. Jpn. J. Appli. Phys., 1994. 33: p. 2329-2334.
- Chen, H., et al., Luminescence study of band gap conversion in the SiGe material. Appl. Phys. Lett., 1997. 71(11): p. 1555-1557.
- Lang, D.V., et al., Measurement of band gap of Ge_xSi_{1-x}/Si strained-layer heterostructures. Appl. Phys. Lett., 1985. 47(12): p. 1333-1335.
- 35. Robbins, D.J., et al., Absorption in p-Si_{1-x}Ge_x quantum well detectors. Appl.
 Phys. Lett., 1995. 66(12): p. 1512-1514.
- 36. Krishnamurthy, S., A. Sher, and A.B. Chen, *Band structures of Si_xGe_{1-x} alloys*.
 Physical Review B, 1986. 33(2): p. 1026-1035.
- 37. Kittle, C., Introduction to solid state Physics 1996, John Wiley & Sons. p. 99-111, 312-316.
- Schroder, D.K., Semiconductor material and device characterization. 1990: John Wiley & Sons Ins.
- Bhattacharya, P., Semiconductor Optoelectronic Devices. second ed. 1997: Prentice Hall.
- 40. Pankove, J.I., *Optical Process in Semiconductors*. 1971, Dover publication. p. 10-14.
- Sturm, J.C., et al., Band-edge exciton luminescence from Si/strained Si₁.
 xGex/Si structures. J. Vac. Sci. Technol. B, 1992. 10(4): p. 1998-2001.

- 42. Fukatsu, S., N. Usami, and Y. Shiraki, Luminescence from Strained Si_{1-x}Ge_x/Si Quantum Wells Grown by Si Molecular Beam Epitaxy. Jpn. J. Appli. Phys., 1993. 32: p. 1502-1507.
- 43. Terashima, K., M. Tajima, and T. Tatsumi, Near-band-gap photoluminescence of Si_{1-x}Ge_x alloys grown on Si(100) by molecular beam epitaxy. Appl. Phys. Lett., 1990. 57(18): p. 1925-1927.
- Walle, C.G.V.d. and R.M. Martin, *Theoritical calculation of heterojunction discontinuities in the Si/Ge system*. Physical Review B, 1986. 34(8): p. 5621-5634.
- 45. Colombo, L., R. Resta, and S. Baroni, *Valence-band offsets at strained Si/Ge interfaces.* Physical Review B, 1991. **44**(11): p. 5572-5579.
- 46. People, R. and J.C. Bean, Band alignment of coherently strained Ge_xSi_{1-x}/Si heterostructures on <001> Ge_ySi_{1-y} substrates. Appl. Phys. Lett., 1986. 48(8): p. 538-540.
- 47. Manku, T. and A. Nathan, *Energy-band structure for strained p-type Si_{1-x}Ge_x*.
 Physical Review B, 1991. 43(15): p. 12634-12637.
- 48. Kurdi, M.E., et al., Comparison between 6-band and 14-band k p formalisms in SiGe/Si heterostructures. Physical Review B, 2003. 68: p. 165333-1-165333-16.
- 49. Dutartre, D., et al., Excitonic photoluminescence from Si-capped strained Si₁₋
 xGex layers. Physical Review B, 1991. 44(20): p. 11525-11527.
- 50. Abstreiter, G., et al., Strained-Induced Two-Dimensional Electron Gas in Selectively Doped Si/Si_xGe_{1-x} Superlattices. Physical Review Letters, 1985.
 54(22): p. 2441-2444.
- 51. Nauka, K., et al., Admittance spectroscopy measurements of band offsets in Si/Si_{1-x}Ge_x/Si heterostructures. Appl. Phys. Lett., 1991. 60(2): p. 195-197.
- 52. Gailev, V.I., et al., *Realistic continuum hole states in Si-SiGe quantum wells*. IEEE Journal of Quantum Electronics, 1997: p. 333-336.
- 53. Ni, W.X., J. Knall, and G.V. Hansson, New method to study band offsets applied to strained Si/Si_{1-x}Ge_x(100) heterojunction interfaces. Physical Review B, 1987. 36(14): p. 7744-7747.
- 54. Rack, M.J., et al., Characterization of strained silicon quantum wells and $Si_{1-x}Ge_x$ heterostructures using Auger electron spectroscopy and spreading

resistance profiles of bevelled structures. Semicond. Sci. Technol., 2000. **15**: p. 291-296.

- 55. Birman, J.L., Space Group Selection Rules: Diamond and Zinc Blende. Physical Review, 1962. 127(4): p. 1093-1106.
- 56. Mitchard, G.S. and T.C. McGill, *Photoluminescence of Si-rich Si-Ge allopys*.
 Physical Review B, 1982. 25(8): p. 5351-5363.
- 57. Boucaud, P., et al., *Photoinduced infrared spectroscopy of bound-to-bound* and bound-to-continum transitions in SiGe/Si quantum wells. Superlattices and Microstructures, 1996. **19**(1): p. 33-38.
- 58. Corbin, E., et al., Optical spectra and Auger recombination in SiGe/Ge heterostructures in 10 μm range of wavelengths. Superlattices and Microstructures, 1996. 19(1): p. 25-32.
- 59. Fujita, K., et al., Intersubband absoprtion in narrow Si/SiGe multiple quantum wells without interfacial smearing. Appl. Phys. Lett., 1992. 61(2): p. 210-212.
- 60. Kruck, P., et al., *Polarization-dependent intersubband absorption and normalincidence infrared detection in p-type Si/SiGe quantum wells.* Superlattices and Microstructures, 1998. **23**(1): p. 61-66.
- 61. Liu, J.L., et al., Intersubband absorption in boron-doped multiple Ge quantum dots. Appl. Phys. Lett., 1999. 74(2): p. 185-187.
- 62. Okhovat-Alavian, S.M.J., A. Afzali-Kusha, and M. Kamarei. Intersubband Transitions in Different Structures of Conduction-Band Quantum Wells. in The 12th International Conference on Microelectronics. 2000. Tehran.
- 63. Polleux, J.L. and C. Rumelhard, *Optical Absorption Coefficient Determination* And Physical Modelling of Strained SiGe/Si Photodetectors. IEEE, 2000: p. 167-172.
- Mitin, V.V., V.A. Kochelap, and M.A. Stroscio, *Quantum Heterostructure Microelectronics and Optoelectronics*. 1999, Cambridge University Press. p. 73-106.
- 65. Cheng, J.P., Cyclotron resonances studies in boron-doped multiplt Ge quantum dots. Appl. Phys. Lett., 1993. 62(13): p. 1522-1524.
- 66. Dresselhaus, G., A.F. Kip, and C. Kittle, Cyclotron Resonance of Electrons and Holes in Silicon and Germanium Crystals. Physical Review, 1955. 98(2): p. 368-384.

- 67. Dresselhaus, G., et al., *Cyclotron Resonance in Ge-Si Alloys*. Physical Review, 1955: p. 1218--1219.
- Yang, L., et al., Si/ SiGe heterostructure parameters for device simulations. Semicond. Sci. Technol., 2004. 19: p. 1174-1182.
- 69. Corbin, E. and M. Jaros, *Optimized SiGe/Si multiple quantum wells for detector applications*. Semicond. Sci. Technol., 1997. **12**: p. 1641-1649.
- 70. Rivas, C. and R. Lake. Three-Dimensional, Full-Band Quantum Modeling of Electron and Hole Transport through Si/SiGe Nano-Structures. in Proceeding of NanoTech. 2003. San Francisco, CA.
- 71. Corbin, E., et al., *Absorption and Recombinaton in p-type SiGe quantum well structures*. Superlattices and Microstructures, 1994. **16**(349-352).
- 72. Crow, G.C. and R.A. Abram, *Monte Carlo simulations of hole transport in SiGe and Ge quantum wells*. Semicond. Sci. Technol., 2000. 15: p. 7-14.
- 73. Dvurechenskii, A.V., A.V. Nenashev, and A.I. Yakimov, *Electronic structure* of Ge/Si quantum dots. Nanotechnology, 2002. **13**: p. 75-80.
- Jain, S.C., Gemanium-Silicon Strained Layers and Heterostructures. Advanced in Electronics and Electron Physics, ed. P.W. Hawkes and B. Kazan. Vol. 24. 1994: Academic Press.
- 75. Elkurdi, M., et al., *Electromodulation of the interband and intraband absorption of Ge/Si self-assembled islands*. Physica E, 2003. **16**: p. 450-454.
- 76. Wang, K.L., S. Tong, and H.J. Kim, *Properties and application of SiGe nanodots*. Material Science in Semiconductor Processing, 2005. **8**: p. 389-399.
- Bonar, J.M., J. Schiz, and P. Ashburn, Selective and non-selective growth of self-aligned SiGe HBT structures by LPCVD epitaxy. Journal of Materials Science: Materials in Electronics, 1999. 10: p. 345-349.
- 78. Mubarek, H.A.W.E., et al., Non-selective growth of SiGe heterojunction bipolar transistor layers at 700°C with dual control of n- and p-type dopant profiles. Journal of Materials Science: Materials in Electronics, 2003. 14: p. 261-265.
- 79. Dilliway, G.D.M., et al., Self-assembled germanium islands grown on (001) silicon substrates by low-pressure chemical vapor deposition. Journal of Materials Science: Materials in Electronics, 2003. 14: p. 323-327.

- Dilliway, G.D.M., et al., Structural and Compositional Evolution os Self-Assembled Germanium Islands on Silicon (001) During Growth Rate LPCVD. Mat. Res. Soc. Symp. Proc., 2003. 775: p. P9.25.1-P9.25.6.
- Mitrovic, I.Z., et al., *Review of SiGe HBTs on SOI*. Solid-State Electronics, 2005. 49: p. 1556-1567.
- Schiz, J.F.W., et al., Leakage Current Mechanisms in SiGe HBTs Fabricated Using Selective and Nonselective Epitaxy. IEEE Transaction on Electron Devices, 2001. 48(11): p. 2492-2499.
- 83. Bain, M., et al., SiGe HBTs on Bonded SOI Incorporating Buried Silicide Layers. IEEE Transaction on Electron Devices, 2005. **52**(3): p. 317-324.
- 84. Waite, A.M., et al., Raised source/drains for 50 nm MOSFETs using a silane/dichlorosilane mixture for selective epitaxy. Solid-State Electronics, 2005. 49: p. 529-534.
- 85. Sulaiman, N. and P. Ashburn. *Feasibility study on vertical CMOS gates*. in *ICSE2000 Proceeding*. 2000: IEEE international.
- Osman, K., et al., Confined epitaxial growth by low-pressure chemical vapor deposition. Journal of Materials Science: Materials in Electronics, 2003. 14: p. 257-260.
- 87. Bonar, J.M., Process Development and Characterization of Silicon and Silicon-Germanium Grown in a Novel Single-Wafer LPCVD System, in Electronics and Computer Sciences. 1995, University of Souhampton: Southampton p. 114-117.
- 88. Bozzo, S., Chemical vapor deposition of silicon-germanium heterostructures. Journal of Crystal Growth, 2000. 216: p. 171-184.
- 89. Fukatsu, S., et al., Spectral blue shift of photoluminescence in strained-layer
 Si_{1-x}Ge_x/Si quantum well structures grown by gas-source Si molecular beam epitaxy. Appl. Phys. Lett., 1992. 61(7): p. 804-806.
- 90. Fukatsu, S., et al., Quantum Size Effect of Excitonic Band-Edge Luminescense in Strained Si_{1-x}Ge_x/Si Molecular Beam Epitaxy. Jpn. J. Appli. Phys., 1992. 31: p. L1319-L1321.
- 91. Shiraki, Y., et al., Formation and optical properties of SiGe/Si quantum structures. Applied Surface Science, 1996. 102: p. 263-271.

- 92. Shiraki, Y. and S. Fukatsu, Investigation of luminescence in strained SiGe/Si modulated quantum well and wire structures. Semicond. Sci. Technol., 1994.
 9: p. 2017-2024.
- Bauer, G., A.A. Darhuber, and V. Holy, Self-assembled Germanium-dot multilayers embedded in Silicon. Cryst. Res. Technol., 1999. 34(2): p. 197-209.
- 94. Elkurdi, M., et al., Silicon-on-insulator waveguide photodetector with Ge/Si self-assembled islands. J. Appl. Phys., 2002. 92(4): p. 1858-1861.
- 95. Strong, R., et al., Ge_xSi_{1-x} infrared detectors I. Absorption in multiple quantum well and heterojunction internal photoemission structures. J. Appl. Phys., 1997. 82(10): p. 5191-5198.
- 96. Tong, S., et al., *Tunable normal incidence Ge quantum dot midinfrared detectors*. J. Appl. Phys., 2004. **96**(1): p. 773-776.
- 97. Palfinger, G., et al., *Absorption measurement of strained SiGe nanostructures deposited by UHV-CVD*. Physica E, 2002. **2**.
- 98. Tsai, C., et al., Growth and characterization of undoped and in situ doped Si₁.
 _xGe_x on patterned oxide Si substrates by very low pressure chemical vapor deposition at 700 and 625C. J. Appl. Phys., 1991. 69(12): p. 8158-8163.
- 99. Suzuki, S. and T. Itoh, Epitaxial growth of Si-Ge layers on Si substrates by plasma dissociation of SiH₄ and GeH₄ mixture. J. Appl. Phys., 1983. 54(11): p. 6385-6389.
- Bremond, G., et al., Photoluminescence characterization of Si_{1-x}Ge_x relaxed "pseudo-substrates" grown on Si. Journal of Crystal Growth, 1995. 157: p. 116-120.
- 101. Usami, N., Y. Shiraki, and S. Fukatsu, Intense photoluminescence from Sibased quantum well structures with neighboring confinement structure. Journal of Crystal Growth, 1995. 157: p. 27-30.
- 102. Fukatsu, S., et al., *Time-resolved dislocation-related luminescence in strainrelaxed SiGe/Si*. Thin Solid films, 1997. **294**: p. 33-36.
- 103. Vescan, L., et al., Optical and structural investigation of SiGe/Si quantum wells. Appl. Phys. Lett., 1992. 60(18): p. 2183-2185.
- 104. Xiao, X., et al., Quantum confinement effects in strained siliocn-germanium alloy quantum wells. Appl. Phys. Lett., 1992. 60(17): p. 2135-2137.

- 105. Dunbar, A., et al., The effect of strain field seeding on the epitaxial growth of Ge islands on Si(001). Appl. Phys. Lett., 2001. 78(12): p. 1658-1660.
- 106. Vescan, L., SiGe nanostructures by selective epitaxy and self-assembling Material Science & Engineering A, 2001. 302: p. 6-13.
- Dunbar, A., et al., Structural Compositional and Optical Properties of Self-Organised Ge Quantum Dots. Phys. stat. sol. (b), 2001. 224(1): p. 265-269.
- 108. Dunbar, A., *Strain seeding of Ge quantum dots Grown on Si (001)*. Phys. stat. sol. (b), 2001. 224(1): p. 265-269.
- Schittenhelm, P., M. Gail, and G. Abstreiter, Self-organized MBE growth of Ge-rich SiGe dots on Si(100). Journal of Crystal Growth, 1995. 157: p. 260-264.
- Schittenhelm, P., et al., Photoluminescence study of the crossover from twodimensional to three-dimensional growth for Ge on Si(100). Appl. Phys. Lett., 1995. 67(9): p. 1292-1294.
- Tang, Y.S., et al., *Photoluminescence and Raman spectroscopy of Si/Si_{1-x}Ge_x quantum dots*. Journal of Crystal Growth, 1995. 157: p. 280-284.
- 112. Brunner, J., et al., *Local Epitaxy of Si/SiGe wires and dots*. Journal of Crystal Growth, 1995. **157**: p. 270-275.
- 113. Apetz, R., et al., *Photoluminescence and electroluminescence of SiGe dots fabricataed by island growth.* Appl. Phys. Lett., 1994. **66**(4): p. 445-447.
- 114. Lyon, S.A., D.L. Smith, and T.C. McGill, *Thermodynamic Determination of Work Functions of Bound Multiexciton Complexes*. Physical Review Letters, 1977. 41(1): p. 56-60.
- 115. Robbins, D.J., P. Calcott, and W.Y. Leong, *Electroluminescence from a pseudomorphic Si_{0.8}Ge_{0.2} alloy.* Appl. Phys. Lett., 1991. **59**(11): p. 1350-1352.
- 116. Presting, H., et al., Room-temperature luminescence from Si/Ge single quantum well diodes grown by molecular beam epitaxy. Journal of Crystal Growth, 1995. 157: p. 15-20.
- 117. Misra, R., D.W. Greve, and T.E. Schlesinger, *Infrared absorption in Ge_xSi_{1-x} quantum wells*. Appl. Phys. Lett., 1995. **67**(17): p. 2548-2550.
- 118. Patella, F., et al., *Self-assembly if InAs and Si/Ge quantum dots on structured surfaces.* Journal of Physics: Condensed Matter, 2004. **16**: p. 1503-1534.

- Kermarrec, O., Y. Campidelli, and D. Bensahel, ABAB organization of Ge/Si(001) islands in multiplanes grown with loe pressure chemical vapor deposition. J. Appl. Phys., 2004. 96(11): p. 6175-6182.
- 120. Elkurdi, M., et al., Near-infrared waveguide photodetector with Ge/Si selfassembled quantum dots. Appl. Phys. Lett., 2002. 80(3): p. 509-511.
- 121. Kurdi, M.E., et al., Silicon-on-insulator and SiGe waveguide photodetectors with Ge/Si self-assembled islands. Physica E, 2002. 2: p. 1-5.
- 122. Rappaport, N., et al., *Photoconductivity of Ge/Si quantum dot photodetectors*. Infrared Physics & Technology, 2003. 44: p. 513-516.
- 123. Tang, Y.S., et al., Room temperature electroluminescence of nanofabricated Si-Si_{1-x}Ge_x quantum dot diodes. Superlattices and Microstructures, 1996.
 20(4): p. 505-511.
- 124. Macfarlane, G.G., et al., Fine Structure in the Absorption-Edge Spectrum of Si. Physical Review, 1958. 111(5): p. 1245-1254.
- 125. Li, C., et al., A study of Si_{1-x}Ge_x/Si quantum-well intermixing by photocurrent spectroscopy. Thin Solid films, 2000. **359**: p. 236-238.
- 126. Vonsovici, A., et al., Room Temperature Photocurrent Spectroscopy of SiGe/Si p-i-n Photodiodes Grown by Selective Epitaxy. IEEE Transaction on Electron Devices, 1998. 45(2): p. 538-542.
- 127. Murtaza, S., Room Temperature Electroabsorption in a Ge_xSi_{1-x} PIN Photodiode. IEEE Journal of Quantum Electronics, 1994. 41(12): p. 2297-2300.
- 128. Macfarlane, G.G. and V. Roberts, *Infrared Absorption of Silicon Near the Lattice Edge*. Physical Review, 1955: p. 1865-1866.
- Qasaimeh, O., J. Singh, and P. Bhattacharya, Electroabsorption and Electrooptic Effect in SiGe-Si Quantum Wells: Realization of Low-Voltage Optical Modulators. IEEE Journal of Quantum Electronics, 1997. 33(9): p. 1532-1536.
- Wendland, P.H. and M. Chester, *Electric Field Effects on Indirect Optical Transitions in Silicon*. Physical Review, 1965. 140(4A): p. 1384-1390.
- 131. Kurdi, M.E., et al., Near-infrared waveguide photodetector with Ge/Si selfassembled quantum dots. Appl. Phys. Lett., 2002. **80**(3): p. 509-511.
- 132. Kurdi, M.E., et al., Silicon-on-insulator waveguide photodetector with Ge/Si self-assembled islands. J. Appl. Phys., 2002. 92(4): p. 1858-1861.

 Zhu, W., Q. Shen, and S. Liu, *Photovoltage Spectroscopy Study of Ge_xSi_{1-x}/Si* Superlattices. Superlattices and Microstructures, 1993. 13(2): p. 275-277.

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Appendix A

Silicon photodetectors

Silicon was used for this device generation in order to optimise and test designed photodiode fabrication sequence. These devices were fabricated by planar process provided by *SUMC*. These samples were formed as a mesa on silicon substrates by using epitaxy process (*LPCVD*), and mesa thickness was designed to have three different thicknesses, which was 1.5, 2.0 and 2.5µm on wafer no.1, no.2 and no.3 respectively. Mesa areas were defined by the set of masks, designed into 5 different dimensions as 500×500 , 100×100 , 50×50 , 10×10 , and $5 \times 5µm^2$ with *KOH* wet etching. *P-i-n* structure was used as device configurations due to *i*-region modifiable advantage and good light absorption enhancement. Both high dope regions were formed by ion implantation technique in order to achieve shallow junction.

A1 Devices Fabrication

Sequence of fabrication processes can be summarised as: <100> plane *p*-type substrates were doped with *p*-type substance by ion implantation technique. Thin oxide deposition was needed before in order to protect surface damage from ion impingement and control shallow junction as shown in figure A1.



Figure A1. The device after p^+ processes.

Wafers were brought to oxide etching and *RCA* clean before epitaxy process began. Silicon epitaxial layer was grown on the surface of substrate with different thickness according to the designs. Ion implantation process took place again for achieving high *n*-type doping cap layer through thin oxide protection. The p-*i*-*n* structures were finished by these sequences as shown in figure A2.



Figure A2. The device after epitaxy and n^+ layer processes

The protect oxide was etched away by 7:1 *BHF*, and new oxide layer was deposited by *LTO* technique in order to make passivation layer. Mesa definition was done by photolithography technique with set of masks. Active area mask, first mask, was processed and developed on wafer surface. Consecutively, wet oxide etching process was used to etch oxide layer surrounding the mesa. At this moment, wafers were exposed silicon only round active area, covered by mask. Then, the mesa was prepared for the next silicon etching process by photoresist striping and cleaning with fuming nitric acid. Silicon etching was provided by *KOH* substance.

A few photolithography processes were carried on wafers in order to define contact windows and metal pads. Wafers with mesa were cleaned by *RCA* clean and deposited oxide on top again. Photoresists on wafers were striped and cleaned again by fuming nitric acid. Before metal process begin, pre-metalisation was required by dip etch in 20:1 *BHF* in 25C for 30 seconds. Metal, Titanium and aluminium mixture, was deposited on wafers by sputter machine (*TRIKON SIGMA*) all over wafer surface, and then metal mask was applied on wafers. Unwanted metal was etched away by dry etching machine (*SRS SS1C*). Alloy annealing process was carried out after wafers finish from resist strip and cleaning process. The final device is shown in figure A3



Figure A3. The finished device

A2 Devices Characterization

Devices characteristics of photodetectors in this report are mainly divided into two categories: one is electrical characteristic and the other is optical characteristic. For electrical characteristic, current-voltage relation and capacitance-voltage relation is obtained by using *HP 4155* and *HP 4280* semiconductor analyser respectively. These experiment results will be shown as table A1.

Wafer no.	Active area μm^2	Dark current pA	Threshold voltage V	Ideality factor η	Capacitance at Vr=0 pF
	50 ²	8.8	0.4	1.54	30.2
1	100 ²	31.6	0.4	1.66	30.6
	500 ²	90.1	0.4	1.53	52
2	50 ²	8	0.5	1.4	34.3
	100 ²	600	0.5	1.48	33.3
	500 ²	800	0.5	1.35	67.6
	50 ²	64.1	0.6	1.44	32.3
3	100 ²	35.6	0.6	1.5	31.2
	500 ²	46	0.6	1.4	55.5

Table A1: I-V and C-V information of silicon detector.

The experiment setup consists of light source (tungsten halogen lamp), light chopper, monochromator, amplifier unit, and data acquisition unit (PC). The wavelength sweep is provided by monochromator ranging from 300 to 1200nm with 10nm resolution. Sample is mounted to the slit at the output of monochromator by optical fixture stage.

There are many devices having various sizes on a single wafer so each device is wired to multi-switch called dipswitch on circuit board. Dipswitch selects one active device for measurement in order to study the spectral response of single device. This experiment uses samples with the absent of bias and under room temperature. The detector signal, voltage across devices, is fed to the pre-amplifier in order to increase the measurement signal, and the output from pre-amplifier goes to lock-in amplifier in order to transform AC signal into DC signal. The DC signal will go to analog to digital converter, A-to-D converter, and the output digital signal will be sent to the interface board, and the results will be collected and plotted on PC monitor by HPVEE universal measurement interface program. The spectral response of each wafer is shown in figure A2, and the summary of essential optical is shown in table A2.



Figure A4: The comparison of spectral response of device on wafer no.1 (Si 1), no.2 (Si 2), and no.3 (Si 3).

		R	Responsivity (A/W) Qua			uantum effici	ency	-	
Wafer no	Active area μm^2	650nm	1000nm	1090nm	650nm	1000nm	1090nm	V _{oc} (V)	I _{sc} (µА)
	50 ²							0.17	0.14
1	100 ²							0.19	0.736
	500 ²	60	1	0.35	0.285	0.003	0.001	0.2	15.2
	50 ²							0.5	0.437
2	100 ²							0.51	2.6
	500 ²	63.3	4.43	1.3	0.3	0.014	0.004	0.58	53
	50 ²							0.51	0.6
3	100 ²							0.52	2.8
	500 ²	85.34	5.3	1.04	0.4	0.016	0.003	0.55	47.9

 Table A2: The summaries of *p-i-n* photodetector performances and some of the process parameters accounting from measurement.

Appendix B

The additional measurements of Si/SiGe photodetectors

B1 Dopant concentration measurement

The electrical characteristics of the devices indicate the performance since they would be connected to the readout or other application circuits. I-V measurements were performed using an HP4155 semiconductor device analyser in order to obtain the basic electrical characteristics. Each chip site on the wafer has test structures used to monitor steps in the fabrication process such as the doping concentration. These structures help engineers to preliminarily evaluate the devices and fabrication processes. Two test structures were placed in each chip for impurity concentration measurements. It is known that a high impurity concentration is required for an ohmic contact and give low series resistance in the p-i-n diode. The test structures are shown in Fig. B1. The four large squares are metal pads which are connected to each corner of a small square test structure.



Figure B1: The sheet resistance test structure (*Van Der Pauw*) for impurity concentration measurement.

The strict conditions of using the Van Der Pauw's method are: firstly, the contacts are at the circumference of the sample. Secondly, the contracts are sufficiently small.

Thirdly, the sample is uniform thick, and fourthly, the surface of the sample is singly connected. The impurity concentration can be accounted by probing the resistance $R_{12,34}$. The $R_{12,34}$ is equal to

$$R_{12,34} = V_{34} / I_{12} \tag{B1}$$

where the current I_{12} enters the sample through contact 1 and leaves through contact 2 and the $V_{34} = V_3 - V_4$ is the voltage difference between contact 3 and 4. With this measurement the sheet resistance (ρ_s) becomes

$$\rho_s = 4.532R_{12.34} \tag{B2}$$

where 4.532 is the correction factor. Then the concentration can be obtained by using relation

$$\rho = \frac{l}{q(n\mu_n + p\mu_p)} \tag{B3}$$

where q is electron charge, n and p is electron and hole concentration, and μ_n and μ_p is electron and hole mobility respectively. The impurity concentrations from four of the wafers for a number of wafer positions are shown in Table B1, and the chip map, used for the chip location in each wafer, is shown in Fig. B2.



Figure B2: The chip sites on each wafer are labelled by numbers.

Chip	hip k2675-1		k2675-3		k26	75-4	k2675-6	
pos.	n	р	n	р	n	р	п	р
C18	1×10 ¹⁹	5×10^{20}	1×10 ¹⁹	5×10^{20}	2×10 ¹⁹	6×10^{20}	1×10 ¹⁹	7×10^{20}
C23	5×10^{18}	5×10^{20}	5×10^{19}	6×10^{20}	9×10 ¹⁸	6×10^{20}	3×10^{19}	7×10^{20}
C40	3×10^{19}	3×10^{20}	5×10^{20}	8×10^{19}	3×10^{19}	6×10^{20}	2×10 ¹⁹	6×10^{20}
C54	2×10^{19}	5×10^{20}	1×10 ¹⁹	6×10^{20}	9×10 ¹⁹	6×10^{20}	9×10^{18}	6×10^{20}
C59	1×10 ¹⁸	5×10^{20}	1×10 ¹⁹	5×10^{20}	9×10 ¹⁸	5×10^{20}	6×10^{19}	6×10^{20}

Table B1: The concentration (cm⁻³) of n^+ and p^+ layers of the investigated devices at different chip locations on wafers 1, 2, 4 and 6.

The measurement indicates that concentration at n^+ and p^+ layer of fabricated devices are slightly variation and also agree with the design. Therefore, the good diode behaviour is likely achieved.

B2 Nwell structure measurement

To reduce dark current, a low concentration *n*-well is formed on the substrate before the p^+ doping; this structure is generally used as latch-up protection in *CMOS* devices. The junction between the p^+ layer and the *n*-well provides a potential barrier to prevent carriers diffusing from outside. Figure B3 exhibits a comparison between the dark current of two different devices. It is found that the *n*-well device provides a lower dark current at small reversed bias. Therefore, the devices chosen to be measured and analysed are *n*-well devices. However, at high reverse bias, the dark current is higher than the devices without an *n*-well.



Figure B3: Example of a comparison between devices with and without an *n*-well from wafer *k2675-3*.

Guard ring structures are designed in several forms such as those in which the border of the device is surrounded by a doped region of either the same or a different species as the substrate. A different dopant species from the substrate, for instance an *n*-well in a *p*-type substrate, generates a space charge region due to the inherent potential, and it can prevent leakage current from outside the device by combining incoming carriers with uncompensated ions. Connecting the guard ring to metal can also enhance the guard ring performance. The guard ring strategy is commonly used in very large scaled integrated (*VLSI*) circuits because there are many devices on the chip located close to each other which may be active at the same time. Planar parasitic effects, for example, the latch-up problem in *CMOS* devices, are also alleviated by using such guard ring structures. For photodetector devices, such structures are also widely used, and the general configuration is to implant p^+ into an *n*-type substrate. The purpose of using guard ring structures is to increase the break down voltage in silicon devices. The larger the number of guard rings the higher the breakdown voltage.

B3 References

- D. K. schroder, Semiconductor material and device characterization, 1990, John Wiley& Sons Ins.
- 2. R. L. Geiger, P. E. Allen, and N. R. Strader, VLSI design techniques for analog and digital circuits, 1990, Mc Graw Hill.
- G. Bolla et. al., First results on radiation damage studied using n+/p/p+ diodes fabricated with multi-guard ring structures, Nuclear Instruments & Methods in Physics Research A, 1999(423): p. 290-296.
- C. Z. Zhou and W. K. Warburton, Comparison of silicon pin diode detector fabrication processes using ion implantation and thermal doping, Nuclear Instruments & Methods in Physics Research A, 1996. 378: p. 529-530.
- 5. M. Sugizaki, Development of the large area silicon OIN diode with 2mm-thick depletion layer for Hard X-ray Detector (HXD) on-broad ASTRO-E. 2003, http://scipp.ucsc.edu/~sugizaki/hxdpapaer_spie_nasda/paper_spie_nasda.html.

Appendix C

Mask Design

C1: Silicon detector mask.



Figure C1: KA68R.

C2: Si/SiGe quantum dot photodetector



Figure C2: KB09RW.

Appendix D

Process listing

See following pages for listing of each fabrication process.

Silicon photodetector process listing

- K2308s Implantation and Silicon epitaxy
- K2479s continue from k2308s to produce silicon p-i-n photodetector
- K2488s Silicon wet etching study

Silicon epitaxy experiment

• K2517s Silicon epitaxy growth with various temperature

Si/SiGe multi-layer epitaxy experiment

- D2452s Si/SiGe multi-layer growth (the first generation)
- K2680s Si/SiGe multi-layer growth (the second generation)
- K2833s Si/SiGe multi-layer growth (the third generation)

Si/SiGe multiple quantum dot infrared photodetector fabrication

• K2675 Si/SiGe Qwips

Running k2308s on 10-26-2005

1	12	2345	6 ID	Description	XCost P	Count
18			P-EM	E-BEAM MaskrReticle Writing	0	0
25			G-S12	Title Page: 12 waters, MATERIAL: P-type <100> 17-33 ohm/cm	0	12
30	2		G-1P	Lithography Notes	0	12
40	2		G-1	Notebook page	0	12
59	2		W-C1	* RCA clean	0	12
65	2		F5-00	* Furnace 5: Load in O2: 950deg C: thickness 60nm, O2 + 3%HCL	0	12
79	2		1B-0	* Implant B+: 1e15 25Kev	0	12
8E	2		F10-0	* Furnace 10: Load in N2: 10 min temp 900 degC annealing	0	12
96	2		WH-7	Strip all SiO2 from wafer: 7:1 BHF 25degC	0	12
10		\square	W-C6	* Pre-epitaxy clean Wafers	0	1
11			LE-0	Low Pressure Epitaxy; 1.50 um intrinsic temp 850 degC Wafers #1	0	1
12	ę	2	W-C6	* Pre-epitaxy clean Wafers #2	0	1
13	E		LE-0	Low Pressure Epitaxy; 2.00 um intrinsic temp 850 degC Wafer #2	s 0	1
14		Ø	W-C6	* Pre-epitaxy clean Wafers #3	0	1
15		2	LE-0	Low Pressure Epitaxy; 2.50 um intrinsic temp 850 degC Wafer #3	s 0	1
16			G-2	* See Engineer for instructions: Wafer#4-12 held for use in another batch	0	9
176	2		X-0	Check quality of single crystal by using normalski microscope	0	12

Running k2479s on 10-26-2005

10 PERM E-BEAM Mask/Retick Writing 0 2 G-56 * Title page: 3 wafers(#1-3),from k2308s 0 340 G-1P Lithography Notes 0 541 Notebook page 0 542 G-1 Notebook page 0 543 U-0 * 1/10 deposition: Somm +-10mm 0 744 D-0 * 1/10 deposition: Somm +-10mm 0 745 W-C1 * RCA clean 0 746 W-C1 * RCA clean 0 747 W-C1 * RCA clean 0 749 W-C1 * RCA clean 0 740 W-C1 * RCA clean 0 741 PC4 * Photolith mask KARSR, AA Li Field: nom. 1.1um resist STANDARD 0 742 PC4 * Photolith mask KARSR, AA Li Field: nom. 1.1um resist STANDARD 0 745 P-R8F * Resist strip 0 0 745 P-R8F * Resist strip 0 0 745 P-R8F * Resist strip 0 0 747 P-R8F * Resist strip 0 0 747 P-R8F * Resist strip 0 0 746 P-R8F * Resist strip 0 0<	1234	5 6 ID	Description	XCost F	Count
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30 G-1P Lithography Notes 0 40 G-1 Notebook page 0 50 W-C1 * RCA clean 0 70 IP-0 Implant PHOS+: 1e15 25Kev 0 80 W-C1 * RCA clean 0 91 F10-0 * Implant PHOS+: 1e15 25Kev 0 80 W-C1 * RCA clean 0 91 F10-0 * Furnace 10: Load in N2: 10 min temp 900 degC annealing 0 92 W-C1 * RCA clean 0 93 F10-0 * Furnace 10: Load in N2: 10 min temp 900 degC annealing 0 94 M-C1 * RCA clean 0 195 W-C1 * RCA clean 0 196 W-C1 * RCA clean 0 197 P-G1 * Photolith mask KA68R, AA U Field: nom. 1.tum resist STANDARD 0 196 W-C1 * RCA clean 0 197 P-RHF Hardbake for wet etch 0 198 W-C2 * See Engineer for instructions 0 198 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 199 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 20 W-C1 * RCA clean 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22 W-C1 * RCA clean 0 23<	2	G-56	* Title page: 3 wafers(#1-3),from k2308s	0	3
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105 Wi-7(Strip all SiO2 from wafer: 7:1 BHF 25degC 0 1125 U-20* LTO deposition: 200m *-20nm at 400degC SiH4 and 02 0 136 P-61 * Photolith mask KA68R, AA L/ Field: nom. 1.1um resist STANDARD 0 146 G-2 * See Engineer for instructions 0 147 P-R8 * Hardbake for wet atch 0 1480 WH-22 Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs. 0 1480 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 1480 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 1480 W-C2 * Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 149 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 21 W-C1 * RCA clean 0 120 W-C1 * RCA clean 0 121 W-C2 * TO deposition: 500nm +- 60nm at 400degC SiH4 and 02 0 222 W-C1 * RCA clean 0 121 W-S2 * Stech Silicon in kOH: 45-60 Deg, 2.5 um depth 0 224 X-11 N anospec scribe lanes on 6 wafers; fiat, middle, curve. 0 232 LO-60* LTO deposition: 500nm +- 60nm at 400degC SiH4 and	92	F10-0	* Furnace 10: Load in N2: 10 min temp 900 deoC annealing	0	3
113 W-C1 * RCA clean 0 120 LO-20* LTO deposition: 200nm +- 20nm at 400degC SiH4 and O2 0 130 P-G1 * Photolith mask KA68R, AA U Field: nom. 1.1um resist STANDARD 0 143 G-2 * See Engineer for instructions 0 150 P-RHE* Hardbake for wet etch 0 160 WH-22 Wet etch oxide, 20:1 BHF 25degC. To hydrophobic SI + 20secs. 0 174 P-RS * Resist strip 0 185 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 185 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 20 WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 22 W-C1 * RCA clean 0 234 W-C1 * RCA clean 0 245 X-T1 Nanospec scribe tanes on 6 wafers; flat, middle, curve. 0 254 Q-2 * See Ted Meech to discuss next stepper stage 0 255 G-2 * See Engineer for instructions 0 26 P-RS * Resist strip 0 27 G-2 * See Engineer for instructions 0 26 P-RHE* Hardbake	100	WH-70	Strip all SiO2 from wafer: 7:1 BHF 25deoC	0	3
125 LO-20* LTO deposition: 200nm +- 20nm at 400degC SiH4 and O2 0 136 P-61* Photolith mask KA68R, AA L/ Field: nom. 1.1um resist STANDARD 0 147 G-2*See Engineer for instructions 0 156 P-RHE* Hardbake for wet etch 0 166 WH-22 Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs. 0 177 P-R8 * Resist strip 0 186 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 192 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 20 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 22 W-C1* RGA clean 0 0 Dielectric 0 236 LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 24 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 G-2 * See Ted Meech to discuss next stepper stage 0 26 P-652* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2um resist (For Si etch+31um or metal) note: 3um focus offset require 0 27 G-2 * See Engineer for instructions 0 0 </td <td>115</td> <td>W-C1</td> <td>* RCA clean</td> <td>0</td> <td>3</td>	115	W-C1	* RCA clean	0	3
33 P-G1 * Photolith mask KA68R, AA L/ Field: nom. 1.1um resist STANDARD 0 14g G-2 * See Engineer for instructions 0 15g P-RHE* Hardbake for wet etch 0 15g P-RHE* Hardbake for wet etch 0 15g P-RHE* Hardbake for wet etch 0 16g WH-2Z Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs. 0 17z P-RS * Resist strip 0 18g W-C2 * Furning Nitric acid clean, 2nd pot only 0 19g WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 20 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22g W-C1 * RCA clean 0 23g L0-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and 02 0 24g X-11 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25g G-2 * See Ted Meech to discuss next stepper stage 0 25g G-2 * See Engineer for instructions 0 25g D-Off Etch Sl02 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 31g G-2 * See Engineer for instructions	125	10-20	* I TO deposition: 200nm +- 20nm at 400denC SiH4 and O2	0	3
132 1.51 International mean for instructions 0 150 P-RHE* Hardbake for wet etch 0 160 WH-2E Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs. 0 172 P-RS * Resist strip 0 180 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 180 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 180 WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 22 W-C1 * RCA clean 0 Dielectric 0 0 230 LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 240 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 252 G-2 * See Ted Meech to discuss next stepper stage 0 26 P-652* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2um resist (For Si etch>*1um or metal) note: 3um focus offset require 0 270 G-2 * See Engineer for instructions 0 0 27 G-2 * See Engineer for instructions 0 0 280 P-RHE* Hardbake for dry etch 0 0	130	P_G1	* Photolith mask KA688 AA I / Field: nom 1 1um resist STANDARD	0	1
150 D-RHE* Hardbake for wet etch 0 160 WH-2E Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs. 0 172 P-RS * Resist strip 0 180 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 190 WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 20 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22 W-C1 * RCA clean 0 23 LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 24 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 G-2 * See Ted Meech to discuss next stepper stage 0 26 P-652* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist (For Si etch-Yum or metal) note: 3um focus offset require 0 27 G-2 * See Engineer for instructions 0 0 28 D-01E Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RS * Resist strip 0 0 31 G-2 * See Engineer for instructions 0 32 W-C2 * Fuming Nitric acid clean, 2nd pot only 0<	14-2	G-2	* Soo Engineer for instructions	0	3
13.5 P-RN: "Raidbake for Wetern" 0 14.64 WH-24 Wet tech oxide, 20:1 BHF 25degC. To hydrophobic SI + 20secs. 0 17.7 P-RS "Resist strip 0 18.7 W-C2 * Furning Nitric acid clean, 2nd pot only 0 19.7 P-RS * Resist strip 0 19.7 WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 20.7 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 21.7 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22.7 W-C1 * RCA clean 0 23.4 LO-60* LTO deposition: 500nm +- 60nm at 400degC SiH4 and O2 0 24.7 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25.0 G-2 * See Ted Meech to discuss next stepper stage 0 26.0 P-GS2* STEPPER Photolifit: reticle KA68R, CW. D/ Field: nom. 2.2 um resist (For Si etch>tum or metal) note: 3 um focus offset require 0 27.0 G-2 * See Engineer for instructions 0 0 28.4 D-01E Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30.2 P-RS * Resist strip 0 0 31.9 G-2 * See Engineer for instructions <	15-2	D DUE	Verdhaka for wet steh	0	2
172 P-RS * Resist strip 0 183 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 183 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 192 WS-0 Etch silicon in KOH: 45-50 Deg, 1.5 um depth 0 20 WS-0 Etch silicon in KOH: 45-50 Deg, 2.0 um depth 0 21 WS-0 Etch silicon in KOH: 45-50 Deg, 2.0 um depth 0 21 WS-0 Etch silicon in KOH: 45-50 Deg, 2.5 um depth 0 22 W-C1 * RCA clean 0 Dialectric 0 0 232 LO-50* LTO deposition: 500nm +- 60nm at 400degC SiH4 and O2 0 24cz X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 250 G-2 * See Ted Meach to discuss next stepper stage 0 26 P-6S2* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2um resist 0 270 G-2 * See Engineer for instructions 0 28 P-RS * Resist strip 0 29 D-01E Etch SiO2 . Anlsot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 302 P-RS * Resist strip 0 0 31c G-2 * See Engineer for instructions 0	160	WH 2	Mot stoh ovide 20:1 PHE 25desC. To budrophobic Si + 20coss	0	3
Image: Price Researce support 0	17	0.00	* Depist strip	0	3
185 W-C2 Fullming Name actor clean, 2nd pot only 0 192 WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 20 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 22 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22 W-C1 *RCA clean 0 Dielectric 0 0 0 23 LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and 02 0 24 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 G-2 'See Ted Meech to discuss next stepper stage 0 26 P-6S2* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2 um resist 0 27 G-2 'See Ted Meech to discuss next stepper stage 0 27 G-2 'See Engineer for instructions 0 28 D-01E Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RS<* Resist strip	11 I	P-R3	Resist sup	0	3
19 c WS-0 Etch silicon in KOH: 45-60 Deg, 1.5 um depth 0 20 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22 c W-C1 * RCA clean 0 23 c LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 24 c X-T1 Nanospace scribe lanes on 6 wafers; flat, middle, curve. 0 25 c G-2 See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2 um resist 0 27 d G-2 See Engineer for instructions 0 28 d P-RHF Hardbake for dry etch 0 0 29 D-O1E Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 d P-RS * Resist strip 0 0 31 c G-2 * See Engineer for instructions 0 0 32 d WH-20 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 0 33 d WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 0 34 Ms-21 Dip etch, 20:1 BHF 25degC. 30 secon	185	W-62	- Furning Mutric acid clean, 2nd pot only	U	3
View 20 20 20 20 20 20 20 21 0 0 21 0 WS-0 Etch silicon in KOH: 45-60 Deg, 2.0 um depth 0 22 W-C1 * RCA clean 0 0 23 c LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and 02 0 24 c X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 c G-2 See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2um resist (For Si etch>tum or metal) note: 3um focus offset require 0 27 d G-2 See Engineer for instructions 0 27 d G-2 * See Engineer for instructions 0 28 d P-RHE* Hardbake for dry etch 0 29 d D-01E Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 d P-RS * Resist strip 0 0 31 d G-2 See Engineer for instructions 0 32 d W-C2 * Furming Nitric acid clean, 2nd pot only 0 0 33 d WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 <td>190</td> <td>WS-0</td> <td>Etch silicon in KOH: 45-60 Deg 1.5 um denth</td> <td>0</td> <td>1</td>	190	WS-0	Etch silicon in KOH: 45-60 Deg 1.5 um denth	0	1
21 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 22 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 23 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 23 WS-0 Etch silicon in KOH: 45-60 Deg, 2.5 um depth 0 23 L0-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and 02 0 24 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 G-2 See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2um resist 0 (For Si etch>tum or metal) note: 3um focus offset require 0 27 G-2 See Engineer for instructions 0 28 P-RHF Hardbake for dry etch 0 0 29 D-01E Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RS * Resist strip 0 0 31 G-2 * See Engineer for instructions 0 32 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 0 33 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) <t< td=""><td>20 3</td><td>WS.O</td><td>Etch silicon in KOH: 45.60 Deg. 2.0 um denth</td><td>0</td><td>4</td></t<>	20 3	WS.O	Etch silicon in KOH: 45.60 Deg. 2.0 um denth	0	4
21 9 Wise Etter sincerim non-especial beg, 2.5 diff deput 0 22 W-C1 * RCA clean 0 Dielectric 0 23 LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 24 X-T1 Nanospec scribe lanes on 6 waters; flat, middle, curve. 0 25 G-2 * See Ted Meech to discuss next stepper stage 0 25 G-2 * See Ted Meech to discuss next stepper stage 0 26 P-652* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist (For Si etch>tum or metal) note: 3um focus offset require 0 27 G-2 * See Engineer for instructions 0 28 P-RHE* Hardbake for dry etch 0 0 29 D-OTE Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RS * Resist strip 0 0 31 G-2 * See Engineer for instructions 0 32 W-C2 * Furning Nitric acid clean, 2nd pot only 0 0 33 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 0 34 MS-TS Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA 0 0	20 0	WIS O	Eich silicon in KOH: 45.60 Dog, 2.5 um depth	0	
222 W-C1 * RCA clean 0 Dielectric 0 232 LO-50* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 242 X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 Contacts 0 250 G-2 * See Ted Meech to discuss next stepper stage 0 250 G-2 * See Ted Meech to discuss next stepper stage 0 260 P-GS2* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist (For Si etch>tum or metal) note: 3um focus offset require 0 270 G-2 * See Engineer for instructions 0 280 P-RHE* Hardbake for dry etch 0 0 29 D-Otif Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 300 P-RS * Resist strip 0 0 312 G-2 * See Engineer for instructions 0 322 W-C2 * Furning Nitric acid clean, 2nd pot only 0 332 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-Th Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA 0 355 G-2 * See Ted Meech to discuss next steppper stage 0		113-0	Etch Shoon in Non. 40-00 beg, 2.5 un deput	U	
Dielectric Dielectric 23 C LO-60* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 24 C X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 Contacts 0 25 C G-2 * See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist 0 27 G G-2 * See Engineer for instructions 0 28 P-RHE* Hardbake for dry etch 0 29 P-RS * Resist strip 0 30 P-RS * Resist strip 0 31 C G-2 * See Engineer for instructions 0 31 C G-2 * See Engineer for instructions 0 32 W-C2 * Furming Nitric acid clean, 2nd pot only 0 0 33 WH-20 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 0 34 MRS-TF Sputter 1000nm Ti-TIN-AUSI 1% in TRIKON SIGMA 0 0 35 C G-2 * See Ted Meech to discuss next stepper stage 0 35 C G-2 * See Ted Meech to discuss next stepper stage 0 35 C G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R, ME. L/Field: nom. 2.2um resist (For	223	W-C1	* RCA clean	0	3
23 c LO-50* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2 0 24 c X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 c G-2 * See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 27 G G-2 * See Engineer for instructions 0 28 P-RHE* Hardbake for dry etch 0 29 D-O1E Etch SiO2. Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RH * Resist strip 0 30 P-RS * Resist strip 0 31 C G-2 * See Engineer for instructions 0 32 W-C2 * Funning Nitric acid clean, 2nd pot only 0 33 W+22 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 35 A G-2 * See Ted Meech to discuss next stepper stage 0 35 A G-2 * See Ted Meech to discuss next stepper stage 0 35 A G-2 * See Ted Meech to discuss next stepper stage 0 36 A P-GS2* STEPPER Photolith: reticle KA688, ME. L/Field: nom. 2.2um resist (For SI etch>1um or metal) note: 3um focus offset require 0			Dielectric		
24 cs X-T1 Nanospec scribe lanes on 6 wafers; flat, middle, curve. 0 25 cs G-2 * See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist 0 27 cs G-2 * See Engineer for instructions 0 27 cs G-2 * See Engineer for instructions 0 27 cs G-2 * See Engineer for instructions 0 28 cs D-OIE Etch SlO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 cs P-RS * Resist strip 0 31 cs G-2 * See Engineer for instructions 0 31 cs G-2 * See Engineer for instructions 0 32 cl W-C2 * Fuming Nitric acid clean, 2nd pot only 0 33 cs WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 ds MS-Th Sputter 1000nm Ti-TIN-Al/SI 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 35 cs G-2 * See Ted Meech to discuss next stepper stage 0 36 ds P-GS2* STEPPER Photolith: reticle KA68R, ME. L/Field: nom. 2.2um resist (For SI etch>1um or metal) note: 3um focus offset require 0 36 ds P-RHE* Hardbake for dry etch 0 0 37 ds G-2 * See Engineer for instruct	230	LO-60	* LTO deposition: 600nm +- 60nm at 400degC SiH4 and O2	0	3
Contacts 0 25 c G-2 * See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist 0 27 G G-2 * See Engineer for instructions 0 28 P-RHE* Hardbake for dry etch 0 29 D-O1E Etch SiO2 . Anlsot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 c P-RS * Resist strip 0 31 c G-2 * See Engineer for instructions 0 31 c G-2 * See Engineer for instructions 0 31 c G-2 * See Engineer for instructions 0 32 d W-C2 * Fuming Nitric acid clean, 2nd pot only 0 32 d W-22 * Fuming Nitric acid clean, 2nd pot only 0 33 d WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 d MS-Th Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 35 d G-2 * See Ted Meech to discuss next stepper stage 0 36 d P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) nole: 3um focus offset require 0 37 d G-2 * See Engineer for instructions 0	24 2	X-T1	Nanospec scribe lanes on 6 waters; flat, middle, curve.	0	3
25 c G-2 * See Ted Meech to discuss next stepper stage 0 26 P-GS2* STEPPER Photolith: reticle KA68R., CW. D/ Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 27 c G-2 * See Engineer for instructions 0 28 c P-RHE* Hardbake for dry etch 0 29 c D-O1E Etch SiO2 . Anlsot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 c P-RS * Resist strip 0 30 c P-RS * Resist strip 0 31 c G-2 * See Engineer for instructions 0 31 c G-2 * See Engineer for instructions 0 32 c W-C2 * Furning Nitric acid clean, 2nd pot only 0 33 c WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 d RESIST PROHIBITED + ARC 30nm TiN 0 35 c G-2 * See Ted Meech to discuss next stepper stage 0 36 d P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 36 d P-RHE* Hardbake for dry etch 0 0 37 d G-2 * See Engineer for instructions 0 38 d P-RHE* Hardbake for dry etc			Contacts	Contra E	
26 P-GS2* STEPPER Photolith: reticle KA68R, CW. D/ Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 27 9 G-2 * See Engineer for instructions 0 28 9 P-RHE* Hardbake for dry etch 0 29 D-O1E Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 9 P-RS * Resist strip 0 30 4 P-RS * Resist strip 0 30 5 G-2 * See Engineer for instructions 0 31 5 G-2 * See Engineer for instructions 0 31 6 G-2 * See Engineer for instructions 0 32 6 W-G2 * Furning Nitric acid clean, 2nd pot only 0 32 7 WH-2t Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 7 MS-Th Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 35 4 G-2 * See Ted Meech to discuss next stepper stage 0 36 7 P-GS2* STEPPER Photolith: reticle KA688R, ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 37 9 G-2 * See Engineer for instructions 0 38 2 P-RHE* Hardbake for dry etch 0 38 2 P-RHE* H	250	G-2	* See Ted Meech to discuss next stepper stage	0	3
(For Si etch>1um or metal) note: 3um focus offset require 270 G-2 * See Engineer for instructions 0 280 P-RHE* Hardbake for dry etch 0 29 D-OIE Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 302 P-RS * Resist strip 0 303 P-RS * Resist strip 0 304 P-RS * Resist strip 0 305 G-2 * See Engineer for instructions 0 306 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 316 G-2 * See Engineer for instructions 0 320 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 321 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 322 WH-2t Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 35 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R, ME. L/Field: nom. 2.2um resist (For 0 37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MA1+ Et	26	P-GS	* STEPPER Photolith; reticle KA68R., CW, D/ Field: nom. 2.2um resist	0	3
270 G-2 * See Engineer for instructions 0 280 P-RHE* Hardbake for dry etch 0 29 D-OIE Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RS * Resist strip 0 30 P-RS * Resist strip 0 31 G-2 * See Engineer for instructions 0 Metal 0 0 320 W-C2 * Furning Nitric acid clean, 2nd pot only 0 33 WH-2C Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 35 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For O Si etch>1um or metal) note: 3um focus offset require 0 37 G-2 * See Engineer for instructions 0 37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 38 D-MA1+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 (WHOLE 4* wfrs) 0 0	f		(For Si etch>1um or metal) note: 3um focus offset require		
28 P-RHE* Hardbake for dry etch 0 29 D-O1E Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 30 P-RS * Resist strip 0 30 P-RS * Resist strip 0 31 P G-2 * See Engineer for instructions 0 Metal 0 32 W-C2 * Furning Nitric acid clean, 2nd pot only 0 33 WH-22 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TP Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 35 P G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) nole: 3um focus offset require 0 37 P G-2 * See Engineer for instructions 0 0 38 P P-RHE* Hardbake for dry etch 0 0 38 P D-MAT+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 (WHOLE 4" wfrs) 0 0	270	G-2	* See Engineer for instructions -	0	3
29 D-O1E Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar 0 302 P-RS * Resist strip 0 312 G-2 * See Engineer for instructions 0 Metal 0 322 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 333 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TP Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 352 G-2 * See Ted Meech to discuss next stepper stage 0 352 G-2 * See Ted Meech to discuss offset require 0 372 G-2 * See Engineer for instructions 0 384 P-RHE* Hardbake for dry etch 0 384 P-RHE* Hardbake for dry etch 0 384 P-RHE* Hardbake for dry etch 0 39 D-MAT+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 0 D-MAT+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0	28	P-RHI	* Hardbake for dry etch	0	3
302 P-RS * Resist strip 0 315 G-2 * See Engineer for instructions 0 Metal 0 322 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 333 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 352 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For SI etch>1um or metal) note: 3um focus offset require 0 372 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MAI+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS \$\$1C Cl2+SiCl4+Ar 0 (WHOLE 4" wfrs)	29	D-01	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar	0	3
31 G-2 * See Engineer for instructions 0 Metal	30点	P-RS	* Resist strip	0	3
Metal 0 320 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 332 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 352 G-2 * See Ted Meech to discuss next stepper stage 0 354 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 372 G-2 * See Engineer for instructions 0 384 P-RHE* Hardbake for dry etch 0 39 D-MAT+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS \$\$1C Cl2+SiCl4+Ar 0 0 D-MAT+ Etch Al, Al/Si and/or Ti . for OPTICAL resist \$\$10 Cl2+SiCl4+Ar 0	31 👳	G-2	* See Engineer for instructions	0	3
322 W-C2 * Fuming Nitric acid clean, 2nd pot only 0 332 WH-21 Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA 0 352 G-2 * See Ted Meech to discuss next stepper stage 0 352 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For SI etch>1um or metal) note: 3um focus offset require 0 37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MA1+ Etch Al, Al/Si and/or Ti . for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 0 0.04400 E 4" wfrs) 0		distant and the	Metal	255	112
33 WH-2t Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation) 0 34 MS-Th Sputter 1000nm Ti-TiN-Al/Si 1% in TRIKON SIGMA 0 35 RESIST PROHIBITED + ARC 30nm TiN 0 35 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MAT+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS \$\$1C Cl2+\$iCl4+Ar 0 0 P.R.D. State 0	320	W-C2	* Furning Nitric acid clean, 2nd pot only	0	3
34 MS-TF Sputter 1000nm Ti-TIN-Al/Si 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TiN 0 35 2 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For SI etch>1um or metal) note: 3um focus offset require 0 37 2 G-2 * See Engineer for instructions 0 38 2 P-RHE* Hardbake for dry etch 0 39 3 D-MA1+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0	33	WH-2	Dip etch, 20:1 BHF 25degC. 30 seconds. (Pre-metalisation)	0	3
35 G-2 * See Ted Meech to discuss next stepper stage 0 36 P-GS2* STEPPER Photolith: reticle KA68R, ME. L/Field: nom. 2.2um resist (For 0 Si etch>1um or metal) note: 3um focus offset require 0 37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MA1+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 40 0.000 E.4* wfrs) 0	34	MS-TI	Sputter 1000nm Ti-TIN-Al/SI 1% in TRIKON SIGMA RESIST PROHIBITED + ARC 30nm TIN	0	3
36 P-GS2* STEPPER Photolith: reticle KA68R, ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require 0 37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MAT+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 40 0.00000000000000000000000000000000000	352	G-2	* See Ted Meech to discuss next stepper stage	0	3
37 G-2 * See Engineer for instructions 0 38 P-RHE* Hardbake for dry etch 0 39 D-MAT+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 (WHOLE 4" wfrs) 0	36	P-GS:	* STEPPER Photolith: reticle KA68R., ME. L/Field: nom. 2.2um resist (For Si etch>1um or metal) note: 3um focus offset require	0	3
38 P-RHE* Hardbake for dry etch 0 39 D-MAT+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 (WHOLE 4" wfrs) 0	370	G-2	* See Engineer for instructions	0	3
39 D-MAT+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar 0 (WHOLE 4" wfrs)	38 2	P-RH	* Hardbake for dry etch	0	3
	39	D-MA	+ Etch Al, Al/Si and/or Ti. for OPTICAL resist SRS SS1C Cl2+SiCl4+Ar	0	3
402 P-RS Resist strip	40 2	P-RS	* Resist strip	0	3
41 X-T2 Nanospec thick field oxide on 12 wafers; flat, middle, curve. 0	41 2	X-T2	Nanospec thick field oxide on 12 waters; flat, middle, curve.	0	3
42 W-C3 * Furning Nitric Acid clean, metallised wafers 0	42 2	W-C3	* Furning Nitric Acid clean, metallised wafers	0	3
43 F9-H4* Alloy/ Anneal: 30mins H2/N2 420deuC 5'N2.30'H2/N2.5'N2. 0	432	F9-H4	* Alloy/ Anneal: 30mins H2/N2 420deaC 5'N2.30'H2/N2.5'N2.	0	3
Running	k2488s	on	10-26-2005		
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1 APLIN III III		~			

123456	ID	Description	Count	Cost
1段	P-EM	E-BEAM Nask/Reticle Writing	1	1628
2	G-S6	* Title page: 2 wafers(#4-5), from k2308s	2	0
3	G-1P	Lithography Notes	0	0
42	G-1	Notebook page	0	0
50	WH-70	Strip all SiO2 from wafer: 7:1 BHF 25degC	2	158
6幸	X-0	Measure Sheet Resistance of 2 wafers	2	0
78	W-C6	* Pre-epitaxy clean	2	158
82	LE-0	Low Pressure Epitaxy; 1.50um silicon intrinsic layer temp 850 degC wafer#4	1	1281
9	LE-0	Low Pressure Epitaxy; 2.50 um silicon intrinsic layer temp 850 degC wafer#5	1	1281
10호	X-0	Check crystal by normalski microscope	2	0
112	W-C1	* RCA clean	2	158
122	LO-0	* LTO deposition: 50nm +-10nm	2	937
13호	IP-0	* Implant PHOS+: 1e15 25Kev	2	1431
142	W-C1	* RCA clean	2	158
15史	F10-0	* Furnace 10: Load in N2: 10 min temp 900 degC annealing	2	641
16史	WH-7	Strip all SiO2 from wafer: 7:1 BHF 25degC	2	158
17读	W-C1	* RCA clean	2	158
18字	LO-20	* LTO deposition: 200nm +- 20nm at 400degC SiH4 and O2	2	937
19.0	P-G1	* Photolith mask KA68R, .AA L/ Field: nom. 1.1um resist STANDARD	2	1067
20호	G-2	* See Engineer for instructions	0	0
21异	P-RHE	* Hardbake for wet etch	2	0
22克	WH-2	Wet etch oxide, 20:1 BHF 25degC. To hydrophobic Si + 20secs.	2	158
230	P-RS	* Resist strip	2	0
24中	W-C2	* Furning Nitric acid clean, 2nd pot only	2	158
250	WS-0	Etch silicon in KOH: 45-60 Deg, 1.5 um depth wafer#4	1	158
26 2	WS-0	Etch silicon in KOH: 45-60 Deg, 2.5 um depth wafer#5	1	158

Running k2517s on 10-26-2005

1	23	456	ID	Description	XCost	PCount
12			P-EM	E-BEAM Mask/Reticle Writing	0	0
20			G-S12	Tible Page: 5 wafers, MATERIAL: P-type silicon 10 ohms/cm <100> FZ	0	5
30			G-1P	Lithography Notes	0	5
42			G-1	Notebook page	D	5
5史		3	W-C1	* RCA clean	0	5
62	4		F4-W0	* Wet oxidation: 600nm, 1000degC: I,rO2,x'wO2,uN2	0	5
7			P-G1	* Photolith mask HALF MASK, DARK Field: nom. 1.1um resist STANDARD	0	5
80			P-RHE	* Hardbake for wet etch	0	5
92		5 5 3	WH-71	+ Wet etch oxide, 7:1 BHF 25degC. To hydrophobic Si + 20secs.	0	5
10호			P-RS	* Resist strip	0	5
112	TT	T	W-C6	* Pre-epitaxy clean	0	1
12			LE-0	Low Pressure Epitaxy; Silicon doping < 1e16 650 degC 300nm thickness #1	0	
13	4		W-C6	* Pre-epitaxy clean	0	1
14	4		LE-0	Low Pressure Epitaxy; Silicon doping < 1e16 700 degC 300nm thickness #2	0	1
15	一中		W-C6	* Pre-epitaxy clean	0	1
16	2		LE-0	Low Pressure Epitaxy; Silicon doping < 1e16 750 degC 300nm thickness #3	0	1
17	11	3	W-C6	* Pre-epitaxy clean	0	1
18		\$	LE-0	Low Pressure Epitaxy; Silicon doping < 1e16 800 degC 300nm thickness #4	0	1
19		18	W-C6	* Pre-epitaxy clean	0	1
20	\prod	B	LE-0	Low Pressure Epitaxy; Silicon doping < 1e16 850 degC 300nm thickness #5	0	
210			X-0	Inspection the surface by Normaski microscope	0	5

Running d2452s on 10-26-2005

12345	56 ID	Description	Count	Cost
10	P-EM	E-BEAM Mask/Reticle Writing	0	(
20	G-S12	Title Page: 2 wafers, MATERIAL: P-type<100> 17-33 ohm/cm	2	(
30	G-1P	Lithography Notes	0	(
40	G-1	Notebook page	0	C
ड्य	W-C6	* Pre-epitaxy clean	1	158
6 2	LE-0	Low Pressure Epitaxy; - Wafer #1 (1) Si 50nm thickness (2) SiGe with Ge 6% 5nm thickness repeat (1) - (2) x 9 times (3) Si 100nm thickness	1	1281
7 0	W-C6	' Pre-epitaxy clean	1	158
8	LE-0	Low Pressure Epitaxy; - Wafer #2 (1) Si 50nm thickness (2) SiGe with Ge 20% 5nm thickness repeat (1) - (2) x 9 times (3) Si 100nm thickness	1	1281
90	X-0	Inspection by Normalski microscope	2	(

Running k2680s on 10-26-2005

1	23456	ID	Description	Count	Cost
1\$		P-EM	E-BEAM Mask/Reticle Writing	0	0
22		G-S12	Title Page: 3 wafers, MATERIAL:P-type 17-33ohms/cm <100>	3	0
32		G-1P	Lithography Notes	0	0
4\$		G-1	Notebook page	0	0
52		W-C6	* Pre-epitaxy clean	3	158
6 		LE-0	Low Pressure Epitaxy; wafer #1 (1) growth undoped sige layer Ge 10% and 5 + - 4 nm thickness (2) growth undoped silicon buffer layer 50 nm thickness repeat (1)-{2) 19 times (3) growth undoped silicon cap layer 200 nm thick	1	1281
7	4	LIE-0	Low Pressure Epitaxy; wafer #2 (1) growth undoped sige layer Ge 20% and 5 + • 4nm thickness (2) growth undoped silicon buffer layer 50 nm thickness repeat (1)-(2) 19 times (3) growth undoped silicon cap layer 200 nm thick	1	1281
80	-	X-0	Inspection the surface of laver by nomarski	2	0
94		G-3	"bring wafer #1 and #2 out for SIMS profile	Ō	0
10	ļ	LE-0	Low Pressure Epitaxy; wafer #3 (1) growth undoped sige layer by try to get max Ge% and min thickness (nm order) (2) growth undoped silicon buffer layer 50 nm thickness repeat (1)-{2) 19 times (3) growth undoped silicon cap layer 200 nm thick	1	1281
11	2	X-0	Inspection the surface of layer by nomarski	1	0

Running k2833s on 10-26-2005

123	456 ID	Description	XCost PO	Count
1史	P-EM	E-BEAM Mask/Reticle Writing	0	0
2	G-S12	Title Page: 13 wafers, MATERIAL: silicon p+ <100> <0.02ohms/cm no.#1-#6 , silicon <100> from batch no.2308s no.#7-#12 and silicon p-type <110> from batch no.k2486s no.#13	0	13
3	G-1P	Lithography Notes	0	13
49	G-1	Notebook page	0	13
		wafer no.1		
5 4	W-C6	* Pre-epitaxy clean	0	1
6	LE-0	Low Pressure Epitaxy; 820degC #1 (1) Undoped Si 100 nm (buffer) (2) Doped B+ 1e19 SiGe 10nm Ge 35-40% (3) Undoped spacer Si 40nm (4) Rpt (2)-(3) 4 times (std SiH4 flow)	o	1
니 덕		(5) Rpt (2)-(3) 5 times (red SiH4 flow) (6) Undoped Si 100nm (cap)		
_h		wafer no.2	1 1 2 5 2 A 1	25
7 8	W-C6	* Pre-epitaxy clean	0	1
8	LE-0	Low Pressure Epitaxy; /50degC #2 (1) Undoped Si 100 nm (buffer) (2) Doped B+ 1e19 SiGe 10nm Ge% 35-40% (3) Undoped spacer Si 40nm (4) Rpt (2)-(3) 4 times (std SiH4 flow) (5) Rpt (2)-(3) 5 times (red SiH4 flow) (6) Undoped Si 100nm (cap)	0	*
μ				
98	X-0	Holding for SIMS measurement and general inspection by normaski	0	1
			M CALLER	
h		wafer no.3		
10 \$	W-C6	* Pre-epitaxy clean	0	1
	LE-0	Low Pressure Epitaxy; 750degC water #3 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	0	
12 1	X-0	General inspection stage with Nomarski and SIMS	0	1
- U				-
		wafer no.4		- AND
13 0	W-C6	* Pre-epitaxy clean	0	1
	LE-0	Low Pressure Epitaxy; 750degC wafer #4 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	0	1
15 卤	X-0	General inspection stage with Nomarski and SIMS	0	1
- H				24
h.		wafer no.5		18 A.
16 中	W-C6	* Pre-epitaxy clean	0	1
	LE-0	Low Pressure Epitaxy; 750degC water #5 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe tayer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times	0	

Running	k2833s	on	10-26-2005

	1234	56 ID	Description	Count	Cost
18	\$	X-0	General inspection stage with Nomarski and SIMS	1	50
	Щ.		and the second		T. They
	h		wafer no.6	1000	123
19	₽	W-C6	* Pre-epitaxy clean	1	109
20		LE-0	Low Pressure Epitaxy; 750degC wafer #6 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
21	卓	X-0	General inspection stage with Nomarski and SIMS	1	50
	μ	1202		1. 2	1923
	5		wafer no.7		
22	¢	W-C6	* Pre-epitaxy clean	1	109
23		LE-0	Low Pressure Epitaxy; 750degC wafer #7 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
24	南	X-0	General Inspection stage with Nomarski and SIMS	1	50
	μ			1 333	
	Ha I		wafer no.8		Logardy.
25	4	W-C6	* Pre-epitaxy clean	1	109
26		LE-0	Low Pressure Epitaxy; 750degC wafer #8 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
27	12	X-0	General inspection stage with Nomarski and SIMS	1	50
	H.				1.1
	h		wafer no.9		11
28	P	W-C6	* Pre-epitaxy clean	1	109
29		LE-0	Low Pressure Epitaxy; 750degC wafer #9 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
30	\$	X-0	General inspection stage with Nomarski and SIMS	1	50
	μt				514
	H		wafer no.10		
31	4	W-C6	* Pre-epitaxy clean	1	109
32		LE-0	Low Pressure Epitaxy: 750degC wafer #10 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
33	2	X-0	General inspection stage with Nomarski and SIMS	1	50
	μT				
	h		wafer no.11		-
34	2	W-C6	* Pre-epitaxy clean	1	109

Running k	2833s on	10-2	6-2005
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1	12345	6 ID	Description	Count	Cost
35		LE-0	Low Pressure Epitaxy; 750degC wafer #11 (1) Undoped SI 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
36	\$	X-0	General Inspection stage with Nomarski and SIMS	1	50
	-		wafer no.12	1.7.5	
37	\$	W-C6	* Pre-epitaxy clean	1	109
38		LE-0	Low Pressure Epitaxy; 750degC wafer #12 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
39	la L	X-0	General inspection stage with Nomarski and SIMS	1	50
Der 1	h	20	wafer no.13		
40	\$	W-C6	* Pre-epitaxy clean	1	109
41		LE-0	Low Pressure Epitaxy; 750degC wafer #13 (1) Undoped Si 100 nm thick (buffer) (2) Doped Boron 1e18 SiGe layer 10nm thick or less with Ge% 35+-5% (3) Undoped spacer Silicon 40+-10nm thick (4) Repeat (2)-(3) 9 times (5) Undoped Si 100nm thick (cap)	1	747
42	2	X-0	General inspection stage with Nomarski and SIMS	1	50

Running k2675s on 10-26-2005

12345	6 ID	Description	Count	Cost
10	P-EM	E-BEAM Mask/Reticle Writing	7	0
20	G-S12	Title Page: 6 wafers, MATERIAL: P-type <100> 17-33 ohm/cm *	6	0
30	G-1P	Lithography Notes	0	0
49	G-1	Notebook page	0	0
5\$	W-C1	* RCA clean	6	109
62	F4-W0	* Wet oxidation: 600nm, 1000degC: I,rO2,x'wO2,uN2	6	659
7	P-GS1	* STEPPER Photolith: reticle KB09R (NW), D/F: nom. 1.1um resist STANDARD	6	441
8字	G-2	* See Engineer for instructions	0	0
9段	P-RHI	* Hardbake for dry etch	6	100
10	D-01	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	6	1494
112	P-RS	* Resist strip	6	109
120	W-C1	* RCA clean	6	109
13.2	F4-00	* Furnace 4: Load in O2: wet exidation 20nm 900DegC	6	659
140	IP-802	2* Implant Phos+: 1.8E12 P+ 80KeV (CMOS N-Well)	6	747
152	W-C1	* RCA clean	6	109
162	F10-0	* Furnace 10: Load in N2: 1150degC, 10'LN2,8hrsN2,10U'N2	6	659
170	W-C2	* Furning Nitric acid clean, 2nd pot only	6	109
18	P-GS	* STEPPER Photolith: reticle KB09R (AA), D/F: nom. 1.1um resist STANDARD	6	441
192	G-2	* See Engineer for instructions	0	0
200	P-RHI	* Hardbake for implant	6	100
21	IB-0	* Implant B+: 8E15B+ 50KeV	6	747
22 2	P-RS	* Resist strip	6	109
230	W-C2	* Furning Nitric acid clean, 2nd pot only	6	109
24	P-0	+ STEPPER Photolith: Blank, L/F ot the alignment sites (76.2mm apart) 1.1um SPRT resist	6	441
250	G-2	* See Engineer for instructions	0	0
26억	P-RHI	* Hardbake for dry etch	6	100
27	D-011	Etch SiO2 . Anisot. For L/F EBMF/OPTICAL resist OPT80+CHF3+Ar	6	1494
28字	P-RS	* Resist strip	6	109
29字	W-C2	* Fuming Nitric acid clean, 2nd pot only	6	109
30	W-C6	* Pre-epitaxy clean	6	109
31	LE-0	Low Pressure Epitaxy; Wafer #1 (1) Si undoped buffer 100 nm thickness (2) SiGe undoped with Ge 5% 10nm thick by 50 sccm Ge flow with undoped silicon spacer 40nm thick repeat (2) x 9 times (3) Si undoped cap 100 nm thick	1	747
32	LE-0	Low Pressure Epitaxy; Wafer #2 (1) Si undoped buffer 100 nm thickness (2) SiGe undoped with Ge 6% 20nm thick by 50 sccm Ge flow with undoped silicon spacer 40nm thick repeat (2) x 9 times (3) Si undoped cap 100 nm thick	1	747
33	LE-0	Low Pressure Epitaxy; Wafer #3 (1) Si undoped buffer 100 nm thickness (2) SiGe undoped with Ge 6% 30nm thick by 50 sccm Ge flow with undoped silicon spacer 30nm thick repeat (2) x 9 times (3) Si undoped cap 100 nm thick	1	747

Running k2675s on 10-26-2005

12	3456	ID	Description	Count	Cost
34	L	E-0	Low Pressure Epitaxy; Wafer #4	1	747
			(1) Si undoped buffer 100 nm thickness (2) SiCa undoped with Ca 201/ 10pm thick by 50 casm Ca flow	1.18	
	2		(2) Side undoped with Ge 20% form thick by 50 sechi Ge now	11/25	
		10.28	repeat (2) x 9 times	3.3%	
		-	(3) Si undoped cap 100 nm thick	1-21	
35	1	.E-0	Low Pressure Epitaxy; Wafer #5	1	747
211		1715	(1) Si undoped buffer 100 nm thickness		
	2		(2) Side undoped with de 20% zonm thick by 50 sccm de now	C'HIS	
			repeat (2) x 9 times		
			(3) Si undoped cap 100 nm thick	1.2	
36	1	E-0	Low Pressure Epitaxy; Waler #6	1	747
			(1) Si undoped 50 nm thickness	72.0	
			(2) SiGe undoped with Ge 20% 30nm thick by 100 sccm Ge flow		
			reneat (2) x 9 times	6	
	1111	1.00	(3) Si undoped cap 100 nm thick	1 4 50	
Η	http://	100		CON CONTRACTOR	
37 2	,	K-0	General inspection stage by nomarski	6	300
38中		N-C1	* RCA clean	6	109
39	ī	_0-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2	6	441
40字	1	P-0	* Implant PHOS+: 1E16 P+ 25KeV	6	747
41		P-GS1	* STEPPER Photolith: reticle KB09R(CRL), L/F: nom. 1.1um resist	6	441
I		2.0	STANDARD		
425		3-2	See Engineer for instructions	0	400
435		NU N	Dis state 20:1 BHE 25dasC. Until just hydrophabia (200pp LTO OVIDE)	0	244
4482			Dipletch, 2017 birr 25degt, onthi just hydrophobic (roonin LTO OADE)	0	4404
40 J	1119	5-0	optical monitor Target etch depth 800nm		1424
T			START WITH NO 6 AS A SET UP TEST WAFER	1 and	
46史		₩-E1	EKC 265 Post ICP Silicon Etch Passivation Removal	6	105
47	1	P-RS	* Resist strip	6	109
48		N-C2	* Fuming Nitric acid clean, 2nd pot only	6	109
49字		NH-70	Dip etch, 7:1 BHF 25degC. To hydrophobic Si + 20secs.	6	218
50户		N-C1	* RCA clean	6	109
512		_0-10	* LTO deposition: 100nm +- 15nm at 400degC SiH4 and O2	6	441
52		P-GS1	STEPPER Photolith: reticle KB09R AR Dark Field: nom. 1.7um resist	6	441
590		G.2	* See Engineer for instructions	0	(
540		P.RHF	* Hardbake for implant	6	100
55		B-0	* Implant B+: 5E15 B+ 25KeV	6	747
56		P-RS	* Resist strip	6	105
572	1	NH-2	Dip etch, 20:1 BHF 25degC. Until just hydrophobic (100nm LTO OXIDE)	6	218
58	1	N-C2	* Fuming Nitric acid clean, 2nd pot only	6	105
59		S-BC	BPSG: Deposit 100nm undoped Silox + 500nm BPSG (4%P/"10%"B	6	664
Ť			approx)	C Vel	
60岁		RA-1	RTA implant activation 10secs 1100degC (Std.CMOS S & D)	6	1308
61 L		P-GS1	STEPPER Photolith: relicie KB09R CW Dark Field: nom. 1.7um resist	6	441
62.2		3.2	* See Engineer for instructions	0	1
63 2		P.RHE	* Hardbake for dry etch	6	100
64		D-01F	Etch SiO2 . Anisot. For D/F EBMF/OPTICAL resist OPT80+ CHF3+Ar	6	1494
\$			(600 nm LTO Oxide)	1 1 1	
65 2		P-RS	* Resist strip	6	109
66 g	1	N-C2	* Furning Nitric acid clean, 2nd pot only	6	109
672	1	NH-20	Dip etch, 20:1 BHF 25degC. 30 seconds.	6	218

Running k2675s on 10-26-2005

123456	ID	Description	Count	Cost
68	MS-T4	Sputter 1000nm Ti-Al/Si1% + ARC in TRIKON SIGMA	6	2241
69	P-GS2	* STEPPER Photolith: reticle KB09R M1 light Field: nom. 2.2um resist (For Si etch>1um or metal)	6	441
70	G-2	* See Engineer for instructions	0	0
71 9	P-RHE	* Hardbake for dry etch	6	100
72	D-MAT	+ Etch AI, AI/Si and/or Ti . for OPTICAL resist SRS SS1C CI2+SICI4+Ar (WHOLE 4" wfrs)	6	1494
73호	P-RS	* Resist strip	6	109
744	W-C3	* Fuming Nitric Acid clean, metallised wafers	6	109
75 2	F9-H4	* Alloy/ Anneal: 30mins H2/N2 420degC 5'N2,30'H2/N2,5'N2.	6	659
762	X-0	General inspection stage	6	300

Appendix E

Simulation syntex

E1: The simulation of chapter 2 physic of p-i-n photodiode.

化电路运输器 化分离分离 化合同分析 化乙烯合物 化乙烯合物

go atlas

#PiN junction Test

```
mesh
x.m l=0.0 spac=1.0
x.m l=50 spac=0.001
y.m l=0.1 spac=0.001
y.m l=0.2 spac=0.01
y.m l=0.4 spac=0.01
y.m l=0.5 spac=0.01
y.m l=0.65 spac=0.001
y.m l=0.7 spac=0.001
```

region num=1 silicon

electrode top name=emitter electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=50 y.t=0.65 y.b=0.7 doping uniform n.type conc=1.e19 x.l=0 x.r=50 y.t=0.0 y.b=0.05

beam num=1 x.origin=25 y.origin=-0.1 angle=90.0 wavelength=.1

model srh conmob bgn auger fldmob

material taurel.el=0.25e-12 taumob.el=0.25e-12 taurel.ho=0.25e-12 taumob.ho=0.25e-12

method newton trap

solve init

solve vemitter=0.2

save outf=PiNspectral.str

log outf=PiNspectral.log

solve prev b1=1 lambda=0.1 solve prev b1=1 lambda=0.2 solve prev b1=1 lambda=0.3 solve prev b1=1 lambda=0.4 solve prev b1=1 lambda=0.5

```
solve prev b1=1 lambda=0.6
solve prev b1=1 lambda=0.7
solve prev b1=1 lambda=0.8
solve prev b1=1 lambda=0.9
solve prev b1=1 lambda=1.0
```

tonyplot PiNspectral.log

E2: The simulation of chapter 5 for the simulated reverse current and simulated forward current, which is used to evaluate ideality factor.

6% Ge devices forward and reverse bias simulation of various thicknesses.

go atlas

#PN junction Test

mesh x.m l=0.0 spac=0.1 x.m l=1.0 spac=0.1 y.m l=0 spac=0.002 y.m l=0.1 spac=0.002 y.m l=0.11 spac=0.002 y.m l=0.7 spac=0.002 y.m l=0.76 spac=0.002

```
region num=1 material=Silicon y.max=0.1 y.min=0.0
region num=2 material=SiGe y.max=0.11 y.min=0.1 x.comp=0.06
region num=3 material=Silicon y.max=0.15 y.min=0.11
region num=4 material=SiGe y.max=0.16 y.min=0.15 x.comp=0.06
region num=5 material=Silicon y.max=0.2 y.min=0.16
region num=6 material=SiGe y.max=0.21 y.min=0.2 x.comp=0.06
region num=7 material=Silicon y.max=0.25 y.min=0.21
region num=8 material=SiGe y.max=0.26 y.min=0.25 x.comp=0.06
region num=9 material=Silicon y.max=0.3 y.min=0.26
region num=10 material=SiGe y.max=0.31 y.min=0.3 x.comp=0.06
region num=11 material=Silicon y.max=0.35 y.min=0.31
region num=12 material=SiGe v.max=0.36 v.min=0.35 x.comp=0.06
region num=13 material=Silicon y.max=0.4 y.min=0.36
region num=14 material=SiGe y.max=0.41 y.min=0.4 x.comp=0.06
region num=15 material=Silicon y.max=0.45 y.min=0.41
region num=16 material=SiGe y.max=0.46 y.min=0.45 x.comp=0.06
region num=17 material=Silicon y.max=0.5 y.min=0.46
region num=18 material=SiGe y.max=0.51 y.min=0.5 x.comp=0.06
region num=19 material=Silicon y.max=0.55 y.min=0.51
region num=20 material=SiGe y.max=0.56 y.min=0.55 x.comp=0.06
region num=21 material=Silicon y.max=0.76 y.min=0.56
```

electrode top name=emitter

electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.66 y.b=0.76 doping uniform n.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.0 y.b=0.05

model srh conmob bgn auger fldmob fnord eigens=2

method newton carriers=2

output band.param con.band val.band eigens=2

solve init

solve previous outf=K2675at10nm06.str

save outf=K2675at10nm06.str

log outf=K2675at10nm06.log

solve vemitter=0 vstep=0.1 vfinal=5 name=emitter ac freq=1e6

log outf=K2675at10nmF06.log

solve vbase=0 vstep=0.01 vfinal=1 name=base ac freq=1e6

tonyplot K2675at10nmF06.log tonyplot K2675at10nm06.str tonyplot K2675at10nm06.log

mesh

x.m l=0.0 spac=0.1 x.m l=1.0 spac=0.1 y.m l=0 spac=0.002 y.m l=0.1 spac=0.002 y.m l=0.11 spac=0.002 y.m l=0.7 spac=0.002 y.m l=0.76 spac=0.002

```
region num=1 material=Silicon y.max=0.1 y.min=0.0
region num=2 material=SiGe y.max=0.12 y.min=0.1 x.comp=0.06
region num=3 material=Silicon y.max=0.16 y.min=0.12
region num=4 material=SiGe y.max=0.18 y.min=0.16 x.comp=0.06
region num=5 material=Silicon y.max=0.22 y.min=0.18
region num=6 material=SiGe y.max=0.24 y.min=0.22 x.comp=0.06
region num=7 material=Silicon y.max=0.29 y.min=0.24
region num=8 material=SiGe y.max=0.31 y.min=0.29 x.comp=0.06
region num=9 material=Silicon y.max=0.35 y.min=0.31
region num=10 material=SiGe y.max=0.37 y.min=0.35 x.comp=0.06
region num=11 material=Silicon y.max=0.41 y.min=0.37
region num=12 material=SiGe y.max=0.43 y.min=0.41 x.comp=0.06
region num=13 material=Silicon y.max=0.47 y.min=0.43
region num=14 material=SiGe y.max=0.49 y.min=0.47 x.comp=0.06
region num=15 material=Silicon y.max=0.53 y.min=0.49
region num=16 material=SiGe y.max=0.55 y.min=0.53 x.comp=0.06
region num=17 material=Silicon y.max=0.59 y.min=0.55
region num=18 material=SiGe y.max=0.61 y.min=0.59 x.comp=0.06
region num=19 material=Silicon y.max=0.65 y.min=0.61
region num=20 material=SiGe y.max=0.67 y.min=0.65 x.comp=0.06
```

region num=21 material=Silicon y.max=0.76 y.min=0.67

electrode top name=emitter electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.71 y.b=0.76 doping uniform n.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.0 y.b=0.05

model srh conmob bgn auger fldmob fnord eigens=2

method newton carriers=2

output band.param con.band val.band eigens=2

solve init

solve previous outf=K2675at20nm06.str

save outf=K2675at20nm06.str

log outf=K2675at20nm06.log

solve vemitter=0 vstep=0.1 vfinal=5 name=emitter ac freq=1e6

log outf=K2675at20nmF06.log

solve vbase=0 vstep=0.01 vfinal=1 name=base ac freq=1e6

tonyplot K2675at20nmF06.log tonyplot K2675at20nm06.str tonyplot K2675at20nm06.log

mesh

x.m l=0.0 spac=0.1 x.m l=1.0 spac=0.1 y.m l=0 spac=0.002 y.m l=0.1 spac=0.002 y.m l=0.11 spac=0.002 y.m l=0.7 spac=0.002 y.m l=0.76 spac=0.002

```
region num=1 material=Silicon y.max=0.1 y.min=0.0
region num=2 material=SiGe y.max=0.13 y.min=0.1 x.comp=0.06
region num=3 material=Silicon y.max=0.16 y.min=0.13
region num=4 material=SiGe y.max=0.19 y.min=0.16 x.comp=0.06
region num=5 material=Silicon y.max=0.22 y.min=0.19
region num=6 material=SiGe y.max=0.25 y.min=0.22 x.comp=0.06
region num=7 material=Silicon y.max=0.28 y.min=0.25
region num=8 material=SiGe y.max=0.31 y.min=0.28 x.comp=0.06
region num=9 material=Silicon y.max=0.34 y.min=0.31
region num=10 material=SiGe y.max=0.37 y.min=0.34 x.comp=0.06
region num=11 material=Silicon y.max=0.4 y.min=0.37
region num=12 material=SiGe y.max=0.43 y.min=0.4 x.comp=0.06
region num=13 material=Silicon y.max=0.46 y.min=0.43
region num=14 material=SiGe y.max=0.49 y.min=0.46 x.comp=0.06
region num=15 material=Silicon y.max=0.52 y.min=0.49
region num=16 material=SiGe y.max=0.55 y.min=0.52 x.comp=0.06
region num=17 material=Silicon y.max=0.58 y.min=0.55
```

region num=18 material=SiGe y.max=0.61 y.min=0.58 x.comp=0.06 region num=19 material=Silicon y.max=0.64 y.min=0.61 region num=20 material=SiGe y.max=0.67 y.min=0.64 x.comp=0.06 region num=21 material=Silicon y.max=0.76 y.min=0.67

electrode top name=emitter electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.71 y.b=0.76 doping uniform n.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.0 y.b=0.05

model srh conmob bgn auger fldmob fnord eigens=2

method newton carriers=2

output band.param con.band val.band eigens=2

solve init

solve previous outf=K2675at30nm06.str

save outf=K2675at30nm06.str

log outf=K2675at30nm06.log

solve vemitter=0 vstep=0.1 vfinal=5 name=emitter ac freq=1e6

log outf=K2675at30nmF06.log

solve vbase=0 vstep=0.01 vfinal=1 name=base ac freq=1e6

tonyplot K2675at30nmF06.log tonyplot K2675at30nm06.str tonyplot K2675at30nm06.log

20% Ge devices forward and reverse bias simulation of various

thicknesses.

go atlas

#PN junction Test

```
mesh
x.m l=0.0 spac=0.1
x.m l=1.0 spac=0.1
y.m l=0 spac=0.002
y.m l=0.1 spac=0.002
y.m l=0.11 spac=0.002
y.m l=0.7 spac=0.002
y.m l=0.76 spac=0.002
```

region num=1 material=Silicon y.max=0.1 y.min=0.0 region num=2 material=SiGe y.max=0.11 y.min=0.1 x.comp=0.2 region num=3 material=Silicon y.max=0.15 y.min=0.11 region num=4 material=SiGe y.max=0.16 y.min=0.15 x.comp=0.2 region num=5 material=Silicon y.max=0.2 y.min=0.16 region num=6 material=SiGe y.max=0.21 y.min=0.2 x.comp=0.2 region num=7 material=Silicon y.max=0.25 y.min=0.21 region num=8 material=SiGe y.max=0.26 y.min=0.25 x.comp=0.2 region num=9 material=Silicon y.max=0.3 y.min=0.26 region num=10 material=SiGe y.max=0.31 y.min=0.3 x.comp=0.2 region num=11 material=Silicon y.max=0.35 y.min=0.31 region num=12 material=SiGe y.max=0.36 y.min=0.35 x.comp=0.2 region num=13 material=Silicon y.max=0.4 y.min=0.36 region num=14 material=SiGe y.max=0.41 y.min=0.4 x.comp=0.2 region num=15 material=Silicon y.max=0.45 y.min=0.41 region num=16 material=SiGe v.max=0.46 v.min=0.45 x.comp=0.2 region num=17 material=Silicon y.max=0.5 y.min=0.46 region num=18 material=SiGe y.max=0.51 y.min=0.5 x.comp=0.2 region num=19 material=Silicon y.max=0.55 y.min=0.51 region num=20 material=SiGe y.max=0.56 y.min=0.55 x.comp=0.2 region num=21 material=Silicon y.max=0.76 y.min=0.56

electrode top name=emitter electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.66 y.b=0.76 doping uniform n.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.0 y.b=0.05

model srh conmob bgn auger fldmob fnord eigens=2

method newton carriers=2

output band.param con.band val.band eigens=2

solve init

solve previous outf=K2675at10nm.str

save outf=K2675at10nm.str

log outf=K2675at10nm.log

solve vemitter=0 vstep=0.1 vfinal=5 name=emitter ac freq=1e6

#log outf=K2675at10nmF.log

#solve vbase=0 vstep=0.1 vfinal=5 name=base ac freq=1e6

#tonyplot K2675at10nmF.log tonyplot K2675at10nm.str tonyplot K2675at10nm.log

mesh x.m l=0.0 spac=0.1 x.m l=1.0 spac=0.1 y.m l=0 spac=0.002

```
y.m l=0.1 spac=0.002
y.m l=0.11 spac=0.002
y.m l=0.7 spac=0.002
y.m l=0.76 spac=0.002
```

```
region num=1 material=Silicon y.max=0.1 y.min=0.0
region num=2 material=SiGe y.max=0.12 y.min=0.1 x.comp=0.2
region num=3 material=Silicon y.max=0.16 y.min=0.12
region num=4 material=SiGe y.max=0.18 y.min=0.16 x.comp=0.2
region num=5 material=Silicon y.max=0.22 y.min=0.18
region num=6 material=SiGe y.max=0.24 y.min=0.22 x.comp=0.2
region num=7 material=Silicon y.max=0.29 y.min=0.24
region num=8 material=SiGe y.max=0.31 y.min=0.29 x.comp=0.2
region num=9 material=Silicon y.max=0.35 y.min=0.31
region num=10 material=SiGe y.max=0.37 y.min=0.35 x.comp=0.2
region num=11 material=Silicon y.max=0.41 y.min=0.37
region num=12 material=SiGe y.max=0.43 y.min=0.41 x.comp=0.2
region num=13 material=Silicon y.max=0.47 y.min=0.43
region num=14 material=SiGe y.max=0.49 y.min=0.47 x.comp=0.2
region num=15 material=Silicon y.max=0.53 y.min=0.49
region num=16 material=SiGe y.max=0.55 y.min=0.53 x.comp=0.2
region num=17 material=Silicon y.max=0.59 y.min=0.55
region num=18 material=SiGe y.max=0.61 y.min=0.59 x.comp=0.2
region num=19 material=Silicon y.max=0.65 y.min=0.61
region num=20 material=SiGe y.max=0.67 y.min=0.65 x.comp=0.2
region num=21 material=Silicon y.max=0.76 y.min=0.67
```

electrode top name=emitter electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.71 y.b=0.76 doping uniform n.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.0 y.b=0.05

model srh conmob bgn auger fldmob fnord eigens=2

method newton carriers=2

output band.param con.band val.band eigens=2

solve init

solve previous outf=K2675at20nm.str

save outf=K2675at20nm.str

log outf=K2675at20nm.log

solve vemitter=-1 vstep=0.1 vfinal=5 name=emitter ac freq=1e6

#log outf=K2675at20nmF.log

#solve vbase=0 vstep=0.1 vfinal=5 name=base ac freq=1e6

#tonyplot K2675at20nmF.log tonyplot K2675at20nm.str tonyplot K2675at20nm.log

```
mesh
x.m l=0.0 spac=0.1
x.m l=1.0 spac=0.1
y.m l=0 spac=0.002
y.m l=0.1 spac=0.002
y.m l=0.11 spac=0.002
y.m l=0.7 spac=0.002
y.m l=0.76 spac=0.002
```

```
region num=1 material=Silicon y.max=0.1 y.min=0.0
region num=2 material=SiGe y.max=0.13 y.min=0.1 x.comp=0.2
region num=3 material=Silicon y.max=0.16 y.min=0.13
region num=4 material=SiGe y.max=0.19 y.min=0.16 x.comp=0.2
region num=5 material=Silicon y.max=0.22 y.min=0.19
region num=6 material=SiGe y.max=0.25 y.min=0.22 x.comp=0.2
region num=7 material=Silicon v.max=0.28 v.min=0.25
region num=8 material=SiGe y.max=0.31 y.min=0.28 x.comp=0.2
region num=9 material=Silicon y.max=0.34 y.min=0.31
region num=10 material=SiGe y.max=0.37 y.min=0.34 x.comp=0.2
region num=11 material=Silicon y.max=0.4 y.min=0.37
region num=12 material=SiGe y.max=0.43 y.min=0.4 x.comp=0.2
region num=13 material=Silicon y.max=0.46 y.min=0.43
region num=14 material=SiGe v.max=0.49 v.min=0.46 x.comp=0.2
region num=15 material=Silicon y.max=0.52 y.min=0.49
region num=16 material=SiGe y.max=0.55 y.min=0.52 x.comp=0.2
region num=17 material=Silicon y.max=0.58 y.min=0.55
region num=18 material=SiGe y.max=0.61 y.min=0.58 x.comp=0.2
region num=19 material=Silicon y.max=0.64 y.min=0.61
region num=20 material=SiGe y.max=0.67 y.min=0.64 x.comp=0.2
region num=21 material=Silicon y.max=0.76 y.min=0.67
```

electrode top name=emitter electrode bottom name=base

doping uniform conc=1e15 p.type doping uniform p.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.71 y.b=0.76 doping uniform n.type conc=1.e19 x.l=0 x.r=1.0 y.t=0.0 y.b=0.05

model srh conmob bgn auger fldmob fnord eigens=2

method newton carriers=2

output band.param con.band val.band eigens=2

solve init

solve previous outf=K2675at30nm.str

save outf=K2675at30nm.str

log outf=K2675at30nm.log

solve vemitter=0 vstep=0.1 vfinal=5 name=emitter ac freq=1e6

#log outf=K2675at30nmF.log

#solve vbase=0 vstep=0.1 vfinal=5 name=base ac freq=1e6

#tonyplot K2675at30nmF.log tonyplot K2675at30nm.str tonyplot K2675at30nm.log

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Appendix F

Publications

P. Iamraksa, N. S. Lloyd and D. M. Bagnall, "Si/SiGe near-infrared photodetectors grown using low pressure chemical vapour deposition," The 6th International Conference on Materials for Microelectronics and Nanoengineering (MFMN 2006), 29th - 31st October 2006, Cranfield Management Development Centre, UK.

M R Hashim, Kifah Q Salih, D Bagnall and P Iamraksa, Modification of Optical Properties of Si_{1-x}Ge_x/p-Si(100) MQWs grown by LPCVD for Photonic Applications, Electrochemical Society Proceedings vol 2004-07, pp299-303, 2004.