UNIVERSITY SOUTHAMPTON

THE APPLICATION OF THICK FILM TECHNIQUES TO THE PRODUCTION OF THE DYE SENSITISED SOLAR CELL

JAMES STEPHEN BAYNHAM MASON

MASTER OF PHILOSOPHY

FACULTY OF SCIENCE

SCHOOL OF CHEMISTRY

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ABSTRACT

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by James Stephen Baynham Mason

The dye sensitised or Grätzel solar cell (DSSC) offers a photovoltaic technology which can be mass produced at relatively low cost using conventional thick film techniques for the production of the electrodes. The photoelectrode comprises of a mesoporous titanium dioxide layer with the counter electrode containing a catalyst layer for the reduction of triiodide to iodine. The TiO_2 layer is dyed with a ruthenium polypyridyl complex to sensitise the electrode to the incoming solar radiation. The two electrodes are sealed with a gasket encapsulating an organic liquid comprising the triiodide / iodide redox electrolyte.

The repeated, controlled deposition of electrodes on 50 mm square substrates has been demonstrated using screen printing equipment capable of printing much larger areas. Different TiO_2 pastes were evaluated for thick film deposition and film quality. The capability for printing complicated TiO_2 film patterns has also been demonstrated. The same techniques were also used for the preparation of the platinum counter electrode to achieve high open circuit potentials for the cell.

It is well known that the performance of the dye sensitised solar cell reduces with increasing cell area. One reason for this degradation is the increasing ohmic resistance which can occur in the transparent current collector with increasing electrode size; resulting in a reduction of output power and fill factor of the cell. Improving the ohmic resistance of both current collectors is an important pre-requisite for the commercial development of DSSC devices. Printed electrodes provide the opportunity to easily implement improved interconnections within the electrode to significantly reduce ohmic loss. This design of the electrode and interconnect layers using thick film techniques is covered in this work, together with their optimisation using computer simulations to model the ohmic performance of the electrode.

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CHAPTER 1: INTRODUCTION

1.1 The opportunity for photovoltaic technologies

The direct generation of electricity from solar radiation using photovoltaic devices is an attractive renewable energy technology. As the cost of fossil fuel based electricity generation increases and the environmental implications of these technologies become more apparent; then interest has increased in using photovoltaic technology for power generation. The silicon solar cell currently dominates the photovoltaic industry with an efficiency of conversion of around 15% for commercial modules. However the silicon cell is expensive to produce mainly due to the high cost of producing semiconductor grade silicon. Over the last thirty years, extensive research and development resource has been expended in trying to reduce the cost of manufacturing silicon cells. Although progress has been made, the best efficiencies are still obtained with the mono crystalline silicon cell which has changed little since its invention at Bell Laboratories in 1954. Reducing the cost of manufacture using multi-crystalline or thin film structures degrades the efficiency of the cell and can affect other parameters such as reliability. However, lower efficiency can still be acceptable if the overall cost of power generation is reduced.

In 1991, O'Regan and Grätzel announced a sensitised nanocrystalline photovoltaic device [1.1] with a conversion efficiency of 7.1% under solar illumination. This efficiency is comparable to commercial amorphous silicon cells and the technology offers a lower cost solution for the production of devices; this could make the large scale use of photovoltaic devices for electricity generation feasible. In their paper, O'Regan and Grätzel stated that the cost of generation from the commercial photovoltaic devices then available was about ten times that of using conventional methods for electricity generation. This differential has reduced in the intervening years. In 2002, the National Renewable Energy Laboratory produced an energy cost trend [1.2] for photovoltaic generation which showed that the cost of generating a unit of electricity (1 kWh) at 25 US cents in 2000, this was approximately three times that of using conventional sources. The crossover point at which photovoltaic devices can compete subsidy-free with conventional generation is not expected until 2015 at the earliest [1.3].

A full description of commercial photovoltaic technology is widely available [1.4] and the potential for the dye sensitised solar cell as a low cost competitor to silicon devices is well known [1.5]. The construction of the dye sensitised solar cell is relatively straightforward and can utilise similar production technologies to those already established for flat panel display products. A significant challenge would be in producing the nanocrystalline titanium dioxide film required for the photoelectrode. Within the microelectronics industry, thick film techniques are routinely used to deposit large area films. The adoption of this method for depositing a large area photo-electrode offers a potentially low cost production process. It is well known that the efficiency of the dye sensitised solar cell reduces with increasing area [1.6] and this work also addresses this issue, exploiting the inherent printing capability of the thick film process, to facilitate a more efficient electrode design.

1.2 The dye sensitised solar cell

A photovoltaic device uses the incoming solar radiation to generated charge carriers and then separates these carriers to the respective cell electrodes. In a silicon solar cell, the charge carriers (holes and electrons) are generated in a p-n semiconductor junction and the in-built field of that junction then separates the holes and electron to the respective sides of the junction. In a photo-electrochemical cell, such as the dye sensitised solar cell, the junction used for the charge separation is a semiconductor-electrolyte interface rather than the solid-state junction used in silicon and other semiconductor photovoltaic devices.

A cross section of the dye sensitised solar cell is shown in Figure 1. A semiconductor, in this case the anatase form of titanium dioxide (TiO_2), is deposited as a thin layer on a transparent conductive glass substrate. This film is made up of nanoparticles of TiO_2 , typically around 25 nm in diameter, which have been fused together to form a nanocrystalline structure. The film is typically around 20 μm thick and is mesoporous, having fine pores with typical diameters less than 50 nm. It has a very large active surface area and so provides a relatively high number of sites where sorption processes can occur.

In a semiconductor, incoming solar radiation generates charge carriers by lifting electrons from the valence band into the conduction band. The bandgap of the material determines the energy threshold required for this step and the photo-electric effect relates the available energy to the incoming frequency of the radiation. If the frequency is lower than the bandgap threshold then no photo-generation of charge carriers occurs. If the frequency of the incoming radiation is higher than the bandgap threshold then only the energy required to raise the electron is absorbed. This process sets the fundamental maximum efficiency of the cell which for a single junction device is approximately 33%.

In photo-electrochemical cells, semiconductor materials which have a bandgap sensitive to incoming solar radiation are also susceptible to corrosion processes at the semiconductor-electrolyte interface which restrict their practical application. A wide bandgap semiconductor, such as TiO_2, provides better resilience against these photo-corrosion processes but have an absorption region is in the ultraviolet section of the electromagnetic spectrum. However by using a dye to sensitise the material to the visible spectrum, it is possible to achieve photogeneration of carriers in the TiO_2 film from the visible spectrum with a reasonable efficiency. It was this approach, using a redox dye, which led to the advance reported by O'Regan and Grätzel [1.1].

Ruthenium based polypyridine dyes have been used as very efficient photosensitisers in dye sensitised solar cells. Excitation of the dye by the incoming solar radiation results in an electron transfer from the metal to the π^* orbital of the carboxylated bipyridyl ligand. The carboxylate component of the dye ensures attachment to the TiO_2 layer through chemisorption with a monolayer of the dye attached to the TiO_2 surface. Consequently the excited electron is released through into the conduction band of the TiO_2. The incident photon to current conversion efficiency is typically high and can exceed 60%, the electron is also released quickly into the TiO_2. The charge transport mechanism through the mesoporous TiO_2 film is complex but is highly efficient despite the low inherent conductivity of the film and the absence of an electric field. Essentially the electron transport is diffusion-like with the electron transferring to the transparent conductive oxide layer which provides the negative terminal of the cell.

The state of the dye is restored by an electron donation from the electrolyte which also prevents the recapture of the conduction band electron from the TiO_2 film by the oxidised dye. The electrolyte is usually an organic solvent containing a redox system such as the iodide / triiodide couple which is a two electron reaction:

$$3\,I^- \rightleftharpoons I_3^- + 2e^-$$

The iodide is oxidised in the vicinity of the dye and yields two electrons which can restore two dye molecules to their original state. The triiodide diffuses to the counter electrode where it is reduced by two incoming electrons back to iodide. A catalyst is deposited on the counterelectrode, usually platinum, for this reaction.

The electrons received at the photoelectrode flow through the external load, producing work, and then back to the counterelectrode. The dye should be stable enough to allow at least 100 million turnover cycles which corresponds to around twenty years of exposure to natural light and this has been demonstrated with some of the ruthenium based sensitisers. All of the components of the dye sensitised solar cell are relatively low cost and readily available materials with the exception of the platinum catalyst and ruthenium based sensitiser. However both the catalyst and dye are used in small amounts within the cell which should also require significantly less energy to produce than silicon photovoltaic devices.

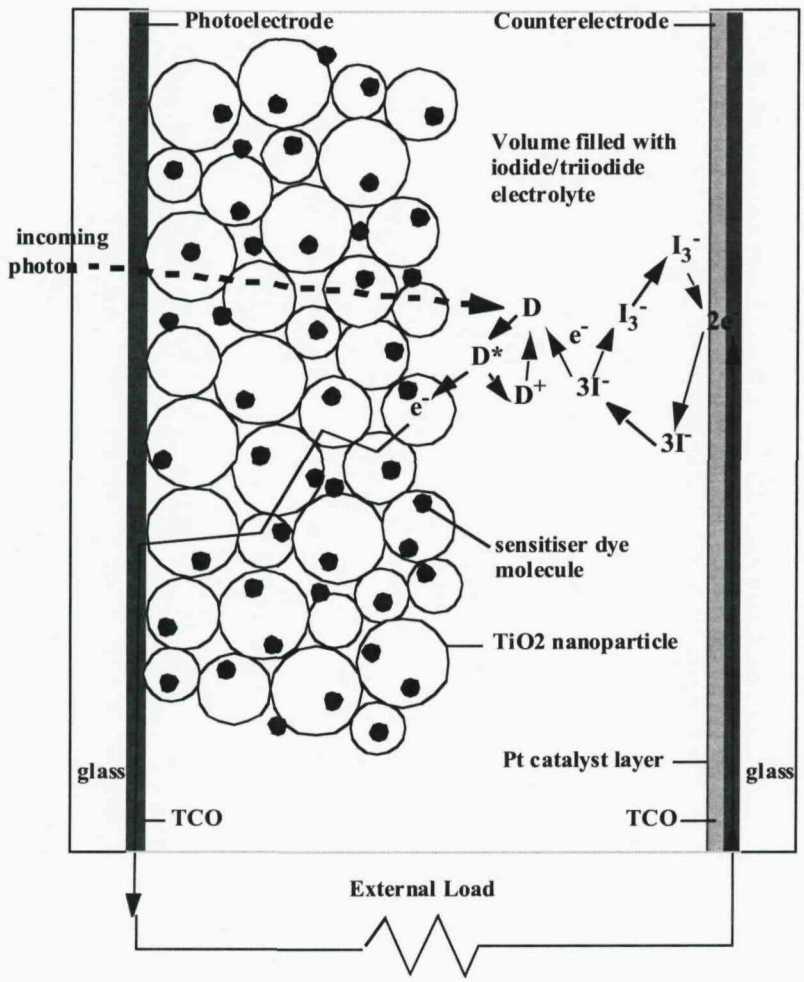


Figure 1: Construction and operation of a nanocrystalline TiO_2 dye sensitised solar cell.

The incoming photon excites the dye species, D, which is attached to the TiO_2 film to a temporary state, D*. The dye then injects an electron into the TiO_2 film and this electron passes through the mesoporous structure into the TCO layer of the photoelectrode. The photoelectrode forms the negative terminal of the cell and the electron flows through the external load, providing energy, and back to the counterelectrode. The ionised dye, D^+, is then reduced back to its original state, D, by the redox electrolyte. The iodide ion is oxidised to triiodide, I_3^-, and gives up two electrons which reduce two dye ions. The triiodide ion then diffuses through the electrolyte back to the counterelectrode where two incoming electrons reduce it back to iodide. The iodide ion then diffuses back to the mesoporous TiO_2 film to repeat the redox process.

1.3 The application of thick film techniques

Film deposition technologies are generally classified as thin film, where the thickness is typically less than one micron, or thick film where the film thicknesses can reach several hundred microns. In thick film manufacture, the technique of screen printing is used to deposit a paste onto a substrate to form a wet film of controlled thickness and with a pattern defined by the screen. This film is then dried and heat treated to form the final structure.

The screen is built from a mesh, which is normally either stainless steel or a polyester material, and this is attached to a frame and held under tension. The pattern to be printed is defined on the mesh using an emulsion layer to close off areas of the mesh corresponding to unprinted regions. A paste of the material to be printed is pressed through the screen onto the substrate by means of a squeegee blade. As the squeegee blade traverses the screen, spreading the paste in front, a shearing action causes a decrease in viscosity of the paste. This causes the paste to pass through the exposed, patterned areas of the mesh and onto the substrate. As the squeegee passes across the substrate, the screen peels away from the substrate behind the squeegee blade leaving a well defined, printed wet film.

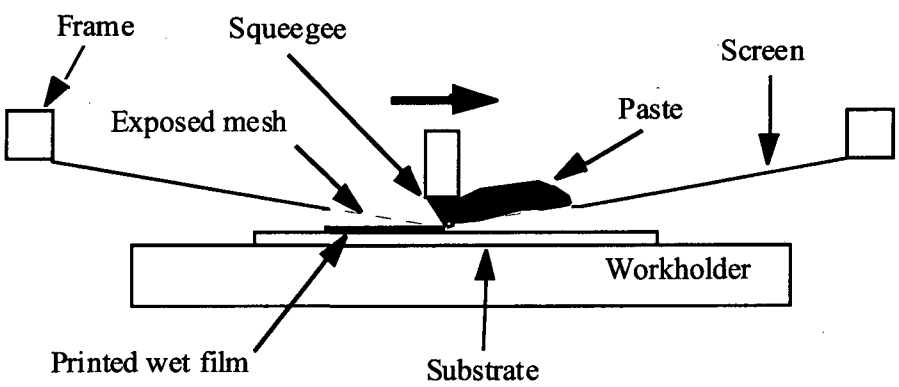


Figure 2: The screen printing process.

The operation of the screen printing process is shown in shown in Figure 2, the squeegee blade is held under pressure against the screen which itself is held off from the surface of the substrate by a set height, known as the snap-off distance. The squeegee blade speed is also important as it spreads the paste in front of the blade and applies the shearing force to push it through the exposed areas of the screen. The mesh number of the screen, which is the number of threads per unit distance in the mesh, and its opening size are both fundamental parameters. These control how much paste can pass though the screen and onto the substrate, setting the thickness of the deposited film.

The paste properties are also important in this process and the rheology of the paste, which determines how the material deforms and flows under the applied stress, has a major influence on the image transfer quality. The pastes used for the TiO_2 film deposition are colloidal suspensions with the TiO_2 nanoparticles held within a carrier medium. These materials often exhibit thixotropic properties where the paste becomes more fluid when disturbed; causing the viscosity of the paste to reduce as it experiences shear stress from the squeegee blade. Clearly there are many variables in the screen printing process which set the thickness and quality of the deposited wet film.

After the screen printing step, the wet film is left to level and then undergoes a drying process. At this stage, the film comprises of loose conglomerates of fine particles which normally need to undergo some form of heat treatment step. In the case of the TiO_2 film, a sintering step is used where the nanoparticles are fused together to form a mesoporous structure. These heat treatment steps are usually at high temperature and often use an oven with a transport belt normally referred to as a belt furnace.

The thick film process offers several important advantages to the production of large area dye sensitised solar cells. It is a relatively low cost technique which is well suited for depositing films onto the large area transparent conductive substrates used as the starting material for cell manufacture. The screen printing process can also print consistently with excellent repeatability. In this research, the main interest was in applying thick film techniques to prepare the mesoporous TiO_2 layer for the photo-electrode. The process was also used to deposit the platinum layer which is the

catalyst for the counterelectrode. The ability to print intricate shapes facilitates the implementation of more elaborate electrode structures which can improve cell efficiency. Improving the current collection across the area of the electrode using an interconnect layer is also possible with this technology; which can support both the deposition of the layer and the patterning of the surrounding TiO_2 electrode material.

1.4 Literature review

The benefits of applying a printing technology to the manufacture of photovoltaic cells have been apparent for many years. The ability to manufacture such devices at a significantly lower cost than the established silicon technologies has been a long term objective of the photovoltaic industry. Burgelman [1.8] provides a good overview of using screen printing techniques in the manufacture solar cells. In this case, the techniques were applied to cadmium sulphide and cadmium telluride photovoltaic technologies.

After the invention of the dye sensitised solar cell, the deposition of the TiO_2 film using a colloidal suspension of TiO_2 nanoparticles became a well established technique. Nazeerudin et al [1.9] describe this method together with a doctor blade technique for depositing the film onto the surface of the TCO substrate. This method has been used extensively by other researchers such as Burnside et al [1.10]. However, although the doctor blade technique is suitable for the small cells used in laboratory research (with areas of several cm^2), it is difficult to produce wet films of reproducible thickness and coverage using this method, especially with large area electrodes.

The application of screen printing techniques to achieve more consistent film deposition started in the late 1990s with attempts to develop larger area DSSC devices. A research program partly funded by the European Commission [1.11] developed a screen printing process for large area (4 cm^2) electrodes which also included silver printed lines for the contacts. The associated report stated that 'at larger sizes series resistance losses, leading to lower fill factors are often observed' ; highlighting that performance degraded with increasing cell area.

The development of screen printed TiO_2 films continued with Burnside et al [1.12] demonstrating the feasibility of reproducibly making a mesoporous, multiple layer thick film structure using screen printing as a deposition process. However, the difficulty of scaling up the area of the DSSC is shown by the separate classes in the Solar Cell Efficiency Tables {1.6] depending on cell area. The best efficiency of 10.4% is achieved with a cell having an area of just $1cm^2$, in the submodule class the efficiency reduces to 6.3% with a cell area of $26.5cm^2$. The poor performance of large area DSSC devices due to the high series resistance of the TCO glass substrates is acknowledged by Ramasamy et al [1.13] and they report a three times increase in maximum power with an embedded silver power grid. These authors also state that there is scope for further improvement through adjustment of the distance between the silver grids and the dimensions of the active layer.

Researchers in large area DSSC devices have realised that improvements are required to reduce the series resistance of the electrode connection. A common approach has been the use of simple interdigitated structures with a low resistance ohmic connection (referred to as an interconnect layer or power grid) between the active areas of the electrode to mitigate the relatively high resistance of the TCO substrate. However there appears to have little work performed in determining the optimum design of such power grid structures.

This work is focussed on exploiting the screen printing process to demonstrate that complex TiO_2 mesoporous structuress can be produced for the photoelectrode. This patterned TiO_2 film could surround a more complicated interconnect layer topology, thereby offering significantly improved performance through a lower series resistance of the cell. The interconnect layer could also be deposited by thick film techniques, or by some other technique, onto the TCO starting material. In addition, simulation techniques are also adopted to understand how the most efficient layout of the interconnect layer within the photoelectrode can be determined.

CHAPTER 2: FABRICATION OF THE DYE SENSITISED SOLAR CELL USING THICK FILM TECHNIQUES

2.1 Design of the dye sensitised solar cell for laboratory testing

The construction of the dye sensitised solar cell used in this research is shown in Figure 3 and comprises of the following components:

- A photoelectrode comprising of a TCO glass substrate with a deposited mesoporous TiO_2 film which is stained with the photosensitiser dye.
- A square gasket which encloses the active area of the photoelectrode, defined by the area of TiO_2 film. This gasket defines the separation between the two electrodes. A liquid iodide / triiodide electrolyte is inserted into the cavity defined by this gasket and the inner surfaces of the two electrodes.
- A counterelectrode comprising of a TCO glass substrate, pre-drilled for electrolyte insertion, which has a platinum catalyst layer deposited over the active area of the electrode.
- Contact strips, formed from tin plated adhesive copper tape, which allow an efficient connection to be made to the TCO substrate of each electrode.

The cell was built from square electrodes with a size of 50 mm x 50 mm since this is a standard format for the thick film microelectronics industry and enabled the use of pre-existing tooling on the screen printing equipment. The TCO glass substrate thickness for the electrodes was normally 1.1 mm, although other thicknesses were used up to 3.2 mm. It was decided to use TCO substrate material for both the photoelectrode and counterelectrode since this simplified the production process and also allowed a translucent cell to be produced. Clearly a different substrate could be used for the counterelectrode which does not necessarily need to be transparent.

An overlap area of 45 mm x 50 mm with these electrodes provides a 5 mm wide contact area on the edge of each electrode for the electrical connection and this is made using the contact strip. A 5 mm border around the overlap area provides the

location for the sealing gasket resulting in an enclosed area of 35 mm x 40 mm which corresponds to an active cell area of 14 cm^2 for the DSSC. An exploded view of the cell showing the assembly of these components is shown in Figure 4.

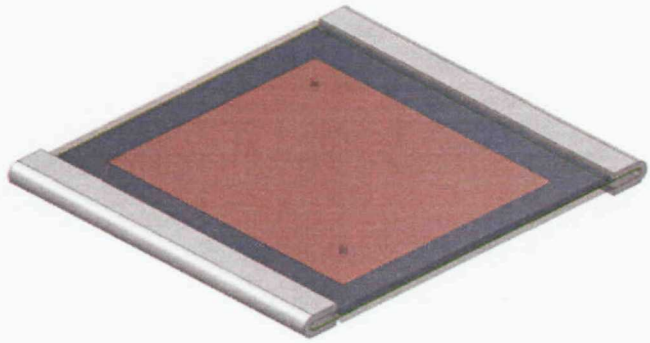


Figure 3: The design of the dye sensitised solar cell used for laboratory testing shown with the counterelectrode at the top.

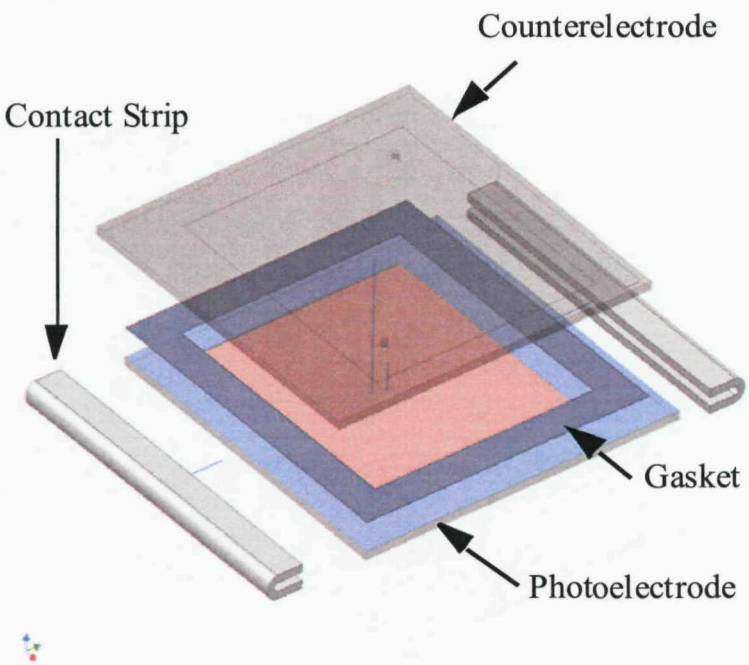


Figure 4: An exploded view of the laboratory DSSC showing the assembly of the components.

The liquid electrolyte is inserted using the holes in the counterelectrode which are subsequently sealed.

2.2 Preparation of the mesoporous TiO_2 electrode

The TiO_2 layer is deposited by screen printing using a paste which is a colloidal preparation of highly dispersed TiO_2 nanoparticles. After drying, this film undergoes a high temperature sintering process which forms the mesoporous structure. The TiO_2 film is then photo-sensitised by soaking the electrode in a ruthenium-polypyridine dye solution to form a monolayer of dye absorption at the TiO_2 film surface.

2.2.1 Paste preparation

A commercially available TiO_2 paste designed for screen printing and containing nanocrystalline TiO_2 particles was obtained from Solaronix SA and was used during the earlier phases of research. Laboratory prepared pastes were later used and these were all produced from a highly dispersed TiO_2 nanopowder (DeGussa Aeroxide TiO_2 P25) which is predominantly in the anatase form. This material has a specific surface area (BET) of 50 ± 15 m^2/g and a specific primary particle size of 21 nm from the manufacturer's specification. A colleague [2.1] has checked how the BET correlated with the line broadening in XRD analysis. The domain size from the half height line width worked out to be about 27 nm. Using this data as the particle diameter in the formula to find the specific surface area:

$$S = \frac{6}{XRDdensityofTiO2 \cdot ParticleDiameter}$$

produced a result of around 50 m^2/g. This material was used to produce several pastes, the initial starting point for these pastes was derived from [2.2] and [1.12]. These preparations were subsequently developed to improve the wet film deposition quality with the thick film process, the pastes are identified as:

1) Paste 1 was the Solaronix Ti-Nanoxide T/SP screen print paste [2.2] which contains colloidal anatase particles with a size of 13 nm and surface area of 120 m^2/g (BET).

2) Paste 2, derived from [1.11], was prepared using 9 g DeGussa P25 TiO_2 , 16.4g terpinol (Fluka 86480), 0.17 g 4-hydroxy benzoic acid (Aldrich 240141) and 0.40 g ethylcellulose (Fluka 00907).
3) Paste 3, derived from [2.2], was prepared using 9 g DeGussa P25 TiO_2 , 25 ml 2-ethyl-1-hexanol (Aldrich 538051), 0.23 g 4-hydroxy-benzoic acid (Aldrich 240141), 3 g polyethylene glycol (Fluka 81170) and 0.58 g ethyl cellulose (Fluka 00907).
4) Paste 4, adapted from Paste 2, was prepared using 10.26 g DeGussa P25 TiO_2 , 0.24 g 4-hydroxy benzoic acid (Aldrich 240141), 25.3 g terpinol (Fluka 86480) and 0.47 g ethylcellulose (Fluka 00907).

The pastes were subjected to agitation and ball milling to improve their rheological properties for screen printing.

2.2.2 Screen design

The screen was designed to deposit the TiO_2 layer onto the 35 mm x 40 mm active area of the photoelectrode defined by the cell design described in section 2.1. The polyester mesh screen design was based on the Dek 1202 screen printer format which can be used with both the Auriel C880 and Dek 248 screen printers.

In general, the tolerance of print features should be around three times [2.3] that of either the wire diameter or the mesh knuckle, which is where the wires cross over each other on the mesh. The mesh opening and its thickness are factors which set the quantity of paste which passes through the screen and is deposited onto the substrate. An emulsion layer is used to define areas which are closed off to the paste on the mesh. The screen is mounted, under tension, on a lightweight, aluminium frame.

A mesh size of 43 threads/cm and wire diameter of 80 μm was generally used on the screen designs for the TiO_2 film deposition, this corresponds to an open area within the mesh of 41%. Patterned screens were designed using a printed circuit design software package (EasyPC from Number One Systems) and this software provides industry standard Gerber format output data for the screen manufacturer.

2.2.3 Thick film deposition

The TiO_2 wet film was screen printed using either an Auriel C880 or Dek 248 screen printer. The Aurel C880 was used for the majority of depositions since it provided convenient, manual control of the printing process. The Dek 248, shown in Figure 6, is designed for production applications and can print an area up to 432 mm x 405 mm. It was used to demonstrate the viability of using such equipment to print electrodes and which could be significantly increased in size.

The Aurel C880 is shown in Figure 5 and holds the substrate under vacuum on a carriage mounted work holder which can be moved and positioned under the screen. The substrate can be aligned to the screen pattern using theta (rotation), x and y micrometer adjustments. The snap height adjustment was set for a clearance between the bottom of the screen and top of the substrate of approximately 1mm. The printer was set up in normal mode with a single printing pass, the flood plate was not used and the paste was reapplied at the front of the squeegee after each pass. The normal setting of the downstop height was 1.0 and the squeegee pressure was set at 6.1.

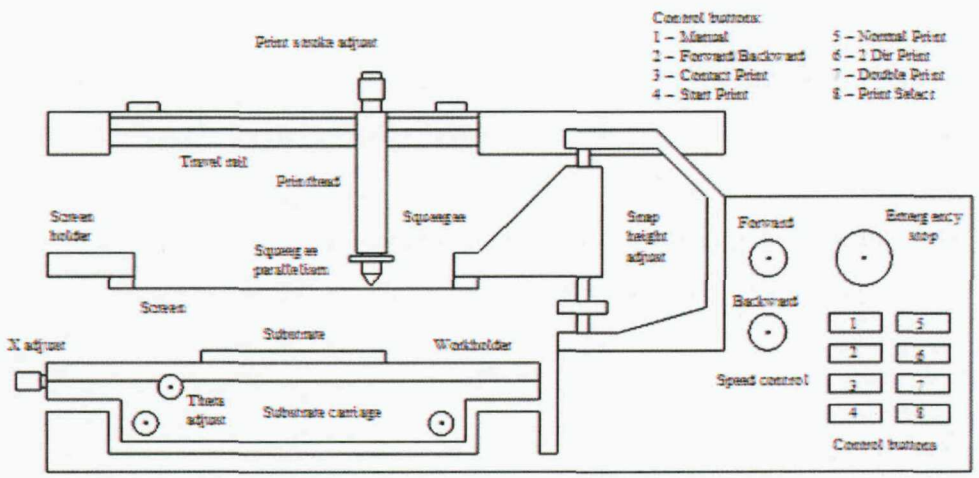


Figure 5: Front and side view of the Aurel C880 Screen Printer (from [2.4]).

After printing, the wet film was left to self level and its thickness was measured with a Z-Check 500 microscope which has an accuracy estimated at approximately ±2μm. The film was then dried at 70°C for at least 30 minutes in a Gallenkamp oven prior to the sintering stage.

Figure 6: The DEK248 screen printer.

2.2.4 Sintering

In the sintering step, the dried TiO_2 film is heat treated such that the nanoparticles of TiO_2 come together in a coalescence phase and fuse together to form the mesoporous structure. The volatile constituents of the original paste which have not already been lost during the drying operation are also dissipated during this operation.

The sintering operation was normally performed using a belt furnace which heated the TiO_2 film to a temperature of 450 °C for up to 30 minutes. The DEK840 and BTU six chamber belt furnaces were most commonly used and Figure 7 shows the temperature profile used with the latter for sintering of the TiO_2 film.

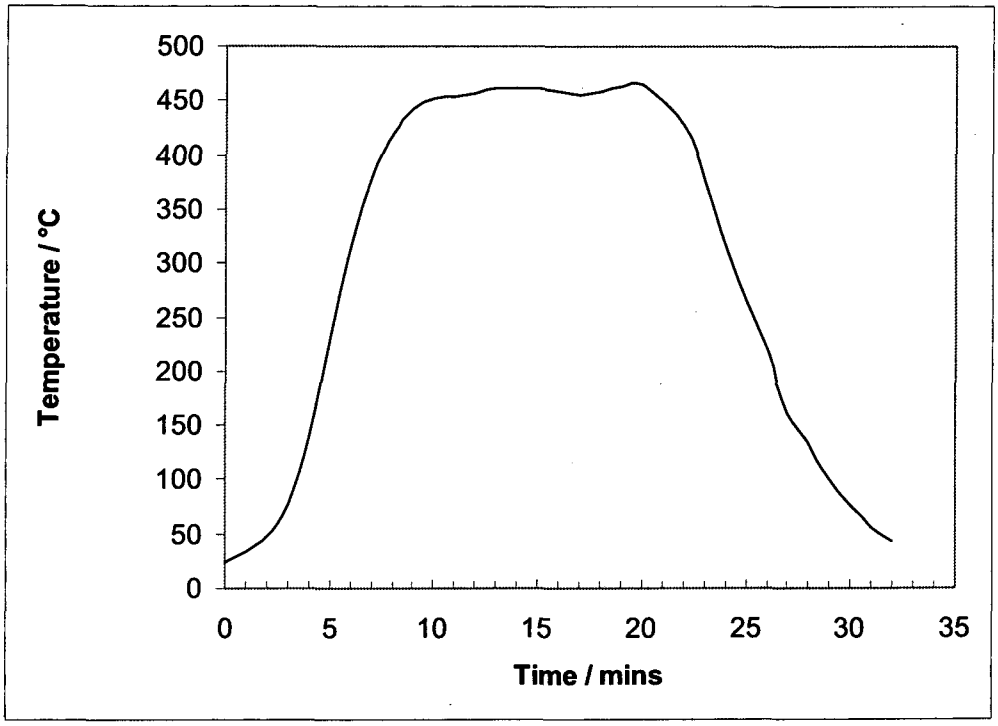


Figure 7: Temperature profile of the BTU 6 chamber furnace used for sintering of the TiO_2 film.

2.2.5 Dye sensitisation

The dye sensitisation of the mesoporous TiO_2 films used a commercial ruthenium-based dye, Ru 535, obtained from Solaronix SA. The Ru 535 dye, also know as N3 dye in the literature, is a wide band gap semiconductor sensitiser which is effective up to 750 nm. The molecular formula of the dye is $C_{26}H_{20}O_{10}N_6S_2Ru$ and its chemical structure is shown in Figure 8.

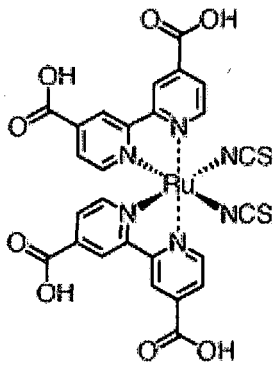


Figure 8: The chemical structure of Ru535 dye (from Solaronix SA).

The dye solution was made from 20mg of Ru535 dye in the powder form dissolved in 100 ml of pure ethanol. The photoelectrodes were stained in this solution at room temperature for at least 12 hours, typically overnight, before being assembled into a cell. The absorbance response of the Ru 535 dye solution was analysed using the Perkin Elmer Lambda25 UV/VIS spectrometer and is shown in Figure 9, this absorbance characteristic is in close agreement to that published in [2.5].

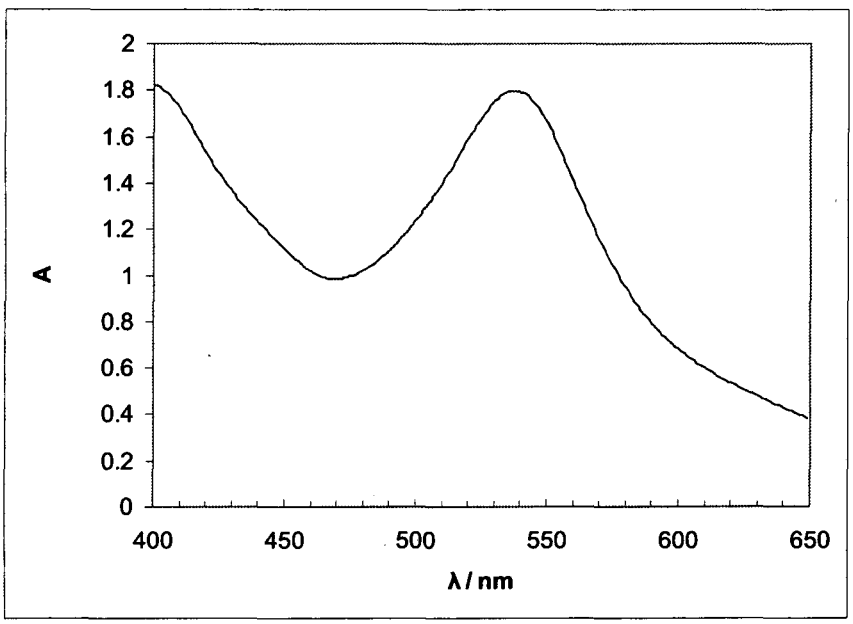


Figure 9: Absorbance plot of the Solaronix Ru 535 dye solution showing absorbance A versus wavelength λ.

The Absorbance is defined as the logarithm of the ratio of incident to transmitted power through a sample.

2.3 Preparation of the counter electrode

The TCO substrate used for the counter electrode was predrilled with two 1mm diameter holes to enable the introduction of the electrolyte after the cell assembly. A technique for easily and reliably drilling through glass was developed using diamond coated drill bits (available from Eternal Tools). Using a small Minicraft electric drill operating at 18,000 rpm with a 1mm diameter diamond drill bit and with water as a coolant, it is possible to reliably drill through the 1.1 mm thick TCO glass substrates used to construct the counter electrode.

A rectangular screen design of 35 mm x 40 mm corresponding to the active area of the cell was used to deposit the platinum catalyst. A mesh size of 90 threads/cm and wire diameter of 48 μm was used which translates to an open area within the mesh of 25%.

A commercial paste was used for depositing the platinum catalyst (Solaronix Pt-Catalyst T/SP), this contains a chemical platinum precursor and is specifically designed for reducing the overpotentials of the iodide / triiodide redox couple. After screen printing, a wet film of around 2 μm was measured. This is at the limits of the Z-Check 500 microscope which has a previously estimated accuracy of approximately ±2 μm. After firing in the BTU six chamber belt furnace at 400 °C for 30 minutes, a transparent, activated platinum layer was obtained.

2.4 The iodide / triiodide electrolyte

Electrolytes based on the iodide / triiodide redox couple were exclusively used for this work with laboratory prepared and commercial electrolytes being used.

An electrolyte solution was prepared using 20 ml ethylene glycol (Aldrich 293237), 0.25 g anhydrous iodine (Aldrich 451045) and 1.66 g anhydrous potassium iodide (Aldrich 429422). This solution contains concentrations of 0.5M KI and 50mM I_2.

The following commercial electrolytes were obtained from Solaronix SA:

Iodolyte TG-50: An iodide based high boiling point electrolyte with 50 mM of tri-iodide in tetraglyme (tetraethylene glycol dimethyl ether).

Iodolyte PN-50: An iodide based low viscosity electrolyte with 50 mM of tri-iodide in propionitrile.

Iodolyte R-150: An iodide based low viscosity electrolyte with 150 mM of tri-iodide in 3-methoxypropionitrile.

During this research, cells made from the same production batch have been filled with different electrolytes without a discernable difference in the laboratory performance. The performance of the electrolyte is of secondary importance for this research providing that its contribution to the series resistance of the cell is much less than that of the electrodes.

2.5 Cell assembly

The cell assembly can be seen from the exploded view of the cell shown in Figure 4. A rectangular shaped gasket of external size 50 mm x 45 mm and with a width of 5 mm was cut from a sheet of thermoplast material (Surlyn 1702 or Solaronix SX1170-60). This gasket fitted between the side of the substrate and the edge ot the active area of the photoelectrode and had a thickness of either 50 μm (1702) or 60 μm (SX1170-60). The separation between the active areas of the electrodes was set by the gasket thickness less the thickness of the deposited TiO_2 and Pt layers on the electrodes and was typically around 30 μm. The cavity defined by this separation and the area enclosed by the gasket was filled with electrolyte.

The cell was assembled at the completion of the staining process for the photoelectrode. Upon removal from the dye solution, the photoelectrode was dried at 70 °C for 10 minutes and the gasket was placed on the electrode and aligned to the active area. The counter electrode was then placed on the top side of the gasket and the assembly was then placed between two aluminium heat spreader plates of 3 mm thickness which were held together by spring clips. The assembly was then heated to 120 °C for 20 minutes which provided good sealing of the thermoplast gasket to the

TCO substrate on the two electrodes. In a production process, a hot press would be used for this operation.

After assembly, the cell was checked for shorts. At this stage before the introduction of the electrolyte, the cell should have high electrical resistance and a threshold of 1 MΩ was set, below which the cell was rejected. These shorts were usually caused by very localised bridging between the electrodes which could normally be cleared by fusing this local short. A technique was developed using a power supply with an output of 2 V and current limit of 1 A which was connected across the cell. This usually fused these faults and restored the cell impedance to above the 1 MΩ threshold. Occasionally the location of the short could be observed as a dark pinhole on the surface of the electrode where the fusing had occurred.

The electrolyte was introduced into the cell by means of the two holes in the counter electrode which were drilled at opposite corners of the electrolyte cavity. If the electrolyte reservoir is placed at one corner, then with careful application the whole cell can be filled with electrolyte. This occurs, without resorting to vacuum methods, under capillary action with the second hole providing an exit for the displaced air. After filling, the two holes are sealed and this was normally performed using a tape to allow subsequent access, a more permanent arrangement used an epoxy based sealant.

Another technique, originating from the Grätzel group at EPFL, Lausanne and shown in Figure 10, has been used and has the advantage of requiring only a single hole in the counter electrode. During filling of the iodine / triiodide electrolyte, a reservoir of electrolyte is held over the hole in the counterelectrode. The assembly is then enclosed and evacuated using a glass funnel which is sealed at its rim by a rubber gasket and is connected to a vacuum pump. During evacuation, air can be seen to be drawn out of the cell though the electrolyte, where it appears as bubbles in the electrolyte reservoir. If the vacuum is now released gradually, electrolyte is drawn into the cell from the electrolyte reservoir and fills the electrolyte cavity. This method does require careful attention in its experimental implementation to ensure that the evacuation can be safely performed and with the design of the electrolyte reservoir. Although this technique was tested, the large majority of electrolyte filling was performed with the previous described method.

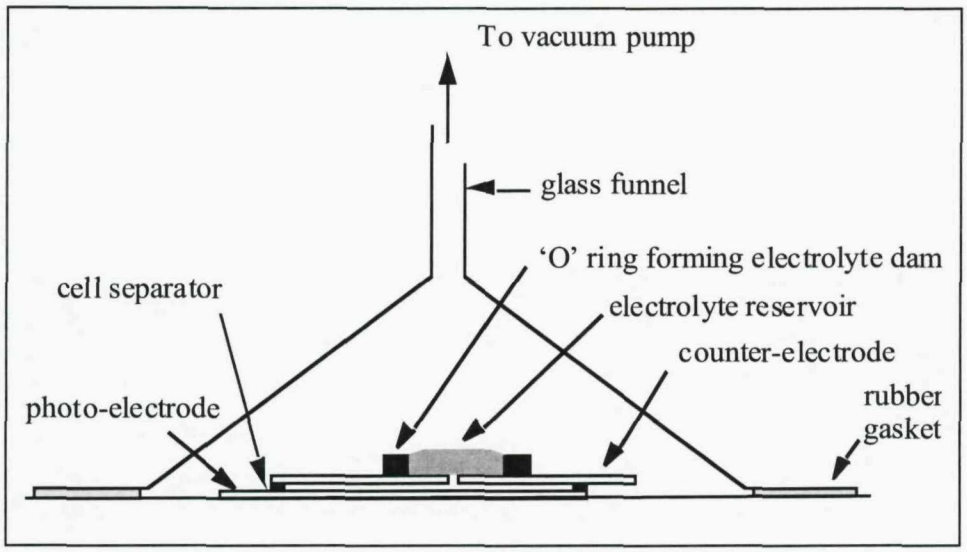


Figure 10: The Grätzel group method of electrolyte insertion into the DSSC using a single hole.

After sealing of the cell, a contact strip was added to the edge of each electrode. These were cut from a tin clad copper foil of 35 μm thickness (Advance AT544) which contains a conductive, acrylic adhesive for attachment to the TCO substrate. The foil is wrapped around the edge of the electrode allowing an electrical connection to be conveniently attached from both sides. After the construction of the DSSC, the open circuit voltage, Voc, and short circuit current, Isc, of the cell were measured to check the photovoltaic operation. This was normally performed with the cell being illuminated by a 20 W xenon lamp from a distance of 20 mm.

CHAPTER 3: EVALUATION OF THE DYE SENSITISED SOLAR CELL CONSTRUCTION AND PERFORMANCE

3.1 Measuring TiO_2 film quality

During the screen printing process, the deposited TiO_2 film was checked visually for coverage and general deposition quality. This information was used during the setup procedure of the screen printer when the adjustments described in 2.2.3 were being made. After the wet film had been deposited, the film thickness was checked to the limits of the Z-Check 500 microscope as detailed in 2.2.3. After the sintering step, the forming of the mesoporous TiO_2 film was complete. The quality of this film was analysed using profilometry and SEM techniques to check the structure and thickness of the TiO_2 film.

3.1.1 Profilometry

A Veeco optical profilometer was used in the vertical scanning interferometry mode to analyse the surface quality of the TiO_2 film. In this mode, the instrument scans the sample in the vertical direction and for each level that is in focus, an intensity maximum occurs. A three dimensional image of the sample can then be formed from the intensity maximum versus vertical height information as the surface of the film is scanned.

The surface profile of a TiO_2 electrode measured in this way is shown in Figure 11, the effect on the surface relief of the screen mesh can clearly be seen. Large scale defects in the TiO_2 film can also be observed and these are mainly due to air bubbles formed in the wet deposited film during deposition. These defects are not a serious impediment to the operation of the electrode in the cell since the nanostructure of the electrode is not greatly affected by macro defects of this type. Defects which cause a raising of the film height, such a large conglomerate of TiO_2 particles or other contaminants, can cause a problem by acting as centres for local shorts between the electrodes when the call is assembled. However with proper paste preparation and

deposition, it was found that films of relatively uniform thickness could be produced with few defects of this type.

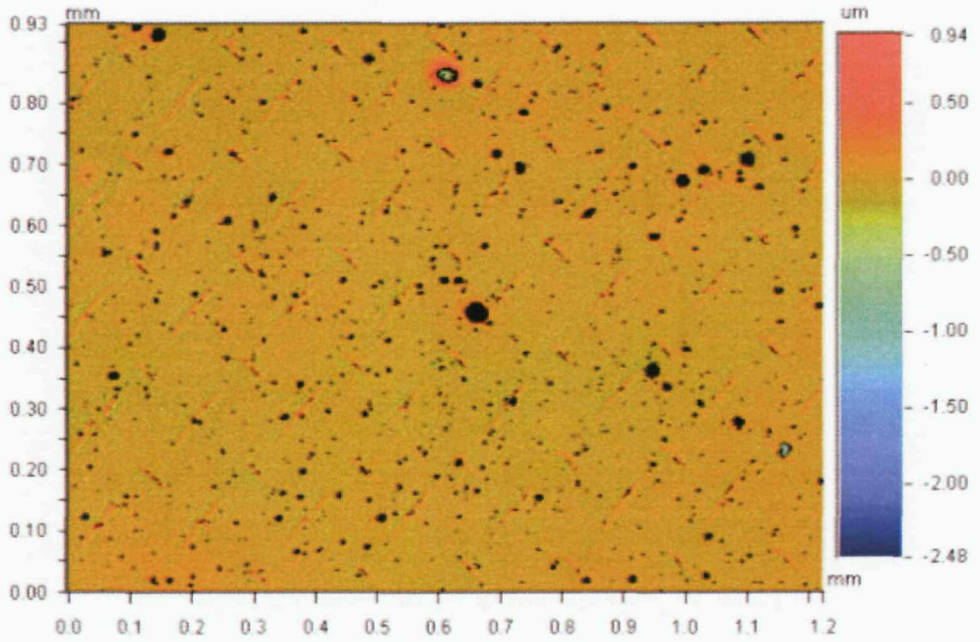


Figure 11: The surface profile of a TiO_2 film prepared using the Solaronix Ti-Nanoxide T/SP paste and a 43 thread/cm screen as measured using the Veeco optical profilometer in VSI mode.

The measurement of film thickness with an optical profilometer requires the deposition of a layer with uniform optical properties across the step height if the material at either side is dissimilar. A profilometer which uses a mechanical stylus to measure height does not have this restriction and is clearly better suited for measuring the TiO_2 film thickness on the TCO substrate. The Tencor Alpha-Step surface profilometer uses a diamond tipped stylus in direct contact with the surface and is capable of a measurement resolution of ±5 nm in the micron measurement mode. Although the mechanical stylus contacts the film and causes a slight scratch as it scans across the area being measured, the damage is negligible for the relatively large area electrode being measured. In Figure 12, the profile of a deposited film has been measured at its edge and the film thickness can be seen to be 20 µm. Local variations in thickness due to the effects of the screen mesh can also be observed. Although the deposited wet film is left to self-level before the sintering stage, local variations in film thickness are still present. As with the local defects present in the

film, these imperfections are a feature of the thick film process but do not significantly affect the electrode performance.

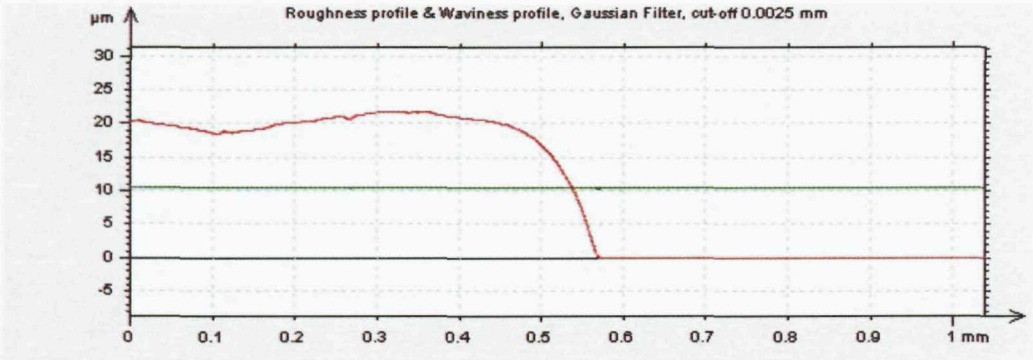


Figure 12: The TiO_2 film profile (red trace) at its edge with the TCO substrate measured for a film prepared using Paste 2 and a 43 thread/cm screen.

3.1.2 SEM analysis

The nanostructure form of the TiO_2 film was examined using scanning electron microscopy (SEM) techniques. The SEM was also used to examine the texture of the deposited film at relatively low levels of magnification to assess the deposition quality. The image of Figure 13 shows some imperfections on the TiO_2 film, such as voids and the deposition of large particles of material.

At higher levels of magnification, the nanostructure form of the film can be observed and best results were obtained with the JSM 5910 SEM. A SEM image of a commercially available nc-TiO_2 electrode surface is shown in Figure 14. This electrode was obtained from STI, Australia and the mesoporous structure can clearly be seen with a particle size of around 50 nm diameter. These images were compared to those provided in the literature, with [1.12] providing a particularly good reference, to assess the quality of deposition.

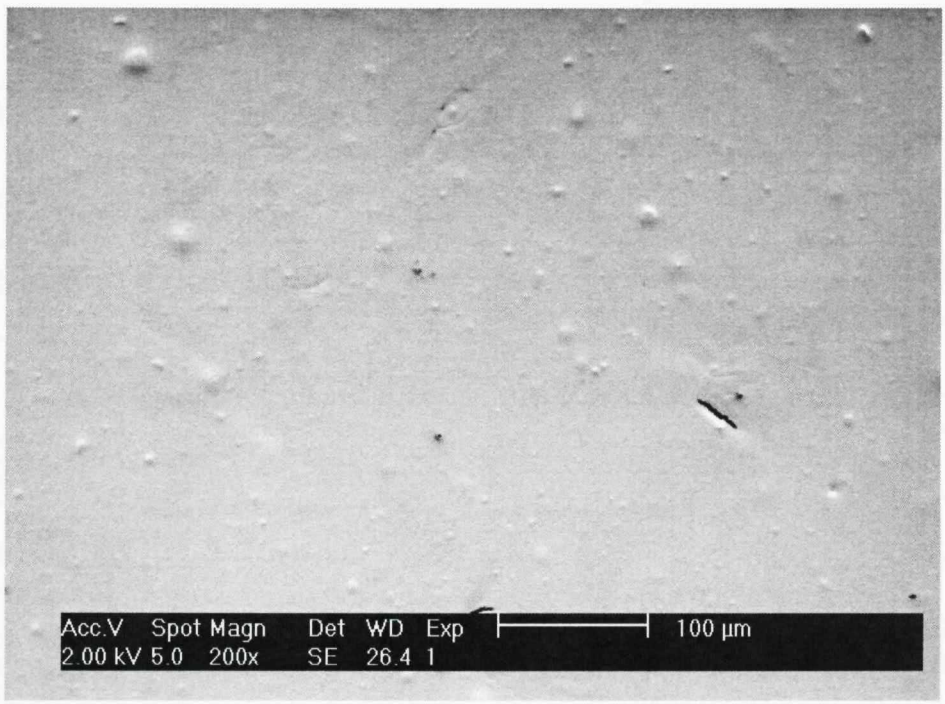


Figure 13: The TiO_2 film quality across a section of the electrode surface imaged using a Philips XL30 SEM, the film was prepared using the Solaronix Ti-Nanoxide T/SP paste and a 43 thread/cm screen.

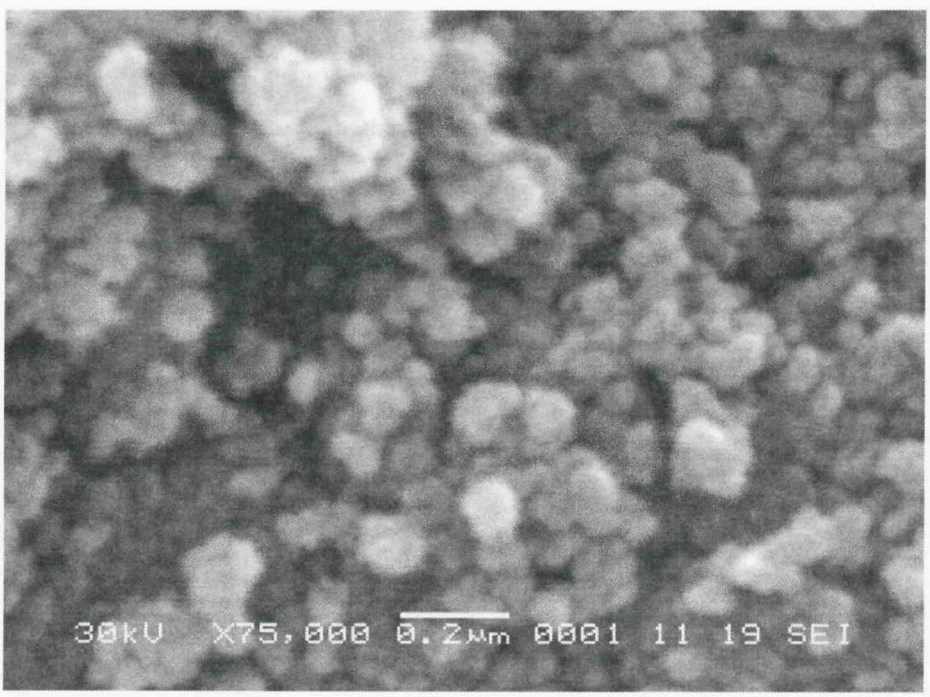


Figure 14: SEM image of the STI nc-TiO_2 electrode surface.

3.2 Output characterisation

Photovoltaic cells are typically evaluated using an industry standard test condition of 1000 W/m^2 irradiance level with a spectrum of AM 1.5 and at a temperature of 25 °C. The AM1.5 specification refers to an air mass of 1.5 (solar zenith angle 48.19°) which is a measure of the atmospheric path for the radiation [1.4] and is given by:

$$m = \frac{1}{\cos\alpha}$$

where α is the zenith angle.

In Figure 15, the energy distribution is plotted against wavelength for the AM1.5 specification.

An I-V (current vs voltage) characterisation is a standard test under this level of illumination where the current is measured as the voltage is swept from zero, where the current is the short circuit value Isc, to the open circuit value Voc where the current is zero. The I-V characteristic of a Centronic OSD100-6 silicon cell, which was used as a reference device, under standard illumination conditions is shown in Figure 16. It can be seen from the form of the I-V characteristic, which is similar for DSSC devices, that there is a maximum power point on the characteristic. Plotting the power against output voltage, which is also shown in Figure 16, shows the maximum power point and the corresponding current, Impp, and voltage, Vmpp, at this operating point.

The operating point corresponding to the maximum power point can be plotted on the I-V characteristic. A figure of merit for photovoltaic devices is the 'fill factor' which is defined as:

$$FF = \frac{Vmpp \cdot Impp}{Voc \cdot Isc}$$

An ideal cell would have a short circuit current which remained constant up to the open circuit voltage and therefore a maximum power which is the product of these

two terms. The fill factor essentially measures how close a cell 'fills' this ideal characteristic.

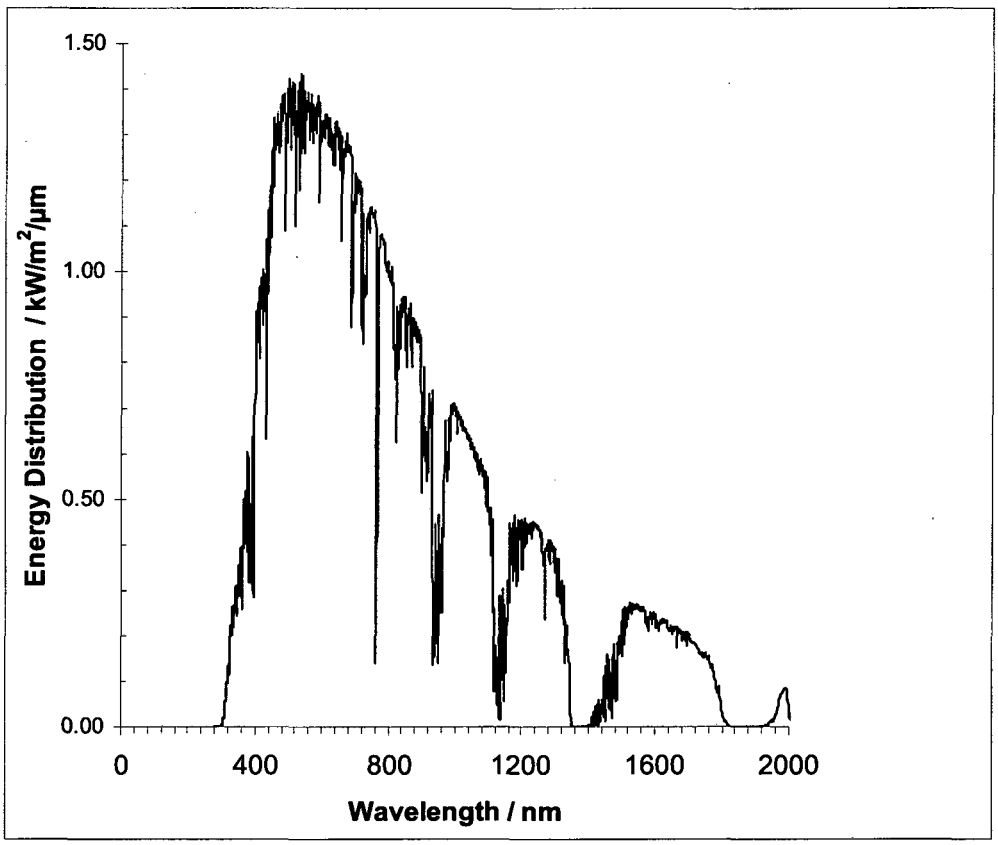


Figure 15: Spectral energy distribution for the AM1.5 standard.

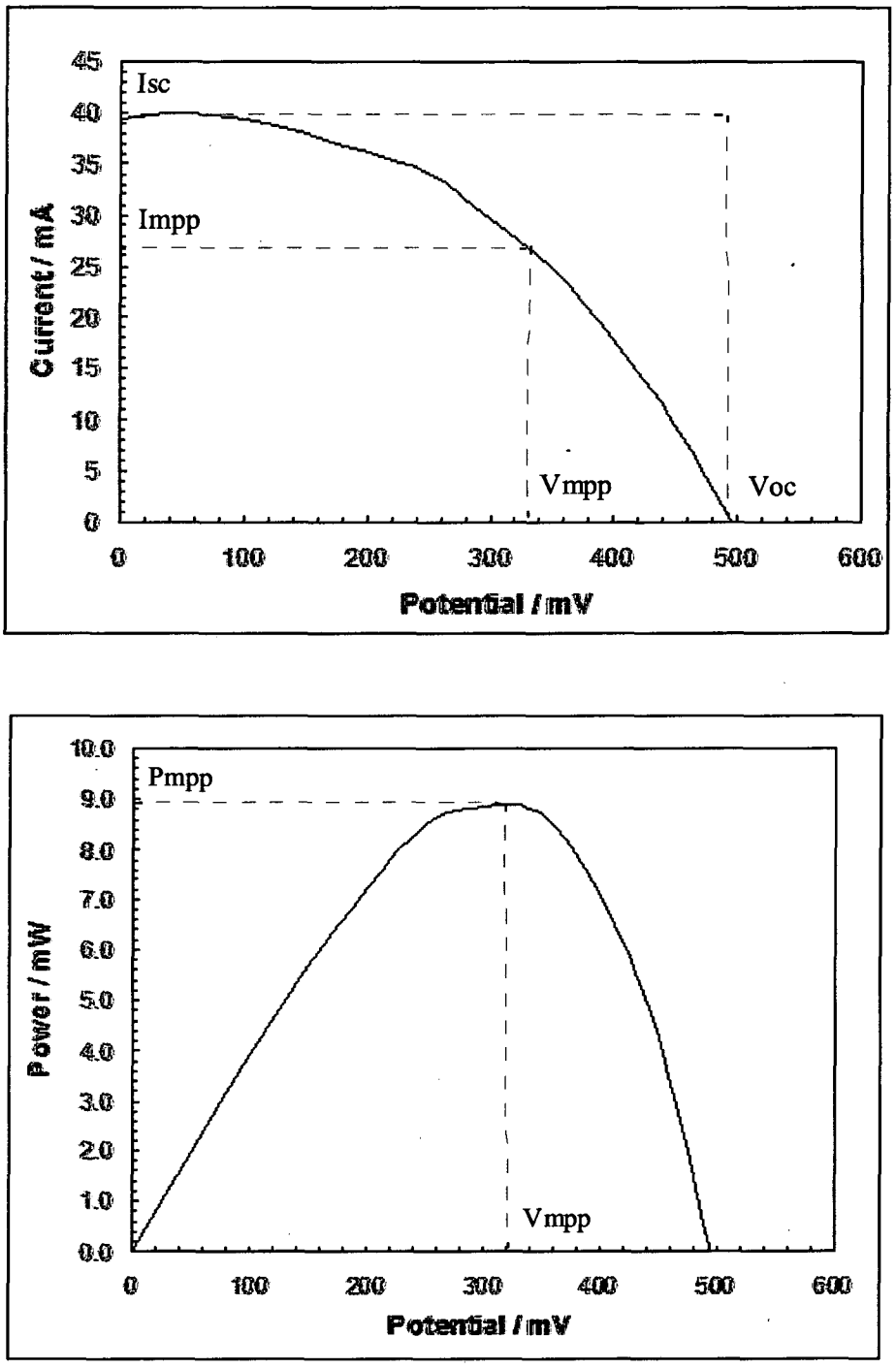


Figure 16: Current vs Voltage and Power vs Voltage for the Centronic OSD100-6 silicon reference cell under standard illumination conditions.

The OSD100-6 is a monocrystalline silicon cell with an active area of 1 cm^2.

3.2.1 Xenon lamp measurement system

This system uses a xenon arc lamp filtered through selected air mass filters to simulate the spectral distribution of the sun. The School of Engineering Sciences has a xenon lamp based photovoltaic measurement system which is capable of measuring the I-V characteristic of a photovoltaic device under standard illumination conditions. The system is calibrated with a monocrystalline silicon cell which has been characterised by the NREL under standard test conditions, more information is provided in Appendix 1. This system was used for testing some of the DSSC devices produced during this research.

3.2.2 LED based solar simulator

A LED based solar simulator was constructed to provide a more convenient reference light source for measurement of the DSSC devices within the laboratory environment. This simulator comprises of 200 LEDs arranged in a five pixel pattern with separate LEDs of wavelength 470 nm, 525 nm, 645 nm, 880 nm and 950 nm. Each bank of 40 LEDs operating at the same wavelength could be individually selected; thereby enabling cells to be tested at individual or multiple wavelengths. The LED array was designed into an enclosure of 55 mm square which could be conveniently fitted over the cell under test with the LEDs approximately 45 mm from the top surface of the cell. The LED solar simulator is described in more detail in Appendix 1 and has provided a convenient means of testing the DSSC devices in the laboratory and for making relative measurements between cells.

3.3 Voltammetry and impedance measurements

The Solartron SI1287 Electrochemical Interface was used in conjunction with the LED solar simulator to obtain I-V characteristics for the DSSC devices in the laboratory. The Corrware application software was used to control this measurement which could also be performed at the individual wavelengths of the simulator. The addition of the SI1250 Frequency Response Analyser and ZPlot application software allowed this setup to perform impedance measurements on the DSSC devices. In

these measurements, a four terminal connection was made onto the contact strips of the cell with WE and REF2 being connected at the contact strip with the same arrangement for CE and REF1. This arrangement could be adapted relatively easily to provide more complex impedance measurements of photovoltaic devices such as Intensity Modulated Photocurrent Spectroscopy (IMPS).

During the experimental work, many measurements of sheet resistivity were made and the four point probe method [3.1] was used for this purpose. In this arrangement, four probes, which are linearly arranged and equally spaced, contact an infinite sheet resistance with a current, I, forced through the outer probes and a voltage, V, measured across the two inner probes. It can be shown that the sheet resistance, Rs, of the material contacted by the probes is given by:

$$Rs = \frac{\pi \cdot V}{\ln 2 \cdot I}$$

A fixture was made using spring-loaded point probes, each separated by 2.54 mm, which could be used with the SI1287/SI1250 instruments to measure the impedance of a film. The measured value was corrected by the factor of $\pi/(\ln 2)$ assuming an infinite sheet and this arrangement was found to provide good results.

3.4 Modelling the impedance of the dye sensitised solar cell

A photovoltaic solar cell can be conveniently modelled in a circuit simulation tool and an elementary equivalent circuit is shown in Figure 17. Applied to the DSSC, the electrode resistance is represented by Rce for the counterelectrode and by Rpe for the photoelectrode. In this model for the DSSC, the reaction resistance for the recombination reaction within the cell is represented by Rs and the surface capacitance by Cs. The photo-generated current is represented by an ideal current source, Ipv, with a parallel diode which models the output current roll off with cell voltage.

This is a simple, but useful, equivalent circuit for the DSSC device and will be used in the interpretation of some of the experimental results. The voltage dependence of the photo-generated current has been well modelled by others [3.2]. In this case since the primary interest is in the effect of electrode resistance, a simple diode element is

used to represent the voltage dependence of the output current. The shunt current, I, taken by this element is given by the diode equation:

$$I = Io \cdot \left(\left(e^{\frac{V}{n \cdot Vt}} \right) - 1 \right)$$

where Io is the reverse saturation current (1E-14 A) and n is the emission coefficient (1), Vt is the thermal voltage given by:

$$Vt = \frac{k \cdot T}{q}$$

where k is the Boltzmann constant, q is the electron charge and T is the temperature (300 K).

The modelling of the photoelectrode is complex and covered in the literature [3.2], the electronic path includes both the path through the TCO substrate and the more complicated path through the TiO_2 mesoporous structure. The latter path is more accurately modelled with a transmission line equivalent circuit and this could be added to this model. However the intended application of this model is to demonstrate the effect of improvements in the resistive path through the TCO substrate and onto the TiO_2 layer and so accurate modelling of the latter is not necessary at this stage. The representation of the electrochemical processes occurring within the cell by Rs and Cs are simple but are considered to be realistic by other workers [3.3] and are again sufficient for the purposes of the model.

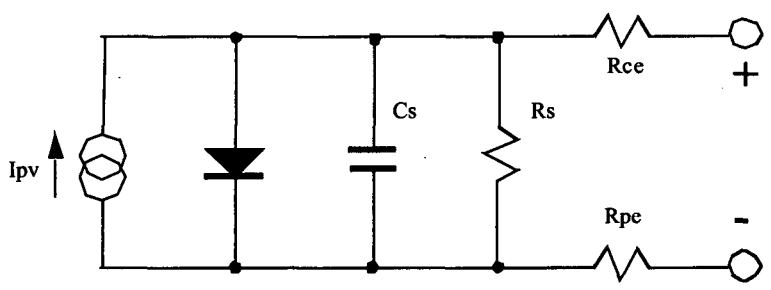


Figure 17: An equivalent circuit of a photovoltaic cell applied to the DSSC.

This model was used in the Spectre[1] circuit simulator with the photo-generated current set at 6 mA and resistances of 1 Ω for both electrodes, the corresponding I-V characteristic is shown in Figure 18.

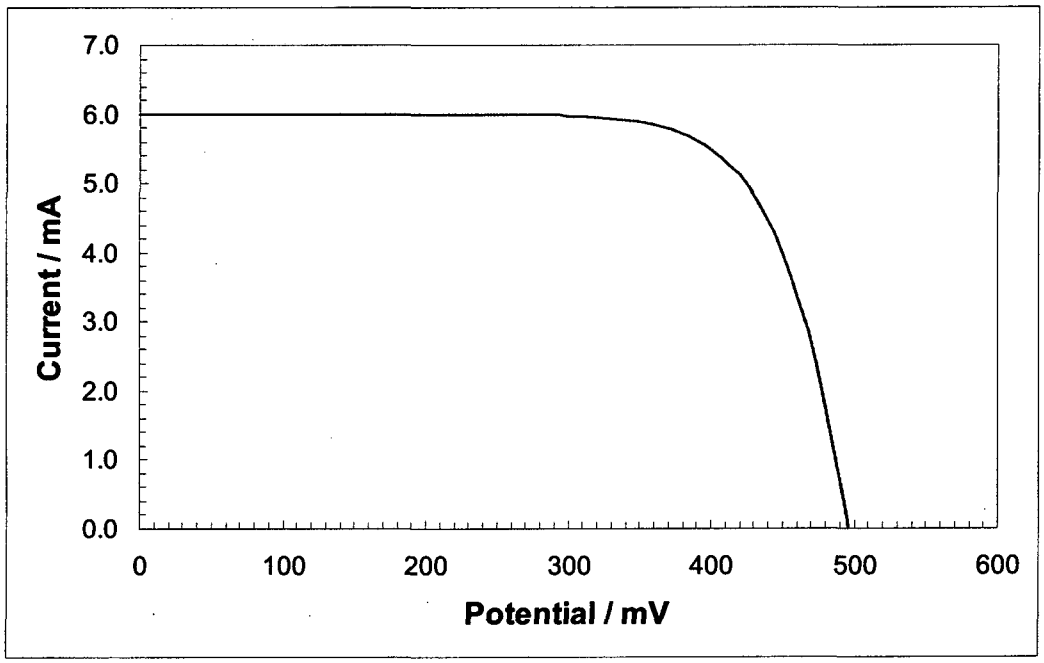


Figure 18: The I-V output characteristic of the DSSC simulation model. In this simulation Ipv=6 mA, Cs=0.25 mF, Rs=1 MΩ, Rce=1 Ω, Rpe=1 Ω and n=1

This model provides a starting point for analysing DSSC performance and can be extended to more accurately model the electron path within the TiO_2 layer itself and other processes within the DSSC device.

[1] Spectre is a product of Cadence Design Systems

CHAPTER 4: ELECTRODE RESISTANCE AND DYE SENSITISED SOLAR CELL PERFORMANCE

4.1 Preparation of the DSSC

The laboratory DSSC devices were produced using the thick film techniques previously described. The production of the TiO_2 mesoporous film for the photoelectrode presents the main challenge in producing an efficient device. This process step was initially developed using a commercial TiO_2 paste, produced for this application, and then with laboratory prepared TiO_2 pastes. The platinum catalyst coated counterelectrode was always prepared using the method described in 2.3; which has the advantage of using a very similar production methodology to that of the photoelectrode. The subsequent cell assembly and electrolyte insertion processes were developed and improved during the research.

4.1.1 Processing the mesoporous TiO_2 photoelectrode

Initial photoelectrode preparation used the Solaronix Ti-Nanoxide T/SP paste and 43 thread/cm screen. After the sintering step, a film of 20 μm thickness could be consistently obtained which was relatively uniform, estimated at ±3 μm, across the 14cm^2 cell area. A SEM image of this deposited film is shown in Figure 19 and this can be compared to that of the commercial electrode obtained from STI in Figure 14. It can be seen that the particle size is slightly smaller at around 30 nm diameter. This is consistent with the Solaronix data [4.1] for this paste which gives an average diameter of 10 to 30 nm depending on the preparation method.

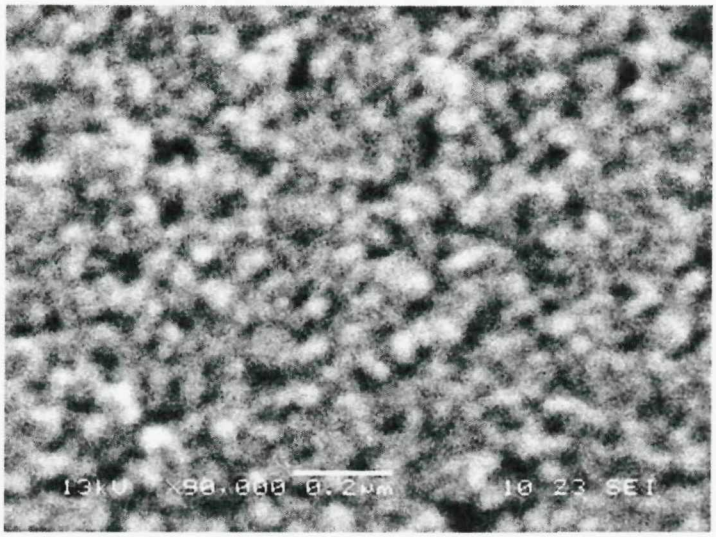


Figure 19: A SEM image of a nc-TiO_2 electrode surface deposited using the Solaronix Ti-Nanoxide T/SP paste.

Photoelectrodes were also constructed using Paste 2 from 2.2.1 and initial results indicated that the paste did not pass through the screen well due to its thick consistency and rheology. Working the paste through the screen was found to improve its properties and the paste was subsequently processed for 40 minutes in a ball mill which significantly improved its screen printing properties. A SEM image of this deposited film is shown in Figure 20 and some of the smaller particles are estimated to be around 35 nm in diameter.

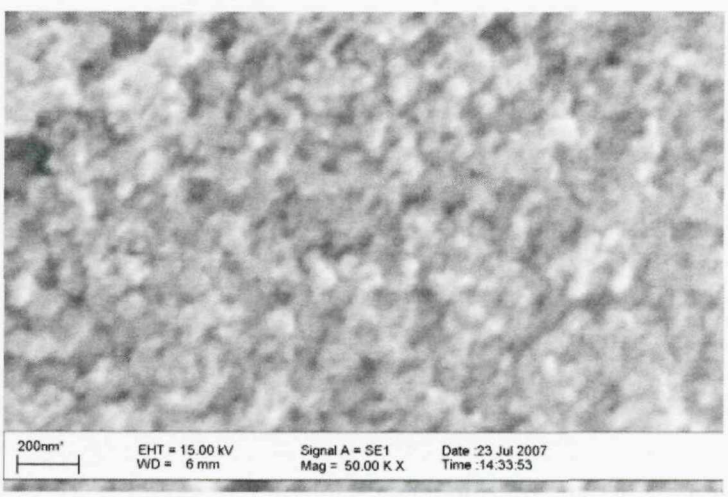


Figure 20: SEM image of a nc-TiO_2 electrode surface deposited using a ball milled version of Paste 2.

Further development of the TiO_2 paste was centred on improving its screen printing properties and these pastes continued to be based on the DeGussa Aeroxide TiO_2 P25 nanopowder.

4.1.2 The TCO Substrate

The TCO material principally used in this research was indium tin oxide (ITO). The Diamox ITO material obtained from Diamond Coatings is deposited on standard annealed glass (BS EN572) of 1.1 mm thickness using magnetron sputtering and has a sheet resistivity of 20 Ω/sq. The Visiontek ITO material is deposited on soda lime float glass of 1.1mm thickness and has a sheet resistivity of 12 Ω/sq. The soda lime float glass is coated with a primary layer of silicon dioxide (SiO_2) and then with a secondary layer of ITO.

The impedance of the ITO substrate material was checked using the impedance analyser and four point probe method. The impedance was found to be predominantly resistive up to the maximum test frequency of 65 kHz and was within the sheet resistivity specification for both sources of ITO material.

4.2 Initial cell performance

The performance of an early DSSC device built using the Solaronix paste is shown in Figure 21 and this non-ideal performance, compared to Figure 18, shows that the output resistance of the cell is high. This resistance is limiting the output current as the terminal voltage of the cell is increased. During the early development of the process, the photogenerated current increased as the photoelectrode TiO_2 film structure improved. However, although the same levels of short circuit current could be developed with the newer cells at lower levels of illumination, the values at higher levels of illumination did not significantly increase. This resistive output characteristic remained and was clearly limiting the device performance.

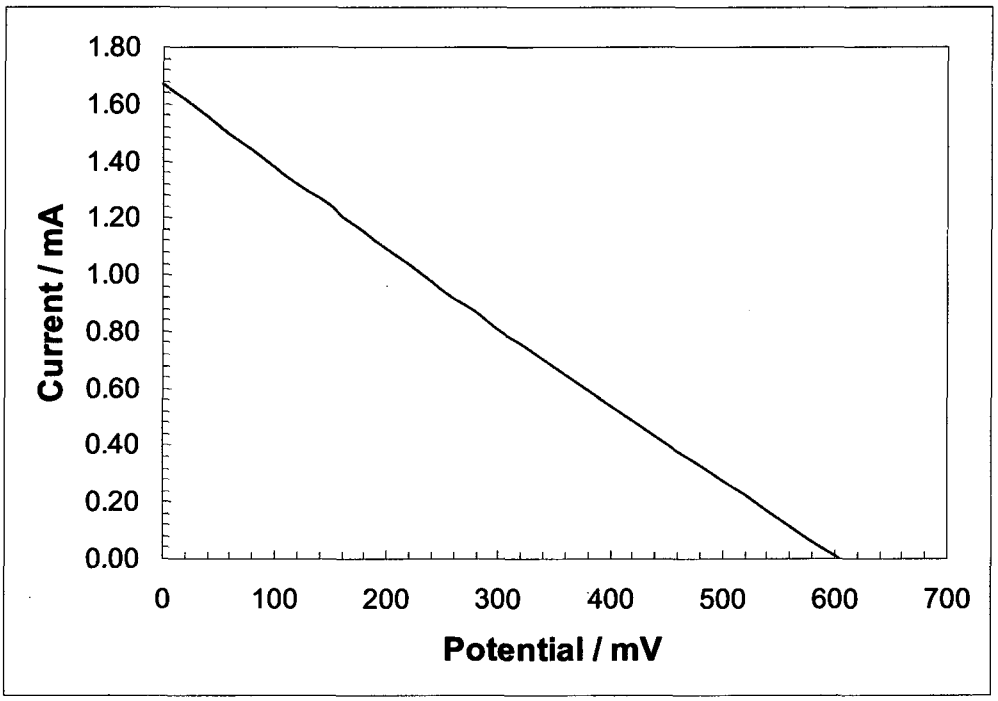


Figure 21: I-V Characteristic under illumination for DSSC cell 1_2305-1 (made with Paste 1 and a cell area of 14cm^2) with the xenon light source at 1000 W/m^2.

The output impedance of a typical cell was measured against frequency and the impedance plot is shown in Figure 22 for low ambient light and illumination conditions. This plot shows that at high frequency, the impedance of the cell reduces to a real impedance of around 100 Ω. Assuming an open circuit voltage of 0.5 V for the cell, then an output resistance of 100 Ω will limit the short circuit current to 5 mA. Clearly this level of output resistance is a serious impediment to the output power of the DSSC device. It would need to be reduced before any performance improvements in photogeneration capacity at the photoelectrode could be realised in an increased output power for the DSSC.

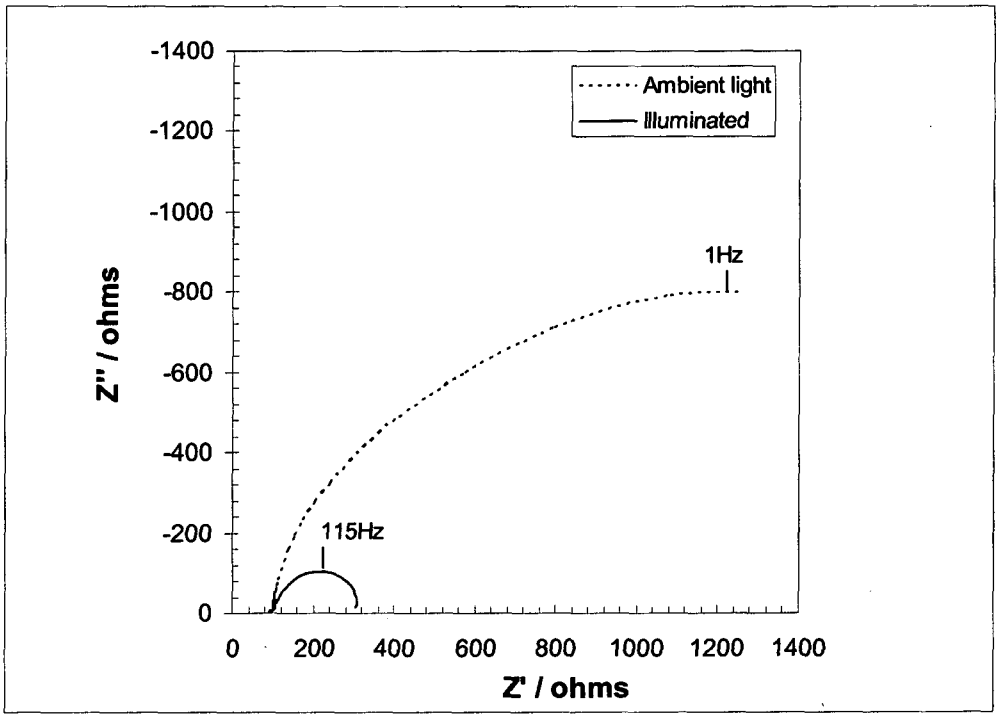


Figure 22: Impedance measurements under low ambient light conditions and illumination (from a 20 W xenon lamp at 5 cm) for DSSC cell 2_1105 (cell area of 14cm^2).

Z' is real and Z'' is imaginary component measured in ohms over the frequency range 1 Hz to 65 kHz.

4.3 Performance at different wavelengths

The LED solar simulator allows the performance of the DSSC to be checked at different wavelengths and the results for a cell made from Paste 4 are shown in Figure 23. It can be seen that the majority of the cell's output is obtained at 525 nm which corresponds to a peak in absorbance of the Solaronix Ru535 dye used to sensitise the cell as shown in Figure 9. At either side of the absorbance peak of the Ru535 dye at 535 nm, the cell output is reduced as shown by the curves for 470 nm and 645 nm with the lowest output obtained at 645 nm. The cell provided negligible outputs at the other wavelengths of 880 nm and 950 nm provided by the LED simulator.

This characteristic also shows the increasing importance of the cell's output resistance as the output current increases with the corresponding reduction in fill factor for the output characteristic. At the relatively low output current obtained with 645 nm, the I-V characteristic can be seen to have a discernable 'plateau' region, where the output current is relatively constant with increasing the cell voltage, before the current starts to fall off more rapidly. As the output current increases, at the more sensitive wavelengths, the output characteristic is dominated by the output resistance of the cell and becomes more linear.

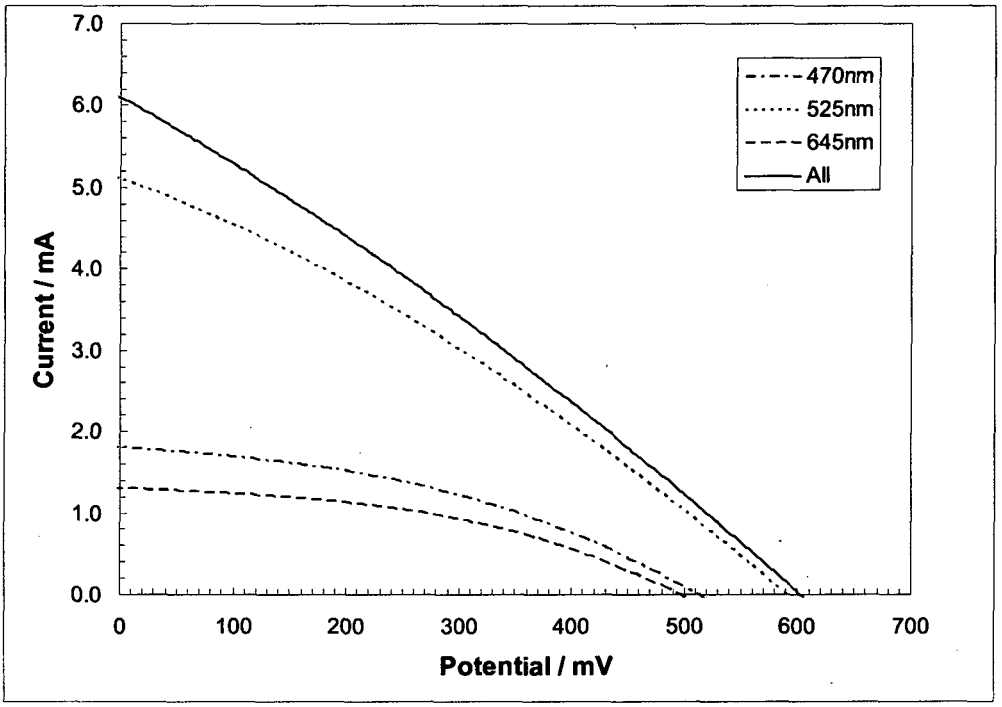


Figure 23: I-V Characteristic under LED illumination for DSSC cell 1_1610 (cell area of 14cm^2) at individual wavelengths and at all wavelengths available (470 nm, 525 nm, 645 nm, 880 nm and 950 nm).

The impedance of this cell was also measured under these conditions and the results are shown in Figure 24. The output resistance can be seen to be around 70 Ω which suggests that the output current will be limited to 7.1 mA with an open circuit voltage of 0.5 V before accounting for other effects within the cell.

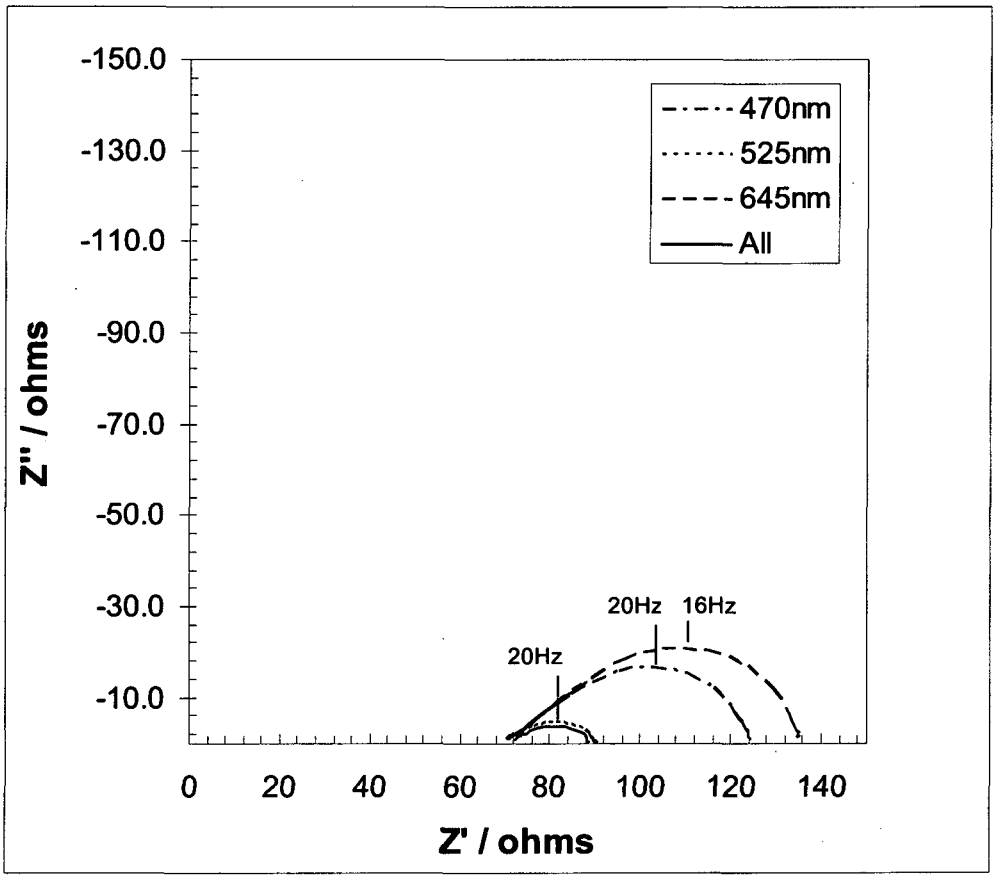


Figure 24: Impedance plot under LED illumination for DSSC cell 1_1610 (cell area of 14cm^2) at individual wavelengths and at all wavelengths (470 nm, 525 nm, 645 nm, 880 nm and 950 nm) over the frequency range 1 Hz to 65 kHz.

4.4 Simulating the effect of electrode resistance on cell performance

The degradation in the output characteristic of a DSSC device with increasing electrode resistance can be modelled with a circuit simulator using the equivalent circuit described in 3.4. The I-V characteristic of the cell can be simulated with a fixed photogeneration current, Ipv, and the value of the electrode resistances, Rce and Rpe, increased. The results are shown in Figure 25 for the case of Ipv=6 mA.

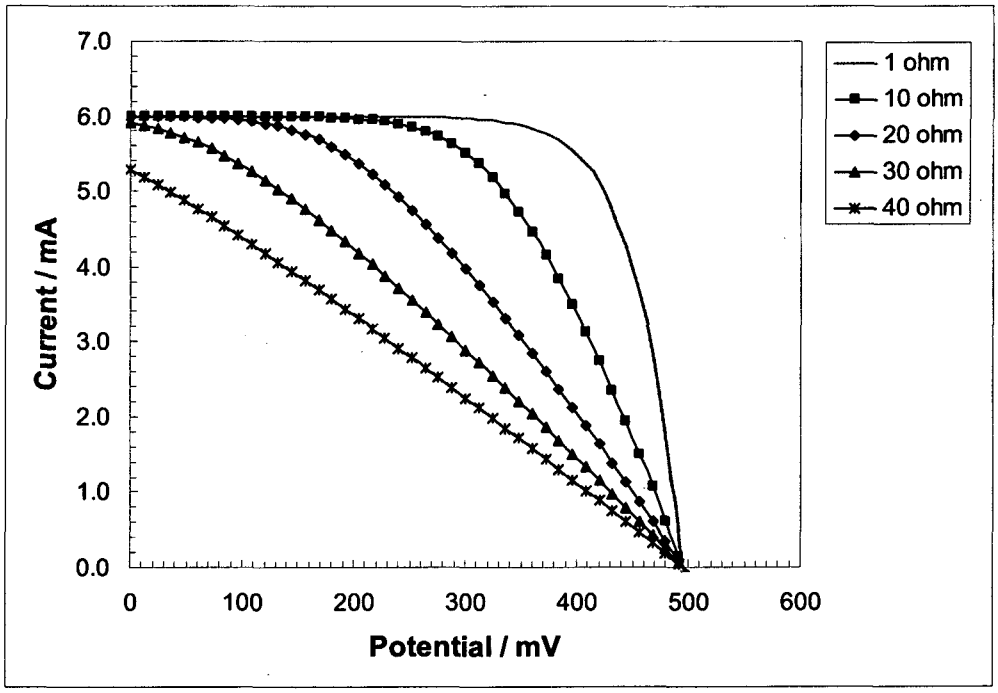


Figure 25: The effect of increasing electrode resistance on the I-V output characteristic of the DSSC simulation model.

This simulation demonstrates how increasing electrode resistance can degrade the fill factor of the cell, thereby reducing the maximum power that can be delivered by the device. As the electrode resistance is increased further, the short circuit current, Isc, also reduces.

The impedance of the cell can also be modelled at an operating point similar to that shown with a real device in Figure 24. After setting the electrode resistance of both the counterelectrode and photoelectrode at 30 Ω, the resulting impedance plot is shown in Figure 26. This model is greatly simplified and does not model the effect of the mesoporous TiO2 structure on the electrode resistance. However, it does show the effect of an increased electrode resistance and can be compared to that measured from a DSSC device in Figure 24.

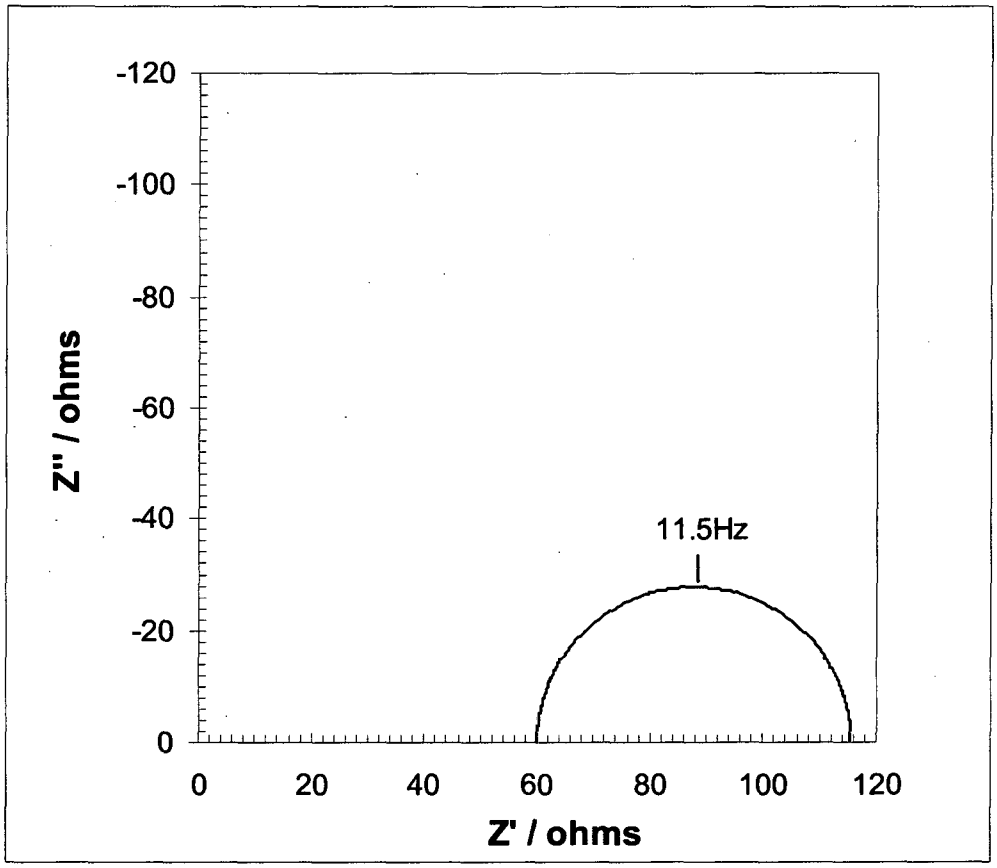


Figure 26: Impedance plot obtained from the DSSC simulation model at a cell voltage of 455 mV with Ipv=4 mA, Rpe=30 ohms, Rce=30 ohms Cs=0.25 mF, Rs=1 MΩ and n=1 over a simulation frequency range of 1 Hz to 65 kHz.

4.5 The TCO substrate and high temperature processing

The contribution of the TCO substrate to the electrode resistance is clearly an issue for the scaling up of the DSSC area. However another problem which was realised from the previous data is that the resistivity of the TCO material is also increasing as a result of the high temperature processing which is required for both the counterelectrode and photoelectrode. The electrodes are subjected to temperatures of 400 °C to 450 °C for the activation of the platinum catalyst on the counterelectrode and sintering of the TiO_2 nanoparticles on the photoelectrode. During these heat treatment processes, it was found that the sheet resistivity of the ITO material was increasing significantly. Analysing the sheet resistivity of the TCO material within the contact area of processed electrodes showed that sheet resistances could exceed 100 Ω/sq for material which started at 20 Ω/sq.

An experiment was performed with the Diamond Coatings ITO material to examine these resisitivity changes. The four probe measurement method gave an initial sheet resistivity of 19.5 Ω/sq compared to the specification maximum of 20 Ω/sq. After heating two samples in air at 450 °C for 40 mins, the measured resistivities were 43.3 Ω/sq and 58.2 Ω/sq. An experiment was also performed where two samples of the same material were heated in an argon atmosphere at 450 °C for 10 mins which resulted in measured sheet resistivities of 48.1 Ω/sq and 66.8 Ω/sq. In another experiment, the material was heated to 400 °C in a tube furnace with a closed air atmosphere, there being no gas flow through the furnace, in this case the measured sheet resistivities were 25.5 Ω/sq and 26.2 Ω/sq.

Clearly ITO is an unstable material at these temperatures and the degradation cannot easily be mitigated by using an inert atmosphere for the heat treatment process. Discussions with suppliers of this material [4.2] confirmed that the degradation is caused by several effects such as changes in stoichiometry, morphology and contamination. Barrier layers, such as SiO_2, can be placed either side of the ITO to protect this layer and this is done on the glass side of the film for the Visiontek material.

Reference to this problem was subsequently found in the literature [4.3]. This stated that the resistance of ITO films can increase more than three times when exposed to temperatures of 300 °C or higher; a similar result to that observed in this research. In [4.3], the authors thought that this change was due to oxygen from the atmosphere bonding to a portion of the oxygen vacant structure within the ITO film during the heating process. This reduction in the oxygen vacancies within the film, which function as an electron supplier, would increase its resistance. Fluorine doped tin oxide (FTO) material is known to be more resistant to increases of resistivity when subjected to high temperatures and it has subsequently been noticed that other research groups developing DSSC devices tend to use FTO substrates. Further work is clearly required in this area to reduce the degradation of the TCO layers during these high temperature processing steps. Possible techniques include the use of barrier layers and optimising the duration and temperature of these steps to minimise any damage to the TCO substrates.

4.6 Limitations with the DSSC performance

These results show the importance of minimising the electrode resistance to obtain the maximum output from a photovoltaic cell. The dependence of the DSSC construction on the resistivity of the TCO substrate is a serious limitation for increasing the area of such devices which can be mitigated by using an interconnect layer in conjunction with the TCO material. The problems with degradation of the TCO material further underline the importance of not relying on this layer entirely for the collection of current throughout the electrode.

The TiO_2 mesoporous structure also contributes to the resistance of the photoelectrode. The sintering process controls the coalescence of the nanoparticles of TiO_2 into this structure and thereby controls the resistance of this film. However the electron flow through this film is predominantly vertically through the cross-section of the DSSC and onto the TCO substrate rather than laterally across the film towards the cell contacts. The current collection within the cell is provided by the TCO layer with lateral current flow through this layer to the contacts of the cell. Consequently, it is the TCO layer which predominantly contributes to the increasing series resistance of the DSSC as the device is increased in area and which becomes a limiting factor to the device performance.

4.7 Improving the electrode interconnect

The thick film production process used to make the DSSC lends itself to the production of a photoelectrode with an active TiO_2 region around an integrated interconnect layer which can be designed to minimise the photoelectrode resistance. The interconnect layer could also be screen printed onto the electrode, using a suitable conductive material, with the TiO_2 film being printed around this conductive layer. Alternatively it may be more efficient to deposit the interconnect layer onto the TCO substrate by some other technique and then to print the TiO_2 region around the interconnect pattern. There are well established methods for the metallization of patterned layers onto glass and this material could be used as the starting material for the TCO deposition which would then be followed by the TiO_2 film deposition.

Although this type of electrode structure has clear advantages, the design of an efficient interconnect layer is non trivial. The published work in this area has frequently used interdigitated structures without clearly defining how the associated geometric parameters were selected. The ability to print the electrode allows more complicated structures to be considered which also compounds the complexity of the design. The following chapters show how the performance of an interconnect geometry can be analysed and optimised.

CHAPTER 5: MODELLING THE ELECTRODE RESISTANCE OF THE DSSC ELECTRODES

The design of an efficient, large area electrode with an interconnect layer for a DSSC device is a complex problem. The interconnect needs to improve current collection in the electrode without significantly reducing the photogeneration capacity of the electrode. The flexibility of the printing process used for the production of the electrodes could allow complex patterns to be implemented at low cost. Clearly, a modelling tool is necessary to explore the possible designs for the electrode structure. Eventually such a tool could also allow the optimisation of an electrode design by finding the best arrangement of the active TiO_2 regions and interconnect layer for a given electrode geometry. The following section describes the finite element analysis methods which were used to model the performance of the DSSC electrodes and to calculate the cell resistances for experimental designs.

5.1 Modelling the electrode performance with Finite Element Analysis methods

Finite element analysis is a computer-based numerical technique which can be used to solve complex problems in applications such as electromagnetics and electrochemistry. In this method, the structure is reduced to an assembly of many small elements and these individual elements can then be modelled by a relatively simple set of equations. These equations, which define the characteristics of the individual elements, can then be assembled together to form a set of equations which define the performance of the structure as a whole.

Finite element analysis is particularly suited to dealing with complex boundaries and this is useful in this application since the electrode structure becomes significantly more complex as it is modified to reduce its resistance. Initially, the structure is relatively simple and the main complexity in the electrode resistance calculation is the distributed, but uniform, nature of the resistance across the electrode area. Using a conductive grid and patterned electrode to reduce the electrode resistance

significant complicates the calculation of the electrode resistance and results in a problem well suited to finite element methods.

The COMSOL Multiphysics package [5.1] enables simulation of a physical process, such as electrical conduction, which can be modelled through partial differential equations. The program facilitates the input of complex geometric structures through a graphical interface and the simulation of two or three dimensional problems. It also provides some convenient support for thin film structures where there are large differences in dimensions for the different subdomains, as is the case with the DSSC structure.

Since it is the electrode resistance which is of interest in this analysis, the DSSC structure has been reduced to a model where the electrodes are separated by a material which has a thickness and electrical conductivity equal to that of the electrolyte. A potential of 0.5 V is placed across the cell which represents an idealised cell voltage and the distribution of the voltage across the area of the electrode is analysed. Measuring the current through the structure allows the self resistance of the cell to be calculated. This current is predominantly dependant on the resistance of the electrodes since the conductivity of the material (electrolyte) between the electrodes is significantly higher than that of the electrodes. In this way, it is possible to analyse and estimate the electrode resistance of the original DSSC structure and to explore improvements in the electrode design using a local interconnect over the surface of the electrode.

5.1.1 3D modelling of the cell

The initial construction of the DSSC shown in Figure 3 can be seen to have a uniform cross-section along its width. The cross-section is shown in Figure 27 and comprises of the TCO substrate for the photoelectrode which is in contact with the conductive media, representing the electrolyte, and this then contacts the TCO substrate of the counterelectrode. Within Comsol, a 3D model can be generated by taking this geometry and using the extrude function to form the DSSC structure.

The conductive layer in the TCO material is very thin, typically around 80 nm [5.4], and since this is much smaller than the electrode areal dimensions it will result in a much finer mesh grid being required within the finite element analysis to achieve a solution. This finer grid size requires more memory and processing time for the computer simulation and the limits of machine resource can be quickly reached under these circumstances. Consequently, an approximation was made where this layer was transformed to a thickness of the same order as the electrolyte spacing with the conductivity value being modified to provide an equivalent sheet resistance for the material using the equation:

$$Rs = \frac{1}{\sigma \cdot t}$$

where Rs is sheet resistivity, σ is conductivity and t is thickness of the material

Representing the TCO layer as a thicker layer for the purposes of the finite element analysis does not have a significant effect on the accuracy of the simulation. The voltage drop in the electrode is predominantly across the area of the electrode rather than through the thickness of the TCO layer. An example of a mesh generation for the DSSC structure is shown in Figure 28

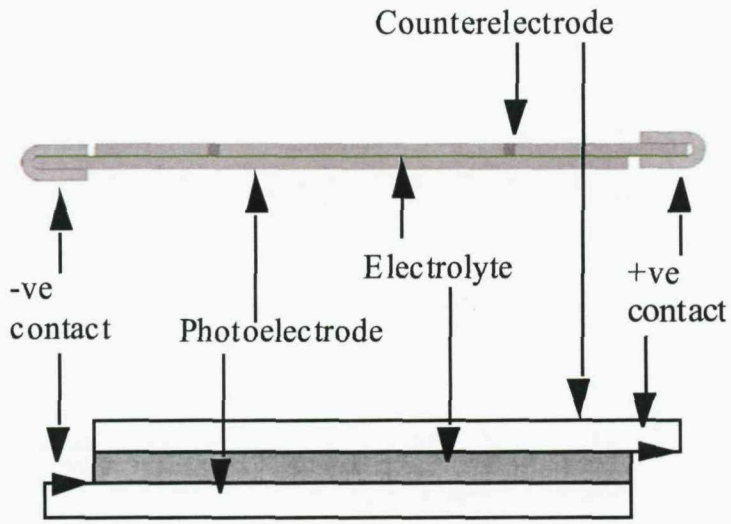


Figure 27: Cross section of the DSSC cell (upper) with the corresponding section of the Finite Element Analysis model (lower).

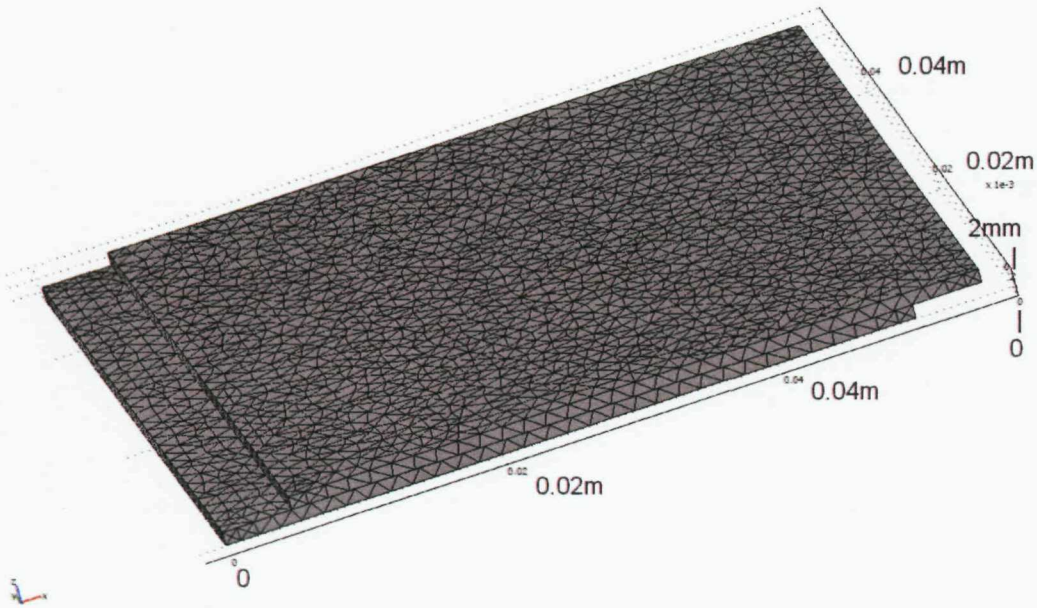


Figure 28: Mesh generation for the DSSC cell structure using the finer mesh setting.

The d.c. conductive media analysis option within Comsol solves for current balance in the separate subdomains (TCO layers and electrolyte) of the cell and this is described by the following equation:

$$\nabla \bullet (-\sigma \nabla V) = 0$$

where V is the electrical potential and σ is conductivity of the material

In the analysis, the conductivity of the materials used in the cell, corrected for thickness in the case of the TCO electrodes, are specified together with the voltage across the cell (set at 0.5 V for this analysis) and the boundary conditions around the cell. It is then possible to solve for the voltage distribution through the cell and for the output current. The total resistance of the structure can then be calculated and compared to the experimental results for the celll resistance.

The electrolyte conductivity used for these simulations was 0.185 S/m and this was taken from [5.2] and was the highest ionic conductivity for an electrolyte consisting of KI and I_2 dissolved in a blending polymer of polyvinyl pyrrolidone (PVP) and polyethylene glycol (PEG). This value is somewhat pessimistic and in [3.2], an

electrolyte of 0.3M NaI and 0.03M I_2 solution in acetonitrile had a bulk resistivity measured as 40 Ωcm which translates to a conductivity of 2.5 S/m. Although the latter electrolyte is more representative of the electrolytes used in this research, the lower conductivity of 0.185 S/m provides a worst case value. Using this value demonstrates that the resistance of the TCO layer, and not the electrolyte conductivity, is the main inhibitor to reducing the internal resistance of the DSSC. This is further demonstrated in [5.3] where the current density supported by a similar cell, taking into account the series resistance of the electrodes, exceeds 60 $mAcm^{-2}$ at a cell voltage of 0.5 V. This translates to an electrolyte path resistance of less than 0.6 Ω for the 14 cm^2 area cell used in this work.

The result for the initial DSSC structure is shown in Figure 29 where the voltage distribution is plotted through a cross-section of the cell. The voltage drop is almost entirely within the electrode path with negligible loss through the electrolyte material. Running this simulation at the finest mesh setting yields a result for the output current of 0.588 A/m, this corresponds to a current of 0.0294 A for the 50 mm width of the cell. These results were obtained assuming an electrolyte conductivity of 0.185 S/m and a conductivity for the electrodes which corresponds to the nominal value of 20 Ω/sq for the TCO material. These results provide a total cell resistance of 16.98 Ω which can be divided between the two electrode resistances neglecting the resistance of the electrolyte.

In this work, the 2D structure of the electrode is important as the initial DSSC structure is refined to include an interconnect pattern to reduce the voltage drop across the TCO material and improve the electrode resistance. Although a full 3D simulation could be run, it was found that memory limits were soon reached for these relatively simple structures and so a more efficient analysis method was required.

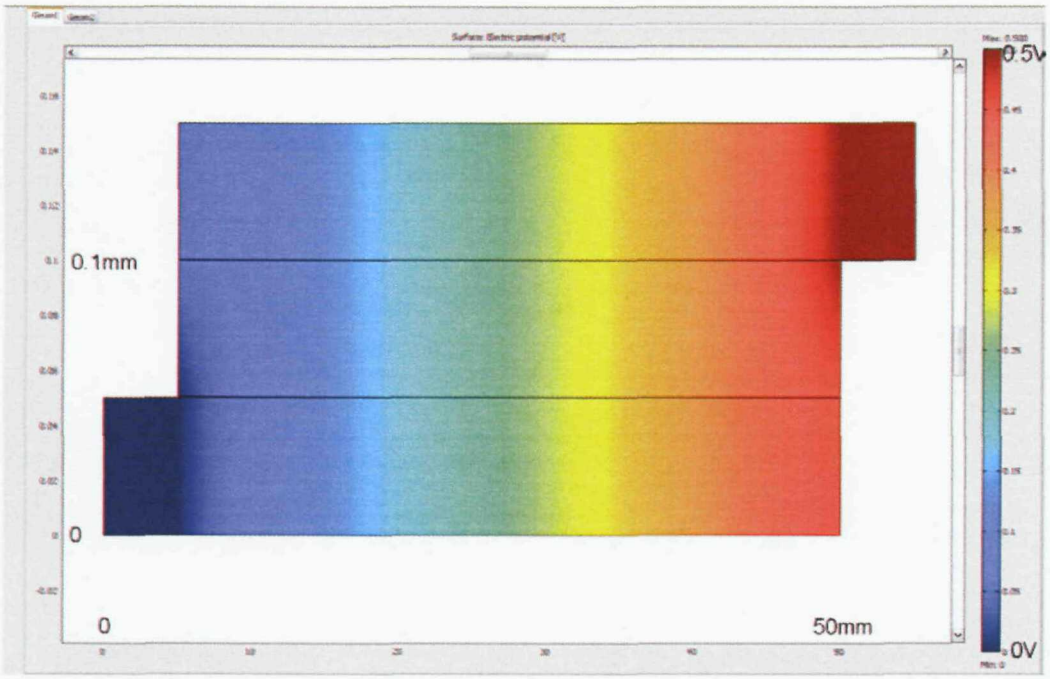


Figure 29: Voltage distribution across the initial DSSC structure viewed through a cross-section of the cell.

5.1.2 Thin film modelling techniques

The modelling of thin film structures, defined as the case where there is large difference in the dimensions of the different subdomains, is a common requirement within finite element analysis. Comsol Multiphysics has a feature [5.1] where the thinnest layers can be replaced with a thin layer approximation which is valid providing that the differences in thicknesses between the sub-domains are large. The electrolyte layer was replaced with this thin layer approximation which enabled the 2D performance of the electrode to be analysed more efficiently.

The initial DSSC structure was modelled using this technique with an isopotential area defined along the edge of each electrode corresponding to the contact strip. This technique is used later to define the areas of the interconnect grid where the implicit assumption is that the conductivity of the interconnect material is much greater than that of the TCO material. The voltage distribution is shown with a 3D view of the cell in Figure 30 and this is consistent with the previous surface plot showing the

cross-section of the cell. This simulation provided an output current of 0.0289 A for the structure biased at 0.5 V which is in close agreement with the previous result of 0.0294 A, thereby confirming the validity of this approach.

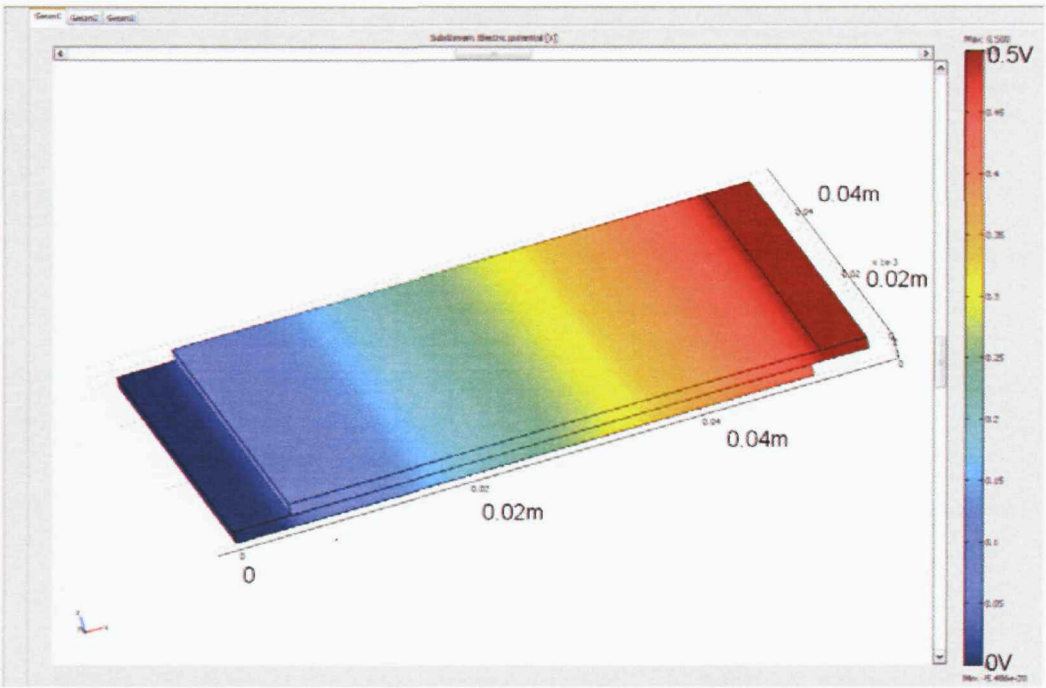


Figure 30: Voltage distribution across the initial DSSC structure modelled using the thin-layer approximation and shown as a 3D plot.

An interconnect pattern can now be analysed using this technique and a simple structure would be the placement of a wire across the electrode to reduce the potential drop along the length of the electrode. The arrangement used is shown in Figure 31 where a conductor of 2 mm width is centrally placed on the electrode and orthogonal to the contact strip. The significant performance improvement which results is evident from the resulting surface plot shown in Figure 32.

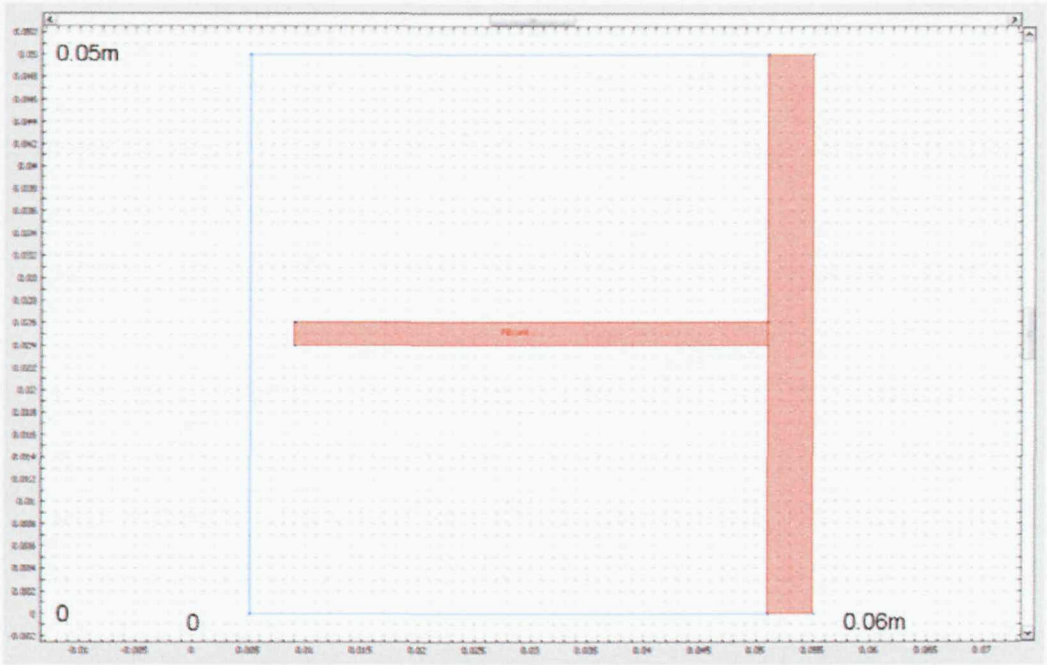


Figure 31: Structure of a photoelectrode interconnection grid where a 2 mm wire is placed orthogonal to the contact strip in the centre of the electrode.

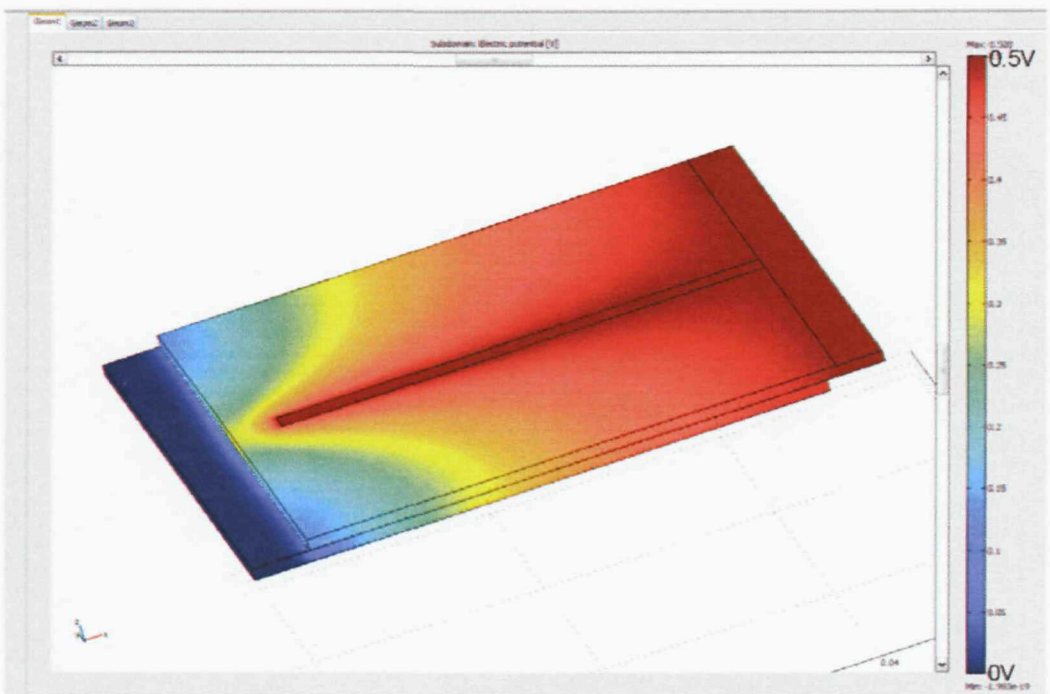


Figure 32: Voltage distribution across the cell with the single finger electrode.

The single finger electrode cell has an output current of 0.0721 A which corresponds to a cell resistance of 6.93 Ω, this is a significant improvement over the previous result of 16.98 Ω.

5.1.3 Modelling the experimental interconnect patterns

In the experimental work, two interconnect patterns were deposited onto the TCO substrate used to make the photoelectrode prior to the deposition of the TiO_2 layer. The interconnect layer was a deposited using gold which was evaporated onto the ITO substrate. Gold has a conductivity of $4.1x10^7$ S/m compared to the ITO layer which has a conductivity of $6.25x10^5$ S/m for the 20 Ω/sq material; the sheet resistivity of the gold layer was calculated at 0.11 Ω/sq. The interdigitated pattern shown in Figure 33 was deposited together with a grid pattern shown in Figure 34.

The analysis for the interdigitated interconnect pattern is shown in Figure 35 and since the photoelectrode is the negative terminal of the cell then this is reflected on this surface plot with the maximum potential of +0.5 V being on the contact strip for the counterelectrode. It is evident that the interdigitated pattern works well at minimising the voltage drop in the electrode between the fingers of the pattern with the only significant loss occurring outside the pattern on the edges of the electrode. The output current was 0.0476 A corresponding to a cell resistance of 10.5 Ω. This result, which is higher than that of the single finger pattern, emphasises the importance of the interconnect grid covering the full length of the electrode in the case where the connection is made on just one edge of the electrode as with this geometry. In this case, the interdigitated pattern should have been orientated such that the fingers were orthogonal to the contact strip rather than parallel to it.

The analysis for the grid interconnect pattern is shown in Figure 36, again its effect in reducing the voltage drop within the grid is clear. Since the pattern extends further towards the far edge of the electrode the overall voltage drop across the electrode is less. This is reflected in the output current of 0.0817 A corresponding to a cell resistance of 6.11 Ω. These results show that the interconnect pattern could be further optimised, with a reduction in the overall area of the interconnect layer, using fewer and thinner conductors which are arranged more efficiently over the area of the electrode.

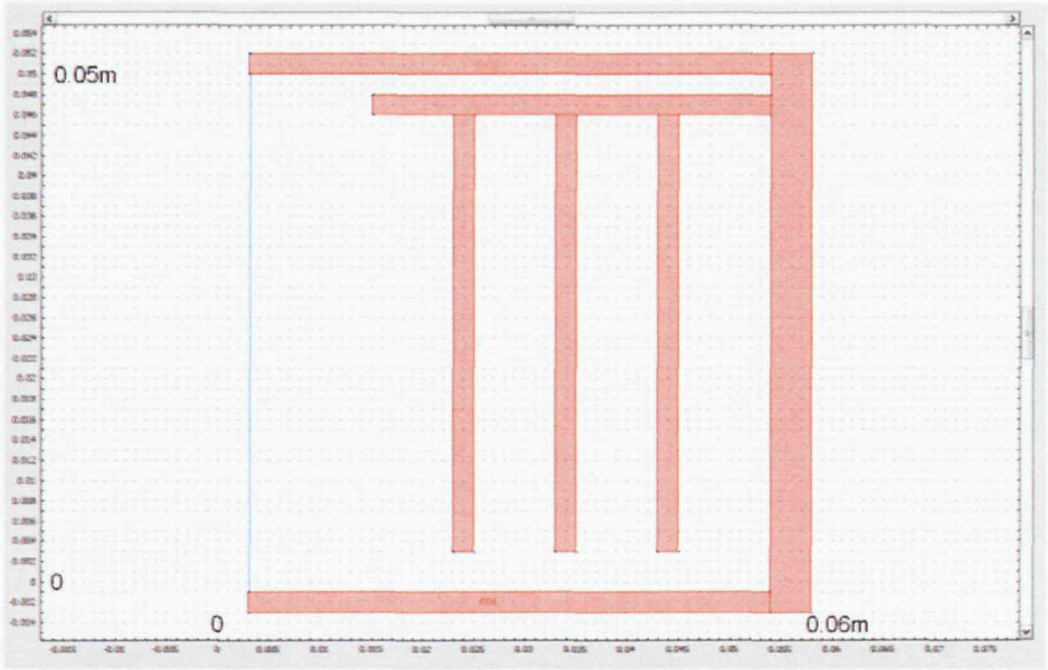


Figure 33: An interdigitated pattern used for the interconnect layer on the photoelectrode (Cell 4_1610).

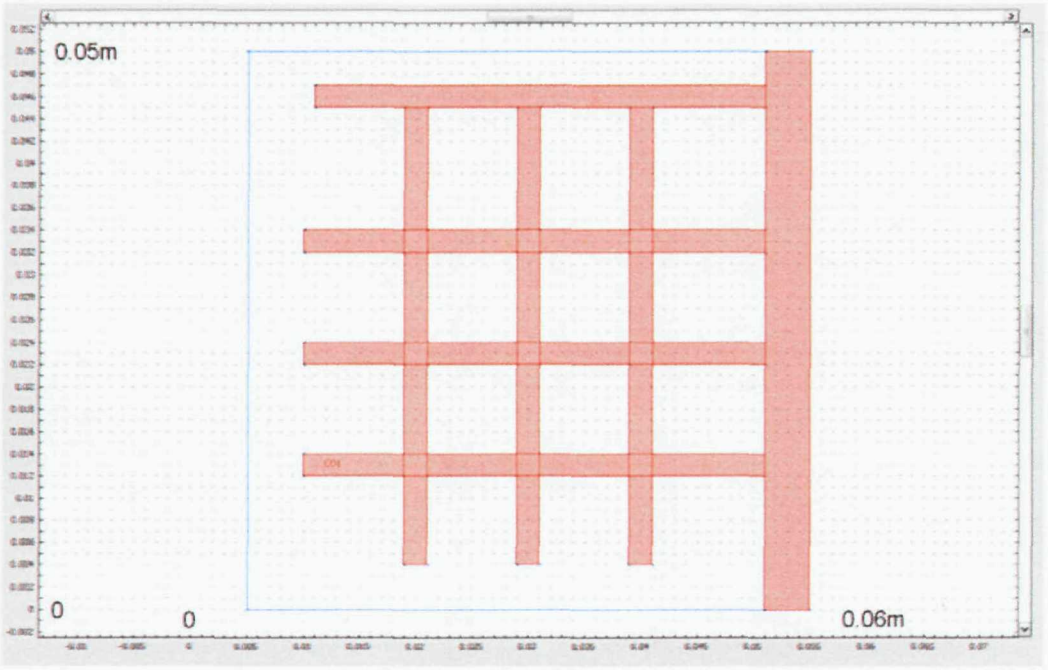


Figure 34: A grid pattern used for the interconnect layer on the photoelectrode (Cell 5_1610).

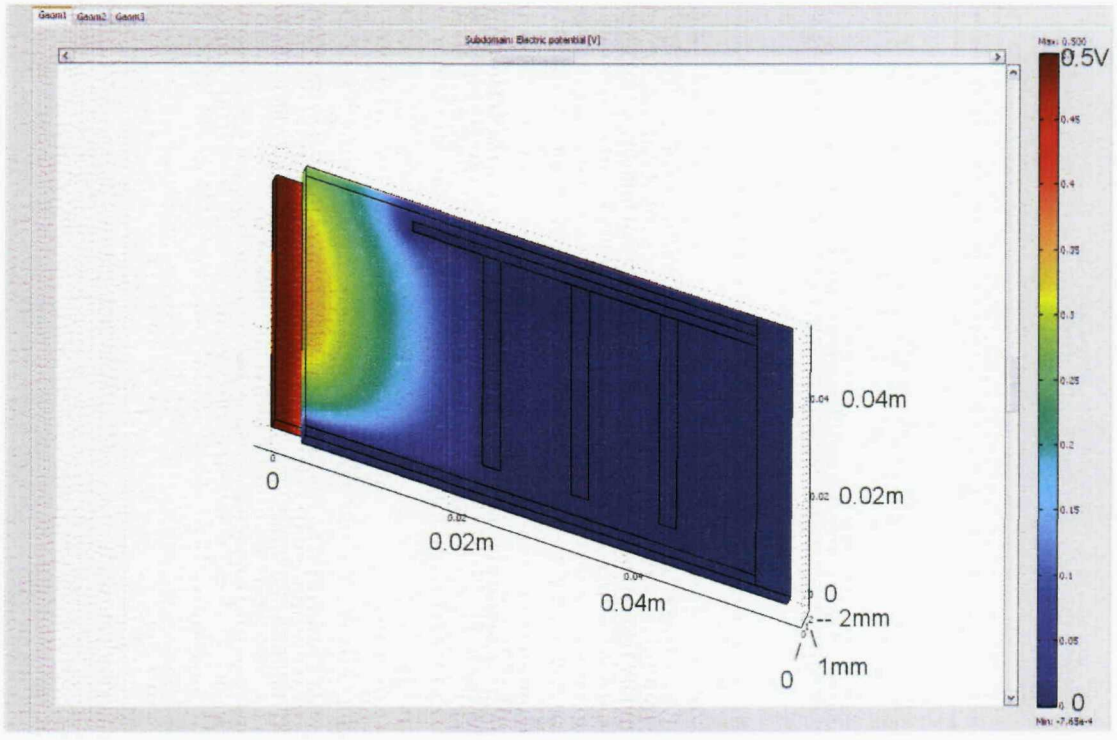


Figure 35: Voltage distribution across the cell with the interdigitated interconnect pattern.

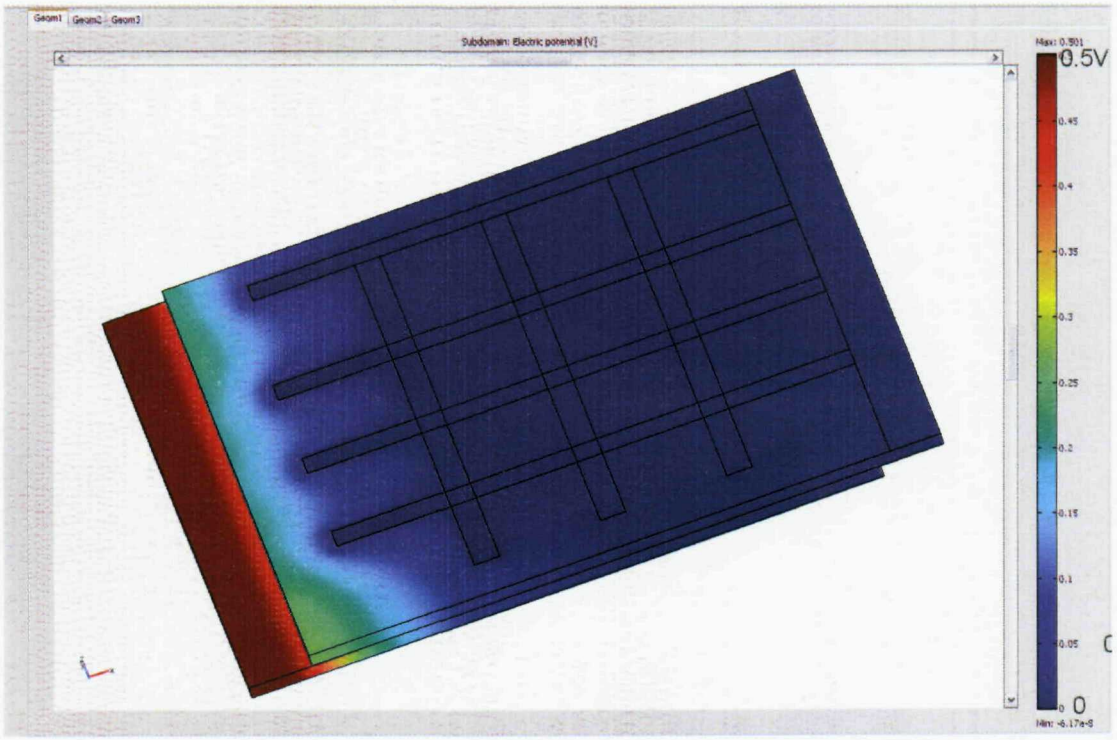


Figure 36: Voltage distribution across the cell with the grid interconnect pattern.

5.1.4 Designing an efficient interconnect layer for the photoelectrode

This analysis shows the value of finite element methods in the design of the interconnect pattern for the photoelectrode. There are obvious improvements which can be made to the laboratory cell design such as using a contact area which runs around the perimeter of the cell. However the design of the interconnect pattern in the interior of the electrode is more complex. An optimum design should balance the loss in output due to the presence of the interconnect with the improvement in power output that the interconnect provides. Clearly this problem becomes more serious as the cell increases in area and the interconnect pattern increases in complexity. On larger arrays, the interconnect could also be used to provide the series connection of multiple cells between islands of TCO material on the same common substrate.

There are interesting trade-offs that can be made in the design of the photoelectrode substrate which could provide further advantages for an interconnection layer. Ideally, the TCO resistivity should be as low as possible but reducing this parameter increases the attenuation of light through this layer. The typical transmission for a 20 Ω/sq ITO coating is 85% [5.3] with optimum transmittance at 500 nm. However with a local interconnect, this coating could be increased in resistivity, improving the incident light to the photoelectrode, with the interconnect handling the higher current collection of the generated photocurrent. In the case of the dye sensitised solar cell, the area taken by the interconnect layer may not be totally lost to photogeneration since the TiO_2 film edges will be exposed around the interconnect layer. Since the TiO_2 film thickness is typically of the order of 20 μm, it could provide some additional photocurrent from light scattered around the interconnect providing some compensation for the lost area.

The optimum design of the photoelectrode interconnect layer is complex with multiple factors influencing its performance. It would be relatively straightforward to use the simulation capabilities of Comsol Multiphysics in conjunction with an optimisation tool such as simulated annealing or the genetic algorithm [5.5] to explore these design possibilities. Indeed, a multi-objective design environment has already been integrated with Comsol Multiphysics for the purpose of multiphysics optimisation [5.6]. In a multi-variable design problem, local minima typically exist

as well as a global minima. The design surface can be represented as a multi-dimensional landscape with many peaks and troughs, representing the minima and maxima of the design. This is shown in Figure 37 for a two dimensional problem. Clearly the objective for an optimisation program is to find the global minimum across this design space for an overall cost function and to avoid getting stuck in a local minimum.

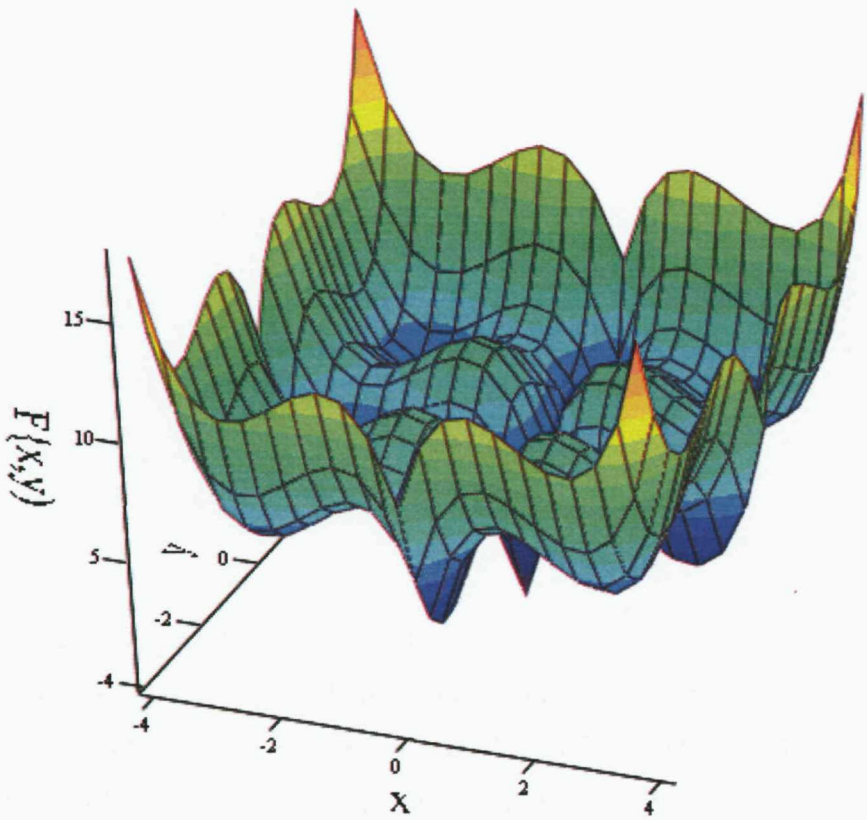


Figure 37: A function F(x,y) dependant upon variables, x and y, exhibiting local minima in addition to a global minimum.

The genetic algorithm can effectively search for a design of best performance which is defined by a minimum cost with the cost function itself being defined by factors such as:

- The loss in photogeneration capacity due to the interconnect layer.
- The power output improvement achieved with the interconnect layer.
- The pattern style used and its ease of manufacture.

- The economic cost of the interconnect material.

The thick film processing enables the photoelectrode and interconnect layer material to be deposited at any point on the photoelectrode with the printing resolution limited by the screen mesh size. The pattern is not inhibited by the structural requirements of a template. This would allow the provision of such features as tapered wires in the interconnect layer where the wire width changes as the collected current increases along the length of the wire. In what would be a relatively simple optimisation problem, the program could search for the best pattern on the photoelectrode balancing performance improvement with cost. These techniques could result in a worthwhile improvement in the efficiency of the DSSC cell at a relatively low marginal cost, enabling the efficient design of large area DSSC devices.

CHAPTER 6: DEVELOPING THE PERFORMANCE OF THE DYE SENSITISED SOLAR CELL USING ELECTRODE PRINTING

6.1 Development of the TiO_2 photoelectrode

6.1.1 Paste Development

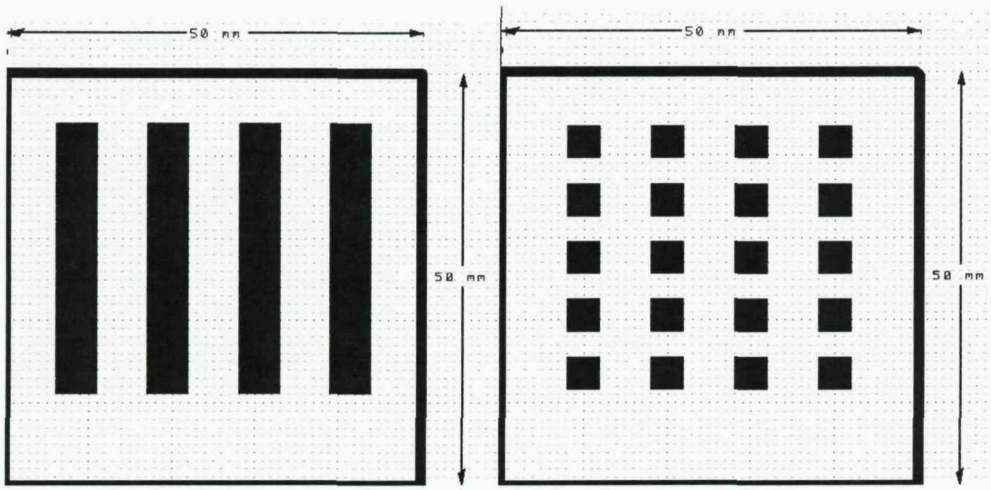
In thick film deposition, the final quality and thickness of the film depends on the composition of the paste and the sintering characteristics of the particles within the paste material. The satisfactory deposition of the wet film is crucial to achieving the desired final properties for the dried film. During the development of the paste, the main objectives were to improve the flow of the paste through the screen and onto the substrate and to improve the quality of the deposited wet film. All the pastes were based on the DeGussa P25 TiO_2 nanopowder which formed an effective mesoporous structure after the sintering process on the dried, deposited film. The sintering step is an important stage of the production process and further work could be performed on improving this process. This could include the investigation of sinter flux materials which could be added to the paste. As previously discussed, the rheology of the paste can be improved by working the paste and after preparation the pastes were subjected to stirring and ball mill processing.

The pastes used during this work were predominantly those described in 2.2.1 and for the results presented later in this section, Paste 4 was used. The 2-ethyl-1-hexanol based Paste 3 yielded a cell which produced Isc = 4.25 mA and Voc = 610 mV (Cell 1_3007 with 14cm^2 area) under illumination from the LED solar simulator which was comparable to the performance achieved with the other pastes. Although all pastes produced working photoelectrodes, the terpinol based pastes were found to provide consistent printing results with an even deposition of the wet film around the print area. The previously published composition of Paste 2 was slightly modified by increasing the relative amount of terpinol to provide a thinner paste. After working, this was found to provide good results with the 43 threads/cm and 90 threads/cm screen sizes used in this work producing final film thicknesses, after sintering, of 20 μm ±3 μm and 6 μm ±2 μm respectively.

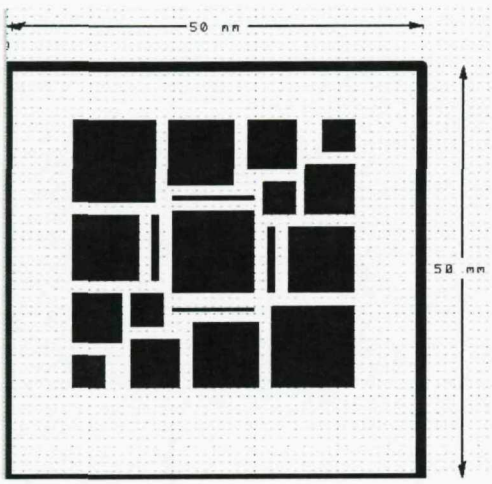
6.1.2 Patterned Electrodes

The ability to print patterned electrodes is a useful feature of the thick film process used to make the photoelectrodes and enables the printing of the active TiO_2 area around an interconnect layer. This interconnect layer is designed to improve the current collection at the photoelectrode and to reduce the electrode resistance. The interconnect layer could itself be deposited with thick film techniques, or it could be pre-deposited onto the TCO substrate and the screen for the TiO_2 deposition simply aligned to it. The ability to print relatively complex 2-D photoelectrode structures for the DSSC also offers other intriguing possibilities for this technology. Possible applications include increasing the active area of the photoelectrode by exposing large areas of the film edge to incident light, and increasing the consumer appeal of the photovoltaic panel through texturing and patterning of the photoelectrode on a cell which could itself be translucent.

Several patterns were designed to test the ability to deposit the TiO_2 film for such electrodes and these are shown in Figure 38. Screens for these patterns were made with a mesh size of 43 threads/cm, these produced a final film thickness of around 20 μm. All of these patterns were successfully deposited onto the TCO substrate using Paste 4. In the case of pattern 'Test', the line thickness is as low as 0.5 mm for several of the shapes and these were all deposited satisfactorily on multiple substrates. This demonstrates the capability to make complex photoelectrode structures to support a fine interconnection grid which could be less than 0.5 mm in width. Clearly the printing resolution is set mainly by the mesh size of the screen which also controls the film thickness. The profilometry results, such as those shown in Figure 12, indicate regular edge profiles with a width of around 0.15 mm. Consequently minimum separation distances between TiO_2 regions in the order of 0.5 mm to 1 mm would be viable to support the integration of an interconnect layer into the photoelectrode.



Bar Square



Test

Figure 38: Patterns for the TiO_2 photoelectrode.

The DSSC devices built directly from the pattern 'Bar' or 'Square' exhibited poor photovoltaic performance. This is thought to be due to the large area of TCO on the photoelectrode which is exposed to the electrolyte, this offers a low impedance shunt path for the photocurrent. The reduction of the electrolyte triiodide ions back to iodide ions can take place at these exposed regions rather than at the counterelectrode, thereby reducing the external current at the cell terminals.

This problem can easily be resolved by introducing a screening layer between the exposed TCO regions and electrolyte to eliminate this shunt path for recombination current. This was tested by depositing a thin layer of TiO_2 over the full area of the photoelectrode using a mesh size of 90 threads/cm. After drying of this film, the patterned region of the photoelectrode was then deposited and after further drying, the composite film was sintered. The resulting surface profile is shown in Figure 39 and it can be seen that the 'background' film thickness is around 6 μm with the thickness in the patterned region increasing to around 25 μm. Of course, a practical screening film need not be of TiO_2, its main role is as an insulator and it could be much thinner. However this method, which was convenient to use because of the availability of the screen and materials, demonstrates how it is also possible to build 3-D structures in the mesoporous TiO_2 film with these screen printing techniques.

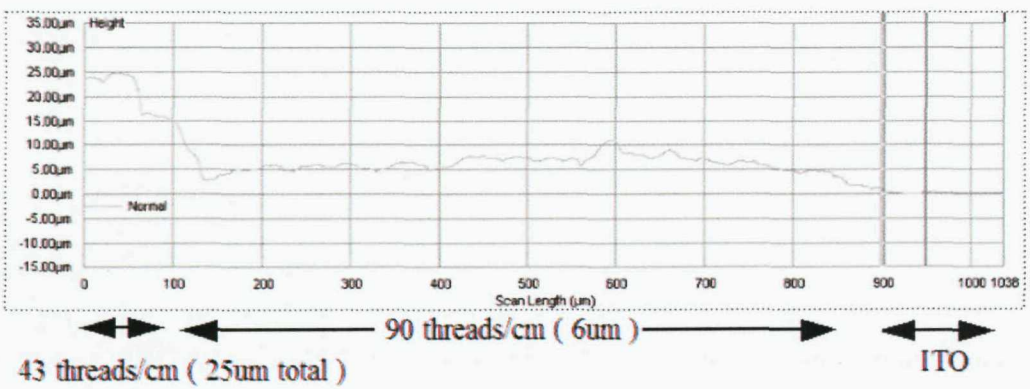


Figure 39: The surface profile of an electrode with a two layer TiO_2 film measured using the Tencor Alpha-Step surface profilometer.

The pattern on the left hand side was deposited using a 43 threads/cm screen onto a background layer deposited using a 90 threads/cm screen with the ITO surface being at the right hand side of this profile

The DSSC devices built using a patterned structure on a background layer exhibited a comparable performance to the plain photoelectrodes previously built as shown in Figure 40. The output is typically less due to the reduced area of the patterned electrode; although the background film is also contributing to the photocurrent, its reduced thickness generates less current.

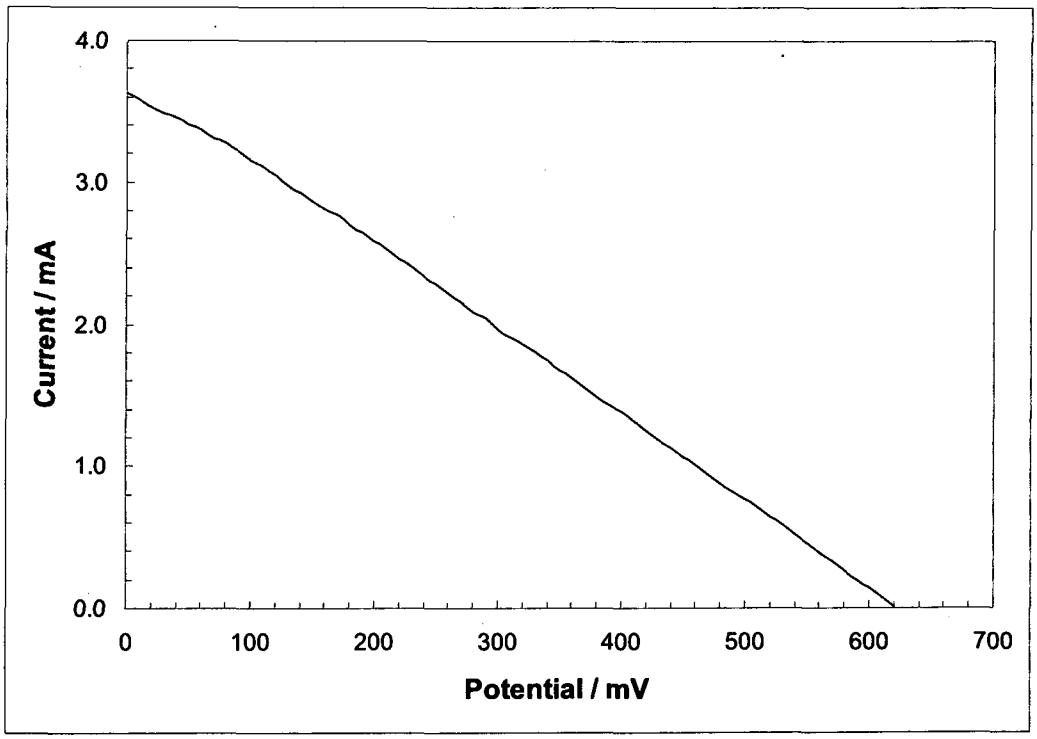


Figure 40: I -V Characteristic under LED illumination for a 'bar' patterned electrode of 20 µm thickness onto a background TiO_2 film thickness of 6 µm (Cell 6_1110 with a patterned cell area of 14cm^2).

6.2 Improving the TCO substrate conductivity with an interconnect layer

6.2.1 A DSSC device with interconnect layers

The interconnect layer can be deposited onto the TCO substrate by various techniques as described previously. This layer could be screen printed using a conductive paste; such pastes which are readily available for laying down conductive traces in thick film applications. In this case, the conductive layer was deposited using evaporation techniques. A stencil was built to implement the three finger interdigitated pattern shown in Figure 33. Turning this stencil through 90° after the first evaporation and depositing a second layer formed the grid pattern shown in Figure 34. Additional gold lines were also formed at the edges of the substrate due to overlap of the substrate with the stencil.

A BOC-Edwards E306A coating system was to evaporate a gold layer through the stencil with an estimated thickness of between 200 nm and 250 nm. Assuming a conductivity for gold of 4.1×10^{-7} S/m, this yields a sheet resistivity for this layer of 0.1 Ω/sq. These substrates were then used to build photoelectrodes by depositing the TiO_2 layer directly on top using the standard 40 mm x 35 mm rectangular pattern. Ideally, a customised screen pattern would be used to deposit the TiO_2 layer around the interconnect layer especially if the latter had been deposited as a thick film rather than as a thin film. However, in this case the thin gold layer allows the TiO_2 layer to be deposited over the top without significantly affecting the quality of the film.

The performance of a DSSC device with the interdigitated interconnect compared to a similar device without the interconnect layer is shown in the I-V characteristic of Figure 41 for devices with a TiO_2 layer thickness of 6 μm. The expected improvement with the interconnect layer can be seen with an increase in the short circuit current and a slightly improved characteristic for the fill factor.

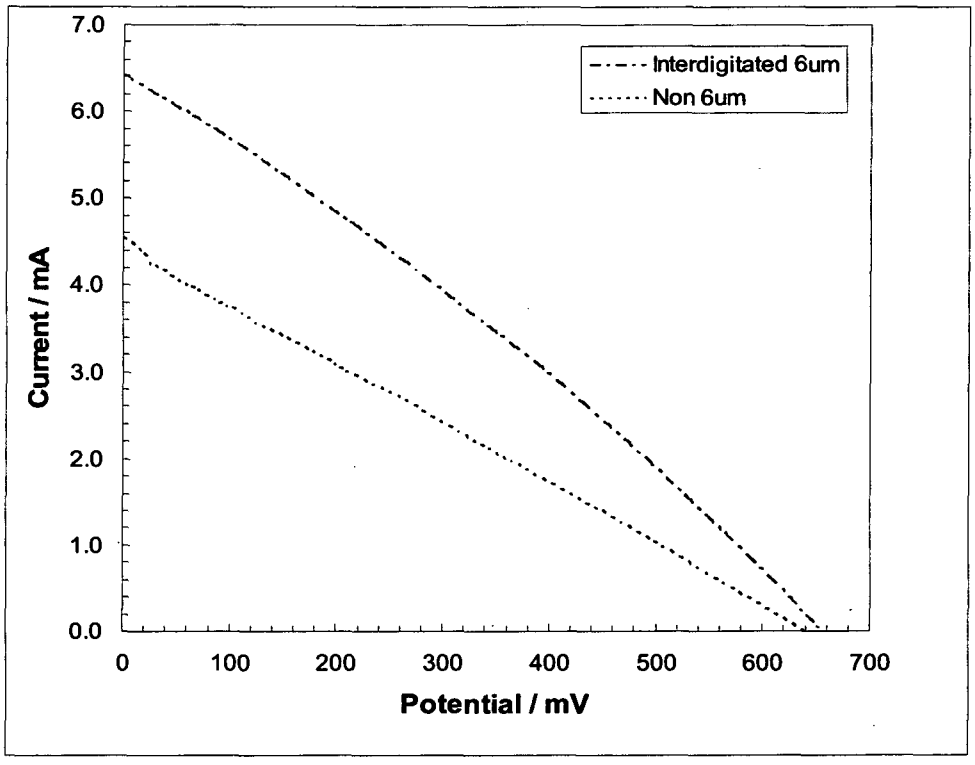


Figure 41: I-V Characteristic for DSSC devices without an interconnect layer (Cell4_1110) and with an interdigitated interconnect (Cell 2_1110).

Both photoelectrodes had a TiO_2 thickness of 6 μm.

This performance improvement is shown in the impedance plots of Figure 42 for devices with and without this interdigitated interconnect layer. The internal resistance of these cells is high because of increased TCO resistivity; but the value for the interdigitated DSSC is significantly reduced at 68 Ω compared to 122 Ω for the DSSC without this interconnect.

Similar results are shown in Figure 43 for DSSC devices with a TiO_2 layer thickness of 20 μm which include both the interdigitated and grid interconnect structures modelled in Chapter 5. Here the grid pattern yields the lowest cell resistance at 77.7 Ω, followed by the interdigitated pattern at 86.6 Ω while the plain cell without an interconnect layer gives 110 Ω.

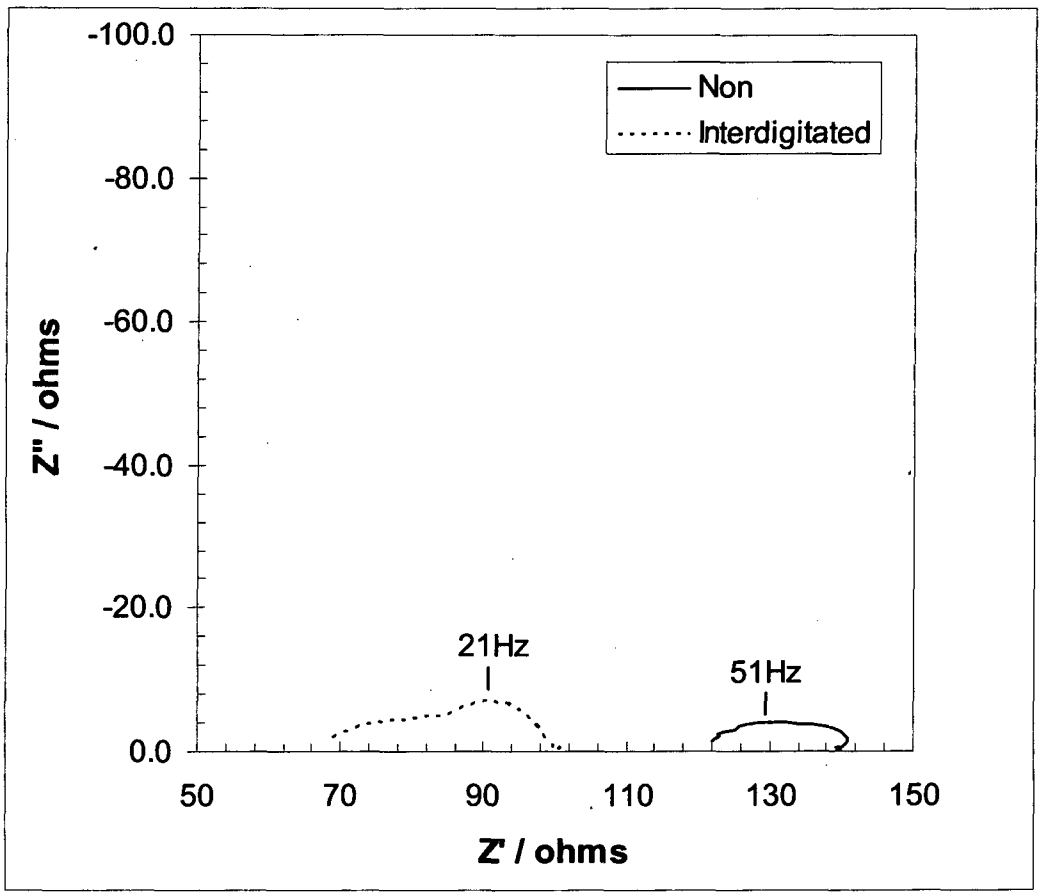


Figure 42: Impedance plot under LED illumination for DSSC devices without an interconnect layer (Cell 8_1110) and with an interdigitated interconnect pattern (Cell 2_1110) over the frequency range 0.1 Hz to 65 kHz.

Both photoelectrodes had a TiO_2 thickness of 6 μm.

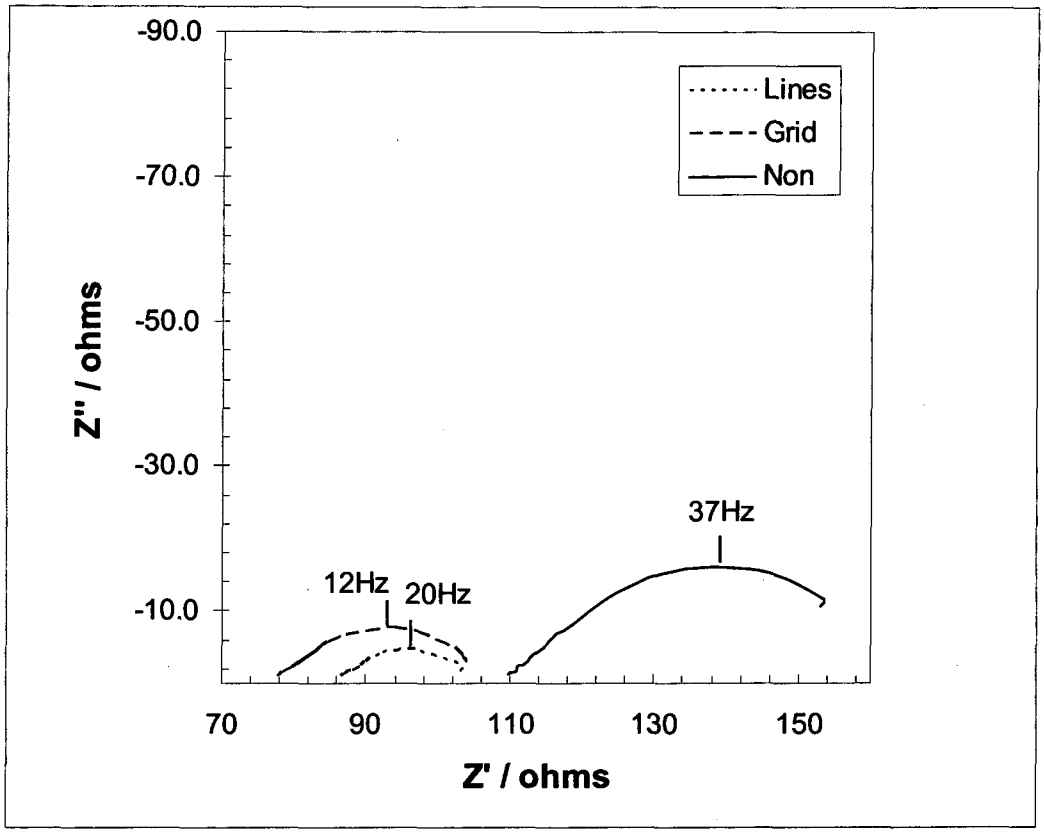


Figure 43: Impedance plot under LED illumination for DSSC devices without an interconnect layer (Cell1_1610), with an interdigitated interconnect pattern (Cell 4_1610) and with a grid interconnect pattern (Cell5_1610) over the frequency range 1 Hz to 65 kHz.

These cells had photoelectrodes with a TiO_2 thickness of 20 μm.

6.2.2 A comparison with simulation results

The simulation performed in Chapter 5 gave the following results for the internal resistance of the DSSC cell:

	No interconnect	Interdigitated	Grid
Internal Resistance	16.98 Ω	10.5 Ω	6.11 Ω

However these results assumed a TCO sheet resistivity of 20 Ω/sq and the sheet resistivity of the laboratory cells was significantly higher due to the previously

described problem with high temperature degradation of the ITO layer. Removing the contact strips for these cells enabled measurement of the final sheet resistivity of the ITO layer for these electrodes:

	No interconnect	Interdigitated	Grid
Counterelectrode	123 Ω/sq	173 Ω/sq	126 Ω/sq
Photoelectrode	101 Ω/sq	N/A	N/A

The sheet resistivity for the interdigitated and grid photoelectrodes could not be accurately measured due to the proximity of the gold interconnect layer within the contact strip area. These values have been assumed to be the same as the photoelectrode without interconnect since all of these photoelectrodes were built in the same batch. The Comsol simulation was rerun with these amended sheet resistivities and the results are compared to the laboratory results:

	No interconnect	Interdigitated	Grid
Simulation	90.9 Ω	61.6 Ω	29.7 Ω
Measured	110 Ω	86.6 Ω	77.7 Ω

The simulation results do not account for the resistance through the mesoporous TiO_2 film and so there is an expected offset with the simulation being less than the measured values due to this component. In [3.3], Bay and West quote an average resistivity of 120 kΩcm for the anatase phase of the TiO_2 film under illumination. Applying this value to an electrode area of 40 mm x 35 mm with an average thickness of 20 μm provides a resistance for the TiO_2 film of 17 Ω. This is close to the difference between the simulated and measured values of internal resistance for the cell without interconnect where the full area of the film is exposed to illumination.

In the case of the interdigitated and grid interconnect, some of the 40 mm x 35 mm area of the TiO_2 film is covered by the gold interconnect layer. Approximately 17% of the TiO_2 film area is covered by the gold layer for the interdigitated pattern which increases to 34% for the grid pattern. The sheet resistivity of the TiO_2 film is strongly dependant upon light as would be expected from a semiconductor. The current flow through this mesoporous structure is predominantly vertically through the film

thickness and onto the TCO layer rather than laterally across the film. Consequently the loss of conductance in part of the TiO_2 film due to shielding by the interconnect layer could account for some of the difference between the simulation and measured values with the interdigitated electrode. However there is still more unaccounted resistance in the case of the grid electrode.

Measurement of the conductivity of the TiO_2 film would be a useful development of this experiment. A more accurate analysis could be provided by including the TiO_2 film into the Comsol simulation and this would be a logical development for the modelling of electrode performance. . Additionally, verification of the simulation results could be performed with a non DSSC device structure which reproduces the simulation arrangement. An electronic thin film conductor could replace the electrolyte between the patterned TCO substrates allowing the resistance of the design geometry to be easily measured. This would also form a useful test arrangement before the substrates are built into a DSSC device.

6.3 Other Improvements

6.3.1 FTO substrates

The susceptibility of ITO substrates to damage from high temperature processing prompted the investigation of fluorine doped (FTO) substrates as a replacement. Extensive use is made of FTO substrates in the literature, however this material is not as readily available as ITO. Although designed for improving the thermal insulation to glazed windows, Pilkington 'K' glass does contain an FTO layer with a suitable resistivity for this application.

The minimum thickness of Pilkington K Glass is 3 mm, however this thickness can be accommodated by the screen printer and so the process of DSSC production is unaltered. The material was cut to form 50 mm x 50 mm substrates and the sheet resistivity was measured at 18.3 Ω/sq. A substrate was subjected to a modified heating profile from that shown in Figure 7 where the belt speed was reduced by 33% to increase the duration at 450°C to 20 mins. The sheet resistivity was then re-measured and found to be 22.7 Ω/sq, this is a significant improvement over the resistivity increases seen with ITO material.

Devices were built using this FTO material for the photoelectrode with a plain 40 mm x 35 mm TiO_2 film of 20μm thickness without an interconnect layer. The counterelectrode used conventional ITO material, the I-V characteristic of one of these devices is shown in Figure 44.

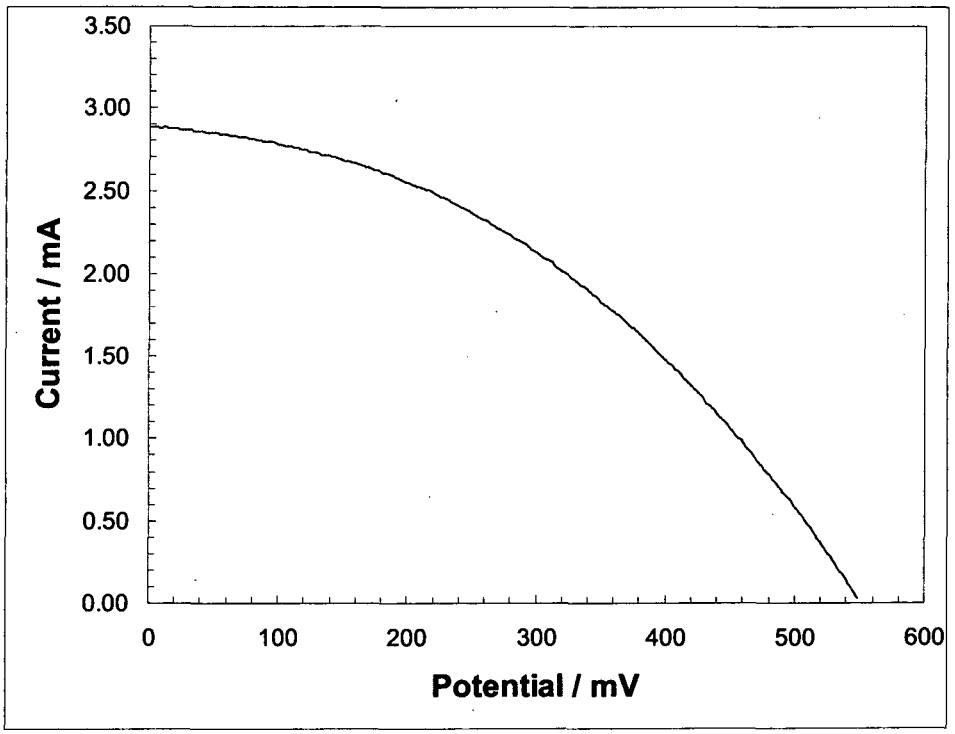


Figure 44: I -V Characteristic under LED illumination for Cell 3_1610 having a Pilkington 'K' glass FTO substrate for the photoelectrode.

40 mm x 35 mm (14cm^2) TiO_2 electrode on FTO glass with a thickness of 20 μm.

The improvement in device performance obtained is evident from the characteristic which shows a significant improvement in the 'fill factor' compared to similar ITO based devices.

6.3.2 Optimisation of the TiO_2 layer thickness

In the screen printing process, the thickness of the TiO_2 layer can be easily adjusted by, for example, controlling the mesh size of the screen. There is an optimum thickness for this layer and [6.1] suggests that this between 18 and 20 μm for a film made from DeGussa P25 TiO_2 nanopowder. At lower thicknesses, the cell efficiency

increases with thickness as dye build up dominates the photocurrent generation. However at higher thicknesses, recombination of the photogenerated electrons with the electrolyte becomes more significant, reducing the overall efficiency.

In Figure 45, the I-V characteristics of DSSC devices with TiO_2 film thicknesses of 6 μm and 20 μm demonstrate the improved efficiency as the film thickness is increased. Further data could be collected using additional screens with different mesh sizes to identify the optimum thickness.

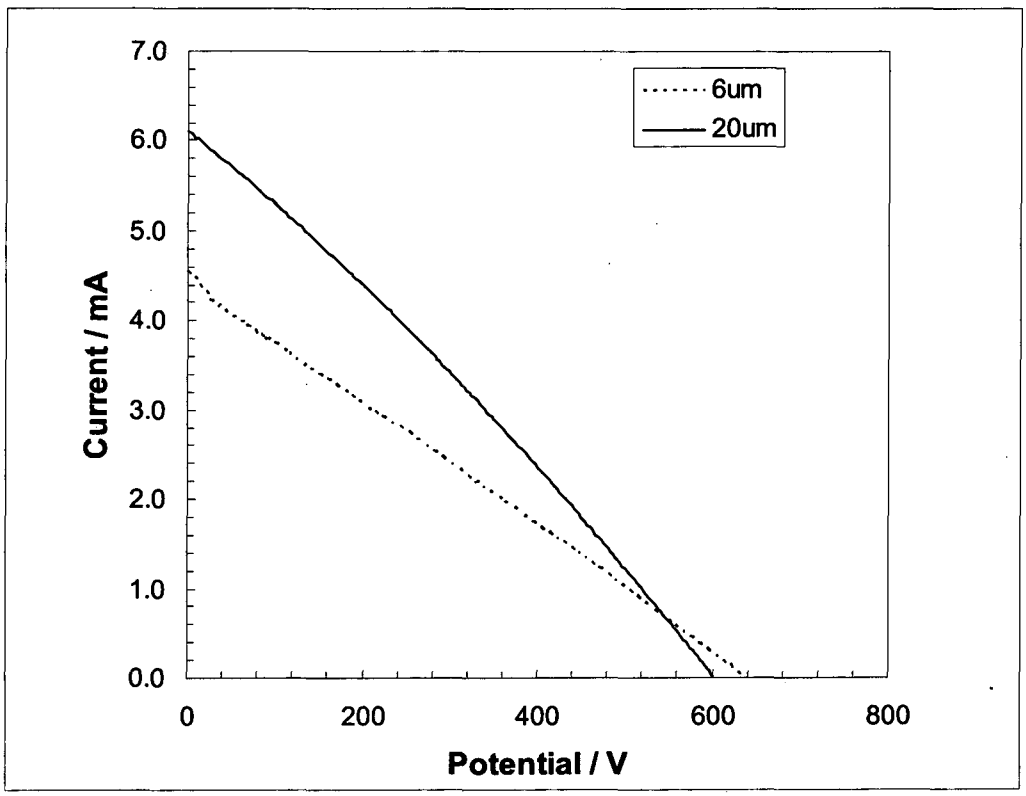


Figure 45: I -V Characteristic under LED illumination for a photoelectrode TiO_2 thickness of 6 μm (Cell 4_1110) and 20 μm (Cell 1_1610).

The cell area was $14cm^2$ for both cells.

6.3.3 Screening and barrier layers

The use of barrier and screening layers could significantly improve the DSSC device performance. It has already been shown how a screening layer could be used at the photoelectrode to reduce recombination of the photogenerated electrons at the electrolyte interface. This screening layer is used to electrically isolate the TCO layer

from the electrolyte interface, cutting off this recombination path and thereby improving the collection of the photogenerated electrons at the photoelectrode. Again the screening layer could be applied through a thick film deposition process and could also be used to protect the interconnect layer from the electrolyte. In this research, gold has been used for the interconnect layer but it may be more desirable to use other materials of lower cost, such as silver. These may need to be isolated from the electrolyte to avoid corrosion processes. This layer could be applied as the final deposition process in the production of the photoelectrode and standard coatings exist for this type of application.

A barrier layer may be desirable at the interface of the TCO and TiO_2 layers on the photoelectrode. This barrier layer could reduce the damage to the TCO film of high temperature processing. It may also improve the electron path between the mesoporous TiO_2 film and the TCO layer. Although outside the scope of this research, it may again be possible to deposit such a layer by thick film methods, although may be more effective or to include it as a separate process within the production of the TCO substrate.

6.3.4 Lower cost materials for the conductive layer

In this research, gold has been used for the conductive layer since it was a convenient material to deposit onto the ITO substrate and has a relatively high conductivity. In practice, a lower cost material would be desirable, especially if the layer was being applied using thick film techniques. Although silver has been used for this type of application, it is also an expensive material. The use of carbon-based conductive inks may provide a solution, especially with the development of carbon nanotube conductive pastes. There are also other metals which could be deposited to provide a more efficient performance in terms of conductivity and cost.

CHAPTER 7: CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

The work has demonstrated the application of thick film techniques to the production of the DSSC. This technology allows the production of large area electrodes at relatively low cost using established manufacturing methods. Laboratory devices have been built with reasonably consistent performance between batches using techniques which can be readily scaled in both device area and production quantity.

The importance of the electrode resistance to DSSC performance as the cell area is increased has also been demonstrated using simulation techniques. The resistance of the TCO layer, which affects the horizontal flow of current through the photoelectrode to the current collector, becomes a significant problem as the device area is increased. Incorporating an interconnect layer into the photoelectrode can alleviate this problem and facilitate the maintenance of cell efficiency with increased cell area.

In the thick film process, the printing capability offers great flexibility in the design of the interconnect layer and the active photoelectrode area. The design of the screen allows patterns to be designed which are not restricted by structural requirements of the mask with resolution only limited by the mesh opening of the screen. This work has demonstrated how patterned electrodes can be produced, together with 3-D contouring of the photoelectrode using the build up of TiO_2 film through repeated depositions. Consequently patterned and textured electrodes can be produced at relatively low cost to improve electrode performance and to enhance the visual appearance of a DSSC product.

The design of the interconnect layer using finite element methods has been demonstrated. Previous work in this area has concentrated on the interdigitated contact structure without a clear definition of how an optimum layout structure can be defined. The finite element analysis allows the voltage distribution across an electrode to be displayed as a voltage contour plot allowing problems with the

electrode design to be more easily identified. This simulation capability can then be coupled with an optimisation technology, such as the genetic algorithm, to search for the best arrangement of the interconnect layer. The cost of implementing such a layer can be balanced against efficiency improvements to determine an optimal design within the constraints of the production technology.

The improvements provided by two interconnection patterns have been demonstrated on laboratory DSSC devices. These results have also been shown to be consistent with the performance predicted by the finite element analysis. However, more work is required in this area to separate out the contribution of the electron path within the TiO_2 mesoporous film to the total internal resistance of the DSSC device. Since this component is controlled by the vertical scaling (cell thickness) rather than the horizontal scaling (cell area) of the device, it is consequently less important than the TCO resistance as the cell area is increased.

The capability to improve the photoelectrode through an interconnection layer also leads to other possible improvements in DSSC design. Light transmission through the TCO material reduces as its resistivity is lowered, thereby reducing the incident light to the active area of the photoelectrode. Incorporating an interconnect layer could enable the use of higher resistivity TCO substrates, since the TCO layer now just needs to handle the local collection of current into the interconnect layer, enabling a better optical performance for the substrate. An interconnect layer could also facilitate the interconnection of individual cells into series connected arrays of DSSC devices. The production of arrays from individual cells is a significant cost for existing photovoltaic technologies. The ability to print individual cells and connect them together through the interconnect layer could be a significant advantage for this technology.

This research has also highlighted some of the production problems for DSSC devices, most notable of which is probably the degradation in the resistivity of the TCO substrate during the high temperature processing steps. However this does also demonstrate the advantage of having an interconnect layer working with the TCO layer. Although FTO material has been shown to be more robust than ITO, further work is clearly required in this area to improve the resilience of the TCO material. The production process could also be improved and optimised during the platinum

catalyst activation and TiO_2 sintering operations to minimise any damage to the TCO material.

This work has shown that the performance of a DSSC device can be improved as it is scaled up in area using an interconnect layer and this improvement can readily be observed in the 'fill factor' of the device. Further work is required to optimise the design of such a patterned photoelectrode and these methods could also be applied to other photovoltaic technologies to improve the current collection across large area devices.

7.2 Future Work

A logical progression of this work would be the development of the interconnect pattern design using the modelling techniques to determine a more efficient geometry. Using a commercial conductive paste for the interconnect layer would allow the design to be tested relatively easily using screens designed with both the TiO_2 and interconnect layer patterns. The work performed suggests that a more efficient interconnect layer can be designed using interconnect patterns which occupy less area than the interdigitated and grid designs tested.

The modelling techniques for electrode resistance can also be extended to include the path through the mesoporous TiO_2 structure for the photoelectrode. Although this resistance path is not so important for the scaling of the device in area, it clearly should be minimised to improve cell performance. The literature already contains significant work in this area and such a modelling capability could be used to more accurately determine the optimum thickness of the TiO_2 layer.

The susceptibility of the TCO substrate to damage during high temperature processing warrants further work. Although FTO material provides improvement over ITO material, it also exhibits resistivity change during these processes. The use of barrier layers with the TCO material may provide some advantage. Although barrier layers are often used on the glass side of the TCO layer, the use of an appropriate barrier layer at the interface with the TiO_2 film could offer a performance improvement. Clearly the barrier layer at this interface has critical requirements since

apart from protecting the TCO layer, it also needs to allow a good ohmic connection between the mesoporous TiO_2 structure and the TCO film during the sintering process.

The high temperature processing steps could also be optimised to minimise the damage to the TCO substrate. In addition, these steps represent a significant cost for the DSSC production process in terms of energy and unit price. Both the sintering of the TiO_2 film on the photoelectrode and activation of the platinum catalyst on the counterelectrode are performed at temperatures in excess of 400°C. The platinisation process for the counterelectrode could probably be adapted for lower temperatures relatively easily and this electrode does not actually need to use a TCO substrate unless a translucent DSSC is required.

However the sintering step for the TiO_2 film does need more attention to optimise its duration and temperature and also to improve the efficiency of the sintering process. The inclusion of a sinter flux in the TiO_2 paste could improve the quality of the mesoporous structure obtained and reduce the resistance of this component of the photoelectrode resistance. Other work has investigated the use of lower sinter temperatures primarily for the application of flexible substrates based on plastic materials. The investigation of more efficient temperature profiles for the sintering process based on minimising the thermal stress and therefore cracking in the TiO_2 film, whilst reducing the period at elevated temperatures for the actual sintering operation, could significantly improve this process step.

The thick film production process developed in this work provides a method for the production of laboratory cells with a relatively consistent performance. It provides a platform for the continued development of the cell design and production process for increased efficiency. This development can proceed beyond the original objective of improving the resistance of the photoelectrode component. The thick film production technique is compatible with industrial manufacturing processes which currently exist for the flat panel display market where the production of large area glass panels with an electrolyte seal are already well established. Consequently these techniques offer a viable route to the large scale manufacture of DSSC systems.

APPENDIX 1: LED SOLAR SIMULATOR

The LED solar simulator was designed to provide a compact light source for testing DSSC devices in the laboratory. It was built around a cluster of five LEDs operating at the wavelengths of 470 nm (Kingsbright L-7104QBC-D), 525 nm (Kingsbright L-7104VGC-H), 645 nm (Osram LS3366), 880 nm (Osram SFH487-2) and 950 nm (Sharp GL380). An array of 40 clusters was assembled into an area of 55 mm square and this array was positioned approximately 45 mm above the cell under test with an enclosure shielding extraneous light sources. Each wavelength group of LEDs were connected together through ballast resistors and voltage driven from independent, adjustable voltage supplies. In this way, the output of each wavelength group could be independently adjusted. This arrangement also allowed the LED groups to be independently selected and could also have been extended to provide intensity modulation through additional control of the voltage driver electronic circuitry.

Although the spectral output of the LED source is clearly limited, the literature [A1.1] indicates that despite a very different spectral distribution, even a three colour LED system can provide results which are close to conventional light sources. In the system described in this reference, using LED sources of 470 nm, 700 nm and 940 nm, the systematic error in the measured efficiency of photovoltaic devices by illumination was given as ±1.4%. Other work [A1.2] indicates that this type of arrangement is capable of illuminating the cell under test evenly. An unevenness of illumination of approximately 3% is quoted and this was achieved with a coarser LED spacing than that used in this design. Although the LED simulator was mainly intended for making comparative measurements for DSSC device performance, its spectral output was also tested. The spectral performance of the LED simulator was compared to a xenon lamp based photovoltaic test chamber whose performance is traceable back to a NREL standard test.

The spectral output of the xenon lamp was analysed using the Avantes 204B spectral measurement system and the results are shown in Figure 46 together with those for the LED simulator in Figure 47. In both plots, the relative output is obtained by

normalising readings to the peak output, the output powers being different in the two systems. A silicon photovoltaic device (W39-3f) which has been characterised by the NREL, as shown in Figure 49, was used as a reference to calibrate the xenon lamp based photovoltaic test chamber.

Another silicon photovoltaic device was used to provide a reference which could be used to compare the outputs of the two systems. The Centronic OSD100 silicon photodetector has an active area of 100 mm^2 and the output power obtained with both illumination sources is shown in Figure 48.

The W39-3f silicon photodetector used for the calibration of the xenon light source had a maximum power output in the NREL test of 7.1 mW/cm^2 whereas the OSD100 had a maximum power output under illumination from the xenon lamp source of 8.85 mW/cm^2. Under illumination from the LED solar simulator, the OSD100 had a maximum power output of 1.93 mW/cm^2, this corresponds to an irradiance level of around 218 W/m^2 for the LED solar simulator.

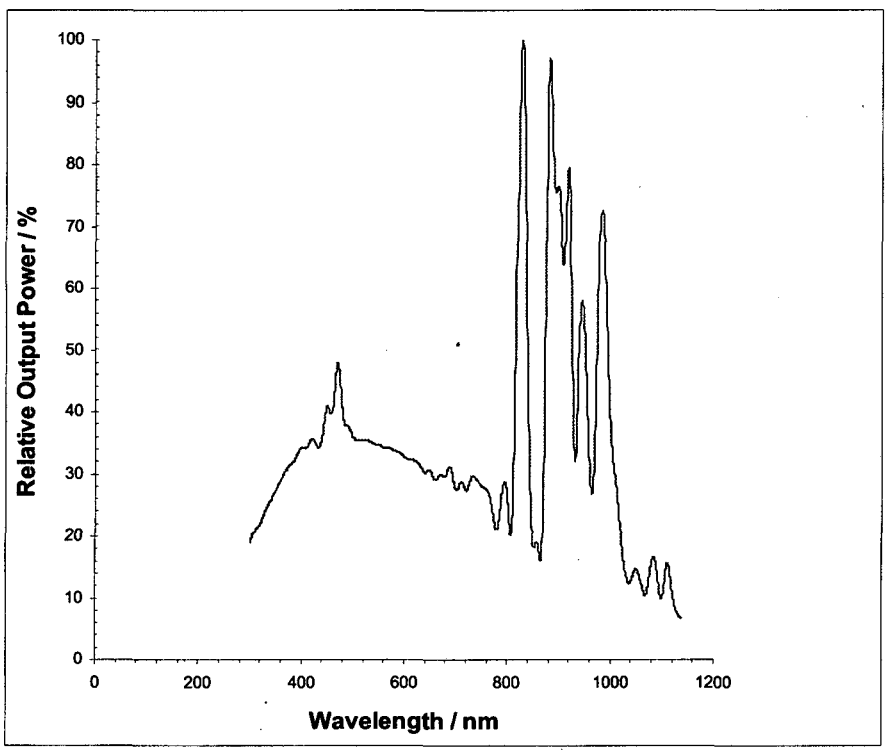


Figure 46: Relative spectral output of the xenon lamp solar simulator measured using the Avantes 204B spectral measurement system.

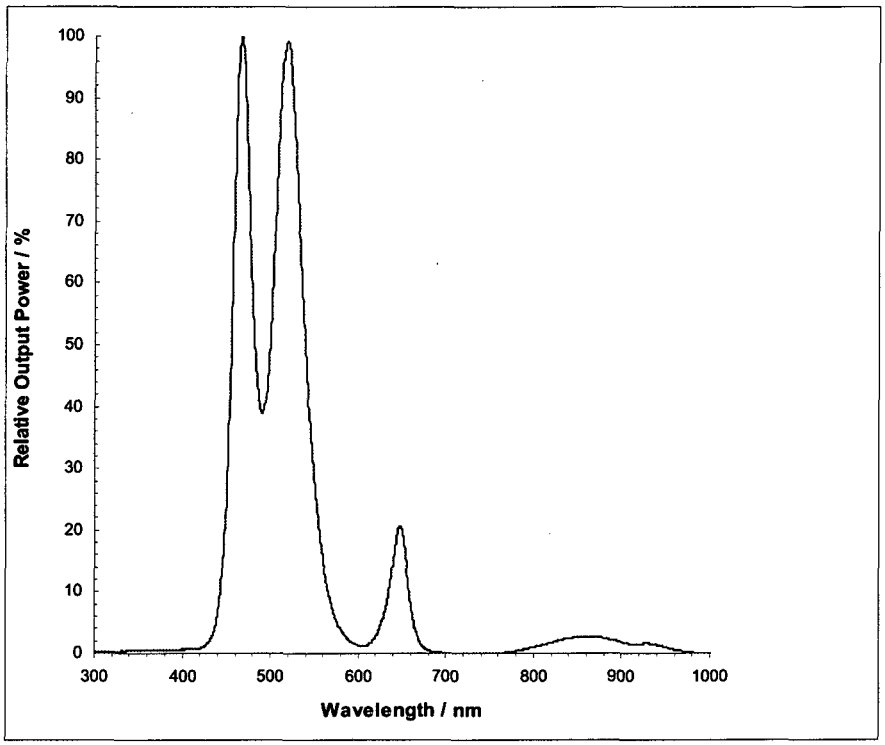


Figure 47: Relative spectral output of the LED solar simulator measured using the Avantes 204B spectral measurement system.

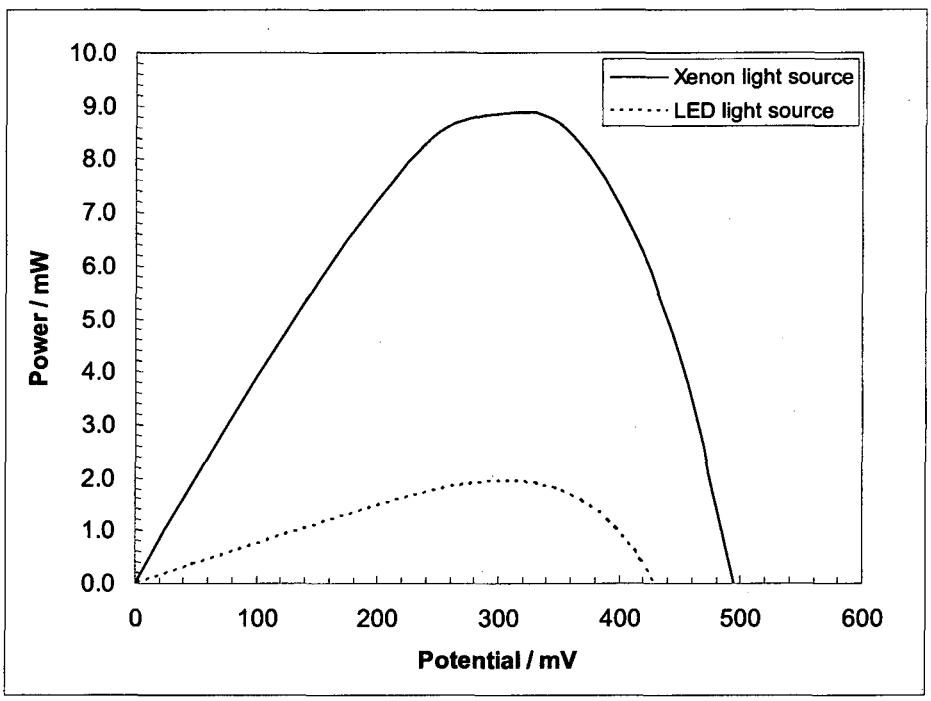


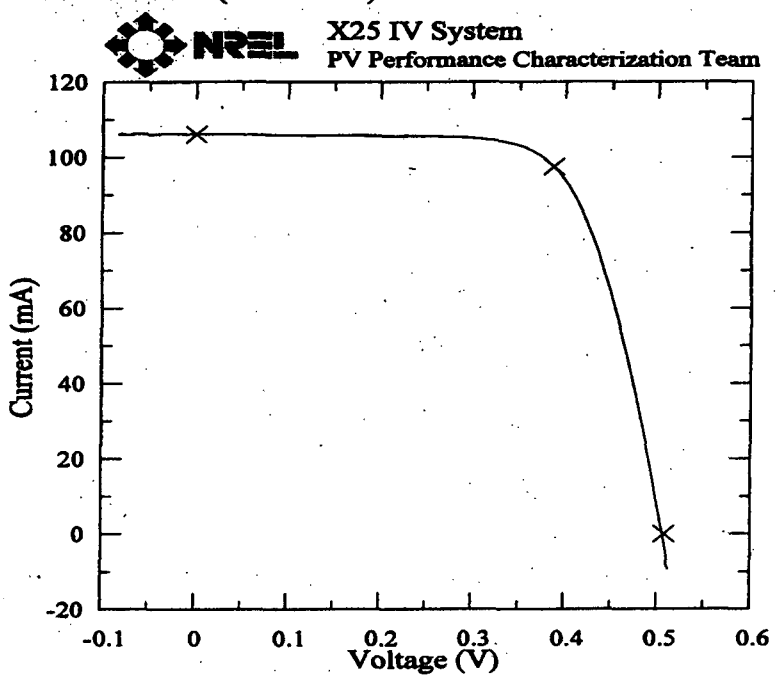
Figure 48: Power vs Voltage for the OSD100 photodetector under illumination from the xenon and LED light sources.

University of Southampton (UK)

mono-Si Cell

Device ID: W39-3f
May 17, 2005 14:44
Spectrum: AM1.5-G (IEC 60904)

Device Temperature: 25.0 ± 1.0 °C
Device Area: 5.306 cm^2
Irradiance: 1000.0 W/m^2



V_{oc} = 0.5079 V
I_{sc} = 0.1061 A
J_{sc} = 19.991 mA/cm^2
Fill Factor = 69.98 %

I_{max} = 97.406 mA
V_{max} = 0.3871 V
P_{max} = 37.703 mW
Efficiency = 7.11 %

Figure 49: Test certificate for the silicon photovoltaic device used as a reference to calibrate the xenon lamp based photovoltaic test chamber.

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GLOSSARY OF TERMS

DSSC -- Dye Sensitised Solar Cell

FEM -- Finite Element Methods

FTO -- Flourine doped Tin Oxide

Impp – Maximum Power Point Operating Current

Isc -- Short Circuit Current

ITO -- Indium Tin Oxide

kWh -- kilowatt hour

LED -- Light Emitting Diode

NC -- Nanocrystalline

NREL – National Renewable Energy Laboratory

PV – Photovoltaic

SEM – Scanning Electron Microscope

TCO -- Transparent Conductive Oxide

Vmpp -- Maximum Power Point Operating Voltage

Voc -- Open Circuit Voltage

VSI -- Vertical Scanning Interferometry