UNIVERSITY OF SOUTHAMPTON

Advanced Characterisation and Modelling of SiGe HBT's

Yue Teng, Tang

A thesis submitted for the degree of

Doctor of Philosophy

Department of Electronics and Computer Science

Faculty of Engineering and Applied Science

May 2000

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING AND APPLIED SCIENCE

DEPARTMENT OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

ADVANCED CHARACTERISATION AND MODELLING OF SIGE HBT's

by Yue Teng, Tang

This thesis investigates advanced characterisation and modelling techniques for silicon-germanium heterojunction bipolar transistor (SiGe HBT's). Two characterisation techniques are proposed and evaluated to enable, as much as is possible, direct electrical extraction of physical device characteristics which are unique to SiGe HBT's, as opposed to standard silicon-only bipolar transistors. Principal objectives motivating the new characterisation techniques are the elimination of silicon control devices and the use of widely available measurement apparatus.

A new electrical method for extracting the bandgap difference across the neutral base of a SiGe HBT is proposed. The method is able to extract the bandgap difference across the neutral base without the need of time consuming and expensive characterisation tools such as SIMS. Also, it does not require detailed modelling of the SiGe HBT, such as bandgap narrowing effect. The accuracy of the method is assessed. Numerical simulations and measurement results proved that the proposed method could achieve its predicted function.

The bandgap difference across the neutral base extraction method is further developed for extracting the parasitic potential barrier height in a SiGe HBT. The proposed method is shown to be able to extract the parasitic potential barrier heights at the emitter-base and collector-base junctions of SiGe HBT's simultaneously in conjunction with numerical space-charge layer modelling using doping secondary-ion-mass spectroscopy (SIMS) profile data. It provides a more direct measure of parasitic barrier-related quantities and does not depend upon a detailed knowledge of the temperature dependence of SiGe density of states functions, carrier mobility, etc.. Numerical simulations and measurement results show that the method gives useful and representative values regarding the parasitic potential barrier height.

Finally, the potential of a proposed novel lateral SiGe HBT structure for high performance rf/microwave applications is assessed. Various issues regarding the lateral structure, including base definition and base contact, are discussed. Compared to a state-of-the art vertical SiGe HBT structure, the lateral structure is found to have many advantages for low power rf/microwave applications. A realistic comparison is carried out by means of full 2-D numerical simulation. Numerical simulation results indicate that a lateral SiGe HBT structure can potentially out-perform a vertical structure in term of low power and high frequency performance.

Contents

List of Figures

Acknowledgement

First of all, I thank my Lord Jesus Christ for making all this possible for me.

I would like to thank my family for their trust, support and patience with me for the last 3 years.

A special acknowledgement must go to my supervisor Dr. John Hamel for his valuable guidance and support in every part of this work. His enthusiasm and readiness to help is something I will always appreciate.

Thanks must also go to Prof. Peter Ashburn for providing the SiGe HBT devices for this work.

I will like to express my gratitude to all my fellow researchers in the microelectronic group for their friendliness and many football games. It is good fun to work in a relaxing environment. Many thanks to all the clean room staff for their help and advice. And the microelectronics group secretaries, nothing will go smoothly without you all.

Finally, my brothers and sisters in church, your support and prayers kept me going. Thank you very much.

Yue Teng, Tang

List of Symbols

0_f	Emitter side of neutral base in forward active mode
0_r	Emitter side of neutral base in reverse active mode
A_c	Collector-base junction area
A_e	Emitter-base junction area
β	Common emitter current gain
β_{ac}	a.c. common emitter current gain
BV_{CEO}	Breakdown voltage between the emitter and collector with base open circuit
C_π	Collector-base capacitance in small-signal hybrid-π model
C_{cs}	Collector-substrate capacitance
C_{jc}	Collector-base depletion capacitance
C_{je}	Emitter-base depletion capacitance
D_n	Electron diffusion coefficient
D_{nb}	Electron diffusion coefficient in base
ϵ	Dielectric permitivity
ϵ_s	Permitivity of silicon
E_c	Conduction band energy
ΔE_c	Parasitic potential barrier height
δE_c	Conduction band discontinuity
E_g	Bandgap energy
ΔE_g	Bandgap narrowing
$\Delta E_g(grade)$	Bandgap grading across the neutral base
ΔE_g^{app}	Apparent bandgap narrowing due to heavy doping effect
ΔE_g^{e-b}	Bandgap difference between emitter and base
E_F	Fermi level
E_{Fn}	Electron quasi-fermi level
E_{Fp}	Hole quasi-fermi level
E_v	Valence band energy
ΔE_v	Valence band variation across a parasitic potential barrier width
δE_v	Valence band discontinuity
f_{max}	Unity power gain frequency
f_T	Cut-off frequency
f_T^{max}	Peak cut-off frequency
g_m	Transconductance
g_{of}	Output conductance in forward active mode
g_{or}	Output conductance in reverse active mode

G_b Base Gummel number
G_n Electron generation rate
G_p Hole generation rate

h Planck's constant
h_{FE} Common emitter current gain

I_b Base current
I_c Collector current
I_{cf} Collector current in forward active mode
I_{cr} Collector current in reverse active mode

J_c Collector current density
J_n Electron current density
J_p Hole current density

k Boltzmann's constant

μ_n Electron mobility
μ_p Hole mobility
m_e Electron effective mass
m_h Hole effective mass

n Electron concentration
n_{ib} Effective intrinsic carrier concentration in base
n_{ie} Effective intrinsic carrier concentration
n_{io} Intrinsic carrier concentration
n_p Electron concentration in p-type
N_b Base doping concentration
N_c Effective density of states in the conduction band
N_e Emitter doping concentration
N_v Effective density of states in the valence band
N_A Acceptor concentration
N_D Donor concentration

ρ_s Surface charge density
p Hole concentration

q Charge of an electron
Q_b Total stored charge in base

r_π Effective input resistance in small-signal hybrid-π model
r_{bb} Base resistance in small-signal hybrid-π model
r_{cc} Collector resistance in small-signal hybrid-π model
r_{ee} Emitter resistance in small-signal hybrid-π model

R_b	Base resistance
R_c	Collector resistance
R_e	Emitter resistance
R_n	Electron recombination rate
R_p	Hole recombination rate
τ_b	Base transit time
τ_c'	Collector charging time
τ_{cbd}	Collector-base depletion region transit time
τ_e	Emitter delay
τ_{ebd}	Emitter-base depletion region delay
τ_{ec}	Total delay across the bipolar transistor from emitter to collector
τ_{je}	Total emitter depletion layer charging time
τ_n	Electron lifetime
τ_p	Hole lifetime
T	Absolute temperature
ϕ_c	Potential increase in depletion region in hybrid mode bipolar
ψ	Electrostatic potential
Ψ_n	Electron injection barrier
Ψ_p	Hole injection barrier
V_b	Base voltage
V_{bc}^r	Base-collector voltage at reverse active mode
V_{be}	Base-emitter voltage
V_{be}^f	Base-emitter voltage at forward active mode
V_{bi}	Build in voltage
V_c	Collector voltage
V_{cb}	Collector-base voltage
V_{cb}^f	Collector-base voltage at forward active mode
V_{dd}	Power supply voltage
V_{eb}^r	Emitter-base voltage at reverse active mode
v_{scl}	Scattering limited velocity
V_A	Early voltage
V_T	Thermal voltage
W	Width
W_b	Neutral base width
ΔW_b	Parasitic potential barrier width
W_f	Collector side of neutral base for forward active mode
W_{jc}	Collector-base depletion layer width
W_{je}	Emitter-base depletion layer width
W_r	Emitter side of neutral base for reverse active mode

Chapter 1

Introduction

The studies into Heterojunction Bipolar transistor (HBT) technology have been intensified enormously for the past 10 years as homojunction technology (mainly silicon) is moving closer to the predicted limit of its capability. It has attracted much attention because of both the device performance and the low cost for many applications such as over 10-Gb/s optical communication systems, LAN, and wireless communication system [1]. Advancement in silicon germanium (SiGe) technology, demonstrated by producing various high performance devices, has proved that SiGe HBT has the potential to be the future silicon-based bipolar technology, taking over from the currently dominant silicon technology. Schuppen *et al.* [2] have fabricated double-mesa type SiGe heterojunction bipolar transistors using MBE where it is possible to obtain a record maximum frequency of oscillation up to 160 GHz for a 2-emitter finger HBT in common emitter configuration. By employing Ultra High Vacuum/Chemical Vapour Deposition (UHV/CVD) system, Oda *et al.* [3] have achieved cut-off frequency up to 130 GHz and current gain up to 29,000 with graded and uniform germanium profiles, respectively. For IC applications, Strohm *et al.* [4] have fabricated a SiGe MMIC amplifier delivering gain up to 4 dB at 26 GHz. In fact, SiGe HBTs were successfully implemented in a 16 Gb/s multiplexer IC [5] and also in ICs (including selector, multiplier, D flip-flop) for a 20 Gb/s optical transmitter [6]. For analogue applications, Harame *et al.* [7] have fabricated a 12-bit D/A converter with SiGe HBT devices in an 8 inch wafer manufacturing line. Also, beta-Early voltage product (βV_A), a key property for analogue devices which measures the quality of the current source, of an

impressive 48,000 was reported in [1] for SiGe transistor. Referring to [1], the SiGe heterojunction transistor is fast enough to replace gallium arsenide in many commercial applications, including digital cellular telephones and wireless LANs. Most importantly, it can be made, with modest increase in processing complexity, on existing process lines. Also, it may be integrated with conventional circuits such as sub-micron VLSI CMOS to form SiGe HBT Bipolar/BiCMOS process. SiGe HBT Bipolar/BiCMOS technology has a unique opportunity in the wireless marketplace because it can provide the performance of III-V HBTs and the integration/cost benefits of silicon bipolar/BiCMOS [7, 8].

The introduction of germanium into the base of silicon bipolar transistor, thereby forming a strained SiGe layer, alters the physical properties of the transistor and enhances the performance of the bipolar transistor tremendously. Germanium has smaller bandgap compared to silicon, thereby reduces the base bandgap in a SiGe base. By using strained SiGe layer in the base to induce bandgap narrowing, heterojunctions are formed at the collector-base junction and the emitter-base junction of the transistor. The reduction of base bandgap results in the lowering of the electron injection barrier from emitter into base. This increases electron injection into base and therefore causes the increase of collector current and hence current gain. As current gain increases, higher base doping can be used without destroying the current gain. High base doping allows the use of thinner base to reduce the forward transit time without compromising the base resistance or fearing that the base will be 'punched through' by depletion region penetration across the base, due to a reverse collector-base bias. It also increases the device output resistance by allowing less depletion region penetration per unit of collector-base applied voltage. Reducing forward transit time improves the high frequency performance of device by increasing the cut-off frequency. Therefore, it is possible to engineer the base bandgap according to the purpose of the transistor. This is known as bandgap engineering where the base bandgap can be adjusted according to the germanium profile and the amount of germanium introduced.

One popular method of base bandgap engineering is to grade the bandgap across the base [8]-[12]. Bandgap grading introduced into the base region of a SiGe HBT

induces a drift field which aids minority carrier transport by accelerating the injected minority carriers as they traverse the base, resulting in lower base transit time. In short, the base bandgap of SiGe HBT can be engineered to enhance device performance, thereby making it suitable for a wide range of high-speed analogue and RF applications.

As device modelling is an essential part of device or circuit designing, it is necessary for new parameters which characterise the behaviour of SiGe HBT to be extracted in order to be included in the physical model. In Chapter 4 of this thesis, a new electrical method is developed to measure the bandgap difference across the neutral base of a SiGe HBT. The base bandgap profile controls the flow of minority carriers and the difference of bandgap across the neutral base determines several other important properties of the transistor including output conductance and base transit time. However, determining the actual bandgap difference across the neutral base can be a complicated matter because, other than the effect of germanium, the base bandgap is also affected by other physical properties such as heavy doping effect. There is no currently existing electrical method that directly measures the bandgap difference across the neutral base. Useful information regarding the impact of germanium on device performance in a SiGe HBT is obtained [13, 14] through comparison with a silicon device that does not contain germanium. However, these methods require the processing of a separate set of silicon devices that have similar doping profile as the SiGe devices. Also, they rely on physical information of silicon and SiGe such as mobility, effective masses and so on. Physical information regarding SiGe is not currently well established and therefore is not always easily available. The proposed new method does not require a silicon control device or rely upon physical information of silicon and SiGe. Using this proposed new method, only the resultant bandgap difference across the neutral base is measured directly from the transistor. Therefore it gives an accurate measurement of the actual bandgap difference across the neutral base inside the transistor. This new method was verified numerically and demonstrated experimentally, and was published in the 1997 Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications [15]. It has been accepted for publication by the Journal of IEEE Transactions on Electron Devices [16].

In Chapter 5, a new electrical method for extraction of parasitic potential barrier heights of SiGe HBT's is presented. Parasitic energy barriers, which do not generally exist in homojunction silicon bipolar transistor, are found to exist in SiGe HBT [17]-[19], if boron is allowed to out-diffuse beyond the SiGe layer boundaries during fabrication of a double heterojunction SiGe HBT. As a result, boron dopant, which defines the transistor's base, is found in the adjacent collector and emitter silicon regions. Since silicon has larger bandgap than SiGe, the bandgap near the edges of the neutral base widens up. This bandgap widening manifests itself as a parasitic energy barrier at both the emitter-base and collector-base junctions. These barriers can have an adverse effect on the SiGe HBT performance. Slotboom *et al.* [20] have shown that the barriers can severely degrade the collector current and cut-off frequency of the device. One way to estimate these parasitic barrier heights has been proposed by Le Tron *et al.* [21] through analysing the temperature dependence of the collector current. This method relies on accurate modelling of the temperature dependence of the silicon and SiGe density of states and carrier mobility. It also requires a control device, a SiGe HBT device (without any parasitic barriers). It requires the same doping profile as the SiGe HBT with parasitic barriers. Here, as shown in Chapter 5, the Le Tron *et al.* method is refined by using the temperature dependence of the ratio of the small signal a.c. output conductance in forward and reverse active operation. This new method is able to simultaneously extract the parasitic potential barrier heights at emitter-base and collector-base junctions of a SiGe HBT. The method is capable of independently determining the height of each barrier without the need for comparison to control devices or a knowledge of the temperature dependence of internal physical properties such as the density of states and carrier mobility. This new method was verified numerically and demonstrated experimentally, and was published in the 28th European Solid-State Device Research Conference [22]. It is to be submitted to the Journal of IEEE Transactions on Electron Devices [23].

Most existing high speed and low power bipolar transistors , suitable for a wide range of high speed analogue and RF applications, make use of the vertical bipolar structure [2, 10, 12]. A narrow base, which is essential for high speed SiGe HBT, can

be grown epitaxially in a vertical bipolar structure using UHV/CVD or Molecular Beam Epitaxy (MBE) [3], [24]-[27]. Especially the approaches using selective epitaxy of the base have proven successful since a record cut-off frequency of $130GHz$ [3], f_{max} of 107 GHz and ECL gate delay of 6.7 ps [28], and CML gate delay of $11ps$ [26] were achieved with this approach. However, the basic vertical structure has some weaknesses. Its main disadvantage lies on the fact that its whole structural alignment (emitter-base-collector) is buried vertically into the silicon substrate. This means that only the emitter can be conveniently contacted from the silicon surface. Self-aligned polysilicon contact and highly doped epitaxial buried layer are therefore required in order to connect the base and collector, respectively, from the silicon surface. This increases the device terminal resistances and capacitances significantly. In many instances, extra processing steps need to be implemented in order to reduce these resistances and capacitances.

The advancement of photolithography process has created an upsurge of interest in lateral bipolar transistors [29]-[31]. Deep sub-micron lithography processes have made possible the production of a thin lateral base down to approximately 0.1 μm. Before this, lateral bipolar transistors have always been handicapped by a wide base structure. With a thin base, high speed lateral bipolar transistors can be realised. In comparison to a vertical structure, the base lateral structure has the advantage of easy accessibility to the base and collector regions from the silicon surface as its emitter-base-collector are aligned parallel to the silicon surface. Also it is more compatible with existing Thin Film Silicon-on Insulator (TFSOI) CMOS technology where epi thickness is about 0.1 μm [32]. Therefore, it becomes a strong candidate for integrated Bipolar CMOS (BiCMOS) process [32], which is highly versatile and especially suitable for low power, low noise and high performance analogue circuits such as RF amplifiers, filters and mixers in wireless communication systems. In Chapter 3, various issues regarding lateral bipolar structures are discussed. The discussion is focused on evaluating the potential of the lateral SiGe device structure for high speed and low power applications. A new mode of lateral bipolar transistor operation, known as the hybrid mode [33], is also discussed. If the hybrid lateral bipolar transistor is designed correctly, it is able to induce virtual heterojunction

effect on the lateral bipolar transistor. Finally, in Chapter 6, since there does not appear to have been a published working lateral SiGe HBT where the emitter, base and collector form a true lateral double heterojunction structure, a novel lateral SiGe HBT structure, meant for high speed and low power applications, is presented. This device is compared to a state of the art, ultra low power and high speed vertical SiGe HBT transistor [10] by means of full numerical simulations using Atlas [34]. The focus of this chapter is to assess the capability of lateral SiGe HBT transistor in comparison to vertical SiGe HBT transistor for low power high speed RF/microwave performance.

Conclusions and suggested further work for this thesis are in Chapter 7.

Chapter 2

Theory of Heterojunction Bipolar Transistors

2.1 Material Properties of Strained $Si_{1-x}Ge_x$

Heterojunction bipolar transistors were first proposed by Shockley [35] in 1951. Electrically, he found out that if the emitter and base are made of different materials, in which they will have dissimilar bandgaps, it could bring about improvement in transistor gain and emitter delay. Initially, different materials with similar crystal structure and lattice constant, such as AlGaAs and GaAs, were combined together to produce heterojunctions. The idea of having a strained heterostructure was only first realised much later by Kasper *et al.* [36, 37] in early 1970s. They employed the concept of a strained $Si_{1-x}Ge_x$ layer on silicon substrate to produce a heterojunction. The problem is that germanium and silicon have different lattice constants. At room temperature, silicon has a lattice constant of 5.43 A^0 and germanium has a lattice constant of 5.66 A^0, which is 4 % larger, as shown in Figure 2.1(a). When SiGe alloy is deposited on a thick silicon substrate, the resultant lattice mismatches cause strain in the SiGe layer (i.e. pseudomorphic layer) [38], as shown in Figure 2.1(b). Therefore, a strained SiGe layer will have lattice constant somewhere in between silicon and germanium, depending upon the percentage of germanium incorporated. If the strained structure is relaxed, structural defects will occur especially along the Si/SiGe

interface area 2.1(c). This is not desirable as relaxed SiGe has a larger bandgap than strained SiGe layers, and is also likely to reduce process yield.

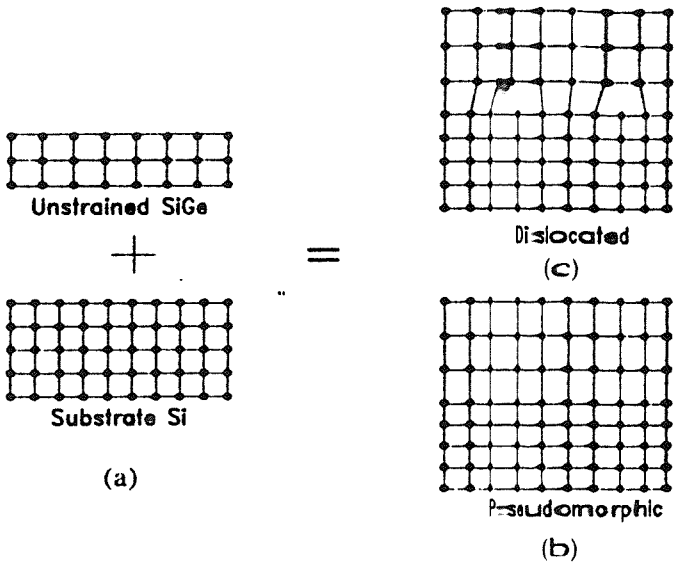

Figure 2.1: 2-Dimensional crystal structure representations [38] of (a) growing SiGe alloy on silicon substrate forming (b) pseudomorphic growth with the lattice constant difference accommodated by tetragonal strain or (c) structural dislocations or defects.

Molecular Beam Epitaxy (MBE) [17, 39] and Ultra High Vacuum/Chemical Vapour Deposition (UHV/CVD) [8, 24] techniques are used to grow strained SiGe layers on silicon substrates. It is possible to grow a strained SiGe layer because the lattice constant of the SiGe during growth is determined by the silicon substrate, shown in Figure 2.1(b). There is a critical thickness for the strained SiGe layer above which the layer will relax resulting in defect formation. This is because as the strained SiGe layer thickness increases, the strain at the Si/SiGe interface will increase as well. The critical thickness is the maximum thickness of the strained SiGe before relaxation. Figure 2.2 shows a plot of the critical thickness versus germanium produced by Hull *et al.* [40]. Here two types of critical thickness are presented. One is the critical thickness of SiGe with a silicon capping layer on top and the other is the critical thickness of SiGe without a capping layer. SiGe with capping layer, which is the silicon emitter layer in a SiGe HBT's [2, 3, 8], is found to have about twice the critical thickness of an uncapped SiGe.

The improvements brought about by SiGe heterojunctions to SiGe Heterojunction

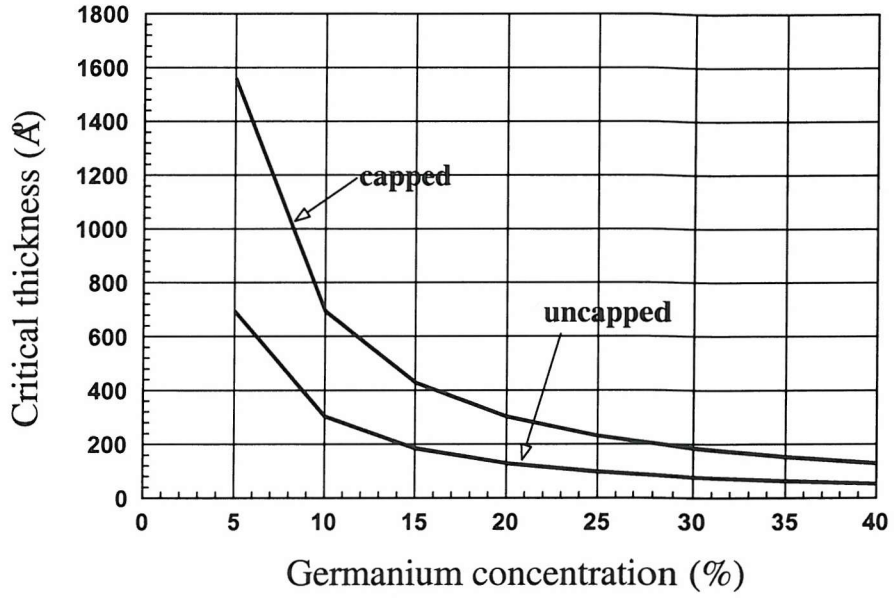

Figure 2.2: Plot showing the critical thickness versus germanium concentration of a strained SiGe layer with and without silicon capping [41, 40].

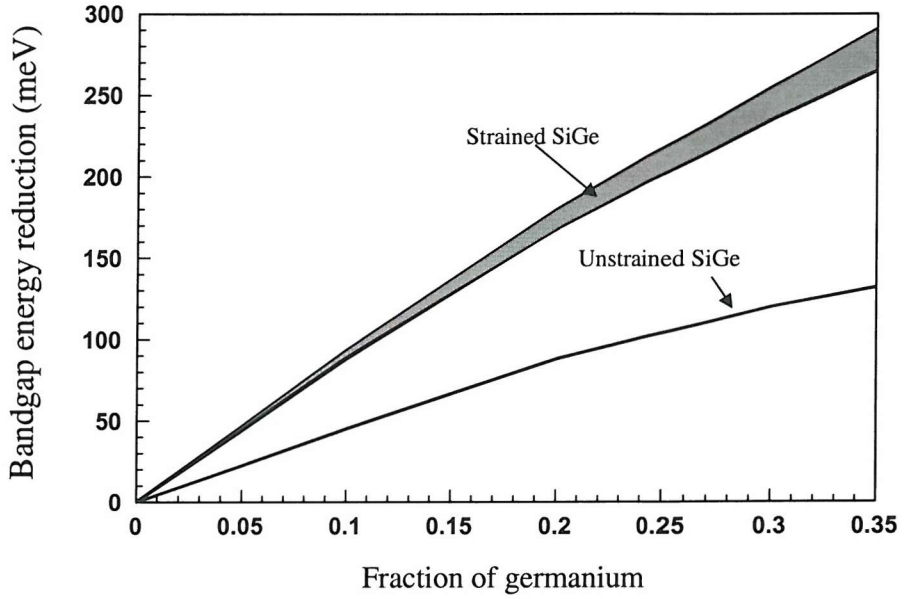

Figure 2.3: Plot of bandgap reduction due to germanium for strained SiGe layer (after [42]) and unstrained SiGe layer (after [43]) at temperature $90K$.

Bipolar Transistor's (HBT's) are mainly related to the bandgap reduction of the SiGe layer compared to silicon in the base region. SiGe has a smaller bandgap generally because it has a larger lattice constant [38]. Strained SiGe has a smaller bandgap compared to unstrained SiGe because the strain causes valence and conduction band splitting [44]. This results in a smaller bandgap. Figure 2.3 shows how the bandgap reduction varies with germanium concentration, at temperature $90K$, for strained SiGe [42] and unstrained SiGe [43].

2.1.1 Bandgap Narrowing Due to Heavy Doping Effects

Besides germanium incorporation, bandgap narrowing can also be induced by heavy impurity doping [45, 46]. For lowly doped semiconductors (i.e. less than $5\times10^{17}\ cm^{-3}$ in silicon), the dopant atoms are sufficiently spaced from each other in the semiconductor lattice that the wave functions associated with the dopant atom electrons do not overlap. Therefore the energy levels of the dopant atoms are discrete. Also, it can be assumed that the sufficiently spaced dopant atoms have no effect on the perfect periodicity of the semiconductor lattice. In this case, the edges of the conduction and valence bands are sharply defined, shown in Figure 2.4.

However, in heavily doped semiconductors (i.e. more than $5\times10^{17}\ cm^{-3}$ in silicon), dopant atoms are close enough to affect their dopant atom electron wave functions. This results in impurity level splitting where an impurity band begins to form within the bandgap. Also, the perfect periodicity of the semiconductor lattice will be disrupted and causes a band tail to form near the band edge. The result of all these effects is that the effective bandgap between the conduction and valence band is reduced, as shown in Figure 2.4. This accounted for electrically by using the term 'apparent bandgap narrowing', ΔE_g^{app}. Figure 2.5 shows the amount of bandgap narrowing with increased impurity doping for three different germanium concentrations (0%, 10%, 20%). The results are obtained from Poortmans *et al.* [45], and as can be seen, strained SiGe has a high apparent bandgap narrowing compared to silicon for similar doping. Bandgap narrowing also increases for increasing germanium concentration.

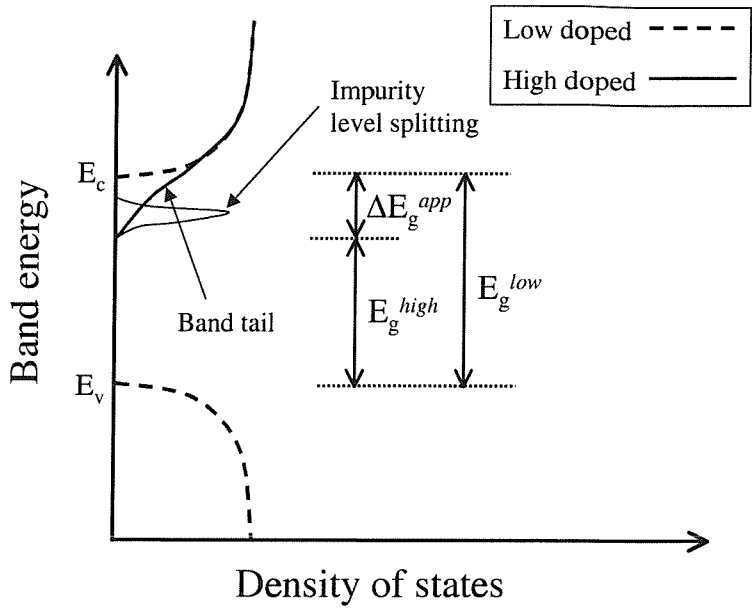

Figure 2.4: Figure illustrating the heavy doping effect on the bandgap of n-type silicon [46]. E_g^{high} is the resultant bandgap due to heavy doping effect and E_g^{low} is the bandgap without heavy doping effect. ΔE_g^{app} is the apparent bandgap narrowing due to heavy doping effect.

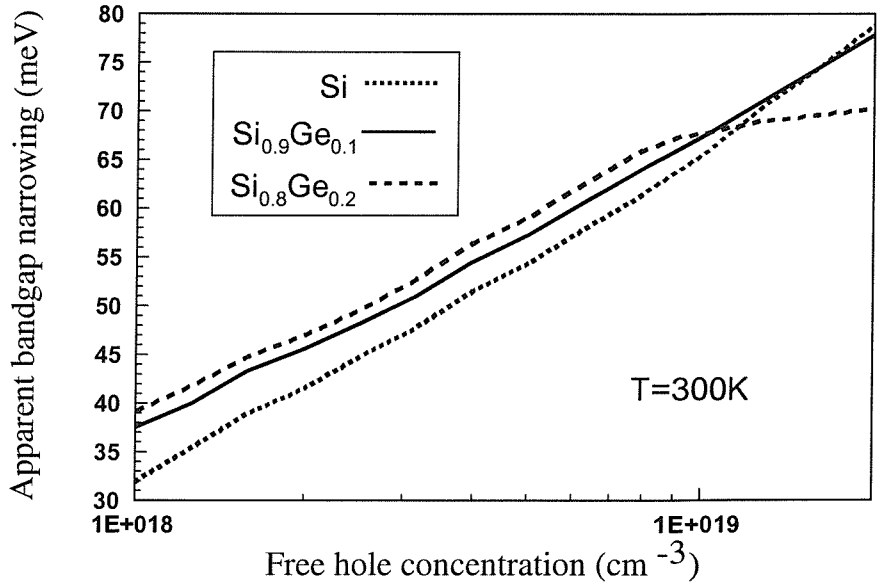

Figure 2.5: Apparent bandgap narrowing due to heavy doping effects for three different germanium concentrations (0%, 10%, 20%) at a temperature of 300K [45].

2.1.2 SiGe Growth using UHV/CVD

Chemical vapour deposition (CVD) is a technique used to grow layers of semiconductor material on an existing substrate (or wafer). It depends on chemical reactions that take place on the substrate surface between different gases inside a growth chamber. The most mature strained SiGe growth method to date for SiGe HBT device and circuit fabrication is ultra-high vacuum/chemical vapour deposition (UHV/CVD) with progress culminating in wafer scale BiCMOS integration [47] in 1992. UHV/CVD of SiGe was first reported by Meyerson in 1986 [48] and it combines the extremely clean growth ambient of UHV techniques with the growth chemistry and batch throughput capability of CVD. Using a turbomolecular pump backed by a rotary pump, clean growth ambient is produced, with oxygen and carbon levels down to 10^{-11} Torr partial pressure. This enables high purity epitaxial growth at low temperature (i.e. below 600^0C). As mentioned above, low temperature processes are vital for strained SiGe because high temperatures may cause it to relax. The cross section schematic of a typical UHV/CVD reactor is shown in Figure 2.6. Before loading wafers into

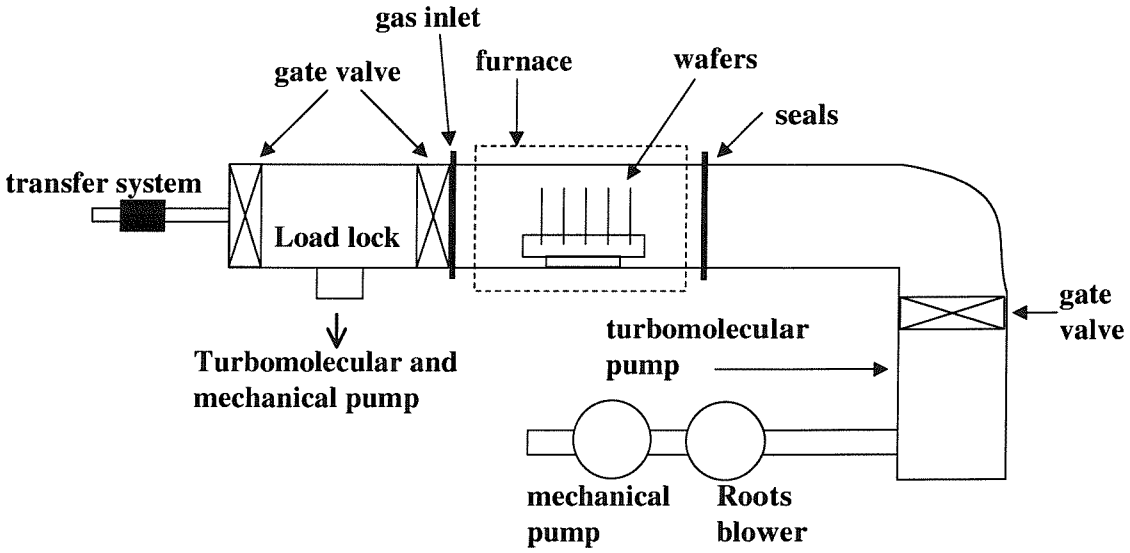

Figure 2.6: Schematic diagram of a UHV/CVD reactor (after Meyerson [8, 50]).

the growth chamber, UHV/CVD relies on hydrogen passivation as a low temperature surface preparation for epitaxy. This is carried out as a simple dip etch for 10-15 seconds in dilute 10:1 H_2O/HF [49]. The resultant hydrogen terminated surface is

able to provide hydrogen termination stable in air for the length of time required to load the wafers into the reactor. Since hydrogen will desorb at about 500^0C, no high temperature desorption step, such as those performed on oxide desorption at $1150 - 1200^0C$ is needed. Wafers are first loaded into the reactor through the load lock, as shown in Figure 2.6, which minimises transfer of contaminants to the growth chamber. The growth temperature is in the range of 400^0 to 500^0C at growth pressures of $1 \times 10^{-3} mbarr$ and the gaseous sources are silane, germane, diborane, and phosphine used to grow in-situ doped SiGe. Film growth rates are typically 0.4-4nm/minute [8] with dimensional control down to the order of 1-2 atomic layers. This enables very good dopant concentration profile control.

P-type doping of $5 \times 10^{21} cm^{-3}$ for boron [51] and n-type doping of $5 \times 10^{18} cm^{-3}$ for phosphorous [52] are reported. UHV/CVD has the advantages of good doping and thickness uniformity, and precise control of doping and germanium profile. Harame *et al.* [8] have reported routine SiGe deposition over small dimensions for graded germanium profiles with run to run and wafer to wafer uniformity and reproducibility at the level of 5% to 1%, respectively. However, UHV/CVD process can be costly because of the UHV equipment involved. Also, for it to be integrated into a technology, it needs to meet all the technology requirements simultaneously such a low thermal budget, good patterned wafer handling, reproducibility, uniformity, reliability and good growth control.

2.2 Electrical Properties of $Si/Si_{1-x}Ge_x/Si$ HBT's

Figure 2.7 shows how the base bandgap changes are brought about by the incorporation of germanium into the base. For the purpose of comparison, it is assumed that both the silicon bipolar and SiGe HBT are similar other than the fact that germanium is present in the SiGe HBT's. In thermal equilibrium, the Fermi level, E_F, is constant across the junction. Therefore, for an abrupt Si/SiGe interface, the difference in bandgap between the emitter and base causes discontinuities to exist at the conduction and valence band, shown in Figure 2.7 as δE_c and δE_v, respectively. Also, the total discontinuity, $\delta E_c + \delta E_v$, is equal to the base bandgap difference between

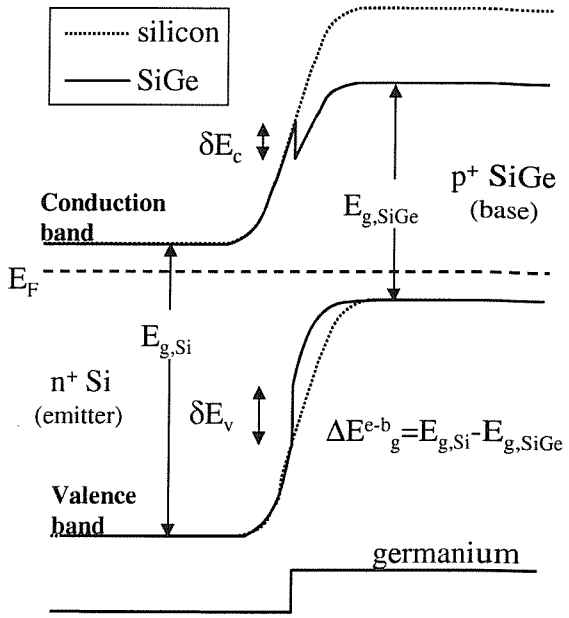

Figure 2.7: Figure illustrating the effect of SiGe strained layer on the bandgap of emitter-base junction for an abrupt Si/SiGe interface.

silicon emitter and SiGe base, ΔE_g^{e-b}. The valence band discontinuity, δE_v, tends to be a considerably larger than the conduction band discontinuity, δE_c.

2.2.1 Collector Current and Current Gain

Figure 2.8 shows the band diagram of a graded SiGe HBT's in forward active mode. Its germanium concentration is graded linearly across the base, increasing from emitter towards the collector. With the presence of germanium, the electron injection barrier from emitter to base, Ψ_n, is reduced and there will be greater electron injection from emitter to base. This means increase in collector current. However, the hole injection barrier from base to emitter, Ψ_p, remains the same as in a silicon bipolar transistor. Therefore, the hole current from base to emitter, which is the main contributor to base current, remains the same. Hence silicon bipolar transistors and SiGe HBT's tend to have approximately the same base current.

The following derivations are used to show enhancements resulting from germanium incorporation which closely follow derivations contained in [8]. The collector current of a graded SiGe HBT can be obtained by altering the collector current equation of a silicon bipolar transistor. Assuming uniform base doping for the device, the silicon bipolar collector current, $J_{c,Si}$, for uniformly doped base can be written using

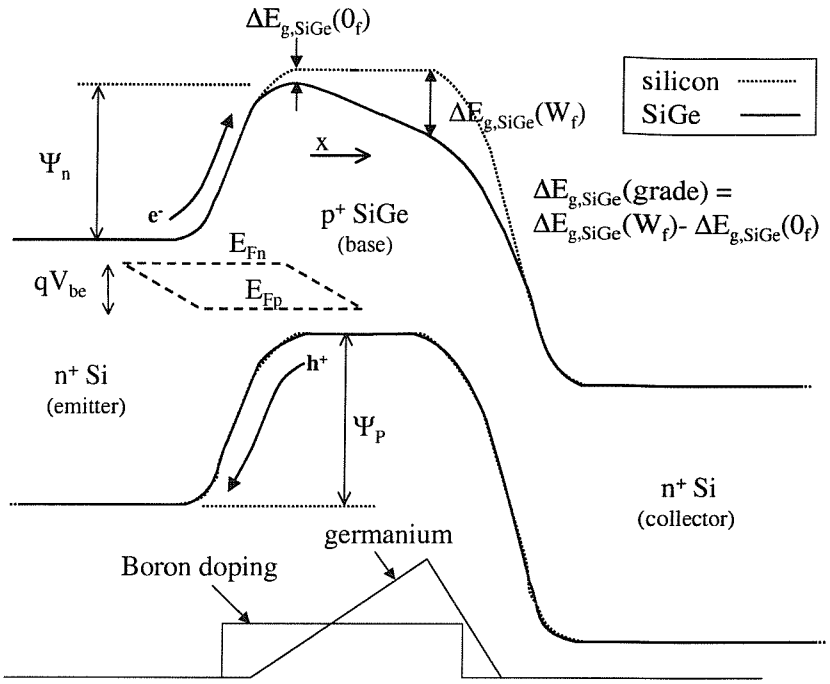

Figure 2.8: Bandgap energy diagram across a graded SiGe HBT in forward active mode of operation. 0_f and W_f are the electrical boundaries of the neutral base region on the emitter and collector sides of the base, respectively.

the Moll-Ross relation [53]:

$$J_{c,Si} = q(\exp(qV_{be}/kT) - 1) \times \left[\int_{0_f}^{W_f} \frac{N_b(x)dx}{D_{nb}(x)n_{ie}^2(x)}\right]^{-1} \quad (2.1)$$

$$= \frac{qD_{nb}n_{io}^2}{W_bN_b} \times \exp\left(\frac{\Delta E_{gb}^{app}}{kT}\right) \times \left[\exp\left(\frac{qV_{be}}{kT}\right) - 1\right] \quad (2.2)$$

where q is the charge on a electron, V_{be} is the forward biased base-emitter voltage, k is the Boltzmann's constant, T is temperature, 0_f and W_f are the base electrical junction positions at the emitter and collector side of the neutral base, in forward active mode, W_b is the neutral base width, $N_b(x)$ is the positional dependent base doping concentration, $D_{nb}(x)$ and $n_{ie}(x)$ are the positional dependent base electron diffusion coefficient and effective intrinsic carrier concentration, respectively, D_{nb} is the base electron diffusion coefficient, n_{io} is the intrinsic carrier concentration in the absence of heavy doping effects, N_b is the base doping, and ΔE_{gb}^{app} is the base apparent bandgap narrowing due to heavy doping effect.

In Equation 2.1, $n_{ie}(x)$ accounts for the effective intrinsic carrier concentration across the base and is a function of bandgap. For a graded SiGe HBT, bandgap

changes across the base, as depicted in Figure 2.8, can be accounted for [8],

$$n_{ie}^2(x) = \gamma \times n_{io}^2 \times \exp\left(\frac{\Delta E_{gb}^{app}}{kT} + \frac{\Delta E_{g,SiGe}(grade) \times \frac{x}{W_b}}{kT} + \frac{\Delta E_{g,SiGe}(0_f)}{kT}\right) \quad (2.3)$$

where,

$$\gamma = \frac{(N_c N_v)_{SiGe}}{(N_c N_v)_{Si}} \approx 0.4 \ [20] \qquad \text{and} \qquad W_b = W_f - 0_f \quad (2.4)$$

The term $E_{g,SiGe}(grade)$ represents the bandgap difference across the neutral base, as shown in Figure 2.8. The term $E_{g,SiGe}(0_f)$ represents the base bandgap at the emitter side of the neutral base, N_c and N_v are the density of states in the collector and valence bands, respectively.

Putting Equations 2.1 and 2.3 together and integrating, the graded SiGe HBT collector current, $J_{c,SiGe}$, can be written as [8]:

$$J_{c,SiGe} = \tilde{\eta}\tilde{\gamma}\frac{qD_{nb}n_{io}^2}{W_b N_b} \times \left[\exp\left(\frac{\Delta E_{gb}^{app}}{kT} + \frac{qV_{be}}{kT}\right) - 1\right] \times \frac{\Delta E_{g,SiGe}(grade)}{kT} \times \frac{\exp\left(\frac{\Delta E_{g,SiGe}(0_f)}{kT}\right)}{1 - \exp\left(-\frac{\Delta E_{g,SiGe}(grade)}{kT}\right)} \quad (2.5)$$

where,

$$\eta = \frac{(D_{nb})_{SiGe}}{(D_{nb})_{Si}} > 1 \ [54] \quad (2.6)$$

where the symbol '$\sim$' refers to a position-averaged quantity. The ratio of $(D_{nb})_{SiGe}$ to $(D_{nb})_{Si}$ accounts for the strain enhancement of the minority carrier electron mobility with increasing germanium content [54].

Taking the ratio of $J_{c,SiGe}$ to $J_{c,Si}$, the collector current enhancement due to bandgap engineering can be estimated by,

$$\frac{J_{c,SiGe}}{J_{c,Si}} \simeq \tilde{\eta}\tilde{\gamma}\frac{\Delta E_{g,SiGe}(grade)}{kT} \times \frac{\exp\left(\frac{\Delta E_{g,SiGe}(0_f)}{kT}\right)}{1 - \exp\left(-\frac{\Delta E_{g,SiGe}(grade)}{kT}\right)} \quad (2.7)$$

where,

$$\tilde{\gamma} = 0.4, \quad \tilde{\eta} > 1, \quad \frac{\frac{\Delta E_{g,SiGe}(grade)}{kT}}{1 - \exp\left(-\frac{\Delta E_{g,SiGe}(grade)}{kT}\right)} > 1 \ \text{ and } \ \exp\left(\frac{\Delta E_{g,SiGe}(0_f)}{kT}\right) > 1$$

Even though $\tilde{\gamma}$ is 0.4 [20], $\exp(\Delta E_{g,SiGe}(0_f)/kT)$ increases the SiGe HBT's collector current exponentially for a finite germanium content. For a SiGe HBT having a

germanium concentration 3 to 8% with a trapezoidal shape across the base, 4.5 times collector current increment has been reported [8]. Also, since the base current of silicon and SiGe HBT's are more or less the same, the current gain enhancement due to germanium incorporation is similar to the collector current enhancement.

With larger gain, a trade off can be made between base doping and current gain. Base doping can be increased to allow a smaller base width in order to reduce base transit time. Higher base doping also reduces base resistance, which has the effect of increasing the maximum oscillation frequency, f_{max}. With base doping increasing beyond a few $\times 10^{18} cm^{-3}$, the emitter doping needs to be reduced to prevent tunnelling leakage currents across the emitter-base junction. For silicon bipolar, reduction of emitter doping and increase in base doping has the effect of reducing the current gain. However, in this case, the current gain is already enhanced by germanium and remains high enough for useful applications. Therefore, the superior current gain potential of a SiGe HBT can be traded off for an increased f_{max} and reduced base resistance leading to higher power gain, faster switching speed, and a lower noise figure.

2.2.2 Base Transit Time

Bandgap grading across the base creates a drift electric field across the base that accelerates the electron minority carriers through the base. The graded electric field reduces the amount of base stored charge per unit collector current. This reduces the energy and time required to move charge in and out of the base during transients. As a result, the base transit time, τ_b, decreases. Theoretically, the base transit time for constant base doping can be written as [53]:

$$\tau_b = \frac{Q_b}{I_c} = \int_{0_f}^{W_f} \frac{n_{ie}^2(z)}{N_b(z)} \left[\int_z^{W_f} \frac{N_b(y)dy}{D_{nb}(y) n_{ie}^2(y)} \right] dz \tag{2.8}$$

where Q_b is the total base stored charge, and I_c is the collector current. Putting Equation 2.3 into 2.8 and integrating, $\tau_{b,Si}$ [46, 55] and $\tau_{b,SiGe}$ [8] become:

$$\tau_{b,Si} = \frac{W_b^2}{2\tilde{D}_{nb}} \tag{2.9}$$

$$\tau_{b,SiGe} = \frac{W_b^2}{\tilde{D}_{nb}} \times \frac{kT}{\Delta E_{g,SiGe}(grade)} \times \left[1 - \frac{kT}{\Delta E_{g,SiGe}(grade)}\left(1 - \exp\left(-\frac{\Delta E_{g,SiGe}(grade)}{kT}\right)\right)\right] \quad (2.10)$$

Taking the ratio of $\tau_{b,SiGe}/\tau_{b,Si}$ gives:

$$\frac{\tau_{b,SiGe}}{\tau_{b,Si}} = \frac{2}{\tilde{\eta}} \frac{kT}{\Delta E_{g,SiGe}(grade)} \times \left[1 - \frac{kT}{\Delta E_{g,SiGe}(grade)}\left(1 - \exp\left(-\frac{\Delta E_{g,SiGe}(grade)}{kT}\right)\right)\right] \quad (2.11)$$

For a finite germanium grading of more than 1% at room temperature, $\tau_{b,SiGe}/\tau_{b,Si}$ will be less than 1 and therefore the SiGe HBT base transit time will be shorter than the silicon bipolar. The cut-off frequency, f_T, of a bipolar device, as explained later in this chapter, is a function of base transit time implying that bandgap grading will also increase the usable frequency of operation of the device.

2.2.3 Output Conductance

Output conductance is a measure of collector current variations with regards to the reverse biased collector-base bias voltage. From Figure 2.9, when the reverse biased collector-base voltage increases, for a fixed base-emitter voltage, the collector-base depletion region widens and therefore reduces the neutral base width. Reduction of the neutral base width leads to an increase in the gradient of the injected electron distribution in the p-type base, as shown in Figure 2.9. Since the electron diffusion current across the base is directly proportional to this gradient, the collector current will increase. A low output conductance is desirable to achieve invariant output current in low frequency analogue applications.

The output conductance can be defined by an Early voltage, V_A, such that

$$V_A \simeq \frac{J_c}{\frac{dJ_c}{dV_{cb}}|_{V_{be}}} \quad (2.12)$$

which is the ratio of the collector current to the output conductance. Therefore, the larger the Early voltage, the lower will be the output conductance. Reference [8] shows that Early voltage enhancement of a graded SiGe HBT can be expressed as,

$$\frac{V_{A,SiGe}}{V_{A,Si}} \simeq \exp\left(\frac{\Delta E_{g,SiGe}(grade)}{kT}\right) \times \left[\frac{1 - \exp\left(-\frac{\Delta E_{g,SiGe}(grade)}{kT}\right)}{\frac{\Delta E_{g,SiGe}(grade)}{kT}}\right] \quad (2.13)$$

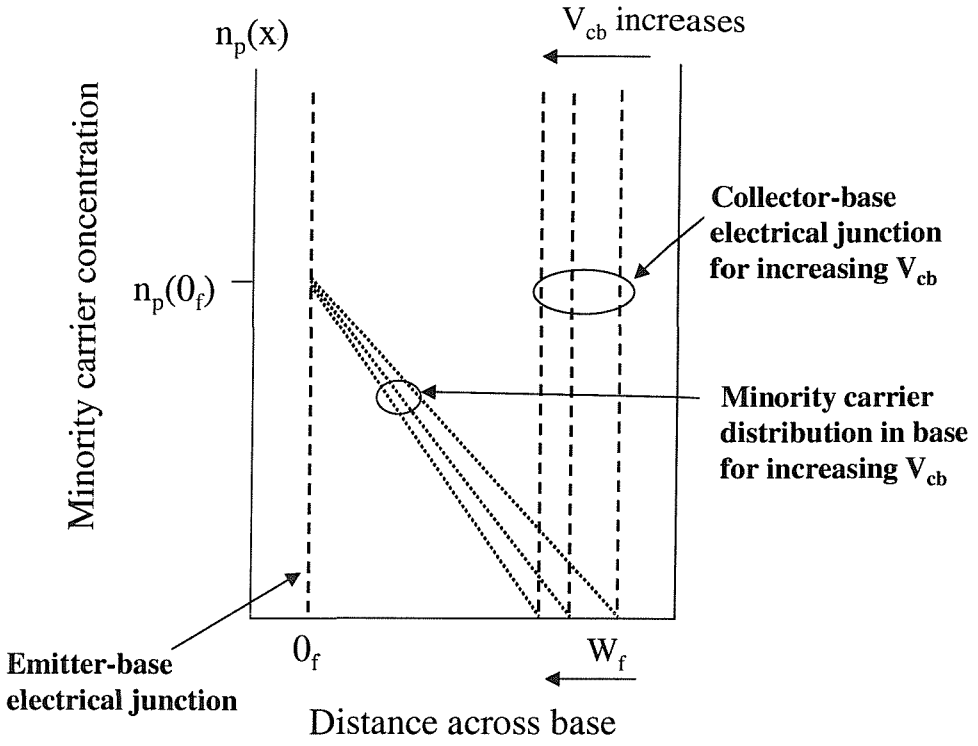

Figure 2.9: Minority carrier distribution in an n-p-n transistor for increasing collector-base reverse bias voltage in forward active mode. n_p is the electron concentration in a p-type.

For finite germanium grading, such as more than 1% germanium across the base at room temperature, the ratio will be larger than 1. Therefore, grading germanium across base improves the Early voltage as well. Also, since both current gain and Early voltage are enhanced by SiGe base and germanium grading, respectively, the βV_A product, which is an important figure of merit for analogue applications, is greatly enhanced.

2.3 Numerical Device Modelling in Medici and Atlas

In Chapters 4, 5, and 6, two full two-dimensional numerical semiconductor solvers, Medici [56] and Atlas [34], were used for full numerical simulations of SiGe HBT's. These solvers are widely used and widely recognised in industry for electrical semiconductor device simulation. Their primary functions are to solve Poisson's equation

and the continuity equations for electrons and holes. Poisson's equation is given by,

$$\epsilon \frac{\partial^2 \psi}{\partial x} = -q(p - n + N_D^+ - N_A^-) - \rho_s \tag{2.14}$$

Continuity equation for electrons and holes are,

$$\frac{\partial n}{\partial t} = \frac{1}{q}\frac{\partial J_n}{\partial x} + (G - R) \tag{2.15}$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q}\frac{\partial J_p}{\partial x} + (G - R) \tag{2.16}$$

where ϵ is the dielectric permitivity, ψ is the electrostatic potential, x is the position, q is the charge of an electron, p and n are the hole and electron concentrations, N_D^+ and N_A^- are the ionised donor and acceptor impurity concentrations, ρ_s is the surface charge density, t is the time, J_n and J_p are the electron and hole current densities, G and R are the generation and recombination rates. Poisson's equation relates variations in electrostatic potential to local charge densities. The continuity equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes.

Besides these three basic partial differential equations, physical models are needed to model the characteristics of the semiconductor. Some of the physical models that are used to model SiGe HBT's are presented here. These are models that are used to numerically investigate the proposed theories in Chapter 4, 5, and 6. Rigid bandgap models were used which do not account for splitting of degenerate bands for low concentrations of germanium [57]. In Medici, the bandgap narrowing due to germanium in strained SiGe is modelled according to [38], such that for T=90K,

$$\Delta E_{g,SiGe}(x) = \begin{cases} E_g(90) - 4.0(E_g(90) - 0.950)x; & \text{for } x \leq 0.25 \\ 0.950 - 0.66666(x - 0.25); & \text{for } 0.25 < x \leq 0.40 \end{cases}$$

where x is the germanium composition fraction and $E_g(90)$ is the bandgap energy at 90K.

In Atlas, the bandgap of strained SiGe alloys is given according to the germanium composition fraction by [34],

$$\begin{aligned} E_{g,SiGe} &= 1.08 + x \times \frac{(0.945 - 1.08)}{0.245}; \quad \text{for } x \leq 0.245 \\ &= 0.945 + (x - 0.245) \times \frac{(0.87 - 0.945)}{(0.35 - 0.245)}; \quad \text{for } 0.245 < x \leq 0.35 \end{aligned}$$

In Medici and Atlas, the bandgap narrowing model describing the effects of heavy doping in silicon [58] was used for SiGe according to,

$$\Delta E_g^{app}(N) = qV_0 \left[\ln \frac{N}{N_0} + \sqrt{\left(\ln \frac{N}{N_0} \right)^2 + C} \right]$$

where ΔE_g^{app} is the apparent bandgap narrowing due to heavy doping effects. $V_0 = 9 \times 10^{-3} eV$, $N_0 = 1 \times 10^{17} cm^{-3}$ and $C = 0.5$, are default parameters which are used for simulations presented in this thesis and N is the doping concentration.

In Medici and Atlas, the bandgap temperature dependency are modelled using [59], such that,

$$\begin{aligned} E_g(T) &= E_g(0) - \frac{\alpha T^2}{T + \beta} \\ &= E_g(300) - \alpha \left[\frac{300^2}{300 + \beta} - \frac{T^2}{T + \beta} \right] \end{aligned}$$

where $E_g(300)$ is bandgap at 300K, which is $1.08eV$, $\alpha = 4.73.10^{-3}$ and $\beta = 636$ are default parameters for Medici in this thesis. For Atlas, α and β, according to the germanium composition fraction, are [34];

$$\begin{aligned} \alpha &= (4.73 + x \times (4.77 - 4.73)) \times 10^{-4} \\ \beta &= 636.0 + x \times (235.0 - 636.0) \end{aligned}$$

Philips Unified mobility model [60, 61], which models silicon bipolar devices, is used to model the SiGe HBT carrier mobilities in Medici. It separately models majority and minority carrier mobilities. The full mobility model is presented in Appendix A. In Medici and Atlas, the electron and hole lifetimes which are concentration dependent are modelled by [62]:

$$\begin{aligned} \tau_n(x, y) &= \frac{TAUN0}{1 + N_{total}(x, y)/NSRHN} \\ \tau_p(x, y) &= \frac{TAUP0}{1 + N_{total}(x, y)/NSRHP} \end{aligned}$$

where $\tau_n(x, y)$ and $\tau_p(x, y)$ are the positional dependent lifetime of the electrons and holes, and $N_{total}(x, y)$ is the positional dependent total impurity concentration. TAUN0, TAUP0, NSRHN and NSRHP are $10^{-7} sec$, $10^{-7} sec$, $5 \times 10^{16} sec$ and

$5 \times 10^{16} sec$, respectively, and are default parameters for simulations presented in this thesis.

In Medici and Atlas, the effective density of states for conduction and valence bands are modelled for their temperature dependencies according to [63]:

$$N_c(T) = NC300 \left(\frac{T}{300}\right)^{3/2}$$
$$N_v(T) = NV300 \left(\frac{T}{300}\right)^{3/2}$$

where $N_c(T)$ and $N_v(T)$ are temperature dependent density of states of the conduction and valence bands, NC300 and NV300 are $2.8 \times 10^{19} cm^{-3}$ and $1.04 \times 10^{19} cm^{-3}$, which are default values when Medici is used in this thesis. In Atlas, NC300 and NV300 are given according to the germanium composition fraction as [34],

$$\begin{aligned} NC300 &= 2.8 \times 10^{19} + x \times (1.04 \times 10^{19} - 2.8 \times 10^{19}) \\ NV300 &= 1.04 \times 10^{19} + x \times (6.0 \times 10^{18} - 1.04 \times 10^{19}) \end{aligned}$$

for all Atlas simulations in this thesis.

Any number of models could have been used; however, it is felt that the models chosen represent the behaviour of the various transport parameters to a sufficient degree of realism and accuracy for the purposes of the numerical studies presented in this thesis.

2.4 Boron Out-diffusion and Parasitic Barrier Formation

Dopant diffuses whenever the silicon wafer is being heated up. In SiGe technology, wafer doping and subsequently dopant diffusion is an essential part of the process in defining device profile and structure. As a result, processing steps that involve heating up the device, such as annealing and oxidation, have to be optimised very carefully in order to produce the required profile and structure. Heterojunction effect of SiGe base has allowed thin, heavily doped base to be used to reduce the base transit time without compromising the base resistance or the emitter injection efficiency.

However, the base dopant, which is usually boron, is able to diffuse much faster. This can easily result in boron out-diffusion at the base where high boron concentration is found outside the germanium doped region of the base. Even in low temperature SiGe growth method, such as rapid thermal chemical vapour deposition (RTCVD) where growth temperature is 625^0C [18], undoped SiGe spacers are grown adjacent to the SiGe base to contain the boron out-diffusion. The size of the parasitic barriers depends on the amount of out-diffusion from the SiGe region, illustrated in Figure 2.10. Dopant diffusion is proportional to dopant gradient. The higher the base doping in thinner bases results in larger dopant gradients at base edges. Therefore, more out-diffusion results which requires larger spacers. Even small amount of out-diffusion (a few nanometers) can severely degrade the collector current and thus the gain of transistor [64].

Figure 2.10 shows the effect of boron out-diffusion at the collector-base junction on the base conduction and valence bands. As boron atoms diffuse, the base width increases and can extend beyond the SiGe region. Depending on the position of the base electrical junction, which depends on collector doping level, the neutral base can also extend beyond the SiGe region and fall into the SiGe and silicon regions. Since SiGe has a much smaller bandgap than silicon, a sharp change of bandgap then exists at the Si/SiGe interface in the neutral base where the bandgap increases towards the silicon region, shown in Figure 2.10. This increase of bandgap manifests itself in the conduction band creating a parasitic potential barrier at the junction. The parasitic potential barrier restricts minority carrier flow across the base, thereby decreasing the collector current, decreases the current gain, and increases the base transit time. The Early voltage is also adversely affected as slight changes in reverse collector-base bias causes large fluctuations in the conduction band edge at the edge of the neutral base region resulting in large changes in collector current. For these reasons, accurate knowledge of parasitic barrier height is required for accurate device modelling purposes.

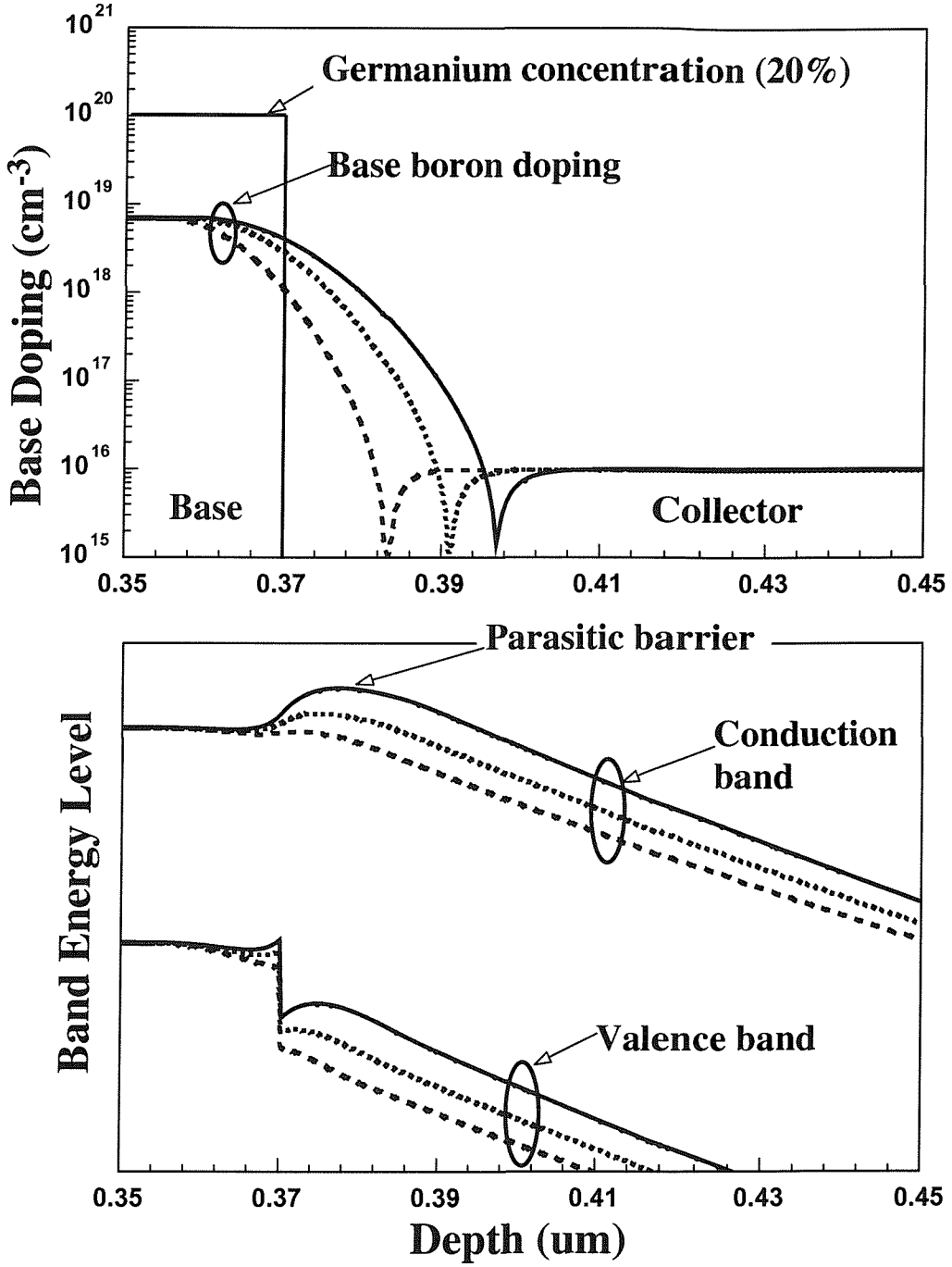

Figure 2.10: Figure showing the effect of boron out-diffusion on the device energy band at the collector-base junction based on results of numerical simulation using Medici. Three types of base boron doping distributions, with different base widths, are shown together with their corresponding band energy diagrams. The size and height of the parasitic potential barriers are dependent on the amount of out-diffusion and can exist at both emitter-base and collector base junction.

2.5 Theory of Previous SiGe HBT Characterisation Technique of Parasitic Potential Barrier

Chapter 5 is focused on a new method that is proposed to measure the parasitic barriers heights that can exist in SiGe HBT due to boron out-diffusion effect. Here, two currently existing methods, which are related to each other, are presented briefly to aid comparison with the newly proposed method. Two existing methods were proposed by Slotboom *et al.* [20] and Le Tron *et al.* [21].

2.5.1 Slotboom Method

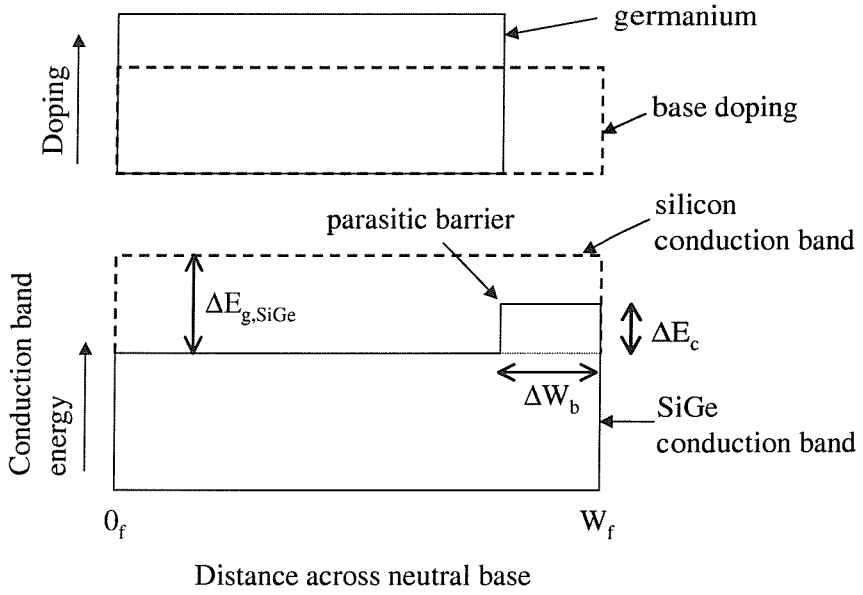

Figure 2.11: The effect of boron out-diffusion on the conduction band for uniform box-like boron and germanium doping (after [20]).

Slotboom *et al.* [20] assume a uniform box-like boron and germanium profile in the base. The resulting conduction band profile is shown in Figure 2.11. ΔW_b and ΔE_c are the parasitic barrier width and parasitic barrier height, respectively. By using the Moll-Ross/Gummel/Kroemer expression [53], a formula is derived for the SiGe HBT collector current (with parasitic barrier) [20] such that,

$$J_{c,SiGe} = \frac{qD_n n_{ib}^2(SiGe)}{N_b W_b} \times \frac{\exp(qV_{be}/kT)}{1 - \Delta W_b/W_b + (\Delta W_b/W_b)\exp(\Delta E_c/kT)} \qquad (2.17)$$

where $n_{ib}(SiGe)$ is the effective intrinsic carrier concentration in the SiGe base. The silicon bipolar collector current for a similar box like boron profile can be written as:

$$J_{c,Si} = \frac{qD_n n_{ib}^2(Si)}{N_b W_b} \exp(qV_{be}/kT) \tag{2.18}$$

where $n_{ib}^2(Si)$ is the effective intrinsic carrier concentration of the silicon base. Since,

$$\frac{n_{ib}^2(SiGe)}{n_{ib}^2(Si)} = \exp(\Delta E_{g,SiGe}/kT) \tag{2.19}$$

where $\Delta E_{g,SiGe}$ is the bandgap reduction due to germanium incorporation, as depicted in Figure 2.11, the ratio of $J_{c,SiGe}/J_{c,Si}$ becomes,

$$\frac{J_{c,SiGe}}{J_{c,Si}} = 0.4 \exp(\Delta E_{g,SiGe}/kT) \times \frac{1}{1 - \Delta W_b/W_b + (\Delta W_b/W_b)\exp(\Delta E_c/kT)} \tag{2.20}$$

where $(N_c N_v)_{SiGe}/(N_c N_v)_{Si} \approx 0.4$ [17]. Here D_n is assumed to be similar for the silicon bipolar and the SiGe HBT. For a significantly large parasitic barrier ($\Delta E_c >> kT$), the current ratio above becomes:

$$\frac{J_{c,SiGe}}{J_{c,Si}} = 0.4 \exp(\Delta E_{g,SiGe}/kT) \times (W_b/\Delta W_b) \exp(-\Delta E_c/kT) \tag{2.21}$$

$$= 0.4 \times W_b/\Delta W_b \times \exp((\Delta E_{g,SiGe} - \Delta E_c)/kT) \tag{2.22}$$

Taking natural logarithm,

$$\ln \frac{J_{c,SiGe}}{J_{c,Si}} = \ln(0.4 \times W_b/\Delta W_b) + (\Delta E_{g,SiGe} - \Delta E_c)/kT \tag{2.23}$$

Therefore, if Equation 2.23 is plotted for $\ln(J_{c,SiGe}/J_{c,Si})$ versus $1/kT$, the slope of the graph will be $(\Delta E_{g,SiGe} - \Delta E_c)$, with a y-axis intercept of $\ln(0.4 \times W_b/\Delta W_b)$. If a control SiGe HBT is available without a parasitic barrier, and which is otherwise identical to the SiGe HBT with a parasitic barrier then $\Delta E_{g,SiGe}$ can be obtained. This is because the $\ln(J_{c,SiGe}/J_{c,Si})$ versus $1/kT$ plot of Equation 2.20 for the control SiGe HBT will have slope equal to $\Delta E_{g,SiGe}$.

The drawback of Slotboom [20] method is that it needs to have an identical SiGe HBT control device without parasitic potential barrier and also an identical silicon bipolar control transistor. It requires detailed mobility and density of states modelling for silicon and SiGe. Also it requires uniformly doped base and germanium concentration which is not realistic in practical SiGe HBT.

2.5.2 Le Tron *et al.* Method

Le Tron *et al.* [21] has proposed a way of measuring the total bandgap reduction due to germanium and heavy doping effects, $\Delta E_{g,SiGe} + \Delta E_{gb}^{app}$, in a SiGe HBT.

$$\frac{J_{c,SiGe}(T)}{J_0(T)} = \exp \frac{\Delta E_{g,SiGe} + \Delta E_{gb}^{app}}{kT} \tag{2.24}$$

where,

$$J_0(T) = C_{(SiGe)} 4q \left(\frac{2\pi}{h^2}\right)^3 (m_n m_p)^{3/2} (kT)^4 \mu_{nb(Si)}(T) \mu_{pb(Si)}(T) \times R_b(T) \exp \frac{qV_{be} - E_g(T)}{kT} \tag{2.25}$$

and

$$C_{(SiGe)} = \frac{(N_c N_v)_{SiGe}(T)}{(N_c N_v)_{Si}(T)} \frac{\mu_{nb(SiGe)}(T)}{\mu_{nb(Si)}(T)} \tag{2.26}$$

where h is the Planck's constant, m_n and m_p are the effective mass for electrons and holes modelled by [65], $\mu_{nb(Si)}(T)$ and $\mu_{pb(Si)}(T)$ are the temperature dependent silicon minority and majority carrier mobilities in a p-type base modelled by [60], $R_b(T)$ is the temperature dependent intrinsic base resistance, $N_{c,SiGe}(T)$ and $N_{v,SiGe}(T)$ are the temperature dependent SiGe base density of states of the conduction and valence bands, respectively, $N_{c,Si}(T)$ and $N_{v,Si}(T)$ are the temperature dependent silicon base density of states of the conduction and valence bands, respectively, $\mu_{nb(SiGe)}(T)$ is the temperature dependent p-type SiGe base minority carrier mobility, and $E_g(T)$ is the silicon bandgap variation with temperature modeled by [59]. For Equation 2.26, Manku *et al.* [66] and Poortmans *et al.* [67] data are used for the density of states and carrier mobility ratios. The density of states ratio is 0.3 for 8% germanium at 300K and the mobility ratio is 1.3. Using the above mentioned models, and also measuring $R_b(T)$ for different temperatures, $J_0(T)$ is derived. By measuring the intrinsic base resistance, the Le Tron *et al.* method accounted for the base doping "tails" and therefore a non-uniformly doped base. From Equation 2.24, a plot of $\ln(J_{c,SiGe}(T)/J_0(T))$ versus $1/kT$ is used to yield a slope of $\Delta E_{g,SiGe} + \Delta E_{gb}^{app}$.

To measure the parasitic barrier height, the Slotboom method is adapted. Using Equation 2.20 from Slotboom *et al.* [20] the $(J_{c,SiGe}(T)/J_0(T))$ ratio from Equation

2.24 for large barrier ($\Delta E_c >> kT$), becomes,

$$\frac{J_{c,SiGe}(with\ parasitic)}{J_0} \approx \frac{W_b}{\Delta W_b} \exp\left(\frac{\Delta E_{g,SiGe} + \Delta E_{gb}^{app} - \Delta E_c}{kT}\right) \tag{2.27}$$

The plot of $\ln(J_{c,SiGe}(with\ parasitic)/J_0)$ versus $1/kT$ will yield a slope of $(\Delta E_{g,SiGe} + \Delta E_{gb}^{app} - \Delta E_c)$, and intercept at the y-axis gives $\ln(W_b/\Delta W_b)$. Once again, as in the Slotboom method, if a control SiGe HBT is available without a parasitic barrier, which is otherwise identical to the SiGe HBT with a parasitic barrier, then $(\Delta E_{g,SiGe} + \Delta E_{gb}^{app})$ can be obtained. This is because $\ln(J_{c,SiGe}/J_0)$ versus $1/kT$ plot of Equation 2.24 for the control SiGe HBT will have a slope equal to $(\Delta E_{g,SiGe} + \Delta E_{gb}^{app})$. Assuming a uniform and abrupt germanium doping concentration, ΔE_c can be determined when $(\Delta E_{g,SiGe} + \Delta E_{gb}^{app})$ is known.

The disadvantage of the Le Tron *et al.* method is that it requires a SiGe HBT control device without parasitic potential barriers but identical to the measured SiGe HBT. Also, it requires detailed mobility and density of states modelling for silicon and SiGe. And by using Slotboom model, it assumes that germanium doping is uniform and abrupt, which for practical SiGe HBT are not possible.

2.6 Figure of Merits for High Frequency Bipolar Transistor Performance

For high frequency a.c. operation, bipolar transistors are often assessed according to two types of figure of merit. The first type is known as the cut off or transition frequency, f_T. The second type is known as the maximum oscillation frequency, f_{max}. It must be said that both figures of merit may not necessarily be suitable for all integrated circuits [68]. However, both are still widely accepted, particularly in device research publications.

2.6.1 Figure of merit f_T

The f_T is defined as the frequency at which the common emitter short circuit a.c. current gain is unity [46]. It is related physically to the bipolar device as the total

delay for the minority carrier across the device from emitter to collector, τ_{ec} [63]. The total delay consists of the minority carrier stored charge delay and the junction capacitance charging delay. It can be written as:

$$f_T = \frac{1}{2\pi\tau_{ec}} \tag{2.28}$$

where τ_{ec} is comprised of:

$$\tau_{ec} = \tau_e + \tau_{ebd} + \tau_b + \tau_{cbd} + \tau_{je} + \tau_c' \tag{2.29}$$

where τ_e and τ_{ebd} are the delays due to excess minority carrier in the emitter and emitter-base depletion layer. They are generally much smaller than the other delay terms. However, for high speed devices, they can be significant [69, 70].

The base transit time τ_b is the delay due to the excess minority charge in the base. This is generally a significant term in Equation 2.29. For an n-p-n bipolar device, τ_b can be written as [55]:

$$\tau_b = \frac{W_b^2}{\alpha D_{nb}} \tag{2.30}$$

where W_b is the neutral base width, D_{nb} is the minority carrier diffusion coefficient, α depends on the base doping profile and which is equal to 2 for a uniformly doped base. Therefore, to increase f_T, the base width needs to be reduced.

The delay term τ_{cbd} is the delay at the collector-base depletion region and is known as the collector depletion layer transit time. It can be written as [46, 71]:

$$\tau_{cbd} = \frac{W_{jc}}{2v_{scl}} \tag{2.31}$$

where W_{jc} is the collector-base depletion layer width, v_{scl} is the carrier scattering limited velocity which is approximately equal to 1×10^{17} cm/s at room temperature for silicon [72]. For high speed devices, the base width is consistently scaled down. As τ_b reduces, τ_{cbd} becomes more and more significant.

The delay term τ_{je} is the total emitter depletion layer charging time and consists of [63]:

$$\tau_{je} \approx \frac{kT}{qI_c}(C_{je} + C_{jc}) \tag{2.32}$$

where C_{je} and C_{jc} are the emitter-base and collector-base depletion capacitances.

The delay term τ_c' is the collector charging time [63]:

$$\tau_c' = R_c C_{jc} \tag{2.33}$$

which can be calculated from the collector-base depletion capacitance, C_{jc}, and series collector resistance, R_c. With epitaxial collector, R_c is quite small and therefore τ_c' is usually not very significant.

Finally, the f_T can be formulated as:

$$f_T = \frac{1}{2\pi}\left(\frac{kT}{qI_c}(C_{je}+C_{jc}) + \frac{W_b^2}{\alpha D_{nb}} + \tau_e + \tau_{ebd} + \frac{W_{jc}}{2v_{scl}} + R_c C_{jc}\right)^{-1} \tag{2.34}$$

Figure 2.12 shows the typical behaviour of f_T with increasing operating I_c. From

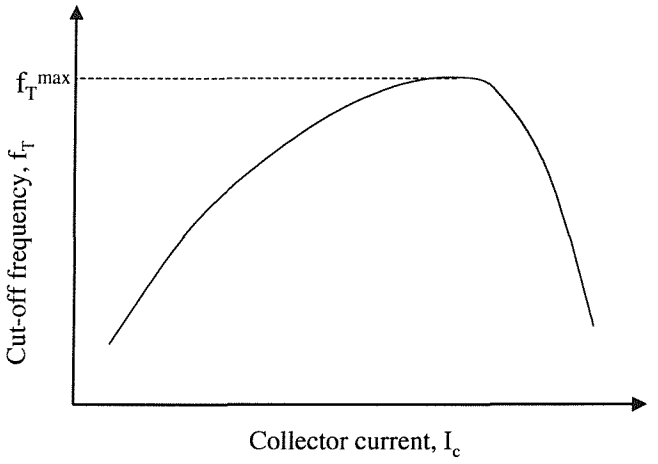

Figure 2.12: Behaviour of cut-off frequency, f_T, for increasing collector current, I_c.

Equation 2.32, τ_{je} is dominant at low collector current, and therefore f_T increases with I_c. However, the influence of τ_{je} reduces drastically as the collector current continues to increase. At peak f_T, which is f_T^{max}, τ_{je}, τ_b and τ_{cbd} are usually dominant for an optimal transistor design [46]. Therefore, to get higher f_T^{max}, all three τ_{je}, τ_b and τ_{cbd} need to be reduced.

2.6.2 Figure of merit f_{max}

The cut-off frequency, f_T, provides a good indication of the delay inside a bipolar transistor. However, it is not usually realistic or practical enough because it assumes that the output is short circuited. This is not relevant for practical applications.

Also it does not take the base resistance collector-base depletion capacitance time constant into account. These are important parameters for determining the transient behaviour of bipolar circuits. Therefore, another more practical and widely accepted figure of merit, f_{max}, is commonly used which characterises the power transfer in and out of the bipolar device. f_{max} is defined as the frequency at which the unilateral power gain becomes unity. Here the output is essentially isolated from the input by an appropriate external neutralising circuit comprising reactive and resistive components. The load that it drives is also assumed to be conjugately matched to the transistor output impedance. It can be written as [73]:

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{jc} R_b}} \tag{2.35}$$

where R_b is the base resistance. To increase f_{max}, the $C_{jc}R_b$ product needs to be reduced. However, as base width decreases rapidly to achieve high f_T, R_b will increase unless the doping is increased. To counter that effect, the base needs to be more highly doped, which means that emitter doping has to be lowered to prevent emitter-base junction tunnelling for very high base doping levels. The increased current gain capability of a SiGe base enables lowering of emitter doping without jeopardising sufficient current gain. One way to reduce C_{jc} is to reduce the collector-base junction area. It will be shown in Chapter 3 and 6 that, theoretically a lateral bipolar structure on a silicon-on-insulator (SOI) substrate provides lower emitter-base and collector-base junctions areas compared to a vertical bipolar structure and are therefore inherently faster than vertical bipolar structure.

Chapter 3

Lateral Bipolar Transistor

With the advent of deep-submicrometer photolithography, bipolar transistor with lateral structure is being reinvestigated as potentially attractive structure for achieving medium to high performance device. Deep-submicrometer photolithography has opened up the possibilities of producing thin base lateral bipolar transistor [29]. Difficulties in base definition and base contact have always been the main issues preventing a high performance lateral bipolar transistor from achieving performances comparable to a bipolar transistor with vertical structure, which is the dominant bipolar transistor structure in the bipolar manufacturing world. However, lateral bipolar transistors could prove to be more popular if it can be improved to achieving performances that is comparable to vertical bipolar transistor, especially in terms of speed and gain. This is because the lateral bipolar transistor's basic structure is simpler than vertical bipolar transistor, and also it has a shallow structure along the wafer surface, which makes it compatible to CMOS process especially when silicon on insulator (SOI) wafer is used [32]. Since CMOS is currently the dominant technology in the transistor manufacturing world and SOI is slowly becoming inevitable for performance enhancement, the lateral bipolar transistor has become a very strong candidate for the highly versatile combined SiGe HBT/BiCMOS technology.

In this chapter, issues facing lateral bipolar transistors, particularly with regard to base definition and base contact, will be discussed. This will include a look into various published novel lateral bipolar transistor structures and processes. The advantages of lateral bipolar transistors compared to vertical bipolar transistors will also

be evaluated. Then a new mode of lateral bipolar operation, known as the hybrid mode is discussed [33].

3.1 Issues Facing High Frequency RF/Microwave Lateral Bipolar Transistor Technology

Initially the issues regarding lateral base definition are examined. A high performance transistor requires a thin base in order to reduce the base transit time and the base minority carrier recombination current. As the emitter-base-collector alignment of a lateral bipolar transistor is aligned parallel to the silicon surface, the transistor base can be directly defined lithographically follow by implantation, as shown in Figure 3.1. In this approach, the base width, and therefore the frequency response, of the of lateral bipolar transistor is dependent on the smallest lithography size available. Before lithography sizes were reduced to deep submicrometer dimensions, lateral bipolar transistor bases always tended to be too wide for high frequency operation. However, recently, with the availability of deep-submicrometer lithography Sauter *et al.* [29] have reported to have achieved base widths of 80 nm using electron-beam lithography to pattern the base region. This is comparable to but still considerably larger than a typical rf vertical bipolar transistor base width, which is usually determined by the base doping diffusion, implantation, or chemical vapour deposition (CVD) layer growth.

There are also other novel methods devised specifically for submicrometer wide base definition in lateral bipolar transistors. One popular method is to use a self-aligned oxide or nitride sidewall spacer to define the lateral base [74, 75]. For example, Sugii *et al.* [75] used silicon nitride (Si_3N_4) as a spacer, as shown in Figure 3.2. An oxide step was firstly formed using oxide deposition followed by a reactive ion etch, as shown in Figure 3.2(a). After thin oxide growth, a Si_3N_4 sidewall was fabricated at the step by Si_3N_4 deposition followed by an anisotropic reactive ion etch (Figure 3.2(b)). Arsenic ions were then implanted without a mask to fabricate the emitter. SiO_2 was thermally grown to isolate the emitter (Figure 3.2(c)). The Si_3N_4 was

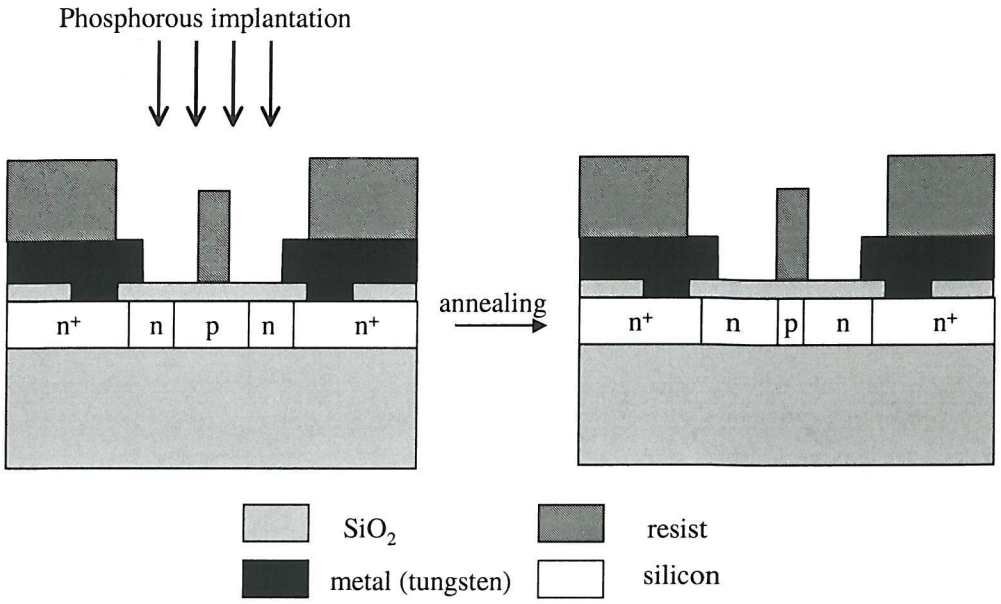

Figure 3.1: Resist is used to pattern the base region and it acts as an implantation mask. Due to high-temperature stability of tungsten, an annealing step could be performed to drive the phosphorous dopant further into the base region to reduce the base width [29].

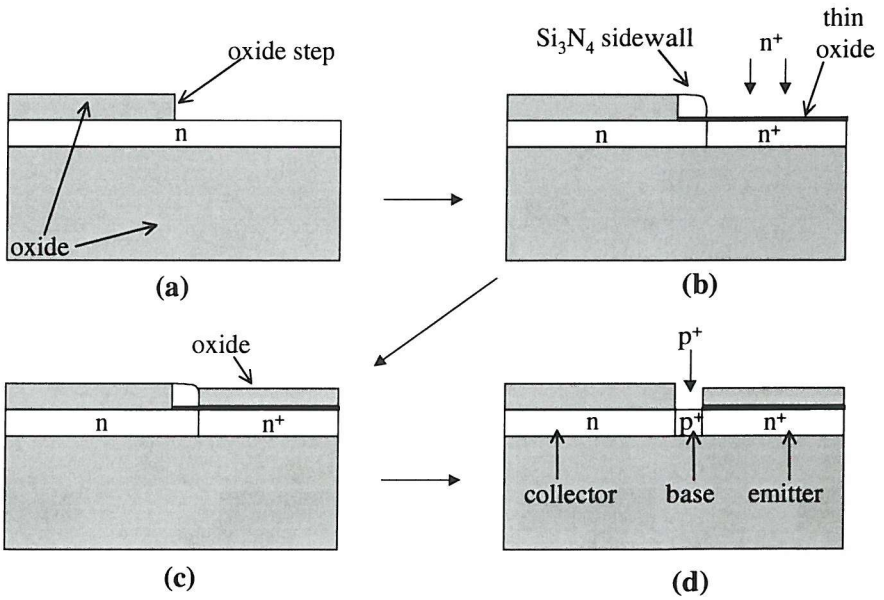

Figure 3.2: The sidewall technique used by Sugii *et al.* [75] to make an 80nm wide base. (a) Oxide step formation, (b) the formation of Si_3N_4 sidewall and emitter implantation, (c) emitter oxide growth, (d) Si_3N_4 and thin oxide strip followed by base implantation.

then selectively etched followed by boron ion implantation to make a thin intrinsic base (Figure 3.2(d)). Self-aligned base contact can be formed directly on top. It was reported that by using this technique, base width of about 80 nm was obtained by Sugii *et al.* [75].

Low base contact resistance is crucial for high speed unity power gain frequency. A lateral bipolar transistor base has the advantage that it can be contacted directly from the wafer surface on top of the active base region thus reducing the base resistance significantly. However, as the base width reduces to submicrometer dimensions, connecting the base becomes a tedious job as the base contact window needs to be opened precisely on top of the base. One solution is to have a self-aligned base contact window. Conveniently, the spacer technique described in Figure 3.2 does have a self-aligned base as part of the base definition process.

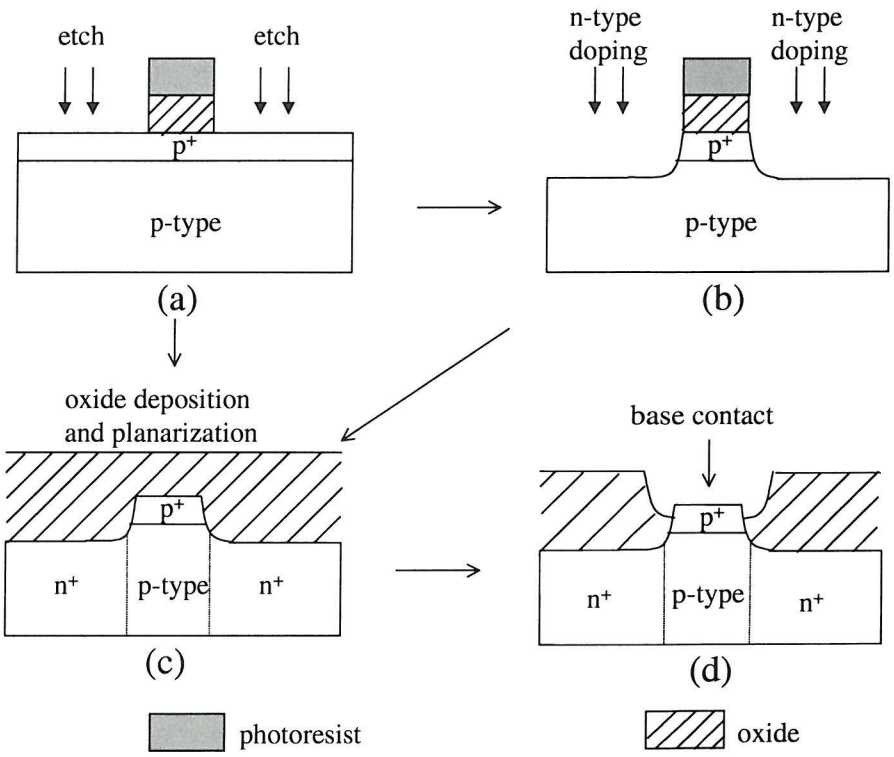

Figure 3.3: Figure illustrating the lateral bipolar transistor process flow used by Sturm *et al.* [31] which enables metal contact on top of the entire base. This method can be use in conjunction with a lithographically defined base.

In the case of a lithographically defined base, Sturm *et al.* [31] has presented a lateral bipolar transistor process, as shown in Figure 3.3, which allows a photolithographically defined base width and yet still provides for a metal contact precisely on

the entire base region. A layer of thermal oxide was grown by thermal oxidation, followed by boron implantation chosen to have its peak at the silicon surface. Lithography was then used to define narrow stripes of photoresist which would eventually define the base region. The minimum dimension was used for minimum base width. The photoresist stripes were then used as a mask for the vertical plasma etching of the oxide, followed by vertical etching of the silicon (Figure 3.3(a)). Arsenic ion implantation and annealing were then used to form the n^+ emitter and collector regions, (Figure 3.3(b)). The photoresist and oxide masked the implant from penetrating into the base region. Following the implantation, the photoresist and oxide were removed and the implant was annealed. An oxide deposition and a planarisation were performed (Figure 3.3(c)). A lithography step then defined windows for the contact to the base region, and wet oxide etch was done to expose the top of base but not the n^+ regions (Figure 3.3(d)). Base resistance of an upper limit of 20 Ω was reported for experiments with metal/silicon base contact area of $2 \times 50\mu m^2$ to $10 \times 50\mu m^2$.

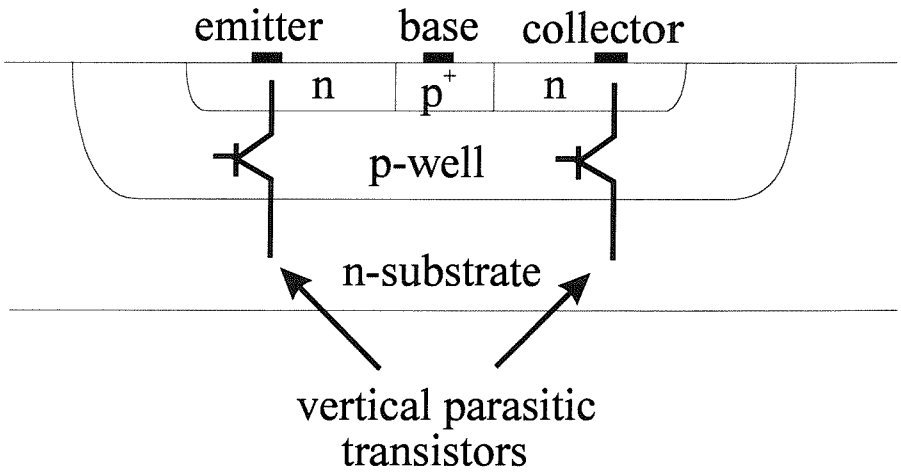

Figure 3.4: Figure illustrating the common isolation problem associated with lateral bipolar transistor caused by two parasitic vertical bipolar transistor that are inherently present in the structure.

All of the new lateral bipolar transistors reported above are based on silicon on insulator (SOI) technology. SOI is widely used for lateral bipolar transistor because a lateral bipolar transistor is inherently difficult to isolate in a silicon bulk substrate technology. This is illustrated in Figure 3.4 where for every n-p-n lateral bipolar transistor that is fabricated on a silicon wafer using a p-well, there are always two parasitic n-p-n vertical bipolar transistors that co-exist with it. With the presence of

two parasitic vertical transistors, extra care needs to be taken regarding the circuit operations so as not to accidentally turn on these vertical transistors. If this happens, these parasitic transistors can cause severe circuitry problems, such as leakage current or latch-up which can paralyse the whole circuit operation. As a result, SOI technology is particularly attractive for lateral bipolar transistor because it basically solves the whole problem of device isolation for the lateral structure by removing the vertical parasitic transistors completely [29, 74, 75]. SOI also has the advantage of having very low device parasitic substrate capacitance which can be an important criterion for high speed devices. Recently, SOI technology advancement has enabled thin film silicon of bulk silicon substrate quality to be bonded on oxide [32, 74, 76]. As SOI becomes more widely adopted, its cost should go down and its benefit could outweigh the extra cost compared to bulk silicon substrates.

3.2 Advantages of the Lateral Bipolar Transistor

In this section, the basic lateral bipolar transistor structure is compared to the basic vertical bipolar transistor structure, the most widely used bipolar transistor structure. For the purpose of comparison, the basic structures of both types of transistor are shown in Figure 3.5.

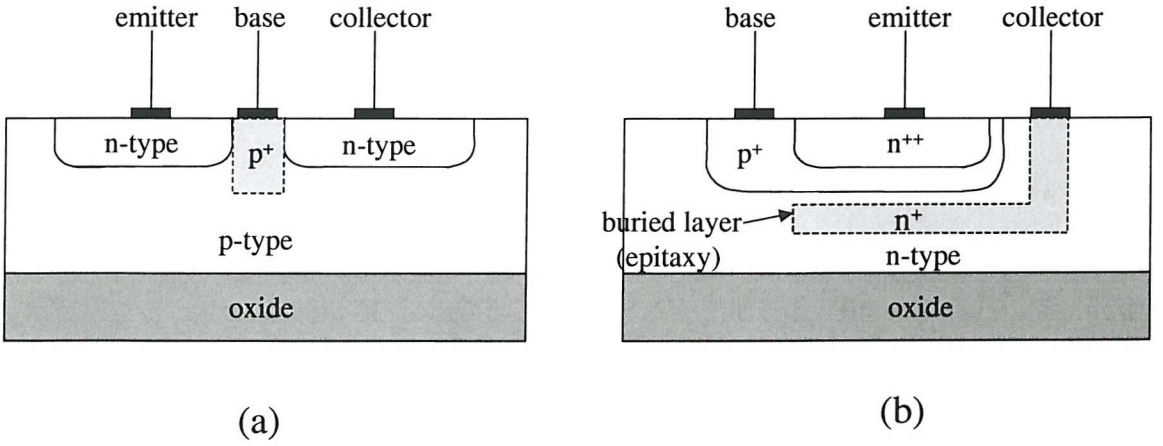

Figure 3.5: The basic structures of (a) Lateral Bipolar Transistor and (b) Vertical Bipolar Transistor.

From the figure, lateral bipolar transistor with its emitter-base-collector aligned parallel to the silicon surface can be easily contacted from the silicon surface. As presented in Section 3.1 above, the base contact can be formed precisely on top of the entire base using either the Sturm [31] or Sugii [75] method, depending on the type of base definition used. For a vertical bipolar transistor, the emitter can be contacted directly from the surface through a contact window. However, it requires more complicated ways of connecting the base and collector regions to the surface. With its basic structure vertically buried inside the silicon, the base and collector dopings need to be engineered in such a way so that the dopings will extend all the way to the silicon surface. This has a significant effect on the device terminal resistances and capacitances. Whereas the emitter can be contacted directly from the surface, the base and collector tend to have high terminal resistances due to their extended connections to the silicon surface. And in many instances, extra processing steps need to be implemented in order to reduce these resistances. In this case, as shown in Figure 3.5 (b), a highly doped n-type buried layer, grown initially using an epitaxy process, is used to create a low resistance route for collector current to reach the collector contact. This is because high terminal resistances can cause significant voltage drops across the terminals. Also, high base resistance causes reduction in the transistor maximum operating frequency and high collector resistance causes early saturation of collector current. In a lateral bipolar transistor, terminal resistances can potentially be made to be very low.

In a lateral bipolar transistor, the electron injection from emitter to base is primarily concentrated along the sidewall portion of the emitter-base junction where the intrinsic base is doped much higher, as shown in Figure 3.5(a). Therefore, the electron injection area is approximately equal to the sidewall area of the emitter-base junction, which is the emitter depth multiplied by the device length. Since the emitter depth, controlled through dopant diffusion, is typically very shallow (i.e., $0.15\mu m$), the electron injection area is small. It is usually smaller than the vertical bipolar transistor electron injection area, which is defined lithographically. Therefore lateral bipolar transistors tend to have smaller operating current compared to vertical bipolar transistors. Devices with small operating current are suitable for low powered mobile

rf applications where power consumption is of importance. High speed applications demand devices with low capacitances. Advanced vertical bipolar transistors in general tend to have much lower capacitances compared to a lateral bipolar transistor fabricated on a bulk silicon substrate. Vertical devices are much smaller and more compact, and therefore have a small junction area and also a small device-substrate interface area. Lateral bipolar transistors on bulk silicon tend to have a big junction area and device-substrate interface area. However, if lateral bipolar transistor is fabricated on SOI technology, the device semiconductor-substrate interface is eliminated and the device junction area will be greatly reduced being equivalent to the lateral electron injection area. In this case, lateral bipolar transistor device capacitances can be potentially made lower than the vertical bipolar transistor device capacitance.

Finally, referring to Figure 3.5 again, it is obvious that, in terms of structural manufacturability, that lateral bipolar transistors require simpler processing compared to vertical bipolar transistors. In fact, a lateral bipolar transistor is basically a CMOS transistor without its gate and is in principle manufacturable using only the existing CMOS technology process [30, 77]. With CMOS technology dominating the silicon world, a lateral bipolar transistor could potentially become a lower cost technology than a vertical bipolar transistor. Lateral bipolar transistor compatibility with CMOS also makes it very suitable for the bipolar-CMOS (BiCMOS) combined technology. BiCMOS is highly versatile and especially useful when both digital and analogue applications are needed on the same chip. Besides, as far as high speed and low power applications are concerned, SOI may continue to increase in importance and use such that a vertical bipolar transistor with its deeper structure may not be suitable with SOI that uses a thin active silicon layer.

3.3 The Hybrid Mode Lateral Bipolar Transistor

A new mode of lateral bipolar transistor operation was reported recently [33], and it is called the hybrid mode bipolar transistor. The basic idea is to operate a MOSFET, which is structurally similar to a lateral bipolar transistor except for the additional gate, with its gate and well connected together to form the base of the bipolar tran-

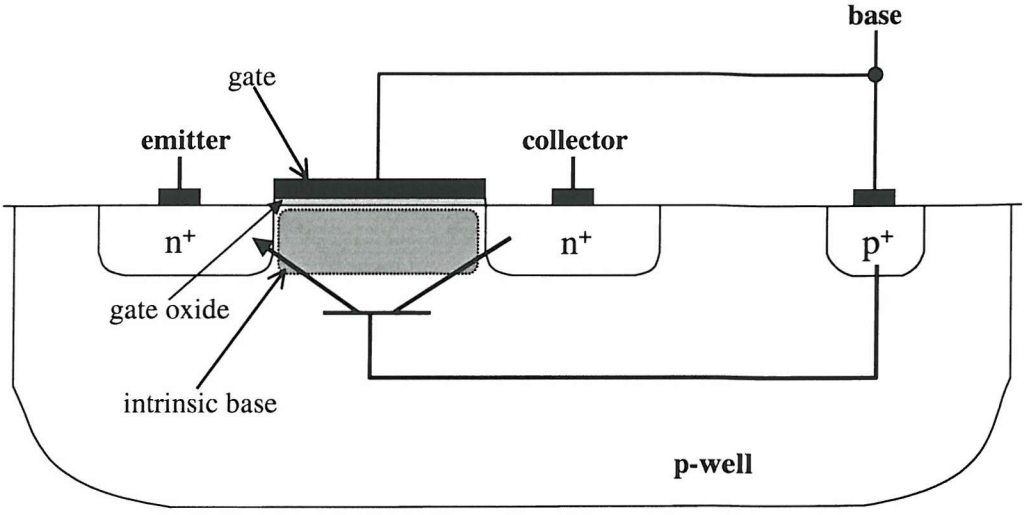

Figure 3.6: Lateral bipolar transistor operating in hybrid mode where the base and gate are connected together. The intrinsic base region, where the depletion region that results in pseudo-heterojunction effect in the lateral bipolar transistor base is also shown in the figure.

sistor, as shown in Figure 3.6. The resulting operational characteristic is like having a MOSFET and a lateral bipolar transistor combined together, operating in parallel with each other. Verdonckt *et al.* [33] has done an extensive study on the hybrid mode bipolar and found out that no additional processing steps are needed to obtain it when the MOSFET is properly designed.

Referring to section 3.2, electron injection from emitter to base of a conventional lateral bipolar transistor is primarily concentrated along the sidewall portion of the emitter-base junction. This portion of the base is known as the intrinsic base, as illustrated in Figure 3.6. The conduction and valence bands energy diagram of the emitter-intrinsic base junction is shown in Figure 3.7.

The potential barrier, Ψ_{bn}, for electron injection into the intrinsic base of the hybrid mode device is

$$\Psi_{bn} = V_{bi} - V_{be} \tag{3.1}$$

where V_{bi} is the built-in potential of the emitter-intrinsic base junction and V_{be} is a small forward emitter-base bias externally applied, Figure 3.7.

The hole injection barrier, Ψ_{bp}, from intrinsic base to emitter is;

$$\Psi_{bp} = (V_{bi} - \Delta E_g^{app}/q) - V_{be} \tag{3.2}$$

where ΔE_g^{app} is the total apparent bandgap narrowing due to heavy doping between the emitter and the intrinsic base. Hence in a conventional bipolar transistor, Ψ_{bp} is lower than Ψ_{bn}, and the difference $\Delta\Psi$ is due to the heavily doped emitter bandgap narrowing.

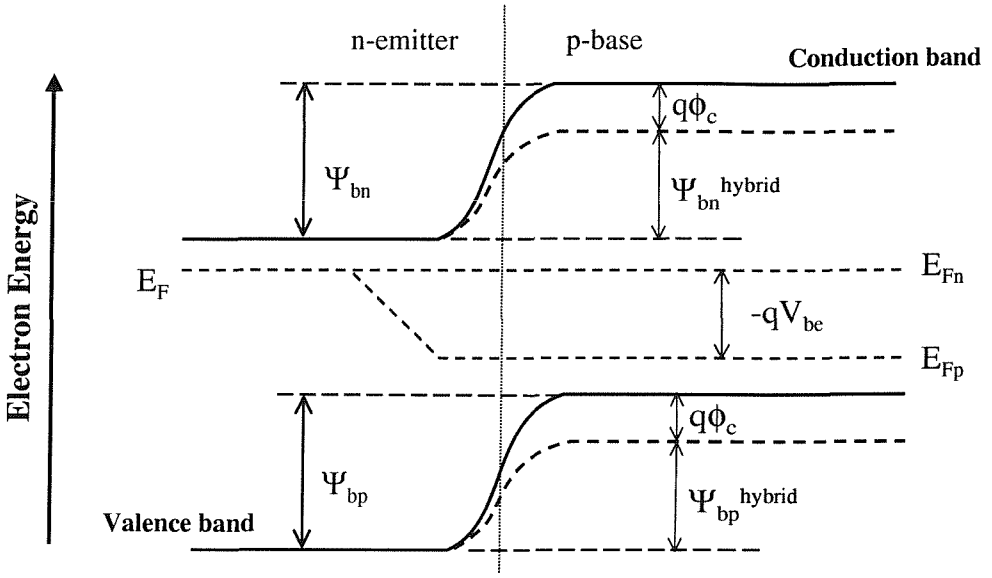

Figure 3.7: Energy band diagram for conventional lateral BJT (solid lines) and the hybrid mode lateral BJT (broken lines), across the emitter-intrinsic base junction in the direction parallel and close to the oxide-silicon interface.

A hybrid-mode lateral Bipolar structure is basically a conventional lateral bipolar transistor with the base contact replaced by a thin gate oxide and an n^+ polysilicon gate on top, shown in Figure 3.8. The polysilicon gate is directly connected to the base (p-well), not shown in Figure 3.8. Since the gate and well are tied together, a depletion region can be created underneath the gate oxide by controlling the voltage drop between the gate and well through optimising the gate oxide thickness and channel doping. This depletion layer is stable as the gate and well are permanently connected together and it is strongest at the oxide silicon interface.

The main part of the emitter current is composed of the electrons which are injected into the depleted part of the intrinsic base, $1e$ in Figure 3.8. Figure 3.9 shows the energy band diagram through the intrinsic base in the direction perpendicular to

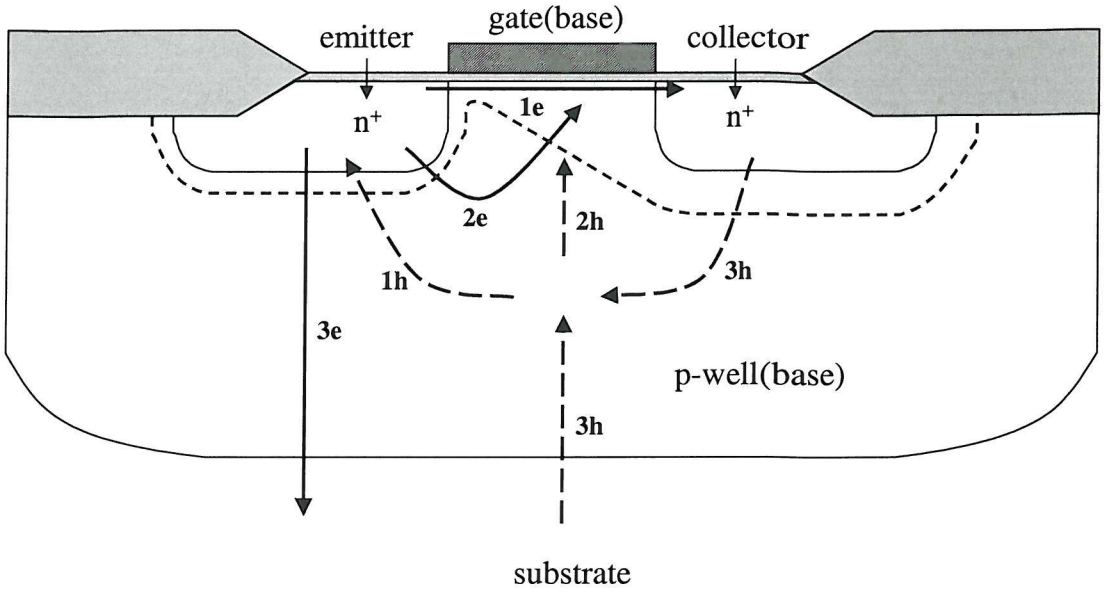

Figure 3.8: Diagram indicating the major electron (solid lines) and hole (broken lines) current components in the hybrid-mode lateral BJT.

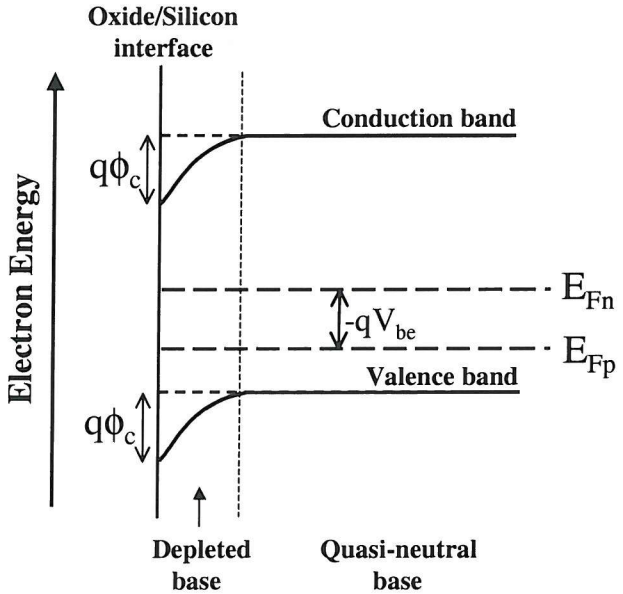

Figure 3.9: Energy band diagram for conventional lateral BJT (solid lines) and the hybrid mode lateral BJT (broken lines), through the intrinsic base in the direction perpendicular to the surface.

the surface. There is a potential increase ϕ_c from the quasi-neutral part of the base to the saddle point in the depletion region. ϕ_c depends on process parameters such as the workfunction difference between the polysilicon gate and the substrate, the interface state density, the fixed oxide charge density, and the surface doping concentration. Therefore the potential barrier of electrons injection into the depleted intrinsic base, Ψ_{bn}^{hybrid} is

$$\Psi_{bn}^{hybrid} = V_{bi} - V_{be} - \phi_c \tag{3.3}$$

The other 2 parts of the emitter current are shown as $2e$ and $3e$, respectively in Figure 3.8. $2e$ consists of electrons which are injected from the emitter over the larger potential barrier into the quasi-neutral base where most of the electrons are attracted towards the saddle point potential and merge into the surface depletion region before reaching the collector. $3e$ is composed of electrons which are injected vertically from the bottom part of the emitter into the extrinsic base region and collected by the lightly doped n substrate. $2e$ and $3e$ are rather small compared to $1e$.

The main part of the base current composed of the holes which are injected from the base into the emitter, $1h$ in Figure 3.8. Since large part of the intrinsic base region is depleted of holes, as indicated in Figure 3.9, most of the holes are injected from the extrinsic base into the bottom of the emitter. The number of holes injected will depend on the bottom area of the emitter and the doping of the well under the emitter. The injection barrier for the holes is given by

$$\Psi_{bp}^{hybrid} = (V_{bi} - \Delta E_g^{app}/q) - V_{be} \tag{3.4}$$

which is larger than that seen by the electrons as long as $q\phi_c > \Delta E_g^{app}$. Other parts of the base current consist of recombination current in the base ($2h$) and hole current from the collector and substrate into the base through the reverse-biased junctions ($3h$). Both $2h$ and $3h$ are rather small compared to $1h$.

Therefore the electron current is mainly determined by the electrons injected from the emitter into the depleted region of the intrinsic base($1e$), while the hole current is mainly determined by the holes injected from the quasi-neutral part of the base in to

the emitter ($1h$). Figure 3.7 shows the energy diagram of the hybrid mode operation. If the hybrid-mode lateral BJT is correctly designed (i.e. $\Psi_{bp} > \Psi_{bn}$ or $q\phi_c > \Delta E_g^{app}$), it behaves as a heterojunction BJT. The emitter injection efficiency approaches unity and as a consequence the current gain is very large. At low collector current levels, lateral bipolar action with a current gain higher than 1000 is achieved [33]. [78] has reported current gain higher than 2000 and a cut-off frequency of 1.6 GHz. [79] also achieve excellent device characteristics with peak current gain, $h_{FE} = 120$, peak breakdown voltage, $BV_{CEO} = 10V$, and peak cut-off frequency, $f_T = 4.5GHz$. Both the emitter injection efficiency and current gain are predicted to improve at reduced temperatures due to their exponential dependence on $q\phi_c - \Delta E_g^{app}$. However, the voltage drop across the gate oxide and depletion region could potentially increase the ideality factor of the hybrid-mode bipolar collector current. Increase in the collector current ideality factor reduces the hybrid-mode bipolar transconductance, g_m, which in turn reduces the cut-off frequency of the device.

3.4 Conclusion

In this chapter, an investigation was carried out to assess the potential of lateral structure SiGe HBT for high performance applications. Various issues regarding lateral bipolar structures such as base definition and base contact were discussed. Comparing the structure of lateral bipolar to vertical bipolar suggests that lateral bipolar has many advantages and suitable for microwave applications. A new mode of silicon bipolar transistor operation known as the hybrid mode was also discussed. The basic idea is to operate a MOSFET, which is structurally similar to a lateral bipolar transistor except for the additional gate, with its gate and well connected together to form the base of the bipolar. The resulting operational characteristic is like having a MOSFET and a lateral bipolar transistor combined together, operating in parallel with each other. If the hybrid-mode lateral BJT is correctly designed, it behaves like a virtual heterojunction BJT. Peak current gain of more than 2000 is reported. However, the hybrid-mode lateral BJT could have problem with increase in collector current ideality.

Chapter 4

An Electrical Method for Measuring The Difference in Bandgap across the Neutral Base in SiGe HBT's

4.1 Introduction

Rapid development of SiGe HBT's has brought about the production of transistors with aggressive bandgap profiles. With such capabilities of bandgap engineering, issues regarding the most suitable bandgap profile for certain types of applications of device has become significantly important. Roulston *et al.* [69, 80] have examined issues concerning the optimum base germanium profile to use for particular applications. It was found that uniform base bandgap profile is most optimum for minimum emitter delay and maximum current gain. Whereas for minimum base delay and/or high output resistance purposes, bandgap grading across the base will be most benefiting [8, 69, 80].

In this chapter, a simple low frequency electrical method will be proposed to measure directly the bandgap difference between the electrical edges of the neutral base in a SiGe HBT. The theoretical basis of this method will firstly be presented where

the physical justification and also certain assumptions for this method is discussed. Then the method shall be verified numerically, by means of full numerical simulation using the Medici [56] semiconductor solver, and also experimentally. With the numerical and experimental results, the effectiveness, accuracy and different usage of this method in device characterisation will be discussed. Finally, conclusions will be drawn.

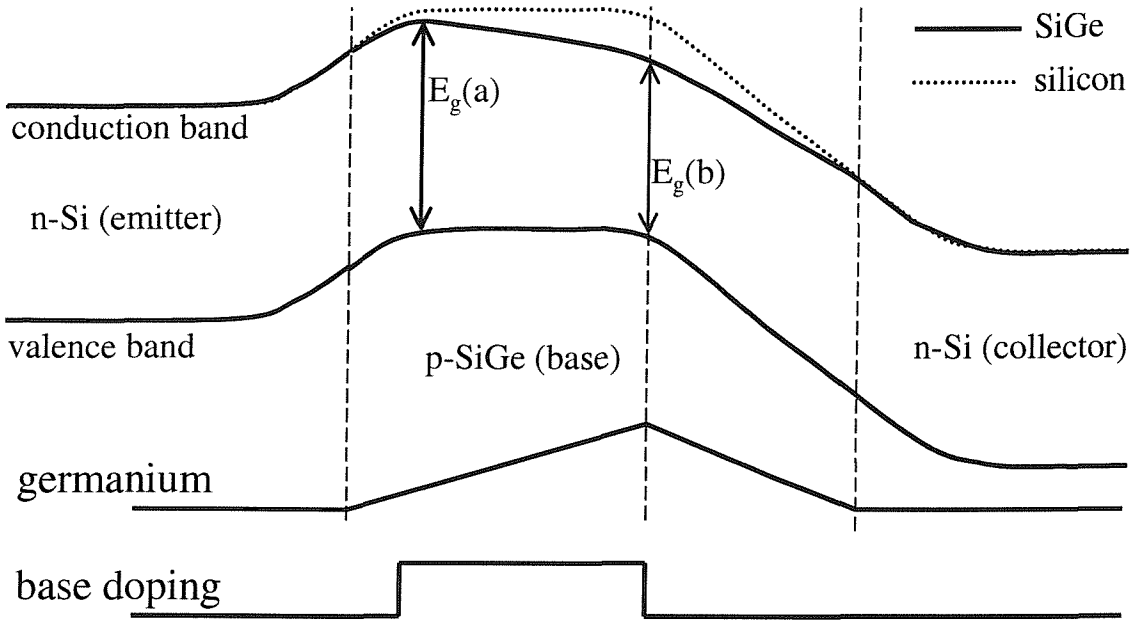

Figure 4.1: Figure showing the effect of grading the germanium concentration across the base region on the device band energy. The difference in bandgap across the neutral base is equivalent to $E_g(a) - E_g(b)$.

The single most important process parameter to control in silicon-germanium heterojunction bipolar transistor (SiGe HBT) process is the quantity and profile of the germanium in the electrical neutral base region. The total quantity of germanium in the neutral base region controls the current gain through bandgap reduction and the resulting increase in emitter injection efficiency [13, 53]. The difference in germanium concentration between the electrical edges of the neutral base region (i.e. at the emitter-base and collector-base edges of the neutral base) determine several other important properties including the device output conductance [81] and base transit time [13]. Both of these parameters can be dramatically improved by grading the

germanium so that the bandgap is smaller at the collector side of the neutral base, shown in Figure 4.1. Advanced high frequency SiGe HBT's usually contain heavily doped bases [82] to reduce intrinsic base resistance, taking advantage of the larger emitter efficiency. The heavy doping results in impurity-induced bandgap reduction or narrowing [83] which must also be taken into account when determining the combined impact of the germanium profile and the impurity profile on the differences in bandgap reduction at the edges of the neutral base region. Design of an optimal SiGe HBT is further complicated by the fact that both the germanium and doping profiles cannot be made truly abrupt in spatial composition which results in concentration "tails" that can inadvertently result in unwanted differences in bandgap across the neutral base. If the base doping extends beyond the Si-SiGe boundaries into the emitter and/or collector regions, parasitic potential barriers will form severely degrading current gain and transition frequency [18, 20, 21].

Clearly it would be extremely useful to be able to measure directly the bandgap difference between the edges of the neutral base region, shown in Figure 4.1, when developing SiGe HBT processes. It is especially advantageous when it is necessary to determine process factors that are contributing to poor overall device performance. The author is not aware of any method at the present time that is able to measure the bandgap grading across the neutral base electrically. To date the only methods available to make a direct determination of this bandgap difference is to measure the actual base dopant and germanium spatial composition in a processed SiGe HBT. This involves using time-consuming and expensive characterisation techniques such as secondary ion mass spectroscopy (SIMS), followed by detailed numerical modelling. To be accurate, it is necessary to be able to resolve dopant and germanium spatial variations to within a few nano-meters, which is beyond present conventional SIMS capabilities. SIMS will only give a relative germanium concentration profile making calibration necessary using some other technique such as x-ray diffraction to obtain absolute germanium concentrations. The collector dopant concentration is also required for electrical modelling, however, this must usually be determined from capacitance-voltage measurements as many transistors have a collector dopant concentration below the measured noise level of SIMS. To determine the actual electrical

impact of the measured germanium and dopant variations, it is then necessary to assume correct bandgap narrowing models. Established bandgap narrowing models exist for silicon [83], however, the development of models for strained SiGe, which include the effects of heavy doping etc. [84], is still an active area of research. Choosing the best bandgap narrowing model is also complicated by the prospect that the grown SiGe layer may not be fully strained due to improper growth conditions [42].

Comparison with a silicon control device that does not contain germanium is another approach [13, 14] that can be adopted to yield useful information regarding the impact of the germanium grading on device performance in the SiGe HBT's. Besides requiring the processing of a separate set of devices, several factors can complicate interpretation of the comparative measurements of current gain and frequency response. These include differences in impurity profiles between the silicon control and the SiGe HBT due to differences in impurity incorporation and diffusion in the presence of Ge, differences in mobility [85] between the silicon base of the control and the strained SiGe base of the HBT, differences in effective masses [66] and also processing variations between wafers. All these can contribute to errors in experimental interpretation of bandgap grading and reduction.

4.2 Theory

From Appendix B, Equation B.6, the low frequency a.c. output conductance for a SiGe HBT operating in forward active mode, g_{of}, as illustrated in Figure 4.2(a), becomes [81];

$$g_{of} = \frac{-I_{cf}C_{jc}^{f}}{qA_cD_{nb}(W_f)n_{ie}^2(W_f)}\left(\int_{0_f}^{W_f}\frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)}dx\right)^{-1} \tag{4.1}$$

where the "f" subscripted and superscripted symbols refer to the transistor operating in the forward active region. q is the electronic charge, I_{cf} is the forward d.c. collector current, as illustrated in Figure 4.2(a), C_{jc}^{f} is the junction capacitance of the reverse biased collector-base junction, A_c is the collector-base junction area, 0_f is the neutral edge of the base region at the emitter side, W_f is the neutral edge of the base region at the collector side, $D_{nb}(W_f)$ and $n_{ie}(W_f)$ are the base electron diffusivity and effec-

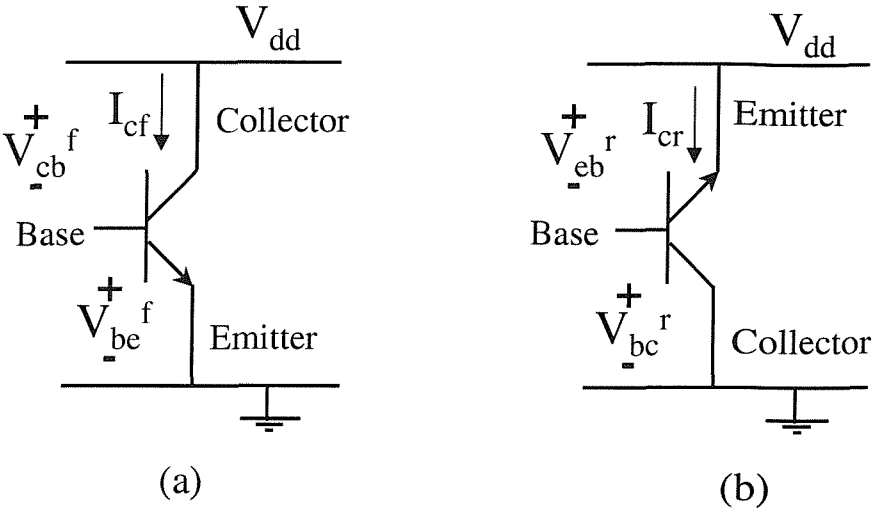

Figure 4.2: Circuit diagram of an n-p-n transistor illustrating the bias condition and the current flow when the transistor is biased at the (a) forward active region of operation, and (b) reverse active region of operation.

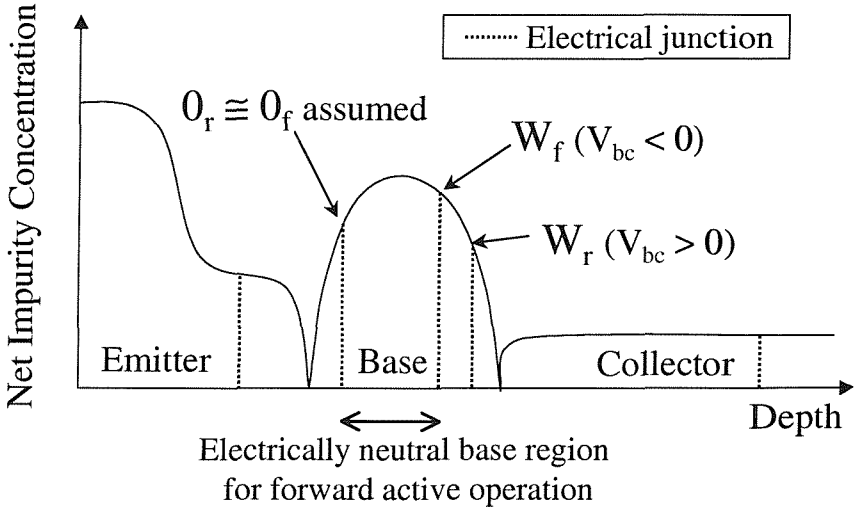

Figure 4.3: Figure illustrating the difference of the neutral base boundary positions in the forward active region mode and reverse active region mode. For a highly doped base, which is common for a SiGe HBT, the position of 0_r for zero emitter-base bias can be made very close to the position of 0_f for normal forward emitter-base junction reverse bias, in reverse active operation. This is because most of the space-charge layer movement will take place in the lower-doped emitter side of the junction.

tive intrinsic carrier concentrations, respectively, at the collector side of the neutral base, $N_b(x)$ is the positional dependent base impurity profile, $D_{nb}(x)$ is the positional dependent base diffusivity of electrons and $n_{ie}(x)$ is the positional dependent effective intrinsic carrier concentration.

Similarly, the low frequency a.c. output conductance in reverse active operation, as illustrated in Figure 4.2(b), g_{or}, can be written as;

$$g_{or} = \frac{-I_{cr}C^r_{je}}{qA_eD_{nb}(0_r)n^2_{ie}(0_r)}\left(\int_{W_r}^{0_r}\frac{N_b(x)}{D_{nb}(x)n^2_{ie}(x)}dx\right)^{-1} \tag{4.2}$$

where the "r" subscripted and superscripted symbols refer to the transistor operating in the reverse active region. I_{cr} is the reverse d.c. collector current, which is the current that flows into the emitter when the transistor is operating in the reverse active region, as illustrated in Figure 4.2(b). C^r_{je} is the junction capacitance of the reverse biased emitter-base junction, A_e is the emitter area, 0_r is the neutral edge of the base region at the emitter side, W_r is the neutral edge of the base region at the collector side, $D_{nb}(0_r)$ and $n_{ie}(0_r)$ are the base electron diffusivity and effective intrinsic carrier concentrations, respectively, at the emitter side of the neutral base.

As different bias voltages are used across the emitter-base and collector-base junctions for the forward and the reverse active operation, the neutral base positions are in general different for both modes of operation. Therefore, as illustrated in Figure 4.3, W_f and 0_f in Equation 4.1 are not necessary the same as W_r and 0_r in Equation 4.2. Also I_{cf}, obtained from Equation B.2 of Appendix B, and I_{cr} can be expressed by,

$$I_{cf} = qA_e\exp\left(\frac{V^f_{be}}{V_T}\right)\left(\int_{0_f}^{W_f}\frac{N_b(x)}{D_{nb}(x)n^2_{ie}(x)}dx\right)^{-1} \tag{4.3}$$

$$I_{cr} = qA_c\exp\left(\frac{V^r_{bc}}{V_T}\right)\left(\int_{W_r}^{0_r}\frac{N_b(x)}{D_{nb}(x)n^2_{ie}(x)}dx\right)^{-1} \tag{4.4}$$

These expressions show that I_{cf} will be different from I_{cr} because they are influenced by the neutral base boundaries. Therefore, to account for the effect of the difference in neutral base boundaries between modes of operation, Equation 4.3 and 4.4 are substituted into Equation 4.1 and 4.2 respectively such that g_{of} and g_{or} become,

$$g_{of} = \frac{-I^2_{cf}C^f_{jc}}{q^2A_cA_eD_{nb}(W_f)n^2_{ie}(W_f)\exp(V^f_{be}/V_T)} \tag{4.5}$$

$$g_{or} = \frac{-I_{cr}^2 C_{je}^r}{q^2 A_c A_e D_{nb}(0_r) n_{ie}^2(0_r) \exp(V_{bc}^r/V_T)} \tag{4.6}$$

where V_{be}^f is the forward bias voltage across the emitter-base junction in the forward active region of operation, V_{bc}^r is the forward bias voltage across the collector-base junction in the reverse active region of operation, and V_T is the thermal voltage. Taking the ratio of Equation 4.6 to Equation 4.5 one obtains;

$$\frac{g_{or}}{g_{of}} = \left(\frac{I_{cr}}{I_{cf}}\right)^2 \left(\frac{C_{je}^r}{C_{jc}^f}\right) \left(\frac{D_{nb}(W_f)}{D_{nb}(0_r)}\right) \exp\left(\frac{V_{be}^f - V_{bc}^r}{V_T}\right) \left(\frac{n_{ie}^2(W_f)}{n_{ie}^2(0_r)}\right) \tag{4.7}$$

The effective intrinsic carrier concentration can be expressed in terms of density of states and the bandgap energy such that,

$$n_{ie}^2(W_f) = N_c(W_f) N_v(W_f) \exp\left(\frac{-E_g(W_f)}{kT}\right) \tag{4.8}$$

$$n_{ie}^2(0_r) = N_c(0_r) N_v(0_r) \exp\left(\frac{-E_g(0_r)}{kT}\right) \tag{4.9}$$

therefore,

$$\frac{n_{ie}^2(W_f)}{n_{ie}^2(0_r)} = \frac{N_c(W_f) N_v(W_f)}{N_c(0_r) N_v(0_r)} \exp\left(\frac{E_g(0_r) - E_g(W_f)}{kT}\right) \tag{4.10}$$

where $N_c(W_f)$ and $N_v(W_f)$ are the effective density of states in the conduction and valence band, respectively, at the collector side of the neutral base when the transistor is operated in the forward active region, and $N_c(0_r)$ and $N_v(0_r)$ are the effective density of states in the conduction and valence band, respectively, at the emitter side of the neutral base when the transistor is operated in the reverse active region. $E_g(0_r)$ is the bandgap energy at the emitter side of the neutral base in reverse active region mode, $E_g(W_f)$ is the bandgap energy at the collector side of the neutral base in forward active region mode, T is the absolute temperature and k is the Boltzmann's constant.

Substituting Equation 4.10 into Equation 4.7 one obtains for the ratio of the output conductance in reverse and forward active operation,

$$\frac{g_{or}}{g_{of}} = \left(\frac{I_{cr}}{I_{cf}}\right)^2 \left(\frac{C_{je}^r}{C_{jc}^f}\right) \left(\frac{D_{nb}(W_f)}{D_{nb}(0_r)}\right) \exp\left(\frac{V_{be}^f - V_{bc}^r}{V_T}\right) \left(\frac{N_c(W_f) N_v(W_f)}{N_c(0_r) N_v(0_r)}\right) \exp\left(\frac{E_g(0_r) - E_g(W_f)}{kT}\right) \tag{4.11}$$

Equation 4.5 shows that the forward active mode output conductance of the SiGe HBT's is inversely affected, among other things, by the effective intrinsic carrier concentration at the collector side of the neutral base. This is not surprising because output conductance is a result of base width modulation due to increase in collector-base junction depletion region. Higher effective intrinsic carrier concentration at the collector side of the neutral base means less depletion region penetration into the base from the collector side and therefore less increment in collector current. This also means reduction of output conductance. In the same way, low effective intrinsic carrier concentration at the collector side of the neutral base will results in an output conductance increase.

Equation 4.6 shows that reverse active mode output conductance of the SiGe HBT's is inversely affected, among other things, by the effective intrinsic carrier concentration at the emitter side of the neutral base. Equation 4.8 and 4.9 show that the effective intrinsic carrier concentration is related to the positional dependent base bandgap energy. Therefore, if the bandgap energy effect can be isolated from Equation 4.11, the relationship between the output conductance and the positional dependent base bandgap energy can be used to create a method to directly extract the base bandgap energy information from the device output conductance.

Taking the natural logarithm for Equation 4.11, an Arrhenius relationship is established, such that,

$$\ln\left(\frac{g_{or}}{g_{of}}\right) - 2\ln\left(\frac{I_{cr}}{I_{cf}}\right) - \ln\left(\frac{C_{je}^{r}}{C_{jc}^{f}}\right) = \ln\left(\frac{D_{nb}(W_f)}{D_{nb}(0_r)}\right) + \left(\frac{V_{be}^{f} - V_{bc}^{r}}{V_T}\right) + \ln\left(\frac{N_c(W_f)N_v(W_f)}{N_c(0_r)N_v(0_r)}\right) + \left(\frac{E_g(0_r) - E_g(W_f)}{kT}\right) \tag{4.12}$$

which is linear with respect to inverse temperature provided that,

$$\ln\left(\frac{D_{nb}(W_f)}{D_{nb}(0_r)}\right) + \left(\frac{V_{be}^{f} - V_{bc}^{r}}{V_T}\right) + \ln\left(\frac{N_c(W_f)N_v(W_f)}{N_c(0_r)N_v(0_r)}\right) \tag{4.13}$$

is constant with respect to temperature. The capacitance term, $\ln\left(C_{je}^{r}/C_{jc}^{f}\right)$, in Equation 4.12 was later found to be virtually constant with temperature in the numerical modelling section, Section 4.5, except for devices where the emitter and collector doping are different by several orders of magnitude. If this situation arises the junction

capacitances can be easily measured using conventional techniques. I_{cf} and I_{cr} are measurable quantities and therefore $\ln(I_{cr}/I_{cf})$ can be easily taken into account in Equation 4.12.

If the transistor is operated in the forward active region of operation and then in the reverse active region of operation, for various temperatures such that the forward biased V_{be}^{f} and V_{bc}^{r} are equal at each temperature, a plot of:

$$\ln\left(\frac{g_{or}}{g_{of}}\right) - 2\ln\left(\frac{I_{cr}}{I_{cf}}\right) - \ln\left(\frac{C_{je}}{C_{jc}}\right) \quad \text{versus} \quad \frac{1}{T} \tag{4.14}$$

will yield, to first order, a straight line which has a slope equal to $(E_g(0_r) - E_g(W_f))/k$. Since k is a constant, $E_g(0_r) - E_g(W_f)$, which is the difference of bandgap between the emitter junction in reverse operation mode and the collector junction in forward operation mode, can be extracted directly from the slope. For a highly doped base, which is common for a SiGe HBT, the position of 0_r for zero emitter-base bias can be made very close to the position of 0_f for normal forward emitter-base junction bias because most of the space-charge layer movement will take place in the lower-doped emitter side of the junction, as shown in Figure 4.3. Therefore, $E_g(0_r)$ is similar to $E_g(0_f)$ and $E_g(0_r) - E_g(W_f)$ becomes the difference of bandgap between the collector-base and emitter-base electrical junctions (i.e. bandgap grading across the neutral base) for forward active region of operation.

Two distinct categories of SiGe HBT impurity profiles have emerged. One type uses a low doped emitter region in conjunction with a highly doped base region which is often more highly doped than the emitter. This type of device trades off the increased emitter efficiency afforded by the reduced bandgap in the base by using a highly doped base to attain lower base resistance. These types of devices take full advantage of the presence of germanium in the base leading to extremely high switching speeds [2, 17]. A second earlier type of SiGe HBT design uses a highly doped emitter region and therefore cannot fully exploit the increased emitter efficiency to reduce base resistance since the base doping must be sufficiently low to avoid unwanted tunnelling leakage currents across that emitter-base junction [86]. The high speed switching properties and rf noise figures in such devices are therefore limited by this requirement. In such devices, a larger error is expected to occur with

respect to the assumption that the zero and forward bias positions of the neutral base edge on the emitter side of the base are in approximately the same position. For such devices it can be estimated, using simple pn-junction theory, that the relative error in using this assumption to estimate the degree of bandgap difference for forward active operation is approximately given by the ratio of the emitter-base space charge layer width divided by the neutral base width in forward active operation, further explained in Appendix C.1. Devices of this type have been reported to have base impurity concentrations on the order of $5 \times 10^{18} cm^{-3}$ and metallurgical base widths of $90nm$ [86]. Use of the proposed technique to measure the bandgap difference across the neutral base region in forward active operation on this structure could lead to an error on the order of 5% to 10%, elaborated in Appendix C.1. If the germanium concentration is purposely graded using a linear distribution, this sort of knowledge can be used to arrive at a simple extrapolation to obtain a more accurate estimate of the bandgap difference in such devices.

Klaassen [60, 61] has shown that in silicon, even though the minority carrier mobility varies with temperature, it does not vary exponentially with $1/T$. In this case, the temperature dependency of the ratio of the electron diffusivities in Equation 4.11 will tend to cancel out or at least be much weaker than an exponential behaviour. If it is significant, the plot of Equation 4.14 will not yield a straight line and therefore the extraction method will not work.

Simple theory (i.e. parabolic band approximation) suggests that the temperature dependence of the ratio of the density of states on either side of the neutral base region will cancel resulting in this ratio becoming,

$$\left(\frac{N_c(W_f)N_v(W_f)}{N_c(0_r)N_v(0_r)}\right) = \left[\frac{m_e(W_f)m_h(W_f)}{m_e(0_r)m_h(0_r)}\right]^{3/2} \tag{4.15}$$

where m_e and m_h are the effective masses of electrons and holes, respectively. Equation 4.15 should be nearly temperature independent if the ratio of effective mass products on either side of the neutral base region is much weaker than the exponential bandgap term in Equation 4.11. The proposed technique does not depend upon the nature of the temperature dependence of the actual density of states provided that such dependence is not purely exponential. For low concentrations of

germanium in has been shown [57] that a portion of the density of states can indeed become exponentially dependent upon temperature due to splitting of degeneracies in the conduction and valence bands. From Equation 4.10 it can be seen that any such exponential dependence in any of the density of states functions N_c and N_v at either edges of the neutral base region will simply introduce an apparent contribution to the overall bandgap variation $E_g(0_r) - E_g(W_f)$ across the neutral base if the strength of the density of states exponential dependence varies across the neutral base region. In other words, any physical effect, be it germanium incorporation, strain, impurity-induced bandgap narrowing, or non-degenerate band splitting, will contribute to the overall bandgap variation across the neutral base that will directly impact transistor electrical behaviour. It is this overall effective bandgap variation that the proposed technique is intended to yield. Obtaining a straight line plot in the technique guarantees that only physical effects which contribute to this overall bandgap variation are being accounted for.

4.3 Experimental Procedure

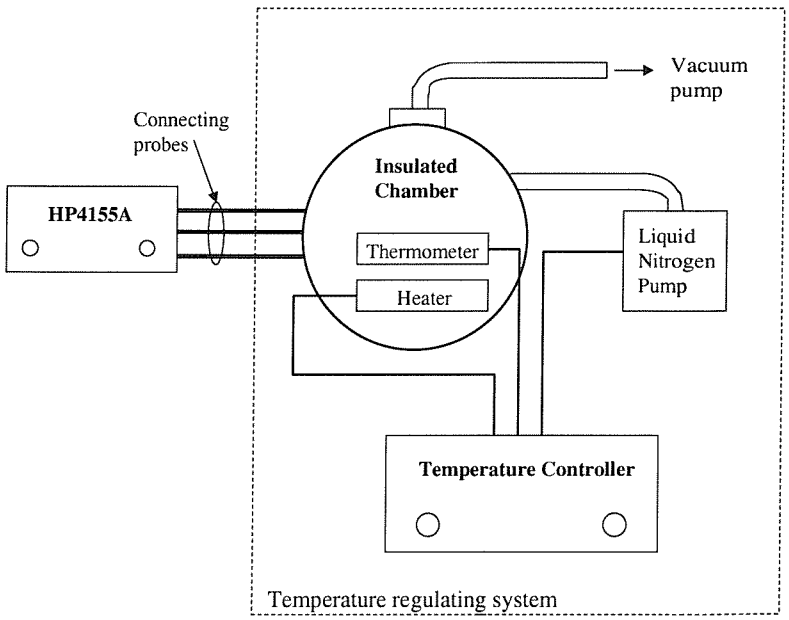

Figure 4.4: Figure shows the experimental setup for the proposed bandgap difference extraction technique. It consisted mainly of the HP4155A parameter analyzer and a temperature regulating system.

The experimental set up of the proposed measurement method is shown in Figure 4.4. It consisted of the HP4155A parameter analyzer and a temperature regulation system. The HP4155A parameter analyzer was used to supply voltages to the device terminals (i.e. emitter, base and collector) and measure currents at the device terminals through the probes. The measured device was placed on a metal plate inside the heat insulated chamber, where air was pumped out to create a vacuum environment. The temperature of the metal plate was regulated by heating it up through the heater or cooling it down using liquid nitrogen. Both the heater and the liquid nitrogen pump were controlled by the temperature controller, which monitored the metal plate temperature through a thermometer in the heat insulated chamber.

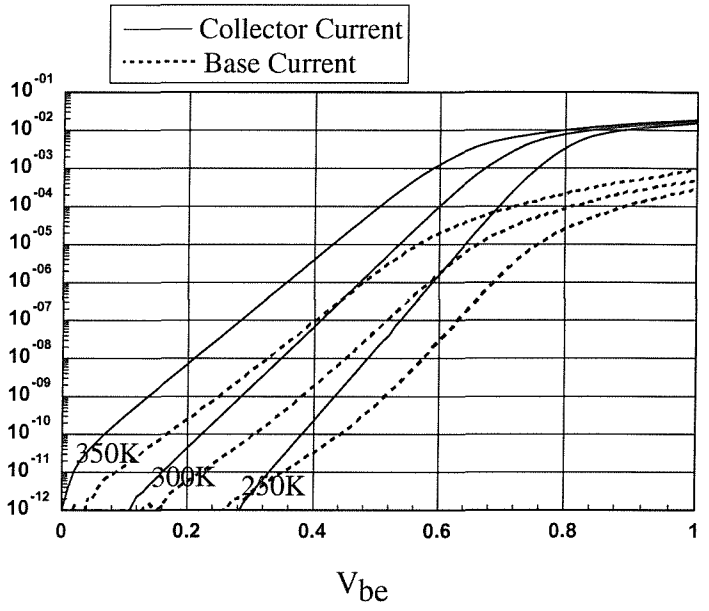

Figure 4.5: Gummel plot for increasing temperature shows that the collector and base current increases with temperature. As a result, the V_{be}^{f} has to the lowered for increasing temperature in order to maintain low operating current.

It is not uncommon to find that the actual device temperature differs from the metal plate temperature due to imperfect conduction between the metal plate and device. Also device self heating, if significant, can increase the device temperature. Therefore, device temperature is seperately measured by extracting the collector current slope in the linear region of the gummel plot, as shown in Figure 4.5. The slope is related to the device temperature as,

$$slope = \frac{q}{nkT}$$

$$T = \frac{q}{nk \times slope} \tag{4.16}$$

where n is the ideality factor of the collector current, which is reported in the G7 process report [87] as 1.007. Figure 4.6 shows the difference between the metal plate temperature, set by the temperature controller, and the device temperature. The device temperature was used for subsequent results analysis.

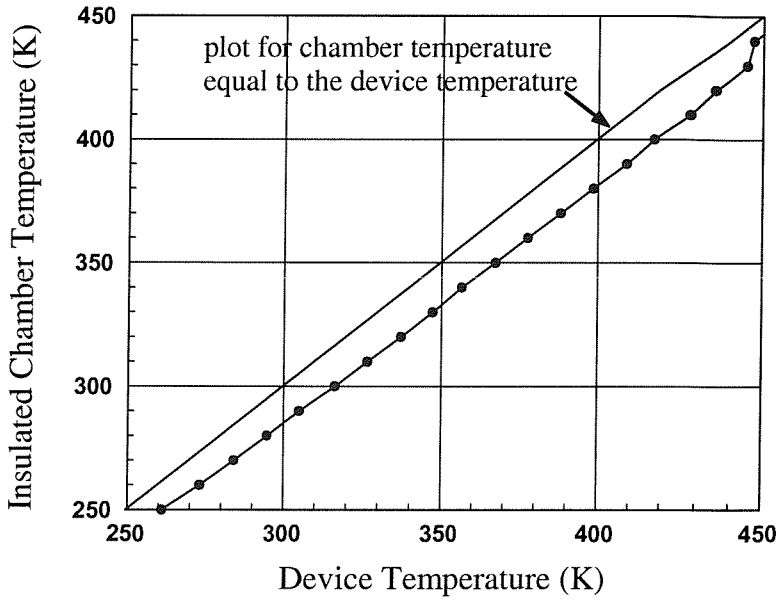

Figure 4.6: Figure shows the difference between the insulated chamber temperature (i.e. metal plate temperature) measured by thermometer and the device temperature measured using gummel plot.

To extract the forward active mode output conductance, I_c is obtained for increasing V_{ce}, in steps of 0.05 V, at fixed V_{be} bias voltage, shown in Figure 4.7. Noise was found in the collector current and therefore a five data points moving average function, built-in to the HP4155A, was performed on the collector current to filter out the noise. The output conductance was extracted from the I_c *vs* V_{ce} plot by differentiating I_c with regarding to V_{ce} between two data points that were adjacent to a certain V_{ce}; this is also a built in function of the HP4155A parameter analyzer. This was performed for the whole range of V_{ce} at fixed V_{be} bias voltage, shown in Figure 4.8, and was repeated for different temperatures. Note that because the collector and base current increase with temperature, shown in Figure 4.5, the V_{be} bias voltage was reduced for increasing temperature to maintain current operation around the micro ampere range, in order to minimise the electrically resistive effect along the current

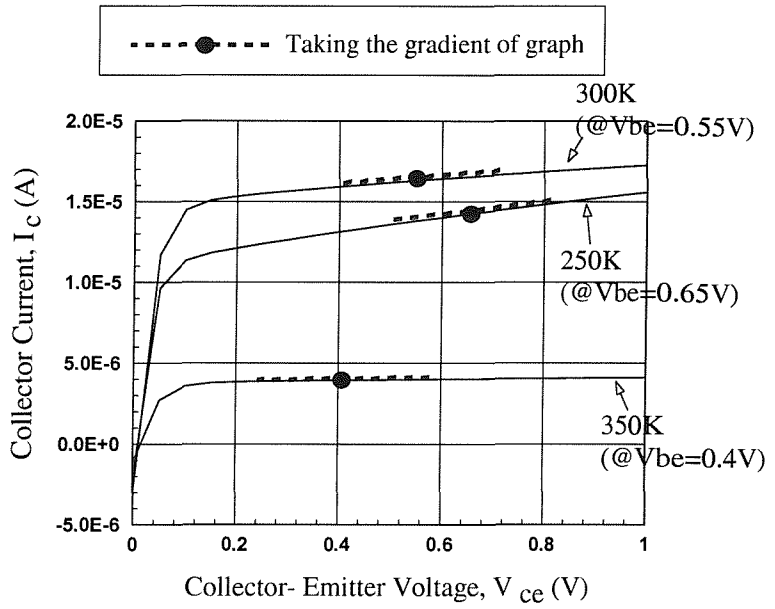

Figure 4.7: Figure illustrating dc output conductance extraction of the SiGe HBT (with 5nm spacers) for forward active operation, at 250K, 300K and 350K, by measuring the gradient of the collector bias *vs* collector current graph.

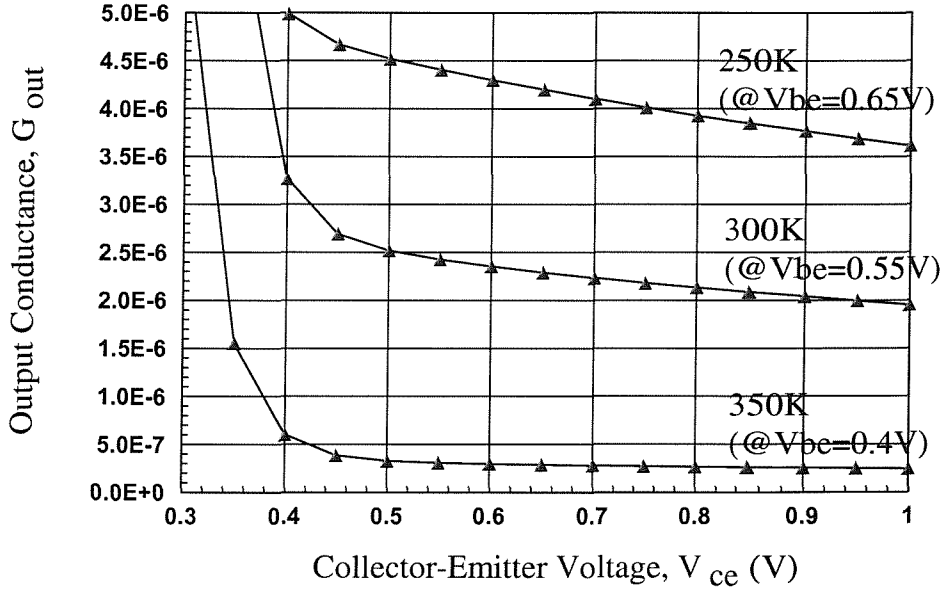

Figure 4.8: Figure showing the output conductance for increasing V_{ce}, at 250K, 300K and 350K, extracted using HP4155A parameter analyzer.

paths. Note that according to Equation 4.12, as long as V_{bc}^{r} is always equal to V_{be}^{f}, the plot of Equation 4.14 will not be affected by the difference of V_{be}^{f} used for different temperatures.

Similarly, output conductance in reverse active operation was extracted by reversing the order of biasing.

4.4 Experimental Results

The proposed technique was demonstrated experimentally using two SiGe HBT structures that were identically processed [64, 87] using low pressure chemical vapour deposition (LPCVD) with the exception that one device (Device A) had larger undoped SiGe spacer layers adjacent to the doped SiGe base region to take up boron out-diffusion from the base towards the collector and emitter regions than the other device (Device B). Figure 4.9 shows a SIMS profile of Device B which is identical to that of Device A except for the larger spacer layers in Device A. The impact of the different undoped spacer layer thicknesses on the base impurity profiles of the two devices is hardly detectable in the SIMS plot further emphasising the requirement for techniques to determine bandgap differences that do not rely on SIMS information. As can be seen in Figure 4.9, the devices were designed to have a nominally flat or constant germanium concentration across the neutral base region. The devices have measured peak germanium concentrations of 10%. The base layers were grown at $610^{o}C$, and the emitters were grown at $700^{o}C$. The nominal peak base impurity dopings were $2 \times 10^{19}\ cm^{-3}$ and polysilicon emitter contacts were used. Base layer widths, not including spacer layers, were nominally $25nm$.

Device A had 15 nm undoped spacer layers and Device B had 5 nm spacer layers, as shown in Figure 4.10. It is known from other measurement methods [88] that Device B possessed a significant parasitic potential barrier at the collector-base junction. This meant for Device B that the edge of the neutral base region on the emitter side resided in the SiGe base layer because of the high emitter doping and the edge of the neutral base region on the collector side resided in the silicon collector layer for low to moderated reverse collector-base bias voltages. An example of the conduction and

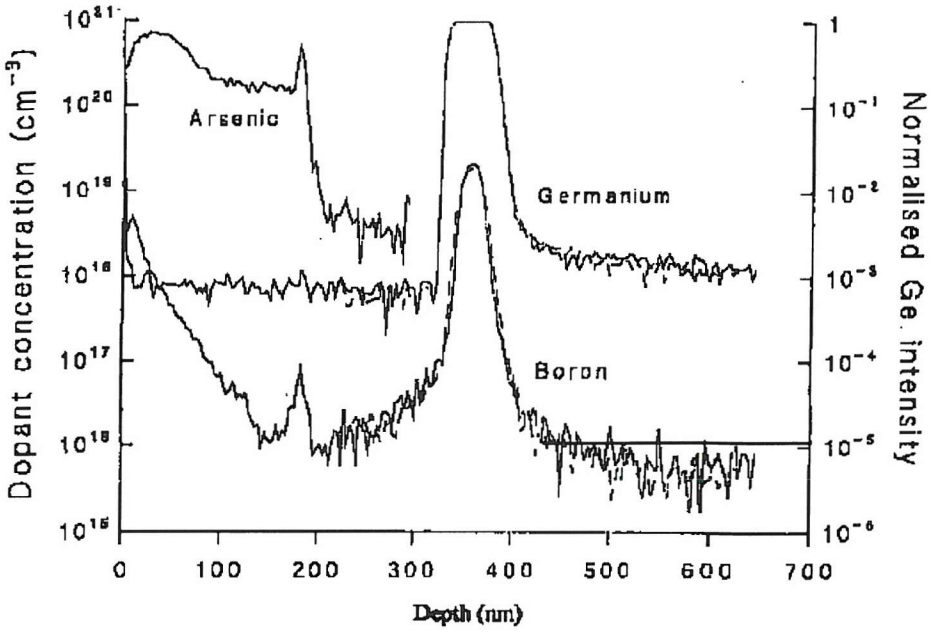

Figure 4.9: SIMS profile of Device A and Device B, used for the experimental verification of the measurement technique.

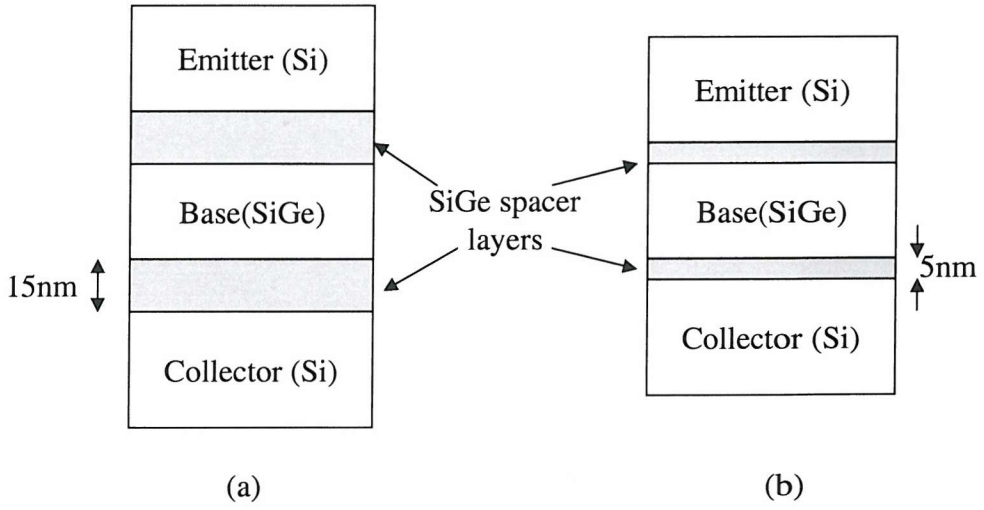

Figure 4.10: (a) Device A, with 15nm wide undoped SiGe base spacers at the emitter and collector sides of the base, used for experimental measurements, (b) Device B, with 5nm wide undoped SiGe base spacers at the emitter and collector sides of the base, used for experimental measurements.

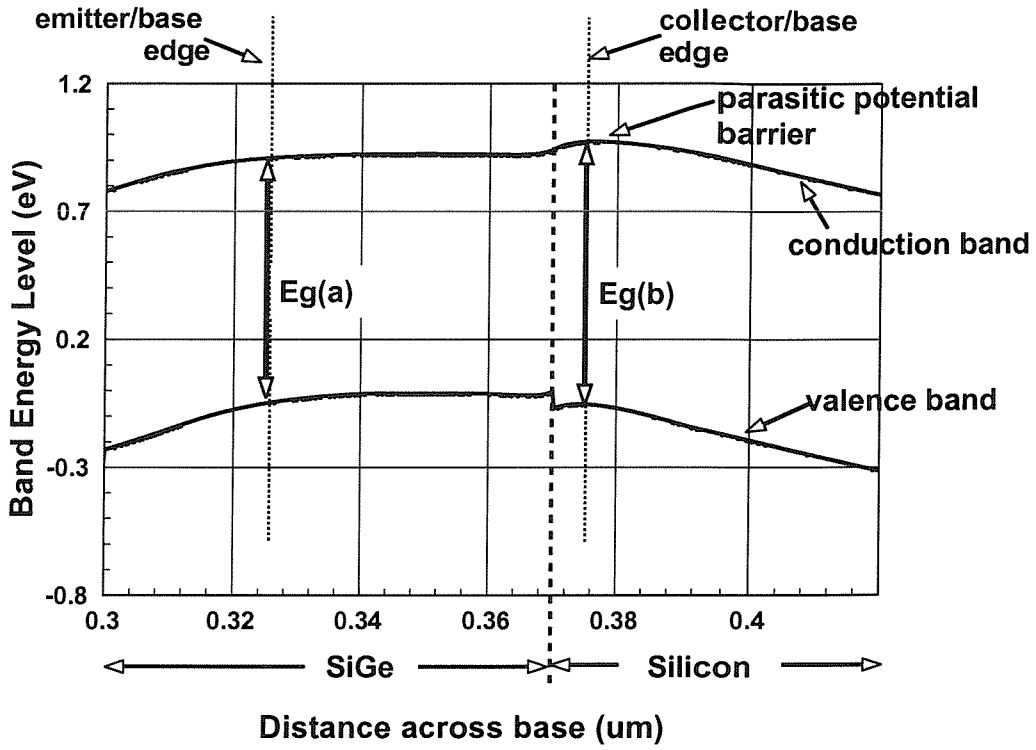

Figure 4.11: Base conduction and valence band energy diagram illustrating possible physical bandgap energy in Device B which was used in experimental measurement. It is shown that the neutral base edge at the collector side resides in the silicon region (parasitic barrier region) whereas the neutral base edge at the emitter side resides in the SiGe region. The bandgap difference across the neutral base is therefore equivalent to $E_g(a) - E_g(b)$.

valence energy bands of such device is shown in Figure 4.11, which is obtained from the semiconductor device simulator Medici [56]. On the other hand, it is known [88] that Device A exhibited behaviour commensurate with no parasitic barriers being present. This implies that both edges of the neutral base would be expected to reside within the SiGe base layer in Device A. For this reason it is expected that there should be a significant bandgap difference across the neutral base region for Device B and not a significant difference for Device A.

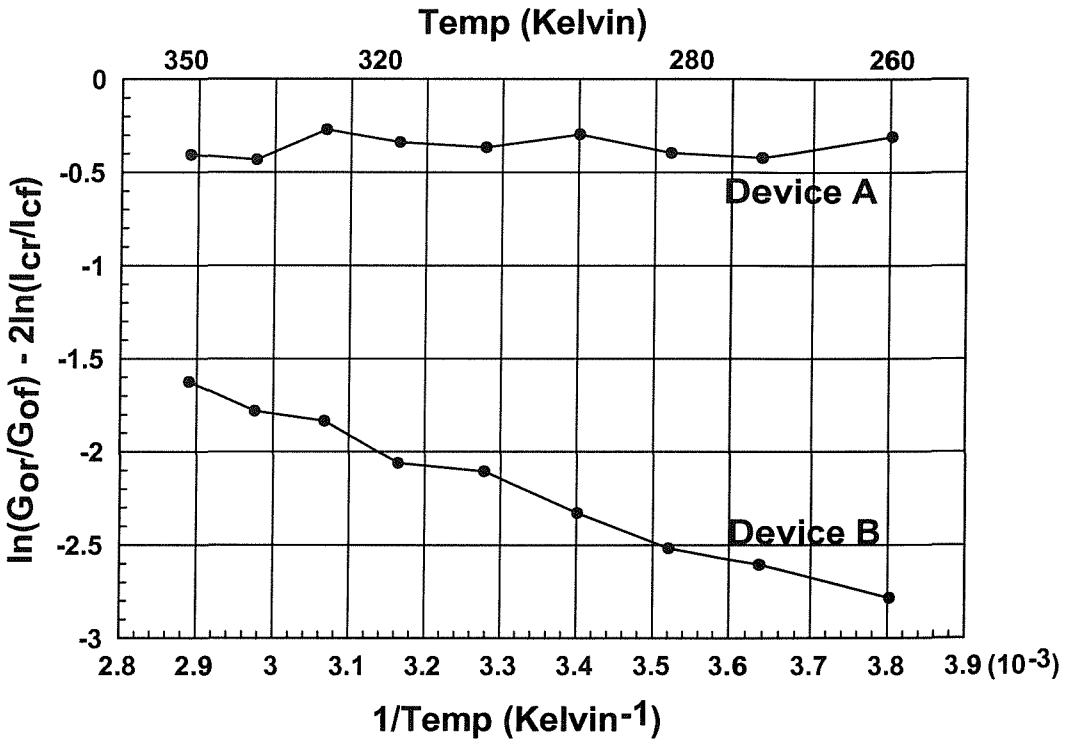

Figure 4.12: Experimental results obtained for Device A (15nm spacers) and Device B (5nm spacers), where bandgap grading across the neutral base (slope of graph) are extracted and found to be 0.002 eV and -0.104 eV respectively. The slopes of the curves give the bandgap difference across the neutral base divided by Boltzmann's constant k for each case. Note that a negative slope indicates a retarding electric field and a positive slope indicates a positive retarding electric field in the base.

From the experimental results, shown in Figure 4.12, the bandgap difference across the neutral base was extracted to be 0.002 eV increasing for Device A and 0.104 eV retarding for Device B. This implies that there is almost no bandgap grading across the neutral base for Device A and that the 15 nm SiGe spacer layers are adequate to contain the base boron diffusion in Device A. For Device B base boron out-diffusion has caused a bandgap difference between the silicon and SiGe regions in the neutral

base of 0.104 eV. This is due to the combined effects of bandgap reduction due to a nominal incorporation of 10 % strained germanium during fabrication [42] and heavy base doping of 10^{19} cm^{-3} [83] in the SiGe portion of the neutral base compared to the lower doped silicon side of the neutral base. Note that a negative slope indicates a retarding electric field and a positive slope indicates an accelerating electric field in the base.

It is interesting to consider an error analysis of the proposed measurement technique. For the experimental results presented it was found that the influence of the junction capacitances were negligible. If the junction capacitances could not have been neglected, a straight line plot would not have been obtained in the preceding data due to the non-linear influences of the differences in temperature dependencies of the emitter-base and collector-base junction capacitance terms. Neglecting the temperature variations of ratios of junction capacitances as well as mobility, density of states and the bias terms, Equation 4.12 becomes,

$$\ln\left(\frac{g_{or}}{g_{of}}\right) - 2\ln\left(\frac{I_{cr}}{I_{cf}}\right) = \frac{\Delta E_g(grade)}{kT} \tag{4.17}$$

where $\Delta E_g(grade) = E_g(0_r) - E_g(W_f)$. Using simple error propagation analysis, the absolute uncertainty in measuring the bandgap difference across the neutral base region $\delta\Delta E_g(grade)$ can be expressed in terms of the relative uncertainties in measuring g_{or}, g_{of}, I_{cr} and I_{cf} such that, also elaborated in Appendix C.2,

$$\begin{aligned}\delta\Delta E_g(grade) &= kT\left[\left(\frac{\delta g_{or}}{g_{or}}\right) + \left(\frac{\delta g_{of}}{g_{of}}\right) + 2\left(\frac{\delta I_{cr}}{I_{cr}}\right) + 2\left(\frac{\delta I_{cf}}{I_{cf}}\right)\right] + \\ &\quad \left(\frac{\delta T}{T}\right)\Delta E_g(grade)\end{aligned} \tag{4.18}$$

For the case where $\Delta E_g(grade) = 0.1eV$, assuming that the relative accuracy of measuring g_{or}, g_{of}, I_{cr} and I_{cf} are each 5% (i.e $\delta g_{or}/g_{or} = \delta I_{cr}/I_{cr} = \delta I_{cf}/I_{cf} = \delta T/T = 0.05$), the absolute uncertainty in measuring $\Delta E_g(grade)$ becomes at 300 degrees K,

$$\delta\Delta E_g(grade) = 0.3kT + 0.05\Delta E_g(grade) = 0.013eV \tag{4.19}$$

This degree of uncertainty would correspond to approximately 1.5 % germanium grading using strained SiGe [42].

4.5 Numerical Results

Numerical simulations were conducted on a number of different idealised SiGe HBT structures in order to demonstrate the potential uses of the proposed technique. The principle motivation for conducting the numerical simulations is to explore the possibility of using the proposed technique in two situations, namely (1) to measure bandgap grading in purposely linearly graded SiGe HBT's, and (2) to assess the impact of impurity related bandgap narrowing on overall bandgap variation in non-graded heavily-doped SiGe HBT's. These simulations are not intended to model the experimental device in the previous section. An attempt to model the experimentally measured device would merely be an elaborate curve-fitting exercise due to the large selection of models and model parameters which are available for mobility, bandgap grading, and lifetime. Indeed, the principle advantage of the proposed technique to measure bandgap difference across the neutral base region is the lack of requirement for knowledge of the various dependencies of these effects on doping, temperature, and germanium concentration.

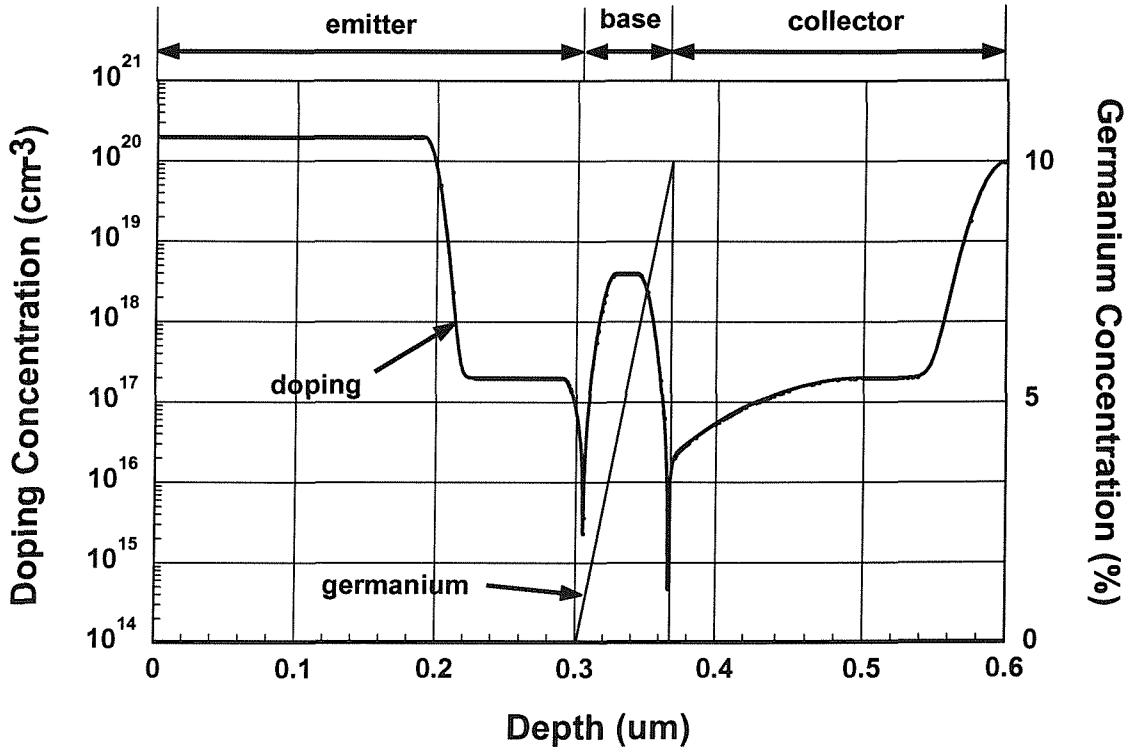

Figure 4.13: Net impurity profile for high performance device structure from [11], used in numerical simulations to produce the results shown in Figures 4.14 and 4.16.

One useful application of the proposed technique is to determine the amount of bandgap grading that would result in a purposely graded SiGe HBT. A realistic device structure intended for superior analogue circuit performance [11], as shown in Figure 4.13, was used to demonstrate the technique with the exception that the germanium grading was altered for the numerical simulations. The device has peak base doping of $4 \times 10^{18} cm^{-3}$ and a metallurgical base width of 70 nm. Figure 4.14 shows numerical simulation data plotted using Equation 4.14 for the device profile of Figure 4.13 with 10% linearly graded germanium in the base between the metallurgical junctions from the emitter increasing towards the collector. Different curves are shown for various terms in Equation 4.14 where curve #1 represents the output conductance ratio term, curve #4 represents the collector current ratio term and #5 represents the capacitance ratio term. A zero bias was used across the reverse biased junction of the transistor for forward and reverse active operation. Collector current was adjusted to ensure operation below the onset of high current effects and to minimise the influence of terminal series resistance loss. Simulation results are shown for temperatures between 340 K and 220 K. As shown in Figure 4.14, curves #2 and #3 are extremely linear and ideal over the whole temperature range. For this device, only the output conductance and current terms needed to be accounted for as the ratio of the junction capacitances (curve #5) was found to be virtually temperature independent.

The positive slopes of the curves #2 and #3 in Figure 4.14 indicate that the bandgap at the collector-base edge of the base region is 0.023 eV smaller than at the emitter-base edge. This result is reasonable taking into account the fact that the space charge layer intrusions into the neutral base will reduce the overall amount of bandgap grading below the 10 % defined between metallurgical junctions. This was confirmed from inspecting internal bandgap information from the numerical simulator, shown in Figure 4.15, where the bandgap variation across the metallurgical base, for germanium concentration increasing from 0 to 10 % linearly, is plotted. With the approximated base electrical junctions, the bandgap difference across the neutral base is found to be 0.022 eV.

Figure 4.16 shows numerical simulation results of plotting Equation 4.14, excluding the capacitive term, for various amount of linear germanium grading. The positive

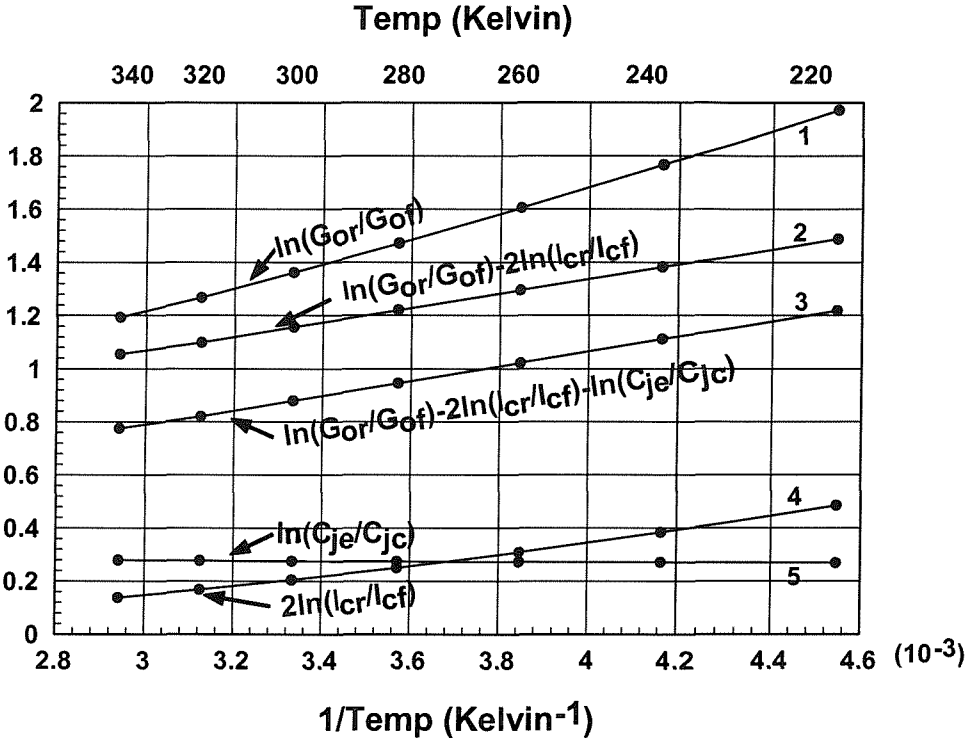

Figure 4.14: Numerical simulations of Equation 4.14 for the device structure shown in Figure 4.13, where various terms are included. The germanium grading between metallurgical junctions was 10% increasing towards the collector. The slopes of curves #2 and #3 give the bandgap difference across the neutral base divided by Boltzmann's constant k. The positive slope indicates that the bandgap is smaller by 0.023 eV at the collector side of the neutral base region than at the emitter side in agreement with the internally defined device in the 2-D numerical simulation.

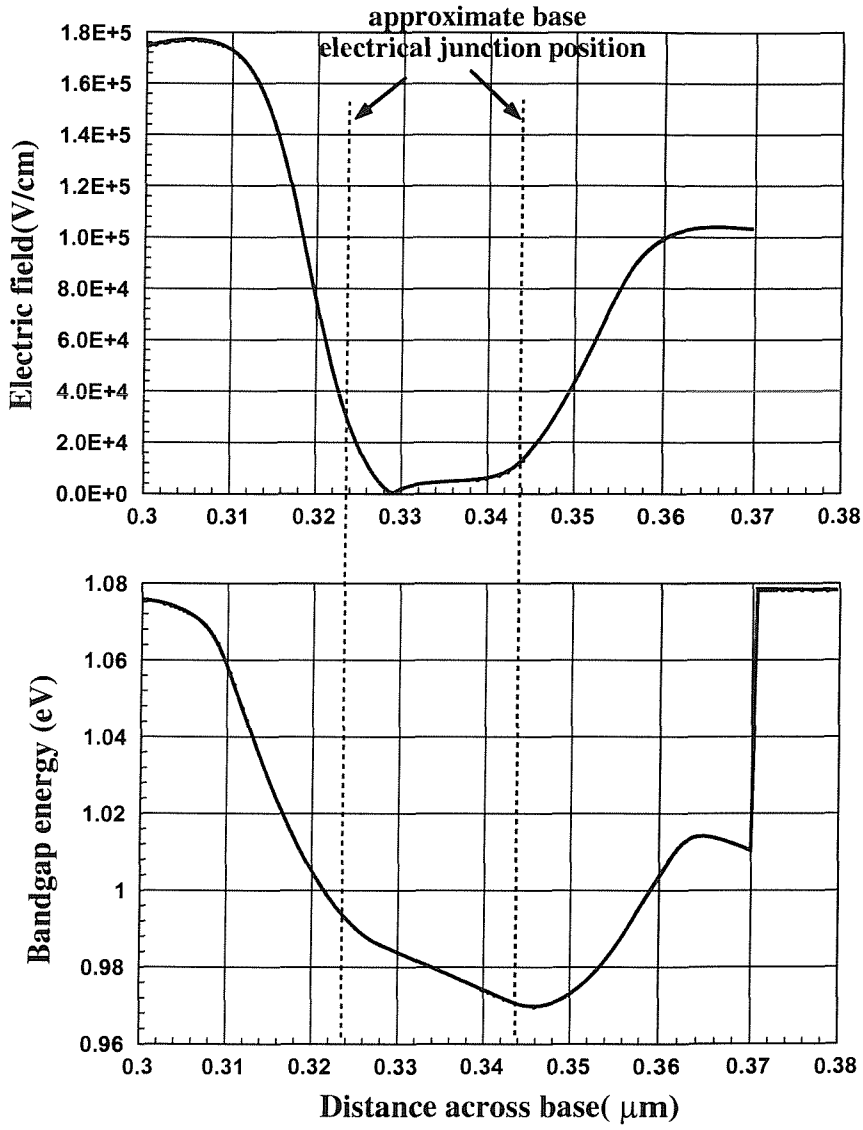

Figure 4.15: Plot showing the bandgap variation across the base metallurgical junction, where germanium concentration increases from 0 to 10% linearly towards the collector, for device structures shown in Figure 4.13. With the approximated base electrical junctions positions using the electric field across the base for zero bias collector-base and emitter-base junctions, the bandgap difference across the neutral base is found to be 0.022 eV.

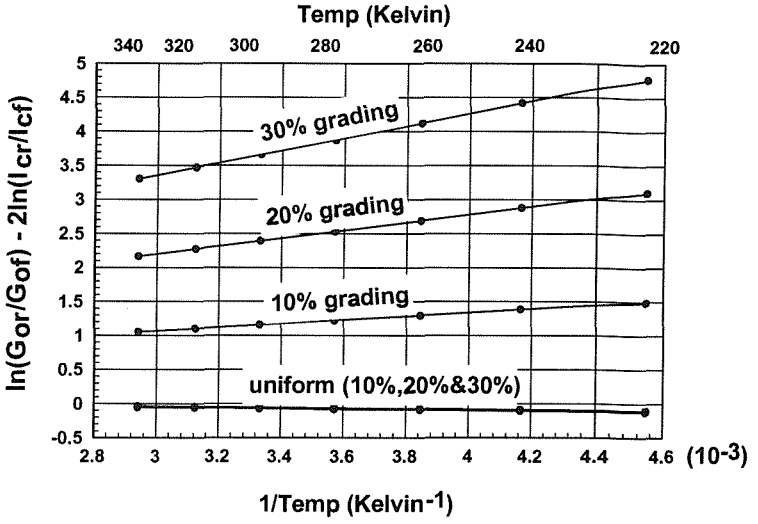

Figure 4.16: Numerical simulations demonstrating the bandgap grading measurement technique for the device structure show in Figure 4.13. Without taking into consideration the capacitance term in Equation 4.14, results for various amounts of bandgap grading are shown. The slopes of the curves give the bandgap difference across the neutral base divided by Boltzmann's constant k for each case.

slope increases as expected for increasing amounts of germanium grading and bandgap differences across the neutral base of 0.023 eV, 0.051 eV and 0.080 eV were found for germanium grading of 10%, 20% and 30% across the metallurgical base, respectively. Note that the small negative slopes noticed even for uniform germanium dopings are explained below.

The technique is also useful for assessing the effects of impurity related bandgap reduction on the overall bandgap variation across the neutral base. Other than Ge, the base bandgap is also affected by high impurity doping and could be significant where impurity doping increased above $10^{17}cm^{-3}$. Because of its increased emitter injection efficiency, SiGe HBT's usually have high base doping which improves the output resistance and reduces the base resistance. With the aid of numerical simulations the proposed technique was used to investigate the heavy doping effects on bandgap grading for a SiGe HBT designed for optimum speed such as that shown in Figure 4.17, which is similar to that of [2]. The device had a uniform bandgap reduction (or "box") germanium profile across the neutral base region to maximise f_T [80], a highly doped base with peak doping $3 \times 10^{19}cm^{-3}$ to minimise base resistance, and a metallurgical base width of $800A^0$.

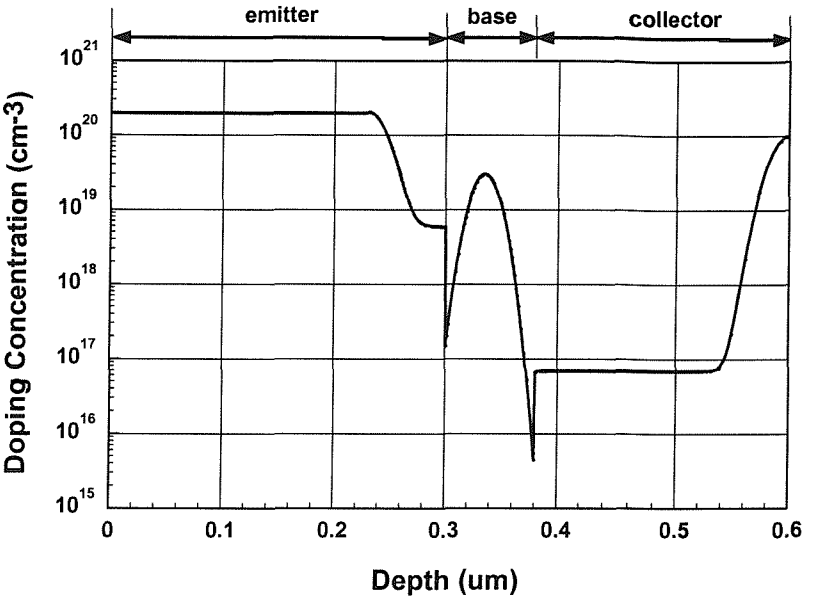

Figure 4.17: Net impurity profile of high speed device structure from [2], used in numerical simulations to produce the results shown in Figures 4.18 to 4.20.

High base doping often leads to a non-uniform base impurity profile due to diffusion effects [21]. Therefore, the bandgap across the neutral base can be unintentionally graded by the non-uniform impurity-induced bandgap narrowing. Figure 4.18 shows numerical simulation results where various terms in Equation 4.14 are plotted for 20% uniform germanium concentration in the base. By including the influence of junction capacitance (curve #1) a straight line plot (curve #5) in Figure 4.18 is obtained which indicates that there is an unintentional net *increase* in bandgap of approximately 0.014 eV across the neutral base, from the emitter to the collector. This is confirmed by Figure 4.19 showing the simulated bandgap, E_g, across the neutral base. Figure 4.19 shows that even though the germanium concentration across the base is uniform and therefore uniformly reduces the base bandgap, the resultant base bandgap is by no means uniform. It indicates that impurity-induced bandgap narrowing can significantly affect the base bandgap and, in this case, is responsible for the unwanted retarding bandgap between the emitter and collector edge of the neutral base. This is equivalent to a decreasing germanium grading from emitter to collector edges of the neutral base region of roughly 1.5%, which can significantly increase the base transit time above the optimum value if this situation were allowed to exist in an actual fabricated device. From the error analysis of the previous sec-

tion, it is clear that the relative error in the measured parameters g_{of}, g_{or}, I_{cf}, I_{cr} and T would have to be better than 5 % to be able to detect this degree of bandgap difference.

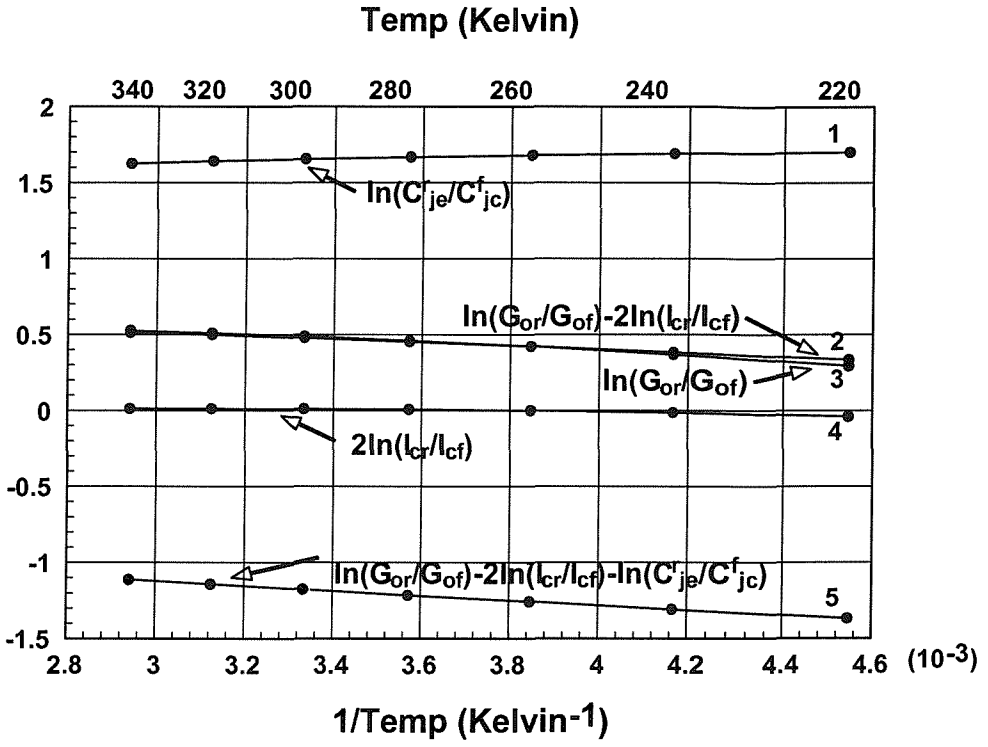

Figure 4.18: Numerical simulations of Equation 4.14 for the device structure shown in Figure 4.17 for 20% uniform germanium concentration in the base, where various terms are included. The slope of curve #5 gives the bandgap difference across the neutral base divided by Boltzmann's constant k. The negative slope of curve #5 indicates that the bandgap is larger by 0.014 eV at the collector side of the neutral base region than at the emitter side.

Figure 4.20 demonstrates how the proposed experimental technique can be used to optimise the germanium grading in such a device to minimise any adverse effects of impurity-induced bandgap grading. It shows numerical results where the full Equation 4.14 is plotted for various germanium profiles. The near horizontal line in this figure labelled "4% grading" indicates that approximately 4% to 5% germanium grading between metallurgical junctions increasing towards the collector should be used to counteract the adverse influence of impurity-induced bandgap grading for optimum transistor performance.

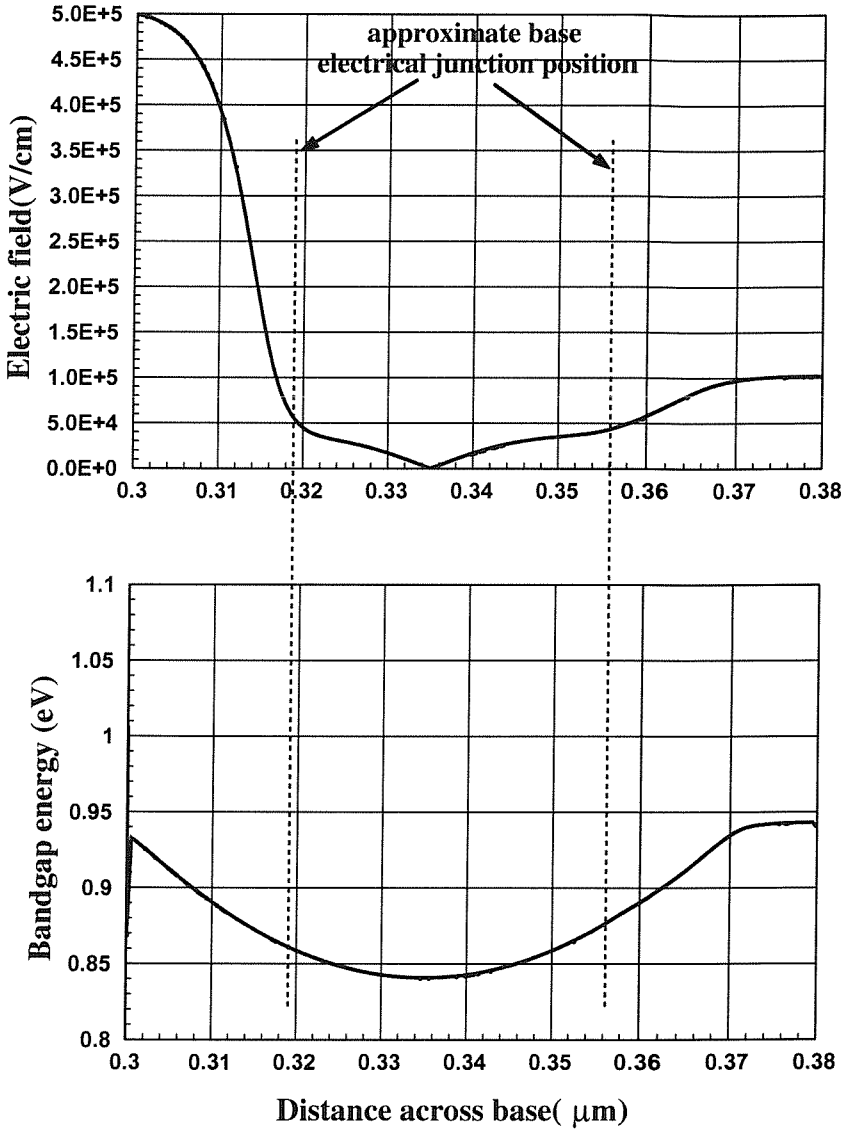

Figure 4.19: Numerical simulation results showing the variation in bandgap energy across the neutral base region due to both germanium and impurity induced bandgap reduction for the device impurity profile shown in Figure 4.17. With the approximated base electrical junctions positions using the electric field across the base for zero bias collector-base and emitter-base junctions, the bandgap difference across the neutral base is found to be 0.015 eV.

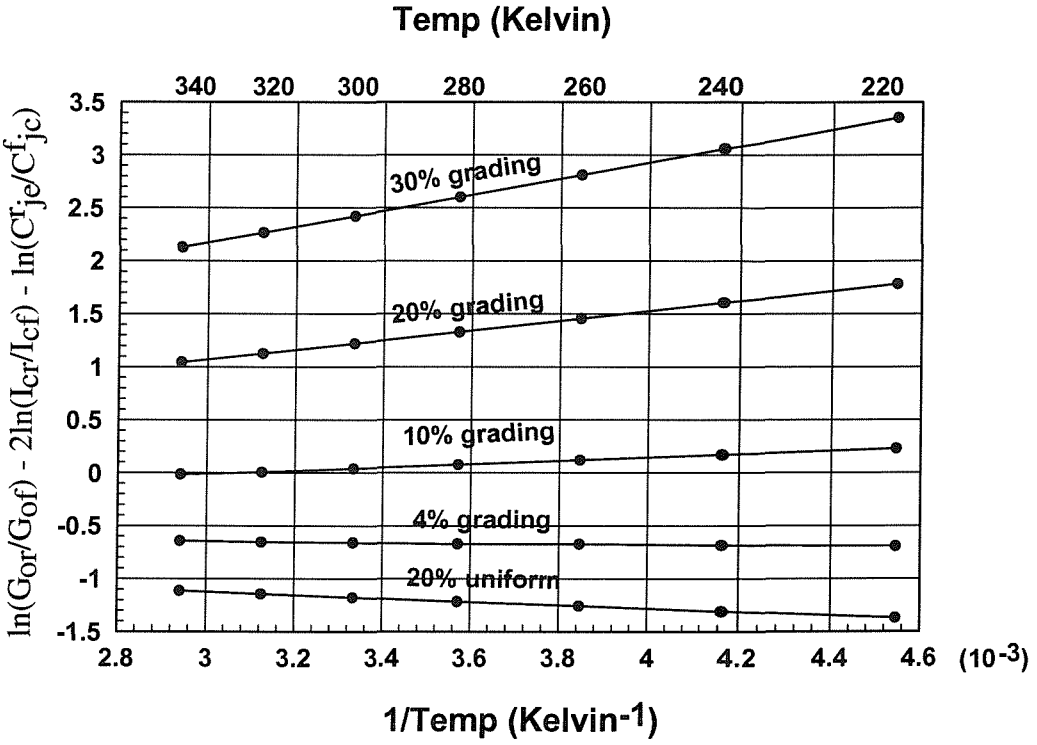

Figure 4.20: Numerical simulations demonstrating the bandgap grading measurement technique for the device structure shown in Figure 4.17 where results for various amount of bandgap grading are shown. The slopes of the curves give the bandgap difference across the neutral base divided by Boltzmann's constant k for each case.

4.6 Conclusion

A simple new low frequency electrical method to measure directly the bandgap difference between the electrical edges of the neutral base in a SiGe HBT has been presented. This method can be used to measure the effective bandgap grading due to the presence of germanium, including the effects of heavy doping. Detailed numerical simulations were used to demonstrate the usefulness of the technique to determine bandgap differences across the neutral base in a variety of practical situations. Experimental measurements on fabricated LPCVD SiGe HBT's verify that the technique can accurately measure the bandgap difference across the neutral base in devices with parasitic potential barriers.

The proposed electrical technique should prove useful in rapidly verifying bandgap grading, or absence of it, in industrial SiGe process development obviating the need for SIMS data, detailed numerical modelling, or control devices. The technique should also prove useful in process monitoring in established SiGe processes.

Chapter 5

An Experimental Method for Simultaneous Extraction of Parasitic Potential Barrier Heights at Emitter-Base and Collector-Base Junctions of SiGe HBT's

5.1 Introduction

The introduction of SiGe as the base in silicon bipolar transistors can greatly improve the performance of a bipolar transistor. This is due to the effect of bandgap narrowing induced in the transistor base by the strained SiGe layer. By adopting SiGe base technique, a thin, highly doped base can be used to reduce the transit time in the base without compromising the base resistance or the emitter injection efficiency. Also, by controlling the germanium profile the bandgap narrowing can be controlled to improve transistor's performances such as lower base resistance, higher cut-off frequency and higher Early voltage [9]. However, small amounts of boron out-diffusion

from the heavily doped base into the emitter and collector regions can seriously degrade the collector current, Early voltage and cut-off frequency enhancement by forming parasitic potential barriers for electrons in the conduction band at the Si/SiGe interface. These may occur during device processing because the base dopant diffuses faster than germanium. Therefore, information about the parasitic barrier that exists in a SiGe HBT is valuable when it comes to device and process modelling.

In this chapter, an alternative electrical method for simultaneous extraction of parasitic potential barrier heights at the emitter-base and collector-base junctions of SiGe HBT's is presented. The theory behind the proposed new method to extract parasitic barrier heights is presented. The method is, firstly, verified numerically by means of full numerical simulation using the Medici [56] semiconductor solver where a device with parasitic barriers are simulated. Then, by applying the method experimentally on a chosen n-p-n SiGe HBT suspected of having parasitic potential barriers due to boron out-diffusion, the method is experimentally demonstrated. The experimental results are further confirmed by full numerical modelling using the SIMS profile of the measured n-p-n SiGe HBT in Medici. Finally, conclusions will be drawn.

Device processing has to be optimised carefully, to avoid boron out-diffusion from the SiGe base layer into either or both the emitter and collector silicon layers [20]. Base dopant, especially when in the presence of implantation damage, diffuses faster than germanium during layer growth and subsequent device processing. This can result in boron out-diffusion where high boron dopant is found outside the SiGe region [20]. When this happens, parasitic energy barriers are formed at the collector-base and emitter-base junctions [17, 18]. They can impair the heterojunction action and can lead to a much smaller enhancement of collector current than would otherwise be expected. Slotboom *et al.* [20] have shown that the existence of parasitic energy barriers can severely degrade the cut-off frequency, the Early voltage and the collector current. Therefore, extra processing steps were taken to avoid the formation of parasitic energy barriers. Prinz *et al.* [18, 21] have shown that the boron out-diffusion can be controlled to some extent by introducing undoped SiGe spacers adjacent to the p^+ SiGe base. The idea is to allow more space in the base for boron to diffuse thus still keeping the boron base doping inside the SiGe base region, illustrated in

Figure 5.1. This has the effect, however, of increasing the overall thickness of the SiGe layer and hence imposes a tighter constraint on the amount of germanium that can be introduced [42].

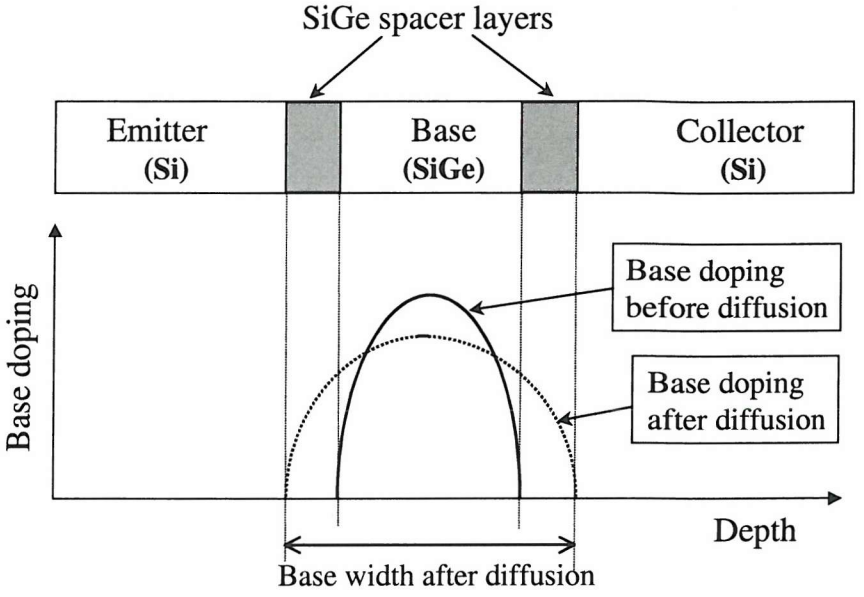

Figure 5.1: Figure showing the diffusion of boron doping from it's original position and the use of SiGe spacer layers to contain the base boron doping inside the SiGe base region.

It has been shown by Slotboom *et al.* [20] and Le Tron [21] that the parasitic barrier height can be estimated by analysing the temperature dependence of the collector current, presented in Section 2.5.1 and 2.5.2. Slotboom *et al.* assume uniform box-like germanium and boron doping profile and Le Tron *et al.*, who adapted the Slotboom *et al.* method, also assume uniformly doped germanium profile. In both cases, accurate modelling of the temperature dependence of the silicon and SiGe density of states and carrier mobility were employed. A control device with no parasitic barriers was used to determine the total bandgap narrowing due to germanium and heavy doping effects. The extraction of the parasitic barrier height relied on comparing the bandgap narrowing of two similar SiGe HBTs, except where one had a parasitic barrier and one did not.

Here, the method in [20, 21] is refined [22] by using the temperature dependence of the ratio of the small signal a.c. output conductance in forward and reverse active operation as opposed to using the temperature dependence of the collector current.

In contrast to using collector current [20, 21], if barriers exist on both sides of the base it will be shown that the new proposed method is capable of independently determining the height of each without the need for comparison to a control device. Also the use of ratios of the output conductances eliminates the need for knowledge of the temperature dependence of internal physical properties such as the density of states and carrier mobility. This feature is especially advantageous since such physical properties of SiGe are not well known at this time.

5.2 Theory

In this chapter, the electrical method proposed in Chapter 4 is extended to measure the parasitic energy barrier height. The proposed electrical method of Chapter 4 measures the difference of bandgap in the base between the collector electrical junction in forward active operation and the emitter electrical junction in reverse active operation, as illustrated in Figure 5.2. It was shown in Chapter 4 [15] that the ratio of the small signal low frequency output conductances of a bipolar transistor operated in the forward and the reverse active mode is given by (i.e. Equation 4.11 of Chapter 4),

$$\frac{g_{or}}{g_{of}} = \left(\frac{I_{cr}}{I_{cf}}\right)^2 \left(\frac{C_{je}^r}{C_{jc}^f}\right) \left(\frac{D_{nb}(W_f)}{D_{nb}(0_r)}\right) \exp\left(\frac{V_{be}^f - V_{bc}^r}{V_T}\right) \left(\frac{N_c(W_f)N_v(W_f)}{N_c(0_r)N_v(0_r)}\right) \exp\left(\frac{E_g(0_r) - E_g(W_f)}{kT}\right) \tag{5.1}$$

where the "f" and "r" subscript or superscript denote parameters for forward and reverse active operation, respectively. g_o is the a.c output conductance, I_c is the d.c. collector current, C_{je} is the emitter-base depletion capacitance, C_{jc} is the collector-base depletion capacitance, D_{nb} is the base diffusivity of electrons, V_{be} is the emitter-base bias voltage, V_{bc} is the collector-base bias voltage, V_T is the thermal voltage, N_c and N_v are the effective density of states in the conduction and valence band, respectively, T is temperature and k is the Boltzmann's constant. $E_g(0_r) - E_g(W_f)$ is the bandgap difference between the collector-base junction edge of the neutral base in forward operation (W_f) and the emitter-base junction edge of the neutral base

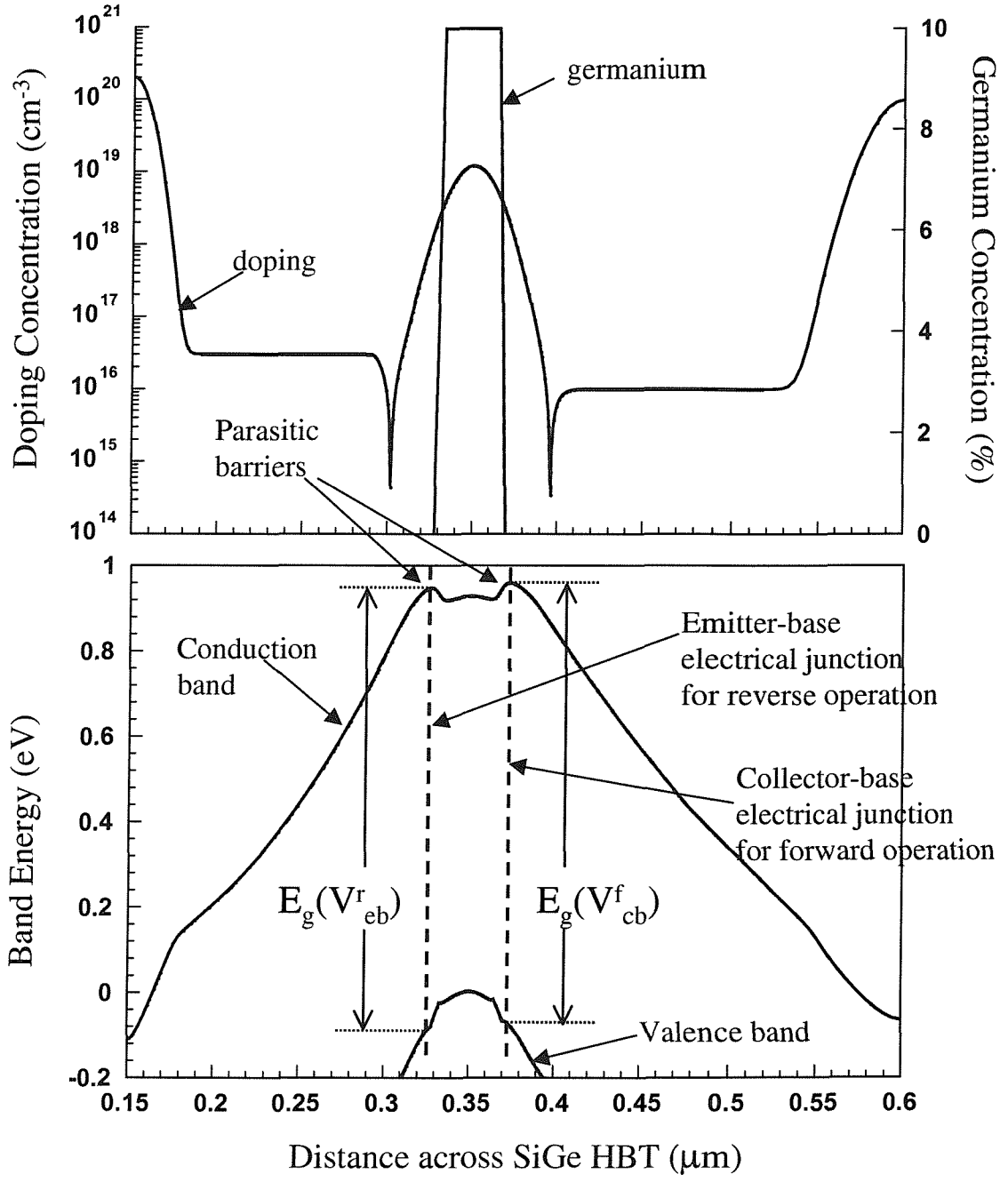

Figure 5.2: Figure illustrates, with the aid of numerical simulations [56], the effect of doping profile and germanium concentration on the base conduction and valence energy bands for a SiGe HBT where boron out-diffusion exists. Parasitic barriers are shown to exist at zero bias. The positions of $E_g(V_{cb}^f)$ and $E_g(V_{eb}^r)$ used in Equation (5.2) are also indicated.

in reverse operation (0_r). Since W_f and 0_r are dependent on the forward active collector-base reverse bias voltage, V_{cb}^f, and reverse active emitter-base reverse bias voltage, V_{eb}^r, respectively, Equation 5.1 can be written as:

$$\frac{g_{or}}{g_{of}} = \left(\frac{I_{cr}}{I_{cf}}\right)^2 \left(\frac{C_{je}^r}{C_{jc}^f}\right) \left(\frac{D_{nb}(W_f)}{D_{nb}(0_r)}\right) \exp\left(\frac{V_{be}^f - V_{bc}^r}{V_T}\right) \left(\frac{N_c(W_f)N_v(W_f)}{N_c(0_r)N_v(0_r)}\right) \exp\left(\frac{E_g(V_{eb}^r) - E_g(V_{cb}^f)}{kT}\right) \tag{5.2}$$

$E_g(V_{eb}^r) - E_g(V_{cb}^f)$, shown in Figure 5.2, can be measured directly by plotting

$$\ln\left(\frac{g_{or}}{g_{of}}\right) - 2\ln\left(\frac{I_{cr}}{I_{cf}}\right) - \ln\left(\frac{C_{je}}{C_{jc}}\right) \text{versus} \frac{1}{kT} \tag{5.3}$$

and then extracting the slope of the plot. Therefore, by analysing the temperature dependence of the output conductances in the forward and reverse active operation, the bandgap difference between the edges of the neutral base, $E_g(V_{eb}^r) - E_g(V_{cb}^f)$, can be extracted.

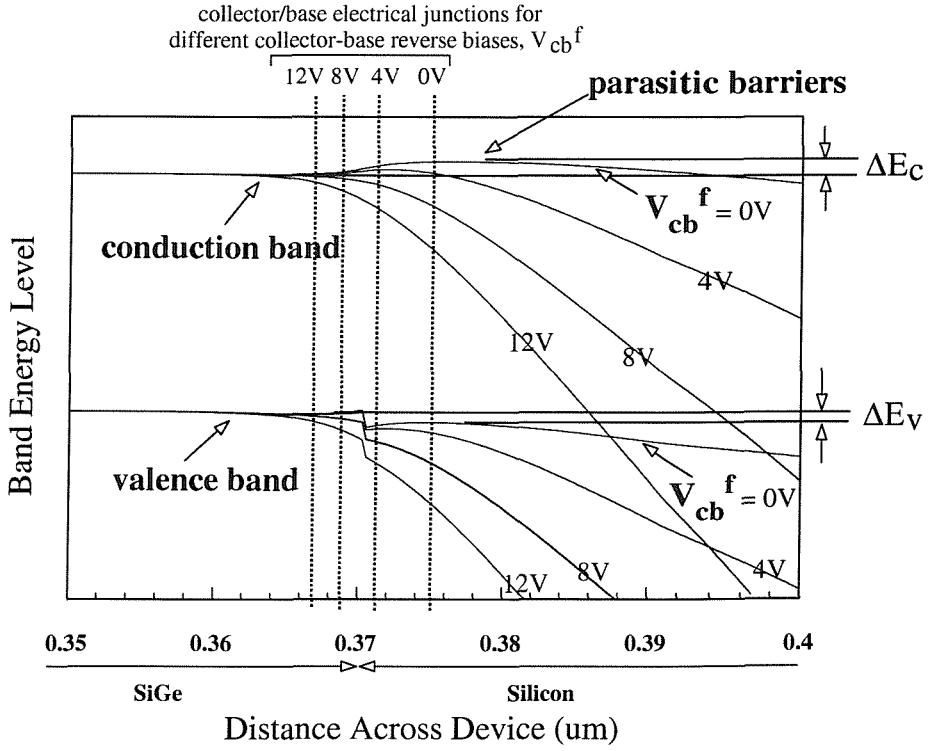

Figure 5.3: Figure illustrates, with the aid of numerical simulations [56], the dependence of the collector-base parasitic barrier's shape on V_{cb}^f. It shows the movement of the electrical junction with regards to V_{cb}^f, and also how the parasitic energy barrier can be lowered by increasing V_{cb}^f. ΔE_c and ΔE_v are also indicated.

The shape of the parasitic barrier is dependent on and varies according to the junction bias voltages, as shown in Figure 5.3. Note that Figure 5.3 is from numerical simulation results [56] of a realistic SiGe HBT structure and is used for the purpose of explaining the measurement method. This change of shape is due to space charge layer expansion or reduction, depending upon whether the junction is more reverse biased or forward biased, respectively [20]. When the space-charge layer expands, the parasitic barrier height and width decreases due to space-charge layer encroachment, whereas when the space-charge layer reduces, the parasitic barrier height and width increases. Note that the position of the electrical junctions, which always follows the peak of the parasitic barriers, varies according to the shape of the parasitic barrier.

In this chapter, the low frequency method mentioned in Chapter 4 [15] was used to monitor the change of bandgap energy difference across the neutral base with regards to the electrical junction position controlled by the junction bias voltage, shown in Figure 5.3. The collector-base junction parasitic energy barrier can be profiled by holding the reverse active operation reverse bias voltage V_{eb}^{r} constant, so that the emitter-base junction bandgap $E_g(V_{eb}^{r})$ can be used as a reference, and then increasing the forward active operation reverse bias voltage V_{cb}^{f} which will cause the collector-base space charge layer edge to sweep through the parasitic energy barrier. The low frequency method to extract $E_g(V_{eb}^{r}) - E_g(V_{cb}^{f})$ was used at every increment of V_{cb}^{f} to monitor the bandgap changes. V_{cb}^{f} was increased until the parasitic energy barrier completely disappeared, resulting in barrier "push-through", as shown in Figure 5.3, where the collector-base electrical junction resided in the SiGe region for high V_{cb}^{f} and the bandgap difference across the neutral base was free from the effects of the parasitic energy barrier. The total bandgap change at the collector side of the neutral base edge, ΔE_g, over the change in applied V_{cb}^{f} can be extracted from plotting Equation 5.3 with regarding to V_{cb}^{f}.

ΔE_g is equivalent to the summation of the changes at the conduction band, ΔE_c, and the changes at the valence band ΔE_v, as shown in Figure 5.3.

$$\Delta E_g = \Delta E_c + \Delta E_v \tag{5.4}$$

ΔE_c results from the effects of germanium and doping induced bandgap narrowing

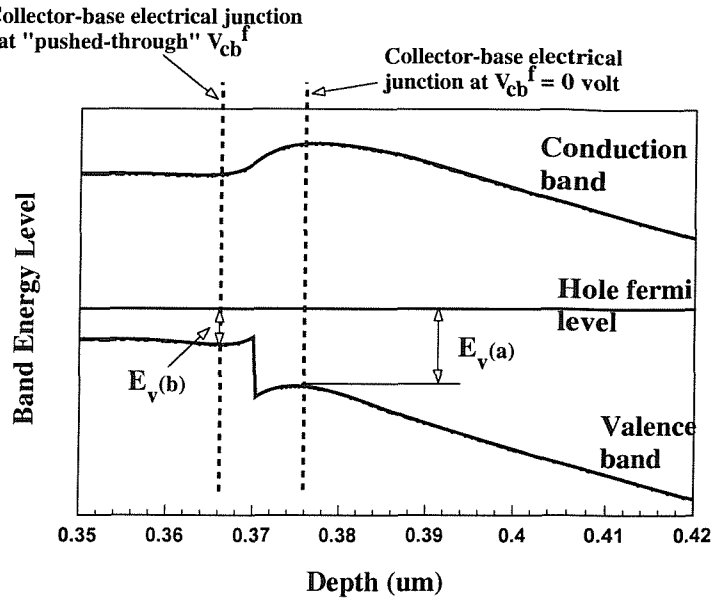

Figure 5.4: Figure showing the valence band variation at the collector-base junction due to non-uniform base doping. The offset between the hole fermi level and the valence band decreases with increasing V_{cb}^f and the total valence band changes, ΔE_v, is equivalent to $E_v(a) - E_v(b)$.

on the base conduction band, manifested as a parasitic energy barrier. ΔE_v is due to the effect of p-type dopant variation with position at the base. The majority carrier (hole) Fermi level in the base is held constant across the Si-SiGe transition region by the emitter-base voltage. If the base impurity concentration is decreasing across the Si-SiGe transition region going towards the collector, the offset between the constant hole Fermi level and the valence band will increase across the transition region. ΔE_v is therefore the difference of E_v between $V_{cb}^f = 0\ V$ and "pushed-through" V_{cb}^f, shown in Figure 5.4. Since $\Delta E_c = \Delta E_g - \Delta E_v$, the knowledge of the base impurity profile is therefore required to determine ΔE_v before extracting the precise parasitic barrier height using this proposed method. Since a real SiGe HBT's base is usually highly doped and non-uniform, especially near the metallurgical junction, the doping level at zero V_{cb}^f and at "pushed-through" V_{cb}^f, is generally significantly different. Note that if the device doping is uniform across the base, as assumed in [20], ΔE_g will be equal to ΔE_c, which is the parasitic potential barrier height.

To extract the collector-base parasitic potential barrier height, Equation 5.3 is plotted versus increasing magnitude of the reverse collector-base bias, $V_{cb}^f > 0$, when the transistor is operated in the forward active region. Note that V_{cb}^f can only be

increased up to the collector-base junction breakdown voltage. Reverse operation data is extracted for fixed values of the reverse emitter-base bias, V_{eb}^r. Values of bias applied to the forward biased junctions in forward and reverse active operation V_{be}^f and V_{bc}^r, respectively, are simply chosen to be equal and so that the collector currents are low enough to neglect series resistance losses. The total change in the slope of Equation 5.3 versus $1/kT$ over the change in reverse collector-base bias is the overall bandgap variation, ΔE_g, between the silicon collector and SiGe base region at the collector side of the neutral base edge. ΔE_v can be calculated by using the equation that models the difference of doping level,

$$\Delta E_v = kT \ln \frac{N(x_1)}{N(x_2)} \tag{5.5}$$

where N is the p-type base doping concentration, x_1 and x_2 are the positions of the electrical junction when the reverse collector-base bias used is at zero volts and the "pushed-through" voltage, respectively. ΔE_c, the parasitic energy barrier height, can then be calculated from Equation 5.4 since ΔE_g and ΔE_v are known.

The emitter-base parasitic potential barrier height, if present, can be independently measured by varying the reverse emitter-base bias, V_{eb}^r, and keeping the reverse collector-base bias, V_{cb}^f, constant in a similar procedure as above. x_1 and x_2 are now the positions of the electrical junction when the reverse emitter-base bias used is at zero volts and "pushed-through" voltage, respectively.

5.3 Numerical Simulation Results

The method is first evaluated by means of full numerical simulation using the MEDICI [56] semiconductor solver to demonstrate the independent parasitic barrier height measurement capability of the proposed technique. An n-p-n SiGe HBT with a Gaussian base doping profile with peak impurity concentration of $10^{19} cm^{-3}$ and 10% uniform germanium concentration, as shown in Figure 5.2, was simulated. Parasitic barriers were purposely introduced at both the collector-base and emitter-base junctions by allowing boron to exist beyond the silicon-SiGe metallurgical boundaries on both sides of the base region, thereby simulating the electrical impact of boron out-diffusion.

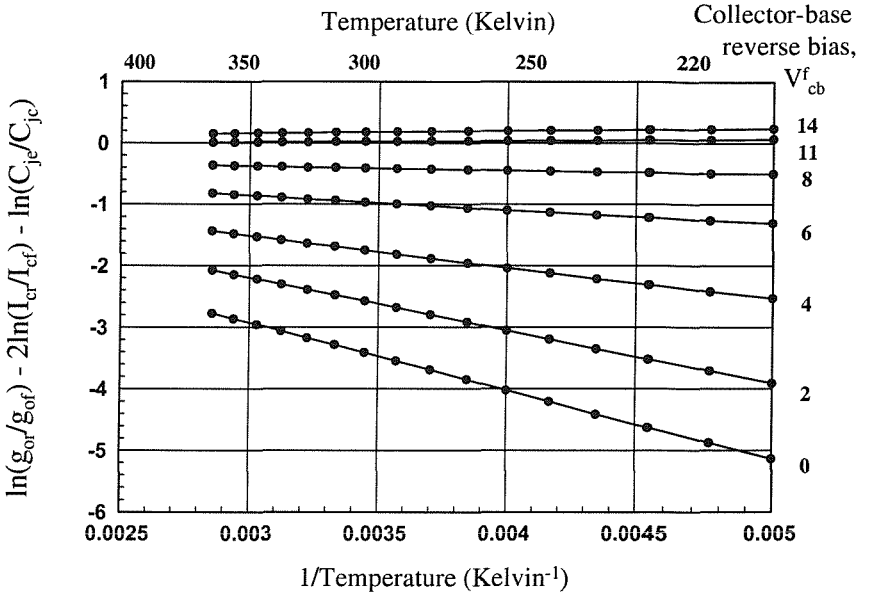

Figure 5.5: Figure showing the change of the slope of Equation 5.3 (i.e. $E_g(V^r_{eb}) - E_g(V^f_{cb})$) with regarding to the increasing V^f_{cb} for the parasitic barrier at the collector-base junction of the simulated device.

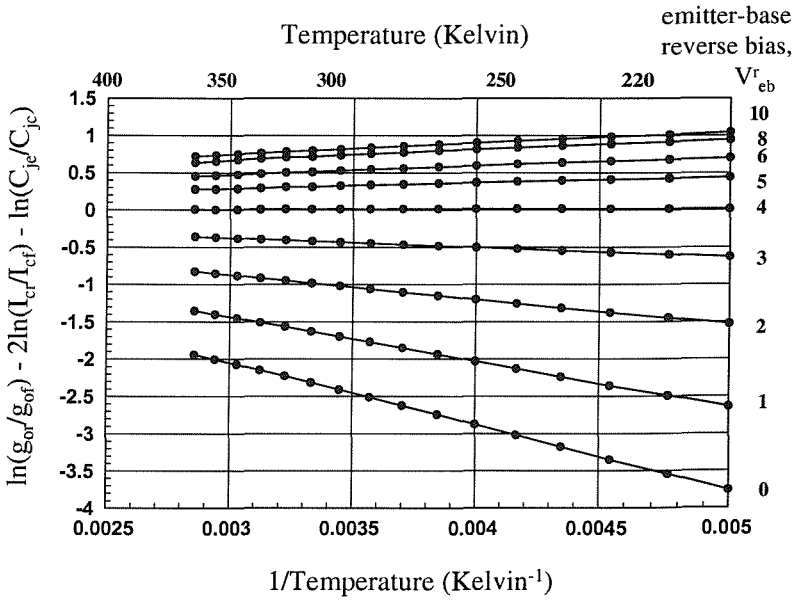

Figure 5.6: Figure showing the change of the slope of Equation 5.3 (i.e. $E_g(V^r_{eb}) - E_g(V^f_{cb})$) with regarding to the increasing V^r_{eb} for the parasitic barrier at the emitter-base junction of the simulated device.

As the reverse collector-base bias, V_{cb}^f, is increased, the bandgap difference between the edges of the neutral base, $E_g(V_{eb}^r) - E_g(V_{cb}^f)$, is reduced by space-charge layer encroachment into the collector side of the neutral base. This changes the slope of Equation 5.3 as shown in Figure 5.5. Eventually, for high enough reverse collector-base bias, V_{cb}^f, the slope no longer changes significantly indicating that the electrical junction has moved into the SiGe area when the parasitic barrier is completely "pushed-through". The final bandgap variation, ΔE_g, of the collector-base junction for zero collector-base bias is the total change in slope of $\ln(g_{or}/g_{of}) - 2\ln(I_{cr}/I_{cf}) - \ln(C_{je}/C_{jc})$ versus $1/kT$ over the reverse collector-base bias, V_{cb}^f, variation. Similarly, the whole process was repeated to extract the emitter-base parasitic barrier height except that V_{cb}^f was fixed at a reference voltage and V_{eb}^r was increased from zero to "push-through" voltage. Equation 5.3 for increasing V_{eb}^r, for the emitter-base parasitic potential barrier extraction is shown in Figure 5.6.

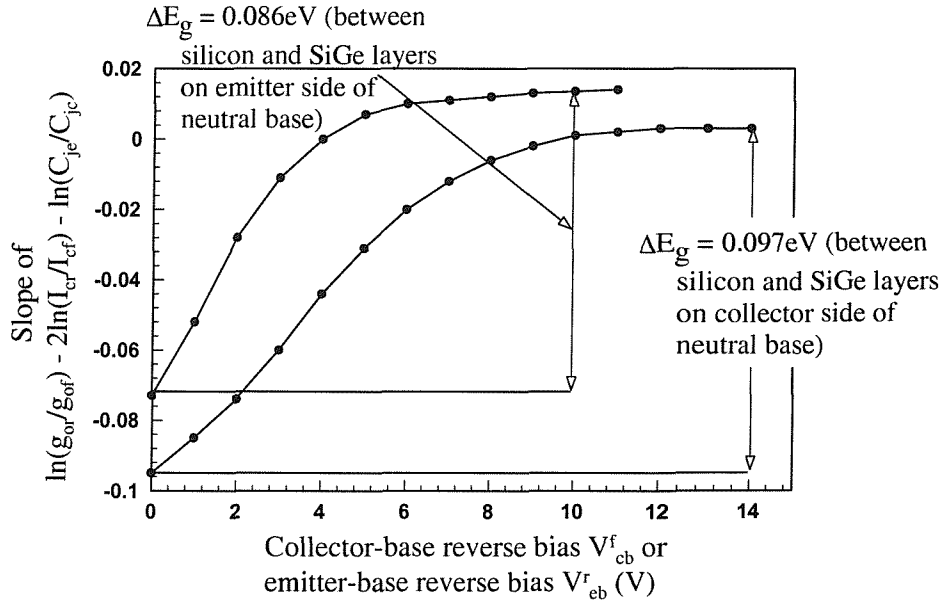

Figure 5.7: Plots of the slope of $\ln(g_{or}/g_{of}) - 2\ln(I_{cr}/I_{cf}) - \ln(C_{je}/C_{jc})$ vs V_{cb}^f (or V_{eb}^r for the emitter-base junction) were used to "measure" the emitter-base and collector-base bandgap variation across the parasitic barrier of the simulated device.

Figure 5.7 shows the simulated extractions of the bandgap variations between the silicon and SiGe regions across the parasitic barriers at the collector and emitter sides of the neutral base region. Applying the proposed measurement technique to the simulated output conductance data of the SiGe HBT, ΔE_g of 0.086 eV and

0.097 eV were "measured" across the emitter and collector parasitic potential barrier regions, respectively. From the internal simulation data, shown in Figure 5.8 and 5.9, ΔE_g was found to be 0.092 eV and 0.093 eV across the emitter and collector parasitic potential barrier, respectively. This shows that the "measured" method and the internal data of Medici is within 10 % of agreement with each other. x_1, x_2, $N(x_1)$ and $N(x_2)$, were extracted directly from internal simulation data and ΔE_v was calculated using Equation 5.5 and found to be 0.064 eV and 0.055 eV for the emitter and collector junctions, respectively, as shown in Figure 5.8 and 5.9. Therefore, according to Equation 5.4, the emitter and collector parasitic barrier heights are 0.022 eV and 0.042 eV, respectively.

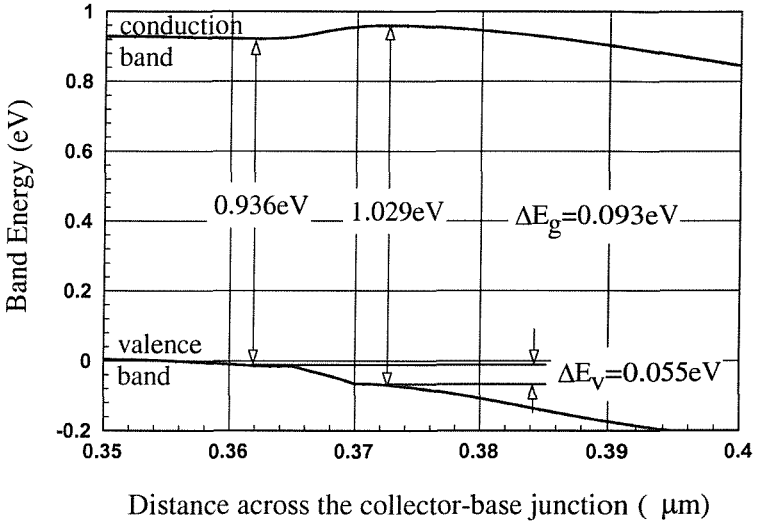

Figure 5.8: Band energy diagram of the collector-base junction for $V_{cb}^f = 0V$ plotted from internal simulation data. ΔE_g and ΔE_v are found to be 0.093 eV and 0.055 eV, respectively.

5.4 Experimental Measurement Results

The experimental method was used on a fabricated n-p-n SiGe HBT [64], from the G7 batch [87], known to have parasitic potential barriers due to boron out-diffusion [88]. It was processed using low pressure chemical vapour deposition (LPCVD) and its doping profile, obtained from secondary-ion mass spectrometry (SIMS), is shown in Figure 5.10. This device had a nominal peak base doping of $2 \times 10^{19} cm^{-3}$, nominally 10% uniform germanium concentrations, and $5nm$ undoped spacer layers to partially

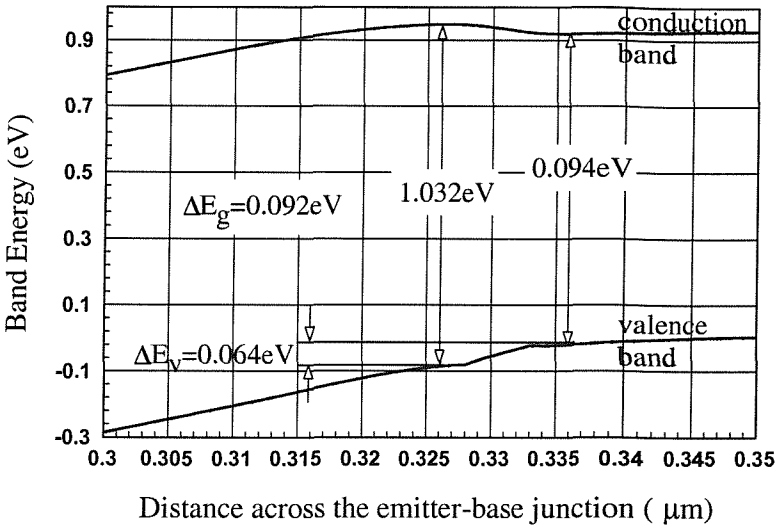

Figure 5.9: Band energy diagram of the emitter-base junction for $V_{eb}^{r} = 0V$ plotted from internal simulation data. ΔE_g and ΔE_v are found to be 0.092 eV and 0.064 eV, respectively.

suppress the effects of boron out-diffusion. Base layer widths, not including spacer layers, were nominally $25nm$ and were grown at 610^oC. The emitters were grown at 700^oC and polysilicon emitter contacts were used.

It was not possible to extract the barrier height at the emitter-base junction since this junction reached break-down at relatively low reverse emitter-base bias. However, it is unlikely that a significant emitter parasitic barrier existed since the emitter doping was significantly higher than the collector doping (10^{18} versus 10^{16} cm^{-3}), which of course also results in a lowered reverse emitter-base junction breakdown voltage. Conveniently, for lower emitter doping where parasitic barrier formation is more likely, the proposed technique could possibly be used since the emitter-base breakdown voltage will be higher. Whether or not a parasitic barrier existed at the emitter-base junction has no impact on the extraction of the collector-base parasitic barrier height, since, as demonstrated in Section 5.3, the proposed method can extract both barrier heights independently. Figure 5.11 shows the forward active mode, collector current versus the reverse biased collector-base voltage characteristic of the measured device for various base bias. It shows that the base-collector junction can be reverse biased up to 19 volts without breaking down. This enables the parasitic barrier extraction method to be applied to the base-collector junction.

Figure 5.12 shows plots of Equation 5.3 for the measured device for increasing

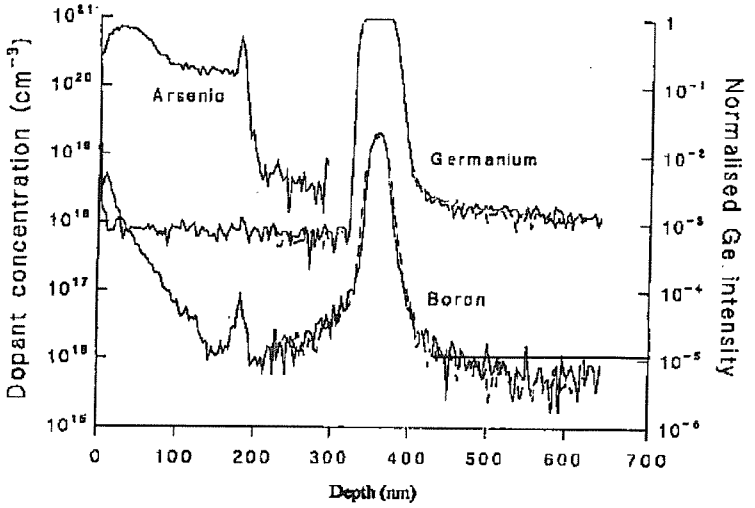

Figure 5.10: Doping profile from SIMS of the fabricated n-p-n SiGe HBT device measured for experimental verification of the new proposed method.

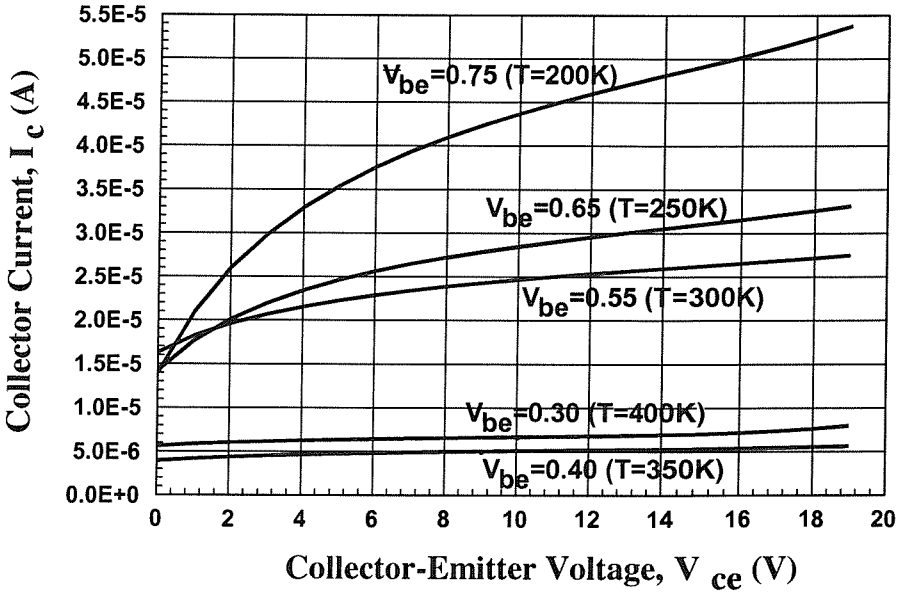

Figure 5.11: The collector current, I_c, versus the reverse biased collector-base voltage, V_{cb}^f, showing that the forward active mode base-collector junction can be reverse biased up to 19 V without breaking down.

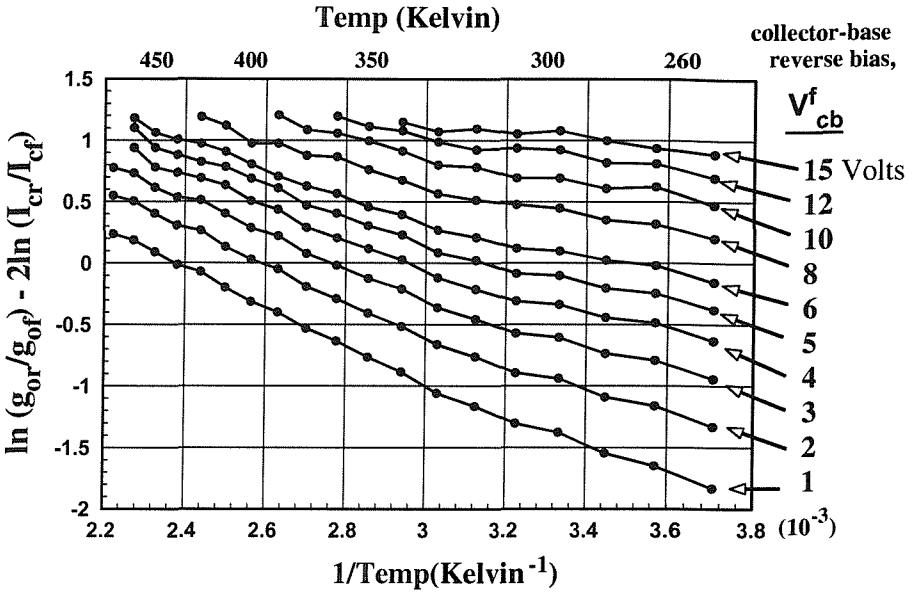

Figure 5.12: The slope of $\ln(g_{or}/g_{of}) - 2\ln(I_{cr}/I_{cf})$ indicates that a rather large bandgap variation, ΔE_g, is present in the measured device as the slope changes considerably with collector-base reverse bias V^f_{cb}.

values of reverse collector-base bias, V^f_{cb}. The effect of the ratio of the depletion capacitance can often be insignificant [15] and has been neglected in these measurements. Figure 5.13 shows the variation in the slopes of the plots in Figure 5.12 versus the reverse collector-base bias, V^f_{cb}. The bandgap difference across the neutral base begins to change rather rapidly as V^f_{cb} increases and this is caused by space-charge layer encroachment into the collector side of the neutral base, which will reduce the parasitic barrier. The bandgap will continue to change rapidly until the parasitic barrier is removed completely by the space-charge layer encroachment, which is at $V^f_{cb} = 17\ V$ in Figure 5.13. From Figure 5.13, the collector-base junction bandgap variation across the parasitic barrier, ΔE_g, can be obtained by extracting the bandgap changes between $V^f_{cb} = 0\ V$ and $V^f_{cb} = 17\ V$, and is found to be $0.110\ eV$. This value of ΔE_g represents a direct measurement of the bandgap difference between the silicon collector layer and the SiGe base region of the SiGe HBT. This value of bandgap reduction is obtained without the need for a silicon control and without the need for knowledge of any transport parameter values or device structural data.

A full numerical simulation using Medici was also performed by modelling the SIMS profile of the measured n-p-n SiGe HBT device, shown in Figure 5.10. The

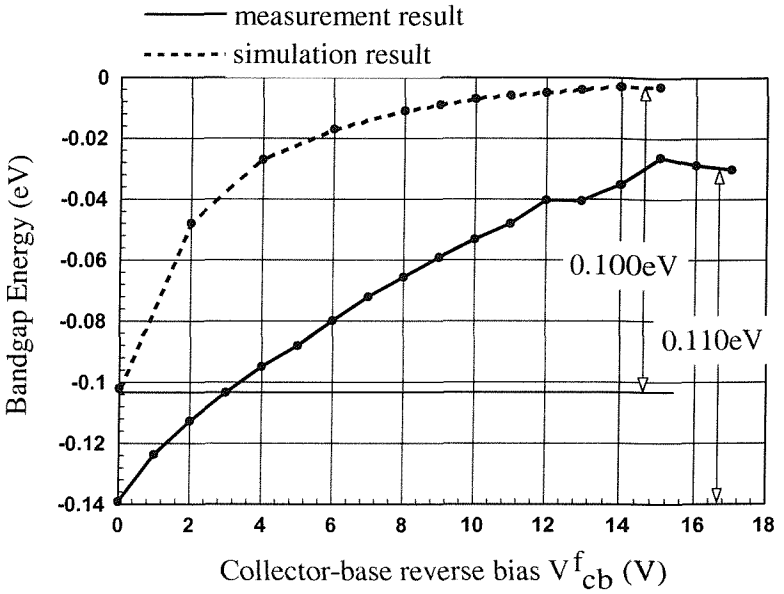

Figure 5.13: The plot illustrates the changes of bandgap with increasing collector-base reverse bias V_{cb}^{f}. ΔE_g of 0.110 eV and 0.100 eV were extracted from the measurement results and simulation results, respectively.

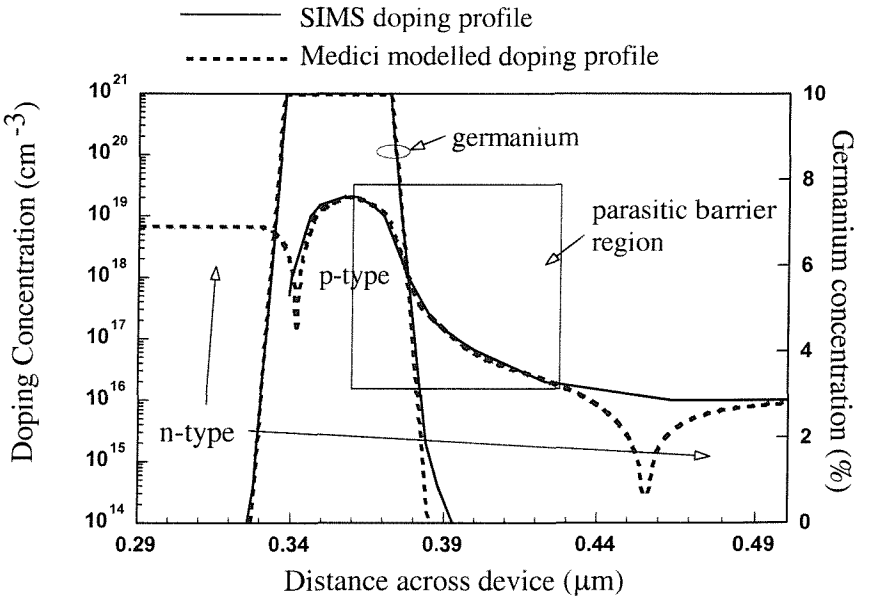

Figure 5.14: The modelling of the measured n-p-n SiGe HBT device doping profile using semiconductor device simulator Medici. Note that the highlighted part of the boron profile, where the collector-base parasitic barrier exists, is modelled very closely in order to reproduce the measurement results in the simulation.

simulation procedure is similar to those described in Section 5.3. As shown in Figure 5.14, the boron and germanium doping profile used in Medici was modelled very closely to the SIMS profile. The germanium concentration is nominally 10%, and the emitter and collector doping are informed by the process report [87] as nominally $7 \times 10^{18} cm^{-3}$ and $10^{16} cm^{-3}$. The simulation result is shown in Figure 5.13 and ΔE_g of $0.100eV$ was extracted using the extraction method. The difference in absolute value of the bandgap between the measurement result and simulation result in Figure 5.13 could be due to inaccuracies in the SIM's data and doping information of the measured device. However, it is the changes of bandgap with increasing V_{cb}^f that yield the bandgap difference across the parasitic barrier. In this case, the simulation result is within 10% of agreement with the measured result. Therefore this increases the confidence that the proposed measurement method is indeed measuring the bandgap difference across the parasitic barrier of the n-p-n SiGe HBT device and this measurement method is not significantly affected by other effects that are not taken into account in the simulations, such as 3-D effect, collector-base avalanche breakdown, etc..

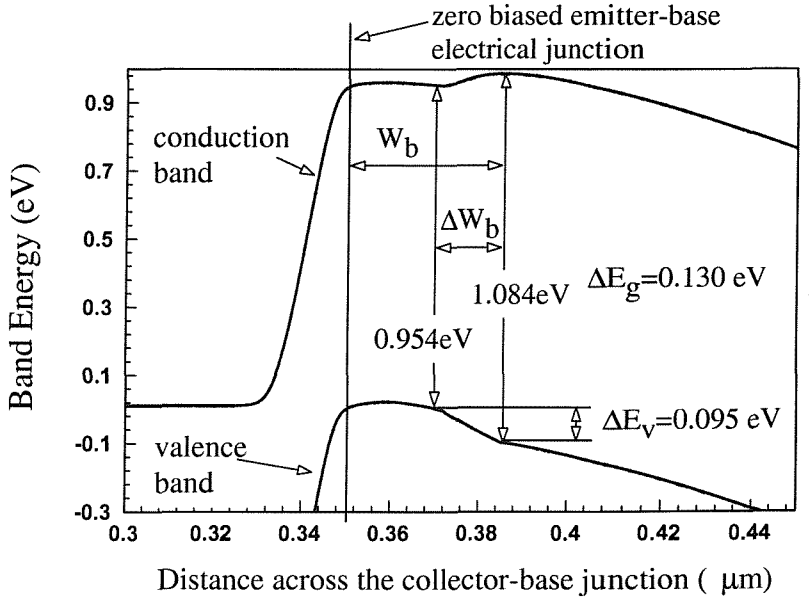

Figure 5.15: Simulated band energy diagram of the collector-base junction for $V_{cb}^f = 0V$ plotted from internal simulation data of experimentally measured device. Modelled ΔE_g and ΔE_v are 0.130 eV and 0.095 eV, respectively.

ΔE_v was found to be $0.095eV$ for the measured device, shown in Figure 5.15.

This was estimated using Equation 5.5 where $N(x_1)$ and $N(x_2)$ were determined from solving Poisson's equation using Medici device simulator on the device SIM's data in Figure 5.10. Therefore the parasitic barrier height, ΔE_c, is found to be $0.110-0.095 = 0.015eV$ for this device. Note that in Figure 5.15, the bandgap difference across the parasitic barrier from solving Poisson's equation, ΔE_g was found to be $0.130eV$ as compared to $0.110eV$ from the measurement. This again could be due to inaccuracy in the SIM's data. Also, from the bandgap energy diagram in Figure 5.15, the electrical junction positions at zero and "pushed-through" V_{cb}^f were estimated from the shape of the parasitic barrier and could not be determined absolutely. Perhaps, the weakness in this proposed parasitic potential barrier extraction method is to rely on solving Poisson's equation to determine ΔE_v. However, it must be said that the currently existing methods to estimate the parasitic potential barrier height by Slotboom [20] and Le Tron [21] assumed a uniformly doped and abrupt germanium profile where ΔE_v did not exist, in which, from Equation 5.4, $\Delta E_g = \Delta E_c$. Since practical SiGe HBT does not have uniform base, ΔE_v was shown above to be significant to the calculation of the parasitic potential barrier height and have to be accounted for in the parasitic potential barrier height extraction method.

It is interesting to approximate the effect of $\Delta E_c = 0.015eV$ on the collector current of the measured device. Refering to Slotboom's collector current model [20] for uniformly doped SiGe HBT with significant parasitic potential barrier, discussed in Section 2.5.1:

$$J_{c,SiGe}^{par} = \frac{qD_n n_{ib}^2(SiGe)}{N_b W_b} \times \frac{\exp(qV_{be}/kT)}{1 - \Delta W_b/W_b + (\Delta W_b/W_b)\exp(\Delta E_c/kT)} \tag{5.6}$$

where $J_{c,SiGe}^{par}$ is the collector current of a SiGe HBT with parasitic barrier, ΔW_b is the parasitic potential barrier width, and the other parameters have their usual meaning. For a SiGe HBT without parasitic potential barrier, ΔW_b and ΔE_c become zero and the collector current becomes:

$$J_{c,SiGe} = \frac{qD_n n_{ib}^2(SiGe)}{N_b W_b} \exp(qV_{be}/kT) \tag{5.7}$$

Therefore, the ratio $(J_{c,SiGe}/J_{c,SiGe}^{par})$ becomes:

$$\frac{J_{c,SiGe}}{J_{c,SiGe}^{par}} = 1 - \Delta W_b/W_b + (\Delta W_b/W_b)\exp(\Delta E_c/kT) \tag{5.8}$$

From Figure 5.15, W_b is 0.036 μm and ΔW_b is 0.016 μm, therefore $J_{c,SiGe}/J_{c,SiGe}^{par}$ is equal to 1.35.

The measured device (with 5 nm SiGe undoped spacer) has extrapolated zero base-emitter bias collector current, I_{co}, of $2.28 \times 10^{-15} A$. From the G7 batch of SiGe HBTs [87], another SiGe HBT was fabricated with 15 nm undoped SiGe spacer. It went through similar processes as the measured SiGe HBT and was known to have no parasitic potential barrier [88]. It has I_{co} of $5.91 \times 10^{-15} A$. Therefore, $(J_{c,SiGe}(15nm)/J_{c,SiGe}(5nm))$ becomes 2.59.

From the Slotboom's model estimated result and the measurement result, it is reasonable to say that the measured value of barrier height of 0.015 eV at the collector-base junction is a reasonable value to be expected.

5.5 Conclusions

An alternative electrical method to measure junction parasitic barrier heights has been presented. By means of simulation and experimental measurement, it was demonstrated that the method enables a direct electrical measurement of the bandgap variation across the barrier. Simulation results also show how the method can be used in principal to measure the height of the collector-base and emitter-base junction parasitic barriers on the same device independently. Even if an emitter-base parasitic barrier cannot be measured due to a lack of a sufficiently high emitter-base breakdown voltage, the method is capable of extracting the parasitic barrier information at the collector-base junction independent of the influence of a possible emitter-base barrier.

The proposed method provides a more direct measure of the parasitic barrier heights at the edges of the neutral base region in SiGe HBT's than previous methods. The method is more direct as it does not depend upon a detailed knowledge of the temperature dependence of SiGe density of states functions or carrier mobility. It depends instead upon a direct measure of the bandgap difference across the Si-SiGe transition region and upon the positional variation of base impurity concentration in the vicinity of the potential barrier. It also does not require the use of a control device

that must be identically structured while at the same time not possessing parasitic barriers.

The technique should also prove useful as a means of directly measuring the electrical bandgap reduction in actual processed SiGe base layers.

Chapter 6

Theoretical Comparison of a Proposed Novel SiGe HBT with Existing Advanced Vertical SiGe HBT Technology

In this chapter, the potential of lateral SiGe HBT transistor structure as high performance device is assessed by means of numerical simulation. In this study, a state of the art ultra low power and high speed vertical SiGe HBT transistor published by Kondo *et al.* [10], and a proposed novel lateral SiGe HBT structure [89] were simulated using Silvaco Atlas 2-D semiconductor solver. Performance of the novel lateral SiGe HBT transistor is assessed by comparison to the performance of the Kondo *et al.* device.

So far as a lateral bipolar transistor is concerned, there does not appear to have been a published working lateral SiGe heterojunction bipolar transistor where the emitter, base and collector form a true lateral double heterojunction structure. The pseudo-heterojunction hybrid mode lateral transistor [33, 90, 91] described in Section 3.3 appears to be the closest to the heterojunction effect ever published for a lateral bipolar transistor. The advantages of SiGe heterojunction bipolar transistors over silicon bipolar junction transistors were already discussed in Chapter 2. By includ-

ing germanium in the base, thereby forming a SiGe base to enable base bandgap engineering, SiGe HBTs have (1) improved emitter injection efficiency; (2) reduced base transit time; (3) reduced output conductance; (4) reduced base resistance and (5) improved low temperature performance [8] over silicon bipolar transistors. A lateral SiGe HBT would combine the advantages of low parasitic and low power of a lateral bipolar transistor with superior speed and analogue performance of a SiGe HBT. Therefore, a SiGe heterojunction lateral bipolar transistor is potentially a high performance technology and well worth investigating. Here, the possibility of making lateral SiGe heterojunction bipolar transistor is examined. A main difficulty here will be in realising a strained SiGe base. Also, the difficulties faced in defining and contacting the lateral bipolar transistor base, as discussed in Section 3.1 for silicon only RF lateral bipolar transistors, applies here as well.

In general there are two known methods of making a strained SiGe layer. The first method is to implant germanium ions directly into the silicon wafer, such as in doping implantation [92]. Germanium implantation produces an amorphous layer and would therefore need to be recrystallined through annealing. However, germanium implantation often creates less satisfying SiGe quality [92, 93] and may not always be practical. Besides, implantation also results in dopant diffusivity enhancement and can cause excessive boron out-diffusion. Parasitic energy band barriers can easily be formed under such conditions and would impair the transistor performance. A second more widely used method is to grow the SiGe layer on the silicon wafer. Two mature growth methods employed in a SiGe HBT device and circuit fabrication are the ultra-high vacuum chemical vapour deposition (UHV/CVD) [8, 48] and molecular beam epitaxy (MBE) [94, 95]. These methods yield strained SiGe layers of high quality.

As in a lateral bipolar transistor, a thin base is still essential for a high performance lateral SiGe HBT for the same reasons. If lithography or oxide/nitride spacer is used for base definition, as explained in section 3.1, germanium implantation would most likely be the most suitable method for SiGe base formation. However, since germanium implantation may not yield good quality strained SiGe layer, only methods that involve CVD, SiGe layer growth processes, and in particular LPCVD are being considered here.

A novel lateral double Si/SiGe heterojunction bipolar transistor structure is proposed in this section [89]. To evaluate its performance, the structure is numerically modelled using Silvaco Atlas semiconductor solver [34] and then compared with an existing advanced ultra-low-power and high speed vertical SiGe heterojunction bipolar transistor that is suitable for RF applications [10]. To compare the performances of the vertical device with the proposed lateral SiGe HBT, both devices were modelled using the Silvaco Atlas semiconductor solver. The same models and parameters used for the vertical HBT simulations in Atlas were then used to model the lateral HBT. This enabled a direct and realistic comparison between both structures.

It will be argued that in principle, a SiGe CVD process can realise a lateral active region identical to that obtained in vertical SiGe HBT's. For this reason, the active region dimensions and doping profiles are made identical in the vertical and lateral simulated devices. In this way the impact of the lateral structure with regards to lower current and lower parasitics on RF performance are determined relative to a reported state-of-the-art vertical device.

In the following sections, the proposed lateral HBT structure with its processing steps is presented in section 6.1. The vertical SiGe HBT [10] used for comparison with the proposed lateral HBT is discussed in section 6.2. Here, the vertical HBT is numerically modelled using the Atlas semiconductor solver in order to reproduce the reported performance in [10]. Finally, the performances of both lateral and vertical HBT are compared in section 6.3 in order to evaluate the performance of the lateral SiGe HBT.

6.1 Proposed Lateral SiGe HBT

The objective of proposing this novel lateral bipolar transistor structure is to enable the development of a transistor that combines the advantages of the lateral transistor with the enhancement brought about by the incorporation of SiGe in the base. To achieve these objectives, the novel transistor is fabricated on Silicon-on-Insulator Substrate (SOI) to reduce parasitic capacitances. It needs to have self-aligned base definition to reduce junction capacitances and to reduce base resistance through direct

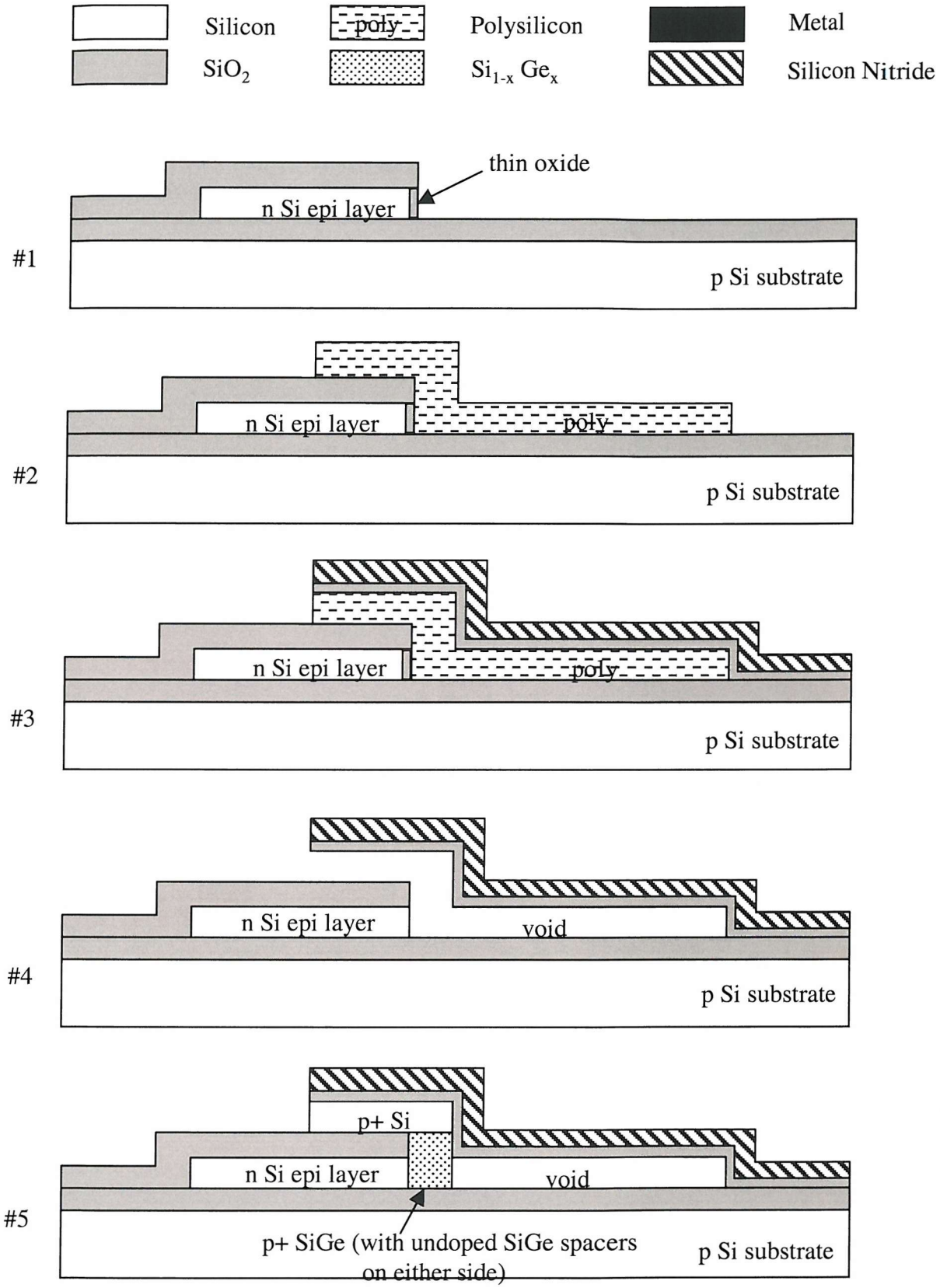

Figure 6.1: First page of figures illustrating the process flow of the proposed Lateral SiGe HBT

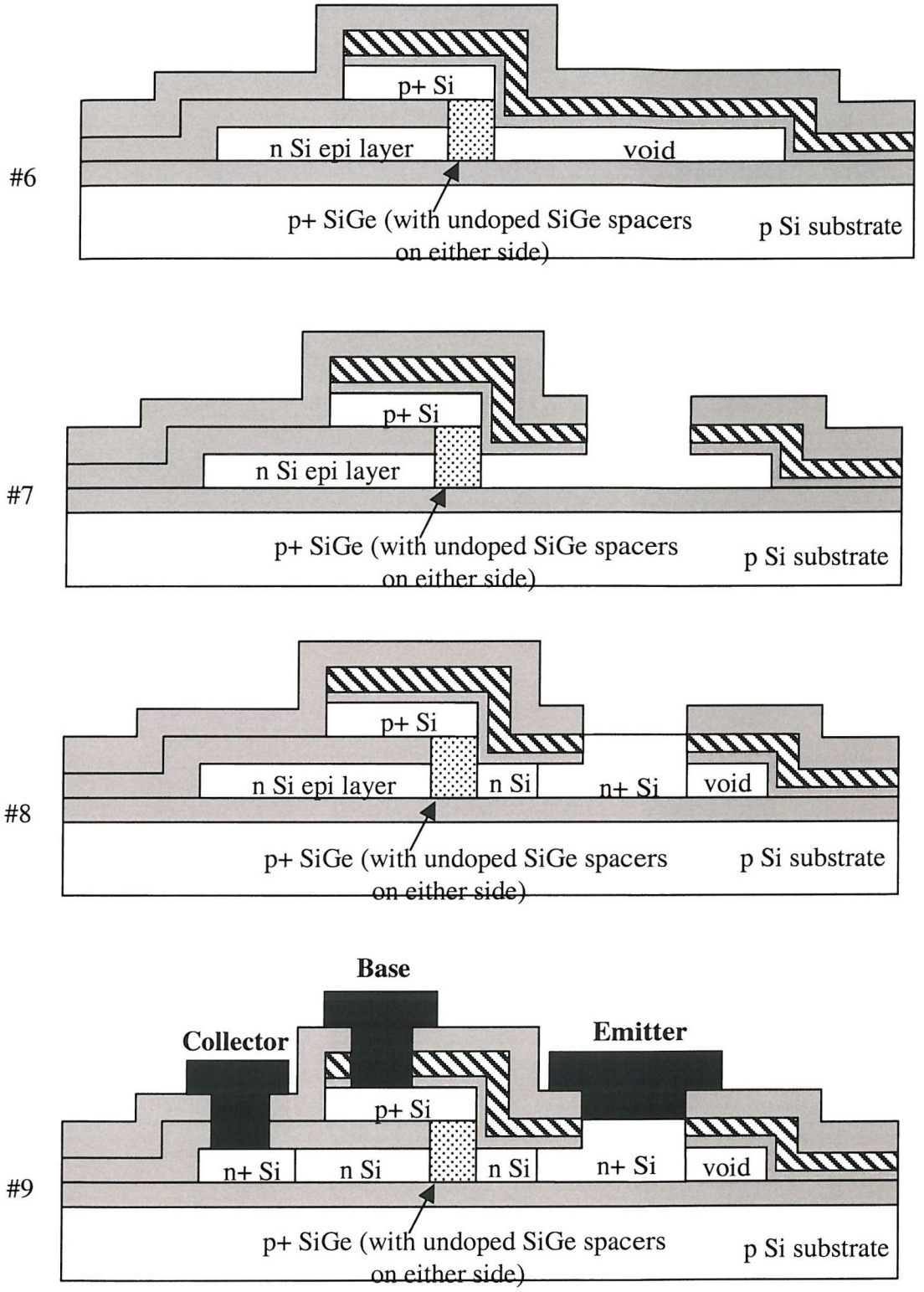

Figure 6.2: Second page of figures illustrating the process flow of the proposed Lateral SiGe HBT

base contact from the top. Low power is achieved by small emitter-base junction area, which is inherent in a lateral structure. And finally, it has to allow lateral epitaxy SiGe growth in order to obtain a high quality strained SiGe base layer.

The proposed structure satisfies all the above requirements. It involves a novel epitaxy processing step called confined lateral selective epitaxy growth, introduced by Schubert *et. al.* [96] to realise the base layer. The technique of Schubert *et. al.* [96] makes use of a micro structure where the silicon growth consists of filling a cavity inside the micro structure towards only one direction with selective silicon epitaxy. This technique was created as a new method of producing SOI. It was reported to have produced single-crystal silicon over insulator of 0.9 μm thick, 8.0 μm wide and 500 μm long.

Processing steps of the proposed lateral SiGe HBT (LHBT) are shown in Figure 6.1 and 6.2. To fabricate the proposed lateral SiGe HBT, a layer of SOI is used as the starting material. This layer, which will become the collector side of the transistor, is thinned to 0.1 μm (one can also obtain commercial thin SOI substrates) and etched to required width. A layer of oxide is then deposited on top. Part of the silicon and oxide layers are etched away vertically in order that the oxide and silicon side wall is exposed, as shown in step #1 in Figure 6.1. The exposed silicon sidewall is the seed hole where SiGe layer will be grown. A very thin layer of oxide is regrown to heal the etching damage at the seed hole and to protect it against a selective polysilicon wet etch later in the process, #1. This thin layer of oxide can in fact be a protective 'RCA' oxide layer, which is nominally 1.5 nm thick, that is introduced onto any silicon surface at the end of an RCA clean [97]. The collector is doped by implantation and annealing.

Next, a layer of sacrificial amorphous silicon is deposited over the oxide and silicon step and patterned, #2. The thickness and shape of this sacrificial layer will determine the growth cavity dimension. To provide a thermal oxide lining for the cavity, the sacrificial layer is partially oxidised. This may also convert the amorphous silicon to polycrystalline silicon, but it should still retain the surface smoothness helpful in reducing defects. Then the entire structure will be covered with silicon nitride for mechanical support of the top layer of the cavity. Part of the nitride and oxide top

layers are etched away to expose the top end of the polysilicon layer, #3.

The polysilicon layer is then removed selectively by selective wet etch (e.g. KOH) to leave a cavity with the seed hole within, as shown in #4. The thin RCA oxide layer thickness is then reduced in dilute HF (150:1 $H_20 : HF$) before being desorbed completely in the SiGe growth chamber, in a hydrogen atmosphere at 750 mTorr and 860 Celsius [97]. This is to prepare for the selective SiGe growth inside the cavity. Epitaxy gases can now enter the cavity through the opening window on top and grow from the exposed silicon at the seed hole. The epitaxy gas composition, temperature and reactor pressure are adjusted for selective growth so that the SiGe deposition occur only from the silicon and not the oxide cavity walls [97]. As SiGe layer begins to grow from the seed hole, it will block off the corner of the cavity eventually and allow the epitaxy to grow only upwards towards the opening, as shown in step #5. By adjusting the epitaxy gas compositions, the epitaxy layer composition and doping profile can be adjusted according to requirement. Note that at this stage, the emitter side is yet to be formed and this region remains void during the first LPCVD epitaxy step.

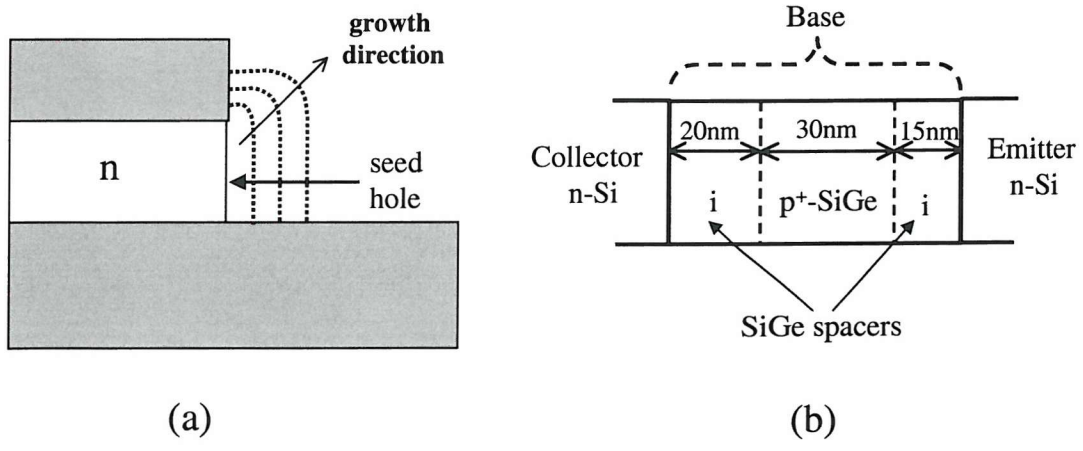

Figure 6.3: (a) Illustrates how the SiGe base layer is expected to grow from the seed hole. (b) An example of the kind of high performance base structure (with its undoped SiGe spacers i) that could be potentially possible with this LPCVD growth technique, in order to suppress boron out diffusion.

Figure 6.3(a) illustrates how the SiGe layer is expected to grow from the seed hole. SiGe layer is expected to grow vertically as well as horizontally since SiGe molecules will bond themselves to any exposed silicon or SiGe surface during the

LPCVD growth. By controlling the epitaxy gas compositions, undoped SiGe spacers can be incorporated at both sides of the p^+ doped SiGe. An example of such a base structure is shown in Figure 6.3(b) where 20 nm and 15 nm of undoped SiGe spacers are incorporated with precise thickness at the collector and emitter sides of the 30 nm thick p^+-SiGe layer respectively [10]. Such base structure is necessary for high speed and high gain devices where the undoped SiGe-spacers are used to take up the effects of boron-out-diffusion that result in parasitic energy barriers [20]. Without such base structure, it will be impossible for the lateral SiGe HBT's to achieve performance that is comparable to state-of-the-art vertical SiGe HBT's. Note that it is difficult, if not impossible, to obtain such a high performance base structure if ion implantation is used to form the SiGe layer.

A blanket oxide is then deposited on the structure for isolation, as shown in step #6. A via hole is etched through the oxide/nitride/oxide layers of the growth cavity to allow epitaxy gases reaching the emitter side for emitter growth, as shown in step #7. The silicon emitter is grown epitaxially with in situ doping through the via hole, as shown in step #8. Finally, via windows are opened for the collector, base and emitter metal contacts directly from the top, as shown in step #9.

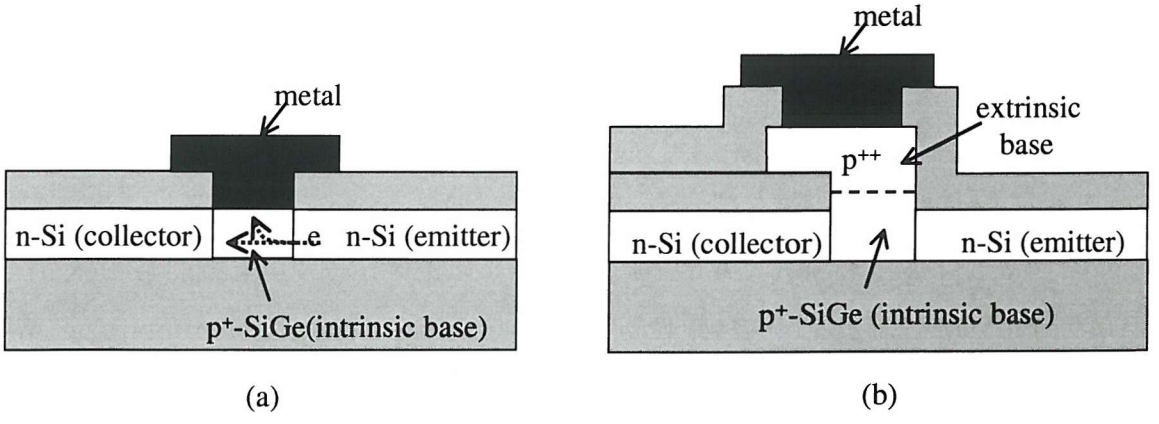

Figure 6.4: (a) Base contact structure with base metal contact close to the intrinsic base (active base) region. (b) Base contact structure of the proposed lateral SiGe HBT, with an extrinsic base region to reduce base current.

The proposed lateral SiGe HBT has self-aligned base definition. The choice of base contact structure for the lateral SiGe HBT will affect the device base current. Figure 6.4(a) shows a base contact structure that has the base metal contact directly

on top of the intrinsic base area. This can be done by etching away the top of the SiGe base layer before laying the metal contact. This structure could give a very low base resistance. However, by having the base metal contact too close to the intrinsic base region, this structure would also be expected to have very high base current due to electrons from the emitter going directly into the base contact, as depicted in Figure 6.4(a).

To avoid this happening in the proposed lateral SiGe HBT, a retarding electric field to minority carrier electrons in the base can be introduced between the base contact and the intrinsic base region (active base region). Otherwise, there must be a significant silicon (or SiGe) extrinsic region with enough ohmic resistance between base metal contact and intrinsic base. Figure 6.4(b) shows the base structure used in the proposed lateral SiGe HBT to solve this problem. There are two different ways to realise a retarding electric field between the base metal contact and the intrinsic base region. The first way is to use a higher p^{++} doping in the 'top' extrinsic base contact layer, shown in Figure 6.4(b), than is in the intrinsic base region. This difference of dopant will create a retarding electric field to the minority carrier electrons. If the same dopant concentration are used for the intrinsic and extrinsic base region (e.g. for the situition where the base already has the maximum p-type doping for very low base resistance), the use of a silicon 'top' extrinsic layer over a SiGe intrinsic base layer will produce a potential barrier as it does in parasitic barrier formation. This potential barrier will restrict the minority carrier electrons from reaching the base contact. This type of contact will be referred to as an "isotype heterojunction" base contact, which will keep the base current low resulting in sufficiently high current gain combined with low base contact resistance.

6.2 Vertical SiGe HBT used for Comparison to the Proposed Lateral SiGe HBT Structure

For the purpose of comparison, a state of the art high performance vertical SiGe HBT device developed by Kondo *et. al.* [10] is chosen to be compared with the

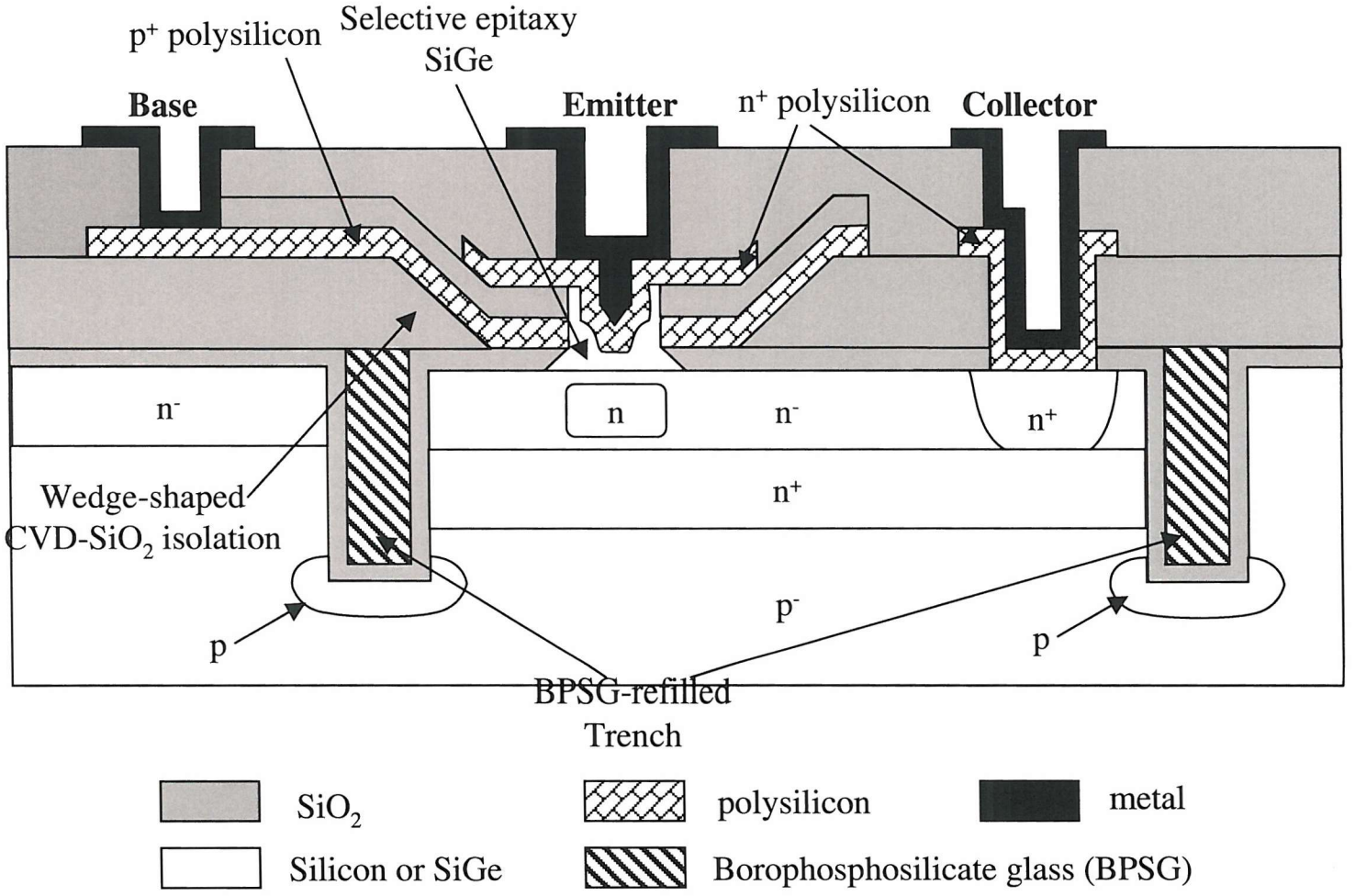

Figure 6.5: The Kondo's device structure.

proposed lateral SiGe HBT. It is an ultra low power and high speed SiGe base bipolar transistor that has been developed for low power high frequency rf/microwave wireless telecommunication applications.

The Kondo device structure is illustrated in Figure 6.5. It has the same structure as a conventional double-polysilicon bipolar transistor. However, to enhance the high speed capability of the device, a couple of new features were specifically introduced in the structure, as indicated in Figure 6.5. Borophosphosilicate glass (BPSG)-refilled trench is used for isolation. The trench is about 0.8 μm wide. The ϵ of the BPSG is about one-third that of silicon and in this case, it minimises the substrate capacitance because its sidewall component has been reduced to only 0.03 $fF/\mu m$ [10]. A wedge-shaped CVD SiO_2 isolation structure was also developed to reduce the base-collector capacitance component below the p^+ polysilicon base electrode. The SiGe base and polysilicon/SiGe base contact, respectively, were simultaneously formed in a UHV/CVD process in a self-aligned manner on the n^- collector and on the sidewall of the p^+ polysilicon base electrode inside the window, as shown in Figure 6.6. Therefore, the width of the base-collector junction is only 0.5 μm, which is the width of the window.

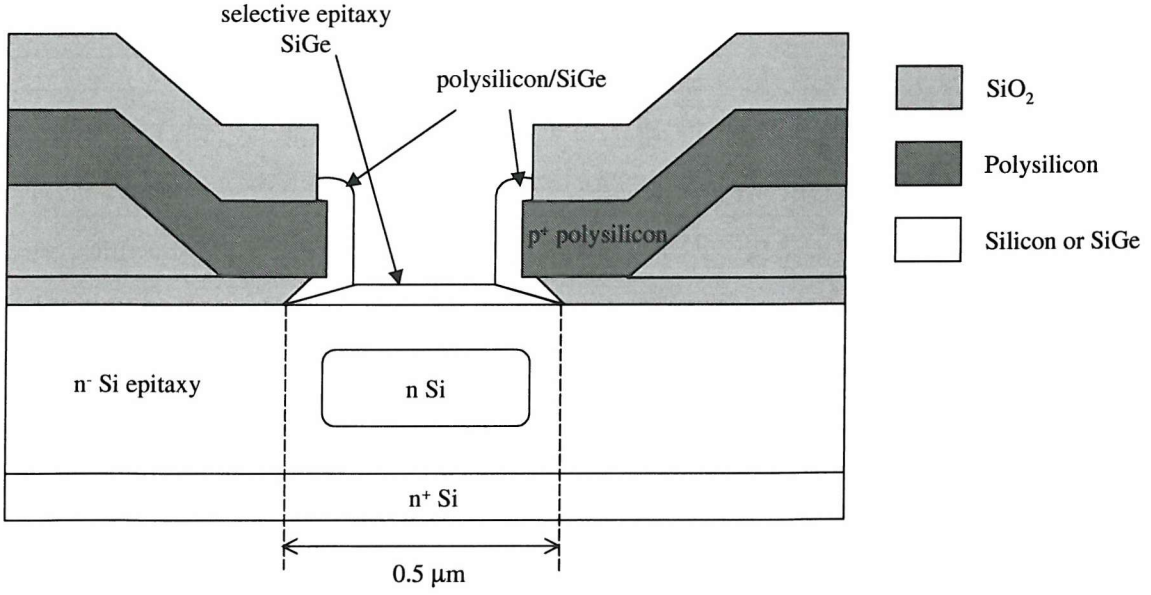

Figure 6.6: The simultaneous formation of SiGe base on the n^- collector with the self-aligned polysilicon/SiGe base contact on the p^+ polysilicon sidewall.

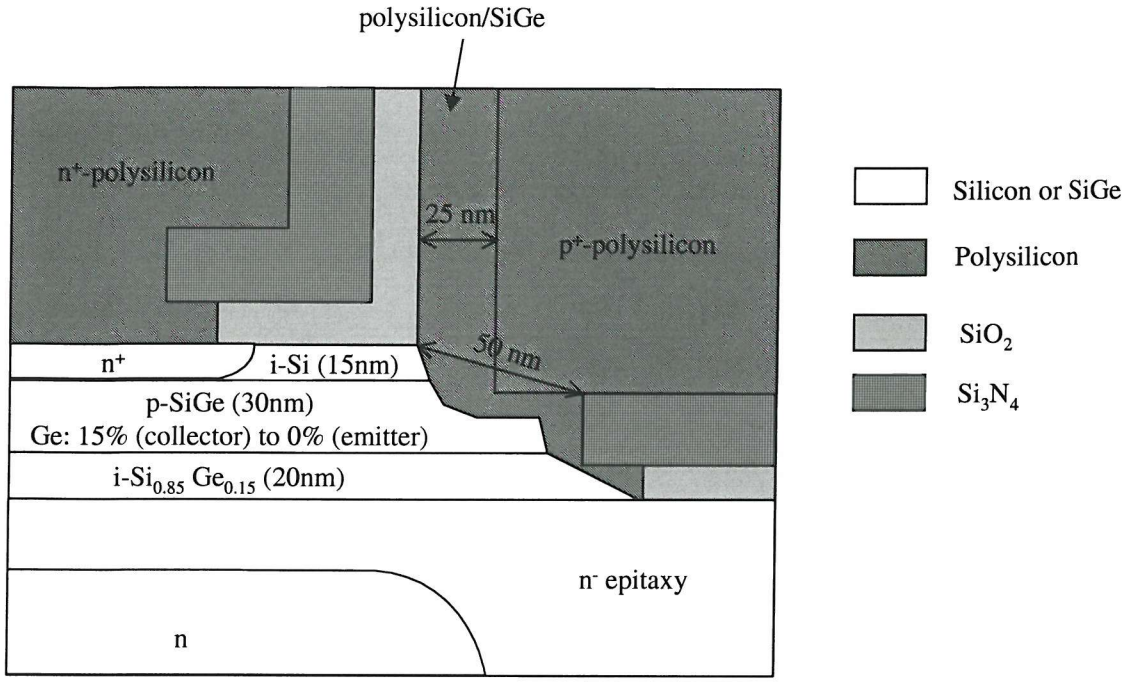

Figure 6.7: Figure illustrating cross section of the base structure of Kondo's transistor [10].

Figure 6.7 illustrates the base structure of the device. The as-grown intrinsic base consists of a 20 *nm* thick nondoped SiGe layer, a 30 *nm* thick p-type graded SiGe layer, and a 15 *nm* thick nondoped silicon layer. SIMS plot of the device is shown in Figure 6.8. The SiGe base is thermally stable for the emitter annealing at 900 Celsius, which is the highest temperature after SiGe growth.

The Kondo structure was modelled using Silvaco Atlas 2-D Semiconductor Solver. Atlas solves Poisson's equation and the continuity equations for electrons and holes in two-dimensions. Poisson's equation relates variations in electrostatic potential to local charge densities. The continuity equations describe the way that the electron and hole densities evolve as a result of transport processes, generation processes, and recombination processes. Physical models used were as follows:

Mobility is function of local electric field, lattice temperature, doping concentration and so on. The Caughey-Thomas mobility model was used to model the field-dependent mobility of electrons and holes in high-field effect [98]. It provides a smooth transition between low-field and high field behaviour. The low-field mobility was also modelled for doping concentration and temperature dependency [98, 99].

Bandgap narrowing effects due to heavy doping were included as spatial variations

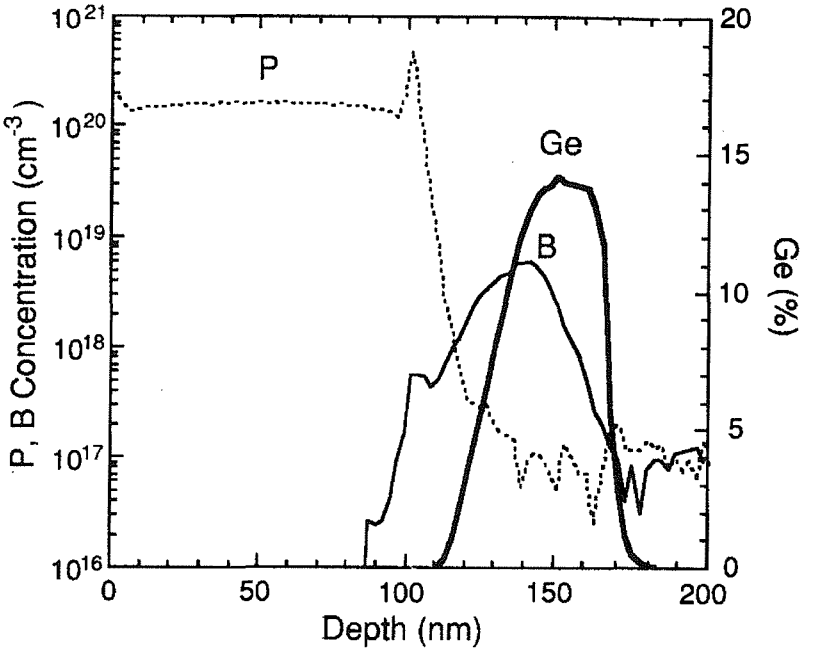

Figure 6.8: Figure illustrating the SIMS profile of the Kondo device [10].

in the intrinsic concentration [58]. Electron and hole recombination mechanisms were modelled by Shockley-Read-Hall recombination using concentration dependent lifetime and Auger recombination, which models the effect of doping concentration on recombination in highly doped silicon [100].

Figure 6.9 shows the doping profile used in Atlas. Peak emitter doping is n-type $1 \times 10^{20} cm^{-3}$, peak base doping is p-type $5 \times 10^{18} cm^{-3}$ and peak collector doping is n-type $5 \times 10^{16} cm^{-3}$. It closely fits the SIMS profile from the Kondo device [10]. The device length in Atlas was 1.7 μm and its dimensions as per [10], as shown in Figure 6.10. The germanium percentage is as shown in Figure 6.7. The Kondo device input file is shown in Appendix D.

The Gummel plot generated from Atlas is shown in Figure 6.11. The published Gummel plot of the Kondo device is also inserted as comparison. Since very similar doping profile and germanium composition are used, the collector current of both published and simulated devices match reasonably well, considering the inaccuracy that usually exists in a SIMS plot. However, the base current of the simulated device is much higher than the published result. The high base current in Atlas could be due to much lower emitter hole lifetime parameters in the polysilicon emitter area which

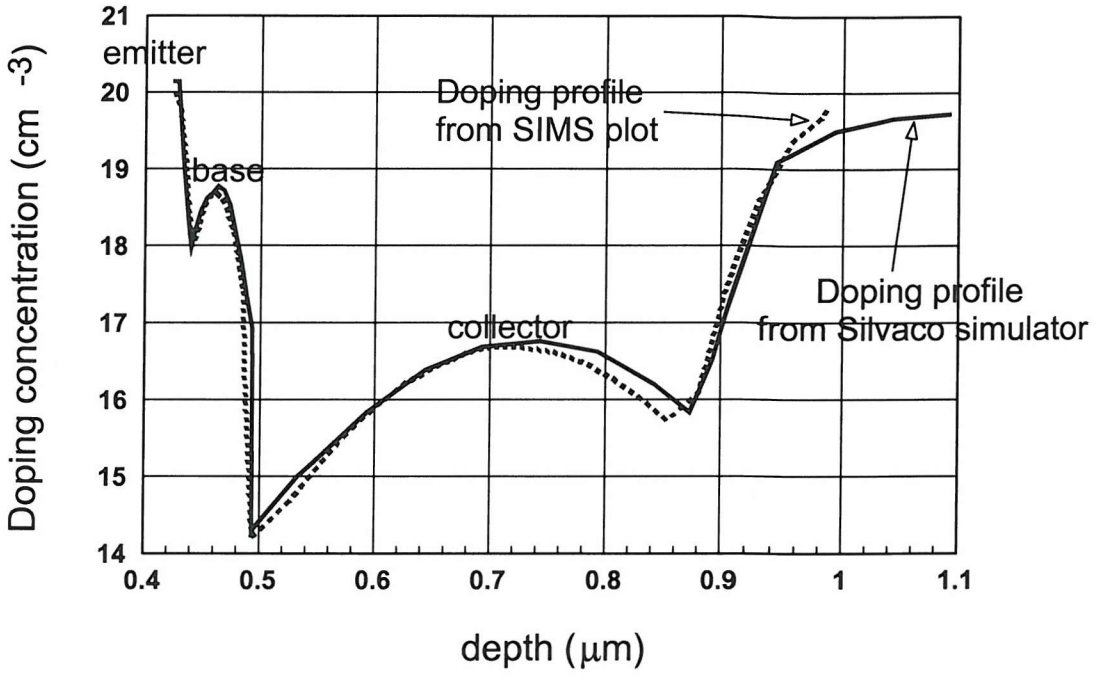

Figure 6.9: Figure shows the doping profile in the published Kondo device and the profile used in the Atlas simulation.

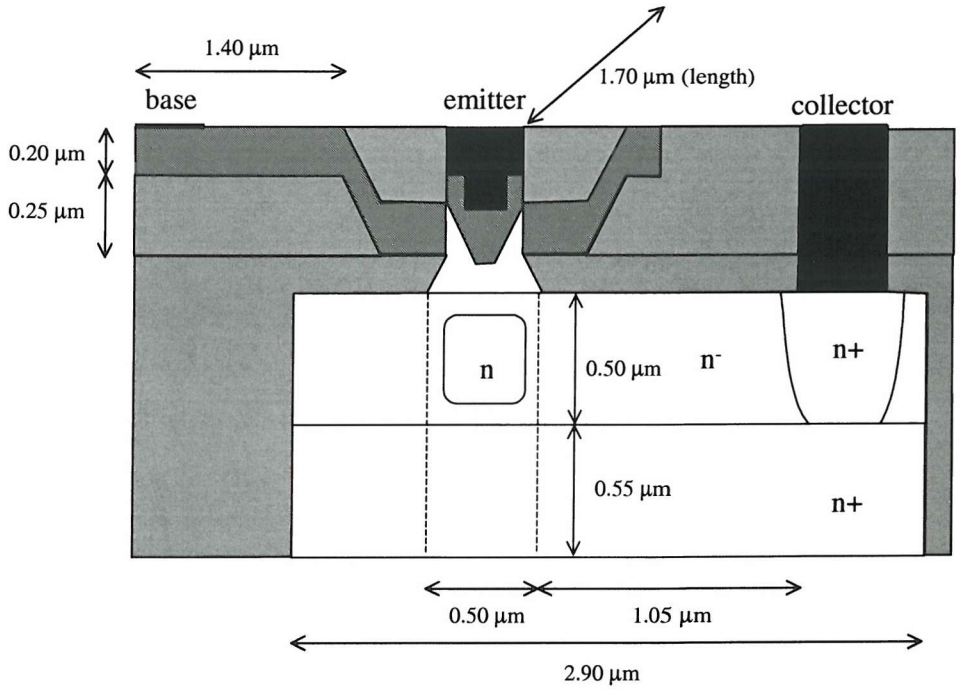

Figure 6.10: Figure shows the dimension of the Kondo structure used in Atlas.

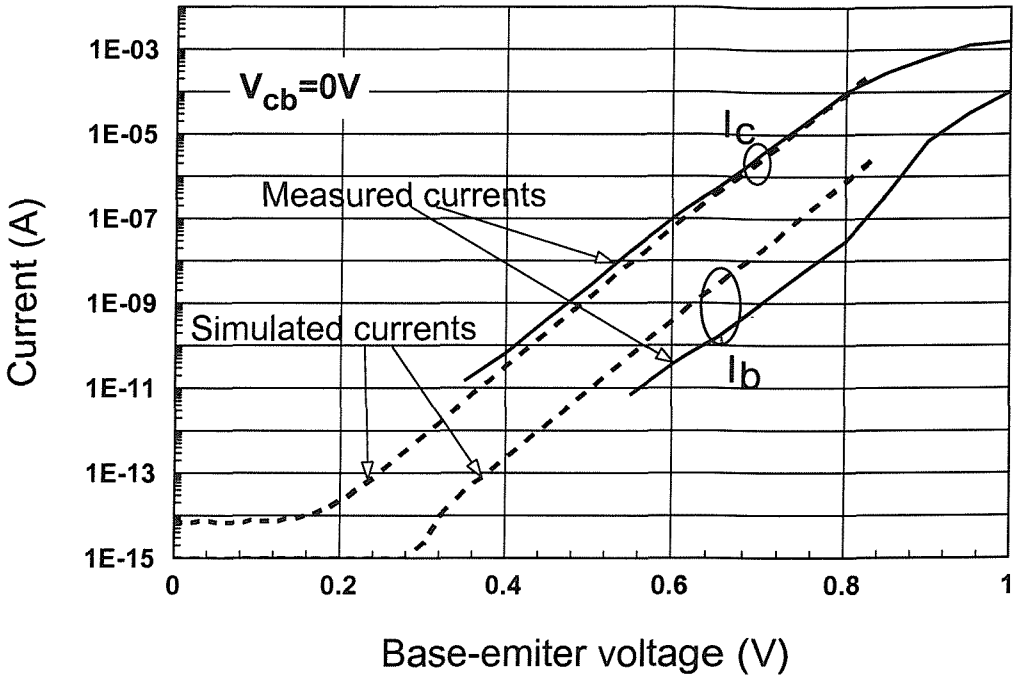

Figure 6.11: Gummel plot comparing the collector and base current from the published Kondo device with those obtained from simulation.

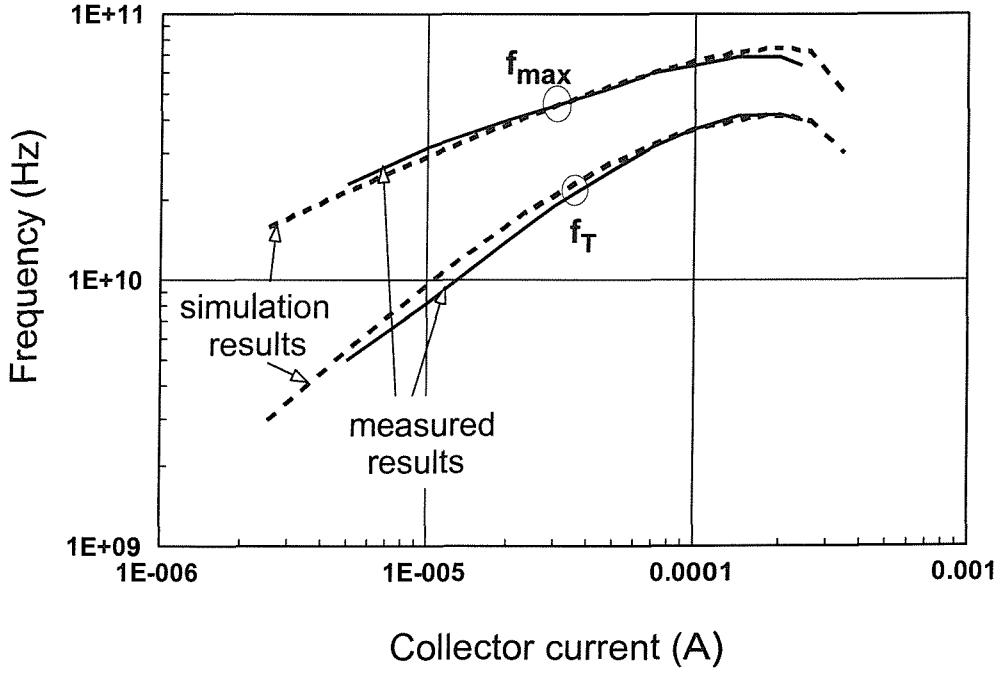

Figure 6.12: f_{max} and f_T plot with regarding to current from published Kondo device and those from simulation results.

increases base current flowing into the emitter. Also, not enough information can be obtained from the research paper [10] regarding the emitter polysilicon/SiGe interface in order to model it properly. However, as the primary concern in this modelling is the speed and power of device no further study was carried out to investigate the cause of the high base current. This is because it does not directly affect the f_T and f_{max} figure of merits which reflect the frequency performance of the device.

f_{max} and f_T are used as figures of merit to assess performance. In the Atlas simulation, sinusoidal voltage or current of different frequencies were applied to the device structure from which sinusoidal terminal currents and voltages were calculated. Then using the relationship

$$\tilde{Y_{ij}} = G_{ij} + j\omega C_{ij} = \frac{\tilde{I_i}}{\tilde{V_j}} \tag{6.1}$$

the frequency dependent admittance matrix can be calculated. The y-parameters are obtained by the formula below;

$$Y_{11} = G_{base,base} + j\omega C_{base,base} \tag{6.2}$$

$$Y_{12} = G_{base,collector} + j\omega C_{base,collector} \tag{6.3}$$

$$Y_{21} = G_{collector,base} + j\omega C_{collector,base} \tag{6.4}$$

$$Y_{22} = G_{collector,collector} + j\omega C_{collector,collector} \tag{6.5}$$

where $G_{base,base}$ and $G_{collector,base}$ are the conductances obtained at the base and collector terminals respectively when a small ac signal is applied at the base terminal. $G_{base,collector}$ and $G_{collector,collector}$ are the conductances obtained at the base and collector terminals respectively when a small ac signal is applied at the collector terminal. $C_{base,base}$ and $C_{collector,base}$ are the capacitances obtained at the base and collector terminals respectively when a small ac signal is applied at the base terminal. $C_{base,collector}$ and $C_{collector,collector}$ are the capacitances obtained at the base and collector terminals respectively when a small ac signal is applied at the collector terminal.

The transducer power gain and ac gain of the device are calculated with the extracted y-parameters using the equation [101]:

$$\beta_{ac}, \text{ a.c. gain} = 20log\left|\frac{Y_{21}}{Y_{11}}\right| \tag{6.6}$$

$$\text{a.c. power gain} = 10log\left(\frac{Re(Y_{21}-Y_{12})^2+Im(Y_{21}-Y_{12})^2}{4[Re(Y_{11})Re(Y_{22})-Re(Y_{12})Re(Y_{21})]}\right) \quad (6.7)$$

The f_{max} and f_T figures of merit are obtained at unity a.c. power gain and zero a.c. gain respectively. Note that a negative sign was required for β_{ac} formula due to the current flow sign convention in Atlas.

Figure 6.12 shows the simulated and the published f_{max} and f_T of the device. Note that the doping profile between the modelled and measured device, shown in Figure 6.9, is very close where no significant "fitting" of structural data was required. The simulation result shows very good agreement with the published result with peak f_{max} of about 70 GHz and peak f_T of about 40 GHz at around 200 μA. This supports the assumption that the difference in base current between the modelled and measured devices does not affect the high frequency modelling. Good agreement in the collector current, f_{max}, and f_T versus I_c indicates that the Atlas modelling is accurate and it is able to model the Kondo device to a very good degree of accuracy.

6.3 Comparison between the Proposed Lateral SiGe HBT and the Vertical SiGe HBT of Kondo *et. al.* [10]

The structural advantages of a lateral structure over a vertical structure is established in this section by comparing, using Atlas, the modelling results of the proposed lateral SiGe HBT and those of the vertical SiGe HBT described in the previous section.

The lateral HBT was assumed to have the same active transistor doping profile and germanium concentration as the Kondo device of the previous section so as to investigate only the extrinsic structural effects of the lateral device on the transistor's performance. Also, since the vertical device was fabricated using a $0.2\mu m$ design rule process [10], the lateral device was also structured according to a 0.2 μm design rule process, as illustrated in Figure 6.13. For the same reason, identical physical models and parameters as those used in the vertical SiGe HBT modelling were used for the lateral simulations. Both device lengths were 1.7 μm in the unsimulated 3rd

dimension. The proposed lateral device input file is shown in Appendix D.

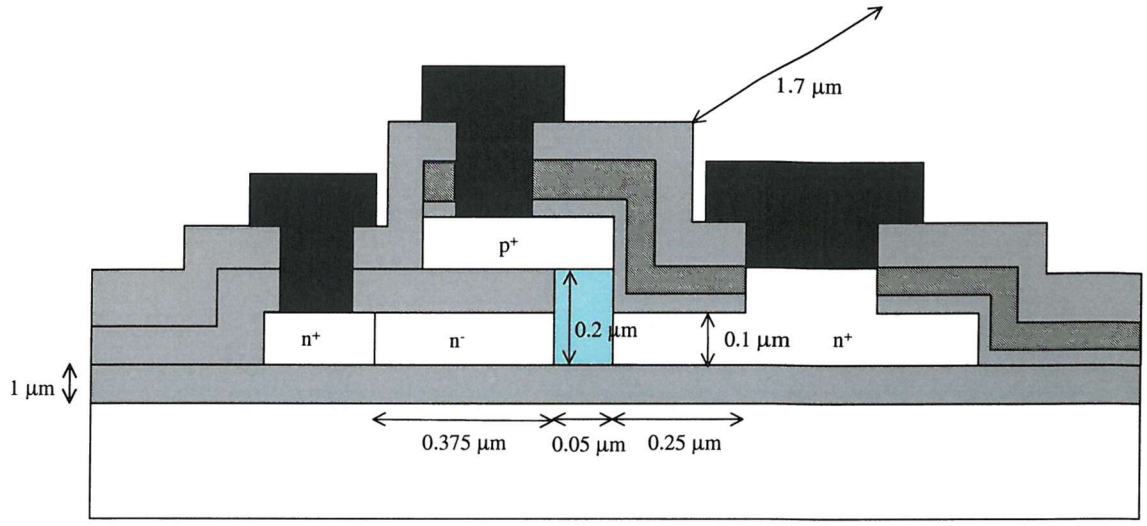

Figure 6.13: Figure showing the structural dimension of the proposed lateral SiGe HBT used in the Atlas modelling.

The Gummel plots of both devices from Atlas modelling are shown in Figure 6.14. As expected, the lateral device, with smaller emitter area ($0.1 \times 1.7\mu m^2$) than the vertical device ($0.2 \times 1.7\mu m^2$), has a smaller collector current than the vertical device for a given V_{be}. Therefore, the lateral device would be more suitable than vertical device for low power operation. This is because one dimension of the lateral device emitter is defined by the epi-layer thickness whereas for vertical device, it was defined by the minimum lithography. The modelled base currents of both the vertical and lateral devices are shown to be almost similar, where the modelled lateral device base current is very slightly lower than the modelled vertical device base current.

Figure 6.15 shows the high frequency performance of both devices. Both lateral f_T and f_{max} peaked at much lower collector current (i.e. 40 μA) than the vertical device (i.e. 200 μA). This shows that lateral devices have an advantage over vertical devices for low power high speed operation. Peak f_T of the lateral device, 33 GHz, is slightly lower than peak f_T of the vertical device, 40 GHz, even though they are expected to be similar because similar active region doping profiles and voltage biases were used. This could be due to more stored charge that may present in the lateral

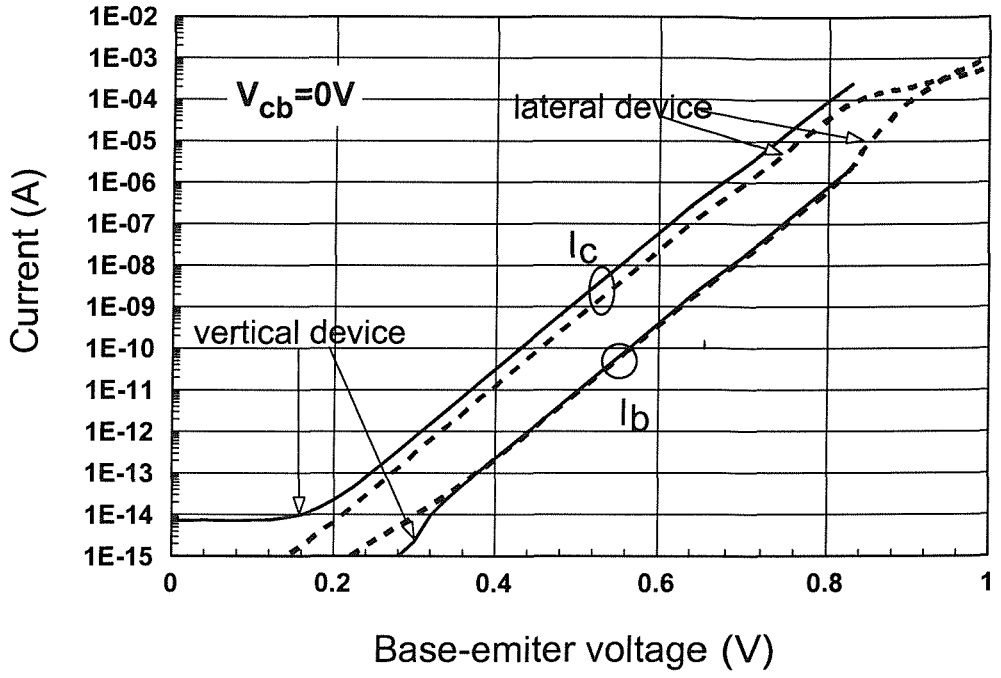

Figure 6.14: The gummel plots from the Atlas modelling of the lateral and vertical device.

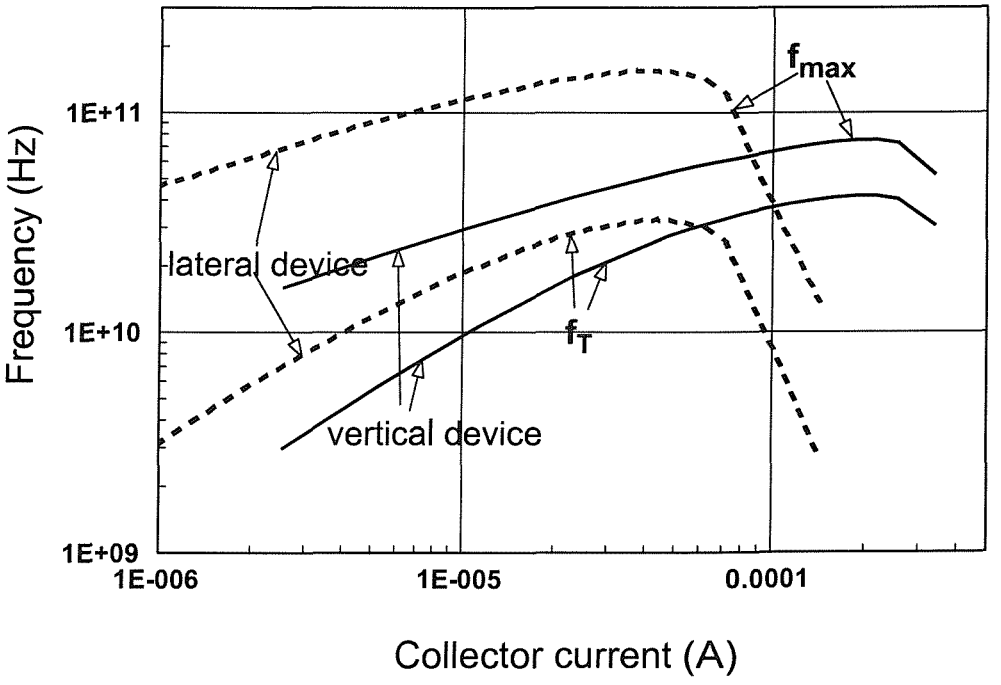

Figure 6.15: The f_T and f_{max} vs collector current plots from Atlas modelling of the lateral and vertical device.

emitter region than in the vertical device emitter as the lateral device emitter is wide (more than 0.25 μm, as shown in Figure 6.13) and not optimised for this simulation. However, the lateral device peak f_{max}, 160 GHz, is much higher than the vertical device peak f_{max} of 75 GHz. To first order approximation, f_{max} is related to f_T as in equation 6.8 below [68],

$$f_{max} = \sqrt{\frac{f_T}{8\pi C_{jc} R_b}} \tag{6.8}$$

where C_{jc} is the collector-base depletion capacitance and R_b is the base resistance. Equation 6.8, shows that both C_{jc} and R_b need to be low in order to enhance f_{max}.

Using the extraction technique in [102], C_{jc} and R_b can be extracted using small signal z-parameters as below,

$$R_b = Re(Z_{11} - Z_{12}) \tag{6.9}$$

$$C_{jc} = -\frac{1}{\omega Im(Z_{22} - Z_{21})} \tag{6.10}$$

where Z_{11}, Z_{12}, Z_{21} and Z_{22} are 2-port Z parameters of bipolar transistor. Equations 6.9 and 6.10 are further explained in Appendix E. Note that Equation 6.9 and 6.10 do not take the substrate capacitance and resistance into account. The Kondo vertical device simulation above did not model the device substrate exactly, as the real thickness of the substrate is not known. Also, in both vertical and lateral device simulations, the substrates were not grounded and were allowed to float. However, it was decided that the substrate does not significantly affect the f_T of the Kondo vertical device as the simulation result matched very well with the published result [10] even without grounding the substrate. Also, Equation 6.9 and 6.10 will be shown later on to predict the base resistance and collector-base capacitance accurately for approximating the device f_{max}.

Using equations 6.9 and 6.10, the base resistance and collector-base capacitance are found to be 319 Ω and 0.861 fF, respectively, for the vertical Kondo device at peak f_{max}. Using Equation 6.8 as a first order approximation, f_{max} is calculated as 76 GHz which is very close to the simulation and published [10] value of 70 GHz. This shows that Equation 6.8, 6.9 and 6.10 give very good prediction of the device f_{max}.

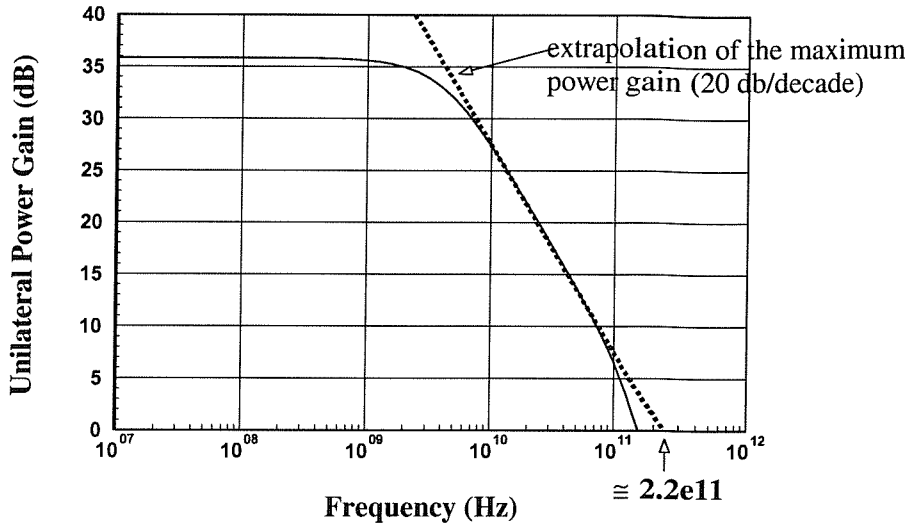

Figure 6.16: The extrapolated f_{max} of the lateral device is found to be approximately 220 GHz. This is consistence with the first order approximation of f_{max} using Equation 6.8.

Similarly for the lateral device, at peak f_{max}, using Equation 6.9 and 6.10, the base resistance and collector/base capacitance are found to be 172 Ω and 0.139 fF, respectively. Again using Equation 6.8, f_{max} is calculated as 234 GHz which is much larger than the simulation value of 160 GHz. This can be explained by looking at the unilateral power gain versus frequency plot, at peak f_{max}, shown in Figure 6.16. The unilateral power gain is the forward power gain in a feedback amplifier with its reverse power gain set to zero. f_{max} is the frequency when the unilateral power gain equal to 0 dB. However in this case, it can be seen that a pole is present in the plot at about 100 GHz and thus causes the unilateral power gain to decrease faster than 20 $dB/decade$. This pole is not taken into account by Equation 6.8 and therefore, the simulation f_{max} is smaller than the calculation f_{max}. By extrapolating the unilateral power gain according to 20 $dB/decade$, as shown in Figure 6.16, the f_{max} without the extra pole at 100 GHz is found to be approximately 220 GHz, which is very close to the calculation value of 234 GHz. Therefore, if the extra pole can be pushed to a frequency much higher than 230 GHz, the f_{max} of the lateral device will be as high as 220 GHz.

From Equations 6.9 and 6.10, the lateral device has a noticeably smaller base resistance and smaller collector-base depletion capacitance than the vertical device because it has a more direct base contact capability from the wafer surface that

reduces the base resistance, and it has much smaller collector-base junction area which reduces the junction capacitance. Therefore, from equation 6.8, it is no surprise to find the lateral device has much more superior f_{max} than the vertical device.

As the comparison indicates, if the proposed lateral HBT is manufacturable, it is good for high performance applications. High performance implies low power and high frequency. Low power implies that the device needs to have low parasitic resistance and capacitances. The lateral HBT was demonstrated to have lower R_b and C_{jc} than the vertical HBT. Also, the lateral HBT uses SOI substrate in order to minimise C_{js}, the substrate capacitance. Lower parasitics allow for lower bias current for a given frequency of operation [103], and the lateral HBT was shown to have much lower operating current than the vertical HBT for similar operating frequency. High frequency also implies that f_T and f_{max} must be high. The lateral HBT has f_T comparable to the vertical HBT but superior f_{max}. Also, from Equation 6.8, high f_{max} implies that R_b and C_{jc} are low. However, R_e and R_c could be high for the lateral HBT due to the very thin epi-layer used in order to reduce C_{je} and C_{jc}. But if the I_c of the lateral HBT is low, the I_cR_c and I_eR_e products are also low implying no real increase in voltage drop relative to a vertical HBT which operates at higher current.

6.4 Conclusion

Since there does not appear to have been a published working lateral SiGe HBT where the emitter, base and collector form a true lateral double heterojunction structure, a novel lateral SiGe HBT structure, meant for high speed and low power applications, was presented. This device was compared to an existing state of the art, ultra low power and high speed vertical SiGe HBT transistor by full numerical simulations using Atlas. The proposed lateral SiGe HBT was found to out-perform the vertical SiGe HBT especially in f_{max}. Its f_{max} was found to be 160 GHz and could potentially be improved up to 220 GHz. With its f_T comparable to the vertical SiGe HBT device, the lateral SiGe HBT has great potential for low power and high speed applications.

Chapter 7

Conclusions and Further Work

SiGe HBT technology has demonstrated itself to be capable of providing continued improvements in bipolar transistor performance. With silicon bipolar technology approaching its limits of capability, SiGe HBT technology can provide the much needed room and space for further exploration and improvement. Perhaps most importantly, SiGe HBT technology has opened up the possibility for its integration into the existing BiCMOS large-scale production line technology. This is fast becoming a reality. However, much work is still remains to be done, especially in characterising the changes in device physical properties due to germanium incorporation. And all these are essential to ensure that this new SiGe HBT technology, when it is finally employed, is reliable and can be implemented with high efficiency and good yield.

The aim of this thesis has therefore concentrated on developing new parameter extraction methods that can be used for studying these new SiGe HBT characteristics and also that can simply be employed as simple and quick measurement tools that yield useful and accurate information regarding SiGe HBT's. It is reckoned that the availability of such methods will facilitate greater control and insight during device processing. On the other hand, this thesis also explores the potential of lateral SiGe HBT structures. A lateral device structure was shown to have many advantages over a vertical device structure, especially for high speed and low power applications.

Previous theory and experimental results have established that bandgap grading across the neutral base can have a significant effect on the electrical properties of SiGe HBT's, including the output conductance and the base transit time. A new low

frequency electrical method was developed to measure the bandgap difference across the neutral base of a SiGe HBT's. The method does not rely on using a silicon or SiGe control device, or detailed modelling of SiGe transport parameters such as bandgap narrowing, mobility, density of states, etc.. By using the temperature dependence of the ratio of the forward active output conduction to the reverse active output conductance, the effective bandgap grading due to the presence of germanium, including heavy doping effects, was successfully measured. The accuracy of the method was derived to be within approximately 1.5% germanium grading, theoretically, assuming a 5% accuracy in measuring device electrical parameters such as collector current, output conductance and temperature. In detailed numerical simulations, the extraction results were found to be within 5% of agreement with the simulator internal data. Experimental results further demonstrated the practicality of the method by producing reasonable measurement results of the bandgap difference across a neutral base of an n-p-n SiGe HBT with parasitic potential barrier.

SiGe bases are usually highly doped and of submicron thickness. It is known that parasitic potential barriers can easily formed under these conditions due to boron out-diffusion. These parasitic potential barriers are known to reduce the SiGe HBT's collector current and the cut-off frequency. An alternative electrical method for simultaneous extraction of parasitic potential barrier heights at emitter-base and collector-base junctions of SiGe HBT's was presented. This method was developed by adapting the neutral base bandgap difference extraction method described above. The method provides a more direct measure of parasitic barrier-related quantities and does not depend upon a detailed knowledge of the temperature dependence of SiGe density of states functions, carrier mobility, etc.. It depends instead upon a direct measure of the bandgap difference across the Si-SiGe transition region and upon the positional variation of base impurity concentration in the vicinity of the potential barrier. In numerical simulation, the extraction results were found to be within 10% of agreement with the simulator internal data. Experimental results show that a reasonable value was extracted for the collector-base junction parasitic potential barrier height when correlated with the collector current reduction compared to an identical SiGe HBT known to have no barrier using the simple model of Slotboom *et al.*. Numerical

modelling of the measured SiGe HBT device further supported this result.

Finally, an investigation was carried out to assess the potential of a lateral SiGe HBT structure for high performance applications. First of all, various issues regarding lateral bipolar structure, such as self-aligned base contact and base width definition were presented. The lateral bipolar structure was assessed by means of comparison to industrial vertical bipolar structures which are a widely used. It was found that a lateral structure has many advantages over the vertical bipolar structure, and is perhaps more suitable for low power microwave applications. Also a pseudo-heterojunction lateral bipolar, known as the hybrid mode bipolar, was discussed. Its operating principle is heterojunction like and yields good results especially in terms of current gain.

However, the practical aim of this investigation was to assess the potential of a real SiGe HBT in a lateral structure. Therefore, as there does not appear to have been a published working lateral SiGe HBT where the emitter, base and collector form a true lateral double heterojunction structure, a novel lateral SiGe HBT structure was proposed. The proposed processing steps for this device was briefly discussed. Numerical simulation work was performed to assess the high-speed capability of this device. An existing industrial state-of-the art vertical SiGe HBT designed for ultra-low-power and high speed operation in rf telecommunication systems, developed by Kondo *et al.*, was used as a yard stick for judging the performance of the proposed lateral SiGe HBT. Similar doping profile, germanium concentration and design rules, from Kondo *et al.*, were applied for the simulations of the vertical and lateral structures. The results show that both devices have comparable f_T but that the lateral device out-performed the vertical device in f_{max}. The lateral device's f_{max} was found to be 160 GHz, more than twice that of the vertical device, and could potentially be improved up to 220 GHz. The tremendous f_{max} capability for the lateral SiGe HBT was recognised to be due to its low base resistance and collector-base depletion capacitance nature. Also, the smaller achievable junction areas of the lateral SiGe HBT enabled its f_T and f_{max} to peak at a low 40 μA, as compared to 200 μA produced by the vertical SiGe HBT. Therefore, in this case, the lateral SiGe HBT was found to out-perform the vertical SiGe HBT in terms of low power and high speed.

There are areas in this work that merits further research. The parasitic potential

barrier height extraction technique can probably be extended to measuring the parasitic potential barrier width as well. Knowing the barrier width would be useful for determining the width of the undoped SiGe spacers needed to suppress boron out-diffusion. Besides, Slotboom *et al.* [20] has a model that is able to predict the f_T and collector current degradation from the parasitic potential barrier width and height. The proposed lateral SiGe HBT is demonstrated numerically to have great potential. Therefore, fabricating it seems to be the logical step to follow next. Some of the new processing steps will require much experimenting and testing. This includes making the growth cavity microstructure, and also perfecting the confined lateral selective silicon and SiGe epitaxy growth technique in the microstructure. The combination of the lateral structure and SiGe heterojunction effect is surely worth further exploring in the light of all these advantages discovered. This can be done with more novel lateral structures or more in-depth study on issues faced by lateral structure such as excess stored charges along the thin emitter body.

Appendix A

Philips Unified Mobility model

The Philips Unified mobility model [60, 61] takes into account the: (1) Distinct acceptor and donor scattering (2) Carrier-carrier scattering (3) Screening

The following expressions describe the carrier mobilities and are reproduced from [56]. The mobility model for electron carrier mobility is:

$$\mu_n^{-1} = \mu_{latt,n}^{-1} + \mu_{D+A+P}^{-1} \tag{A.1}$$

where

$$\mu_{latt,n} = MMXN \left(\frac{T}{300}\right)^{-TETN} \tag{A.2}$$

$$\mu_{D+A+P} = \mu_{N,n}\frac{N_{SC,n}}{N_{SC,eff,n}}\left(\frac{NRFN}{N_{SC,n}}\right)^{ALPN} + \mu_{c,n}\frac{n+p}{N_{SC,eff,n}} \tag{A.3}$$

where $MMXN$ is the maximum electron mobility, 1417.0 default, $TETN$ is an exponent used for temperature dependence of lattice scattering, 2.285 default, $NRFN$ is the reference impurity concentration, 9.68×10^{16} default, $ALPN$ is 0.68 default, n is the electron concentration, p is the hole concentration, T is the temperature. $\mu_{N,n}$, $\mu_{c,n}$, $N_{SC,n}$ and $N_{SC,eff,n}$ are given by

$$\mu_{N,n} = \frac{MMXN^2}{MMXN - MMNN}\left(\frac{T}{300}\right)^{3(ALPN)-1.5} \tag{A.4}$$

$$\mu_{c,n} = \frac{MMXN \times MMNN}{MMXN - MMNN}\left(\frac{300}{T}\right)^{0.5} \tag{A.5}$$

$$N_{SC,n} = N_D^* + N_A^* + p \tag{A.6}$$

$$N_{SC,eff,n} = N_D^* + N_A^* G(P_n) + \frac{p}{F(P_n)} \tag{A.7}$$

where $MMNN$ is a parameter to determine electron mobility at high dopant and/or carrier levels, 52.2 default. The effective impurity levels N_D^* and N_A^* take ultra-high doping effects into account and are defined by

$$N_D^* = N_D\left[1+\frac{1}{CRFD+\left(\frac{NRFD}{N_D}\right)^2}\right] \tag{A.8}$$

$$N_A^* = N_A\left[1+\frac{1}{CRFA+\left(\frac{NRFA}{N_A}\right)^2}\right] \tag{A.9}$$

where N_D is the donar concentration, N_A is the acceptor concentration, $CRFD$ is a factor determining the ultra-high doping effects for donors, 0.21 default, $CRFA$ is a factor determining the ultra-high doping effects for acceptors, 0.5 default, $NRFD$ is a reference impurity concentration for donors to model ultra-high doping effects, 4×10^{20} default, $NRFA$ is the reference impurity concentration for acceptors to model ultra-high doping effects, 7.2×10^{20}.

The functions $F(P_n)$ and $G(P_n)$ that take the finite mass of scattering holes and the repulsive potential for acceptors into account, are given by

$$F(P_n) = \frac{0.7643P_n^{0.6478}+2.2999+6.5502\frac{m_e}{m_h}}{P_n^{0.6478}+2.3670-0.8552\frac{m_e}{m_h}} \tag{A.10}$$

$$G(P_n) = 1-\frac{0.89233}{\left[0.41372+P_n\left(\frac{m_0}{m_e}\frac{T}{300}\right)^{0.28227}\right]^{0.19778}}+\frac{0.005978}{\left[P_n\left(\frac{m_e}{m_0}\frac{300}{T}\right)^{0.72169}\right]} \tag{A.11}$$

For values of $P_n \leq P_{n,min}$, $G(P_{min})$ is used instead of $G(P_n)$, where $P_{n,min}$ is the value at which $G(P_n)$ reaches it's minimum. The P_n parameter that takes screening effects into account, is given by

$$P_n = \left(\frac{2.459}{3.97\times10^{13}N_{SC,n}^{-2/3}}+\frac{3.828}{\frac{1.36\times10^{20}}{n+p}\frac{m_e}{m_0}}\right)^{-1}\left(\frac{T}{300}\right)^2 \tag{A.12}$$

Similar expressions hold for holes. The effective electron and hole mass that are used are $m_e = 1.0m_0$ and $m_h = 1.258m_0$ with m_0 being the free electron rest mass, 9.108×10^{-31}kg.

Appendix B

Derivation of the Electrical Bandgap Grading Extraction Technique

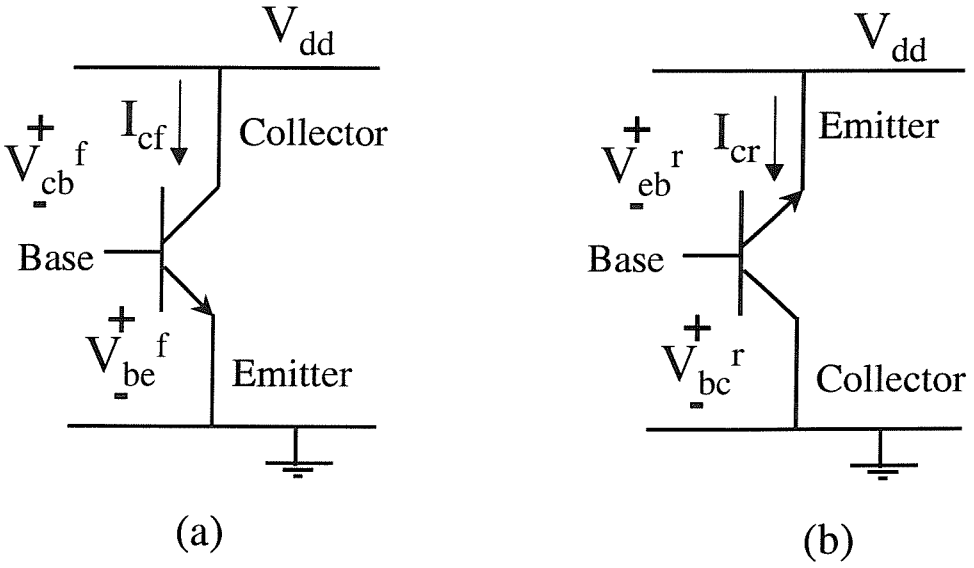

Figure B.1: Circuit diagram of an n-p-n transistor illustrating the bias condition and the current flow when the transistor is biased at the (a) forward active region of operation, and (b) reverse active region of operation.

For a SiGe HBT operating in forward active region, the output conductance is

written as,

$$\begin{aligned} g_{of} &= \left.\frac{dI_{cf}}{dV_{cb}^{f}}\right|_{dV_{be}^{f}=0} \\ &= \left.-\frac{dI_{cf}}{dW}\frac{dW}{dV_{bc}^{f}}\right|_{dV_{be}^{f}=0} \end{aligned} \tag{B.1}$$

where the "f" subscripts and superscripts refer to the transistor operating in the forward active region. g_{of} is the a.c. output conductance, I_{cf} is the collector current, illustrated in Figure B.1, V_{cb}^{f} is the reverse biased collector-base voltage, V_{be}^{f} is the forward biased base-emitter voltage and W is the width across the neutral base region.

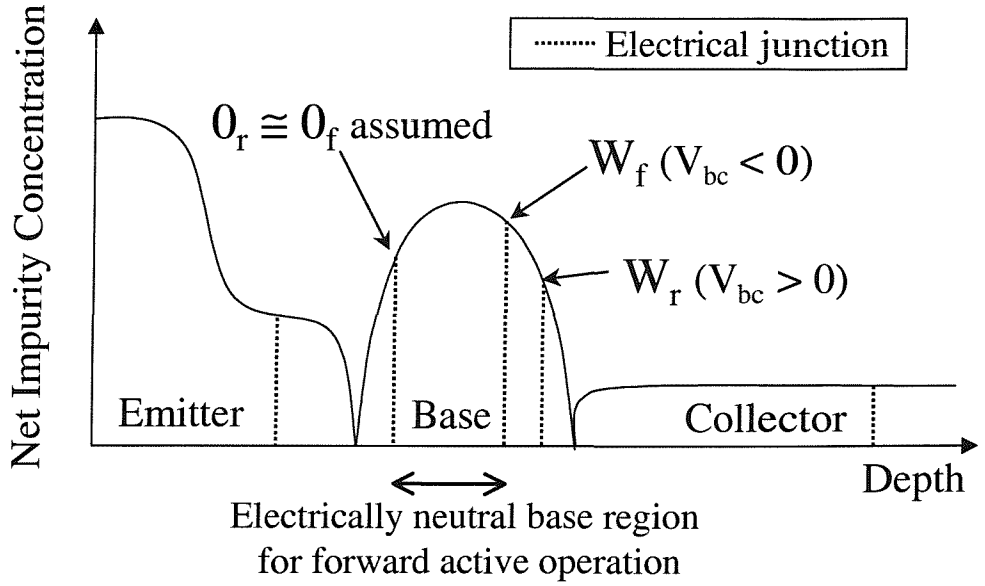

Figure B.2: Figure illustrating the difference of the neutral base position in the forward active region mode and reverse active region mode. For a highly doped base, which is common for a SiGe HBT, the position of 0_r can be made very close to the position of 0_f for low emitter/base junction reverse bias, in reverse active operation, because most of the space-charge layer movement will take place in the lower-doped emitter side of the junction.

SiGe HBT collector current in forward active region mode is written as [104],

$$\begin{aligned} I_{cf} &= -\frac{qA_e n_{io}^2}{G_b^f} exp\frac{qV_{be}^f}{kT} \\ &= -qA_e exp\left(\frac{V_{be}^f}{V_T}\right)\left(\int_{0_f}^{W_f}\frac{N_b(x)}{D_{nb}(x)n_{io}^2(x)}exp\left(-\frac{\Delta E_{gb}}{kT}\right)dx\right)^{-1} \\ &= -qA_e exp\left(\frac{V_{be}^f}{V_T}\right)\left(\int_{0_f}^{W_f}\frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)}dx\right)^{-1} \end{aligned} \tag{B.2}$$

since,

$$
\begin{aligned}
G_b^f &= \text{Gummel number} = \int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)} exp - \frac{\Delta E_{gb}}{kT} dx \\
n_{ie}^2(x) &= n_{io}^2(x) exp\left(\frac{\Delta E_{gb}}{kT}\right) \\
V_T &= \frac{kT}{q}
\end{aligned}
$$

where q is the electronic charge, A_e is the emitter-base junction area, n_{io} is the intrinsic carrier concentration, k is the Boltzmann constant, T is the absolute temperature, V_T is the thermal voltage, W_f and 0_f are the neutral edge of the base region at the collector and emitter side respectively, shown in Figure B.2, $N_b(x)$ is the positional dependent base impurity profile, $D_{nb}(x)$ is the positional dependent base diffusivity of electrons, ΔE_{gb} is the total bandgap narrowing in the base, $n_{ie}(x)$ and $n_{io}(x)$ are the positional dependent effective intrinsic carrier concentration and intrinsic carrier concentration, respectively.

$$
\begin{aligned}
\left.\frac{dI_{cf}}{dW}\right|_{dV_{be}^f=0} &= -qA_e exp\left(\frac{V_{be}^f}{V_T}\right) \frac{d}{dW}\left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)^{-1} \\
&= qA_e exp\left(\frac{V_{be}^f}{V_T}\right) \left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)^{-2} \times \\
&\quad \frac{d}{dW}\left[\left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)_{W_f} - \left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)_{0_f}\right] \\
&= qA_e exp\left(\frac{V_{be}^f}{V_T}\right) \left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)^{-1} \times \\
&\quad \left(\frac{N_b}{D_{nb}n_{ie}^2}\right)_{W_f} \left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)^{-1} \\
&= I_{cf}\left(\frac{N_b}{D_{nb}n_{ie}^2}\right)_{W_f} \left(\int_{0_f}^{W_f} \frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)} dx\right)^{-1}
\end{aligned} \tag{B.3}
$$

The SiGe HBT base-collector depletion capacitance is written as,

$$
\begin{aligned}
C_{jc}^f &= \frac{dQ_b^f}{dV_{bc}^f} \\
&= qA_c \frac{d\int_{0_f}^{W_f} N_b(x)dx}{dW} \frac{dW}{dV_{bc}^f} \\
&= qA_c \left(\int_{0_f}^{W_f} \frac{dN_b}{dW} dx + N_b(W_f)\right) \frac{dW}{dV_{bc}^f}
\end{aligned}
$$

$$= qA_cN_b(W_f)\frac{dW}{dV_{bc}^f} \tag{B.4}$$

$$\frac{dW}{dV_{bc}^f} = \frac{C_{jc}^f}{qA_cN_b(W_f)} \tag{B.5}$$

C_{jc}^f is the junction capacitance of the reverse biased collector-base junction, Q_b^f and V_{bc}^f are the base charge and voltage across the reverse biased collector-base depletion region, A_c is the collector-base junction area.

Putting Equation B.5 and Equation B.3 together, the low frequency a.c. output conductance for a SiGe HBT operating in forward active mode, illustrated in Figure B.1, becomes [81];

$$\begin{aligned} g_{of} &= -\frac{dI_{cf}}{dW}\frac{dW}{dV_{bc}^f} \\ &= -\frac{C_{jc}^f}{qA_cN_b(W_f)}\left[I_{cf}\left(\frac{N_b}{D_{nb}n_{ie}^2}\right)_{W_f}\left(\int_{0_f}^{W_f}\frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)}dx\right)^{-1}\right] \\ &= -\frac{I_{cf}C_{jc}^f}{qA_cD_{nb}(W_f)n_{ie}^2(W_f)}\left(\int_{0_f}^{W_f}\frac{N_b(x)}{D_{nb}(x)n_{ie}^2(x)}dx\right)^{-1} \end{aligned} \tag{B.6}$$

Appendix C

Error analysis of the bandgap difference across neutral base extraction method

C.1 Error Analysis for High Emitter Doping

Assuming uniform base doping, if the germanium is graded linearly across the base, the bandgap reduction due to germanium will be increasing linearly across the base. Since the germanium affect the bandgap linearly across the base, from Figure C.1, the error in the neutral base bandgap difference extraction method that is caused by the difference in emitter-base electrical junction positions for forward bias, 0_f, and zero reverse bias, 0_r, will be equivalent to $\Delta W/W_b$.

Using simple theory, the emitter-base depletion capacitance can be written as [105]:

$$C_{je} = \frac{\epsilon_s}{W_{je}} \tag{C.1}$$

For high emitter doping where almost all the depletion junction is in the base, a one-sided abrupt junction C_je [105]:

$$C_{je} = \sqrt{\frac{q\epsilon_s N_b}{2(V_{bi} - V_{be})}} \tag{C.2}$$

where ϵ_s is the permitivity of silicon, $1.05 \times 10^{-10} C^2/Nm$, W_{je} is the emitter-base

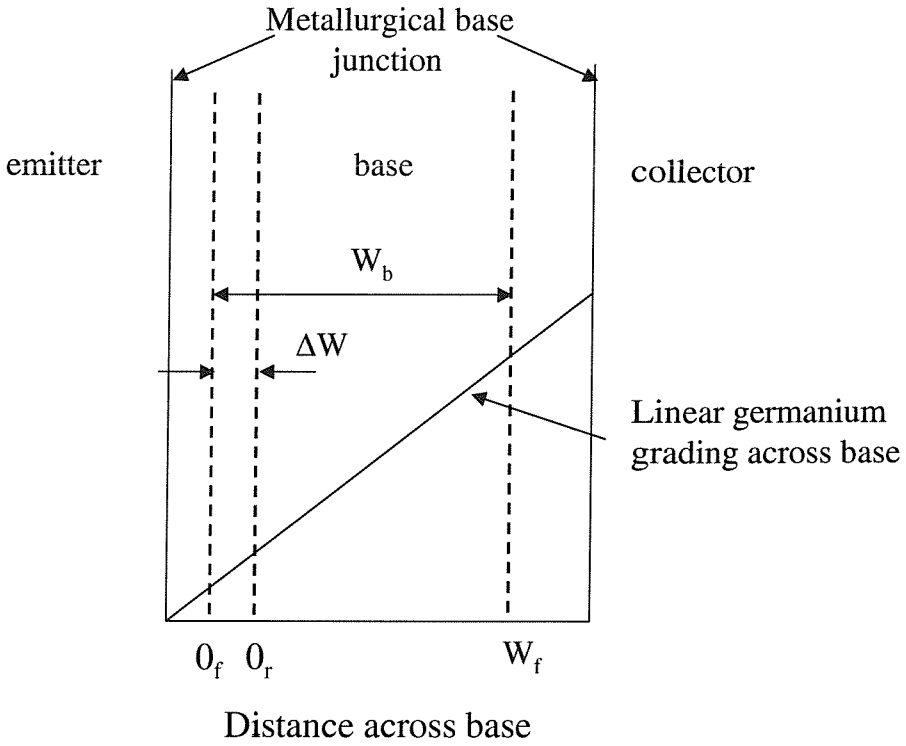

Figure C.1: Figure showing difference between the emitter-base electrical junction positions for forward bias, 0_f, and zero reverse bias, 0_r. It was assumed to be similar in the neutral base bandgap difference extraction method and it is found that the error can be approximated by $\Delta W/W_b$.

depletion region width, N_b is the base doping, V_{bi} built-in voltage, V_{be} voltage across the emitter-base junction. The built in voltage for abrupt and one-sided junction, with uniform doping and in room temperature, is [105]:

$$V_{bi} = \frac{kT}{q} \ln\left(\frac{N_e N_b}{n_{io}^2}\right) \tag{C.3}$$

From [86] $N_e = 10^{21} cm^{-3}$ and $N_b = 5 \times 10^{18} cm^{-3}$. V_{bi} becomes 1.153 eV. Therefore, if the base-emitter junction is forward biased for 0.7 V, $C_{je}(0_f)$ becomes $0.919 \times 10^{-6} F/cm^2$. As for zero reverse biased base-emitter junction, $C_{je}(0_r)$ becomes $0.605 \times 10^{-6} F/cm^2$. From Equation C.1:

$$\frac{W_{je}(0_f)}{W_{je}(0_r)} = \frac{C_{je}(0_r)}{C_{je}(0_f)} \approx 0.65 \tag{C.4}$$

For uniformly doped device, heavy doped emitter where most of depletion width is in the base:

$$W_{je}(V_{be} = 0) = W_{je}(0_r) = \sqrt{\frac{2\epsilon V_{bi}}{qN_b}} \tag{C.5}$$

$$\approx 17nm \tag{C.6}$$

Therefore, $W_{je}(0_f) = 11nm$, and $\Delta W = W_{je}(0_r) - W_{je}(0_f) = 6nm$. From [86], W_b is 90 nm, so $\Delta W / W_b \approx 7\%$.

C.2 General Error Analysis

Neglecting the temperature variations of ratios of junction capacitances as well as mobility, density of states and the bias terms, Equation 4.12 becomes,

$$\ln\left(\frac{g_{or}}{g_{of}}\right) - 2\ln\left(\frac{I_{cr}}{I_{cf}}\right) = \frac{\Delta E_g(grade)}{kT} \tag{C.7}$$

where $\Delta E_g(grade) = E_g(0_r) - E_g(W_f)$.

$$\Delta E_g(grade) = kT\left(\ln g_{or} - \ln g_{of} - 2\ln I_{cr} + 2\ln I_{cf}\right) \tag{C.8}$$

Differentiate with temperature,

$$\frac{\delta \Delta E_g(grade)}{\delta T} = \frac{\Delta E_g(grade)}{T} + kT\left(\frac{1}{g_{or}}\frac{\delta g_{or}}{\delta T} - \frac{1}{g_{of}}\frac{\delta g_{of}}{\delta T} - 2\frac{1}{I_{cr}}\frac{\delta I_{cr}}{\delta T} + 2\frac{1}{I_{cf}}\frac{\delta I_{cf}}{\delta T}\right) \tag{C.9}$$

$$\delta \Delta E_g(grade) = \Delta E_g(grade)\frac{\delta T}{T} + kT\left(\frac{\delta g_{or}}{g_{or}} - \frac{\delta g_{of}}{g_{of}} - 2\frac{\delta I_{cr}}{I_{cr}} + 2\frac{\delta I_{cf}}{I_{cf}}\right) \tag{C.10}$$

Appendix D

Kondo device and proposed lateral device input files and 2-D cross sectional diagrams

Kondo device input file

```
go atlas

# vertical SiGe BJT based on advanced low power device by Kondo
# SiGe/Si base layer, 0-15% Ge

mesh  width=1.7
x.m l=0.0    spacing=0.25
x.m l=0.5    spacing=0.25
x.m l=1.2    spacing=0.05
x.m l=1.3    spacing=0.05
x.m l=1.4    spacing=0.05
x.m l=1.65   spacing=0.05
x.m l=1.83   spacing=0.05
x.m l=1.85   spacing=0.03
x.m l=1.87   spacing=0.03
x.m l=1.885  spacing=0.03
x.m l=1.89   spacing=0.03
x.m l=1.90   spacing=0.02
x.m l=1.905  spacing=0.02
x.m l=1.91   spacing=0.02
x.m l=1.92   spacing=0.02
x.m l=1.925  spacing=0.02
x.m l=1.935  spacing=0.03
x.m l=1.955  spacing=0.03
x.m l=1.96   spacing=0.03
x.m l=1.99   spacing=0.03
x.m l=2.00   spacing=0.03
x.m l=2.025  spacing=0.03
x.m l=2.055  spacing=0.03
x.m l=2.09   spacing=0.03
x.m l=2.11   spacing=0.03
x.m l=2.145  spacing=0.03
x.m l=2.175  spacing=0.03
x.m l=2.20   spacing=0.03
x.m l=2.21   spacing=0.03
x.m l=2.24   spacing=0.03
x.m l=2.245  spacing=0.03
x.m l=2.265  spacing=0.03
x.m l=2.275  spacing=0.03
x.m l=2.28   spacing=0.02
x.m l=2.29   spacing=0.02
x.m l=2.295  spacing=0.02
x.m l=2.30   spacing=0.02
x.m l=2.31   spacing=0.02
x.m l=2.315  spacing=0.03
x.m l=2.33   spacing=0.03
x.m l=2.35   spacing=0.03
x.m l=2.37  spacing=0.075
x.m l=2.47  spacing=0.075
x.m l=2.55  spacing=0.05
x.m l=2.80  spacing=0.05
x.m l=2.95  spacing=0.075
x.m l=3.40  spacing=0.075
x.m l=3.95  spacing=0.075
x.m l=4.15  spacing=0.1
x.m l=4.20  spacing=0.1
x.m l=4.30   spacing=0.1
```

```
y.m l=0.00 spacing=0.03
y.m l=0.05 spacing=0.03
y.m l=0.10 spacing=0.03
y.m l=0.13 spacing=0.03
y.m l=0.17 spacing=0.03
y.m l=0.20 spacing=0.03
y.m l=0.23 spacing=0.03
y.m l=0.25 spacing=0.03
y.m l=0.37 spacing=0.03
y.m l=0.40 spacing=0.03
y.m l=0.425 spacing=0.005
y.m l=0.44 spacing=0.005
y.m l=0.45 spacing=0.005
y.m l=0.455 spacing=0.005
y.m l=0.47 spacing=0.005
y.m l=0.49 spacing=0.005
y.m l=0.50 spacing=0.025
y.m l=0.98 spacing=0.025
y.m l=0.99 spacing=0.025
y.m l=1.29 spacing=0.025
y.m l=1.54 spacing=0.1


# eliminate x-nodes

eliminate x.direction x.min=0.00 x.max=1.8 y.min=0.42 y.max=0.487
eliminate x.direction x.min=0.00 x.max=1.8 y.min=0.40 y.max=0.487
eliminate x.direction x.min=0.00 x.max=1.5 y.min=0.40 y.max=0.487

eliminate x.direction x.min=2.4 x.max=4.3 y.min=0.42 y.max=0.487
eliminate x.direction x.min=2.4 x.max=4.3 y.min=0.40 y.max=0.487

eliminate x.direction x.min=0.00 x.max=1.8 y.min=0.6 y.max=1.35
eliminate x.direction x.min=0.00 x.max=1.8 y.min=0.6 y.max=1.35
eliminate x.direction x.min=0.00 x.max=1.2 y.min=0.51 y.max=1.35

eliminate x.direction x.min=0.00 x.max=1.2 y.min=0.25 y.max=0.4

eliminate x.direction x.min=2.40 x.max=3.3 y.min=0.6 y.max=0.95
eliminate x.direction x.min=2.40 x.max=3.3 y.min=0.6 y.max=0.95

eliminate x.direction x.min=4.00 x.max=4.3 y.min=0.6 y.max=1.35
eliminate x.direction x.min=4.00 x.max=4.3 y.min=0.6 y.max=1.35

eliminate x.direction x.min=3.45 x.max=3.9 y.min=0.0 y.max=0.487
eliminate x.direction x.min=3.45 x.max=3.9 y.min=0.0 y.max=0.487
eliminate x.direction x.min=3.45 x.max=3.9 y.min=0.0 y.max=0.487

eliminate x.direction x.min=2.0 x.max=2.2 y.min=0.0 y.max=0.23
eliminate x.direction x.min=2.0 x.max=2.2 y.min=0.0 y.max=0.23

# eliminate y-nodes

eliminate y.direction x.min=1.875 x.max=2.03 y.min=0.55 y.max=1.54
eliminate y.direction x.min=2.20 x.max=2.325 y.min=0.55 y.max=1.54
```

```
# Silicon substrate

region num=1 silicon  \
      P1.X=1.20    P1.Y=0.49  \
      P2.X=4.50    P2.Y=0.49  \
      P3.X=4.50    P3.Y=1.54  \
      P4.X=1.20    P4.Y=1.54

region num=10 silicon  \
      x.min=1.85 x.max=2.35 y.min=0.49 y.max=0.99

region num=11 silicon  \
       x.min=1.30 x.max=4.20 y.min=0.99 y.max=1.54

# Si emitter layer

region num=8 silicon \
      P1.X=1.935    P1.Y=0.425  \
      P2.X=2.265    P2.Y=0.425  \
      P3.X=2.28    P3.Y=0.44  \
      P4.X=1.92    P4.Y=0.44

region num=9 silicon \
      x.min=2.00 x.max=2.20 y.min=0.425 y.max=0.440

# right hand side oxide

region num=2 oxide \
      P1.X=2.31    P1.Y=0.45  \
      P2.X=4.50    P2.Y=0.45  \
      P3.X=4.50    P3.Y=0.49  \
      P4.X=2.35    P4.Y=0.49

region num=2 oxide \
      P1.X=2.275    P1.Y=0.05  \
      P2.X=2.30    P2.Y=0.05  \
      P3.X=2.30    P3.Y=0.20  \
      P4.X=2.275    P4.Y=0.20

region num=2 oxide \
      P1.X=2.24    P1.Y=0.20  \
      P2.X=2.3    P2.Y=0.20  \
      P3.X=2.3    P3.Y=0.23  \
      P4.X=2.24    P4.Y=0.23

region num=2 oxide \
      P1.X=2.24    P1.Y=0.23  \
      P2.X=2.265    P2.Y=0.23  \
      P3.X=2.265    P3.Y=0.40  \
      P4.X=2.24    P4.Y=0.40

region num=2 oxide \
      P1.X=2.20    P1.Y=0.40  \
      P2.X=2.265    P2.Y=0.40  \
      P3.X=2.265    P3.Y=0.425  \
      P4.X=2.20    P4.Y=0.425

# left hand side oxide
```

```
 region num=2 oxide \
       P1.X=0.00     P1.Y=0.45   \
       P2.X=1.89     P2.Y=0.45   \
       P3.X=1.85     P3.Y=0.49   \
       P4.X=0.00     P4.Y=0.49

 region num=2 oxide \
       P1.X=1.9     P1.Y=0.05   \
       P2.X=1.925     P2.Y=0.05   \
       P3.X=1.925     P3.Y=0.20   \
       P4.X=1.9     P4.Y=0.20

 region num=2 oxide \
       P1.X=1.90     P1.Y=0.20   \
       P2.X=1.96     P2.Y=0.20   \
       P3.X=1.96     P3.Y=0.23   \
       P4.X=1.90     P4.Y=0.23

 region num=2 oxide \
       P1.X=1.935     P1.Y=0.23   \
       P2.X=1.96     P2.Y=0.23   \
       P3.X=1.96     P3.Y=0.40   \
       P4.X=1.935     P4.Y=0.40

 region num=2 oxide \
       P1.X=1.935     P1.Y=0.40   \
       P2.X=2.00     P2.Y=0.40   \
       P3.X=2.00     P3.Y=0.425   \
       P4.X=1.935     P4.Y=0.425


 # Silicon Nitride left

 region num=3 Si3N4 \
       P1.X=1.925     P1.Y=0.05   \
       P2.X=1.955     P2.Y=0.05   \
       P3.X=1.955     P3.Y=0.17   \
       P4.X=1.925     P4.Y=0.17

 region num=3 Si3N4 \
       P1.X=1.925     P1.Y=0.17   \
       P2.X=1.99     P2.Y=0.17   \
       P3.X=1.99     P3.Y=0.20   \
       P4.X=1.925     P4.Y=0.20

 region num=3 Si3N4 \
       P1.X=1.96     P1.Y=0.20   \
       P2.X=1.99     P2.Y=0.20   \
       P3.X=1.99     P3.Y=0.37   \
       P4.X=1.96     P4.Y=0.37

 region num=3 Si3N4 \
       P1.X=1.96     P1.Y=0.37   \
       P2.X=2.025     P2.Y=0.37   \
       P3.X=2.025     P3.Y=0.40   \
       P4.X=1.96     P4.Y=0.40

 # Silicon Nitride right

 region num=3 Si3N4 \
```

```
       P1.X=2.245     P1.Y=0.05   \
       P2.X=2.275     P2.Y=0.05   \
       P3.X=2.275     P3.Y=0.17   \
       P4.X=2.245     P4.Y=0.17

 region num=3 Si3N4 \
       P1.X=2.21     P1.Y=0.17   \
       P2.X=2.275     P2.Y=0.17   \
       P3.X=2.275     P3.Y=0.20   \
       P4.X=2.21     P4.Y=0.20

 region num=3 Si3N4 \
       P1.X=2.21     P1.Y=0.20   \
       P2.X=2.24     P2.Y=0.20   \
       P3.X=2.24     P3.Y=0.37   \
       P4.X=2.21     P4.Y=0.37

 region num=3 Si3N4 \
       P1.X=2.175     P1.Y=0.37   \
       P2.X=2.24     P2.Y=0.37   \
       P3.X=2.24     P3.Y=0.40   \
       P4.X=2.175     P4.Y=0.40

 # base poly-Si and poly-SiGe left

 region num=7 POLYSILICON \
       P1.X=1.90     P1.Y=0.23   \
       P2.X=1.935     P2.Y=0.23   \
       P3.X=1.935     P3.Y=0.25   \
       P4.X=1.90     P4.Y=0.25

 region num=7 POLYSILICON \
       P1.X=1.91     P1.Y=0.25   \
       P2.X=1.935     P2.Y=0.25   \
       P3.X=1.935     P3.Y=0.425   \
       P4.X=1.91     P4.Y=0.45

 region num=7 POLYSILICON \
       P1.X=1.89     P1.Y=0.45   \
       P2.X=1.91     P2.Y=0.45   \
       P3.X=1.905     P3.Y=0.455   \
       P4.X=1.885     P4.Y=0.455

 region num=5 POLYSILICON \
       P1.X=1.65     P1.Y=0.25   \
       P2.X=1.91     P2.Y=0.25   \
       P3.X=1.91     P3.Y=0.45   \
       P4.X=1.65     P4.Y=0.45

 region num=5 POLYSILICON \
       P1.X=0.00     P1.Y=0.00    \
       P2.X=1.40     P2.Y=0.00    \
       P3.X=1.40     P3.Y=0.20   \
       P4.X=0.00     P4.Y=0.20

 region num=5 POLYSILICON \
       P1.X=1.40     P1.Y=0.00    \
       P2.X=1.65     P2.Y=0.25    \
       P3.X=1.65     P3.Y=0.45    \
       P4.X=1.40     P4.Y=0.20
```

```
# base poly-Si and poly-SiGe right

region num=7 POLYSILICON \
      P1.X=2.265    P1.Y=0.23  \
      P2.X=2.3    P2.Y=0.23  \
      P3.X=2.3    P3.Y=0.25  \
      P4.X=2.265    P4.Y=0.25

region num=7 POLYSILICON \
      P1.X=2.265    P1.Y=0.25  \
      P2.X=2.29    P2.Y=0.25  \
      P3.X=2.29    P3.Y=0.45  \
      P4.X=2.265    P4.Y=0.425

region num=7 POLYSILICON \
      P1.X=2.29    P1.Y=0.45  \
      P2.X=2.31    P2.Y=0.45  \
      P3.X=2.315    P3.Y=0.455  \
      P4.X=2.295    P4.Y=0.455

region num=5 POLYSILICON \
      P1.X=2.29    P1.Y=0.25  \
      P2.X=2.55    P2.Y=0.25  \
      P3.X=2.55    P3.Y=0.45  \
      P4.X=2.29    P4.Y=0.45

region num=5 POLYSILICON \
      P1.X=2.55    P1.Y=0.25  \
      P2.X=2.80    P2.Y=0.00  \
      P3.X=2.80    P3.Y=0.20  \
      P4.X=2.55    P4.Y=0.45

region num=5 POLYSILICON \
      P1.X=2.80    P1.Y=0.00  \
      P2.X=2.95    P2.Y=0.00  \
      P3.X=2.95    P3.Y=0.20  \
      P4.X=2.80    P4.Y=0.20

# emitter poly-Si centre

region num=4 POLYSILICON \
      P1.X=2.00    P1.Y=0.40  \
      P2.X=2.20    P2.Y=0.40  \
      P3.X=2.20    P3.Y=0.425  \
      P4.X=2.00    P4.Y=0.425

region num=4 POLYSILICON \
      P1.X=2.025    P1.Y=0.37  \
      P2.X=2.175    P2.Y=0.37  \
      P3.X=2.175    P3.Y=0.40  \
      P4.X=2.025    P4.Y=0.40

region num=4 POLYSILICON \
      P1.X=1.99    P1.Y=0.25  \
      P2.X=2.21    P2.Y=0.25  \
      P3.X=2.21    P3.Y=0.37  \
      P4.X=1.99    P4.Y=0.37
```

```
# SiGe layers

region num=6 material=SiGe  \
      P1.X=1.87     P1.Y=0.49    \
      P2.X=1.89     P2.Y=0.47    \
      P3.X=2.31     P3.Y=0.47    \
      P4.X=2.33     P4.Y=0.49    \
      x.compose=0.15  \
      GRAD.12=0.00 GRAD.23=0.03 \
      GRAD.34=0.00 GRAD.41=0.00

region num=6 material=SiGe  \
      P1.X=1.85     P1.Y=0.49    \
      P2.X=1.885     P2.Y=0.455    \
      P3.X=1.905     P3.Y=0.455    \
      P4.X=1.87     P4.Y=0.49    \
      x.compose=0.15  \
      GRAD.12=0.00 GRAD.23=0.00 \
      GRAD.34=0.00 GRAD.41=0.00

region num=6 material=SiGe  \
      P1.X=2.33     P1.Y=0.49    \
      P2.X=2.295     P2.Y=0.455    \
      P3.X=2.315     P3.Y=0.455    \
      P4.X=2.35     P4.Y=0.49    \
      x.compose=0.15  \
      GRAD.12=0.00 GRAD.23=0.00 \
      GRAD.34=0.00 GRAD.41=0.00


# left-side trench and other oxide layers

region num=2 oxide \
      P1.X=0.00    P1.Y=0.49  \
      P2.X=1.30    P2.Y=0.49  \
      P3.X=1.30    P3.Y=1.54  \
      P4.X=0.00    P4.Y=1.54

region num=2 oxide \
      P1.X=0.00    P1.Y=0.20  \
      P2.X=1.40    P2.Y=0.20  \
      P3.X=1.65    P3.Y=0.45  \
      P4.X=0.00    P4.Y=0.45

region num=2 oxide \
      P1.X=1.45    P1.Y=0.05  \
      P2.X=1.90    P2.Y=0.05  \
      P3.X=1.90    P3.Y=0.25  \
      P4.X=1.65    P4.Y=0.25

region num=2 oxide \
      P1.X=1.40    P1.Y=0.00  \
      P2.X=1.955    P2.Y=0.00  \
      P3.X=1.955    P3.Y=0.05  \
      P4.X=1.45    P4.Y=0.05

# right-side trench and other oxide layers

region num=2 oxide \
      P1.X=4.20    P1.Y=0.49  \
```

```
       P2.X=4.30     P2.Y=0.49  \
       P3.X=4.30     P3.Y=1.54  \
       P4.X=4.20     P4.Y=1.54

region num=2 oxide \
       P1.X=2.245     P1.Y=0.05  \
       P2.X=2.245     P2.Y=0.00  \
       P3.X=2.80     P3.Y=0.00  \
       P4.X=2.75     P4.Y=0.05

region num=2 oxide \
       P1.X=2.30     P1.Y=0.05  \
       P2.X=2.75     P2.Y=0.05  \
       P3.X=2.55     P3.Y=0.25  \
       P4.X=2.30     P4.Y=0.25

region num=2 oxide \
       P1.X=2.95     P1.Y=0.00  \
       P2.X=3.4     P2.Y=0.00  \
       P3.X=3.4     P3.Y=0.15  \
       P4.X=2.95     P4.Y=0.15

region num=2 oxide \
       P1.X=2.95     P1.Y=0.15  \
       P2.X=3.4     P2.Y=0.15  \
       P3.X=3.4     P3.Y=0.20  \
       P4.X=2.95     P4.Y=0.20

region num=2 oxide \
       P1.X=2.8     P1.Y=0.20  \
       P2.X=3.4     P2.Y=0.20  \
       P3.X=3.4     P3.Y=0.45  \
       P4.X=2.55     P4.Y=0.45

region num=2 oxide \
       P1.X=3.95     P1.Y=0.00  \
       P2.X=4.30     P2.Y=0.00  \
       P3.X=4.30     P3.Y=0.15  \
       P4.X=3.95     P4.Y=0.15

region num=2 oxide \
       P1.X=3.95     P1.Y=0.15  \
       P2.X=4.30     P2.Y=0.15  \
       P3.X=4.30     P3.Y=0.45  \
       P4.X=3.95     P4.Y=0.45


electrode num=1 name=emitter \
       x.min=1.955 x.max=2.245 y.min=0.00 y.max=0.17
electrode num=1 name=emitter \
       x.min=1.99 x.max=2.21 y.min=0.17 y.max=0.25

electrode num=2 name=collector \
       x.min=3.40 x.max=3.95 y.min=0.00 y.max=0.49

electrode num=3 name=base \
       x.min=0.00 x.max=0.50 y.min=0.00 y.max=0.00

# basic substrate doping
doping uniform conc=1.0e12 p.type \
```

```
      x.min=1.20 x.max=4.30 y.min=0.00 y.max=1.54

# n+ collector buried layer
doping uniform conc=5.0e19 n.type \
       region=11
doping uniform conc=5.0e19 n.type \
       x.min=3.40 x.max=3.95 y.min=0.49 y.max=0.99
doping gauss conc=5.0e19 char=0.038 n.type \
       x.min=1.30 x.max=4.20 y.min=0.99 y.max=1.54

# n- collector layer
doping gauss conc=6.0e16 char=0.088 n.type peak=0.72 \
      region=10

doping uniform conc=1.0e14 n.type  \
       x.min=1.30 x.max=4.20 y.min=0.49 y.max=0.99

# emitter and collector poly-Si
doping uniform conc=1.0e20 n.type \
      region=4

# emitter Silicon layer
doping gauss conc=1.0e20 char=0.007 n.type \
      peak=0.425 region=9
doping uniform conc=1.0e14 n.type \
      region=8

# base SiGe
doping gauss conc=5.0e18 char=0.0145 p.type \
      peak=0.460 region=6

# base poly-Si
doping uniform conc=5.0e19 p.type \
      region=5

# base poly-SiGe
doping uniform conc=5.0e19 p.type \
      region=7

models bipolar bgn print

# material taun0=1.0e-05 taup0=1.0e-05 region=8
# material taun0=1.0e-05 taup0=1.0e-05 region=9
# material taun0=1.0e-05 taup0=1.0e-05 region=6

method  newton autonr trap

symbolic newton carriers=2

solve init

save outf=vsige_kon_init_red_1a.str

method  newton autonr trap

symbolic newton carriers=2

solve vemitter=0.0 vbase=0.0 \
     vcollector=0.0 vstep=0.1 vfinal=0.9 name=collector
log outf=vsige_kon_gum_red_1a.log
```

```
solve vemitter=0.0 vcollector=1.0 \
      vbase=0.0 vstep=0.02 vfinal=0.7 electrode=3
save outf=tmp_red_1a.str
log outf=vsige_kon_gum_red_1a.log append
solve vemitter=0.0 vcollector=1.0 \
      vbase=0.72 vstep=0.02 vfinal=0.78 electrode=3
solve vemitter=0.0 vcollector=1.0 \
      vbase=0.79 vstep=0.005 vfinal=0.83 electrode=3
solve vemitter=0.0 vcollector=1.0 \
      vbase=0.84 vstep=0.02 vfinal=1.00 electrode=3

load master infile=tmp_red_1a.str
log outf=vsige_red_ac_b0p7_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.7 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p72_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.72 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p74_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.74 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p76_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.76 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p78_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.78 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p79_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.79 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p795_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.795 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p8_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.8 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p805_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.805 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p81_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.81 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p815_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.815 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p82_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.82 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
```

```
log outf=vsige_red_ac_b0p825_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.825 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p83_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.83 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p84_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.84 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p86_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.86 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p88_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.88 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p9_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.9 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p92_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.92 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p94_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.94 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p96_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.96 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b0p98_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=0.98 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=vsige_red_ac_b1p0_1a.log
solve vemitter=0.0 vcollector=1.0 vbase=1.0 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
quit
```

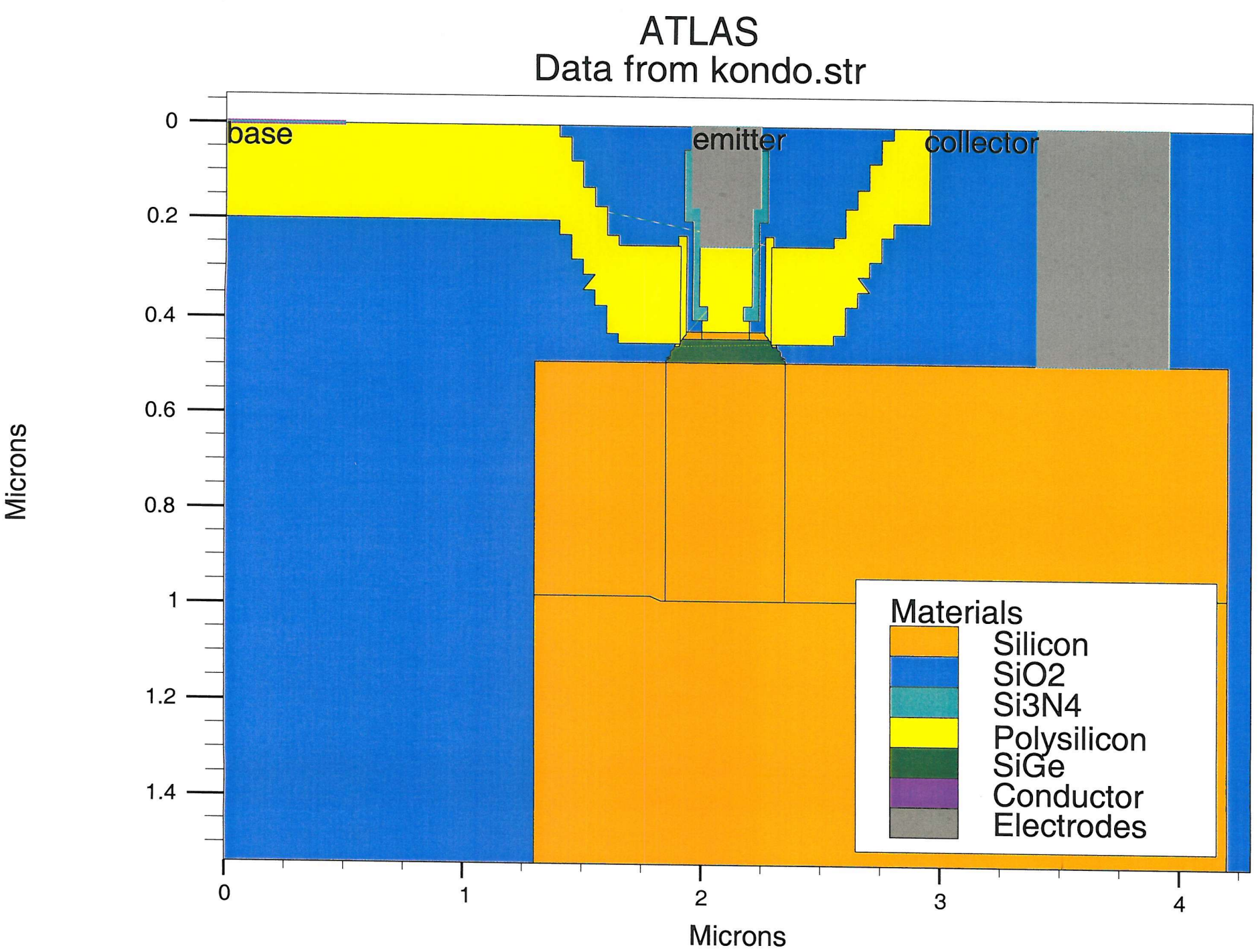

Figure D.1: The Kondo device structure generated by input file.

Lateral device input file

```
go atlas

# proposed lateral bjt, doping profile after Kondo device
# SiGe/Si base layer, 15% graded Ge

mesh  width=1.7
x.m l=0.0  spacing=0.05
x.m l=0.2  spacing=0.01
x.m l=0.625 spacing=0.01
x.m l=0.675 spacing=0.005
x.m l=0.725 spacing=0.005
x.m l=0.775 spacing=0.01
x.m l=0.825 spacing=0.01
x.m l=0.975 spacing=0.01
x.m l=1.175 spacing=0.05

y.m l=0.0  spacing=0.005
y.m l=0.025  spacing=0.005
y.m l=0.05 spacing=0.005
y.m l=0.075 spacing=0.005
y.m l=0.1  spacing=0.01
y.m l=0.2  spacing=0.01
y.m l=1.2  spacing=0.4
y.m l=2.2  spacing=0.6

# eliminate y-nodes

eliminate y.direction x.min=0.0 x.max=1.175 y.min=0.4 y.max=2.1
eliminate y.direction x.min=0.0 x.max=1.175 y.min=0.4 y.max=2.1

eliminate y.direction x.min=0.21 x.max=0.665 y.min=0.01 y.max=0.09
eliminate y.direction x.min=0.21 x.max=0.665 y.min=0.01 y.max=0.09
eliminate y.direction x.min=0.21 x.max=0.665 y.min=0.01 y.max=0.09
eliminate y.direction x.min=0.735 x.max=0.955 y.min=0.01 y.max=0.09
eliminate y.direction x.min=0.735 x.max=0.955 y.min=0.01 y.max=0.09

# substrate region
region num=1 silicon \
       x.min=0.0 x.max=1.175 y.min=1.2 y.max=2.2

# collector region, region=4
region num=4 silicon \
       x.min=0.0 x.max=0.675 y.min=0.1 y.max=0.2

# emitter region, region=5
region num=5 silicon \
       x.min=0.725 x.max=1.175 y.min=0.1 y.max=0.2

region num=2 oxide \
       x.min=0.2 x.max=0.675 y.min=0.0 y.max=0.1
region num=2 oxide \
       x.min=0.725 x.max=0.975 y.min=0.0 y.max=0.1
region num=2 oxide \
       x.min=0.0 x.max=1.175 y.min=0.2 y.max=1.2

region num=3 material=SiGe \
      P1.X=0.675     P1.Y=0.2    \
```

```
       P2.X=0.675      P2.Y=0.075    \
       P3.X=0.695      P3.Y=0.075    \
       P4.X=0.695      P4.Y=0.2    \
       x.compose=0.15  \
       GRAD.12=0.00 GRAD.23=0.00 \
       GRAD.34=0.03 GRAD.41=0.00

region num=3 material=SiGe \
       P1.X=0.675      P1.Y=0.075  \
       P2.X=0.675      P2.Y=0.000    \
       P3.X=0.725      P3.Y=0.000    \
       P4.X=0.725      P4.Y=0.075    \
       x.compose=0.15  \
       GRAD.12=0.00 GRAD.23=0.00 \
       GRAD.34=0.00 GRAD.41=0.00


electrode num=1 name=emitter \
       x.min=0.975 x.max=1.175 y.min=0.0 y.max=0.1
electrode num=2 name=collector \
       x.min=0.0 x.max=0.2 y.min=0.0 y.max=0.1
electrode num=3 name=base \
       x.min=0.575 x.max=0.775 y.min=0.0 y.max=0.0
electrode num=4 name=substrate \
       x.min=0.0 x.max=1.175 y.min=2.2 y.max=2.2

# substrate
doping uniform conc=1.0e15 p.type \
       x.min=0.0 x.max=1.175 y.min=1.2 y.max=2.2

# base contact
doping gauss conc=5e19 char=0.008 p.type \
       x.min=0.675 x.max=0.725 y.min=0.00 y.max=0.075

# active SiGe base
doping  gauss conc=5.0e18 char=0.0145 lat.char=0.0145 p.type \
      x.min=0.705 x.max=0.705 y.min=0.1 y.max=0.2 region=3

# n+ collector
doping gauss conc=5.0e19 char=0.038 lat.char=0.038 n.type \
       x.min=0.0 x.max=0.2 y.min=0.1 y.max=0.2

# n- collector
doping gauss conc=6.0e16 char=0.088 lat.char=0.088 n.type \
       x.min=0.470 x.max=0.470 y.min=0.1 y.max=0.2 region=4

# n- emitter
doping gauss conc=1.0e20 char=0.007 lat.char=0.007 n.type \
       x.min=0.740 x.max=1.175 y.min=0.1 y.max=0.2 region=5


models bipolar bgn print

method  newton autonr trap

symbolic newton carriers=2

solve init

save outf=kon_lat_init_5a.str
```

```
method  newton autonr trap

symbolic newton carriers=2

solve vemitter=0.0 vbase=0.0 v4=0.0  \
      vcollector=0.0 vstep=0.1 vfinal=0.9 name=collector
log outf=kon_lat_gum_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  \
      vbase=0.0 vstep=0.02 vfinal=0.7 name=base
save outf=kon_lat_tmp_5a.str
log outf=kon_lat_gum_5a.log append
solve vemitter=0.0 vcollector=1.0 v4=0.0  \
      vbase=0.72 vstep=0.02 vfinal=0.78 name=base
log outf=kon_lat_gum_5a.log append
solve vemitter=0.0 vcollector=1.0 v4=0.0  \
      vbase=0.79 vstep=0.005 vfinal=0.83 name=base
log outf=kon_lat_gum_5a.log append
solve vemitter=0.0 vcollector=1.0 v4=0.0  \
      vbase=0.84 vstep=0.02 vfinal=1.00 name=base

load master infile=kon_lat_tmp_5a.str
log outf=kon_lat_ac_b0p7_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.7 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p72_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.72 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p74_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.74 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p76_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.76 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p78_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.78 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p79_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.79 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p795_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.795 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p80_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.80 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p805_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.805 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p81_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.81 \
```

```
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p815_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.815 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p82_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.82 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p825_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.825 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p83_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.83 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p84_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.84 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p86_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.86 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p88_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.88 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p9_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.9 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p92_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.92 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p94_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.94 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p96_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.96 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b0p98_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=0.98 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
log outf=kon_lat_ac_b1p0_5a.log
solve vemitter=0.0 vcollector=1.0 v4=0.0  vbase=1.0 \
      ac freq=1.0e07 fstep=1.258925412 mult.f nfstep=50 \
      vss=0.01 term=32
quit
```

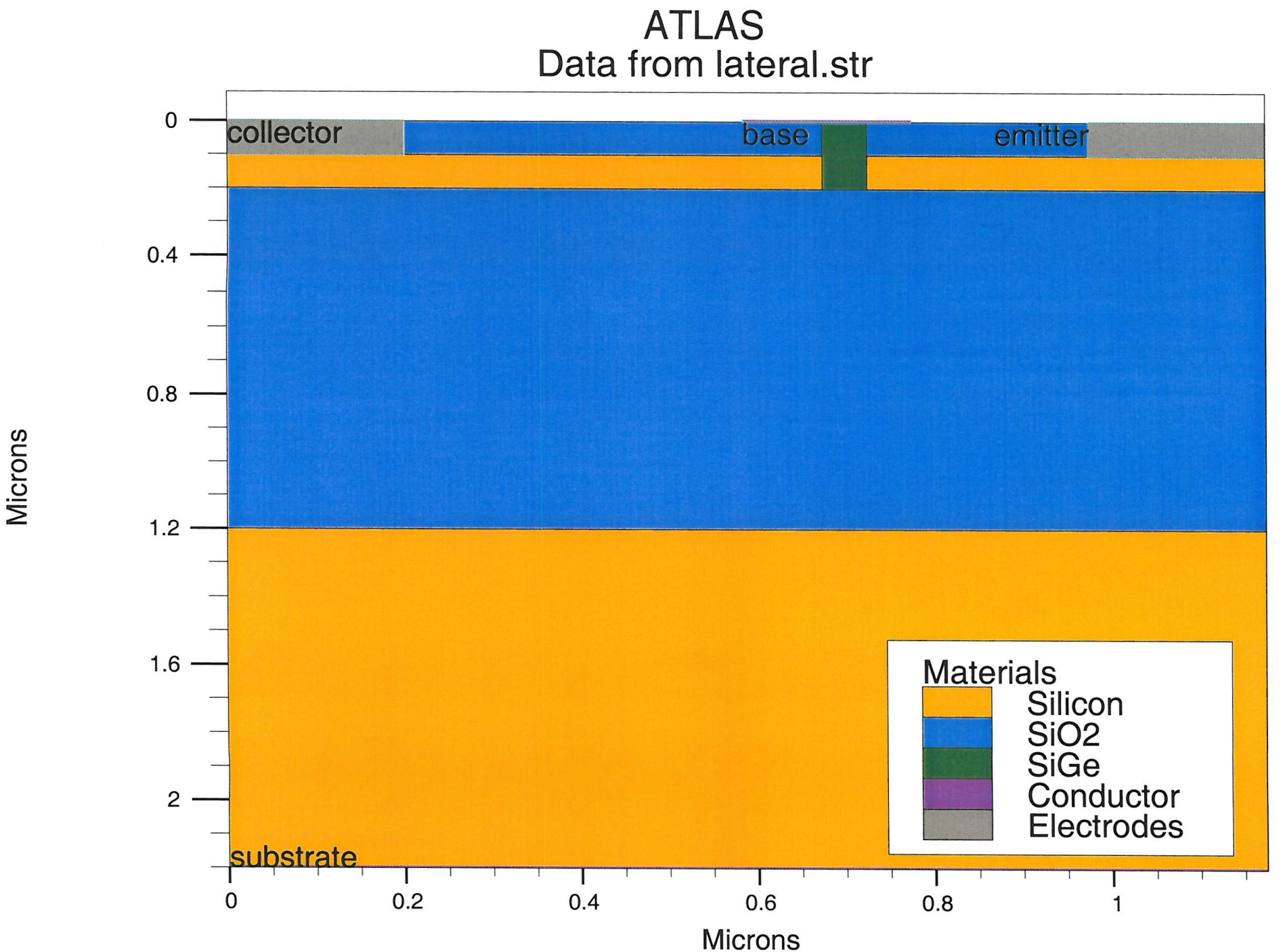

Figure D.2: The proposed lateral device structure generated by input file.

Appendix E

Base resistance and Collector/Base depletion capacitance extraction using Z parameters.

The following are derivations of device z-parameters theory obtained from Lee *et al.* [102]. The small signal hybrid-π equivalent circuit bipolar transistor is shown in Figure E.1.

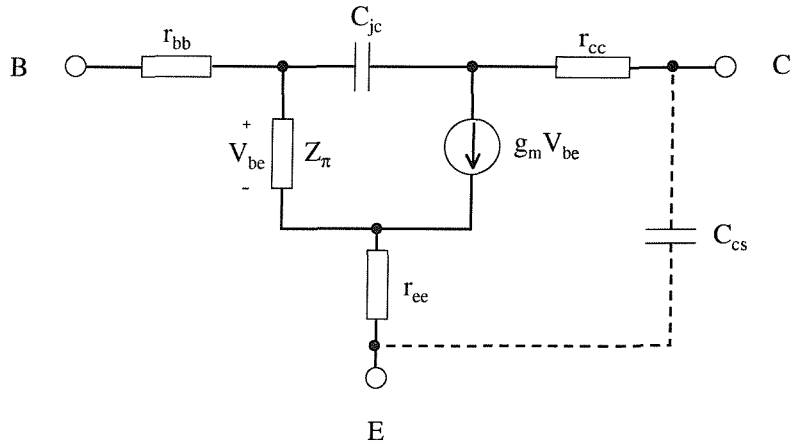

Figure E.1: Small signal hybrid-π model representation of bipolar transistor.

where Z_π is the effective impedence of C_π parallel to r_π. r_{bb} is the base resistance, r_{cc} is the collector resistance, r_{ee} is the emitter resistance, C_{jc} is the base-collector junction capacitance, g_m is the transconductance, C_{cs} is the collector-substrate capacitance, C_π is the sum of the emitter-base depletion capacitance and the emitter

diffusion capacitance, r_π is the input resistance representing the linearized emitter-base diode and V_{be} is the voltage across r_π. Note that C_{cs} is neglected from the extraction.

Taking the Z-parameter of the hybrid-π bipolar transistor [102], for Z_{11};

$$Z_{11} = \left.\frac{V_b}{I_b}\right|_{I_c=0} \tag{E.1}$$

as shown in Figure E.2.

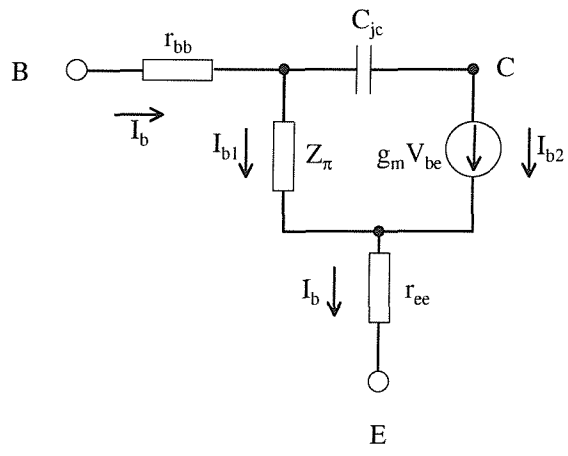

Figure E.2: Bipolar transistor's hybrid-π equivalent model for zero collector current (i.e. $I_c = 0V$)

$$\begin{aligned} I_{b2} &= g_m V_{be} \\ &= g_m (I_{b1} Z_\pi) \\ \text{Therefore,} \qquad I_{b1} &= \frac{I_{b2}}{g_m Z_\pi} \end{aligned} \tag{E.2}$$

$$\begin{aligned} I_b &= I_{b1} + I_{b2} \\ &= I_{b1} + I_{b1} g_m Z_\pi \\ \text{Therefore,} \qquad I_{b1} &= \frac{I_b}{g_m Z_\pi + 1} \end{aligned} \tag{E.3}$$

$$\begin{aligned} V_b &= I_b r_{bb} + I_{b1} Z_\pi + I_b r_{ee} \\ &= I_b \left(r_{bb} + r_{ee} + \frac{Z_\pi}{g_m Z_\pi + 1} \right) \end{aligned} \tag{E.4}$$

$$\text{Therefore,} \qquad Z_{11} = \left(r_{bb} + r_{ee} + \frac{Z_\pi}{g_m Z_\pi + 1} \right) \tag{E.5}$$

For extracting Z_{21};

$$Z_{21} = \left.\frac{V_c}{I_b}\right|_{I_c=0} \tag{E.6}$$

as shown in Figure E.2. From Equation E.2 and Equation E.3,

$$\begin{aligned} I_{b2} &= I_{b1} g_m Z_\pi \\ &= I_b \frac{g_m Z_\pi}{g_m Z_\pi + 1} \end{aligned} \tag{E.7}$$

$$V_c = V_b - I_b r_{bb} + \frac{I_{b2}}{j\omega C_{jc}} \tag{E.8}$$

Substituting Equation E.4 and E.7 into Equation E.8

$$V_c = I_b r_{bb} + I_b r_{ee} + I_b \frac{Z_\pi}{g_m Z_\pi + 1} - I_b r_{bb} + \left(\frac{1}{j\omega C_{jc}}\right)\left(\frac{g_m Z_\pi}{g_m Z_\pi + 1}\right) I_b$$

$$\text{Therefore,} \qquad Z_{21} = r_{ee} + \frac{Z_\pi}{g_m Z_\pi + 1}\left(1 - \frac{g_m}{j\omega C_{jc}}\right) \tag{E.9}$$

For extracting Z_{12};

$$Z_{12} = \left.\frac{V_b}{I_c}\right|_{I_b=0} \tag{E.10}$$

as shown in Figure E.3.

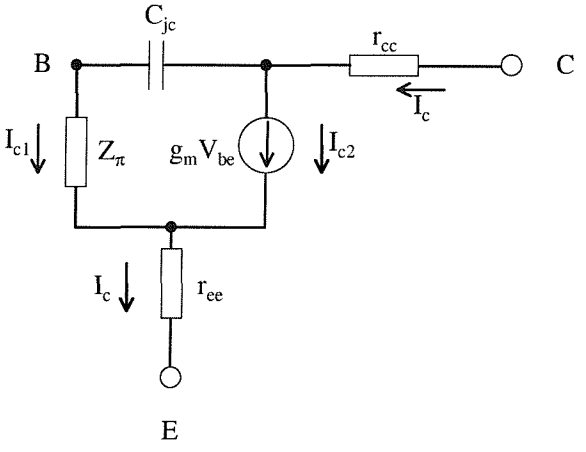

Figure E.3: Bipolar transistor's hybrid-π equivalent model for zero base current (i.e. $I_b = 0V$)

$$\begin{aligned} I_{c2} &= g_m V_{be} \\ &= g_m (I_{c1} Z_\pi) \end{aligned} \tag{E.11}$$

Using Equation E.11,

$$\begin{aligned} I_c &= I_{c1} + I_{c2} \\ &= I_{c1} + g_m Z_\pi I_{c1} \end{aligned}$$

$$\text{Therefore,} \qquad I_{c1} = \frac{I_c}{1 + g_m Z_\pi} \tag{E.12}$$

Using Equation E.12,

$$\begin{aligned} V_b &= I_{c1} Z_\pi + I_c r_{ee} \\ &= \frac{I_c Z_\pi}{1 + g_m Z_\pi} + I_c r_{ee} \end{aligned}$$

$$\text{Therefore,} \qquad Z_{12} = r_{ee} + \frac{Z_\pi}{1 + g_m Z_\pi} \tag{E.13}$$

For extracting Z_{22};

$$Z_{22} = \left.\frac{V_c}{I_c}\right|_{I_b=0} \tag{E.14}$$

as shown in Figure E.3.

$$V_c = I_c r_{cc} + I_{c1}\left(Z_\pi + \frac{1}{j\omega C_{jc}}\right) + I_c r_{ee} \tag{E.15}$$

Using Equation E.12,

$$V_c = I_c r_{cc} + I_c \left(\frac{1}{1 + g_m Z_\pi}\right)\left(Z_\pi + \frac{1}{j\omega C_{jc}}\right) + I_c r_{ee}$$

$$\text{Therefore,} \qquad Z_{22} = r_{cc} + r_{ee} + \left(\frac{1}{1 + g_m Z_\pi}\right)\left(Z_\pi + \frac{1}{j\omega C_{jc}}\right) \tag{E.16}$$

$$\begin{aligned} Z_{22} &= r_{cc} + r_{ee} + \left(\frac{1}{1 + g_m Z_\pi}\right)\left(Z_\pi + \frac{1}{j\omega C_{jc}}\right) \\ &= r_{cc} + r_{ee} + \frac{1 + j\omega C_{jc} Z_\pi}{j\omega C_{jc}(1 + g_m Z_\pi)} \\ &= r_{cc} + r_{ee} + \frac{1}{j\omega C_{jc}(1 + g_m Z_\pi)} + \frac{Z_\pi}{1 + g_m Z_\pi} \\ &= r_{cc} + r_{ee} + \frac{Z_\pi}{1 + g_m Z_\pi} + \frac{(1 + g_m Z_\pi) - g_m Z_\pi}{j\omega C_{jc}(1 + g_m Z_\pi)} \\ &= r_{cc} + r_{ee} + \frac{Z_\pi}{1 + g_m Z_\pi} + \frac{1}{j\omega C_{jc}} - \frac{g_m Z_\pi}{j\omega C_{jc}(1 + g_m Z_\pi)} \\ &= r_{cc} + r_{ee} + \frac{1}{j\omega C_{jc}} + \frac{Z_\pi}{1 + g_m Z_\pi}\left(1 - \frac{g_m}{j\omega C_{jc}}\right) \end{aligned} \tag{E.17}$$

Regrouping the z-parameters together from Equation E.5, E.9, E.13 and E.17;

$$
\begin{aligned}
Z_{11} &= r_{bb} + r_{ee} + \frac{Z_\pi}{g_m Z_\pi + 1} \\
Z_{21} &= r_{ee} + \left(\frac{Z_\pi}{g_m Z_\pi + 1}\right)\left(1 - \frac{g_m}{j\omega C_{jc}}\right) \\
Z_{12} &= r_{ee} + \frac{Z_\pi}{1 + g_m Z_\pi} \\
Z_{22} &= r_{cc} + r_{ee} + \frac{1}{j\omega C_{jc}} + \left(\frac{Z_\pi}{1 + g_m Z_\pi}\right)\left(1 - \frac{g_m}{j\omega C_{jc}}\right)
\end{aligned}
$$

where $Z_\pi = \frac{r_\pi}{1+j\omega r_\pi C_\pi}$. From the Z parameters, we can determine the base resistance and the collector-base capacitance directly as follows:

$$r_{bb} = Re(Z_{11} - Z_{12}) \tag{E.18}$$

$$C_{jc} = -\frac{1}{\omega Im(Z_{22} - Z_{21})} \tag{E.19}$$

Appendix F

List of publications

(1) Y.T. Tang, J.S. Hamel,"An Electrical Method for Measuring Bandgap Grading in SiGe HBT's," 1997 Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications, EDMO, pp. 267-272, 1997.

(2) Y. T. Tang, J.S. Hamel,"An Electrical Method for Measuring The Difference in Bandgap across the Neutral Base in SiGe HBT's," accepted for publication by IEEE Transactions of Electron Device.

(3) Y. T. Tang, J. S. Hamel, "An Experimental Method for Simultaneous Extraction of Parasitic Barrier Heights at Emitter-Base and Collector-Base Junctions of SiGe HBT's," Proc. European Solid-State Device Research Conference, pp. 96-99, 1998.

(4) Y. T. Tang, J. S. Hamel, to be submitted to IEEE Transactions of Electron Devices.

Bibliography

[1] J. Mosely, "Silicon-germanium: the integrated future?" Electronics World And Wireless World, pp.656-658, August, 1994.

[2] A. Schuppen, U. Erben, A. Gruhle, H. Kibbel, H. Schumacher, U. Konig,"Enhanced SiGe heterojunction bipolar transistors with 160 $GHz-f_{max}$," IEDM Tech. Dig., pp. 743-746, 1995.

[3] K. Oda, E. Ohue, M. Tanabe, H. Shimamoto, T. Onai, K. Washio,"130-GHz f_T SiGe HBT Technology," IEDM Tech. Dig., pp. 791-794, 1997.

[4] K. M. Strohm, J. F. Luy, F. Schaffler, H. Jorke, H. Kibbel, C. Rheinfelder, R. Doerner, J. Gerdes, F. J. Schmuckle, W. Heinrich, "Coplanar ka-band SiGe MMIC amplifier," Electronics Letters, vol. 31, pp. 1353-1354, August 1995.

[5] H. U. Schreiber, J. N. Albers, B. G. Bosch, "16Gbit/s multiplexer IC using double mesa Si/SiGe heterojunction bipolar transistors," Electronics Letters, vol. 29, pp. 2185-2187, December 1993.

[6] T. Hashimoto, H. Tezuka, F. Sato, M. Soda, T. Suzaki, T. Tatsumi, T. Tashiro, "SiGe bipolar IC for 20 Gb/s optical transmitter," Bipolar/BiCMOS Circuits and Technology Meeting, pp. 167-170, 1994.

[7] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y. C. Sun, B. S. Meyerson, T. Tice, "Si/SiGe epitaxy-base transistors-Part II: process integration and analogue applications," IEEE Transactions on Electron Devices, Vol. 42, No. 3, pp. 469-482, March 1995.

[8] D. L. Harame, J. H. Comfort, J. D. Cressler, E. F. Crabbe, J. Y. C. Sun, B. S. Meyerson, T. Tice, "Si/SiGe Epitaxy-Base Transistors-Part I: Materials, Physics and Circuits," IEEE Transactions on Electron Devices, Vol. 42, No. 3, pp. 455-467, March 1995.

[9] E. F. Crabbe, J. D. Cressler, G. L. Patton, J. M. C. Stork, J. H. Comfort, J. Y. C. Sun,"113-Ghz fT graded-base SiGe HBT's," IEEE Transactions on Electron Devices, Vol. 40, No. 11, pp. 2100, Nov 1993.

[10] M. Kondo, K. Oda, E. Ohue, H. Shimamoto, M. Tanabe, T. Onai, K. Washio, "Ultra-Low-Power and High-Speed SiGe Base Bipolar Transistors for Wireless Telecommunication Systems," IEEE Transactions on Electron Devices, vol. 45, no. 6, pp. 1287-1294, June 1998.

[11] A. J. Joseph, J. D. Cressler, D. M. Richey, R. C. Jaeger, D. L. Harame, "Neutral Base Recombination and It's Influence on the Temperature Dependence of Early Voltage and Current Gain-Early Voltage Product in UHV/CVD SiGe Heterojunction Bipolar Transistors," IEEE Transaction of Electron Devices, vol. 44, No. 3, pp.404-413, March 1997.

[12] D. Harame, L. Larson, M. Case, S. Kovacic, S. Voinigescu, T. Tewksbury, D. Nguyen-Ngoc, K. Stein, J. Cressler, S. J. Jeng, J. Malinowski, R. Groves, E. Eld, D. Sunderland, D. Rensch, M. Gilbert, K. Schonenberg, D. Ahlgren, S. Rosenbaum, J. Glenn, B. Meyerson "SiGe HBT Technology: Device and application issues," IEDM Tech. Dig., pp. 731-734, 1995.

[13] R. Hueting, J. Slotboom, W. de Boer, C. Timmering, and N. Cowern, "On optimization of SiGe-base bipolar transistors," IEEE Transaction of Electron Devices, vol. 43, pp. 1518-1524, September 1996.

[14] C. A. King, J. L. Hoyt, J. F. Gibbons, "Bandgap and transport properties of $Si/Si_{1-x}Ge_x/Si$ by analysis of nearly ideal $Si/Si_{1-x}Ge_x/Si$ heterojunction bipolar transistors," IEEE Transaction of Electron Devices, vol. 36, pp. 2093-2103, October 1989.

[15] Y.T. Tang, J.S. Hamel,"An Electrical Method for Measuring Bandgap Grading in SiGe HBT's," 1997 Workshop on High Performance Electron Devices for Microwave and Optoelectronic Applications, EDMO, pp. 267-272, 1997.

[16] Y. T. Tang, J.S. Hamel,"An Electrical Method for Measuring The Difference in Bandgap across the Neutral Base in SiGe HBT's," accepted for publication by IEEE Transactions of Electron Device.

[17] A. Pruijmboom, J. W. Slotboom, D. J. Gravesteijn, C. W. Fredriksz, A. A. van Gorkum, R. A. van de Heuvel, J. M. L. van Rooij-Mulder, G. Streutker, G. F. A. van de Walle, " Heterojunction Bipolar Transistors with SiGe Base Grown by Molecular Beam Epitaxy," IEEE Electron Device Letters, Vol. 12, No. 7, pp. 357-359, July 1991.

[18] E. J. Prinz, P. M. Garone, P. V. Schwartz, X. Xiao, James C. Sturm, " The Effects of Base Dopant Outdiffusion and Undoped SiGe Junction Spacer Layers in Si/SiGe/Si Heterojunction Bipolar Transistors," IEEE Electron Device Letters, Vol. 12, No. 2, pp. 42-44, Febuary 1991.

[19] A. Pruijmboom, C. E. Timmering, J. M. L. van Rooij-Mulder, D. J. Gravesteijn, W. B. de Boer, W. J. Kersten, J. W. Slotboom, C. J. Vriezema, R. de Kruif, "Heterojunction bipolar transistors with $Si_{1-x}Ge_x$ base," Proc. European Solid-State Device Research Conference, pp. 427-433, 1992.

[20] J. W. Slotboom, G. Streutker, A. Pruijmboom, D. J. Gravesteijn, " Parasitic Energy Barriers in SiGe HBT's," IEEE Electron Device Letters, Vol. 12, No. 9, pp. 486-488, September 1991.

[21] B. Le Tron, M. D. R. Hashim, P. Ashburn, M. Mouis, A. Chantre, G. Vincent,"Determination of Bandgap Narrowing and Parasitic Energy Barriers in SiGe HBT's Integrated in a Bipolar Technology," IEEE Transactions on Electron Devices, Vol. 44, No. 5, pp. 715-722, May 1997.

[22] Y. T. Tang, J. S. Hamel, "An Experimental Method for Simultaneous Extraction of Parasitic Barrier Heights at Emitter-Base and Collector-Base Junctions of SiGe HBT's," Proc. European Solid-State Device Research Conference, pp. 96-99, 1998.

[23] Y. T. Tang, J. S. Hamel, to be submitted to IEEE Transactions of Electron Devices.

[24] G. L. Patton, J. H. Comfort, B. S. Meyerson, E. F. Crabbe, G. J. Scilla, E. de Fresart, J. M. C. Stork, J. Y. C. Sun, D. L. Harame, J. N. Burghartz, "75 GHz f_T SiGe-base heterojunction bipolar transistor," IEEE Electron Device Letters, vol. 11, pp. 171-173, April 1990.

[25] J. D. Cressler, J. H. Comfort, E. F. Crabbe, G. L. Patton, W. Lee, J. Y. C. Sun, J. M. C. Stork, B. Meyerson "Sub-30ps ECL circuit operation at liquid nitrogen temperature using self-aligned epitaxial SiGe-base bipolar transistors," IEEE Electron Device Letters, vol. 12, pp. 166-169, April 199.

[26] T. F. Meister, H. Schafer, M. Franosch, W. Mozler, K. Aufinger, U. Scheler, C. Walz, M. Stolz, S. Boguth, J. Bock, "SiGe base bipolar technology with 74 GHz f_{max} and 11 ps gate delay," IEDM Tech. Dig., pp. 739-742, 1995.

[27] K. Wasio, E. Ohue, K. Oda, M. Tanabe, H. Shimamoto, T. Onai, "A selective epitaxial SiGe HBT with SMI electrodes featuring 9.3 ps ECL-gate delay," IEDM Tech. Dig., pp. 795-798, 1997.

[28] K. Washio, M. Kondo, E. Ohue, K. Oda, R. Hayami, M. Tanabe, H. Shimamoto, T. Harada, "A 0.2 μm self-aligned SiGe HBT featuring 107 GHz f_{max} and 6.7 ps ECL," IEDM Tech. Dig., December, 1999.

[29] M. Sauter, E. Bertagnolli, E. Knapek, A. Stemmer, B. Froschle, I. Eisele, H. Klose " Application of Electron Beam Lithography for Downscaling of SOI-Bipolar and BiCMOS," Microelectronic Engineering, pp. 31-34, 1996.

[30] N. Akiyama, A. Tamba, Y. Wakui, Y. Kobayashi " CMOS-Compatible Lateral Bipolar Transistor for BiCMOS Technology: Part I - Modeling," IEEE Transactions on Electron Devices, Vol.39, No.4, pp. 948-950, April 1992.

[31] J. C. Sturm, J. P. Mcvittie, J. F. Gibbons, L. Pfeiffer "A Lateral Silicon-On-Insulator Bipolar Transistor with a Self-Aligned Base Contact," IEEE Electron Device Letters, vol. EDL-8, no. 3, March 1987.

[32] W. L. M. Huang, K. M. Klein, M. Grimaldi, M. Racanelli, S. Ramaswami, J. Tsao, J. Foerstner, B. Y. C. Hwang, "TFSOI complementary BiCMOS technology for low power applications," IEEE Transactions of Electron Devices, vol. 42, No. 3, pp.506-512, March 1995.

[33] S. Verdonckt-Vandebroek, J. C. S. Woo, P. K. Ko, S. S. Wong " High-Gain Lateral Bipolar Action in a MOSFET Structure," IEEE Transactions on Electron Devices, Vol.38, No.11, pp. 2487-2495, November 1991.

[34] *Atlas User's Manual, Device Simulation Software, Version 4.0*, Silvaco International, Inc., June, 1995.

[35] W. Shockley, "U.S. Patent 2569347," September 1951.

[36] E. Kasper, H. J. Herzog, "Elastic strain and misfit dislocation density in $Si_{0.92}Ge_{0.08}$ films on silicon substrates," Thin Solid Films, vol. 44, pp. 357-370, 1977.

[37] E. Kasper, H. J. Herzog, H. Kibble, "A one-dimensional SiGe superlattice grown by UHV epitaxy," App. Phys., vol. 8, pp. 199-205, 1975.

[38] S. S. Iyer, G. L. Patton, J. M. C. Stork, B. S. Meyerson, D. L. Harame, "Heterojunction Bipolar Transistors Using Si-Ge Alloys," IEEE Transactions on Electron Devices, Vol. 36, No. 10, pp. 2043-2064, October, 1989.

[39] A. Gruhle, H. Kibbel, U. Konig, U. Erben, E. Kasper, "MBE-Grown Si/SiGe HBT's with high β, f_T and f_{max}," IEEE Electron Device Letters, vol. 13, no. 4, pp. 206-208, April, 1992.

[40] R. Hull, J. C. Bean, D. J. Eaglesham, J. M. Bonar, C. Buescher, Thin Solid Films, vol. 183, pp.117, 1989.

[41] M. Green, B. Weir, D. Brasen, Y. Hsieh, G. Higashi, A. Feygenson, L. Feldman, R. Headrick, "Mechanically and thermally stable Si-Ge films and heterojunction bipolar transistors grown by rapid thermal chemical vapour deposition at 900^0C," Journal of Applied Physics, vol. 69, pp. 745-751, 1991.

[42] R. People, "Physics and Applications of Ge_xSi_{1-x}/Si Strained-Layer Heterostructures," IEEE Journal of Quantum Electronics, Vol. QE-22, No. 9, pp. 1696-1710, September 1986.

[43] R. Braunstein, A. R. Moore, F. Hermann,"Intrinsic optical absorption in germanium-silicon alloys," Phys. Rev., vol. 109, no. 3, pp. 695-710, 1958.

[44] R. People, J. Bean, "Band alignments of coherently strained Ge_xSi_{1-x}/Si heterostructures on ¡001¿ Ge_ySi_{1-y} substrates," Applied Physics Letters, vol. 48, pp. 538-540, 1986.

[45] J. Poortmans, S. C. Jain, D. H. J. Totterdell, M. Caymax, J. F. Nijs, R. P. Mertens, R. V. Overstraeten, "Theoretical calculation and experimental evidence of the real and apparent bandgap narrowing due to heavy doping in p-type Si and strained $Si_{1-x}Ge_x$ layers," Solid State Electronics, vol. 36, no. 12, pp. 1763-1771, December, 1993.

[46] P. Ashburn, *Design and Realization of Bipolar transistors*, Chichester, John Wiley & Sons, 1988.

[47] D. L. Harame, E. F. Crabbe, J. D. Cressler, J. H. Comfort, J. Y. C. Sun, S. R. Stiffer, E. Kobeda, J. N. Burghartz, M. M. Gilbert, J. C. Malinowski, A. J. Dally, "A high performance epitaxy SiGe-Base ECL BiCMOS technology," IEDM Tech. Dig., pp. 19-22, December, 1992.

[48] B. S. Meyerson, "Low temperature silicon epitaxy by ultra-high vacuum/chemical vapour deposition," Applied Physics Letters, vol. 48, no. 12, pp. 797-799, 1986.

[49] G. S. Higashi, Y. J. Chabal, G. W. Trucks, K. Raghavachari, "Ideal hydrogen termination of the Si(111) surface," Applied Physics Letters, vol.56, no. 7, pp. 656-658, 1990.

[50] B. S. Meyerson, K. E. Ismail, D. L. Harame, F. K. LeGoues, J. M. C. Stork, "UHV/CVD growth of Si/SiGe heterostructures and their implications," Semiconductor Science and Technology, vol. 9, pp. 2005-2019, 1994.

[51] B. S. Meyerson, " High-Speed Silicon-Germanium Electronics," Scientific American, pp.42-47, March, 1994.

[52] R. Kircher, M. Furuno, J. Murota, S. Ono, "Low-temperature epitaxy and in-situ doping of silicon films," Journal De Physique IV, vol. 1, pp. C2:787-C2:794, 1991. Colloque C2.

[53] H. Kroemer, "Two integral relations pertaining to the electron transport through a bipolar transistor with a nonuniform energy gap in the base region," Solid-State Electronics, vol. 28, pp. 1101-1103, November 1985.

[54] L. E. Kay, T. W. Tang, "Monte Carlo calculation of strained and unstrained electron mobilities in SiGe using an improved ionized impurity model," J. Appl. Phys., vol. 70, no. 3, pp. 1483-1488, 1991.

[55] J. Lindmayer, C, Wrigley, "The high injection level operation of drift transistors," Solid State Electronics, vol. 2, pp. 79, 1991

[56] *TMA MEDICI Two-Dimensional Device Simulation Program, Version 2.2*, Technology Modeling Associates, Inc., 1997.

[57] E. Prinz, P. Garone, P. Schwartz, X. Xiao, J. Sturm, "The effect of base-emitter spacers and strain-dependent densities of states in $Si/Si_{1-x}Ge_x$ heterojunction bipolar transistors," IEDM Tech. Dig., pp. 639-642, 1989.

[58] J. W. Slotboom, "The pn product in silicon," Solid-State Electronics, 20, pp.279-283, 1977.

[59] C. D. Thurmond, "The Standard Thermodynamic Function of the Formation of Electrons and Holes in Ge, Si, GaAs, and GaP", J. Electrochem. Soc., 122, 1133, 1975.

[60] D. B. M. Klaassen, "A unified mobility model for device simulation - I. Model equations and concentration dependence," Solid-State Electronics, Vol. 35, No. 7, pp. 953-959, 1992.

[61] D. B. M. Klaassen, "A unified mobility model for device simulation - II. Temperature dependence of carrier mobility and lifetime," Solid-State Electronics, Vol. 35, No. 7, pp. 961-967, 1992.

[62] D. Roulston, N. Arora, S. Chamberlain, "Modeling and measurement of minority-carrier lifetime versus doping in diffused layers of n^+p silicon diodes," IEEE Transactions on Electron Devices, vol. 29, pp. 284-291, Febuary 1982.

[63] S. M. Sze *Physics of Semiconductor Devices*, John Wiley & Sons, Inter-Sciences Publication, 1981.

[64] Z. A. Shafi, P. Ashburn, I. R. C. Post, D. J. Robbins, W. Y. Leong, C. J. Gibbings, S. Nigrin, " Analysis and Modeling of the Base Current of Si/SiGe Heterojunction Bipolar Transistors Fabricated in High and Low Oxygen Content Material," J. Appl. Phys. vol. 78, pp. 2823-2829, Aug 1995.

[65] M. A. Green, "Intrinsic concentration, effective density of states, and effective mass in silicon," Jpn. J. Appl. Phys., vol. 67, pp. 2944, 1990.

[66] T. Manku and A. Nathan, "Effective mass for strained p-type $Si_{1-x}Ge_x$," J. Appl. Phys., vol. 69, pp. 8414-8416, 1991.

[67] J. Poortmans, M. Catmax, A. Van Ammel, M. Libezny, K. Werner, S. C. Jain, J. Nijs, R. Merten, "On the electron minority carrier mobility and the effective bandgap in heterojunction bipolar transistors with strained $Si_{1-x}Ge_x$ base," in Proc. Europ. Solid-State Device Ressearch Conf., 1993, pp. 317.

[68] G. W. Taylor and J. G. Simmons, "Figure of merit for integrated bipolar transistors," Solid State Electronics, vol. 29, pp. 941, November, 1986.

[69] D. M. Richey, J. D. Cressler, A. J. Joseph, "Scaling issues and Ge profile optimization in advanced UHV/CVD SiGe HBT's," IEEE Transactions of Electron Devices, vol. 44, No. 3, pp.431-440, March 1997.

[70] J. A. Kerr, F. Berz,"The effect of emitter doping gradient in f_T in microwave bipolar transistors," IEEE Trans. Electron. Devices, ED22, pp. 15, 1975.

[71] R. G. Meyer, R. S. Muller, "Charge control analysis of the collector base space-charge region contribution to bipolar transistor time constant," IEEE Trans. Electron. Devices, EN34, pp. 450, 1987.

[72] P. Smith, M. Inoue, J. Frey, "Electron velocity in Si and GaAs at very high electric fields," App. Phy. Lett., vol. 37, pp. 797, 1980.

[73] R. L. Pritchard, Proc. IRE, pp. 1075-1085, September, 1955.

[74] B. Edholm, J. Olsson, A. Soderbarg " A Self-Alligned Lateral Bipolar Transistor Realized on SIMOX-Material," IEEE Transactions on Electron Devices, Vol.40, No.12, pp. 2359-2360, December 1993.

[75] T. Sugii, M. Kojima, A. Fukuroda, T. Fukano, Y. Arimoto " A New SOI-Lateral Bipolar Transistor for High-Speed Operation," Japanese Journal of Applied Physics, Vol.30, No.12B, pp. 2080-2082, December 1991.

[76] G. G. Shahidi, D. D. Tang, B. Davari, Y. Taur, P. Mcfarland, K. Jenkins, D. Danner, M. Rodriguez, A. Megdanis, E. Petrillo, M. Polcari, T. H. Ning " A Novel High-Performance Lateral Bipolar on SOI," IEDM Tech. Dig., pp. 663-666, 1991.

[77] S. Parke, F. Assaderaghi, J. Chen, J. King, C. M. Hu, P. K. Ko,"A versatile SOI BiCMOS technology with complementary lateral BJT's," IEDM Tech. Dig., pp. 453-456, 1992.

[78] J. Olsson, B. Edholm, A. Soderbarg, K. Bohlin, "High current gain hybrid lateral bipolar operation of DMOS transistors," IEEE Transactions on electron devices, vol. 42, no. 9, pp. 1628-1634, September 1995.

[79] S. A. Parke, C. M. Hu, P. K. Ko, " A High-Performance Lateral Bipolar Transistor Fabricated on SIMOX," IEEE Electron Device Letters, Vol.14, No.1, pp. 33-35, January 1993.

[80] D. J. Roulston, J. M. McGregor, "Effect of Bandgap Gradient in the Base Region of SiGe Heterojunction Bipolar Transistors," Solid-State Electronics, Vol. 35, No. 7, pp. 1019-1020, 1992.

[81] E. J. Prinz, J. C. Sturm, "Current Gain-Early Voltage Products in Heterojunction Bipolar Transistors with Nonuniform Base Bandgaps," IEEE Electron Device Letters, Vol.12, No.12, pp.661-663, December 1991.

[82] R. Gotzfried, F. Bebwanger, S. Gerlach, A. Schuppen, H. Dietrich, U. Seiler, K.-H. Bach, and J. Albers, "RFIC's for mobile communication systems using SiGe bipolar technology," IEEE Transactions on Microwave Theory and Techniques, vol. 46, pp. 661-668, May 1998.

[83] J. W. Slotboom, H. de Graaff, " Measurements of bandgap narrowing in Si bipolar transistors," Solid-State Electron, Vol. 19, pp. 857-862, 1976.

[84] T. Manku and A. Nathan, "Energy band structure for strained p-type $Si_{1-x}Ge_x$," Phys. Rev. B, vol. 43, pp. 12634-12637, 1991.

[85] T. Manku and A. Nathan, "Lattice mobility of holes in strained and unstrained $Si_{1-x}Ge_x$ alloys," IEEE Electron Device Letters, vol.12, pp. 704-706, December 1991.

[86] J. Cressler, "SiGe HBT technology: a new contender for Si-based RF and microwave circuit applications," IEEE Transactions on Microwave Theory and Techniques, vol. 46, pp. 572-589, May 1998.

[87] G7 batch process report from the Microelectronic Centre, Department of Electronics and Computer Science, University of Southampton, U.K.

[88] J. S. Hamel, R. J. Alison, R. J. Blaikie, "Experimental Method to Extract AC Collector-Base Resistance from SiGe HBT's," IEEE Transactions on Electron Devices, Vol. 44, No. 11, pp. 1944-1949, November, 1997.

[89] J. S. Hamel, J. Bonar, "Lateral Silicon Germanium Heterojunction Bipolar Transistors," EPSRC Research Grant Proposal GR/M99132, June, 1999.

[90] Z. X. Yan, M. J. Deen, D. S. Malhi " Gate-Controlled Lateral PNP BJT: Characteristics, Modelling and Circuit Applications," IEEE Transactions on Electron Devices, Vol.44, No.1, pp. 118-128, January 1997.

[91] K. K. Au, P. G. Y. Tsui, Y. S. Kim, K. K. Diogu, M. L. Kosty, C. M. Palmer " Field-Plated High Gain Lateral Bipolar Transistor in Standard CMOS Process for BiCMOS Application," IEEE 1991 Custom Integrated Circuits Conference, Ch.159, pp. 477-480, 1991.

[92] S. Lombardo, A. Pinto, V. Raineri, P. Ward, S. U. Campisano, " Si/Ge_xSi_{1-x} HBTs with the Ge_xSi_{1-x} base formed by high dose Ge implantation in Si," IEDM Tech. Dig., pp.1019-1021, 1995.

[93] A. Fukami, K. Shoji, T. Nagano, T. Tokuyama, C. Y. Yang " Graded-bandgap SiGe Bipolar Transistor Fabricated with Germanium Ion Implantation," Microelectronic Engineering, pp.15-18, 1991.

[94] D. J. Eaglesham, H. J. Gossman, M. Cerullo, L. N. Pfieffer, K. N. West, "Limited thickness epitaxy of semiconductors and Si MBE down to room temperature," in IOP Conference Series, vol. 117, pp. 431-434, Institute of Physics, 1991.

[95] A. A. van Gorkum, G. F. A. van de Walle, R. A. van de Heuvel, D. J. Gravesteijn, C. W. Fredriksz, "Performance and processing line integration of a silicon molecular beam epitaxy system," Thin Solid Films, vol.184, pp. 207-219, 1990.

[96] P. J. Schubert, G. W. Neudeck, "Confined Lateral Selective Epitaxy Growth of Silicon for Device Fabrication," IEEE Electron Device Letters, vol. 11, no. 5, pp. 181-183, May 1990.

[97] J. M. Bonar *Process Developement and Characterization of Silicon and Silicon-Germanium Grown in a Novel Single-Wafer LPCVD System.* Ph.D Thesis, University of Southampton, June 1996.

[98] D. M. Caughey, R. E. Thomas, "Carrier mobilities in silicon empirically related to doping and field," proc. IEEE, vol. 55, pp. 2192-2193, 1967.

[99] S. Selberherr, "Process and device modeling for VLSI," Microelectron. Reliab., vol. 24, no. 2, pp. 225-257, 1984.

[100] J. Dziewior, W. Schmid, "Auger coefficients for highly doped and highly excited silicon," App. Phys. Lett., 31, 346, 1977.

[101] A. P. Laser, D. L. Pulfrey, "Reconciliation of methods for estimating f_{max} for microwave heterojunction transistor," IEEE Transactions on Electron Devices, vol. 38, no. 8, pp. 1685-1692, August, 1991.

[102] S. Lee, B. R. Ryum, S. W. Kang, "A New Parameter Extraction Technique for Small-Signal Equivalent Circuit of Polysilicon Emitter Bipolar Transistors," IEEE Transactions of Electron Devices, vol. 41, no.2, pp. 233-238, February 1994.

[103] R. Dekker "Silicon Process Technology Innovations for Low-Power RF Applications," 28th European Solid-State Device Research Conference, pp. 71-80, 1998.

[104] H. K. Gummel, "A Charge Control Relation for Bipolar Transistors," The Bell System Technical Journal, pp. 115-120, January 1970.

[105] S. M. Sze *Semiconductor Devices Physics and Technology*, John Wiley & Sons, 1985.