UNIVERSITY OF SOUTHAMPTON

THE DEVELOPMENT OF CCD PARALLEL TRANSFER STRUCTURES FOR ANALOGUE SIGNAL PROCESSING

by

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CONTENTS

List of Figures

Nomenclature

A	-	Area of an RGR electrode.
A_n	-	Area of nth electrode.
A_s	-	Area over which surface states are filled.
A_V	-	Inverter voltage gain.
$A(f)$	-	Amplitude response of a CCD
a_n	-	Recursive filter feedforward coefficient.
B_n	-	Thick oxide area of the nth electrode.
b_n	-	Recursive filter feedback coefficient.
C_B	-	Storage capacitance associated with sample/hold circuit (F).
C_e	-	Inter-electrode capacitance (F).
C_F	-	Capacitance associated with sample/hold gate (F).
C_g	-	Gate capacitance (F).
C_{ox}	-	Oxide capacitance per unit area ($F.cm^{-2}$).
C_s	-	Stray capacitance (F).
C_w	-	Metering well capacitance per unit area ($F.cm^{-2}$).
D_N	-	Dynamic range of a non-recursive integrator.
f	-	Signal frequency.
f_c	-	Clock frequency.
h_n	-	Transversal filter tap weight.
I_D	-	Drain current.
I_N	-	Integration improvement obtained with a non-recursive integrator.
I_R	-	Integration improvement obtained with a recursive integrator.
K	-	Integer

k	-	Gain of the feedback amplifier.
$\mathcal{k}$	-	Boltzmann's constant (J/K^{O}).
L	-	Electrode length.
M	-	Ratio of stray capacitance to oxide capacitance.
m	-	Number of radar returns to be integrated.
N	-	Number of CCD bits.
N_D	-	Substrate doping density.
N_R	-	The noise output from a recursive integrator.
N_{ss}	-	Surface state density ($cm^{-2}.eV^{-1}$).
n	-	Integer.
$P(x)$	-	Probability distribution.
P	-	Number of CCD phases.
Q_{dep}	-	Depletion charge per unit area ($C.cm^{-2}$).
Q_g	-	Gate charge per unit area ($C.cm^{-2}$).
Q_{in}	-	Charge transferring down RGR (C).
Q_{loss}	-	Charge lost per transfer attributed to a specific type of loss.
Q_s	-	Signal charge per unit area ($C.cm^{-2}$).
Q_T	-	Total charge in a floating-gate assembly (C).
q	-	Electronic charge.
R_a, R_b	-	Diffusion resistance associated with the driver source and load drain.
R_e	-	Inter-electrode resistance.
R_g	-	Gate-to-substrate resistance.
R_N	-	Residual signal in a non-recursive integrator.
R_R	-	Residual signal in a recursive integrator.
S	-	Signal level in a recursive integrator after integrating an infinite number of radar returns.

S_N - Signal output from a non-recursive integrator.

S_R - Signal output from a recursive integrator.

T - Absolute temperature.

T_c - Clock period.

t_F - Transfer time necessary to achieve an ε of 10^{-4}.

t_{ox} - Oxide thickness.

V - Clock voltage amplitude.

V_{DD} - MOST supply voltage.

V_{FB} - Flatband voltage.

V_g - Gate voltage.

$V_g(0)$ - Floating-gate resting potential.

$V_g(Q)$ - Floating-gate potential when storing a charge.

V_{in} - Input signal voltage.

V_o = $qN_D\varepsilon_s/C_{ox}^2$.

V_R - Reset voltage.

V_s - Source bias.

V_{TL}, V_{TD} - Threshold voltage of an MOST load and driver respectively.

W - Electrode width.

x - Instantaneous clutter amplitude.

$\bar{x}$ - Mean clutter amplitude.

x_d - Depletion region width

α - $(1 - \varepsilon)$

β_1, β_2 - Gain of the load and driver of an MOST inverter.

$\Delta P(f)$ - Additional phase shift due to transfer inefficiency (rads).

ΔQ - Total charge lost per transfer.

$\Delta\bar{Q}_s^2$	-	Mean square fluctuations in signal charge.
$\Delta\bar{Q}_{TR}^2$	-	Mean square fluctuations introduced by the transfer process.
ΔV_g	-	Variation in floating-gate potential.
σ	-	r.m.s. amplitude of sea clutter.
ϕ_F	-	Fermi potential.
ϕ_s	-	Surface potential.
ϕ_R	-	Reset waveform.
ϕ_1, ϕ_2, ϕ_3	-	CCD driving phases.

CHAPTER ONE

INTRODUCTION

The charge-coupled device (CCD) was conceived in late 1969 by Boyle and Smith[1,2] of Bell Telephone Laboratories, during an investigation to develop a semiconductor analogue of magnetic bubble devices. The first device consisted of a row of closely spaced MOS capacitors; each electrode was 100 x 100μm and they were separated with 3μm gaps. Minority carriers stored at the silicon/silicon dioxide could be manipulated along the row of capacitors by applying a suitable sequence of voltage pulses to the electrodes. After a series of transfers, the charge 'packet' could be detected by sensing the current produced by injecting the minority carriers into the substrate. Since the fabrication of these devices relied upon well established MOS technology, the simple idea was quickly developed in many laboratories; the size and complexity of the devices grew rapidly until today CCD's digital memories, for example, containing as many as 65K bits are commercially available.

Since 1969, a considerable amount of work has been published on many aspects of the fabrication, operation and performance limitations of CCDs; it is only relatively recently, however, that specific applications for these devices have been discussed in detail. Nevertheless, the great potential for CCDs in very many areas of electronics has been recognised and systems engineers are already beginning to regard CCDs simply as a powerful addition to the circuit functions which are already available.

Reference has already been made to the application of CCDs in digital memories. The most powerful impact that CCDs are likely to have, however, is in the field of analogue signal processing; this is because of the ease with which variable sized charge packets may be positioned, spatially manipulated and delayed in a CCD structure. Hitherto the delay of analogue signals has usually been

a difficult and cumbersome task; mercury and quartz delay lines have tended to be unwieldy and to lack sufficient control over the delay duration, while digital storage techniques have involved the need for bulky and costly A-D and D-A converters which often have the additional disadvantage of high power consumption. By comparison, CCDs provide a very straightforward approach: they can handle analogue signals directly, and in addition, each analogue sample is accurately positioned in time with respect to the other samples and the delay duration can be accurately controlled since it is dependent solely upon the frequency of the applied clock waveform. Conceptually the device has many of the advantages of information processing in the digital domain, i.e. stable, fixed and accurately variable delays, whilst retaining the advantages of conventional analogue signal processing, i.e. high bandwidth and large dynamic range. This capability allows quite complex mathematical operations such as convolution and correlation (which depend upon accurate temporal positioning of each waveform) to be performed with ease. Furthermore, these operations can be carried out with substantially reduced circuitry compared with digital techniques and so units of low cost, size and weight, consuming comparatively little power can be designed. Moreover, the reduction in component count and the integrity of the fabrication technology allows high reliability to be achieved.

Although the CCD evolved directly from the concepts used to develop magnetic bubble devices, several competitors such as the Bucket Brigade Device[3] (BBD) and the Serial Analogue Memory[4] (SAM) emerged at about the same time. Unlike the CCD, which has no discrete circuit equivalent, these devices are based upon the implementation of an analogue delay line with discrete components. There are, however, several disadvantages associated with these alternative schemes such as higher transfer inefficiency, low dynamic range, and increased circuit complexity which makes charge-coupling a more favourable technique.

Another device which has become increasingly important in recent years due to its analogue delay capability is the surface acoustic wave (SAW) device. However, these devices operate at relatively high frequencies (>10MHz) where CCDs generally cease to become usable, and so rather than compete with CCDs they complement them; in fact since there is a small overlap in operating frequencies (at ≈10MHz), particularly if buried channel CCDs are used, the two devices can be used together to advantage in some systems.[5]

The first CCD was very simple and had a relatively poor performance. However, as a result of intensive research and development over the last few years their performance has improved dramatically; in particular, transfer inefficiency has been decreased by several orders of magnitude, and values of 45dB and 90dB for linearity and dynamic range respectively have been obtained. Thus their future in many signal processing systems, both digital and particularly analogue, seems increasingly assured.

In this thesis the application of CCDs to the specific problem of radar clutter reduction by the use of signal integration is discussed in detail. A novel CCD architecture is described that substantially overcomes the problem of transfer inefficiency, an effect that seriously limits the performance of conventional CCD integrators. Before discussing this system, however, CCD techniques and their application to a number of analogue signal processing schemes are briefly reviewed in Chapters 2 and 3, with particular emphasis placed upon performance limitations. In the fourth Chapter, the problem of detecting marine targets in sea clutter is discussed and the signal integrator is identified as a useful and versatile processor to improve target detection. Two types of integrator, i.e. recursive and non-recursive, are described and methods of implementing these systems with parallel transfer CCD structures to reduce sensitivity to transfer inefficiency are proposed. Since both these schemes employ floating-gate charge sensing methods, a rigorous analysis of this technique is carried

out in Chapter 5. In Chapter 6 the design and fabrication of a three-bit test recursive integrator is described and in the following Chapter experimental results on the device are presented. The successful operation of this test device led to the development of a second test recursive integrator which included a number of modifications to improve performance. The design procedure and operation of this device is presented in Chapter 8.

Since the recursive design involves a less complex and smaller chip layout than the non-recursive approach, more attention was paid to the development of the recursive integrator. However, some thought was given as to the most desirable approach to achieve non-recursive integration using parallel transfer CCD structures. This work is reported in Chapter 9, which also includes an investigation of the distortion associated with the type of multiple floating-gate structure to be used in the non-recursive integrator.

CHAPTER TWO

CCD TECHNIQUES AND LIMITATIONS

2.1 Introduction

In the last Chapter the enormous potential of CCDs in many areas of electronics was briefly outlined. Although CCDs exhibit a number of important features that give them a distinct advantage over alternative analogue delay implementations, they have certain inherent limitations; in practice these require careful consideration in order that the CCDs' performance, particularly in analogue signal processing applications, will not degrade the overall system performance.

In this Chapter, therefore, several important aspects of surface channel CCD (SCCD)* design and operation are considered, with particular emphasis being placed upon the performance limitations. In view of the fact that a considerable amount of literature on each of these topics has been published, the sections that follow must be regarded only as a summary of the present situation: this Chapter may be omitted, therefore, by the reader already familiar with the problems associated with CCDs. Before discussing these problems, however, the basic principles of CCD operation are discussed very briefly.

2.2 Basic Principles of Operation

A CCD consists basically of a row of closely spaced MOS capacitors, as illustrated in figure 2.1. If one of the electrodes is pulsed to a sufficiently negative potential (see figure 2.1a), a depletion region is formed in the underlying silicon and minority carriers, which can be made to represent a signal sample, can be stored in an inversion region at the silicon/silicon dioxide

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* Since buried channel devices are not used in the radar application to be described later, the following discussion will be concerned exclusively with surface channel CCD operation.

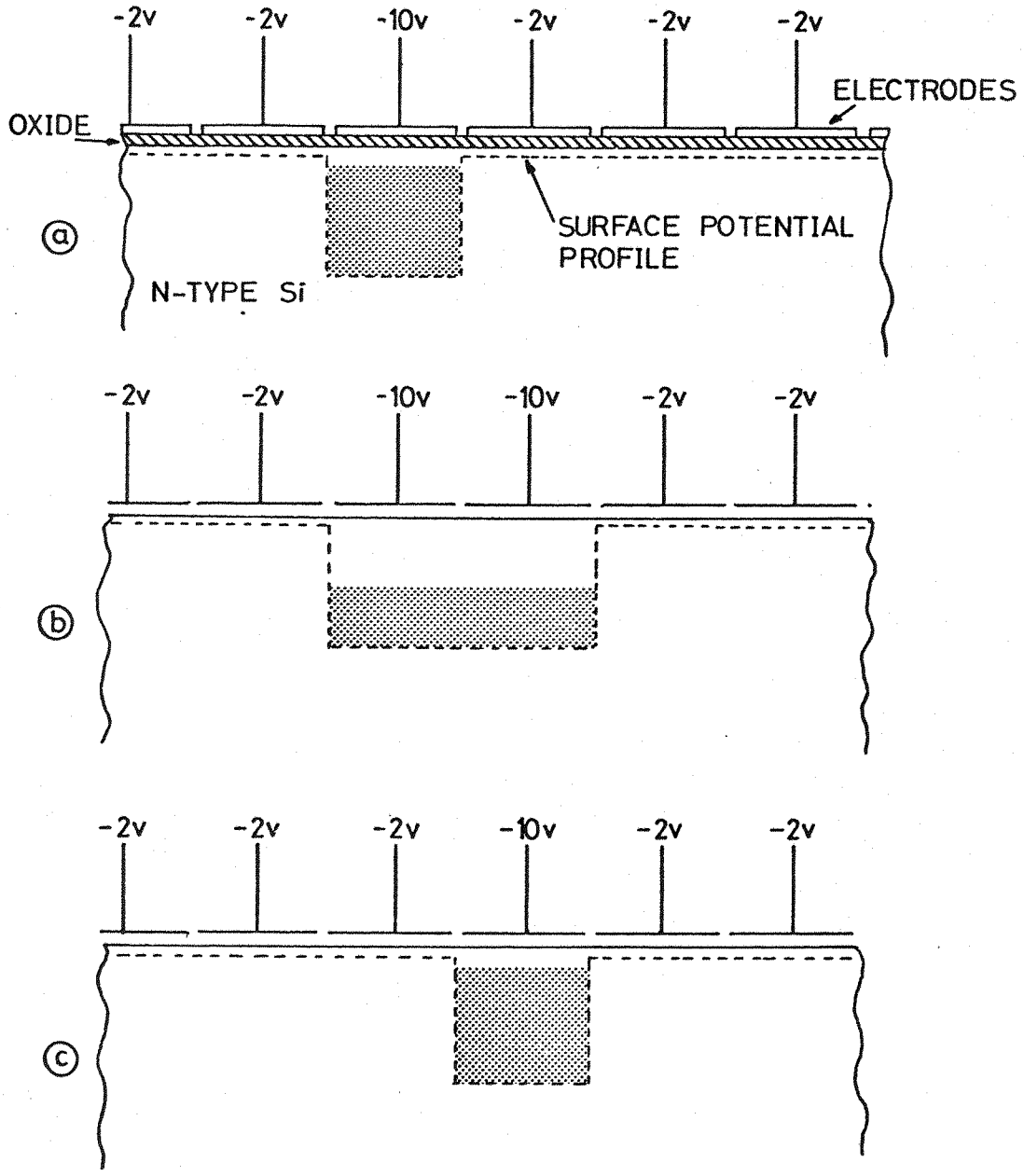

Fig 2.1 The principles of charge-coupled device operation.

interface. If one of the adjacent electrodes is then pulsed to the same potential as the first, the 'signal' charge will distribute itself beneath both electrodes (see figure 2.1b). By reducing the potential on the first electrode, this redistribution will continue until all of the original charge resides beneath the second electrode. If this sequence of operations continues, the charge packet can be manipulated from one end of the row of capacitors to the other.

The equation relating the surface potential, ϕ_S, of an MOS capacitor to the stored charge per unit area, Q_S, and the gate voltage, V_g, can be derived from the one-dimensional form of Poisson's equation; assuming the depletion approximation and a uniformly doped substrate, the relationship is as follows:

$$\phi_S = V_g' + V_o - (V_o^2 + 2V_oV_g')^{\frac{1}{2}} \qquad 2.1$$

where $V_g' = V_g - V_{FB} - Q_S/C_{ox}$

V_{FB} is the flatband voltage of the MOS structure

C_{ox} is the oxide capacitance per unit area

and $V_o = \dfrac{qN_D\epsilon_S}{C_{ox}^2}$

where q is the electronic charge

N_D is the substrate doping level

and ϵ_S is the dielectric constant of silicon.

The manner in which CCD operation is normally depicted is shown in figure 2.1. Immediately underneath the physical structure we depict (by the dotted line) the variation of surface potential of the empty CCD structure. We see that beneath the electrode biased to -10V a 'potential well' is created. With reference to equation 2.1, if V_o is small (for a typical substrate doping level of $10^{15}cm^{-3}$ and a 0.1μm thick oxide layer V_o = 0.14V),

then the surface potential is approximately linearly related to the stored charge. Thus the introduction of charge into the potential wells and the consequent reduction in surface potential is analogous to the filling of the wells with a fluid. When the voltages on the gates change (as shown in figure 2.1 b and c) and a new surface potential profile is defined, the 'fluid' charge flows so that it always resides in the deepest adjacent potential well.*

The manner in which charge may be injected into a CCD and how it may be detected will be discussed in sections 2.4 and 2.5.

2.3 Transfer Electrode Structures and Driving Methods

In order that the number of connections to a CCD may be small and that many charge packets can be transferred along the device, the electrodes are connected together periodically and each 'phase' driven from clock pulse generators synchronised with each other. Many CCD electrode configurations have been proposed which trade off the number of clock waveforms required for satisfactory operation against some other parameter such as charge handling capacity, cell size or circuit complexity. However, only a few structures have emerged that have found wide acceptance and some of these will be discussed below. It is convenient to classify the various structures by referring to the number of driving phases required by the device.

2.3.1 The Three-Phase Configuration

The simplest electrode arrangement is similar to that shown in figure 2.1. This consists of a thin oxide layer, approximately 0.1μm thick, with metal electrodes defined on the surface of the oxide. The minimum number of driving phases to

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* Although it is very useful to employ this analogy to describe the operation of a CCD, it must be remembered of course, that the charge is actually stored at the Si/SiO_2 interface in a partially inverted region approximately 10nm wide.

ensure uni-directional charge transfer is realized by connecting every third electrode together; thus each 'bit' of the CCD consists of three electrodes. This configuration is illustrated in figure 2.2. Unfortunately this simple implementation has associated with it a number of fabrication difficulties. Firstly, in order that efficient charge coupling is maintained between adjacent potential wells, the gap between the electrodes must not exceed two or three microns; this is very much smaller than normal artwork geometries and so, if the electrodes are to be defined in a single layer of metal, stringently controlled photolithographic and etching techniques are necessary. Such narrow gaps inevitably cause a serious reduction in yield since dust particles and mask defects are often of the order of a gap width. Secondly, the connection of the three phases presents a topological problem, which can be overcome in the single level metallization process only by using underpass diffusions; again, this contributes to a reduction in yield.

To overcome these difficulties, several modifications to the basic structure have been suggested and implemented. One solution is to use the structure shown in figure 2.3, fabricated using a polysilicon gate process. Since each polysilicon gate is insulated from its neighbour by a layer of thermally grown SiO_2, typically 0.1μm thick, inter-electrode shorts are few and the possibility of ionic contamination in the gap region is low. Furthermore, phase connections are simplified since the connecting bus for each phase can be defined at each polysilicon stage. However, a disadvantage of this structure is that more processing steps are required, many of which are at elevated temperatures.

If the configuration has to be made with an aluminium gate process (e.g. if a polysilicon process is not available), two schemes have been demonstrated which rely upon a shadowing technique to obtain submicron gaps. The first, invented at Southampton University,[7] employs a double metallization process. Half of each electrode is defined in the first level of aluminium (see figure 2.4a) and a second layer is then obliquely evaporated on

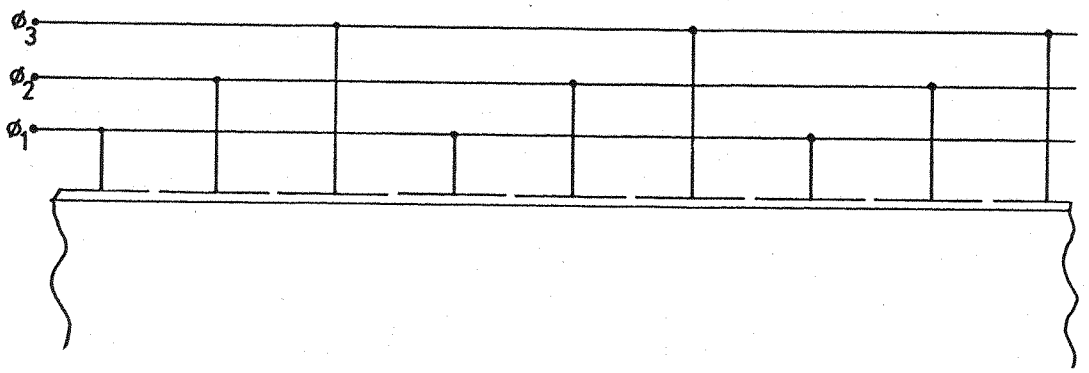


Fig 2.2 The basic three-phase CCD configuration.

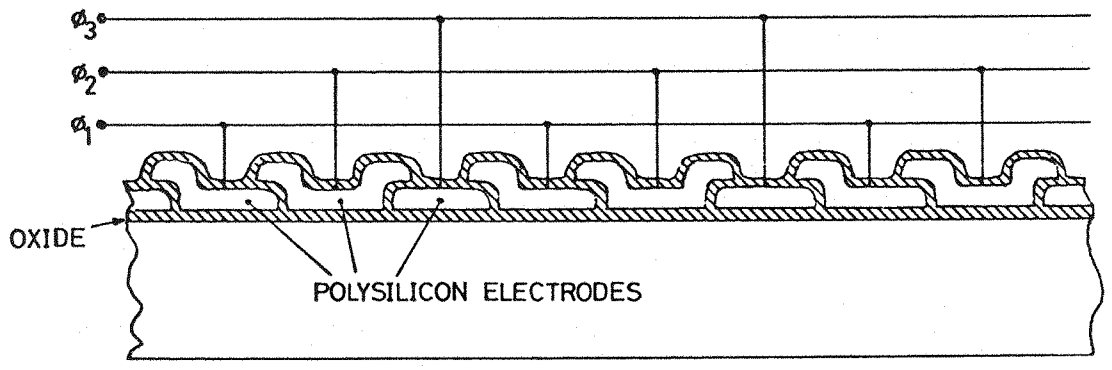


Fig 2.3 The three-level polysilicon three-phase structure.

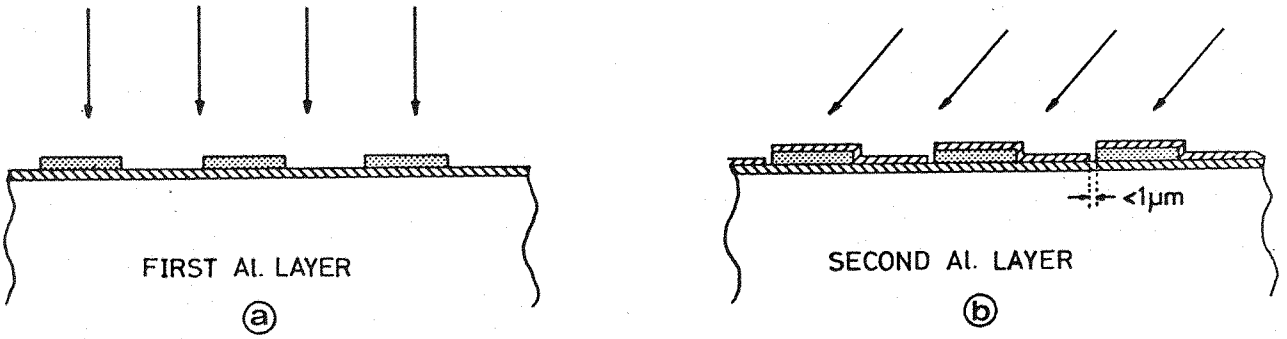


Fig 2.4 A three-phase structure in which sub-micron shadowed gaps are formed with an oblique evaporation.

to the surface (see figure 2.4b). In this way, a gap whose length is dependent on the evaporation angle and the thickness of the first aluminium layer is produced at the 'trailing edge' of each half gate. The second technique also uses two metallizations[8] and is similar to the undercut isolation method described by Berglund et al.[9] Although these techniques do not overcome the problem of interconnecting the phases, they are (particularly at first) very easy to implement, and do not require any increase in high temperature processing time. Furthermore, since the electrodes are non-overlapping, the inter-electrode capacitance is smaller than that of the polysilicon structure; consequently clock feed-through between phases and clock driver power dissipation are reduced.

2.3.2 The Two-Phase Configuration

The number of driving phases required by a CCD may be reduced to two if the charge transfer along the CCD channel is aided by the physical structure of the device. In this case, each 'bit' consists of only two electrodes, thus simplifying the inter-connection of each phase. Unfortunately, however, the charge handling capacity of a two-phase device is less than a three-phase device with the same operating parameters. This is because the maximum charge is determined by the surface potential difference ($\Delta\phi_S$ in figure 2.5) resulting from the asymmetry of the structure rather than on the magnitude of the surface potential in the storage region.

There are several ways of building directionality into the CCD structure. The most obvious is perhaps to fabricate asymmetrical electrodes using a double level oxide layer. Such a structure is shown in figure 2.5, using polysilicon and aluminium gates. However, a much simpler approach is to use a slight modification of the angled evaporation technique described in the last subsection. Workers at Southampton University have extended this technique to enable two-phase structures to be easily

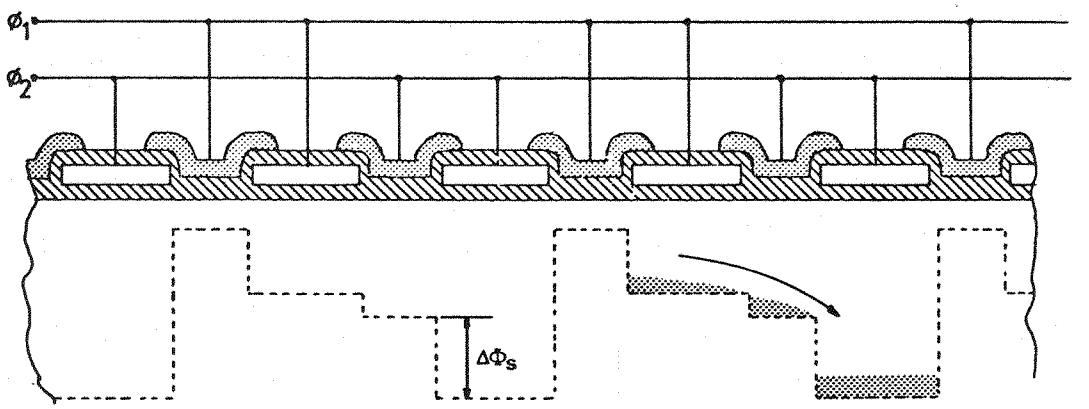


Fig 2.5 A two-phase configuration using an asymmetrical electrode structure.

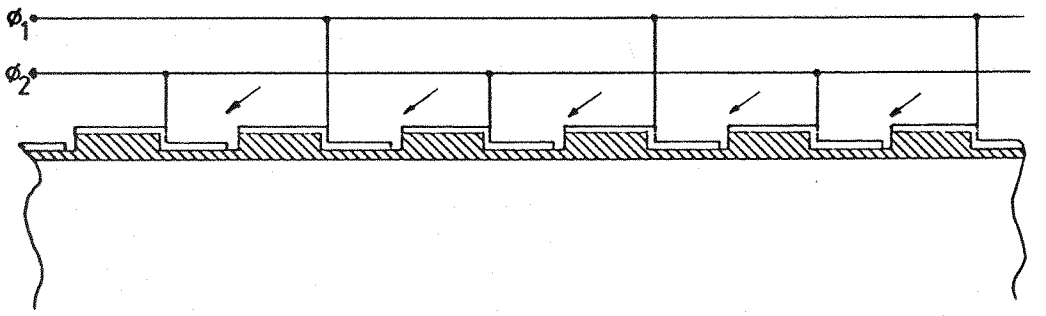


Fig 2.6 Asymmetrical electrodes for a two-phase structure fabricated with an oblique evaporation.

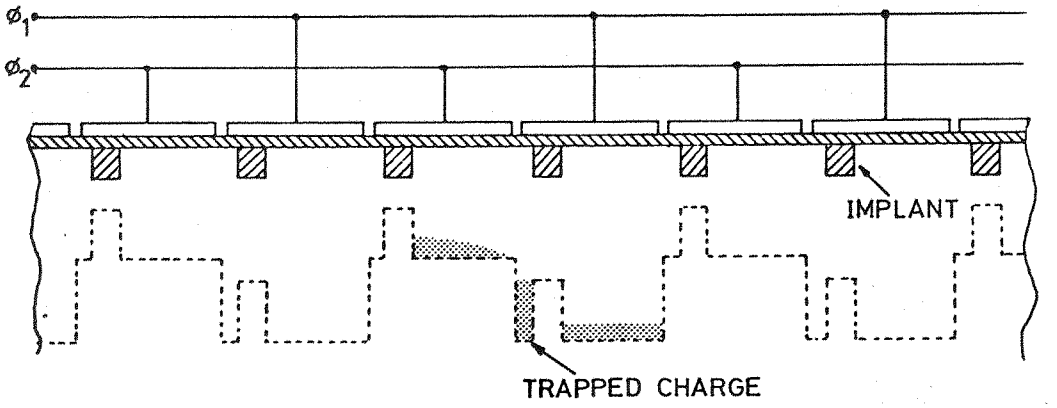


Fig 2.7 An implanted barrier two-phase CCD.

fabricated.[7] In this instance, the metal is evaporated obliquely on to a castellated structure comprising the thick and thin oxide gate regions; gaps in the aluminium film are thus formed in the shadow of each oxide step (see figure 2.6). Another, slightly more complex, fabrication procedure for two-phase CCDs using an undercut isolation technique has been described by Berglund et al.[9]

The asymmetrical potential well produced by the two level oxide structure can also be created if a barrier is implanted beneath each electrode, as shown in figure 2.7.[11] This arrangement has the advantage that by adjusting the level of the implant, it is relatively easy to create a large surface potential step, $\Delta\phi_S$, than with a two level oxide structure, thus enabling larger charge packets to be handled. However, the implant must be placed at least a registration tolerance inside the 'leading edge' of each electrode. This is necessary in order that mask misalignment will not cause the barrier to appear under the inter-electrode region and thus prevent charge transfer. Therefore, it is unavoidable that charge will be trapped behind the barrier and cause the device to operate in the incomplete transfer mode. This is a disadvantage, since it leads to higher transfer inefficiency and transfer noise.

The types of clock waveform required by the three-phase and two-phase structures are shown in figure 2.8. It is desirable that, in addition to the overlapping of three-phase pulses, the falling edges slope or have an exponential decay. If this is not the case, then the source well may collapse faster than the charge can flow into the receiving well, thus part of the charge packet may be lost due to recombination in the substrate as the source well overflows. Indeed, it has been shown[12] that appropriately shaped clocks enhance the critical final stages of charge transfer and so allow the CCD to be driven at higher clocking rates (up to 10MHz). Unfortunately, sloping falling edges can be generated only at the expense of relatively high clock driver power dissipation. However, similar improvements in the charge transfer

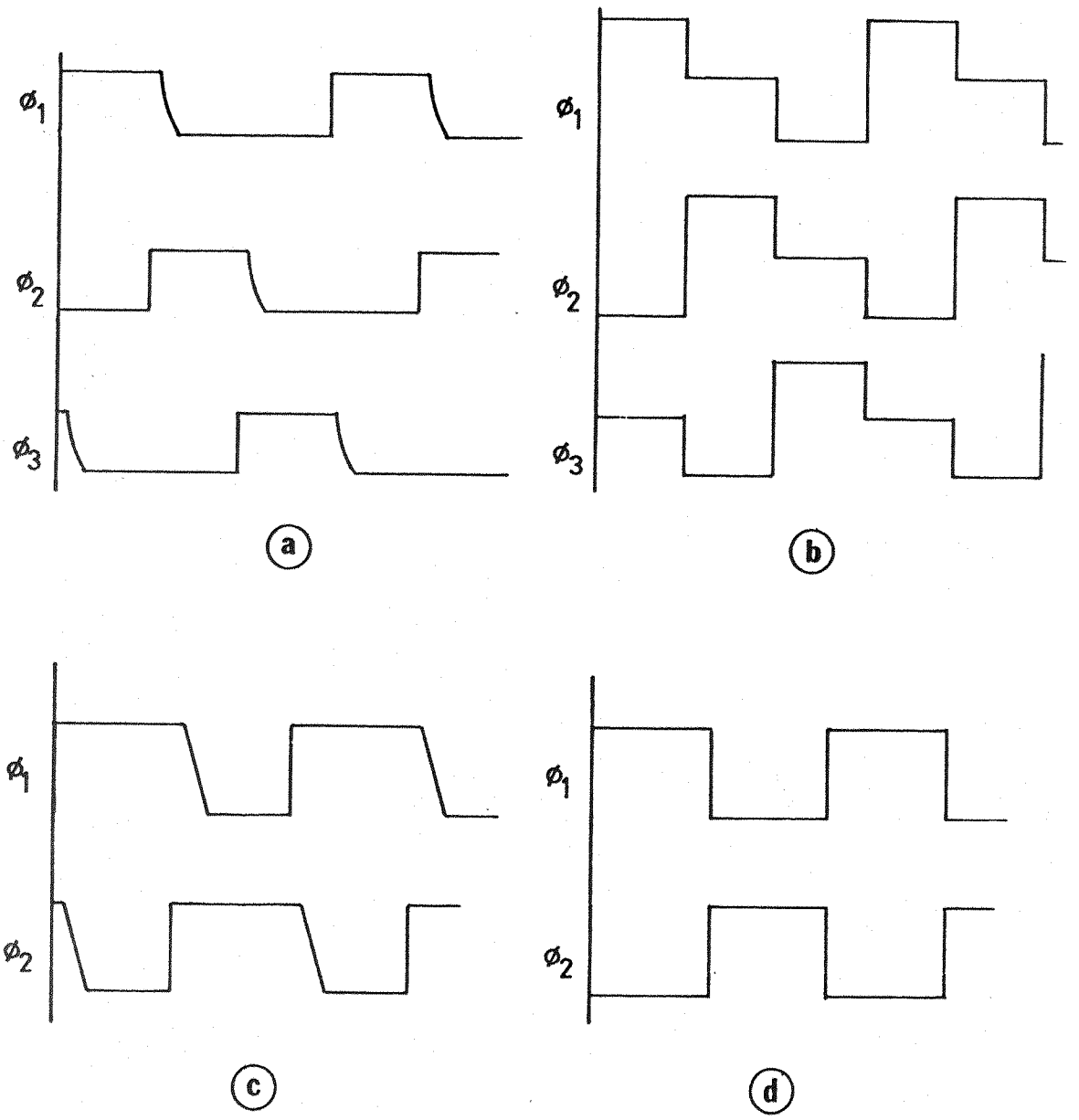


Fig 2.8 Operating clock waveforms for 3 and 2 phase configurations:

(a) Three phase clocks with shaped falling edges.

(b) Stepped three phase clocks.

(c) Two phase overlapping clocks (push clocks).

(d) Two phase complementary clocks (drop clocks).

process may be realized if stepped clocks, as shown in figure 2.8b, are employed. Since shaped falling edges of the waveform are not required in this driving scheme, low power drivers may be designed. A simple low power driving circuit that generates this type of waveform, which could be integrated on to the CCD chip has recently been described.[13]

On the other hand, the asymmetrical potential well created beneath each 'bit' of a three-phase CCD by the stepped clock operation is simulated by the two-phase structure. Thus, higher data rates can be used with these devices whilst retaining a simple clocking scheme (e.g. figure 2.8d) which could more readily be integrated on-chip.

Even further simplification of the clocking arrangement can be realized if one phase of a CCD is biased to a DC level, and the other phase or phases are allowed to swing above and below this level.[14] The charge handling capacity of a CCD operated in this mode is slightly smaller than with conventional clocking; this shortcoming is, however, more than offset by the simple drive requirements, particularly for two-phase devices, which now require only one clock waveform. When a two-phase device is operated in this '1½-phase' mode, there is a danger of incomplete charge transfer[10] if the DC bias and the clock amplitude are wrongly set. This mode of operation, termed the Bucket Brigade mode, is undesirable since it leads to an increase in transfer inefficiency and transfer noise. With care, however, this condition will not occur and so its effects will not be discussed further at this stage.

To summarize this section, it will be readily appreciated that two-phase CCDs have a number of advantages over other configurations. In particular, simple clock generation and driving circuits can be used and, because of their in-built potential well asymmetry, these devices can be easily driven at comparatively

high speeds; furthermore, two-phase structures can be more simply fabricated.

2.4 Charge Injection Techniques

The signal charge in a CCD can be generated either optically or electrically; however, since this thesis is concerned primarily with the signal processing applications of CCDs, only the electrical inputting of charge will be discussed here.

Since the invention of CCDs, much work has been done to develop techniques that inject an accurately controlled amount of charge into the CCD channel; these schemes fall into two clearly defined categories: those techniques that ideally launch a charge packet whose magnitude is linearly dependent upon the input voltage, and those techniques in which ideally the surface potential of the first potential well (and under certain conditions, the potential wells in the rest of the device) is linearly dependent upon the input signal voltage. Some commonly used input schemes for achieving one or the other of these conditions will now be discussed, with particular reference to linearity and noise performance.

2.4.1 Potential Equilibration Charge Injection Schemes

Several structures have been proposed that provide a linear input voltage-to-charge transfer function in both two and three-phase CCDs; these have variously been described as potential equilibration,[15] fill and spill,[16] charge preset[17] or supply charge isolation[18] methods. They all require at least two separately accessible electrodes before the first regular CCD electrode, and a source of minority carriers in the form of a diode diffusion fabricated adjacent to the first electrode of the structure. Several implementations and their operation are shown in figure 2.9; the transfer characteristics of these injection schemes may be easily derived by first rearranging equation 2.1 to obtain an expression for signal charge, Q_s, in terms of gate voltage and

surface potential

$$Q_s = C_{ox} (V_g - \phi_s - \sqrt{2V_o\phi_s} - V_{FB}) \qquad 2.2$$

Considering first the structure in figure 2.9a, during the period when ϕ_1 is off, the input diode is pulsed to a low voltage and the potential wells beneath G_1 and G_2 are allowed to overfill. When the diode potential is restored to a high level, excess charge spills back into the diode leaving a charge Q_s trapped beneath the G_2 electrode. Q_s is given by equation 2.2 in which V_g is the signal voltage, V_{in}, applied to G_2. The surface potential, ϕ_s, will be defined by the potential on G_1; in fact by further rearranging equation 2.2, and bearing in mind that no charge is stored beneath G_1, we have that

$$V_{g1} = \phi_s + \sqrt{2V_o\phi_s} + V_{FB} \qquad 2.3$$

if the MOS parameters for each gate are the same. By substituting 2.3 into 2.2, we obtain

$$Q_s = C_{ox} (V_{in} - V_{g1}) \qquad 2.4$$

thus Q_s is linearly dependent upon the differential voltage between G_1 and G_2. Clearly, the roles of G_1 and G_2 may be reversed (see figure 2.9b), giving a complementary charge injection scheme.

By connecting the input diode to ϕ_1, the 'phase referred' input method is realized (figure 2.9c) which has several advantages over the previous two schemes: in particular, the need for a diode injection pulse is eliminated, and sampling distortion at frequencies close to the Nyquist limit is reduced. This distortion arises as a result of the finite time interval during which the input signal is sampled. Sequin and Mohsen[19] have analysed this effect, but have shown experimentally that for sampling intervals of less than $\simeq 2\mu s$, the distortion due to this

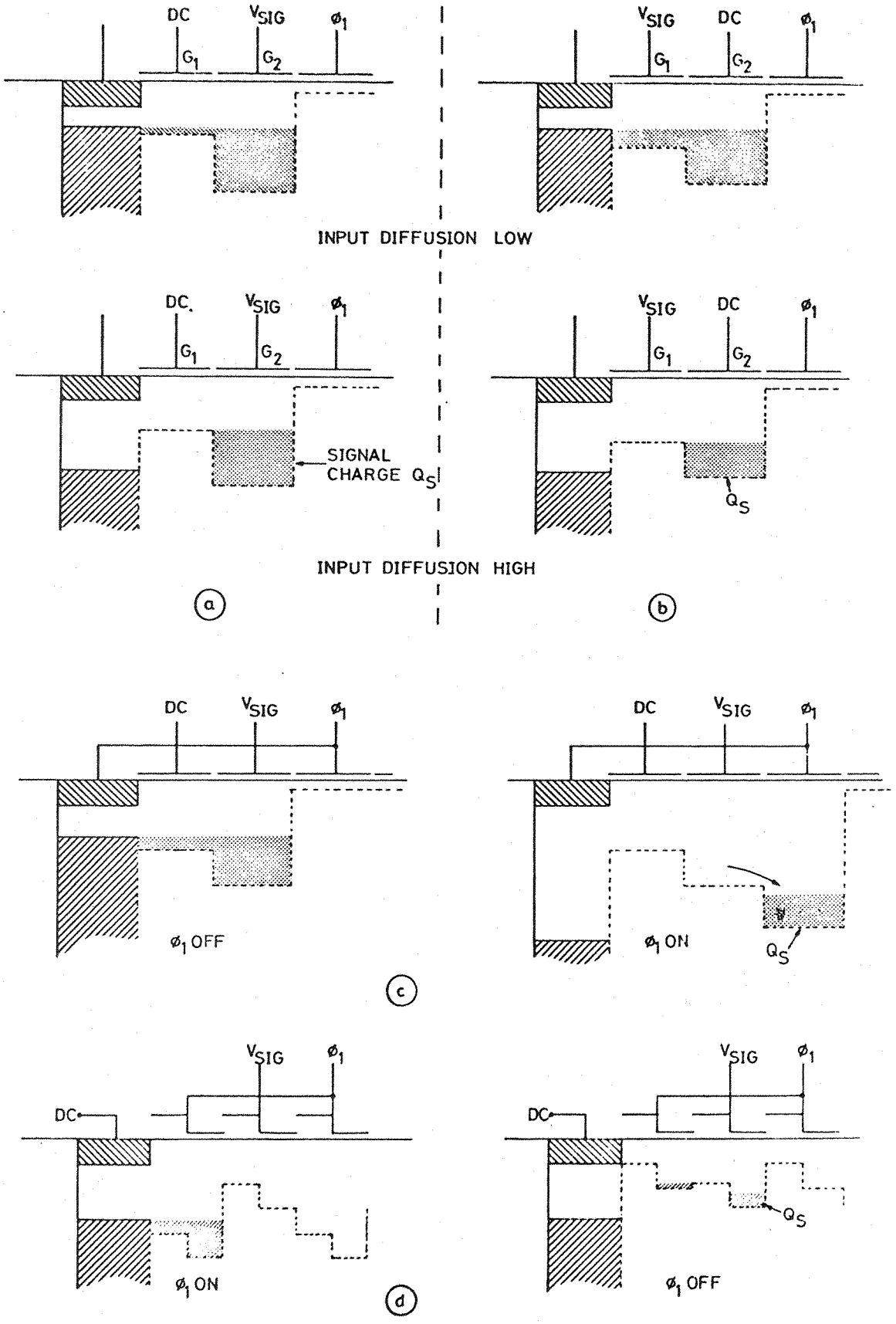


Fig 2.9 Various potential equlibration charge injection schemes.

effect is much less than is predicted. The reason for this is that the finite time required for the charge packet to equilibrate reduces the effective width of the sample interval and so an actual 2μs sample window is significantly reduced. Since the sample interval of the phase referred method is approximately equal to the turn-off time of the ϕ_1 clock waveform, this type of distortion is not evident even at very low data rates.

Figure 2.9d shows a simple highly linear charge injection scheme for two-phase CCDs, requiring only the existing ϕ_1 clock waveform. An analysis of this scheme (Appendix 1)[18] shows that the signal charge, Q_s, is proportional to the potential difference between the two input electrodes. Unfortunately this scheme presents the worst case for sampling distortion at low clock frequencies, since the sample interval is equal to the off period of the ϕ_1 clock waveform. However, this could be reduced if the pseudo-high frequency clocking scheme described by Haken et al.[20] were used.

Experimental measurements have confirmed that, if sampling effects are negligible, the techniques just described do give a highly linear input voltage-to-charge conversion. However, observation has also shown that the linearity is reduced if the second input electrode area is reduced. It has been suggested that the causes of this non-linearity are the increasing influence of fringing fields on the smaller charge packet. This would also account for the slightly inferior performance observed for the scheme of figure 2.9b; in this case, the application of the signal to G_1 causes equilibration of the metered charge packet to occur at different values of surface potential and consequently with different fringing fields. Some published results on these schemes are shown in figure 2.10. It can be seen that second harmonic distortion levels of less than 0.5% (-46dB) can be obtained, and it has been estimated that by careful electrode design, this figure could be decreased to 0.1% (-60dB).

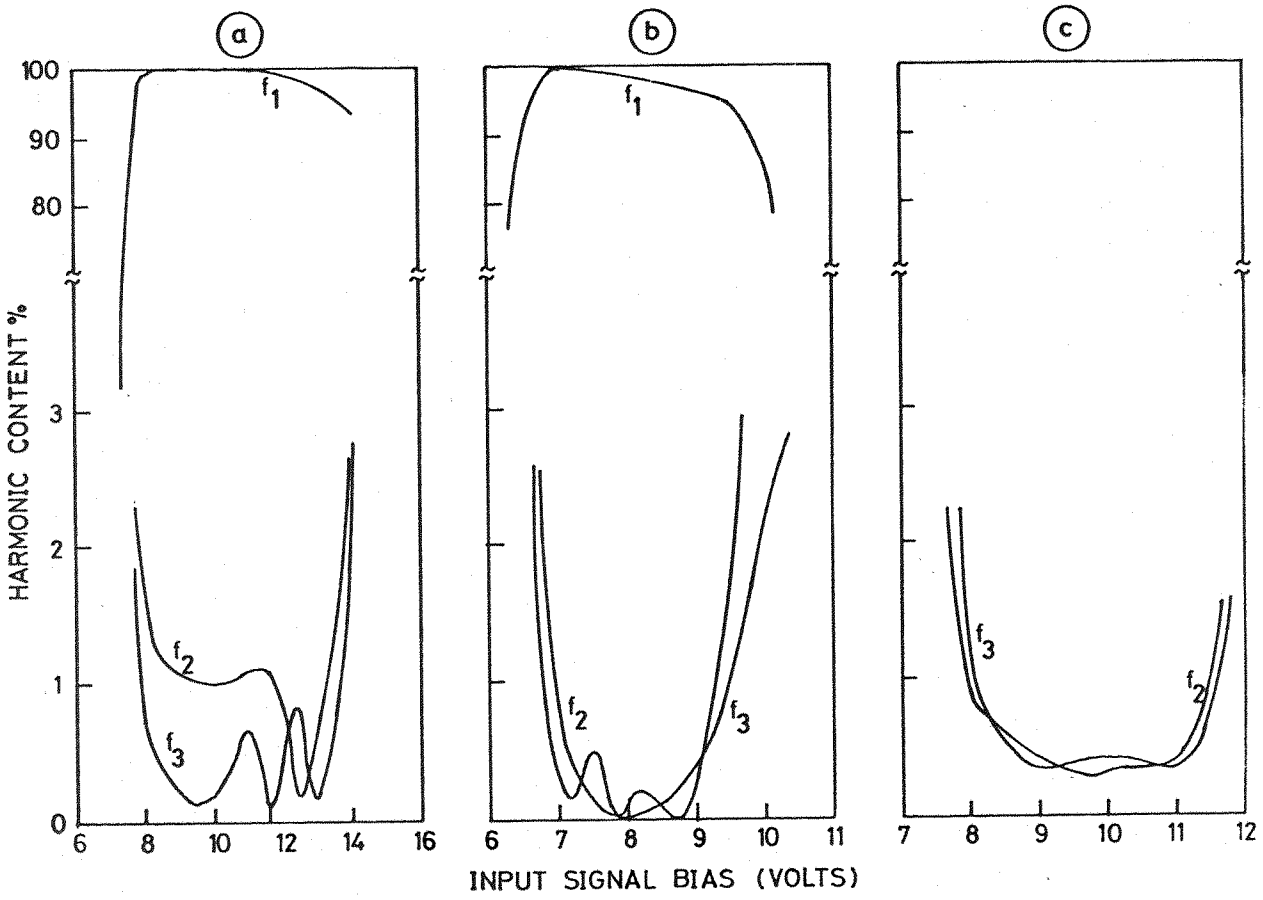


Fig 2.10 Measured harmonic components of various potential equilibration charge injection schemes. (a) and (b) are three-phase schemes with the signal applied to the first and second gate respectively. (c) is the two-phase method.

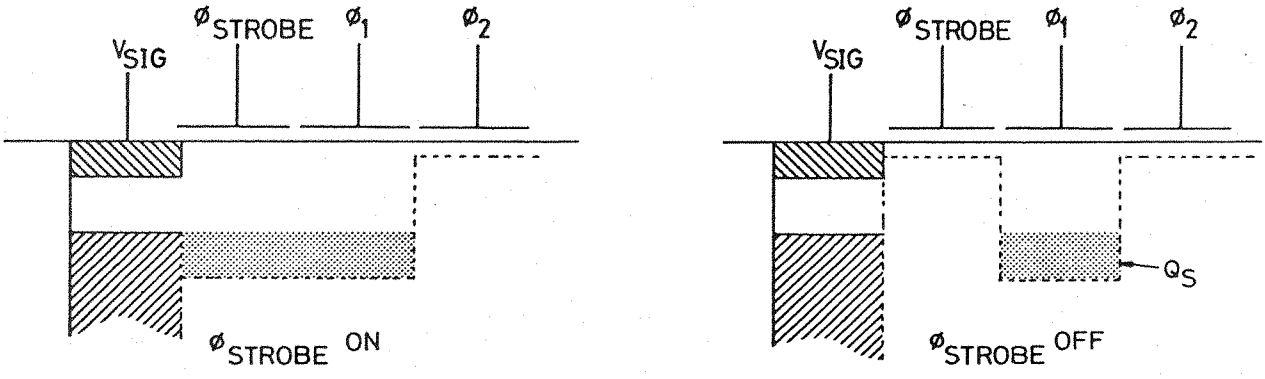


Fig 2.11 The diode cut-off charge injection technique.

The major noise source associated with the charge injection techniques described in this section are fluctuations in the emission of excess carriers over the metering barrier potential. This noise is introduced at each charge equilibration and can be characterised by the thermal noise associated with an MOSFET draining (or charging) a capacitance, C_w, representing the metering well capacitance. A rigorous derivation[21] yields the following expression for the mean square fluctuations in charge retained on C_w.

$$\Delta\bar{Q}_s^2 = {}^2/_3\, kT\, C_w \qquad 2.5$$

where k is Boltzmann's constant in J/K^o and T is the absolute temperature. If sufficient time is allowed for the equilibration, then the process becomes emission limited and equation 2.5 is modified to

$$\Delta\bar{Q}_s^2 = \tfrac{1}{2}kT\, C_w \qquad 2.6$$

For typical well capacitances of 0.4pF, then r.m.s. noise fluctuations would be approximately 200 electrons; the charge storage capacity of such a well with a 10V surface potential variation would be approximately $25 \cdot 10^6$ electrons, thus with these schemes it is possible to introduce a charge packet with a signal-to-noise ratio of ≈100dB. However Carnes[22] and Mohsen[23] have reported noise fluctuations in excess of the figures predicted by equation 2.5, and have suggested that the additional noise is due to random variations in clock amplitude and pulse width coupled to the input section through electrode overlap capacitances. This suggestion was supported by measurements of the spectral density of the noise which showed a linear increase with frequency, as would be expected from capacitive coupling. Additionally, Kandiah,[24] using a different measurement technique, has obtained good agreement between his results and the theoretical values

predicted by equation 2.5. These results were obtained on devices with non-overlapping electrodes separated by 4μm gaps and clocked from accurately controlled clock sources; in this system, therefore, clock noise feedthrough was probably very small.

2.4.2 The Diode Cut-Off Charge Injection Scheme

The diode cut-off technique[25] for introducing charge into a CCD is so far the only technique that attempts to provide a linear transfer function between the input voltage and the surface potential of the first potential well. The scheme is illustrated in figure 2.11; the signal is continuously applied to the input diode, whilst the input gate, G_1, is strobed during the 'on' period of the ϕ_1 clock. When G_1 is switched on, minority carriers from the diode flow into the potential wells under G_1 and G_2 until the surface potential beneath these electrodes is equal to the reverse bias on the diode, i.e. the input voltage. G_1 is then switched off. Although the charge retained beneath G_1 is not a linear function of the input voltage (from equation 2.2), the surface potential beneath this, and any other subsequent transfer electrode maintained at the same voltage will be. This scheme is not suitable for use in a conventional CCD analogue delay application since the charge-to-voltage conversion at the output of a CCD is generally fairly linear. It can be used to advantage, however, in tapped delay line applications; for example, in transversal filters, where potentially, this scheme can yield a linear overall transfer response (see Appendix 2). Unfortunately, however, there is associated with this injection technique, a non-linearity due to the partitioning of the charge beneath G_1 between the diode and the signal charge as G_1 switches off. The extent of the non-linearity depends upon electrode geometries and clock waveform shape. For example, it could be reduced by the use of a minimum-geometry input gate in conjunction with long transfer gates, and by slowing down the falling edge of the strobe pulse applied to G_1 to allow the signal charge to equilibrate with the diode up until the moment of cut-off. Experimental[19] and analytical[26] results

have shown that with 10μm long electrodes, non-linearities as high as 5% (-26dB) may be introduced, however, on carefully designed structures, non-linearities of better than -45dB have been observed (see Appendix 2).

If charge partitioning is ignored, the expected noise fluctuations in the charge packet size can be derived in a similar fashion to that of section 2.4.1, but in this case the well capacitance, C_W, is charged through the channel of a MOST operating in the linear region. An analysis of this situation yields a mean square fluctuation in signal charge, Q_S, of

$$\Delta\bar{Q}_S^2 = kT\, C_W \qquad 2.6$$

As discussed previously, clock coupling also introduces an additional source of noise. By far the largest noise fluctuations associated with this technique arise, however, because of charge partitioning; values many times the thermal noise associated with the charge packet have been reported.[23] Clearly, this is a highly undesirable situation and so careful attention must be paid to the design and operation of devices employing this technique.

2.5 Charge Sensing Schemes

In this section, several schemes for sensing the transferred charge packet are described.

2.5.1 Diffusion Current Sensing

Although this scheme does not have extensive implementation in CCDs at present, it enables a highly linear charge-to-voltage conversion to be achieved and for this reason, is briefly described here.

The scheme in its simplest form is shown in figure 2.12; a diffusion is fabricated at the end of the CCD channel and reverse-

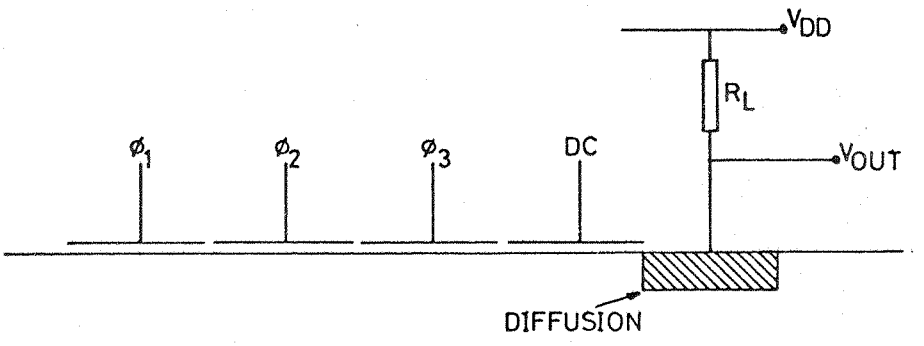


Fig 2.12 The diode current sensing charge detection scheme.

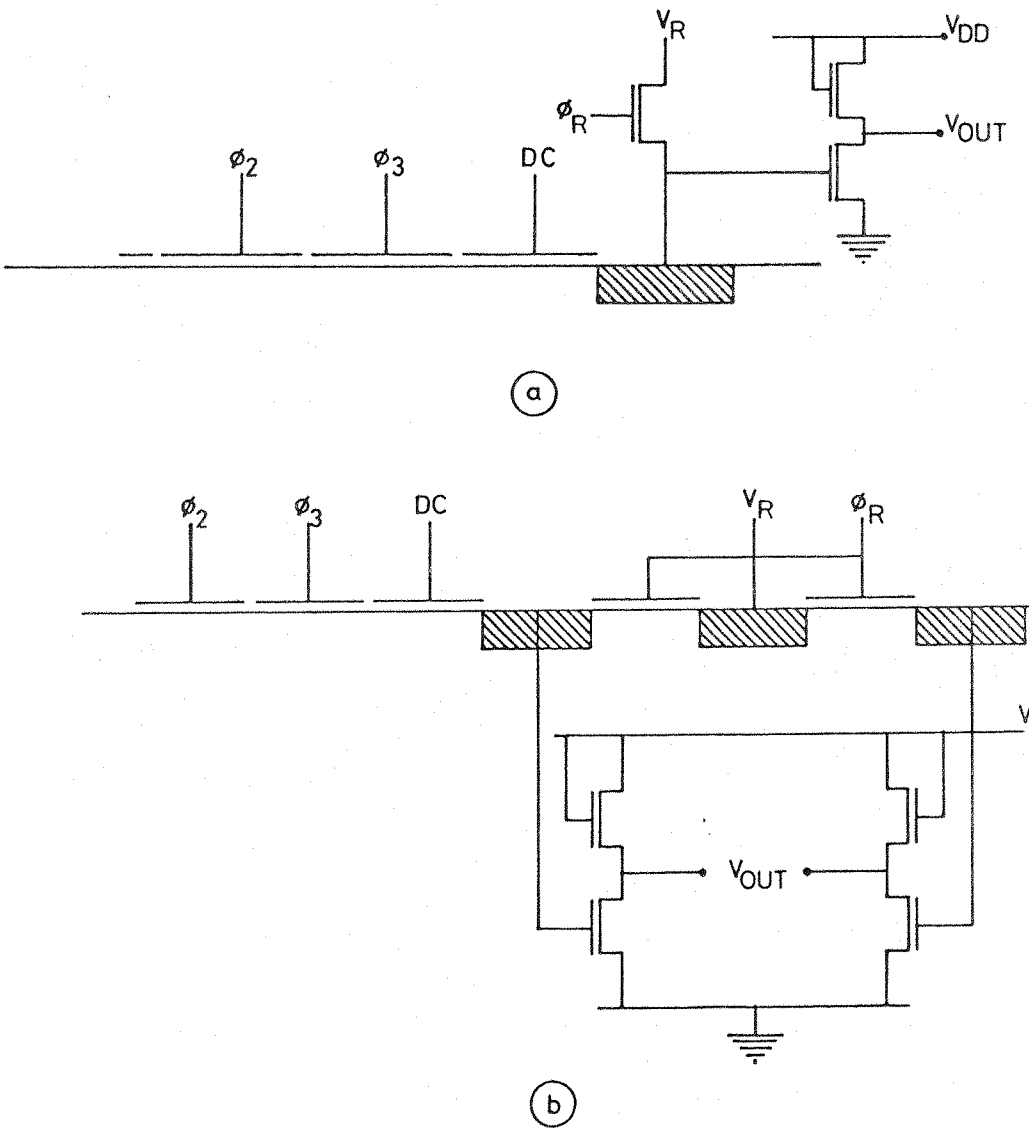


Fig 2.13 Floating diffusion charge sensing schemes.

(a) Conventional circuit.

(b) An arrangement for cancelling reset pulse feedthrough.

biased through a large impedance. As charge is transferred on to the diode, current will flow through the load, R_L, in order to restore the original potential of the diode. The resulting voltage spike across R_L may then be detected with a high input impedance amplifier. The drawback associated with this simple technique is that subsequent signal processing of the series of voltage spikes is difficult, and so designers have favoured the sensing techniques to be described later.

The noise fluctuations introduced with this technique are those associated with the capacitance of the reverse-biased diffusion, and any clock noise coupled to the diode from adjacent clocked electrodes. This latter source can be considerably suppressed by interposing an electrode biased to a DC level between the last phase gate and the diffusion.

2.5.2 Floating Diffusion Sensing

In this scheme, the charge packet is transferred to a diffusion, at the end of the CCD channel, which has been preset to a voltage V_R, via an MOS switch (see figure 2.13a). The voltage developed across the diffusion and load capacitances is then sensed, usually by an on-chip, MOST amplifier. However, at the sensing node, a trade-off between linearity and dynamic range arises; increasing the (linear) loading capacitance at the input of the sense amplifier reduces the effect of the non-linear depletion capacitance of the diode, but unfortunately simultaneously reduces the amplitude of the signal voltage.

Feedthrough of the clock waveform and the reset transistor switching waveform, ϕ_R, with their associated noise fluctuations, can be suppressed in a manner similar to that suggested for the last scheme, i.e. by employing an appropriately positioned DC-biased gate. Another method of reducing the reset pulse feedthrough is to fabricate a dummy sense diode and MOST amplifier of identical dimensions to the regular sensing array (see figure 2.13b). Reset

feedthrough on to this diode can then be subtracted from the main output. The dominant remaining noise associated with this technique, is kTC noise arising from the charging of the sense node capacitance through the reset MOST. However, this can largely be eliminated if a technique known as correlated double sampling (CDS)[27] is employed.

2.5.3 Electrode Current Sensing

This scheme is similar in principle to the diode current sensing method, except that the diode is replaced by an electrode above the CCD channel (see figure 2.14). The capacitive coupling between the electrode and the channel will result in a detectable current flow on to the electrode, when charge is transferred to the underlying potential well. An important feature of this method is that the transferred charge remains unaffected by the sensing process and so may be transferred, unchanged, along the channel to other sensing points; this forms the basis of a tapped delay line which may be used to implement a transversal filter.

Although the depletion capacitance of the potential well beneath the electrode introduces a non-linearity into the charge sensing operation, it can be shown (Appendix 2) that, by using a surface potential setting charge injection scheme, the overall transfer function, from the input of the CCD to the output from the charge amplifier, is linear provided that the sense electrode is maintained at the same potential as the input gate.

The noise sources associated with this method are similar to those of the diode current sensing scheme.

2.5.4 Floating-Gate Voltage Sensing

In its simplest form, this technique employs an electrode structure similar to that described for electrode current sensing. Having been set to a sufficiently large potential, the sensing electrode (see figure 2.15a) is electrically isolated. As the

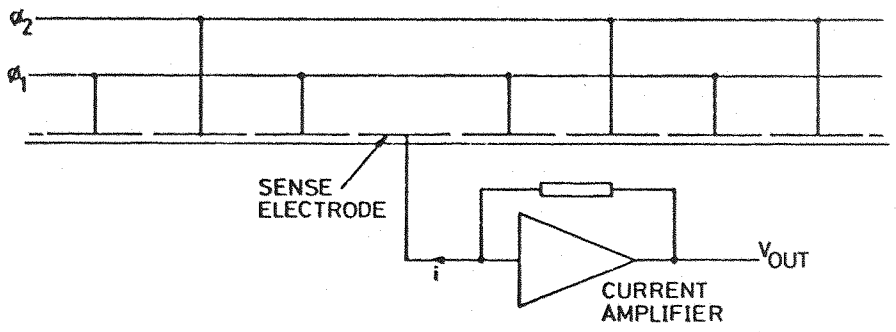


Fig 2.14 Electrode current sensing.

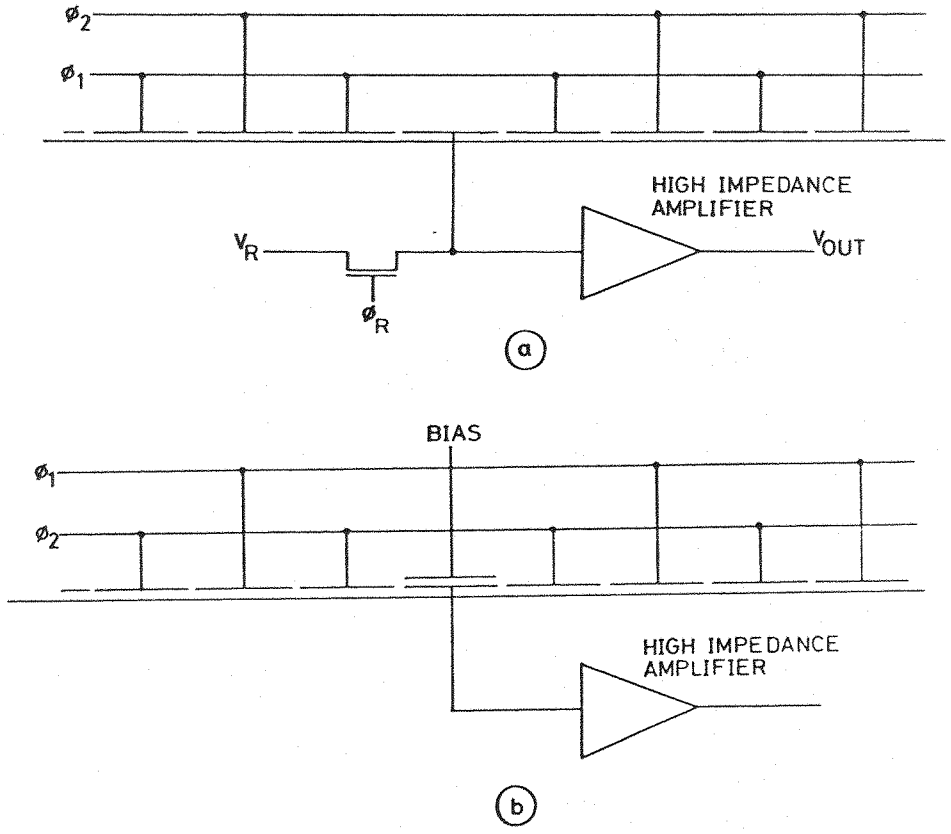


Fig 2.15 Floating gate voltage sensing. (a) with MOST reset; (b) with capacitive biasing.

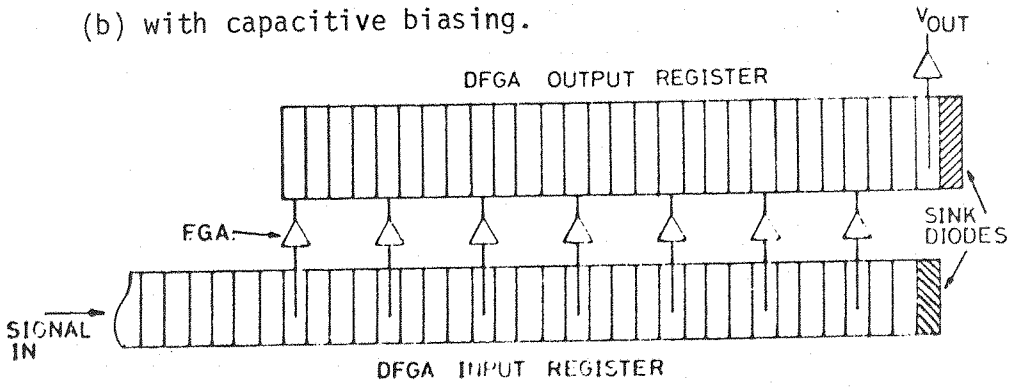


Fig 2.16 A schematic of the distributed floating gate amplifier.

potential well receives charge, the surface potential falls, inducing a corresponding change in the 'floating' electrode potential. In any practical system, the sensing amplifier capacitively loads the electrode and it can be shown (Appendix 2) that the resulting charge-to-voltage conversion is non-linear. As with electrode current sensing, however, this scheme has the desirable feature that the charge is sensed non-destructively.

It has already been indicated that if a capacitance is charged through a conductance kTC noise arises; thus for this simple floating-gate arrangement the noise performance will be limited by the thermal noise in the channel of the reset transistor. However, by suitably modifying the structure the charging process and hence the kTC noise can be avoided. Such a modification is shown in figure 2.15b. The floating-gate is sandwiched between the channel and a DC biasing gate which sets the floating potential by capacitive division. With this arrangement the dominant noise sources[28] are the $^1/_f$ and thermal noise of the sensing MOST. This improvement can be extended further by making use of the non-destructive charge sensing facility to implement a distributed floating-gate amplifier (DFGA)[29] shown schematically in figure 2.16. It has been estimated that this method can be used to detect charge packets as small as only 10's of electrons.

Another floating-gate implementation which avoids periodically resetting the electrodes and does not rely upon complex two layer fabrication schemes necessary for the capacitive biasing system may be realized by connecting the floating electrodes to a large potential through a high impedance; this may either take the form of a high value resistor[30] or, even more simply, the electrodes can be allowed to float to the average potential of the adjacent transfer electrodes; this latter scheme will be described in greater detail later.

2.6 Transfer Inefficiency

One of the most important parameters used to specify the performance of a CCD is the inefficiency involved in transferring charge from one potential well to another. This parameter, usually designated by ε, was defined by Berglund[31] as

$$\varepsilon = \frac{\Delta Q}{Q_s} \qquad 2.7$$

where ΔQ is the charge lost per transfer from the signal charge Q_s. The considerable amount of work done on this effect can be subdivided as follows:

(i) The modelling of the dispersion.[31,32,33,34]

(ii) Investigations into the quantitative effects of ε on CCD performance.[35,36]

(iii) Development of methods to mitigate the effects of ε.[37]

Clearly, in the space available here, the subject of transfer inefficiency can be discussed only very briefly.

It is useful when considering transfer inefficiency to distinguish between three types of loss.

(i) *Proportional loss:* In this case the charge lost, Q_{loss}, is proportional to the size of the charge packet, and thus the transfer inefficiency parameter will be a constant, i.e.

$$Q_{loss} = \varepsilon Q_s \qquad 2.8$$

In general this loss is caused when insufficient time is allowed for the transfer process, and by surface state trapping at the edges of the storage well. Although it can usually be decreased

slightly by increasing the level of background charge, it cannot be eliminated.

(ii) *Fixed loss:* In this case a fixed amount of charge is lost at each transfer, independent of signal amplitude. The major causes of this effect are the Si/SiO_2 interface (surface) states which will trap charge from a charge packet as it propagates along a device. This effect is particularly marked if prior to the introduction of a charge packet, the states have been completely discharged by transferring a long series of completely empty wells through the device. The introduction of a background charge or fat-zero considerably reduces this loss by ensuring that the charge trapped is replenished by the emission of a similar amount of charge trapped during the previous transfer cycle.

(iii) *Non-linear loss:* In this case the charge lost is non-linearly dependent on the signal charge packet, and so ε will be a function of Q_s, i.e.

$$Q_{loss} = \varepsilon (Q_s) Q_s \qquad 2.9$$

In general this type of loss is caused by potential barriers occurring between electrodes that are too widely separated. Although types (i) and (ii) are special cases of (iii), it is useful to retain the distinction since it can simplify device characterization.

An analysis of the transfer process can be carried out most usefully by employing the potential well model (in contrast to the charge control model of Berglund and Thomber[33]) described earlier. However, the assumption of rectangular potential wells of the idealized model tends to lead to pessimistic estimates of transfer inefficiency; in practice, the wells merge (see figure 2.17) giving rise to an electrostatic field in the direction of charge transfer, generally termed a 'fringing field'. For CCDs fabricated on lightly doped substrates ($<10^{15}cm^{-3}$), after the initial transfer

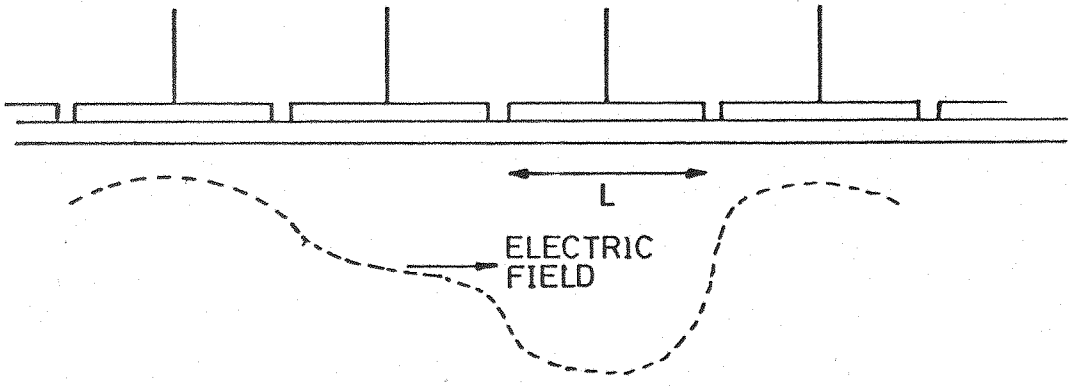


Fig 2.17 Longitudinal fringing fields caused by merging potential wells.

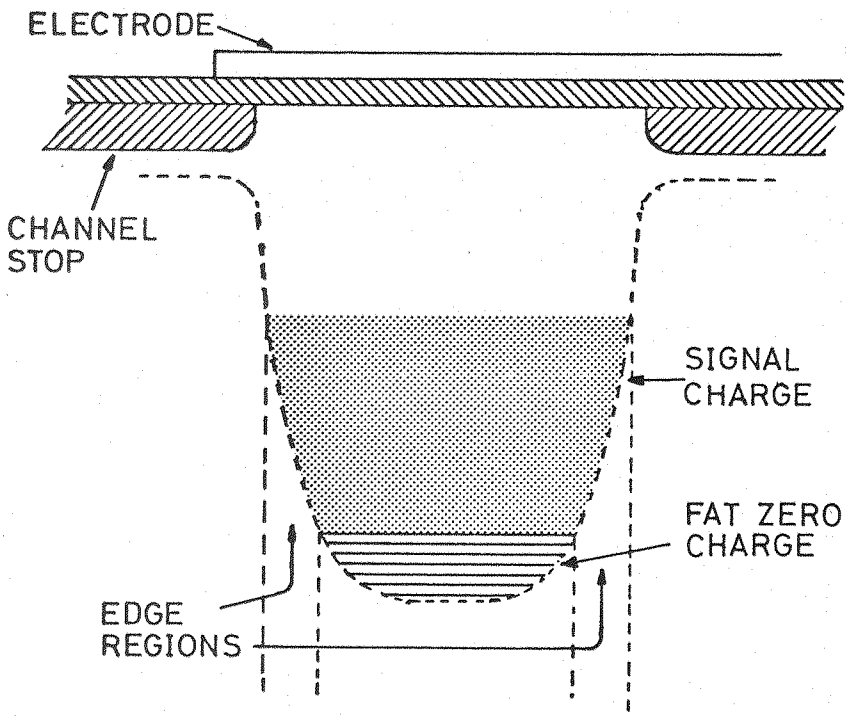


Fig 2.18 A cross sectional view of the channel showing the regions not covered by the fat-zero charge.

transient, the fringing field-induced drift dominates thermal diffusion and self-induced drift and so considerably reduces the decay time constant of the charge in the source well. By ignoring other loss effects, Carnes et al.[38] have derived an approximate expression for the minimum transfer time, t_F, to achieve an ε of 10^{-4} under fringing field-aided drift. The expression is

$$t_F \simeq 0.62 \left[\frac{L^3}{\mu x_d V}\right]\left[\frac{5x_d/L + 1}{5x_d/L}\right]^4 \quad ; \qquad 2.10$$

where L is the electrode length, μ is the carrier mobility, x_d is the depletion region width beneath the centre of the source electrode, and V is the clock voltage amplitude. For a device with typical parameters, i.e. L = 10μm, $N_D = 10^{15}cm^{-3}$, V = 10V, and an oxide thickness of 0.1μm, $t_F \simeq$ 8ns which is an order of magnitude less than if fringing fields were absent. Since the transfer process depends non-linearly upon the gate length, a reduction of this geometry will result in a significant decrease in transfer time, thus allowing higher clocking rates to be satisfactorily employed.

The foregoing discussion was concerned mainly with the transfer inefficiency in three-phase CCDs. Estimates of this parameter in two-phase CCDs is complicated by the fact that the initial stage of the transfer process is limited by the maximum current that can flow through the 'channel' region beneath the thick oxide portion of each phase electrode. This part acts as the gate of an MOST operated at pinch-off with the storage wells comprising the source and drain regions. During the last stages, however, the rate of charge transfer becomes dependent upon how fast the source well can be emptied. If the thick oxide gate portion is much shorter than the thin oxide section, the fringing fields in this area are large enough to immediately sweep any charge leaving the source well into the receiving well; thus the final stages can be characterised by a three-phase type transfer.[39]

It was indicated earlier that surface state trapping is a major cause of transfer inefficiency, but that it may be reduced by injecting a fat-zero alongwith the signal charge. Although the surface states beneath the centre of the electrode can be 'neutralized' by this technique, the states beneath the edges of the electrodes cannot since the signal packet occupies a larger area of the Si/SiO_2 interface than the bias charge, as illustrated in figure 2.18. Clearly by keeping the area of the interface not exposed to the fat-zero charge to a minimum, the loss caused by this so-called 'edge effect' can be mitigated. This can be accomplished by shortening the electrodes and increasing the substrate doping level to 'sharpen' the potential well edges (this latter solution will, however, conflict with the desire to have large fringing fields). An analysis of this situation shows that the best transfer inefficiency, ε_E, due to the edge effect achievable in an SCCD is given by [40]

$$\varepsilon_E \simeq 9.8 \times 10^{-4} \left[\frac{1}{W}\right]\left[\frac{N_{SS}}{10^{10}}\right]\left[\frac{10^{15}}{N_D}\right]^{\frac{1}{2}} \qquad 2.11$$

where W is the electrode width in microns and N_{SS} is the surface state density in $cm^{-2}ev^{-1}$.

The effect of inefficient charge transfer in a CCD is to cause a frequency dependent phase shift and attenuation of the signal. Characterization of this effect can most conveniently be carried out by using the z-transform.[35,41] An approximate expression for the amplitude response of a CCD with a constant transfer inefficiency is[42]

$$A(f) \simeq \exp\ -Np\varepsilon\ (1 - \cos 2\pi\ f/f_c) \qquad 2.12a$$

and for the additional phase shift with respect to the ideal CCD

$$\Delta P(f) \simeq Np\varepsilon\ \sin(2\pi\ f/f_c)\ \text{rads} \qquad 2.12a$$

where N is the number of bits, p is the number of phases and f_c is the clock frequency. The amplitude and phase response are plotted in figure 2.19 for different values of $Np\varepsilon$ product; from this it can be seen that provided $Np\varepsilon < 0.1$, the analogue performance is not unduly degraded.

In addition to causing an attenuation of high signal frequencies, the charge left behind at each transfer also shows a random fluctuation in size, and therefore adds noise to the signal being processed. However, since a fluctuation causing an excess of charge to be left behind results in a larger deficit in the main charge packet, and vice versa, the variations in adjacent charge packets will be correlated, and so the noise spectral density will have a special characteristic; in fact it will be suppressed at low frequencies and enhanced at high frequencies and has the form[43]

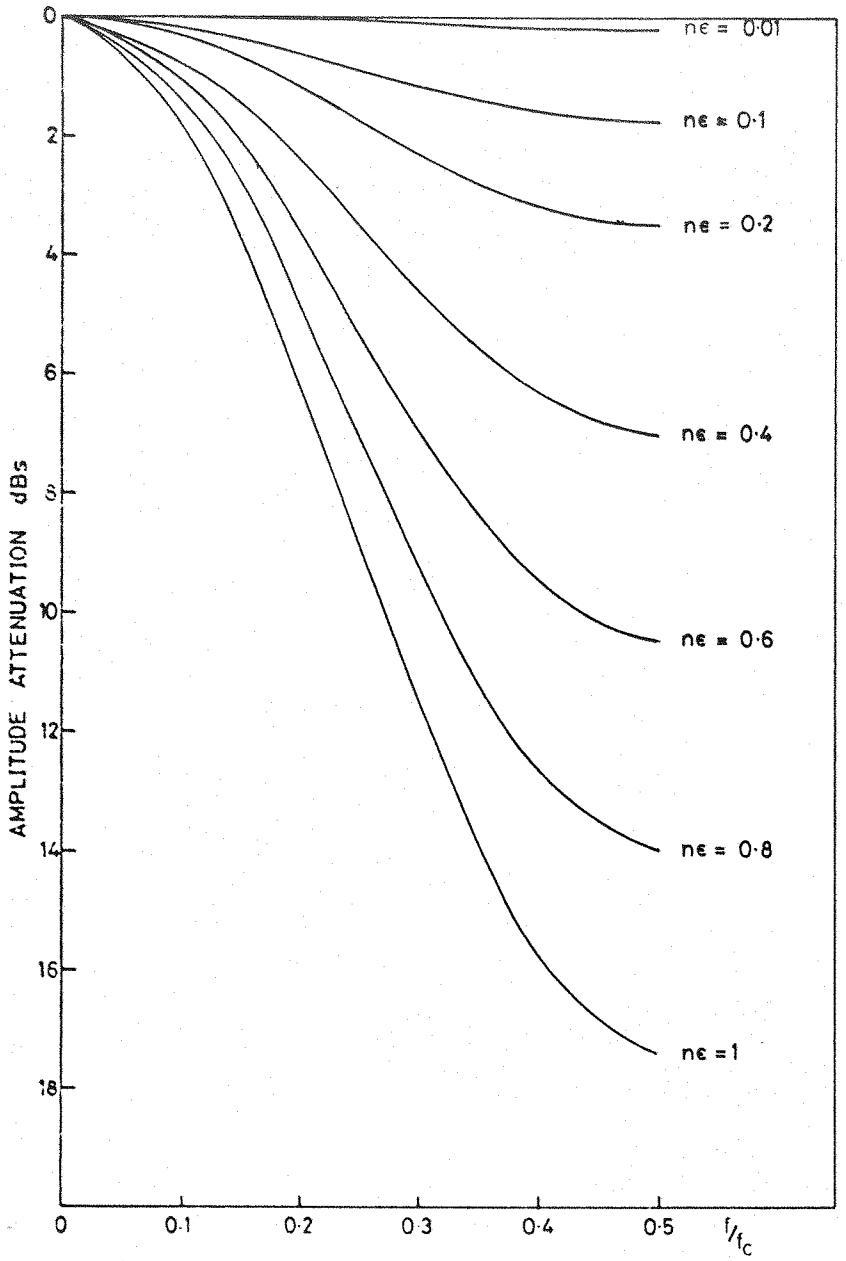
$$S(f) = \frac{4 N f_c}{q} \overline{\Delta Q^2}_{TR} (1 - \cos 2\pi f/f_c) \qquad 2.13$$

where ΔQ^2_{TR} is the mean square fluctuations introduced by each transfer process.

The dominant noise source in devices operated in the complete transfer mode is due to the fluctuations in the magnitude of charge released from the surface states, in particular those having re-emission time constants of the order of the available transfer time. These fluctuations have been shown to be[44]

$$\overline{\Delta Q^2}_{TR} = q\, kT\, A_s\, N_{ss}\, \ln 2 \qquad 2.14$$

where A_s is the area over which the surface states are filled (approximately the electrode area). There will be two fluctuations associated with each transfer, i.e. a fluctuation in charge trapped beneath the receiving electrode and a fluctuation in the charge



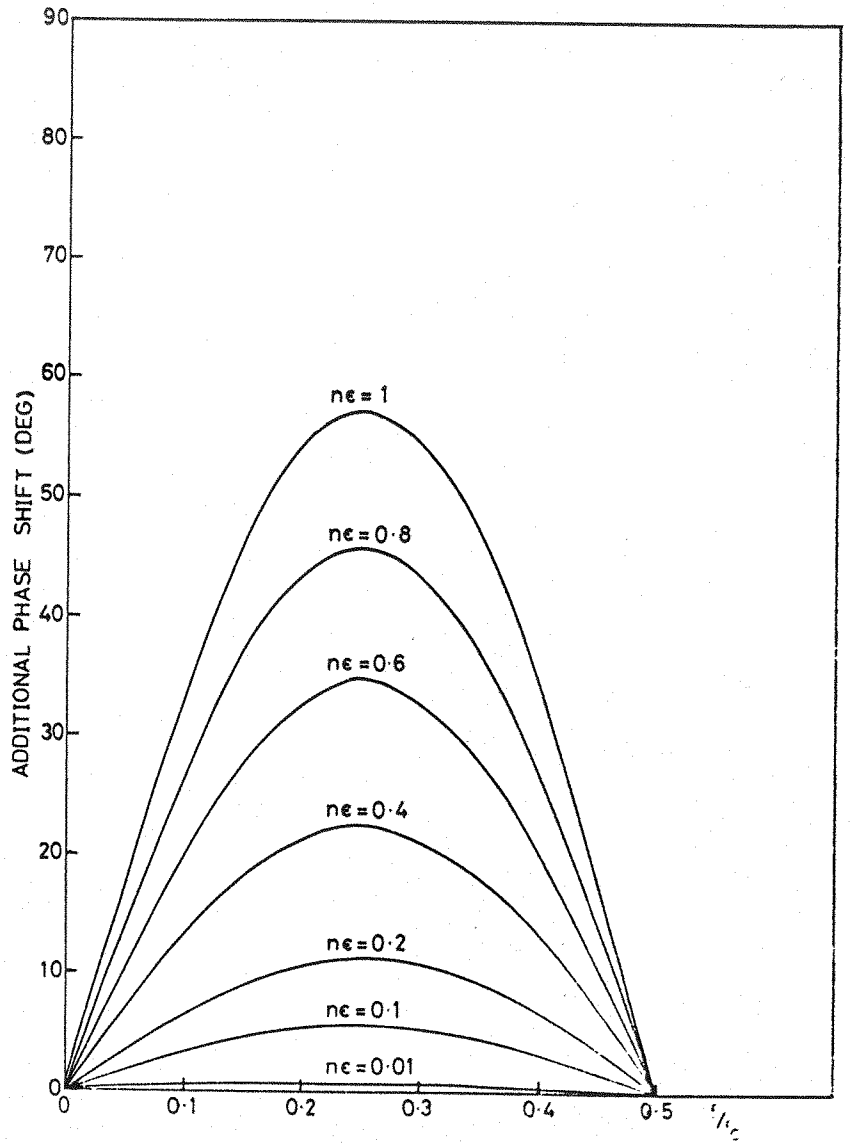


Fig 2.19 The amplitude and phase response of a CCD resulting from transfer inefficiency.

emitted from the states beneath the source electrode; these processes will be independent and so the total mean square fluctuations in a charge packet after Np transfers will be

$$\overline{\Delta Q^2}_S = 2Np\ \overline{\Delta Q^2}_{TR} \qquad 2.15$$

Whilst transfer inefficiency is an important parameter for many signal processing applications, constraints on device design to minimize this effect may be relaxed in certain cases. For instance, relatively high values of ε can be tolerated in CCD transversal filters, whereas CCD recursive filters and integrators are highly sensitive to this parameter. This important topic will be discussed in greater detail in the later Chapters of this thesis.

2.7 Dark Current Generation

Charge is stored in a CCD under non-thermal equilibrium conditions; consequently a maximum storage time exists before significant degradation of the signal charge occurs due to the accumulation of thermally generated carriers. The generation process is not only random but spatially non-uniform, and so in addition to the shot noise contributed to each charge packet, the CCD output shows a fixed pattern noise. The dominant source of this so-called 'dark current' is generation in the depleted region of the substrate and via mid-band interface states.[45] Both processes are highly temperature dependent and significant increases in storage times can be achieved by cooling the CCD. Different processing conditions also introduce a wide variation in dark current magnitude, and at present a considerable amount of work is being done to optimise fabrication procedures to consistently achieve low dark current densities. Indeed, close correlation of large dark current spikes with stacking faults in the CCD channel has already been observed[46] and CCDs fabricated with the appropriate processing sequence which includes carefully controlled annealing treatments have exhibited storage times of several seconds at room temperature.[47]

2.8 Summary

In this Chapter, the implementation of various CCD input and output configurations have been discussed. Emphasis has been placed upon performance limitations imposed by fabrication constraints, linearity, noise generation and transfer inefficiency. Although the CCD is conceptually a very simple structure, device layout, geometry, substrate material and driving mode play an important role in determining the signal processing performance. However, if attention is paid to these areas, performance comparable to that achieved with conventional digital techniques can be easily realized. For example, Table 1 shows the noise sources of a typical three-phase CCD structure containing 256 bits when operated at 1MHz. The table shows that the device has a potential dynamic range of ≈90dB. Non-linearities of less than -45dB have been obtained and the possibility exists of reducing this to -60dB.

Thus it can be seen that despite the inherent shortcomings of CCDs, they are a very competitive alternative to traditional signal processing techniques, particularly in view of their simple analogue storage capability. Some of the many and varied ways in which CCDs may be used for analogue signal processing will be described in the next Chapter.

Noise Source	Noise Equivalent Signal in SCCD
Electrical Insertion of Fat-zero	600-900(220*)
Electrical Insertion of Signal	600-900(220*)
Trapping Noise $N_{ss}=10^{9}cm^{2}eV^{-1}$	720
On-chip Amplifier Noise	180
Dark Current Noise for 1ms Delay	60
Total Noise	960(770*)
Maximum Signal	$40x10^{6}$
Dynamic Range	94dB*

Table 1. The RMS noise equivalent signal in electrons per charge packet. The values denoted by (*) are the theoretical figures given by $\sqrt{2/3kTC}$. The others are measured values.

CHAPTER THREE

THE APPLICATION OF CCDs TO ANALOGUE SIGNAL PROCESSING

3.1 Introduction

The implementation of many analogue signal processing techniques requires the realization of an accurate and sometimes variable time delay. It has already been indicated that a CCD fulfils to a large extent these requirements, since it provides direct analogue signal storage in the form of variable sized charge packets whose propagation from the input to the output can be accurately controlled by an external clock. Moreover, the small size of the devices allows a high storage density to be achieved with low power consumption. Consequently many signal processing functions have been identified for implementation with CCDs.*

Many types of CCD signal processor have been proposed and implemented, however, in this Chapter only those systems that are relevant to the work to be reported later will be discussed. First, the use of tapped CCD delay lines will be discussed, and then the use of the conventional serial in/serial out type of delay line will be described. Following this, some work carried out by the author to demonstrate the use of a serial CCD delay line in television signal processing will be presented.

3.2 Transversal Filters

A transversal filter[49] is a system in which the output is formed by summing weighted temporal samples of the input waveform; such a system is illustrated in figure 3.1a. By inspection of this figure, it can be seen that the output voltage is given by

$$V_{out}\ (KT_c) = \sum_{n=1}^{N} h_n\ V_{in}\ (KT_c - nT_c) \qquad 3.1$$

---

* It should be pointed out, however, that in some applications the efficacy of substituting CCDs for existing delay lines is debatable. For instance, the replacement of traditional simple glass delay lines in PAL colour television receivers with a CCD would probably result in a considerable increase in cost and circuit complexity.[48]

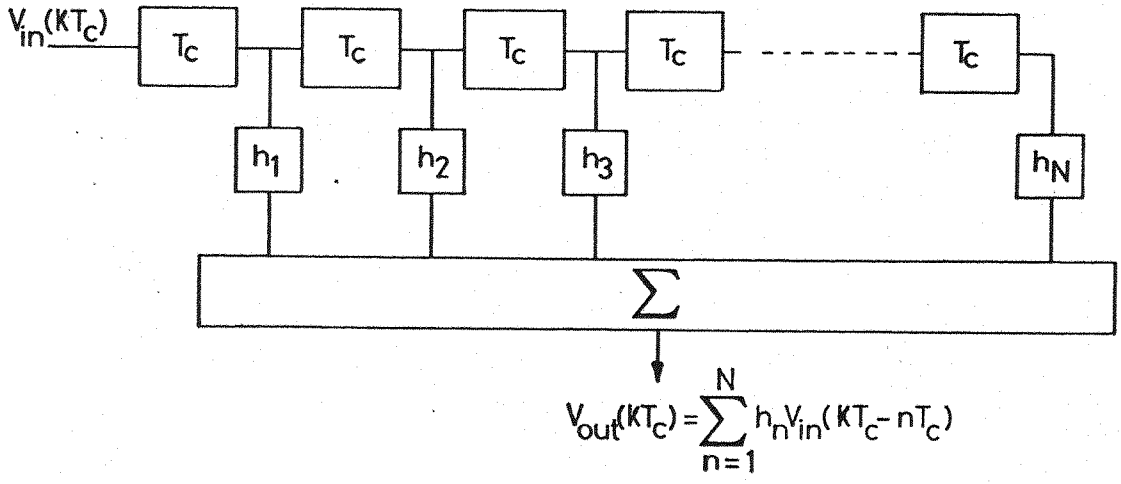


Fig 3.1a The implementation of a transversal filter.

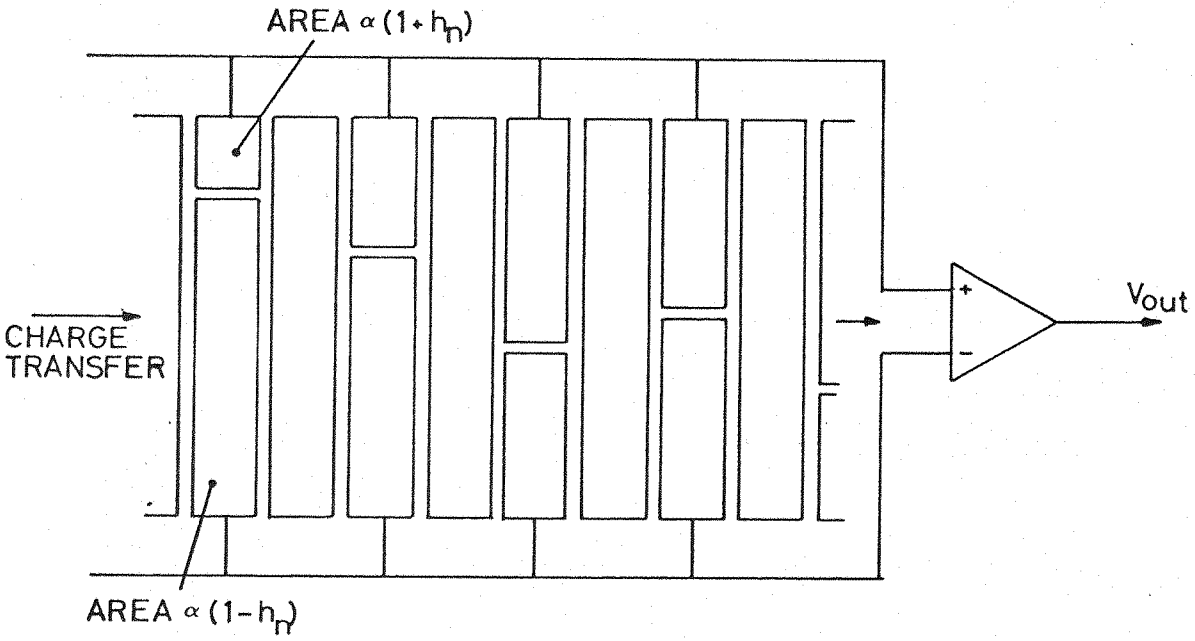


Fig 3.1b The split gate tapping technique.

where h_n is the weighting attached to each sample, T_c is the time delay of each stage, and K is an integer. If the waveform $V(KT_c)$ is clocked into a CCD at a rate f_c ($=1/T_c$) the samples V_{in} $(KT_c - nT_c)$ will be stored in adjacent bits of the device. Thus if the charge representing each sample is sensed non-destructively, a transversal filter providing any desired finite impulse response can, in principle, be realized to be appropriately weighting and summing the outputs of the sensing points. The large number of multiplications and subsequent summation may be carried out very simply using a modified form of either of the charge sensing techniques discussed in section 2.5.3 and 2.5.4 called split-gate tapping.[50] The technique involves splitting each sensing electrode at a point determined by the required tap weight (see figure 3.1b) so that the area of each section is in the ratio $(1 + h_n) : (1 - h_n)$. Summation is carried out by connecting each section to two separate bus bars which are common to the corresponding sections of the other sensing electrodes. The signals generated on these two bus bars are then differentially amplified to provide the filter output. The calculation of the tap weights to produce the desired filter response can be done easily using computer techniques, e.g. using the Parks and McClellan algorithm.[51]

The linearity of split-gate tapped transversal filters depends upon the type of charge injection scheme used and whether floating-gate voltage or current sensing is employed. A detailed analysis of the various configurations have been carried out by the author[52] and is reproduced in Appendix 2; it is shown that if a surface potential setting charge injection scheme (i.e. the diode cut-off scheme described in section 2.4.2) is used in conjunction with current sensing, a highly linear overall transfer response can be achieved. Unfortunately the diode cut-off scheme introduces a non-linearity due to charge partitioning. However, it may be possible to minimize this by careful design of the input section. Indeed, a transversal filter employing this configuration has demonstrated non-linearities of less than -45dB.[53]

The noise sources associated with CCD transversal filters are similar to those discussed in Chapter 2. However, the band-limiting effect of the filter allows a potential increase in signal-to-noise ratio at the output.

The disadvantages of split-gate tapping schemes are that the filter response is fixed by the chip artwork, and any tap weight inaccuracy caused by quantization errors in positioning the split along the electrode, mask misalignments, transfer inefficiency, or charge-hogging beneath the sensing electrodes[52] are difficult to rectify after fabrication. The effects of quantization errors can be reduced by using wide electrodes and if the magnitude of the transfer inefficiency is known, it is possible to pre-distort the tap weights.[50] However, a more versatile solution which enables adaptive filter systems to be designed is to use complete electrode taps individually amplified before summation. This enables the transfer function to be modified at will by appropriately programming the amplifier gains; furthermore, any variation in tap sensitivity, e.g. due to over-etching, can be compensated by trimming individual amplifiers. Several systems employing this idea have been described,[54,55] however, despite their versatility and the possibility of good linearity by employing feedback techniques the considerable increase in circuit complexity has severely restricted their development in favour of split-gate filter. Several authors have amply demonstrated the simplicity of this latter approach, including workers at Texas Instruments, who have fabricated a complete 800 stage CCD transversal filter containing sensing and clock-driving circuitry on a 5 x 3.5mm silicon chip.[56]

As well as being able to realize a simple filtering function with a CCD transversal filter, they may also be used in another important area of analogue signal processing - spectral analysis. Rather than use a bank of bandpass transversal filters for this purpose, a more elegant approach is possible; before discussing this, however, currently used spectral analysis techniques will be briefly reviewed. The most common method at present is to employ a

local oscillator to sweep the frequency band of interest. This method necessitates a continuously applied signal and the scanning time for high resolution in the frequency domain can be considerable. If the spectrum of a finite set of data samples is required, e.g. in radar Doppler processing, alternative techniques must be employed, and recently this has necessitated the use of digital processing with the fast Fourier transform (FFT) algorithm. Unfortunately such systems are inherently bulky, expensive, and may be too slow for real time applications. However, by restructuring the discrete Fourier transform (DFT)[57,58] the so-called chirp z-transform (CZT) can be derived in which the bulk of the spectral computations are carried out in the form of complex convolutions of the input signal with a set of fixed weights.

Inspection of figure 3.1 reveals that the output from a CCD transversal filter is the convolution of the input waveform with the tap weights; therefore by employing CCD transversal filters whose tap weights are defined according to the CZT implementation, a real time spectrum analyser can be realized with the additional attraction of low cost and size. Indeed, several CCD CZT spectral analysers have been reported,[53,59,60] demonstrating data rates as high as 1MHz[60] and frequency resolution as low as 1Hz.[53]

3.3 Recursive Filters

The facility offered by CCDs of accurate delay duration independent of signal frequency, ideally suit them to the implementation of recursive filters. These filters employ feedback and feedforward elements around delay stages to achieve an infinite impulse response. The generalized form of a Kth order recursive filter is shown in figure 3.2; and by adjusting the values of the feedback and feedforward coefficients, the filter characteristic can be altered with relative ease.

A three pole Chebychev filter designed by Bounden et al.[61] to investigate MTI filtering is shown in figure 3.3. Each delay

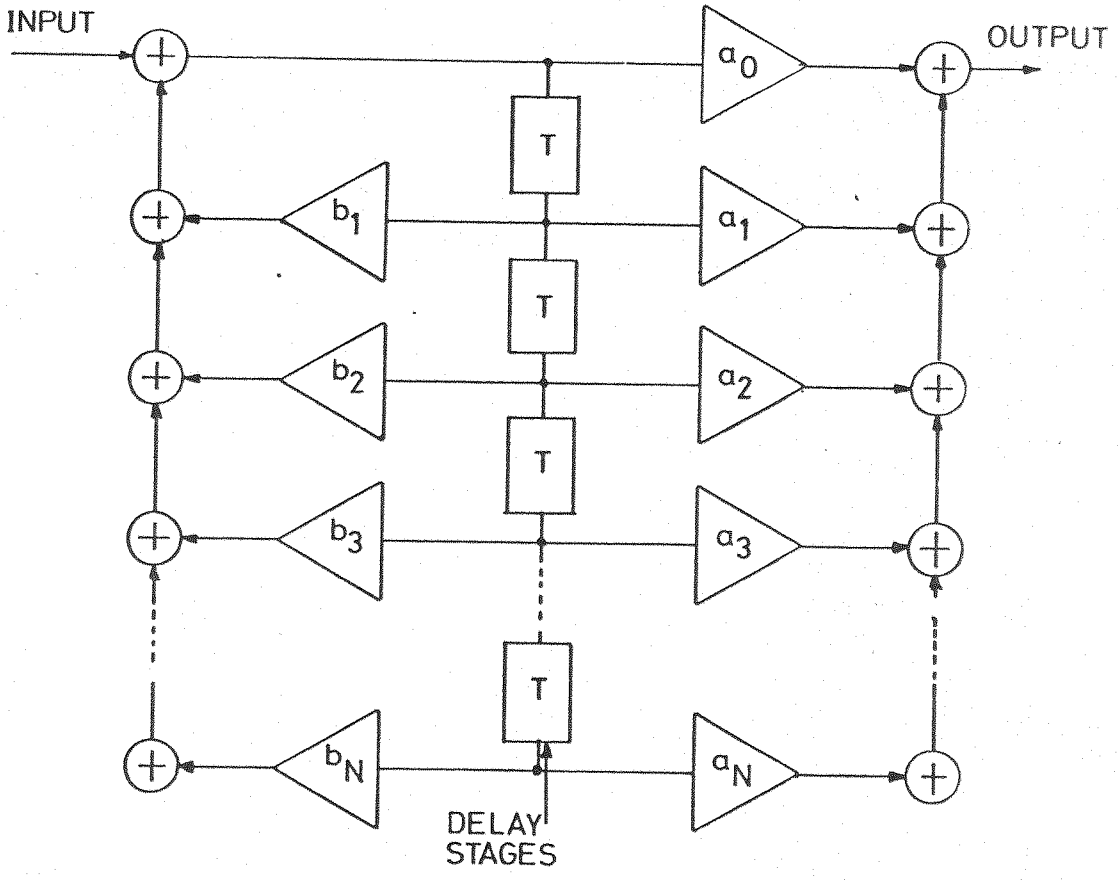


Fig 3.2 The generalized form of the Kth order recursive filter.

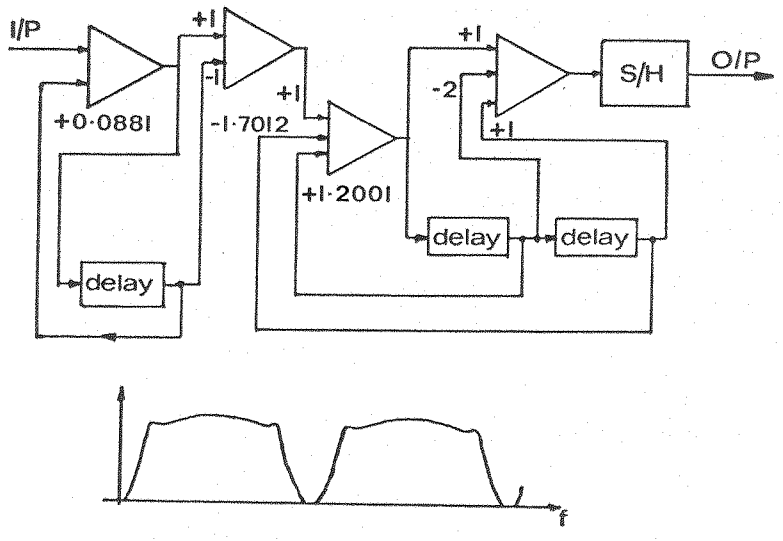


Fig 3.3 A three-pole Chebychev filter implemented with CCDs.

stage is an 8-bit three-phase CCD operated with an interrupted 330kHz clock to give a delay duration of 26μs. Response minimas occur at integral multiples of 38.4kHz with the first minima giving 32dB attenuation.

By setting all the feedforward and feedback coefficients, except $a_0 = 1$ and $b_1 < 1$, to zero, it is possible to realize a special case of the recursive filter, the recursive signal integrator. This has an important application in radar video processing where signal-to-noise ratio improvements can be obtained by integrating several successive returns as the antenna rotates, or when the noise is clutter, by integrating several successive returns from a single bearing. Since the CCD implementation of video integrators will be a major topic of concern in this thesis, further discussion of this application will be postponed until the later Chapters.

As mentioned in section 2.6, charge transfer inefficiency causes a more noticeable departure from the designed response of recursive filters than transversal filters. This is due to the build-up of charge residuals as the signal recirculates through the delay lines via the feedback elements. By utilizing the z-transform analysis of a CCD delay line exhibiting charge transfer inefficiency,[62] it can be shown[63] that transfer inefficiency increasingly modifies the filter coefficients with increasing signal frequency. Two terms are involved; the first introduces a frequency independent modification which could be compensated for by simply introducing it into coefficient. The second part is, however, frequency dependent and causes a significant disparity between the measured and predicted performance as the ratio between the signal frequency and the clock frequency increases.[63] In particular, the maximas suffer an increasing attenuation with increasing signal frequency, and the nulls and peaks shift towards lower frequencies. This disparity has been observed[63,64] and relatively good agreement between the measured frequency response and that predicted using the z-transform analysis has been obtained.

Several methods have been suggested to reduce the sensitivity of recursive filters to transfer inefficiency, but discussion of these will be delayed until a later Chapter.

3.4 Time Axis Conversion

The temporal spacing of the samples of an analogue signal stored in a CCD is dependent solely upon the frequency of the clock waveform. Thus the bandwidth and duration of a signal can be altered if it is clocked into a CCD at one frequency and the device is emptied at a different frequency.

Several applications of this fairly novel facility of time axis conversion have been identified and demonstrated. These applications include the correction of speed errors in video-tape recorders, correction of speeded up speech signals from tape recorders,[65] transient data recording[67] and signal multiplexing.[68,69] This technique has also recently been used to adjust the time duration and bandwidth of a radar signal for subsequent processing with surface acoustic wave (SAW) spectrum analysers,[5] and also in sonar beamforming.[70]

Although CCDs may be operated in this differential-clock mode in a fairly straightforward manner, certain aspects merit some attention. For instance, the presence of dark currents may produce a significant fixed pattern noise in the output signal. Consider first fixed clock CCD operation; the time allowed to accumulate charge in each charge packet propagating along the device is constant, thus the dark currents merely contribute a DC level and shot noise to the signal. If, however, the clock is suddenly increased and is sufficiently high, the spatial distribution of the dark current generation sites will tend to be 'frozen' into the output waveform and thus will constitute a fixed pattern noise. This situation can be improved by ensuring that the low clock frequency is such that a relatively insignificant amount of charge accumulates in each packet, thereby reducing the magnitude of the resulting fixed pattern noise.

Another consideration of this mode of operation is that if there exists a fairly large interelectrode capacitance due to overlapping electrodes, then the increase in clock frequency will also result in an increase in clock noise feedthrough, as discussed in section 2.4.

3.5 A Feasibility Study on the Application of CCDs to TV Broadcasting

3.5.1 Introduction

To provide experience of using CCDs in analogue signal processing, the feasibility of applying CCD time axis conversion to a TV system was studied. The concept of the scheme, which was proposed by the Independent Broadcasting Authority, is as follows. During the transmission of TV programmes to relay stations, or during communication between TV cameramen and the control room, the audio and video information are sent on two completely separate channels. However, approximately 17 redundant scan lines exist at the beginning of every half-frame period, and so the possibility arises of employing this unused time interval for transmitting the audio signal, provided it can be suitably processed.

Consider a single TV line; approximately 50μs are available for data insertion. The half-frame period is 20ms, so if during transmission the audio is sampled over this period and time compressed by a factor of 400, provided the resulting bandwidth of the compressed audio is not greater than the video bandwidth, it can be inserted into one of the redundant lines. By reversing this procedure at the receiver, the audio signal can be restored. As discussed already, the CCD is ideally suited to the implementation of a time axis conversion facility.

3.5.2 The Specifications

The video bandwidth of present TV transmissions is 5.5MHz, so the inserted information must not exceed this limit. Consequently

if a single scan line is used to carry the audio sampled during the previous half-frame period, the maximum audio frequency is 13.75kHz (if two lines are employed, then the maximum frequency would be 27.5kHz, well in excess of the present audio frequency bandwidth of 15kHz). During the compression cycle 50μs of audio information is lost, but this is a negligible fraction ($^1/400$) of the total sample period and so only one CCD would be required. The storage capacity of the CCD can be determined from the product of the clock frequency (governed by the Nyquist sampling criterion) and the total sample period. Using the figures presented above, a CCD with a minimum of 550 bits is required.

3.5.3 Specifications for the Feasibility Study

A 550 bit CCD is required in a system demonstrating full broadcasting capability, in order that a full audio bandwidth signal may be acquired during a half-frame period. However, a CCD of such capacity is not required in order to demonstrate time axis conversion. In fact the largest CCD available to the author at the time of the study contained only 39 bits, thus imposing a restriction on the audio bandwidth and read-in interval, nevertheless the feasibility of using CCDs in such an application could still be investigated. It was also decided to reduce the maximum clock frequency to 1MHz since, although the device was capable of operating at 11MHz, the lower frequency would simplify the initial evaluation of the prototype circuit. To partially offset the resulting decrease in time compression factor, the minimum clock frequency was reduced to 14kHz yielding a time compression factor of ≈71. The read-in and read-out times during the compression cycle are thus 2.8ms and 39μs respectively.

3.5.4 The CCD Peripheral Circuitry

The 39 bit CCD used in this study (see figure 3.4) was a two-phase stepped oxide device fabricated using the self-aligned gap technique.[7] It was operated in the 1½-phase mode with the gate of the reset transistor connected externally to the ϕ_1

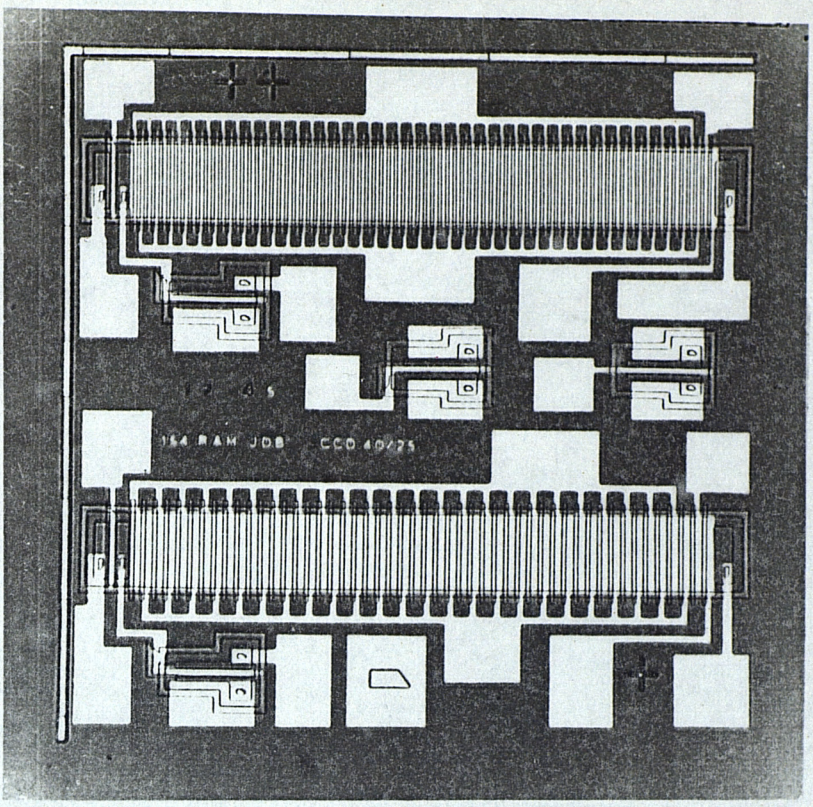


Fig.3.4 Photomicrograph of the chip used for the feasibility study.The 39-bit device is at the top of the picture.

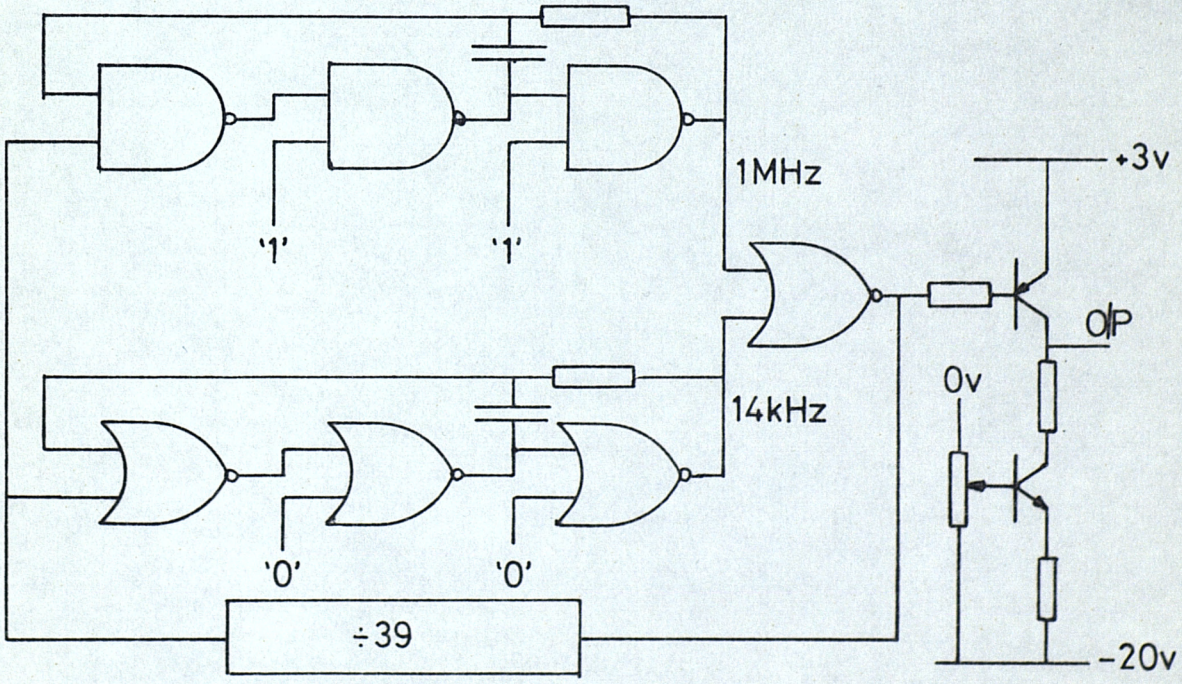


Fig 3.5 The circuit used to generate 39 clock pulses alternately at 14kHz and 1MHz.

electrodes. The clock pulse generator was required to generate 39 pulses alternately at 14kHz and 1MHz. The frequency generators were designed using standard TTL NAND and NOR gates, as shown in figure 3.5. This implementation enables the transition between frequencies to be made very easily; the NAND gate circuit will only oscillate if all unused inputs are at logic '1' and conversely for the NOR circuit. Hence if the unused inputs of each generator are appropriately connected, control over the output frequency can be exercised simply with a binary input. The control bit is provided by a counter whose output alternates between logic levels every 39 input pulses. The discrete transistor circuit in figure 3.5 amplifies the resultant pulses to the required magnitude to drive the CCD.

Since the feasibility study was to include an investigation of both the compression and subsequent expansion of the audio signal, simulation of the transmission channel was also required. This would cause bandlimiting of the output from the CCD; i.e. the sampled data nature of the output waveform would be interpolated to a 'smooth' signal. This was simulated in the investigation by a simple low-pass active filter with a cut-off frequency at approximately 500kHz.

In order that noise from the compression system, the majority of which would be part of the audio signal stored in the CCD during the application of the high clock frequency, is not added to the video information, the compressed audio signal must be applied to the video circuits via a gate properly synchronized to the line frequency. The circuits required to achieve this were not investigated at this stage, but instead the audio signal could be set to zero prior to being applied to the CCD. This facility was provided in the circuitry of the signal source used to generate the audio waveform; this arrangement realized the additional advantage of improving the trace synchronization on the monitoring oscilloscope.

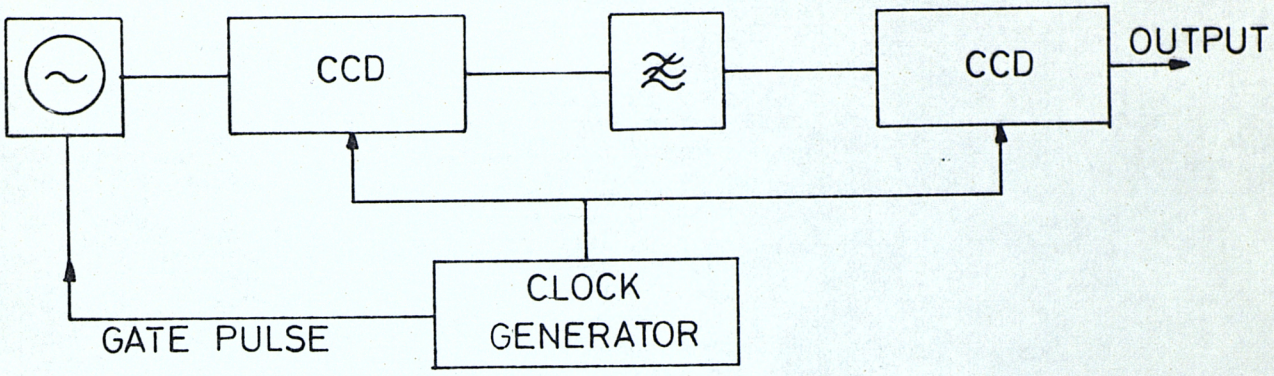


Fig 3.6 The experimental set up of the feasibility study.

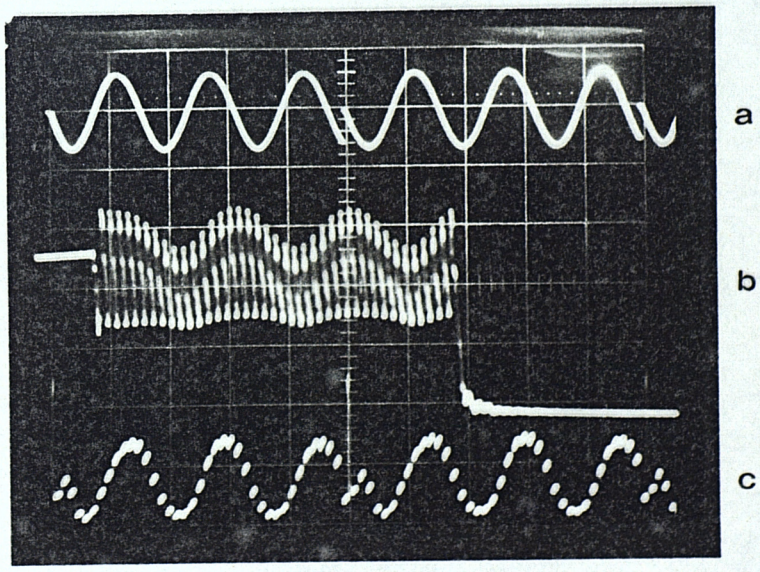


Fig 3.7 An oscillograph of the signal at various parts in the circuit.

(a) The input waveform. 0.56 ms/horiz.div.

(b) The compressed, unfiltered output from the first CCD. 6.5 μs/horiz.div.

(c) The signal restored to its original time duration. 0.56 ms/horiz.div.

Figure 3.6 shows the experimental arrangement for the feasibility study. In order to simplify the synchronization of the read-in and read-out cycles of the two CCDs, the same clock generator was used to drive both devices.

3.5.4 Results

The performance of the circuit for compression and subsequent expansion of an audio frequency sine wave is illustrated in figure 3.7, which comprises a series of photographs of the signal taken at various points in the circuit. The trace (a) shows the gated input signal; trace (b) shows the unfiltered output from the first CCD on an expanded time-base. The input signal has undergone time compression by a factor of 71; trace (c) shows the output of the second CCD where the input signal has been restored to its original time duration. Although no quantitative measurements of noise and linearity were made at this stage, the analogue performance of the system seems highly acceptable. (Haken subsequently reported measurements on the input technique used in the CCDs showing it to be very linear.[18])

3.5.5 Conclusion and Further Work

The preliminary investigations on the experimental circuit reported above establish the feasibility of using CCDs for time axis conversion in a TV system. Furthermore, the ease with which a two-phase CCD may be operated with just a single clock waveform is demonstrated.

Unfortunatley due to lack of financial support, the project had to be terminated at this stage, so no further experimental work was undertaken which would have determined the noise performance and linearity of the CCDs when operated in the differential-clock mode. Although the circuit was designed to a restricted specification, larger CCDs are currently available, and the implementation of a full broadcast-compatible system using a 22 x 25 bit serial-parallel-serial CCD array to reduce the effects

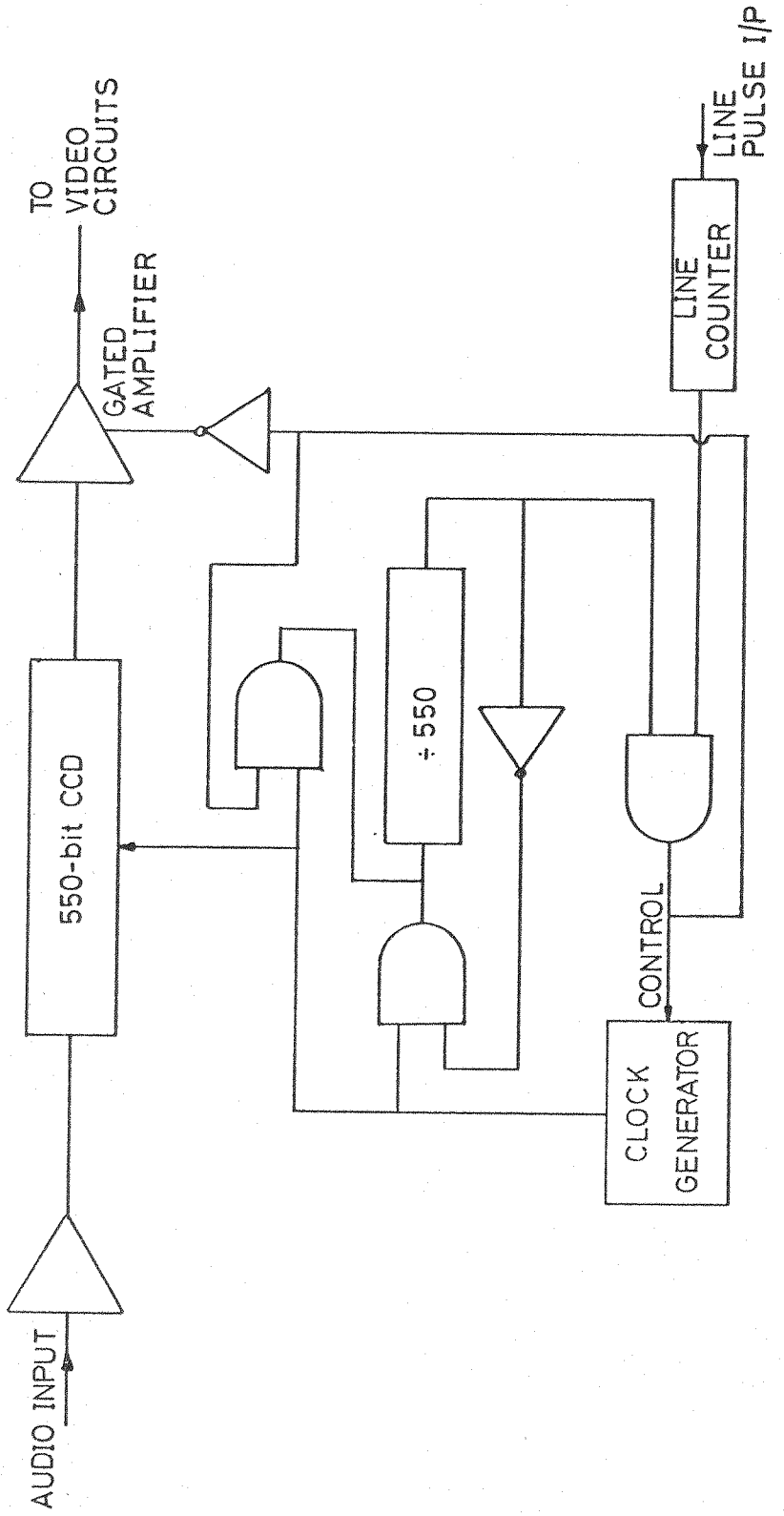


Fig 3.8 The circuit of the proposed TV system.

of transfer inefficiency would be straightforward. It is proposed that the circuit of figure 3.8 might be used for the insertion of the compressed audio on to the correct line, with a similar arrangement at the receiver. Several clock generation schemes for a full broadcast system have also been considered. The first uses existing high accuracy frequency sources within the TV system; the line scan frequency (15.625kHz) and the colour subcarrier (4.434MHz) both suitably scaled could provide the low and high clock frequencies. Alternatively, if the compressed audio is distributed over three scan lines, then the high clock frequency falls within the video bandwidth and could therefore be transmitted. Detection and processing of this frequency would provide the read-in clock at the receiver.

In conclusion, it is felt that such a CCD signal processing scheme could readily be used in a TV system with significant advantages over alternative, e.g. digital, implementation.

3.6 Summary

A small number of CCD implementations of the many possible signal processing systemshave been discussed in this Chapter. The simplification of system design and the reduction in component count made possible by the analogue storage capability of the CCD is perhaps most significant, but in addition the substantial reduction in cost, bulk and power consumption of complete processors over alternative implementations is also attractive.

In the remaining Chapters, the application of CCDs to one specific radar signal processing task will be described in detail, i.e. the signal integrator. Signal integration is first described in detail and then the significant problem of transfer inefficiency effects associated with existing CCD implementations is discussed. Finally, a novel CCD architecture is described that substantially reduces this problem and some preliminary results are presented.

CHAPTER FOUR

THE DETECTION OF TARGETS IN SEA CLUTTER

4.1 Introduction

A significant difficulty encountered in many radar systems is the detection of a genuine target echo in the presence of spurious echoes. These spurious echoes are termed 'clutter' and may be caused by either single point scatterers (isolated clutter targets), e.g. an electricity pylon or water tower, or a cluster of many individual scatterers (composite clutter targets) which is characteristic of most sea and ground clutter, chaff and meteorological echoes. Composite clutter targets are most troublesome, however, since they more readily obscure the genuine target echoes.

In marine applications, the detection of small targets at or near sea-level is seriously limited by the presence of sea clutter; thus a considerable amount of work has been done to characterize sea echoes and so improve target detection. It has been found that the strength of sea clutter returns depends upon such factors as the depression angle, wavelength and polarisation of the transmitted beam, the sea state and wind direction. Although several mechanisms have been proposed to explain sea echoes[71,72,73] none wholly explains the dependence on the above factors. However, for the purposes of clutter reduction, it is sufficient to know only its statistical nature. The model most commonly used for theoretical analysis assumes a large number of independent scatterers within the radar resolution cell;[71] the variation of clutter amplitude can then be defined by the Rayleigh probability distribution given by

$$P(x)\,dx = \frac{2x}{\sigma^2}\exp\left(\frac{-x^2}{\sigma^2}\right)dx \qquad 4.1$$

where σ is the r.m.s. value of the clutter amplitude and the mean

level is

$$\bar{x} = \frac{\sigma}{2}\sqrt{\pi} \qquad 4.12$$

The decorrelation time of sea clutter has been established to be approximately 100ms.[74]

4.2 Clutter Reduction

There is a variety of ways of processing cluttered radar returns in order to improve target detection, and some of the more important techniques will be considered below.

4.2.1 Moving Target Indication (MTI)

This method relies upon the Doppler shift of an echo from a moving target. The return signal is mixed with the transmitted frequency and the moving target shows as an amplitude variation at the Doppler frequency; the Doppler component can then be extracted by filtering. This can be carried out using either a simple delay line canceller or a circuit such as shown in figure 3.3 which gives a more uniform response in the passband, thus yielding a more uniform detection probability. These relatively simple cancellers unfortunately suffer from the fact that certain target speeds (i.e. corresponding to the notches in the filter characteristic) are undetectable, and so more complex schemes are necessary to overcome this problem. Moreover, targets stationary relative to the transmitter cannot be detected with this system.

4.2.2 Matched Filtering

A matched filter is a network, the transfer response of which maximizes the peak signal-to-mean-noise (power) at the output for a given input waveform, and so provides optimum detection of signals in noise. It is evident that the required transfer response of a matched filter will depend upon the signal waveform

and the power spectrum of the noise. Urkowitz[75] has discussed the implementation of a matched filter for the detection of targets buried in clutter which can be described by the Rayleigh model. Under these conditions the power spectrum of the clutter will be the same as that of the transmitted pulse,[76] and he has shown that a matched filter for clutter rejection should have a transfer response proportional to the transmitted spectrum.* The realization of matched filters is considerably eased by the use of CCDs, as described in Chapter 3. However, if the signal or the clutter spectrum change, e.g. due to motion relative to the radar set, target detection ability will be impaired.

4.2.3 Signal Integration

The clutter associated with radar returns will vary in a random manner from sweep to sweep. However, a genuine target will produce a periodic signal, and so the summation of successive returns from a single bearing will lead to an increase in signal-to-clutter ratio. Probability theory states that the variance of the sum of independent probability distributions is the sum of the variances. The variance of sea clutter, σ^2, is simply the mean square amplitude fluctuations; thus the r.m.s. clutter amplitude of the sum of m returns will be $m.\sigma$ (assuming that the sweep period is longer than the clutter decorrelation time). Since the target amplitudes will add linearly, a $\sqrt{m}$ increase in signal-to-clutter ratio can be realized by summing m returns.

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* Whilst the derivation of Urkowitz's result seems reasonably clear, the author does not understand the physical processes of clutter rejection with a matched filter; having read the relevant references and having had lengthy discussion with radar experts, the following problem remains unresolved: Each radar return is processed individually by the matched filter, i.e. previous returns do not affect the output voltage unlike an MTI processor. Implicit in Urkowitz's derivation is that the clutter and the target are stationary; consequently there will be no Doppler shift or other effect that will distinguish a reflection due to a clutter scatterer from the reflection due to a target in the same resolution cell. Hence the target could be considered as simply another clutter scatterer thus, upon reception of the composite echo, upon what criterion does the matched filter enhance only the target reflection?

A signal integration system is potentially the most useful clutter reduction scheme since it is not sensitive to the received target or clutter waveforms, i.e. both stationary and moving targets can be detected without impairing target detection ability* and any additional noise source, provided it is decorrelated (such as receiver noise), can easily be accommodated.

Various integration schemes have been tried using long persistence CRTs and photographic integration. Unfortunately, both these methods are somewhat cumbersome and a more versatile system would be one that employed delay line storage techniques. However, until recently the implementation of a delay line of duration greater than 100ms has been difficult. For example, analogue magnetic tape storage and digital systems tend to be bulky and expensive - undesirable attributes for small marine radar sets. Furthermore, the delay duration of the comparatively simpler tape storage system is unstable and difficult to synchronize with the radar sweep period. On the other hand the CCD, as indicated before, has many features that make its use in a signal integrator highly attractive; i.e. apart from its simple analogue storage capability, storage times in excess of several seconds are potentially realizable, and accurate synchronization of the delay duration with the sweep period of the antenna is possible.

In view of this, it was decided to investigate the application of CCDs to signal integration in greater detail; however, before discussing this approach the basic methods of integrating signals with delay lines will be considered.

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* This is true provided the target does not move completely out of a range bin during the period required to integrate 'm' returns, e.g. for 15m range bins, m = 10 and a minimum decorrelation time of 100ms, the maximum radial speed of the target relative to the transmitter would be ≃ 30mph. A system that enables maximum integration improvements on targets that violate this condition will be proposed in Chapter 10.

4.3 Methods of Implementing a Delay Line Signal Integrator

The simplest form of delay line signal integrator is the non-recursive integrator shown in figure 4.1; (m - 1) delay lines are connected in cascade, each with a delay equal to the sweep period, T. Thus by summing the outputs of each delay line an integration improvement, defined as the increase in signal-to-clutter ratio, can be achieved; if ρ consecutive returns containing the target signal are received, the integration improvement in dBs, I_N, will be

$$I_N = 20 \log \frac{\rho}{\sqrt{m}} \qquad 4.2$$

However, since a maximum of only m returns can be integrated, $I_N \leqslant 20 \log \sqrt{m}$.

Whereas a non-recursive integrator forms a sum of equally weighted returns, it requires (m - 1) delay lines; an integration technique requiring only one delay line is the recursive integrator which forms the exponentially weighted sum of all the past returns (see figure 4.2). In this system a fraction of the output from a delay line of duration T is fed back to be summed with the next radar return. The integration improvement obtained with this system can be derived as follows. If the gain of the feedback amplifier is k, then for ρ returns containing a unity target signal, the output signal, S_R, will be given by

$$S_R = 1 + k + k^2 + k^3 + \ldots\ldots k^{\rho} = \frac{1 - k^{\rho}}{1 - k} \qquad 4.3$$

If it is assumed that an infinite number of cluttered waveforms has been applied to the system, as will usually be the case, the r.m.s. clutter amplitude, N_R, at the output will be given by the infinite series

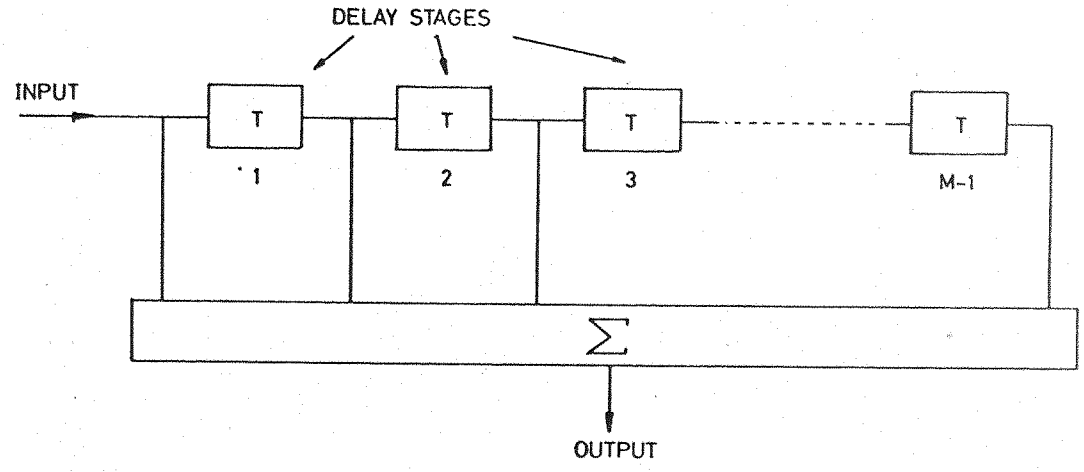

Fig 4.1 The implementation of a non-recursive integrator employing delay lines.

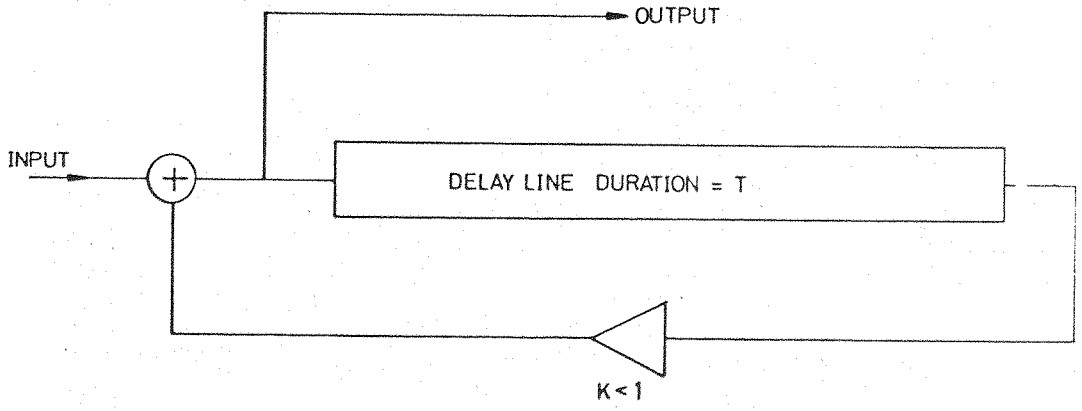

Fig 4.2 The non-recursive integrator using a single delay line.

$$N_R = \sigma\left[1 + k^2 + k^4 + k^6 + \ldots\ldots\right]^{\frac{1}{2}} = \sigma\left(\frac{1}{1 - k^2}\right)^{\frac{1}{2}} \qquad 4.4$$

Thus the integration improvement, found by combining equations 4.3 and 4.4 is

$$I_R = 20 \log \left(1 - k^{\sigma}\right)\left(\frac{1 + k}{1 - k}\right)^{\frac{1}{2}} \qquad 4.5$$

It is useful when considering recursive integration, to determine the effective number of input signal waveforms forming the integrated output signal. This can easily be derived by allowing $\rho \to \infty$ in equation 4.3. The output signal amplitude thus becomes

$$S = \frac{1}{1 - k} \qquad 4.6$$

By comparing this with the signal output from a non-recursive integrator, the effective number of integrated waveforms is seen to be $1/(1 - k)$. In the following discussions this quantity will also be designated by the letter m.

Equations 4.2 and 4.5 are plotted in figure 4.3 for $m = 10$, in order to compare the clutter reduction performance of the two schemes. It can be seen that if ρ is either small or large compared with m, the recursive integrator gives greatest improvement, but if $\rho \simeq m$ then the non-recursive system is better. This is because the latter system sums equally weighted returns to a maximum of only m, whereas the output from the recursive integrator is formed from the weighted sum of all the past returns.

The recursive integrator appears to be the best implementation since in general, a slightly larger integration improvement may be achieved; furthermore, this parameter may be easily varied by adjusting k. However, if m is required to be large, i.e. $k \simeq 1$, restrictions will be imposed upon the input dynamic range, and problems of instability may arise. Thus if large integration

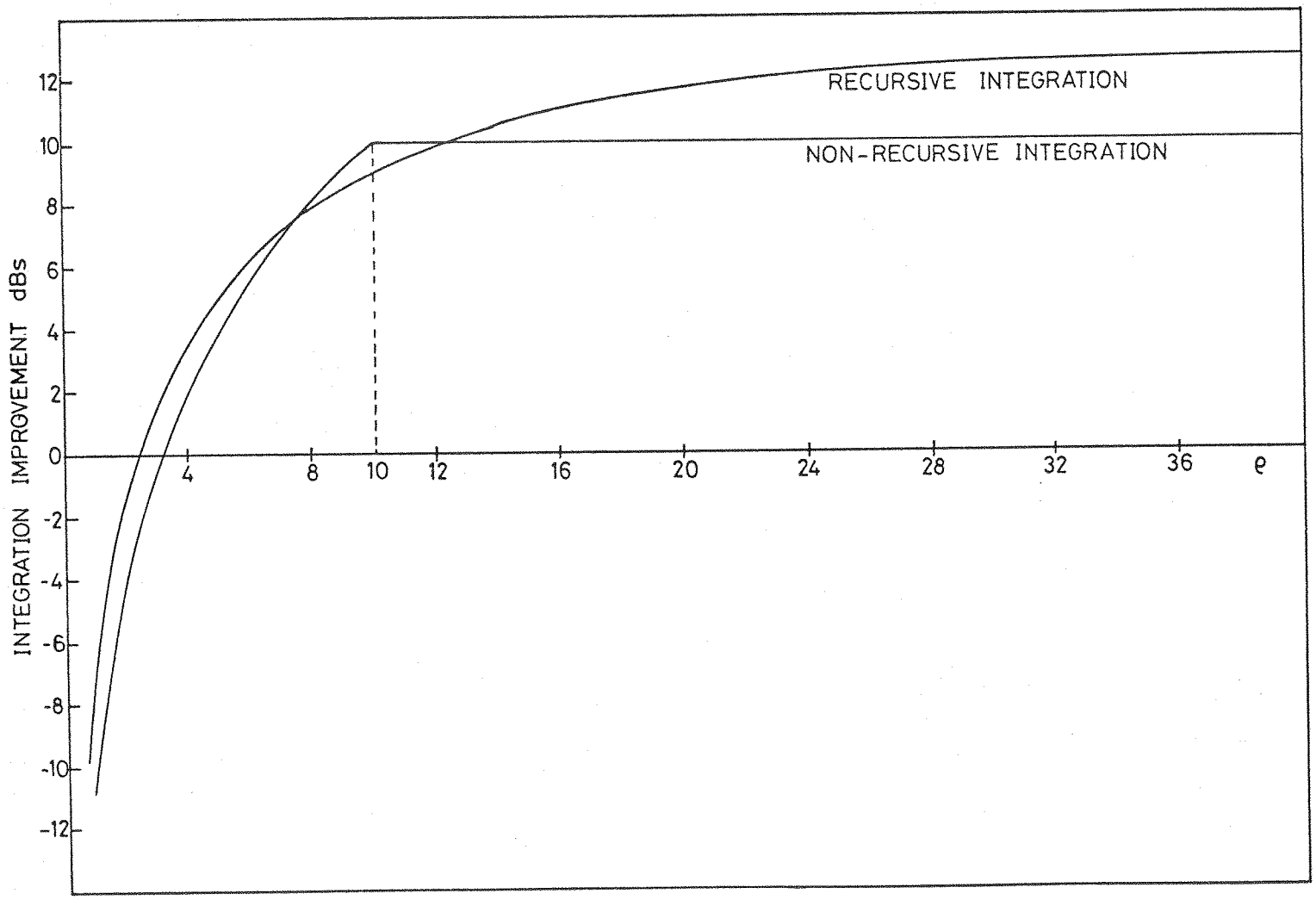

Fig 4.3 A graphical comparison of the integration improvement obtainable with non-recursive and recursive integration as a function of received target waveforms. In this case m = 10.

improvements are required, the use of a non-recursive system would be more appropriate.

In the next section the implementation of a signal integrator with CCDs will be described; in particular, the performance limitations imposed by transfer inefficiency and methods of mitigating its effects will be described.

4.4 CCD Implementation of Radar Video Integrators

The implementation of the delay lines in the signal integrators described in the last section with conventional (i.e. serial) CCDs is conceptually straightforward and has much to commend it. However, in a practical system, the large signal-to-clutter ratio improvements predicted by the simple equations 4.2 and 4.5, by employing large integration sample sizes, cannot be achieved. The reason for this is that spurious or residual signals caused by transfer inefficiency build-up after relatively few transfers to a level comparable with the clutter amplitude, thus making any further attempts to improve target detection by integration impossible.

In this section, the simple equations will be modified to account for the effects of transfer inefficiency, thus enabling realistic estimates of integration improvements to be made.

The non-recursive integrator is considered first of all. If the transfer inefficiency of the CCD delay line is ε, we can define a parameter α (= 1 - ε) as the charge transferred forward per transfer (we assume that no charge is permanently lost due to trapping or recombination). If the CCD is a p-phase device containing N-bits, the signal level after Np transfers will be a fraction α^{Np} of the input amplitude. For practical values of $Np\varepsilon(<0.1)$, only the first trailing charge is significant,* and will

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* Chowaniec and Hobson[77] have carried out a more rigorous analysis of transfer inefficiency effects in recursive video integrators, taking into account the second trailing charge packet. However, for the argument presented here, consideration of only the first trailing charge is sufficient.

be a fraction approximation $1 - \alpha^{Np} \simeq Np\varepsilon$ of the input signal. Thus, for m unity input signals, the output signal from a non-recursive integrator containing (m - 1) CCD delay lines will be given by

$$S_N = 1 + \alpha^{Np} + \alpha^{2Np} + \ldots\ldots \alpha^{(m-1)Np} = \frac{1 - \alpha^{mNp}}{1 - \alpha^{Np}} \qquad 4.7$$

The residual signal, R_N, due to the summation of the trailing charges will be

$$R_N = Np\varepsilon + 2Np\varepsilon\alpha^{Np} + 3Np\varepsilon\alpha^{2Np} + \ldots\ldots (m-1)Np\varepsilon\alpha^{(m-2)Np}$$

$$= Np\varepsilon \left[\frac{1 - \alpha^{(m-1)Np}}{(1 - \alpha^{Np})^2} - \frac{(m-1)\alpha^{(m-1)Np}}{1 - \alpha^{Np}} \right]$$

$$\simeq (m-1)^2 Np\varepsilon \qquad 4.8$$

The dynamic range at the output, D_N, is therefore

$$D_N = 20\log \left[\frac{1 - \alpha^{mNp}}{1 - \alpha^{Np}} - \frac{1}{(m-1)^2 Np\varepsilon} \right] \qquad 4.9$$

$$\simeq 20\log \left[\frac{m}{(m-1)^2 Np\varepsilon} \right] \qquad 4.10$$

If a range resolution of 15m is required, and N = 100, the overall range will be 1.5km. Choosing m = 10, p = 2 and $\varepsilon = 10^{-4}$ (a state-of-the-art figure for SCCDs), the dynamic range will be only 15.8dB.

A similar analysis for the recursive integrator may be carried out, as follows. For an infinite number of unity input signals the output signal, S_R, is given by

$$S_R = 1 + k\alpha^{Np} + (k\alpha^{Np})^2 + (k^{Np})^3 + \ldots\ldots$$

$$= \frac{1}{1 - k\alpha^{Np}} \qquad 4.11$$

The residual R_R will be

$$R_R = kNp\varepsilon\left[1 + 2k\alpha^{Np} + 3(k\alpha^{Np})^2 + \ldots\ldots\right]$$

$$= kNp\varepsilon\left[\frac{1}{(1 - k\alpha^{Np})^2}\right] \qquad 4.12$$

Thus the dynamic range at the output of the recursive integrator, D_R, will be

$$D_R = 20\log\left[\frac{1 - k\alpha^{Np}}{kNp\varepsilon}\right] \qquad 4.13a$$

From equation 4.11 it can be seen that the occurrence of incomplete transfer causes a modification of the effective number of waveforms integrated. However, by adjusting k, we can arrange that

$$1/(1 - k\alpha^{Np}) = m.$$

Thus we can write

$$D_R = 20\log\frac{1}{mkNp\varepsilon} \qquad 4.13b$$

By substituting the previously used parameters into equation 4.13b, i.e. N = 100, p = 2, m = 10 and $\varepsilon = 10^{-4}$, the dynamic range can be calculated to be 14.7dB, which is slightly less than can be achieved with the non-recursive system. Clearly a dynamic range of this order is much too small.

Thus it can be seen that the performance of an integrator employing a simple serial CCD delay line is severely restricted by the effects of transfer inefficiency. The limitation clearly becomes more serious for larger values of m, N and ε.

Several methods have been suggested for reducing the sensitivity of CCD integrators to transfer inefficiency:

(i) The input signal could be sampled once every two clock cycles, in order to separate the data in the CCD by initially empty bits. As the integration proceeds, a spurious signal will build up but will reside predominantly in the 'empty' bits. Thus at the output, the signal could be partially restored by summing the genuine charge packet with its residual. Alternatively, the nominally empty elements could be set to zero periodically to prevent the build-up of a third trailing charge.[77] However, both these schemes have the disadvantage that storage area is wasted, and the CCD must be clocked at twice the desired data rate.

(ii) Another approach could be to delay a fraction of the output signal for a clock period and subtract it from the next output. If the fraction is chosen correctly, then the residuals will tend to cancel.[77]

(iii) A variation of the approach in (ii) has been described by Cooper et al.[78] for a recursive integrator. In this scheme the input to an N-bit CCD is multiplied by a code cycling through three values every (N + 1) clock period. By correctly decoding the output, it is possible to cancel the residuals. Although this works reasonably well, it has some disadvantages. The radar video signal normally applied to an integrator is unipolar. However, the code generates a bipolar signal which consequently must be handled by the CCD, thus necessitating a reduction in the dynamic range of the input signal. Furthermore, the coding and decoding circuitry must be stable and all units must be DC coupled.

All the techniques just described attempt to suppress the residual signal once it has been generated. Obviously a more satisfactory approach would be to prevent or minimize the formation of residuals. Consider a serial CCD delay line; most of the transfers the signal undergoes do not contribute directly to the processing function as such, but are merely input and output operations. It is these redundant transfers that contribute most to the residual build-up, therefore if these could be eliminated, a considerable increase in performance could be achieved. It is proposed in this thesis that this increased performance may be realized by employing a parallel transfer CCD architecture in which all redundant transfers are eliminated. Implementation of the non-recursive and recursive integrators based on this concept will now be described.

4.5 Integrators Implemented with Parallel-Transfer CCD Architecture

The proposed implementation of a non-recursive integrator is shown in figure 4.4. Each radar range bin is implemented in the form of an 'm' bit two-phase CCD which is tapped at every bit. Successive returns are loaded into the CCDs by sequentially operating the analogue gates G_1, G_2 ..... G_N. Thus at any instant each CCD contains the last m echoes from one particular range bin. Since each CCD has all its taps connected together, integration over the m samples is achieved; the integrated signal is then gated to the output through gates G_1', G_2' ..... G_N'. Although the number of returns summed in this scheme is essentially fixed by the chip artwork, a limited degree of flexibility could be provided by segmenting the summing bus bars with MOST couplings.

In the recursive system, illustrated in figure 4.5, the returns are similarly loaded sequentially into each range bin storage site which comprises a single bit CCD. The stored signal

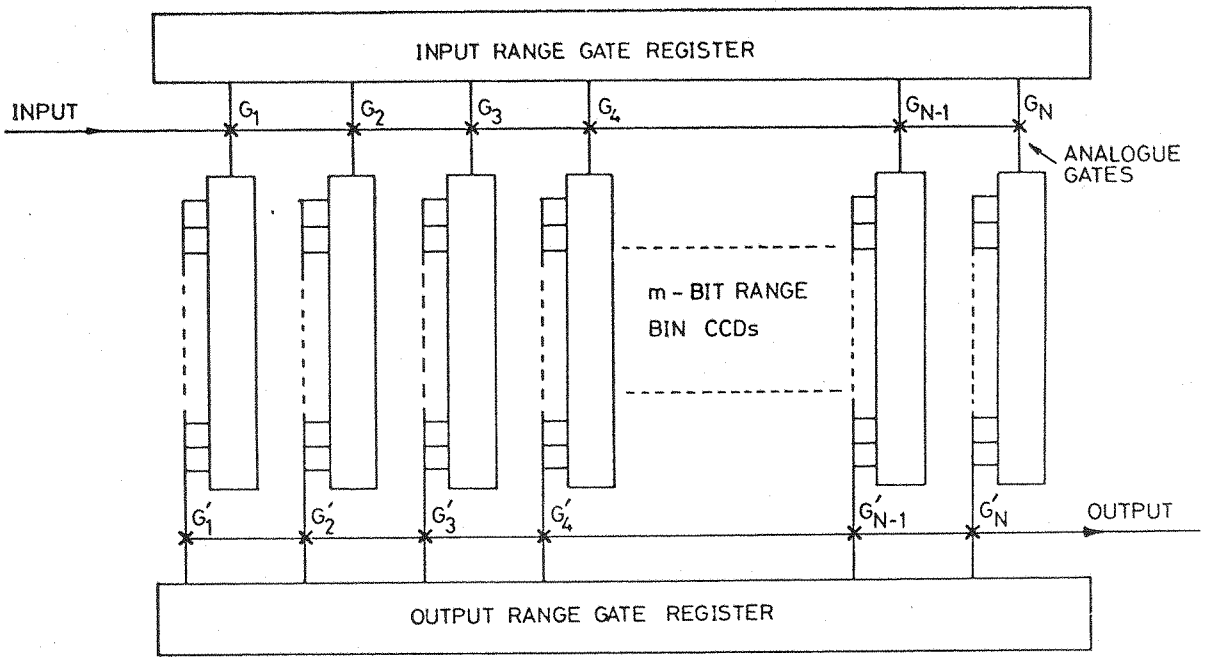

Fig 4.4 The parallel transfer approach to non-recursive integration.

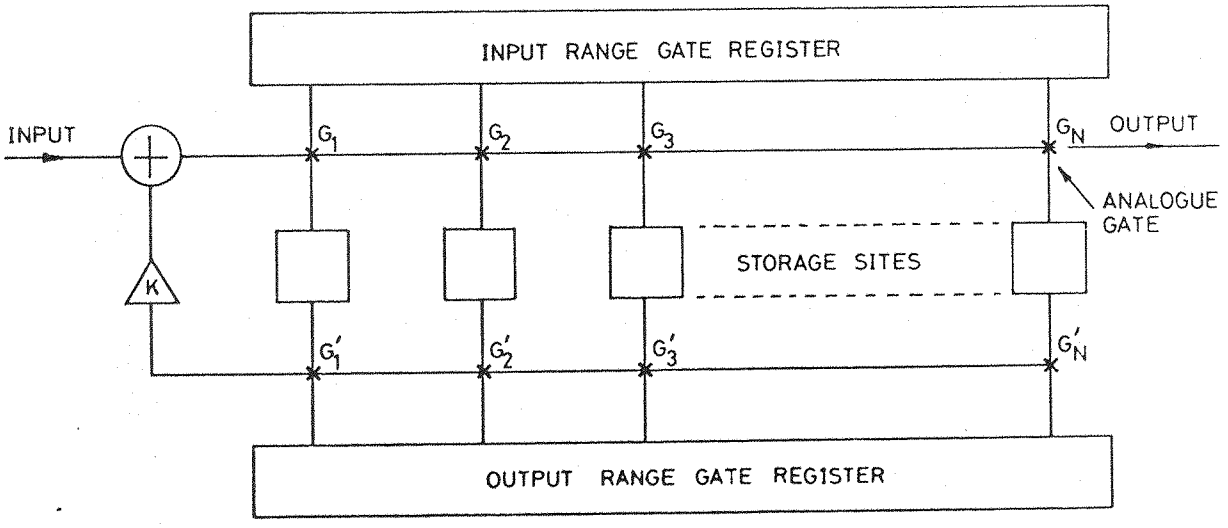

Fig 4.5 The parallel transfer approach to recursive integration.

is then gated out through G_1' G_2' ..... G_N' to be scaled and added to the appropriate range bin information of the next radar return.

Although the analogue gates shown in figure 4.4 and 4.5 are shown as components separate from the range bin storage areas, they can in fact be implemented as part of the CCD structures forming the storage areas. In both integrators each radar return undergoes a minimal number of CCD transfers (i.e. two per processing step), and so residuals are maintained at a very low level. For instance, for m = 10 and $\varepsilon = 10^{-4}$, the maximum dynamic range imposed by transfer inefficiency now becomes approximately 54.8dB. Furthermore, since each range bin is processed individually, residuals are confined to their respective range bins rather than smearing into adjacent range bins. Thus target range ambiguity is considerably reduced.

It will be appreciated that in order to implement the parallel processing integrators illustrated in figures 4.4 and 4.5, an on-chip addressing technique is essential to minimize the number of external connections. Such a scheme has been implemented by means of a 'range gate register' (RGR). This consists of a floating-gate tapped, two-phase CCD operated in the 1½-phase mode as a digital shift register and propagating a single charge packet. As the charge packet passes beneath each tapping point, an address pulse is generated that operates its corresponding analogue gate. In order that chip complexity is not increased by the inclusion of MOST or resistive biasing of each floating electrode,[79] a novel scheme is employed in which each gate is allowed to 'float' completely, any loading being purely capacitive. As a result, the floating-gates acquire their bias voltage by virtue of the lateral leakage of charge from the adjacent switched electrodes. Apart from the simplicity of this approach, it has the advantage that capacitive loading on each tap can be minimized; as will be seen later, this allows a large address pulse to be generated with each floating-gate, allowing each analogue gate to be driven directly without intermediate amplification.

Although parallel signal processing architectures have been described before, they use either surface charge transistors[80] or MOST accessed capacitors[4] as storage elements in conjunction with an on-chip MOST shift register addressing technique. The use of exclusively CCD structures, however, has the advantages of higher operating speeds and less chip complexity, with potentially higher device yields and lower operating failure rates due to the low number of diffusions.

4.6 Summary

In this Chapter the nature of sea-cluttered radar returns has been briefly introduced and several methods of improving target detection have been discussed; of those, the signal integrator provides the simplest and most versatile solution since the detection procedure is not based upon the target waveform but simply upon its regular occurrence during each sweep of the antenna. Two types of signal integrator were then described; the first technique formed the sum of the last m equally weighted returns, whilst the second formed an exponential sum of all the past returns. The implementation of these schemes with CCD delay lines has many advantages, but in simple serial processing systems a serious limitation on performance is imposed by transfer inefficiency. This limitation may be considerably eased by employing a parallel transfer CCD architecture in which all redundant transfers can be eliminated; the implementation of the recursive and non-recursive integration schemes based upon this approach was described.

The features of the two parallel processing integrators may be summarized as follow.

(i) In both schemes, the radar signal undergoes a minimum number of transfers and so residual signals are kept at a low level.

(ii) The number of range bins may be increased as desired without degrading the performance, simply by cascading the required number of devices together.

(iii) Although the effective number of returns summed using the recursive scheme can be easily varied, it is prone to instability if large integration improvements are required. On the other hand, this problem does not arise in the non-recursive scheme where it may also be possible to vary the integration improvement by segmenting the summing bus bars.

(iv) Although the non-recursive scheme is conceptually simpler, the recursive integrator would be easier to realize as an integrated circuit, i.e. interconnections and the need for orthogonal CCDs would pose fabrication problems.

(v) The parallel architecture of both integrators could be used to implement other signal processing systems. For instance, a recursive Fourier transformer[81] or a simple delay line with low sensitivity to transfer inefficiency.

If the impulse response of the range bin CCDs in the non-recursive approach were varied by employing CCD transversal filter techniques, more complex filtering of each range bin information could be performed.

Thus since each scheme possesses advantages that tend to complement the other, both have been investigated to some extent and the results are described in the remaining chapters of this thesis.

It has been indicated already that the operation of the RGR is crucial to the implementation of both integration systems. This scheme relies upon the floating-gate tapping scheme being able to provide sufficiently large address pulses to drive the

analogue gates. Moreover, whilst the RGR employs isolated floating-gate taps, it is proposed that the non-recursive integration method will employ either multiple floating-gate taps or the multiple electrode current sensing scheme. Therefore in the next Chapter these types of charge sensing techniques will be investigated in greater detail.

The parallel processing structures proposed in this chapter have been the subject of two papers recently published by the author; these are reproduced at the back. These structures are also the subject of UK Patent Application 47349/75 and US Patent Application 742182.

CHAPTER FIVE

NON-DESTRUCTIVE CHARGE SENSING

5.1 Introduction

The function of the RGR CCD in the parallel processing integrators described in the last Chapter is to operate sequentially the analogue gates. Each address pulse is generated by employing floating-gates above the CCD channel to sense non-destructively a single charge packet propagating along the device. One of the advantages of using a CCD for this operation, rather than an MOST shift register, is its higher operating speed; for this reason, any intermediate amplification between the taps and their corresponding analogue gates in the form of say MOST inverters is undesirable. Consequently, the voltage pulse generated by each floating-gate must be large enough to operate the analogue gates directly, i.e. ≃10V.

It was also indicated in the last Chapter that integration in the non-recursive integrator could be performed using multiple floating gate sensing. However, this technique introduces distortion due to the non-linear dependence of the depletion capacitance beneath the sensing electrode upon the surface potential.

Since very little theoretical work has been carried out on both these type of floating-gate sensing scheme, a rigorous analysis of these techniques has been undertaken in order to determine the parameters which influence floating-gate performance. In particular, whether large voltage swings are possible from single floating-gates, and whether acceptable non-linearities can be obtained from a multiple floating-gate array.

The analysis for the more general case of a multiple floating-gate system is presented first, and then this will be used to obtain an expression for the specific case of a single floating-gate.

An alternative integration technique for the non-recursive integrator is electrode-current sensing. Depletion capacitance also introduces a non-linearity into this method and so an analysis of this technique will also be presented.

First, however, we will consider floating-gate voltage sensing.

5.2 Floating-Gate Voltage Sensing

Although the use of a floating-gate is a widely accepted charge sensing technique, particularly in CCD transversal filters, comparatively little theoretical analysis of the technique has been published. In particular, any analysis has generally either neglected the effects of depletion capacitance[82] or included it incorrectly.[79] In this section, therefore, a method is described which may be used to analyse rigorously any type of floating-gate structure simply.

First, however, let us consider a simple MOS structure in which the gate has been pre-charged to a potential V_g and is then isolated. The equation relating V_g and the surface potential, ϕ_s, is simply

$$V_g = \frac{Q_g}{C_{ox}} + \phi_s \qquad 5.1$$

where the gate charge, Q_g, is the sum of the depletion charge Q_{dep} and the inversion or signal charge Q_s. Since the gate is 'floating' Q_g is constant, and so $\Delta V_g = \Delta\phi_s$. Furthermore, since Q_g is fixed, $\Delta Q_s = -\Delta Q_{dep}$ and so, because Q_{dep} is dependent upon $\sqrt{\phi_s}$, the relationship between V_g and Q_{dep} will be non-linear.

This MOS system forms the basis of the floating-gate sensing technique. In practice, however, the above relationship must be modified since there will exist a finite stray capacitance which

loads the gate. In the simplest practical system where the gate is loaded by a linear capacitance, Q_g will no longer be constant and so the change in gate voltage ΔV_g will be reduced by capacitive division. Clearly, if the loading capacitance is non-linear, the relationship between the gate voltage and the surface potential as well as the signal charge will be non-linear. But this is just the case one has when several floating electrodes are connected together, i.e. each electrode is loaded by the remaining electrodes in a non-linear fashion that depends upon the common gate voltage and stored charge.

In the past, capacitive models have been used for analysing floating-gate structures.[79,82] However, such an approach leads to confusion in modelling the depletion capacitance and difficulties in the subsequent analysis. These problems will not be discussed further here, but are illustrated in Appendix 2. Instead, rather than use the concept of 'capacitance' which is a derived quantity, the analysis will be carried out using the fundamental concept of 'charge'; as will be seen, this approach is considerably more straightforward.

The 'charge-balance' method is based on the fact that charge neutrality must be maintained in an MOS structure; in particular

$$Q_g = Q_{dep} + Q_s \qquad 5.2$$

Consider several floating-gates connected together and loaded by a stray capacitance, C_s (see figure 5.1). The total charge Q_T on the gate assembly is constant, thus we can write

$$Q_T = \sum_{n=1}^{N} A_n Q_{gn} + C_s V_g = \text{constant} \qquad 5.3$$

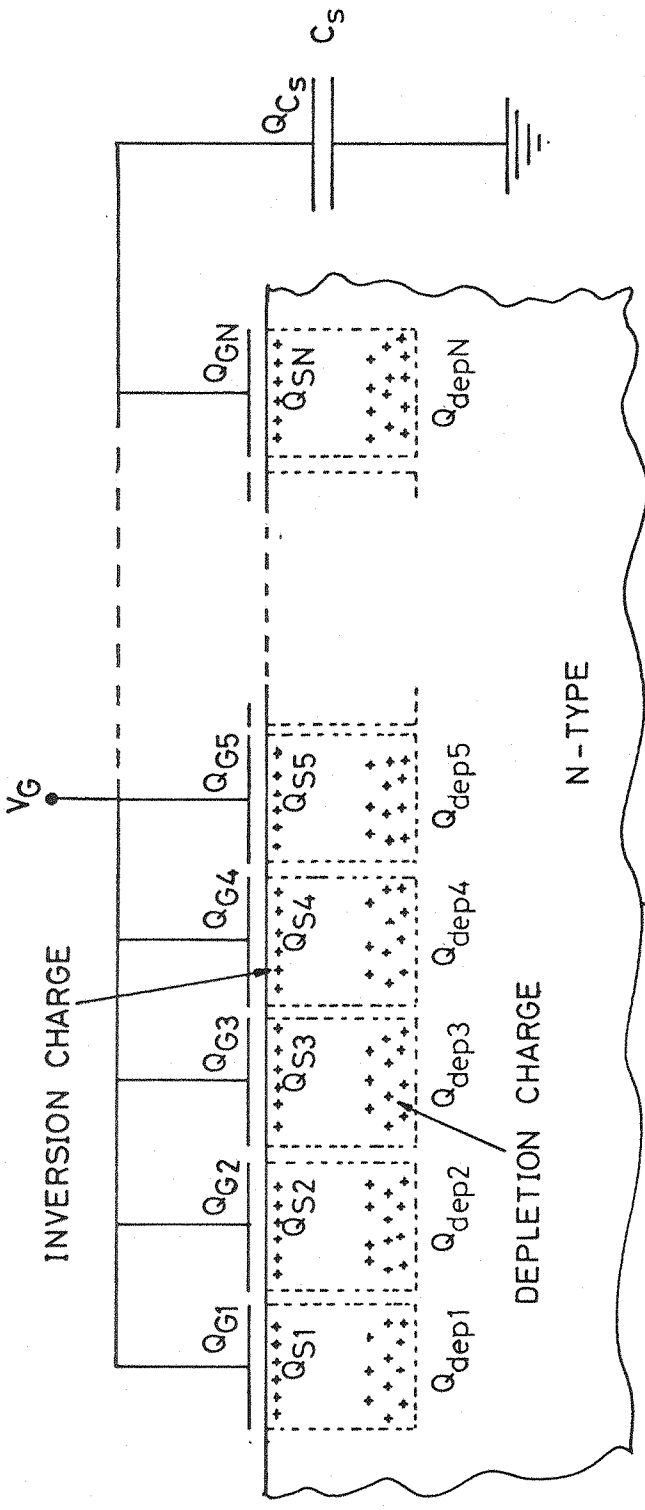

Fig 5.1 The charge distribution in a multiple floating gate system loaded by a fixed stray capacitance C_s.

where A_n is the area of the nth electrode.*

If charges Q_{s_1}, Q_{s_2}, Q_{s_3} ..... Q_{s_N} are injected beneath the gates 1, 2, 3 ..... N (previously assumed to have empty potential wells), the gate voltage will change by ΔV_g from $V_g(0)$ to $V_g(Q)$ and the surface potentials will fall from $\phi_{s1}\left\{0, V_g(0)\right\}$, $\phi_{s2}\left\{0, V_g(0)\right\}$, ... to $\phi_{s1}\left\{Q_{s1}, V_g(Q)\right\}$, $\phi_{s2}\left\{Q_{s2}, V_g(Q)\right\}$ ..... Denoting the change in the depletion charge beneath the nth electrode by ΔQ_{depn}, we may from equations 5.2 and 5.3 deduce that

$$\Delta Q_T = \sum_{n=1}^{N} A_n \left(Q_{sn} + \Delta Q_{depn}\right) + \Delta V_g C_s = 0 . \qquad 5.4$$

Since $Q_{depn} = \sqrt{2q\epsilon_s N \phi_{sn}}$, this equation can be rewritten as follows

$$\sum_{n=1}^{N} A_n Q_{sn} = \sum_{n=1}^{N} A_n \sqrt{2q\epsilon_s N}\left(\sqrt{\phi_{sn}\left\{0, V_g(0)\right\}} - \sqrt{\text{sn}\left\{Q_{sn}, V_g(Q)\right\}}\right) - \Delta V_g C_s \qquad 5.5$$

Finally, substituting for $\sqrt{\phi_s}$ using equations 2.1 and 2.2 yields

$$\sum_{n=1}^{N} A_n Q_{sn} = \sum_{n=1}^{N} A_n C_{ox}\left[V_o^2 + 2V_o\left(V_g(0) - V_{FB}\right)\right]^{\frac{1}{2}} - \sum_{n=1}^{N} A_n C_{ox}\left[V_o^2 + 2V_o\left(V_g(Q) - \frac{Q_{sn}}{C_{ox}} - V_{FB}\right)\right]^{\frac{1}{2}} - \Delta V_g C_s \qquad 5.6$$

where $\Delta V_g = V_g(Q) - V_g(0)$.

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* For the non-recursive integration technique, all the electrodes will of course be of the same area; however, the analysis is kept as general as possible in order that the results can be easily applied to split-gate transversal filters. In this case, each sensing electrode is split into two sections of area A_n^+ and A_n^-, where $A_n^{\pm} = A(1 \pm h_n)/2$ and h_n is the tap weighting coefficient.

This equation may be solved iteratively to evaluate ΔV_g, if $N > 1$. For $N = 1$, e.g. an RGR tap, ΔV_g can be obtained in closed form and is

$$\Delta V_g = \left\{ P - MQ_s/C_{ox} - \left[P^2 - 2V_oQ_sM(1+M)/C_{ox} \right]^{\frac{1}{2}} \right\} \Big/ M \qquad 5.7$$

where $P = V_o + M\left\{ V_o^2 + 2V_o\left[V_g(0) - V_{FB} \right] \right\}^{\frac{1}{2}}$

and $M = C_s/C_{ox}A_1 \neq 0.$

Equation 5.6 was derived for a floating-gate structure consisting of single level electrodes, (e.g. as in a three-phase CCD), but the extension of the analysis to a stepped oxide floating-gate structure (e.g. a two-phase device), is a simple matter. The thick oxide portion of each gate will constitute a non-linear loading capacitance on each thin oxide portion. This loading effect can be included by simply adding more 'gates' to the three-phase model which do not, of course, store charge.* Thus equation 5.6 can be rewritten

$$\begin{aligned} \sum_{n=1}^{N} A_nQ_{sn} = & \sum_{n=1}^{N} A_nC_{ox_{TN}} \left(V_{o_{TN}}^2 + 2V_{o_{TN}}\left[V_g(0) - V_{FB_{TN}} \right] \right)^{\frac{1}{2}} \\ & + \sum_{n=1}^{N} B_nC_{ox_{TK}} \left(V_{o_{TK}}^2 + 2V_{o_{TK}}\left[V_g(0) - V_{FB_{TK}} \right] \right)^{\frac{1}{2}} \\ & - \sum_{n=1}^{N} A_nC_{ox_{TN}} \left(V_{o_{TN}}^2 + 2V_{o_{TN}}\left[V_g(Q) - \frac{Q_{sn}}{C_{ox_{TN}}} - V_{FB_{TN}} \right] \right)^{\frac{1}{2}} \\ & - \sum_{n=1}^{N} B_nC_{ox_{TK}} \left(V_{o_{TK}}^2 + 2V_{o_{TK}}\left[V_g(Q) - V_{FB_{TK}} \right] \right)^{\frac{1}{2}} \\ & - \Delta V_gC_s \qquad 5.8 \end{aligned}$$

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* Clearly this analytical method may be used to include any non-linear loading capacitance, e.g. the electrodes of the CCD structures forming the analogue gates.

where the suffixes TN and TK denote the thin and thick oxide parameters respectively, and B_n is the thick oxide area of the nth electrode.

5.3 Electrode Current Sensing

The concept of electrode current sensing was discussed briefly in subsection 2.5.3. The analysis of a multiple-electrode current sensing scheme is more straightforward than the previous case because the gate voltage is maintained at a constant potential, thus eliminating one variable from the equations. The incremental charge, ΔQ_T, on the electrode assembly can be found simply by rearranging equation 5.1 and substituting for ϕ_S from equation 2.1; thus

$$\Delta Q_T = \sum_{n=1}^{N} \left\{ A_n Q_{sn} + A_n C_{ox} \left(V_o^2 + 2V_o \left[V_g - \frac{Q_{sn}}{C_{ox}} - V_{FB} \right] \right)^{\frac{1}{2}} - A_n C_{ox} \left(V_o^2 + 2V_o \left[V_g - V_{FB} \right] \right)^{\frac{1}{2}} \right\} \qquad 5.9$$

where V_g is the gate voltage.

5.4 Numerical Analysis

In this section two typical charge sensing structures are analysed using the equations derived above: the first structure is a single floating-gate tap, as would be used in the RGR, and the second a 63-tap low-pass CCD transversal filter. The latter case is analysed using both the voltage and the current sensing equations.

5.4.1 The Single Floating-Gate Tap

The single RGR floating-gate tap had the following parameters:

Electrode area	=	$8800\mu m^2$
Oxide thickness	=	$0.12\mu m$
Substrate doping density	=	$10^{15} cm^{-3}$
$V_g(0)$	=	15V

Although the RGR is a two-phase device, the loading effect of the thick oxide portion was assumed to be linear in order that the simple equation 5.7 could be used. This is a realistic assumption because in practice, it would be desirable to make the thick oxide length much shorter than the thin oxide section in order to optimise the transfer process and to realize a large charge handling capacity. Thus the loading effect will, in any case, be fairly small.* Figure 5.2 shows plots of the floating-gate voltage swing as a function of stored charge for various values of stray capacitance. The non-linear response which is evident from these plots, especially for small C_s, is not too important in this particular application; the most significant observation is that whilst the voltage variation is strongly dependent upon C_s, if the value of this parameter is sufficiently small, large voltage swings (i.e. ≃10V) are obtainable. Figure 5.3 shows the effects of varying the substrate doping levels and oxide thickness respectively, for a constant stray capacitance and percentage of charge filling the storage well. The floating-gate voltage swing is clearly not critically dependent upon these parameters in the range likely to be encountered in practice.

5.4.2 The Low-Pass Filter

The analysis on the 63-tap low-pass CCD transversal filter was performed to investigate the linearity of the charge sensing schemes and also to determine the effects on the overall transfer response of using either a potential equilibration type charge injection scheme, or the surface potential setting (diode cut-off) technique. A low-pass transversal filter was chosen for this analysis instead of the simple case of identical electrodes in order to illustrate the use of the equations. It also allowed a rough comparison to be made between the analysis and the experimental results obtained by other workers, e.g. Brodersen et al.[53]

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* The presence of the thick oxide section of the floating electrode may also cause incomplete transfer of charge. This effect will be discussed later, but at this stage is ignored.

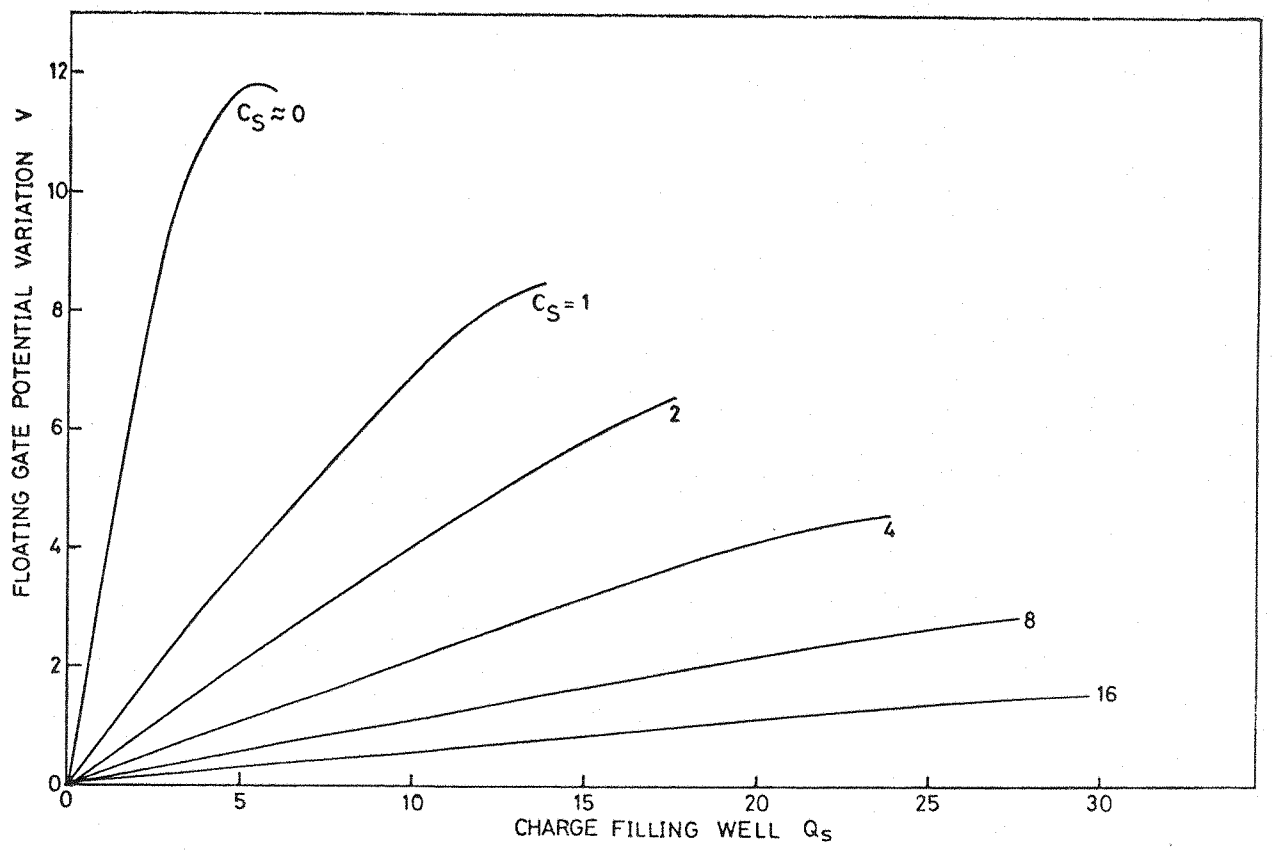

Fig 5.2 Response of a single floating gate to signal charge. Stray capacitance is the parameter.

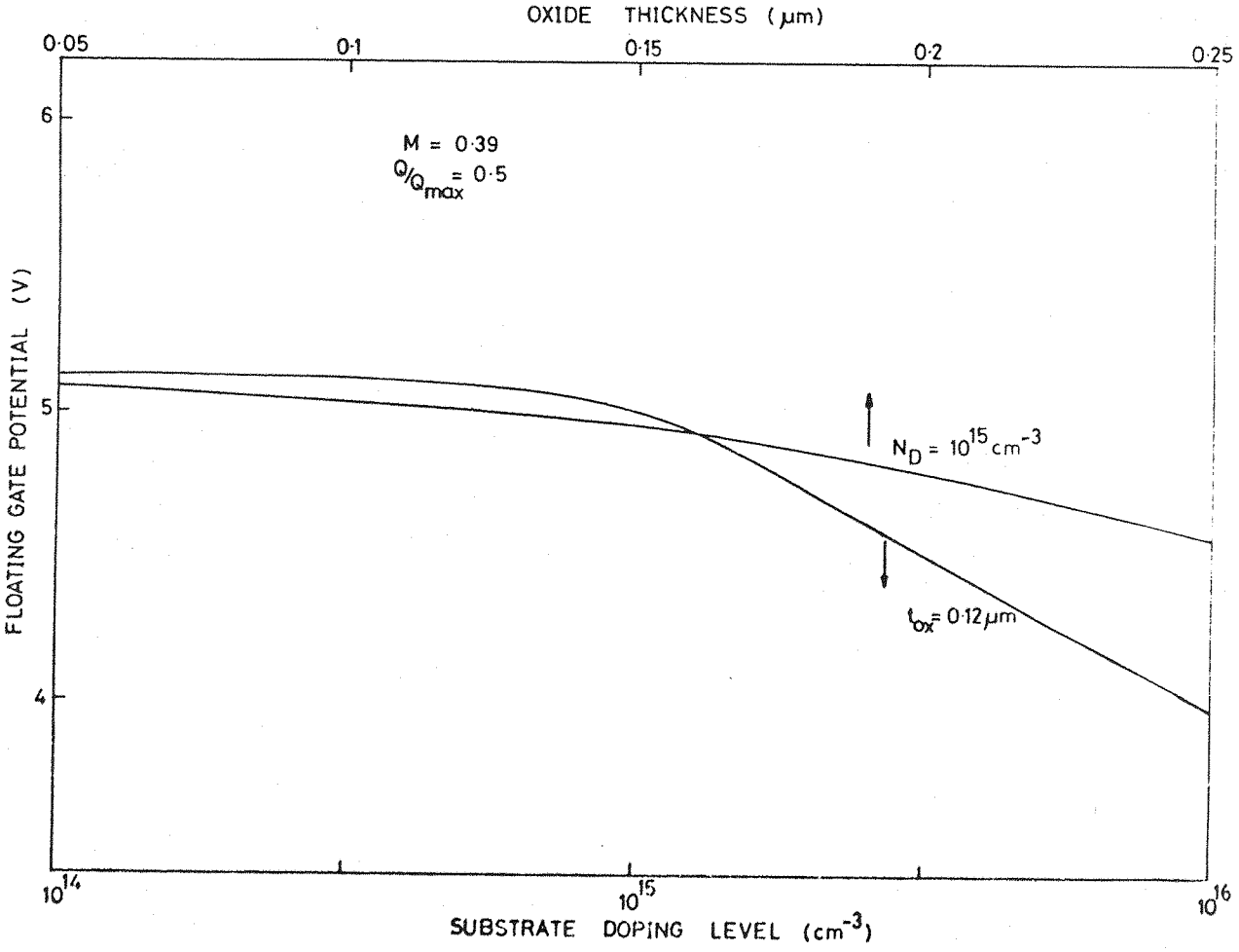

Fig 5.3 The effect of varying the oxide thickness and substrate doping level on the floating gate response.

and Baertsch et al.,[83] at a stage when charge sensing structures of this nature were not available to the author for investigation.

The weighting coefficients of the filter were calculated using a computer program[51] to achieve optimum equi-ripple characteristics and had the following parameters: $f_p/f_c = 0.1$, $f_s/f_c = 0.131$, $\delta_1/\delta_2 = 1$, where δ_1 and δ_2 are the passband and stopband ripples and f_p, f_s and f_c are the passband edge, stopband edge and clock frequencies respectively. The parameters of the CCD were:

Electrode area	=	$1000\mu m^2$
Oxide capacitance	=	$0.1\mu m$
Substrate doping density	=	$10^{15} cm^{-3}$
$V_g(0)$	=	15V
C_s	=	50pf

In order to calculate the overall response, the two injection schemes were modelled as follows:

(i) $Q_s = KV_{in}$ for the potential equilibration scheme;

(ii) $Q_s = C_{ox}\left\{V_{g_1} - V_{in} - \sqrt{2V_o V_{in}}\right\}$ to simulate the ideal diode cut-off technique. (This equation is simply derived from equation 2.2 where the surface potential beneath the input electrode is equal to the voltage on the diode, i.e. V_{in}.) V_{g_1} is the (fixed) voltage on the input electrode.

Ordinarily, these relationships must be substituted into equations 5.6 and 5.9 to obtain the overall response. However, a significant simplification can be identified for the special case when current sensing is used in conjunction with the ideal diode cut-off scheme, provided sensing electrodes are at the same

potential as the input gate, i.e. consider the nth electrode of a current sensing system. We may write from equation 5.1

$$Q_{g_n} = C_{ox} (V_g - \phi_{s_n}) \qquad 5.10$$

from which we see that the gate charge is proportional to the surface potential. If $V_g = V_{g_1}$, then ϕ_{s_n} will simply be the input voltage n clock waveforms previously, and so we may write

$$\Delta Q_T(KT_c) = \sum_{n=1}^{N} A_n C_{ox} V_{in}(KT_c - nT_c) \qquad 5.11$$

From equation 5.11 we see that if this combination is used, a linear overall response may be realized.

In order to determine the overall response for the remaining cases, a computer program was used. A subroutine was included to simulate the propagation of charge along the CCD so that transfer inefficiency effects could be investigated. Full details of the program are given in Appendix 2. By considering sinusoidal inputs of appropriate frequencies and evaluating the discrete Fourier transform of the output, the frequency response and harmonic distortion of the filter could be obtained. Full details of the results obtained from the analysis of the 63-tap low-pass transversal filter are given in Appendix 2; they may be summarized as follows:

(i) For the device parameters chosen, the current sensing scheme gives least overall distortion; the best choice of charge injection technique depends upon the level of non-linearity introduced by charge partitioning in the diode cut-off scheme; this effect was not included.

(ii) The distortion introduced by voltage sensing can be decreased by increasing the stray capacitance and in the limit of large C_s approaches the distortion introduced by the current sensing technique. However,

increasing C_s also decreases the output voltage amplitude and so would result in an inferior signal-to-noise ratio during subsequent amplification.

(iii) The analysis shows that second harmonic distortion of the order of -49dB can be obtained. Obviously no direct comparison can be drawn, but this figure is in reasonable agreement with results obtained by Baertsch on a similar filter operated with approximately the same parameters.[83]

Although these results indicate that the best performance is obtained with a current sensing arrangement, the implementation of this scheme requires more complex peripheral circuitry than the voltage sensing scheme.[83] In practice, the advantages of a more straightforward implementation may outweigh its slightly inferior performance; thus the choice of sensing technique for the non-recursive integrator will require further careful consideration.

In the analysis of the voltage sensing configurations, two minor second-order effects were not considered. The first effect arises if the floating-gate assembly is not reset to $V_g(0)$ at some point during every clock cycle. For instance, if resistive biasing is employed, only the average value of the voltage waveform on the floating gate assembly is clamped to the bias voltage. Thus $V_g(0)$ will vary according to the mean amplitude of the floating-gate voltage. This effect has not yet been modelled, but it is felt that if the output voltage amplitude is kept reasonably small (< 1V pk-pk say), it can be ignored. The second effect only occurs in split-electrode voltage sensing schemes, and is termed 'charge-hogging'. It is due to the voltage differential on the two gate assemblies causing an unequal charge distribution beneath each electrode section. Recent work[84] has shown that in general, this effect can also be neglected.

5.5 Summary

In this Chapter, an analytical technique for investigating both floating-gate voltage sensing and electrode current sensing techniques has been described. An analysis of a single RGR-tap has shown that provided stray capacitance is minimized, sufficiently large voltage pulses can be generated to drive each analogue gate directly.

Analysis of a 63-tap filter has shown that, despite the non-linearities introduced by depletion capacitance effects in both charge sensing schemes, acceptable overall distortion levels ($\simeq$ -45dB) can be obtained provided the appropriate charge injection scheme is employed; indeed, tentative agreement has been obtained between these results and experimental results of other workers. Thus it is reasonable to assume that a non-recursive integrator could be designed in which distortion would not unduly degrade performance.

It was pointed out at the end of Chapter 4 that the recursive integrator required a less complex IC layout than the non-recursive. For this reason, it was decided to place more emphasis on the development of a recursive system initially. In the next Chapter, the implementation of the recursive scheme is considered in detail.

CHAPTER SIX

THE CCD IMPLEMENTATION OF THE RECURSIVE INTEGRATOR

6.1 Introduction

The basic concepts of the parallel transfer recursive integrator have been discussed in Chapter 4. In this Chapter the design of a test integrated circuit to evaluate this implementation is presented.

As indicated already, the storage sites and associated analogue gates are combined as a single-bit CCD, thus allowing the higher operating speed capabilities of these structures to be employed whilst reducing chip complexity. In the device described in this Chapter, a further simplification is introduced by eliminating the second RGR associated with the output gating shown in figure 4.5. This is possible because the necessary addressing pulses for both input and output analogue gates can, in fact, be obtained from a single RGR.

In this test device, MOST inverting buffers were inserted between the RGR taps and the analogue gates so that the low frequency performance of the RGR could be evaluated without excessive loading effects. Clearly, removing the second RGR and so halving the required number of buffers allows a substantial reduction in chip complexity and size.

A schematic of the test device is shown in figure 6.1. It consists of a 4-bit RGR, four buffers and three storage cells. The sample/hold circuitry, scaling amplifier and summing network shown in figure 6.1 were not included on the test chip. The operation of the circuit is as follows: the output bus is set to a reference level and a '1' is loaded into the first bit of the RGR. The information stored in the first storage site is thus gated to the output bus where it is sampled and held. This value

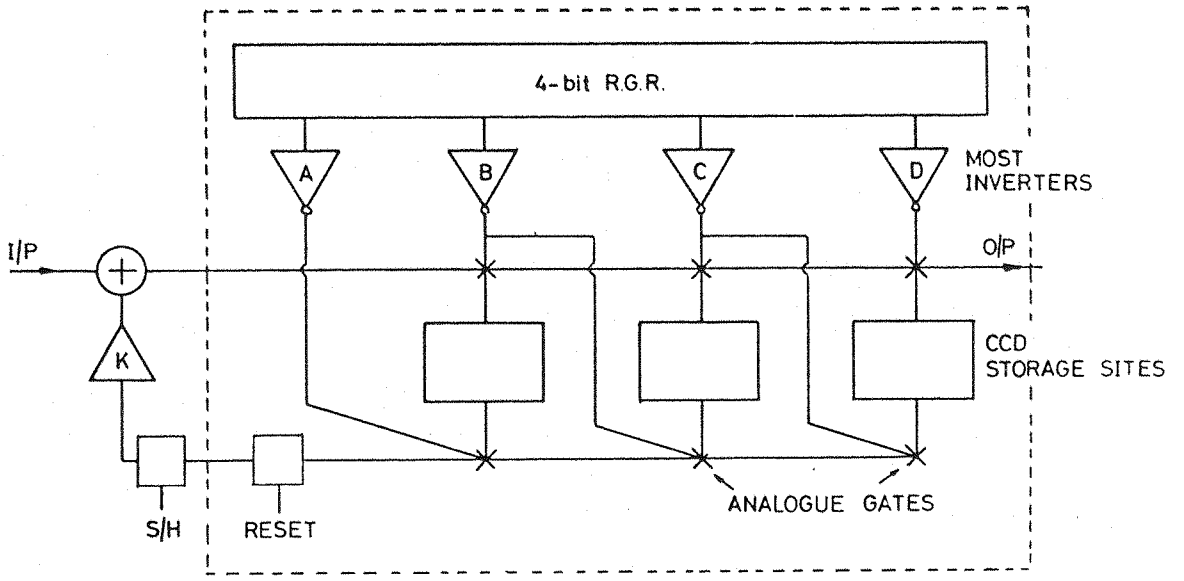

Fig 6.1 A schematic of the test recursive integrator. The components inside the dotted box are fabricated on-chip.

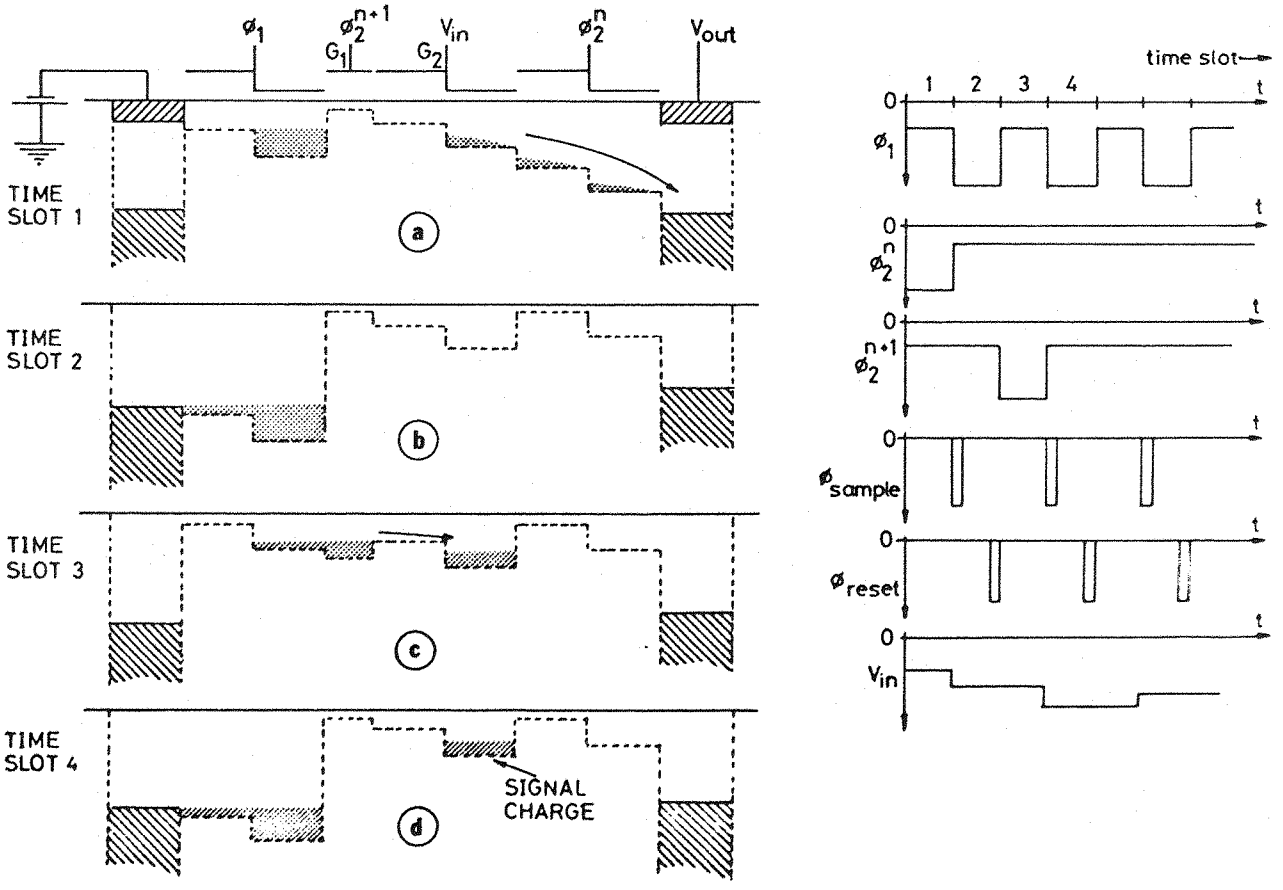

Fig 6.2 A cross-section of a storage site showing its operation and timing waveforms.

is scaled and summed with the next input; in the meantime, the output bus has been reset. The RGR is then clocked, transferring the '1' to the next bit, thus generating an address pulse enabling the first storage site to be loaded with the new information; simultaneously, the information in the second storage site is gated to the output bus. The sequence continues until all the storage sites have been updated.

6.2 The Operation of the Storage Site

A cross-section of a storage site is shown in figure 6.2. This structure is operated in the 1½-phase mode by the ϕ_1 clock waveform which is also used to drive the RGR. The input analogue gate is simply the input section of this two-phase CCD structure, comprising electrodes ϕ_1, G_1 and G_2 and employs the charge injection technique described in section 2.4.1. As indicated already, charge injected by this method has demonstrated a high signal-voltage to charge-packet-size linearity.[18] Output gating is accomplished by pulsing $\phi_2{}^n$ and thus transferring the signal charge stored beneath G_2 to the output diode.

The operation of the storage site is as follows: consider an address pulse from the nth bit of the RGR arriving at the $\phi_2{}^n$ electrode. Signal charge previously stored beneath G_2 will flow onto the output diode (which is connected to the output bus) (see figure 6.2a). Upon application of the next clock pulse to the RGR, the charge representing the '1' will be transferred onwards and so $\phi_2{}^n$ will turn off. Simultaneously, the ϕ_1 electrode is pulsed so that its storage wells can accept charge from their adjacent diode diffusions (figure 6.2b). During the ON period of ϕ_1 the signal voltage on the output diode is sampled and the diode immediately reset to a reference level. As ϕ_1 turns off, the charge in the RGR is transferred to the (n+1)th tap causing $\phi_2{}^{n+1}$ to pulse on. Since the ϕ_1 well is now in the 'supply' position, the well formed beneath the gate G_2 will fill with charge

proportional to the new signal voltage, V_{in} (figure 6.2c). During the next clock cycle, this signal charge is isolated in the G_2 well (figure 6.2d); thus within two clock periods, any storage site can be accessed and updated.

In order that a signal integrator can be used to effectively reduce clutter amplitude, the interval between successive radar returns from a single bearing must be greater than 100ms; consequently each return must be stored for an equivalent period multiplied by the integration sample size, m. The storage times achievable with CCDs, as indicated in section 2.7, are limited by dark current generation, but must clearly be longer than m x 100ms if they are to be usable in this application. Dark current generation rates are strongly dependent upon the fabrication process used and the operating temperature of the device, as discussed. CCDs fabricated in the microelectronics laboratory here at Southampton University have exhibited storage times of typically only 10ms, however, it is hoped that with the appropriate processing procedures, this figure can be increased to about 10 secs. The development of suitable procedures is beyond the scope of this investigation and is in fact being studied by other workers in the laboratory.[85] Therefore, this vast topic will not be discussed further here.

6.3 The Design of the Test Chip

The procedures used to design the test device and to ensure that the three main components - the RGR, buffers, and storage sites - interface correctly are described below.

6.3.1 The Storage Sites

The design of the test device is best approached by first considering the storage sites, since the required driving voltages of these components determine the parameters of the buffers and RGR.

The pitch of the storage sites determines the length of each RGR bit,* which from transfer efficiency considerations should be as small as possible. The storage sites were therefore designed using minimum geometry design rules (the smallest feature dimension is 4μm) but allowing for a reasonable charge handling capacity. Although this parameter is normally determined by the electrode width also, this dimension had been constrained to 200μm to maintain a small overall chip size. Figure 6.3 is a dimension photomicrograph of a storage site, and it can be seen that in order to reduce the pitch to 100μ the output diode has been placed beneath G_3.

In order to simplify process monitoring, the standard CCD fabrication schedule was used; this yields thick and thin oxide thickness of 0.5μm and 0.12μm respectively. The silicon used in the process was 2-5Ωcm <100> n-type (i.e. $N_D \simeq 1{\cdot}8.10^{15}cm^{-3}$).

The remaining design considerations are best illustrated by referring to figure 6.4. In this diagram the minimum and maximum value of surface potential that must exist beneath the storage site electrodes set to their maximum (broken line) and minimum potential (continuous line) respectively, is shown. These conditions ensure that complete charge transfer between potential wells takes place and that a maximum sized charge packet can be stored. From this diagram and figure 6.5, which shows the variation of surface potential beneath the thin and thick oxides as a function of gate voltage, the bias voltages can be calculated. For instance, if the minimum potential of the ϕ_1 waveform, ϕ_{1OFF}, is 4V, the voltage on $\phi_2{}^n$ must swing from 4V to 17.6V so that a full charge packet can be stored beneath G_2 and subsequently transferred to the output diode. Similarly, the voltage on G_1 must

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* There is no possibility of making the RGR bit length half the storage site pitch by placing the storage sites each side of the RGR; the gates of adjacent storage sites must be connected together and this approach would create an enormous interconnection problem.

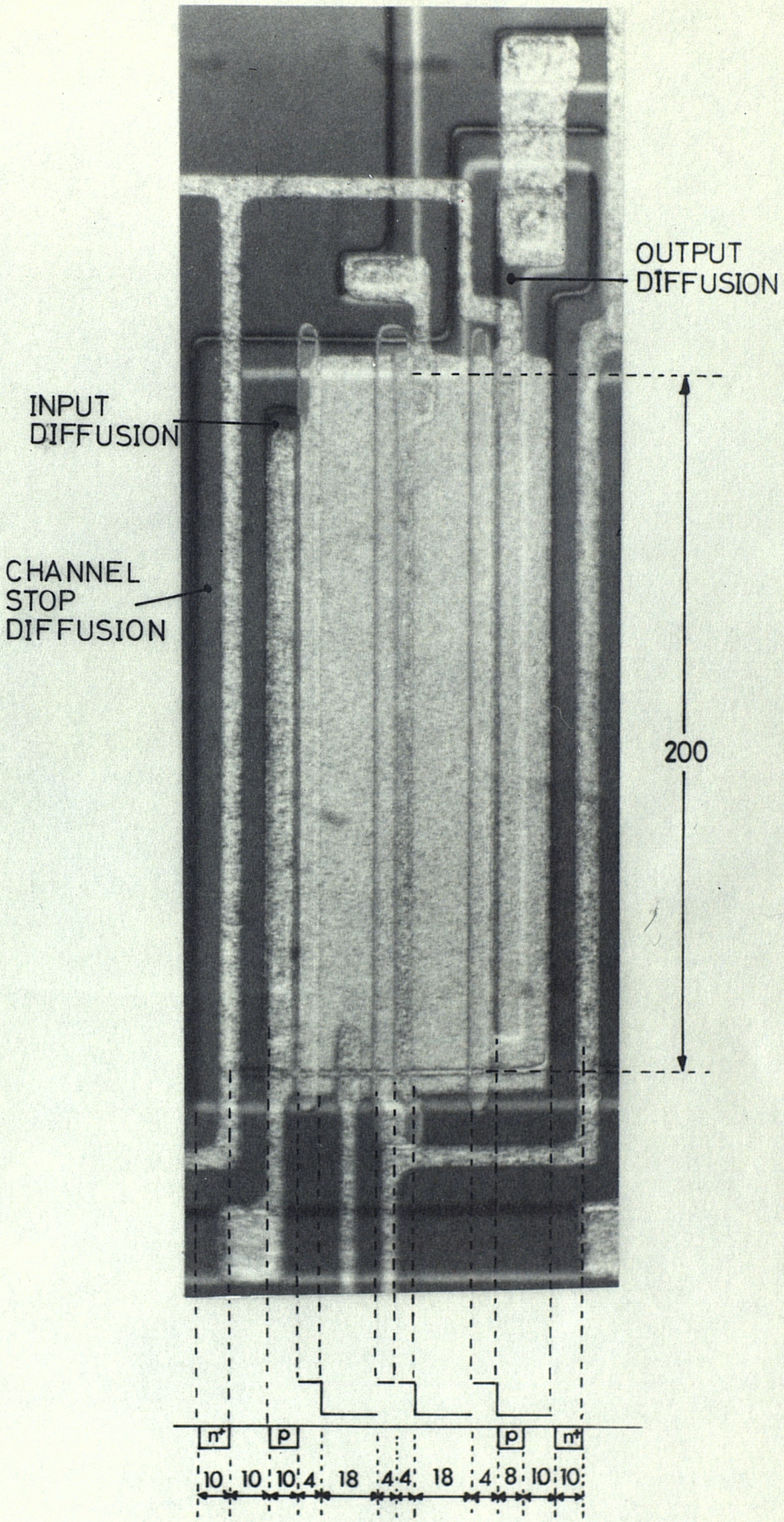

Fig 6.3 A photomicrograph of a storage site. The dimensions are

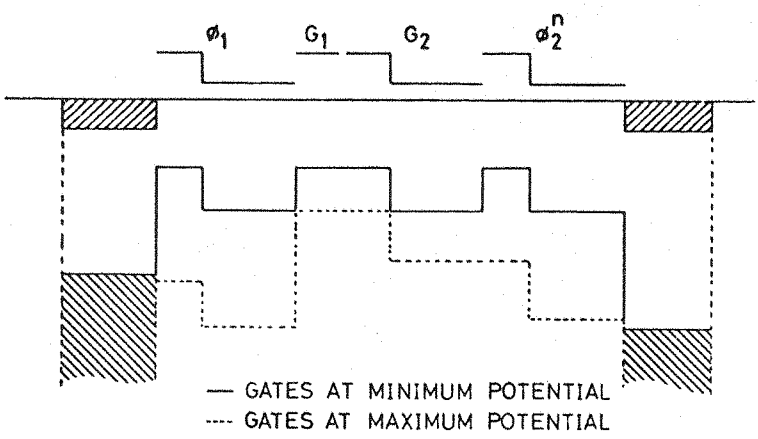

Fig 6.4 The surface potential profiles in the storage site that will ensure complete transfer and storage of a full charge packet.

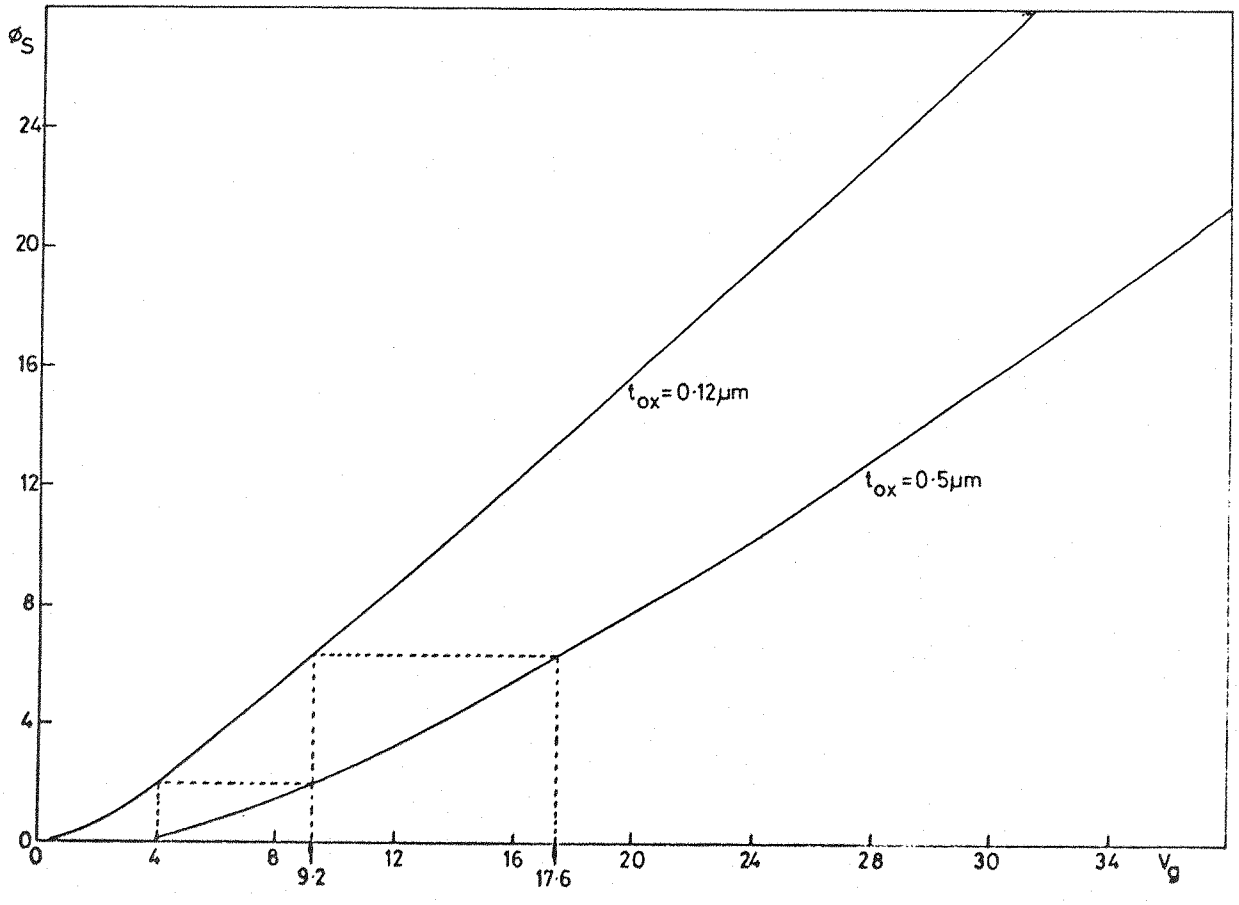

Fig 6.5 The variation of surface potential beneath the thick and thin oxide gates with gate voltage. The parameters used were appropriate for the processing used to fabricate the devices.

vary between 4V and 9.2V to ensure that charge in the ϕ_1 well is isolated from G_2, except during the appropriate clock cycle when a full charge packet may be transferred. In fact, the voltage on G_1 will rise to more than 9.2V since it is connected to ϕ_2^{n+1}. As a result a small amount of charge will be trapped beneath G_1, and so reduce the maximum charge that can be metered into G_2. This is minimized by making G_1 as short as possible, i.e. 4μm; furthermore, since ϕ_1 will switch on before G_1 turns off, this 'residual' charge will transfer back to beneath the ϕ_1 electrode and not forwards. The maximum charge handling capacity under these conditions is ≈4pC. Since the capacitance of each output diode when reverse-biased to ≈19V is less than 0.02pF, considerable capacitive loading of the output bus is required to reduce the signal voltage developed on it to a reasonable level, say 2V pk-pk; otherwise distortion due to the non-linear sense diode capacitance would be unacceptable.

Having discussed the bias voltage requirements of the storage site, we will now consider the buffers.

6.3.2 The Buffers

Each buffer is implemented as a standard MOST driver and load configuration. To ease interfacing with the storage sites, it would be desirable for the voltage gain of each buffer to be as high as possible. However, in the limited silicon area available, voltage gain can be increased only by sacrificing switching speed. The switching speed was required to be 1μs with each buffer operating into a capacitance of ≈15pF (the capacitance of the storage site gates, interconnecting tracks, bonding pad and scope probe). Thus the gain of the load device was calculated upon this criterion.[86] The space available to fabricate each buffer was determined by the storage site pitch and the distance between the RGR and the storage sites. This later dimension was set to 500μm in order that the chip size did not exceed that which

could be handled by the step-and-repeat camera, i.e. ≈1.5 x 1.5mm. The buffer layout was then optimised using these criteria, to maximize the voltage gain whilst maintaining the required switching speed. As a result, the maximum voltage gain that could be realized was only three. (However, provision was included in the artwork for the gain to be easily increased - but at the expense of switching speed.) A dimensioned photomicrograph of a buffer is shown in figure 6.6.

So that a reasonable degree of control over the operating characteristics of the buffers could be exercised, provision was included on the test device to vary the source bias of the driver transistors. The transfer characteristics may be easily derived, bearing in mind that the substrates of both transistors are connected to ground.[87] Thus in the linear region the transfer characteristic can be described by the equation

$$V_{in} = \frac{(V_{DD} - V_{out} - V_{TL} - \Delta V_{TL})}{A_V} + V_{TL} + V_s + \Delta V_{TD} \qquad 6.1$$

and in the non-linear region

$$V_{in} = \frac{(V_{DD} - V_{out} - V_{TL} - \Delta V_{TL})^2}{2A_V^2(V_{out} - V_s)} + \frac{V_{out} - V_s}{2}$$

$$+ V_{TD} + V_s + \Delta V_{TD} \qquad 6.2$$

where $$\Delta V_{TL} = \sqrt{2V_o}\left\{\sqrt{2\phi_f V_{out}} - \sqrt{2\phi_f}\right\} \qquad 6.3$$

$$\Delta V_{TD} = \sqrt{2V_o}\left\{\sqrt{2\phi_f V_s} - \sqrt{2\phi_f}\right\} \qquad 6.4$$

V_{DD} is the supply voltage = 30V

V_{out} is the buffer output voltage

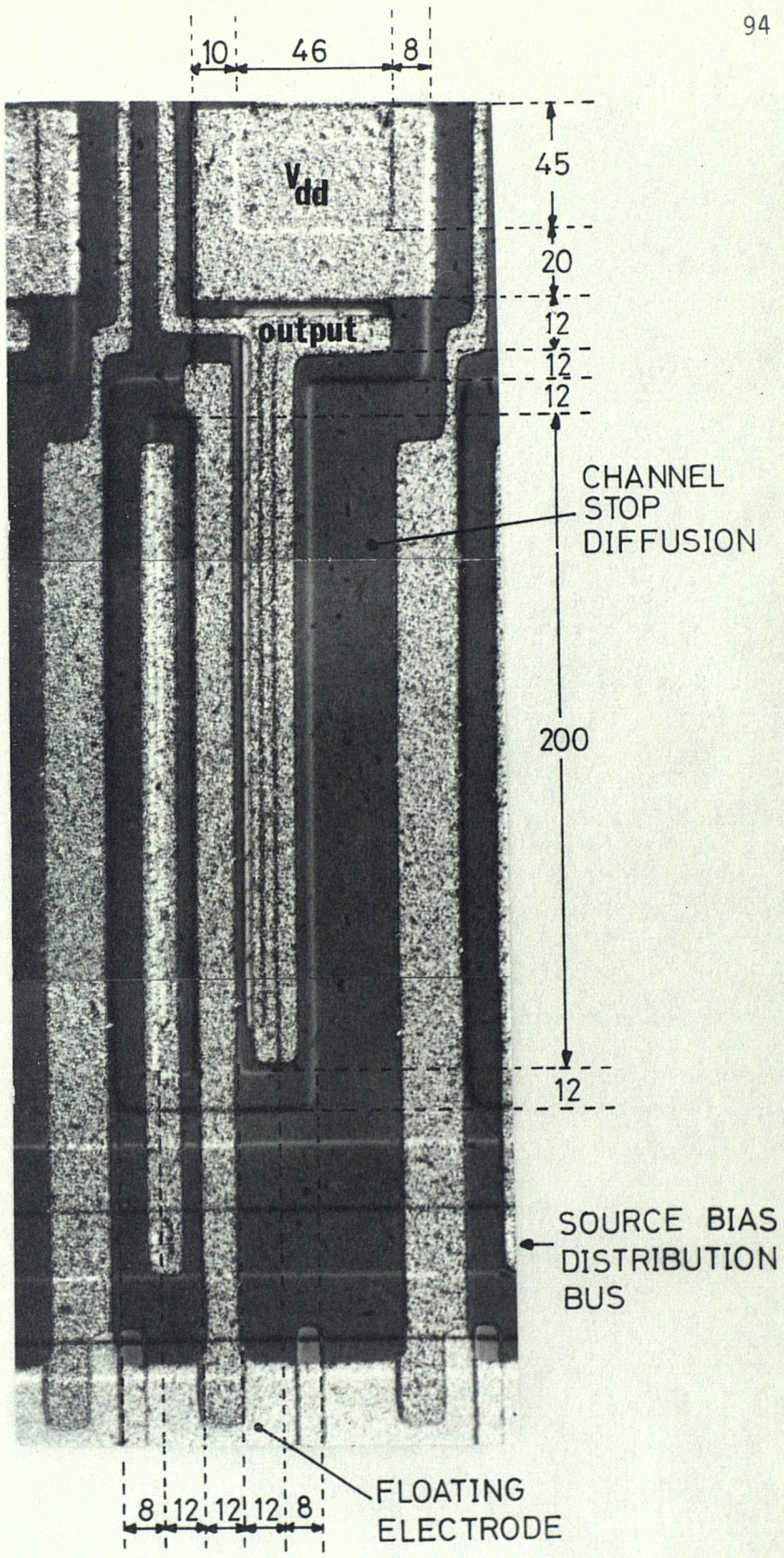

Fig 6.6 A photomicrograph of a buffer. The dimensions are in μm.

V_{TL} is the load MOST threshold voltage = 2V

V_{TD} is the driver MOST threshold voltage = 2V

V_s is the driver MOST source bias

A_v is the buffer gain = 3

V_o = 0.35V

and ϕ_f is the Fermi potential = 0.6V.

The evaluation of these equations was aided by the use of an HP-25 programmable calculator and the results are plotted in figure 6.7 for several values of V_s. Using these curves, and the conditions that ensure correct operation of the storage sites, the required voltage deviation of each floating-gate tap in the RGR can be obtained. Further details of this procedure will be postponed until the design of the RGR has been described.

6.3.3 The RGR

As described in Chapter 4, the RGR is a floating-gate tapped two-phase CCD. This device is operated in the 1½-phase mode with alternate electrodes (the floating electrodes) biased by the surface leakage of charge from the adjacent electrodes. Figure 6.8 shows an equivalent circuit of the structure; C_e and R_e represent the inter-electrode capacitance and resistance, C_g and R_g represent the gate-to-substrate capacitance and resistance and C_s the stray capacitance. C_e (being effectively the parallel plate capacitance between the edges of adjacent electrodes) is negligible compared with $C_g + C_s$ and under normal circumstances R_g is much larger than R_e, the latter being approximately $10^{12}\Omega$ (the validity of these assumptions will be discussed in the next Chapter). The time constant of $(C_g + C_s)$ and R_e is approximately 10 secs., considerably longer than the clock period, and so the voltage at X will be simply the average value of the ϕ_1 waveform.

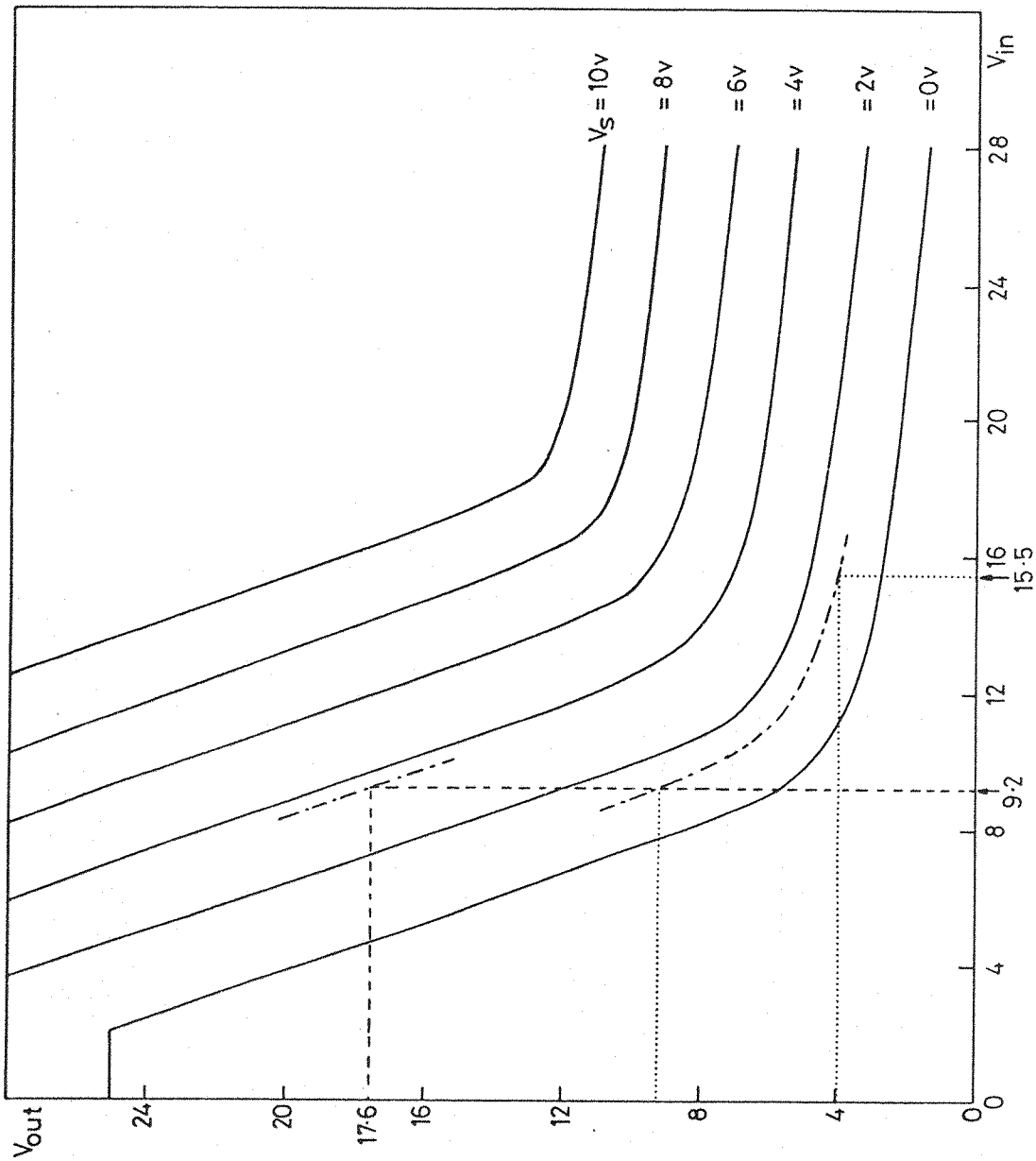

Fig 6.7 The theoretical response of the buffers with source bias as a parameter.

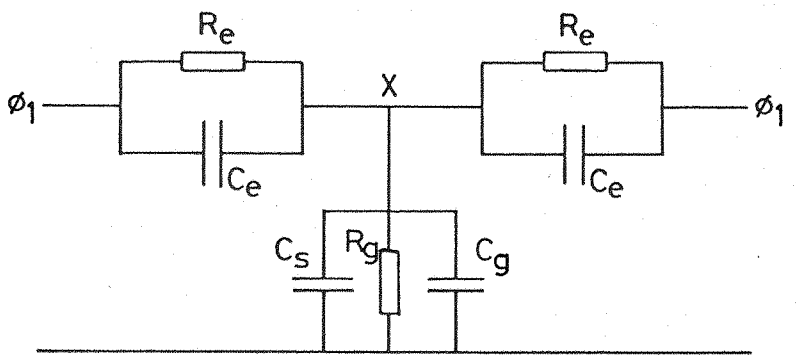

Fig 6.8 The equivalent circuit of the floating electrode biasing arrangement.

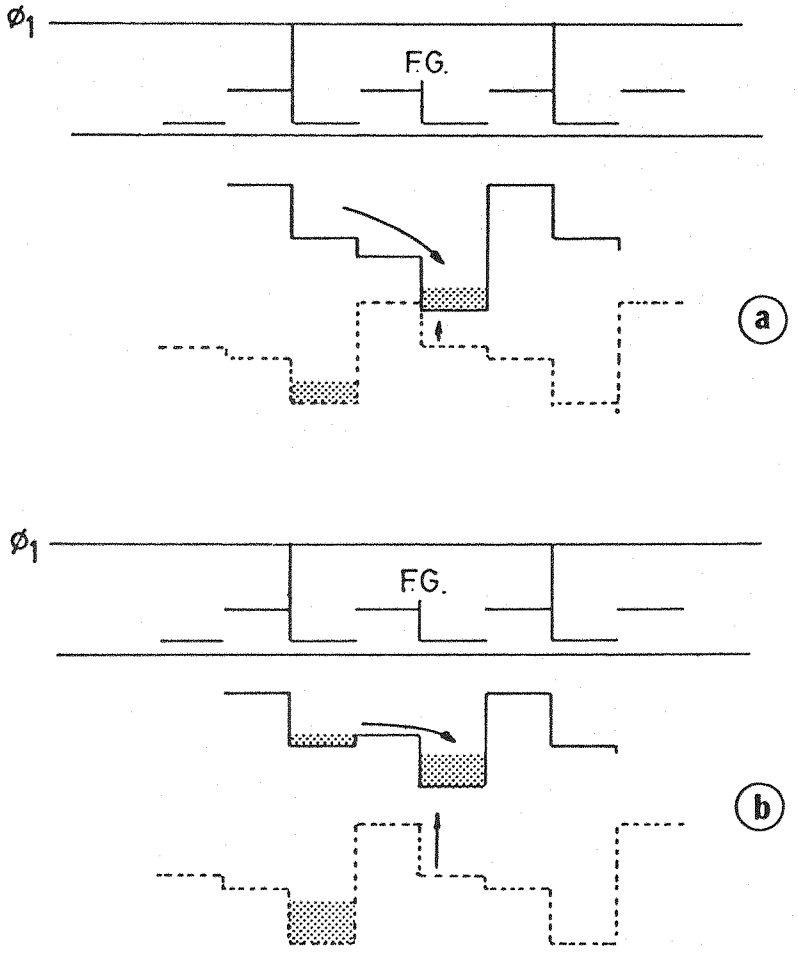

Fig 6.9 Incomplete transfer caused by large charge packets.

It was shown in the last Chapter, that if the floating-gate is required to generate large voltage swings, the capacitive loading on the gate should be small. However, in a two-phase device, where the floating-gate is simply a thick/thin oxide structure, an additional limit is imposed upon the minimum potential to which the gate can fall. Consider figure 6.9: these diagrams illustrate the surface potential profile when a small charge packet (figure 6.9a) and a large charge packet (figure 6.9b) is transferred along the RGR. The continuous line shows the condition when ϕ_1 is off and the broken line when ϕ_1 is on. It can be seen that whilst the smaller charge is transferred completely, the falling potential of the floating-gate in response to the larger charge packet prevents complete charge transfer. Consequently a certain amount of charge will be trapped in the ϕ_1 well; more importantly though, the floating-gate voltage will be clamped at a value corresponding to the condition that its thick oxide surface potential is approximately equal to the thin oxide surface potential beneath the ϕ_1 electrodes. Thus if the minimum ϕ_1 potential is 4V, then from the graphs in figure 6.5, we see that the minimum floating-gate potential will be ≃9.2V. This should correspond to a voltage on G_1 or G_3 of 17.6V; by using the curves drawn in figure 6.7, it can be seen that this condition can be achieved by applying a source bias of approximately 3.5V to the buffers. The 'off' potential on G_1 and G_3 should be 4V which from figure 6.6, and using the same value for V_s, corresponds to a floating-gate bias of 36V. For a 4V offset clock, this would require a clock voltage amplitude of 64V. Apart from the difficulties of generating a clock waveform of this magnitude, the maximum voltage is approaching the breakdown voltage of the thin oxide layer.[88] In any case, the clock generators available to the author could generate a maximum amplitude of only 27V; thus with a 4V offset, the floating electrodes would be biased to ≃17.5V. This corresponds to an output voltage from the buffer of approximately 6.5V, but this is not low enough to prevent charge flowing from the ϕ_1 well into the storage well under G_2 at every

clock cycle. In fact, it is impossible to achieve satisfactory interfacing of all the components on the test device due to the low gain of the buffers. However, by modifying the waveform applied to the input gate, G_2, this situation may be retrieved.

It will be recalled from figure 6.2 that the input signal is continually applied to G_2; however, if this waveform is strobed so that when ϕ_1 is off the voltage on G_2 falls to ϕ_{1OFF}, correct operation of the storage sites can be obtained, e.g. assume that ϕ_{1OFF} = 4V; if the above modification is implemented, then the voltage on G_3 need only swing between 4V and 9.2V. The floating-gate will swing between 15.5V and 9.2V, thus the voltage swings required for G_1 and G_3 can be obtained by setting the buffer source bias to ≈1.5V.

It has been assumed thus far that the capacitive loading of the floating-gates does not limit the voltage swing. In fact, the width of the RGR was chosen to be 200μm and the length of thin oxide portion of the gates to be 44μm. The ratio of the stray capacitance to the gate capacitance was then ≈0.25, thus ensuring the above condition. Although an electrode length of 50μm is rather long for low transfer inefficiency, it was estimated,[38] based upon self-induced drift calculations, that at f_c = 700kHz, $\varepsilon = 10^{-3}$. Since the RGR is only 4-bits long, this level of ε is unlikely to cause trailing charges large enough to cause spurious switching of the analogue gates.

6.4 Device Fabrication

Fabrication of the test device required six masks; these were laid out in Rubylith, 250 times the final size. The fabrication of the inter-electrode gaps was carried out using the oblique evaporation shadowing technique described in Chapter 2. An added advantage of using this technique is that small features can be fabricated without the need to allow for the possibility of mask misalignments. For instance, the input gate G_1, which is

only 4μm long, and its interconnection track is defined completely with the shadow technique (see figure 6.10), i.e. the 'leading edge' is defined by the oxide step, and the trailing edge by the edge of G_2. Full details of the processing schedule can be found in Appendix 4. A photomicrograph of the complete device is shown in figure 6.11.

During the fabrication of these devices, several problems were encountered which seriously impeded the production of potentially working integrators. A considerable amount of effort was required to overcome these difficulties which are discussed briefly below:

(i) Mask Resolution: As already indicated, in order to minimize the gate lengths of the RGR, the storage areas had to be designed with geometries as small as 4μm. Since mask production involved at least one contacting stage before step-and-repeating and three afterwards, considerable care had to be exercised at each stage, in order that the small features were accurately defined and that defects due to dust or emulsion blemishes, etc, were suppressed.

(ii) High Threshold Voltages: At the time that these devices were being processed, it became impossible to fabricate aluminium gate MOS devices with threshold voltages on the thin and thick oxides of less than ≈12V and ≈25V respectively. Attempts to isolate the cause of this problem by running process check slices containing MOS capacitors proved futile, since these could be fabricated with the expected threshold voltages (≈2V and ≈6V) consistently! Extensive efforts were made to improve processing cleanliness, particularly during the photomechanical and etching stages, e.g. the etching of phosphorous doped oxide and ordinary oxide was carried out in separate beakers. Experiments on the faulty devices established that phosphorous auto-doping during fabrication steps subsequent to the n+ diffusion step were not

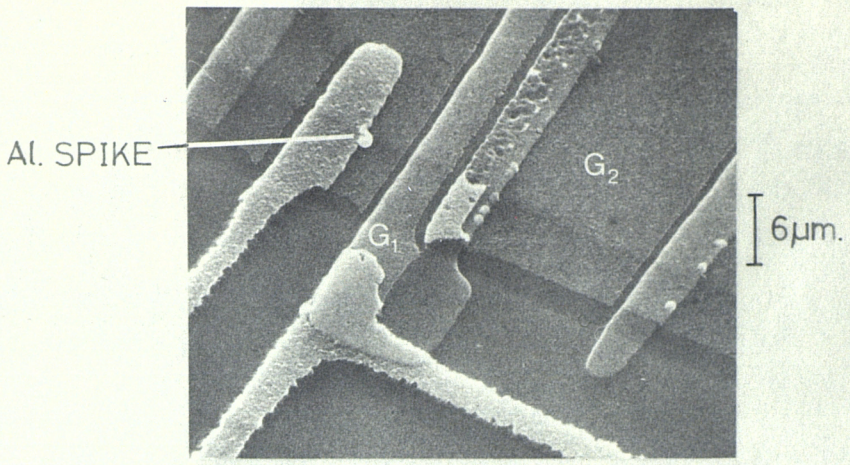

Fig 6.10 An SEM photograph of the minimum geometry gate G_1. Several aluminium spikes can also be seen.

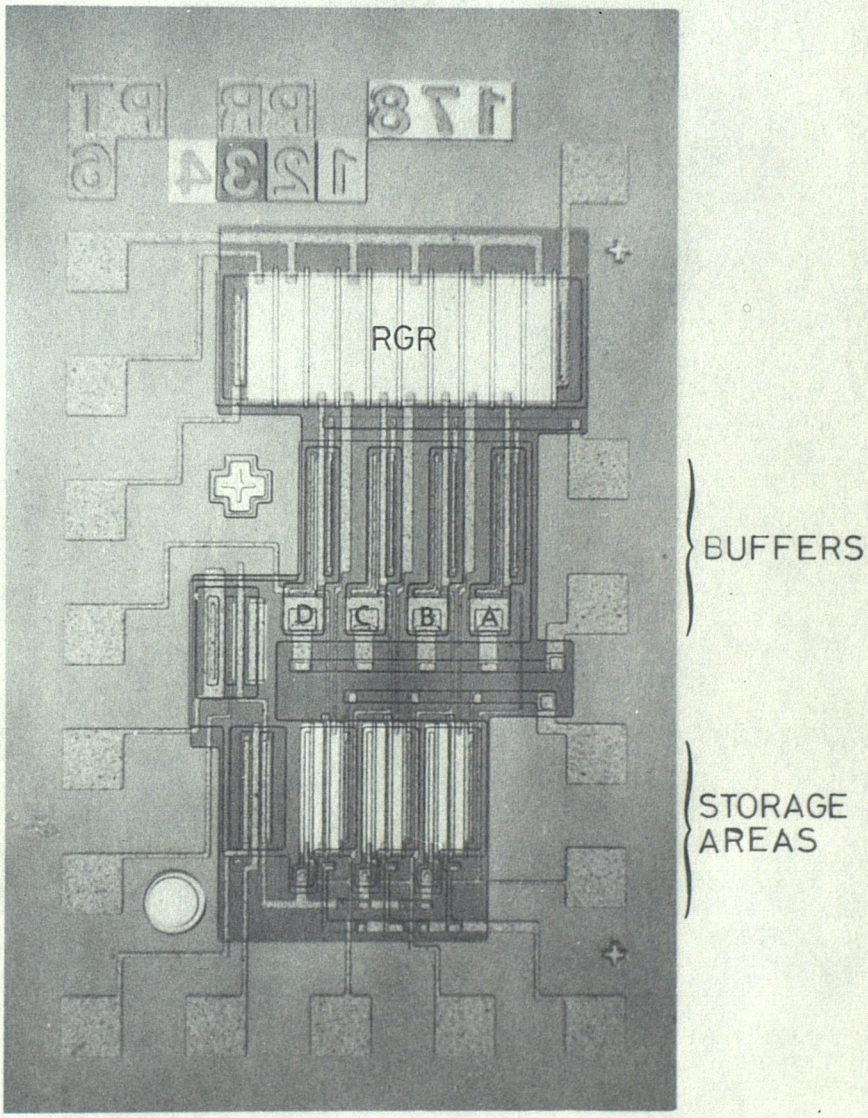

Fig 6.11 A photograph of the recursive test device.

taking place. The cause was finally attributed to sodium contamination of the oxide at the aluminium evaporation stage, when it was learned that the tungsten heating spirals in the evaporator were saturated with sodium as a necessary part of their production. Indeed, the acquisition of an E-gun evaporator in which the aluminium was evaporated from a carbon crucible enabled low threshold devices to be fabricated consistently. Furthermore, the threshold variations over a 2" wafer could be kept relatively low with this system, e.g. 2V ± 0.2V and 6V ± 0.5V for the thin and thick oxides respectively. Unfortunately the apparent cause of the problem (i.e. sodium contamination) is not entirely consistent with the fact that capacitors could be successfully fabricated using tungsten evaporated aluminium. The reason for this has not yet been established.

(iii) Aluminium Spikes: As was mentioned above, the aluminium source in the E-gun was contained in a carbon crucible. However, each carbon crucible lasts only several evaporations since the molten aluminium tends to 'soak' into the carbon and pulverise it. Also, during the life of a carbon crucible, the evaporated film thickness varies considerably and is particularly 'grainy'. These features are undesirable, especially for the three-phase shadow technique used to fabricate the input gate G_1, since the gap is dependent upon the height and shape of the aluminium step. The use of cermet crucibles enabled more reproducible and uniform aluminium films to be evaporated, but during subsequent low temperature alloying and annealing treatments,* a considerable number of aluminium 'spikes' grew out of the aluminium layer (see figure 6.10), and produced visible shorts between the electrodes of the CCD structures. The size and number of spikes increases with temperature and time of the heat treatment. The cause of

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* The annealing treatment after evaporation was necessary to remove X-ray damage produced in the E-gun.

this phenomena is contamination of the aluminium from interaction with the crucible, and possibly also due to the evaporation of the cermet since it has been observed that the lip of the crucible becomes eroded after prolonged use. Careful observation has in fact shown that most crucibles (e.g. carbon, boron nitride) produce this effect to some extent and the most promising solution appears to be the use of aluminium oxide crucibles, or preferably a water-cooled 'hearth' type E-gun.

(iv) Scribing and Mounting: Testing procedures subsequent to bonding revealed that many devices had failed due to inter-electrode shorts caused by conductive dust particles (e.g. silicon) wedged in the sub-micron inter-electrode gap region. Thus a special procedure was developed to prevent damage to the gaps during scribing and mounting. It entailed covering the active area of the wafer with a positive photoresist pattern (using the final aluminium mask) before scribing. After scribing, the wafers were first cleaned upside-down in an ultrasonic water bath and then the defective devices were ink-spotted. The wafer was then broken up and the individual chips mounted onto headers with silver loaded Araldite and baked for 30' at 150^{o}C. Then just prior to bonding, the devices were ultrasonically cleaned upside-down in acetone. A modification of this technique in which the active area is permanently enclosed in aluminium oxide is under consideration.

6.5 Summary

In this Chapter, the operation of a recursive integrator to test the performance of the RGR and the storage sites has been described in detail, together with the design procedure of the test device.

In the next Chapter, the results obtained from experiments on this device are presented.

CHAPTER SEVEN

TEST INTEGRATOR RESULTS

7.1 Introduction

In this Chapter the results of experiments performed on the test integrator will be presented. They are divided into three sections: in the first and second sections the floating-gate tap transfer response (quasi-static operation of the RGR), and the dynamic operation of the RGR will be described. Details of the storage sites will be discussed in the third section.

7.2 The Quasi-Static Operation of the RGR

Before detailed measurements of the operation of the test devices were undertaken, the device parameters were first established. These are listed below:

	Specification	Measured	Units
Substrate doping level, N_D	1.8×10^{15}	--	cm^{-3}
Thin oxide depth, t_{OXTN}	0.12	0.11	μm
Thick oxide depth, t_{OXTK}	0.5	0.51	μm
V_{OTN}	0.35	0.29	V
V_{OTK}	6.08	6.32	V
Thin oxide flatband voltage, V_{FBTN}	1	1	V
Thick oxide flatband voltage, V_{FBTK}	4.5	4.5	V
RGR gate capacitance, C'_{ox}	2.53	3.04	pF
Floating-gate stray capacitance, C_s	0.63	1.33	pF
M	0.25	0.44	--

The oxide thicknesses were determined during processing by observing the colour of the oxide, and the flatband voltages were calculated from measurements of the threshold voltages of MOSTs fabricated on the thin and thick oxides. It can be seen that the floating-gate loading factor, M, is larger than expected. This was due to an increase in area of the gate of the buffer driver-MOST which occurred during mask production. The capacitances C'_{ox} and C_s were calculated from the dimensions of the RGR and buffers measured on large photomicrographs of these features.

The object of the experiments presented in this section was to investigate the transfer response of the RGR floating-gate taps. The experimental approach was to transfer a series of variable sized charge packets along the RGR, then by characterizing the inverters, the floating-gate transfer response could be determined. Since the buffers are employed primarily to reduce capacitive loading on the RGR taps, there are no external connections to the buffer input; thus the transfer response of the buffers could not be readily determined. In fact, the only way to gain access to the buffer inputs was to short the floating taps to the ϕ_1 electrodes (figure 6.11), consequently destroying the RGR. Thus an experiment on a device could only be carried out once. In spite of this difficulty, experiments were performed on several devices and consistent results were obtained. The experimental set-up is shown in figure 7.1. To evaluate the quasi-static performance of the RGR, the input diode was connected to a variable voltage source in series with an RC network. The charge being injected and transferred in the RGR could be calculated by measuring the voltage drop across the resistor with a DVM. The relationship between the charge, Q_{in}, and the voltage drop, V, can be derived as follows. The charge being injected into the device gives rise to a current, i, flowing through the RC network. This current is given by

$$i = \frac{V}{R} + \frac{Cdv}{dt} \qquad 7.1$$

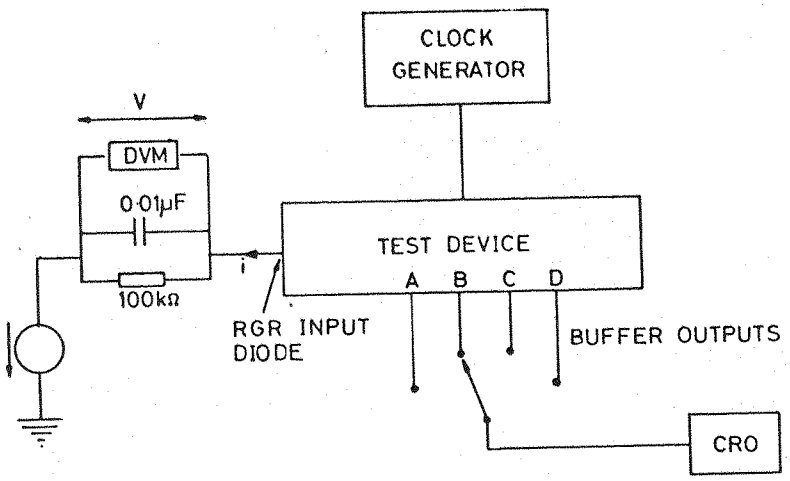

Fig 7.1 The experimental set-up to measure the transfer response of the RGR floating gate taps.

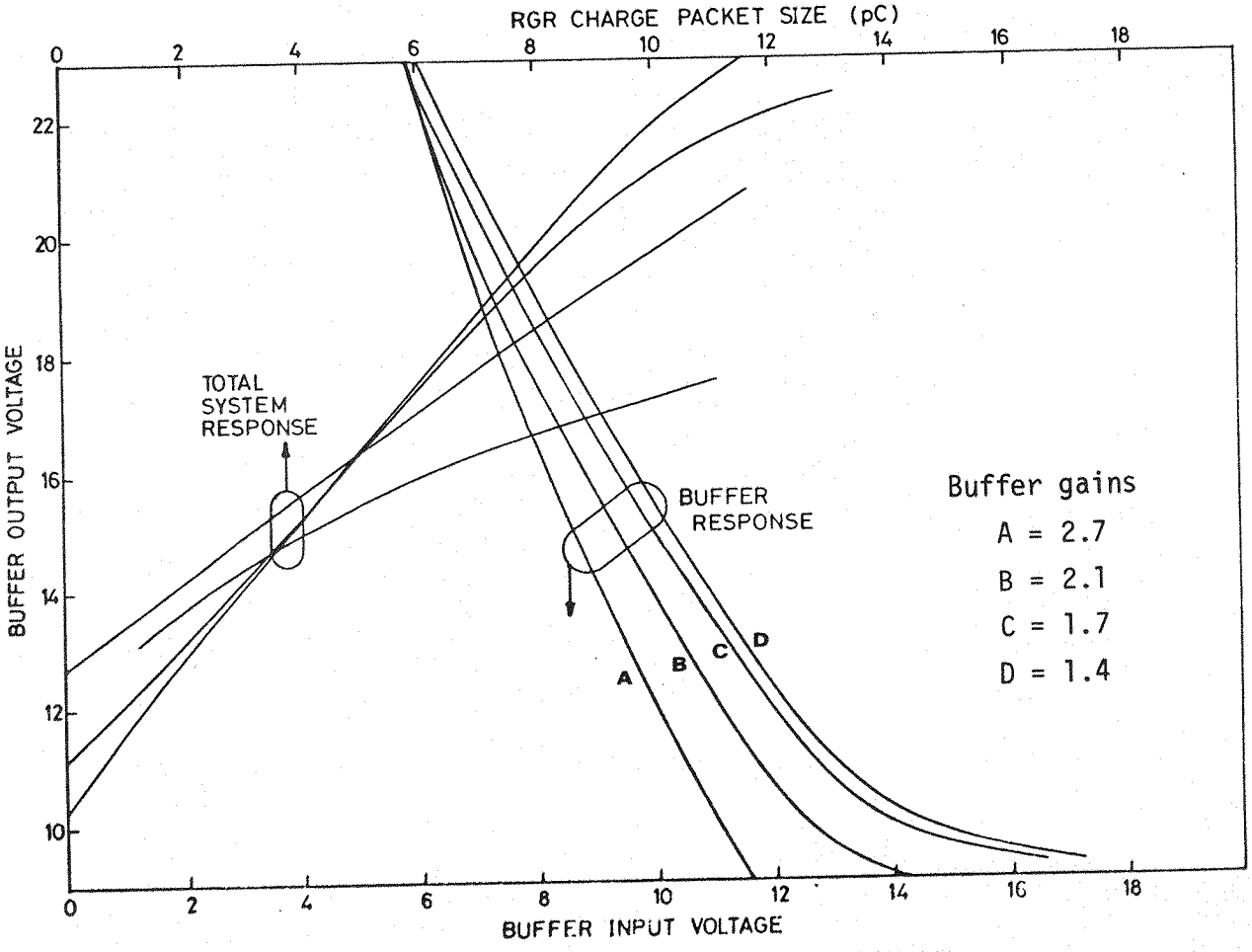

Fig 7.2 The transfer response of buffers and of the overall system, ie the RGR and buffers.

If the RC time constant is sufficiently long compared with the clock period, then $\frac{dv}{dt} = 0$. Thus

$$Q_{in} = \frac{V}{R} T_c \qquad 7.2$$

where T_c is the clock period.

The absolute voltage levels at the buffer outputs were measured on a Tektronix 7704A oscilloscope with a 7A18 plug-in. A source bias was applied to the buffer drivers and adjusted to ensure that the MOSTs were always operating in saturation over the complete range of floating-gate potential variation, thus providing maximum sensitivity. In figure 7.1, the buffers are designated 'A' to 'D', 'A' being nearest the input of the RGR.

In order to characterize the buffers, the floating electrodes were shorted to the ϕ_1 electrodes with silver-loaded Araldite; a variable voltage source was then connected to ϕ_1 whilst the buffer outputs were monitored on the oscilloscope. In the discussion on the RGR design in section 6.3.3, it was indicated that an incomplete transfer mode of operation could occur in the RGR which would limit the maximum transferable charge. In order that the floating-gate response could be investigated over a relatively large range of charge packet sizes, incomplete transfer was suppressed by operating the device with a zero offset clock. Consequently when ϕ_1 switched off, the stored charge was forced to transfer to beneath the floating electrodes, any excess recombining in the substrate. The clock amplitude was 27.5V; details of the clock generation circuitry are given in Appendix 5.

Care had to be taken when analysing the results of experiments on the RGR, since two effects were observed that could cause errors. The first was due to clock feedthrough via inter-electrode capacitance, and the second arose because of accumulation

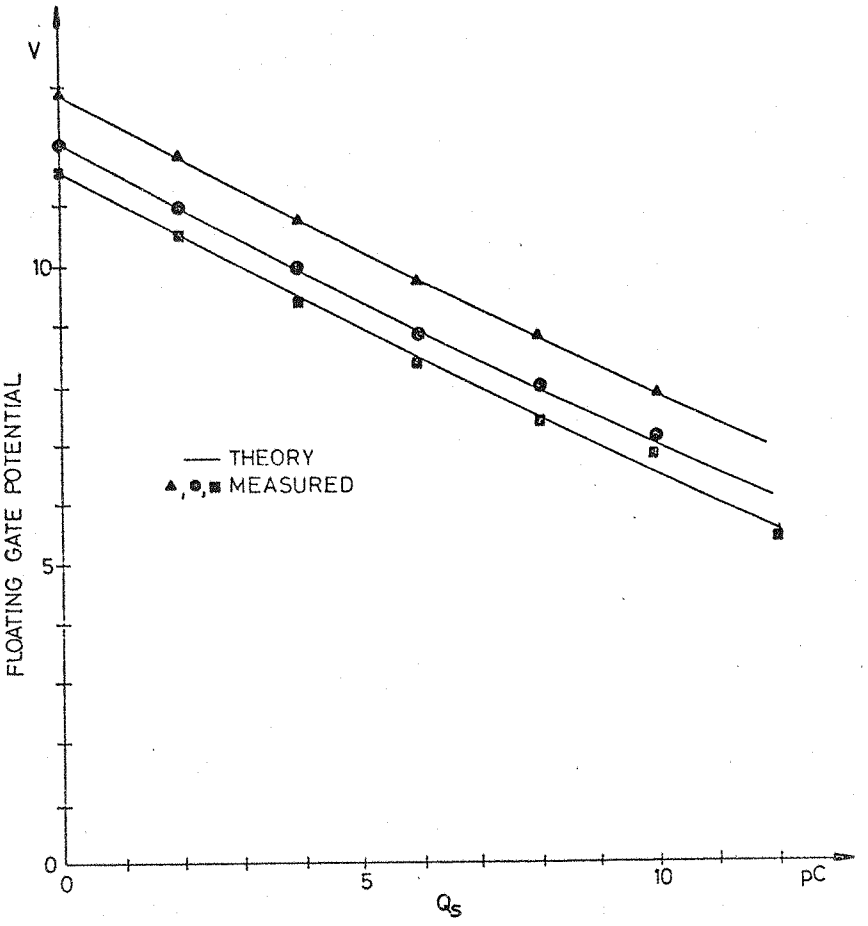

Fig 7.3 A comparison of the measured and theoretical response the floating taps.

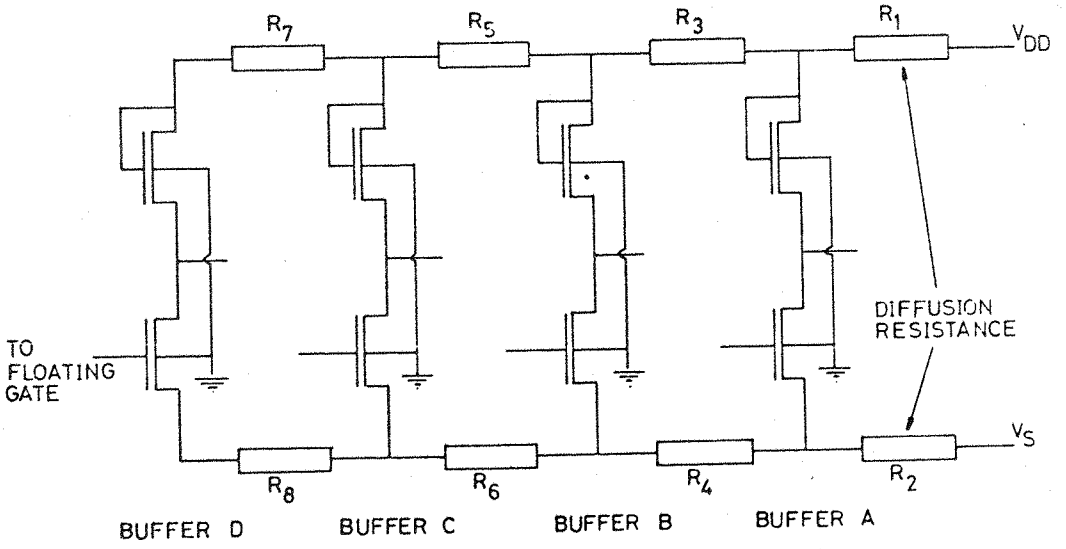

Fig 7.4 The equivalent circuit of the buffer array on the test device including the V_{DD} and source bias bus diffusion resistance.

of charge beneath the floating electrodes due to dark current generation. Both these effects caused a small output to appear when the RGR input was biased off. Although the output due to dark current generation could be identified and suppressed by increasing the clock frequency, both effects could be compensated by simply subtracting the output produced with no charge injected into the RGR from the regular output.

Measurements were undertaken on several devices, and typical results are presented in figure 7.2 and figure 7.3. The transfer responses of the buffers of one device are plotted in figure 7.2, together with the overall transfer response of the RGR and the buffers. The measured transfer response of some floating-gate taps are shown in figure 7.3, the theoretical response is also plotted (continuous curves). It can be seen that the model gives a very close fit to the measured response, and this led the author to feel confident that the model could be used to design subsequent devices.

Two anomalous effects were observed during the experiments and these can be seen in figure 7.2. It is evident that the gains of the inverters differ from each other in spite of the fact that they all have the same geometries. Furthermore, on all the devices tested, the gains consistently decreased from buffer A to buffer D. The dominant cause of this was thought to be the resistance of the underpass diffusions providing the source bias to each driver, and the supply voltage V_{DD}. This hypothesis was investigated using the equivalent circuit shown in figure 7.4 of the buffer array; the resistances R_1, R_2, ... R_8 represent the appropriate diffusion resistances. In order to simplify the analysis, however, only a single buffer was considered using the circuit shown in figure 7.5. If the MOSTs are assumed to operate in saturation, then the equations describing this circuit are as follows

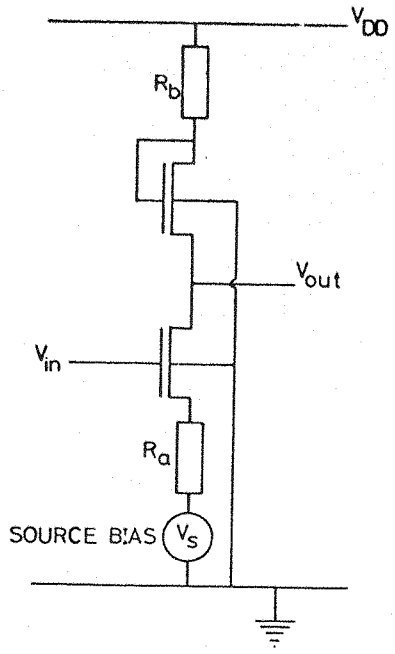

Fig 7.5 The equivalent circuit of the single buffer used in the analysis.

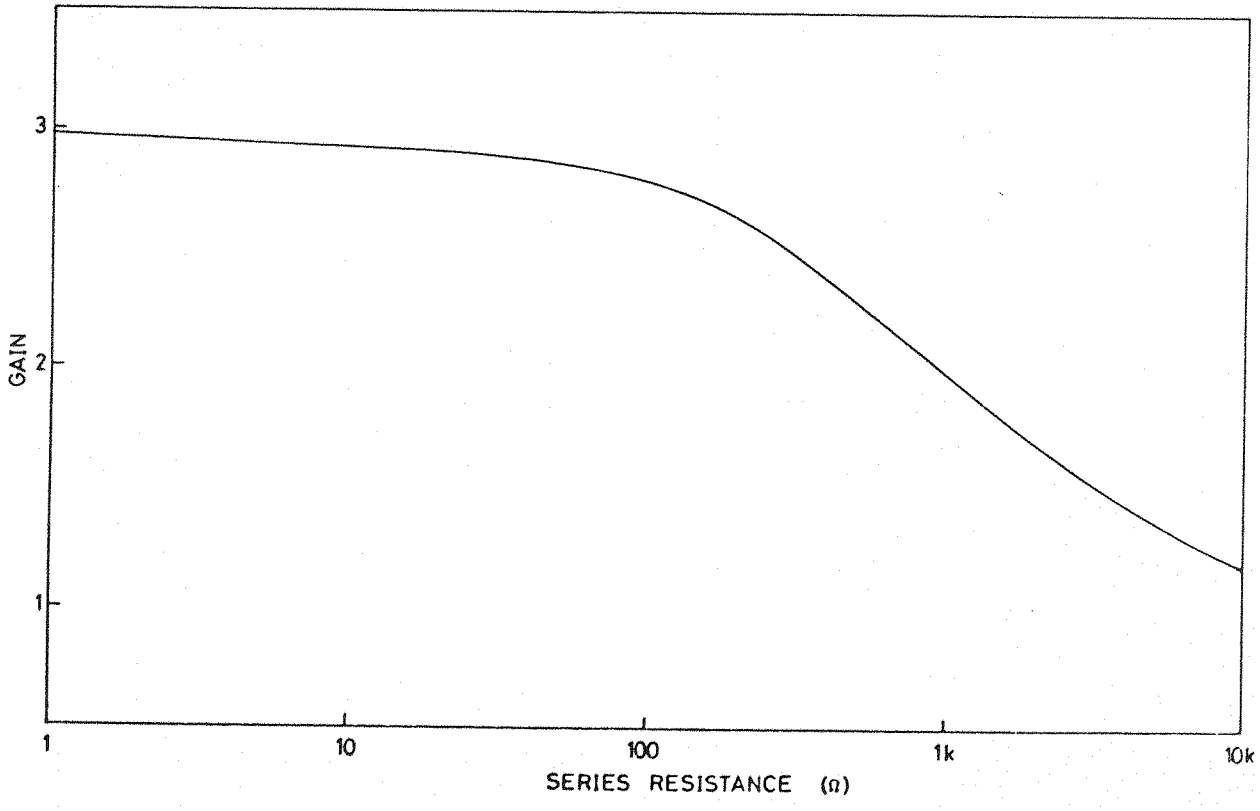

Fig 7.6 The theoretical variation of buffer gain as a function of series resistance.

$$I_D = \frac{\beta_1}{2} (V_{in} - I_D R_a - V_s - V_T - \Delta V_{T_1})^2 \qquad 7.3$$

$$I_D = \frac{\beta_2}{2} (V_{DD} - I_D R_b - V_{out} - V_T - \Delta V_{T_2})^2 \qquad 7.4$$

where $\Delta V_{T_1} = \sqrt{2V_o} \left(\sqrt{I_D R_a + V_s + 2\phi_f} - \sqrt{2\phi_f} \right)$ 7.5

and $\Delta V_{T_2} = \sqrt{2V_o} \left(\sqrt{V_{out} + 2\phi_f} - \sqrt{2\phi_f} \right)$ 7.6

where I_D is the drain current of each transistor,

β_1 and β_2 are the gains of the driver and load MOSTS respectively,

V_{in} is the buffer input voltage,

R_a, R_b are the underpass diffusion resistances associated with driver and load respectively,

V_s is the driver source bias,

V_T is the threshold voltage of each transistor,

and ΔV_{T_1} and ΔV_{T_2} are the threshold increases due to back-gate bias.

The parameters β_1 and β_2 were calculated using geometries measured from large photographs of the buffers; the mobility was 206cm^2/V-s which was calculated from the V_g versus $\sqrt{I_D}$ characteristic of another more easily accessible MOST on the device. The equations 7.4 to 7.6 are more easily evaluated, for various values of R_a and R_b by solving for V_{in}; this was considerably further simplified by employing the computer program detailed in Appendix 3.

Figure 7.6 shows a plot of the theoretical voltage gain variation as a function of series resistance, when $R_a = R_b$. Direct measurement of the series resistance associated with each buffer shows that in figure 7.4

$$R_1 = R_2 = 2.1k\Omega$$
$$R_3 = R_4 = 1.6k\Omega$$
$$R_5 = R_6 = 1.6k\Omega$$
$$R_7 = R_8 = 1.7k\Omega$$

To predict the gain of each buffer, these values must be modified to take into account the interaction of the buffers via the series resistances. To a first approximation, if the currents drawn by each buffer are approximately equal, then R_1 and R_2 must be increased by a factor of four, R_3 and R_4 by a factor of three and R_5 and R_5 by a factor of two; i.e. since R_1 and R_2 supply current to four buffers, the voltage drop across them will be four times the magnitude caused by a single buffer, etc. Thus the effective series resistances for each buffer are

	Buffer A	Buffer B	Buffer C	Buffer D
$R_a = R_b$	8.4kΩ	13.2kΩ	16.4kΩ	18.1kΩ

However, if these values are inserted into equations 7.3 to 7.6, the calculated gain is considerably smaller than the measured values, as seen from figure 7.6. The reason for this has yet to be established, but the indication of the analysis is that the progressive reduction in gain of buffer A to buffer D is caused by series resistance.

The second effect is associated with the resting potential of the floating electrodes. The mark space ratio of the 27.5V amplitude clock was 1.3 : 1; thus the resting potential of the floating electrodes should be 15.6V according to the simple theory. However, it can be seen from figure 7.3 that the measured values differ significantly from the theoretical value. In deriving the simple model of the floating-gate structure in section 6.3.3, the

gate leakage was assumed to be considerably smaller than the inter-electrode leakage; this assumption may in fact be invalid for very low humidity ambients. To investigate this possibility, further consideration was given to the floating-gate structure.

The gate to substrate leakage resistance of a floating-gate tap can be calculated using the bulk resistivity of SiO_2, typically > $10^{16}\Omega$cm,[88] to be > 1.2 . $10^{15}\Omega$. However, the sheet resistivity of the oxide may vary from 8 x $10^{18}\Omega/\square$ at 40% humidity to $10^{15}\Omega/\square$ at 100% humidity,[89] thus a simple calculation using the dimensions shown in figure 7.7 for a typical oxide step, shows that the inter-electrode resistance can vary between ≃ 5.5 x $10^{15}\Omega$ and 5.5 x $10^{12}\Omega$ for 40% and 100% humidity respectively.

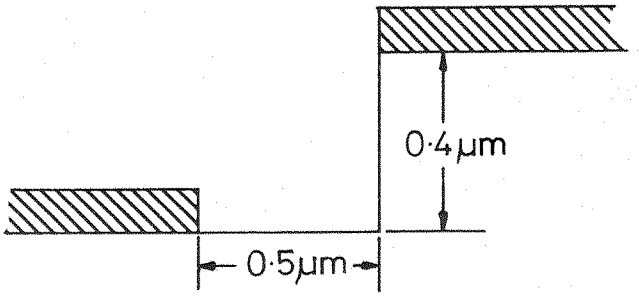

Fig 7.7 A simple model of the oxide step and the shadowed inter-electrode gap

For a typical humidity of 70%, the inter-electrode resistance will be ≃ 5 x $10^{14}\Omega$. So for the clock amplitude specified above, the resting potential of the floating electrodes will be ≃14V. Clearly then, the value of resting potential will depend upon humidity, and for individual electrodes upon the shape of the inter-electrode gap; it was found that in general the resting potentials of the floating electrodes of an RGR differed by

approximately 0.8V. Although tap-to-tap voltage variations are likely to cause fixed pattern noise in the stored signal, it was decided to postpone the treatment of this topic to a later stage, when the feasibility of CCD parallel processing architectures had been well established. However, some thought was given to how the floating-potential could be more reliably defined. For instance, the effects of gate to substrate leakage could be considerably reduced if the DC coupling between electrodes was increased. This could be done for example, by depositing a thin layer (≃0.1μm) of silicon onto the oxide surface before the first aluminium evaporation. Such a modification would also reduce short-term variation in floating potential due to local humidity fluctuations (although there was no evidence that this occurred).

7.3 The Dynamic Operation of the RGR

Figure 7.8 shows the dynamic operation of the RGR when propagating a single charge packet; the waveform at the top is the input pulse applied to the RGR and the inverter outputs are shown below. The small trailing pulse is caused by incomplete transfer, as discussed previously. The clock waveform has been offset by 4V to demonstrate this effect which becomes more pronounced as the charge packet size is increased (figure 7.9). As was discussed in the last section, incomplete transfer can be suppressed by operating the device with a below-threshold offset clock. A second method, involving separating the thick and thin oxide regions of the floating electrodes, will be discussed in the next Chapter.

The transfer inefficiency of the RGR was determined by monitoring the output from the first floating-gate buffer, i.e. buffer A. Accurate measurements of this parameter were difficult since the charge packet size had to be kept small to minimize incomplete transfer effects.* Thus the magnitude of the main pulse

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* If charge is trapped in the source well, the last stages of 'free' charge transfer are slowed down, thus causing an increase in the intrinsic transfer inefficiency.

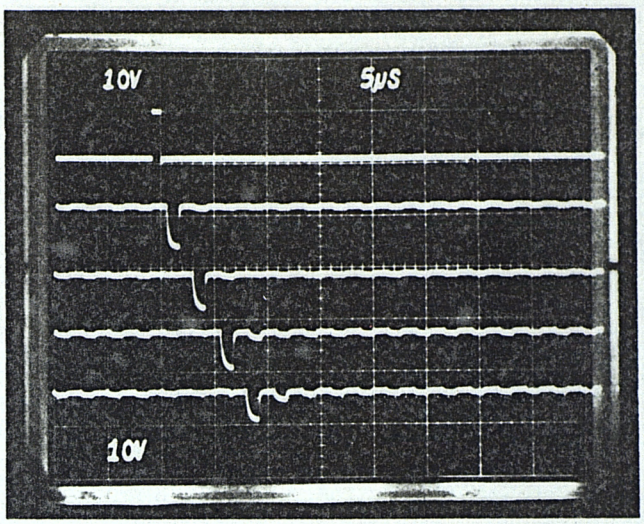

Fig 7.8 An oscillograph of the dynamic operation of the RGR. The scale is as shown.

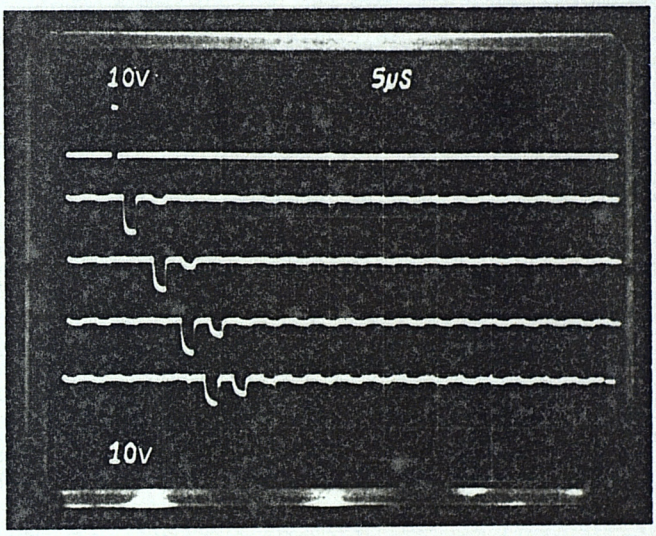

Fig 7.9 The dynamic operation of the RGR showing incomplete transfer. The scale is as shown.

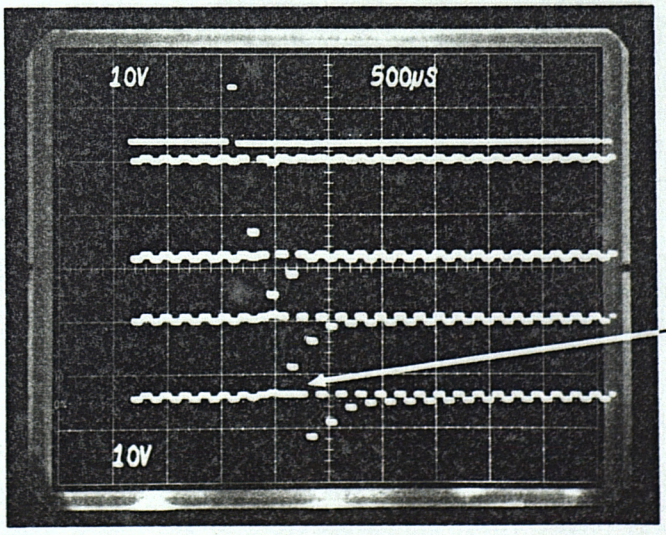

Fig 7.10 An oscillograph of the RGR operation showing the feedthrough of pulses from adjacent buffers

at the buffer output was of the order of 1V. Since the charge packet had only undergone a single transfer at this stage, if a transfer inefficiency of 10^{-3} was to be measured, a trailing pulse amplitude of the order of 1mV had to be accurately measured. Although measurements at these levels could be made, the accuracy of the results was questionable; this was because feedthrough of the main pulse from adjacent buffers partially cancelled the required waveform and so made the establishment of a reference level difficult. This cancellation effect can be seen, considerably exaggerated in the device under test, on the pulses preceding the main pulse in figure 7.10.

In spite of these difficulties, however, the transfer inefficiency at 700kHz was estimated to be less than 2×10^{-2}. As the charge packet size was increased to a level corresponding to the onset of incomplete transfer, the transfer inefficiency increased by a factor of about five. This was attributed to the fact that as the floating electrode potential swings more positive with larger charge packets, the underlying potential well 'looks' less like an infinite sink to the transferring charge.

The rise time of the buffers was measured to be ≃700ns which is in reasonable agreement with the designed value.

7.4 The Storage Sites

Unfortunately, due to a mask error, it was not possible to operate the storage sites. The error, two missing channel stop diffusions, caused parasitic MOST action between the storage site input diodes and the supply voltage distribution bus diffusion, and between the output bus diffusion and the signal input bus diffusion. Since the mask artwork was hand cut in Rubylith, it was not possible to correct the fault easily. However, since the storage sites are simply standard CCD structures, they should work satisfactorily. Furthermore, a pre-scribing wafer test procedure to establish defective devices included a test to operate the RGR

and storage sites CCDs as MOSTs. This test could be carried out satisfactorily on the storage sites since all unused pads were connected to ground; the test confirmed that each electrode of the structure could act independently as a control gate.

7.5 Conclusions

The experiments performed on the test integrator device and presented in this Chapter have established the feasibility of using a floating-gate tapped CCD as an on-chip address register. In particular, measurements on the transfer response of the floating-gate taps have demonstrated a close correlation with theory and so confirms the earlier floating-gate analysis which showed that large amplitude pulses can be generated at each tap; thus it is possible to connect the tap outputs directly to the analogue gates without intermediate amplification, and so enable the high speed capability of CCD structures to be utilized.

Although a mask fault prevented the storage sites from working, these untested functions employ conventional CCD techniques. Thus, rather than correct the fault on the existing design, it was decided to proceed with the design of a second recursive test device, incorporating several modifications arising from the experience gained from operating the first test integrator. In the next Chapter the modifications and the device design are discussed in detail, and some preliminary experimental results presented.

CHAPTER EIGHT

DESIGN AND OPERATION OF THE MODIFIED INTEGRATOR

8.1 Introduction

At the outset of the development of the parallel processing signal integrator, it was intended that CCD structures should be used exclusively to enable high speed operation to be realized. The results of experiments performed on the test integrator chip and presented in the last Chapter, demonstrated that this is possible.

This Chapter describes the design and operation of a second test recursive integrator which employs direct addressing from the RGR. Several other design modifications are also included which improve the propagation and detection of the charge in the RGR, and which could enable an increase in storage site packing density to be achieved.

8.2 The Design Modifications

The structure of the recursive integrator was modified in the following ways.

(a) Since the analogue gates are included in the structure of the storage sites, the direct addressing scheme requires a radical modification of the storage site operation, as negative logic must now be used for the addressing. A cross-section of a single storage site and its timing sequence is shown in figure 8.1; the feedback circuit is also shown in this diagram. Gates G_1 and G_3 form the input and output analogue gates respectively, and are both connected directly to the nth tap of the RGR. G_3 also serves as the storage gate for the charge metered by the input electrode G_2; the gate G_4 enables G_3 to be used for this purpose. The sequence of operation is as follows. Normally G_1 and G_3 are at a

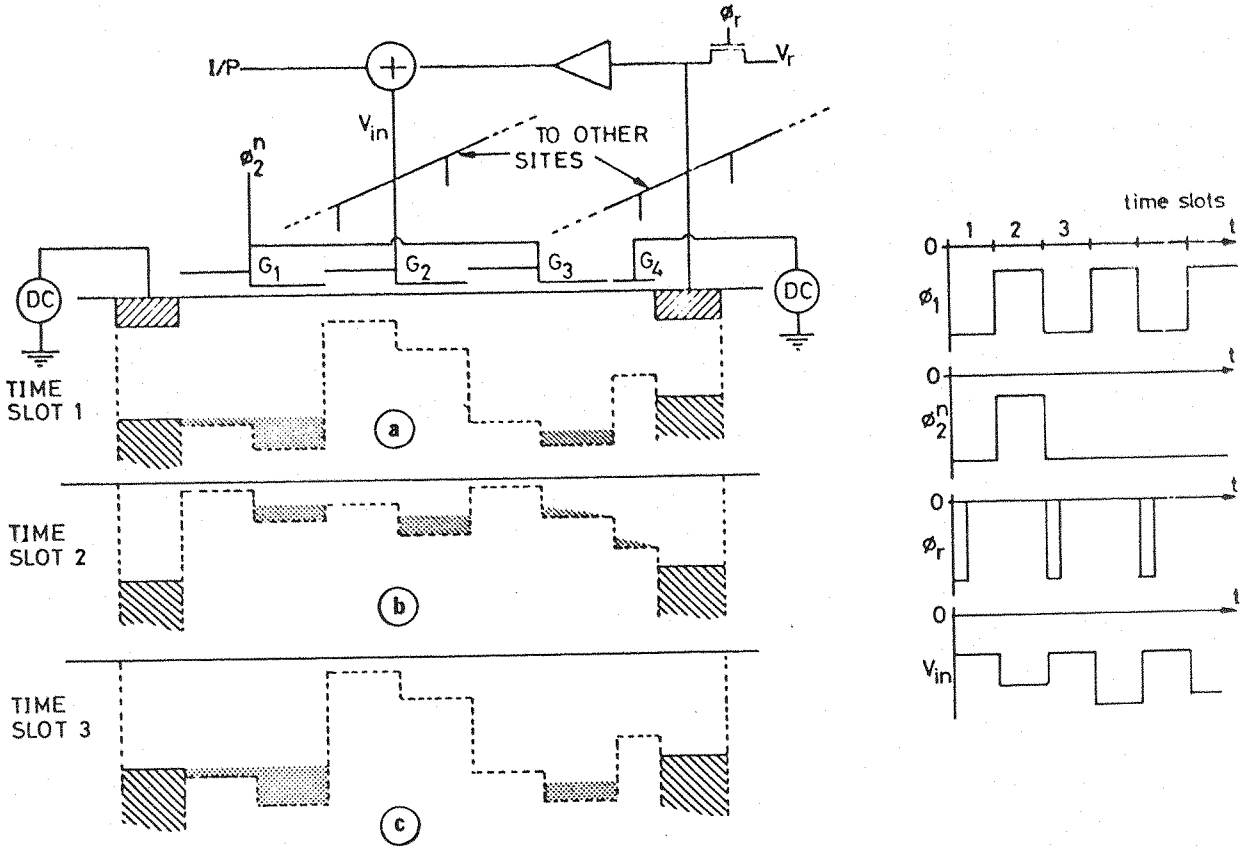

Fig 8.1 The cross-section and timing diagram for the modified recursive integrator storage site.

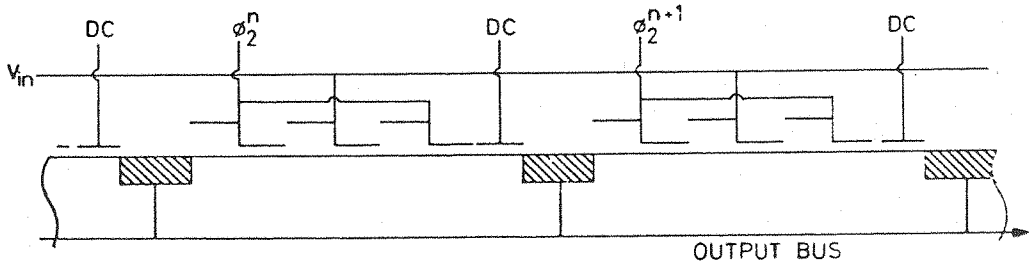

Fig 8.2 A method of increasing packing density by combining the input and output diffusions of adjacent storage sites.

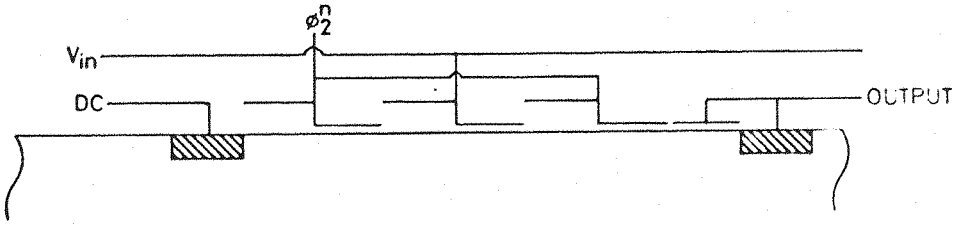

Fig 8.3 A second method of increasing packing density by biasing the output gate from the output diode.

high potential equal to the resting potential of the RGR floating electrodes (time slot 1); thus the potential well beneath G_1 is continually 'primed' with charge, and the signal charge is stored beneath G_3. When the charge packet in the RGR is transferred beneath the nth tap, the potentials on G_1 and G_3 fall and so the signal charge transfers onto the output diode (time slot 2). The output voltage is immediately summed with the corresponding range bin sample of the next radar return and the resulting signal is applied to the input gate G_2. Since the potential well beneath G_1 has collapsed to the 'supply' position, charge corresponding to the input signal is metered into the potential well beneath G_2. As the address charge is transferred along the RGR, the potentials on G_1 and G_3 rise to their original values and the updated signal charge transfers to beneath G_3, where it is again stored (time slot 3). It can be seen that storage site updating is carried out during only one clock cycle, and so a sample/hold function in the feedback circuitry is unnecessary.

(b) Two modifications to the basic storage site configuration discussed in (a) were implemented. The first modification was to fabricate the output diode of one storage site and the input diode of the next storage site as a single diffusion (see figure 8.2). This may be done since the input diode merely primes the potential well beneath G_1 and any variation of its potential, provided it is relatively small, is not critical. As a result, the storage site pitch may be reduced since a channel stop diffusion need not be fabricated between the storage sites.

The second modification was simply to bias the gate G_4 by connecting it directly to the output diode (figure 8.3) Again, this enables an increase in packing density to be achieved since an additional biasing interconnection is not required.

These modifications were implemented separately on the test device in the form of two sets of storage areas driven from

a common RGR. In this way, the operating ranges of the two types of storage site could be established and the possibility of combining the modifications investigated.

(c) Another advantage of the modified operation of the storage site is that adjacent sites do not need to be interconnected as in the previous design. Thus it is possible to position storage sites on each side of the RGR, one set of which operate from even taps and the other from odd taps. This enables the bit length of the RGR to be reduced to 50μm; the width was increased to 400μm, to ensure that the stray capacitance loading factor, M, would be small. The storage site electrodes are 100μm wide and 14μm long, 4μm of which is over thick oxide, thus M < 0.27;* the output gate, G_4, is 4μm long.

(d) So that more precise control could be exercised over the transfer of charge in the RGR, and to aid the suppression of incomplete transfer, the thick and thin oxide sections of the floating-gate were separated; the thick oxide section, referred to as the transfer gate, is externally biased to a DC level.

(e) By employing the two-phase charge injection scheme described in section 2.4.1, the charge packet size in the RGR can be more precisely controlled.

(f) The charge propagating to the end of the RGR is detected using the novel sample/hold circuit shown in figure 8.4. It consists of a floating-gate which is sensed with an MOST buffer via a triple-gate sampling MOST switch. The two outer electrodes of the MOST switch are set to a DC bias in order that sample pulse feedthrough may be reduced. The floating-gate is biased through a very low gain (6×10^{-8}S/v) MOS diode. C_F and C_B represent the

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* The stray capacitance of the floating-gate is composed predominantly of the gate capacitance of G_1 and G_3 which will vary according to the charge stored beneath them.

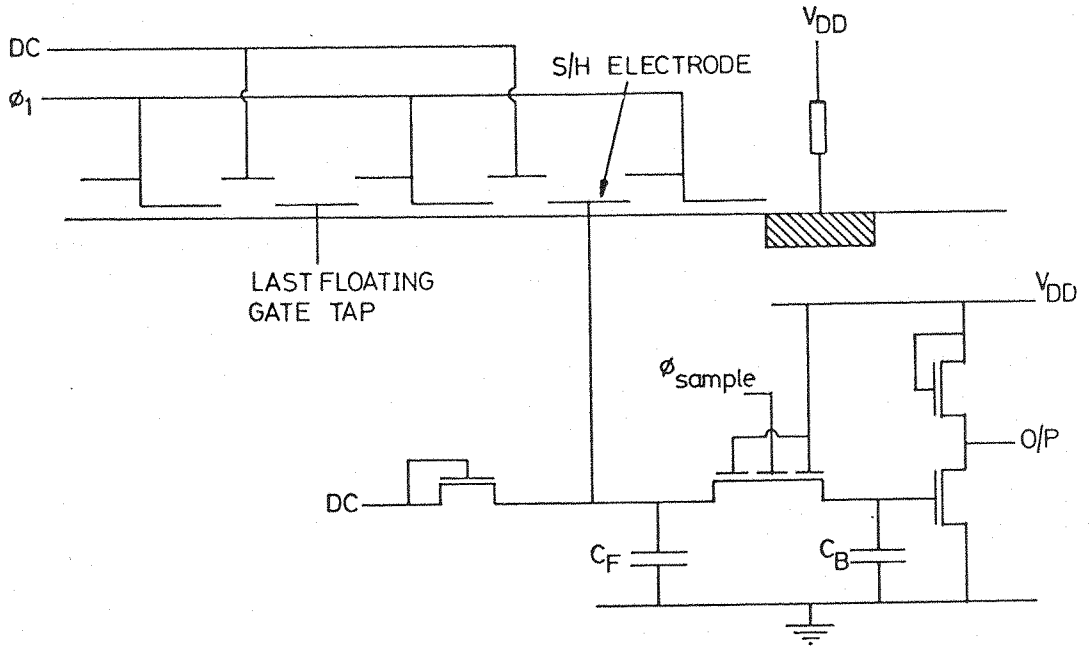


Fig 8.4 The output section of the RGR showing the sample/hold circuit.

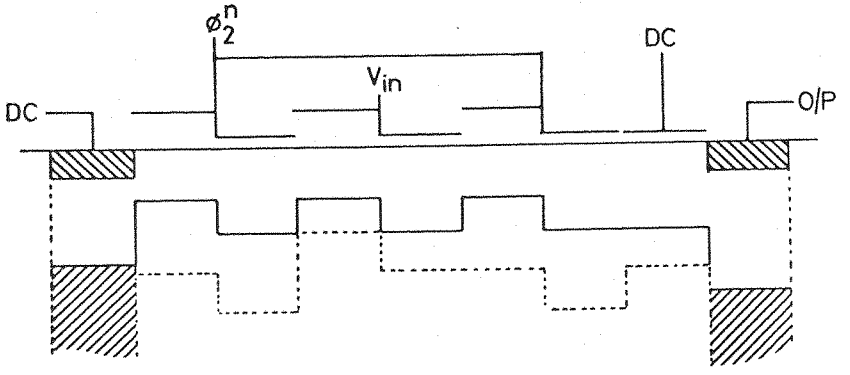


Fig 8.5 The surface potential profiles in the storage site for complete transfer and storage of a full size charge packet.

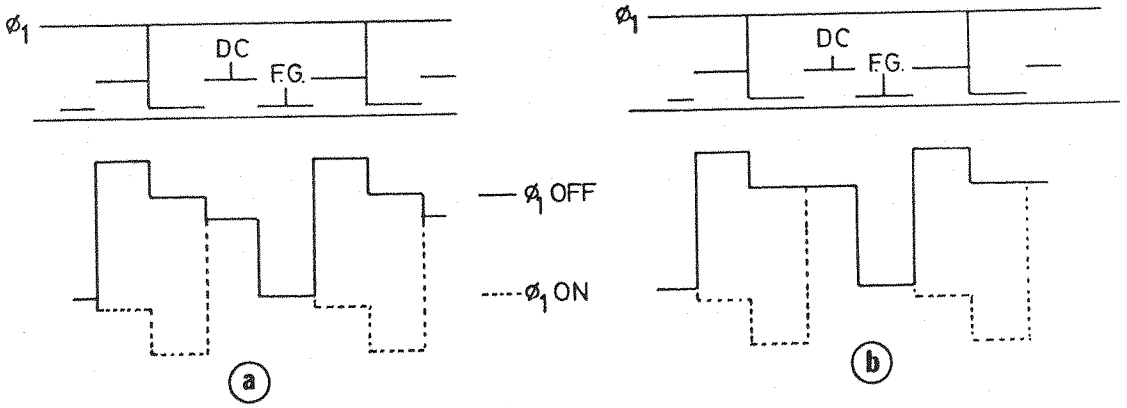


Fig 8.6 The surface potential profiles in the RGR for ϕ_1 OFF and ON. (a) is a typical biasing condition, and (b) shows the transfer gate bias set to transfer a maximum charge packet.

capacitance associated with the floating-gate and the input of the MOST buffer respectively. During operation, the total charge on C_F and C_B remains constant and simply partitions between the capacitors, depending upon the magnitude of the charge beneath the floating-gate. Redistribution of charge occurs every time the sample switch is closed.

This circuit will permit easier coupling of the address bit between chips if several devices are cascaded together. Its use as a charge detector in the non-recursive parallel processing integrators which were described in Chapter 4, is also being considered.

8.3 The Design Procedure

The design procedure for the modified integrator is made slightly easier than for the first test device since only two CCD structures need to be interfaced. Although many modes of operation are possible, by studying the operation of both the RGR and storage sites, the most satisfactory conditions can be relatively easily deduced. For example, the conditions for complete transfer in the storage sites is illustrated in figure 8.5. Again, the minimum value of surface potential that must exist beneath the storage site when G_1 and G_3 are at their maximum potential is shown as the dotted line. The maximum value of surface potential when G_1 and G_3 are at their minimum potential is shown by the continuous line.

The operation of the RGR is slightly more complex. The typical surface potential profile of the empty device is shown in figure 8.6a. It can be seen that the DC bias on the transfer gate should be high enough to ensure complete transfer from the ϕ_1 well, and that the floating-gate resting potential, or clock amplitude, should be appropriate to allow complete transfer into the ϕ_1 well. Another criterion governing the value of the DC bias on the transfer gate is the maximum size of charge packet that is required to propagate along the RGR; furthermore, the DC bias will also affect

the resting potential of the floating electrode and thus the maximum amplitude of the address pulse. Clearly there are many interrelated factors which will influence the performance of the device. For the initial design steps therefore, the biasing conditions were chosen to give the most satisfactory operation based upon an intuitive assessment.

It was assumed that a maximum sized charge packet could be transferred along the RGR, if the surface potential beneath the transfer gate was equal to the thin oxide surface potential of the ϕ_1 electrodes when ϕ_1 was OFF (see figure 8.6b). Thus for a given clock amplitude, the floating-gate resting potential can be determined (gate to substrate leakage is ignored at this stage). It is also apparent that the magnitude of the floating-gate voltage variation will be limited by the maximum charge packet that can be stored beneath the floating-gate rather than the loading capacitance (assuming the latter is small). Thus in order to calculate the amplitude of the address pulse, the maximum charge packet that could be stored beneath the floating electrode must be first determined. This can be done by rearranging equation 5.5, which, for a single gate, is

$$Q_{in} = A\sqrt{2q\epsilon_s N}\left[\sqrt{\phi_s(0,V_g(0)} - \sqrt{\phi_s(Q_{in},V_g(Q)}\right] - \left[V_g(Q) - V_g(0)\right]C_s \qquad 8.1$$

where Q_{in} is the signal charge in Coulombs and A is the electrode area. By substituting for $V_g(Q)$ and $V_g(0)$ in terms of ϕ_s and recalling that $\sqrt{2q\epsilon_s N} = C_{ox}\sqrt{2V_o}$, we can write:

$$Q_{in} = A\,C_{ox}\sqrt{2V_o}\left[\sqrt{\phi_s(0,V_g(0)} - \sqrt{\phi_s(Q_{in},V_g(Q)}\right] + \frac{A.C_{ox}C_s}{A.C_{ox}+C_s}\left[\phi_s(0,V_g(0) - \phi_s(Q_{in},V_g(Q)\right] \qquad 8.2$$

Thus by inserting the initial ($\phi_s\{0,V_g(0)\}$) and final ($\phi_s\{Q_{in}V_g(Q)\}$) values of the surface potential beneath the floating electrode into equation 8.2, the maximum charge packet can be calculated.

As discovered when designing the first test integrator, the most expedient way of determining the biasing conditions for a given set of device parameters is to use a set of design curves. These consist of plots of the surface potential beneath the thick and thin oxides as a function of gate voltage; the floating-gate potential variation as a function of signal charge,(equation 5.7), and the maximum stored charge beneath the floating electrode as a function of empty well surface potential (equation 8.2). The compatibility of the storage sites and RGR when fabricated with the standard processing schedule was investigated initially, i.e. the substrate resistivity was assumed to be 2-5Ω.cm with thin and thick oxide depths of 0.12μm and 0.5μm respectively. With a clock amplitude of 27.5V, no satisfactory biasing condition can be achieved that would ensure complete transfer in the storage sites. The obstacle to achieving this is that the surface potential differential beneath the thin and thick oxides is too large. Thus the effects of reducing this by:

(i) increasing the thin oxide depth to 0.2μm;

or by (ii) decreasing the thick oxide depth to 0.4μm

were investigated.

The design curves for case (i) are shown in figures 8.7 to 8.9, and for case (ii) in figures 8.10 to 8.12. Consider case (i) first: the design proceeds by first establishing the bias level for the transfer gate, i.e. if ϕ_1 is offset by 10V, then from figure 8.7 the DC bias should be 18.4V. If the clock amplitude is 27.5V, then the resting potential of the floating electrodes is 21.1V. Thus using figure 8.7 again, the initial and

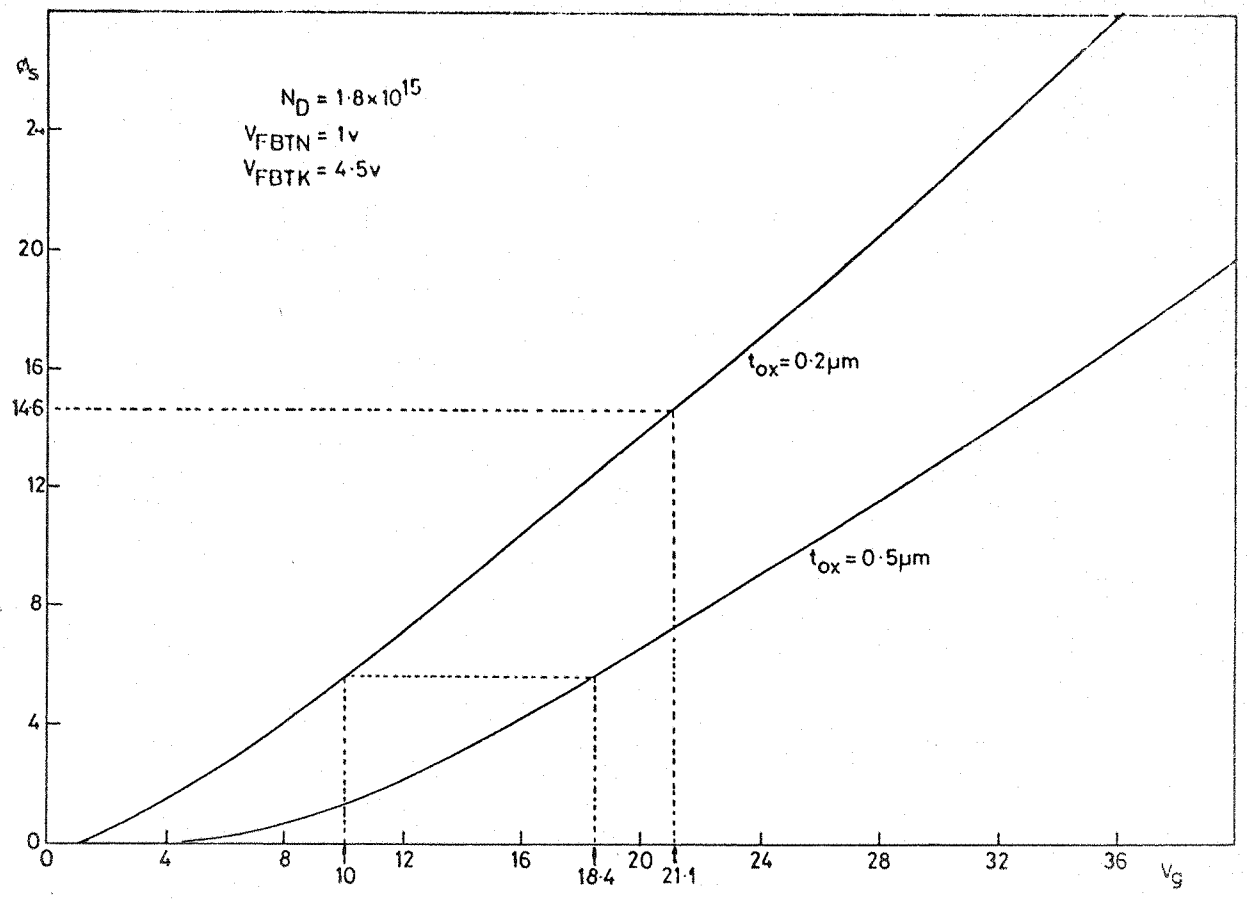


Fig 8.7 The surface potential versus gate voltage for case (i).

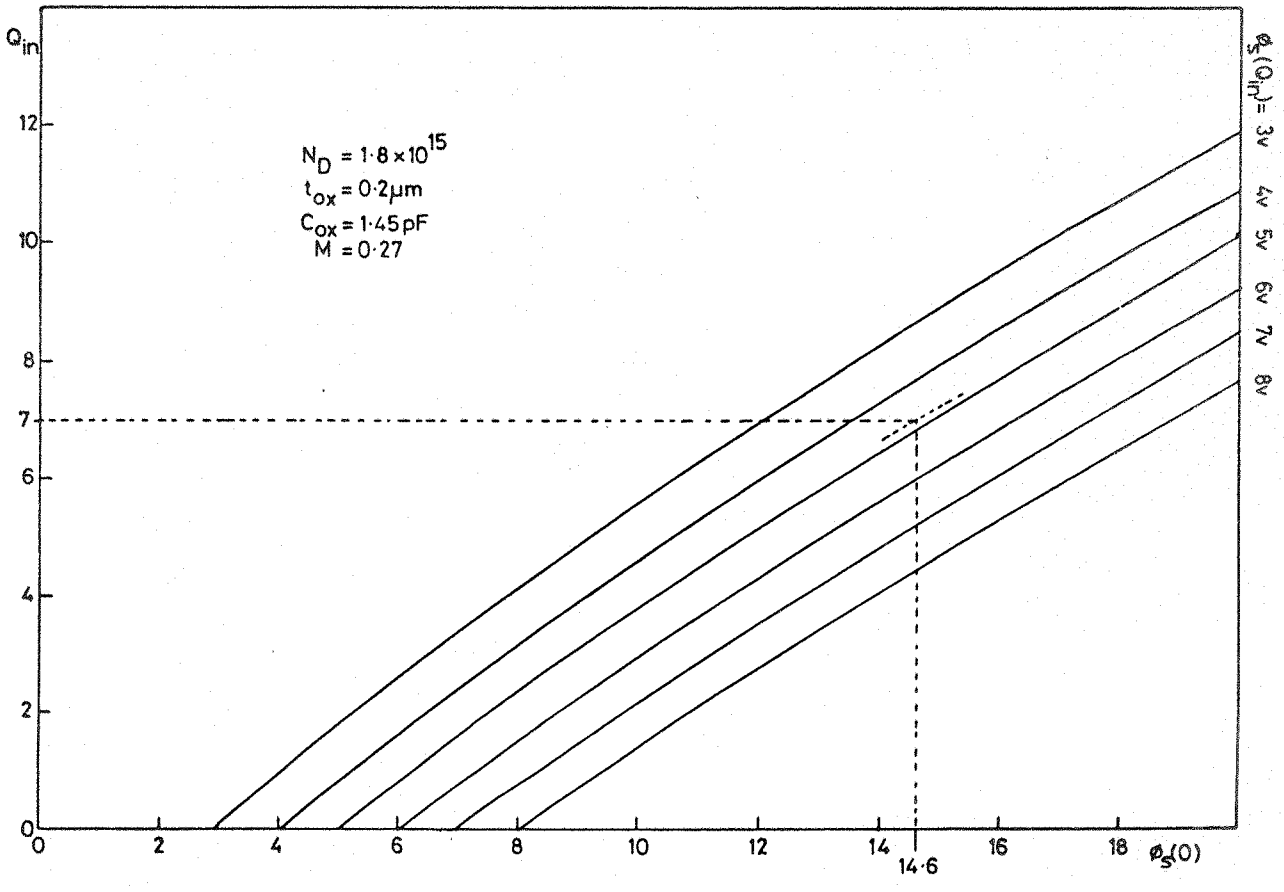


Fig 8.8 The maximum stored charge beneath a floating gate as a function of empty well surface potential; case (i).

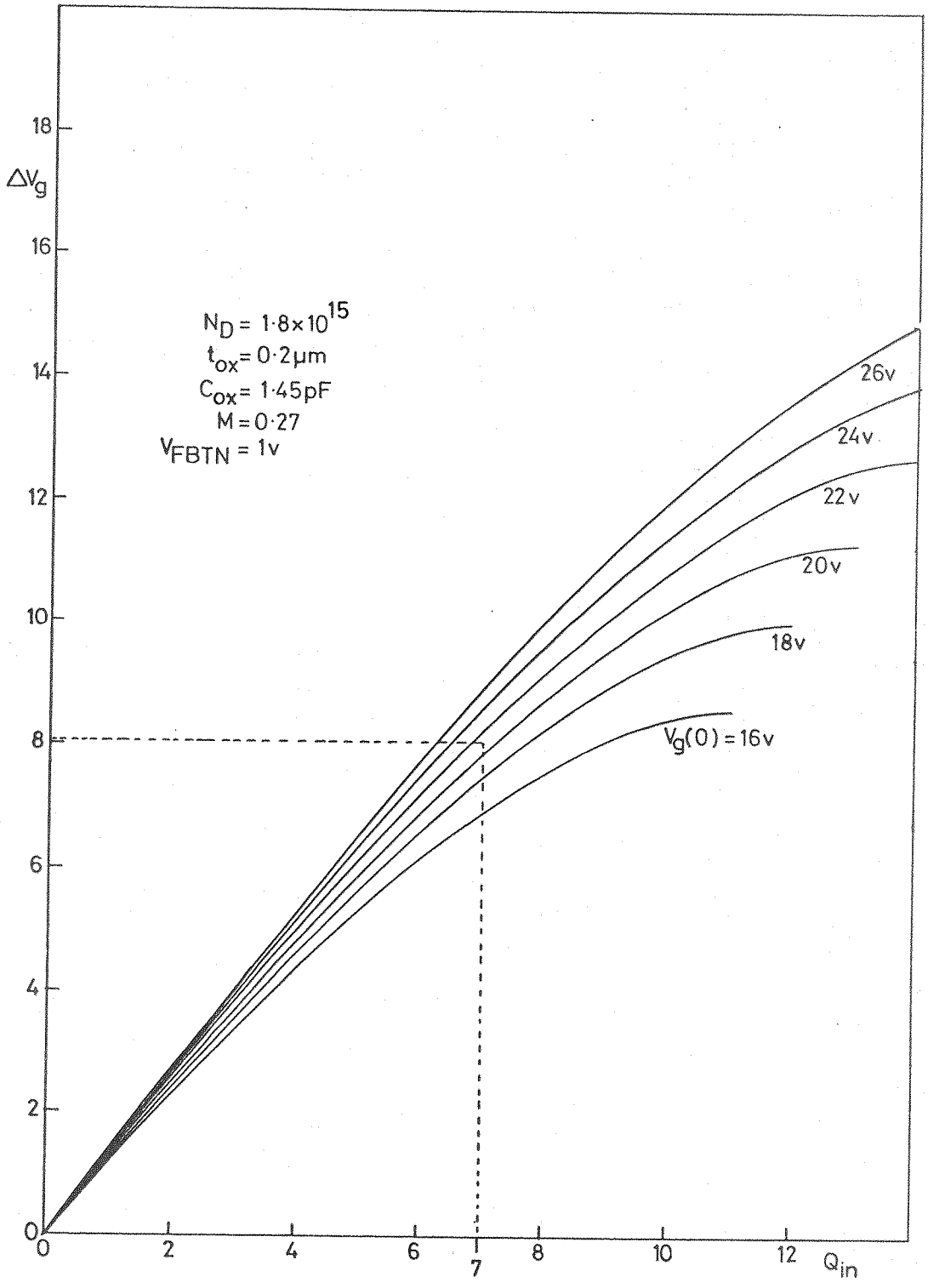


Fig 8.9 The floating gate potential variation versus stored charge; case (i).

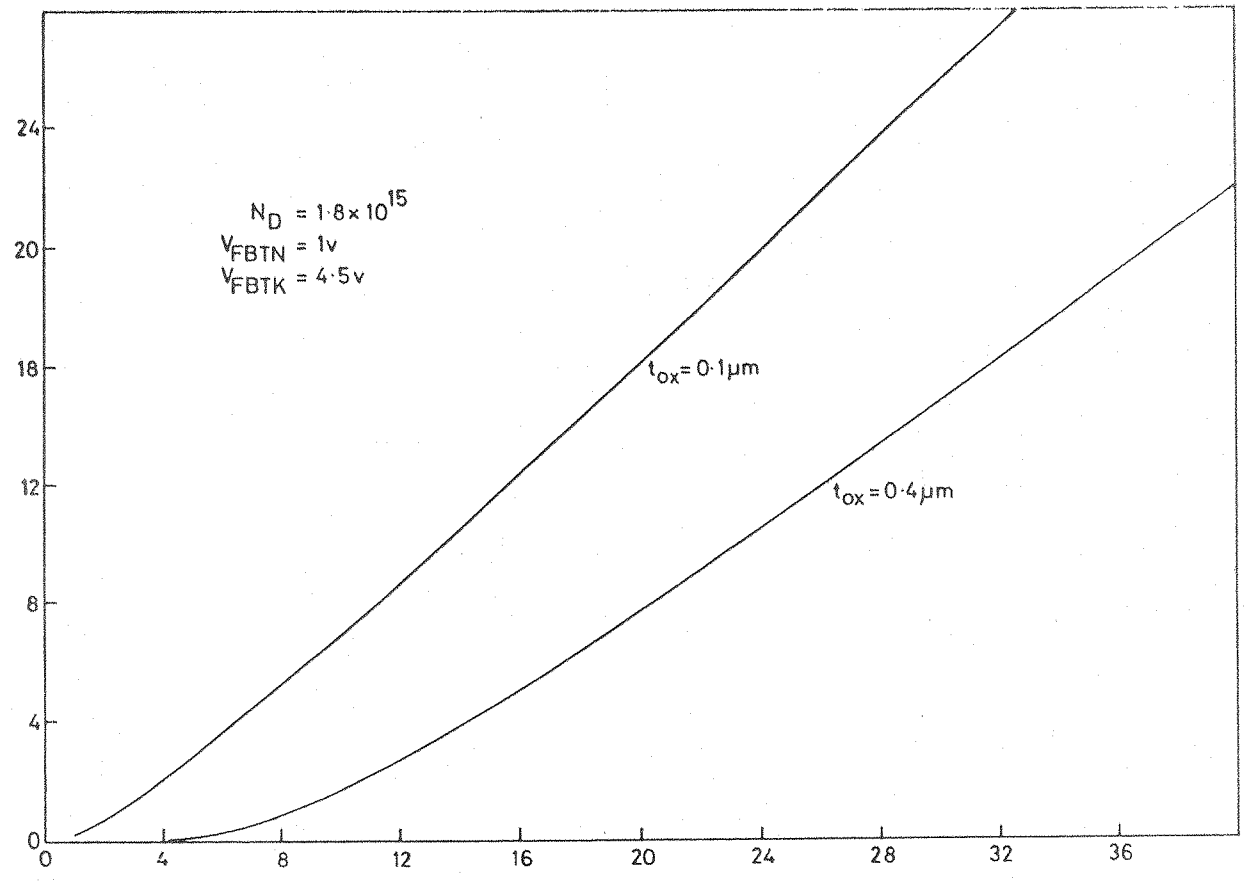


Fig 8.10 The surface potential versus gate voltage for case (ii).

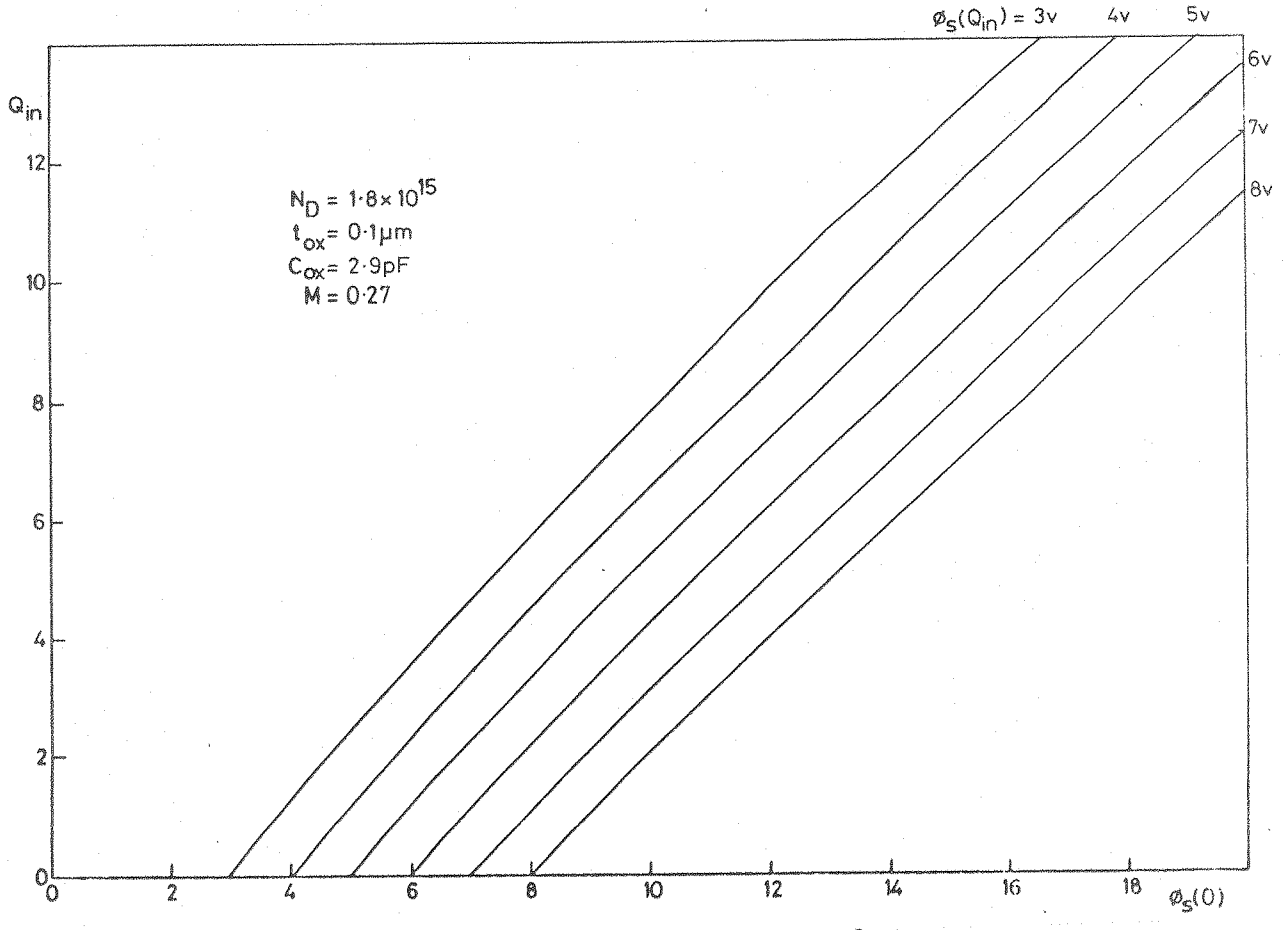


Fig 8.11 The maximum stored charge beneath a floating gate as a function of empty well surface potential; case (ii).

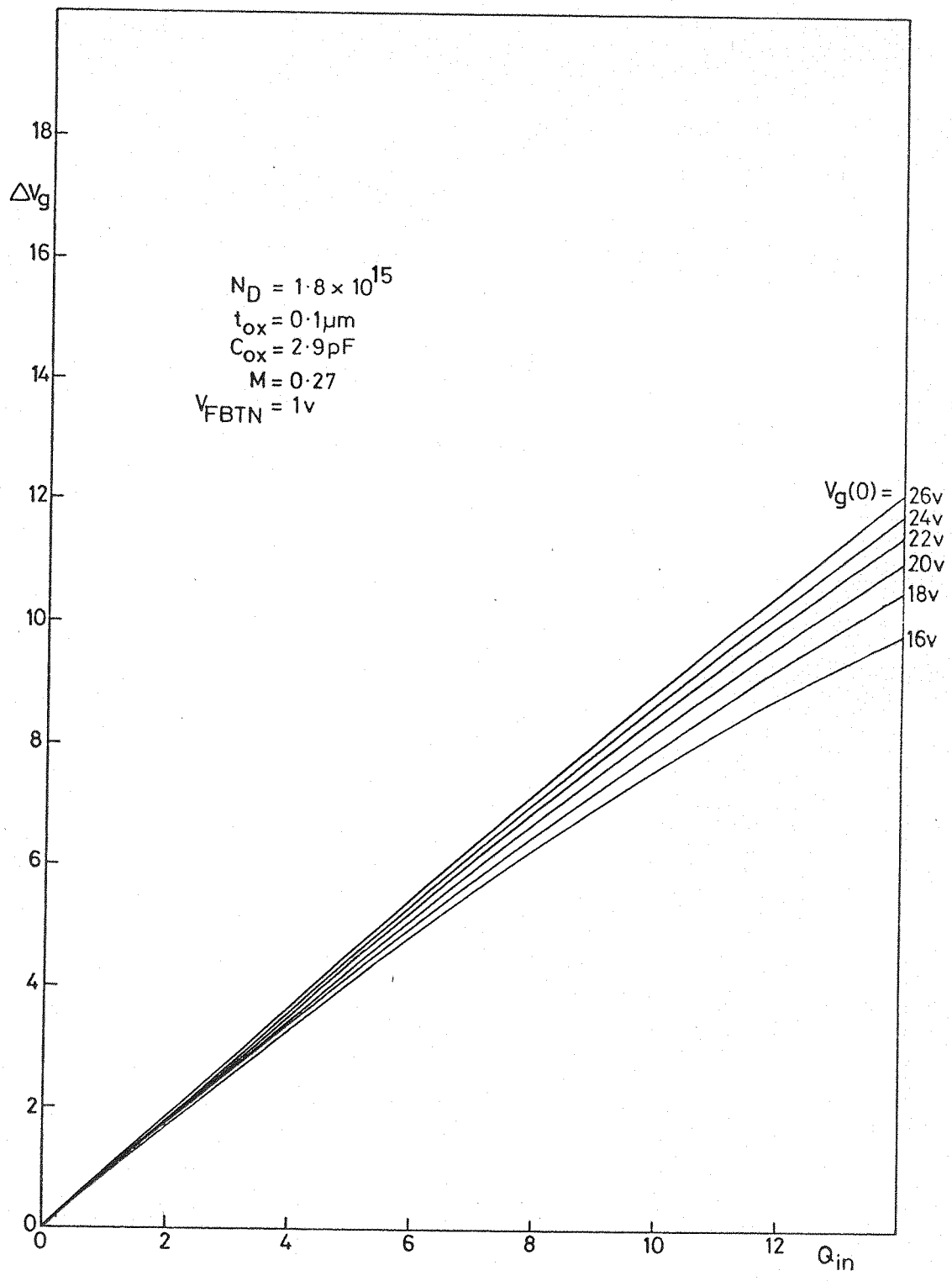


Fig 8.12 The floating gate potential variation versus stored charge; case (ii).

final values of the surface potential beneath the floating electrode can be determined. The maximum transferable charge packet can be found from figure 8.8, and thus the magnitude of the address pulse can be established from figure 8.9. Since the storage site has the same MOS parameters, figure 8.7 can be used to determine whether the address pulse amplitude is sufficient to ensure complete transfer. It can be shown that for the above example complete transfer does not occur; in fact approximately 19% of a full charge packet will be trapped. If the design procedure is repeated for a clock offset of 8V, complete transfer is still unobtainable, but only ≈9% of the full charge packet is retained.

A similar analysis for case (ii) indicates that for 10V and 8V offset clocks, ≈19% and ≈11% respectively of a full charge packet is retained.

A second method of reducing the surface potential differential, is to reduce the substrate doping level. The design curves shown in figures 8.13 to 8.15 are for a device fabricated on 8-16Ω.cm material with 0.1μm and 0.5μm oxide thicknesses. If the design procedure is undertaken for these conditions, it is found that complete transfer in the storage sites is possible, even with a 10V offset clock. Therefore it would be desirable to fabricate the devices on the lower doped substrate. However, at the time, 8-16Ω.cm material was not available to the author and so it was decided to use a 2-5Ω.cm substrate, and increase the thin oxide depth to 0.2μm. The analysis indicated that the charge trapping in this case would be less serious than for case (ii).

The modified test device consists of a 9-bit RGR and eight storage sites. Four sites with common input and output diffusions were positioned below the RGR and four storage sites in which G_4 is connected to the output diodes were positioned above the RGR. Both sets have their own floating diffusion charge detection circuitry which contains an MOST buffer with approximately unity gain.

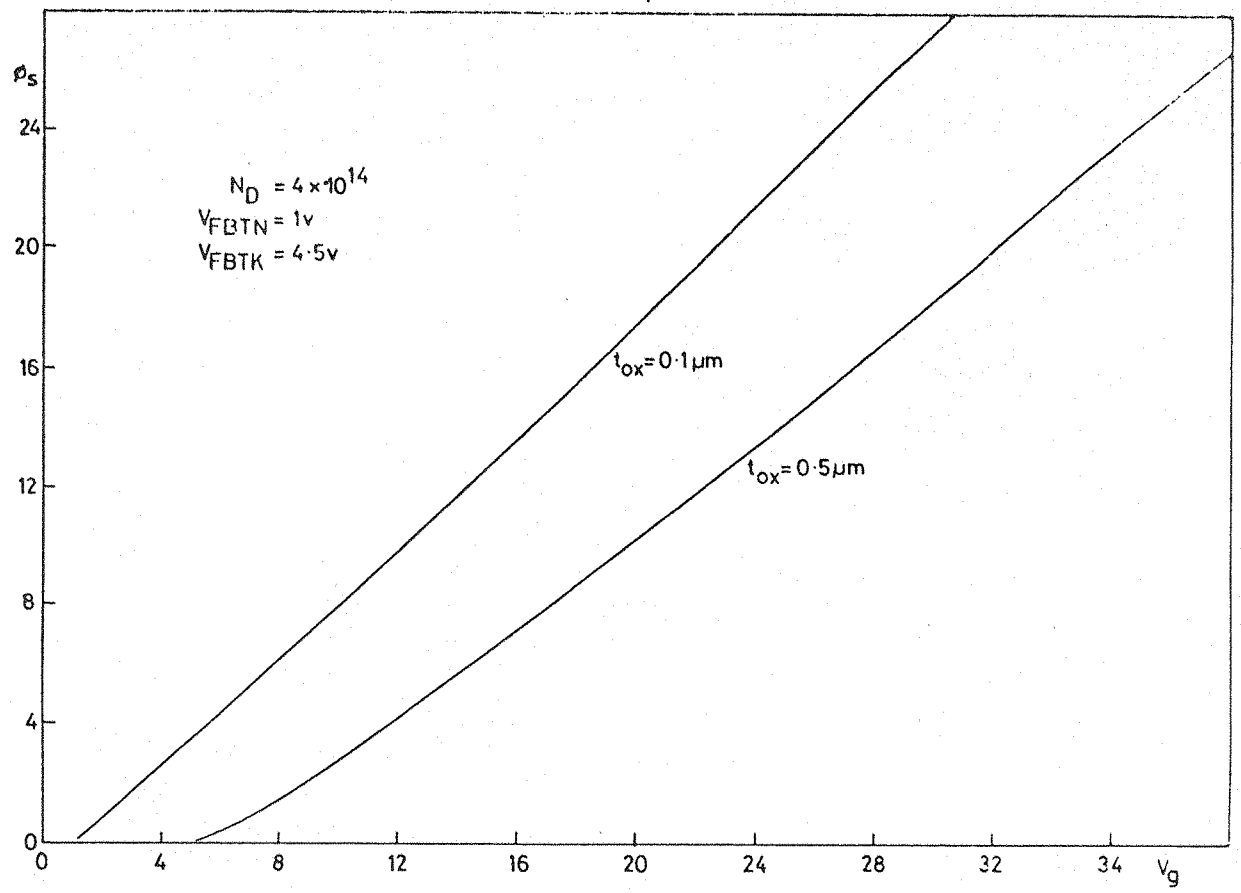


Fig 8.13 The surface potential versus gate voltage for a low doped substrate.

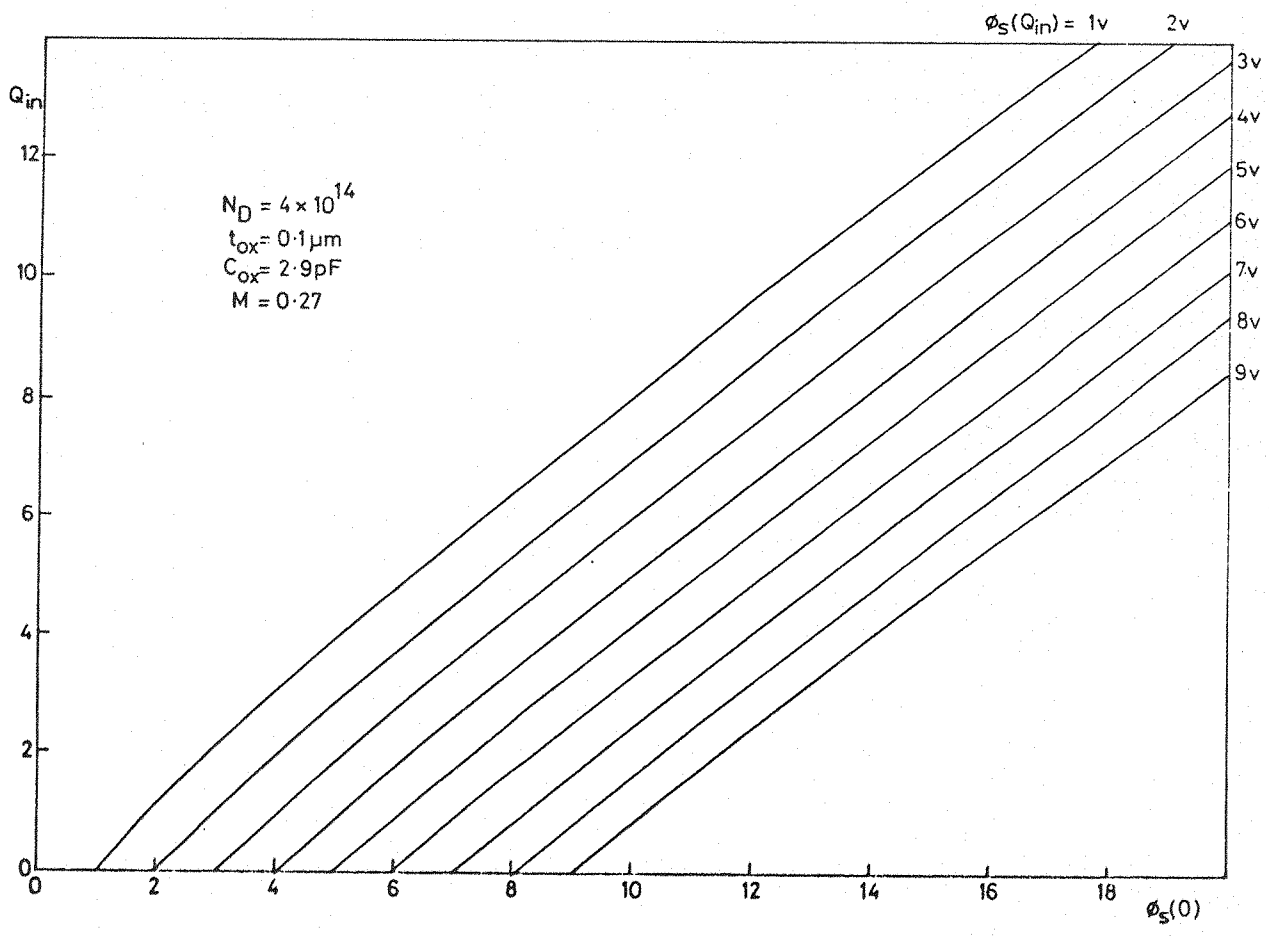


Fig 8.14 The maximum stored charge beneath a floating gate as a function of empty well surface potential on a low doped substrate.

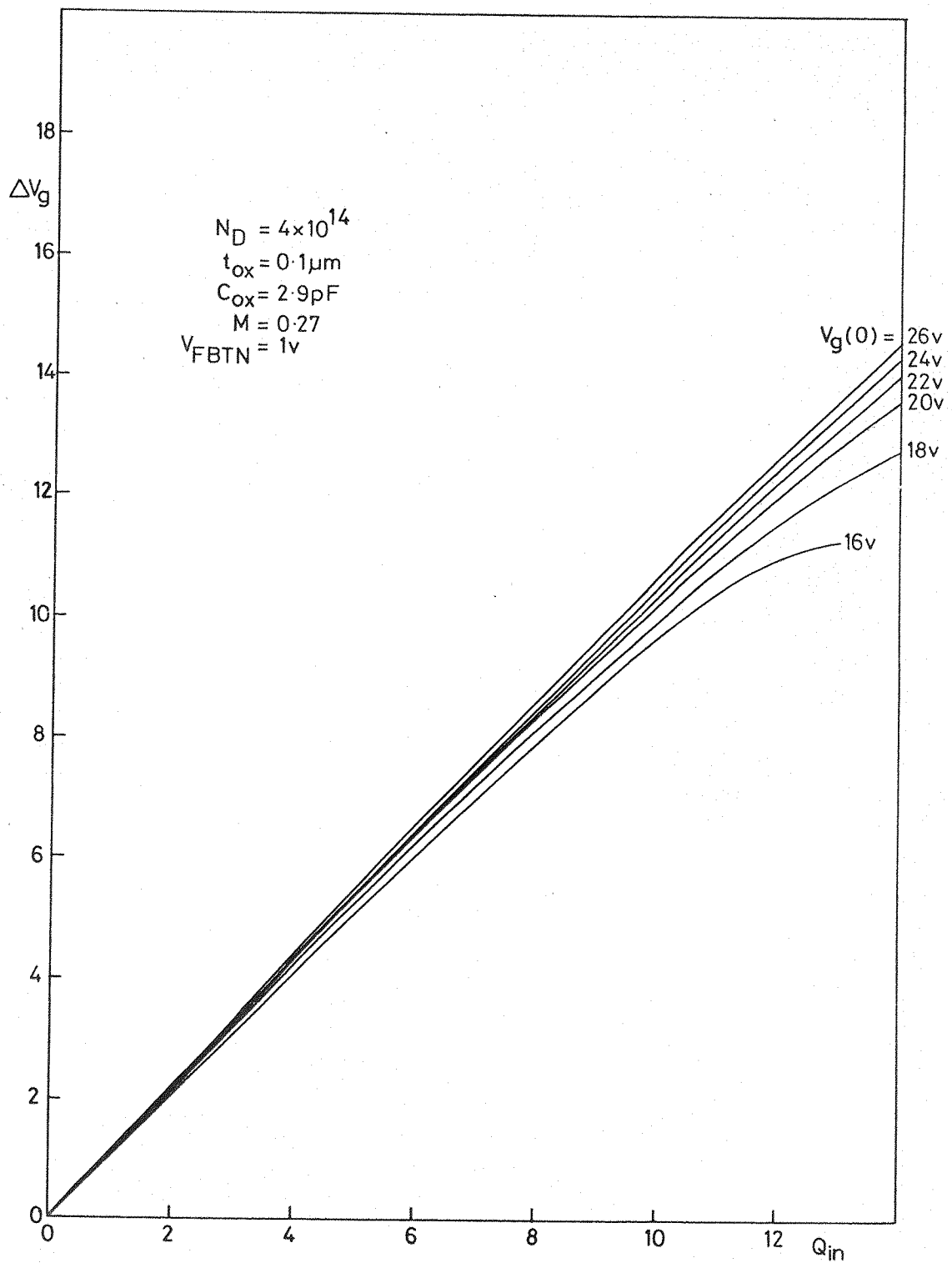


Fig 8.15 The floating gate potential variation versus stored charge on a low doped substrate.

Each mask was laid out using a rudimentary computer-aided design system developed by the CAD group in the Electronics Department.[90] It consists basically of a vector-coded rectangular pattern generator which is used to construct the artwork of each mask in software. When each mask has been coded, a paper tape is generated that is used to drive a photo-composing reticle camera, also developed by the CAD group. The reticle is then used to produce the final mask using standard processing techniques. Clearly, the advantage of generating artwork with a CAD system is that complex patterns can be generated more accurately, and that error correction is considerably simplified since it can be performed in software.

A photomicrograph of the complete device measuring 1.25 x 1.25mm, including contact pads, can be seen in figure 8.16.

8.4 Operation of the Modified Integrator

In accordance with the design procedure presented in the last section, the standard processing schedule was modified to increase the thin oxide depth to 0.2μm. Unfortunately during the fabrication of the first batch of wafers, a processing fault caused the thick oxide to be increased to 0.6μm from 0.5μm. Since subsequent developments in the processing laboratory indicated that the fabrication of more wafers would be delayed considerably, it was decided to carry out some exploratory tests on the devices in hand first. The wafers were diced, as explained in Chapter 6, and mounted on 40-pin DIL plastic headers.

The relevant parameters of the devices tested were:

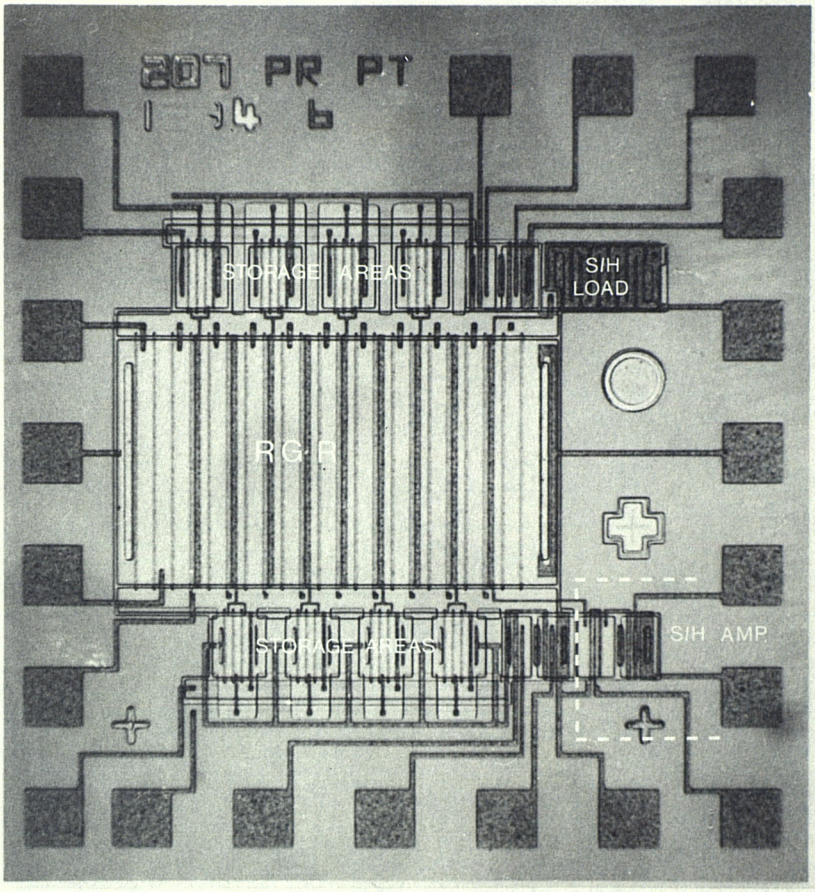
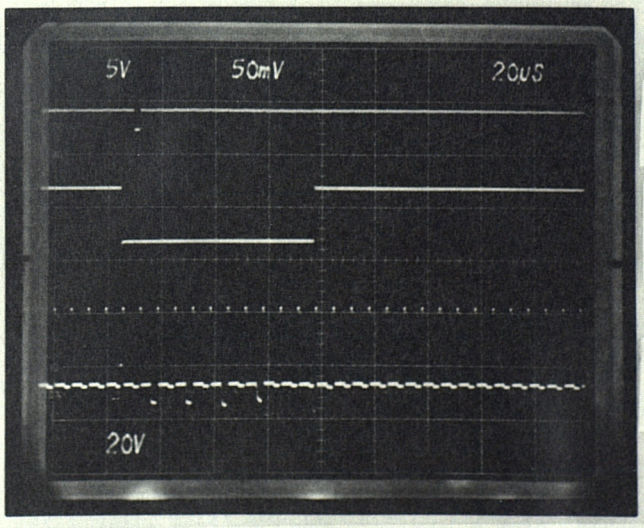


Fig 8.16 A photomicrograph of the modified test recursive integrator chip.



RGR input
5V/vert.div

Storage site
input; 20V/vert.div.

Storage site
output; 50mV/vert.div.

Fig 8.17 An oscillograph showing the storage of a rectangular waveform in the upper set of storage sites.

	Specification	Measured	Units
Substrate doping level, N_D	1.8×10^{15}	--	cm^{-3}
Thin oxide depth, t_{OXTN}	0.2	0.2	μm
Thick oxide depth, t_{OXTK}	0.5	0.6	μm
V_{OTN}	0.97	0.97	V
V_{OTK}	6.32	8.63	V
Thin oxide flatband voltage, V_{FBTN}	1	1	V
Thick oxide flatband voltage, V_{FBTK}	4.5	3	V
RGR gate capacitance, C_{ox}	1.45	1.5*	pF
Floating-gate stray capacitance, C_s	0.39	0.48*	pF
M	0.27	0.32	--

* These values were calculated from the geometries of the finished devices.

It was expected that, due to the increase in thin oxide depth, incomplete transfer in the storage sites would be a significant problem, and furthermore, operation of the lower set of storage sites would be prevented. The reason for this is that these storage sites have common input and output diodes, and in order to correctly bias the diffusion so that it both receives the signal charge and primes the well beneath G_1, complete charge transfer between wells is a prerequisite. Therefore, a device was set up simply to store a rectangular waveform in the upper set of storage sites. This was done by first setting the bias voltages so that a suitable address pulse was propagating along the RGR. This could be monitored by observing the output from the sample/hold circuit. A photograph of the device operating in this storage mode is shown in figure 8.17; the top trace is the

RGR input waveform; the middle trace is the signal waveform, and the lower trace is the output from the storage sites which occurs during alternate clock cycles due to the positioning of the sites. The largest output voltage obtainable was only ≈30mV. Since the total loading capacitance on the output diodes is ≈1.5pF, and the output buffer gain is ≈1, this indicates that a charge of only 0.045pC could be completely transferred through the storage sites. In fact with the biasing conditions used, the maximum charge that could be stored was ≈0.7pC, thus ≈93% of the charge was being incompletely transferred.

The delay duration of the signal is equal to the period between the data pulses applied to the input of the RGR; in this case it is 700μs. In figure 8.18 the effect of introducing additional pulses into the RGR can be seen; again, the waveform at the top shows the input to the RGR. The left-hand pulse can be considered as a 'storage' pulse. The second pulse is used to ouput the stored information, thus the time delay is simply the duration between the two pulses, in this case 80μs.

By reducing the amplitude of the stored signal, it was possible to observe a variation in the amplitude of the output pulses. However, a large amount of fixed pattern noise was also observed which prevented any useful information being gathered on the analogue performance of the devices. The fixed pattern noise was assumed to be predominantly due to the variation of the floating-gate resting potential from tap to tap. However, as explained in the last Chapter, it was decided not to investigate this effect further at this stage. Since analogue operation was difficult, it was not possible to perform analogue recursive integration; however, an attempt was made to operate the device as a recirculating digital shift register. The output was connected to the input via an amplifier; a digital word, consisting of four '1's was then inserted into the feedback path and stored in the device. Figure 8.19 illustrates this capability;

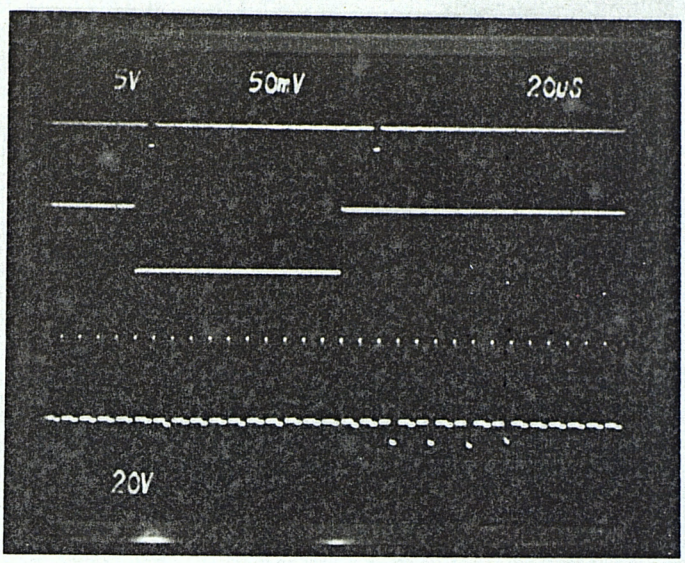


Fig 8.18 The storage and read out of a rectangular waveform with two consecutive RGR pulses. The scale is as shown in Fig 8.17.

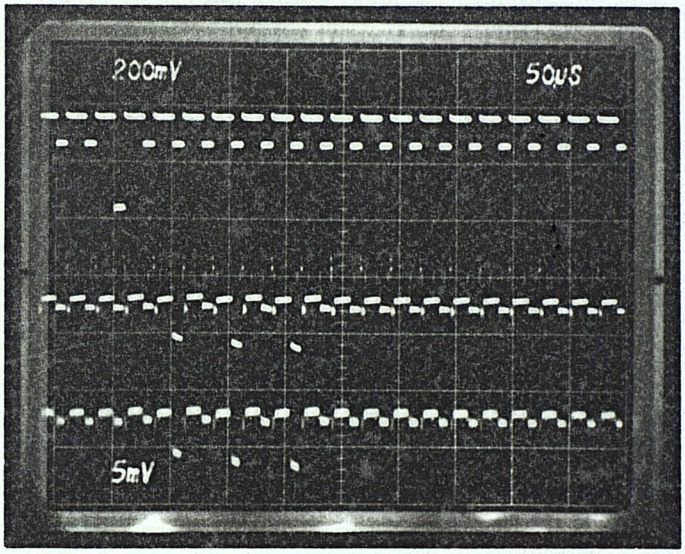


Fig 8.19 The recirculating digital storage capability of the integrator. The top trace is the RGR input; 2.5V/vert.div. The storage site input and output are shown respectively below. The middle trace is 200mV/ vert.div. and the bottom trace is 5mV/vert.div.

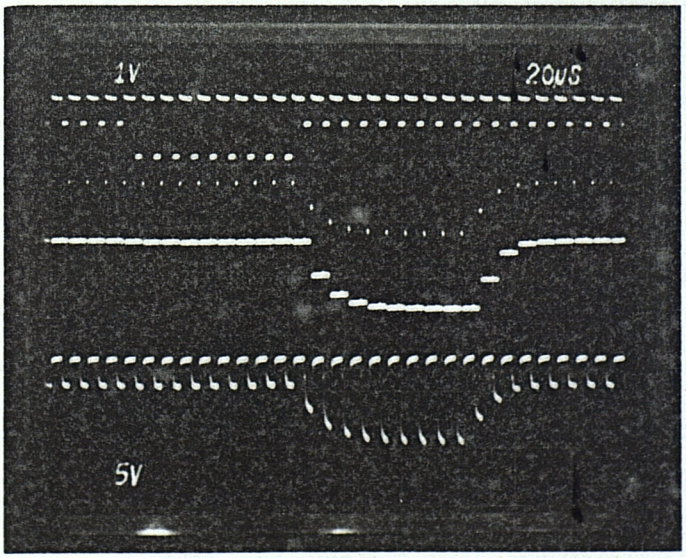


Fig 8.20 The operation of the sample/hold ciruit. The top trace is the RGR input; 1V/vert.div. The middle trace is the sample and held output and the bottom trace is the normal floating gate voltage. Both traces are 5V/vert.div.

the trace at the top is the RGR input, the middle trace is the input to the storage sites, and the lower trace is the output. Only three pulses are observed since the fourth storage site has failed. The information could be erased from the device by momentarily breaking the feedback loop.

The operation of the sample/holding charge detection circuit on the RGR is shown in figure 8.20. The upper trace is the input to the RGR; the lower trace is the conventional output waveform from the floating gate, and the middle trace is the sample and held form. A rather large amount of sample pulse breakthrough can be observed on the middle trace; the reason for this has yet to be established.

8.5 Conclusions

In this Chapter the design and performance of a parallel transfer signal processor employing exclusively CCD structures has been presented. The design procedure showed that the use of a low doped substrate (8-16Ω.cm) should permit satisfactory interfacing of the RGR and storage sites. However, since a suitable substrate material was not available at the time, the devices were fabricated on 2-5Ω.cm material (but with a thin oxide depth of 0.2μm to reduce incomplete transfer). During the fabrication of the first batch of devices, the thick oxide was inadvertently grown to a depth of 0.6μm instead of 0.5μm. In spite of this, it was decided to mount and test these devices. Although, as expected, significant incomplete transfer and fixed pattern noise prevented the evaluation of the analogue performance of the devices, it was possible to store a rectangular waveform and operate the device as a recirculating digital shift register.

The success of these preliminary investigations on the digital storage capability of these devices indicates that if the correct substrate material were used, an analogue storage capability would be realized and thus permit the construction of

a prototype radar recursive signal integrator. Silicon wafers of 8-16Ω.cm resistivity have recently been acquired and the fabrication of devices on this material is currently in progress.

This Chapter concludes the work done to date on the implementation of a CCD parallel processing recursive integrator. In the next Chapter, the implementation of the non-recursive system will be discussed.

CHAPTER NINE

THE CCD IMPLEMENTATION OF THE NON-RECURSIVE INTEGRATOR

9.1 Introduction

In Chapter 4, the concept of parallel processing CCD structures for signal integration was proposed. Two techniques were described, one performing non-recursive integration and the other recursive integration. It was also indicated that, although the features of both techniques were complementary, the recursive approach would be investigated first since this implementation required a less complex chip layout.

Whilst the fabrication of a non-recursive device would not be possible at Southampton University because the size of such a device would exceed the University's present mask production capability, some thought has been given to the implementation of this approach; in addition, some investigations of the linearity of the integration method have also been performed.

9.2 CCD Implementation of the Non-Recursive Integrator

It will be recalled that in the non-recursive integrator, each radar return is sequentially gated into a series of tapped m-bit CCDs which comprise the range bin storage areas. Information reaching the end of each CCD is transferred onto a drain diffusion and destroyed, thus at any instant each CCD contains the last m-returns from one particular range bin. The integration of the m samples is achieved using conventional transversal filter techniques and the resulting signal is gated to the output.

The signal charge in the range bin CCDs may be sensed using either floating-gate voltage sensing or electrode current sensing. In addition, there are also two methods of transferring the charge along the range bin CCDs, i.e. by clocking each CCD individually from an on-chip source such as the RGR, or by clocking

all the driving electrodes together with an external source. Thus there are basically four implementations of the non-recursive integrator; proposals for realizing these are considered below.

9.2.1 Current Sensing with On-Chip Clocking

This scheme is illustrated in figure 9.1. Each range bin CCD is a two-phase device with its sense electrodes connected together and also to the sensing electrodes of the other range bin CCDs. The charge injection scheme used is the two-phase input technique described in Chapter 2; the first electrode of this structure, and the clocked electrodes of each CCD is driven from its corresponding RGR tap. However, because of the large capacitance associated with the driven electrodes, it would be necessary to buffer the RGR taps with an MOST amplifier. The mode of operation is as follows: As the address bit propagates along the RGR, the potential well beneath the first electrode of each range bin CCD is primed with charge and subsequently metered according to the signal applied to the input electrode; simultaneously, the stored signal samples associated with each range bin are shifted to the next bit. Since current sensing is employed, the charge samples may be detected during the transfer operation, thus by employing the proposed sensing electrode configuration, the stored data is automatically multiplexed onto the serial output bus.

The disadvantage of this implementation is that MOST buffers are required for each RGR tap output, thus preventing high speed operation.

9.2.2 Floating-Gate Voltage Sensing with On-Chip Clocking

This scheme, illustrated in figure 9.2, is architecturally similar to the last scheme except that multiplexing of the output has to be done in conjunction with floating-gate voltage sensing. The integrated signal from the nth range bin is multiplexed onto the output bus via a buffer which is switched on by the (n+1)th

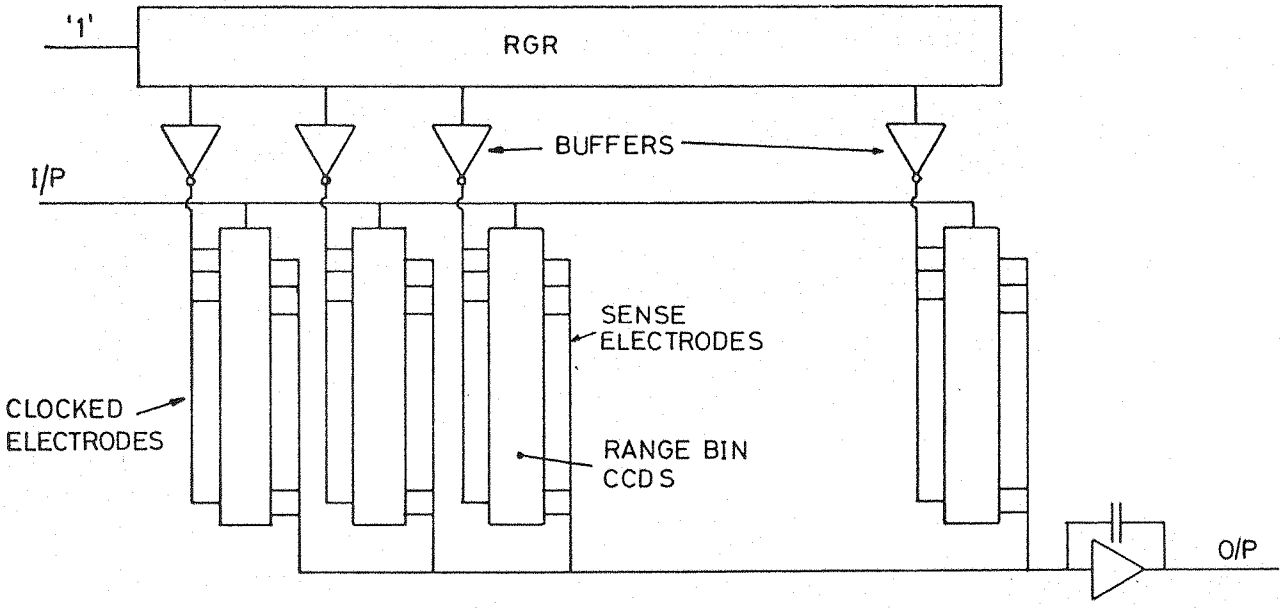


Fig 9.1 The implementation of the non-recursive integrator using current sensed range bin CCDs individually clocked from the RGR.

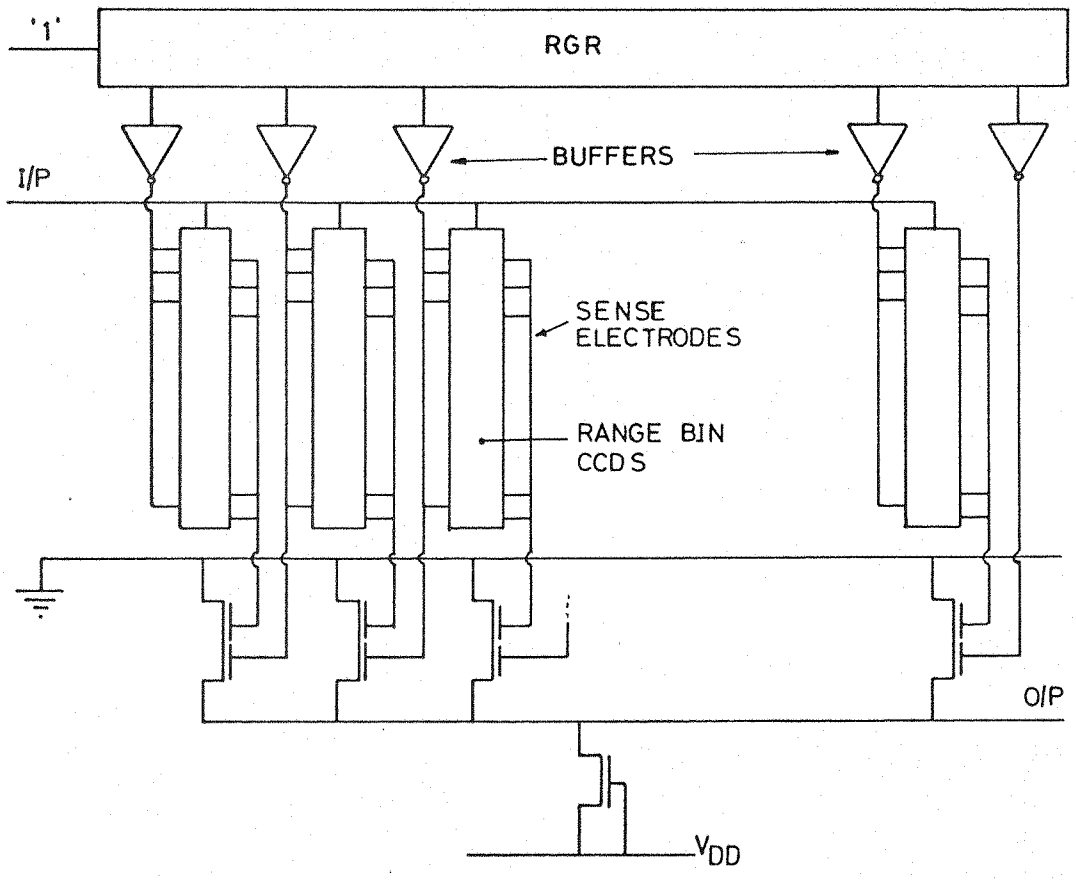


Fig 9.2 The implementation of the non-recursive integrator using voltage sensed range bin CCDs individually clocked from the RGR.

address pulse.

Again, the necessary use of MOS buffers precludes high speed operation.

9.2.3 Current Sensing with Off-Chip Clocking

As in the previous implementations, this scheme (see figure 9.3) employs two-phase CCDs for each range bin, but the driven electrodes of all the devices are connected together and clocked from an off-chip clock driver which amplifies the address pulse arriving at the end of the RGR. The standard two-phase charge injection scheme is employed, but the first electrode of the structure is driven directly from the appropriate RGR tap. Thus the potential well adjacent to the input diffusion is primed continually, except when the overlying electrode is addressed from the RGR. When this happens, a charge proportional to the input signal is metered into the adjacent potential well. The charge samples in all the CCDs are transferred simultaneously, when the address pulse has traversed the RGR. The integrated signal from each range bin is detected as a charging current that restores the corresponding floating electrodes to a reference potential as the appropriate output MOST switch is operated. It will be noted that it is necessary to invert the RGR tap waveform to operate these switches. Whilst this would prevent the operational speed of a totally CCD system being realized, the data rate of this scheme could be higher than that achievable with the implementations described before, since the loading capacitance on the buffers would be considerably less.

9.2.4 Floating-Gate Voltage Sensing with Off-Chip Clocking

This system, illustrated in figure 9.4, uses a similar architecture to the last system, but voltage sensing is employed and the integrated signal is multiplexed onto the output bus using a charge transfer technique. A cross-section of a range bin CCD

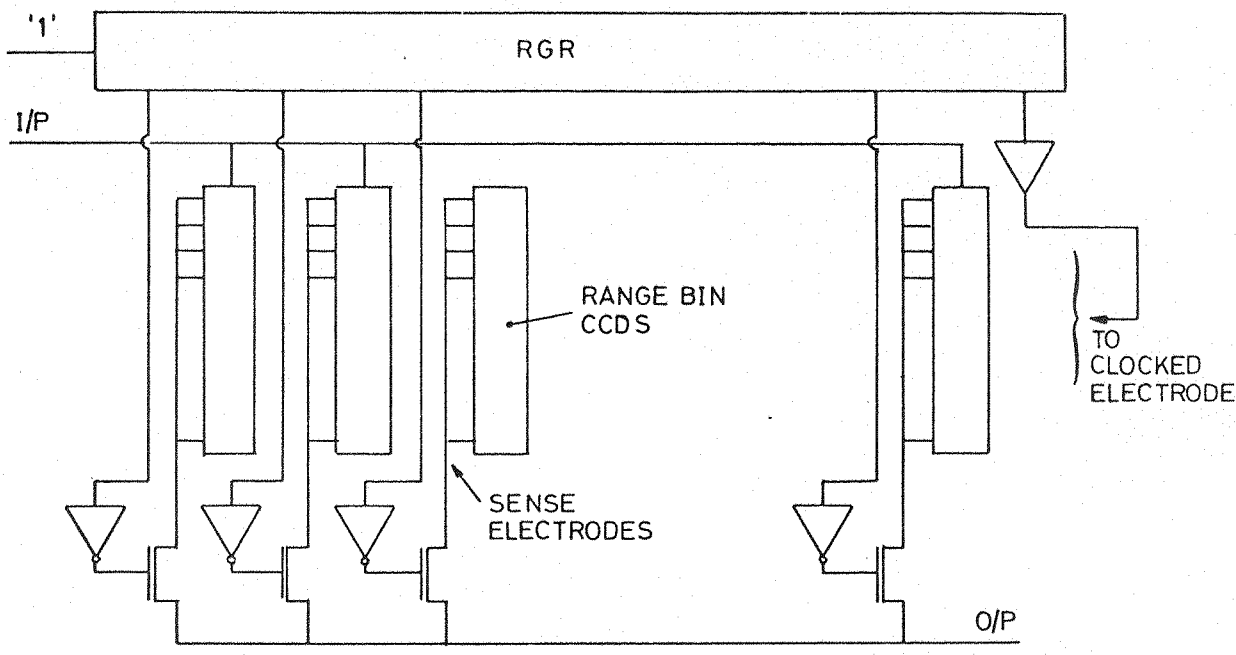


Fig 9.3 The non-recursive implementation employing current sensed range bin CCDs clocked simultaneously from the RGR.

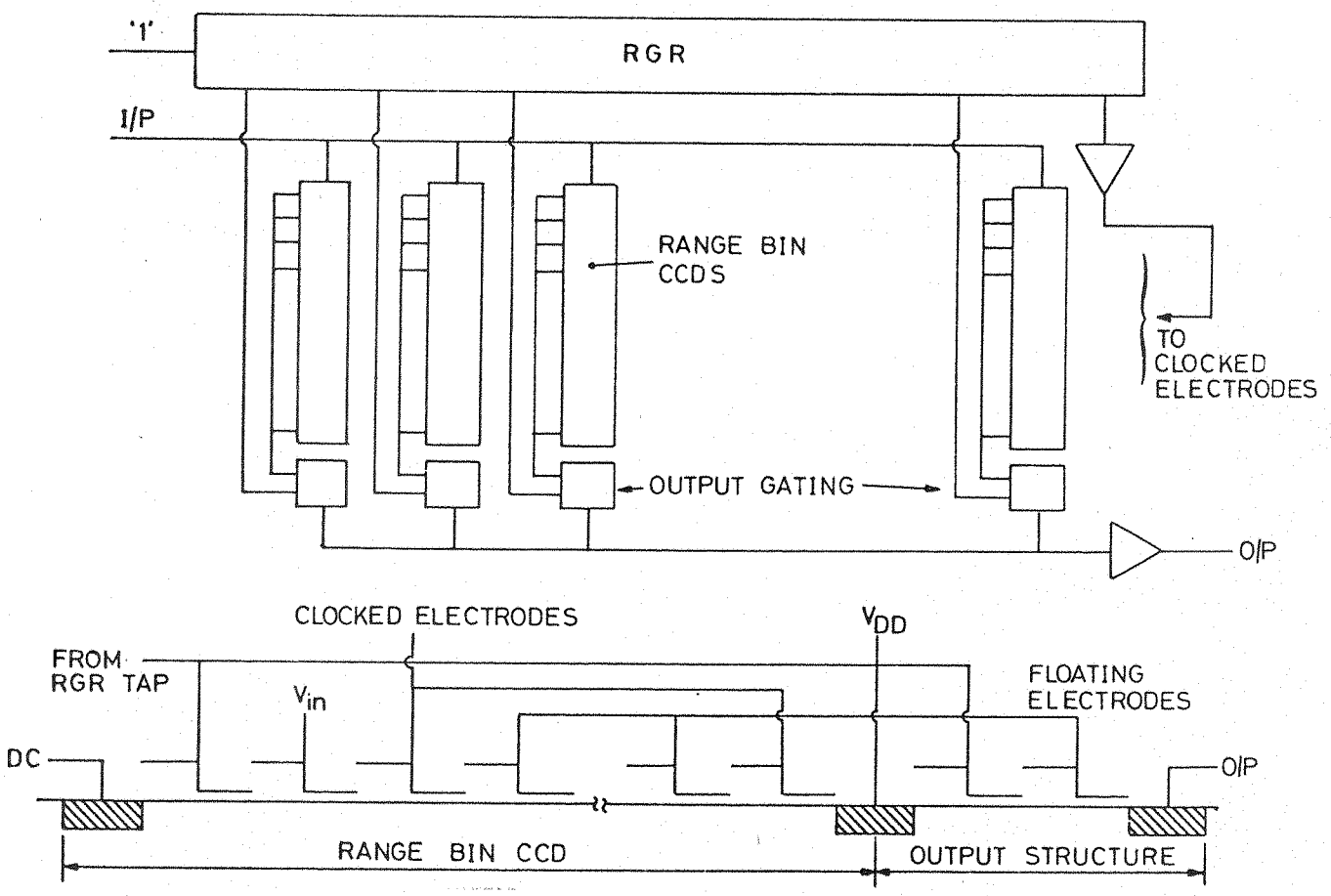


Fig 9.4 The non-recursive implementation using voltage sensed range bin CCDs with off-chip clocking. A cross-section of the output structure is also shown.

and its output gating structure is shown in figure 9.4b. The output scheme comprises the input electrodes of a 'zero-bit' CCD. The first electrode of this structure is driven by the RGR tap output, and the integrated signal voltage from the range bin CCDs is applied to the second electrode. Thus upon application of the address pulse, charge proportional to the integrated signal is metered onto the output diode, which is common to all other range bins; the signal charge can then be sensed with a conventional floating diffusion detector.

Clearly the most desirable system would be one that minimized distortion, noise, chip complexity and should preferably be capable of high speed operation. The analysis of the charge sensing schemes which was presented in Chapter 5, indicated that high linearity can be achieved by using a current sensing scheme in conjunction with the diode cut-off charge injection method. However, since the charge injected with this technique can exhibit high noise and non-linearity due to partitioning effects, it was decided to avoid this scheme. Although a voltage sensing scheme is inherently less linear than a current sensing method, the implementaions described above, using the latter sensing technique, employ on-chip MOST buffers and so would not be capable of high speed operation. Furthermore, the sensing node capacitance could be quite high and therefore limit the signal-to-system noise ratio.

On the other hand, the implementation described in section 9.2.4 employs exclusively CCD structures, has a relatively low chip complexity, and by using double correlated sampling at the output, detection noise could be kept reasonably low. Thus it is proposed that this implementation should be investigated in greater detail when a facility for producing larger masks becomes available.

9.3 Voltage Sensing Linearity

As mentioned already, the fabrication of a complete test non-recursive integrator would be difficult. However, it was decided to investigate the linearity of the floating-gate voltage sensing scheme which it is recommended would be used in the prototype system.

These investigations were carried out on a 50-bit two-phase CCD; on this device the second phase electrodes are connected to an on-chip MOST, thus forming the basis of a floating-gate voltage sensing scheme. This arrangement not only minimizes the stray capacitance associated with the sensing electrodes, but also ensures that its value (which is fairly critical) does not alter unpredictably during the experiments. Consequently, an accurate experimental determination of this parameter could be made for subsequent computer analysis of the structure. The device has a 400μm wide channel and each electrode is 14μm long, 4μm of which are on thick oxide. Charge reaching the end of the device is detected with a floating diffusion charge detector which contains a nominally unity gain buffer; the diffusion is loaded with the capacitance of a 100μm x 100μm contact pad to increase detection linearity. A dummy sense circuit is also included, so that reset pulse feedthrough can be reduced. Figure 9.5 shows a photomicrograph of the device.

Whilst the experiments were in progress, great care was taken to ensure that spurious responses were being suppressed. For instance, in the first experimental set-up, a plug-in amplifier type 7A18 on a Tektronix 7704A monitoring oscilloscope was used to match the signal under scrutiny to a Marconi Instruments TF2370 spectrum analyser. During measurements on the linearity of the floating-gate sense amplifier, anomalous results were observed. These were traced to the 7A18 plug-in; although the distortion of this unit was relatively low, it was found to vary with beam position. A similar effect was also noticed when using

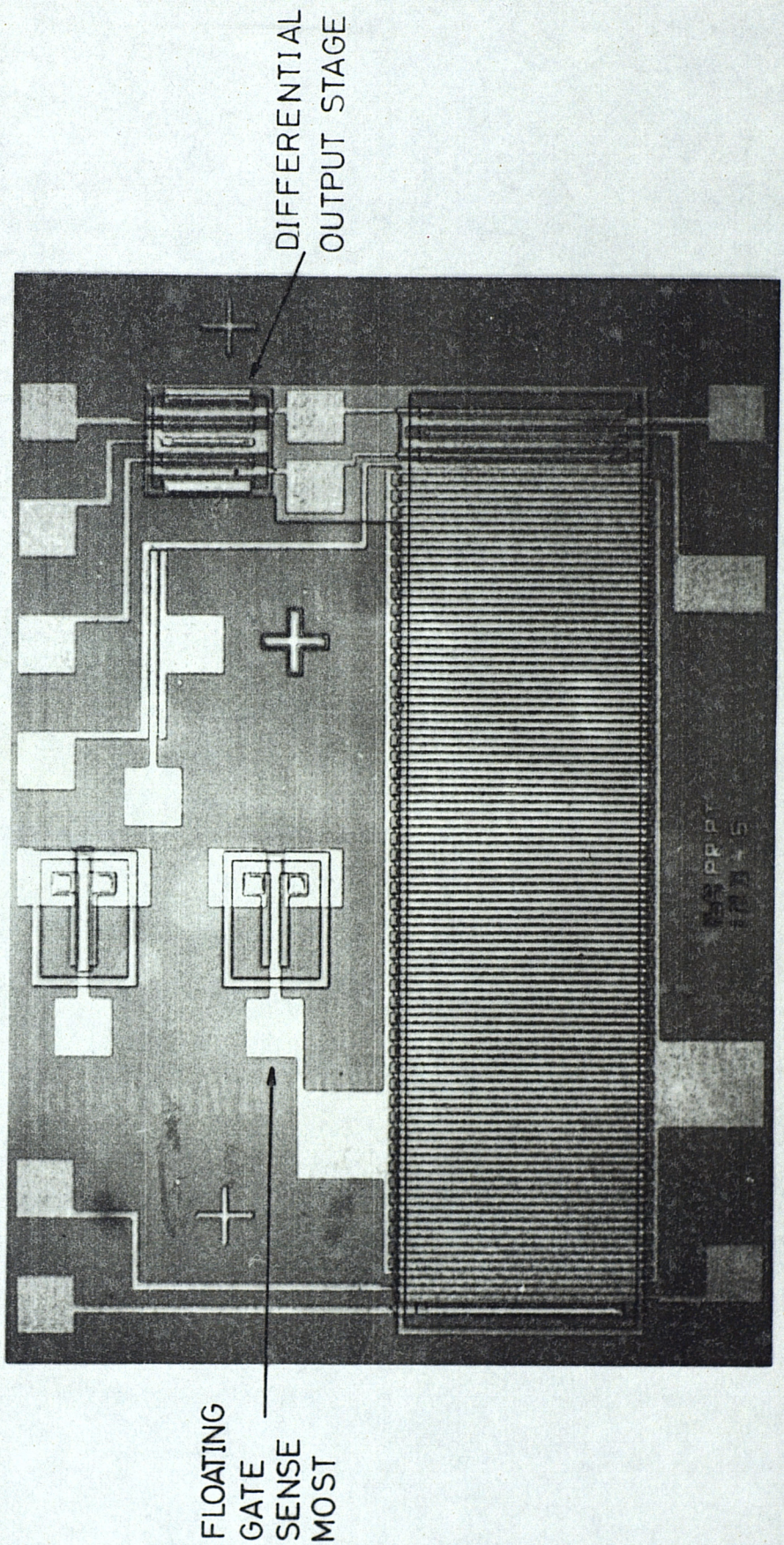


Fig 9.5 A photomicrograph of the floating gate voltage sensing chip.

the differential amplifier plug-in type 7A13. It was finally decided to use a Brookdeal Precision AC Amplifier type 425 for impedance matching purposes; this amplifier has an input impedance of 10MΩ and a specified linearity of 0.001%; with the input short-circuited, the 3kHz bandwidth noise level was more than 70dB below the fundamental signal component at all frequencies of interest. Although care was taken to prevent intermodulation distortion caused by overloading the spectrum analyser input, detection of this condition was sometimes difficult. Therefore it was decided to use an HP310A wave analyser since, although measurements were more tedious, an overload condition was more easily detected. The input impedance of this unit is between 10kΩ and 100kΩ. Figure 9.6 shows a schematic of the final experimental set-up.

The input signal, from a Lyons Instruments SQ10 sine wave generator, was connected to the CCD input gate via a simple RC level shifting network; the DC bias level of the signal was measured with a Solartron 7040 DVM. An ML101B MOST was connected as a load for the on-chip floating-gate sensing MOST; following this arrangement was an attenuator to prevent overloading of the 425 amplifier.

The experimental procedure adopted was first to determine the distortion associated with charge packet being injected into the CCD. This was done by measuring the linearity of the CCD when used as a conventional delay line, and then subtracting the distortion due to the floating diffusion charge detector. This result, and measurements of the non-linearity of the floating-gate amplifier, could then be used to determine the floating-gate linearity.

A clock waveform of 200kHz and amplitude 27.5V offset by 5V was connected to the device, and the various bias voltages set to achieve lowest transfer inefficiency; this parameter was found to be 2.10^{-3}. A 1V pk-pk sine wave at 1kHz with less than -60dB

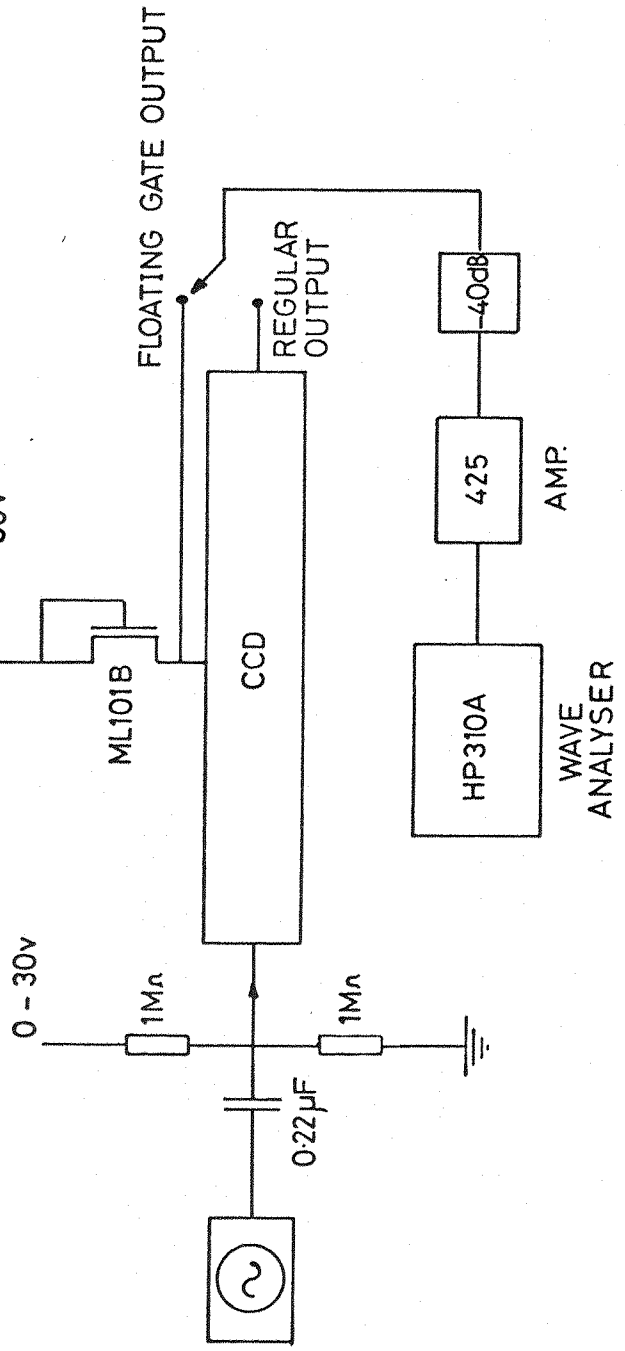


Fig 9.6 The experimental set-up used to measure the non-linearity of the floating gate voltage sensing technique.

harmonic distortion was then connected to the input gate and the harmonic components at the output of the floating diffusion detector were measured as a function of input DC bias; the DC bias, V_{DCmin}, which gave lowest distortion was noted. A sine wave was then applied to the drain of the reset MOST, and its gate was biased on. The DC level and amplitude of the signal was then adjusted to simulate charge packets representing a 1V pk-pk sine wave with a DC bias of V_{DCmin} arriving at the sense diode. Thus the distortion of the detector under the previous operating conditions was determined. In fact, the magnitude of the second harmonic component generated by the detector was indistinguishable from that of the signal source, whilst the third harmonic was more than 75dB below the fundamental. The harmonic components generated at the CCD input as a function of DC bias, are shown in figure 9.7.

The 1V pk-pk signal biased at V_{DCmin} was reconnected to the CCD input and the harmonic components at the output of the floating-gate sense amplifier were measured as a function of frequency up to 10kHz (measurements of harmonics less than -55dB was limited by the noise generated in the CCD). The signal source was then connected to the input of the sense amplifier to simulate the floating-gate signal. The harmonic distortion of this amplifier was measured and found to be more than 50dB below the fundamental. In view of the fact that the second and third harmonics generated by the charge injection technique and the sense amplifier were more than 20dB below the harmonics generated by the overall floating-gate system, it seems reasonable to deduce that these latter results are a direct measurement of the floating-gate non-linearity.

An analysis of the floating-gate structure was also carried out using the charge balance model presented in Chapter 5 and the computer program described in Appendix 2. The parameters used in the calculations were measured on the device under test

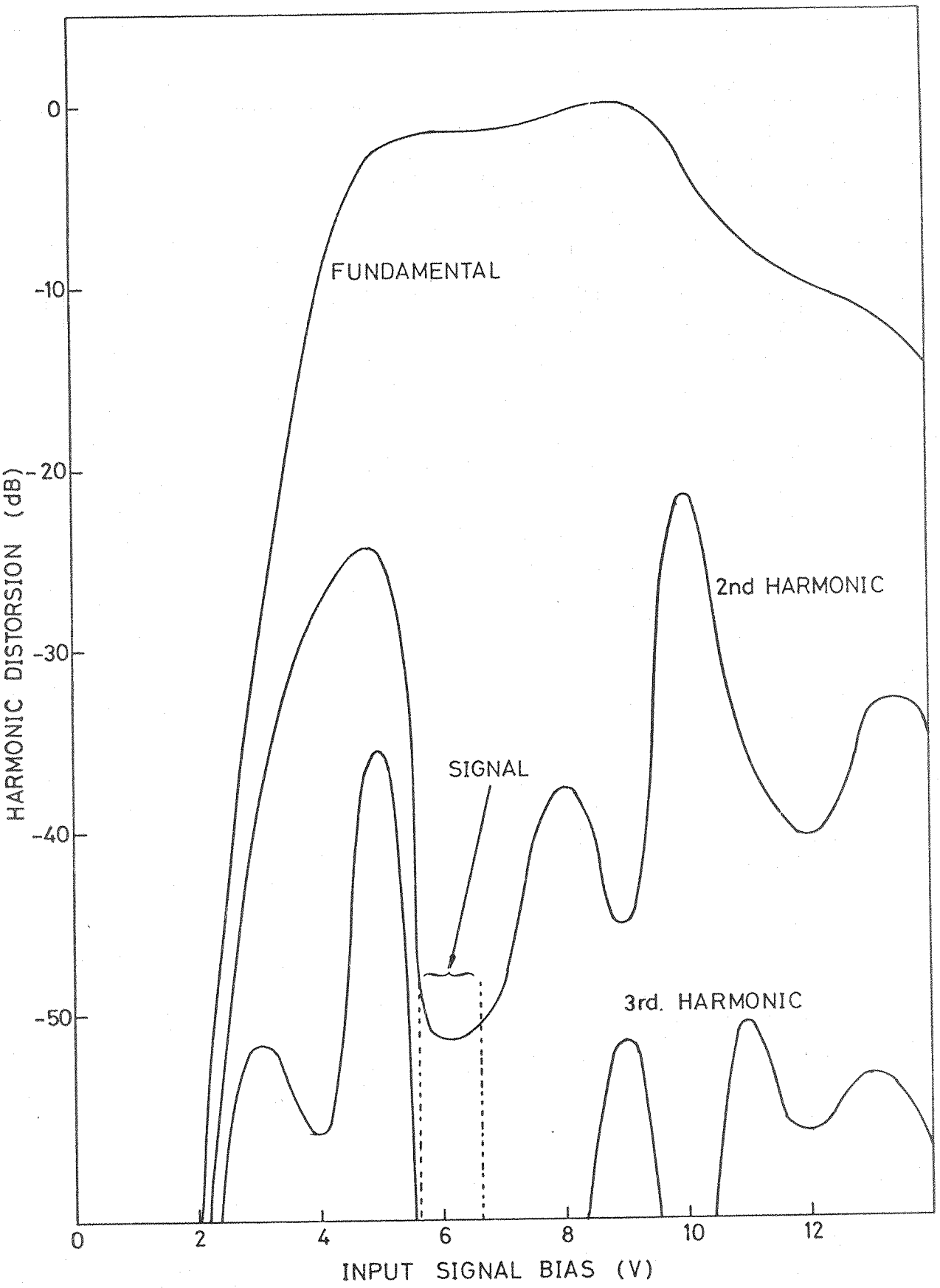


Fig 9.7 The harmonic distortion of the charge injection scheme as a function of the bias level of a 1v pk-pk sine-wave input.

and were

Thin oxide flatband voltage, V_{FBTN}	=	0.8V
Thick oxide flatband voltage, V_{FBTK}	=	2.5V
V_{OTN}	=	0.4V
V_{OTK}	=	6.95V
Floating-gate oxide capacitance, C_{ox}	=	0.96pF
Floating-gate stray capacitance, C_s	=	10.9pF
Fat-zero charge level, Q_{DC}	=	1.19pC
Pk-pk signal charge level, Q_{PK}	=	0.94pC

The oxide capacitance, C_{ox}, was calculated form the CCD input transfer response, and the stray capacitance was measured with a capacitance bridge. Great care was exercised in the latter measurement to ensure that all stray capacitances were included, i.e. pin-to-pin capacitance of the package, bonding wire capacitance, input capacitance of the sense MOST, capacitance of the interconnection tracks, capacitance of the thick oxide portion of the floating-gates and the inter-electrode capacitance.

The theoretical and measured response are plotted together in figure 9.8; 0dB on the vertical scale represents a signal of 0.54V pk-pk measured on the floating-gate. It can be seen that the model gives a very close fit to the measured response, and thus gives further confidence in the use of the charge balance model for analysing floating-gate structures.

9.4 Conclusions

In this Chapter, several implementations of the parallel processing non-recursive integrator have been described. It is proposed that a system employing voltage sensing of the range bin CCDs with simultaneous clocking of these structures from an off-chip source should be investigated in greater detail, since this

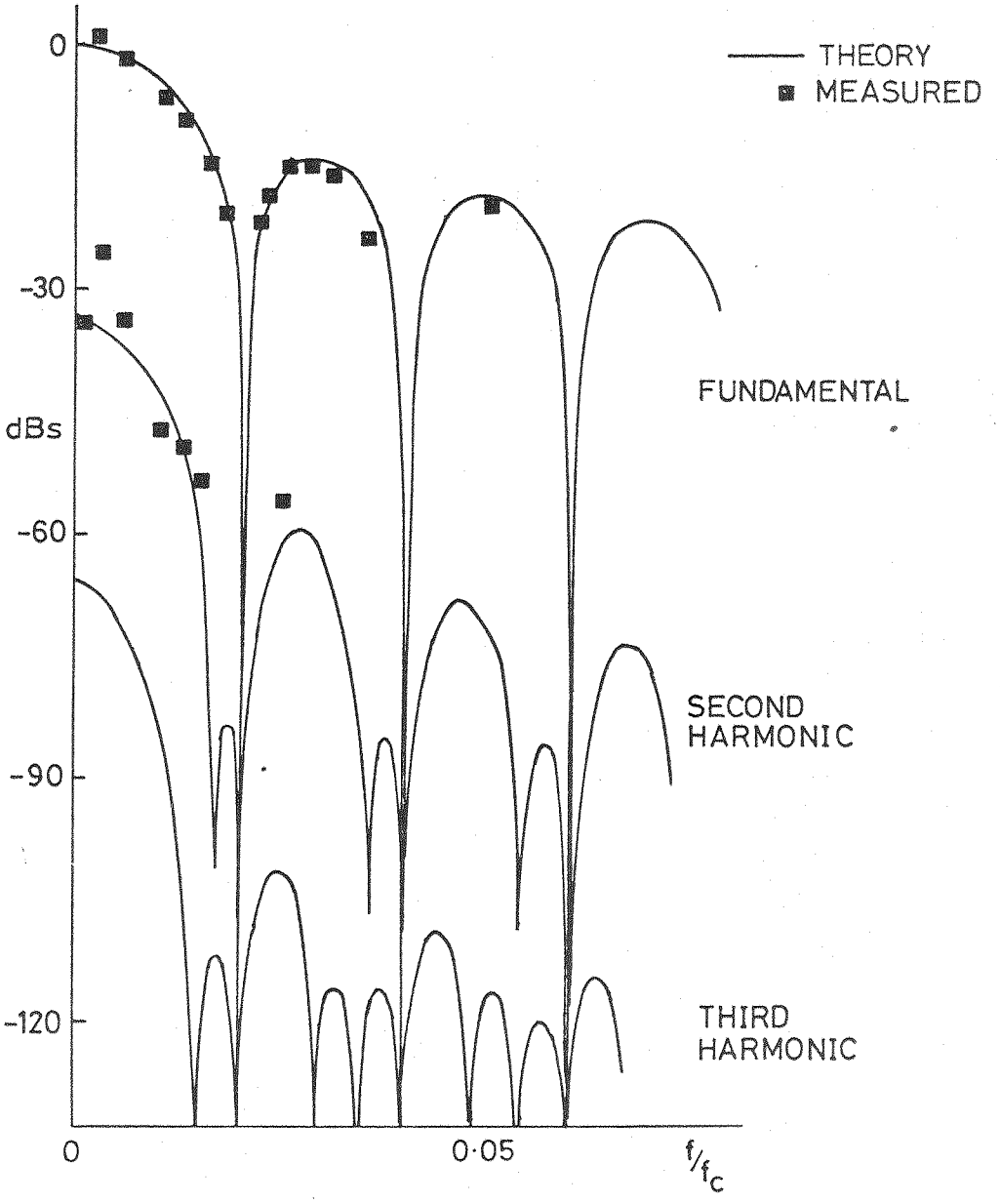


Fig 9.8 The measured and theoretical response of the floating gate charge sensing scheme.

scheme can be designed using CCDs exclusively. Construction of a prototype chip could be done, if facilities for making larger masks were made available.

An investigation of the non-linearity of the voltage sensing technique has also been presented. The measured transfer response and harmonic component levels agreed very well with calculations based upon the charge balance model. Thus it is felt that the linearity of floating-gate voltage sensing schemes can be predicted fairly accurately, and that suitable structures could be designed in which the stray capacitance is chosen to optimise linearity and noise performance.

CHAPTER TEN

CONCLUSIONS AND SUGGESTIONS FOR FURTHER WORK

This thesis has been concerned with the application of charge-coupled devices to analogue signal processing. In the earlier Chapters, basic CCD techniques were described together with a feasibility study to investigate the use of a CCD time-compressor to insert the audio information of a TV transmission onto redundant video lines. Although a full broadcast compatible system could not be investigated, the system that was constructed successfully demonstrated the feasibility of this application.

The bulk of the thesis, however, describes the application of CCDs to the development of a CCD signal integrator to obtain signal-to-clutter improvements in marine radar signals. Although CCDs had previously been used to implement the delay line of such systems, the signal-to-clutter improvement that could be obtained with an integrator employing a conventional (i.e. serial) CCD was limited by the build-up of signal residuals caused by transfer inefficiency. Methods of cancelling the residuals had been suggested by various authors, but it was clear that a more satisfactory technique was required. The system adopted was one in which all redundant CCD transfers were eliminated by the use of a parallel transfer structure. In this approach, the signal undergoes a minimal number of transfers and so residuals are maintained at a very low level.

Two basic integration techniques were investigated; one uses non-recursive integration in which the last 'm' returns are summed with equal weighting, and the other uses recursive integration in which the returns are summed with exponential weighting. In both systems, each radar return is sequentially gated into storage areas using an on-chip addressing scheme called a range gate register (RGR). The RGR consists of a floating-gate

tapped two-phase CCD operated as a digital shift register. It was proposed that each tap should drive the corresponding analogue gates directly without intermediate amplification, thus enabling the high speed capability of an exclusively CCD system to be realized.

In order that the feasibility of this proposal could be investigated, and also since the integration scheme in the non-recursive integrator was likely to use floating-gate voltage sensing, a detailed analysis of floating-gate structures was carried out. However, rather than use a capacitive model which has given rise to difficulties in the past, a charge balance model was used; this led to the derivation of a general expression for the potential variation on a multiple floating-gate assembly, loaded by a non-linear stray capacitance (such as the thick oxide section of a two-phase electrode), as a function of stored charge. A numerical analysis for two special cases was then carried out; these were a 63-tap low-pass transversal filter, and a single RGR tap. It was shown that, although the potential variation is highly dependent upon the magnitude of the stray capacitance, if this parameter is sufficiently small, address pulses large enough to operate an analogue gate directly from an RGR tap could be generated. In addition to the voltage sensing configuration, a low-pass CCD filter was also analysed, assuming an electrode current sensing scheme. The effects of using two types of charge injection scheme, i.e. potential equilibration and diode cut-off, were also investigated. The results indicated that in general the current sensing scheme exhibited the least non-linearity, and if charge partitioning was ignored, the diode cut-off injection scheme would yield a linear overall response. However, because the peripheral circuitry for the voltage sensing technique is simpler than for the current sensing method, the choice of charge sensing technique for the non-recursive integrator is not straightforward.

Since the recursive integrator could be implemented with a fairly simple chip layout, a test chip was designed and fabricated to investigate the performance of the RGR and storage areas. MOST buffers were included on this design, so that a rigorous evaluation of the floating-gate tap response could be made. Experimental measurements of the transfer response of the RGR taps agreed very well with the theoretical predictions, and established the feasibility of using a CCD for on-chip addressing. An anomalous variation of the buffer gains was observed which was attributed to the series resistance of the power and source-bias distribution diffusions. Also a discrepancy between the measured floating-gate resting potentials and the predicted values was noted. This appeared to be due to gate-to-substrate leakage effects. Since this also caused a variation in resting potential from tap-to-tap which could give rise to a large amount of fixed pattern noise, further work to suppress these variations, with say a process modification, will be necessary. Another possible way of reducing fixed pattern noise would be to employ an identical set of storage sites driven from the same RGR taps. By storing a DC level in these sites and subtracting their outputs from the regular sites, tap resting potential and threshold variations could be cancelled.

Unfortunately, a mask error prevented the operation of the storage sites. Rather than correct this, however, it was decided to proceed with the design of another layout which incorporated several improvements. The major modifications were to employ direct driving of the analogue gates, and to separate the thin and thick oxide portions of the RGR taps. A set of design curves were used to ensure that storage sites and RGR taps would interface properly. Even so, the design procedure was rather tedious, and could usefully be transferred to a computer for future designs. If this were done, the effects of parameter changes and tolerance to bias voltage variation could easily be evaluated.

The design procedure indicated that satisfactory operation should be achieved if devices were fabricated on 8-16Ωcm substrates with the standard two-phase CCD process schedule. However, since this material was not available, 2-5Ωcm substrates were used and the thin oxide depth increased to 0.2μm from 0.1μm. In spite of the fact that a process error caused an increase in thick oxide depth, working chips were bonded and tested. As expected, a large amount of incomplete transfer prevented the evaluation of the analogue performance of the device, but a rectangular waveform was successfully stored and the device could be operated as a recirculating digital shift register. Again, however, a large amount of fixed pattern noise was observed.

Devices are currently being fabricated on 8-16Ωcm material and future work will involve characterizing these devices for linearity and noise performance. It is expected that a complete non-recursive integrator could also be constructed with these devices.

Although the fabrication of a CCD parallel transfer non-recursive test chip would be difficult at present, some thought was given as to how such a system could be implemented. A scheme employing voltage sensing of the stored charge and off-chip clocking of the range bin CCDs appears to be the best choice since the chip complexity of this implementation is relatively low, and CCD structures could be used exclusively. The measured non-linearity of the voltage sensing scheme was compared with that predicted by the floating-gate analysis and close agreement was observed. Thus it is felt that the performance of a complete non-recursive integrator could be predicted fairly accurately.

Two fairly major topics concerning the integrators were purposely omitted from the discussions in this thesis. The first is the storage time capability of the devices. It was mentioned in Chapter 4 that storage times in excess of at least m x 100ms

are necessary for efficient clutter reduction. Future work would necessarily involve the inclusion of suitable fabrication procedures to consistently yield storage times of this order. The enormity of this subject, however, precluded further discussion here.

The second topic concerns the capability of the integration system to operate with moving platform radars. No problem arises as long as the target does not move out of its range resolution cell during the acquisition of at least m radar returns. However, if this condition is violated, then a provision for electronically adjusting the range gating operation must be made so that 'm' consecutive target echoes can be properly integrated. This could be accomplished for instance, by providing a number of parallel input sections along the RGR so that the sequential gating operation could be incremented or decremented by a resolution cell, as appropriate. Clearly, however, this subject warrants investigation in much greater detail.

As mentioned in Chapter 4, the parallel processing structures described in this thesis could be applied to many other areas of signal processing. This leaves a wide scope for further investigations.

APPENDIX 1: Analysis of the Two-Phase Charge Injection Scheme

The input structure of the two-phase charge injection scheme is shown in figure A1.1. Consider the situation when ϕ_1 is switching off. As the potential on the ϕ_1 electrode collapses, the surface potential differential beneath the thick and thin oxides decreases and excess charge will flow back onto the diode. There will come a point when the potential on ϕ_1 is equal to V_{in} (figure A1.1a); subsequent to this occurring, charge will begin to transfer forward into the metering well created by V_{in}. The charge, Q_1, at this instant is given by equation 2.2, and is

$$Q_1 = C_{ox}\left(\phi_o - V_{FBTN} - \phi_{STK} - \sqrt{2V_{oTN}\,\phi_{STK}}\right) \qquad A1.1$$

where ϕ_o will be equal to V_{in}, ϕ_{STK} is the surface potential beneath the thick oxide of G_1 held at a potential V_{in}, and the subscript TN denotes a thin oxide parameter.

As ϕ_1 continues to fall, more charge will be metered into the well below G_1; when ϕ_1 is OFF (figure A1.1b), the charge remaining, Q_2, can again be found from equation 2.2, and is

$$Q_2 = C_{ox}\left(\phi_{1_{OFF}} - V_{FBTN} - \phi_{STK} - \sqrt{2V_{oTN}\,\phi_{STK}}\right) \qquad A1.2$$

The signal charge, Q_s, metered by V_{in} is given by the difference between equation A1.1 and equation A.1.2, i.e.

$$Q_s = Q_1 - Q_2 = C_{ox}\,(\phi_o - \phi_{1_{OFF}}) \qquad A1.3$$

Since $\phi_o = V_{in}$,

$$Q_s = C_{ox}\,(V_{in} - \phi_{1_{OFF}}) \qquad A1.4$$

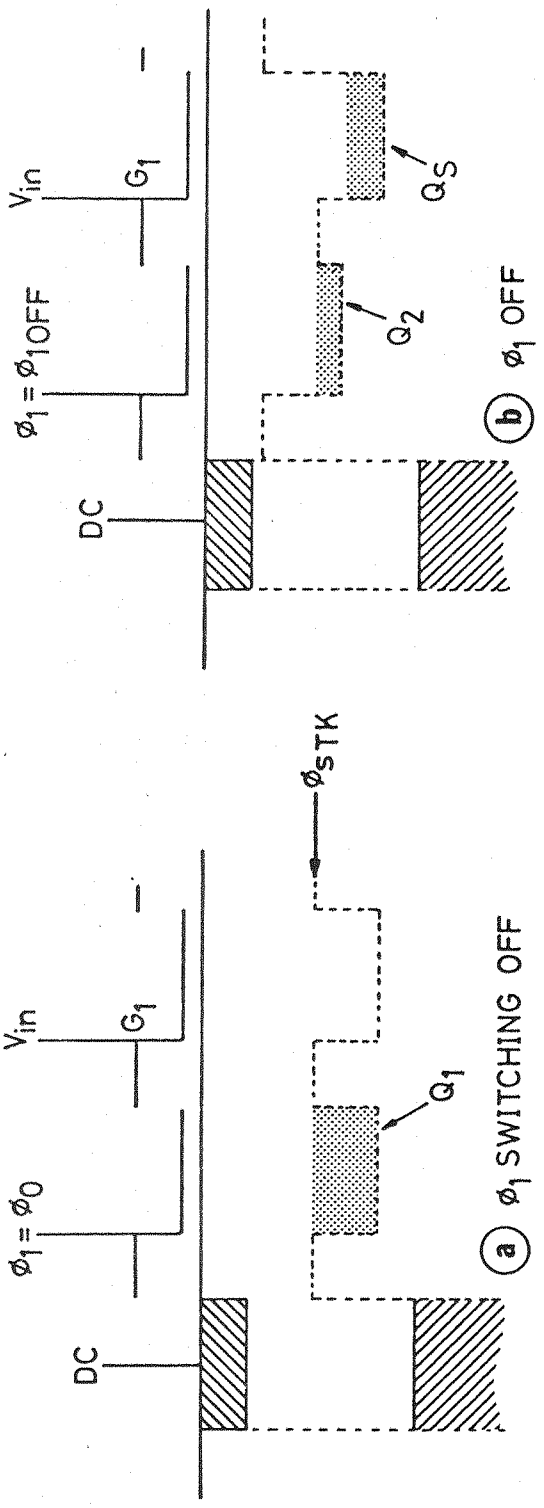


Fig A1.1 The two-phase charge injection scheme.

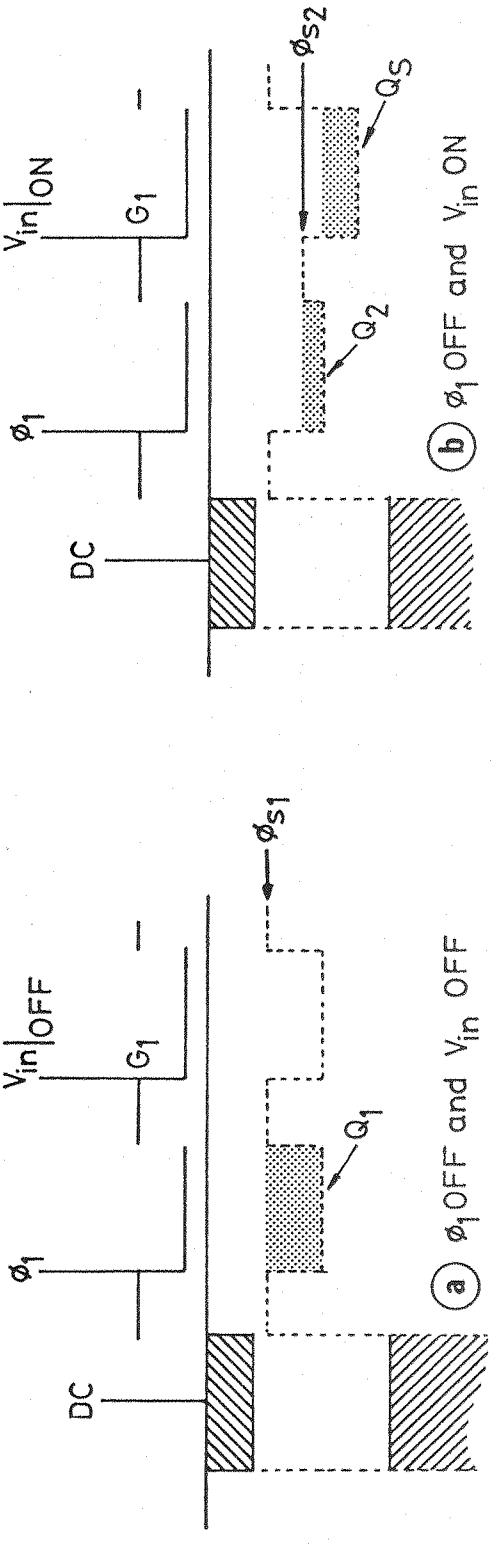


Fig A1.2 The two-phase charge injection scheme using a strobed input waveform.

It can be seen that the signal charge is linearly related to the input voltage.

Equation A1.4 was derived for the case when the input signal is continuously applied to G_1. If the input signal is strobed so that it is applied to G_1 only when ϕ_1 is off, the expression for Q_s can be derived as follows. The charge stored beneath ϕ_1 when both ϕ_1 and V_{in} are off (see figure A1.2a) is

$$Q_1 = C_{ox}\left(\phi_{1_{OFF}} - V_{FBTN} - \phi_{s_1} - \sqrt{2V_{oTN}\,\phi_{s_1}}\right) \qquad A1.5$$

When V_{in} is strobed on (see figure A1.2b), charge will flow beneath G_1 leaving a charge, Q_2, behind given by

$$Q_2 = C_{ox}\left(\phi_{1_{OFF}} - V_{FBTN} - \phi_{s_1} - \sqrt{2V_{oTN}\,\phi_{s_1}}\right) \qquad A1.6$$

The signal charge, Q_s , is thus given by

$$Q_s = Q_1 - Q_2 = C_{ox}\left[\phi_{s_2} - \phi_{s_1} + \sqrt{2V_{oTN}}\left\{\sqrt{\phi_{s_2}} - \sqrt{\phi_{s_1}}\right\}\right] \qquad A1.7$$

Substituting of ϕ_s and rearranging equation 2.2 to obtain expressions for $\sqrt{\phi_s}$ in terms of the gate voltage, equation A1.7 becomes

$$Q_s = C_{ox}\left[\left\{V_{in} - \phi_{1_{OFF}}\right\} + \left(1 - \sqrt{\frac{V_{oTN}}{V_{oTK}}}\right)\left(V_{oTK}^2 + 2V_{oTK}\left\{\phi_{1_{OFF}} - V_{FBTK}\right\}\right)^{\frac{1}{2}} - \left(V_{oTK}^2 + 2V_{oTK}\left\{V_{in} - V_{FBTK}\right\}\right)^{\frac{1}{2}}\right] \qquad A1.8$$

Clearly now, the signal charge is non-linearly related to the signal voltage.

APPENDIX 2: Analysis of Floating-Gate Voltage and Electrode Current Sensing Structures

In this Appendix, a paper recently published by the author in the IEE Journal of Solid-State and Electron Devices presenting an analysis of depletion capacitance-induced distortion in transversal filters, is reproduced. Both voltage and current sensing are discussed and the effects of using either a potential equilibration or the diode cut-off charge injection scheme are investigated.

Two computer programs used to evaluate the equations are also included. Program 1 enables the response of a three-phase split gate transversal filter to be analysed using any combination of charge injection and sensing scheme. The subroutines prefixed SN determine the harmonic components at a frequency f_cxNNF/NNN. The last two letters of the subroutine name indicate the type of charge input and sensing scheme used, i.e. V in the third position indicates voltage sensing, whilst Q indicates charge sensing. S in the last position indicates the diode cut-off input scheme, and Q represents the potential equilibration scheme, e.g. calling subroutine SNVQ (NNF, NNN, QPK, QDC) would evaluate the harmonic components at f_cxNNF/NNN for a signal charge of QPK and a fat-zero level of QDC.

Subroutines prefixed LF evaluate the low frequency harmonic components. Again, the last two letters specify the type of charge sensing and charge injection scheme used.

Subroutines prefixed DC can be used to determine the DC characteristics of the structure, similarly the last two letters are used to specify the charge sensing and injection techniques. The term VGG is a dummy parameter, and NFLG is generally set to 0.

The charge transfer inefficiency can be specified in the subroutine EPSILON(Q), and the tap weightings are simply included as data at the end of the program.

Program 2 was used to evaluate the non-linearity of the device described in Chapter 9. The computations include the loading effect of the thick oxide section of each gate. The subroutine CLOCKIT (W, 0.938, 1.119) evaluates the harmonic components at frequency W, with a peak-to-peak signal charge of 0.938pC and a fat-zero of 1.119pC.

Following this is a simple HP-25 programmable calculator routine for determining the potential variation of a single floating-gate as a function of charge.

PROGRAM 1

```
:EL1010.PAUL                    COMPILED BY FORTRAN LARGE BATCH COMPILER MARK 25A1 AT 12:29:15

            COMPILER OPTIONS

            FULL LIST
            NO PAGE SKIPS
            NO ATTRIBUTES LIST
            NO CROSS REFERENCE LIST
            NO EXTERNAL REFERENCE LIST
            NO OBJECT CODE LIST
            MEDIUM MESSAGES
            ALL MESSAGES LISTED
            MESSAGES INTERSPERSED
            COMMENTS LISTED
            DIRECTIVES LISTED
            NO SKIPPED LINES LISTED
            NOT SHAREABLE
            NOT LIBRARY PROCEDURE
            CODE PRODUCED UNLESS ERRORS
            POSTMORTEM LEVEL=2
            MAPPING OPTIONS :- E=8 D=8 Q=16 R=4 I=4 J=8 K=4 L=4 M=8 N=1
            MAXIMUM TRACE OPTIONS ALLOWED ARE :- ALL
            DEFAULT TRACE OPTIONS ARE :- NONE


REFERENCE   DIAGNOSTIC   SOURCE LISTING
        1                        PROGRAM PAULS LIST
        2                C       FLOATING GATE CCD ANALYSIS
        3                C       FLOATGATE ANALYSIS AS IN CCD 76
        4                        COMMON/BLOCK/M,Q(100),COX,VGO,VFB,CS,VO,DELVG,
        5                       *  CRAP(94),VB,CRIP(5),CCS
        6                C       INITIAL DATA
        7                C       CHARGES IN PC, CAPACITANCES IN PF
        8                C       M=NUMBER OF GATES
        9                        M=63
       10                C       VFB=FLATBAND VOLTAGE
       11                        VFB=0.0
       12                C       COX=OXIDE CAPACITANCE PER GATE
       13                        COX=0.3
       14                C       CCS=STRAY CAPACITANCE
       15                        CCS=50.
       16                C       VC=KSI*Q*N*TOT*TOX/KOX*KOX*EPSILON(?)
       17                        VO=0.173
       18                C       VGO=GATE VOLTS WITH NO SIGNAL CHARGE
       19                        VGO=15.
       20                C       VB= DIODE BIAS AT ZERO CHARGE INPUT
       21                        VB=12.888
       22                        CALL WEIGH
       23                C
       24                C       INSERT REQUIRED SUBROUTINES HERE  ********************************
       25                C       E.G.:
       26                        CALL SNVS(100,20,3.1,0.5)
       27                        CALL LEVQ(1.0,0.0)
       28                        CALL DOUG(0.5,DUMMY,0)
       29                C       ************************************************************************
       30                C
       31                        STOP
       32                        END
```

NO DIAGNOSTIC MESSAGES IN MODULE PAULSLIST

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
      33                       SUBROUTINE LFQQ(QPK,QDC)
      34                 C     GIVES LOW-FREQUENCY DISTORTION CHARACTERISTICS
      35                 C     FOR LINEAR CHARGE IN
      36                 C     FOR CHARGE SENSE OUT
      37                 C     DFT COMPONENTS EVALUATED EXPLICITLY
      38                       COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,COMPT(5),
      39                      *    CRAP(93),NPRINT,QMAX,CCS,PHI
      40                 C
      41                       WRITE(2,270) M,VO,VFB,COX,VGO
      42                   270 FORMAT(1HO,
      43                      1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
      44                      3' OXIDE CAP =',F6.3,
      45                      4' INITIAL GATE VOLTS =',F6.3,
      46                      5' LOW FREQUENCY')
      47                       WRITE(2,271) QPK,QDC
      48                   271 FORMAT(' QPK =',F7.4,' QDC =',F7.4)
      49                 C
      50                       QIN=QDC+QPK*2.0
      51                       CALL DCQQ(QIN,VG1,1)
      52                       IF(VG1.LE.0.) RETURN
      53                 C
      54                       QIN=QDC+QPK*1.5
      55                       CALL DCQQ(QIN,VG2,2)
      56                       QIN=QDC+QPK
      57                       CALL DCQQ(QIN,VG3,2)
      58                       QIN=QDC+QPK*0.5
      59                       CALL DCQQ(QIN,VG4,2)
      60                       CALL DCQQ(QDC,VG5,2)
      61                 C
      62                 C     EVALUATION OF COMPONENTS
      63                       COMPT(1)=(VG1-VG5)/2.
      64                       COMPT(2)=(VG1-2.*VG3+VG5)/4.
      65                       COMPT(3)=(VG5-2.*VG4+2.*VG2-VG1)/6.
      66                 C
      67                       DO 76 NH=1,3
      68                       COMPT(NH)=ABS(COMPT(NH))
      69                       IF(COMPT(NH).LT.1.E-20) COMPT(NH)=1.E-20
      70                       DB=20.*ALOG10(COMPT(NH))
      71                       WRITE(2,272) NH,COMPT(NH),DB
      72                    76 CONTINUE
      73                   272 FORMAT(' AMPLITUDE OF ',I2,'TH COMPONENT =',1PE10.3,
      74                      1' =',0PF6.1,' DB')
      75                 C
      76                       RETURN
      77                       END
```

NO DIAGNOSTIC MESSAGES IN MODULE LFQQ

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
```

```
      SUBROUTINE DCQQ(QDC,QOUT,NFLG)
      COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,CRAP(98),NPRINT,
C     D.C. CHARACTERISTIC
C     FOR LINEAR CHARGE IN
C     FOR CHARGE SENSE OUT
C     NFLG=0 UNLESS CALLDE BY LFQQ
     *  QMAX,CCS,PHI
WARNING(104) COMMENTS SHOULD NOT INTERSPERSE CONTINUATION LINES
      COMMON/WAIT/W(100),WBAR(100),H(100),W2(100),WB2(100),WWB(100),
     *   SUMW,SUMWBA,SUMWWB
      IF(NFLG.EQ.2) GOTO 12
      IF(NFLG.EQ.1) GOTO 11
      WRITE(2,2100) M,VC,VFB,COX,VGO
 2100 FORMAT(1HO,
     1 14,' GATES   VO =',F7.3,'   VFB =',F6.2,
     2 3'   OXIDE CAP =',F6.3,
     3 4'   INITIAL GATE VOLTS =',F6.3,
     4 5'  CHARGE SENSE')
   11 CONTINUE
C     CHECK FOR CHARGE OVERFLOW
      QMAX=COX*(VGO-VFB)
      IF(QDC.GT.QMAX) GOTO 95C
   12 CONTINUE
      S=SQRT(VC*(VO+2.*(VGO-VFB)))
      QDUM=(QDC/COX)-S+SQRT(VGO-VFB-QDC/COX)
      QPLUS=SUMW*QDUM
      QMIN=SUMWBA*QDUM
      QOUT=QPLUS-QMIN
      IF(NFLG.NE.0) RETURN
      GAIN=QOUT/QDC
      WRITE(2,2101) QDC,QOUT,GAIN
 2101 FORMAT(' QDC =',F6.3,' FC',
     1'   QOUT =',F8.4,' PC',
     2'   GAIN =',F7.3)
      RETURN
  950 WRITE(2,295) QDC,QMAX
  295 FORMAT(' CHARGE CAPACITY EXCEEDED  QIN =',F8.4,' QMAX =',F8.4)
      QOUT=-1.
      RETURN
      END
```

NO ERRORS , 1 WARNING AND NO COMMENTS IN MODULE DCQQ

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
      SUBROUTINE SNQQ(NNN,NNF,QPK,QDC)
C     FUNDAMENTAL AND HARMONICS AT FREQUENCY FC*NNF/NNN
C     FOR LINEAR CHARGE IN
C     FOR CHARGE SENSE OUT
C     DFT COMPONENTS OF O/P WAVEFORM GIVEN BY S/R FOURIER
C     ALLOWS FOR FINITE EPSILON USING FUNCTION EPSILON
      COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,CRAP(98),NPRINT,
     *  QMAX,CCS,PHI
      DIMENSION QQ(1500)
      CALL REDUCE(NNN,NNF,NN,NF)
      F=FLOAT(NF)/FLOAT(NN)
      WDYFC=6.28318530718*F
      WRITE(2,220) M,VC,VFB,COX,VGO,NF,NN,F
  220 FORMAT(1HO,
```

```
     1H4,' GATES   VO =',F7.3,'   VFB =',F6.2,
     3' OXIDE CAP =',F6.3,
     4'  INITIAL GATE VOLTS =',F6.3,
     5'  F/FC =',I3,'/',I4,' = ',F5.4
     6/)
C
C      INITIALISATION
       QMAX=VGO-VFB
       QMAX=QMAX*COX
       IF((QPK+QDC).GE.QMAX) GOTO 950
       DO 50 I=1,M
   50  Q(I)=0.0
C
       NMAX=M+NN
C
C      CLOCKING
       DO 52 N=1,NMAX
       M2=M+2
       DO 51 I=2,M
       II=M2-I
   51  Q(II)=EPSILON(Q(II))*Q(II)
     1   +(1.-EPSILON(Q(II-1)))*Q(II-1)
C
C      INPUT
       Q(1)=QDC+QPK*(1.+COS(WBYFC*N))
C
C      OUTPUT
       IF(N.GE.M) CALL SOLVQ(QQ(N))
C
   52  CONTINUE
C
       CALL FOURIER(NMAX,NN,NF,QQ,1,COMPNT1)
       CALL FOURIER(NMAX,NN,NF,QQ,2,COMPNT2)
       CALL FOURIER(NMAX,NN,NF,QQ,3,COMPNT3)
       RETURN
  950  WRITE(2,295) Q(1),QMAX
  295  FORMAT(' CHARGE CAPACITY EXCEEDED  QIN =',F8.4,' QMAX =',F8.4)
       RETURN
       END
```

NO DIAGNOSTIC MESSAGES IN MODULE SNQQ

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
       SUBROUTINE SNQS(NN,NF,VFK,VDC)
C      FUNDAMENTAL AND HARMONICS AT FREQUENCY FC*NNF/NNN
C      FOR SURFACE POTENTIAL SETTING INPUT
C      FOR CHARGE SENSE CUT
       COMMON/BLOCK/M,Q(100),COX,VGO,VFB,CS,VO,DELVG,
     *   CHAP(94),VB,CRIP(5),CCS
       DIMENSION QQ(1500)
       DIMENSION QQQ(1500)
C      CLOCKS A SIGNAL CHARGE 'QIN' ALONG CCD
C      OUTPUT FROM FLOATING GATE AMP GIVEN BY S/R SOLVIT
C      DFT COMPONENTS OF O/P WAVEFORM GIVEN BY S/R FOURIER
C      ALLOWS FOR FINITE EPSILON USING FUNCTION EPSILON
       W=(6.283185307I8*NF)/NN
       WRITE(2,220) M,VO,VFB,COX,VGO,NF,NN,VB,VPK,VDC
  220  FORMAT(1HO,
```

```
     185                     114,' GATES   VO =',F7.3,'   VFB =',F6.2,
     186                     3' OXIDE CAP =',F6.3,
     187                     4'  INITIAL GATE VOLTS =',F6.3,
     188                     5'  F/FC =',I3,'/',I3
     189                     6/'  DIODE BIAS =',F8.4,
     190                     7'   VPK =',F8.4,'   VDC =',F8.4,
     191                     8'SVQS'/)
     192               C
     193               C     INITIALISATION
     194                     DO 50 I=1,M
     195                  50 Q(I)=0.0
     196               C
     197                     NMAX=M+NN
     198                     DO 52 N=1,NMAX
     199               C
     200               C     CLOCKING
     201                     M2=M+2
     202                     DO 51 I=2,M
     203                     II=M2-I
     204                  51 Q(II)=EPSILON(Q(II))*Q(II)
     205                    1  +(1.-EPSILON(Q(II-1)))*Q(II-1)
     206               C
     207               C     INPUT
     208                     VD=VIN(W,N,VPK,VDC,VB)
     209                     QQG(N)=COX*(VGO-VD-SQRT(2.*VO*VD))
     210                     Q(1)=QQG(N)
     211               C
     212               C     OUTPUT
     213                     CALL SOLVQ(QG(N))
     214               C
     215                  52 CONTINUE
     216               C
     217                     WRITE(2,259)
     218                259 FORMAT(' INPUT CHARGE')
     219                     CALL FOURIER(NMAX,NN,NF,QQQ,1,C)
     220                     CALL FOURIER(NMAX,NN,NF,QQQ,2,C)
     221                     CALL FOURIER(NMAX,NN,NF,QQQ,3,C)
     222                     WRITE(2,258)
     223                258 FORMAT(' OUTPUT CHARGE')
     224                     CALL FOURIER(NMAX,NN,NF,QG,1,COMPNT1)
     225                     CALL FOURIER(NMAX,NN,NF,QG,2,COMPNT2)
     226                     CALL FOURIER(NMAX,NN,NF,QG,3,COMPNT3)
     227                     RETURN
     228                     END
```

NO DIAGNOSTIC MESSAGES IN MODULE SNQS

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     229                     SUBROUTINE SOLVQ(QDIFF)
     230               C     FLOATING GATE CCD ANALYSIS
     231               C     OBTAINS OUTPUT QDIFF FOR CHARGE SENSE OUTPUT
     232               C     FOR ARBITRARY CHARGE PACKETS Q(1),...,Q(M)
     233                     COMMON/WAIT/W(100),WBAR(100),H(100),W2(100),WB2(100),WWB(100),
     234                    *   SUMW,SUMWBA,SUMWWB
     235                     COMMON/BLOCK/M,Q(100),CCX,VFB,CS,VC,VGO,DELVG,CRAP(98),NPRINT,
     236                    *   QMAX,CCS,PHI
     237               C
     238                     S=SQRT(VO*(VO+2.*(VGO-VFB)))
```

```
239                         QPLUS=0.0
240                         QMIN=0.
241                         DO 20 I=1,M
242                         QP=Q(I)/COX-S+
243                        1      SQRT(VO*(VO+2.*(VGO-VFB-Q(I)/COX)))
244                   C     KNICKERS
245                         QPLUS=QPLUS+W(I)*QP
246                         QMIN=QMIN+WBAR(I)*QP
247                      20 CONTINUE
248                         QPLUS=QPLUS*COX
249                         QMIN=QMIN*COX
250                         QDIFF=QPLUS-QMIN
251                         RETURN
252                         END
```

NO DIAGNOSTIC MESSAGES IN MODULE SOLVQ

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
253                         SUBROUTINE DCVQ(QDC,VGG,NFLG)
254                   C     D.C. CHARACTERISTIC
255                   C     FOR LINEAR CHARGE IN
256                   C     VOLTAGE SENSING OUTPUT
257                   C     NFLG=0 UNLESS CALLDE BY LFVQ
258                         COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,CRAP(98),NPRINT,
259                        *  QMAX,CCS,PHI
260                         COMMON/WAIT/CRIP(600),SUMW,SUMWBA,SUMWWB
261                         CS=CCS/COX
262                         PHI=1.0+(VGO-VFB)*2./VO
263                         IF(NFLG.EQ.2) GOTO 12
264                         IF(NFLG.EQ.1) GOTO 11
265                         WRITE(2,2100) M,VC,VFB,CCS,COX,VGO
266                      2100 FORMAT(1HU,
267                        1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
268                        3'   STRAY CAP =',F6.3,
269                        3'   OXIDE CAP =',F6.3,
270                        4'   INITIAL GATE VOLTS =',F6.3,
271                        6'DCVQ'/)
272                        11 CONTINUE
273                   C     CHECK FOR CHARGE OVERFLOW
274                         QMAX=(SQRT(PHI)+PHI*CS/(SUMW*2.))/(1.+CS/SUMW)
275                         QMB=(SQRT(PHI)+PHI*CS/(SUMWBA*2.))/(1.+CS/SUMWBA)
276                         IF(QMB.LT.QMAX) QMAX=QMB
277                         QMAX=VO*COX*QMAX
278                         IF(QDC.GT.QMAX) GOTO 95C
279                        12 CONTINUE
280                         PSI=VC/CS + VC*SQRT(PHI)
281                         QSIG=QDC
282                         ARG=PSI*PSI-2.*QSIG*VC*(1.+(1./CS))/COX
283                         VGG=((QSIG/COX)-PSI+SQRT(ARG))/CS
284                         IF(NFLG.NE.0) RETURN
285                         SEX=VGG/QDC
286                         WRITE(2,2101) QDC,VGG,SEX
287                      2101 FORMAT(' QDC =',F6.3,' PC',
288                        1'   VOUT =',F7.3,' V',
289                        2'   VOUT/QIN =',F8.4,' /PF'
290                        3)
291                         RETURN
292                      95C WRITE(2,295) QDC,QMAX
```

```
      293                  295 FORMAT(' CHARGE CAPACITY EXCEEDED  QIN =',F8.4,'  QMAX =',F8.4)
      294                      VGG=-1.
      295                      RETURN
      296                      END
```

NO DIAGNOSTIC MESSAGES IN MODULE DCVQ

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
      297                      SUBROUTINE LFVQ(QPK,QDC)
      298                C     GIVES LOW-FREQUENCY DISTORTION CHARACTERISTICS
      299                C     FOR LINEAR CHARGE IN
      300                C     VOLTAGE SENSING OUTPUT
      301                C     DFT COMPONENTS EVALUATED EXPLICITLY
      302                      COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,COMPT(5),
      303                     *  CRAP(93),NPRINT,QMAX,CCS,PHI
      304                C
      305                      WRITE(2,270) M,VO,VFB,CCS,COX,VGO
      306                  270 FORMAT(1HO,
      307                     1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
      308                     2' STRAY CAP =',F6.3,
      309                     3' OXIDE CAP =',F6.3,
      310                     4' INITIAL GATE VOLTS =',F6.3,
      311                     5'  LOW FREQUENCY',
      312                     6'LFVQ'/)
      313                      WRITE(2,271) QPK,QDC
      314                  271 FORMAT(' QPK =',F7.4,' QDC =',F7.4)
      315                      NPRINT=0
      316                      QIN=QDC+QPK*2.0
      317                      CALL DCVQ(QIN,VG1,1)
      318                      IF(VG1.LE.0.) RETURN
      319                      QIN=QDC+QPK*1.5
      320                      CALL DCVQ(QIN,VG2,2)
      321                      QIN=QDC+QPK
      322                      CALL DCVQ(QIN,VG3,2)
      323                      QIN=QDC+QPK*0.5
      324                      CALL DCVQ(QIN,VG4,2)
      325                      CALL DCVQ(QDC,VG5,2)
      326                C
      327                C
      328                C     EVALUATION OF COMPONENTS
      329                      COMPT(1)=(VG1-VG5)/2.
      330                      COMPT(2)=(VG1-2.*VG3+VG5)/4.
      331                      COMPT(3)=(VG5-2.*VG4+2.*VG2-VG1)/6.
      332                C
      333                      DO 76 NH=1,3
      334                      COMPT(NH)=ABS(COMPT(NH))
      335                      IF(COMPT(NH).LT.1.E-20) COMPT(NH)=1.E-20
      336                      DB=20.*ALOG10(COMPT(NH))
      337                      WRITE(2,272) NH,COMPT(NH),DB
      338                   76 CONTINUE
      339                  272 FORMAT(' AMPLITUDE OF ',I2,'TH COMPONENT =',1PE10.3,
      340                     1' =',0PF6.1,' DB')
      341                      RETURN
      342                      END
```

NO DIAGNOSTIC MESSAGES IN MODULE LFVQ

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     343                        SUBROUTINE SNVQ(NNN,NNF,QPK,QDC)
     344                  C     FUNDAMENTAL AND HARMONICS AT FREQUENCY FC*NNF/NNN
     345                  C     FOR LINEAR CHARGE IN
     346                  C     VOLTAGE SENSING OUTPUT
     347                  C     DFT COMPONENTS OF O/P WAVEFORM GIVEN BY S/R FOURIER
     348                  C     ALLOWS FOR FINITE EPSILON USING FUNCTION EPSILON
     349                        COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,CRAP(98),NPRINT,
     350                       *   QMAX,CCS,PHI
     351                        COMMON/WAIT/W(100),WBAR(100),H(100),W2(100),WB2(100),WWB(100),
     352                       *   SUMW,SUMWBA,SUMWWB
     353                        DIMENSION VG(1500)
     354                        CALL REDUCE(NNN,NNF,NN,NF)
     355                        F=FLOAT(NF)/FLOAT(NN)
     356                        WBYFC=6.283185307178*F
     357                        WRITE(2,220) M,VO,VFB,CCS,COX,VGO,NF,NN,F
     358                   220  FORMAT(1HC,
     359                       1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
     360                       2'STRAY CAP=',F6.3,
     361                       3' OXIDE CAP =',F6.3,
     362                       4'  INITIAL GATE VOLTS =',F6.3,
     363                       5'   F/FC =',I3,'/',I4,' =',F6.4,
     364                       6'SNVQ'/)
     365                  C
     366                  C     INITIALISATION
     367                        PHI=1.0+(VGO-VFB)*2./VO
     368                        CS=CCS/COX
     369                        QMAX=(SQRT(PHI)+PHI*CS/(SUMW*2.))/(1.+CS/SUMW)
     370                        QMB=(SQRT(PHI)+PHI*CS/(SUMWBA*2.))/(1.+CS/SUMWBA)
     371                        IF(QMB.GT.QMAX) QMAX=QMB
     372                        QMAX=VO*COX*QMAX
     373                        QM=QDC+2.*QPK
     374                        IF(QM.GE.QMAX) GOTO 950
     375                        DO 50 I=1,M
     376                   50   Q(I)=0.0
     377                        NMAX=M+NN
     378                  C
     379                  C     CLOCKING
     380                        DO 52 N=1,NMAX
     381                        M2=M+2
     382                        DO 51 I=2,M
     383                        II=M2-I
     384                   51   Q(II)=EPSILON(Q(II))*Q(II)
     385                       1  +(1.-EPSILON(Q(II-1)))*Q(II-1)
     386                  C
     387                  C     INPUT
     388                        Q(1)=QDC+QPK*(1.+COS(WBYFC*N))
     389                  C
     390                  C     OUTPUT
     391                        IF(N.GE.M) CALL SOLVV(VG(N))
     392                  C
     393                  C
     394                   52   CONTINUE
     395                        CALL FOURIER(NMAX,NN,NF,VG,1,COMPNT)
     396                        CALL FOURIER(NMAX,NN,NF,VG,2,COMPNT)
     397                        CALL FOURIER(NMAX,NN,NF,VG,3,COMPNT)
     398                        RETURN
     399                  950   WRITE(2,295) QM,QMAX
     400                  295   FORMAT(' CHARGE CAPACITY EXCEEDED  QIN =',F8.4,' QMAX =',F8.4)
```

```
      401                         RETURN
      402                         END
```

NO DIAGNOSTIC MESSAGES IN MODULE SNVQ

```
REFERENCE    DIAGNOSTIC   SOURCE LISTING
      403                         SUBROUTINE DCVS(VV)
      404                   C     D.C. CHARACTERISTIC
      405                   C     VOLTAGE SENSING OUTPUT
      406                   C     FOR SURFACE POTENTIAL SETTING INPUT
      407                         COMMON/BLOCK/M,Q(100),COX,VGO,VFB,CS,VO,DELVG,
      408                        *  CRAP(94),VB,CRIP(5),CCS
      409                         WRITE(2,2100) M,VC,VFB,COX,VGO,VB
      410                2100   FORMAT(1HO,
      411                       1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
      412                       3'   OXIDE CAP =',F6.3,
      413                       4'   INITIAL GATE VOLTS =',F6.3,
      414                       *1X
      415                       */'   DIODE BIAS =',F8.4,
      416                       5'DCVS'/)
      417                         VD=VB-VV
      418                         QDC=COX*(VGO-VD-SQRT(2.*VO*VD))
      419                         DO 101 I=1,M
      420                  101  Q(I)=QDC
      421                         CALL SOLVITW(QOUT)
      422                         SEX=QOUT/VV
      423                         WRITE(2,2101) VV,VD,QDC,QOUT,SEX
      424                2101   FORMAT(
      425                       *'   VIN =',F8.4,
      426                       *'   DIODE VOLTS =',F8.4,
      427                       *'   I/P CHARGE PACKET =',F8.4,
      428                       *'   O/P CHARGE =',F8.4,
      429                       *'   QOUT/VIN =',F8.4,
      430                       *1X)
      431                         RETURN
      432                         END
```

NO DIAGNOSTIC MESSAGES IN MODULE DCVS

```
REFERENCE    DIAGNOSTIC   SOURCE LISTING
      433                         SUBROUTINE LFVS(VPK,VDC)
      434                   C     GIVES LOW-FREQUENCY DISTORTION CHARACTERISTICS
      435                   C     FOR SURFACE POTENTIAL SETTING INPUT
      436                   C     VOLTAGE SENSING OUTPUT
      437                   C     DFT COMPONENTS EVALUATED EXPLICITLY
      438                         COMMON/BLOCK/M,Q(100),COX,VGO,VFB,CS,VO,DELVG,
      439                        *COMPT(5),QQQ(5),CRAP(84),VB,CRIP(5),CCS
      440                   C
      441                         WRITE(2,270) M,VC,VFB,COX,VGO,VB,VPK,VDC
      442                  270    FORMAT(1HO,
```

```
     1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
     3' OXIDE CAP =',F6.3,
     4' INITIAL GATE VOLTS =',F6.3,
     5'   LOW FREQUENCY',
     *1X
     6/'  DIODE BIAS =',F8.4,
     7'   VPK =',F8.4,'   VDC =',F8.4,
     5'LEVS'/)
C
      VD=-2.0*VPK-VDC+VB
      QQ1=COX*(VGO-VD-SQRT(2.*VC*VD))
      DO 71 I=1,M
   71 Q(I)=QQ1
      CALL SOLVV(VG1)
C
      VD=-1.5*VPK-VDC+VB
      QQ2=COX*(VGO-VD-SQRT(2.*VC*VD))
      DO 72 I=1,M
   72 Q(I)=QQ2
      CALL SOLVV(VG2)
C
      VD=-1.0*VPK-VDC+VB
      QQ3=COX*(VGO-VD-SQRT(2.*VO*VD))
      DO 73 I=1,M
   73 Q(I)=QQ3
      CALL SOLVV(VG3)
C
      VD=-0.5*VPK-VDC+VB
      QQ4=COX*(VGO-VD-SQRT(2.*VC*VD))
      DO 74 I=1,M
   74 Q(I)=QQ4
      CALL SOLVV(VG4)
C
      VD=-VDC+VB
      QQ5=COX*(VGO-VD-SQRT(2.*VC*VD))
      DO 75 I=1,M
   75 Q(I)=QQ5
      CALL SOLVV(VG5)
C
C     EVALUATION OF COMPONENTS
      WRITE(2,279)
  279 FORMAT(' INPUT CHARGE')
      COMPT(1)=(QQ1-QQ5)/2.
      COMPT(2)=(QQ1-2.*QQ3+QQ5)/4.
      COMPT(3)=(QQ5-2.*QQ4+2.*QQ2-QQ1)/6.
      DO 77 NH=1,3
      COMPT(NH)=ABS(COMPT(NH))
      IF(COMPT(NH).LT.1.E-20) COMPT(NH)=1.E-20
      DB=20.*ALOG10(COMPT(NH))
      WRITE(2,272) NH,COMPT(NH),DB
   77 CONTINUE
      WRITE(2,278)
  278 FORMAT(' OUTPUT CHARGE')
      COMPT(1)=(VG1-VG5)/2.
      COMPT(2)=(VG1-2.*VG3+VG5)/4.
      COMPT(3)=(VG5-2.*VG4+2.*VG2-VG1)/6.
      DO 76 NH=1,3
      COMPT(NH)=ABS(COMPT(NH))
      IF(COMPT(NH).LT.1.E-20) COMPT(NH)=1.E-20
      DB=20.*ALOG10(COMPT(NH))
      WRITE(2,272) NH,COMPT(NH),DB
   76 CONTINUE
  272 FORMAT(' AMPLITUDE OF ',I2,'TH COMPONENT =',1PE10.3,
     1' =',0PF6.1,' DB')
C
      RETURN
```

```
 509                      END

          NO DIAGNOSTIC MESSAGES IN MODULE LFVS

REFERENCE   DIAGNOSTIC   SOURCE LISTING
    510                      SUBROUTINE SNVS(NN,NF,VPK,VDC)
    511                C     FUNDAMENTAL AND HARMONICS AT FREQUENCY FC*NNF/NNN
    512                C     FOR SURFACE POTENTIAL SETTING INPUT
    513                C     VOLTAGE SENSING OUTPUT
    514                C     DFT COMPONENTS OF O/P WAVEFORM GIVEN BY S/R FOURIER
    515                C     ALLOWS FOR FINITE EPSILON USING FUNCTION EPSILON
    516                      COMMON/BLOCK/M,Q(100),COX,VGO,VFB,CS,VO,DELVG,
    517                     *  CRAP(94),VB,CRIP(5),CCS
    518                      DIMENSION QG(1500)
    519                      DIMENSION QQQ(1500)
    520                      W=(6.28318530718*NF)/NN
    521                      WRITE(2,220) M,VO,VFB,COX,VGO,NF,NN,VB,VPK,VDC
    522                  220 FORMAT(1HC,
    523                     1I4,' GATES   VO =',F7.3,'   VFB =',F6.2,
    524                     3' OXIDE CAP =',F6.3,
    525                     4'  INITIAL GATE VOLTS =',F6.3,
    526                     5'  F/FC =',I3,'/',I3
    527                     6/'  DIODE BIAS =',F8.4,
    528                     7'   VPK =',F8.4,'   VDC =',F8.4,
    529                     8'SNVS'/)
    530                C
    531                C     INITIALISATION
    532                      DO 50 I=1,M
    533                   50 Q(I)=0.0
    534                C
    535                      NMAX=M+NN
    536                      DO 52 N=1,NMAX
    537                C
    538                C     CLOCKING
    539                      M2=M+2
    540                      DO 51 I=2,M
    541                      II=M2-I
    542                   51 Q(II)=EPSILON(Q(II))*Q(II)
    543                     1  +(1.-EPSILON(Q(II-1)))*Q(II-1)
    544                C
    545                C     INPUT
    546                      VD=VIN(W,N,VPK,VDC,VB)
    547                      QQQ(N)=COX*(VGO-VD-SQRT(2.*VO*VD))
    548                      Q(1)=QQQ(N)
    549                C
    550                C     OUTPUT
    551                      CALL SOLVV(QG(N))
    552                C
    553                   52 CONTINUE
    554                C
    555                      WRITE(2,259)
    556                  259 FORMAT(' INPUT CHARGE')
    557                      CALL FOURIER(NMAX,NN,NF,QQQ,1,C)
    558                      CALL FOURIER(NMAX,NN,NF,QQQ,2,C)
    559                      CALL FOURIER(NMAX,NN,NF,QQQ,3,C)
    560                      WRITE(2,258)
    561                  258 FORMAT(' OUTPUT VOLTS')
    562                      CALL FOURIER(NMAX,NN,NF,QG,1,COMPNT1)
```

```
      CALL FOURIER(NMAX,NN,NF,QQ,2,COMPNT2)
      CALL FOURIER(NMAX,NN,NF,QQ,3,COMPNT3)
      RETURN
      END
```

NO DIAGNOSTIC MESSAGES IN MODULE SNVS

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
      SUBROUTINE SOLVV(VDIFF)
C     GETS 'VDIFF' - OUTPUT FROM VOLTSENSE OUTPUT
C     FOR ARBITRARY CHARGE PACKETS Q(1),...,Q(M)
      COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,CRAP(98),NPRINT,
     *   QMAX,CCS,PHI
      COMMON/WAIT/W(100),WBAR(100),H(100),W2(100),WB2(100),WWB(100),
     *   SUMW,SUMWBA,SUMWWB
      DIMENSION QQ(100)
C     .FLOATING GATE CCD ANALYSIS
C     SOLVES EQN F(PSI,QQ,...)=0
      SUMQ=0.0
      SUMQW=0.0
      SUMQWB=0.0
      QMOST=0.0
      DO 29 I=1,M
      QQ(I)=Q(I)/(VO*COX)
      SUMQ=SUMQ+QQ(I)
      SUMQW=SUMQW+QQ(I)*W(I)
      SUMQWB=SUMQWB+QQ(I)*WBAR(I)
      IF(QQ(I).GT.QMOST) QMOST=QQ(I)
   29 CONTINUE
C
      PHI=1.0+(VGO-VFB)*2.0/VO
      PSIMIN=QMOST-PHI/2.
      CS=CCS/COX
C
C     CHECK FOR NON-ZERO CHARGE PACKET
      IF(QMOST.GT.1.E-8) GOTO 23
      PSI=0.0
      PSIBA=0.0
      GOTO 26
   23 CONTINUE
C     CHECK FOR NONZERO TAP WEIGHTING
      IF(SUMW.GT.1.E-6) GOTO 28
      PSI=0.0
      GOTO 22
   28 CONTINUE
C     CHECK FOR CHARGE OVERFLOW
      QMAX=(SQRT(PHI)+PHI*CS/(SUMW*2.))/(1.+CS/SUMW)
      IF(QMOST.LE.QMAX) GOTO 302
      QMAX=QMAX*VO*COX
      WRITE(2,298) QMAX
  298 FORMAT(1H+,
     1   25X,'CCD HAS OVERFLOWED (PERHAPS) QMAX =',
     2   F8.3)
      VDIFF=VGO
      RETURN
  302 CONTINUE
C     NEWTON-RAPHSON METHOD
      PSI=-SUMQW/(CS+SUMW)
```

```
      NIT=0
      PSIOLD=0.0
   21 CONTINUE
      NIT=NIT+1
      IF(PSI.LE.PSIMIN) PSI=(PSIOLD+PSIMIN)/2.
      PSIOLD=PSI
      T= FW(PSI,QQ,CS,PHI,M,W,SUMW)
      B=DFW(PSI,QQ,CS,PHI,M,W,SUMW)
      PSI=PSI-T/B
      IF(PSI.EQ.0.0) GOTO 22
      ERR=1.-PSIOLD/PSI
      ERR=ABS(ERR)
      IF(NIT.LT.30.AND.ERR.GT.1.E-6) GOTO 21
      IF(NIT.EQ.30) WRITE(2,299)ERR,PSI
  299 FORMAT(' NO CONVERGENCE',1PE10.3,E10.3)
   22 CONTINUE
C
C     FOR OTHER TAPS
C     CHECK FOR NONZERO TAP WEIGHTING
      IF(SUMWBA.GT.1.E-6) GOTO 288
      PSIBA=0.0
      GOTO 26
  288 CONTINUE
C     CHECK FOR CHARGE OVERFLOW
     .QMAXB=(SQRT(PHI)+PHI*CS/(SUMWBA*2.))/(1.+CS/SUMWBA)
      IF(QMOST.LE.QMAXB) GOTO 303
      VDIFF=-VGC
      QMAXB=QMAXB*COX*VC
      WRITE(2,298) QMAXB
      RETURN
  303 CONTINUE
      PSIBA=-SUMQWB/(CS+SUMWBA)
      NIT=0
      PSIOLD=0.0
   25 CONTINUE
      NIT=NIT+1
      IF(PSIBA.LE.PSIMIN) PSIBA=(PSIOLD+PSIMIN)/2.
      PSIOLD=PSIBA
      T= FW(PSIBA,QQ,CS,PHI,M,WBAR,SUMWBA)
      B=DFW(PSIBA,QQ,CS,PHI,M,WBAR,SUMWBA)
      PSIBA=PSIBA-T/B
      IF(PSIBA.EQ.0.0) GOTO 26
      ERR=1-PSIOLD/PSIBA
      ERR=ABS(ERR)
      IF(NIT.EQ.30) WRITE(2,299) ERR,PSI
      IF(ERR.GT.1.E-6.AND.NIT.LT.30) GOTO 25
   26 CONTINUE
C
C     DENORMALISATION AND PRINT OUT
      DELVG=-PSI*VO
C     KNICKERS
      DELVGB=-PSIBA*VO
      VDIFF=DELVG-DELVGB
      RETURN
      END
```

NO DIAGNOSTIC MESSAGES IN MODULE SOLVV

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     672                        FUNCTION  FW(PSI,QQ,CS,PHI,M,W,SUMW)
     673                        DIMENSION QQ(100)
     674                        DIMENSION W(100)
     675                        SUMQ=0.
     676                        SUMSQT=0.
     677                        PH2SI=PHI+2.0*PSI
     678                        DO 30 I=1,M
     679                        SUMQ=SUMQ+QQ(I)*W(I)
     680                        SUMSQT=SUMSQT+SQRT(PH2SI-2.0*QQ(I))*W(I)
     681                     30 CONTINUE
     682                        FW=SUMQ+SUMSQT-SUMW*SQRT(PHI)+CS*PSI
     683                        RETURN
     684                        END
```

NO DIAGNOSTIC MESSAGES IN MODULE FW

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     685                        FUNCTION DFW(PSI,QQ,CS,PHI,M,W,SUMW)
     686                        DIMENSION QQ(100)
     687                        DIMENSION W(100)
     688                        DFW=CS
     689                        PH2SI=PHI+2.0*PSI
     690                        DO 40 I=1,M
     691                        DFW=DFW+W(I)/SQRT(PH2SI-2.0*QQ(I))
     692                     40 CONTINUE
     693                        RETURN
     694                        END
```

NO DIAGNOSTIC MESSAGES IN MODULE DFW

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     695                        SUBROUTINE WEIGH(NFLAG1)
     696                        COMMON/WAIT/W(100),WBAR(100),H(100),W2(100),WB2(100),WWB(100),
     697                       *   SUMW,SUMWBA,SUMWWB
     698                        COMMON/BLOCK/M,CRAP(208)
     699                        WRITE(2,280)
     700                   280  FORMAT(' TAP WEIGHTS'/5X,'I    H(I)     W(I)     1-W(I)')
     701                        SUMW=0.
     702                        SUMWBA=0.
     703                        SUMWWB=0.
     704                        HMAX=0.0
     705                        HMIN=0.0
     706                        DO 80 I=1,M
     707                        READ(1,*) H(I)
     708                        IF(H(I).GT.HMAX) HMAX=H(I)
     709                        IF(H(I).LT.HMIN) HMIN=H(I)
     710                     80 CONTINUE
     711                        IF(ABS(HMIN).GT.HMAX) HMAX=ABS(HMIN)
     712                        DO 81 I=1,M
```

```
      713                       HOR=H(I)/(HMAX*2.)
      714                       IF(NFLAG1.NE.1) HOR=H(I)
      715                       W(I)=0.5+HOR
      716                       WBAR(I)=0.5-HOR
      717                       W2(I)=W(I)*W(I)
      718                       WB2(I)=WBAR(I)*WBAR(I)
      719                       WWB(I)=W(I)*WBAR(I)
      720                       SUMW=SUMW+W(I)
      721                       SUMWBA=SUMWBA+WBAR(I)
      722                       SUMWWB=SUMWWB+WWB(I)
      723                       WRITE(2,281) I,H(I),W(I),WBAR(I)
      724                    81 CONTINUE
      725                   281 FORMAT(I6,3F8.4)
      726                       IF(SUMW.LT.1.E-6.OR.SUMWBA.LT.1.E-6) STOP
      727                       RETURN
      728                       END
```

NO DIAGNOSTIC MESSAGES IN MODULE WEIGH

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
      729                       SUBROUTINE REDUCE(NNN,NNF,NN,NF)
      730                    C  REDUCTION OF NNF/NNN TO LOWEST NUMBERS
      731                       NFAC=1
      732                       NF=NNF
      733                       NN=NNN
      734                       IF(MOD(NN,NF).NE.0) GOTO 54
      735                       NN=NN/NF
      736                       NF=1
      737                       RETURN
      738                    54 NFMAX=INT(SQRT(FLOAT(NF)))
      739                    55 NFAC=NFAC+1
      740                    56 CONTINUE
      741                       IF(NFAC.GT.NFMAX) RETURN
      742                       IF(MOD(NF,NFAC).NE.0.OR.MOD(NN,NFAC).NE.0) GOTO 55
      743                       NF=NF/NFAC
      744                       NN=NN/NFAC
      745                       GOTO 56
      746                       END
```

NO DIAGNOSTIC MESSAGES IN MODULE REDUCE

```
REFERENCE   DIAGNOSTIC   SOURCE LISTING
      747                       FUNCTION VIN(WBYFC,N,VPK,VDC,VB)
      748                       VV=1.+COS(WBYFC*N)
      749                       VV=VDC+VV*VPK
      750                       VIN=VB-VV
      751                       RETURN
      752                       END
```

NO DIAGNOSTIC MESSAGES IN MODULE VIN

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     753                        FUNCTION EPSILON(Q)
     754                        EPSILON=1E-2
     755                        RETURN
     756                        END
```

NO DIAGNOSTIC MESSAGES IN MODULE EPSILON

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
     757                        SUBROUTINE FOURIER(NMAX,NN,NF,SIGNAL,NH,COMPNT)
     758                        DIMENSION SIGNAL(1500)
     759                  C     'COMPNT' IS 'NH'TH COMPONENT OF DISCRETE FOURIER TRANSFORM OF
     760                  C     LAST 'NN' POINTS OF ARRAY 'SIGNAL' ENDING WITH 'SIGNAL(NMAX)'
     761                        PI2=6.28318530718
     762                        TIT=2.*COS(((PI2*NH)*NF)/NN)
     763                        A=0.
     764                        B=0.
     765                        II=NMAX
     766                        DO 60 I=1,NN
     767                        AA=A
     768                        A=TIT*A-B+SIGNAL(II)
     769                        B=AA
     770                   60   II=II-1
     771                        COMPNT=A*A-A*B*TIT+B*B
     772                        COMPNT=COMPNT*4./(NN*NN)
     773                        IF(COMPNT.LT.1.E-24) COMPNT=1.E-24
     774                        COMPNT=SQRT(COMPNT  )
     775                        DB=20.*ALOG10(COMPNT)
     776                        WRITE(2,260) NH,COMPNT,DB
     777                  260   FORMAT(' AMPLITUDE OF ',I2,'TH HARMONIC =',1PE10.3,
     778                       1' =',CPF6.1,' DB')
     779                        RETURN
     780                        END
```

NO DIAGNOSTIC MESSAGES IN MODULE FOURIER

```
REFERENCE    DIAGNOSTIC    SOURCE LISTING
```

DIAGNOSTIC MESSAGES OCCUR IN THE FOLLOWING SOURCE MODULES:

PROGRAM 2

```
14/10/76 UNIVERSITY OF MINNESOTA 7600 FORTRAN COMPILER SCOPE  2,1,3 VER4,5      07/07/77
      MNF(E=5)
 000000B        1       PROGRAM FGOO(INPUT,OUTPUT,TAPE1=INPUT,TAPE2=OUTPUT)
 000047B        2       COMMON/BLOCK/M,Q(100),COX,VFB,CS,V0,VG0,DELVG,QOLD(100),CCS
 000047B        3       COMMON/TWOPH/V0K,ALPHA,VFBK
                C       FLOATING GATE CCD ANALYSIS
                C       GIVEN CHARGES, TO FIND NEW GATE POETENTIAL
                C       FOR TWO-LEVEL OXIDE DEVICE
                C
                C       INITIAL DATA
                C       CHARGES IN PC, CAPACITANCES IN PF
                C       M=NUMBER OF GATES
 000047B        4       M=50
                C       VFB=FLATBAND VOLTAGE
 000047B        5       VFB=0.8
                C       VFBK=THICK VFB
 000050B        6       VFBK=2.5
                C       CCS=STRAY CAPACITANCE
 000052B        7       CCS=10.5
                C       COX=OXIDE CAPACITANCE PER GATE
 000053B        8       COX=0.05588
                C       V0=FSI*Q*N*TOT*TOX/KOX*KOX*EPSILON(0)
 000055B        9       V0=0.4
                C       V0K=THICK OXIDE V0
                C       V0K/V0=TOXK*TOXK/TOXN*TOXN
 000056B       10       V0K=6.946
                C       ALPHA=RATIO OF AREAS OF THICKTHIN GATES
 000060B       11       ALPHA=0.375
                C       VG0=GATE VOLTS WITH NO SIGNAL CHARGE
 000061B       12       VG0=11.6
                C       Q(I)=SIGNAL CHARGES UNDER EACH GATE (PC)
 000063B       13       PI=3.141592654
 000064B       14       CALL LOFREQ(0.938,1.119)
 000067B       15       I=200
 000067B       16       W=2.*PI/I
 000071B       17       CALL CLOCKIT(W,0.938,1.119)
 000074B       18       DO 1 I=6,25
 000075B       19       W=2.*PI/I
 000076B       20       CALL CLOCKIT(W,0.938,1.119)
 000102B       21     1 CONTINUE
 000104B       22       DO 2 I=26,100,2
 000106B       23       W=2.*PI/I
 000107B       24       CALL CLOCKIT(W,0.938,1.119)
 000113B       25     2 CONTINUE
 000115B       26       STOP
 000116B       27       END


 000000B        1       SUBROUTINE SOLVIT
 000000B        2       COMMON/BLOCK/M,Q(100),COX,VFB,CS,V0,VG0,DELVG,QOLD(100),CCS
 000000B        3       COMMON/TWOPH/V0K,ALPHA,VFBK
 000000B        4       DIMENSION QQ(100)
                C       FLOATING GATE CCD ANALYSIS
                C       SOLVES FOR F(PSI,QQ,...)=0
 000000B        5       SUMQ=0.0
 000144B        6       DO 29 I=1,M
 000147B        7       SUMQ=SUMQ+Q(I)
 001479         8     29 CONTINUE
                C
                C       NORMALISATION
 001548B        9       QMAX=0.0
 001548B       10       CS=CCS/COX
 001556B       11       DO 20 I=1,M
 001561B       12       QQ(I)=Q(I)/(V0*COX)
 001563B       13       IF(QQ(I).GT.QMAX) QMAX=QQ(I)
```

```
000167B    14      20 CONTINUE
000171B    15         PHIN=1.0+(VGP-VFB)*2./V0
000175B    16         PHIK=V2K/V0 + 2.*(VGP-VFBK)/V0
000201B    17         PHIK=ALPHA*ALPHA*PHIK
000203B    18         QBYCOX=SUMQ/(COX*M)
                C
                C     NEWTON-RAPHSON METHOD
000205B    19         PSI=-QBYCOX/V0
000207B    20         NIT=0
000210B    21         PSIMIN=QMAX -  PHIN/2.0
000213B    22      21 CONTINUE
000214B    23         NIT=NIT+1
000215B    24         PSIOLD=PSI
000216B    25         T= F2PH(PSI,QQ,CS,PHIN,PHIK,M,ALPHA)
000220B    26         B=DF2PH(PSI,QQ,CS,PHIN,PHIK,M,ALPHA)
000222B    27         PSI=PSI-T/B
000224B    28         IF(PSI.LE.PSIMIN) PSI=(PSIMIN+PSIOLD)*0.5
000230B    29         IF(PSI.EQ.0.0) GOTO 22
000230B    30         ERR=1.-PSIOLD/PSI
000233B    31         ERR=ERR*ERR
000233B    32         GOTO 999
                C     PRINTOUT OF ITERATION
000234B    33         WRITE(2,223) NIT,PSI,T
000243B    34    223  FORMAT(' AFTER',I4,'ITERATIONS, PSI=',1PE10.3,' F(PSI)=',E10.3)
000243B    35         WRITE(2,299) B
000247B    36    299  FORMAT(1H+,1PE60.3)
000247B    37    999  CONTINUE
000247B    38         IF(NIT.LT.30.AND.ERR.GT.1.E-6) GOTO 21
000247B    39      22 CONTINUE
                C
                C     DENORMALISATION AND PRINT OUT
000253B    40         DELVG=-PSI*V0
                C     PRINTOUT OF VG VS TIME
000254B    41         VGG=VGP-DELVG
000256B    42         GOTO 9999
000257B    43         WRITE(2,224) VGG
000264B    44    224  FORMAT(25X,'VG=',F8.3,' V')
000264B    45   9999  CONTINUE
000264B    46         RETURN
000266B    47         END


000000B     1         FUNCTION  F2PH(PSI,QQ,SIG,PHIN,PHIK,M,ALPHA)
000000B     2         DIMENSION QQ(100)
                C     EVALUATES CHARGE-BALANCE EQN FOR A (GUESSED) PSI
                C     FOR TWO-LEVEL OXIDE DEVICE
000000B     3         SUMQ=0.0
000001B     4         SUMSQT=0.0
000001B     5         PH2SIN=PHIN+2.*PSI
000004B     6         PH2SIK=PHIK+2.*PSI*ALPHA*ALPHA
000007B     7         DO 30 I=1,M
000011B     8         SUMQ=SUMQ+QQ(I)
000012B     9         SUMSQT=SUMSQT+SQRT(PH2SIN-2.*QQ(I))
000020B    10      30 CONTINUE
000023B    11         F2PH=SUMQ+SUMSQT+SIG*PSI
                     1    +MA(SQRT(PH2SIK)-SQRT(PHIN)-SQRT(PHIK))
000042B    12         RETURN
000045B    13         END


000000B    10         FUNCTION DF2PH(PSI,QQ,SIG,PHIN,PHIK,M,ALPHA)
                C     EVALUATES DIFFTL OF CHARGE-BALANCE EQN W R T PSI
                C     FOR TWO-LEVEL OXIDE DEVICE
000000B     2         DIMENSION QQ(100)
000000B     3         PH2SIN=PHIN+2.*PSI
000003B     4         ALF=ALPHA*ALPHA
```

```
000004B      5          DF2PH=SIG + M*ALP/SQRT(2.*PSI*ALP + PHIN     )
000014B      6          DO 40 I=1,M
000016B      7          DF2PH=DF2PH + 1./SQRT(PH2SIN * 2.*QQ(I))
000016B      8       40 CONTINUE
000030B      9          RETURN
000032B     10          END

000000B      1          FUNCTION QIN(WBYFC,N,QPK,QDC)
                 C      QIN YIELDS A SINE WAVE, PERIOD = 2PI/WBYFC CLOCK PERIODS
                 C      AMPLITUDE = QPK/2
                 C      SUPERIMPOSED ON D.C. LEVEL OF QDC
000000B      2          QIN=QPK*COS(WBYFC*N)
000005B      3          QIN=QIN/2.
000007B      4          QIN=QIN+QDC
000010B      5          QIN=QIN+QPK/2.
000011B      6          RETURN
000014B      7          END

000000B      1          SUBROUTINE CLOCKIT(W,QPK,QDC)
000000B      2          COMMON/BLOCK/N,Q(100),COX,VFB,CS,V0,VG0,DELVG,QOLD(100),CCS
000000B      3          COMMON/TWOPH/V0K,ALPHA,VFBK
000000B      4          DIMENSION VG(1500)
                 C      CLOCKS A SIGNAL CHARGE 'QIN' ALONG CCD
                 C      OUTPUT FROM FLOATING GATE AMP GIVEN BY S/R SOLVIT
                 C      DFT COMPONENTS OF O/P WAVEFORM GIVEN BY S/R FOURIER
                 C      ALLOWS FOR FINITE EPSILON USING FUNCTION EPSILON
                 C      FOR TWO-LEVEL OXIDE DEVICE
000000B      5          FR=6.283185308/W
002735B      6          WRITE(2,220) N,V0,VFB,CCS,COX,VG0,FR
002750B      7      220 FORMAT(1H0,
                       1I4,'GATES  V0=',F6.2,' VFB=',F6.2,
                       2'STRAY CAP=',F6.3,
                       3' OXIDE CAP =',F6.3,
                       4'  INITIAL GATE VOLTS =',F6.3,
                       5'  F/FCLOCK = 1/',F5.1)
002750B      8          WRITE(2,251) V0K,VFBK,ALPHA
002756B      9      251 FORMAT(5X,'THICK V0=',F6.2,'  VFB=',F5.2,'  AREA THIN/AREA',
                       1    ' THICK=',F5.2)
                 C
                 C      INITIALISATION
002756B     10          PI=3.141592654
002756B     11          DO 50 I=1,M
002761B     12       50 Q(I)=0.0
002763B     13          NMAX=M+NINT(10.0/W)
                 C
002767B     14          DO 52 N=1,NMAX
                 C
                 C      CLOCKING
002771B     15          M2=M+2
002772B     16          DO 51 I=2,M
002775B     17          II=M2-I
002776B     18       51 Q(II)=EPSILON(Q(II))*Q(II)
                       1  +(1.-EPSILON(Q(II-1)))*Q(II-1)
                 C
                 C      INPUT
003015B     19          Q(1)=QIN(W,N,QPK,QDC)
003022B     20          IF(Q(1).GE.0.) GOTO 53
003023B     21          WRITE(2,253)
003027B     22      253 FORMAT(1H+,50X,'INPUT CLIPPED')
003027B     23          Q(1) =0.0
003027B     24       53 CONTINUE
                 C
                 C      OUTPUT
003030B     25          CALL SOLVIT
```

```
0003032B   20          VG(N)=VG0-DELVG
                  C
0003033B   27          GOTO 999
                  C    PRINTOUT OF INPUT
0003035B   28          WRITE(2,250) N,Q(1)
0003042B   29      250 FORMAT(1H+,I4,'  QIN=',F8.3,' PC')
0003042B   30      999 CONTINUE
                  C
0003042B   31       52 CONTINUE
                  C    HARMONIC ANALYSIS
0003044B   32          NN=NINT(2.0*PI/W)
0003047B   33          WRITE(2,256)
0003053B   34      256 FORMAT('OUTPUT VOLTAGE')
0003053B   35          CALL FOURIER(NMAX,NN,VG,1,COMPNT)
0003055B   36          CALL FOURIER(NMAX,NN,VG,2,COMPNT)
0003057B   37          CALL FOURIER(NMAX,NN,VG,3,COMPNT)
0003061B   38          WRITE(2,257)
0003064B   39      257 FORMAT(///)
0003064B   40          RETURN
0003066B   41          END


0000000B    1          SUBROUTINE FOURIER(NMAX,NN,SIGNAL,NH,COMPNT)
0000000B    2          DIMENSION SIGNAL(1500)
                  C    'COMPNT' IS 'NH'TH COMPONENT OF DISCRETE FOURIER TRANSFORM OF
                  C    LAST 'NN' POINTS OF ARRAY 'SIGNAL' ENDING WITH 'SIGNAL(NMAX)'
0000000B    3          PI2=6.283185308
0000000B    4          NSTART=NMAX-NN
0000002B    5          NSTART=NSTART+1
0000003B    6          S=0.0
0000004B    7          C=0.0
0000004B    8          DO 60 I=NSTART,NMAX
0000007B    9          II=I
0000007B   10          S=S+SIGNAL(II)*SIN((PI2*I*NH)/NN)
0000022B   11          C=C+SIGNAL(II)*COS((PI2*I*NH)/NN)
0000034B   12       60 CONTINUE
0000037B   13          S=S/NN
0000041B   14          C=C/NN
0000043B   15          COMPNT=S*S+C*C
0000045B   16          IF(COMPNT.LT.1.E-24) COMPNT=1.E-24
0000050B   17          COMPNT=SQRT(COMPNT  )
0000053B   18          DB=20.*ALOG10(COMPNT)
0000056B   19          WRITE(2,260) NH,COMPNT,DB
0000066B   20      260 FORMAT(' AMPLITUDE OF ',I2,'TH HARMONIC =',1PE10.3,
                     1' =',0PF6.1,' DB')
0000066B   21          RETURN
0000070B   22          END


0000000B    1          FUNCTION EPSILON(Q)
0000000B    2          EPSILON=0.0
0000001B    3          RETURN
0000004B    4          END


0000000B    1          SUBROUTINE LOFREQ(QPK,QDC)
0000000B    2          COMMON/BLOCK/M,Q(100),COX,VFB,CS,VO,VGO,DELVG,QOLD(100),CCS
0000000B    3          COMMON/THOPH/VOK,ALPHA,VFBK
                  C    GIVES LOW-FREQUENCY DISTORTION CHARACTERISTICS
                  C    OUTPUT FROM FLOATING GATE AMP GIVEN BY S/R SOLVIT
                  C    FET COMPONENTS EVALUATED EXPLICITLY
                  C    FOR TWO-LEVEL DEVICE
                  C
0000000B    4          WRITE(2,270) M,VO,VFB,CCS,COX,VGO
0000011B    5      270 FORMAT(1H0,
                     1I4,' GATES  VO =',F6.2,'  VFB =',F6.2,
```

```
                     2' STRAY CAP =',F6.3,
                     3' OXIDE CAP =',F6.3,
                     4' INITIAL GATE VOLTS =',F6.3,
                     5' LOW FREQUENCY')
00011B          6          WRITE(2,271) VBK,VFBK,ALPHA
00017B          7      271 FORMAT(5X,'THICK V0 =',F5.2,
                     1'  VFB=',F5.2,
                     2'  AREA THIN/AREA THICK =',F5.2)
                C
00017B          8          DO 71 I=1,M
00021B          9       71 Q(I)=QDC+QPK
00024B         10          CALL SOLVIT
00027B         11          VG1=VG0-DELVG
                C
00030B         12          DO 72 I=1,M
00033B         13       72 Q(I)=QDC+QPK*0.75
00037B         14          CALL SOLVIT
00041B         15          VG2=VG0-DELVG
                C
00042B         16          DO 73 I=1,M
00045B         17       73 Q(I)=QDC+QPK*0.5
00051B         18          CALL SOLVIT
00053B         19          VG3=VG0-DELVG
                C
00054B         20          DO 74 I=1,M
00057B         21       74 Q(I)=QDC+QPK*0.25
00063B         22          CALL SOLVIT
00065B         23          VG4=VG0-DELVG
                C
00066B         24          DO 75 I=1,M
00071B         25       75 Q(I)=QDC
00073B         26          CALL SOLVIT
00075B         27          VG5=VG0-DELVG
                C
                C       EVALUATION OF COMPONENTS
00076B         28          COMPT1=(VG1-VG5)/2.
00100B         29          COMPT2=(VG1-2.*VG3+VG5)/4.
00104B         30          COMPT3=(VG5-2.*VG4+2.*VG2-VG1)/6.
00111B         31          COMPT1=ABS(COMPT1)
00113B         32          COMPT2=ABS(COMPT2)
00115B         33          COMPT3=ABS(COMPT3)
00117B         34          COMPT1=COMPT1/2.
00121B         35          COMPT2=COMPT2/2.
00123B         36          COMPT3=COMPT3/2.
                C
00124B         37          NH=1
00125B         38          DB=20.*ALOG10(COMPT1)
00130B         39          WRITE(2,272) NH,COMPT1,DB
00140B         40          NH=2
00140B         41          DB=20.*ALOG10(COMPT2)
00143B         42          WRITE(2,272) NH,COMPT2,DB
00153B         43          NH=3
00153B         44          DB=20.*ALOG10(COMPT3)
00156B         45          WRITE(2,272) NH,COMPT3,DB
00166B         46      272 FORMAT(' AMPLITUDE OF ',I2,'TH COMPONENT =',1PE10.3,
                     1' =',0PF6.1,' DB')
                C
00166B         47          WRITE(2,273)
00171B         48      273 FORMAT(//)
00171B         49          RETURN
00173B         50          END


00000B          1          FINISH
00000B          2  &END
00000B          3           END
```

HP-25 Program Form

Title To calculate V_g of a single floating gate with a finite C_s Page 1 of 2

Switch to PRGM mode, press [f] [PRGM], then key in the program.

DISPLAY LINE	DISPLAY CODE	KEY ENTRY	X	Y	Z	T	COMMENTS
00							
01	31	↑					
02	24 02	RCL 2					
03	41	-					
04	24 01	RCL 1					
05	61	×					
06	02	2					
07	61	×					
08	24 01	RCL 1					
09	15 02	$\sqrt{x}$					
10	51	+					
11	14 02	x^2					
12	24 05	RCL 5					
13	61	×					
14	24 01	RCL 1					
15	51	+					
16	23 04	STO 4					
17	34	CL x					
18	74	R/S					
19	23 00	STO 0					
20	24 05	RCL 5					
21	31	↑					
22	24 00	RCL 0					
23	61	x					
24	24 03	RCL 3					
25	71	÷					
26	23 06	STO 6					
27	24 05	RCL 5					
28	31	↑					
29	01	1					
30	51	+					
31	61	x					
32	24 01	RCL 1					
33	61	x					
34	02	2					
35	61	x					
36	24 04	RCL 4					
37	15 02	$\sqrt{x}$					
38	21	x⇆y					
39	41	-					
40	14 02	x^2					
41	24 06	RCL 6					
42	51	+					
43	24 04	RCL 4					
44	21	x⇆y					
45	41	-					
46	24 05	RCL 5					
47	15 02	$\sqrt{x}$					
48	71	÷					
49	13 18	GTO 18					

REGISTERS	
R_0	Will contain Q_s
R_1	V_{OTN}
R_2	V_{FBTN}
R_3	C_{OX}
R_4	
R_5	M
R_6	
R_7	

HP-25 Program Form

Title To calculate V_g of a single floating gate with a finite C_s Page 2 of 2

Programmer

STEP	INSTRUCTIONS	INPUT DATA/UNITS	KEYS	OUTPUT DATA/UNITS
1	Key in programme			
2	Store V_{OTN}	volts	STO 1	
3	Store V_{FBTN}	volts	STO 2	
4	Store C_{OX}	pF	STO 3	
5	Store M		STO 5	
6	Input resting potential			
	$V_g(0)$	volts	R/S	
7	Input charge packet size	pC	R/S	V_g volts
8	Repeat step 7 for			
	different charge size			
9	Repeat step 6 - 7 for			
	new value of $V_g(0)$			
10	IF ERROR OCCURS		GTO 19	

APPENDIX 3: Program to Analyse the Effects of Series Resistance in a Simple MOST Inverter

The following program was used to investigate the effects of series resistance in the load-drain and driver-source on the gain of a simple MOST inverter. The routine evaluates the equations 7.3 to 7.6 in Chapter 7, and calculates the input voltage for a specified output voltage. The gain can then be determined graphically.

```
C      PROGRAM TO ANALYSE THE EFFECT OF SERIES RESISTANCE
C      IN THE LOAD DRAIN AND DRIVER SOURCE OF A MOS AMPLIFIER
C      ANALYSIS CALCULATES INPUT VOLTAGE FOR A GIVEN OUTPUT VOLTAGE
C      ALL VARIABLES DOUBLE PRECISION TO ELIMINATE ROUNDING
C      ERROR PROBLEMS IN FUNCTION ZID
C      INPUT CONSTANT PARAMETERS
       CALL SETUP
C      SET UP LOOP TO REPEAT ANALYSIS MANY TIMES WITH DIFFERENT
C      CONSTANT PARAMETERS
       DO 100 II=1,10000
C      ASK IF FINISHED
       WRITE(1,1000)
1000   FORMAT(10H ALL DONE?)
C      IF ANALYSIS COMPLETE, RETURN TO BOS
       IF(IANS(IDUM).EQ.1)CALL EXIT
C      INPUT VARIABLE PARAMETERS
       CALL INPUT
C      PERFORM ANALYSIS
       CALL DOSUMS
100    CONTINUE
C      SHOULD NEVER BE HERE, ABORT JUST IN CASE
       CALL EXIT
       END


C
C**********
C
       FUNCTION IANS(IDUM)
C      FUNCTION TO PULL IN YES/NO ANSWER FROM USER
C      CODE KEEPS TRYING TILL SENSIBLE ANSWER GIVEN
C      YES - IANS=1
C      NO  - IANS=2
C      DUMMY ARGUMENT TO SATISFY COMPILER CUE
       DO 100 I=1,1000
       IANS=LETSOR(1,2,2HYN)
       IF(IANS.NE.3)RETURN
       WRITE(1,1000)
1000   FORMAT(6H ..EH?)
100    CONTINUE
       END
```



```
C
C**********
C
       SUBROUTINE SETUP
       COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
       DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
C      READ CONSTANT PARAMETERS FROM ASR:
C      B1 : GAIN (BETA) OF DRIVER TRANSISTOR
C      B2 : GAIN (BETA) OF LOAD TRANSISTOR
C      VT : THRESHOLD VOLTAGE OF BOTH TRANSISTORS
C      PHIF : FERMI POTENTIAL
C      VDD : SUPPLY VOLTAGE
C      VO : (SUBSTRATE DOPING LEVEL)*(PERMITTIVITY OF SILICON)
C      *(ELECTRONIC CHARGE)/(CAPACITANCE PER UNIT AREA)**2
       WRITE(1,1000)
1000   FORMAT(5H B1 :)
       B1=READ(1)
       WRITE(1,1001)
1001   FORMAT(5H B2 :)
       B2=READ(1)
       WRITE(1,1002)
1002   FORMAT(5H VT :)
       VT=READ(1)
       WRITE(1,1003)
1003   FORMAT(7H PHIF :)
       PHIF=READ(1)
       WRITE(1,1004)
1004   FORMAT(6H VDD :)
       VDD=READ(1)
       WRITE(1,1005)
1005   FORMAT(5H VO :)
       VO=READ(1)
       A=DSQRT(2.0/B2)
       RETURN
       END
```

```
C
C************************
C
      SUBROUTINE INPUT
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
C       R1 : DRIVER SERIES RESISTANCE
C       R2 : LOAD SERIES RESISTANCE
C       VOU : UPPER OUTPUT VOLTAGE
C       VOL : LOWER OUTPUT VOLTAGE
C       SIZE : INCREMENTAL OUTPUT VOLTAGE
C       VX : DRIVER SOURCE BIAS VOLTAGE
C       READ VARIABLE PARAMETERS FROM ASR
      WRITE(1,1000)
 1000 FORMAT(5H R1 :)
      R1=READ(1)
      WRITE(1,1001)
 1001 FORMAT(5H R2 :)
      R2=READ(1)
      WRITE(1,1002)
 1002 FORMAT(6H VOU :)
      VOU=READ(1)
      WRITE(1,1003)
 1003 FORMAT(6H VOL :)
      VOL=READ(1)
      WRITE(1,1004)
 1004 FORMAT(7H SIZE :)
      SIZE=READ(1)
      WRITE(1,1005)
 1005 FORMAT(5H VX :)
      VX=READ(1)
      RETURN
      END
```



```
C
C************************
C
      SUBROUTINE DOSUMS
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
C       PERFORM ANALYSIS FOR A GIVEN SET OF PARAMETERS
C       OUTPUT HEADING FOR OUTPUT DATA
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION VOUT
C       PERFORM ANALYSIS FOR A GIVEN SET OF PARAMETERS
C       OUTPUT HEADING FOR OUTPUT DATA
C       PERFORM ANALYSIS FOR A GIVEN SET OF PARAMETERS
C       OUTPUT HEADING FOR OUTPUT DATA
      WRITE(1,1000)
 1000 FORMAT(4X,4HVOUT,7X,3HVIN,6X,4HDVT1,6X,4HDVT2,7X,2HID,8X,1HB)
C       SET OUTPUT VOLTAGE AT LOWER LIMIT
      VOUT=VOL
C       INCREMENT VOUT
C       SET UP LOOP TO INCREMENT OUTPUT VOLTAGE BY
C       PARAMETER 'SIZE'
      DO 100 I=1,10000
C       IF OUTPUT VOLTAGE GREATER THAN UPPER LIMIT, RETURN
C       PERFORM ANALYSIS FOR GIVEN VOUT
      CALL ONESUM(VOUT)
C       INCREMENT VOUT
      VOUT=VOUT+SIZE
  100 CONTINUE
      RETURN
      END


C
C************************
C
      SUBROUTINE ONESUM(VOUT)
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      COMMON/ANS/DVT2X,BX,ZIDX,DVT1X,VINX
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION VOUT,DVT2X,BX,ZIDX,DVT1X,VINX
C       PERFORM ANALYSIS FOR A GIVEN VOUT
      DVT2X=DVT2(VOUT)
      BX=B(VOUT,DVT2X)
      ZIDX=ZID(BX)
      DVT1X=DVT1(ZIDX)
      VINX=VIN(ZIDX,DVT1X)
C       OUTPUT RESULTS
      CALL OUTPUT(VOUT)
      RETURN
      END
```

```
C
C*************************
C
      SUBROUTINE OUTPUT(VOUT)
      COMMON/ANS/DVT2X,BX,ZIDX,DVTIX,VINX
      DOUBLE PRECISION VOUT,DVT2X,BX,ZIDX,DVTIX,VINX
C      ROUTINE TO OUTPUT RESULTS OF A SINGLE ANALYSIS
      WRITE(1,1000)VOUT,VINX,DVTIX,DVT2X,ZIDX,BX
1000  FORMAT(1H ,6(1PE9.2,1X))
      RETURN
      END


C
C*************************
C
      FUNCTION DVT2(VOUT)
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION DVT2
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION VOUT
C      FUNCTION TO RETURN CANGE IN THRESHOLD OF LOAD
C      TRANSISTOR FOR A GIVEN VOUT
      DVT2=DSQRT(2.0*VO*(VOUT+PHIF))-DSQRT(2.0*VO*PHIF)
      RETURN
      END


C
C**********************
C
      FUNCTION B(VOUT,DVT2X)
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION B
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION VOUT,DVT2X
      B=VDD-VOUT-VT-DVT2X
      RETURN
      END


C
C**********************
C
      FUNCTION ZID(BX)
      DOUBLE PRECISION ZID
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION BX
C      FUNCTION TO RETURN LOAD CURRENT FOR A GIVEN VOUT
      ZID=(0.0-A+DSQRT((A*A)+(4.0*R2*BX)))/(2.0*R2)
      ZID=ZID*ZID
      RETURN
      END
```



```
C
C**********************
C
      FUNCTION DVTI(ZIDX)
      DOUBLE PRECISION DVTI
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION ZIDX
C      FUNCTION TO RETURN CHANGE IN THRESHOLD OF DRIVER TRANSISTOR
C      FOR A GIVEN VOUT
      DVTI=DSQRT(2.0*VO*((ZIDX*R1)+PHIF+VX))-DSQRT(2.0*VO*PHIF)
      RETURN
      END


C
C**********************
C
      FUNCTION VIN(ZIDX,DVTIX)
      DOUBLE PRECISION  VIN
      COMMON/CONSTS/A,B1,B2,VT,PHIF,VDD,VO
      COMMON/VAR/VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION A,B1,B2,VT,PHIF,VDD,VO
      DOUBLE PRECISION VX,R1,R2,VOU,VOL,SIZE
      DOUBLE PRECISION ZIDX,DVTIX
C      FUNCTION TO RETURN VIN FOR A GIVEN LOAD CURRENT AND
C      DRIVER THRESHOLD INCREMENT
      VIN=DSQRT((2.0*ZIDX)/B1)+(ZIDX*R1)+VT+DVTIX+VX
      RETURN
      END


C
$
```

APPENDIX 4: The Standard Two-Phase CCD Processing Schedule

Starting material - Wacker <100>, 2.5-5Ω.cm, N-type.

1) RCA clean:

Boil wafers in a solution of Electronic Grade double distilled water, ammonia solution and hydrogen peroxide in volume ratio 5:1:1, for 10 minutes.

Quench in double distilled water and rinse once.

Place wafers in recirculating water system and leave until effluent resistivity is >10MΩ.cm.

Then boil wafers in a solution of double distilled water, hydrochloric acid and hydrogen in volume ratio 6:1:1, for 10 minutes.

Quench in double distilled water and rinse once.

Place wafers in recirculating water system and leave until effluent resistivity approaches 18MΩ.cm.

Spin dry and continue immediately with next step.

2) Initial oxidation:

Insert wafers into initial oxide furnace set to 1100^{o}C with a gas flow of 1 litre/min of wet oxygen (bubbler at 85^{o}C). Leave for 90 minutes and change gas flow to 1 litre/min of dry oxygen for 5 minutes.

Oxide thickness should be 0.5μm.

Proceed with photomechanical stage.

3) Standard negative photomechanical process:

If not proceeding directly from a high temperature process, bake slice at 80^{o}C for 10 minutes.

Spin 'Isopoly' MR40 negative resist at 5000 r.p.m. for 30 seconds.

3) Pre-bake resist at 80°C for 10 minutes.

Expose resist for 4-6 seconds.

Spray develop in 'Isopoly' developer for 1 minute.

Rinse in 'Isopoly' rinse for 20 seconds and spin dry.

Inspect beneath microscope and reject if defective.

Post-bake resist at 120°C for 15 minutes.

4) Standard silicon dioxide etch procedure:

Etch in buffered HF (7:1) at room temperature until wafer is hydrophobic on the back. Etch rate is approximately 0.1μm/min.

Inspect to ensure that windows are clear.

Remove resist in Microimage 'Resist-stripper' or use concentrated fuming nitric acid.

5) Channel stop diffusion:

RCA clean.

Insert wafers into phosphorous deposition furnace set at 1050°C and previously flushed for 30 minutes with N_2. Gas flow is 1 litre/min N_2, 10cc/min O_2 and 20cc/min of N_2 doped at 0°C with $POCl_3$.

Withdraw wafers and dip etch in buffered HF for ≈5 seconds.

Rinse in double distilled water, and spin dry.

Measure sheet resistivity (should be 5-10Ω/□).

Wash in recirculating water system until effluent ≈18MΩ.cm.

Spin dry.

Insert into phosphorous drive-in furnace set to 1050°C for 10 minutes with a gas flow of 1 litre/min of wet oxygen. Then change gas flow to 1 litre/min of N_2 for 5 minutes.

Proceed with next photomechanical stage.

6) Standard negative photomechanical stage to define source and drain diffusions.

7) Etch and strip resist.

8) Source and drain diffusions:

RCA clean.

Insert into mouth of boron deposition furnace set to 900°C with gas flow of 1 litre/min of N_2.

Flush tube for 20 minutes.

Push slices to centre zone and leave for 30 minutes.

Remove slices and measure sheet resistivity (should be ∿100Ω/□).

Wash in recirculating water system until effluent ≈18MΩ.cm.

Spin dry.

Insert wafers into boron drive-in furnace set to 1100°C, with gas flow of 1 litre/min N_2 for 10 minutes. Then change gas flow to 1 litre/min of wet O_2 for 80 minutes, followed by 5 minutes of N_2 at 1 litre/min.

Remove slices and measure resistivity (should be ≈100-200Ω/□).

9) Remove oxide in buffered HF.

10) Thick gate oxide growth:

RCA clean.

Proceed with standard initial oxide.

Oxide thickness should be 0.5μm.

Proceed with next photomechanical stage.

11) Standard negative photomechanical process to define thin oxide window.

12) Etch and strip resist.

13) Thin gate oxide growth:

RCA clean.

Insert into gate oxide furnace set to 1150°C for 30 minutes with gas flow of 2 litre/min O_2 and 30cc/min HCl. Change gas to N_2 at litre/min and immediately withdraw wafers to mouth of furnace and replace end cap.

Reduce furnace temperature to 1050°C and after 5 minutes reduce N_2 gas flow to 1 litre/min.

When furnace has reached 1050°C, insert wafers and leave for 30 minutes.

Then quickly withdraw wafers to the mouth of the furnace and replace end cap.

Leave to cool for 10 minutes.

Oxide thickness should be 0.12μm.

14) Phosphorous glass stabilization:

After step 13, immediately insert wafers into phosphorous furnace set to 900°C with a gas flow of 500cc/min N_2 and 20cc/min of N_2 doped at 0°C with $POCl_3$.

Leave for 10 minutes, then turn off doped N_2 and withdraw wafers to mouth and replace end cap.

Leave to cool for 10 minutes.

Proceed with the next photomechanical stage.

15) Standard negative photomechanical process to define the contact windows.

16) Contact window etching:

Etch in buffered HF for ≈10 seconds to remove phosphorous glass from windows.

Bake at 120°C for 10 minutes.

Continue etching, inspecting frequently to ensure that undercutting does not occur.

Strip resist.

17) Pre-metallization bake in annealing furnace at 450°C with gas flow of 60:40 H_2/N_2 at 1 litre/min for 10 minutes.

18) Metallization:

Mount wafers in metallization jig to enable an oblique evaporation to be carried out (20° to the plane of the wafer).

Carry out evaporation of 99.999% aluminium from carbon crucible in E-gun for 3 minutes 15 seconds; evaporation pressure $<2.10^{-5}$ torr, beam current is 60mA at 2kV.

Unload jig.

Evaporated film should be 0.5μm thick.

19) Positive photomechanical stage:

Bake wafers at 80°C for 10 minutes.

Spin Shipley AZ350 positive resist at 3000°C for 30 seconds.

Pre-bake resist at 80°C for 5 minutes.

Expose resist for 12-16 seconds.

Immersion-develop resist in Superfine Non-Ionic developer for ≈5 seconds diluted with double distilled water in volume ratio 100:11.

Rinse in double distilled water and spin dry.

Inspect.

Post-bake resist at 120°C for 5 minutes.

20) Aluminium etch:

Immerse in Isoform Aluminium Etchant at 50°C until pattern has been defined.

Inspect at frequent intervals towards end of etching.

Rinse in double distilled water five times.

Strip resist in acetone or Isoclean 'Resist-stripper'.

Rinse in double distilled water once.

Wash in recirculating water system until effluent ≃18MΩ.cm.

Spin dry.

21) Alloying and annealing:

Insert wafers into alloy furnace at 500°C for 10 minutes with gas flow of 1 litre/min of 60:40 H_2/N_2.

Then withdraw wafers and insert into annealing furnace at 420°C with gas flow of 1 litre/min 60:40 H_2/N_2.

After 30 minutes, withdraw wafers and store in luoroware tray in laminar flow cabinet to await testing.

For the test integrators, the two-phase process is combined with the three-phase shadow gap process. Insert the following processing before step 18:

(i) Flat metallization:

Insert in metallization jig to enable a normal evaporation to be carried out.

Proceed with evaporation as in step 17.

(ii) Standard negative photomechanical stage to define first metallization pattern.

(iii) Etch aluminium as in step 20. Caution should be exercised here to ensure that the etched edge is as straight as possible. Agitation of wafers in etch is helpful in obtaining this.

Rinse in double distilled water five times.

Strip resist.

Rinse in double distilled water once.

Wash in recirculating water system until effluent is $\simeq 18 M\Omega.cm$.

Spin dry.

(iv) Pre-metallization bake as step 17.

Proceed with step 18, etc.

APPENDIX 5: Test Apparatus

In this Appendix, the design and performance of apparatus built to drive the CCD structures discussed in this thesis and to evaluate the performance of the integrators are described.

A5.1 Clock Generation

The clock generator used to drive the test integrators, had in fact been constructed in order to drive a variety of CCD structures. The design of the clock amplifiers is however, somewhat novel and although simple, allows high speed operation (up to 10MHz) to be achieved whilst power dissipation is kept reasonably low. Thus it is described briefly here.

The clock generator provides a ϕ_1 clock waveform, data input waveform and reset pulse train, all synchronized to a master clock. The DC offset and amplitude of the ϕ_1 and reset waveforms are independently adjustable internally. The DC level of the data input waveform may also be adjusted internally, but the data amplitude can be adjusted with a front panel control. A fat-zero may also be introduced, the magnitude of which may be adjusted independently of the data amplitude, also with a front panel control. The data is in the form of a binary word which repeats every 35 clock cycles, and which can be set with front panel thumbwheel switches. It is also possible to switch the generator into an 'integrate' mode in which a pre-set number of clock cycles is followed by an integrate period when all waveforms are stopped, with ϕ_1 either on or off.

Clock timing and generation was performed using standard Schottky clamped TTL circuits, however, rather than use traditional amplification techniques such as class A or complementary pair driver circuits, a novel zener diode clamping circuit was employed.

The circuit for the ϕ_1 and reset pulse drivers is shown in figure A5.1a: figure A5.1b is a simplified circuit diagram. Upon the application of a pulse to the input, T_2 switches off and a current impulse (T_3) is driven through the zener diode. The voltage across the diode rises rapidly until the zener breakdown voltage is reached. When the input pulse switches off, T_2 switches on, thus shorting the output node to ground. A simple modification to the circuit to exercise control over the charging and discharging currents at the output node would allow the rise and fall times of the output waveform to be adjusted, however, this facility was not included in the final design. The diode and capacitor at the output form a simple level shifting circuit. The data driver is slightly more complicated, in order that the data and fat-zero level can be continuously adjusted; the circuit is shown in figure A5.2. Amplitude control is exercised through the emitter followers T_4, T_6.

With this type of zener clamped circuit, rise and fall times of approximately 30ns are possible for 20V amplitude output pulses, when loaded with 100pF.

A5.2 Scaling and Summing Amplifiers

In order for the recursive test devices to integrate signals, the device output has to be sample and held, then scaled and summed with the next signal sample.

It was decided not to construct a sample/hold unit since one was already available in the form of a Brookdeal 9415 Linear Gate.* This unit has a frequency response from DC to in excess of 50MHz, and was ideally suited to the purpose in hand. The rest of the feedback circuitry was constructed with CA3140 MOS operational amplifiers.

---

* This unit was designed to operate with the Brookdeal Scan Delay Generator as a boxcar detector for making accurate measurements of small signals. However, its sample/hold facility may be employed by accessing the terminals on the rear panel of the unit.

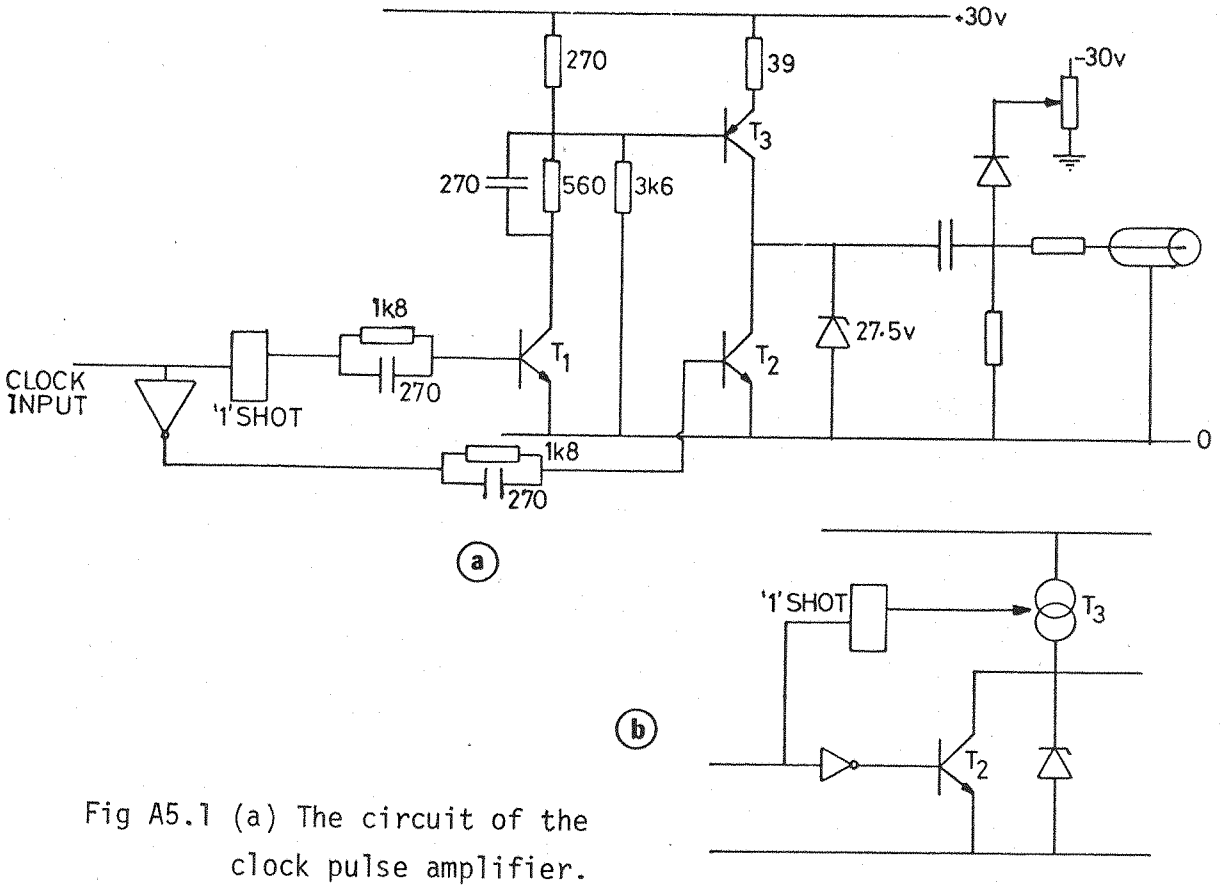


Fig A5.1 (a) The circuit of the clock pulse amplifier. (b) A simplified circuit of the amplifier.

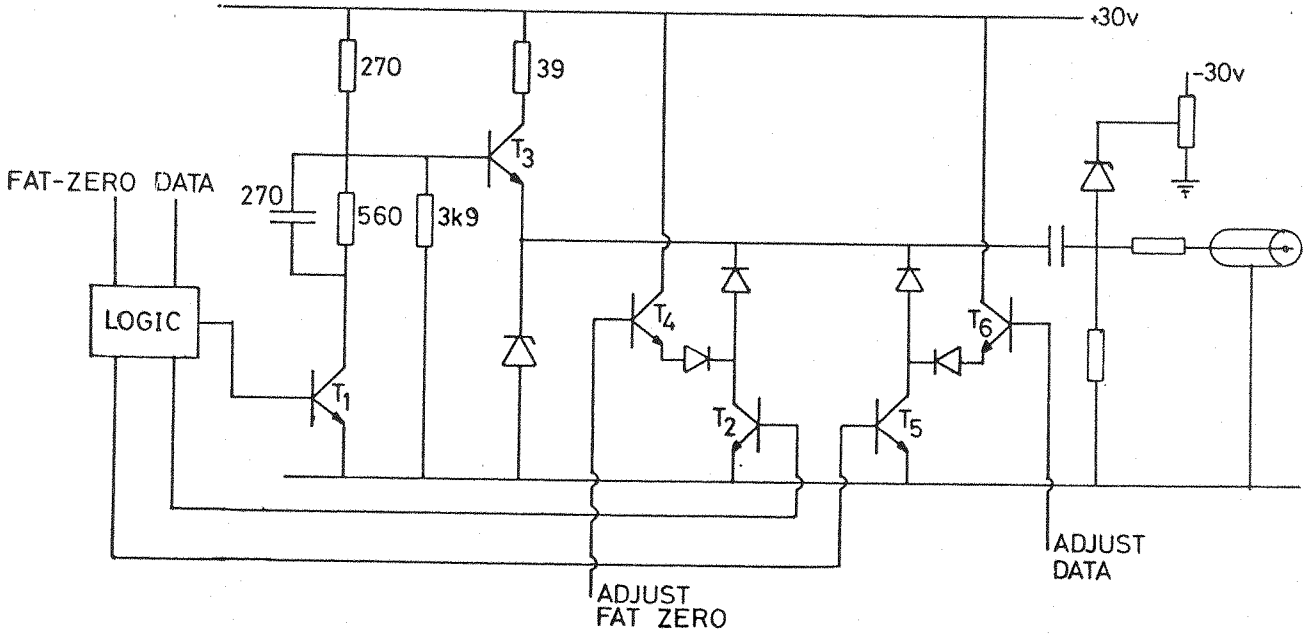


Fig A5.2 The circuit of the data and fat-zero amplifier.

The specification for this circuit was that it should accurately scale the delayed signal before summing it with the unprocessed input waveform. This signal formed the input of the test device. The integrated output was also required to be divided by the effective integration sample size, m; this would enable more rapid visual assessment of the integrated waveforms when compared with the unprocessed signal. The circuit of this system is shown in figure A5.3. It can be seen that a facility is also included that enables noise to be mixed with a signal for test purposes. The gain of the scaling amplifier can be accurately set with a switched attenuator which is calibrated in effective integration sample size; this control is also ganged with the output attenuator which appropriately scales the integrated waveforms. The frequency response of the unit extended from DC to approximately 2.5MHz. For preliminary testing of the recursive test devices, this bandwidth would allow the resolution of a single range bin for data rates up to approximately 1MHz. After an initial warm up period of 30 minutes, the gain drifted by less than 0.4%/hr. Since the output signal is AC coupled to the test device through a level shifting network, the DC drift is unimportant, however, this was less than 0.5mV/hr.

A5.3 Rayleigh Noise Generator

The integration improvement of $\sqrt{m}$ obtainable with a signal integration system depends only on the condition that the noise in successive signal samples is uncorrelated, i.e. it is independent of the amplitude probability distribution of the noise. In a radar system, the presence of a target is usually indicated by the occurrence of a signal above a pre-set threshold level; this is usually set to maximize the probability of detecting genuine targets, whilst minimizing the probability of false alarms caused by large clutter spikes. Clearly, it would be desirable for a signal processor which is used to improve target detection to process the signal in such a way so as to ensure that the threshold level which is subsequently set according to the criterion

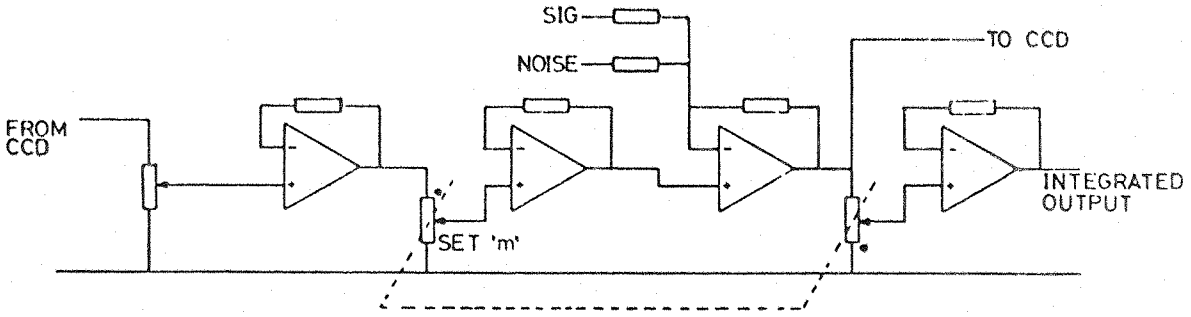


Fig A5.3 The circuit diagram of the scaling and summing amplifier.

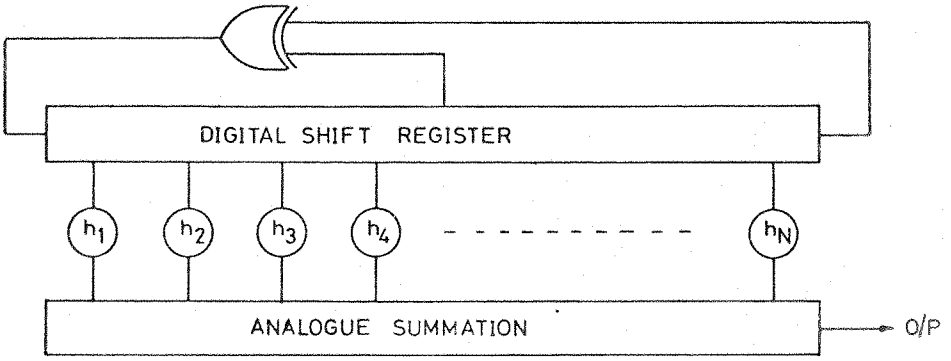


Fig A5.4 Digital filtering of a pseudorandom binary sequence to generate a modified probability distribution.

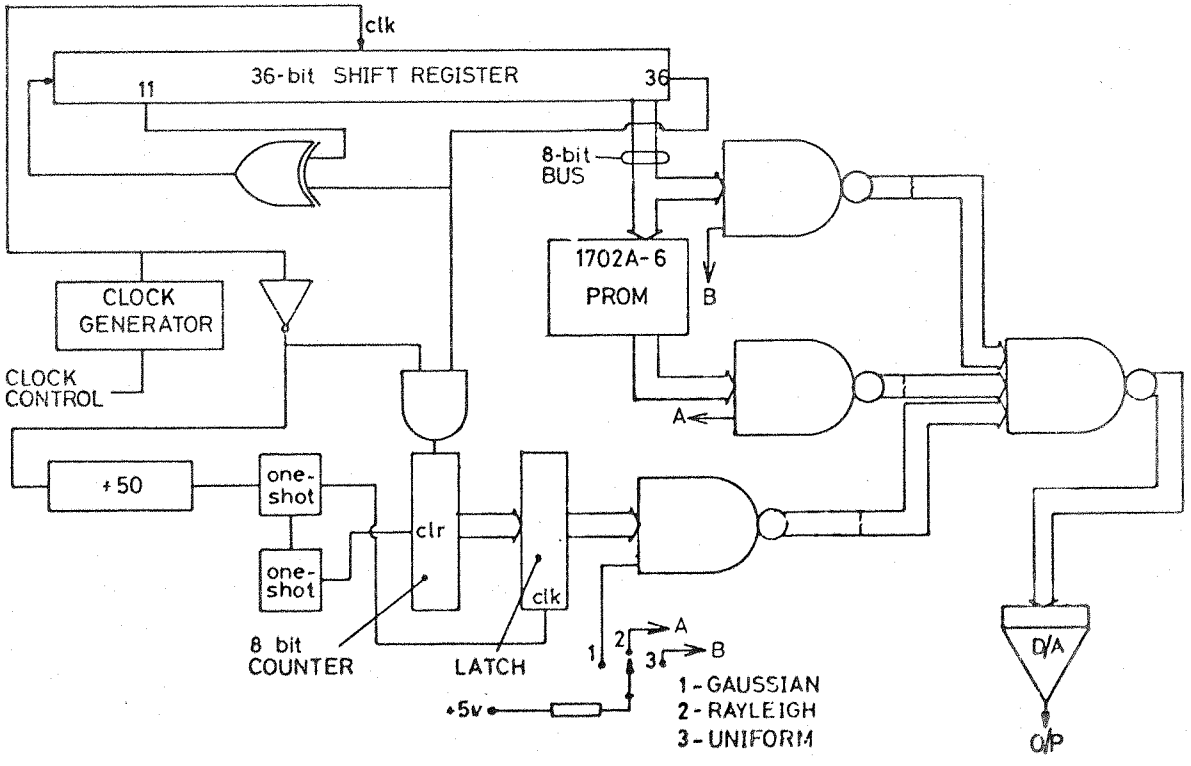


Fig A5.5 The circuit of the noise generator using a ROM look-up table to generate Rayleigh noise.

above, will be the best that is possible. The design of such an 'optimum' processor and the determination of an optimum threshold level can be performed only with prior knowledge of the noise statistics.

It can be shown[91] that for signals of constant amplitude (such as might be obtained from a target during several antenna sweeps) buried in Gaussian noise, the optimum processor is indeed a signal integrator.* However, for signals in Rayleigh noise, the integrator is slightly less than optimum.

Thus in order to experimentally determine the performance of the integrator to Rayleigh distributed noise, a generator was constructed providing noise with a Rayleigh amplitude probability distribution. Several generation techniques were investigated before a suitable method was found.

(a) *Demodulation of Gaussian Noise:* It can be shown[92] that the envelope of narrowband Gaussian noise has a Rayleigh distribution. Thus envelope detecting an appropriately filtered Gaussian process would yield the required noise density. However, this method was rejected for several reasons; e.g. it would be necessary to generate a Gaussian waveform at relatively high frequency (≈100MHz), in order that the resulting Rayleigh noise bandwidth was sufficiently large. However, the main reason was because the system finally chosen was the most flexible of those considered.

(b) *The Use of a Pseudo-Random Binary Sequence (PRBS):* By applying module 2 feedback around an N-bit digital shift register, it is possible to generate a pseudo-random binary sequence with a repeat period of 2^N-1 clock cycles[93] and which has a uniform probability distribution. Other probability distribution may be

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* This is in fact a special case of the matched filter. If the signal varies, then the optimum processor would be one that weights each signal sample according to its magnitude, i.e. a matched filter.

generated from this sequence by employing either digital filtering or applying a density shaping function. As an example, if the circuit of figure A5.4 is used, the output has a Gaussian distribution if all the tap weights, h_1 ..... h_N, are equal. This follows from the Central Limit theorem which states that the sum of many independent random variables (i.e. the 'bit' outputs) has a Gaussian distribution. Unfortunately the techniques for determining the appropriate filter weights to generate a desired probability distribution are not well advanced, and the author did not succeed in realizing a Rayleigh noise filter.

A more attractive approach is to apply a density shaping function. If a probability distribution p(x) is operated on by a monotonic function $y = f(x)$, it can be shown[94] that the resulting probability distribution is

$$p(y) = p\left\{f^{-1}(y)\right\} . \left| dx/dy \right| \qquad \text{A5.1}$$

Thus since the PRBS has a uniform distribution, the density shaping function required to yield a Rayleigh probability density is of the form

$$y = -\sqrt{-\ln x} \qquad \text{A5.2}$$

Two methods of implementing this were considered.

The first was a digital differential analyser (DDA). The DDA can be used to implement fairly complex mathematical functions relatively simply[95] by forming the product of two numbers incrementally in an accumulator. Although this technique works well for simple density shaping functions,[96] it becomes rather costly, slow and inaccurate when several DDAs are required to implement a more complex function such as equation A5.2.

The second method, which was finally chosen, employs a 'look-up table' technique and has several advantages over the techniques discussed so far. With reference to equation A5.2, if the number y is stored in a read only memory (ROM) location which corresponds to the address x, a Rayleigh distributed binary number sequence can be generated by simply interrogating the ROM with the PRBS. The number can then be converted into an analogue sample with a D/A converter.

This system has the significant advantage that noise with any probability density can be generated simply by reprogramming the ROM. For example, if narrow beams (1^{o}) are used in marine radars, the clutter becomes non-Rayleigh.[97] Thus by characterizing the clutter statistics for a given set of radar parameters and appropriately programming the ROM, the performance of a signal processing system, e.g. an integrator, could be easily evaluated in the laboratory.

The circuit of the noise generator is shown in figure A5.5. The PRBS is generated with a 36-bit shift register clocked at 200kHz and has a repeat period of the order of 95 hours; the ROM is a 256 x 8-bit Intel 1702-A UV erasable PROM. In addition to generating Rayleigh distributed noise, Gaussian and uniformly distributed noise is also available. The Gaussian noise is generated by summing the outputs from a single bit of the PRBS register in an up-counter over a period of 50 clock cycles: the output from the counter is then gated in parallel to the D/A converter at the end of the summing period. The uniform noise is generated by gating the last 8-bits of the PRBS register to the D/A converter.

Photographs of the noise waveforms can be seen in figure A5.6. The characteristic asymmetric distribution of the Rayleigh noise waveform can be clearly seen in figure A5.6a. The spectral

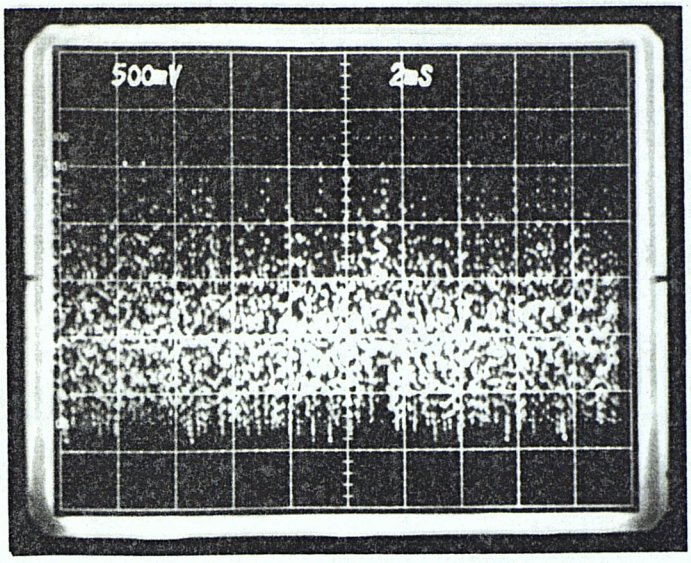

Fig A5.6a An oscillograph of the Rayleigh noise waveform.

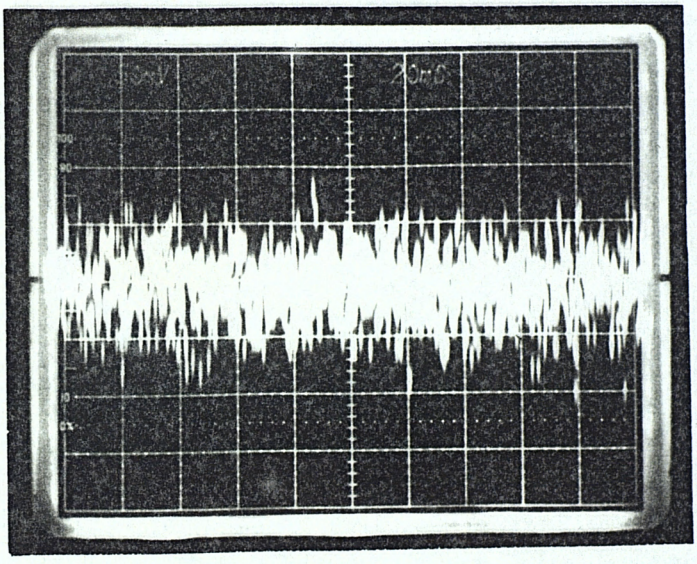

Fig A5.6b An oscillograph of the Gaussian noise waveform.

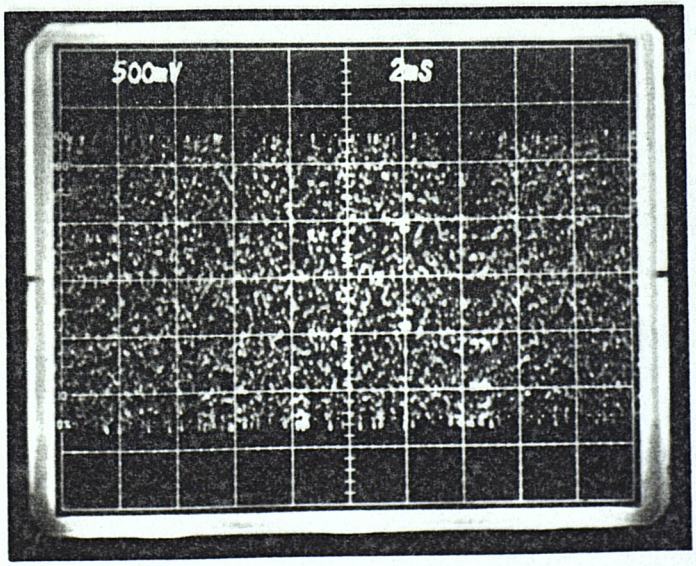

Fig A5.6c An oscillograph of the uniform noise waveform.

response of the three noise sources are shown in figure A5.7, which also shows the spectral response of the unprocessed PRBS (figure A5.7d). The departure of the processed waveforms from the PRBS response is thought to be due to bandlimiting in the D/A converter.

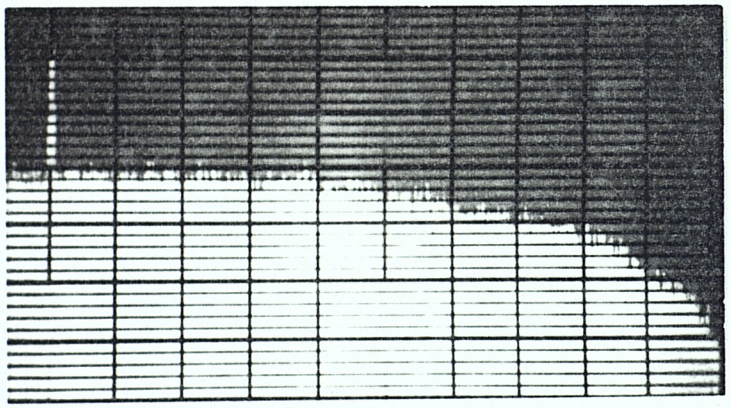

Fig A5.7a The spectral density of the PRBS. 10dB/div. vert., 20kHz/div. horiz.

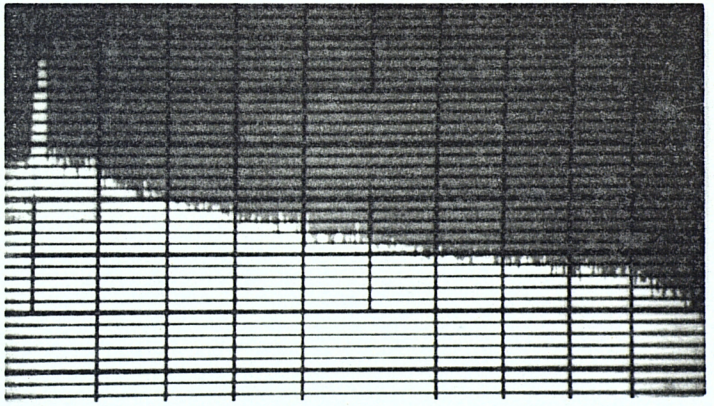

Fig A5.7b The spectral density of the Rayleigh noise source. Scale as in (a).

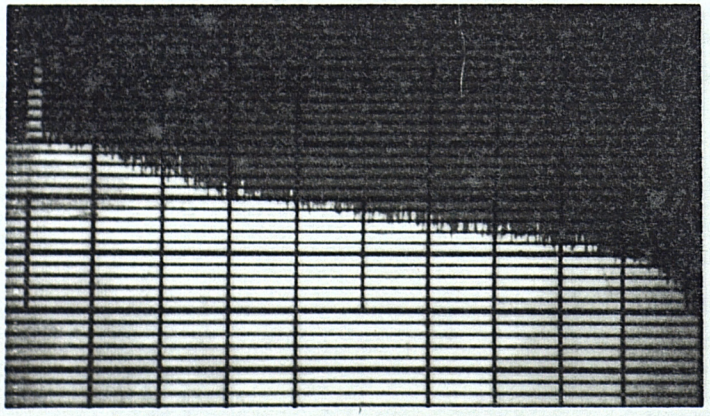

Fig A5.7c The spectral density of the uniform noise source. Scale as in (a).

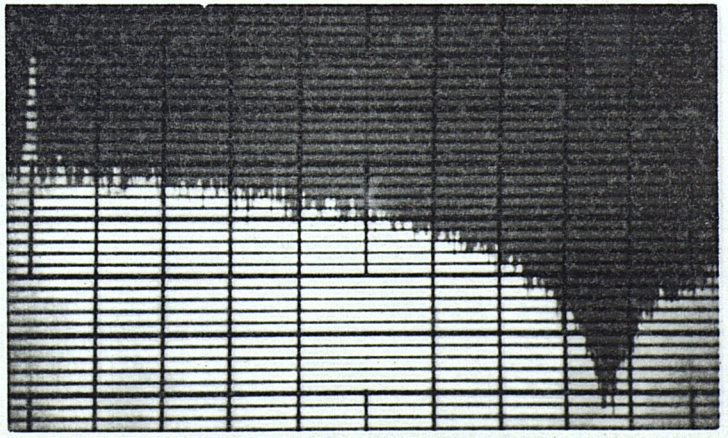

Fig A5.7d The spectral density of the Gaussian noise source. 10dB/div.vert., 10kHz horiz.

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