ADVANCED ELECTRONIC MATERIALS
www.advelectronicmat.de

Single-Contact, Four-Terminal Microelectromechanical Relay for Efficient Digital Logic

*James D. Reynolds, Sunil Rana, Elliott Worsey, Qi Tang, Mukesh K. Kulsreshath, Harold M. H. Chong, and Dinesh Pamunuwa**

Nano and microelectromechanical relays can be used in lieu of transistors to build digital integrated circuits that can operate with zero leakage current at high operating temperatures and radiation levels. Four-terminal (4-T) relays facilitate efficient logic circuits with greatly reduced device counts compared to three-terminal (3-T) relay implementations. Existing 4-T relays, however, require two moving contacts to simultaneously land on two stationary electrodes, which can adversely impact reliability, or have complex out-of-plane fabrication methods that can reduce yield and increase cost while having poor scalability. In this work an in-plane four-terminal relay with a single moving contact is demonstrated for the first time, through successful fabrication and characterization of prototypes with a critical dimension of 1.5 µm. Body biasing is shown to reduce the pull-in voltage of this 4-T relay compared to a 3-T relay with the same architecture and footprint. The potential of the 4-T relay to build efficient logic circuits is demonstrated by fabricating and characterizing a 1-to-2 demultiplexer (DEMUX) circuit using only two devices, a saving of eight devices over a 3-T relay implementation.

1. Introduction

The industrial internet-of-things (IIoT) is an important proving ground for developing many cutting-edge technologies and methods that are essential for realizing the full potential of the IoT. A key requirement of many IIoT applications is to provide data security in elevated temperatures and radiation levels, such as condition monitoring in industrial manufacturing environments, replacing hydraulic controllers with electronic ones in "more-electric" aircraft, and automotive battery passports that monitor provenance, storage, and usage conditions to enable second and third lives of the batteries. Nanoelectromechanical (NEM) relays provide the harsh-environment capability to build solutions for such applications.[1,2] These circuits comprise logic switches[3] and non-volatile memory[4,5] that can potentially be combined to build energy-efficient, reprogrammable field-programmable gate arrays that are harsh-environment capable while eliminating leakage current.[6,7] Heterogeneous 3D integration methods[6,8,9] allow dense multi-layer interconnect stacks, while top–down design methodologies and simulation models[10–13] that leverage existing very large scale integration design tools are an essential part of an efficient design flow.

Two significant challenges in realizing NEM switch-based circuits are achieving the requisite number of hot switching cycles for the given application, and minimizing circuit area, as an individual relay can occupy an area that is several times larger than a transistor. Carbon-based contact coatings offer a pathway to achieve reliability,[14,15] especially nanocrystalline graphite (NCG).[3] Four-terminal (4-T) relays allow efficient circuit architectures to reduce the number of relays for a given logic function, but previously proposed 4-T relays either have two or more contacts[16–18] or an out-of-plane architecture with a complex seven-mask fabrication process.[19] As contact degradation is the biggest cause of failure, reducing the number of contacts is desirable, while out-of-plane architectures generally lead to complex fabrication process flows that can result in low yield, high cost, and poor scalability.

In this paper, we present the first in-plane, single-contact electrostatic 4-T relay to address these issues. We have fabricated prototypes with a 1.5 µm critical dimension with NCG coated contacts, and measured cycling and body biasing[20] where we change the pull-in voltage of the relay by applying a bias voltage to the body terminal. We also demonstrate complex logic functionality, a 1-to-2 demultiplexer (DEMUX), using two interconnected devices. The measured pull-in voltages agree with finite-element simulations. The comparison of our relay with previously reported 4-T relays is given in **Table 1**. The smaller actuation gaps in refs. [16, 17] result in a lower pull-in voltage, but our relay architecture is scalable by reducing the lithographically printed critical dimension. We have carried out a scaling study

J. D. Reynolds, H. M. H. Chong
School of Electronics and Computer Science
University of Southampton
University Road, Southampton, Hampshire SO17 1BJ, UK

S. Rana, E. Worsey, Q. Tang, M. K. Kulsreshath, D. Pamunuwa
Department of Electrical and Electronic Engineering
University of Bristol
Woodland Road, Bristol BS8 1UB, UK
E-mail: dinesh.pamunuwa@bristol.ac.uk

The ORCID identification number(s) for the author(s) of this article can be found under https://doi.org/10.1002/aelm.202200584.

DOI: 10.1002/aelm.202200584

Table 1. Comparison of 4-T relays.

Reference	[16]	[17]	[18]	[19]	This work
Architecture	Out-of-plane four-hinge membrane, two contacts	Out-of-plane dual-ended see-saw relay, two contacts	In-plane six-terminal relay, two contacts	Out-of-plane four-hinge membrane with cantilevered beam, one contact	In-plane cantilevered dual beam, one contact
Footprint	111 μm × 82 μm	76 μm × 53 μm	Not given	620 μm × 620 μm	237 μm × 70 μm
Actuation airgap	200 nm	200 nm	440 nm	1.4 μm	1.5 μm
Contact material	W	W	TiN	Au	NCG
Pull-in voltage	2 V (body bias 8.5 V)	3.16 V (body bias 10 V)	31 V	23–30 V	25 V (body bias −10 V)
Fabrication complexity	Four-mask process	Four-mask process	Three-mask process	Seven-mask process	Two-mask process

to quantify the variation of pull-in voltage with proportionate scaling of the device, to show that a pull-in voltage of ≈3.1 V can be achieved with a critical dimension of 80 nm, easily achievable with e-beam or stepper lithography. By combining a scaled relay with body biasing, sub 1 V switching is achievable.

2. Experimental Section

2.1. 3-T and 4-T Device Architecture

An in-plane device architecture comprising a straight and angled beam section was developed to reduce the effect of the actuation airgap pinching off toward the tip as the beam deflects, and thus the propensity of the beam to collapse on the gate,[3] see **Figure 1**a. The moving beams are anchored via two sections of the beam that are thinner than the main beam, which serve as the hinges where the majority of the deflection occurs. The switch was patterned in the silicon device layer of a silicon-on-insulator (SOI) wafer and suspended by performing an etch of the buried oxide (BOX) layer of the SOI wafer. With this architecture, three-terminal (3-T) relays were developed by structuring the moving beams entirely in silicon, or 4-T relays by connecting the two beams via an insulating plug (shown in red in Figure 1a). The electrical isolation between the two beams resulting from the insulating plug means that the potential difference between the gate and body, V_{GB}, that causes the movement, and the potential difference between the drain and source, V_{DS}, that defines the data signal, are applied via distinct electrodes. Thus, in the 4-T relay, the control and data signals are decoupled, whereas in the 3-T relay, the signals shared a common electrode (the source). This decoupling results in lower, often much lower, device counts for 4-T compared to 3-T implementations of a given logic function. In previous work 3-T relays coated with NCG were demonstrated to improve cycling reliability.[3] Here, for the first time, a 4-T relay with an insulating plug, and a DEMUX circuit were demonstrated to showcase the advantages of a 4-T relay in reducing the device count.

Having one device-level architecture to serve as the basis for 3-T and 4-T relays has the advantage that finite-element modeling and optimization of the hinge and beam geometries, and many of the processing steps, are common to both relays. Assuming negligible flex in the coupler, the electromechanical behavior is identical between the 3-T and 4-T relays. Thus, the

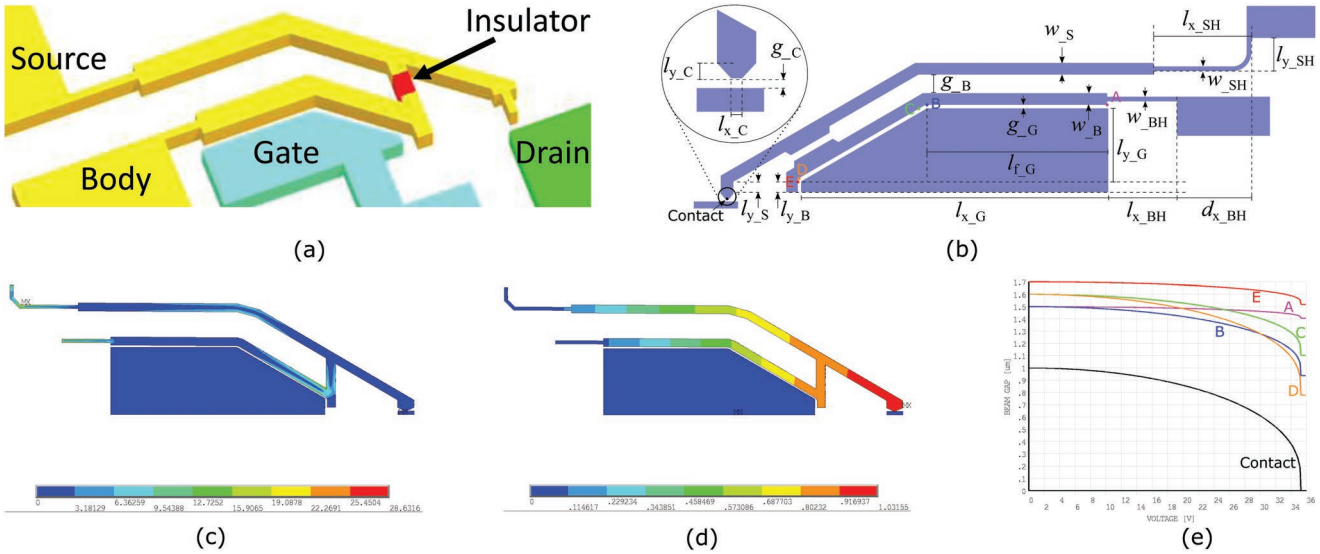

Figure 1. a) In-plane architecture for 3-T and 4-T relays. If the mechanical bridge between the beams is defined by the device silicon, the resulting relay is 3-T, as both beams are electrically connected; instead, if the bridge is implemented using an insulating plug (as shown in red), the resulting relay is 4-T, as the electrical isolation between the beams allows the control and data signals to be decoupled. b) Relay dimensions common to both 3-T and 4-T versions. c) Stress distribution in relay. d) Vertical displacement of relay. e) Displacement of points A, B, C, D, E, and contact highlighted in (b). The plots of (c), (d), and (e) have been extracted from finite-element simulations.

mechanical latency and footprint of this 4-T relay is identical to the corresponding 3-T relay, unlike previous 4-T relays where complex structures or extra gates result in a larger footprint and latency compared to comparable in-plain or out-of-plain 3-T relay implementations (see Table 1). The geometrical parameters of the relay are defined in Figure 1b. The airgaps, beam lengths, and widths are designated as *g*, *l*, and *w*, divided into *x* and *y* components where relevant. The inner beam (body terminal), outer beam (source terminal), gate and hinge are identified with the qualifiers *B*, *S*, *G*, and *H*. Thus, for example, the source and body hinges are identified respectively by the qualifiers *SH* and *BH*. Finally, the displacement between the body and source hinge anchors is defined as d_{x_BH}.

The electrostatic force between the body beam and gate for a given potential difference is determined by the gate (i.e., actuation) airgap g_G and the total length of the airgap is given by the sum of the horizontal and angled sections $l_{f\_G} + (l_{x\_G} - l_{f\_G})/\cos\{\tan^{-1}[l_{y\_G}/(l_{x\_G} - l_{f\_G})]\}$. The pull-in voltage is further affected by the stiffness of the two hinges, as to a first order, the flexing of the beams is negligible in comparison to that of the hinges. The nature of pull-in can be controlled by the relative gaps at the contact (tip to drain) and gate (body to gate). Cantilevered straight beams exhibit snap in when the beam traverses approximately a third of the rest-state airgap;[4,5] thus, by designing the contact gap g_C such that the beam tip lands on the drain contact before the far end of the beam has moved this critical distance, that is, $g_C = 3g_G$, snap-in can potentially be avoided. However, designing the gate gap to be 3× the contact gap might result in large actuation voltages or large beam lengths to keep the pull-in voltage low.

To investigate the electromechanical behavior of this relay architecture, a parametrizable finite-element model (FEM) of the structure was constructed in Ansys. This FEM model allowed all dimensions to be conveniently varied, either independently or with relative dependencies. 3-T and 4-T relays were fabricated and characterized with dimensions as defined in **Table 2**, with the gate gap g_G = 1.5 µm and the contact gap g_C = 1 µm. The distribution of stress across the relay is shown in Figure 1c according to the color map defined at the bottom, showing that most of it occurs in the hinges. Some stress could also be seen in the bottom beam near the coupler, and in the coupler itself, indicating that a robust connection between the beams is required.

The vertical displacements of selected points along the beam, down to the contact, were extracted from a finite-element simulation and are shown in Figure 1e. The slope of the displacement of the end of the beam, point D, starts to increase rapidly at around 1 µm gap distance, indicating onset of snap-in. This prediction conforms with the expected behavior. While the margin of $g_C = \frac{2}{3} g_G$ was not enough to completely eliminate snap-in, it provided a sufficient buffer to ensure the beam end did not collapse on the gate. The angular design also helped in that regard, and point D maintained a closed-state airgap of 0.8µm. Thus, this sizing strategy represented a good compromise; the margin between the contact gap and gate gap reduced the force on the contact and ensured that the beam had less chance of making contact with the gate, with a manageable pull-in voltage of 35 V according to Figure 1e.

Table 2. Nominal geometrical parameters for the relay.

Thickness (SOI wafer device layer thickness)	t	2 µm
Gate airgap	g_G	1.5 µm
Contact airgap	g_C	1 µm
Body-to-source airgap	g_B	8 µm
Body beam width	w_B	5 µm
Body beam hinge width	w_BH	2 µm
Body beam hinge length	l_{x_BH}	30 µm
Source beam width	w_S	5 µm
Source beam hinge width	w_SH	2 µm
Source beam hinge horizontal length	l_{x_SH}	40 µm
Source beam hinge vertical length	l_{y_SH}	14.28 µm
Gate horizontal length	l_{x_G}	131.34 µm
Gate vertical length	l_{y_G}	31.6 µm
Gate flat length	l_{f_G}	77.38 µm
Contact tip horizontal length	l_{x_C}	0.4 µm
Contact tip vertical length	l_{y_C}	2.3 µm
Beam hinge anchor displacement	d_{x_BH}	31.94 µm

It is desirable to achieve low pull-in voltages as the dynamic energy consumed per binary switching transfer is proportional to CV^2, where C is the gate capacitance and V the voltage swing across the gate. In 4-T relays, V could be reduced by biasing the body beam statically to V_B, so that the voltage across the actuation airgap is $V - V_B$. For the beam to pull-in, $V - V_B > V_{pi\_0}$ where V_{pi_0} is the zero-bias pull-in voltage. Thus, to achieve a desired pull-in voltage V_{pi} (which might be lesser or greater than the zero-bias pull-in voltage V_{pi_0}), the body beam should be biased to $V_B = V_{pi} - V_{pi\_0}$. Therefore, any negative bias on the beam results in a reduced voltage swing across the gate, and reduced energy consumption. The latency of the relay is dominated by the mechanical switching delay, around 5 µs for the prototype, extracted from transient finite-element simulations.

By contrast, the electrical *RC* delay is a few tens of ps for the NCG contacts (15–20 kΩ "on" resistance, combined with 4–5 fF parasitic gate capacitance as the load). The mechanical latency reduces as the device is scaled, as the reduction in size increases the natural frequency of oscillation of the structure. A transient simulation of the prototype proportionately scaled (see Section 4) to 80 nm critical dimension shows pull-in occurs at 3.1 V with a mechanical latency of 225 ns.

2.2. Circuit Design Considerations

Digital logic circuits in complementary metal oxide semiconductor (CMOS) technology are constructed by using transistors as switches that are driven to the "on" (linear regime) or "off" (cut-off) state by controlling the gate-to-source voltage. The most common circuit style is to use PMOS and NMOS transistors separately in complementary pull-up and pull-down networks; after switching is complete, for a logic high output,

the pull-up network is on, and the pull-down network off, and vice versa for a logic low output. Thus, the minimum number of devices required for an n-input function is $2n$. The popularity of this "complementary" circuit style, in spite of the high device count, is due to the fact that these circuits do not draw any static energy, and have the highest possible noise resilience compared to other static styles that use transistors as pass gates, or dynamic approaches that store charge on parasitic capacitances.[21]

Three-terminal relays can be used to build circuits using a complementary style with pull-up and pull-down networks, where the same relay populates both networks. This is because electrostatic relays are ambipolar, that is, only the potential difference between the moving beam and control electrode is relevant for pull-in, and the polarities can be interchanged. An example of a circuit, a 2-to-1 multiplexer (MUX) gate, built in this style using 3-T relays is shown in **Figure 2**b (3-T device symbol defined in Figure 2). A 3-T relay-based complementary style circuit implementation has a one-to-one correspondence with a CMOS implementation in the same style. However, along with the high device count this entails ($2n$ devices for an n-input device) and restrictions on the exact formulation of the Boolean equation, devices in series must switch sequentially in order from nearest to furthest from the power rail (if in the pull-up network) or ground rail (if in the pull-down network).[2] For example, if S is high, the output of the inverter (labeled "Inv 1") in the first stage is low. Now, if signal In_0 makes a low-to-high transition, relays R4 and R3 in the pull-down network should turn on, but can only switch in the sequence R4, R3; only after R4 has turned on is the beam in R3 driven to ground, establishing the gate-to-beam potential for R3 that causes its beam to deflect. An analogous situation arises for series devices in the pull-up network, where switching can only occur in the sequence R1 and R2. Thus, the worst-case switching latency is proportional to the maximum number of devices in series vertically, which can result in large logic propagation delays for more complex logic functions. Unfortunately, with 3-T relays, logic circuits can *only* be constructed using a complementary circuit convention. Fundamentally, this is because the control signal (gate-to-source voltage V_{GS}) and data signal (drain-to-source voltage V_{DS}) in 3-T relays share a common electrode, the source.

By contrast, 4-T relays allow the control signal (gate-to-body voltage V_{GB}) to be decoupled from the data signal (drain-to-source voltage V_{DS}). Thus, circuits can be built from 4-T relays using other circuit styles, and allow efficiencies that are not possible with transistors. Although CMOS field-effect transistors have four terminals, in digital logic circuit construction, the body terminal has to be driven to either the lowest potential (NMOS) or the highest potential (PMOS) to avoid parasitic diode structures becoming forward biased[22]. By contrast, 4-T relays have no such restriction. A 2-to-1 MUX circuit built using 4-T relays is shown in Figure 2c. When the select signal S is low, the bottom relay stays off while the top relay turns on, connecting the output Out to signal In_0; when S is high, the top relay is switched off, while the bottom relay turns on, connecting Out to In_1. As can be seen, only two 4-T relays are required compared to twelve 3-T relays, a significant saving. As the mechanical latency τ_m of the 3-T and 4-T relays is identical, the worst-case input to output propagation delay (which is dominated by the mechanical latency) is reduced sixfold from $6\tau_m$ for the 3-T circuit (τ_m for the "Inv 1" stage delay, followed by $2\tau_m$ each for the next two stages due to the presence of two series devices in the pull-up and pull-down networks of each, and τ_m for the "Inv 2" stage delay) to τ_m for the 4-T circuit (as only one device needs to switch). Similar device count and latency savings can be achieved through 4-T relay implementations in most logic functions widely used in digital computers. A DEMUX circuit constructed in complementary style from 3-T relays is shown in Figure 2d, and requires ten devices, with a latency of $4\tau_m$. By contrast, the same circuit can be implemented using only two 4-T relays, with a latency of τ_m as depicted in Figure 2e (this circuit was fabricated and characterized, please see the Section 3 for a discussion).

2.3. Fabrication Process Flow

The 3-T and 4-T relays were patterned on SOI wafers with a 2 µm thick doped device layer (resistivity 0.02 Ω cm) and 1 µm thick BOX layer. First, a 600 nm thick SiO_2 layer was deposited as a hard mask using plasma-enhanced chemical vapor

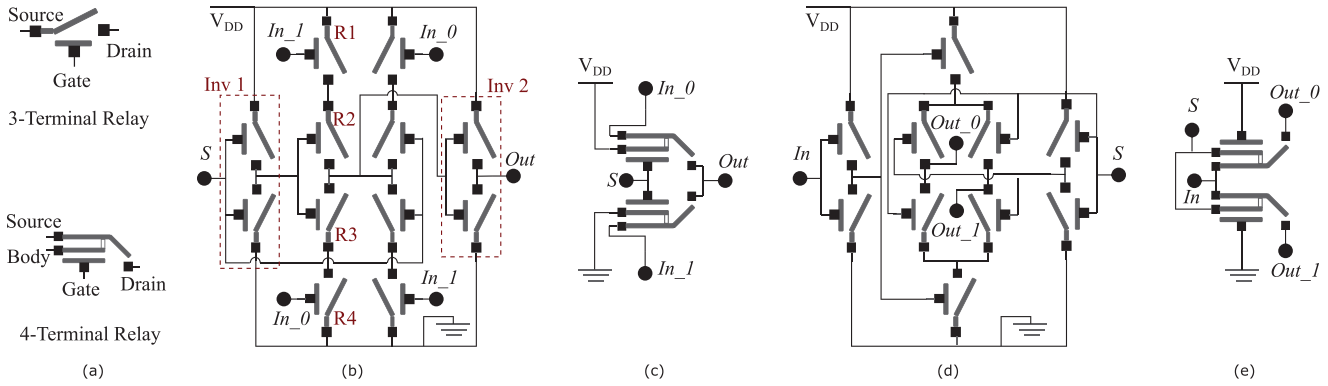

Figure 2. a) 3-T (top) and 4-T (bottom) relay symbols. b,c) A 2-to-1 multiplexer (MUX) gate constructed from 3-T and 4-T relays, respectively. d,e) A 1-2 demultiplexer constructed from 3-T and 4-T relays, respectively.

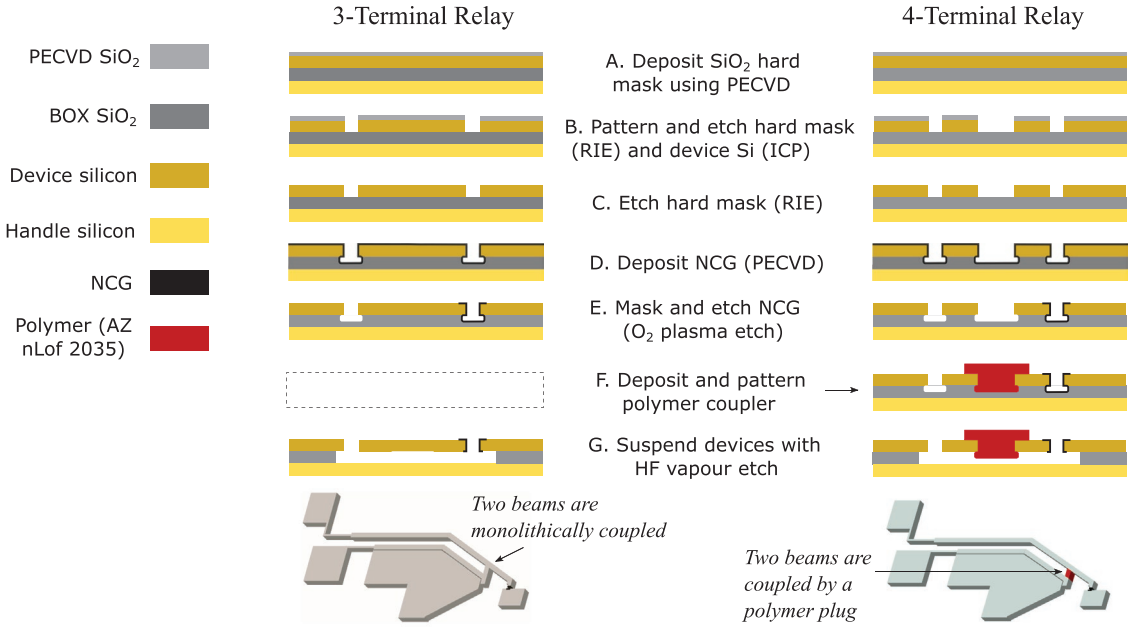

Figure 3. Fabrication process flow for 3-T (left) and 4-T (right).

deposition (PECVD) and patterned using a reactive ion etch (RIE). Next, the device Si is etched using inductively coupled plasma (steps A and B in **Figure 3**). The designs for the two types of relays differed only by the gap between the beams for the 4-T relay shown in Figure 2b, whereas the 3-T relay had a continuous bridge. Next the hard mask was stripped using RIE (step C, Figure 3) and a blanket layer of NCG was deposited using PECVD with CH_4 and H_2 plasma.[3] Optionally, a buffered HF etch was performed before NCG deposition to obtain an undercut of the BOX to help avoid leakage, depending on the thickness of the deposited NCG layer. Afterward, the NCG layer was patterned and etched using O_2 plasma to strip it everywhere except over the beam tip and drain contact regions, in order to avoid shorts. Afterward, the 3-T devices were suspended using an HF vapor etch (step G, Figure 3), while the 4-T devices needed a few more processing steps to implement the insulating coupler. The coupler was implemented using a polymer plug (AZ nLof 2035 photo resist), which was patterned in step F, Figure 3. The photo resist plug was used for ease of processing but it should also be possible to use other materials that do not cause distortion or bending after the release step. Afterward, the devices were suspended in an HF vapor etch step, similar to the 3-T devices. For thin NCG layers, the continuous film in the contact gap broke off in the release step, while thicker films required a directional plasma etch that retained the sidewall coverage. The patterning of 3-T relays was carried out using e-beam lithography (on a Raith Voyager system) to facilitate design space exploration with quick turnaround of design revisions, while the 4-T patterning was carried out using contact photo lithography. An alternative, simpler contact solution was used for 3-T relays that only needed to be switched once to verify the pull-in voltage: steps D and E were omitted, the relays were suspended in step G, and a thin layer of Au (10–20 nm) was thermally evaporated.

3. Experimental Results

3.1. 4-T Relay

A 4-T relay with the dimensions cited in Table 2 and an NCG contact is shown in **Figure 4**a. One concern was how the photo resist plug would react to the final release etch in HF vapor. The micrograph, taken after device suspension, shows the plug survives this step well, while subsequent actuation tests (over several hundred cycles) showed the structural integrity was maintained. This relay had a pull-in voltage of 35 to 36 V with a body bias of zero, (Figure 4b) in agreement with the prediction from a finite-element simulation (see Section 2.2). It was also cycled with body bias voltages ranging from –10 to 10 V, and the variation of pull-in voltage with the bias voltage is shown in Figure 4c. As can be seen, the variation matches up well with the linear relationship $V_{pi} = V_{pi\_0} - V_B$ that we expect in the ideal case, which is plotted as a dashed line.

We have also fabricated and characterized a prototype of the DEMUX circuit of Figure 2e, which is shown in Figure 4d. When the gate of relay R1 is connected to the logic high voltage V_{DD} and the gate of relay R2 is grounded (as depicted in Figure 2e), the logic value on signal *S* determines which relay is on, and which is off; when *S* is low, relay R1 is on, if *S* is high, relay R2 turns on. Thus, *S* = "0" connects *In* to *Out*_0, while *S* = "1" connects *In* to *Out*_1. In order to test this circuit with a limited number of source measure units (SMU), we have taken advantage of the fact that the connection between drain and source is bidirectional with no threshold drop as would occur in CMOS. In our test setup we connected *Out*_0 and *Out*_1 to V_{DD} and grounded both beams, setting *S* to "0". Afterward, while monitoring the current through *In*, the common source, we varied the gate voltages to both relays to test the different logic combinations. The resulting waveforms are shown in Figure 4e. The NCG coated contacts of the relays in this prototype had an "on" resistance of ≈15–20 kΩ. As the focus of this experiment was

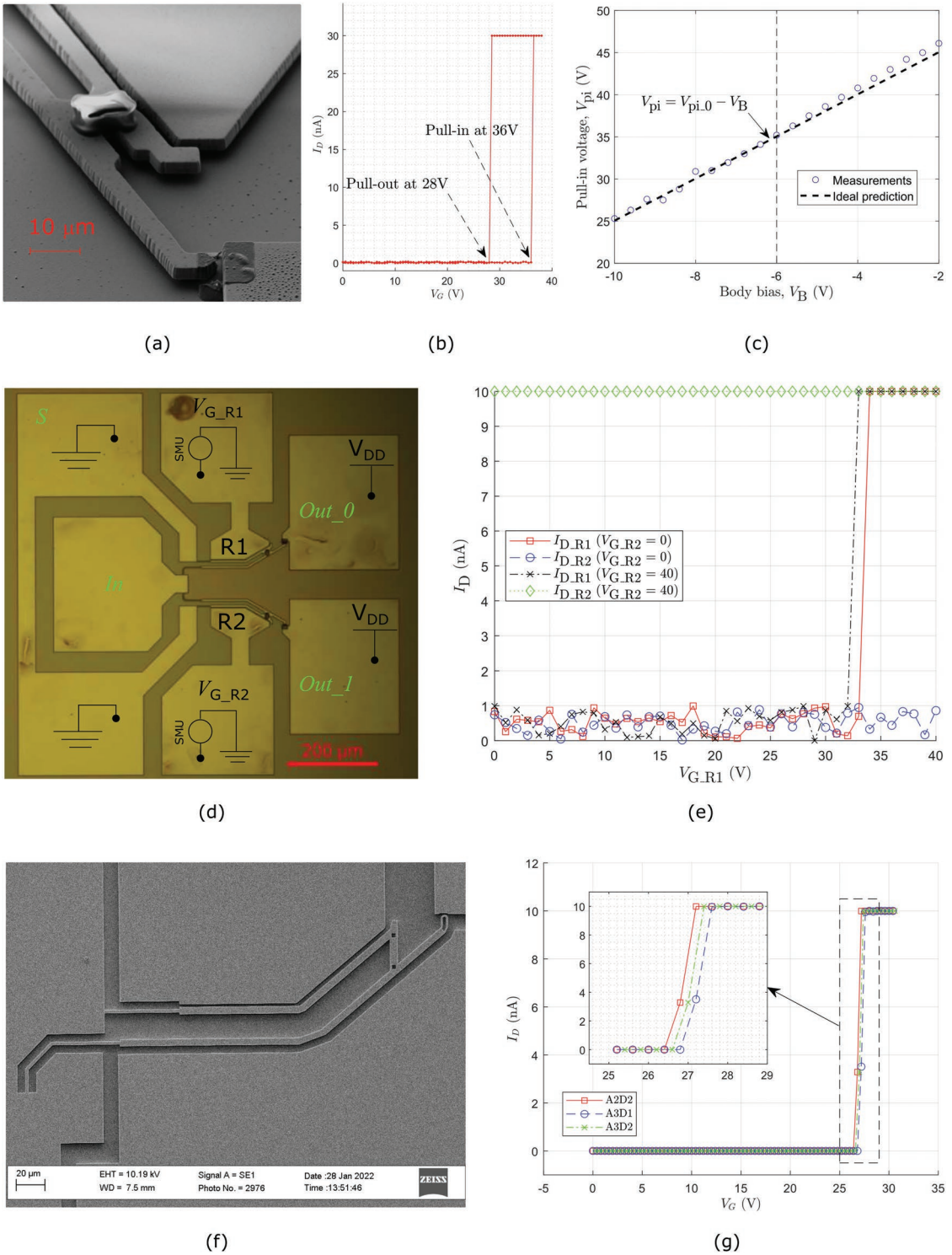

Figure 4. a) 4-T relay prototype with polymer plug and NCG contact. b) Single switch cycle showing hysteresis. c) Variation of pull-in voltage with body (beam) bias extracted from multiple switching events. d) DEMUX circuit prototype constructed from 4-T relays. e) Electrical measurement of DEMUX circuit. f) 3-T relay. g) First switching event of 3-T relay.

on demonstrating DEMUX functionality, and higher currents accelerate degradation, we set a compliance of 10 nA. It should be noted, though, that NCG coated contacts are capable of sustaining much higher currents and many millions of cycles.[3]

Here, four different waveforms are shown, corresponding to the four possible logic combinations {"00," "01," "10," and "11"} for V_{G_R1} and V_{G_R1}. The waveforms depict the currents through the drains of relays R1 and R2 with increasing V_{G_R1},

Table 3. Truth table for DEMUX prototype for $S = 0$.

V_{G_R1}	V_{G_R2}	*Out*_0	*Out*_1
0	0	"Z"	"Z"
0	1	"Z"	*In*
1	0	*In*	"Z"
1	1	*In*	*In*

when V_{G_R2} is set to 0 V (logic "0") and 40 V (logic "1"). For $V_{G\_R2} = 0$ V, I_{D_R2} remains at zero (the current up to ≈1 nA is due to the noise floor in our measurement setup with multiple SMU channels required for circuit characterization, and not indicative of leakage through the plug, which we verified through measurement of individual devices) throughout, while I_{D_R1} shows a step increment to 10 nA (the imposed current compliance level) at 33 V when relay R1 pulls in. For $V_{G\_R2} = 40$ V, I_{D_R2} remains at 10 nA throughout, while I_{D_R1} pulls in at 33 V. The truth table for the DEMUX circuit for the configuration where the select signal S is grounded is shown in **Table 3**. Given the modular style of the circuit construction, the bit width can be increased by combining individual bit slices in parallel, similar to CMOS.

3.2. 3-T Relay

As the 3-T and 4-T relays have a common architecture, design space exploration can be carried out on the 3-T relay that requires fewer process fabrication steps compared to the 4-T relay, which results in a quicker turnaround and also makes it easier to manage yield. Within the constraints of a given critical dimension, which is the smallest feature that can be patterned by the chosen lithography system, it is desirable to minimize both the overall footprint and pull-in voltage. The design parameters or "knobs" to reduce the zero-bias pull-in voltage of our 3-T/4-T relay architecture are hinge stiffness, gate airgap, and body beam length. Of the two hinges, the source hinge is designed to be much softer than the beam hinge, and the body hinge has the main influence on the pull-in voltage. The hinge stiffness is affected by both its length l_{x_BH} and width $w_{\_BH}$ for a given device layer thickness. In order to reduce the zero-bias pull-in voltage without reducing the critical dimension, we fabricated 3-T relay types with a longer body-beam hinge l_{x_BH} (50 µm compared to 30 µm for the 4-T relay), and a longer beam to increase the electrostatic force per applied gate potential, by increasing the gate vertical length l_{y_G} (50 µm compared to 31.6µm for the 4-T relay). All other dimensions that affect pull-in were kept nearly identical (within the constraints of our lithography and processing setup).

Further, we used a thin Au layer which is thermally evaporated as a blanket layer after device suspension to serve as the contact coating rather than NCG, for a quicker turn around. A 3-T relay prototype with a Au contact and the dimensions cited above is shown in Figure 4f. The increased body beam hinge length l_{x_BH} and gate vertical length l_{y_G} mean the footprint of the 4-T relay is less than half (47%) of the 3-T relay (237 µm × 70 µm for the 4-T relay and 296 µm × 120 µm for the 3-T relay). With a contact layer such as Au, which deteriorates rapidly with cycling, the first cycle gives the most accurate measure of the pull-in voltage; in subsequent cycles, to reach the set compliance, some gate overdrive may be required. We measured the pull-in voltage from the first switch cycle of three prototypes with identical dimensions, shown in Figure 4g (labeled with the device identifiers on our test die). The pull-in voltages for these relays are 26.4, 27.6, and 26.8 V (as could be best determined with the applied gate voltage increment step size), ≈27 V on average. The 4-T relay, on the other hand, can be switched at 27 V with a body bias of −8 V (see Figure 4c), which occupies only half the area of the 3-T relay. Further reductions in pull-in voltage are possible, limited only by potential electromechanical integrity concerns such as causing the beam to bend out of plane by putting too high a bias on it. When combined with the major reductions in device count made possible by using 4-T relays (see Section 2.2), the overall savings in area for digital logic implementations can be very high.

4. Discussion and Conclusions

More than Moore type approaches with novel materials[23] and computing schemes[24] have potential to give advantages over CMOS for specific applications. NEM relay-based electronics could hold the key to realizing the low-power and harsh-environment-capable electronics required to serve the edge of the network. As relays will always be larger than transistors, efficient circuits that uses the minimal possible number of devices for a given logic function provide a way of controlling the die area. Alongside area, reducing the actuation voltage reduces the dynamic energy consumed in switching. Within a given technology imposed feature size constraint, 4-T relays facilitate both; 4-T control allow body biasing to reduce the voltage swing required to turn the relays on and off, and allow extremely efficient circuit architectures.

Previously proposed 4-T relay architectures require two moving contacts to simultaneously land on two stationary electrodes[16–18] or have an out-of-plane architecture with a complex seven-mask fabrication process.[19] As the contact is the source of many reliability issues, we have proposed and successfully characterized a 4-T relay that has only one moving contact, with an in-plane architecture for a simple and low cost fabrication process. This 4-T relay shares a common device architecture with a 3-T relay and the fabrication processes between the two differ only by a few extra processing steps needed to implement an electrically isolating mechanical coupler in the 4-T relay. Thus, this device supports modular layout of circuits compatible with a standard cell library approach[6,10] where both types of devices can be used as needed (e.g., 3-T relays for inverters and 4-T relays for more complex logic functions) to facilitate large-scale integration.

We have fabricated 4-T relay prototypes using a lithography and processing platform that has a critical dimension of ≈1 µm, and obtained an almost perfectly linear change of the pull-in voltage with the bias voltage applied to the body terminal, a close match to the ideal, theoretical prediction (see Figure 4c). We have also constructed and characterized a 1-to-2 DEMUX circuit to showcase the efficiency of using 4-T relays, leading to a saving of eight devices over a 3-T relay implementation.

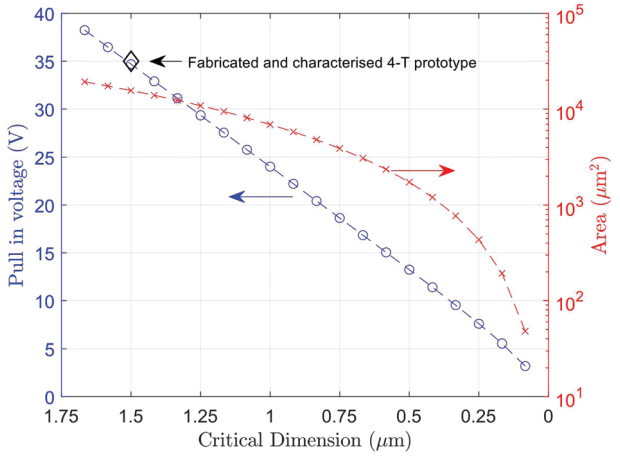

Figure 5. Reduction in (zero-bias) pull-in voltage and footprint achievable through proportionate scaling of 3-T and 4-T relay.

Alongside circuit-level efficiencies, body-biasing also introduces significant opportunities to reduce area under feature size limits. For example, for a 1.5 µm critical dimension, the pull-in voltage can be reduced from 35 to 27 V using body-biasing in a 4-T relay, with a device footprint that is 50% smaller than a 3-T relay for the same pull-in voltage.

To investigate how the pull-in voltage can be reduced by scaling, we have carried out a simulation study using a parametrizable FEM. In this study all dimensions of the relay bar the device layer thickness are scaled by the same factor; we call this type of scaling "proportionate scaling" (**Figure 5**). As can be seen, proportionate scaling results in a near linear variation of the pull-in voltage (see ref. [4] for a discussion of how the surface adhesion at the contact and pull-out varies with scaling) with critical dimension (the actuation gap g and hinge widths w_B and w_S). Thus, for example, an 80 nm critical dimension yields a zero-bias pull-in voltage of 3.1 V. Reducing the critical dimension from 1.5 µm for the fabricated prototype to 80 nm with proportionate scaling also results in a 325-fold reduction in the footprint of the device, from an area equivalent to 125 × 125 µm^2 to 6.9 × 6.9 µm^2. The biggest challenge in miniaturization is obtaining sufficient alignment accuracy to pattern the insulating plug, but it should be possible to reach a critical dimension of a few tens of nm in a state-of-the-art foundry. Hence in conclusion, we have demonstrated a single-contact 4-T relay that can be used to build efficient circuits, is readily scalable, and compatible with body-biasing to achieve low actuation voltages and energy consumption. Thus, this work advances the goal of developing NEM relay-based circuits for use in applications with limited access to wired power sources and harsh environmental conditions, such as in IIoT edge devices.

Acknowledgements

This research received funding from the Royal Academy of Engineering Senior Research Fellowship (RCSRF1920-9-53) awarded to D.P. and the EU H2020 research and innovation programme under grant agreement No. 871740 (ZeroAMP). This work was also supported by the University of Bristol Cleanroom Facility through UK EPSRC grant QuPIC (EP/N015126/1) and the Nanofabrication Centre at the University of Southampton through EPSRC Platform Grant EP/N013247/1.

Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

body biasing, demultiplexers, four-terminal relay, microelectromechanical technology, nanocrystalline graphite, nanoelectromechanical technology, relay-based circuits

Received: May 24, 2022
Revised: July 8, 2022
Published online:

[1] V. Pott, H. Kam, R. Nathanael, J. Jeon, E. Alon, T.-J. K. Liu, *Proc. IEEE* **2010**, *98*, 2076.
[2] S. Rana, Q. Tian, A. Bazigos, D. Grogg, M. Despont, C. L. Ayala, C. Hagleitner, A. M. Ionescu, R. Canegallo, D. Pamunuwa, *IEEE Trans. Circuits Syst., I* **2014**, *61*, 2348.
[3] S. Rana, J. D. Reynolds, T. Y. Ling, M. S. Shamsudin, S. H. Pu, H. M. Chong, D. Pamunuwa, *Carbon* **2018**, *133*, 193.
[4] D. Pamunuwa, E. Worsey, J. D. Reynolds, D. Seward, H. M. H. Chong, S. Rana, *J. Microelectromech. Syst.* **2022**, *31*, 283.
[5] S. Rana, J. Mouro, S. J. Bleiker, J. D. Reynolds, H. M. Chong, F. Niklaus, D. Pamunuwa, *Nat. Commun.* **2020**, *11*, 1181.
[6] T. Qin, S. J. Bleiker, S. Rana, F. Niklaus, D. Pamunuwa, *IEEE Access* **2018**, *6*, 15997.
[7] C. Chen, R. Parsa, N. Patil, S. Chong, K. Akarvardar, J. Provine, D. Lewis, J.f Watt, R. T. Howe, H.-S. Philip Wong, S. Mitra, in *Proc. of the 18th annual ACM/SIGDA international symposium on Field programmable gate arrays (FPGA '10)*, Association for Computing Machinery, New York, NY **2010**, pp. 273–282.
[8] R. Weerasekera, D. Pamunuwa, L.-R. Zheng, H. Tenhunen, *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2009**, *28*, 1237.
[9] A. C. Fischer, M. Grange, N. Roxhed, R. Weerasekera, D. Pamunuwa, G. Stemme, F. Niklaus, *J. Micromech. Microeng.* **2011**, *21*, 085035.
[10] T. Qin, S. Rana, D. Pamunuwa, in *Proc. IEEE/ACM Int. Conf. Computer-Aided Design (ICCAD)*, Association for Computing Machinery, New York, NY **2015**, pp. 641–648.
[11] S. Rana, T. Qin, D. Grogg, M. Despont, Y. Pu, C. Hagleitner, D. Pamunuwa, in *Proc. IEEE Int. Symp. Circuits and Systems (ISCAS)*, IEEE, Piscataway, NJ **2013**, pp. 805–808.
[12] A. Bazigos, C. L. Ayala, M. Fernandez-Bolanos, Y. Pu, D. Grogg, C. Hagleitner, S. Rana, T. T. Qin, D. Pamunuwa, A. M. Ionescu, *IEEE Trans. Electron Devices* **2014**, *61*, 2186.
[13] A. Bazigos, C. L. Ayala, S. Rana, D. Grogg, M. Fernandez-Bolaños, C. Hagleitner, T. Qin, D. Pamunuwa, A. M. Ionescu, *Solid-State Electron.* **2014**, *99*, 93.
[14] D. Grogg, C. L. Ayala, U. Drechsler, A. Sebastian, W. W. Koelmans, S. J. Bleiker, M. Fernandez-Bolanos, C. Hagleitner, M. Despont, U. T. Duerig, in *Proc. IEEE Int. Conf. Microelectromechanical Systems (MEMS)*, IEEE, Piscataway, NJ **2014**, pp. 143–146.
[15] O. Loh, X. Wei, C. Ke, J. Sullivan, H. D. Espinosa, *Small* **2011**, *7*, 79.
[16] R. Nathanael, V. Pott, H. Kam, J. Jeon, T.-J. K. Liu, in *2009 IEEE Int. Electron Devices Meeting (IEDM)*, IEEE, Piscataway, NJ **2009**, pp. 1–4.
[17] J. Jeon, V. Pott, H. Kam, R. Nathanael, E. Alon, T.-J. K. Liu, *IEEE Electron Device Lett.* **2010**, *31*, 371.

[18] D. Lee, W. S. Lee, C. Chen, F. Fallah, J. Provine, S. Chong, J. Watkins, R. T. Howe, H.-S. P. Wong, S. Mitra, *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.* **2013**, *32*, 653.
[19] Y.-H. Yoon, Y. Jin, C.-K. Kim, S. Hong, J.-B. Yoon, *J. Microelectromech. Syst.* **2018**, *27*, 497.
[20] C. Qian, A. Peschot, I.-R. Chen, Y. Chen, N. Xu, T.-J. K. Liu, *IEEE Electron Device Lett.* **2015**, *36*, 862.
[21] J. M. Rabaey, A. P. Chandrakasan, B. Nikolic, *Digital Integrated Circuits*, vol. *2*, Prentice Hall, Hoboken, NJ **2002**.
[22] A body bias may occasionally be applied to tune the threshold voltage,[21] but the body terminal cannot be used to control turn-off and turn-on in the manner of 4-T relays.
[23] J. T. Best, M. A. Masud, M. P. de Boer, G. Piazza, *Adv. Electron. Mater.* **2022**, 2200085, https://doi.org/10.1002/aelm.202200085.
[24] G. Zhou, Z. Wang, B. Sun, F. Zhou, L. Sun, H. Zhao, X. Hu, X. Peng, J. Yan, H. Wang, W. Wang, J. Li, B. Yan, D. Kuang, Y. Wang, L. Wang, S. Duan, *Adv. Electron. Mater.* **2022**, *8*, 2101127.