Research Article | Vol. 12, No. 5 / 1 May 2022 / Optical Materials Express 1991
Optical Materials EXPRESS

Graphene microheater for phase change chalcogenides based integrated photonic components [Invited]

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Abstract: In order to effectively control the state of an active integrated photonic component based on chalcogenide phase change materials, an efficient microheater operating at low voltage is required. Here, we report on the design of a graphene based microheater. The proposed system contains two separate graphene layers between which the phase change material cell of $Ge_2Sb_2Te_5$ is placed. Three distinct switching possibilities are explored, using only the bottom layer, only the top layer or both graphene layers. A detailed investigation of the heater parameters is performed to optimise switching performance. A self-consistent multiphysics simulation of the crystallization process in the phase change material cell is conducted demonstrating the switching capabilities of the proposed design.

1. Introduction

The growing demand on reconfigurability of photonic-electronic integrated circuits [1,2] in neuromorphic computing [3,4], quantum computing [5–8] and microwave photonics [9–11] is drawing a particular attention towards active photonic devices compatible with CMOS circuitry requirements. Different physical mechanisms and materials have emerged as possible switching methods, e.g., liquid crystals [12], graphene [13], p-n junctions [14–16], non-linear materials [17], (EO) polymers [18,19] and electro-optic materials [20]. These methods enabling phase modulation are volatile and rely on a constant voltage being applied to sustain a particular phase shift. Alternatively, utilization of chalcogenide phase change materials (PCMs) [21,22] results in simultaneously non-volatile and large refractive index change between different phases, in both, real (phase modulation) and imaginary part (amplitude modulation) of the index [23,24].

Reversible phase transition in PCM based photonic integrated components have been demonstrated by means of free space optical heating, on-chip optical heating, and electrical threshold switching. Free-space optical heating by focused laser pulses [25,26] is not viable for large-scale integration due to the slow, diffraction-limited, inaccurate alignment process and its intrinsically sequential nature [27]. On-chip optical heating [28–31], achieved by the absorption of the waveguide mode in the PCM cell, allows fully integrated all-optical operations, but has difficulty with switching of large PCM volumes. Both optical heating approaches also suffer from high switching power necessary to achieve all-optical re-crystallization of the amorphous phase [32,33]. Whilst classical electrical threshold switching [34] allows for large-scale integration, the limited

#452153 https://doi.org/10.1364/OME.452153
Journal © 2022 Received 23 Dec 2021; revised 16 Mar 2022; accepted 16 Mar 2022; published 21 Apr 2022

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phase transition volume due to the nonuniform heating and the crystallization filamentation [35] is not always suitable for photonic applications. Recently, electrical switching with external heaters [36–38] has shown promising results in PCM-integrated photonics. However, in these demonstrations, an insertion loss (<1 dB per component) for large-scale integrated components is produced due to the use of indium tin oxide (ITO) heaters [36–38]. In the case of conventional metallic heaters, metal presence in the vicinity of photonic integrated components results in even higher losses of the order of hundreds of dB/mm [39]. In order to overcome these drawbacks, a PCM-integrated silicon rib waveguide has been recently realized in a silicon-on-insulator (SOI) platform using in-situ silicon PIN (p-type, intrinsic, n-type junction) heaters [27] demonstrating near-zero additional loss (~ 0.02 dB/μm). Furthermore, a Sb_2Se_3 based phase shifter using a doped-silicon microheater has been experimentally shown on SOI platform [40]. The SOI platform is fundamental to CMOS photonic circuits. However, in order to enhance the density of integration, backend-of-the-line (BEOL) compatible materials such as Silicon Nitride (SiNx) can be added to provide 3D stacking waveguide capability [41–43]. The integration of new switching mechanism to SiN waveguides such as non volatile electrically switched PCM provide a path to greater scalability whilst retaining CMOS compatibility.

(SiNx) provides an alternative low-cost CMOS compatible platform in which all fundamental non-amplifying photonic components can be implemented. The advantages over Si are fabrication flexibility, low temperature processing (<400°C), low temperature sensitivity [44], refractive index tunability by varying the deposition conditions on the stoichiometry of the films [45] and higher transparency, which all enable the exploitation of SiNx in different ranges of the spectrum for different applications, e.g., quantum information processing [46]. A stoichiometric tuning of the refractive index between 1.8 for N-rich layers and 2.6 for Si-rich layers has been demonstrated within the tuning range of the N/Si ratio [45]. As a result, SiNx waveguides have been widely employed for light propagation in the mid-infrared, the near-infrared and in the visible spectral ranges [47–50]. The versatility of the SiNx platform is key in the implementation of complex multi-layer photonic circuitry. The reduced mode confinement compared to Si, allows for compact active regions of programmable devices reducing the energy required for PCM tuning [51,52]. The fabrication of photonic integrated silicon nitride structures in combination with PCMs has been demonstrated and detailed in [53].

While SiNx cannot be easily doped, design of SiN based nano-heater is nontrivial. As an alternative, the graphene microheaters have been recently proposed to control the temperature of the phase change material on a chip [39,54]. Graphene large in plane thermal conductivity, ultra-low heat capacity [55] and high optical transparency (between 0.5 and 2 μm) [56,57] allows to limit additional losses to 0.07 dB/μm at 1550 nm wavelength for one layer graphene [58] increasing up to 0.015 dB/μm when two graphene layers are considered. Despite the progress in ITO and doped silicon based heaters (which present lower loss when compared to graphene heater), they still suffer from slow switching speed (~10MHz) and high switching energy (~nJ) [49], allowing the graphene heater to reduce the energy consumption for switching and increase the switching speed [54].

In this paper, we study a SiNx-PCM based integrated switching cell. We proposed to utilize two separate single layer graphene as a microheater in order to tune the PCM cell with one more degree of freedom compared to single graphene layer, allowing a finer control of the PCM cell phase, achieving efficient slow and fast crystallization in the same design. Phase change material, $Ge_2Sb_2Te_5$, is sandwiched between the graphene layers allowing three distinct switching schemes, using only the bottom layer, only the top layer or both graphene layers as a microheater. We report on a detailed optimization of the proposed microheater parameters to obtain optimal switching performance. A self-consistent multiphysics simulation of the crystallization process in the phase change material cell is conducted demonstrating the switching capabilities of the proposed design. The rest of the paper is organized as follows. In section 2. the basic principles

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of the microheater design and optimization are discussed. In Section 3. a systematic analysis of the switching performance is reported. Section 4. concludes the paper.

2. Design and optimization

The design of the SiNx-PCM based integrated switching cell is shown in Fig. 1. It is based on a silicon nitride rib waveguide with 300 nm total thickness, 1300 nm width and a slab thickness of 120 nm. The parameters are chosen in order to satisfy the single-mode condition. A 10 nm thin film of SiO_2, a 10 nm layer of $Ge_2Sb_2Te_5$ (GST), capped with a 10 nm Al_2O_3 layer to avoid oxidation are placed above the rib waveguide. The Al_2O_3 was chosen due to its high thermal conductivity leading to a more uniform temperature distribution. The SiO_2 layer below the GST is chosen for its low thermal conductivity to thermally isolate the PCM cell from the SiN waveguide, which acts as a thermal sink. This allows to increase a temperature in the GST cell. The width of the PCM cell is equal to the width of the rib waveguide, while the thickness and length are optimized for best amplitude modulation efficiency of the waveguide. Below and above these 3 layers, CVD single layer graphene is placed acting as an ohmic microheater. In order to transfer the graphene layers, chemical mechanical planarization (CMP) must be carried out in the silicon nitride waveguide as indicated in [59]. The planarization of the waveguide prevents the graphene from rupturing or introducing undesired strain that in turn, modify the electrical conductivity properties of graphene [60]. The proposed design allows to explore three different configurations of microheater biasing. Namely, one graphene layer above the SiNx waveguide, one graphene layer on top of the multilayer structure (SiO_2+GST+Al_2O_3) and both graphene layers can be biased. In the last case, two graphene layers also act as a graphene capacitor which allows to tune the Fermi level to the Pauli blocking region and consequently to reduce the optical loss [13].

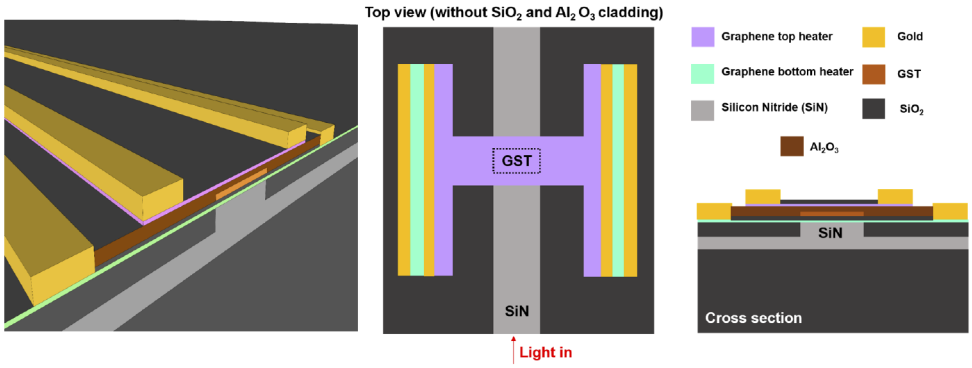

Fig. 1. 3D, top and cross-section view of the proposed graphene microheater placed on top of a rib silicon nitride waveguide with width and thickness of 1300 and 300 nm, respectively. The slab thickness is set to 120 nm. Over the first graphene layer, a 10 nm layer of SiO_2, a layer of GST and another 10 nm layer of Al_2O_3 are placed. It is capped by the second graphene layer and an additional 10 nm layer of SiO_2. Gold contacts are placed on the bottom and top graphene layers on both sides of the waveguide.

Efficiency of the three biasing configurations was studied using coupled electric and thermal co-simulations in CST Microwave Studio [61]. The electric simulations were performed using the stationary current field solver with open boundary conditions. Voltage is applied to the top of the gold contacts (Fig. 1). A contact resistivity of 500 $\Omega\mu$m was used at the gold/graphene interface [62]. Ohmic losses are used to calculate corresponding heat supply via a heat source in the thermal simulation. A heat source with a variable pulse length and an upward and downward flank time of 10 ns has been employed. Open boundary conditions are applied in all spatial

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directions in the heat transfer analysis. A thermal interface conductance of 1.2×10^{8} $Wm^{-2}K^{-1}$ was used for all graphene/substrate and graphene/superstrate interfaces [63]. Transmission efficiency of the waveguide in the presence of the microheater were analysed using transient electromagnetic solver. Finite integration technique with open boundary condition has been employed. Waveguide ports have been used to launch the fundamental waveguide mode and to calculate transmission efficiency. The electrical, thermal and optical properties of the different materials used in the simulations are given in Table 1. The material properties are approximated as temperature independent in the simulations. However, they do depend significantly on temperature in experiments.

Table 1. Physical properties of the different materials used in the simulations. Values marked with * are given for a wavelength of 1550 nm but are wavelength dependent in the simulations.

Property	Graphene [39,64–66]	SiO_2	Si_3N_4	a-GST [67,68]	c-GST [67,68]	Al_2O_3 [69]	Gold
C_p (J kg^{-1} K^{-1})	420	703	673	213	213	880	130
k (W $m^{-1}K^{-1}$)	160	1.38	10	0.17	0.5	25	314
σ (S m^{-1})	$2.98\cdot10^{6}$	$1.1\cdot10^{-14}$	$2\cdot10^{-12}$	-	-	-	$4.56\cdot10^{7}$
n	1.4 + j 0.97 *	1.444	2.01	4.54 + j 0.20 *	6.95 + j 2.06 *	1.75	0.52 + j 10.74
ρ (kg m^{-3})	2267	2203	3000	5870	6270	3100	19320

A presence of the GST cell inevitably compromises optical performance of the waveguide. We systematically analyzed the transmission efficiency of the waveguide as a function of PCM cell thickness and length. The transmission loss spectrum in dB of the waveguide around the operating wavelength of 1550 nm is shown in Fig. 2(a) for PCM cell with thickness of 10 nm and length of 700 nm for a completely amorphous state (blue line) and a completely crystalline (red line) state. The transmisission loss is between 0.65 dB and 1.17 dB (3.86 dB and 5.50 dB) for the amorphous (crystalline) state. At 1550 nm for the completely amorphous PCM cell the total loss due to the graphene layers is 0.45 dB, the loss due to the PCM is 0.26 dB and the loss due to the gold contacts is 0.01 dB. The change of transmission at 1550 nm is 3.93 dB. The change in the transmission loss ($\Delta L = L_c - L_a$) upon full crystallization of the PCM cell for different thickness and lengths are shown in Fig. 2(b) at the wavelength 1550 nm. Here, L_c (L_a) is the transmission loss in dB of the waveguide with the PCM cell being in fully crystalline (amorphous) state. The highest ΔL of around 6 dB can be observed at a thickness of 17 nm and a length of 800 nm. The lowest transmittance modulation can be identified for thickness higher than 30 nm and lengths larger than 700 nm. In this parameter range, the overall transmittance for both phases is low and typically around 0.05-0.2. For PCM integrated photonic waveguides acting as amplitude modulators, both a high absolute transmittance in the amorphous state and large transmittance modulation between states are required. Larger thickness and length lead to overall lower transmittance for both amorphous and crystalline states of the PCM cells. We define the figure of merit as $L_{FOM} = (L_c - L_a)/(L_a)$. The figure of merit as a function of the PCM cell thickness and length is shown in Fig. 2(c). The L_{FOM} demonstrates a behavior similar to the transmittance difference (ΔL) with its maximum value shifted towards smaller thickness and lengths. To maximize the overall transmittance, a small PCM cell thickness and length should be chosen. To maximize the transmittance contrast a small thickness but large length are necessary. For all further simulations, a compromise between these two criteria has been chosen setting a thickness and length of the PCM cell to 10 nm and 700 nm, respectively.

Although utilization of graphene as microheater material allows to considerably reduce associated optical loss, the necessity to wire graphene itself requires to optimize location of further electrical contacts. In the proposed design, graphene layers are biased through four gold contacts (Fig. 1). The main parameters influencing optical and heating performance are

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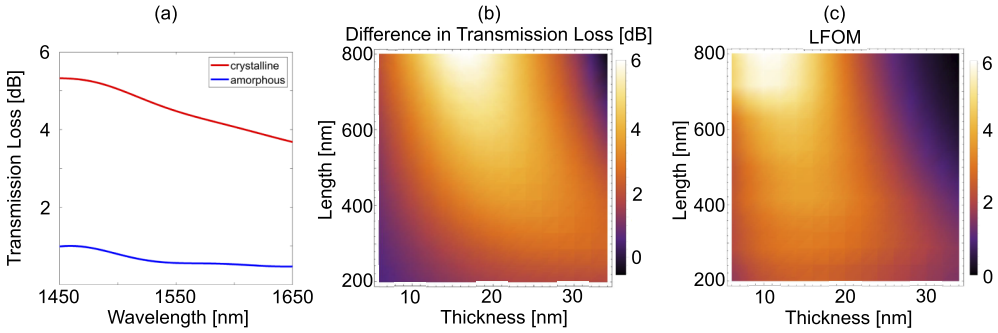

Fig. 2. Transmission loss spectrum of a PCM cell with 10 nm thickness and 700 nm length for a completely amorphous (blue line) and a completely crystalline (red line). Colormaps of the difference in transmission loss (ΔL) (b) and the L_{FOM} (c) as a function of the length (y-axis) and the thickness (x-axis) of the PCM cell. (b) Bright colors represent a large modulation, dark colors represent a small modulation. (c) Bright colors represent a high L_{FOM} while dark colors represent regions with a low L_{FOM}.

the distance between the gold contacts and the rib waveguide and the length and width of the graphene heater "bridge" over the waveguide. To minimize the influence of gold contacts on the waveguide mode, the lateral distance to the waveguide was chosen larger than 1 µm (with 3.3 µm being the distance between top contacts). The length and the width of the graphene bridge were chosen to be 1400 nm and 2000 nm respectively as a compromise between a high maximum temperature and a minimum temperature difference in the PCM cell. In Fig. 3(a) a temperature distribution at the middle of the PCM cell is shown at the end of a 500 ns long voltage pulse. Both graphene layers are biased with peak voltage being 5 V at the top and bottom layer. It can be seen that the maximum temperature is reached at the edges of the PCM cell. Along the waveguide direction, the temperature distribution remains nearly uniform, while across the waveguide the temperature increases sharply at the edges. Decreasing the width of the graphene bridge results in an increase of the maximum temperatures, but also in larger inhomogenity in the cell (Fig. 3(b)). As a consequence, by reducing the bridge width, one can reduce the voltage needed to switch between the states of the PCM cell, at the cost of spatial in-homogeneity in the switched state.

The lateral temperature distribution is not significantly changed when using only the top or bottom graphene heater, only the voltage needed to reach a certain temperature varies. As can be seen in Fig. 4(a) for a maximum temperature around 850 K using the bottom heater requires the highest voltage (7.5 V), using the top heater needs lower voltages (6 V) and the lowest voltages are needed using both heaters (5 V bottom, 5 V top). The choice of heater influences the vertical temperature distribution in the PCM cell (not shown here). The highest gradient can be observed using the top heater where the maximum temperature is near the top side. A smaller gradient can be observed using the bottom heater where the maximum temperature is on the bottom side of the PCM cell. The smallest temperature gradients can be achieved using both heaters by adjusting the voltages on the two heaters accordingly. For the chosen thickness of 10 nm the vertical temperature gradient is not of big importance, but for larger thickness its influence will become more significant.

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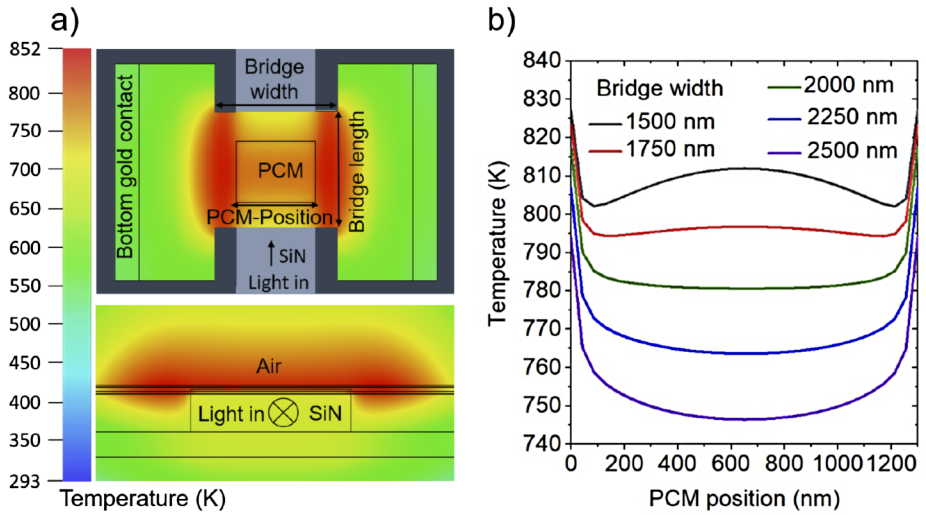

Fig. 3. (a) A colormap of the x-y-plane and cross-ssection temperature distribution in the microheater through the center of the PCM cell. The temperature distribution after 500 ns due to 500 ns long voltages pulse with 5 V applied on the bottom graphene layer and 5 V on the top graphene layer is shown. (b) Temperature distribution after 500 ns along the PCM width for different graphene bridge widths ranging from 2500 nm down to 1500 nm. The same biasing as in (a) has been used.

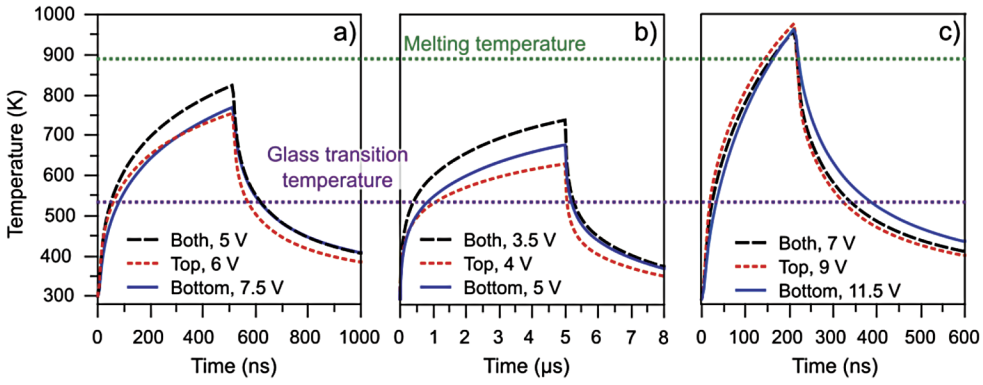

Fig. 4. Temperature evolution in the PCM cell for set (a-b) and reset (c) steps. Fast (a) and slow (b) switching regimes are shown. Biasing with only bottom (blue), top (red) and both bottom and top (black) layers are shown.

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3. Phase transition kinetics

There are several aspects that should be considered when choosing the electric pulse parameters for crystallization (set step). The pulse should be long enough and with enough power to ensure that the PCM is heated above its glass transition temperature (T_g = 534 K), but below the melting point (T_m = 889 K). A maximum of the nucleation rate of GST is near 600 K and a maximum of the growth velocity is near 750 K [70]. To achieve the fastest complete crystallization of the PCM cell, it is best to aim for temperatures near the growth velocity maximum. In this situation, the nucleation rate maximum will be reached at some moment of time during the heating step. On the other hand, higher temperatures require higher voltages, which for on-chip CMOS compatible microheaters are typically limited to 10 V [71,72]. Therefore, depending on the application requirements, a trade-off has to be made between operation voltage and switching time. A fast switching can be achieved by utilizing a higher voltage. If slower switching is acceptable, the voltage can be considerably reduced.

To simulate the crystallization kinetics in the GST cell, a custom phase field code [73] self-consistently coupled to the electric and thermal co-simulations [61] has been employed. The phase field method [74–76] is a phenomenological model that has been successfully applied to describe the phase transition through the time evolution of an order parameter. The non-conserved order parameter, ϕ, is used to describe the local crystallinity of the material, where $\phi = 0$ represents a completely amorphous phase and $\phi = 1$ represents a completely crystalline phase. The time evolution of the order parameter is described by the Allen-Cahn [77] equation:

$$\frac{\partial \phi}{\partial t} = -M_\phi \frac{\delta G}{\delta \phi}, \tag{1}$$

where t is the time, G is the total Gibbs free energy, M_ϕ is the phase field mobility and $\frac{\delta G}{\delta \phi}$ represents the functional derivative of G with respect to ϕ. A detailed description of the method, implementation and parameters can be found in Ref. [73].

For the set step we explore both fast (500 ns) and slow (5 µs) switching regime, corresponding to high and low voltages. Three different biasing combinations are analyzed, with only bottom or top graphene layer and with both bottom and top layers biased simultaneously. In Fig. 4 an evolution of the maximum temperature in the PCM cell is shown for set (a-b) and reset (c) steps. A given required temperature can be achieved at lower voltage, if both graphene layers are biased. To reach the same temperature with biasing only top or bottom layer one needs higher voltages.

For the fast switching, a pulse of 500 ns with a fall/rise time of 10 ns is used. The target temperature is set to be above 750 K. To achieve this, a peak voltage of 7.5 V (6.0 V) at the bottom (top) heater is required, if only one layer is biased. If both graphene layers are biased, the peak voltage can be reduced to 5.0 V at bottom and top layers. The distribution of phases during set step is shown in Fig. 5 for three biasing configurations. After 300 ns, several large crystalline nuclei have been formed for all considered configurations. A cut through the PCM cell shows that most of the crystalline volume reaches through the complete thickness of the cell. After 400 ns the PCM cell with both biased layers is already completely crystallized.

For the slow switching, a pulse of 5.0 µs is employed. In this case, the target temperature can be lower. This allows to reduce peak voltages to and below 5.0 V. A peak voltage of 5.0 V (4.0 V) at bottom (top) layer is required, if only one layer is biased. If both graphene layers are biased, the peak voltage can be reduced to 3.5 V at bottom and top layers. The corresponding distribution of phases during set step is shown in Fig. 6 for three biasing configurations. Smaller nuclei are formed compared to the fast switching simulations. This is due to lower temperatures in the PCM cell which are located closer to the maximum of the nucleation rate and further away from the maximum of the growth rate. The crystallization process is nucleation dominated for the slow switching and growth dominated for the fast switching. After 2.0 µs, the PCM cell is fully crystallized for the bottom/top layer biasing configuration. Due to the lower peak temperatures

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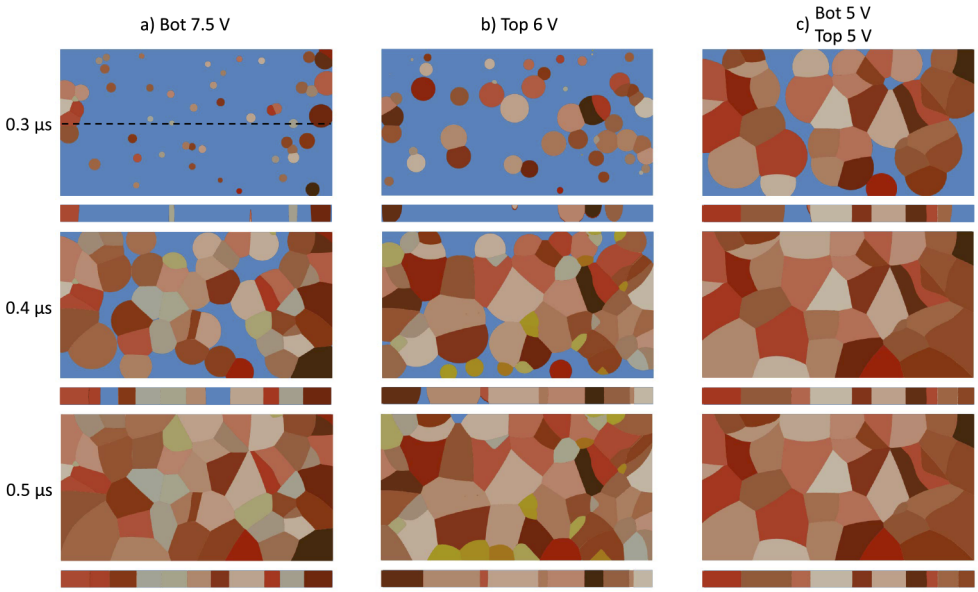

Fig. 5. Crystallization kinetics during the fast set step. Images of the top of the PCM cell and a cut through its center (dashed line in (a)) are shown after 300 ns, 400 ns and 500 ns. Blue colour represents amorphous phase and the other colours are for different grains of crystalline phase. Phase distributions for configurations for biasing only bottom (a), top (b) and both bottom and top (c) graphene layers are shown.

reached with the single layer biasing, the crystallization is delayed for approximately 1-2 µs in this case. Further reduction of the target temperature will allow to reduce operating voltage at the price of further increase of the pulse length.

For the reset step the PCM cell should be heated above GST melting temperature and then quickly cooled down to prevent re-crystallization. This can be achieved with a pulse of 200 ns and the following peak voltages. A peak voltage of 11.5 V (9.0 V) at bottom (top) layer is required, if only one layer is biased. If both graphene layers are biased, the peak voltage can be reduced to 7.0 V at bottom and top layers simultaneously. The minimum temperature in the PCM cell during reset step is shown in Fig. 4(c). A cooling rate of approximately 3 K ns^{-1} is obtained. Such a cooling rate is near the range necessary to ensure amorphization of the GST cell without re-crystallization [78].

In Table 2, the switching efficiencies reported here are compared to other published graphene heater designs. A design in Ref. [54] employs a 20 nm GST layer on a silicon waveguide. A power of 24 mW and a switching energy density of 19.2 aJ/nm^3 are reported. While the power for our fast (16.42 mW) and slow (8.07 mW) crystallization process are lower, the energy per volume is significantly higher for both the fast (0.9 fJ/nm^3) and the slow (4.4 fJ/nm^3) crystallization process. In the same time, results reported in Ref. [54] are obtained using two-dimensional simulations, which also do not take into account the phase transition kinetics. This could lead to a considerable overestimation of the switching efficiency. A design presented in Ref. [39] utilizes a 30 nm thick GSST cell on silicon nitride waveguides. The power consumption in our work is 4 times larger than reported in Ref. [39] in the amorphization process and 3 (1.5) times larger in the fast (slow) crystallization step. However, our design is optimized for much higher operation speed being 40000 (fast set) and 4000 (slow set) times faster. This confirms a general trend: the lower power consumption is achievable in a price of slower switching. It is important to note, that overall switching speed is also dependent on the physical properties of PCM used.

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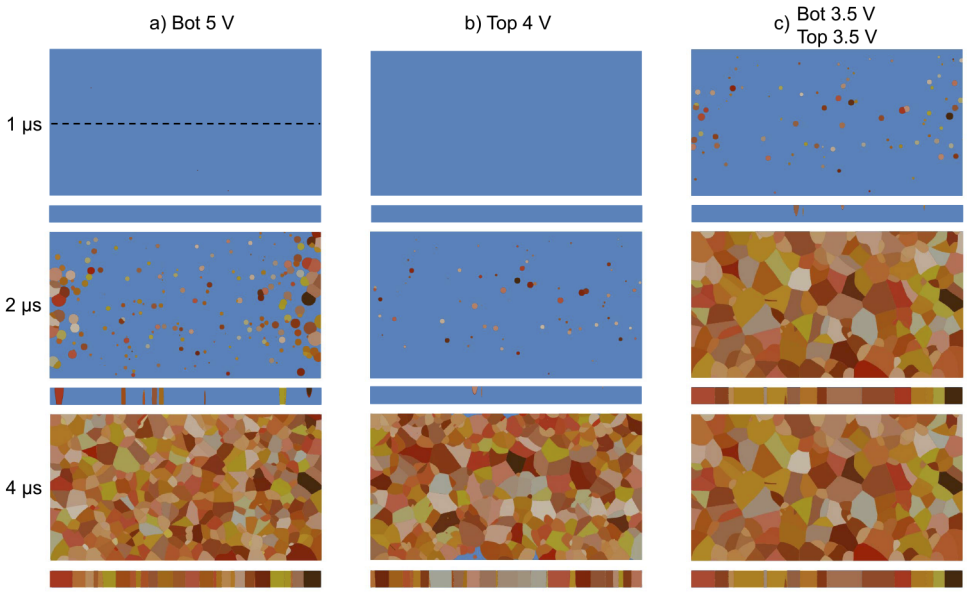

Fig. 6. Crystallization kinetics during the slow set step. Images of the top of the PCM cell and a cut through its center (dashed line in (a)) are shown after 1 µs, 2 µs and 4 µs. Blue colour represents amorphous phase and the other colours are for different grains of crystalline phase. Phase distributions for configurations for biasing only bottom (a), top (b) and both bottom and top (c) graphene layers are shown.

In this respect, designs employing GSST are intrinsically slower, as a switching speed of GSST is slower than one of GST. Application of two separate graphene layers allows to considerable reduce operating voltages. So, in the proposed design we have demonstrated voltages as small as 5.0 V (3.5 V) for fast and slow set step. By carefully choosing target operation temperature and switching time one can further reduce peak voltage. This compares favorably to the both discussed examples from the literature being 20 V (reset) and 6 V (set) in Ref. [54] and Ref. [39], respectively.

Table 2. Comparison of different graphene microheater designs for PCM cell switching.

Waveguide material	PCM	Thickness (nm)	PCM area (μm^2)	N.Pulses	Amorphization	Power (mW)	N.pulses	Crystallization	Power (mW)
Silicon [54]	GST	20	2D simulation	1	0.22 ns	300	1	8 ns	24
Silicon Nitride [39]	GSST	30	2.4	2	13 μs	8.6	3	20 ms	5.5
Silicon Nitride (this work)	GST	10	0.91	1	200 ns	32.28	1	Fast (500 ns) Slow (5 μs)	16.42 (fast) 8.07 (slow)

4. Conclusions

We proposed an optimized design of the graphene based microheater for non-volatile programmable photonic integrated circuits based on chalcogenide phase change materials. By employing two graphene layers biased simultaneously, we manage to reduce required peak switching voltage well below 10 V. For the best performing parameters we numerically achieve powers as low as 2.33 mW for fast (500 ns) and 1.37 mW for slow (5 μs) switching for set and

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3.71 mW for reset steps, which favorably compares with previously reported data as can be seen in Table 2. To numerically characterize our PCM cell we performed self-consistent multiphysics simulations of the crystallization process demonstrating the superior switching capabilities of the proposed design. This opens a way towards non-volatile integrated programmable 3D stacking waveguide capability, which can be exploited in different ranges of the spectrum, ranging from visible to mid infrared.

Funding. Agencia Estatal de Investigación (FJC2020-042823-I); Engineering and Physical Sciences Research Council (EP/T007303/1); Horizon 2020 Framework Programme (871391); Deutsche Forschungsgemeinschaft (CH 407/13-1).

Disclosures. The authors declare no conflicts of interest.

Data Availability. Data relating to this manuscript can be obtained from the authors.

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