UNIVERSITY OF SOUTHAMPTON

# Tunable spin and charge transport using CMOS-compatible silicon quantum dots for quantum information applications

by

Joseph William Hillier

A thesis submitted in partial fulfilment for the degree of Doctor of Philosophy

in the

Faculty of Engineering and Physical Sciences

School of Electronics and Computer Science

April 2022

UNIVERSITY OF SOUTHAMPTON

ABSTRACT

FACULTY OF ENGINEERING, SCIENCE AND MATHEMATICS
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

by Joseph William Hillier

Scaling in commercially available silicon (Si) complementary-metal-oxide-semiconductor (CMOS) devices has inevitably led to single carrier behaviour exhibited at low temperatures owing to the strong orbital quantization of disorder based quantum dots (QDs). As a consequence, p-type Si metal-oxide-semiconductor-field-effect-transistors (MOSFETs) fabricated and supplied by Hitachi provide an excellent platform to evaluate and explore a plethora of rich phenomena that arise from the interplay of single hole transport and spin interactions. Through the use of the well terminal acting as a pseudo-gate in a MOSFET, I discover the formation of a double-QD system exhibiting Pauli spin-blockade and investigate the magnetic field dependence of the leakage current. This enables attributes that are key to hole spin state control to be determined, where I calculate a tunnel coupling $t_c$ of 57 $\mu$eV and a short spin-orbit length $l_{SO}$ of 250 nm. The outcome of a strong spin-orbit interaction at the interface when using disorder based QDs demonstrates support for electric-field mediated control.

In addition, I experimentally investigate the impact of electrical stress on the tunability of single hole transport properties in a MOSFET device. This is achieved by monitoring Coulomb-blockade from three disorder based QDs at the channel-oxide interface, which are known to lack tunability as a result of their stochastic origin. My findings indicate that when applying gate biases between -4 V to -4.6 V, nearby charge trapping enhances Coulomb-blockade leading to a stronger QD confinement that can be reversed to the initial device condition after performing a thermal cycle reset. Re-applying stress then gives rise to a predictable response from reproducible changes in the QD charging characteristics with consistent charging energy increases of up to $\approx 50\%$ being observed. A threshold is reached above gate biases of -4.6 V, where the performance and stability become reduced due to device degradation occurring as a product of large-scale trap generation. These results not only suggest stress as an effective technique to enhance and reset charging properties, but also offer insight on how industry compatible Si devices can be harnessed for single charge transport applications by investigating interactions which are useful for quantum information processing.

# Contents

# List of Figures

## University of Southampton Thesis Licence

## Declaration of Authorship

I, Joseph W. Hillier, declare that this thesis and the work presented in it is my own and has been generated by me as the result of my own original research.

I confirm that:

1. This work was done wholly or mainly while in candidature for a research degree at this University;
2. Where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
3. Where I have consulted the published work of others, this is always clearly attributed;
4. Where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
5. I have acknowledged all main sources of help;
6. Where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
7. Parts of this work have been published as:

**J. Hillier**, K. Ono, K. Ibukuro, F. Liu , Z. Li , M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi and S. Saito. Probing hole spin transport of disorder quantum dots via Pauli spin-blockade in standard silicon transistors. *Nanotechnology*, 32, 260001, 2021.

**J. Hillier**, K. Ibukuro, F. Liu, M. K. Husain, J. Byers, I. Tomita, H. N. Rutt, Y. Tsuchiya, and S. Saito. Investigating stability and tunability of quantum dot transport in silicon MOSFETs via the application of electrical stress. *J. Phys. D: Appl. Phys.* 55, 105107, 2022.

**J. Hillier**, K. Ono, K. Ibukuro, F. Liu , Z. Li , M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi and S. Saito. Single spin sensing in silicon p-type Metal-Oxide-Semiconductor Field-Effect Transistors. *International conference for the quantum science and technology community*, 3193, 2020.

**J. Hillier**, K. Ono, K. Ibukuro, F. Liu , Z. Li , M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi and S. Saito. Atomically flat trapezoidal silicon nanowires for tunable gate defined quantum dots. *Silicon Quantum Information Processing Workshop*, 2021.

Signature: Date:

# Acknowledgements

Firstly, I wish to give my sincere thanks and admiration to my supervisors Prof. Shinichi Saito and Dr. Yoshishige Tsuchiya who gave me the opportunity to pursue this project at The University of Southampton. Their leadership, guidance and global contacts enabled me to develop the necessary tools to thrive in a research environment, including an unforgettable 3-month collaboration at The Riken Institute under Dr. Keiji Ono in Tokyo, Japan, who it was an honour to work under.

I would also like to thank the other members of my research group for their continued support, post-doctoral researcher Dr. Muhammad Khaled Husain and fellow PhD students Dr. Li Zuo, Dr. Fayong Liu, and Dr. Kouta Ibukuro - who I worked closely with. All of whom shared their extensive knowledge and experience throughout my four years. In addition, I'd like to recognise Dr. Kapil Debnath, Dr Moise Sotto, Dr. Daniel Burt and Dr James Byers who provided valuable feedback during the initial stages of my project.

Finally, I feel that the successful completion of my PhD would have not been possible without the immense support of my parents, William and Jayne, and of course my wife Jessica.

# Chapter 1

# Introduction

Silicon (Si) based devices have become the cornerstone of modern technology, and are now a leading candidate for quantum information processing architectures [1, 2, 3, 4]. Promising alternatives to traditional metal-oxide-semiconductor field-effect transistors (MOSFETs) take the form of quantum dots (QDs) acting as quantum bits (qubits) in single electron devices through the use of charge and spin as the fundamental building blocks [5, 6, 7]. The use of multi-gate device architectures in particular has led to many breakthroughs by tuning the potential profiles defining QDs as well as the inter-dot tunneling barriers for precise control, where development is undertaken by academia and large pre-industrial fabrication facilities [8, 9, 10, 11, 12, 13, 14].

Various methods to observe and control spin phenomena have been also proposed [15, 16, 17]. Spin based quantum information devices through multi-gate QD systems in particular have led to many breakthroughs by tuning the potential profiles defining the QD as well as the inter-dot tunneling barriers for precise control [18, 19, 20]. However, although employing many gates certainly adds flexibility, it is a fabrication intensive process. One alternative is to use devices which are Si VLSI (very-large-scale integration) compatible. Efforts have been made to take advantage of features already present at the single electron level in Si VLSI technology. The use of trap states within Si quantum devices can complement and even enhance single charge transport, with applications ranging from quantum information and quantum metrology, to bio-sensing and hardware security [21, 22, 23, 24].

One technological obstacle to overcome is that of electric-field mediated control for spin-based quantum information processing schemes, which relies on a strong spin-orbit (SO) interaction. This has led to investigations of spin transport schemes with an enhanced SO interaction through the use of holes, valley states and inversion layer asymmetry at the oxide interface [25, 26, 27, 28, 29]. Pauli spin-blockade (PSB), a double-QD phenomenon and common measurement tool used in spin transport systems, can also be

harnessed to study the SO interaction strength given that a device can be tuned into a PSB configuration.

Ultimately, technological impact as a result of such endeavours can only become a reality if the physical components can be manufactured on a large-scale, which are reproducible and have guaranteed stability. Although, if the origin and behaviour of defect based QDs were better understood, this would show a path towards controlling single charging characteristics through manipulating the disorder, with the possibility of tuning MOSFET QDs. This would satisfy the need for an efficient and scalable device capable of single carrier manipulation using a VLSI platform. The most significant challenge in this regard is that of device variability owing to random and uncontrollable charges in the vicinity of the QD, which are the leading causes of unpredictable behaviour. This has meant exploring methods to improve the consistency and tunability of features that are essential to single carrier transistor function, such as charging energy ($E_c$), capacitive couplings and activation energy ($E_a$) [30]. One method is through the application of electrical stress in the form of a large gate bias. Applying this technique draws parallels from the significant effort put forward historically into oxide reliability when downscaling transistors in search of better performance, together with the development of resistive memory, where state switching is initiated as a consequence of voltage driven structural change within the oxide [31, 32].

The aim of this project is to investigate Si devices which can be fabricated by industry compatible processes for use in quantum information applications. This includes taking advantage standard Si transistors which were provided by industrial sponsor Hitachi, through tuning disorder based QDs present in Si MOSFETs, as well as the fabrication of Si nanowires to produce gate-defined QDs. The first goal is to demonstrate PSB, which would enable the benchmarking of disorder QDs for electric-field mediated control and high frequency spin manipulation, and therefore supply information on the SO interaction of disorder state spin. Moreover, in search of an alternative method to investigate the tunability of disorder QDs, the second goal is to explore the application gate electrical stress as a way mitigate the inflexibility of controlling a QD system with a single gate through inducing controlled charge trapping. Implementing such a technique, which can produce beneficial changes to single carrier transport characteristics by altering the QD charging properties, would allow the potential of a MOSFET QD system to be evaluated as a single charge memory or single carrier transistor if some level of tunability can be reached. Finally, in an attempt at exploring multi-gate devices for fine control over QD formation, the third goal is to fabricate a batch of Si nanowires and assess their performance, level of tunability as well as robustness in comparison to MOSFET disorder based QDs.

This thesis consists of six chapters following the introduction, with a literature review and background theory chapter outlining QD transport and PSB in Chapter 2, followed by a methodology describing the low temperature equipment and setups employed for QD characterisation in Chapter 3. The following three chapters present the results, with each also containing analysis and a discussion, where single spin sensing and SO strength extraction via PSB is displayed in Chapter 4 and an investigation into stress induced tunability in Chapter 5 using disorder based QDs in Si MOSFETs. Chapter 6 summarises the Si nanowire fabrication process as well as outlining the level of single and double-QD control achieved. The thesis then ends with a conclusion in Chapter 7, consisting of an overview of the most significant findings as well as both the advantages and disadvantages of the techniques employed along with future recommendations.

# Chapter 2

# Literature review and theory

This chapter is divided into two sections, the first reviews literature concerning work completed previously in the areas of single carrier transport devices, single spin detection and control, together with an alternative application from using MOSFET QDs for security purposes. The second section describes the basics behind MOSFET technology, followed by QD and spin transport, spin-orbit relaxation and the physical principles behind cooling.

## 2.1 Advancements in Si quantum information technology

### 2.1.1 Single carrier transport devices

The ability to form QDs through the fabrication of dedicated multi-gate devices as well as single impurity based structures has led numerous breakthroughs in quantum transport and quantum information processing schemes through manipulating individual charges [5, 104, 116, 117, 124, 132]. Various single electron and hole device architectures were designed and developed over the years, from single electon or hole transistors (SETs or SHTs) and single carrier pumps, to charge sensors and qubits [1, 9, 120, 122, 123, 133, 134].

SET device operation relies on single carrier transport between electrodes tunnel coupled to a QD in-between, which is facilitated by discrete energy levels, or prohibited due to the electrostatic charging energy of Coulomb-blockade, depending on voltage and charging parameters [42]. The main advantages of SET devices, aside from their nanometre scale compact size, is low power consumption, high sensitivity and high speed of operation [56]. As a product of this, SETs can be harnessed for various applications such as high sensitive electrometers, single electron memory devices and, of course, as a programmable SET logic device, similar to traditional MOSFETs [9, 124, 132, 133].

The disadvantages which limit their effectiveness are a low voltage gain, high output impedance and parasitic background charges, in additional to the major issue of VLSI compatibility owing to the sizes required (less than 10 nm) for room temperature operation [57]. Although such feature sizes are achievable they pose fabrication difficulties.

Currently the SI unit of electric current, the ampere, is defined as the force of attraction between by two straight parallel conductors of infinite length each carrying 1 A, at a distance of one metre apart in vacuum, a force equal to equal to $2\text{x}10^{-7}$ N/m [134]. This definition, adopted in 1948 and based on a thought experiment, does not meet the accuracy required for present day electrical measurements. Instead, like the metre and the second, a new definition based on fundamental constants of nature is needed based on elementary charge and frequency. In this field, known as quantum metrology, single carrier pumps fit the criteria of establishing a new current standard and closing the metrological triangle, where both resistance and voltage already have quantum electrical standards which are traceable to the quantum hall effect and Josephson voltage [46, 123]. Single carrier transport is necessary for a new definition of current, which is based not on the ampere but elementary charge, $e$, and frequency of operation, where carriers ar individually pumped across to generate a current of $I = ef$ [134]. Si nanowire devices with tunable barriers to define the QD, as well as offering a gate to apply high-frequecy to, have demonstrated successful pumping in the GHz range [102]. A record high frequency benchmark of 7.4 GHz for single carrier pumping has been achieved so far, as a consequence of a coupling between a QD and trap state under a gate, making the most effective single carrier pumps trap mediated by yielding improved operation [103].

Coulomb-blockade also occurs within industry grade Si MOSFETs at low temperatures as a consequence of disorder based QDs [78, 79, 106, 119]. This is advantageous for not only controlling discrete charges but also enables information on the dimensions and charging parameters of a QD system to be determined [148]. As such, MOSFETs provide an excellent test platform to explore single charge interactions. However, QDs originating from defects present in MOSFETs suffer from the inability to control aspects such as carrier number, size and coupling which are largely fixed by the poly-Si grains and interface defects that produce them [78, 79, 111, 112]. Despite this, successful attempts at mitigating the random nature of disorder QDs for use as a single carrier memory devices, as well as exploring singlet-triplet spin interactions have been carried out [88, 101]. Other works on Si nanowires demonstrate control of charge traps using a triple gate structure, together with disorder states acting as single electron memory at room temperatures [113, 115].

### 2.1.2 Single spin sensing and manipulation

Using Si for spin based quantum computing regimes is a natural choice for not only scalability and ease of integration with industrial fabrication techniques, but also long coherence times owing to isotopically enriched zero nuclear spin $^{28}$Si [15, 83]. The feasibility of spin qubits has also been demonstrated by high fidelitys exceeding 99.8%, which can be utilized in combination with quantum error correction towards achieving fault tolerant quantum computing, promoting spin as a competitive candidate in this space with respect to trapped ion and superconducting platforms [54, 80, 81, 82, 84, 85].

So far, single shot spin detection as well qubit operation has been achieved using QDs formed in CMOS compatible devices [11, 13, 55]. In order to develop qubits using CMOS technology the importance of sensing and manipulation cannot be understated. Although gate defined QDs have garnered much recognition, and employing many gates certainly adds flexibility, it is a fabrication intensive process. To promote better integration with classical control hardware, attempts are being made to develop functioning single charge devices using industry standard fabrication processes, which have the clear advantage of utilizing well established silicon (Si) fabrication technology and promote very large-scale integration (VLSI) [13, 121]. Recently, MOSFETs have gained attention within the field of quantum information technology owing to the need for closer system integration of cryogenic circuits and large-scale quantum computers [138, 139]. This approach has many advantages including reducing wiring complexity by simplifying interconnects, improving signal-noise ratio and low power consumption with sufficiently high power output [140].

Alongside scalability, another technological obstacle to overcome is that of electric-field mediated control, which relies on a strong SO interaction, but in the case of electrons in Si is intrinsically weak [89, 90, 92]. This has given rise to investigations into transport schemes with an enhanced SO interaction, where attempts using holes, valley states and the inversion asymmetry at the oxide interface has led to strong SO effects [25, 26, 27, 28, 29]. In parallel, hole spin resonance of trap states within a p-type MOSFET was achieved using Pauli spin-blockade (PSB) to study spin-orbit (SO) state mixing [101].

PSB is a phenomenon where current through a double-QD system is blocked due to the Pauli exclusion principle, as such the configuration and spin state of electrons, or holes, within QDs can be inferred. The first demonstration of PSB was carried out by K. Ono *et al* in 2002 using a GaAs lateral device [74]. The effect was observed by utilizing spin-to-charge conversion, i.e. the ability to infer spin orientation (up or down) by a change in current through a double-QD. As mentioned in the previous section, Coulomb-blockade is achieved where electrons cannot tunnel through QDs because of the absence

of energy levels. The key difference during a PSB configuration is the asymmetry in current between positive and negative $V_{SD}$. This is brought about by the fact that $QD_2$ (the second QD in the transport scheme) has one carrier occupying a level in a given orbital with a certain spin orientation, and since orbitals fill in pairs, this limits the next available state within the $QD_2$ to be of the opposite polarity. However, if the spin of a carrier tunnelling onto $QD_1$ (the first level within an orbital) has the same spin as $QD_2$ then no current can flow since it would form a triplet state. This situation describes a system operating under positive bias ($V_{SD} > 0$). Where as for negative bias, single carrier transport from the drain onto QD2 can always occur to the source because QD2 ia the spin selective QD, and in this situation the double-QD acts as a spin filter, since the energy level in $QD_1$ can accept any spin orientation.

In 2008, H. W. Liu *et al* became the first to fabricate a Si double-QD device exhibiting PSB [47]. A short time later, another Si MOS device was used to explore intra-dot coupling, such as how double-QDs exchange energy and interact as a function of coupling strength, as well as measuring the singlet-triplet (S-T) splitting [48]. In 2014 PSB was achieved with doner atoms, as opposed to isolated semi-conductor nano-structures with gates [49]. In this work, single dopant implants produced a double-QD consisting of phosphors atoms which were weakly coupled to a top gate (in order to control the energy levels for each donor) and source/drain electrodes. D. Kotekar-Patil *et al* were able to show PSB in a CMOS device and measured the S-T splitting [51]. Building on this K. Ono *et al* in 2017 became the first to show PSB in a standard MOSFET device with just one gate, which relayed upon the uncontrollable coupling between a two QDs produced by random defects in the gate [65]. The fact that a phenomenon associated with the spin orientation of two holes coupled together can be reproduced in a standard MOSFET at low temperatures is quite remarkable. K. Ono then provided further evidence by applying spin-resonance with an applied magnetic field to prove verify PSB and explore the S-T transitions within the system.

R. Li *et al* investigated PSB in the few hole regime and map the spin relaxation ($T_1$) induced leakage as a function of coupling [50]. The advantage of using valence band holes compared to conduction band electrons is that in Si they have an even weaker hyperfine interaction (an interaction between the spin of an electron and the nucleus) but a strong SO interaction due to their p-orbital nature. S. Nadj-Perge *et al* were then able to disentangle the dominant relaxation mechanism for a given system via the magnitude and scale of the magnetic field induced triplet leakage peaks, in order to identify and separate hyperfine interactions from SO hybridization [91].

The difficulty in establishing PSB in an ordinary MOSFET sample is that the QDs formed in the channel occur randomly due to defects in the gate oxide or poly-Si grains in the gate itself, causing surface roughness. This non-uniformity leads to variation in

the potential profile when applying gate voltage, and if the grain is small enough, discrete levels are formed in the potential profile, creating a QD. As a double-QD is needed for PSB, two poly-Si grains need to be in close proximity and coupled to one another to cause such an interaction, which is less likely in such an uncontrollable, single-gate system.

Therefore the requirement of detecting and manipulating single electron states for quantum information purposes is an importance issue, since Si spin qubits in particular are gaining momentum as a contender in qauntum computing platforms. There still remains work to be undertaken however to secure Si QDs as reliable quantum information candidates from standard industry fabrication processes.

### 2.1.3 Unclonable charging characteristics

The benefit of using standard industry CMOS devices is that they are notably easier to fabricate when compared to many-gated Si nanowires. However, although disorder QDs lead to a wide range of diverse charging properties, the varied single carrier phenomena associated with Coulomb-blockade can be taken advantage of in their current form by utilizing the inherent randomness. This was demonstrated though using the unique charging properties of a QDs within a MOSFET as a physically unclonable function (PUF), where each QD acts as a fingerprint for a given device [107]. The uniqueness of disorder QD Coulomb-diamonds present in this type of device allowed the individual characteristics of a transistor to be used as a kind of fingerprint to identify specific devices, with applications in security due to it's unclonable nature.

## 2.2 Fundamentals in silicon technology and physics

### 2.2.1 MOSFET operation

The basic structure and operating principles of MOSFETs will first be introduced. MOSFETs are incredibly important and useful devices, their miniaturisation has led to huge advances in technology and has arguably shaped the modern world more than any other electrical component over the past half a century as a result of aggressive scaling [35]. The basic idea behind scaling lays in producing smaller devices, and thereby increasing the transistor density, with increased switching performance and reduced power consumption with respect to the previous generation [66][67][68]. As of 2021, the device feature size entering full scale production has reached 5 nm, where the platform enables a 15% speed gain, or 30% power reduction, in comparison to 7 nm node [34].

One of the important applications of MOSFETs in CMOS digital circuits is when they are utilised as a simple, fast-switching electrical device. In such a scenario, a barrier imposed by the channel for a depletion mode MOSFET can be overcome through applying a gate voltage to form a conducting channel, known as the inversion layer, between two ohmic contacts (source/drain) [36]. In the lateral direction perpendicular to the channel, known colloquially as the metal-oxide-semiconductor (MOS) structure, the number of mobile charges is controlled at the interface through capacitive coupling, which is also dependant on the materials used and voltages applied, together with parameters such as oxide thickness ($t_{ox}$) and substrate doping concentration ($N_a$). A diagram showing the basic MOSFET structure is given in Figure 2.1. The gate is separated from the channel by an insulating layer which is usually Si-dioxide ($SiO_2$) or Si-oxynitride (SiON). The charge carriers of the conducting channel induce an inversion layer which are confined in 1-dimension at the oxide-Si interface that consists of electrons, known as a 2-dimensional-electron-gas (2DEG) in the case of an n-type device, or holes (2DHG) in the case of p-type device [69].

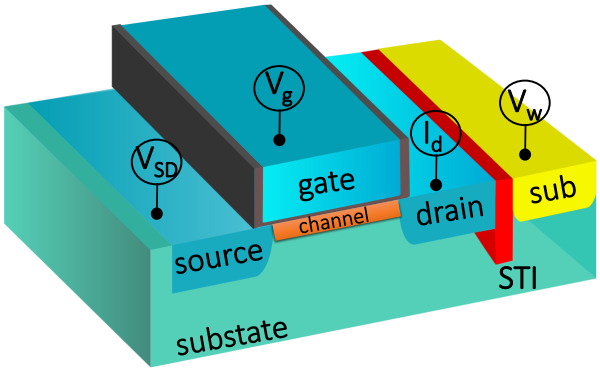



FIGURE 2.1: Basic structure of a MOSFET. Typical oxides include $SiO_2$ or SiON, with the gate usually consisting of heavily doped poly-Si and shallow trench isolation (STI) separates the substrate terminal.

Conventionally, the source and substrate terminals are usually grounded and a potential is applied to the drain, ($V_{SD}$) and gate ($V_g$). The threshold voltage, $V_{th}$, corresponds to the onset of the strong inversion and is effectively the point at which current flows ($I_d$) and the device switches on, making $V_{th}$ as one of the most important device parameters when characterising a MOSFET. The two most common measurement schemes when measuring MOSFETs are known as the transfer ($I_d - V_g$) and output ($I_d - V_{SD}$) characteristics. For transfer, the gate is swept while monitoring $I_d$ with fixed $V_{SD}$, as opposed to measuring the output, where $V_g$ is fixed while $V_{SD}$ is swept. The current is negligible before reaching $V_{th}$ for both schemes. During transfer characteristics when $V_{SD}$ is fixed, an increasing $V_g$ leads to an exponential $I_d$ curve as the inversion layer increases. For output characteristics when $V_g$ is fixed, increasing $V_{SD}$ bias shows ohmic behaviour up to a saturation region where the current no longer increases, known as the cut-off region. This cut-off region is caused by the reduction in the local $V_g$ bias due to

positive $V_{SD}$ bias, since the reduction is greatest near the drain the resulting pinch-off leads to saturation in $V_{SD}$ for output characteristic plots.

After a brief introduction on the importance of MOSFETs and the basic operating parameters, the role of energy bands and the physics behind how semiconductors function will now be described. Semiconductors have such useful properties due to their band-gap nature, a region void of energy states between the conduction band ($C_b$) and the valance band ($V_b$), however unlike insulators this band gap can be overcome by an modest electric field in the form of the applied gate voltage $V_g$. The band-gap of a semiconductor is the minimum energy required to excite an electron from a bound state (in the $V_b$) to a free state (in the $C_b$), where it can then participate in conduction within the crystal structure.

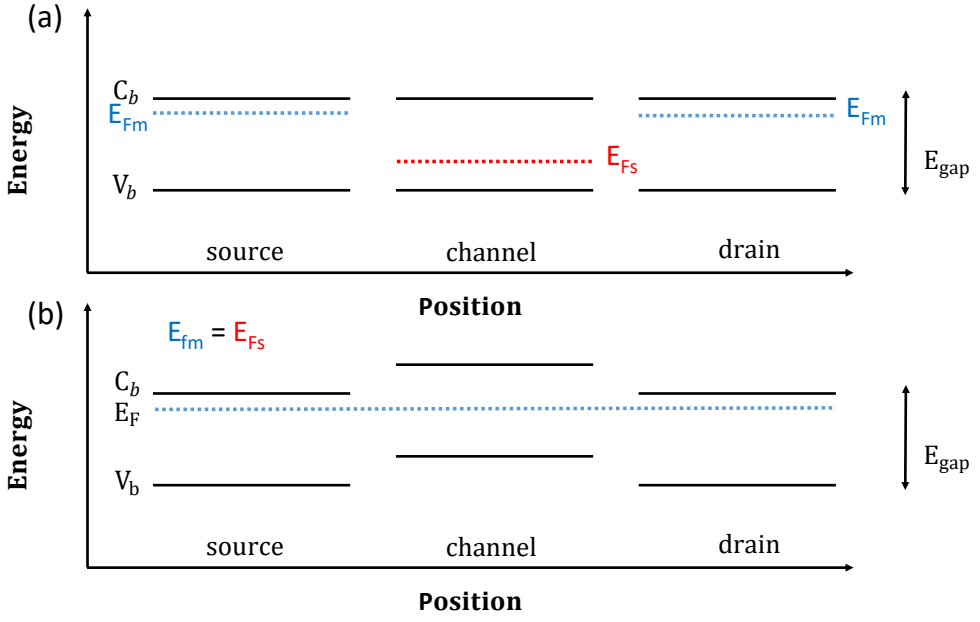



FIGURE 2.2: (a) Fermi-levels of the highly doped n-type source/drain ($E_{Fm}$) and p-type Si channel ($E_{Fs}$) together with the conduction ($C_b$) and valence ($V_b$) bands, when all three are separated. (b) Shows the $E_f$ alignment after joining the three materials together, since $E_{Fs}$ is lower in the channel both $C_b$ and $V_b$ both shift upwards.

For semiconductors the Fermi-energy ($E_F$), which is the average energy of an electron at 0 K within the material, exists within the band-gap between $C_b$ and $V_b$. The Fermi-level will remain constant inside the semiconductor, independent of the biasing conditions. Figure 2.2 shows the relative Fermi-levels of the source/drain terminals as well as the p-type channel when the regions are disconnected in (a), and then connected in (b). When materials of different Fermi-levels are joined together an equilibrium is reached as a product of charge transfer. In the case of Figure 2.2(b), the $E_F$ of the channel is shifted upwards together with $C_b$ and $V_b$. Figure 2.3 shows how $V_g$ and $V_{SD}$ induces band bending of these three regions in order to open the channel. As the p-type

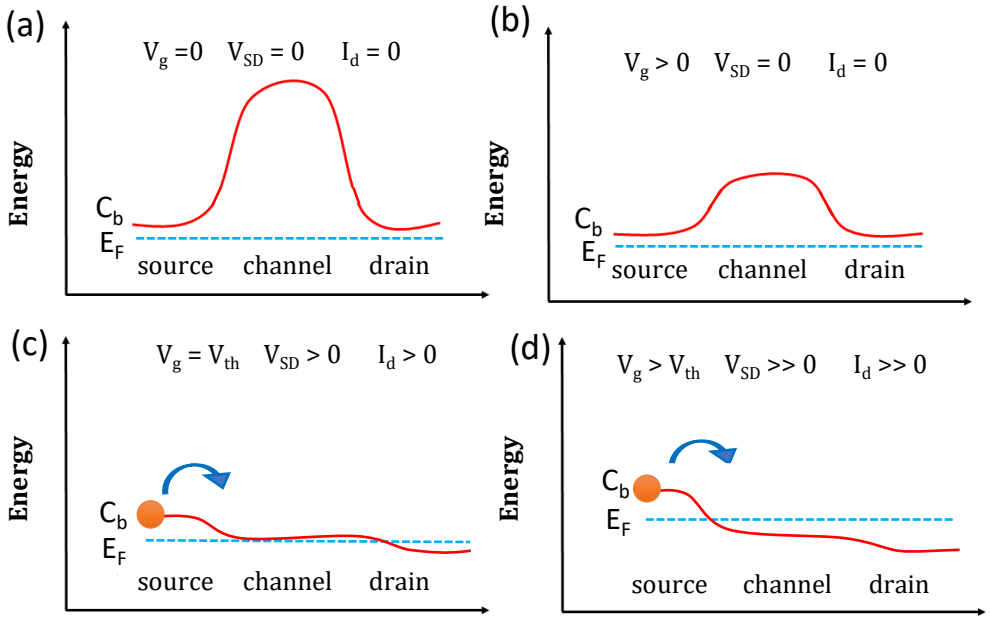



FIGURE 2.3: (a) $V_g$ is below threshold voltage ($V_{th}$) therefore the conduction band is energetically out of reach within the channel. (b) $V_g$ is approaching $V_{th}$, but no drain current ($I_d$) flows. (c), $V_g$ is at $V_{th}$ and has a small $V_{SD}$ bias, $I_d$ flows through the channel. (d) $V_g$ is above $V_{th}$ and $V_{SD}$ is large, and a large $I_d$ flows.

Si substrate in the channel is effectively an insulator when $V_g$ is zero, $I_d$ is negligible (Figure 2.3(a)-(b)), even when applying $V_{SD}$ bias. In Figure 2.3(c), once $V_{th}$ is reached and $C_b$ is sufficiently close to $E_F$ then $I_d > 0$. Applying larger $V_{SD}$ then generates a larger $I_d$ from further barrier lowering across the channel as shown in Figure 2.3(d).

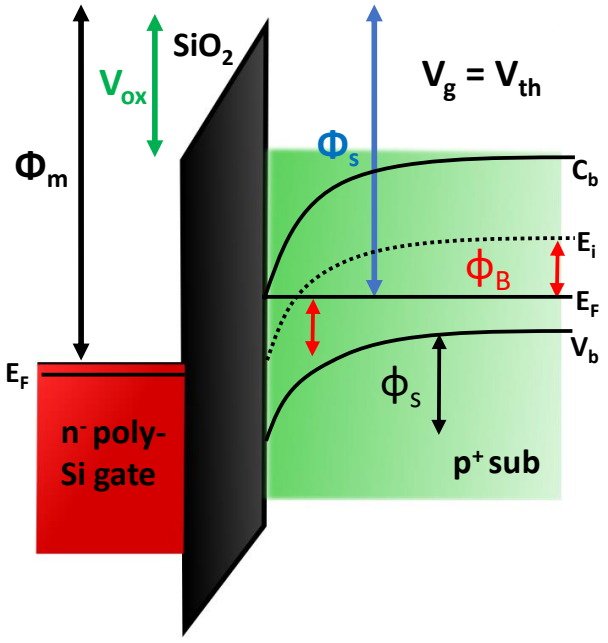



FIGURE 2.4: Energy band diagram at the MOS interface with $V_g$=$V_{th}$. Here, $V_{ox}$ is the voltage across the oxide, $\Phi_m$, $\Phi_s$, $\phi_B$ and $\phi_s$ are the work functions for the poly-Si and substrate, and the Fermi potential of the bulk and surface potential respectively.

Figure 2.4 displays an energy band diagram across the MOS structure at the threshold condition $V_{\mathrm{g}} = V_{\mathrm{th}}$. The Fermi-levels of the n-type poly-Si gate and p-type substrate are given, together with the voltage across the oxide ($V_{\mathrm{ox}}$). Also labelled in Figure 2.4 are $\phi_m$ and $\phi_s$, which represent the work functions of the highly doped poly-Si and the p-type semiconductor substrate respectively, along with $\phi_{\mathrm{s}}$ the surface potential and $\phi_{\mathrm{B}}$ the bulk (or substrate) potential. $\phi_{\mathrm{s}}$ represents the amount of band bending due to the external potential, while the bulk potential represents the acceptor concentration in the substrate. At zero applied voltage, energy band bending is determined by the interface charge due to the difference in Fermi-levels. At the oxide-Si interface inducing charge is incredibly important since it alters the distribution of the energy bands at the interface to form a 2DEG. Applying a gate voltage then induces inversion charge by altering $\phi_{\mathrm{s}}$ and $V_{\mathrm{ox}}$ according to [70]

$$V_{\mathrm{g}} = V_{\mathrm{FB}} + \phi_{\mathrm{s}} + V_{\mathrm{ox}} \tag{2.1}$$

where $V_{\mathrm{FB}}$ is flat-band voltage, the required bias in order to remove any band bending as a result of electrostatic interactions at the oxide interface when joining materials with different $E_{\mathrm{F}}$. The significance of the flat-band voltage is that no charge is present in the channel under these conditions, and is given by

$$V_{\mathrm{FB}} = (\Phi_{\mathrm{m}} - \Phi_{\mathrm{s}})/q \tag{2.2}$$

The voltage across the oxide is dependant on the amount of charge in the substrate ($Q_{\mathrm{sub}}$) and the oxide capacitance ($C_{\mathrm{ox}}$) via

$$V_{\mathrm{ox}} = -Q_{\mathrm{sub}}/C_{\mathrm{ox}} = \frac{\sqrt{qN_{\mathrm{a}}2\epsilon_s\phi_{\mathrm{s}}}}{C_{\mathrm{ox}}} \tag{2.3}$$

here, $q$ is elementary charge. In the case of Figure 2.4, at the threshold condition

$$\phi_{\mathrm{s}} = 2\phi_{\mathrm{B}} \tag{2.4}$$

using these physical relations in equations 2.1-2.4, $V_{\mathrm{th}}$ can be calculated to give

$$V_{\mathrm{th}} = V_{\mathrm{FB}} + 2\phi_{\mathrm{B}} + \frac{\sqrt{qN_a2\epsilon_s2\phi_B}}{C_{\mathrm{ox}}} \tag{2.5}$$

where $C_{\mathrm{ox}} = \epsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$, using the known permittivity of the oxide $\epsilon_{\mathrm{ox}}$.

As a consequence, equation 2.5 produces a $V_{\mathrm{th}}$ value from the conditions detailed to allow the formation of a 2DEG at the oxide-Si interface. This crucial aspect enables the MOS structure to function as an efficient conductive/insulating switching device through the simple application of a $V_{\mathrm{g}}$ driven electric field.

### 2.2.2 QD transport and properties

So far MOSFETs have been discussed in the context of typical operation at room temperature ($\approx$ 295 K). However, this project is dedicated to study of quantum devices and single carrier phenomena. Therefore this section introduces the concept of quantum dots (QDs), which can be formed through the use of gates in dedicated nano-electronics devices in addition to disorder based QDs within MOSFETs at low temperatures.

QDs are often described as artificial atoms, attributed to their discrete energy level spacing as a result of quantum confinement [40]. Quantum confinement is an effect whereby the reduction in the dimensions of an object causes energy bands to eventually manifest as discrete levels, and allows quantum effects to be observed and probed directly. The QD confinement energy can be approximated by

$$E_{\text{confine}} = \frac{h^2}{2m^* d_{\text{QD}}^2} \tag{2.6}$$

where $h$ is Planks constant, $m_e^*$ is the effective carrier mass and $d_{\text{QD}}$ is QD diameter [71].

A QD illustration is shown in Figure 2.5(a), where an isolated island is in contact with gate, source and drain terminals capacitively. The device structure and biasing conditions alters the relative position of the energy levels within the QD, permitting the transfer of individual carriers by a process known as quantum tunnelling [41]. Figure 2.5(b) displays an energy level diagram where tunneling is permitted as a result of a level existing between the source/drain barriers. When tunneling occurs, the charge on

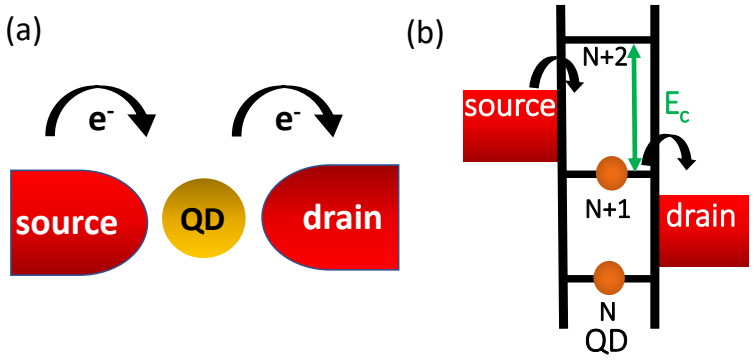



FIGURE 2.5: (a) Illustration showing how carriers quantum tunnel from source to drain via a QD. (b) Energy level diagram with the relative source/drain potentials as well a quantum levels between barriers for carriers to tunnel through in the QD, where N refers to carrier occupation.

the island suddenly changes by the quantized amount $e$. For every carrier that tunnels onto a QD, the electrostatic potential is increased to a value known as the charging energy ($E_c$), which must be overcome for additional carrier occupation as shown in Figure 2.5(b) [42]. This parameter becomes particularly important at low temperatures

when

$$E_c = \frac{e^2}{2C_\Sigma} \gg k_b T \tag{2.7}$$

where $C_\Sigma$ is the total capacitance, $k_B$ is the Boltzmann constant, and T is the temperature. Increasing $V_g$ lowers the energy levels within the QD, so for example, in Figure 2.5(b), applying $V_g$ would eventually lead to the N + 2 level to fall between the source/drain, where transport would be allowed through this level. $V_{SD}$ changes the potential energy between the source/drain terminals, whereby a larger $V_{SD}$ in Figure 2.5(b) would align the level N with the drain, affecting the transport dynamics by opening another energy state for carriers to tunnel through. During the absence of available levels between the source/drain, a phenomenon called Coulomb-blockade occurs, where current cannot flow due to the $E_c$ as a result of Coulomb repulsion within the QD. Applying $V_g$ bias until a level becomes available would then resume current flow.

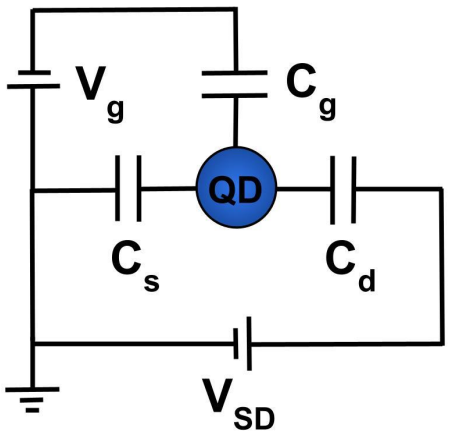



FIGURE 2.6: A circuit diagram showing how a QD in the channel is capacitively coupled to the gate ($C_g$), source ($C_s$) and drain ($C_d$).

The difference in energy due to an individual charge can be expressed in terms of the capacitance [71]. A circuit diagram of a QD, which iteslf acts as a capacitor, along with the gate and source/drain capacitances ($C_g$ and $C_s/C_d$) and respective terminals ($V_g$ and $V_{SD}$) are shown in Figure 2.6. During this regime, tunnelling is blocked due to the electrostatic charging energy of the occupying holes or electrons [72]. However, applying a gate voltage, which capacitively coupled to a QD via $C_g$, alters the potential continuously for a given sweep. During such a sweep, the conventional build-up of induced charge is instead compensated for by periodic intervals of discrete charge tunnelling onto the QD. This competition, between continuously induced charge and discrete compensation, leads to Coulomb oscillations within the transport window, and Coulomb-blockade when transport is prohibited. This is essentially a quantized version of what occurs in traditional MOSFET transport.

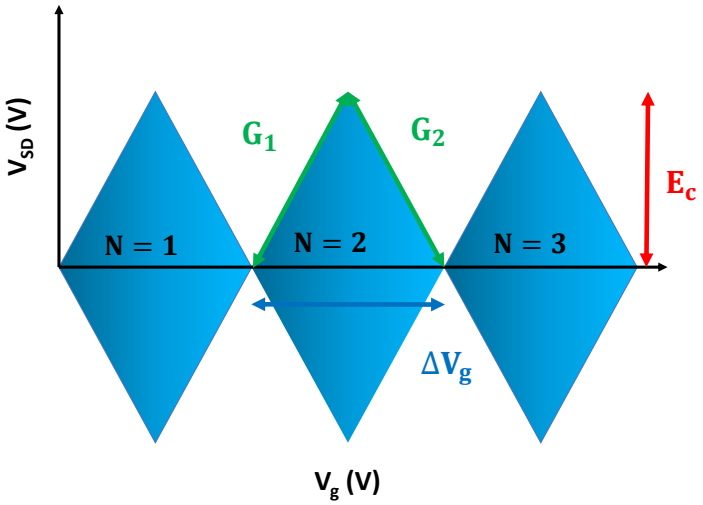



FIGURE 2.7: A simplified charge stability diagram (CSD) showing ideal Coulomb-diamonds from QD charging characteristics. Parameters such as the charging energy $E_c$, gradients $G_1$ and $G_2$ as well as $\Delta V_g$ for reference.

Figure 2.7 displays a physical representation of Coulomb-diamonds, which are generated by a charge stability diagram (CSD) by measuring $I_d$ whilst sweeping $V_g$ and $V_{SD}$ voltage space. As described above, each Coulomb-diamond represents blocked current flow from the absence of energy levels within the QD for single carrier transport, therefore increasing the $V_{SD}$ or $V_g$ bias to outside of the blue region will then allow current flow. Simply put, the regions outside the Coulomb-diamonds are where there are energy levels available, whereas within the Coulomb-diamonds they are absent. Therefore a CSD is a very important and useful tool in characterising and visualising the charging properties and transport characteristics of QDs. Coulomb-diamonds are a key measurement tool to visualize the charging and transport properties of QDs, which appear in $I-V$ characteristics as a result of Coulomb-blockade in the sub-threshold region. Each successive Coulomb-diamond therefore represents an additional single carrier occupying a QD energy level which is capacitively controlled by gate and source/drain terminals. Typically temperatures below 4 K are sufficient to observe single carrier tunneling due to discrete energy levels.

Using the highlighted features in the CSD displayed in Figure 2.7, the transport boundary edge gradients $(G_1/G_1)$ produces values for $C_s$ and $C_d$ through

$$G_1 = C_g/C_s \tag{2.8}$$

$$G_2 = C_g/(C_g + C_d) \tag{2.9}$$

where the Coulomb-diamond width ($\Delta V_{\mathrm{g}}$) can be used to determine $C_{\mathrm{g}}$ and the lever arm parameter ($\alpha$), together with $C_{\Sigma}$ defined as [72]

$$\Delta V_{\mathrm{g}} = \alpha e / C_g \tag{2.10}$$

$$C_{\Sigma} = C_g + C_s + C_d \tag{2.11}$$

Equations 2.8-2.11 then allow the determination of $E_{\mathrm{c}}$ via

$$E_c = e/C_{\Sigma} + \Delta_{N+1} \quad \approx \quad E_c = e/C_{\Sigma} \tag{2.12}$$

Finally, $d_{\mathrm{QD}}$ can be estimated by

$$d_{QD} = \sqrt{4C_g/\pi C_{\mathrm{ox}}} \tag{2.13}$$

assuming the QD acts as a 2-dimensional isolated disk.

For MOSFET devices, QD transport is realised as the channel becomes inverted and a 2DEG (2DHG) begins to form. Structural randomness from poly-Si grains or trap state then leads to additional confinement via electron (valance) band bending along the lateral directions of the channel, generating island-like structures (QDs) as a product of quantum confinement due to their size [37]. Single carrier transport is then observed as a result of discrete charging from levels within the altered potential profile. Consequently, applying sufficient gate voltage leads to non-uniformity across the channel because of the modified threshold for inversion at these small regions, since electrons (holes) are able tunnel through the defect originated levels, whereas tunnelling barriers exist on either side.

The tunability of a QDs make them an ideal candidate for controlling individual carriers which can be utilised for applications such as single electron or hole transistors (SETs or SHTs) and single carrier pumps, where fine and stable control is a necessity. Using double-QDs acting as a test bed for the most basic many-body system would allow other rich physical phenomena associated with spin to be probed. Such as system would aid in understanding the interactions of two or more quantum states and allow fundamental laws of quantum mechanics such as the Pauli-exclusion principle and superposition of states to be explored, which is introduced in Section 2.2.3. This is of immense interest for quantum information processing and quantum computing [43].

### 2.2.3 Pauli spin-blockade and spin-orbit interaction

Pauli spin-blockade (PSB), a common measurement tool used throughout quantum information protocols, is dependant on the spin-orbit (SO) interaction when detecting spin states [74, 77, 97, 98, 100]. PSB is manifested as the suppression of current through a

double-QD system in a Triplet state as a consequence of the Pauli exclusion principle [44]. Such a technique effectively allows individual spins to be read by correlating the spin state with the charge state through monitoring the double-QD current [75, 76]. As discussed in Section 2.1.2, within this regime S-T state mixing, relaxation mechanisms, and SO coupling can be probed, since the SO interaction offers a mechanism for coupling hole spin with their orbital motion [95]. In this section the basic physics of electron/hole spin together with the operating principles of PSB are explained.

The quantum mechanical effect that allows PSB to occur is due to the fact that two or more fermions (half-integer spin particles) cannot occupy the same space, so for example, no two electrons can have the same quantum numbers within an atom [43]. This is more commonly known as the Pauli Exclusion Principle and is key to orbital filling and the chemical properties of matter. The spin of a particle is one such quantum parameter, which can exist in either an up (↑), or down (↓) state, and can pair together to form a S or T state as summarized in Figure 2.8.

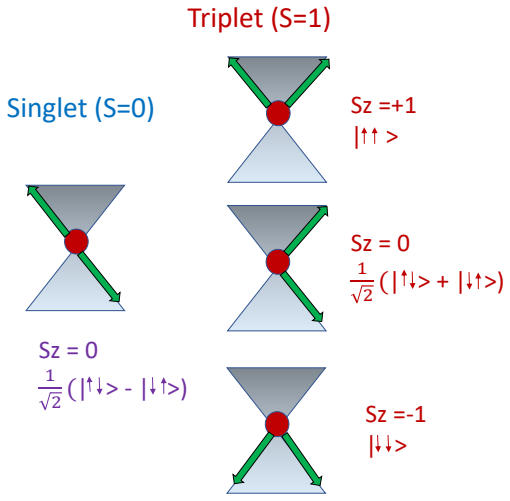



FIGURE 2.8: Summary of four different electron/hole spin configurations which are dependant on the spin orientation (up or down). The charge carrier is given in red at the centre and the precession axis is marked by the green arrow. This leads to a spin singlet when two opposing spins pair, or a spin triplet when two spins pair with the same orientation (note that the $S_z$=0 triplet state is a linear combination of singlet states).

Since PSB is a spin based phenomenon, applying a magnetic field induces an interaction known as the Zeeman effect. Pieter Zeeman discovered this effect in 1896 when measuring the spectral line broadening of a sodium discharge tube in a magnetic field, from this he was able to obtain the charge to mass ratio of the electron, one year before Thompson's measurement [73]. At the time, neither the existence of the electron or nucleus were known. Zeeman's colleague, Lorentz, was able to explain the observation by postulating the existence of a moving "corpuscular charge" that radiates electromagnetic

wave. The emitted light forms a discrete spectrum, reflecting the quantized nature of the energy levels. The result of this interaction, between the magnetic moment generated by electron/hole spin and an external magnetic field causes an energy level splitting [63]. Electrons which align parallel with the external field experience a reduction in energy, while spins anti-aligned increase in energy [7]. The Zeeman splitting energy ($\Delta E_z$) is given by

$$\Delta E_z = g\mu_B B_z \tag{2.14}$$

where $g$ is the gyromagnetic ratio ($\approx 2$), $B_z$ is the external magnetic field in the z-direction and $\mu_B$ is the Bohr magnetron (equal to $57.8\mu$ eV/T), calculated via

$$\mu_B = \frac{e\hbar}{2m_e} \tag{2.15}$$

For a single spin, the readout is only effective at very low carrier temperature and high magnetic fields where

$$k_B T \ll \Delta E_z \tag{2.16}$$

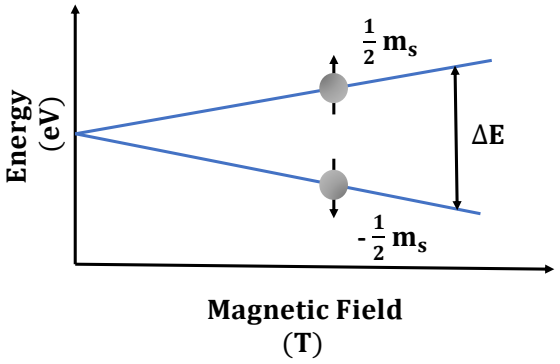



FIGURE 2.9: A single energy level is split depending on the spin being ↑ or ↓, where the spin quantum number is represented by $m_s$. At 0 T both spin states are degenerate in energy, while after applying an external field the zeeman splitting increases according to equation 2.14.

As discussed in the Section 2.2.2, quantum confinement causes QDs to behave as individual atoms with discrete energy levels. If two QDs are coupled together then PSB should be observable under appropriate biasing conditions [45]. In Figure 2.10.(a)-(b) energy level diagrams are displayed with the S and T state configurations for PSB to occur, along with ($N_{QD_1}$,$N_{QD_2}$) which refers to the number of carriers in the highest occupied orbitals of $QD_1$ and $QD_2$. In the absence of a magnetic field only the S(1,1) state can provide a direct route to S(0,2) (Figure 2.10(a)) which are tunnel coupled by $t_c$, and if the system enters the T(1,1) state PSB is initiated (Figure 2.10(b)). The blocked T(1,1) states with parallel spins can be lifted however by both relaxation to the S(1,1) state as well as the S(0,2) through mixing on account of the SO interaction

introducing non spin-conserving tunnelling between the QDs [91]. When a magnetic field is applied, the blocked T states are split by the Zeeman energy which effectively alters the relaxation rate by providing faster alternative routes between the T(1,1) and S(0,2) by state mixing and leads to an increase in PSB leakage current.

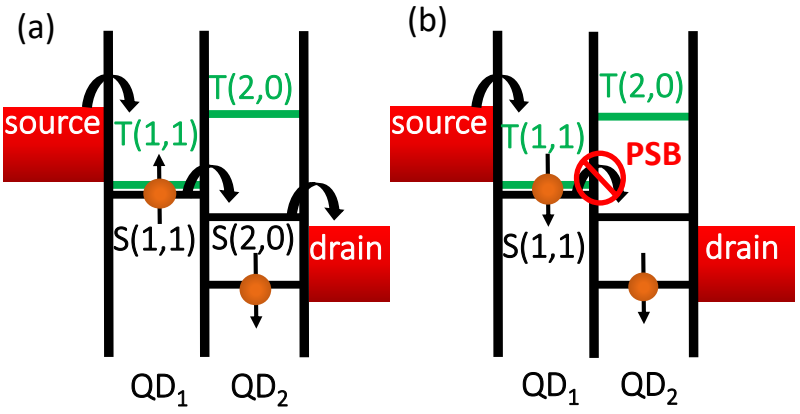



FIGURE 2.10: Energy level diagrams for PSB occurring in a double QD, where the path through to S(0,2) is allowed in (a) from the S(1,1) state, but blocked in (b) due to parallel spins in each QD as a result of T(1,1).

The SO interaction is of particular interest when controlling spin, and originates from the interaction between the spin and the orbital angular momentum of an electron or hole. A model was put forward by [33] to study the effect of magnetic-field on spin relaxation during the PSB regime in the presence of a strong SO interaction. In particular it includes the lifting of PSB at high-fields, or at low $t_c$. However, the model produces a single peak in the magnetic-field dependant leakage current as a result of the hyperfine interaction being the dominant spin mixing mechanism, as opposed to the SO interaction. To compensate for the differing mechanism, this framework was expanded upon by [89] where only the spin relaxation to the ground state was considered, to produce a double-peak structure in the triplet leakage current.

As such, spin relaxation during PSB due to the SO interaction can be investigated through magnetic field dependant peaks appear due to different relaxation processes competing with each other from a combination of both the SO interaction and the Zeeman effect on account of the applied magnetic field, where the latter becomes more efficient at higher fields and therefore allows transitions between S-T configurations [90]. Based on this, the peaks at a finite field are explained by the lifting of PSB as a result of strong spin-orbit induced S-T mixing [25]. A model was put forward in [89] which describes the physical mechanism. At zero-field there are three blocked states due to the Pauli-exclusion principle, with each being degenerate, that can relax to the hybridized (1,1) - (0,2) ground state due to the SO interaction, where they then pass to the drain

and are measured as current. This path transports an average of four holes across the double-QD system in a time $3\Gamma_{rel}^{-1}$ and produces a leakage current of $I = \frac{4}{3}\Gamma_{rel}$. Here, $\Gamma_{rel}$ is the average relaxation rate at zero-field from (1,1) to S(0,2). When a magnetic field is applied, a coupling of $\approx \alpha B$ between two of the blockaded states provides an alternative path and generates a greater leakage current. Such an interaction becomes significant when the relaxation rate, $\approx \alpha B^2\Gamma/t^2$, becomes comparable to $\Gamma_{rel}$, namely when $B \approx (t/\alpha)\sqrt{\Gamma_{rel}/\Gamma}$, where $\alpha$ is a ratio characterizing the relative strength of tunnel and spin orbit couplings $t_c$ and $t_{SO}$, and B is the applied field. As the magnetic field is increases further the leakage tends to its maximum value $I = 4\Gamma_{rel}$, occuring when only a single blocked state remains, resulting in an average of four holes being transported in a time $\Gamma_{rel}^{-1}$. As a result, a zero-field dip in the leakage of width $B \approx (t/\alpha)\sqrt{\Gamma_{rel}\Gamma}$ and a maximum reduction of 1/3 of the current when B = 0.

As relaxation rate $\Gamma$ (the total transfer rate from of all states to the drain) is finite and all relaxation is directed toward the ground state, Coulomb blockade can occur between the (1,1) ground state and a triplet state. Therefore when the magnetic field is increased, the current will eventually be suppressed to zero and generate a double-peak leakage current. Approximately, the scale of the magnetic field required for this to occur should be $\approx \Gamma$, since the level width of the S(0,2) state is set by $\Gamma$, in addition to $B \geq \Gamma$, the relaxation rate from the triplet state, which eventually becomes zero. However, the actual scale of the magnetic-field needed is actually dependant upon the competition of $\Gamma$ with $\Gamma_{rel}$. Accordingly, only when the magnetic field induced suppression becomes so strong that escape from the triplet state is the main bottleneck for the leakage current, the decrease in current becomes significant. As such, this escape rate, $\approx (\alpha t)^2\Gamma/B^2$, can be compared with $\Gamma_{rel}$ to find an estimate for the width of the overall double-peak structure $B \approx (\alpha t)\sqrt{\Gamma/\Gamma_{rel}}$. Therefore when a $B_{\|}$ is applied S-T hybridization occurs, where its effect is dependant on the interdot coupling and SO interaction strength, which can then be exploited to quantify important parameters such as the SO length ($l_{SO}$) and tunnel coupling $t_c$. $l_{SO}$ describes the ballistic distance travelled by a carrier during which its spin precesses by 1 radian and is a direct measure of the SO interaction strength.

In summary, by analysing PSB leakage current, tunneling events due to spin relaxation can also be investigated. Important physical parameters such as $l_{SO}$ and the tunnel coupling $t_c$ can be quantified [96]. The typical energy spacing of a QDs is in the order of a few meVs, where the thermal energy of carriers at room temperature is 26 meV. This means that for measurements concerning charging and the small energy differences associated with spin-related phenomena requires low temperatures to ensure the energy scale is larger than the noise due to thermal activation.

### 2.2.4 Basics of refrigeration and Joule-Thomson expansion

To observe single carrier transport, measurement at sufficiently low temperatures requires methods of cooling samples from temperatures of 300 K to below 2 K. This essentially comes down to the fundamental concepts of the first two laws of thermodynamics, together with mechanical refrigeration and the expansion of real gases at a needle valve.

The first law of thermodynamics is based around the conservation of energy, whereby the sum of energy or heat flow into a system is simply equal to the sum of energy out of the system, assuming steady state conditions [109]. This energy is anything where heat flow exists, and because any material flow (as a product of pumping) consists of some thermal or mechanical energy transfer, the thermomechanical energies of material flow has to be taken into account by means of enthalpy flow. As such, an additional heat flow must exist, a heat flow out of the system (or refrigerator) in order to balance the system. The abbreviation for this waste energy flow is $\dot{\mathrm{Q}}_{amb}$. Therefore, when describing a refrigerator the first law becomes:

$$\dot{Q} + P = \dot{Q}_{\mathrm{amb}} \tag{2.17}$$

where $\dot{\mathrm{Q}}$ is the heat flow from a cooling object, P is the power which enters the system and $\dot{Q}_{\mathrm{amb}}$ is the waste heat [109].

The first law simply sums all heat flow into and out of the system, in order use the cooling capacity of a refrigerator to determine the efficiency, the second law of thermodynamics is required in the form of the Carnot equation. This assumes the system to be an ideal refrigerator where waste energy is absent. The value of the so called coefficient of performance (COP) can then be used to characterize the efficiency of refrigerator and is defined as the ratio of the cooling capacity to the driving power. The COP for the refrigerator is:

$$COP = \frac{\dot{Q}}{P} = \left(\frac{T_h}{T_c} - 1\right)^{-1} = \frac{T_c}{T_h - T_c} \tag{2.18}$$

where $T_h$ and $T_c$ are the 'hot' and 'cold' body temperatures [109].

These two laws of thermodynamics are employed within a G-M refrigerator, the most common type of cryocooler which is used for initial cooling stages of many cryostats. In such a system, room temperature helium gas is first compressed and then supplied to the refrigerator, where the compressed helium is then cooled by expansion, This provides cooling to the heat stations on the refrigerator, and after cooling, the gas is

returned to the compressor to repeat the cycle. In order to reach temperatures below 4.2 K with helium, however, an alternative cooling process known as throttling is needed.

Throttling is an effect where gas flowing through a restriction experiences a reduction in temperature, together with a pressure drop. This phenomenon, whereby gas forced through a valve from high to low pressure is known as the Joule-Thomson effect. Any expansion of a gas at valve, capillary or other vent where the is a resistance differential is called Joule-Thomson expansion. The effect is characterized by the coefficient $\mu$, and is given by [109]:

$$\mu_j = \left(\frac{dT}{dP}\right)_{h=const} \tag{2.19}$$

An important point of this process is that during Joule-Thomson expansion there are no changes in the energy of the gas throughout the throttling procedure, meaning that there isn't any heat flow into or out of the system. Therefore the thermomechanical energy of the gas, or enthalpy of the gas, during the throttling process is constant. This means that the enthalpy at the inlet into the valve and the enthalpy at the outlet are identical. The Joule-Thomson coefficient is a material property, like the density or specific heat capacity. It depends on thermodynamic conditions such as pressure, temperature, and phase state, and differs between materials. The Joule-Thomson coefficient is also a property of real gases, which means gases that cannot be described adequately by the ideal gas equation ($pV = nRT$). As such, the final stage of cooling within cryogenic systems forces helium to enter through a high resistance valve known as a needle valve, which then leads to throttling and further a reduction in temperature.

# Chapter 3

# Preparations and methodology

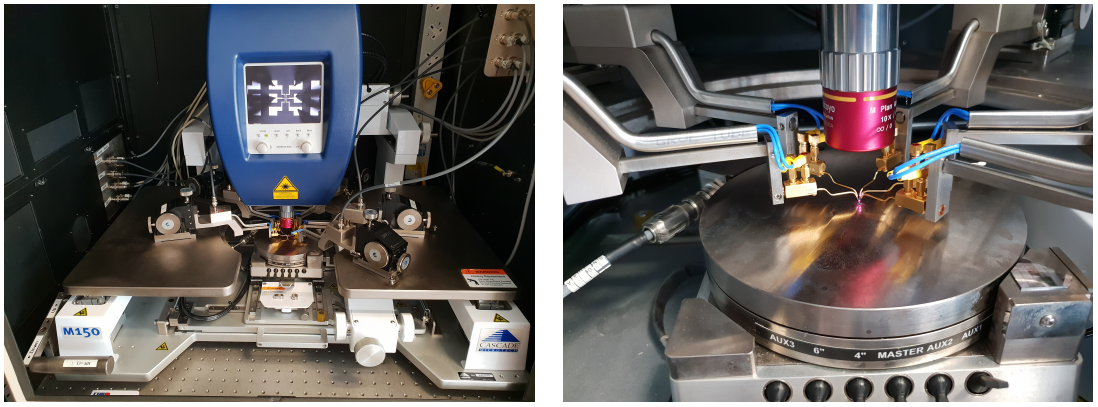
## 3.1 Introduction

This chapter outlines the experimental setups used for data collection together with device preparation methods. Three measurement systems in total were employed, one room temperature system (probe-station) and two low temperature systems (LHe cryostat and Cryogen-free measurement system (CFMS)). The probe-system was necessary for device validation. Both the probe system and LHe cryostat were fully operational, where as the CFMS required significant repairs in order to measure at sustained low temperatures. The methodology concerning the use and implementation of all three systems, including the repairs and optimisations applied to the CFMS, as well as the sample preparation techniques such as wire bonding are also described.

## 3.2 Probe-station measurement system

A probe-station connected to a Keysight B1500A semiconductor analyser was used to collect the $I-V$ characteristics for CMOS samples at room temperature. The probe-station setup consists of a Cascade M150 probe-station with 4-6 prober arms and a Polytec MSA-400 microscope which is focused onto centre of the sample platform (chuck) where the arm tips are located. The probe-station itself is housed inside a metal box which acts as a Faraday cage, as displayed in Figure 3.1(a), which removes external noise that would otherwise dominate the sensitive low current measurements. The microscopic prober arms are manufactured with gold tips to provide excellent electrical contact, together with precision placement of the tip ends onto the device electrical pads using the microscope (Figure 3.1(b)). In order to achieve such accurate probing, the system lays on a Thorlabs anti-vibration optical table which is attached to a pump to maintain sufficient table leg pressures.

Each prober arm is electrically connected to an SMU inside a B1500A via triaxial cables through the probe-station housing as per the drawing in Figure 3.2. Each SMU is capable of outputting an accurate voltage whilst measuring a very small current (a resolution of 10 $\mu V$ and 200 fA). Measuring the transfer characteristics, i.e. sweeping the potential of various gates whilst measuring the $I_{\mathrm{d}}$, is the main characterisation method for testing our devices, and as discussed in Chapter 2, is also prevalent in research literature along with the output characteristics (sweeping the source-drain potential.)




(a) Entire probe-station setup inside a Faraday cage.

(b) Enhanced image displaying the probe-station chuck, needle arms for probing and the microscope lens (x40 zoom).

FIGURE 3.1: Cascade M150 probe-station for room temperature measurement.

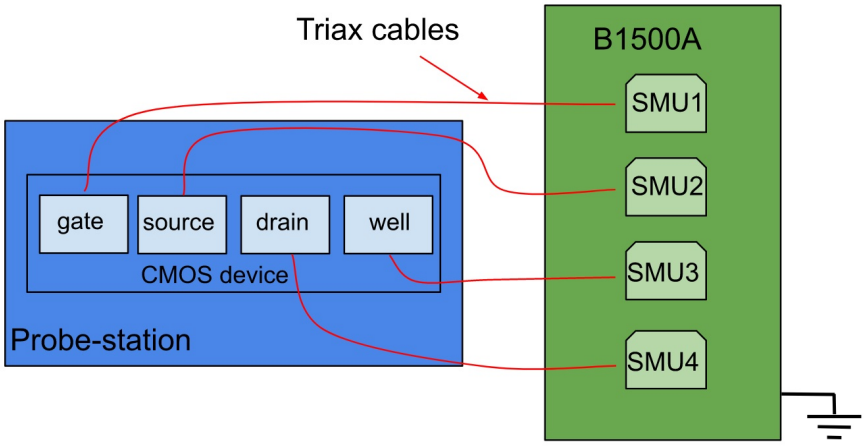
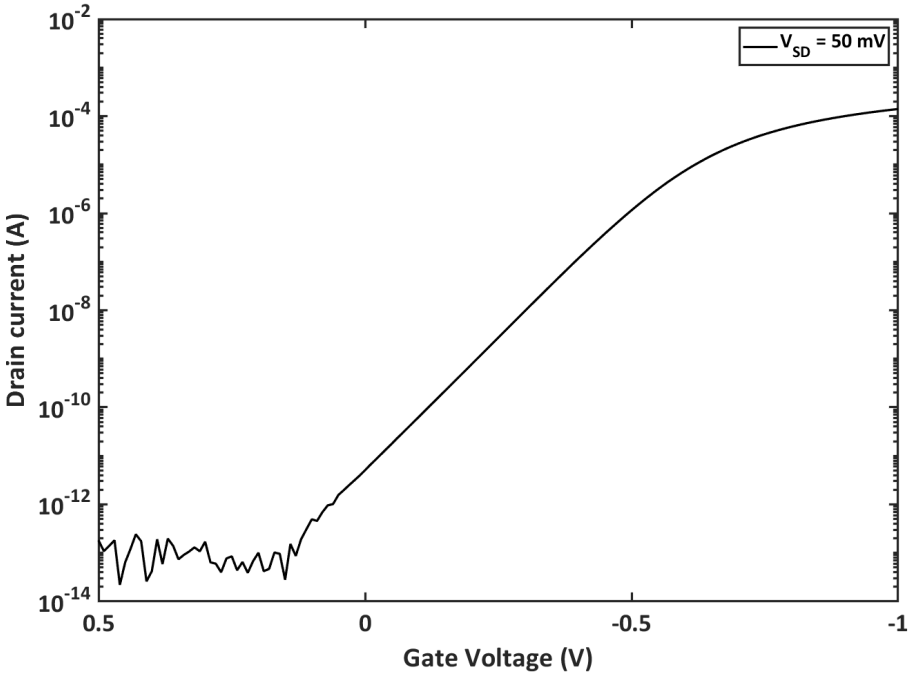


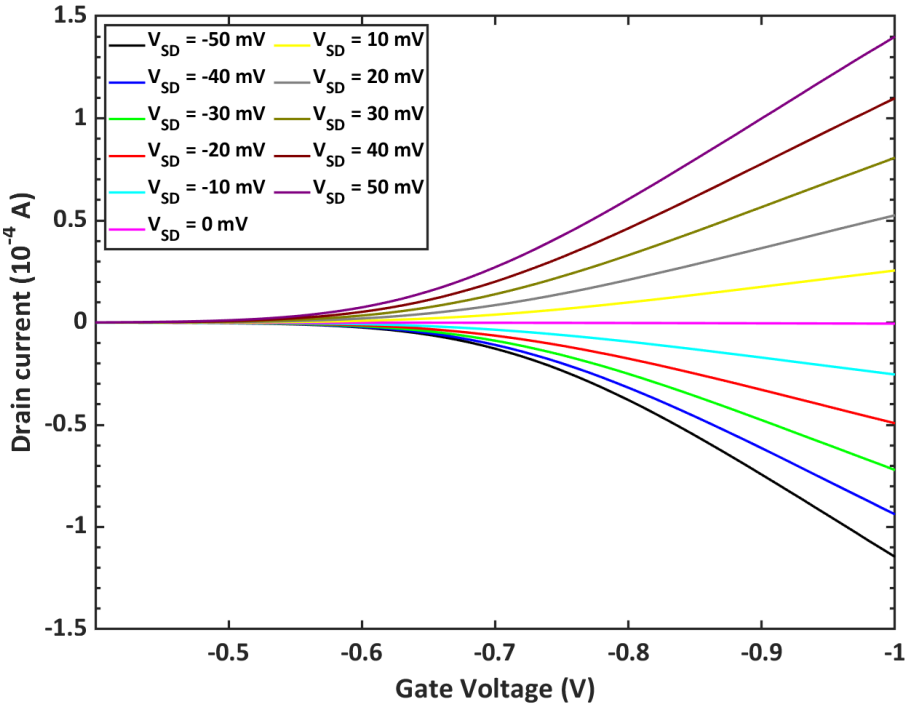

FIGURE 3.2: Diagram displaying SMU connections to device pads

Figure 3.3 shows the typical $I-V$ characteristics for a working Hitachi PMOS device with a gate length of 10 $\mu$m, width of 60 nm and oxide thickness of 2.4 nm. The transfer characteristic (Figure 3.3(a)) is required to demonstrate ideal MOSFET operation, meaning that it can be switched off ($I_{\mathrm{d}}$ at noise level for low $V_{\mathrm{g}}$), followed by an exponentially rising $I_{\mathrm{d}}$ as the channel is inverted. The output characteristics, as displayed in Figure 3.3(b), allows the $I_{\mathrm{d}}$ symmetry for positive/negative $V_{\mathrm{SD}}$ bias to

be gauged. The purpose of these measurements is to confirm that the device is fully working at room temperature, before investigating the samples for quantum transport at low temperatures which requires significant preparations.




(a) PMOS $I_d$-$V_g$ measurement between 0.5 V to -1 V for $V_{SD}$ = 50 mV and T = 295 K.




(b) PMOS $I_d$-$V_g$ characteristics for $V_{SD}$ = -50 mV to 50 mV at T = 295 K

FIGURE 3.3: Room temperature PMOS $I_d$-$V_g$ measurements using Cascade probe station.

## 3.3 Low temperature measurement systems

The measurement of samples at low temperatures (below 10 K) is crucial in order to resolve energy splittings and spin interactions which occur within an energy range far below the thermal activation at room temperature ($E << K_{\mathrm{B}}T$). Therefore the $I-V$ characteristics to study quantum transport must be undertaken using cryostats. This section briefly outlines the two cryostat systems used during this project, a LHe system and a cryogen-free based system, together with the necessary steps to achieve low temperatures and prepare the samples.

### 3.3.1 RIKEN Oxford Instruments LHe cryostat

The following section describes the cryostat system used as part of a 3-month collaboration with The Riken Institute, where the information detailed here is derived from the training and safety talks received, as well as from a guidebook on operating cryogenic instruments [61]. The cryostat employed throughout the stay at the Riken Institute was an Oxford Instruments 'wet system', meaning it used liquid helium (LHe), instead of helium gas, as the cooling substrate. This allowed the cyrostat to be cooled down much quicker, although the main trade off being that it is more expensive to maintain. Helium is the cooling substrate of choice owing to a very low latent heat of vaporisation, where only a very small amount of heat is required to evaporate it. However, helium gas has a very high enthalpy, meaning once gaseous it is difficult to warm up.

In order to sustain the low temperatures of below 4 K, LHe needed to be transferred from a vacuum insulated dewar to the cryostat bath twice a week via a transfer line known as a siphon. An insulated storage dewar is required to ensure it is thoroughly isolated from the room temperature surroundings. It is crucial to adjust the pressure within the storage dewar to set the helium transfer rate since a balance must be maintained for pressure both within the dewar and the cryostat bath. If it is too low, then the pressure will not be sufficient to initiate transfer and too high poses the risks of overfilling the cryostat as well as venting high pressure helium gas into the laboratory. The needle valve must also be closed during refilling stage to avoid ice build up, which also generates risk due to exposure to moisture that can block helium lines and cause valves to stick.

In a dynamic continuous flow cryostat such as this, the sample is in thermal contact with the helium vapour near the needle valve, where its temperature is greatly influenced by the vapour. The needle valve controls the flow of LHe into the sample space, where it is continuously fed into the refrigerator and pumped to a low pressure so that it cools. The cooling power is determined by the liquid flow rate and the size of the pump,

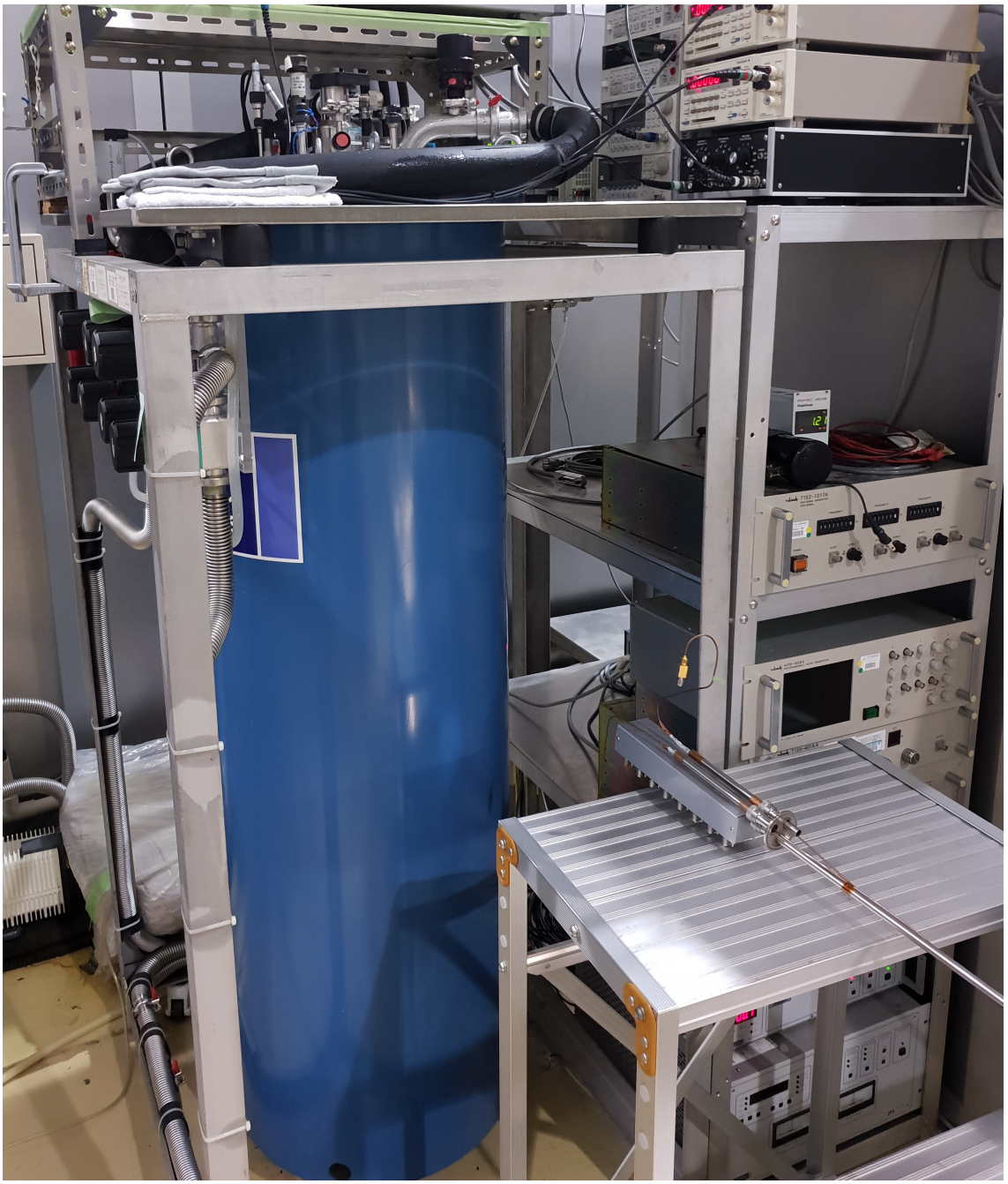


FIGURE 3.4: Oxford instruments LHe cryostat for low temperature measurements based at The RIKEN Institute.

which is adjusted via the needle valve. High flow rates are used at elevated temperatures to cool the system quickly or to obtain high cooling power, but when the base temperature is reached, the flow is reduced to make operation as economical as possible. The fluid temperature is controlled by passing it through a heat exchanger at the bottom of the sample space. The heat exchanger temperature is set by simultaneously controlling the LHe flow rate via the needle valve and the heater on the heat exchanger. The LHe flows over the sample and out of the exhaust port of the insert to the pump. This type of insert is easy to operate and allows samples to be replaced readily as well as providing

a fast response to the set temperature.

The superconducting magnet housed within the system is effectively a pure inductor with zero resistance. One of the main advantages of the superconducting magnet is the ability to operate in 'persistent mode'. In this type of operation, the superconducting circuit is closed to form a continuous loop, and the power supply can then be switched off, leaving the magnet at a fixed field, where the field then decays incredibly slowly. This is important, as the main purpose of the Riken collaboration is to investigate PSB which is a magnetic field dependant phenomenon, and therefore required high fields for sustained periods of time. The magnet will also only function properly if all the conductors remain in the superconducting state. If any part of the windings becomes resistive, the current passing through it will cause ohmic heating. This heating increases the size of the resistive zone and once the process has started, it is only possible to stop if the disturbance is very small. Otherwise, the resistive zone propagates rapidly through the whole of the coil and can spread into other parts of the magnet. All of the stored energy in the magnet becomes dissipated, which evaporates the LHe very quickly and often warms the magnet significantly above 4.2 K. This process is known as a quench. Therefore the magnet is usually fitted with a protection circuit to assist in the dissipation of energy and to prevent damage to the windings. The high voltage induced during the quench still occurs inside the magnet, but the electrical insulation is sufficient to withstand it.

### 3.3.2 Southampton Cryogenic CFMS

Southampton houses a Cryogenic CFMS which is able to achieve stable temperatures of 1.8 K, with the possibility of measuring below 300 mK using a $^3$He insert [60]. This system did require a considerable amount of repair and maintenance however in order to achieve consistent and stable low temperatures, which is detailed in the following section (Section 3.3.3). Since the physical principles associated with extracting heat were described in Section 2.2.4, here I will purely list the operating procedures behind the cryogen-free low temperature system.

The important sensory output for the cryostat, such as pressure and temperature, together with instruments such as heaters and valves are controlled through a LabVIEW program via an external computer. The measurement data is then obtained through BNC cables connected to a B1500A (as with the probe-station) which records the current whilst applying bias on each terminal for a given sample.

A cryostat which uses helium gas that is mechanically cooled are known as cryogen-free systems, this removes the issues associated with handling liquid cryogens and the additional costs. The basic principle of how low temperatures are achieved mechanically is by simply using a combination of pumps and compressors to extract heat during the condense/expand phases of the helium gas as described in the previous section. The Cryogenic CFM system operating procedure is outlined below.

- Helium gas is stored in a gas dump (see Figure 3.5) adjacent to the cryostat, this is connected to an oil free pump (to avoid contamination) which drives the circulation of the gas into the system through the gas inlet.
- Helium then passes through a charcoal filter which removes any impurities before entering the first stage of the G-M cryocooler, which reduces the gas temperature to 40 K.
- Second stage cooling then occurs where the gas is cooled further to below 4.2 K and condenses in the helium pot.
- The liquid helium then flows across the needle valve, after which Joule-Thomson expansion occurs and cools it further to approximately 1.8 K.
- It then travels through an annular tube around the sample chamber called the VTI heat exchanger (see Figure 3.5).
- Helium gas then flows through the coils to the VTI exchanger where it returns back to the pump, and finally, the helium dump, where a dial gauge allows the flow rate to be set and monitored.
- The sample is inside the sample chamber, isolated from the VTI cooling circuit but in thermal contact via static helium exchange gas and therefore reaches thermal equilibrium with the 1.8 K helium gas after a given time.

The heat exchanger at the bottom of the VTI is fitted with a temperature sensor and a heater, controlled using the external computer. The heater can then be used to adjust the temperature of the helium gas and therefore regulate the sample temperature. A sensor is located on the VSM sense coils to monitor the sample temperature, together with a small heater present on the sense coils for fine adjustment of the sample temperature. Readings from the thermometers on the heat exchanger and VSM sense coils are displayed as channels A and B on the temperature controller VI LabVIEW program. Another benefit of this system is that an airlock allows samples to be changed without contaminating the sample chamber, so the system can remain at low temperatures for a significant amount of time.

To achieve cooling below 1.8 K, a $^3$He insert is top-loaded into the VTI. The 1.5 cc of liquid $^3$He in the probe insert is able to maintain a temperature of 285 mK, due to $^3$He does not transition into a superlfuid like $^4$He so is able to condense using a sorption pump (mounted within the probe) to achieve lower temperatures. A magnetic field can also be applied using this cryostat, of up to 12 T.

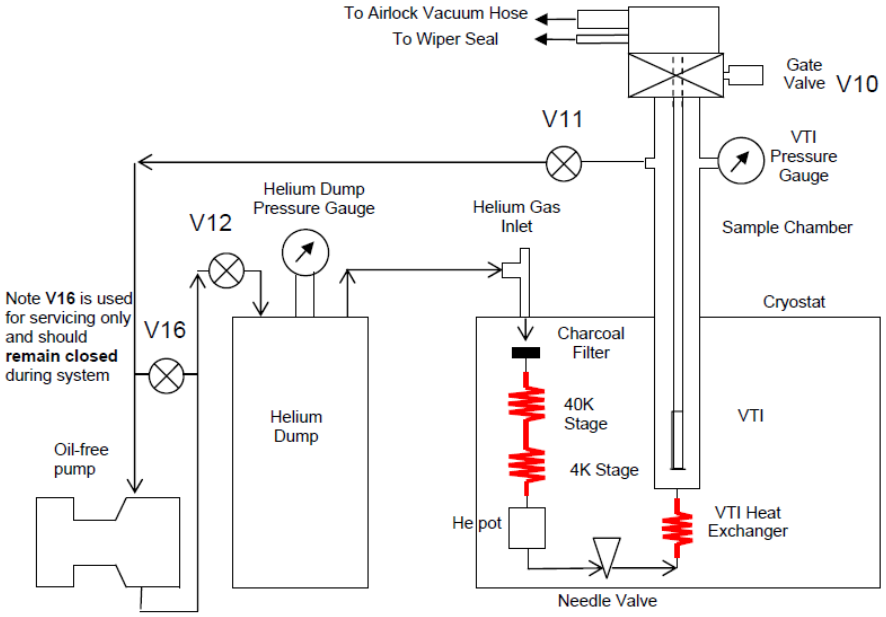



FIGURE 3.5: Schematic diagram showing the helium flow as well as the VTI cooling circuit within the Cryogenic cryostat [60].

### 3.3.3 CFMS repair

As briefly mentioned in Section 3.3.2, the Cryogenic system was not operational during the start of the project, with multiple issues rendering the initial cooldown, below 4 K cooldown and low-current measurements not possible as the result of four main issues, together with lack of maintenance. These issues were:

- Helium gas leakage from the input/output hoses between the compressor and the GM cryocooler, posing a danger to individuals within the lab as well as inadequate cooling
- Low signal-to-noise ratio from a 12-pin Fisher connector on the probe insert which required a junction box to convert to individual BNC lines.
- Scroll pump failure, which prohibits sustained pumping over several hours
- A Stiff needle valve with worn thread, which made fine tuning of the valve incredibly difficult

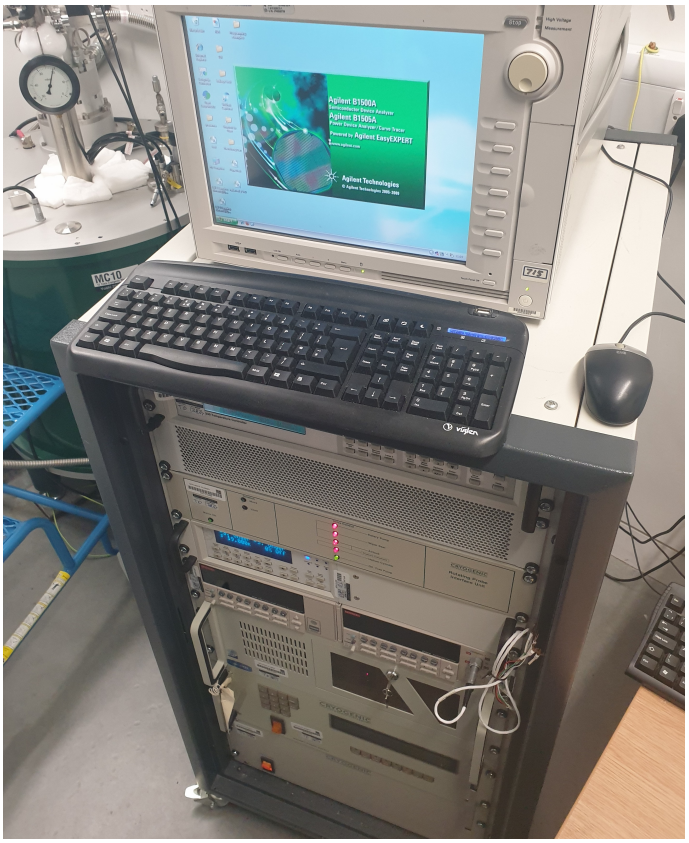



FIGURE 3.6: B1500 (top) and Cryogenic control system (rack).

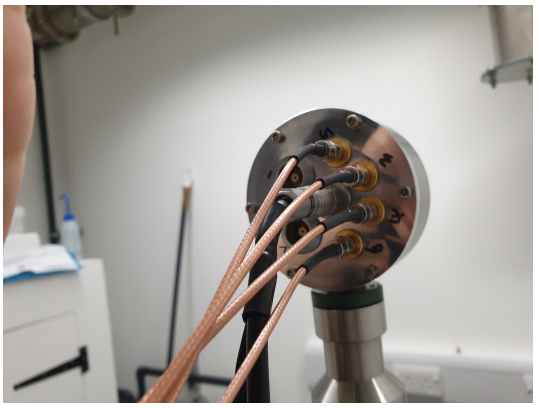
The first task in order to obtain a functioning cryostat was to replace the flexible helium gas hoses which transfer the high/low pressure helium gas from the dump, to the compressor and then finally onto GM cryocooler within the cryostat. When helium gas was detected on the exterior of the system, the use of leak detector allowed the discovery of several holes in the supply hoses. Helium leakage at the first stage of cooling within a confined room such as where the cryostat was housed is unacceptable, therefore both input/output lines were replaced.

Figure 3.7(a) displays the previous head wiring with A 12-pin Fisher connector as well as a connector for the thermometer and heater. The lines from the 12-pin connector demonstrated significant noise as well as poor performance for high-frequency signals. In addition, a junction box was needed to convert th 12-pin port to individual signal lines which added further noise. Such aspects interfered with the sensitive measurements needed for single charge and spin phenomena such as Coulomb-blockade and PSB. Therefore a new probe insert face was designed and constructed with 4 x SMA and 2 x triaxial ports, as shown inFigure 3.7(b). Using a dedicated SMA line for each device terminal, in contrast to a junction box previously, showed a much greater signal-to-noise ratio, with the added benefit of SMA being high-frequency compatible of up to 18 GHz.

After constructing and re-wiring a new probe head, the failing scroll pump was replaced. The noise during operation was likely a consequence of pump age, where the sounds were indicative of bearings failure (Figure 3.7(c)). The pump needed to be replaced or repaired. It was decided to buy a new nXDS vacuum pump from Edwards Vacuum, which had a comparable size (required for the custom helium lines) along with fulfilling the pumping specifications (Figure 3.7(d)). The final part to be replaced was the needle valve, where the increment gauge of the old valve is shown in Figure 3.7(e). The valve itself resembles a metal rod, with an increment guage on one end and the narrow valve at the other. Replacement was straightfoward and after completion the cryostat only required routine maintainence before preparing the system for cooling. The maintenace consisted of pumping down the vacuum sheild (recommended after the system is warmed to room temperature), cleaning of the VTI sample space and finally cleaning and applying vacuum grease to all o-rings to reduce contaminants and provide good seals.

In Figure 3.8 are graphs displaying the cool-down stages of the CFMS system, with the initial cool-down in Figure 3.8(a) to reach T = 190 K, the second stage once the scroll pump is activated to reach around 10 K in Figure 3.8(b), and finally when the needle valve is fine tuned to achieve the low-temperatures of 2 K in Figure 3.8(a). As a result of these endeavours, the ability to measure with low-noise and high frequency compatible SMA lines at a temperature of 2 K with 200 femto-ampere precision was acquired. The collaboration with the Advanced Device Laboratory at The RIKEN institute enabled the transfer of experience and practical knowledge to Southampton that aided in the repair and operation of the CFMS.

(a) Old Cryogenic sample insert with low signal-noise wiring.



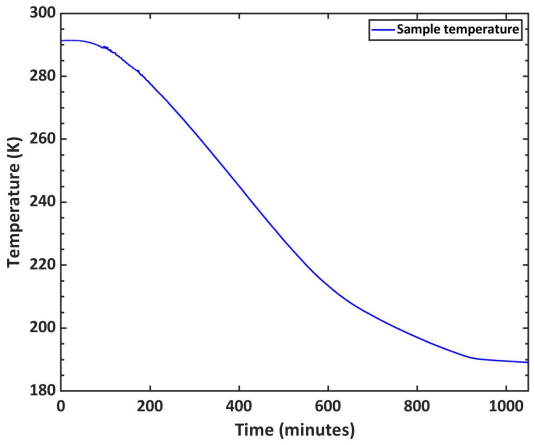
(b) Modified sample insert, with new SMA wiring for low-current and low-noise measurements.

(c) Failing scroll pump with worn out bearings.

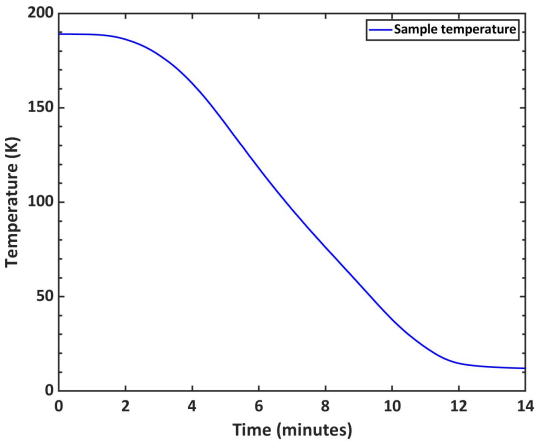
(d) New scroll pump fitted for continuos cryostat operation.

(e) Replacement of needle valve in order to reach stable temperatures below 4.2 K.

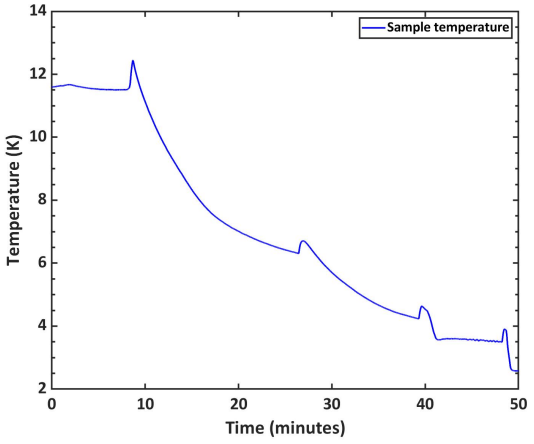
FIGURE 3.7: Modifications and component repair required in order to operate the Cryogenic cryostat.




(a) Initial cool-down (compressor only) from room temperature to 190 K.




(b) Second cool-down stage (scroll pump initiated) from 190 K to 10 K.




(c) Final cool-down stage (needle valve) from 10 K to 2 K.

FIGURE 3.8: Cryogenic cryostat cool-down stages.

## 3.4 Sample preparation

This section describes the process of sample preparation in order to be able to characterize devices at low-temperatures. The main two steps are wire-bonding and sample loading, both of which pose risks to device and cryostat operation if done incorrectly.

### 3.4.1 Wire-bonding

Once a working device has been identified which shows stable operation at room temperature using the probe-station, the first step is to wire bond the device terminals to the sample holder pads. Every sample holder is unique for a given cryostat system, however each posses the common traits of a mounting area where device sub-chips are glued, as well as gold, or highly conducting, pads in which wires are then bonded to. Sub-chips can be glued using conducting or insulating glue, depending on whether the wafer back

needed a ground connection, almost all devices bonded for this project used conductive glue.

Two different wire-bonders were utilised throughout the project, a West-Bond fully manual wire-bonder as displayed in Figure 3.9(a) and a Devotech semi-automatic wire-bonder as shown in Figure 3.9(b). The West-Bond system utilised during the Riken collaboration, where as at Southampton the Deveotech is employed. Both have their advantages, with a manual wire-bonder allowing more flexibility and generally, are easier to use, where as semi-automatic wire-bonders can facilitate mass bonding much more effectively. The main cause for concern is that of grounding. When a device is to be wire-bonded, an electrical connection is made between a pad on the sample holder and a terminal pad on the device. If the grounding is not properly checked, especially for devices harnessed in quantum applications, then there can be a small charge imbalance leading to trap generation, or worse, device damage. To avoid this, connections between any anti-static wrist band worn, the wire-bonder stage, bonding arm and sample holder were all made to be at the same potential.

In Figure 3.10 an image was taken of a sample post wire-bonding through the microscope lens where the whole sub-chip can be viewed. During the wire-bonding process, the user focuses the microscope onto the sample area which requires bonding, then a bond is made onto the sample holder pads (gold squares around the edge of the sub-chip). Immediately following this, the wire is uncoiled from within the arm as the bonding needle is moved to the device pad, where the other end of the wire is placed and the final bond is made. For the sample in Figure 3.10, two pMOS device with four terminals each are bonded, allowing two devices per sample load to be measured.

(a) West-Bond manual wire-binding system at the RIKEN institute.

(b) Devotech semi-automatic wire-bonding system at Southampton

FIGURE 3.9: Wire-bonding systems used for sample preparation at low temperatures.

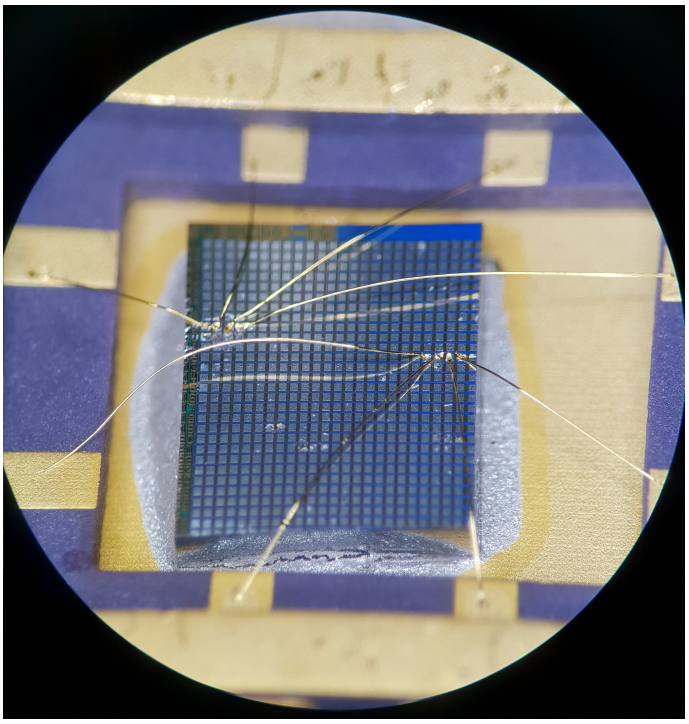


FIGURE 3.10: Microscope image (20x zoom) of two CMOS devices wire-bonded.

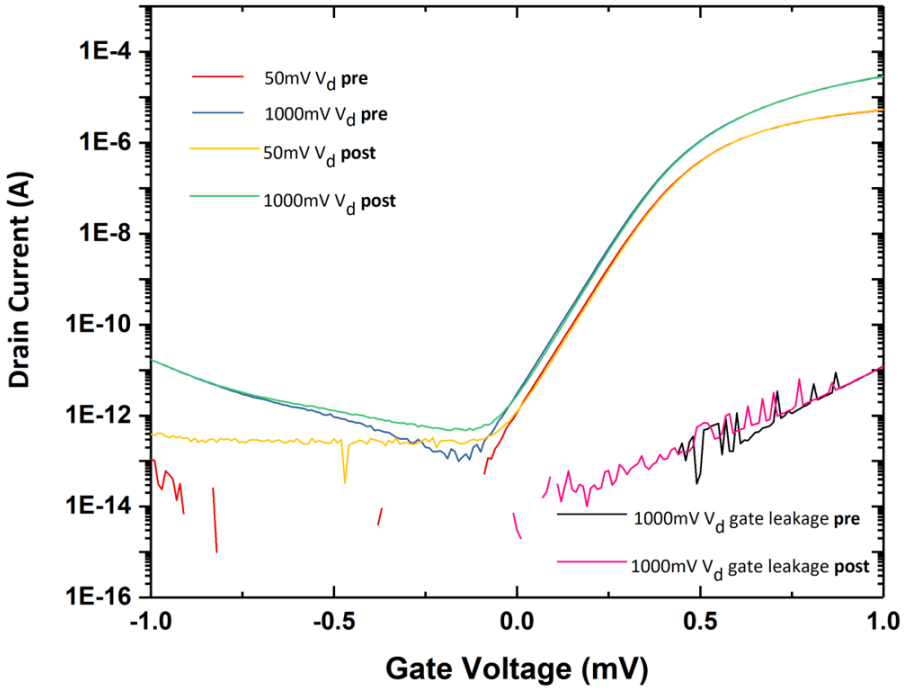



FIGURE 3.11: A comparison of pre and post wire-bonded samples to compare $I_{\mathrm{d}}$-$V_{\mathrm{g}}$ characteristics.

In order to characterise any effect wire-bonding has on device operation, a comparison is generated between the pre and post wire-bonding drain current and gate leakage of a pMOS sample, as shown in Figure 3.11. The results clearly establish that wire-bonding

produces negligible differences to the sample, although charge trapping in the gate leakage does give rise to some variability, however the subtle differences only appear in the pA range. As such, the technique employed when wire-bonding MOSFET samples can be concluded as successful.

### 3.4.2 Sample loading

The final procedure before low temperature characterisation can begin is that of loading the sample into the cryostat. Since both the cryostats employed probe inserts, the sample loading and removing procedure was very similar, however due to it's importance in avoiding system or device damage, an overview of the steps are described here.

In Figure 3.12(a) the sample end of the probe insert is displayed. After successfully wire-bonding a device, the sample holder is plugged into the copper chamber using tweezer while wearing an anti-static wristband, before sealing the chamber with a plate and wrapping in PTFE tape to reduce the amount of moisture within the chamber space. The connections to the probe face are then made to the source meters and current amplifiers at this point. To load the probe insert, the needle valve is closed and the pressure inside the cryostat sample space is first increased to approximately 1 atm. After removing the cap to the sample space and wearing cryogenic resistant gloves, the probe insert is carefully pushing into the cryostat, ensuring that pressure spikes to not occur from completing this action too quickly. Once fully submerged, the insert is locked in place and the needle valve is opened and the pressured decreased to reach the base temperatures of 1.6 K using this system.

(a) Sample insert for Oxford instruments cryostat at the RIKEN institute.

(b) Sample insert for Cryogenic cryostat at Southampton.

FIGURE 3.12: Comparison between different sample inserts for low temperature measurements.

Loading the sample into the CFMS cryostat at Southampton follows a very similar procedure, with the main difference being an interlock is used for a loading space, where

flushing occurs to remove contaminants and moisture before entering the low temperature sample space. Figure 3.12(b) displays the sample end of the probe stick, where the device and sample holder are exposed (uncovered) during characterisation in this system.

# Chapter 4

# Probing hole spin transport of disorder quantum dots via Pauli spin-blockade in standard silicon transistors

## 4.1 Introduction

This chapter describes the content of the publication in IOP Nanotechnology titled 'Probing hole spin transport of disorder quantum dots via Pauli spin-blockade in standard silicon transistors' by J. Hillier *etal* [136], as part of a collaboration with The Riken Institute in Tokyo, Japan. Additional data collected from the same device after remeasuring at The university of Southampton for the conference poster titled 'Single spin sensing in silicon p-type Metal-Oxide-Semiconductor Field-Effect Transistors' is also included [127]. In these works, the coupling and SO interaction of Si QDs are investigated via disorder based states present in p-type Si MOSFETs through PSB, achieved via tuning gate and well voltage to form a double-QD. This allowed the determination of $t_c$ and $l_{SO}$ which offers a direct measure of the SO interaction strength and therefore a method to evaluate the potential of a given system for electric-field mediated control, as well as high frequency spin manipulation. As a result, standard Si transistors can be taken advantage of to find enhanced SO effects by using disorder QDs at the oxide interface and obtain a $l_{SO}$ much shorter than anticipated using Si QDs.

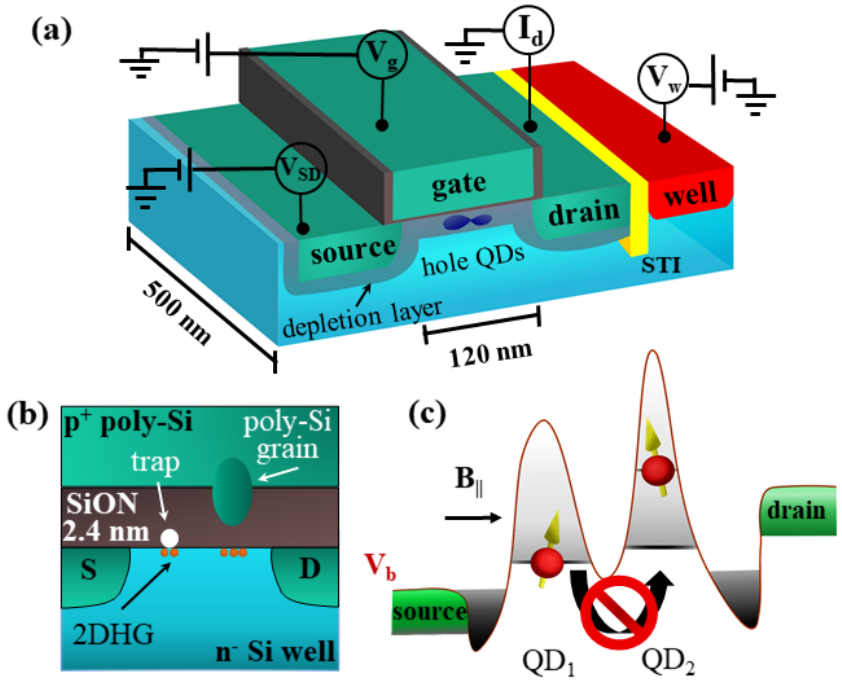



FIGURE 4.1: (a) Schematic of p-type Si MOSFET sample with channel dimensions 500 nm width and 120 nm length. (b) Cross-section of device displaying disorder at the Si-oxide interface leading to a 2DHG forming below defects. (c) Energy band diagram showing valance band bending which leads to double-QD formation and the conditions for PSB.

## 4.2 Device and methodology

A schematic of the Si p-type MOSFET sample measured is displayed in Figure 4.1.(a), with a 2.4 nm thick SiON gate dielectric and a highly doped poly-Si gate with a channel length/width of 120 nm and 500 nm respectively. As the channel becomes inverted a 2DHG begins to form and single charging characteristics from QDs can be observed due to quantum confinement. In such a device, this is a consequence of surface edge roughness by poly-Si grains in the gate, dopants, as well as traps at, or close to, the Si-oxide interface based on the charging properties observed, as depicted in Figure 4.1.(b) [78, 79, 88, 111]. All measurements here are carried out within the Oxford instruments $^4$He cryostat detailed in Chapter 3 Section 3.3.1 at a temperature of 1.6 K.

The method to electrically characterize QDs is via $I-V$ characteristics using Yokogawa source meters. This is achieved through biasing the gate ($V_g$) and source ($V_{SD}$) terminals while measuring current from a grounded drain terminal ($I_d$), to generate a CSD. A CSD not only allows information on the size and couplings of QDs to be calculated, but also the presence of multiple Coulomb-diamonds overlapping highlight double-QD transport features, a key requirement for PSB (Figure 5.1.(c)) in order to study SO effects. Here, a p-type MOSFET is used in particular to take advantage of the enhanced SO interaction of valance-band holes, owing to their p-orbital nature [26].

## 4.3 Investigating spin interactions of disorder states

### 4.3.1 Pauli spin-blockade via tuning the well

The resulting CSDs are displayed in Figure 4.2, where differential conductance ($dI_d/dV_{SD}$) is plotted to aid in highlighting finer features outside Coulomb-blockade, including excited states, and most importantly, to better visualize PSB. This method is more effective than plotting current, where the magnitude can vary as a result of offsets from both triplet leakage and parasitic current paths through the channel. The experimental data is plotted in Figure 4.2.(a)-(c), with simplified CSDs drawn in Figure 4.2.(d)-(f) to better visualize the significant changes. Coulomb-blockade appears as blue in Figure 4.2.(a)-(c), with red denoting high $dI_d/dV_{SD}$ due to the availability of levels for single hole transport. Amplifier current saturation occurred at 1.3 nA producing blue regions at high $V_g$ and $V_{SD}$. Each Coulomb-diamond, corresponding to blockaded transport within the QD system, are marked by a letter and number in Figure 4.2.(d)-(f).
A well voltage ($V_w$) of 1 V is applied in Figure 4.2.(d), and a series of largely closed Coulomb-diamonds are observed. This suggests that transport is occurring through a single QD, where the Coulomb-diamonds A1-C1 are deduced from $QD_2$, and Coulomb-diamond D1 from $QD_1$. The energy band diagram depicting this situation is shown in Figure 4.2.(g) for the region marked by the star in Figure 4.2.(d). Due to the small size of the Coulomb-diamonds B1 and C1 in Figure 4.2.(d), single QD transport can occur as a consequence of a reduction in tunneling barrier distance between the source and drain due to the larger QD size, shown schematically in the valence band diagram in 4.2.(g).

When $V_w = 2$ V in Figure 4.2.(b) the CSD changes significantly from the shift and overlap of Coulomb-diamonds, in particular the appearance of a low $dI_d/dV_{SD}$ region can be noted, enclosed by the red dotted line outside of the Coulomb-diamond B2 for positive $V_{SD}$ in Figure 4.2.(e). This can be interpreted as an initial indicator of PSB, since the transport path will not be completed blockaded due to a slightly elevated $I_d$ from triplet leakage that leads to a non-zero, low $dI_d/dV_{SD}$. The optimum contrast is at a threshold of 0.05-0.1 nS to make the PSB region most visible. Coulomb-blockade of the dominant transport path also expands considerably between Figure 4.2.(a)-(b), from the enhanced confinement of the smaller Coulomb-diamonds observed in Figure 4.2.(d) as a result of the large scale changes. $QD_1$ emerges from a partially joined potential profile in Figure 4.2.(g)-(h) which separates due to the application well voltage forming a tunnelling barrier between the QDs as well as increasing the confinement of $QD_2$. The valance band schematic given in Figure 4.2.(h) during PSB highlights the important changes leading to this result, such as the formation of a weakly coupled double QD through a modified tunneling barrier between them. The number of confined holes in each QD also now satisfies the conditions of PSB, due to the spin selective nature of the

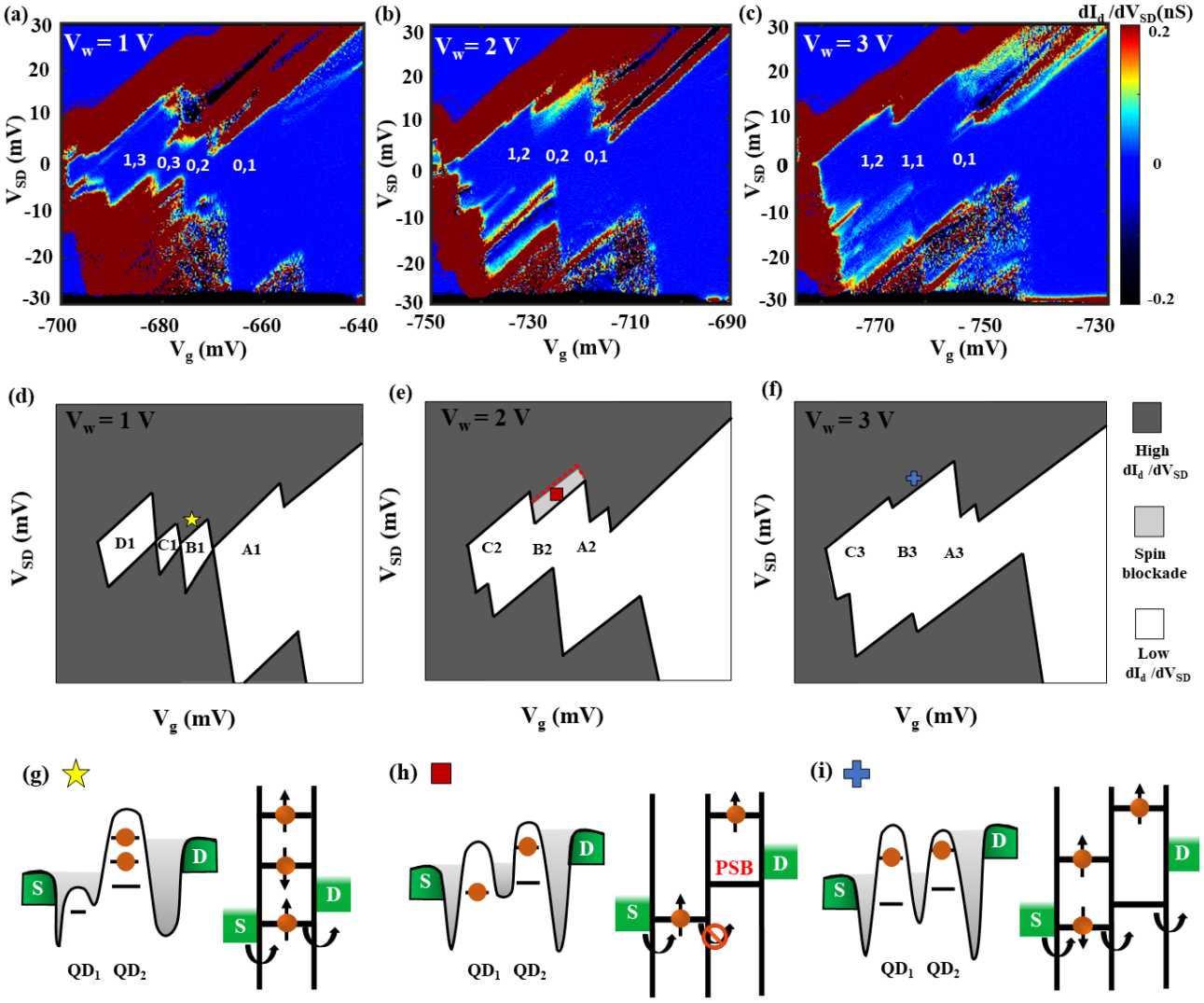



FIGURE 4.2: CSDs for $V_{SD}$ = -30 to 30 mV over a 60 mV gate voltage ($V_g$) range at different well voltages ($V_w$). Within the Coulomb-diamonds the number of confined holes in each QD ($QD_1$, $QD_2$) are labelled. (a) $V_w$ = 1 V, a row of single Coulomb-diamonds appear with various charging energies. (b) $V_w$ = 2 V, the alignment of the QD energy levels change, resulting in overlapping of the Coulomb-diamonds which strongly suggests double-QD transport. (c) $V_w$ = 3 V, the alignment of the Coulomb-diamonds is further altered, leading to regions of extended Coulomb blockade. The confinement of an additional hole within the dominant transport path is marked by letters A, B, C and D in simplified CSDs (d)-(f), where the number refers to the $V_w$ magnitude, however the same letter does not necessarily denote the same QD energy level in each CSD. The appearance of a PSB like low $dI_d/dV_{SD}$ region at the edge of B2 for positive $V_{SD}$ is annotated in (e), where the absence is noted at the edge of B3 in (f) from a change in coupling between the confined levels. (g)-(i) show energy band diagrams marked by the star, square and cross in (d)-(f) respectively. At $V_w$ = 1 V the transport is assumed to occur largely through a single QD, upon increasing $V_w$ to 2 V the confinement changes (from larger Coulomb-diamonds), together with the QDs becoming weakly coupled and form a double QD exhibiting PSB. When $V_w$ = 3 V the energy level alignment shifts between the double QD, removing PSB and allowing transport to occur.

TABLE 4.1: Single hole charging properties of Coulomb-diamonds as labelled in Figure 5.2.

| $V_w(V)$ | Coulomb-diamond (No.) | $E_c$(meV) | $C_g$(aF) |
|---|---|---|---|
| 1 | A1 | 13.3 | 10.4 |
| 1 | B1 | 6.3 | 24.6 |
| 1 | C1 | 5.5 | 28.6 |
| 1 | D1 | 12.5 | 11.8 |
| 2 | A2 | 8.9 | 13.3 |
| 2 | B2 | 16.1 | 9.8 |
| 2 | C2 | 12.7 | 10.4 |
| 3 | A3 | 10.3 | 11.7 |
| 3 | B3 | 19.8 | 7.2 |
| 3 | C3 | 12.1 | 11.1 |

second hole entering $QD_2$. Therefore a combination of both the appropriate number of confined holes and the extended region of low $dI_d/dV_{SD}$ strongly suggests PSB. Upon increasing $V_w$ further to 3 V in Figure 4.2.(c) the CSD pattern, and therefore the dominate transport path, largely resembles that of Figure 4.2.(b) with the exception of the B2, which displays an extended Coulomb-blockade and the absence of the unique low $dI_d/dV_{SD}$ feature highlighted previously when comparing Figure 4.2.(e) and (f). This can be explained by the energy band diagram and valance band schematic in Figure 4.2.(i) for the cross in Figure 4.2.(f). The energy level alignment shifts, allowing hole transport through the second level in both QDs.

Along with changes to tunneling barriers and QD energy level alignment at higher $V_w$ values, a considerable threshold shift is also evident. This is explained by an increasing depletion layer width causing more positively charged ionized dopants to be exposed, and therefore requires a more negative gate voltage to compensate to achieve the same 2DHG formation.

Upon further analysis, the physical attributes of the dominant transport path are determined through estimating the dimensions of charge stable regions in Figure 4.2 for positive $V_{SD}$. This is achieved by calculating $C_g$ and $E_c$ according to $E_c = \frac{e^2}{C_\Sigma}$ and $C_g = \frac{e}{\Delta V_g}$ [86], where $e$ and $C_\Sigma$ are elementary charge and total capacitance respectively, as summarised in Table 4.1. $E_c$ represents the energy required to add an additional hole to the QD and $C_g$ is associated with the strength of the coupling between a given confined level and the gate. Determining such values allows a greater understanding of the systems components and their relationship with respect to $V_w$. Since Si dangling bonds have charging energies of 13 meV above the valence band the proposed origin of the confined levels where $E_c$ is close to 13 meV are likey due to dangling bonds or trap sites at the oxide interface [149]. Coulomb-diamonds with $E_c$ values less than this (such as B1 and C1) are assumed be generated by fine poly-Si grains. The QD diameter, $d_{QD}$, can be estimated from $S_{QD}$ and $t_{eff}$ by $d_{QD} = \sqrt{4S_{QD}/\pi}$, using $S_{QD} = C_g/C_{eff}$ and

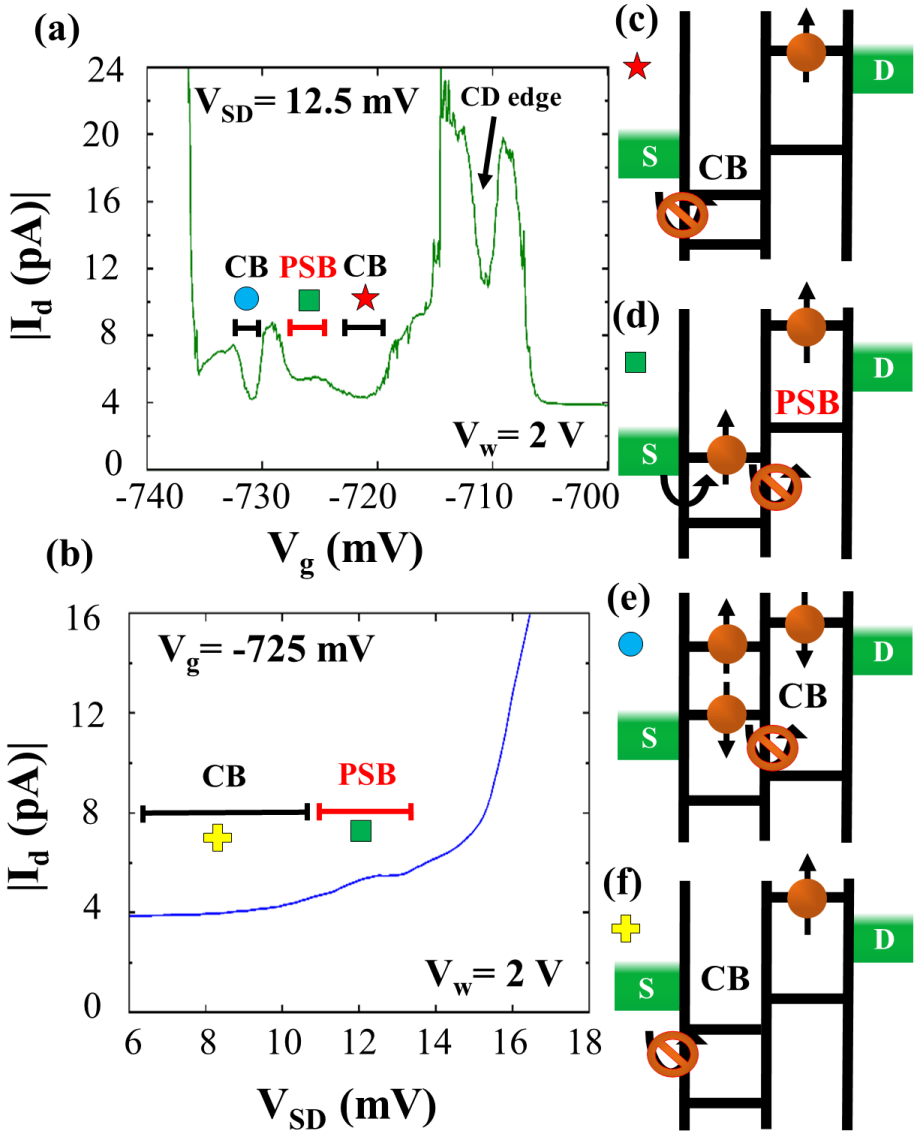



FIGURE 4.3: For $V_w$ fixed at 2 V, a gate sweep with $V_{SD}$ = 12.5 mV is shown in (a), and a source sweep with $V_g$ = -725 mV is displayed in (b). Coulomb-blockade, as well as the suspected PSB region from low $dI_d/dV_{SD}$ are labelled. (c)-(e) show energy band diagrams marked by the star, square and circle in (a), for the Coulomb-blockade regions as well as PSB. In (f), an energy band diagram for Coulomb-blockade conditions marked by the cross in (b) is displayed, where PSB then occurs at higher $V_{SD}$.

$C_{eff} = \epsilon_{ox}/t_{eff}$, where $\epsilon_{ox}$ is the permittivity of the oxide. Given this, the projected $d_{QD}$ of the smaller Coulomb-diamonds B1 and C1 in Figure 4.2.(a) is calculated to be $\approx$ 50 nm. This further supports poly-Si grains as the confining potential origin given that fine poly-Si grain structures reach diameters of the order 50 nm [99]. Although the CSD pattern is similar when comparing Figure 4.2.(b) and (c), the highlighted region in Figure 4.2.(e) disappeared when $V_w$ = 3 V. As shown schematically in Figure 4.2.(h), the specific transport path in Figure 4.2.(b) is no longer available in Figure 4.2.(c). Such changes which lead to increases in $E_c$ and $C_g$ further demonstrate that the response of each confined level varied according to $V_w$, where the energy level alignment between

the QDs shifted, together with the barrier height between them. This is also likely attributable to QD origin, since each QD will have a different capacitive coupling to $V_w$, as with $V_g$, depending on the location and size of the QD as the depletion layer changes [87]. The formation of $QD_2$, as the likely product of a poly-Si grain, appears to be more susceptible to $V_w$ from the enlargement of Coulomb-diamond B1 to B2 which is ascribed to the same origin, in comparison to the change of Coulomb-diamond D1 to C2 of $QD_1$ from what is likely an interface trap given the $E_c$. In Figure 4.2.(c) dopants may also be a likely candidate for QD origin due to $E_c$ values reaching 20 meV for B3.

### 4.3.2 Enhanced triplet leakage due to magnetic-fields

Focusing on the low $dI_d/dV_{SD}$ region in Figure 4.2.(e), a $V_g$ and $V_{SD}$ sweep at fixed $V_w$ = 2 V is shown in Figure 4.3.(a) and (b) respectively. The $I_d$ valleys in Figure 4.3 denote Coulomb-blockade, whereas the marginally elevated $I_d$ plateaus correspond to PSB. A dip in current at $V_g$ = -710 mV signifies the profile sweep nearing a Coulomb-diamond edge, although the system does not enter Coulomb-blockade. Figures 4.3.(c)-(f) show energy band diagrams for the regions labelled by the star, square, circle and cross in Figures 4.3.(a) and (b). These visually demonstrate how the transport scheme is altered through the application of $V_g$ and $V_{SD}$. For the star marked in Figure 4.3.(a), an energy band diagram in Figure 4.3.(c) shows the system entering Coulomb-blockade due to the absence of a level for the first QD. In Figure 4.3.(d), at larger $V_g$ a level becomes available, but transport is blocked between the QDs due to Pauli selection rules. PSB is temporarily lifted at higher $V_g$ due to the lowering of a level for $QD_1$ within the transport window, however Coulomb-blockade then occurs as displayed in Figure 4.3.(e) due to a level dropping above the drain for $QD_2$ (circle). An energy band diagram is also given for the Coulomb-blockade region preceding PSB at lower $V_{SD}$ (cross) in Figure 4.3.(f). While an $I_d$ leakage current of 4 pA is observed in the Coulomb-blockade region due to parasitic current paths in the channel, an $I_d$ of 5.6 pA within the PSB region suggests the triplet leakage is 1.6 pA, which is comparable to similar devices exhibiting PSB [90, 91, 95].

Further to the $I_d$ leakage measurements suggesting that the system is in a PSB configuration, much more tangible evidence can be obtained by investigating the magnetic field dependence, offering a window into the prevailing mechanism and any resulting spin related phenomena. Figure 4.4 shows a higher resolution CSD generated to identify the PSB region clearly. The area within the white dashed-circle in Figure 4.4 is examined and a magnetic field parallel to the channel is applied to investigate spin transport relating to PSB, where a parallel field is applied to the channel to minimize orbital effects [101]. Figure 4.5.(a) shows $I_d$ as a function of B-field from -2 T to 2 T for $V_g$ = -715

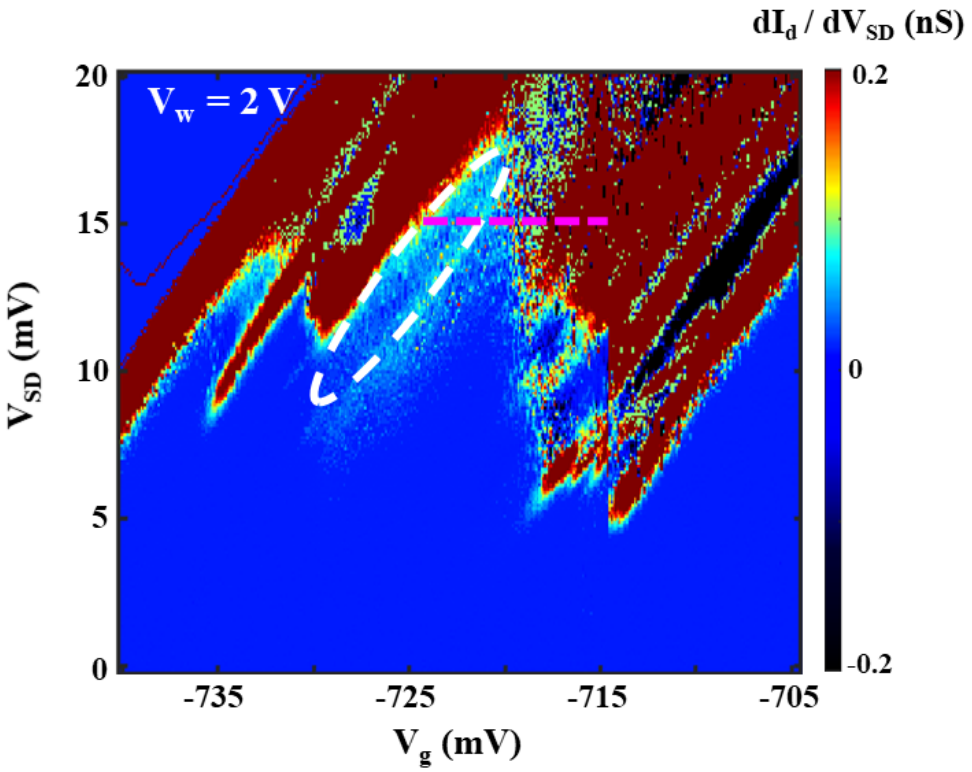



FIGURE 4.4: CSD for $V_{\mathrm{SD}}$ = 0 to 20 mV and $V_{\mathrm{g}}$ = -705 to -740 mV with $V_{\mathrm{w}}$ = 2 V at the edge of a Coulomb diamond (white dash semi-circle), where a reduction in current is observed due to blockaded transport through a double-QDs.

mV to -725 mV along the pink dashed line in Figure 4.4. Two peaks become visible at ± 0.5 T due to an elevation in $I_{\mathrm{d}}$ from around 10 pA to 15 pA. A higher resolution B-field sweep from 0 to 1 T is displayed in Figure 4.5.(b). Here the $I_{\mathrm{d}}$ peak centred around 0.5 T can be observed to extend over a $V_g$ region of approximately -723.5 mV to -727.5 mV (marked by red arrow), which closely matches the voltage space dimensions of the low $dI_{\mathrm{d}}/dV_{\mathrm{SD}}$ in Figure 4.4. As described in Section 2.1.2 the resulting magnetic field dependant peaks appear due to different relaxation processes competing with each other. In Figure 4.5.(c)-(d) energy level diagrams are displayed, where the singlet and triplet states are represented by S and T respectively, and ($N_{\mathrm{QD}_1}$,$N_{\mathrm{QD}_2}$) refers to the number of holes in the highest occupied orbitals of $\mathrm{QD}_1$ and $\mathrm{QD}_2$. In the absence of a magnetic field only the S(1,1) state can provide a direct route to S(0,2) which are tunnel coupled by $t_c$, and PSB occurs if the system enters the T(1,1) state (Figure 4.5.(c)). The blocked T(1,1) states with parallel spins can be lifted however by both relaxation to the S(1,1) state and S(0,2) through mixing on account of the SO interaction introducing non spin-conserving tunnelling between the QDs. When a magnetic field is applied the blocked triplet states are split by the Zeeman energy which effectively alters the relaxation rate by providing faster alternative routes between the T(1,1) and S(0,2) mixed states and leads to an increase in $I_d$ leakage (Figure 4.5.(d)).

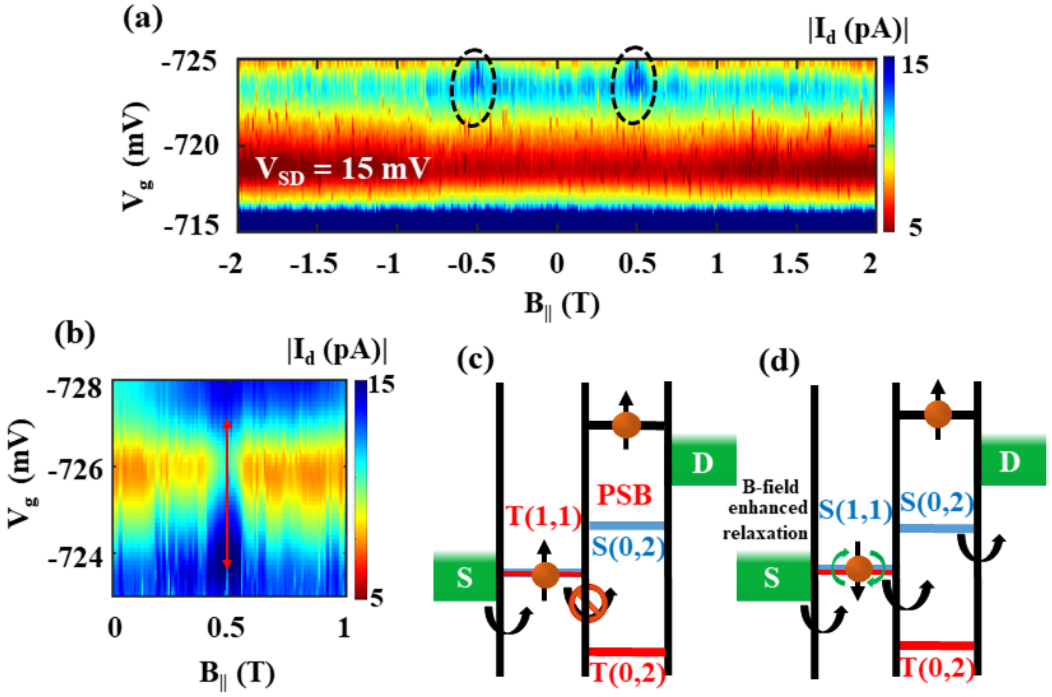



FIGURE 4.5: (a) Current as a function of magnetic field in the PSB region at fixed $V_{SD}$ = 15 mV between $V_g$ = -715 to -725 mV (pink dashed line in (a)), two peaks are present due to an increase in the PSB leakage current at 0.5 T. (b) High resolution magnetic field spectroscopy scan with a clearly identifiable peak, where the extent of the maximum magnetic field enhanced spin relaxation current with respect to $V_g$ is indicated by the red arrow. (c) Energy level diagrams for PSB occurring in a double QD, where the path to S(0,2) is blocked due to parallel spins in each QD, and (d) where the blockade is partially lifted due to enhanced relaxation from S-T mixing when a finite magnetic field is applied.

The enhanced leakage current effect may be directly observed through magnetic field sweeps of individual points within the PSB region, where the outcome of these measurements are displayed in Figure 4.6 in the form of leakage current peaks at ± 0.5 T. The magnetic field is swept form -1 T to 1 T while $V_{SD}$ is fixed to 15 mV, with $V_g$ values of -723 mV, -723.5, -724 mV and -725 mV in Figure 4.6 (a)-(d) respectively. These profiles demonstrate the sensitivity of the PSB region via the narrow window for maximum S-T mixing. From studying the peaks highlighted in Figure 4.6, the minimum increase in the leakage current occurred for $V_g$ = -723 mV (around 2 pA), in contrast to a when $V_g$ = -724 mV, yielding an almost 5 pA increase relative to the offset. The most apparent feature however is the spike noise plaguing the entire sweep in Figure 4.6 (a) and (b), a consequence of short lifetime charge traps charging and then discharging. In Figure 4.6 (c) and (d) there is evidence of longer lifetime single hole trapping from the appearance of RTS. Such artefacts, in combination with parasitic offsets of 8-12 pA through the channel, impose difficulties when performing analysis of the peak structure to gain insight on the SO interaction. Therefore, in Section 4.3.4, Figure 4.6 (c) is processed to

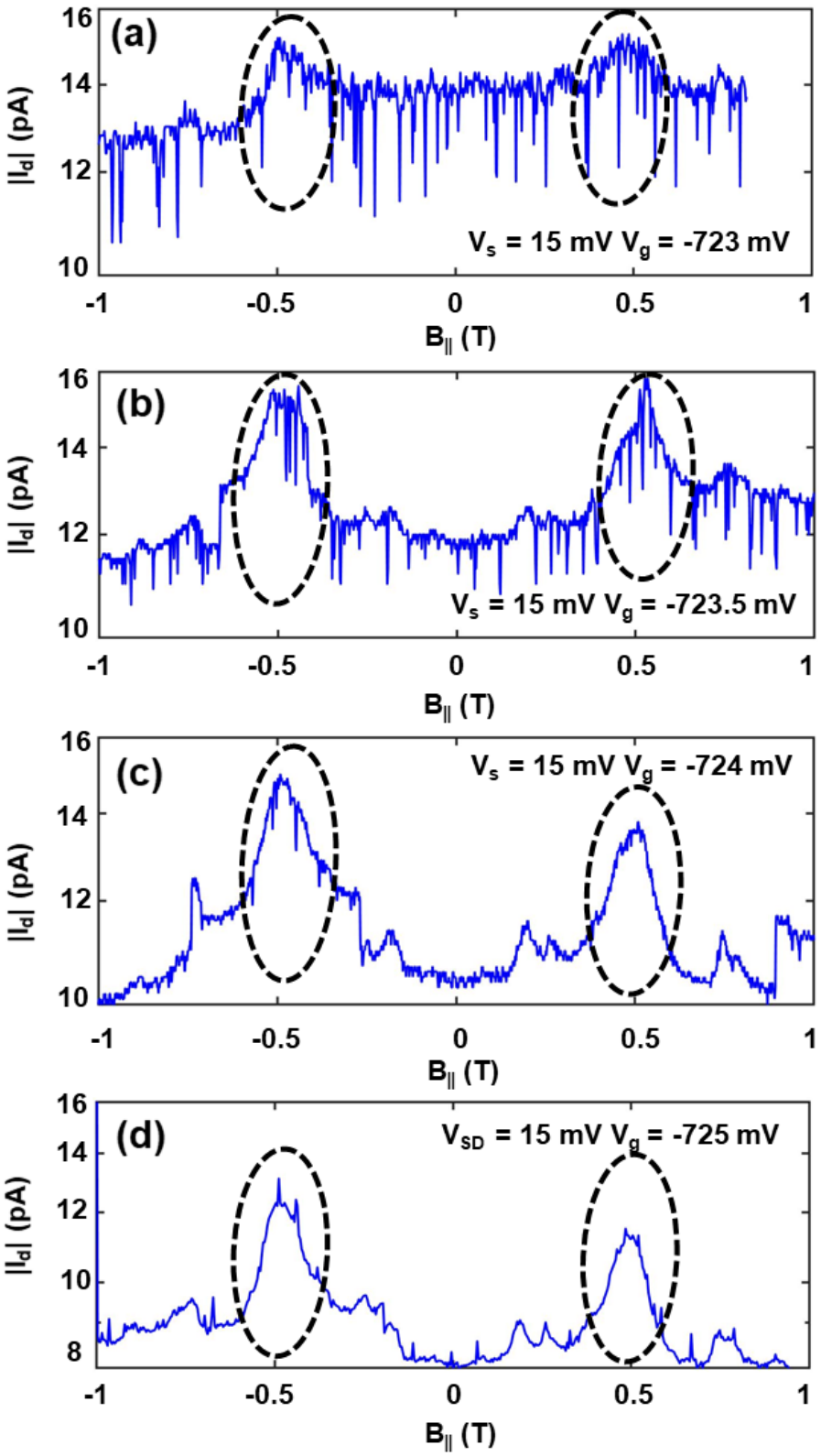



FIGURE 4.6: (a)-(d) Profile plots showing the magnetic field dependant leakage current (blue) of a single point centered within the PSB region at a $V_{SD}$ of 15 mV and $V_g$ = -723 mV, -723.5 mV, -724 mV and -725 mV. Peaks begin to appear at ±0.5 T where a total leakage current of around 15 pA is observed.

remove the parasitic offset and any significant trapping to allow a model to be applied in order to investigate SO interaction strength by calculating $t_c$ and $l_{SO}$.

### 4.3.3 CSDs at fixed magnetic-fields

So far, the measurement data considered within this chapter was acquired at The Riken institute in Japan. In view of the sample still being operational on return to Southampton, the device was prepared for low-temperature measurement and re-wire-bonded for further characterisation. This is to study the stability and reproducibility of PSB by replicating the CSD parameters set during the Riken collaboration, in addition to new $V_w$ - $V_g$ CSDs at fixed magnetic fields. These new types $V_w$ CSD, with $V_{SD}$ fixed to 15 mV, are displayed in Figure 4.7 for fixed fields of 0 T and 0.4 T in (a) and (b) respectively. Coulomb-blockade appears as blue, with excited states in dark red. One important difference when generating a plot in $V_w$ voltage space is the evolution of states since this type of CSD displays the impact of $V_w$ on the transport properties and therefore the coupling of QDs to either $V_w$ or $V_g$ can be directly observed from the gradient.

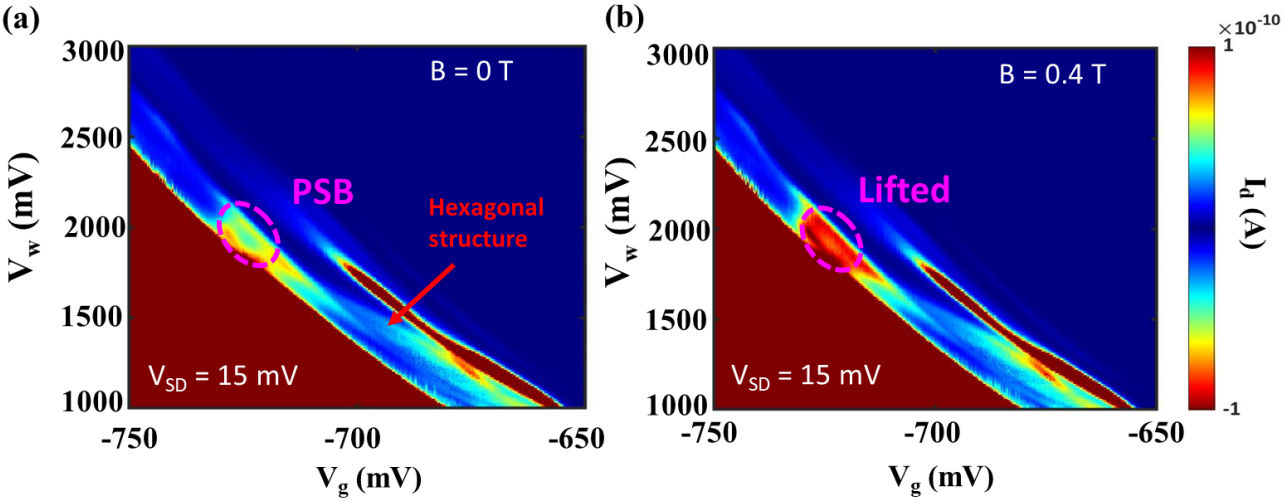



FIGURE 4.7: (a) CSDs generated by sweeping the $V_w$ and $V_g$ to identify coupled QD transport. (b) Identical parameters to (a) but with a static B = 0.4 T applied, where triplet leakage is maximized when T = 2 K.

From such CSDs in Figure 4.8 a honey-comb like pattern emerges at the PSB site and nearby, as identified in both plots. A hexagonal structure away from PSB is also highlighted in Figure 4.8 (a) providing further proof of a coupling between states originating from a double-QD. PSB can be easily discovered via the magnetic field dependant behaviour, providing an interesting artefact from which the size in voltage space PSB is present. As described in the previous section, at a certain field (B = 0.4 T in Figure 4.7 (b)) the area outlined appeared darker red due to increased triplet leakage in PSB region.

Strangely, the magnetic field required for peak leakage current demonstrated variation, shifting to 0.4 T in comparison to 0.5 T for the Riken data. This is believed to be a result of either the temperature difference (1.6 K at Riken, vs 2 K at Southampton) or a slight change in the charging properties (and therefore coupling) of the double-QD as a result of nearby trapping or condition of the QDs.

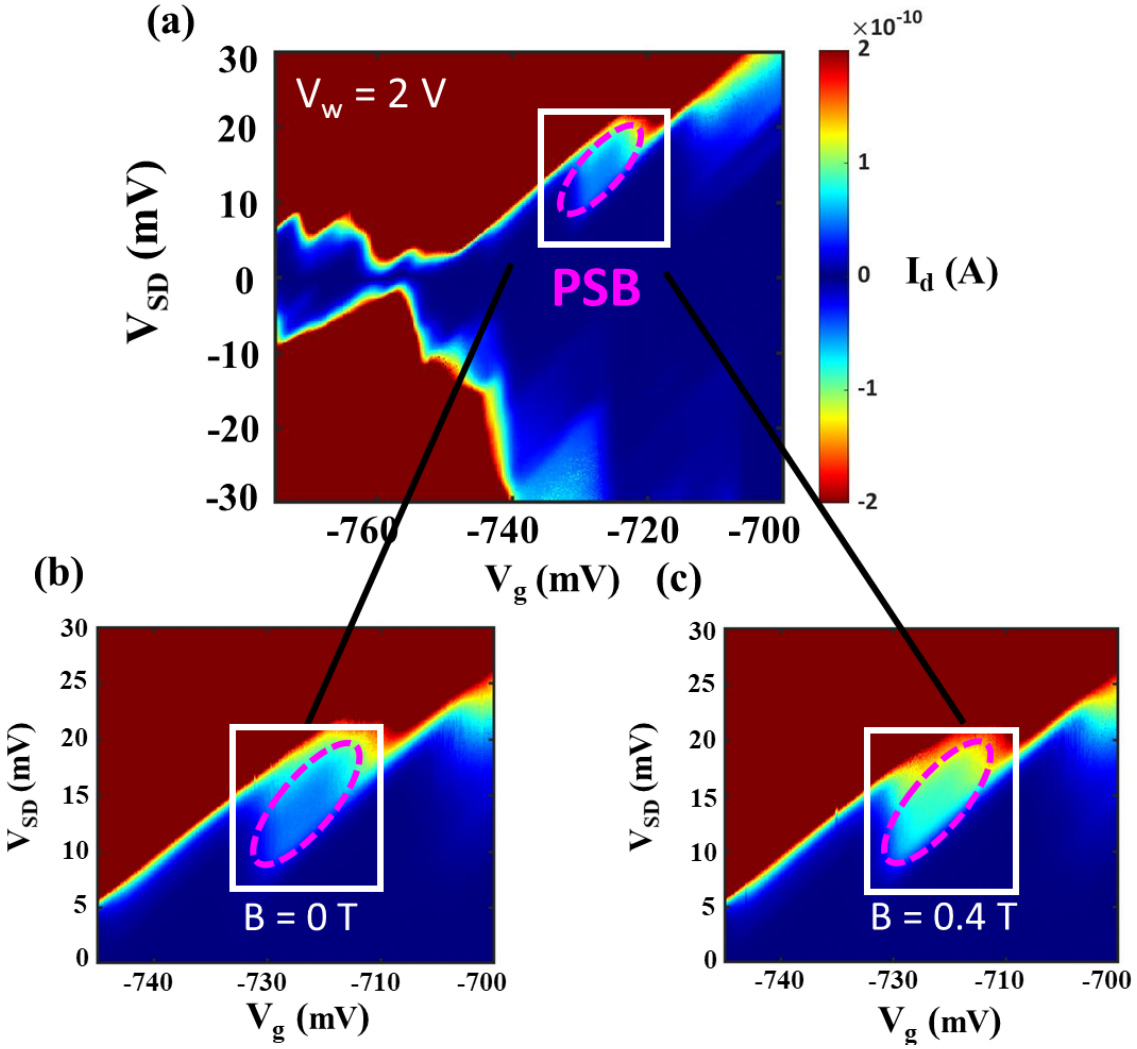



FIGURE 4.8: (a) CSDs with $V_w$ fixed at 2 V to observe PSB double QD conditions from Figure 4.7. An enhanced image is shown of PSB at B = 0 T (b) and B = 0.4 T (c) where it is partially lifted at T = 2 K.

An additional CSD covering the same voltage space of Figure 4.6 is generated and displayed in Figure 4.8 (a). This plot bears a great deal of resemblance to Figure 5.2 (b) and Figure 4.6 aside from a more diffuse Colomb-diamond pattern as a product of an elevated temperature and increased noise of the measurement equipment. This is not a trivial matter, given the sensitive nature of various trap states that must exist within the device, together with further sample preparation which subjects the device to various stresses (electrical and physical). Consequently, Figure 4.8 (a) provides evidence that PSB remained and in at the same location between the Coulomb-diamonds.

From Figure 4.8, further CSDs zoomed in on the PSB region created, as highlighted in Figure 4.8 (b) and (c). A light blue of what can be described as a PSB-diamond, from the small amount of zero-field triplet leakage, is visible in Figure 4.8 (b), in contrast to Figure 4.8 (b) with the maximum magnetic-field enhanced relaxation, where this structure is absent. The dimensions of this spin-selective feature represents the extent at which the coupling exists for the double-QD in voltage space before an additional state becomes available, within either QD or nearby trap, and hence PSB is no longer held. As a product of this investigation, the sample demonstrated its robustness, from not only reproducibility after thermal cycles but also when using different measurement equipment along with the need for further preparation such as wire-bonding and sample loading.

### 4.3.4 Spin-orbit strength and tunnel coupling determination

The model described in [89] can also be applied to the data measured at Riken. This was accomplished via the shape and magnitude of the double-peak triplet-leakage during the application of a magnetic-field, so the SO coupling and $t_c$ can be calculated. The enhanced relaxation rate is mediated by the SO coupling and proportional to $\alpha B$. As a consequence, this leads to significant changes when the enhanced leakage becomes comparable to $\Gamma_{rel}$, and therefore a noticeable change in leakage $I_\mathrm{d}$ due to the lifting of PSB becomes apparent. The equation derived in [89] to describe the leakage $I_\mathrm{d}$ is given by 4.1.

$$I_\mathrm{d}(B) = \Gamma_{rel}\frac{[\omega - B^2 + \tau^2][\omega(1+4\gamma) + B^2 - \tau^2]}{6\gamma\omega^2 + 2\mathrm{B}^2\alpha^2\mathrm{t}_\mathrm{c}^2} \tag{4.1}$$

Here, $\omega = \sqrt{(B^2-\tau^2)^2 + 8B^2\alpha^2t_c^2}$, $\gamma = \Gamma_{rel}/\Gamma$ and $\tau = t_c\sqrt{1+3\alpha^2}$ which is the total coupling energy.

To convert an applied magnetic field to the energy splitting; the Zeeman energy is calculated via $\Delta E_\mathrm{z} = g\mu_\mathrm{b}B_\parallel$, where $\mu_\mathrm{b}$ is the Bohr magnetron and $g$ is the gyro-magnetic ratio which is assumed to be $\approx 2$. This theory is applied in the form of fitting (red) to the data in Figure 4.9, where a single point centered around the site of PSB at $V_\mathrm{g}$ = -724 mV is plotted. A - field dip can be noted, together with two clear leakage $I_\mathrm{d}$ peaks at $\pm$ 0.5 T with a magnitude of around 5 pA. As discussed earlier a parasitic current path elsewhere through the channel led to an additional current measured within Coulomb-blockade, therefore this offset is subtracted, as well as the current from an isolated charge trap event, to produce a PSB leakage current of around 1.6 pA at zero-field. With the combination of the known splitting energy and equation (1), a $t_c$ value of 57 $\mu eV$ is extracted from the data, which is in good agreement for gate defined silicon QDs

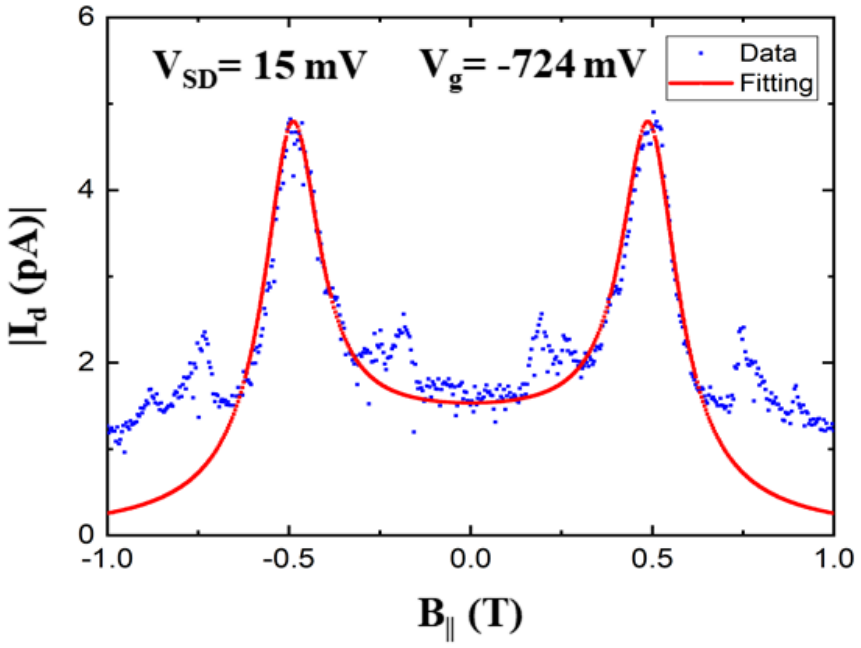



FIGURE 4.9: A profile plot showing the magnetic field dependant leakage current (blue) of a single point centered within the PSB region at a $V_{SD}$ of 15 mV and $V_g$ = -724 mV. Peaks begin to appear at ±0.5 T where a leakage current of around 5 pA is observed. Using equation 4.1 a fitting is applied to the peaks (red) to extract a $t_c$ of 57 $\mu$eV and an $l_{SO}$ of 250 nm.

in a MOSFET device with similar dimensions [10]. Since $\alpha$ is a ratio that can be used to parametize the QD diameter to $l_{SO}$, it enables a way to gauge the SO interaction strength relative to the confining potential, where $l_{SO}$ describes the ballistic distance travelled by a hole relative to its spin precession [91, 96]. Due to this, $l_{SO}$ is related to $d_{QD}$ via $l_{SO} \approx (t_c/t_{SO})d_{QD}$, which for a calculated $d_{QD}$ of around 30 nm using Figure 4.2.(e) gives an $l_{SO}$ value of 250 nm.

Comparing the $l_{SO}$ obtained with others reported in Si reveals that our value is almost two orders of magnitude smaller than bulk Si, where 20 $\mu$m has been measured [94]. The value obtained is much lower than expected when compared to a Si spin qubit device with an $l_{SO}$ of 1 $\mu$m which is achieved using electron based QDs. Lengths as low as 110 nm have been estimated in Si but using heavy holes in a planar multi-gate defined QD device, operating at temperatures an order of magnitude smaller with reference to our MOSFET device [25, 27]. Generally speaking our results indicate that the $l_{SO}$ of Si disorder QDs characterized here are closer to those measured in III-IV materials which are typically ≈ 130-250 nm [91, 92, 93]. Therefore as a result of PSB formation in the device measured here, a relatively strong SO interaction was yielded given the $l_{SO}$ extracted. Such an effect has been previously attributed to inversion asymmetry at the interface possibly due to position dependent electric fields at the oxide boundary [27].

# Chapter 5

# Tunable quantum dot transport in Si MOSFETs via electrical stress

## 5.1 Introduction

This chapter describes the content of the publication titled 'Investigating stability and tunability of quantum dot transport in silicon MOSFETs via the application of electrical stress', by J. Hillier *et al* [137], together with supporting data from two other devices. In this work, stress is intentionally induced within a Si MOSFET by systematically applying high gate biases and then investigating the beneficial changes to quantum transport via $E_c$ and $E_a$ through monitoring Coulomb-blockade at a temperature of 2 K. The aim was to study the change in single hole transport characteristics from the stress in order to observe if the charging properties can be enhanced or controlled in disorder based QD devices. In addition, the threshold voltage ($V_{th}$) shift and gate leakage are quantitatively analysed to assess the effect on conventional MOSFET operation as well as to identify a threshold of stability upon which further stress compromises the performance. There are four sections in total, divided into Section 5.2 outlining the device specification and stress procedure, followed by the results in Section 5.3 and a discussion in Section 5.4, comparing and summarizing the findings together with an explanation of the proposed model. Finally, Section 5.5 details how the stress-induced changes are beneficial for future quantum technologies when utilizing disorder based QDs.

## 5.2 Device specification and stress procedure

This section addresses the device specification and QD formation, together with the stress procedure and how oxide-interface trapping and enhanced gate leakage occur as a result of elevated gate biases. The necessary high-resolution $I-V$ characterisations are acquired by utilising a B1500 semiconductor analyser through biasing $V_{\mathrm{g}}$ and $V_{\mathrm{SD}}$ whilst measuring the gate leakage $I_{\mathrm{g}}$ and $I_{\mathrm{d}}$. As detailed in Chapter 3 Section 3.3.2, the experimental procedure for measurement and application of stress is conducted at a temperature of 2 K via wire-bonding and mounting the sample into the CFMS. The three devices under investigation are all Hitachi p-type Si MOSFETs fabricated by standard 65 nm-node technology at an industrial foundry with an identical gate length of 60 nm and width of 10 $\mu$m. The gate and oxide materials are composed of highly doped poly-Si and SiON respectively, with an equivalent oxide thickness of 2.4 nm. A channel length of 60 nm is chosen, as it is reported that distances of less than 80 nm are required for single carrier tunnelling [135]. A schematic of the device structure is given in Figure 5.1(a) with the associated terminals for $I-V$ measurements. These terminals control the transport of individual charges via QDs in the channel acting as a capacitor that is coupled to each of the three terminals, depending on the gate and source/drain voltage conditions $V_{\mathrm{g}}$ and $V_{\mathrm{SD}}$.

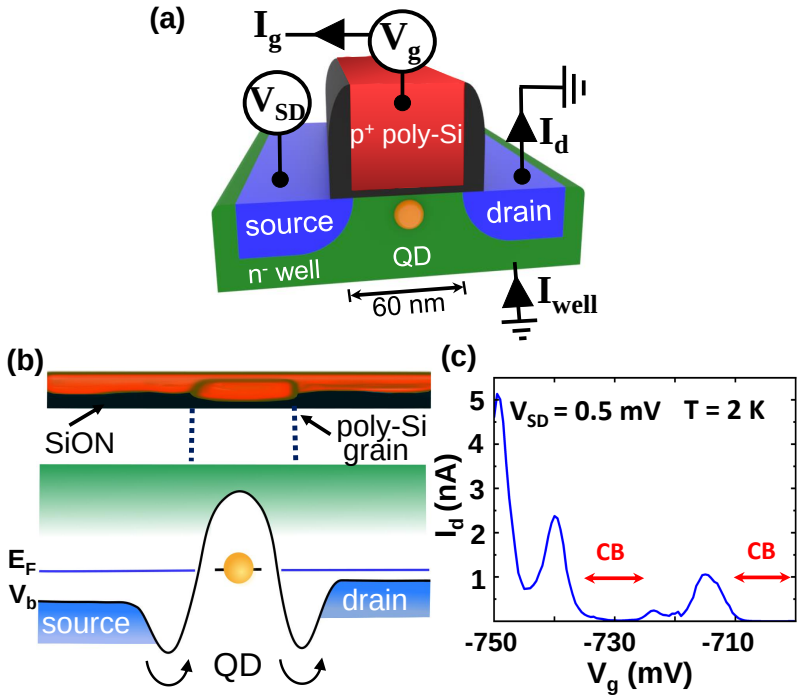



FIGURE 5.1: (a) A schematic of the p-type MOSFET structure with an illustration of a QD in the channel. (b) A QD can be created by Si dangling bonds, poly-Si grains (depicted) or dopants at the gate-oxide interface which results in valance band bending and quantized energy levels for single hole transport. (c) An $I_{\mathrm{d}}$-$V_{\mathrm{g}}$ plot displaying Coulomb-oscillations and Coulomb-blockade as a result of QD formation in the channel at a temperature of T = 2 K.

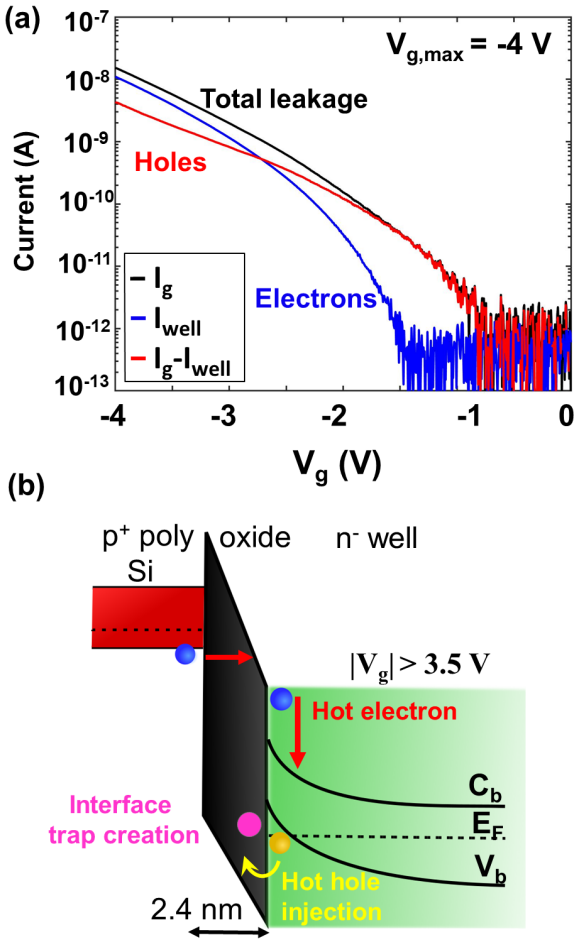



FIGURE 5.2: (a) $I_g$-$V_g$ stress sweep for $V_{g,max}$ = -4 V. The total $I_g$ (black) is separated into the respective carriers, with electrons tunnelling from the gate (blue) and holes from the channel (red). For each stress sweep $V_{SD}$ is set to 10 mV and the well is grounded. (b) A band diagram illustration displaying the leakage mechanisms as a result of anode-hole injection for $|V_g| > 3.5$ V, where hot electrons tunnelling across the oxide lead to the generation of hot holes, which are injected back into the oxide and create interface traps.

Electrical stress is performed by applying a double gate sweep, from 0 V to a maximum gate voltage for given sweep ($V_{g,max}$), and then back to 0 V while recording $I_g$. The stressing procedure commenced at an initial value of $V_{g,max}$ = -4 V up to a maximum $V_{g,max}$ = -5.6 V through -200 mV increments. The effect of such large $V_g$ biases on quantum transport is monitored via Coulomb-diamonds by generating a CSD before and after applying stress. In this type of device, the structural randomness is suspected to originate from disorder-based defects such as Si dangling bonds, dopants or poly-Si grains, as depicted in Figure 5.1(b). Single hole transport as a product of these defects is confirmed in Figure 5.1(c) for low $V_{SD}$ by the presence of Coulomb oscillations (current peaks) and Coulomb-blockade.

The first gate sweep stress measurement, $V_{g,max}$ = -4 V, is displayed in Figure 5.2(a) with the total gate leakage $I_g$ (black), and the carriers separated into electrons (blue) and holes (red). Separating the leakage current into the corresponding carriers is important to document trapping and oxide breakdown mechanisms which can be carrier specific. As observed in Figure 5.2(a) $I_g$ is predominantly composed of hole tunnelling at the onset of stress from the n-Si well to the p+ poly-Si gate ($I_g$ - $I_{sub}$). However when $|V_g| > 1.5$ V electrons ($I_{sub}$) begin to tunnel directly from the p+ poly Si valence band to the n- well conduction band. The magnitude of $V_g$ bias applied is sufficient to induce electron and hole traps in combination with interface states, which can lead to non-trivial effects to QD charging characteristics and therefore heavily influences changes to the interface disorder. Because of these processes, stress has been widely reported to trap both holes and electrons within the oxide together with the generation of interface states as illustrated in Figure 5.2(b) [141, 142]. The origin of stress-induced leakage current and charge trapping can be attributed to carrier specific tunnelling across the oxide through mechanisms such as anode-hole injection [108, 114, 118]. During anode-hole injection, biases above $|V_{g|} \approx 3.5$ V are able to generate sufficiently high fields for electrons to be injected into the n-Si well [146]. Here, the energy is transferred to an electron deep in the valence band, creating a hot hole [118, 125, 128]. These hot holes then tunnel back through the oxide and induce trap generation at the interface and create weak points in the oxide layer, as shown in Figure 5.2(b). If the stressing duration is significantly longer than the sweep procedure described above, such mechanisms until the oxide completely breaks down and the device no longer functions as a transistor, known as hard-breakdown.

## 5.3 Impact of stress on device operation

### 5.3.1 Charging energy and single hole transport enhancement

It is not well understood how Coulomb-diamonds present in the channel of Si MOSFETs at low temperatures can be affected by trap formation due to variations in the capacitive couplings or QD confinement. Therefore, acting as a sensitive detector, any change in the charging characteristics of the Coulomb-diamonds of three devices are monitored before and after stress in the form of CSDs to investigate the effect. This section displays the results from device 1, with device 2 and 3 described in the Section 5.3.2.

Fig. 5.3 (a) to (d) displays the current CSDs for device 1 at a temperature of T = 2 K. For each plot, $V_{SD}$ is swept from -20 mV to 20 mV at fixed $V_g$ values from -600 mV to -720 mV. An initial CSD is taken before stress, then immediately after $V_{g,max}$

= -4 V, -4.4 V and -4.6 V in Fig. 5.3 (a) to (d) respectively. A Coulomb-diamond, which is fully observable throughout the stressing procedure, is highlighted by a white dotted line in Fig. 5.3 (a)-(d) to mark the progressive change in the charging properties of the QD energy level it represents. To quantify the change, the $C_g$ and $E_c$ of these two Coulomb-diamonds are calculated, using equations $C_g = \frac{e}{\Delta V_g}$ and $E_c = \frac{e}{C_\Sigma}$, and displayed in Table. 5.1.

For device 1, the marked Coulomb-diamond initially had a $E_c$ of 8.1 meV in Fig. 5.3 (a), which dropped to 8 meV in (b) and but then increased to 10.3 meV and finally 11.6 meV in (c) and (d), an overall increase of 43%. From this a transition is observed from stress that leads to a slight reduction in $E_c$, but when $V_{g,max}$ values approach -4.4 V, Coulomb-blockade, and hence the charging properties, become enhanced due to the onset of significant oxide-trapping. This can be understood as a product of a significant number of traps within and at the oxide-interface, causing capacitive changes and therefore altering the electrical profile. These values outline both the subtle changes to the Coulomb-diamond when subjected to stresses up to $V_{g,max}$= -4 V, as well as the more drastic changes in Figure 5.3 (c) and (d), which produces a very large increase in

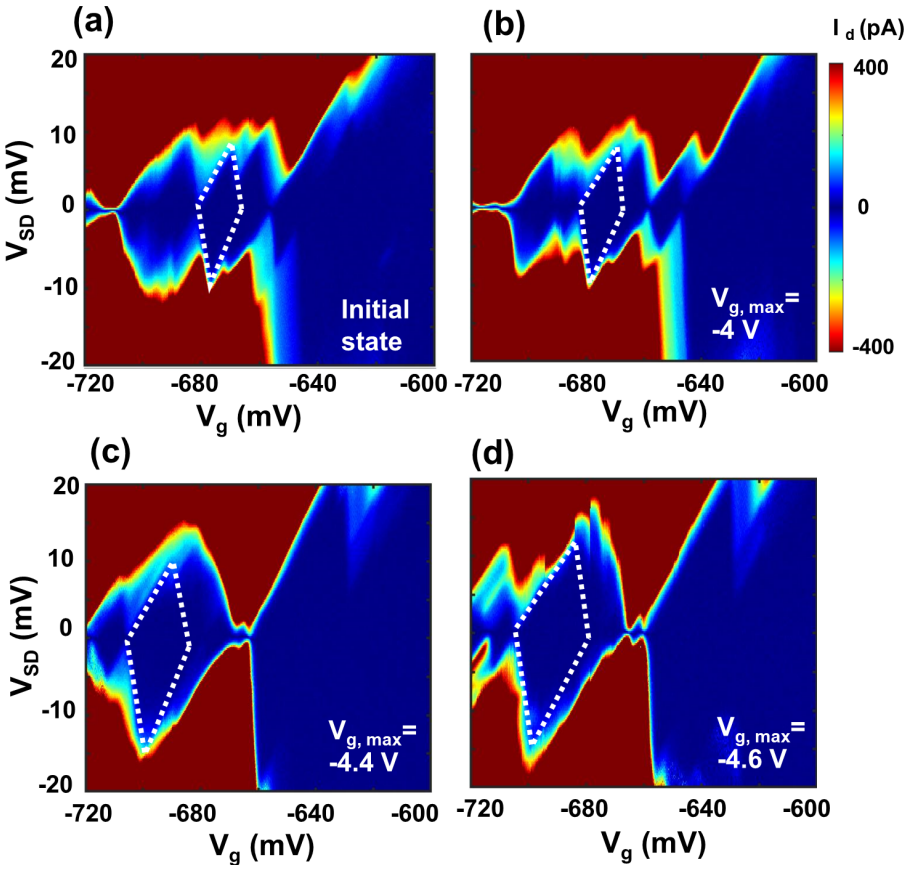



FIGURE 5.3: CSDs generated by biasing the source and gate, whilst measuring drain current in the sub-threshold region for device 1. (a)-(d) Current CSDs with the initial state, $V_{g,max}$ = -4 V, -4.4 V and -4.6 V. Coulomb-diamonds are overlaid by a white dotted line in (a)-(d) to monitor the QD changes during stress.

TABLE 5.1: Summary of single hole charging properties of the two Coulomb-diamonds for device 1 when subjected to electrical stress.

| $V_{g,max}$(V) | $C_g$(aF) | $E_c$(meV) |
|---|---|---|
| Initial | 11.4 | 8.1 |
| -4 | 11.7 | 8 |
| -4.4 | 8.3 | 10.3 |
| -4.6 | 6.4 | 11.6 |

$E_c$ but an unstable Coulomb-diamond pattern when $V_{g,max}$ approaches -4.6 V. It should be noted that between Figure 5.3 (a) and (b) there may be a large increase in $E_c$ for Coulomb-diamonds at the sub-threshold (boundary of single hole when regime begins) but these could not be accurately tracked.

To this end, between $V_{g,max}$= -4.4 V to -4.6 V in Figure 5.3 (c) to (d), the most noticeable changes are due to traps from the unstable regions surrounding, and sometimes within the Coulomb-diamonds. This can be correlated with the increase in interface traps and RTS from the leakage current measurements in Figure 5.2 (a) and suggests that trapping by mechanisms such as anode-hole injection, within the oxide and at the oxide-channel interface, are beginning to hinder the operating stability of the device. Since $E_c$ showed variation, the peak-to-valley current is also investigated to verify if another useful transport feature for SHT performance is enhanced by stress. Here, $I_{peak}$ is the highest $I_d$ value measured during the single hole transport regime between the two largest Coulomb-diamonds (at $V_g \approx$ -660 mV), for $V_{SD} = 1$ mV. The valley current $I_{valley}$ remained less than 10 pA within Coulomb-blockaded region, however, $I_{peak}$ increased from 40 pA in the initial state, to 78 pA, 246 and finally 249 pA for $V_{g,max}$ = -4 V to -4.6 V respectively.

### 5.3.2 Reversible and repeatable changes to Coulomb-blockade

In this section, a more in-depth probe into the impact and beneficial changes to single hole transport via stress through two additional devices is outlined. A second short channel MOSFET, device 2, is stressed to assess the stability and reproducibility of stress-induced changes, up to $V_{g,max}$= -4 V, before significant trap formation could occur. These results are again displayed via CSDs in Figure 5.4 (a)-(b) as a comparison. The initial state in Figure 5.4 (a) clearly shows multiple Coulomb-diamonds present, as with device 1, although a different pattern due to the variation of the transport levels as a consequence of the unique defects which produce them in every device. After applying a $V_{g,max}$ of -4 V, a reduction in $E_c$ is evident when tracking a medium sized Coulomb-diamond in the region labelled as $\beta$ in (a)(i) and $\eta$ in (a)(ii). Device 2 then underwent a thermal cycle, from 2 K to 295 K and then back to 2 K, as a way to determine the permanency of stress-induced changes and to gain further evidence on the mechanism. Figure 5.4 (b)(i) displays the resulting CSD after a thermal cycle, with the outcome of

applying a repeated stress of -4 V shown in (b)(ii). The most striking feature is the similarity in the Coulomb-diamonds in Figure 5.4 between regions $\alpha$, $\beta$ and $\gamma$ in (a)(i) and (b)(i) as well as $\epsilon$, $\eta$ and $\Delta$ in (a)(ii) and (b)(ii), evidencing that the variation caused by moderate stress is temporary and there exists not only a similar trend between devices, but a consistent response for a given device.

The impact of stress on $I_{\text{peak}}$ is also measured for device 2 at a $V_{\text{SD}}$= 1 mV. As there are multiple Coulomb-diamonds overlapping in the $\gamma$ region of Figure 5.4 (a), $I_{\text{peak}}$ is measured between two Coulomb-diamonds at the boundary where $\beta$ and $\gamma$ intersect in (a)(i) and (a)(ii), and where $\eta$ and $\Delta$ intersect in (b)(i) and (b)(ii). $I_{\text{valley}}$ within the Coulomb-diamonds adjacent to this region is typically 5-10 pA. $I_{\text{peak}}$ is found to improve substantially from 420 pA in (a)(i) to 3.27 nA in (a)(ii), and 390 pA in (b)(i) to 2.91 nA in (b)(ii), in combination with lower gate biases in both instances. These trends are

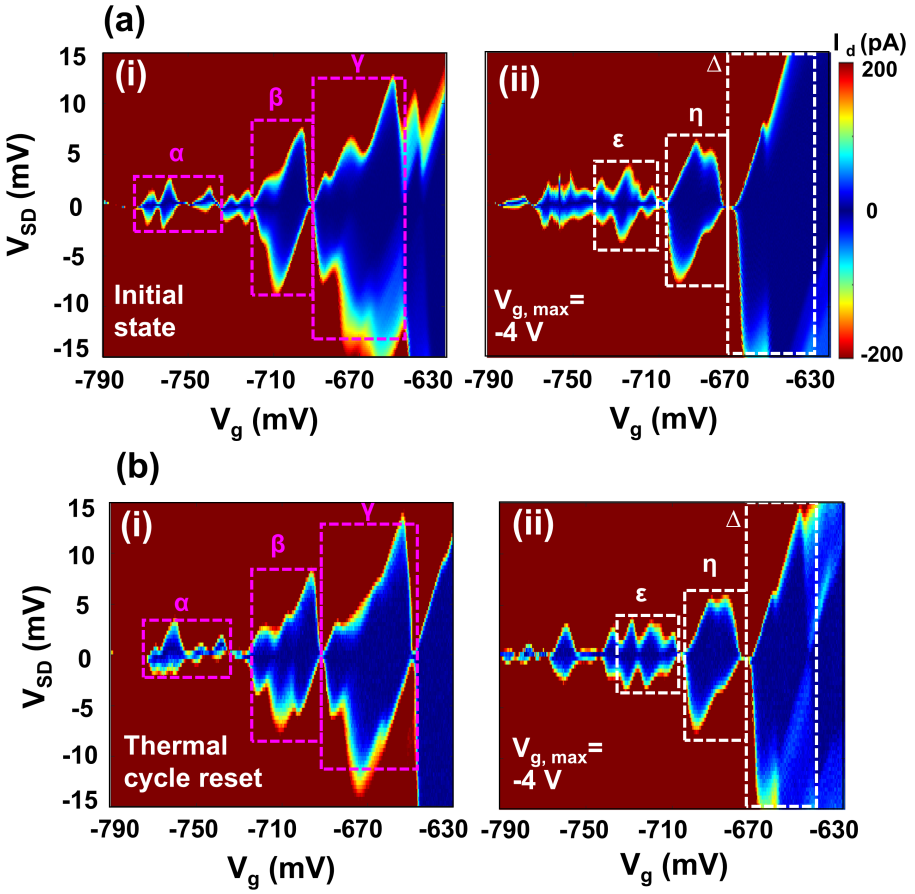



FIGURE 5.4: CSDs generated by biasing the source and gate, whilst measuring the drain current in the sub-threshold region for device 2. (a) Current CSDs with the initial pre-stressed state (a)(i) and moderate stress, $V_{\text{g,max}}$ = -4 V (a)(ii). After a thermal cycle, from 2 K to 295 K and back to 2 K, another CSD is taken (b)(i) as well as after applying a second stress of -4 V (b)(ii). The rectangles outlined in dashed pink highlight Coulomb-diamonds which closely match in (a)(i) and (b)(i). The white dashed rectangles in (a)(ii) and (b)(ii) highlight similarities in regions after applying the first and second -4 V stress.

consistent with data collected from device 1, with some discrepancy on the magnitude of $V_{g,max}$ required to produce a large increase in $E_c$ (-4.4 V for device 1 compared to -4 V for device 2), although device 1 may have displayed this behaviour but the difficulty in tracking the Coulomb-diamonds at low $V_g$ in Figure 5.3 (a) to (b) prohibited verification of this.

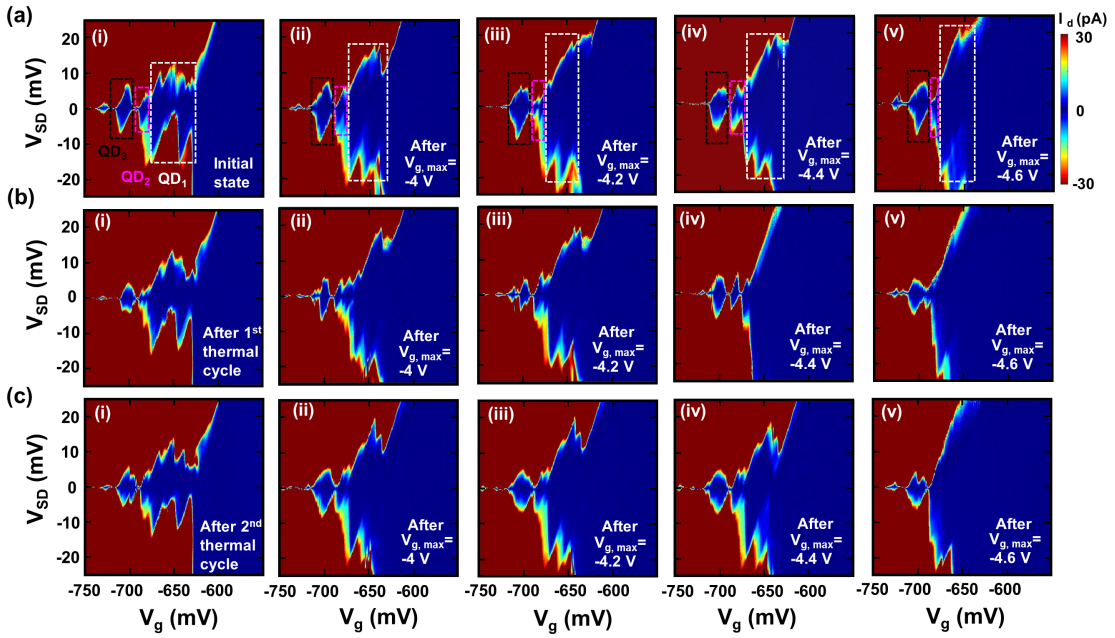



FIGURE 5.5: CSDs generated from experimental data from device 3 by biasing the source ($V_{SD}$) and gate ($V_g$), whilst measuring drain current ($I_d$) in the sub-threshold region. (a) CSDs taken of the initial state and immediately after $V_{g,max}$ = -4 V, -4.2 V, -4.4 V and -4.6 V stress sweeps in (i)-(v) respectively. The white, pink and black dashed rectangles highlight the changes to the Coulomb-diamond pattern from $QD_1$, $QD_2$ and $QD_3$ respectively, as a result of stress-induced changes at the interface. (b) After performing one thermal cycle from 2 K to 295 K and back to 2 K, the CSDs are remeasured with identical parameters in (i)-(v). (c) A second thermal cycle is performed and the CSDs are retaken again in (i)-(v) to verify a consistent response.

The results from a final device to undergo electrical stress, device 3, are displayed in Figure 5.5(a)-(c). Here, CSDs with identical $V_{SD}$ and $V_g$ parameters are shown, where each sub-plot in a given row only differs in the amount of stress applied prior to measurement. An initial CSD is taken before stress, and then immediately after $V_{g,max}$ = -4 V, -4.2 V, -4.4 V and -4.6 V in Figure 5.5(i)-(v) for each column respectively. A $V_{g,max}$ value of -4 V is chosen in particular to identify any differences which emerge from the onset of trapping at the interface due to anode-hole injection as with device 2, together with elevated biases of -4.4 V and beyond to investigate the threshold of instability revealed by device 1. The resulting Coulomb-blockade patterns are a product of three distinct QDs, from the analysis outlined in Section 5.3.4. In Figure 5.5(a)(i)-(v) $QD_1$, $QD_2$ and $QD_3$ are highlighted by the white, pink and black regions to track the progressive change from $V_{g,max}$ = -4 V to -4.6 V. Between Figure 5.5(a)(v)- (b)(i), as well as (b)(v)-(c)(i),

the device underwent a thermal cycle, from 2 K to 295 K and then back to 2 K, as a way to determine the permanency of the stress related changes and to gain further evidence on the mechanism. Repeat stress measurements in Figure 5.5(b) and (c) also allow the stability and reproducibility of the Coulomb-diamond structure to be assessed, serving as a comparison to Figure 5.5 (a).

After applying $V_{g,max}$ of -4 V, the same significant increase in charging energy of $QD_1$ is observed with a moderate increase for $QD_2$, however a less consistent change in the charging properties of $QD_3$ as $V_{g,max}$ increased can be noted. The most prominent feature is the similarity of the regions outlined in Figure 5.5(a)(i)-(v) when compared to (b)(i)-(v) and (c)(i)-(v) evidencing that the variation caused by stress is temporary, and there exists not only a reversible trend but also a consistent response due to stress which confirms the behaviour displayed by device 2. The initial states in Figure 5.5(b) and (c) clearly show an almost identical Coulomb-diamonds pattern when compared to (a). This provides further support on the relationship between stress and QD changes when analysing the Coulomb-diamonds after the 1st and 2nd thermal cycles where the Coulomb-blockade pattern reverted to the initial device condition. $QD_1$ most notably matches the enhanced features after stress, with $QD_2$ appearing moderately more confined but less consistent, and as before an unpredictable relationship between stress-induced changes and the charging properties of $QD_3$.

### 5.3.3 Large-scale trapping and device degradation

An enlargement is made of two central Coulomb-diamonds after subjecting device 1 to $V_{g,max}$ = -4.6 V in Figure 5.3 (d) and plotted in Figure 5.6 (a), to highlight the influence of stress induced traps on transport. From this CSD, an $I_d$ profile is taken at $V_{SD}$ = -12.4 mV (white dotted line) and plotted in Figure 5.6 (b). A single, large discrete switching event from an RTS is clearly visible at $V_g$ = -678 mV. Such an event corresponds to a $V_{th}$ shift leading to a sudden change in $I_d$ from two high/low states. Here, the high/low signals refer to an occupied or unoccupied trap due to a single charge, where each state results in a $V_{th}$ shift from a modified electric field in the channel and therefore leads to a sudden change in $I_d$ [105, 115, 131, 147]. The trap remained for entire $V_{SD}$ sweep it was present (independent of $V_{SD}$) and had a calculated $V_{th}$ shift of 3 mV. Such features allowed this particular trap to be easily identified from the magnitude of $V_{th}$ shift, and because the hole trapping occurred in a region sensitive to voltage, which can be observed from the $I_d$-$V_g$ gradient in Figure 5.6 (b).

An additional trap related artefact became apparent at $V_g$ = -715 to -718 mV in Figure 5.6 (a) and (b). This event is believed to be a result of trap assisted tunneling between an excited state of a QD and a trap level. As this feature is only present at negative $V_{SD}$ values outside of a CD, it cannot be due to a simple $V_{th}$ shift which would

not be so dependant on $V_{SD}$ and its polarity. The trap level is thought have arisen from a charge occupying a stress induced interface state, forming a single level close to the drain. Holes in the QD would then be able to tunnel through this additional level causing an increase in $I_d$ as observed.

To examine instabilities at even greater gate biases, further CSDs are generated at $V_{g,max}$ values of -4.8 V to -5.2 V (Figure 5.7(a)(i)-(iii)) using device 3. The effect of applying biases greater than $V_{g,max}$ = -4.6 V clearly demonstrates device degradation. This is evident from the manifestation of Coulomb-diamond features gradually appearing smaller, fewer in number, and unstable when moving from (i)-(iii) in Figure 5.7(a). To highlight the impact of stress-induced traps on QD stability, $I_d$ - $V_g$ sweeps are taken after $V_{g,max}$ = 5.2 V and plotted (Figure 5.7(b)) where significant RTS appeared in $I_d$ [130]. Large discrete switching events between high/low states are plainly visible throughout the sweep as with device 1 but more severe, and appear to be most detrimental around $V_g$ = -720 mV for low $V_{SD}$, owing to their magnitude relative to the Coulomb oscillation peak. This suggests that breakdown mechanisms within the oxide and at the channel-oxide interface are beginning to considerably hinder device stability.

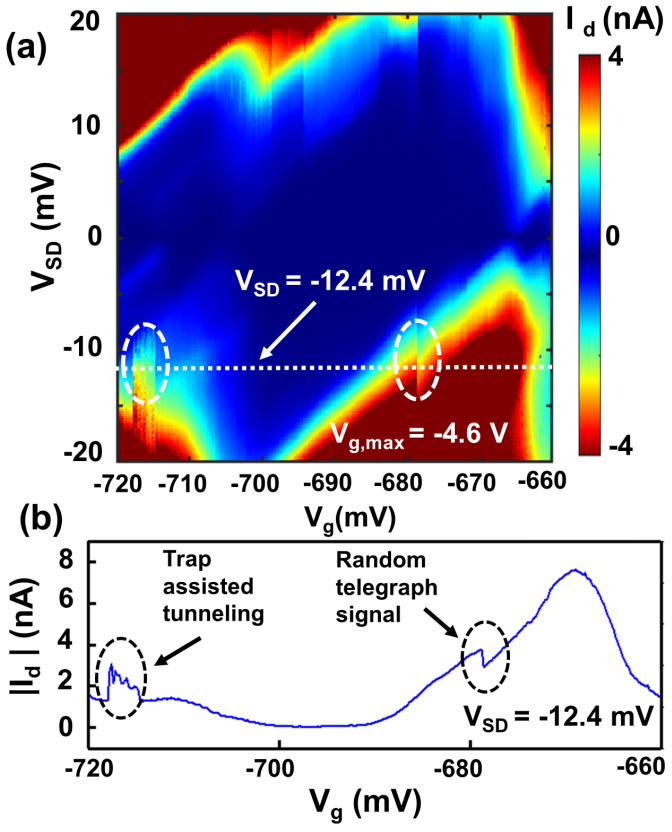



FIGURE 5.6: (a) Enlargement of unstable region of device 1 at the edge of a Coulomb-diamond after $V_{g,max}$ = -4.6 V, showing discrete switching from a trap in the highlighted areas. (b) $I_d - V_g$ sweep with $V_{SD}$ = -12.4 mV. A significant random telegraph signal event can be identified at -678 mV $V_g$ as well as trap assisted tunneling at -715 mV $V_g$
.

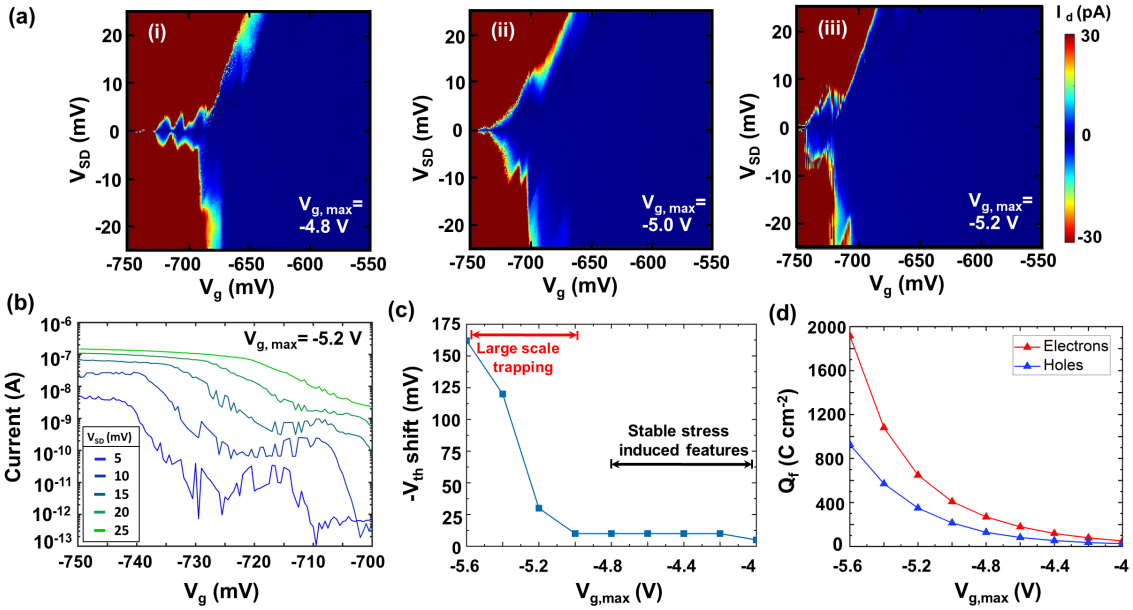



FIGURE 5.7: For $V_{g,max}$ = -4.8 V and beyond, the experimental data of device 3 suggests that the device stability is compromised from large-scale trapping. (a)(i)-(iii) CSDs at elevated $V_{g,max}$ values of -4.8 V, -5 V and -5.2 V respectively. The Coulomb diamonds appear unstable in (i) with RTS becoming more prominent in (ii) and (iii). (b) $I_d$-$V_g$ sweeps after $V_{g,max}$ = -5.2 V for $V_{SD}$ = 5-25 mV, the RTS becomes very prominent and greatly affects device performance. (c) The respective change in threshold voltage ($V_{th}$) shift as the maximum applied stress voltage, $V_{g,max}$, increased from -4 V to -5.6 V. A significant shift can noted above $V_{g,max}$ = -5 V. (d) Charge fluence ($Q_f$) for both electrons and holes through the oxide at each $V_{g,max}$.

Greater insight on stress-induced changes can be unveiled through calculating $V_{th}$ shift, an important parameter for characterising global transport changes across the MOSFET channel as an outcome of trapped oxide charge. Since $V_{th}$ shift is a clear indicator that charge is becoming trapped within the oxide, or at the interface, it represents capacitive changes experienced across the whole channel in response to oxide breakdown. Here, $V_{th}$ is defined as the gate bias at which $I_d$ becomes greater than 1 nA . Therefore a negative $V_{th}$ shift corresponds to an increase in negative gate bias in order to invert the channel and compensate for trapped positive charge [110]. Based on this, $V_{th}$ shift is calculated after every $V_{g,max}$ sweep. In Figure 5.7(c) a -160 mV $V_{th}$ shift is attained when comparing the initial $I_d$ and after applying $V_{g,max}$ = -5.6 V. This is consistent with the injection of holes into the oxide layer leading to a negative shift in $V_{th}$. A very similar trend is observed in Figure 5.7(d) for the charge fluence ($Q_f$) through the oxide, which is calculated via the equation [38]:

$$Q_f = A \int_0^t I_g(t)dt \tag{5.1}$$

where $A$ is the channel surface area, $I_g$ is the leakage current of each respective carrier and $t$ the total measurement time for a given sweep. Focusing on the increase in carrier

tunnelling across the oxide in Figure 5.7(d), it is worth noting that between $V_{g,max}$ = -4 V to -4.6 V, $Q_f$ rises from 25 C cm$^{-2}$ to 81 C cm$^{-2}$ for holes and 50 C cm$^{-2}$ to 179 C cm$^{-2}$ for electrons. This is in contrast to an increase by more than an order of magnitude between $V_{g,max}$ = -4.6 V to -5.6 V, whereby the values rise to 927 C cm$^{-2}$ and 1916 C cm$^{-2}$ for holes and electrons respectively within the unstable region.

### 5.3.4 Quantifying activation energy and QD coupling when subjected to stress

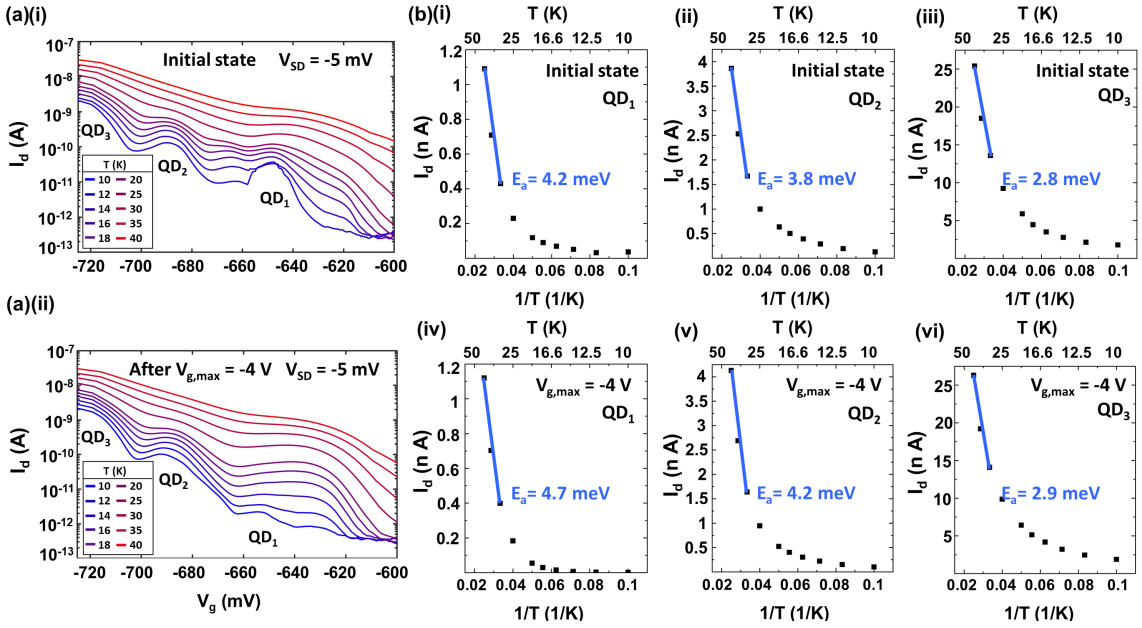



FIGURE 5.8: Estimating changes to the $E_a$ after stress by using the QD temperature dependence of device 3. (a)(i) Coulomb oscillation peaks at 10-40 K for $QD_1$, $QD_2$ and $QD_3$ in the initial pre-stressed state and after applying $V_{g,max}$ = -4 V in (a)(ii). (b)(i)-(iii) Arrhenius plots over a 10-40 K temperature range to extract $E_a$ from the Coulomb oscillation peaks of each QD during the initial state and after applying $V_{g,max}$ = -4 V in (b)(iv)-(vi).

Another key attribute of QDs is the barrier height, otherwise known as $E_a$, which can be utilized to study any stress-induced changes to the system. $E_a$ can be calculated by measuring the temperature dependence of $I_d$ during the Coulomb oscillation peaks between Coulomb-diamonds. The $I_d$ temperature dependence of device 3 is displayed in Figure. 5.8(a)(i) and (a)(ii), where $I_d$-$V_g$ plots over a temperature range of 10-40 K are displayed for the initial state and after $V_{g,max}$ = -4 V respectively. Evidently, increases in temperature are met with elevated $I_d$, in addition to the Coulomb oscillation peaks for each QD (labelled) becoming less defined and shifting to lower $V_g$ values. This is consistent with the thermal emission of holes within the QDs. Comparing Figure 5.8(a)(i) and (a)(ii), the most significant change after stress, mirroring the CSDs in Figure 5.5, is the drop in $I_d$ due to the Coulomb-diamond expansion for $QD_1$. Using the peak $I_d$ oscillation for each QD level at a given temperature, $E_a$ can be approximated according

to the well known Arrhenius model via the equation [150]:

$$I_{\mathrm{d}} = I_{\mathrm{d0}} e^{\frac{-E_{\mathrm{a}}}{kT}} \tag{5.2}$$

where $I_{\mathrm{d0}}$, k, and T are the initial drain current as the temperature approaches 0 K, the Boltzmann constant and temperature respectively.

Arrhenius plots based on this model are shown in Figure 5.8(b)(i) -(vi) where $E_{\mathrm{a}}$ is estimated via the gradient during the thermal emission regime as indicated. Figure 5.8(b)(i)-(iii) display plots for extracting $E_{\mathrm{a}}$ of the initial state for $QD_1$, $QD_2$ and $QD_3$. Figure 5.8(b)(iv)-(vi) depict the same plots after $V_{\mathrm{g,max}}$ = -4 V which yield increases of 0.5 meV for $QD_1$ and 0.4 meV for $QD_2$, while a modest increase of 0.1 meV is observed for $QD_3$. Given the magnitude of $E_{\mathrm{a}}$ in Figure 5.8, it would be more correct to associate these values with the energy needed to escape the quantum level, rather than the activation energy, since the values extracted are smaller than $E_{\mathrm{c}}$ and the barrier height must be larger than $E_{\mathrm{c}}$.

To summarize the key differences as a result of stress, $E_{\mathrm{a}}$, $E_{\mathrm{c}}$ and lever arm ($\alpha$) of the three QDs after each stress voltage were determined for device 3. This was achieved using Figure 5.5(a)(i)-(v) with equations $E_{\mathrm{c}} = \frac{e}{C_{\Sigma}}$ and $\alpha = \frac{V_{\mathrm{SD}}}{V_{\mathrm{g}}}$ together with Figure 5.8(a)(i)-(ii) and equation (2). These parameters for each QD during the initial state and after $V_{\mathrm{g,max}}$ = -4 to -4.6 V are displayed in Table 5.2 above. In addition, the initial QD diameter ($d_{\mathrm{QD}}$) can also be approximated given the QD surface area ($S_{\mathrm{QD}}$) and effective oxide thickness ($t_{\mathrm{eff}}$) by $d_{\mathrm{QD}} = \sqrt{4S_{\mathrm{QD}}/\pi}$, using $S_{\mathrm{QD}} = C_{\mathrm{g}}/C_{\mathrm{eff}}$ and $C_{\mathrm{eff}} = \epsilon_{\mathrm{ox}}/t_{\mathrm{eff}}$, where $\epsilon_{\mathrm{ox}}$ is the permittivity of the oxide. This yields a $d_{\mathrm{QD}}$ of 28 nm, 46 nm and 31 nm for $QD_1$, $QD_2$ and $QD_3$ respectively.

## 5.4 Discussion on changes to single hole transport and trapping model

In this section the important findings are discussed and a model is put forward to explain the stress-induced changes. In Table 5.2 the $\alpha$ values obtained serve as a strong indicator that each of the Coulomb-diamonds tracked after applying stress to device 3 are indeed from the same three distinct QDs. Considering that $\alpha$ reflects the ratio of QD couplings (from Coulomb-diamond dimensions), a higher value such as 0.8 for $QD_1$ suggests a strong coupling and in close proximity to the gate, whereas a lower value of 0.3 implies $QD_3$ is located further away from the interface. Based on this, the origin of $QD_1$is proposed to be a Si dangling bond at the oxide-interface, given the high $\alpha$ value as well as an $E_{\mathrm{c}}$ close to 13 meV above the valence band, which is agreeable for this type of trap site [149]. $QD_2$ and $QD_3$ on the other hand are presumed to be generated by disorder of a different nature, for example, poly-Si grains, where small

TABLE 5.2: Summary of single hole transport properties of $QD_{1-3}$ for device 3 when subjected to electrical stress.

| No. | $V_{g,max}(V)$ | $E_a$ (meV) | $E_c$(meV) | $\alpha$ |
|---|---|---|---|---|
| $QD_1$ | Initial | 4.2 | 12.5 | 0.7 |
| | -4 | 4.7 | 13.8 | 0.7 |
| | -4.2 | 4.7 | 16.8 | 0.8 |
| | -4.4 | 4.9 | 15.0 | 0.7 |
| | -4.6 | 4.4 | 19.3 | 0.8 |
| $QD_2$ | Initial | 3.8 | 2.5 | 0.4 |
| | -4 | 4.2 | 3.8 | 0.4 |
| | -4.2 | 4.4 | 2.0 | 0.4 |
| | -4.4 | 4.5 | 4.0 | 0.5 |
| | -4.6 | 3.9 | 4.0 | 0.5 |
| $QD_3$ | Initial | 2.8 | 5.5 | 0.3 |
| | -4 | 2.9 | 7.3 | 0.4 |
| | -4.2 | 3.1 | 5.5 | 0.4 |
| | -4.4 | 3.3 | 3.5 | 0.3 |
| | -4.6 | 2.4 | 5.5 | 0.4 |

non-uniformities in the gate are small enough to create confined levels for single carrier transport. $QD_1$ initially had a larger $E_c$ of 12.5 meV in Figure 5.5(a)(i), which then gradually increased to 19.3 meV in (a)(v), a rise of more than 50%. This overall pattern is matched for $QD_2$, although its $E_c$ decreased after applying $V_{g,max}$ = -4.2 V, from 2.5 meV in Figure 5.5(a)(i) to 2.0 meV in (a)(iii), before finally reaching an enhanced 4 meV in (a)(v). For $QD_3$ however this tendency of an increasing $E_c$ for larger a $V_{g,max}$ is not observed. The first -4 V stress sweep resulted in a 30% enlargement in $E_c$, but despite this, after the application of stress for all other values from -4.2 V to -4.6 V the outcome was either a reduction to the initial $E_c$ or less. These findings suggest that $QD_1$ yielded the greatest stress response from the largest increases in $E_c$ by magnitude, although $QD_2$ demonstrated a similar response relative the Coulomb-diamond dimensions.

The enhanced charging properties can be explained by changes to the oxide integrity in combination with the likely QD origin. If single hole transport is a product of traps, dopants or poly-Si grains at the oxide interface, charge traps are more likely to form close to these sites as a consequence of weaker oxide performance. As a natural outcome, stress-induced trapping would then lead to a build up of charge at the interface close to regions harbouring the defects, resulting in the narrowing of the potential profile and hence stronger confinement. Aside from anomalous trapping which can produce matching responses, a model to explain the similarity between $QD_1$ and $QD_2$ may be related to the larger size of $QD_2$ (46 nm), when compared to $QD_1$ (28 nm). The reasoning is that a smaller $\alpha$ value of $QD_2$, and therefore weaker interaction with the interface charge, may be compensated for by the greater QD surface area exposed to oxide trapping. $QD_3$ on the other hand not only exhibited less predictable changes but also possessed the weakest interface coupling in combination with a smaller size of 31 nm.

Comparisons between the impact of stress and $E_a$ from Table 5.2 yield the same tendencies for all QDs. A systematic trend is ascertained from an enlargement in $E_a$ after $V_{g,max}$ = -4 V , which differed in magnitude and then revealed the same tendency of a sudden decrease at $V_{g,max}$ = -4.6 V, close to or below the initial value. In fact, when $|V_{g,max}| > 4.6$ V, a transformation in the behaviour is expected to take place in order to reflect the precipice of significant oxide degradation. At higher $V_{g,max}$ values the sheer magnitude of charge trapping within the oxide cannot be efficiently removed and therefore leads to the instabilities as displayed in Figure 5.7 (a) and (b). A rising $V_{th}$ shift in Figure 5.7(c), accompanied by an escalating $Q_f$ through the oxide in Figure 5.7(d) is to be expected due to anode-hole induction, as described in Section 5.2. This may also explain the possible reason behind the drop in $E_a$ at $V_{g,max}$ = -4.6 V, since the potential barrier height between the QD and source/drain may well become reduced from many trapped oxide charges. Furthermore, the anode-hole injection model offers a solution to the polarity of carrier trapping, where positive charge associated with trapped holes and interface states collectively dominate the negative charge and therefore result in a negative threshold shift Figure 5.7(c) [143]. This can be explained by electron trapping at defect sites being far less efficient even though the electron fluence is significantly higher than the hole fluence [144, 145]. Interface states however have been found to remain for considerable periods of time, with their effect being the most dominant on QD charging properties within the $V_{g,max}$ = -4 V to -4.6 V region due to the absence of $V_{th}$ shift. Subsequently, the variation experienced by single hole transport is considerably more dependant on local anomalies in contrast to changes in $E_a$, that are associated with differences in barrier height on either side of a QD. As such, any correlation reflects both large-scale changes to the valance band across the channel and at the QD site. For example, the introduction of a single trap state in the near vicinity of a QD would alter the interface disorder and therefore modify the capacitive coupling, which then leads to differing Coulomb-diamond charging properties. A scenario such as this is largely independent of any global stress-induced trends across the channel as a product of large-scale trapping within the oxide.

## 5.5 Outlook and applications

The repeatability of the Coulomb-diamond pattern when subjected to stress in Figures 5.5(a)-(c) also reinforces that the induced changes are predictable and controllable to an extent. The significance of observing similar responses for all three QDs after stress and reset cycles is not a trivial matter, considering that the physical nature behind the changes is a consequence of stochastic phenomena and hence should lead to a plethora of varied charging characteristics. For example, the CSDs obtained in Figure 5.5 are a result of three QDs which vary in location and size. Accordingly, the response due

to stress will likely always display some variation, depending upon the sensitivity and proximity of the defect level to both the differences at the interface and within the oxide. Therefore stress-induced trapping can only be claimed to be consistent (at the same sites) for a given device in order to produce the matching Coulomb-diamond response. The reasoning as to why this happened is suggested to be a product of charges becoming trapped at the same preferential sites due to unique structural non-uniformities at the oxide-interface. These include poly-Si grain edges within the oxide, or close to the oxide-interface near Si dangling bonds, which would lead to a repeatable effect for a given device. Considering the repeatable and reversible nature alone suggests poly-Si grains or dopants as the originators of the single carrier phenomena, since these defects are very stable in nature and robust against thermal cycles [151].

This almost fully resettable nature back to the initial state in Figures 5.5(a)(i), (b)(i) and (c)(i) therefore highlights a complete annihilation of the stress-induced interface states by relaxation at elevated temperatures, which is also confirmed device 2. The stress technique put forward offers a path towards tuning charging characteristics in a controllable and reversible way that enables Si MOSFETs to perform as optimized QD devices. For example, because stress introduces temporary interface traps it can aid in offsetting the parasitic background charges of SHTs that produce unwanted device variability. Furthermore, increasing $E_c$ is advantageous for optimizing SHT performance to aid in reducing the gate leakage together with higher temperatures of stable operation. The large-scale changes due to stress also demonstrate that the Coulomb-diamond pattern for a given device can be altered to such a degree that the pattern becomes unrecognisable when compared to the original state, which is then fully resettable to the initial condition. This stressing method is therefore capable of introducing an appreciable difference to Coulomb-blockade and $E_c$, which provides support for single charge memory applications from the formation of two distinct device states that can be written, erased and re-written.

The trap assisted tunnel feature after stress in Figure 5.6 for device 1 is also significant, as it involves a unique case where transport between a QD and defect level or a stress induced trap level occurs. Such a scenario would enable the spin state of a trap to be read by PSB, where charge can be correlated with spin configurations. This would allow the spin of individual charges to be manipulated and read, and therefore could function as a spin qubit. The ability to tune charging characteristics in a controllable way, such as improving $I_{peak}$ or alter the charging would prove useful for SHTs [30]. A moderate stress of -4 V can introduce temporary interface traps to help offset the parasitic background charges of SHTs producing unwanted variability. This could aid in achieving control over the number of fixed charges surrounding electrically defined QDs. Increasing the charging energy as a result of high stress would also be useful for optimizing SHTs if higher temperatures of operation are desired. As such, highlighted

in this chapter are the advantageous changes induced within QDs of three devices which are largely consistent between the three devices, as well as emphasising the threshold of stability for useful properties to occur.

# Chapter 6

# Silicon nanowire devices - design, fabrication and measurement

## 6.1 Project aim and overview

In addition to characterising industry standard CMOS devices provided by Hitachi for quantum information related investigations, our group also fabricated two lots of Si nanowires, designated SET48 and SET57. These devices were intended for use as SEPs owing to the tunable nature of gate defined QDs in order to close the quantum metrological triangle. However, as a consequence of the versatile device architecture, a plethora of other QD transport phenomena and interactions can also be investigated using such samples. Lot SET48 was fabricated before my arrival, in October 2016, while SET57 was successfully completed in early 2019. The fabrication of both projects were led by the post-doctoral researcher within our group, Dr M. K. Husain. My involvement for SET48 was through back-end processing, room temperature validation and low temperature characterisation, where as my roles for SET57 were via aiding in the design, fabrication, back-end processing, as well as both room temperature and low temperature validation.

Outlined in this chapter is a fabrication overview in Section 6.2, detailing the significant fabrication steps from nanowire definition and gate patterning to metallisation, together with a titanium nitride/titanium/aluminium (TiN/Ti/Al) metal stack test lot. Following this, the device yield check and back-end processing steps are described including laser cutting, cleaning and wire-bonding in Section 6.3 and Section 6.4 respectively. Finally, Section 6.5 presents the low temperature characterisation results for single and double-QD transport.

From the work undertaken, a first author conference publication in Silicon Quantum Information Processing Workshop (2021) titled 'Atomically flat trapezoidal silicon nanowires for tunable gate defined quantum dots' by J. Hillier *et al* [126] was achieved, which describes how confinement becomes enhanced due to the trapezoidal nanowire shape. Two co-author publications were also attained, with one in IOP Nanotechnology titled 'Manipulation of random telegraph signals in a silicon nanowire transistor with a triple gate'(2018) by F. Liu *et al* [115], where RTS from a thermally activated QD could be controlled by the triple gate nanowire device structure to a high degree of precision. The second publication was realised in AIP Advances titled 'Silicon single-electron random number generator based on random telegraph signals at room temperature' (2020) by K. Ibukuro *et al* [39], based on using RTS as a random number generator through 'supervised learning'.

## 6.2 Fabrication process flow

Both SET48 and SET57 were fabricated on 6-inch <100> silicon-on-insulator (SOI) wafers with a 145 nm buried oxide (BOX). Figure 6.2 lists the process flow for fabrication which includes the 6 major fabrication steps: nanowire definition, dopant diffusion, patterning Finger gates (FG) and Top gate (TG), metallisation and finally back-end processing.

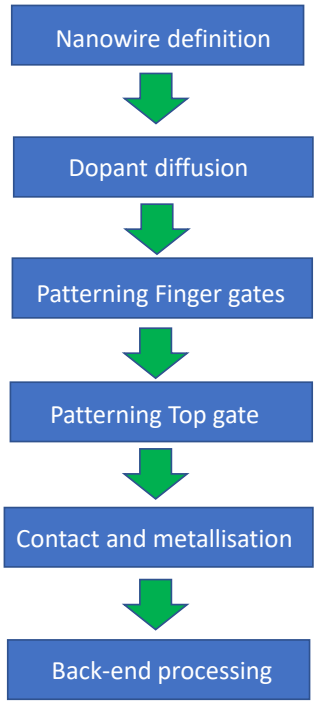



FIGURE 6.1: The process flow for the fabricating Si nano-wires

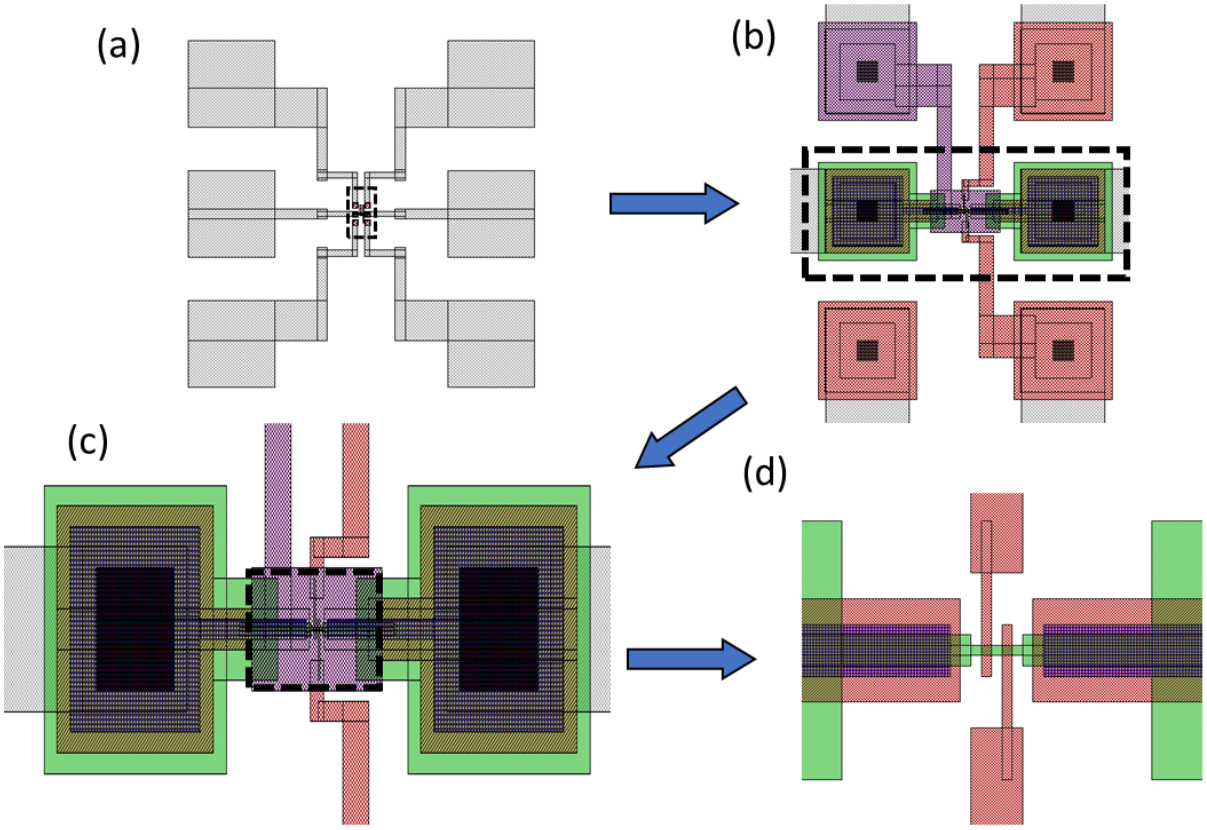



FIGURE 6.2: Device images at various levels within the L-edit design software (a) Entire device overview with metal layer and pads visible. (b) Zoomed in image of device contact level. (c) Higher magnification from highlighted region in (b) with gate structures becoming visible. (d) Enhanced image from highlighted area in (c), showing the device core with nanowire and $FG_1$ and $FG_2$. TG is omitted for clarity which would cover the entire area in (d).

Figure 6.2 displays images of various device levels during the design process on software package L-edit. (a) shows the entire device with Al device pads, where magnification increases from (b) to (d) until the device core is visible, consisting of the nanowire and FGs (TG covers this area on top). Intrinsic silicon is denoted as green, poly-Si as red and doped source/drain regions as blue. The FGs as seen in Figure 6.2 (d) are a crucial element in order to electrically define a QD within the nanowire as a consequence of quantum confinement, with TG offering additional tunability. The ideal nanowire and FG diameters in order to observe single electron transport are typically 30 nm - 100 nm, therefore electron-beam (e-beam) lithography was used for all layers in order to satisfy the required resolution.

A summary of the wafer split for lot SET48 is given in Table 6.1 where out of a total of four wafers only one was successful (wafer 4). Within this lot, the tetramethylammonium hydroxide (TMAH) wet etching technique was used exclusively to define the nanowires. This is in contrast to the wafer split for SET57 in Table 6.2 which incorporated TMAH as well as inductive-coupled-plasma (ICP) dry etching for nanowire definition wafers, in

TABLE 6.1: Four-wafer nanowire fabrication summary of lot SET48.

| Wafer No. | Purpose | Nanowire definition | Total No. devices | Working No. devices | Notes |
|---|---|---|---|---|---|
| 1 | No TG | TMAH | N/A | N/A | Contact failure |
| 2 | FG patterning | TMAH | N/A | N/A | For imaging |
| 3 | SOG structure | TMAH | N/A | N/A | Short circuit |
| 4 | Direct poly-Si deposition | TMAH | 736 | 98 | Successful |

TABLE 6.2: Six-wafer nanowire fabrication summary of lot SET57.

| Wafer No. | Purpose | Nanowire definition | Total No. devices | Working No. devices | Notes |
|---|---|---|---|---|---|
| 1 | SOG structure TG absent | TMAH | N/A | N/A | Nanowire failure |
| 2 | Direct poly-Si deposition | TMAH | N/A | N/A | Contact failure |
| 3 | SEM imaging for Nanowire definition | TMAH | N/A | N/A | For imaging |
| 4 | SOG structure TG present | TMAH | N/A | N/A | Contact failure |
| 5 | Direct poly-Si deposition | ICP | 1076 | 192 | Successful |
| 6 | Backup wafer | ICP | N/A | N/A | Contact failure |

addition to wafers for imaging and test spin-on-glass (SOG) lots. Out of the 6 wafers only one was successful, wafer 5, where an 17.8% yield was achieved in comparison to the 12.8% yield for SET48. With the exception of the etching technique, the only other difference between the lots was a change to gate oxide thickness from 17.6 nm for SET48 to 8 nm for SET57. As a product of only two differences between SET48 an SET57, the fabrication overview as described in the following section is applicable to both lots unless stated otherwise. Figure 6.3 displays cross-section of a completed device and Figure 6.4 shows a 3D schematic with TG omitted for simplification.

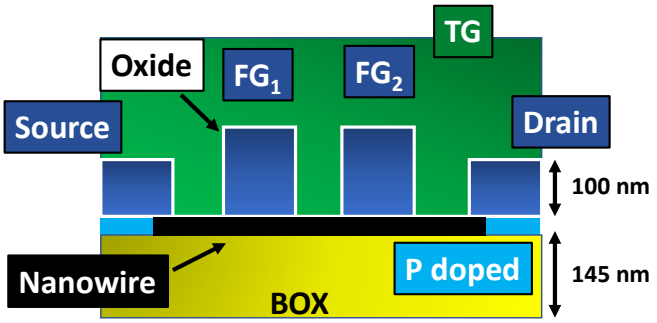



FIGURE 6.3: Device cross-section with gate stack, source/drain and oxide visible.

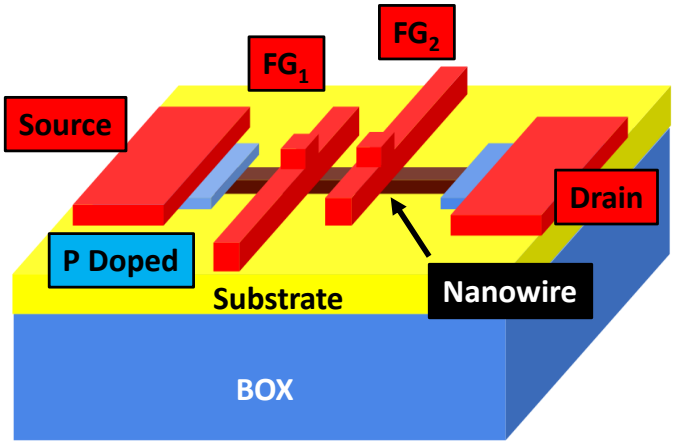



FIGURE 6.4: 3D schematic of a standard device design with the nanowire, source/drain and $FG_1$ and $FG_2$ shown (TG removed for display purposes).

### 6.2.1 Nanowire definition

The initial fabrication step is that of nanowire definition. The nanowires are formed via a bottom up process, consisting of thinning the SOI, followed growing an $SiO_2$ layer and coating hydrogen silsesquioxane (HSQ) on top. The SOI was reduced from 100 nm to 24 nm via oxidising the Si layer at 1000 °C and then removing the resulting $SiO_2$ by hydrofluoric acid (HF), after which 20 nm of $SiO_2$ was grown. A 30 nm HSQ layer was then deposited on top which was patterned by e-beam lithography and etched along with $SiO_2$ by Reactive ion etching (RIE) via an etching rate of HSQ to $SiO_2$ of 2:1, producing a 5 nm $SiO_2$ hard mask. After, the nanowire was wet etched with 25% TMAH solution (diluted with isopropyl alcohol (IPA)) to perform a 1500% over-etch. This was to ensure an atomically flat surface along the <111> plane. This is in contrast to the SET57 lot where ICP dry etching was utilised to achieve vertical etching of the nanowire. HF was then used to remove the hard mask, generating the trapezoidal structure as seen in Figure 6.5 for SET48.

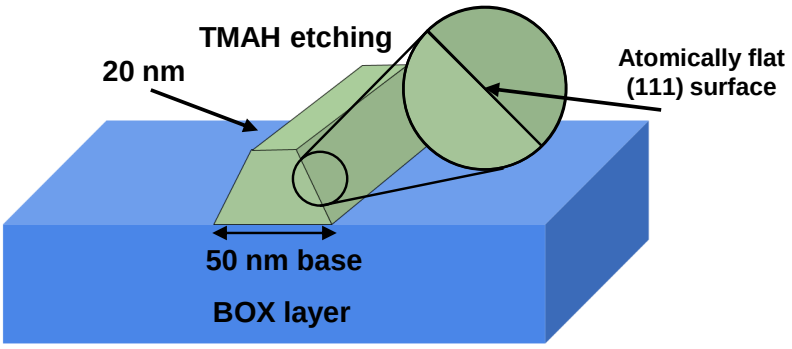



FIGURE 6.5: A diagram displaying the nanowire trapezoidal shape after tetramethylammonium hydroxide (TMAH) wet etching and removing the hard mask.

Figure 6.5 displays an SEM image of a nanowire with a designed diameter of 75 nm, however this was measured to be measured 64.3 nm as a result of the overetch.

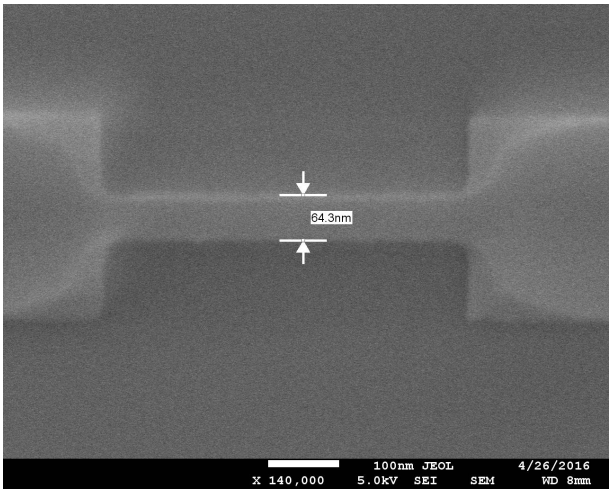



FIGURE 6.6: SEM image showing nanowire definition after Tetramethylammonium Hydroxide (TMAH), with a measured width of 64.3 nm for a nanowire with a designed width of 75 nm before an overetch was applied.

### 6.2.2 Dopant diffusion

Next, the nanowire was oxidised by thermally growing a 17.6 nm oxide (8 nm for SET57) to form the gate oxide. In order to open a window for the dopants to form the source and drain, the surface was coated with polymethyl methacrylate (PMMA950) resist and patterned by e-beam lithography. RIE was again used to etch away $SiO_2$ to create dopant diffusion windows as observed in the SEM in Figure 6.7.

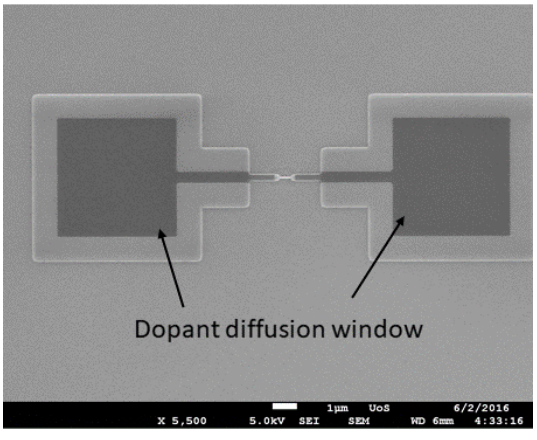



FIGURE 6.7: SEM image showing the dopant diffusion window for the source/drain.

Once the window was open, undoped poly-Si was deposited via low-pressure chemical vapour deposition (LPCVD) to form a raised source/drain structure. Raising the source

and drain aided in protecting the nanowire from any stray dopants entering. Doping was then achieved through a 'drive in' process, where phosphorus spin-on-dopant (SOD) diffused into the poly-Si via rapid thermal annealing (RTA) at 950 ° C in $N_2$, generating the source and drain regions

### 6.2.3 Patterning Finger gates

The first gates to be created were the 'finger gates', named after their shape. The FG poly-Si layer was formed at the same time as the raised source/drain structure which was described in Section 6.2.2, where after opening the dopant window, 100 nm of poly-Si was deposited. A HSQ layer was then patterned with e-beam and ICP etched the desired pattern to create the FGs and source/drain as displayed in Figure 6.8.

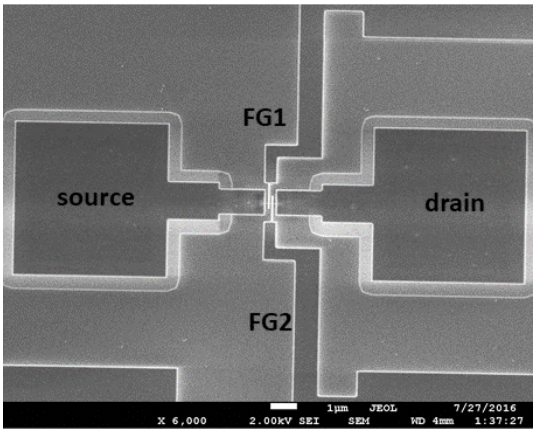



FIGURE 6.8: SEM image of nanowire device after FG and source/drain patterning.

An enhanced SEM image is given in Figure 6.9, where the raised source/drain and FG structures are easily identified. The nanowire and FG widths are 75 nm in Figure 6.9. The location of QD formation has also been superimposed onto the image for clarity.

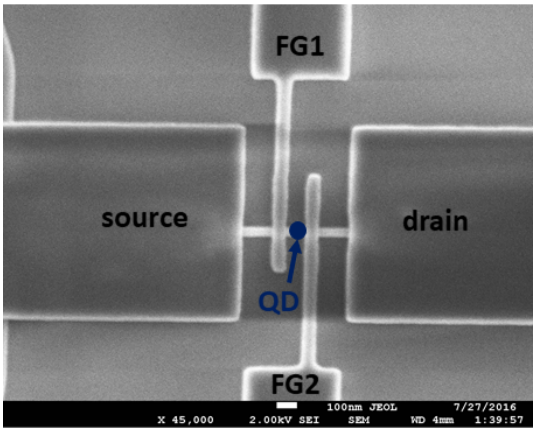



FIGURE 6.9: Higher magnification SEM image of nanowire device after FG patterning with the area of QD formation indicated.

### 6.2.4 Patterning Top gate

To prepare for the TG layer, the poly-Si surface was oxidised by RTA for 3 minutes at 950 ° C in $O_2$, to form 9 nm of $SiO_2$ to electrically isolate the FGs from TG. Using the same process as described in Section 6.2.2 and Section 6.2.3, poly-Si was deposited by LPCVD followed by SOD and RTA, where HSQ was again used for e-beam patterning which was then etched by ICP to form TG. The final result is displayed in Figure 6.10, which represents the front end of line steps coming to a conclusion.

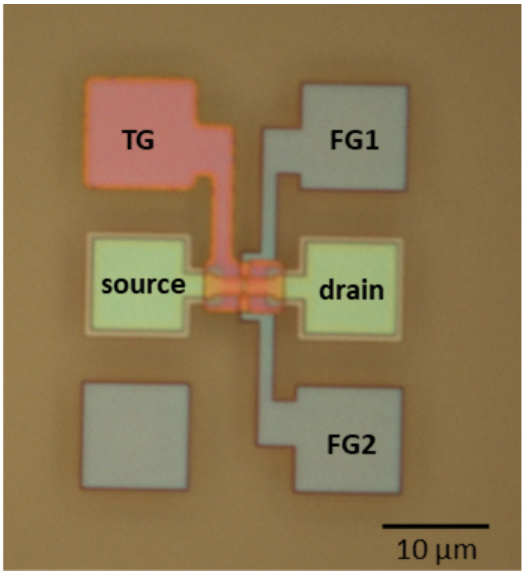



FIGURE 6.10: Optical image after TG patterning, where TG cover the entire device core area.

### 6.2.5 Contact and metallisation

Once TG was successfully patterned, a 250 nm thick oxide was deposited via plasma-enhanced-chemical-vapor-deposition (PECVD) and annealed in the furnance to avoid contaminating the samples. ZEP resist was then coated on top and patterned by e-beam, followed by HF etching of the oxide to form contact holes to the poly-Si pads before metallisation. Figure 6.11 shows an optical image of device after etching the contact holes in the 5 pads, each square hole measured 2 $\mu$m.

For metallisation a process known as lift off was utilised. After etching away any native oxide on the poly-Si surface, PMMA resist was deposited and patterned through e-beam where 200 nm of Al was evaporated on top. With NMP as the developer in a ultrasonic bath, 'lift off' of the Al was then performed to create the metal layer. Optical images after this process are shown in Figure 6.12, where (a) depicts the location of Al contact with the poly-Si pads and (b) shows the device terminals which are probed during characterisation. Furnace annealing within a $H_2$ and $N_2$ environment was carried out

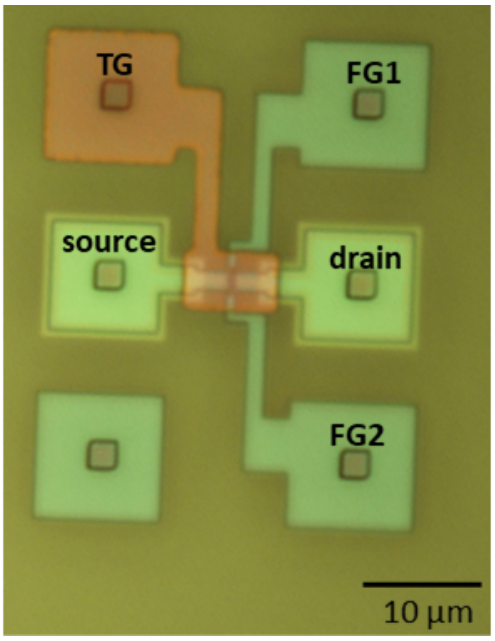



FIGURE 6.11: Optical image after contact holes are made in the device pads before metallisation.

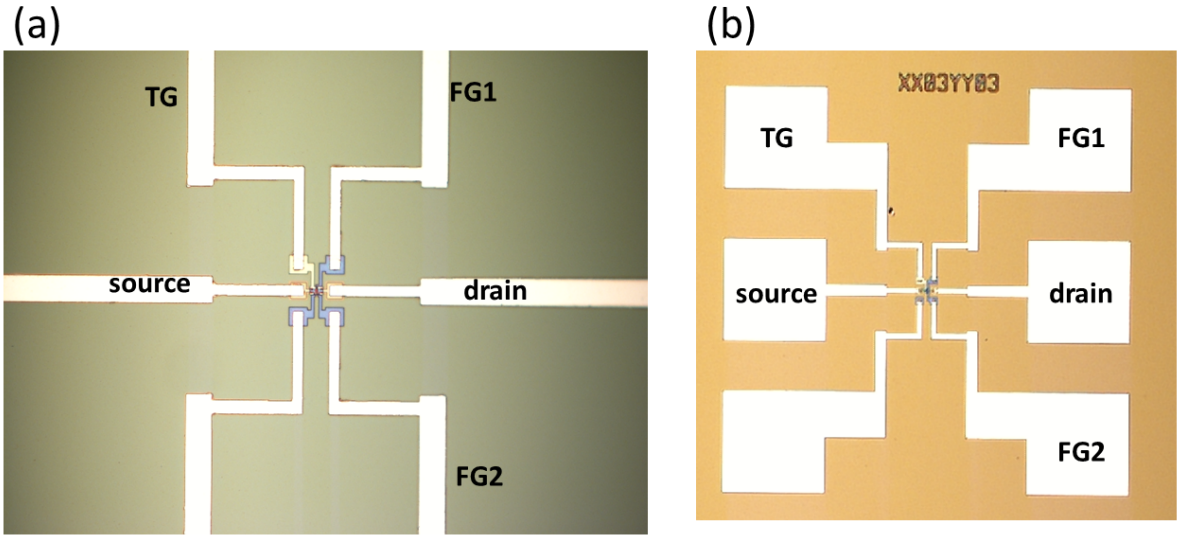



FIGURE 6.12: (a) Optical image after metallisation. (b) Optical image of an entire completed device with aluminium pads visible

as a final step at 450 °C in order to improve the metallisation contact. Finishing this step marked the end of the fabrication process to produce wafers of completed devices. Validation was then required to check the yield and device quality.

TABLE 6.3: Four-wafer fabrication summary of metal stack test.

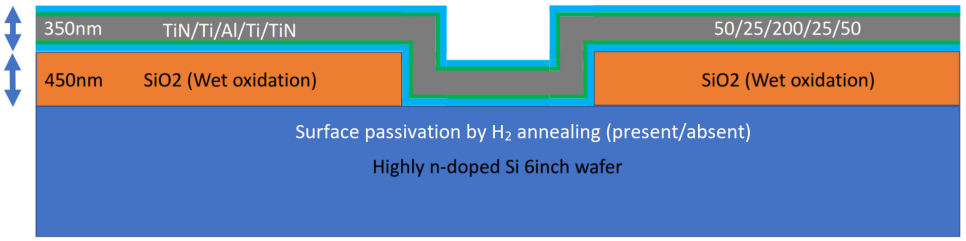
| Wafer No. | Purpose | Metal stack | Pad size($\mu$) | $R_c$ ($\Omega$) |
|---|---|---|---|---|
| 1 | TiN no anneal | TiN/Ti/Al/Ti/TiN | 5000 | 92 |
| 1 | TiN no anneal | TiN/Ti/Al/Ti/TiN | 50 | 2.0x10$^6$ |
| 2 | Al no anneal | Al | 5000 | 31 |
| 2 | Al no anneal | Al | 50 | 35 |
| 3 | TiN with anneal | TiN/Ti/Al/Ti/TiN | 5000 | 112 |
| 3 | TiN with anneal | TiN/Ti/Al/Ti/TiN | 50 | 1.9x10$^6$ |
| 4 | Al with anneal | Al | 5000 | 18 |
| 4 | Al with anneal | Al | 50 | 56 |

### 6.2.6 TiN/Ti/Al metal stack investigation

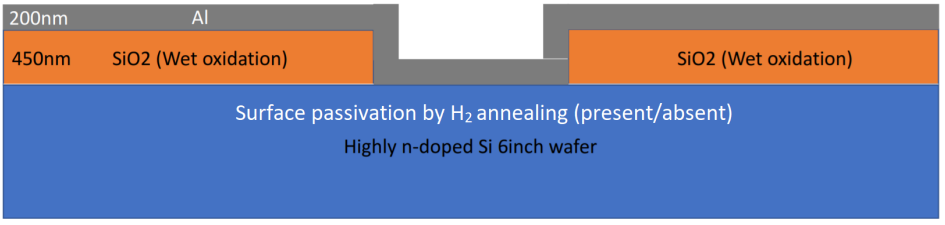
In order to optimize the electrical contact for SET57 compared to SET48, a lot was designed and fabricated to test a different metal stack structure which make contact to the poly-Si device pads, consisting of both TiN and Ti for capping the Al layer. SET48 devices did not have a TiN/Ti layer, only Al, which risked low device yield as a result of Al diffusion into the nanowire that Ti could possibly prevent. Therefore the main purpose was to check the electrical effect of a TiN/Ti structure via resistance measurements. This lot consisted of four wafers: wafers 1 and 3 had a TiN/Ti/Al/Ti/TiN layer with thicknesses of 50/25/200/25/50, where as wafers 2 and 4 only had a 200 nm Al layer. The distinction between each sub-lot (1 and 3, and 2 and 4) was simply an additional check to verify the necessity of surface passivation via annealing with $H_2$. A summary of the four wafer split is displayed in Table 6.3. Figure 6.13(a) displays a schematic of the metal stack structure for wafers 1 and 3, and Figure 6.13(b) for wafers 2 and 4. The metal pad layout is shown in Figure 6.13(c), where 8 different pad size widths from 5000 $\mu m$ to down to 50 $\mu m$ (sample pad size) were fabricated to check how scaling effects electrical contact.

The probe-station, as detailed in Chapter 3, was used to carry out $I-V$ measurements in order to calculate the contact resistance ($R_c$) from the surface to the wafer chuck, as a way to assess the metal stack interface quality for each wafer. One SMU was connected to a prober tip on the surface of a metal pad, where as another SMU was connected to the back of the wafer, which due to the substrate being highly n-doped was conductive. As the voltage was swept, the current between the metal surface and wafer back was measured, this allowed the resistance to be calculated by simply using Ohms law. After calculating the resistances, it became clear that the TiN/Ti/Al/Ti/TiN stack of wafers 1 and 3 lead to much larger $R_c$ for small pad sizes when compared to Al alone as demonstrated in Table 6.3. Initially the resistances of wafers 2 and 4 were 31 to 35 $\Omega$ and 18 to 56 $\Omega$ respectively with little dependence on pad size. In comparison, for wafers 1 and 3 $R_c$ was measured to be 92-112 $\Omega$ for 5000 $\mu m$, which then increased dramatically to 2 M$\Omega$ and 1.9 M$\Omega$ at a pad width of 50 $\mu m$ respectively. The effect of

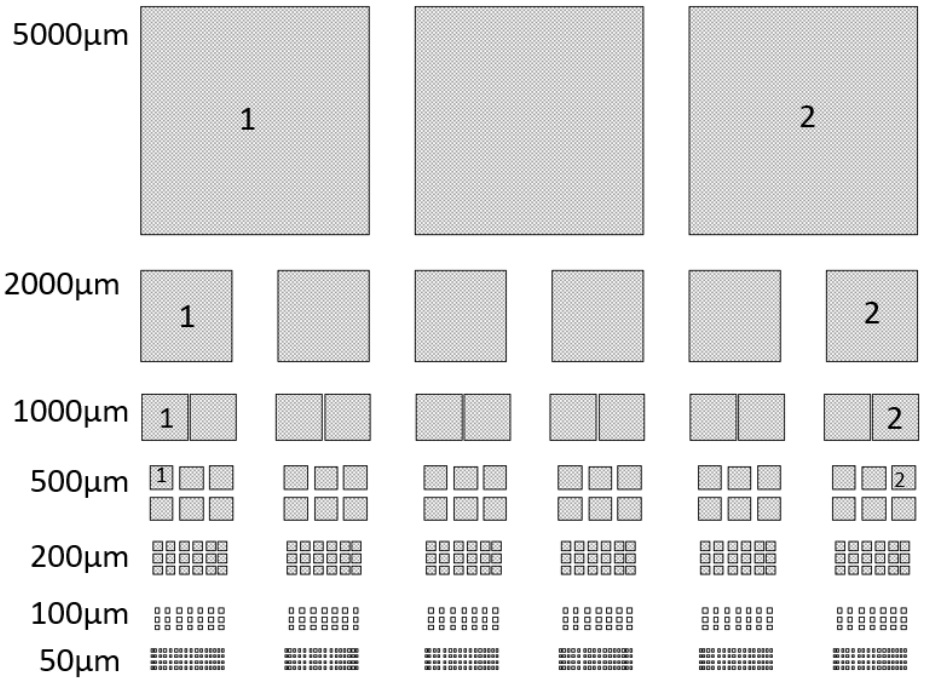
annealing proved to be negligible in comparison to the choice of metal stack. The reasoning as to why small pad widths were greatly affect is believed to be the result of far fewer conductive paths through the stack due to poor interface quality. The discovery of an exponentially increasing $R_c$ as pad sized decreased was crucial in ruling out TiN/Ti as a capping layer for Al. Therefore, SET57 was fabricated with only an Al layer.




(a) Schematic of wafers 1 and 3, with a TiN/Ti/Al/Ti/TiN metal stack on top of a n-doped conductive substrate. Wafer 1 was not annealed, where as wafer 3 was annealed in a $H_2$ enviroment for surface passivation




(b) Schematic of wafers 2 and 4, with only an Al layer on top of a n-doped conductive substrate. Wafer 2 was not annealed, where as wafer 4 was annealed in a $H_2$ enviroment for surface passivation




(c) Metal pad layout for each wafer. Each row contained a pad with a different width to check the resistance dependence on pad size. Two pad of each size were measured to calculate an average.

FIGURE 6.13: Schematics for the metal stack structures of the four wafers as well as the pad layout and sizes for electrical measurements.

## 6.3 Device yield check

Once fabrication had been completed, the devices which are most likley to function (based on optimal design parameters) are characterised first at the wafer scale via the probe-station and B1500A semiconductor analyser. Figure 6.14 shows the probe-station microscope screen with the Al nanowire sample pad. Contact is initiated between the probe tip and source/drain, TG and $FG_1$/$FG_2$. Initial validation measurements were identical for SET48 and SET57, which consisted of $V_{SD}$ fixed at 50 mV while one gate TG, $FG_1$ or $FG_2$ is swept and the others, including the drain, were grounded. Figure 6.15 displays the $I-V$ transfer characteristics from SET48 with a nanowire width of 50 nm and FG width/spacing of 100 nm/ 100 nm. Obtaining a strong TG modulation is especially important even though $FG_1$ and $FG_2$ are crucial for QD formation, since TG is needed to invert the channel and source/drain region, after which tuning the QD barriers and energy levels with the FGs can be achieved. Figure 6.15 shows the TG transfer characteristic where excellent modulation is observed. For this particular device, $FG_1$ and $FG_2$ in (b) and (c) also exhibited good modulation, where the response from both FGs is very similar aside from a slightly negative $V_{th}$ shift for $FG_1$. Therefore such a device would make a promising candiate to prepare for low temperature single electron transport characterisation. Due to the number of samples fabricated, this was the chosen method of measurement. Out of a total of 736 devices, 98 were found to be fully working (all three gates showed some modulation). The primary cause for devices to fail on wafer 4 (the only wafer to be successfully fabricated, as summarised in Table 6.1) was primarily open circuits, where no modulation is observed, as well as short circuits between the gates and source/drain.

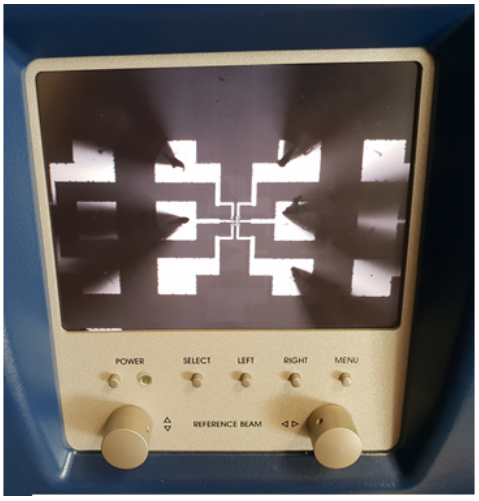



FIGURE 6.14: Probe-station microscope image of nanowire device during the validation process

The same measurement procedure is carried out for SET57 and the typical device transfer characteristics are given in Figure 6.16 for a device with a nanowire diameter of 40 nm and FG width/spacing of 100 nm / 100 nm. The most striking feature when comparing Figure 6.15 (a) and Figure 6.16 (a) is the sub-threshold swing under TG modulation. The gradient for the SET48 sample is clearly far steeper in comparison to SET57 device. Since TG is arguably the most important gate, obtaining such characteristics is a disaster for tunable quantum transport applications, even though the FGs showed some modulation (although weaker with reference to SET48). This was unfortunately a common theme for SET57. The explanation is likely due to ICP dry etching, as opposed to TMAH wet etching for SET48, which forms a rougher nanowire sidewall and therefore strongly affects its transport characteristics. Despite this, an increase in the total device yield for SE57 was achieved, where out of 1076 samples fabricated, 192 were discovered to be fully functioning with a total yield of 17.8%, in contrast to 12.8% for SET48. This can be attributed to the experienced gained following the first lot, where feedback was then integrated into SET57.

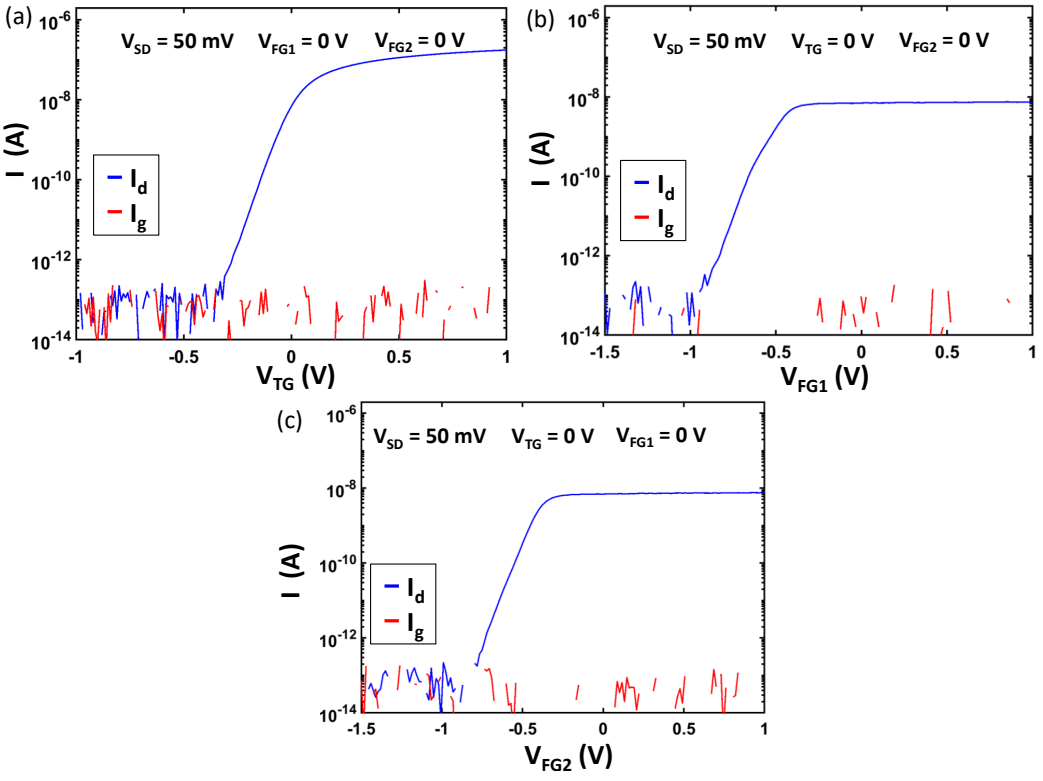



FIGURE 6.15: $I-V$ characteristics for a SET48 device with a nanowire diameter of 50 nm together with FG width and spacing equal to 100 nm. (a) displays a TG sweep, while (b) and (c) show FG1 and FG2 sweeps respectively at $V_{SD} = 50$ mV.

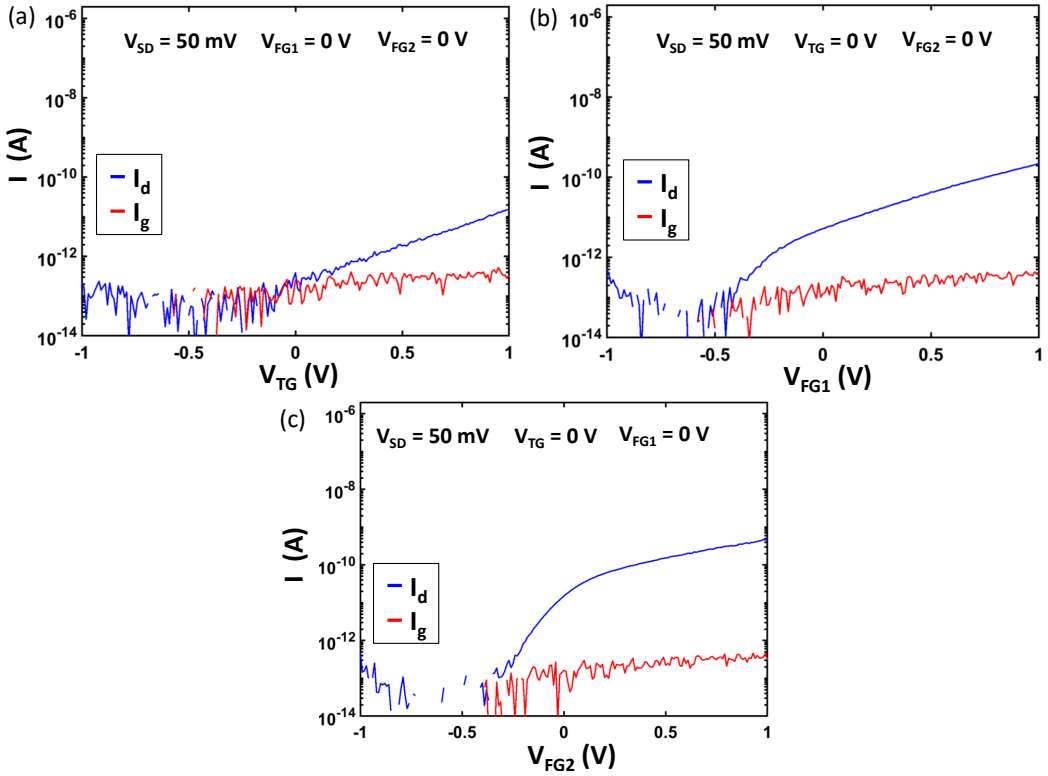



FIGURE 6.16: $I-V$ characteristics for a SET57 device with a nanowire diameter of 40 nm together with FG width and spacing equal to 100 nm. (a) displays a TG sweep, while (b) and (c) show FG1 and FG2 sweeps respectively at $V_{SD} = 50$ mV.

## 6.4 Back-end processing

This section is dedicated to processing steps following wafer scale validation, commonly referred to as back-end processing, which includes dicing/laser cutting, cleaning and preparations for low temperature measurement.

### 6.4.1 Laser cutting and cleaning

Once validation had been completed and fully functioning nanowire samples were identified, wafer 4 was diced into chips, and then laser cut into 2.5 mm x 2.5 mm sub-chips. The schematic is shown in Figure 6.17. The services of commercial company were employed who possessed a Nd:YAG laser, located at The Harwell Science and Innovation campus, Didcot, Oxford. The reasoning behind laser cutting into sub-chips was to acquire precision cut samples as well to avoid possible damage during the dicing process as a result of static discharge from sticky tape used in the process. The whole process from wafer, to chip and finally individual sub-chips is displayed in Figure 6.18.

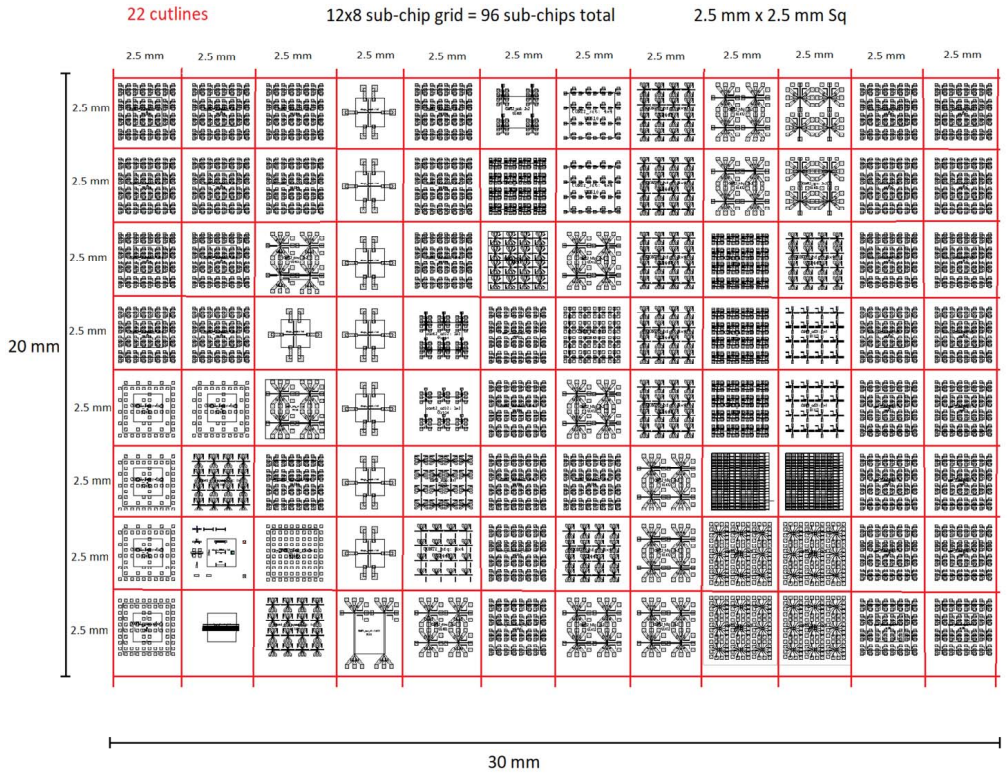
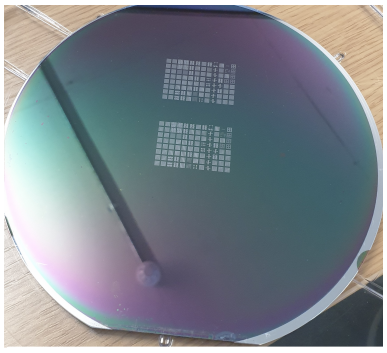
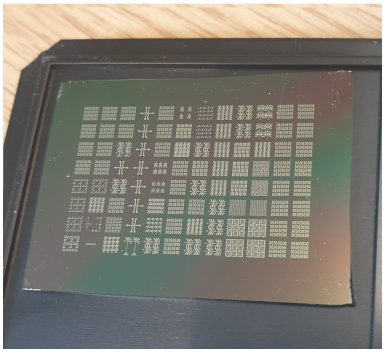



FIGURE 6.17: SET57 chip with lines added for laser cutting into 2.5 mm sub-chips



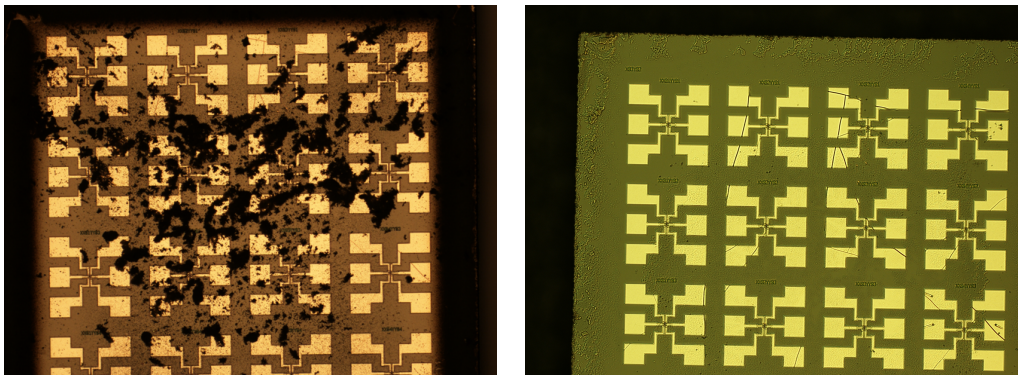
(a) Whole wafer with 2 chips



(b) Post diced chip

(c) Post laser cut sub-chips

FIGURE 6.18: Dicing and laser cutting samples from SET57



(a) Sub-chip post laser cutting with a significant amount of debris on the sample surface

(b) Clean sub-chip after acetone, IPA and ultrasonic NMP bath for 30 seconds

FIGURE 6.19: Clean debris from device terminals after laser cutting

After laser cutting, it was discovered that each sub-chip had acquired a considerable amount of debris on the sample surface as shown in Figure 6.19(a). In some instances the debris completely covered the pad terminals, so an additional cleaning process was necessary. This process consisted of an acetone and IPA surface clean, followed by a 30 second ultrasonic NMP bath, followed by a further acetone, IPA and water rinse. The result is displayed in Figure 6.19(b), a significant improvement. The sub-chips are then ready for the final stage before low temperature measurement, wire-bonding.

### 6.4.2 Wire-bonding

In order to characterise at the low temperatures needed to observe single electron transport, the sub-chips must be attached to a cryogenic sample holder and then wire-bonded for electrical contact. The first task was to fix the sub-chip onto the sample holder using a conductive silver-based glue, where a conductive medium ensures the sub-chip base is properly grounded. After annealing the glue by heating the sample and holder for 10 minutes at 150°C, the manual wire-bonder as described in Section 3.4.1 was used to bond a single device. An image taken through an optical microscope after successfully wire-bonding is shown in Figure 6.20. Here, the silver glue attached to the sub-chip base, together with the individual gold wires connecting the device terminal pads and sample holder contacts are visible. The final step required positioning the sample holder into the cryogenic probe insert, ensuring that good electrical contact is made. A successfully seated sample inside the probe insert is shown in Figure 6.21, which is then loaded into the cryostat before the cooling down process is initiated.

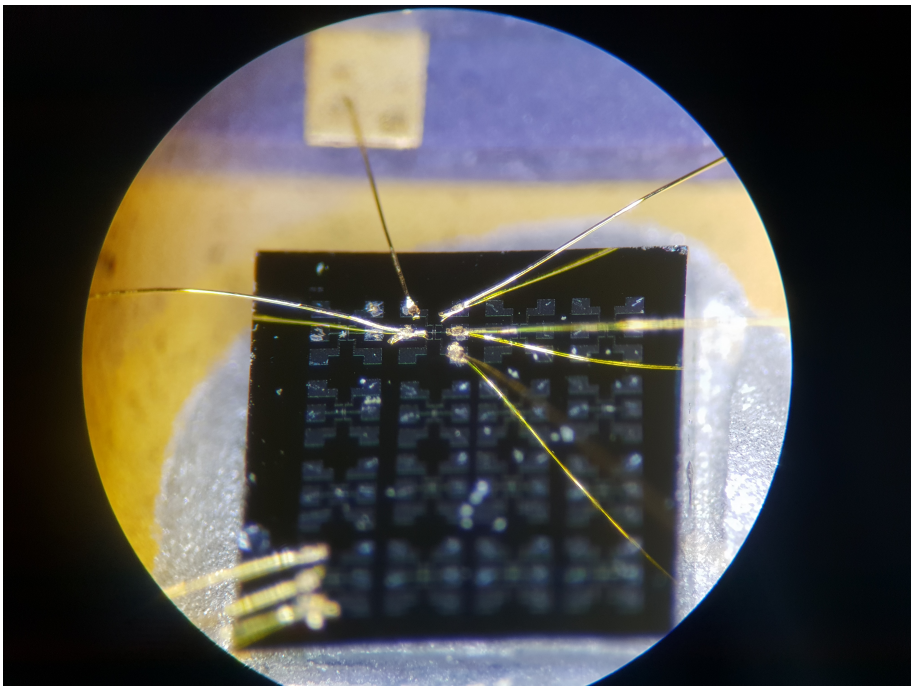


FIGURE 6.20: Wire-bonded SET48 device onto the cryostat sample holder viewed through a x20 zoom optical microscope lens

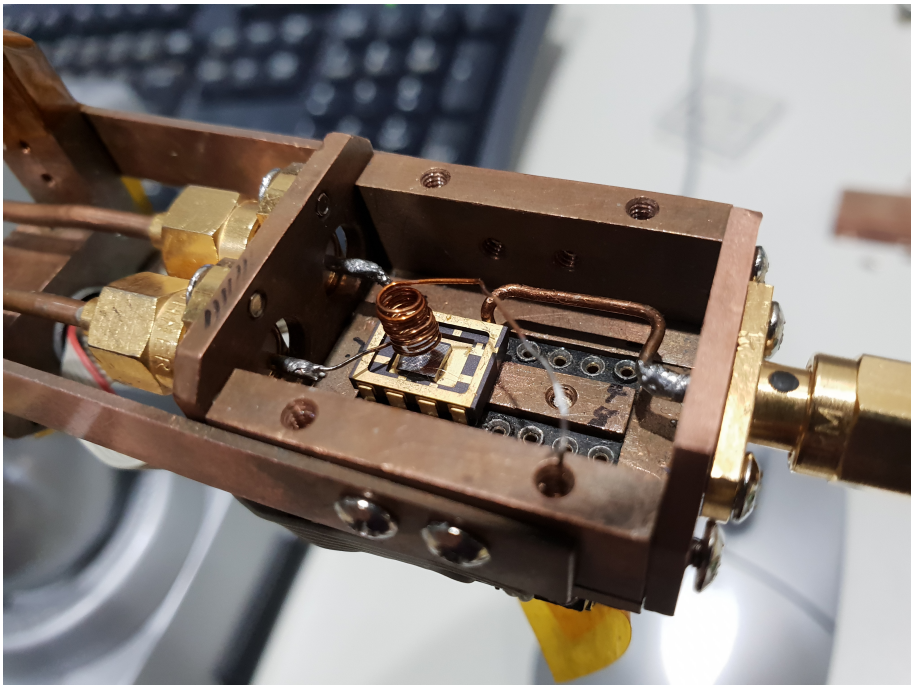


FIGURE 6.21: Nanowire device after loading into the probe insert for low temperature characterisation at The Riken Institute.

## 6.5 Low temperature characterisation

This section presents the low temperature results from two SET48 devices which are characterised at The Riken Institute via the Oxford Instruments LHe cryostat described in Section 3.3.1.

### 6.5.1 Single-QD transport

Once the sample is stabilised at T = 1.6 K, $I - V$ transfer characteristics are made for low $V_{SD}$ to determine the appropriate voltage parameters for TG and FG in order to observe Coulomb-diamonds. A charge-stability diagram (CSD) is then generated to identify the quantum transport parameters. Figure 6.22 displays CSD 1, where QD transport from two Coulomb-diamonds (highlighted) are observed as a consequence of a singular QD. The sample had a nanowire width and FG width/spacing of 100 nm/100 nm/150 nm respectively. $FG_1$ and $FG_2$ are both fixed at 0.5 V while TG is swept from 1 V to 2 V over a small $V_{SD}$ range (± 20 mV). For this device, TG voltages in excess of 2.5 V lead to a significant amount of gate leakage, meaning that negative FGs are out of the question since, as can be observed in Figure 6.22, when 0.5 V on the FGs is applied a $V_{TG}$ of 2 V is needed. This limited the device flexibility and hindered the creation of heavy confined QDs, as well as a double-QD system owing to the TG voltage window.

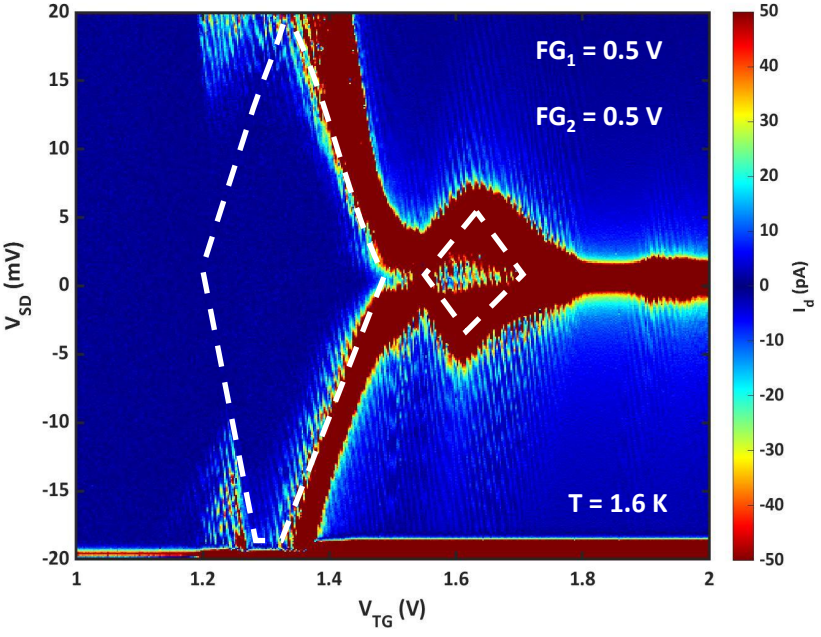



FIGURE 6.22: CSD 1, showing single QD transport observed for device 1 from an SET48 sample with a nanowire and FG width/spacing of 100 nm/100 nm/150 nm at T = 1.6 K. $V_{FG1}$ and $V_{FG2}$ are both fixed at 0.5 V, while $V_{SD}$ and $V_{TG}$ are swept from -20 mV to 20 mV and 1 V to 2 V respectively.

Based on this, CSD 2 is generated as seen in Figure 6.22, where FG voltages are increased to 0.8 V in order to sweep at reduced TG voltages over the same $V_{SD}$ range. A single, smaller Coulomb-diamond is identified (highlighted) as a likely consequence of the more positive bias on the FGs which increase the electrical size of the QD, as QD diameter is inversely proportional to Coulomb diamond width. At least two excited states are also visible on the lower left side of the Coulomb-diamond.

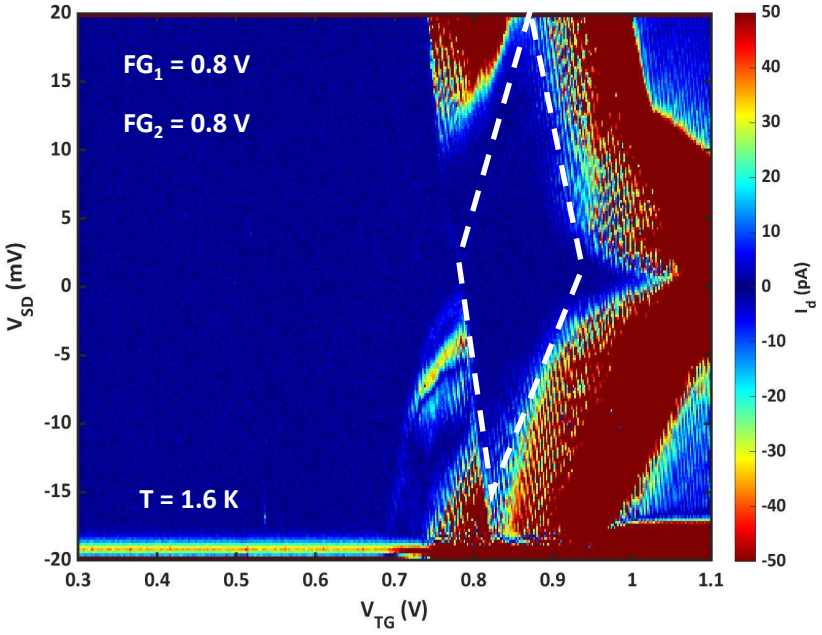



FIGURE 6.23: CSD 2, showing single QD transport for device 1, observed from an SET48 sample with a nanowire and FG width/spacing of 100 nm/ 100 nm/150 nm at T = 1.6 K. $V_{FG1}$ and $V_{FG2}$ are both fixed at 0.8 V, while $V_{SD}$ and $V_{TG}$ are swept from -20 mV to 20 mV and 0.3 V to 1.1 V respectively.

In spite of this, key QD parameters are investigated using both CSDs to assess the electrical characteristics of the system, where the QD diameter ($d_{\mathrm{QD}}$), charging energy ($E_c$), gate capacitance ($C_g$), and lever arm parameter ($\alpha$) are calculated. This is achieved through the following equations [86]:

$$E_{\mathrm{c}} = \frac{e^2}{C_{\Sigma}} \tag{6.1}$$

$$C_{\mathrm{g}} = \frac{e}{\Delta V_{\mathrm{g}}} \tag{6.2}$$

$$\alpha = \frac{V_{\mathrm{SD}}}{V_{\mathrm{g}}} \tag{6.3}$$

$$C_{\mathrm{eff}} = \epsilon_{\mathrm{ox}}/t_{\mathrm{eff}} \tag{6.4}$$

$$S_{\mathrm{QD}} = C_{\mathrm{g}}/C_{\mathrm{eff}} \tag{6.5}$$

$$d_{\mathrm{QD}} = \sqrt{4S_{\mathrm{QD}}/\pi} \tag{6.6}$$

TABLE 6.4: Electrical characteristics analysis summary of SET48 sample from single-QD data in Figure 6.22 and Figure 6.23.

| CSD No. | FG (V) | $E_c$ (meV) | $C_g$ (aF) | $\alpha$ | $d_{QD}$(nm) |
|---|---|---|---|---|---|
| 1 | 0.5 | 22.0 | 69 | 0.09 | 219 |
| 2 | 0.8 | 15.2 | 101 | 0.09 | 273 |

where $e$, $C_\Sigma$, $\epsilon_{ox}$, $t_{eff}$ and $S_{QD}$ are elementary charge, total capacitance respectively, permittivity of the oxide, effective oxide thickness and QD surface area. $E_c$ represents the energy required to add an additional electron to the QD (from the Coulomb diamond height in $V_{SD}$ voltage space), and finally $C_g$ and $\alpha$ are associated with the strength of the coupling between a given confined level and the gate. The results from applying these equations to each of the large Coulomb-diamonds highlighted in Figure 6.22 and Figure 6.22 are given in Table 6.4. Both of the QDs generated a matching $\alpha$ value alluding to the fact that they originate from the same location, and hence, posses the same TG coupling and controllability. However, Table 6.4 does highlight that the QDs differed in diameter, where the Coulomb-diamond in CSD 1 is 30% smaller than CSD 2, which is also reflected in $C_g$ and $E_c$. Such an effect can be ascribed to the greater FG bias of 0.8 V in comparison to 0.5 V in Figure 6.23 and Figure 6.22 respectively. The reasoning is that a more positive FG bias creates a wider potential profile, and thus, a larger QD between the FGs. The ability to alter the Coulomb-diamond shape and size altered as a product of the gate voltage applied therefore demonstrated some tunability. The $d_{QD}$ magnitude of 200-300 nm indicates that the QD formed broadly in an elliptical shape since the nanowire had a base diameter of 100 nm. Therefore the QD formed not only between the FGs but also underneath the gates (due to the width/spacing is 100 nm/150 nm) as a result of the FGs inverting the channel during this measurement scheme.

### 6.5.2 Double-QD formation

The second SET48 sample measured at Riken is a device with nanowire diameter and FG width/spacings of 50nm/150nm/150nm respectively. In contrast to device 1 in Section 6.5.1, device 2 had stronger modulation for both TG and $FG_1$ and $FG_2$, although all gates still suffered from elevated gate leakage above voltage of $\approx$ 2.5 V. Figure 6.24 displays a CSD with FGs fixed at 0.8 V (as with Figure 6.23) but with larger $V_{TG}$ and $V_{SD}$ applied. When studying Figure 6.24, the immediate difference between device 1 and 2 is the sheer number of Coulomb-diamonds, together with the $E_c$ magnitude. The ability cycle through around 30 Coulomb-diamonds, and therefore add around 30 electrons to the QD system over a 1 V $V_{TG}$ range, signifies a strong gate coupling, where as a large $E_c$ can be attributed to strong confinement as a result of high $FG_1$ and $FG_2$ modulation.

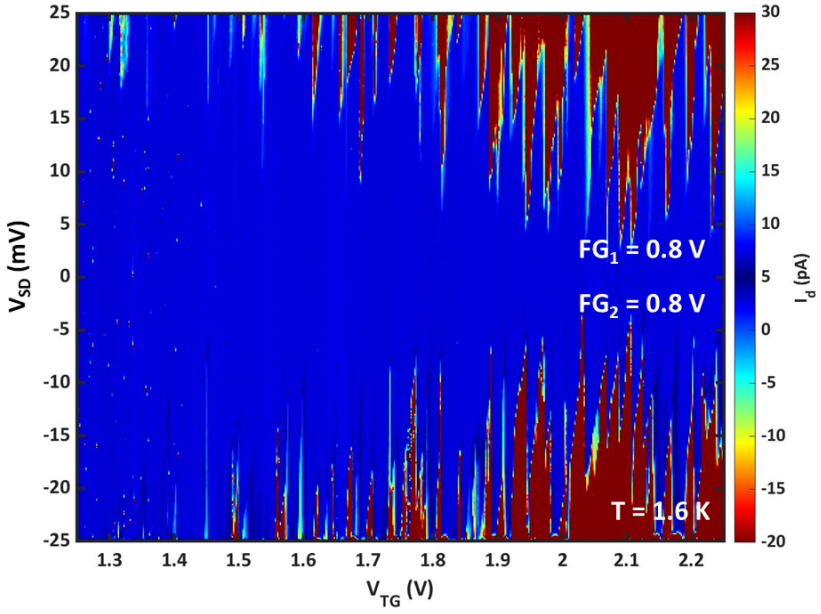



FIGURE 6.24: CSD displaying single electron transport for device 2 through a series Coulomb-diamonds from an SET48 sample with nanowire and FG width/spacing of 50 nm/150 nm/150 nm respectively at T = 1.6 K. $V_{FG1}$ and $V_{FG2}$ are both fixed at 0.8 V, while $V_{SD}$ and $V_{TG}$ are swept from -25 mV to 25 mV and 1.25 V to 2.25 V respectively. It is estimated that the QDs contain more than 30 electrons when $V_{TG}$ = 2.25 V.

To further investigate this more fruitful device, $FG_1$ and $FG_2$ are increased to 1.6 V and the $V_{TG}$ range is narrowed to 1.25 V to 2.25 V, in order study in detail the QD composition and charging configurations. The result is the CSD shown in Figure 6.25. From this, multiple, well defined and overlapping Coulomb-diamonds are observed where the two particular QDs are highlighted (in pink and white). A double-QD transport scheme is thought to have arisen due to the strong FG modulation, which makes more confined QD potential profiles possible. This led to a completely different system created with reference to device 1, in that a single potential profile is able to separate into two distinct QDs even though both the FGs and TG are positively biased. A physical representation of this scenario, with the device and energy level diagram is displayed in Figure 6.26 for clarity. From the equations given in 6.1-6.6, the $d_{QD}$ of both $QD_1$ and $QD_2$ are determined to be 76 nm and 86 nm respectively. These values are more agreeable for a 50 nm nanowire with 150 nm width FGs which are utilised to form the confining potentials.

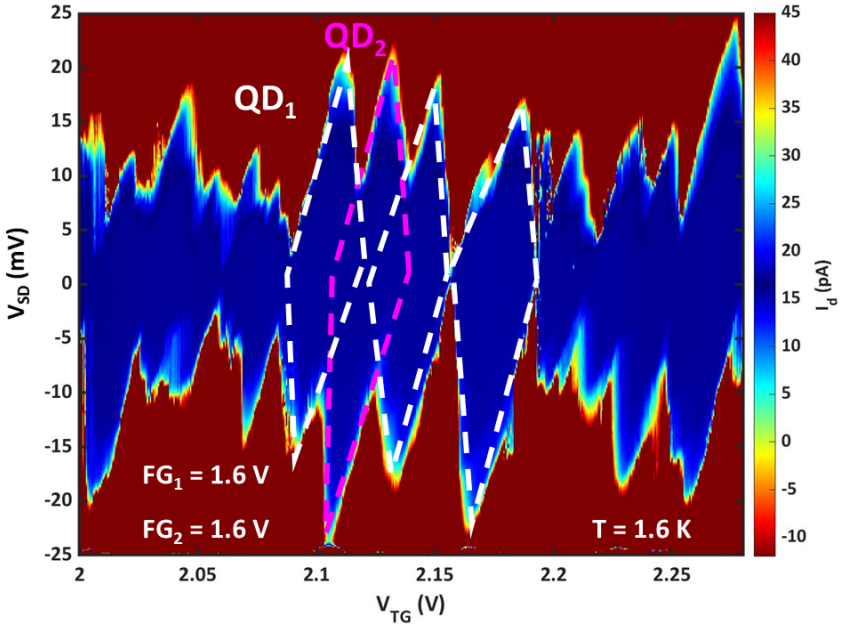



FIGURE 6.25: CSD showing double-QD transport observed for device 2 from an SET48 sample with nanowire and FG width/spacing of 50 nm/150 nm/150 nm respectively at T = 1.6 K. $V_{FG1}$ and $V_{FG2}$ are both fixed at 1.6 V, while $V_{SD}$ and $V_{TG}$ are swept from -25 mV to 25 mV and 2 V to 2.3 V respectively. The overlapping of the highlighted Coulomb-diamonds suggests two QD are present, and are of a similar size.

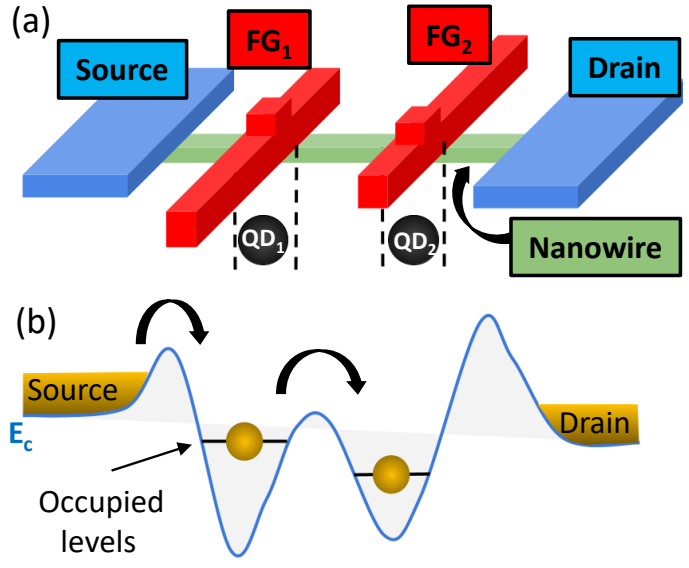



FIGURE 6.26: (a) Device schematic showing the formation of two QDs below $FG_1$ and $FG_2$. (b) Energy level diagram of how conduction band bending enables discrete levels to form as a product of quantum confinement.

### 6.5.3 Difficulties when characterising SET57

The low temperature characterisation results presented within this chapter were collected using samples from lot SET48 only. This is a product of three main factors:

- SET57 devices had poorer transistor characteristics from weak gate modulation in comparison to SET48, which meant even greater voltages were needed to be applied at low temperatures due to threshold shift.
- During the wire-bonding process, the transistor characteristics always became worse, which led to even worse gate modulation that needed to be compensated for.
- The SET48 samples were wire-bonded at Riken using well grounded equipment located next to the measurement system, where as all SET57 samples were characterised at Southampton in environments which were more prone to static discharge and therefore led to device damage.

## 6.6 Summary

Two batches of Si nanowire devices were successfully fabricated at The University of Southampton, with the yield increasing from 12.8% to 17.8% for the first and second lot respectively. This is an achievement in itself, given that this project consisted of complicated fabrication processes undertaken within a university clean-room where contamination is more likely to be an issue, and a such, is a testimony to both the universities clean-room protocols and the lead project fabricator's ability.

Following room temperature validation, two devices were characterised at low temperatures where single electron transport was confirmed. The tunable FG structure together with global TG control, enabled both single-QD and double-QD transport features to be analysed. The calculated $d_{QD}$ values confirmed the origin of the QDs to be a product of inversion due to the FGs, and as a result of quantum confinement, led to discrete charging and single electron transport which was observed through TG operation.

# Chapter 7

# Conclusions

To conclude, there were three main outcomes of this PhD project. Firstly, pseudo control over the QD confinement potentials originating at the Si-oxide interface was achieved as a consequence of well tuning. As a result, the energy level alignment and coupling between two QDs was shifted and allowed double QD transport phenomena to be probed in a disorder based QD system. This enabled spin related transport properties to be investigated through PSB, producing a significantly short $l_{SO}$ of 250 nm as well as a $t_c$ of 57 $\mu$eV. This outcome therefore highlights a path for exploring alternative quantum information technologies through the use of disorder based QDs by accommodating their advantageous SO properties at the interface on an accessible platform such as industry standard Si MOSFETs. Secondly, after successfully repairing and developing the cryogen free measurement system at Southampton for sustained low temperature use, electrical stress was implemented as a new method to selectively modify single hole transport characteristics in p-type MOSFETs. When applying stress up to $V_{g,max}$ = -4.6 V the QD charging energies were found to become enhanced, with reproducible changes following thermal cycles owing to stable device operation. A threshold was reached at further greater biases however, and a crossover occurred where the benefits were diminished from instability and poorer performance on account of large-scale oxide tunnelling and trap generation. Therefore, applying systematic stress demonstrated consistent operation, where useful the attributes outlined are proposed to be advantageous towards quantum transport applications including single hole transistors and single charge memory devices. As such, the beneficial transitions in device characteristics are worth considering given the VLSI platform.

Finally, a batch of Si nanowire devices were successfully fabricated producing a total yield of 17.8%, which was improvement considering a total yield of 12.8% for the previous batch. A TiN/Ti layer was suggested to improve the metal stack by limiting Al diffusion, however, after investigations via a test lot it was found to increase $R_c$ exponentially as pad sized decrease owing to poor Ti/Al interface quality, and hence was ruled

out as a metal stack option. Although the fully functioning devices were discovered to possess significant fragility, which often resulted in nanowire failure after wire-bonding and cooling down, two devices exhibited single and double QD behaviour. Therefore, the in-house fabricated multi-gate Si nanowires demonstrated flexibility through tunable, barrier-formed QDs, from the observed single electron transport characteristics.

Based on the work undertaken during this project, disorder QDs in Si MOSFETs provided an excellent platform to explore single hole spin interactions and transport through added tunability as a product of the well and electrical stress. However it should be noted that single hole transport here is only possible owing to QD formation in such devices as a result of defects at the interface. Whether they are local to the gate, such as poly-Si grains and traps, or other impurities such as single dopants which create variable potential profile, are largely a natural consequence of stochastic processes. Although the inability to control the number of QDs in this type of system remains, the use of the well allowed control over the transport properties within a multi-level system which lead to the emergence of PSB. The creation of such a configuration yielded a relatively strong SO interaction given the $l_{SO}$ extracted, which is likely attributed to inversion asymmetry at the interface. Therefore these results support engineering strong SO interactions at the interface in Si, with focus on exploring the useful properties of disorder QDs, particularly at the Si-oxide interface. This may well be of interest for industries where standard MOSFETs can act as a testing platform for quantum information processing schemes.

The stress technique put forward offers a path towards tuning charging characteristics in a controllable and reversible way that enables Si MOSFETs to perform as optimized QD devices. Although the nature of the material and device specific stress mechanism will always lead to some variability, hence more work must be done to gain a better insight. Therefore a balanced approach is needed to limit trap generation, in order for QDs to remain stable, but also still allow the trapping of some charge to initiate beneficial changes. In addition, when using the Coulomb-diamond structure as a PUF (unique fingerprint) for transistors, the variation induced by stress to Coulomb-blockade should be considered when developing applications for device identification and security purposes.

# Appendix A

# LabVIEW program creation for HP4142 source-meter

A retired HP4142 source-meter unit (Figure A.1) which was unused for over a decade was returned to operation use by having new SMUs installed, undergoing a calibration and then controlled through the creation of a new LabVIEW program. This was to acquire the ability to output a fixed voltage on 3 channels (as well as a grounding line), whilst sweeping the voltage on a 4th channel, in to characterise single electron pumps (SEPs) using Janis cryostat (Appendix B). The voltage and current values for each channel are saved to a .csv file. The sweeping voltage (x-axis) and the corresponding current measured on each channel (y-axis) are also displayed by four graphs during measurement Figure A.2.


FIGURE A.1: HP4142 measurement system after installation of new SMUs.

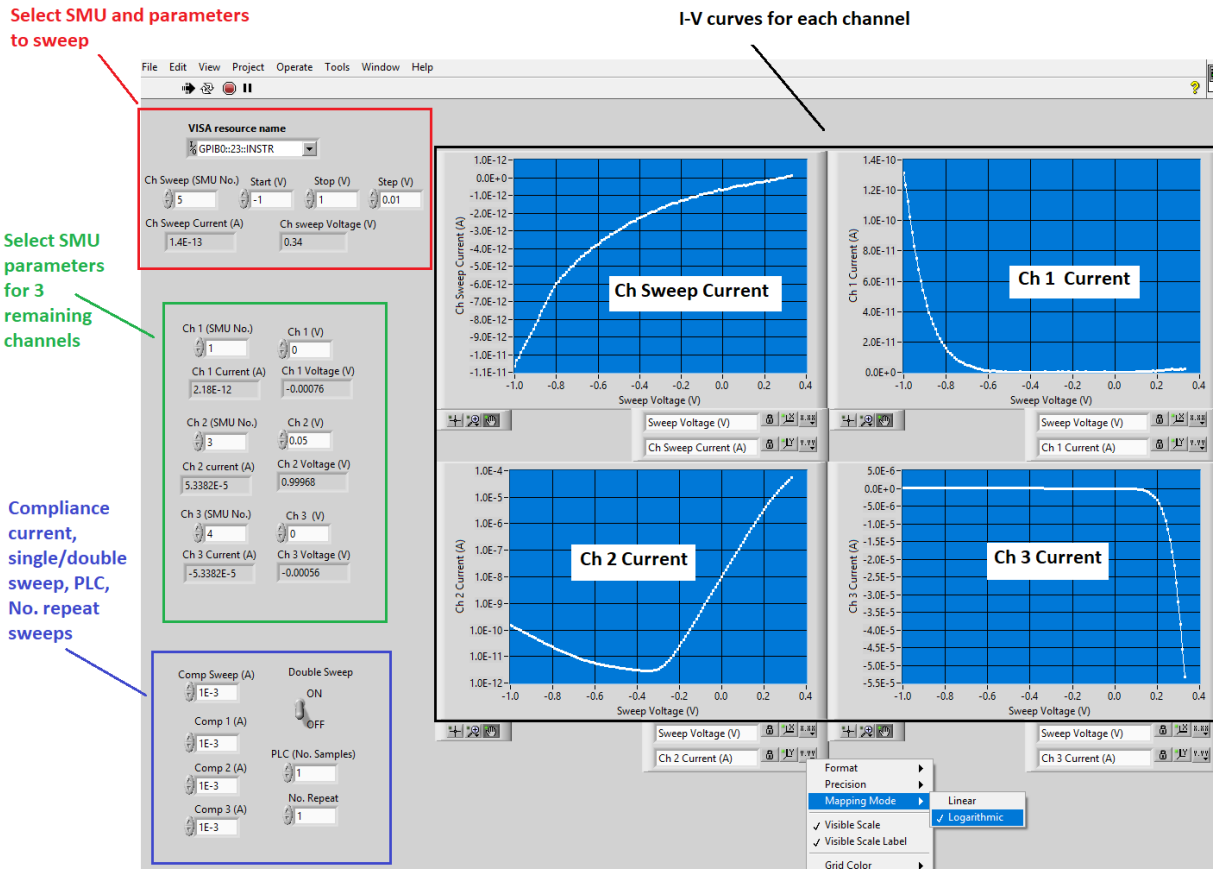



FIGURE A.2: LabVIEW program created to operate a HP4142 system for CMOS characterisation.

# Appendix B

# Janis cryostat development for single electron pumps

A Janis pulsed-tube (P-T) cryostat was re-developed as a low temperature system for high-frequency (HF) SEP measurements. This involved re-configuring what was previously a cryogenic optical setup, in order to characterise SEPs. This was achieved by reducing the significant amount of noise entering through the quartz windows within the radiation shield and then re-wiring the system with SMA cabling in order to be HF compatible for SEP operation (Figure B.1). In addition, a new sample holder was engineering and optimized by Dr. F. Liu to ensure the maximum amount HF signal reached the sample, where I then soldered the signal lines for contact, together with wire-bonding and loading. The sample holder is displayed in Figure B.2. Before the system became operational, I also replaced the diaphragm pump (1000 to 5 mBar range), in order to activate the turbo-molecular pump and reach the vacuum pressures required ($1x10^{-8}$ mBar). The entire functioning system is shown in Figure B.3 after performing a helium leak detector test followed by replacing damaged o-rings to vacuum seal the closed system.

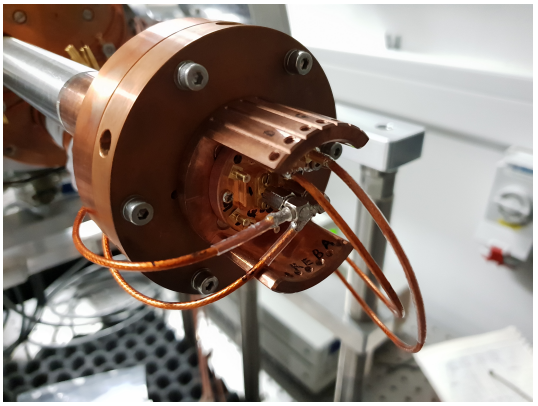


FIGURE B.1: Image taken of the Janis cryostat after re-wiring with SMA cables with new sample holder mounted.

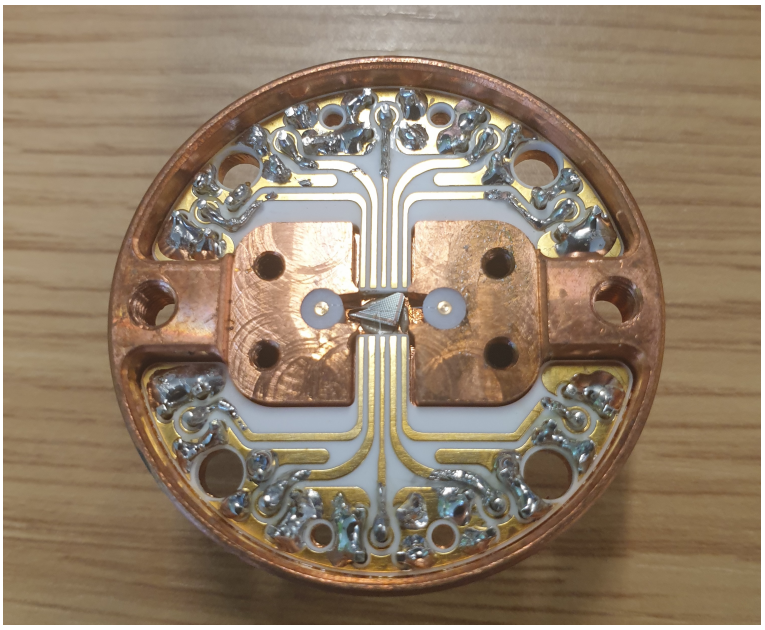


FIGURE B.2: Custom made HF sample holder designed for SEP operation using the Janis cryostat

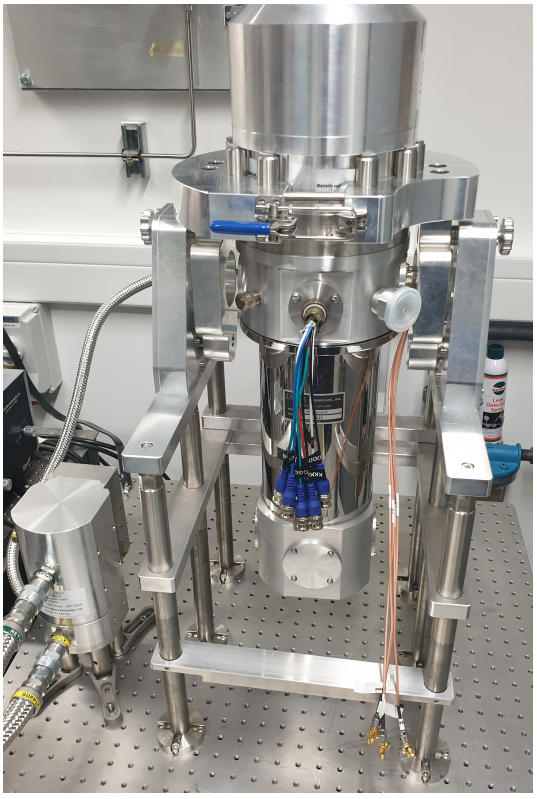


FIGURE B.3: Image of the entire Janis cryostat system with radiation shield and vacuum cover fitted, ready for the cool-down process.

# Appendix C

# List of publications

## C.1 Publications as first-author

**J. Hillier**, K. Ono, K. Ibukuro, F. Liu , Z. Li , M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi and S. Saito. Probing hole spin transport of disorder quantum dots via Pauli spin-blockade in standard silicon transistors. *Nanotechnology*, 32, 260001, 2021.

**J. Hillier**, K. Ibukuro, F. Liu, M. K. Husain, J. Byers, I. Tomita, H. N. Rutt, Y. Tsuchiya, and S. Saito. Investigating stability and tunability of quantum dot transport in silicon MOSFETs via the application of electrical stress. *J. Phys. D: Appl. Phys.* 55, 105107, 2022.

**J. Hillier**, K. Ono, K. Ibukuro, F. Liu , Z. Li , M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi and S. Saito. Single spin sensing in silicon p-type Metal-Oxide-Semiconductor Field-Effect Transistors. *International conference for the quantum science and technology community*, 3193, 2020.

**J. Hillier**, K. Ono, K. Ibukuro, F. Liu , Z. Li , M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi and S. Saito. Atomically flat trapezoidal silicon nanowires for tunable gate defined quantum dots. *Silicon Quantum Information Processing Workshop*, 2021.

## C.2 Publications as co-author

F. Liu, K. Ibukuro, M. K. Husain, Z. Li, **J. Hillier**, I. Tomita, Y. Tsuchiya, H. Rutt and S. Saito. Manipulation of random telegraph signals in a silicon nanowire transistor with a triple gate. *Nanotechnology*, 29, 47, 2018.

K. Ibukuro, M. K. Husain, M. Sotto, Z. Li, **J. Hillier**, F. Liu, I. Tomita, Y. Tsuchiya, H. Rutt, and S. Saito. Single Electron Memory Effect Using Random Telegraph Signals at Room Temperature. *Front. Phys.* 7, 152, 2019.

K. Ibukuro, F. Liu, M. K. Husain, M. Sotto, **J. Hillier**, Z. Li, I. Tomita, Y. Tsuchiya, H. Rutt, and S. Saito. Silicon single-electron random number generator based on random telegraph signals at room temperature. *AIP Adv.* 10, 115101, 2020.

K. Ibukuro, **J. W. Hillier**, F. Liu, M. K. Husain, Z. Li, Y. Tsuchiya, I. Tomita, H. Rutt and S. Saito. Random telegraph signals caused by a single dopant in a metal-oxide-semiconductor field effect transistor. *AIP Adv.* 10, 055025, 2020.

J. Byers, K. Debnath, H. Arimoto, Hideo, M. K. Muhammad, M. Sotto, **J. Hillier**, K. Kiang, D. J. Thomson, G. T. Reed, M. Charlton and S. Saito. 10 nm $SiO_2$ TM Slot Mode in Laterally Mismatched Asymmetric Fin-Waveguides. *Front. Phys.* 9, 237, 2021.

# Bibliography


[1] T. D Ladd, F. Jelezko, R. Laflamme, Y. Nakamura, C. Monroe, and J. L. O'Brien. Quantum computers. *Nature.*, 464:45, 2010.

[2] M. Veldhorst, H. G. J. Eenink, C. H. Yang, and A. S. Dzurak. Silicon CMOS architecture for a spin-based quantum computer. *Nat. Commun.*, 8:1766, 2017.

[3] W. Huang, C. H. Yang, K. W. Chan, B. Hensen T. Tanttu, R. C. C. Leon, M. A. Fogarty, F. E. Hudson J. C. C. Hwang, K. M. Itoh, A. Morello, A. Laucht, and A. S. Dzurak. Fidelity benchmarks for two-qubit gates in silicon. *Nature*, 569:532, 2019.

[4] E. Ferraro and E. Prati. Is all-electrical silicon quantum computingfeasible in the long term? *Phys. Lett. A*, 384:126352, 2020.

[5] and D.P. DiVincenzo D. Loss. Quantum computation with quantum dots. *Phys. Rev. A*, 57(1):120, 1998.

[6] Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa. *J. Phys. Condens. Matter*, 14:R995, 2002.

[7] R. Hanson, L. P. Kouwenhoven, J. R. Petta, S. Tarucha, and L. M. K. Vandersypen. Spins in few-electron quantum dots. *Rev. Mod. Phys.*, 79:1217, 2007.

[8] A. R. Stegner, C. Boehme, H. Huebl, M Stutzmann, K. Lips, and M. S. Brandt. Electrical detection of coherent 31P spin quantum states. *Nature Phys.*, 2:835, 2006.

[9] A. Morello, J. J. Pla, A. Zwanenburg, K. W. Chan, K. Y. Tan, H. Huebl, M. Mottonen, C. D. Nugroho, C. Yang, J. A. van Donkelaar, A. D. C. Alves, D. N. Jamieson, C. C. Escott, L. C. L. Hollenberg, R. G. Clark., and A. S. Dzurak. Single-shot readout of an electron spin in silicon. *Nature*, 467:687, 2010.

[10] H. G. J. Eenink, L. Petit, W. I. L. Lawrie, J. S. Clarke, and L. M. K. Vandersypen. Tunable coupling and isolation of single electrons in silicon metal-oxide-semiconductor quantum dots. *Nano. Lett.*, 19:8653, 2019.

[11] M. Xiao, M. G. House, and H. W. Jiang. Measurement of the spin relaxation time of single electrons in a silicon metal-oxide-semiconductor-based quantum dot. *Phys. Rev. Lett.*, 104:096801, 2010.

[12] C. H. Yang, A. Rossi, R. Ruskov, N. S. Lai, F. A. Mohiyaddin, S. Lee, C. Tahan, G. Klimeck, A. Morello, and A. S. Dzurak. Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting. *Nat. Commun.*, 4:2069, 2013.

[13] R. Maurand, X. Jehl, D. Kotekar-Patil, A. Corna, H. Bohuslavskyi, R. Lavie ville, L. Hutin, S. Barraud, M. Vinet, M. Sanquer, and S. De Franceschi. A CMOS silicon spin qubit. *Nat. Commun.*, 7:13575, 2016.

[14] URL https://www.imec-int.com/en/articles/moving-quantum-computing-lab-fab.

[15] J. R. Petta, A. C. Johnson, J. M. Taylor, E. A. Laird, A. Yacoby, M. D. Lukin, C. M. Marcus, M. P. Hanson, and A. C. Gossard. Coherent manipulation of coupled electron spins in semiconductor quantum dots. *Science*, 309:2180, 2005.

[16] C. H. Yang, A. Rossi, R. Ruskov, N. S. Lai, F. A. Mohiyaddin, S. Lee, C. Tahan, G. Klimeck, A. Morello, and A. S. Dzurak. Spin-valley lifetimes in a silicon quantum dot with tunable valley splitting. *Nat. Commun.*, 4:2069, 2013.

[17] Patrick Harvey-Collard, N. T. Jacobson, C. Bureau-Oxton, R. M. Jock, V. Srinivasa, A. M. Mounce, J. M. Anderson D. R. Ward, R. P. Manginell, J. R. Wendt, T. Pluym, M. P. Lilly, D. R. Luhman, M. Pioro-Ladri‘ere, and M. S. Carroll. Spin-orbit interactions for singlet-triplet qubits in silicon. *Phys. Rev. Lett.*, 122: 217702, 2019.

[18] S. Nadj-Perge, S. M. Frolov, J. W. W. van Tilburg, J. Danon, Yu. V. Nazarov, R. Algra, E. P. A. M. Bakkers, and L. P. Kouwenhoven. Disentangling the effects of spin-orbit and hyperfine interactions on spin blockade. *Phys. Rev. B*, 81:201305, 2010.

[19] A. Zarassi, Z. Su, J. Danon, J. Schwenderling, M. Hocevar, B. M. Nguyen, J. Yoo, S. A. Dayeh, , and S. M. Frolov. Magnetic field evolution of spin blockade in gesi nanowire double quantum dots. *Phys. Rev. B.*, 95:155416, 2017.

[20] G. Xu, F. Gao, K. Wang, T. Zhang, H. Liu, G. Cao, T. Wang, J. Zhang, H. Jiang, H. Li, and G. Guo. Hole spin in tunable ge hut wire double quantum dot. *App. Phys. Exp.*, 13(065002), 2020.

[21] M. Xiao, I. Martin, and H. W. Jiang. Probing the spin state of a single electron trap by random telegraph signal. *Phys. Rev. Lett.*, 91:078301, 2003.

[22] M. Xiao, I. Martin, E. Yablonovitch, and H. W. Jiang. Electrical detection of the spin resonance of a single electron in a silicon field-effect transistor. *Nature*, 430: 435, 2004.

[23] J. Li, S. Pud, M. Petrychuk, A. Offenhäusser, and S. Vitusevich. Sensitivity enhancement of si nanowire field effect transistor biosensors using single trap phenomena. *Nano. Lett.*, 14:3504, 2014.

[24] T. Tanamoto, Y. Nishi, and K. Ono. Application of single-electron effects to fingerprints of chips using image recognition algorithms. *Appl. Phys. Lett.*, 115: 033504, 2019.

[25] R. Li, F. E. Hudson, A. S. Dzurak, and A. R. Hamilton. Pauli spin blockade of heavy holes in a silicon double quantum dot. *Nano. lett.*, 15:7314, 2015.

[26] S. Shankar, A. M. Tyryshkin, Jianhua He, and S. A. Lyon. Spin relaxation and coherence times for electrons at the si/sio2. *Phys. Rev. B.*, 82:195323, 2010.

[27] P. Harvey-Collard, N. T. Jacobson, C. Bureau-Oxton, R. M. Jock, V. Srinivasa, A. M. Mounce, J. M. Anderson D. R. Ward, R. P. Manginell, J. R. Wendt, T. Pluym, M. P. Lilly, D. R. Luhman, M. Pioro-Ladri‘ere, and M. S. Carroll. Spin-orbit interactions for singlet-triplet qubits in silicon. *Phys. Rev. Lett.*, 122: 217702, 2019.

[28] A. Corna, and R. Maurand L. Bourdet, A. Crippa, D. Kotekar-Patil, H. Bohuslavskyi, R.Laviéville, L. Hutin, S. Barraud, X. Jehl, M. Vinet, S. Franceschi, Y. Niquet, and M. Sanquer. Electrically driven electron spin resonance mediated by spin–valley–orbit coupling in a silicon quantum dot. *npj Quantum Inf.*, 4:6, 2018.

[29] R. M. Jock, N. T. Jacobson, P. Harvey-Collard, A. M. Mounce, V. Srinivasa, J. M. Anderson D. R. Ward, R. P. Manginell, J. R. Wendt, M. Rudolph, T. Pluym, J. K Gamble, A. D Baczewski, W. M. WItszel, and M. S. Carroll. A silicon metal-oxide-semiconductor electron spin-orbit qubit. *Nat. Commun.*, 9:1768, 2018.

[30] S. Lee, Y. Lee, E. B. Song, and T. Hiramoto. Modulation of peak-to-valley current ratio of coulomb blockade oscillations in si single hole transistors. *Appl. Phys. Lett.*, 103(103502), 2013.

[31] Jun Yao, Zhengzong Sun, Lin Zhong, Douglas Natelson, and James M. Tour. Resistive switches and memories from silicon oxide. *Nano Letters*, 10(10):4105–4110, 2010. doi: 10.1021/nl102255r. PMID: 20806916.

[32] Mark Buckwell, Luca Montesi, Adnan Mehonic, Omer Reza, Leon Garnett, Manveer Munde, Stephen Hudziak, and Anthony J. Kenyon. Microscopic and spectroscopic analysis of the nature of conductivity changes during resistive switching in silicon-rich silicon oxide. *physica status solidi c*, 12(1-2):211–217, 2015. doi: https://doi.org/10.1002/pssc.201400160.

[33] J. Danon and Yu. V. Nazarov. Pauli spin blockade in the presence of strong spin-orbit coupling. *Phys. Rev. B*, 80:041301, Jul 2009. doi: 10.1103/PhysRevB.80.041301. URL https://link.aps.org/doi/10.1103/PhysRevB.80.041301.

[34] G. Yeap, X. Chen, B. R. Yang, C. P. Lin, F. C. Yang, Ying-Keung Leung, and D. W. Lin *et al.* 5nm CMOS Production Technology Platform featuring full-fledged EUV, and High Mobility Channel FinFETs with densest 0.021µm$^2$ SRAM cells for Mobile SoC and High Performance Computing Applications. *2019 IEEE International Electron Devices Meeting (IEDM)*, pages 36.7.1–36.7.4, 2019.

[35] Y. Cheng T. Ytterdal and T. A. Fjeldly. *Device Modeling for Analog and RF CMOS Circuit Design, 1.2.1 Interface Charge*. John Wiley and Sons, 2003.

[36] Y. Cheng T. Ytterdal and T. A. Fjeldly. *Device Modeling for Analog and RF CMOS Circuit Design 1.1 Introduction*. John Wiley and Sons, 2003.

[37] K. Ono, T. Tanamoto, and T. Ohguro. Pseudosymmetric bias and correct estimation of Coulomb/confinement energy for unintentional quantum dot in channel of metal-oxide-semiconductor field-effect transistor. *App. Phys. Lett*, 103:183107, 2013.

[38] J.F. Verweij and J.H. Klootwijk. Dielectric breakdown i: A review of oxide breakdown. *Microelectronics Journal*, 27:611–622, 1996.

[39] K. Ibukuro, F. Liu, M. K. Husain, M. Sotto, J. Hillier, Z. Li, I. Tomita, Y. Tsuchiya, H. Rutt, and S. Saito. Silicon single-electron random number generator based on random telegraph signals at room temperature. *AIP Adv.*, 10: 115101, 2020.

[40] Marc A. Kastner. Artificial atoms. *Physics Today*, 46(1):24, 1993.

[41] B. Zorman, M. V. Ramakrishna, and R. A. Friesner. Quantum confinement effects in cdse quantum dots. *Journal of Physical Chemistry*, 99:7649–7653, 1995.

[42] Gregory L. Timp. *Nanotechnology*. Springer, 1999.

[43] Xuedong Hu and S. Das Sarma. Overview of spin-based quantum dot quantum computation. *phys. stat. sol*, 2003.

[44] Michela Massimi. *Pauli's Exclusion Principle: The Origin and Validation of a Scientific Principle*. Cambridge University Press, 2005.

[45] J. Fransson and M. Råsander. Pauli spin blockade in weakly coupled double quantum dots. *Physical Review B*, 2006.

[46] Yehuda B. Band and Yshai Avishai. *Quantum Mechanics with Applications to Nanotechnology and Information Science*. ELSEVIER, 2013.

[47] H. W. Liu, T. Fujisawa, Y. Ono, H. Inokawa, A. Fujiwara, K. Takashina, and Y. Hirayama. Pauli-spin-blockade transport through a silicon double quantum dot. *Physical Review*, 77(073310), 2008.

[48] N. S. Lai, W. H. Lim, C. H. Yang, F. A. Zwanenburg, W. A. Coish, F. Qassemi, A. Morello, and A. S. Dzurak. Pauli spin blockade in a highly tunable silicon double quantum dot. *Scientific Report, Nature*, 2011.

[49] Bent Weber, Y. H. Matthias Tan, Suddhasatta Mahapatra, Thomas F. Watson, Hoon Ryu, Rajib Rahman, Lloyd C. L. Hollenberg, Gerhard Klimeck, and Michelle Y. Simmons. Spin blockade and exchange in coulomb-confined silicon double quantum dots. *Nature Nanotechnology*, 2014.

[50] Ruoyu Li, Fay E. Hudson, Andrew S. Dzurak, and Alexander R. Hamilton. Pauli spin blockade of heavy holes in a silicon double quantum dot. *Nano Letters*, pages 7314–7318, 2015.

[51] D. Kotekar-Patil, A. Corna, R. Maurand, A. Crippa, A. Orlov, S. Barraud, L. Hutin, M. Vinet, X. Jehl, S. De Franceschi, , and M. Sanquer. Pauli spin blockade in cmos double quantum dot devices. *Phys. Status Solidi B*, 254(3): 1600581, 2017.

[52] Xuedong Hu, Rogerio de Sousa, and S. Das Sarma. Decoherence and dephasing in spin-based solid state quantum computers. *Condensed Matter Mesoscale and Nanoscale Physics*, 2001.

[53] Brandur Thorgrimsson, A Dohun Kim, Yuan-Chi Yang, L. W. Smith, C. B. Simmons, and Daniel R. Ward et al. Extending the coherence of a quantum dot hybrid qubit. *NPJ, Quantum Information*, 2017.

[54] Jun Yoneda, Kenta Takeda, and Tomohiro Otsuka et al. A quantum-dot spin qubit with coherence limited by charge noise and fidelity higher than 99.9%. *Nature Nanotechnology*, pages 102–106, 2018.

[55] K. Ono, M. Takahiro, and M. Satoshi. High-temperature operation of a silicon qubit. *Sci. Rep.*, 9:1, 2019.

[56] C. Rai, A. Khursheed, and FZ. Haque. Review on single electron transistor (set). *Austin J Nanomed Nanotechnol*, 7:1, 2019.

[57] A. Singh SB. Singh, VP. Agrawal. Analytical Discussion of Single Electron Transistor (SET). *International Journal of Soft Computing and Engineering (IJSCE)*, 2, 2012.

[58] Zuo Li, Moïse Sotto, Fayong Liu, Muhammad Khaled Husain, Hiroyuki Yoshimoto, Yoshitaka Sasago, Digh Hisamoto, Isao Tomita, Yoshishige Tsuchiya, and Shinichi

Saito. Random telegraph noise from resonant tunnelling at low temperatures. *Scientific Reports, Nature*, 8(250), 2018.

[59] Zuo Li, Moïse Sotto, Fayong Liu, Muhammad Khaled Husain, Hiroyuki Yoshimoto, Yoshitaka Sasago, Digh Hisamoto, Isao Tomita, Yoshishige Tsuchiya, and Shinichi Saito. Single carrier trapping and de-trapping in scaled silicon complementary metal-oxide semiconductor field-effect transistors at low temperatures. *Semicond. Sci Technol.*, 32(075001), 2017.

[60] *High Field Measurement System User Manual, Cryogenic Limited, 2006.*

[61] *Practical Cryogenics: An Introduction to Laboratory Cryogenics, by N H Balshaw. 1996.*

[62] M. Xiao, I. Martin, and H.W. Jiang. Probing the spin state of a single electron trap by random telegraph signal. *Phys.Rev. Lett.*, 91(7), 2003.

[63] E. H. Poindexter. *Semiconductor Interfaces, Microstructure, and Devices.* Institute of Physics, 1993.

[64] M. Xiao, I. Martin, and H.W. Jiang. Electrical detection of the spin resonance of a single electron in a silicon field-effect transistor. *Nat. Lett.*, 430(435), 2004.

[65] K. Ono, G. Giavaras, T. Tanamoto, T. Ohguro, X. Hu, and F. Nori. Hole spin resonance and spin-orbit coupling in a silicon metal-oxide-semiconductor field-effect transistor. *PRL*, 119(156802), 2017.

[66] Hiroshi Iwai. Silicon mosfet scaling beyond 0.1 micron. *Int. Conf. on Microelectronics*, 21(pp11-18), 1997.

[67] Robert H. Dennard, Fritz H. Gaensslen, Hwa N. Yu, V. Leo Rideout, Ernest Bassous, and Andre R. Leblanc. Design of ion-implanted mosfet's with very small physical dimensions. *IEEE J. of Solid-State Circuits*, 87(668-678), 1999.

[68] Robert H. Dennard Bijan Davari and Ghavam G. Shahidi. "cmos scaling for high performance and low power-the next ten years. *Proc. of The IEEE*, 83, 1995.

[69] Charles Kittel. *Introduction to Solid State Physics,7th Edition.* Wiley, 2007.

[70] Y. Taur and T. H. Ning. *Fundamentals of Modern VLSI Devices.* Cambridge University Press, Cambridge:UK, 1998.

[71] L. Jacak P. Hawrylak and A. Wojs. *Quantum dots.* Springer, 1998.

[72] T. Ando, Y. Arakawa, K. Furuya, S. Komiyama, and H. Nakashima. *Mesoscopic Physics and Electronics.* Springer, 1998.

[73] Paul Tipler. *Modern physics.* W. H. Freeman, 2008.

[74] K. Ono, D. G. Austing, Y. Tokura, and S. Tarucha. Current rectification by pauli exclusion in a weakly coupled double quantum dot system. *Science*, 297:1313, 2002.

[75] H. W. Liu, T. Fujisawa, Y. Ono, H. Inokawa, A. Fujiwara, K. Takashina, and Y. Hirayama. Pauli-spin-blockade transport through a silicon double quantum dot. *Phys. Rev. B.*, 77:073310, 2008.

[76] N. S. Lai, W. H. Lim, C. H. Yang, F. A. Zwanenburg, W. A. Coish, F. Qassemi, A. Morello, and A. S. Dzurak. Pauli spin blockade in a highly tunable silicon double quantum dot. *Sci. Rep.*, 1:110, 2011.

[77] B. Weber, S. Tan, Y. H. M. Mahapatra, T. F. Watson, H. Ryu, R. Rahman, L. C. L. Hollenberg, G. Klimeck, and M. Y. Simmons. Spin blockade and exchange in coulomb-confined silicon double quantum dots. *Nat. Nano.*, 9:430, 2014.

[78] Z. Li, M. K. Husain, H. Yoshimoto, K. Tani, J. D. Fletcher Y. Sasago, D. Hisamoto, M. Kataoka, Y. Tsuchiya, and S. Saito. Single carrier trapping and de-trapping in scaled silicon complementary metal-oxide-semiconductor field-effect transistors at low temperatures. *Semicond. Sci. Technol.*, 32:075001, 2017.

[79] Z. Li, M. Sotto, F. Liu, M. K. Husain, H. Yoshimoto, D. Hisamoto Y. Sasago, I. Tomita, Y. Tsuchiya, and S. Saito. Random-telegraph-noise by resonant tunnelling at low temperatures. *Nat. Sci. Rep.*, 8:250, 2018.

[80] E. Kawakami, P. Scarlino, D. R. Ward, F. R. Braakman, D. E. Savage, M. G. Lagally, M. Friesen, S. N. Coppersmith, M. A. Eriksson, and L. M. K. Vandersypen. Electrical control of a long-lived spin qubit in a si/sige quantum dot. *Nat. Nanotechnol.*, 9:666, 2014.

[81] J. J. Pla, K. Y. Tan, J. P. Dehollain, W. H. Lim, J. J. L. Morton, D. N. Jamieson, A. S. Dzurak, and A. Morello. A single-atom electron spin qubit in silicon. *Nature*, 489:541, 2012.

[82] P. W. Shor. Scheme for reducing decoherence in quantum computer memory. *Phys. Rev. A.*, 52:2493, 1995.

[83] F. A. Zwanenburg, A. S. Dzurak, A. Morello, M. Y. Simmons, L. C. L. Hollenberg, G. Klimeck, S. Rogge, S. N. Coppersmith, and M. A. Eriksson. ilicon quantum electronics. *Rev. Mod. Phys.*, 85:961, 2013.

[84] J. J. Pla, K, Y. Tan, J. P. Dehollain, W. H. Lim, J. J. L. Morton, D. N. Jamieson F. A. Zwanenburg, A. S. Dzurak, and A. Morello. High-fidelity readout and control of a nuclear spin qubit in silicon. *Nature*, 496:334, 2013.

[85] B. M. Terhal. Quantum error correction for quantum memories. *Rev. Mod. Phys.*, 87:307, 2015.

[86] H. Grabert and M. H. Devoret. *Single Charge Tunneling.* Plenum Press, 1992.

[87] K. Ono, T. Tanamoto, and T. Ohguro. Pseudosymmetric bias and correct estimation of coulomb/confinement energy for unintentional quantum dot in channel of metal-oxide-semiconductor field-effect transistor. *App. Phys. Lett.*, 103:183107, 2013.

[88] K. Ibukuro, J. W. Hillier, F. Liu, M. K. Husain, Z. Li, I. Tomita, Y. Tsuchiya, H. N. Rutt, and S. Saito. Random telegraph signals caused by a single dopant in a metal–oxide–semiconductor field effect transistor at low temperature. *AIP Adv.*, 10:055025, 2020.

[89] A. Zarassi, Z. Su, J. Danon, J. Schwenderling, M. Hocevar, B. M. Nguyen, J. Yoo, S. A. Dayeh, , and S. M. Frolov. Magnetic field evolution of spin blockade in ge/si nanowire double quantum dots. *Phys. Rev. B.*, 95:155416, 2017.

[90] G. Xu, F. Gao, K. Wang, T. Zhang, H. Liu, G. Cao, T. Wang, J. Zhang, H. Jiang, H. Li, and G. Guo. Hole spin in tunable ge hut wire double quantum dot. *App. Phys. Exp.*, 13(065002), 2020.

[91] S. Nadj-Perge, S. M. Frolov, J. W. W. van Tilburg, J. Danon, Yu. V. Nazarov, R. Algra, E. P. A. M. Bakkers, and L. P. Kouwenhoven. Disentangling the effects of spin-orbit and hyperfine interactions on spin blockade. *Phys. Rev. B*, 81:201305, 2010.

[92] C. Fasth, A. Fuhrer, L. Samuelson, V. N. Golovach, and D. Loss. *Phys. Rev. Lett.*, 98:266801, 2007.

[93] S. Nadj-Perge, V. S. Pribiag, J. W. G. van den Berg, K. Zuo, S. R. Plissard, E. P. A. M. Bakkers, S. M. Frolov, and L. P. Kouwenhoven. *Phys. Rev. Lett.*, 108: 166801, 2012.

[94] S. Mehl and D. P. DiVincenzo. Inverted singlet-triplet qubit coded on a two-electron double quantum dot. *Phys. Rev. B*, 90:195424, 2014.

[95] J. Danon and Yu. V. Nazarov. Pauli spin blockade in the presence of strong spin-orbit coupling. *Phys. Rev. B.*, 80:041301, 2009.

[96] D. M. Zumbuhl. *Coherence and Spin in GaAs Quantum Dots.* PhD thesis, Harvard, Cambridge, 2004.

[97] S. Amasha, K. MacLean, Iuliana P. Radu, D. M. Zumbuhl, M. A. Kastner, M. P. Hanson, and A. C. Gossard. *Phys. Rev. Lett.*, 100:046803, 2008.

[98] G. Yamahata, T. Kodera, H. O. H. Churchill, K. Uchida, C. M. Marcus, and S. Oda. *Phys. Rev. B.*, 86:115322, 2012.

[99] J. Yamauchi, N. Hajjar and R. Reif. *IEEE Trans. Electron Dev.*, 38:55–60, 1991.

[100] Y. Yamaoka, K. Iwasaki, S. Oda, and T. Kodera. *Jpn. J. Appl.*, 56:04CK07, 2017.

[101] K. Ono, G. Giavaras, T. Tanamoto, T. Ohguro, X. Hu, and F. Nori. *Phys. Rev. Lett.*, 119:156802, 2017.

[102] G. Yamahata, K. Nishiguchi, and A. Fujiwara. Gigahertz single-trap electron pumps in silicon. *Nat. Commun*, 5:5038, 2013.

[103] G. Yamahata, S. P. Giblin, M. Kataoka, T. Karasawa, and A. Fujiwara. High accuracy current generation in the nanoampere regime from a silicon single-trap electron pump. *Sci. Rep.*, 7:45137, 2017.

[104] W.G. Unruh. Maintaining coherence in quantum computers. *Phys. Rev. A*, 51(2): 992, 1995.

[105] K. K. Hung, P. Ko, C. Hu, and Y. C. Cheng. Random telegraph noise of deep-submicrometer mosfets. *IEEE Elec. Dev. Lett.*, 11:90–92, 1990.

[106] K. Ono, G. Giavaras, T. Tanamoto, T. Ohguro, X. Hu, and F. Nori. Hole spin resonance and spin-orbit coupling in a silicon metal-oxide-semiconductor field-effect transistor. *Phys. Rev. Lett.*, 119:156802, 2017.

[107] T. Tanamoto, Y. Nishi, and K. Ono. Application of single-electron effects to fingerprints of chips using image recognition algorithms. *Appl. Phys. Lett.*, 115 (033504):033504, 2019.

[108] D. J. DiMaria and H. J. Stathis. Anode hole injection, defect generation, and breakdown in ultrathin silicon dioxide films. *J. App. Phys.*, 89:5015, 2001.

[109] A. Alekseev. Basics of Low-temperature Refrigeration. *CAS-CERN Accelerator School: Superconductivity for Accelerators*, pages 111–139, 2013.

[110] A. Ortiz-Condea, F.J. G. Sáncheza, J.J. Lioub, A. Cerdeirac, M. Estradac, and Y. Yued. A review of recent MOSFET threshold voltage extraction methods. *Microelectronics Reliability*, 42:583, 2002.

[111] S. Saito, K. Torii, Y. Shimamoto, S. Tsujikawa, H. Hamamura, O. Tonomura, T. Mine, D. Hisamoto, T. Onai, J. Yugami, M. Hiratani, and S. Kimura. Effects of remote-surface-roughness scattering on carrier mobility in field-effect-transistors with ultrathin gate dielectrics. *Appl. Phys. Lett.*, 84:1395, 2004.

[112] J. Li and T. P. Ma. Scattering of silicon inversion layer electrons by metal/oxide interface roughness. *J. App. Phys.*, 62:4212, 1987.

[113] K. Ibukuro, M. K. Husain, Z. Li, J. Hillier, F. Liu, I. Tomita, Y. Tsuchiya, H. Rutt, and S. Saito. Single electron memory effect using random telegraph signals at room temperature. *Front. Phys.*, 7:152, 2019.

[114] D. J. DiMaria, E. Cartier, and D. A. Buchanan. Anode hole injection and trapping in silicon dioxide. *Appl. Phys. Lett.*, 68:304, 1996.

[115] F. Liu, K. Ibukuro, M. K. Husain, Z. Li, J. Hillier, I. Tomita, Y. Tsuchiya, H. Rutt, and S. Saito. Manipulation of random telegraph signals in a silicon nanowire transistor with a triple gate. *Nanotechnology*, 29:475201, 2018.

[116] W. Lu, Z. Ji, L. Pfeiffer, K. West, and A. Rimberg. Real-time detection of electron tunnelling in a quantum dot. *Nature*, 423:422–425, 2003.

[117] Arne Laucht, Frank Hohls, Niels Ubbelohde, M Fernando Gonzalez-Zalba, David J Reilly, Søren Stobbe, Tim Schröder, Pasquale Scarlino, Jonne V Koski, Andrew Dzurak, Chih-Hwan Yang, Jun Yoneda, Ferdinand Kuemmeth, Hendrik Bluhm, Jarryd Pla, Charles Hill, Joe Salfi, Akira Oiwa, Juha T Muhonen, Ewold Verhagen, M D LaHaye, Hyun Ho Kim, Adam W Tsen, Dimitrie Culcer, Attila Geresdi, Jan A Mol, Varun Mohan, Prashant K Jain, and Jonathan Baugh. Roadmap on quantum nanotechnologies. *Nanotechnology*, 32(16):162003, feb 2021.

[118] I. C. Chen, S. Holland, K. K. Young, C. Chang, and C. Hu. Substrate hole current and oxide breakdown. *Appl. Phys. Lett.*, 49:669–671, 1986.

[119] H. M. Branz and M. Silver. Potential auctuations due to inhomogeneity in hydrogenated amorphous silicon and the resulting charged dangling-bond defects. *Phys. Rev. B.*, 42(12), 1990.

[120] H. Ishikuro and T. Hiramoto. Quantum mechanical effects in the silicon quantum dot in a single-electron transistor. *Phys. Rev. Lett.*, 71:3691–3693, 1997.

[121] M. A. Fogarty, K. W. Chan, B. Hansen, W. Huang, T. Tanttu, C. H. Yang, A. Laucht, M. Veldhorst, F. E. Hudson, K. M. Itoh, D. Culcer, T. D. Ladd, and A. S. Dzurak. Integrated silicon qubit platform with single-spin addressability, exchange control and single-shot singlet-triplet readout. *Nat. Comm.*, 9(4370), 2018.

[122] Andrea Morello. Silicon quantum dots: fine-tuning to maturity. *Nanotechnology*, 26(50):502501, 2015.

[123] S. P. Giblin, S. J. Wright, J. D. Fletcher, M Kataoka, M Pepper, T J B M Janssen, D. A. Ritchie, C. A. Nicoll, D. Anderson, and G. A. C. Jones. An accurate high-speed single-electron quantum dot pump. *New Journal of Physics*, 12(7):073013, 2010.

[124] Y. Takahashi, Y. Ono, A. Fujiwara, and H. Inokawa. Silicon single-electron devices. *J. Phys. Condens. Matter*, 14, 2002.

[125] D. L. Crook. In *Proc. 17th Int. Rel. Phys. Symp*, page 1, 1979.

[126] J. Hillier, K. Ono, K. Ibukuro, F. Liu, Z. Li, M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi, and S. Saito. Atomically flat trapezoidal silicon nanowires for tunable gate defined quantum dots. In *Silicon Quantum Information Processing Workshop*, page 16, 2021.

[127] J. Hillier, K. Ono, K. Ibukuro, F. Liu, Z. Li, M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi, and S. Saito. Single spin sensing in silicon p-type metal-oxide-semiconductor field-effect transistors. In *International conference for the quantum science and technology community*, page 3193, 2020.

[128] K. F. Schuegraf and C. Hu. In *IEEE Trans. Elec. Dev*, 1994.

[129] R. Degraeve, G. Groseneken, R. Bellens, J. L. Ogier, M. Depas, P. J. Roussel, and H. E. Maes. New insights in the relation between electron trap generation and the statistical properties of oxide breakdown. *IEEE. Trans. Elec. Dev*, 45(4), 1998.

[130] F. Martinez, C. Leyris, G. Neau, M. Valenza, A. Hoffmann, J.C. Vildeuil E. Vincent, F. Boeuf, T.Skotnicki, M.Bidaud, D.Barge, and B.Tavelc. Oxide traps characterization of 45 nm MOS transistors by gate current R.T.S noise measurements. *Micro. Elec. Eng.*, 80:54–57, 2005.

[131] Eddy Simoen and Cor Claeys. *Random Telegraph Signals in Semiconductor Devices*. IOP Publishing, Bristol, 2016.

[132] K. K. Likharev. Single-electron devices and their applications. In *Proc. IEEE*, volume 87, page 606, 1999.

[133] M. A. Kastner. The single-electron transistor. *Rev. Mod. Phys.*, 64:849, 1992.

[134] A. Fujiwara, K. Nishiguchi, and Y. Ono. Nanoampere charge pump by single-electron ratchet using silicon nanowire metal-oxide-semiconductor field-effect transistor. *Appl. Phys. Lett*, 92(042102), 2008.

[135] K. Ono, T. Mori, and S. Moriyama. High-temperature operation of a silicon qubit. *Sci. Rep.*, 9(469), 2019.

[136] J. Hillier, K. Ono, K. Ibukuro, F. Liu, Z. Li, M. K. Husain, H. N. Rutt, I. Tomita, Y. Tsuchiya, K. Ishibashi, and S. Saito. Probing hole spin transport of disorder quantum dots via pauli spin-blockade in standard silicon transistors. *Nanotechnology*, 32:260001, 2021.

[137] J. Hillier, K. Ibukuro, F. Liu, M. K. Husain, J. Byers, H. N. Rutt, I. Tomita, Y. Tsuchiya, and S. Saito. Investigating stability and tunability of quantum dot transport in silicon MOSFETs via the application of electrical stress. *J. Phys. D: Appl. Phys.*, 55:105107, 2022.

[138] Bishnu Patra, Rosario M. Incandela, Jeroen P. G. van Dijk, Harald A. R. Homulle, Lin Song, Mina Shahmohammadi, Robert Bogdan Staszewski, Andrei Vladimirescu, Masoud Babaie, Fabio Sebastiano, and Edoardo Charbon. Cryo-cmos circuits and systems for quantum computing applications. *IEEE Journal of Solid-State Circuits*, 53:309–321, 2018.

[139] S. J. Pauka, K. Das, R. Kalra, A. Moini, Y. Yang, M. Trainer, A. Bousquet, N. Dick C. Cantaloube, G. C. Gardner, M. J. Manfra, and D. J. Reilly. A cryogenic cmos chip for generating control signals for multiple qubits. *Nat Electron*, 4:64–70, 2021.

[140] Xiao. Xue, Bishnu. Patra, P. G. van Dijk, Jeroen, Nodar. Samkharadze, Sushil. Subramanian, Andrea. Corna, Brian. Paquelet Wuetz, Charles. Jeon, Farhana. Sheikh, Esdras. Juarez-Hernandez, Huzaifa. Esparza, Brando Perez.and Rampurawala, Brent. Carlton, Surej. Ravikumar, Carlos. Nieva, Sungwon. Kim, Hyung-Jin. Lee, Amir. Sammak, Giordano. Scappucci, Menno. Veldhorst, Masoud. Sebastiano, Fabio. Babaie, Stefano. Pellerano, Edoardo. Charbon, and Lieven M. K. Vandersypen. Cmos-based cryogenic control of silicon quantum circuits. *Nature*, 593:205–210, 2021.

[141] W. J. Liu, Z. Y. Liu, D. Huang, C. C. Liao, W. Wong L. F. Zhang, and Z. H. Gan, C. Shen, and M.-F. Li. On-the-fly interface trap measurement and its impact on the understanding of nbti mechanism for p-mosfets with sion gate dielectric. *IEDM Tech. Dig.*, page 813–816, 2007.

[142] Y. Nissan-Cohen, J. Shappir, and D. Frohman-Bentchkowsky. Trap generation and occupation dynamics in sio2 under charge injection stress. *J. Appl. Phys.*, 60, 1986.

[143] and H. Iwasaki T. Hori and K. Tsuji. Charge-trapping properties of ultrathin nitrided oxides prepared by rapid thermal annealing. *IEEE Trans. Elect. Dev.*, 35, 1988.

[144] E. Lusky, Y. Shacham-Diamand, I. Bloom, and B. Eitan. Electrons retention model for localized charge in oxide-nitride-oxide (ono) dielectric,. *IEEE Elect. Dev. Lett.*, 23, 2002.

[145] Satake H. *et al. App. Phys. Lett.*, 69:1128–1130, 1996.

[146] Paul E. Nicollian, Anand T. Krishnan, Cathy A. Chancellor, Rajesh B. Khamankar, Srinivasan Chakravarthi, Chris Bowen, and Vijay K. Reddy. In *IEEE Rel. Phys.*, pages 197–208, 2007. doi: 10.1109/RELPHY.2007.369892.

[147] Kouta Ibukuro, Joseph William Hillier, Fayong Liu, Muhammad Khaled Husain, Zuo Li, Isao Tomita, Yoshishige Tsuchiya, Harvey Nicholas Rutt, and Shinichi Saito. Random telegraph signals caused by a single dopant in a

metal–oxide–semiconductor field effect transistor at low temperature. *AIP Advances*, 10(5):055025, 2020. doi: 10.1063/5.0009585.

[148] Devoret MH. Grabert H. *Single Charge Tunneling: Coulomb Blockade Phenomena in Nanostructures*. NY: Springer US, New York, 1992.

[149] P. C. Spruijtenburg, S. V. Amitonov, F. Mueller, W. G. van der Wiel, and Floris A. Zwanenburg. *Sci. Rep.*, 6:38127, 2016.

[150] M. Leroux, N. Grandjean, B. Beaumont, G. Nataf, F. Semond, J. Massies, and J. P. Gibart. Temperature quenching of photoluminescence intensities in undoped and doped gan. *J. App. Phys.*, 86, 1999.

[151] Jehl X, Niquet YM, and Sanquer M. Single donor electronics and quantum functionalities with advanced CMOS technology. *J. Phys. Condens. Matter.*, 28, 2016.