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Name: Thomas Abbey

Title of Thesis: Exploring and Utilising the Effects of Environmental Factors on Memristor Behaviour

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”Thermal Effects on Initial Volatile Response and Relaxation Dynamics of Resistive RAM Devices”, T. Abbey, C. Giotis, A. Serb, S. Stathopoulos and T. Prodromakis, in IEEE Electron Device Letters, vol. 43, no. 3, pp. 386-389, March 2022, doi: 10.1109/LED.2022.3145620.

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”Compact Modeling of the Switching Dynamics and Temperature Dependencies in TiOx-Based Memristors—Part I: Behavioral Model”, D. Vaidya, S. Kothari, T. Abbey, A. Khiat, S. Stathopoulos, L. Michalas, A. Serb, T. Prodromakis, in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 4877-4884, Oct. 2021, doi: 10.1109/TED.2021.3101996.

”Compact Modeling of the Switching Dynamics and Temperature Dependencies in TiOx Memristors—Part II: Physics-Based Model”, D. Vaidya, S. Kothari, T. Abbey, A. Khiat, S. Stathopoulos, L. Michalas, A. Serb, T. Prodromakis, in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 4885-4890, Oct. 2021, doi: 10.1109/TED.2021.3102002.

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UNIVERSITY OF SOUTHAMPTON

Exploring and Utilising the Effects of Environmental Factors on Memristor Behaviour

by

Thomas R. Abbey

A thesis submitted in partial fulfillment for the degree of Doctor of Philosophy

in the

Faculty of Physical Sciences and Engineering

School of Electronics and Computer Science

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ABSTRACT

FACULTY OF PHYSICAL SCIENCES AND ENGINEERING
SCHOOL OF ELECTRONICS AND COMPUTER SCIENCE

Doctor of Philosophy

by Thomas R. Abbey

Electronic devices are sensitive to environmental conditions, the most well studied of these parameters being temperature, leading to the need for full characterisation to determine any environmental dependencies. Memristors are a new class of two-terminal metal-insulator-metal device that show great promise in applications such as high density data storage and physical neural networks. Being a new class of device, with many different combinations of materials means that a method and system for rapidly characterising the environmental dependencies of these devices needs to be developed.

Humidity has been demonstrated to affect the behaviour of some memristors (most notably hafnium based), however, the effects of this on titanium based devices have not been investigated.

To this end, a low-cost, miniaturised environmental control chamber has been developed, capable of reaching temperatures up to 90°C while simultaneously controlling atmospheric humidity. This system has then been used to investigate the impact of temperature and humidity of memristors constructed with a gold/titanium oxide/platinum stack at four resistivities, from "pristine" to very low resistivity. The data retrieved from these investigations indicates that TiO_2 based devices would make for effective resistive temperature sensors. Characteristics of these devices such as the IV, switching, and volatile recovery behaviour have been demonstrated to be affected by changes in temperature, and temperature dependant models of these behaviours have been developed and integrated with existing models (IV, volatility and switching behaviour), allowing for a more comprehensive understanding of how memristors may be affected by real world conditions when integrated into systems that experience thermal cycling.

Leveraging the thermal dependencies of the studied devices, the emulation of a homeostatic neuron was undertaken, with a number of memristors acting as the synapses, first in simulation as a proof of concept. For this project, the temperature of the devices was altered as a method of providing global synapse weight control.

An initial investigation into the impact of humidity on these devices was conducted, showing evidence that exposure to atmospheric humidity can result in the restoration of switching behaviour on previously broken devices.

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Nomenclature

VCM	Valence Change Memory
ECM	Electro-Chemical Metallisation
PCM	Phase Change Memory
HRS	High Resistance State
LRS	Low Resistance State
IV	Current/Voltage
ANN	Artificial Neural Network
LIF	Leaky-Integrate-Fire
RRAM/ReRAM	Resistive Random Access Memory
DRAM	Dynamic Random Access Memory
SRAM	Static Random Access Memory
PCB	Printed Circuit Board
PID	Proportional Integral Derivative
PLA	Polylactic Acid
PMMA	Polymethyl Methacrylate (Acrylic)
CNC	Computer Numerical Control
DUT	Device Under Test
LED	Light Emitting Diode
R	Resistance
R0	Initial Resistance
T	Temperature
Φ	Shottky Barrier
A	Richardson Constant X Area
k	Boltzmann Constant

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Chapter 1

Introduction

1.1 Background and Motivation

Due to the nature of metal oxides featuring low numbers of free carriers, electronic devices featuring these materials are sensitive to external conditions, the most well documented being the effects of temperature [1, 2], however humidity may also impact operation and performance. [3, 4]

Because of these factors, it is important that electronic devices are characterised under varying environmental conditions in order to understand the impacts that these factors may have on operation to ensure reliability in electronic systems.

Memristors are a relatively new class of electronic device. These are two terminal devices which act as non-volatile variable resistors whose resistivity is dependent upon the voltages previously applied across the device. Applications for these new devices are still being developed, but they show great promise as non-volatile memory due to their small footprint and the highly compact architectures for memory systems they theoretically allow for. Further applications of interest are in neuromorphic computing systems [5, 6, 7] due to the memristors behaviour being analogous to that of a biological synapse, and adjustable threshold logic gates. [8, 9, 10]

With memristors being as new as they are, various architectures of these devices are being developed [11] and require accurate characterisation in order to ensure the reliability of these devices during operation. The various configurations of memristors are often referred to as "stacks", with this referencing the material the top and bottom electrodes and the active material in between, for example, the devices focused on in this work are $Au/TiO_2/Pt$ stacks, meaning they have a gold bottom electrode, titanium dioxide middle layer and platinum top electrode. Other configurations of devices are under study, with alternative electrode and middle layer materials, some featuring a multiple layer

construction [12], with possible electrode materials including silver, copper and niobium and middle materials including hafnium, aluminium and zinc oxides. [13, 14]

In addition, the effects of environmental parameters on the operation of memristors provide the opportunity to develop a method for using the devices as sensors, and implement a global control variable over memristor networks, allowing for various alterations to the behaviour, without impeding on operation.

1.2 Project Aim

The aim of this project was to understand and model the behaviour of RRAM devices under different environmental conditions and if possible, demonstrate how these might be leveraged in an example application. To this end, the impact of temperature on parameters such as static resistance, IV characteristics, switching behaviour and volatile recovery were investigated and subsequent behavioural models were developed. Memristors were demonstrated to be easily applicable as passive temperature sensors, with the behaviours observed in this being subsequently utilised to model a synapse with homeostatic properties. The application of high humidity environments to these devices demonstrated the ability for limited recovery/self repair of these devices.

1.3 Project Objectives

The main objectives of this project include the following targets:

1. Develop a thorough methodology for establishing and isolating the impact of environmental parameters on memristors and studying these effects.
2. Identify and investigate the operation and failure mechanisms for these devices with correlation to the temperature and humidity variables.
3. Use the gathered data to inform empirical models for devices operating in environments where temperature and humidity are factors.
4. Exploit any dependence in these variables in practical applications.

1.4 Thesis Structure

The structure of this thesis is as follows; The first section is a literature review covering and differentiating between the various operating mechanisms of memristors currently prominent in research, including the existing models developed within my research group

as well as an overview on the various methods of electrically measuring temperature and humidity and a brief insight into artificial neural networks. The second section contains an overview of the development of the miniaturised environmental control chamber, including a summary of the work conducted before starting the project. Section 3 contains the experiments and observed effects of temperature changes on the memristors studied in my research. The experiments and observed effects of exposure to high humidity environments on TiOx based memristors is presented in section 4. Section 5 presents the various temperature dependency models I have developed utilising the data from my research. Section 6 covers the process of developing a system exploiting the temperature dependencies of memristors in order to emulate the homeostatic effects observed in neurons.

Chapter 2

Solid State Memristor Models, Applications and Tools

2.1 Memristor Theory

A memristor is a device whose resistance is dependent upon the history of potentials that have previously been applied across it, and for how long those potentials were applied. Typically for memristors, a higher voltage applied across the device will result in a change in resistive state, and a lower voltage will not, allowing for the device resistance to be measured non-invasively, that is, without changing the resistive state. A physical memristor is usually a stack of three layers, metal/metal oxide/metal, though more complex architectures do exist. This structure forms two back to back connected Schottky diodes, figure 2.1. [15, 13]

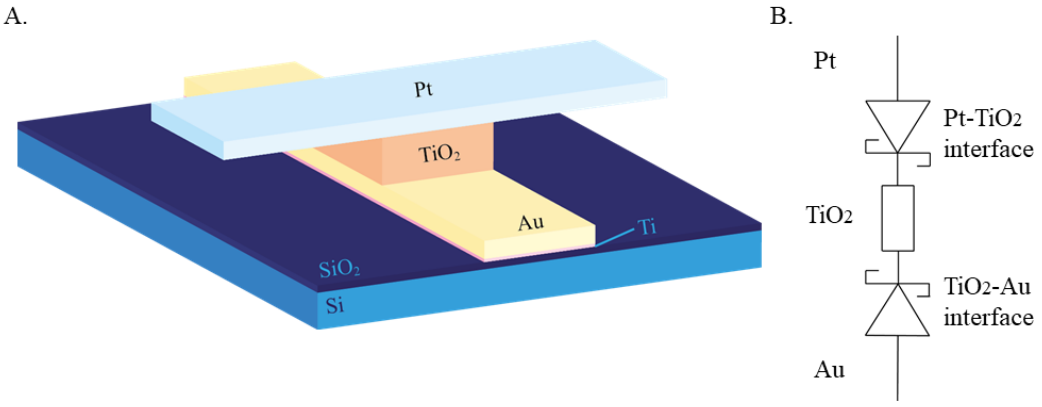

FIGURE 2.1: A. An example memristor diagram of the devices used in this research. B. equivalent circuit diagram.

Conceptualised in 1971 by Leon Chua [16] as a missing component linking electric charge with magnetic flux, the physical memristor was not realised until 2007 [17], when R. Stanley Williams managed to connect the response of platinum/titanium oxide/platinum devices to Chua's theory. The theory of this device was developed due to the existence of 3 other "core" components linking the other electronic characteristics, with the resistor being the link between voltage and current, the capacitor linking charge and voltage, and the inductor linking magnetic flux and current, leaving the link between magnetic flux and charge un-covered. Some of the more common oxides used for constructing memristors are those of titanium, aluminium and hafnium, as well as some non-metal oxides such as silicon. [18]

2.2 Memristor Technologies

2.2.1 Forming and Operational Characteristics

When a metal/oxide/metal memristor is first fabricated it is said to be pristine and does not function as a true memristor, but more like a pair of back to back connected Schottky diodes due to the pair of metal/metal oxide contacts, meaning the device demonstrates no memristive properties. [15, 19] Usually, the memory behaviour of these devices is only introduced after a process known as forming, though "forming free" devices have been developed, which feature switching behaviours without the prior requirement of a forming process.[20] The forming process involves applying a high potential across the terminals of the device, which results in the reduction in resistivity of the device. This can occur in several ways, including the formation of conductive filaments, figure 2.2, [21, 22] and a reduction in Schottky barrier height.[23] In filamentary devices, depending upon the polarity of this voltage and the memristor itself, the filaments change in radius and number, altering the conductivity and resulting in a high or low resistive state.[24] [25] For interfacial devices, the resistivity change is caused by the applied voltage altering the Schottky barrier height, which is induced by the movement of charges towards the barrier. This is not considered a "true" switching mechanism in these devices, as it is volatile, meaning that once the applied voltage is removed the device will return back to it's original resistive state. This method of changing device resistance is still an area of interest for shorter term memory storage. Memristor switching behaviour can be split into four key terms, high resistive state (HRS), low resistive state (LRS), volatile and non- volatile. The high resitive state of a device refers to the resistance of a device after the conductive filaments are "dissolved" in the bulk material, leading to a higher resistance reading. The LRS refers to the state of a device after filaments have been formed again by a switching voltage. These two states are both defined as being stable, meaning that a device will stay in the HRS/LRS for a prolonged period of time, and can be cycled between the two states with minimal change in the resistance

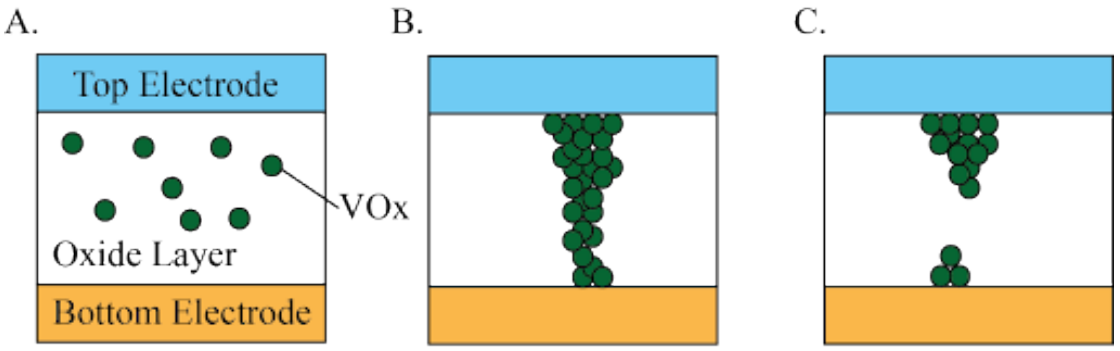

FIGURE 2.2: The operation of a filamentary valence-change memory A. The state of a pristine device before forming, showing un-ordered oxygen vacancies (VOx). B. A formed device in the low resistive state, showing a bridging conductive filament. C. A formed device in the high resistive state, showing a broken conductive filament.

of the HRS/LRS. Once a non-volatile state is set it remains with a potentially very long lifetime making memristors promising devices for memory applications due to their non-volatility and ability to be constructed in highly compact architectures due to their two terminal construction and ability to be scaled down to the nanoscale. Some devices exhibit a combination of volatile and non-volatile switching behaviours, meaning that they will exhibit some drift back towards their initial resistance after switching, but still exhibit a long term change in resistance.

Volatile devices do not exhibit long term memory, with the device eventually returning back to its original resistance. While this prevents this type of device being used to memory storage, the memory lifetime of the device may still be long enough to be useful in applications where the data is read/re-written frequently. It is possible to set a resistivity between the high and low states, [26] providing useful applications in neuromorphic systems, however, these states may be volatile, with varying recovery times before the device settles back to either of the stable states. [27] While volatile memory characteristics are not the most desired function of a memristor for traditional memory applications, they can still prove useful in systems such as artificial neurons, where this feature may provide in-built depression of the neuron and RAM, where long memory lifetimes are not necessary.

Formed devices may be either bipolar or unipolar, with bipolar devices receiving the majority of attention. When an electrical bias is applied to a bipolar device, the direction of change in resistivity will follow the polarity of the applied bias. With a unipolar device, a single polarity can be used to set and reset the device's resistive state.

The configurable resistivity of these devices leads to the applications in neuromorphic systems [28, 29, 30], as neurons possess similar memristive properties as the more they are stimulated, the stronger the weight of their response becomes (Hebb's rule). This is replicated in a memristor's change in resistance, with a lower resistance providing a stronger response. This similarity allows for memristors to be used as a bridging

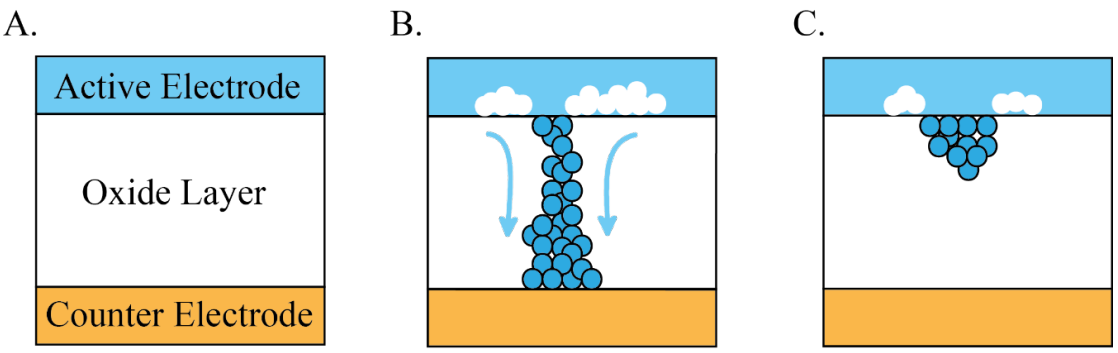

FIGURE 2.3: The forming and operation of an ECM device, arrows showing the direction of ion movement A. The device in the pristine state B. the device in the LRS C. the device in the HRS.

synapse between two areas of a system, and the more that bridge is used, the stronger its influence becomes, though it could be controlled independent of data flow by utilising low voltage data pulses, and higher voltage stimulation pulses.

2.2.2 Switching Mechanisms

Several classes of memristive device exist, with varying switching mechanisms, most falling into the categories of filamentary or interfacial mechanisms. The most widely studied of the filamentary mechanisms are electro-chemical metallisation (ECM) memory and valence change memory (VCM).

2.2.2.1 Electro-Chemical Metallisation Memory

ECM devices utilise metal ions generated from an active electrode, usually copper or silver to generate a low resistive state. During formation and switching, ions of the active metal diffuse into the solid electrolyte, resulting in the formation of metallic nano-wires that bridge the two electrodes. When the reset voltage is applied to the cell, the filament dissolves, with the ions drifting back to the active electrode, figure 2.3. [5] The majority of research into the impact of humidity and temperature has been performed on this class of devices rather than VCM devices. These devices tend to have larger on/off resistive ratios and switch more suddenly, as a result, these often need to be used with a current limited system, to prevent "burning" the device when it switches to a low resistance state. This gives rise to their typical IV behaviour seen in figure 2.4, featuring areas of constant current despite voltage changes.

2.2.2.2 Valence Change Memory

The main switching mechanisms in VCM memristors are typically ionic and thermal.

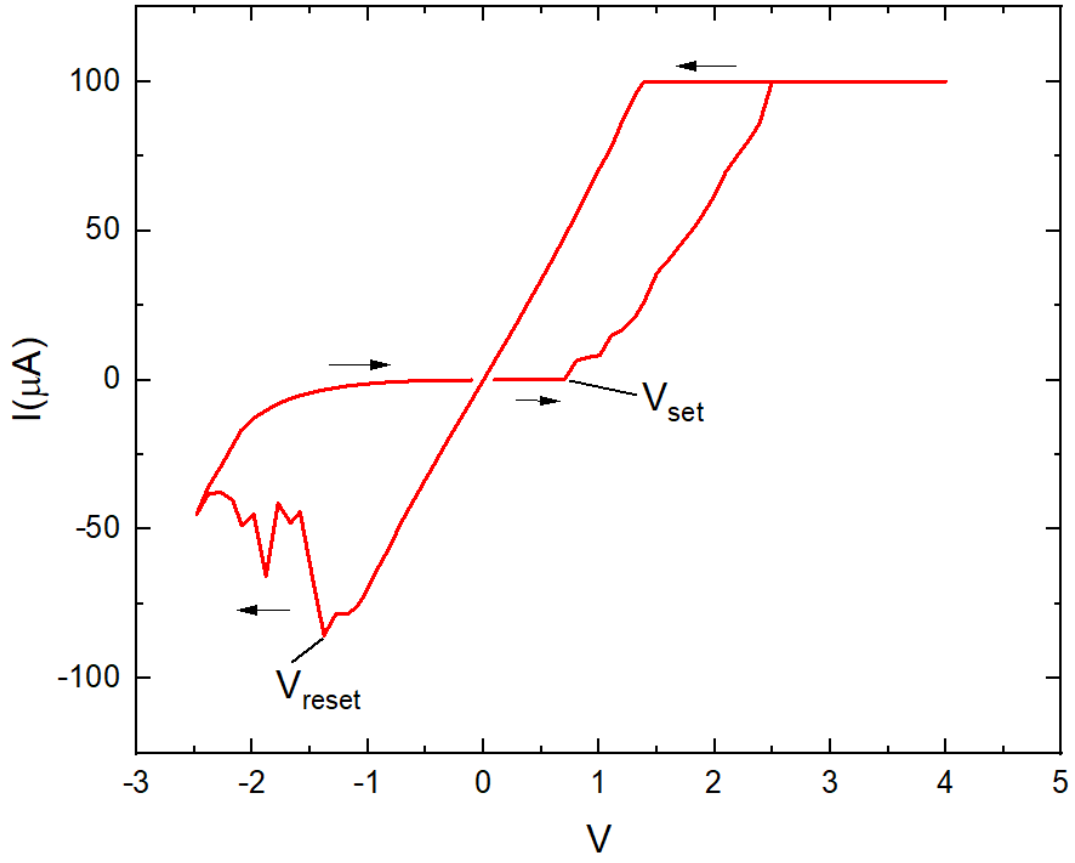

FIGURE 2.4: A typical IV for an ECM device, with the arrows showing the direction of voltage change. V_{set} is the voltage at which the device resistance begins to drop, V_{reset} is the voltage at which the device begins to "reset" to its HRS. The presence of ohmic characteristics in the LRS support the presence of metallic filament formation.

The ionic mechanism involves the migration of oxygen vacancies within the metal oxide layer, under the right conditions this leads to the formation of a filament of an un-saturated metal oxide which becomes metallically conductive when the oxygen concentration is low enough, leading to the reduction in resistivity, illustrated in figure 2.2. [31] It has also been suggested that hydroxide ions can be involved in this switching process, lending support to the idea that humidity may be able to be used as a controlling factor for behaviour. [32]

The thermal switching mechanism is based around Joule heating, where the application of electric fields and current flow can result in heating and changes to the structure of a material. In metal oxide thin films, this can result in the destruction of conductive filaments described above, as resistive heating of the filament occurs. The conductive channels are generally Ohmic, and the resistance and set/reset voltage vary little with different metal oxides (TiO, NiO and ZnO), indicating that there is thermally activated dissolution of conductive filaments. [33] This effect is thought to be a source of observed unipolar behaviour.

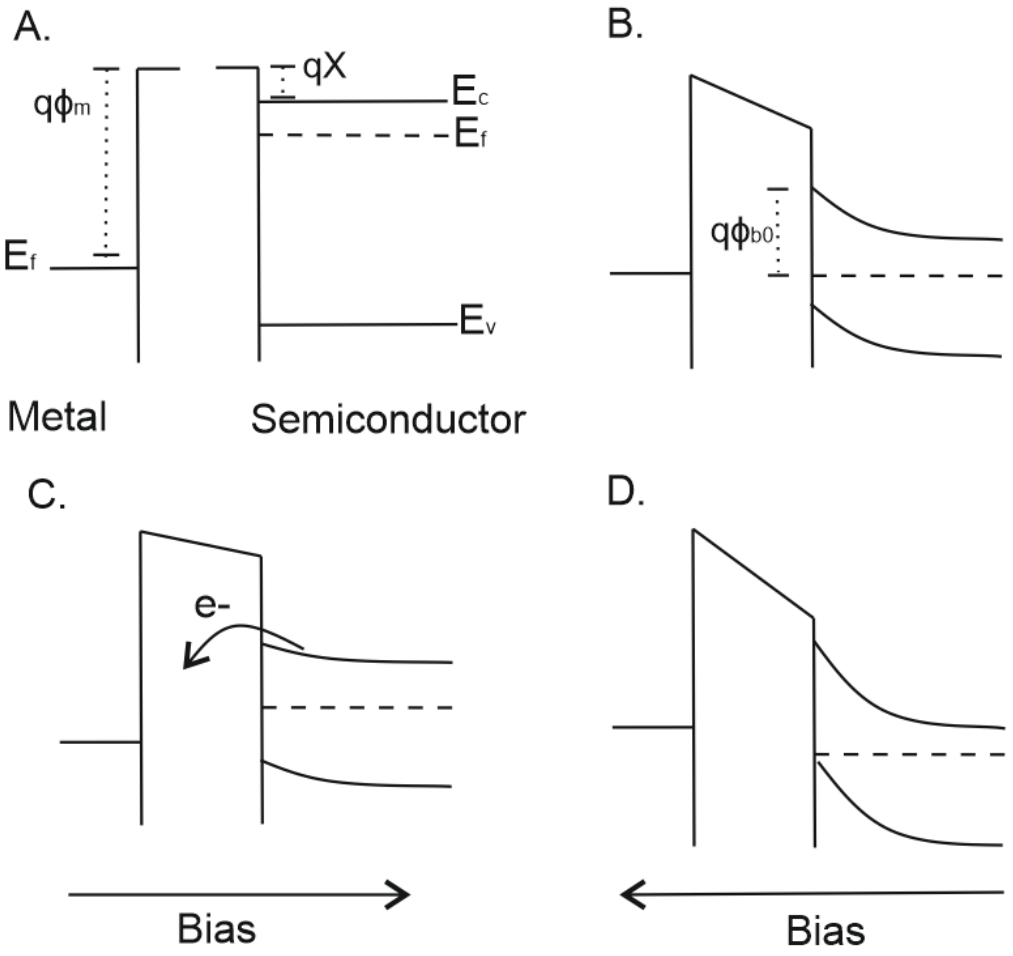

FIGURE 2.5: A. The energy band diagram of a metal and semiconductor when separated. B. The band diagram for a Schottky barrier with no bias applied, with the metal and semiconductor in contact. C. The band diagram for a forward biased Schottky barrier. D. The band diagram for a reverse biased Schottky barrier.

2.2.2.3 Interfacial Switching

When a metal and non-metal are in contact, a schottky barrier can form at the interface between the materials, fig 2.5. In the case of this diagram, q is the electron charge, ϕ_m is the work function of the metal, X is the electron affinity of the connecting material, and ϕ_{b0} is the Schottky barrier height, which is equal to $\phi_m - X$. When the two materials are bought into contact, the fermi levels each side of the junction are equalised, resulting in no flow of charge. When a forward bias is applied, the fermi level in the semiconductor is raised above that of the metal, resulting in electrons with sufficient thermal energy to cross the barrier. When the reverse bias is applied, the fermi level of the semiconductor moves down, making the electrons require a higher thermal energy to be able to cross the barrier, resulting in the junction being rectifying, that is, having a much higher resistivity in reverse bias compared to forward.

Memristors are typically constructed using a metal-insulator-metal stack, which (when other conduction mechanisms aren't dominant) results in the formation of two Schottky barriers, one of which will always be reverse biased when voltages are applied to the device terminals, the current through which is governed by (2.1). [1]

$$I = AT^2 e^{-\frac{\Phi_{B0} - \alpha\sqrt{V}}{kT}} \tag{2.1}$$

Where I is the current, A is the area of the device multiplied by the Richardson constant, T is the temperature, V is the voltage applied across the device, Φ_{B0} is the Schottky barrier height at zero bias, α is the barrier lowering factor and k is the Boltzmann constant. For simplicity, the $\Phi_{B0} - \alpha\sqrt{V}$ term is sometimes expressed as Φ_{App}, the apparent barrier. In this mechanism, the change in resistivity is provided by the barrier lowering factor, with the applied bias altering the apparent barrier height. This switching mechanism tends to be more volatile when compared to filamentary devices, and is known to be present in TiO2 devices, though offers the advantage of greater analogue control of the device's resistivity. [23]

2.2.3 Temperature Effects

Metal oxides are insulators, however oxygen vacancies may be present in the active area of the devices under study. This leads to the conductivity of the metal oxide being dependent upon its temperature, with an increase in temperature leading to an increased conductivity, due to the liberation of charge carriers from the valence band.

In the case of high resistance metal/metal oxide/metal devices, the transport is typically controlled by the interface barriers formed. These Schottky interfaces formed by the metal-metal oxide contacts are known to be affected by temperature, resulting in an overall increase in conductivity, following equation 2.1.

The properties of thermionic emission are more pronounced in pristine devices. These effects may be observable in formed devices, but typically with decreased magnitude. This effect is introduced via the formation of metallically conducting filaments in the bulk material which behave in opposition to the interfacial mechanisms, increasing resistance with temperature. Depending upon the gaps present between filaments, carrier tunnelling effects may also be present, although, this is not temperature dependent.

This will result in an asymmetry in the response of formed memristors depending upon their state, with the high resistance state being more greatly reduced than the low resistance state due to the larger presence of Ohmic conduction mechanisms. [31, 34]

As the switching mechanisms for both ECM and VCM devices require the movement of charged particles throughout the device. In the case of VCM devices, this is through the

migration of oxygen vacancies, where increased temperatures will assist in the liberation of oxygen ions from the metal valences.[35] Given that the switching voltage of VCM devices is characterised by the voltage at which the resistance of the device changes by a certain proportion, this will both lower the switching threshold of the device, and increase the rate of resistance change. In the case of ECM devices, where metal ions are moved into the material of the device,

Temperature has been shown to decrease the switching voltages of ECM memristors, due to an increase in ion mobility, allowing for an increased rate of filament formation. This decreases the switching time of the devices, allowing for more rapid operation. [34, 36, 37, 38] This is a likely candidate for a global control implementation, allowing for the control of the device's sensitivity to stimuli, also known as the learning rate. These decreases in switching voltages were also observed to correspond with a greater separation of the HRS and LRS of these devices.

The temperature dependencies of VCM devices has not been studied as deeply, however a physics based model of a Pt/TiO/Pt memristor indicates that both HRS and LRS would be decreased with increasing temperature at proportionally similar rates, preserving the HRS/LRS ratio.[39] Furthermore, this model also predicts that switching times will decrease with increases in temperature and that the memory lifetime of a device will be reduced. In VCM devices where interfactial mechanisms are dominant, it can be expected that switching voltages will be decreased, due to the lowering of the effective barrier height, resulting in a larger voltage drop across the core material of the device, resulting in higher currents through the device, this will assist in the migration of oxygen vacancies within the device, which should increase the switching speed.

2.2.4 Humidity Effects

The effects of humidity on ECM devices fabricated from various materials have been researched, but the same experiments have yet to be applied to VCMs. It appears that the presence of moisture or oxygen are essential for the operation of metal oxide memristors, with devices ceasing to either form before electrical breakdown or switch resistive state while subject to vacuum conditions.[37] The application of atmospheric humidity to devices results in the absorption of water due to the nano-porous structure of sputtered materials. [40] This absorbed moisture adsorbs to the walls of the pores, altering the charge around these areas in the device. This is thought to increase the likelihood of ions travelling around the grains of the material rather than through them due to the presence of hydroxide ions in the areas between the material grains. These hydroxide ions will increase the conductivity around the grains and will also have the ability to oxidise metallic components within the material of the device. The magnitude of this effect is dependent upon the material, but the majority of research has been performed upon Hafnium and Tantalum Oxide devices. Devices have been shown to

vary in their recovery periods after moisture exposure, with Silicon Oxide memristors allowing absorbed moisture to desorb, restoring device behaviour, whereas Tantalum Oxide devices retain the absorbed moisture, only releasing it at high temperatures (over 600 K) under vacuum. The retention of moisture in Titanium Oxide has been shown, with strong adsorption properties making the study of the effects on performance more complex due to the difficulty in removing the present moisture. The requirement for high temperatures to remove the moisture from these materials is due to the strength of electro-chemical bonds between the polar molecules of water. The stronger the polarity of the metal oxides, the stronger the interaction between the two molecules, resulting in more thermal energy required to break the interaction and release the moisture. Due to the sputtered nature of the oxide layer in the studied devices, this will result in moisture being present throughout the oxide layer. [41]

The absorption of water by the oxide layers will not be instantaneous, due to the fact that the devices are not two dimensional, and the top of the device will be at least partially shielded from the ingress of moisture due to the presence of the top electrode, in addition to factors such as the fixed diffusion law. This states that the rate of diffusion of a substance is controlled by the concentration gradient, in the situation presented with these devices, the initial absorption of water will be faster due to the lack of moisture in the oxide, however, as the concentration of moisture in the oxide increases relative to the humidified air, this absorption will slow down. This means that when performing experiments involving these devices and humidity, they will have to be exposed to the moisture a period of time that will allow for the humidity to diffuse throughout the device.

The impact of these effects on TiO_2 devices has yet to be researched in conclusive detail, but the magnitude of the effects are known to be smaller than Tantalum and Hafnium Oxide devices, requiring a more careful methodology to isolate effects.

2.3 Artificial Neural Networks

Artificial Neural Networks (ANN) are systems built around functionality that resembles that found within natural neurons. [42] Each synapse has a parameter known as the weight. This weight determines the strength of the synapse's influence on a neuron, and can be altered via the process of potentiation, increasing the weight, or depression, a decrease of the weight. [43] In the case of a leaky-integrate-fire (LIF) neuron, an input is multiplied by a function of the weight of the neuron, this then goes into a "leaky" accumulator (the value stored in this accumulator will decrease to zero if no inputs are registered). Once the value in the accumulator reaches a threshold value, the output of the neuron will "fire" and output an impulse. [44, 45]

When it comes to getting these systems to work on data sets, they need to be trained.[46] One method of achieving this involves feeding the network a set of known data, and the output monitored, the more a neuron is used and has the "correct" output, the more it's weight will be increased, or in the case of an incorrect result, decreased, essentially resulting in the system coming to the correct answer via an iterative reward process, with each synapse converging upon an optimised value. [47, 48]

This process is of interest in computing as it provides the potential for ANNs to be capable of tackling non-standardised data, particularly present in fields such as image and pattern recognition [49, 50], and the systems ability to adapt their processing methodology leads to them being potentially useful in solving problems that are difficult to solve using traditional computing methods.

2.3.1 Homeostasis

Homeostasis is a cellular property by which the cell responds to internal or external changes in order to maintain a baseline condition. In the case of neurons, this causes the output of the cell to respond to changes in stimulation, as opposed to a steady state input. [51] This can allow the neuron to respond to maintain output functionality and stability when presented with abnormal input behaviours, such as those from damaged neurons. [52] This concept is of interest in the area of ANNs as it provides the potential for systems to self-adapt in order to overcome issues such as sensor failures without a loss of functionality. Homeostasis is typically achieved in circuits using spiking neural networks [53], where the output spiking rate can be controlled via altering the weights of the input synapses in order to balance their input strength to avoid overloading. This can either be controlled globally (all inputs altered at once), or on a synapse-by-synapse basis. The potential for individual synapse weighting leads to the idea of utilising memristors as artificial synapses.

2.3.2 Implementation of ANNs With Memristors

The ability for a memristor to vary its resistance results in it frequently being looked at as a potential for ANN implementation. [54, 55]

In this case, voltage spikes can be used to program a memristor to its desired weight, while smaller signals will leave the resistance of the device unaffected. This behaviour is similar to that of a natural synapse, where the repeated use of the synapse results in the increasing of the weight.

Memristors in ANNs also allow for the greater parallelisation of computations, a significant hurdle when it comes to implementing ANNs in traditional Von-Neumann computing systems. [56]

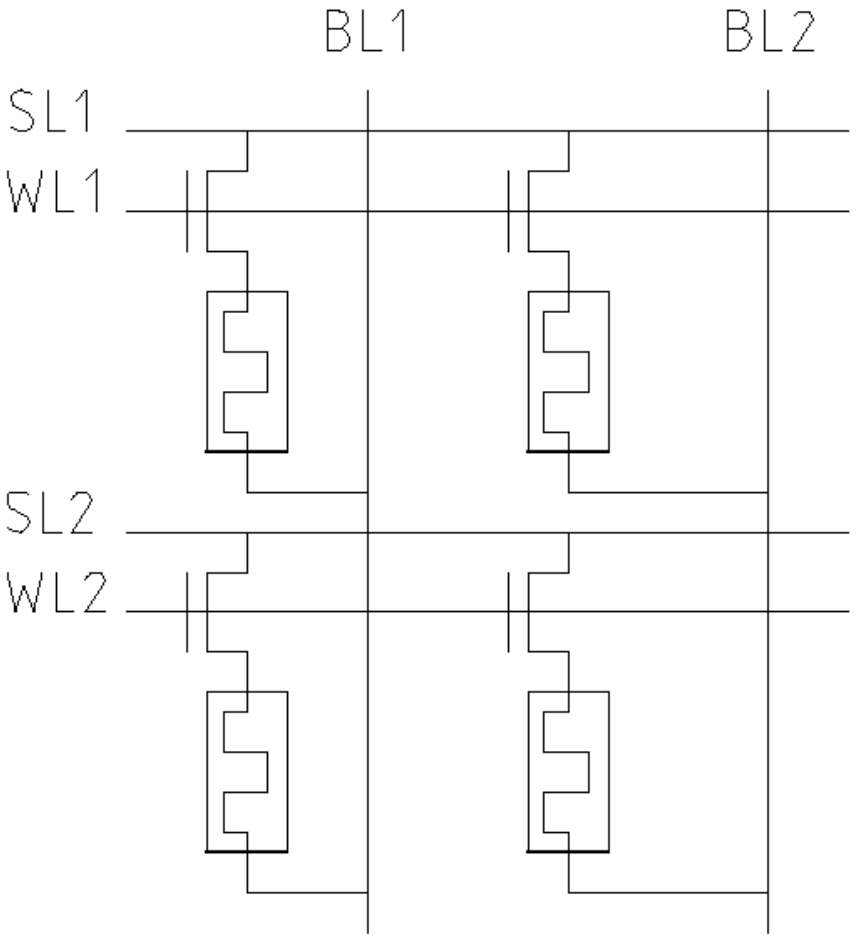

FIGURE 2.6: The schematic for a 1T1R memristor memory consiting of four memory cells, this may be expanded in either direction.

2.4 Memristors as Memory Storage

The main area of interest in memristor utilisation is in memory storage, particularly in the crossbar, 1T1R (one transistor, one resistor) configuration shown in figure 2.6. In this configuration, each memory cell requires only 2 components, and can be constructed in a crossbar array system. [57] This provides modular memory cells that can be constructed with very high density and are highly expandable, providing up to n^2 memory addresses, where n is the number of bit, source and word lines. While this structure is similar to DRAM (dynamic random access memory), the replacement of capacitors with memristors provides the potential for a much longer memory lifetime in combination with the memristor's ability to store multiple bits of information. This leads to the possibility of vastly improving upon the density and efficiency of existing solid state memory. [58, 26]

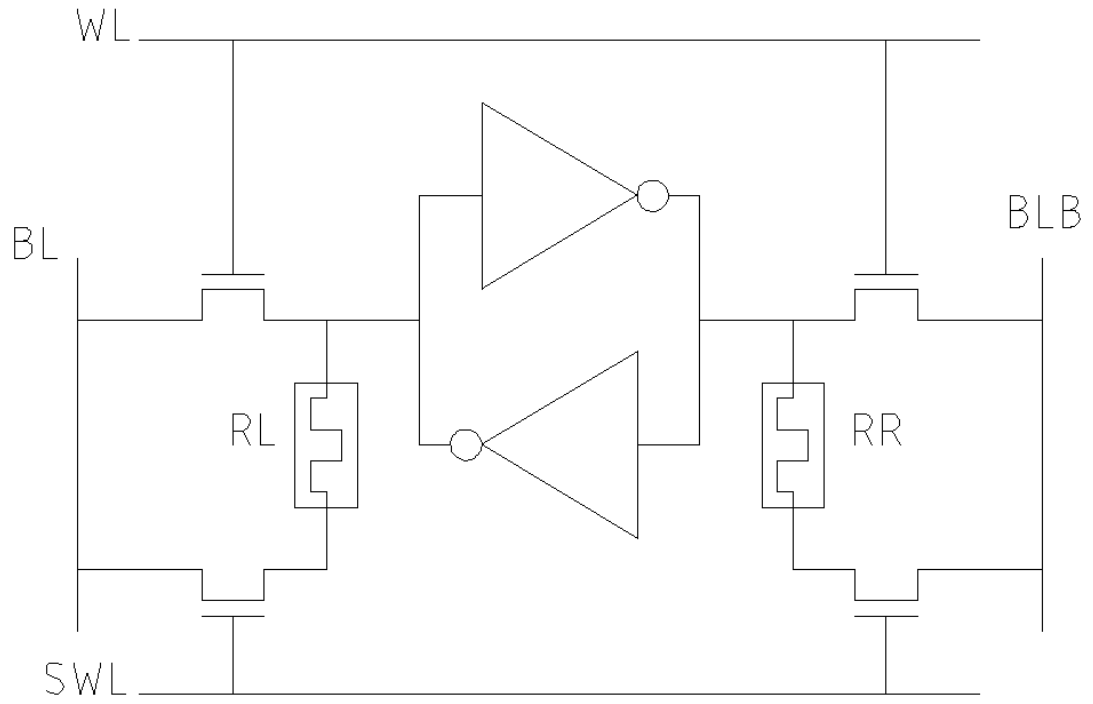

FIGURE 2.7: The schematic for a memristor based SRAM cell.

To perform a read operation the source line (SL) charges the bit line (BL) through the transistor and memristor. To perform a write operation on a specific device, the word line (WL) is charged, and the bit line for the selected device is charged to a voltage that will change the resistance of the memristor in that cell to an HRS or LRS. [59]

Memristors are also of interest in the designing of SRAM (static random access memory) cells, with one such schematic shown in figure 2.7. [60] The advantage this design provides compared to traditional SRAM cells is that the inclusion of the memristors results in the cell being non-volatile; the memory state of the cell will be maintained between power cycles.

The operation of this SRAM cell is as follows: during read operations, the switch line (SWL) is held low in order to isolate the memristors from any voltages that may change their values while the word line (WL) is pulled high to connect the complimentary outputs to the bitlines (BL and BLB). To write a value to the cell, the SWL line is pulled high, while the state to be written is held on both bitlines. If a "set" state is desired, BL and BLB are held high, this provides RL with a positive bias, switching it to the LRS. To apply a "reset" state, the SWL is again pulled high, and a negative voltage is applied to both bitlines, this applies a negative bias across RR, placing it in its HRS.

2.5 Environmental Sensing

2.5.1 Temperature Sensors

2.5.1.1 Thermistors

Thermistors are thermally dependent resistors, and are available with either a positive or negative temperature coefficient meaning that components can be selected to increase or decrease their resistance with increasing temperature. One operational method used to produce a positive temperature coefficient is through the use of carbon particles encased in plastic. With this type of device, the contact of carbon particles with each other is the method of resistance control, as the temperature of the thermistor increases, the plastic expands, moving the carbon particles apart, reducing the number of conductive paths through the device, increasing the resistivity. [61]

Negative temperature coefficient devices are typically manufactured from metal oxides, operating through the thermal liberation of charge carriers to decrease the resistivity as temperature increases. [62] Due to this relationship, the power dissipated by the device needs to be kept at a level where self-heating is not a significant effect. The majority of thermistors are non-linear devices, requiring either use of a Wheatstone bridge circuit to produce a more linear output [63], or through data processing using the equations governing the resistive response to temperature such as the Steinhart-Hart equation 2.2.

$$1/T = A + Bln(R) + Cln(R)^3 \tag{2.2}$$

Where T is the temperature (in K), R is the resistance at T and A, B and C are coefficients specific to each type of thermistor. [64] These systems are much more suitable for temperature measurement than thermostats, with some increase in complexity.

Another common use for thermistors is as a inrush current limiter in power supplies, as when a system is turned on, a large current impulse can be generated, possibly breaking fuses. This large current heats the thermistor, changing the resistance, resulting in a smoothing of the current impulse. [65]

2.5.1.2 Resistive Temperature Sensors

These devices use the properties of Ohmic conduction in a metal wire (generally platinum), resulting in a variation upon the positive temperature coefficient resistor. [66] These devices are linear unlike thermistors, making the processing of their output easier, and more accurate if processed well, and are able to operate over a wider temperature range due to the materials used. These devices are not very sensitive however, with

a lower temperature coefficient than those of thermistors. Mechanical stress may also produce errors in results due to deformation of the wires. [67]

2.5.1.3 Thermocouples

Thermocouples are one of the most widely used thermal measurement components due to their simplicity and operating range. These devices exploit the thermo-electric effect created when two dissimilar metals are in contact with each other. Two of these junctions are created, with one kept at a constant reference temperature, and the other used as the measurement probe. The thermal gradient along the wires generates a small voltage as per 2.3, where V is the voltage, S is the Seebeck coefficient and ΔT is the temperature gradient. [68, 69]

$$V = S * \Delta T \tag{2.3}$$

Due to the simplicity of their design, they are low cost and can be designed operate over a wide temperature range, however, they only generate small voltages, meaning that they require amplification to create a usable signal, increasing circuit complexity.

2.5.2 Humidity Sensors

2.5.2.1 Capacitive Sensors

Capacitive humidity sensors are capacitors manufactured using a hygroscopic dielectric. This dielectric absorbs a quantity of water proportional to the relative humidity of the atmosphere around it, as the dielectric constant of water is higher than that of the dielectric, the device's capacitance increases. In order to allow for the dielectric to have direct contact with the atmosphere, one of the contacts of the device is scored. As the relative humidity is a function of the temperature of the atmosphere, these sensors must be paired with a temperature sensor in order to provide accurate readings. The majority of humidity sensors used are capacitive due to their more linear nature, however, there is more complex circuitry required to measure the values from the device. [70, 71]

2.5.2.2 Resistive

Resistive sensors operate similarly to capacitive sensors, the material the sensor is constructed from (usually a hygroscopic polymer or metal oxide) absorbs moisture from the air. This increases the quantity of mobile ions, reducing the resistivity of the device. These devices are less suitable for measuring very low humidities due to the high

impedance. Again, these devices need to be paired with a temperature sensor in order to compensate for changes in the resistance with temperature. [71]

2.6 Memristor Modeling

Modeling refers to the process of attempting to mathematically describe behaviour and relationships observed in systems and devices and are a strong tool in many fields of study. [72] In the case of my research, models have been developed in order to help those developing circuits utilising the studied devices simulate their behaviours before having to resort to physical testing. For physical devices, four categories of mathematical model are used. These are stochastic, deterministic, behavioural and physics based. Stochastic models are models for which a given input will provide a probability of a certain output. These are most useful in statistical modeling, but given the nature of some memristor technologies, particularly filamentary devices, can be used to model switching behaviours, for example, at X voltage across the device, the probability of switching resistive state is Y, and the value of that state is most likely to be Z. [73] Deterministic models provide fixed relationships between input and result. This is more useful for devices where the switching behaviour is less dramatic than that of filamentary devices. In my work, I have developed deterministic models, due to the methods implemented in controlling the devices and the nature of their behaviour.

2.6.1 Physics Based Models

Physics based models attempt to match the behaviours of systems with existing physics based phenomena, for example, the schottky equation. [74] When modelling memristors, this is simpler for devices featuring fewer contributing conduction mechanisms, such as devices in the pristine state, and is more useful for understanding and analysing the underlying physics of the devices being modeled.[75]

2.6.2 Behavioural Models

Behavioural models are typically data-based and simpler to generate. These models apply fitting equations to data taken from the devices being studied in order to predict behaviours in devices or systems. [76] This method of modeling is more useful for design and simulation, as they are typically mathematically higher level, not requiring too much of an understanding of the internal workings of the devices being simulated.

2.6.3 Our Existing Models

My research group has developed several models that can be combined in an attempt to accurately simulate memristor behaviour in real-world applications. The behaviours modeled so far can be split into four categories, static IV, volatile switching, non-volatile switching and thermal.

2.6.3.1 Static IV

The static IV model developed during my work attempts to model the IV characteristics of a Pt/TiO based memristor across various resistive states, ranging from pristine to around 8kΩ in the voltage range of 0-1v, within the typical read voltage range. This model focuses on the IV relationship within the HRS of these devices, which is largely governed by interfacial conduction mechanisms. The equation for this model is presented in the form:

$$I = A(R)e^{B{V^C}_{(R)}} \tag{2.4}$$

2.6.3.2 Volatile Switching

Volatility in the case of memristors is described as the passive change in a memristor's resistance after a displacing stimulation has been applied.[77] This behavioural model was generated via displacing pristine devices from their "natural" state, as prior to forming the devices are completely volatile, leading to non-volatile characteristics being able to be excluded from the results. This relaxation, like the IV characteristics, follows a stretched exponential function. The generated model for this mode of switching is:

$$R(t) = \alpha exp^{-(t/\tau)^{\beta}} + \gamma \tag{2.5}$$

Where R is the device resistance, t is time in seconds, α is the relative initial displacement from R_0 caused by the stimulation, τ is the relaxation time constant, β is the exponential stretch factor and γ is the predicted saturation point at $t = \infty$. [78] The fitting of this model is demonstrated in figure 2.8. [79]

2.6.3.3 Dynamic Non-Volatile Switching

Non-volatile switching is defined as the non-time varying component of changes in resistance. [80] A model describing the change in resistance when stimulation is applied to the device was developed. [81] This model was generated in several layers. The high level description of the switching behavior is described using

$$\frac{dR}{dt} = m(R, v) = s(v)f(R, r(v)) \tag{2.6}$$

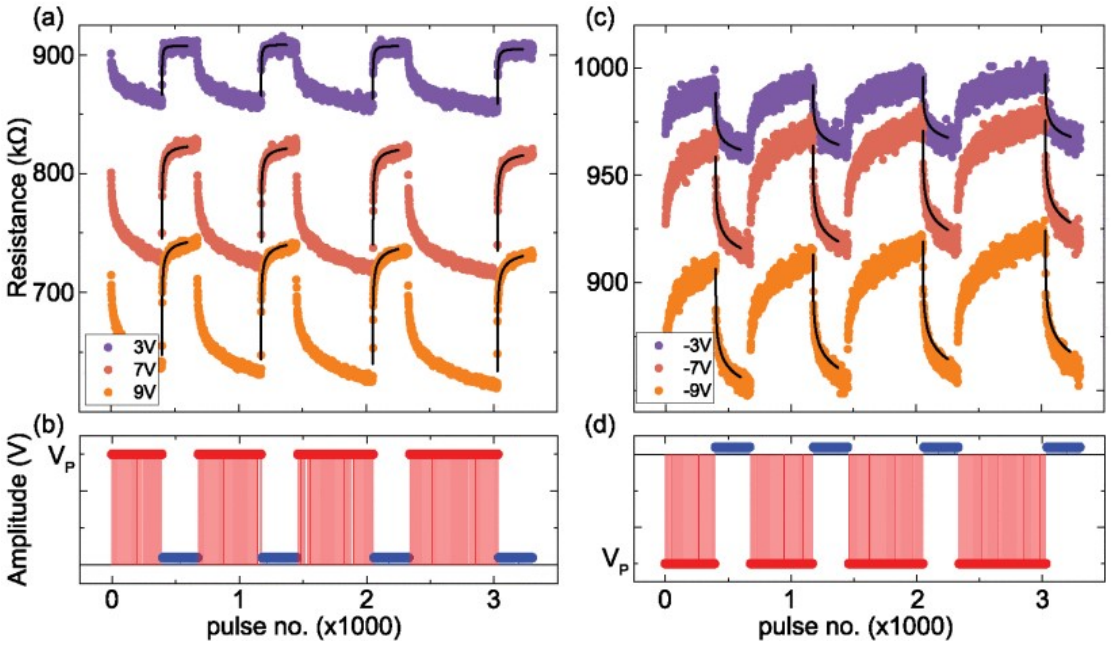

FIGURE 2.8: The fitting of the volatility model for (a) positive and (c) negative stimulation, with the corresponding stimulation protocols shown in (b) and (d). *C.Giotis 2020*

In this equation, $m(R, v)$ is a three dimentional surface (figure 2.9 [81]) correlating device switching rate to the initial resistance R_0, and the stimulus voltage v. The function $s(v)$ is the device's switching sensitivity, which is determined by the stimulation voltage and $f(R, r(v))$ is the device window function, which is determined by both the device's resistance at the time of measurement, and the device "absolute voltage threshold", or, the switching threshold $r(v)$.

Going a level further into this model gives the functions the definitions of:

$$r(v) = \begin{cases} r_p(v) = a_0 + a_1 v, v > 0 \\ r_n(v) = b_0 + b_1 v, v \leq 0 \end{cases} \tag{2.7}$$

$$s(v) = \begin{cases} A_p(-1 + e^{\frac{|v|}{t_p}}), v > 0 \\ A_n(-1 + e^{\frac{|v|}{t_n}}), v \leq 0 \end{cases} \tag{2.8}$$

In these equations a_0,a_1,b_0,b_1,A_p,A_n,t_n and t_p are fitting parameters. When these expansions are re-incorporated into the basic form of the model, it results in the expression

$$\begin{aligned} \frac{dR}{dt} = m(R, v) = A_p\Big(-1 + exp\Big(\frac{|v|}{t_p}\Big)\Big) stp(r_p(v) - R)^2 stp(v) + \\ A_n\Big(-1 + exp\Big(\frac{|v|}{t_n}\Big)\Big) stp(R - r_n(v))^2 stp(-v) \end{aligned} \tag{2.9}$$

where stp represents the step function.

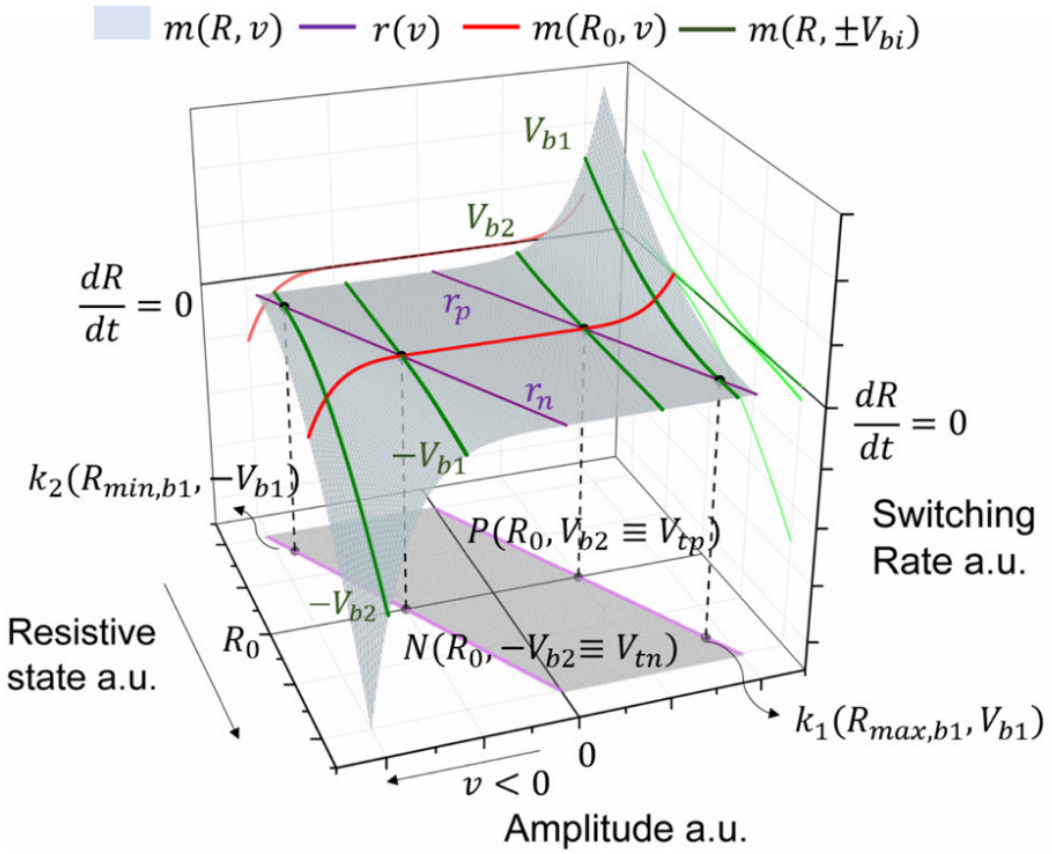

FIGURE 2.9: An example switching surface generated from the dynamic non-volatile switching model. Green lines correspond to the change in resistance over time when the device has a constant bias placed across it, while the red lines depict the relationship between the rate of resistance change compared to the bias voltage when switching from the same R_0. The purple lines show the absolute voltage threshold function, where biases within this window will not affect the resistance of the device. *Messaris 2017*

2.6.3.4 Thermal Switching Model

From data produced over the course of my research, a model for the switching behaviour of the studied devices was developed. For this model, a train of switching pulses were applied to a device, alternating polarity and increasing voltage, see figure 2.10.[82] It was noted that the first switching pulse would result in the largest change in resistance, with subsequent pulses incrementally altering the resistance of the device more gradually. The shape of the switching curve was modelled for constant voltage stimulation, providing saturating curves which were subsequently fitted to data at different voltages, providing a model with the expression

$$\frac{d\Delta R}{dt} = s(V,T)exp\left(\frac{\Delta R}{R_p(V,T)}\right) + \frac{d\Delta R}{dt}|_{t=0-} \tag{2.10}$$

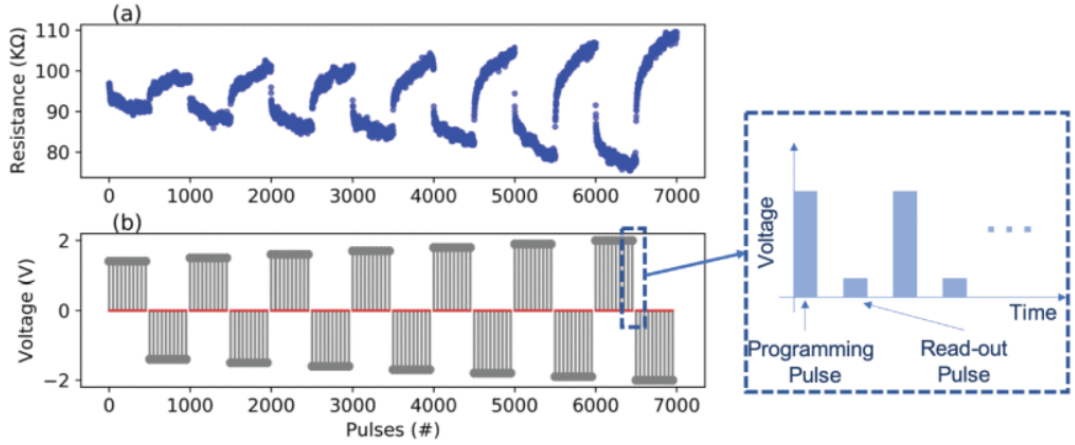

FIGURE 2.10: (a) The observed saturating behaviour of the memristors under switching voltages, (b) The stimulation protocol. *Vaidya 2021*

Where s and R_p are fitting parameters, V is the stimulation voltage, T is the device temperature, R is device resistance and t is time. If the device is starting from equilibrium (i.e no previous stimulation pulses applied), then the $\frac{d\Delta R}{dt}|_{t=0-}$ expression becomes 0, leading to the equation having the form

$$\Delta R(t) = -R_p \, ln\left(\frac{-st}{R_p} + exp\left(\frac{-\Delta R_0}{R_p}\right)\right) \tag{2.11}$$

where ΔR_0 is the initial discrepancy from R_0. As the stimulation method is pulsed rather than a continuous voltage, this expression is subsequently expanded to describe the resistance at the end of the nth stimulation pulse.

$$\begin{aligned} \Delta R_n &= -R_p \, ln\left(\frac{-st_w}{R_p} + 1\right) \; for \, n = 1 \\ \Delta R_n &= -R_p \, ln\left(\frac{-st_w}{R_p} + exp\left(\frac{-\Delta R_{n-1}}{R_p}\right)\right) \; for \, n > 1 \end{aligned} \tag{2.12}$$

In these expressions, t_w is the pulse width of the stimulation pulses. With the model for switching behaviour at constant temperature complete, the next stage of generating this model is to calculate the thermal dependencies of each parameter. Fitting these equations to data taken from two memristors at varying temperatures resulted in s and R_p having the forms of

$$s(V,T) = s_0(T) \tag{2.13}$$

$$R_p(V,T) = A(T)exp(k(T)V) \tag{2.14}$$

where all variables other than voltage and temperature are fitting parameters. Fitting the temperature dependencies of s_0, A and k gave rise to the third and final layer of the

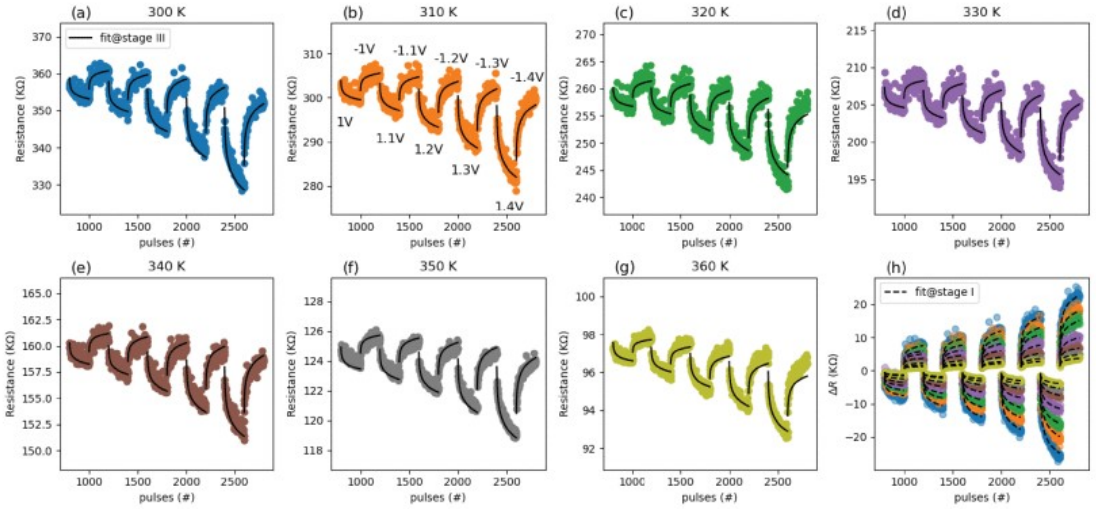

FIGURE 2.11: The fitting of the thermal switching behavioural model, showing the device at different temperatures (a)-(g), and (h) the relative switching model for this device. *Vaidya 2021*

model, with these variables being governed by a polynomial relationship of

$$s_0(T) = p_2^{s_0}T^2 + p_1^{s_0}T + p_0^{s_0} \tag{2.15}$$

$$A(T) = p_2^{A}T^2 + p_1^{A}T + p_0^{A} \tag{2.16}$$

$$k(T) = p_2^{k}T^2 + p_1^{k}T + p_0^{k} \tag{2.17}$$

The final fitting of this model is shown in figure 2.11. [82]

2.6.3.5 Physics Based Thermal Switching Model

In addition to this behavioural model of switching, a physics based model was also developed beginning with an analysis of the temperature dependencies of the dominant conduction mechanism, [83] the Schottky emission equation:

$$I = AA_m^* T^{C_T} exp\left(- \frac{q(\phi_B - \alpha\sqrt{V}}{k_B T} \right) \tag{2.18}$$

This slightly modified version of the previously shown Schottky equation features A_m^* and C_T, the former being the modified Richardson constant, and the latter is a fitting parameter. The area of the device is also separated from the Richardson constant in this instance. From this relationship, a static IV model was developed with the form

$$ln(I) = A' + \frac{q\alpha\sqrt{V}}{k_b T} \tag{2.19}$$

from this equation, the temperature dependence of α is defined as

$$\alpha(T) = \alpha_2 T^2 + \alpha_1 T + \alpha_0 \tag{2.20}$$

the resistance of a device at two temperatures can subsequently be expressed as a ratio

$$\frac{R(T_1)}{R(T_2)} = \left(\frac{T_1}{T_2}\right)^{C_t} exp\left(\frac{q(\phi_B - \alpha\sqrt{V_r}(T_1 - T_2))}{k_B T_1 T_2}\right) = \kappa(T_1, T_2) \tag{2.21}$$

where V_r is the resistance read voltage. Combining this expression with 2.12 results in the following equation.

$$R_n(T_2) = \kappa R_0(T_1) - \kappa R_p(T_1)\, ln\left(\frac{-\kappa s(T_1) t_w}{\kappa R_p(T_1)} + exp\left(\frac{\kappa(R_{n-1}(T_1) - R_0(T_1)}{\kappa R_p(T_1)}\right)\right) \tag{2.22}$$

This equation allows for the prediction of $R(T_x)$ for any temperature within the valid range provided that a value of $R(T_y)$ is known. Within this equation it is inferred that:

$$s(T_2) = \kappa(T_1, T_2) s(T_1) \tag{2.23}$$

$$R_p(T_2) = \kappa(T_1, T_2) R_p(T_1) \tag{2.24}$$

These expressions indicate that the switching behaviours of a device will be scaled by changes in temperature in line with the Schottky equation.

Chapter 3

Development of the Environmental Control Microchamber

The work undertaken in this project led to the requirement of a system that allows easy, user-definable control of environmental parameters. This resulted in the continued development of an environmental control micro-chamber, a previous, less advanced version of which was developed as a part of my undergraduate degree. An intermediate version of this apparatus was published in the proceedings for ISCAS 2018, with the final version being presented and demonstrated at the conference in May and at Memrisys 2018 in July. [84] Electrical measurement of the devices is performed using the ArC One memory characterisation platform, a system developed within the research group, resulting in the micro-chamber being designed around use in conjunction with this system.

3.1 Undergraduate Work

3.1.1 Construction

The version of the micro-chamber developed for my undergraduate degree featured a 3D printed chamber body sealed by silicone o-rings, capped with a PCB containing environmental sensors for temperature, humidity and pressure. This system was secured over the package in the ArC One. This system was connected to an Mbed LPC1687 microcontroller which would interpret the data received from the sensor board and provide transducer control signals determined by proportional integral derivative control (PID) software. The information from the sensors is relayed to the user through use of a terminal window on a host computer.

Pressure control was achieved using solenoid valves on the input and output, providing air flow control, with a pressurised input provided via manual operation of a syringe. Two approaches for the flow rate control were attempted, one being the partial opening of the valves using higher frequency pulse width modulation and the second being the pulse width modulation of the valves using lower frequencies. Due to the operation of the solenoid valves, it was discovered that partial opening of the valves was impossible, so the latter approach was developed and implemented.

Temperature control was designed but not implemented due to issues with the sensor. The heating method was designed to use a resistor through which current was pulse width modulated to allow for variation in heating power. The use of 3D printing for the manufacture of the body of the chamber was chosen due to cost and manufacture time. This method of manufacture provided some level of pressure retention and would allow for temperature control within the specified limits of up to 20°C above ambient.

3.1.2 Results

This system achieved control of chamber pressure up to 50kPa above ambient with a +5% -25% accuracy. Temperature control in the system was unsuccessful, due to issues with the temperature and humidity sensor, but specific heat capacity calculations indicated that temperature control would be possible with the implemented heating system, with a target temperature increase of 20K above ambient in this version of the design, humidity was only to be monitored in this prototype.

3.2 Apparatus Refinement

3.2.1 Temperature Control and Construction

The first stage of my work was to improve the functionality of the micro-chamber, the key development being the addition of humidity control. Firstly, temperature control was achieved after achieving monitoring of both temperature and humidity, the issue with which was found to be destruction of the sensor during assembly. This was then used to enable the control of the chamber temperature through the resistive heater. The temperature increase prediction model was updated utilising Fourier's law of conduction 3.1. This equation isn't fully suited for the system due to the lack of terms governing the loss of energy via convection and radiation, however, only a rough estimate of the power required to reach certain temperatures is needed.

$$\frac{q}{A} = \frac{k\Delta T}{s} \tag{3.1}$$

Where q is the heat flux (the heater power at equilibrium) in W, A is the surface area of the system under consideration in m^2, k is the corresponding thermal conductivity in W/m K and s is the thickness of the surface in m and ΔT is the temperature difference between the two sides of the chamber wall in K. The chamber model was approximated as a cylinder with solid 1cm thick PLA walls, capped with a PCB on one end and ceramic on the other, which immediately highlighted the need for a much more powerful heater to achieve the target temperatures, and upon physical testing predictions were within 2°C of the maximum temperatures achieved by the system. The power of the heating element was increased from 0.1W to 1.2W and the 3D printed chamber replaced with a CNC milled PMMA version allowing for a far more precise design due to not having to account for varying thermal expansion/shrinkage and resolution of the 3D printed version which varied depending on the age and quality of the PLA filament used for manufacture, while providing a much more robust chamber. This allows for much higher temperatures to be achieved without endangering the integrity of the chamber, indicated by the glass transition temperature of the materials (varying between 85-165°C for PMMA [85] vs. 60°C for 3D printed PLA) this increase in power allowed for the system to achieve the target set for the initial prototype of an increase in temperature of 20°C, with a maximum temperature increase of 22.4°C above ambient achieved. With the change in material of the chamber body, the heater power was increased further from 1.2W to 4.7W in order to allow the system to reach temperatures over 85°C to allow for thermal ageing tests at industry standard temperatures and increase the temperature in the chamber more rapidly. A further change made to the construction of the system was the replacement of the o-ring between the top PCB and chamber body with a thick rubber gasket, with aims to reduce the thermal losses from the chamber through the PCB, which was the area of the micro-chamber with the highest thermal conductivity. Using the old model of the system the theoretical maximum temperature of the system put the maximum temperature increase at 98.6°C when using the same model as before, with an additional 3mm silicone layer and the wall materials changed from solid PLA to solid PMMA, due to the thermal conductivity data for laserable rubber not being available. Physical measurements indicated a maximum increase of around 120°C, both theoretical and measured results were beyond the maximum operating temperature of both the temperature sensor, the acrylic body and the socket holding the DUTs, so the temperature control system was calibrated to minimise overshoot. The final version of the micro-chamber and its electronic schematics can be seen in figures 3.1 and 3.2.

The system was altered from something to be mounted to the ArC One, to a separate peripheral, as a breakout board holding the DUTs, connected to the ArC via ribbon cables, enabling a re-design of the securing mechanism for the micro-chamber to the device. The mounting/securing method for securing the chamber over the devices was updated to screws, which offered far greater security and an improved seal. The improved system can control temperatures up to 90°C with less than $\pm$1% error as shown in figure

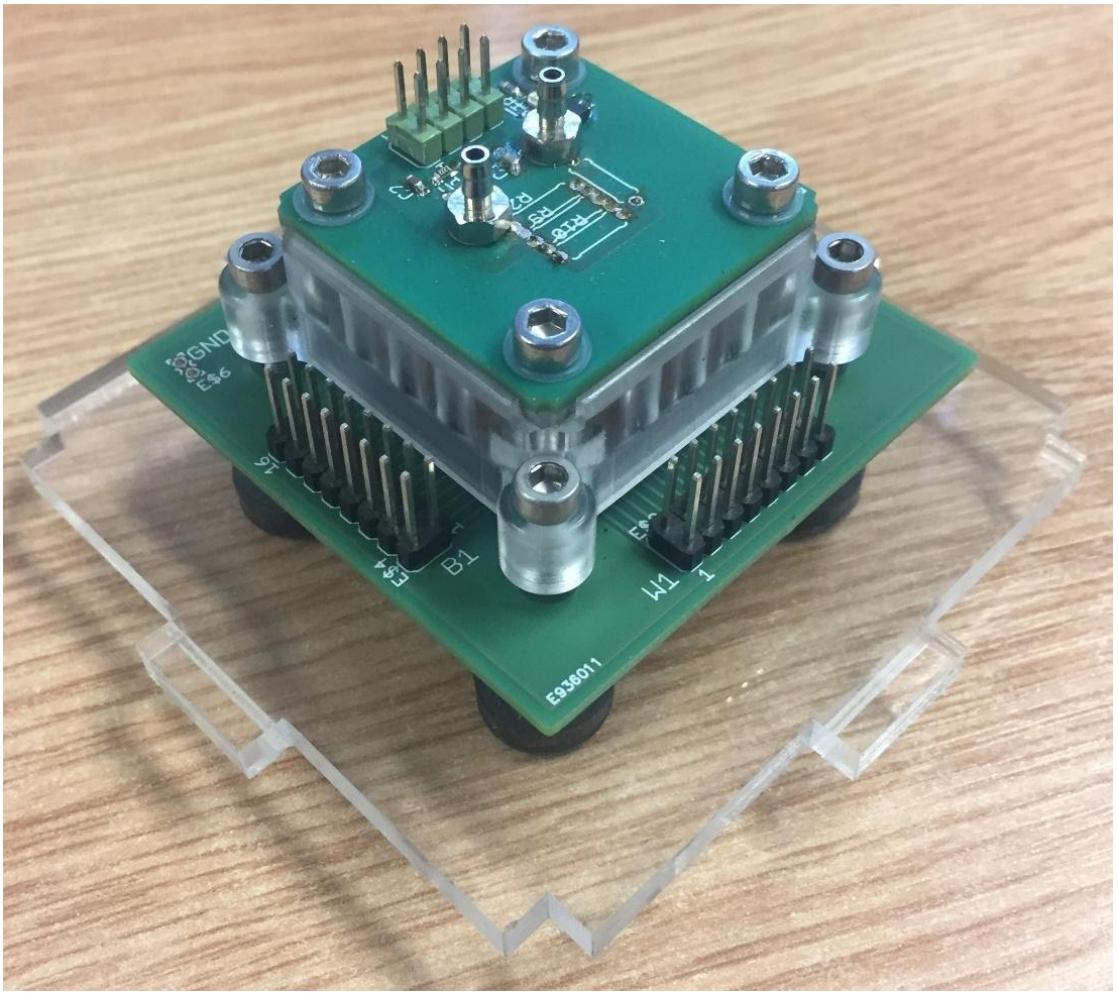

FIGURE 3.1: The final micro-chamber design with the PMMA body secured over a memristor package using the updated securing system.

3.3, with temperature software limited as pushing the system any higher could result in damage to the body and components of the micro-chamber.

The connections for the system were updated to ensure the system was more user friendly, requiring a minimal amount of setup before use. A manifold control board was designed and added to the system, condensing the solenoid valves, switching transistors, indicator LEDs and microcontroller onto one PCB. There are only two essential connections between the manifold PCB and the micro-chamber, a ribbon cable for communications and power transfer, and a silicone tube connecting the output of the manifold to the micro-chamber. An optional extra is the addition of a tube between the micro-chamber and the exhaust section of the manifold to allow for reduced gas flow and recycling. The full experimental setup can be seen in figure 3.5.

An acrylic safety enclosure was also designed due to the system being capable of reaching potentially hazardous temperatures. This enclosure isolates the user from the chamber, preventing accidents. It is manufactured using 5mm acrylic with several finger joints on each piece to ensure the enclosure is sturdy and will not move or fail during operation,

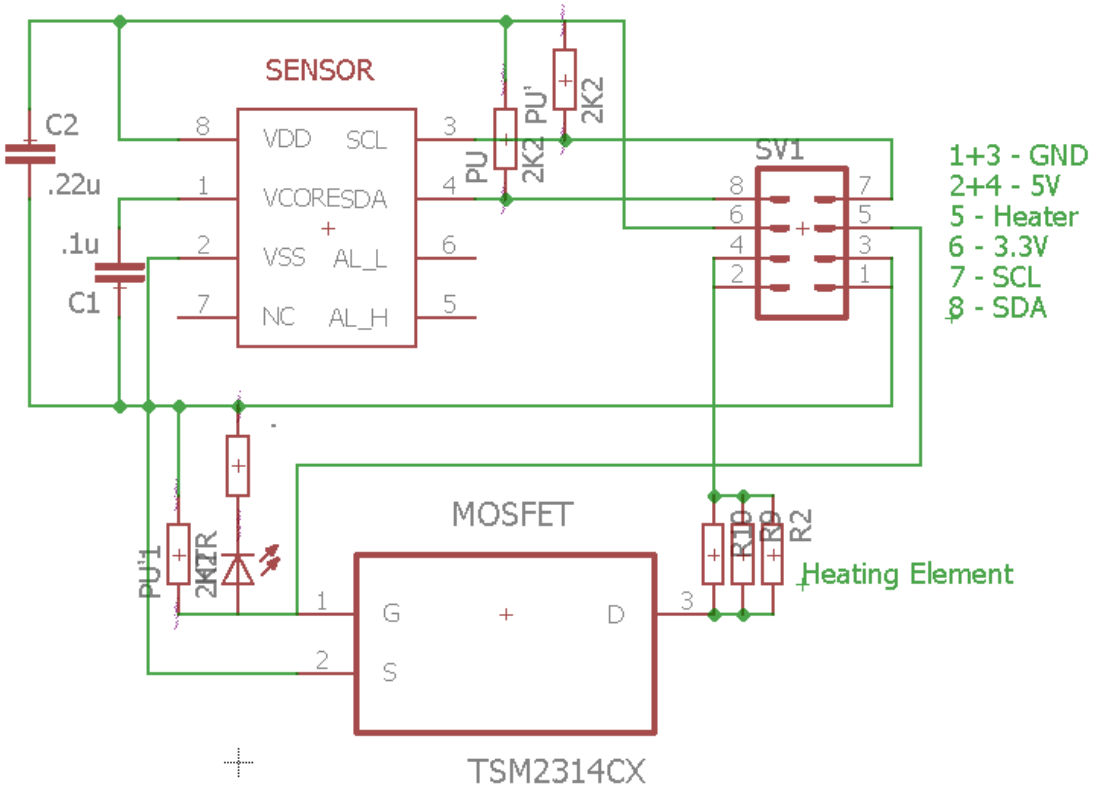

FIGURE 3.2: Schematic for the final micro-chamber design. The sensor is a Honeywell HIH6130 and SV1 is a 8 pin header to which the ribbon cable is connected.

even if subjected to mechanical force. Each section is held to the other sections via use of metal 90° angles, nuts and bolts in order to simplify manufacturing procedure while maximising strength. The micro-chamber and breakout board are attached to the base of the enclosure, which is in turn locked onto the bottom of the enclosure through the use of four latches, which lock into grooves etched on the underside of the base. Slots have been made in the walls of the enclosure to allow for connections to the chamber using ribbon cables between the ArC One and the breakout board for the devices, the micro-chamber and control manifold, shown in figure 3.4.

3.2.2 Pressure Control

Improving the level of control over pressure was attempted, using a combination of high and low resistance air flow paths selected via solenoid valves with master on/off solenoid valves to create pressure inside the chamber with a smoother control response, essentially trying to implement the previously attempted partial opening of the solenoid valves. Numerous methods of creating the high resistance paths were attempted, generally based on 3.2. [86]

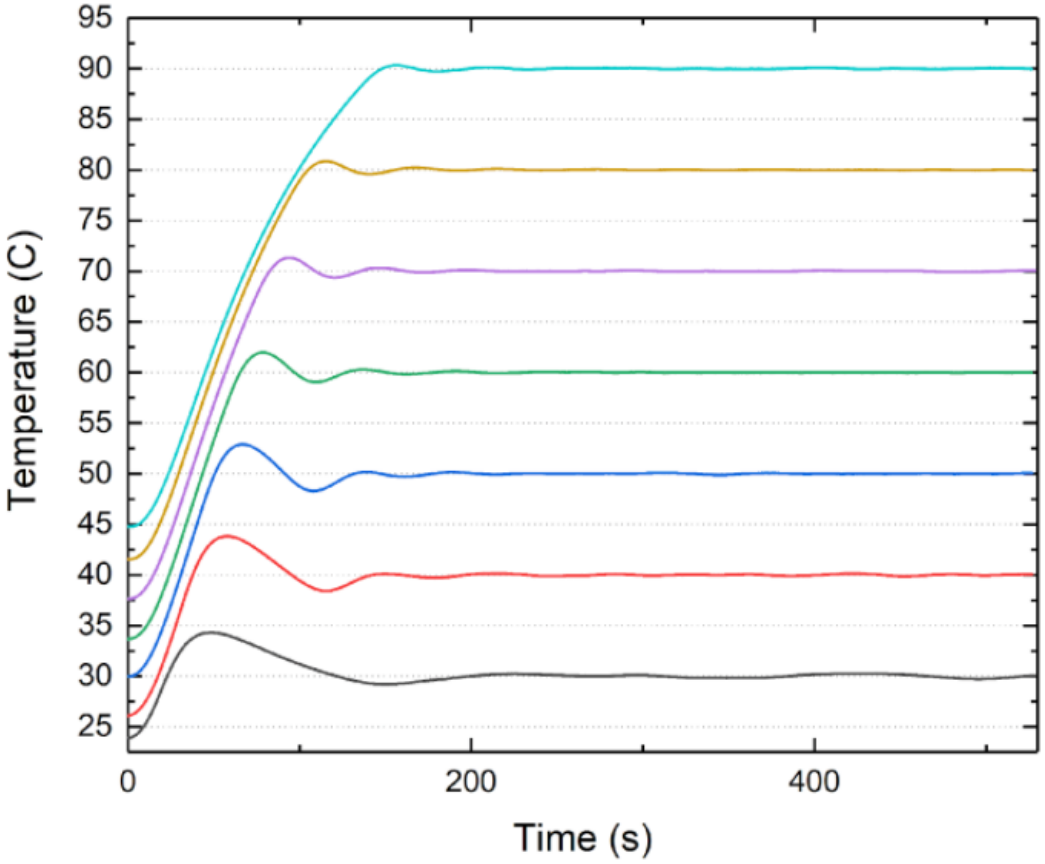

FIGURE 3.3: The temperature control response of the final micro-chamber design, with the target temperature set from 30°C to 90°C in 10°C steps.

$$Q = \frac{\pi D^4 \Delta P}{8 \mu L} \tag{3.2}$$

Where Q is the volumetric flow rate in ml/s, ΔP is the pressure differential across the tubing in Pa, μ is the dynamic viscosity of the fluid in N s/m^2 and L is the length of the path in m. The first approach attempted was the design of a microfluidic manifold to which solenoid valves would be mounted, with the restriction being provided by micro channels etched in acrylic. This method would provide the most precise and reliable control, but the cost proved prohibitive. The concept of a manifold with mounted solenoid valves was kept and expanded upon, developing into a sandwich of two acrylic layers with a silicone gasket between them, seen in figure 3.6.

Cheaper alternatives to the flow restriction problem were investigated including passing the air through capillary tubing and tubing stuffed with open cell foam. These methods proved either too fragile, or too inconsistent to be useful. In the end it was discovered that the natural flow restriction resulting from the manifold was sufficient. This flow restriction was introduced via the tightening of the assembly nuts and bolts around the edge of the manifold, partially crushing the sealing gasket into the channels of the acrylic

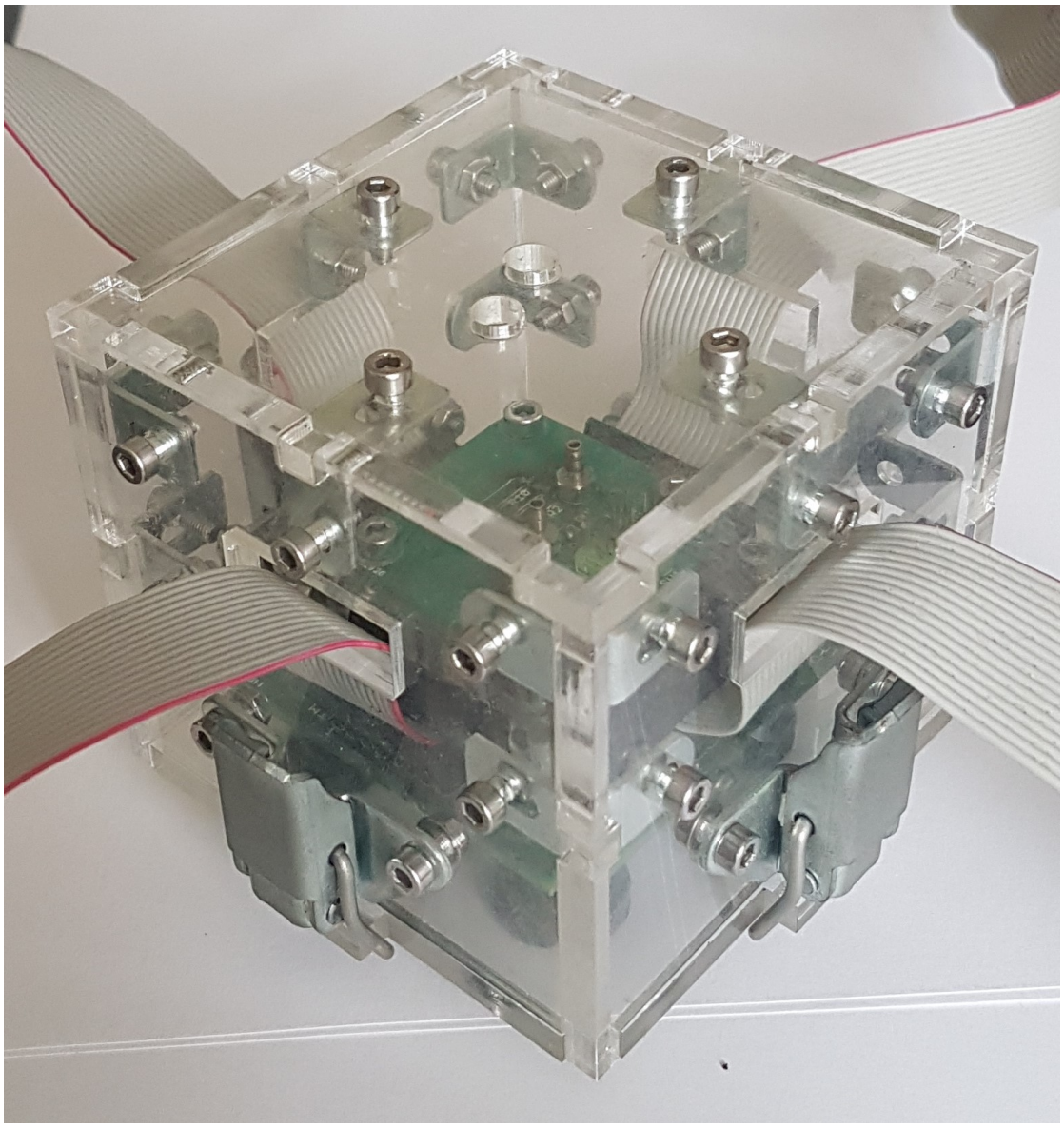

FIGURE 3.4: The microchamber with the enclosure and ribbon cables for memristor connections.

pieces, reducing their effective diameter. It was discovered that despite the silicone gasket, there was leakage of air from the manifold as when connected to the manifold, the ability of the chamber body to retain a pressure was greatly reduced. This leakage measured and investigated by forcing air through the system using a syringe in order to fill a second syringe attached to the output. While not entirely accurate due to the compressible nature of gas, it did provide information as to the approximate leakage levels in the system, with initial results showing a 50% loss in the air through the manifold. To reduce this, a thin layer of silicone glue was applied to the gasket before assembly, reducing the loss of air through the manifold to approximately 5%.

It was discovered that using an unstable pressure source for the system induced further instability in the control system, which was the case when using a manually operated

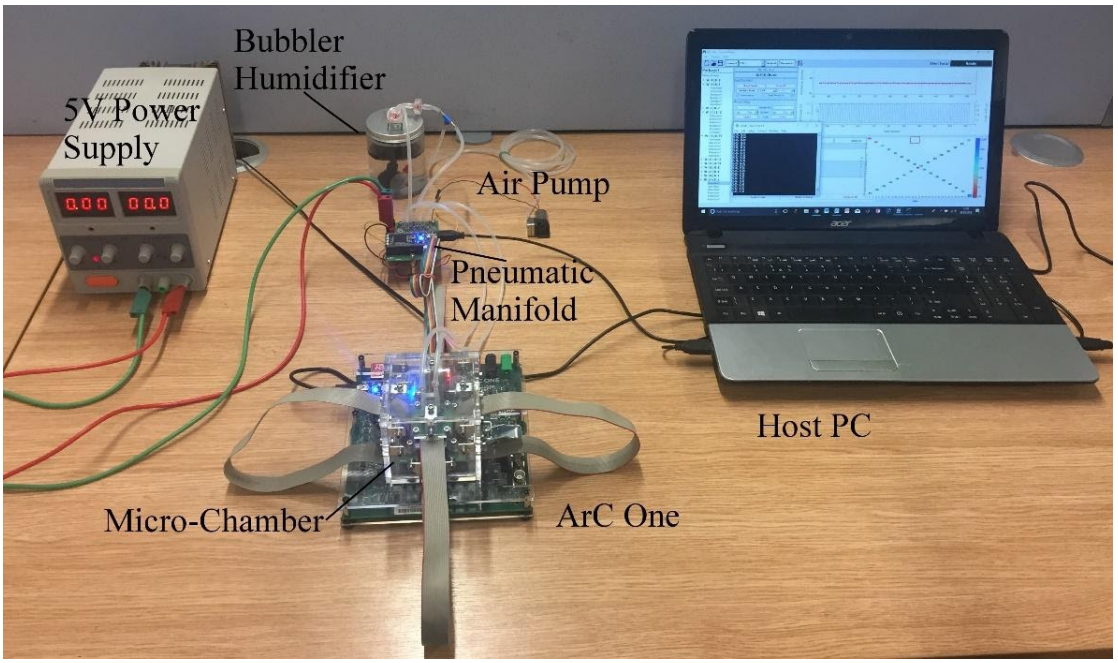

FIGURE 3.5: The final chamber operational setup with all components used.

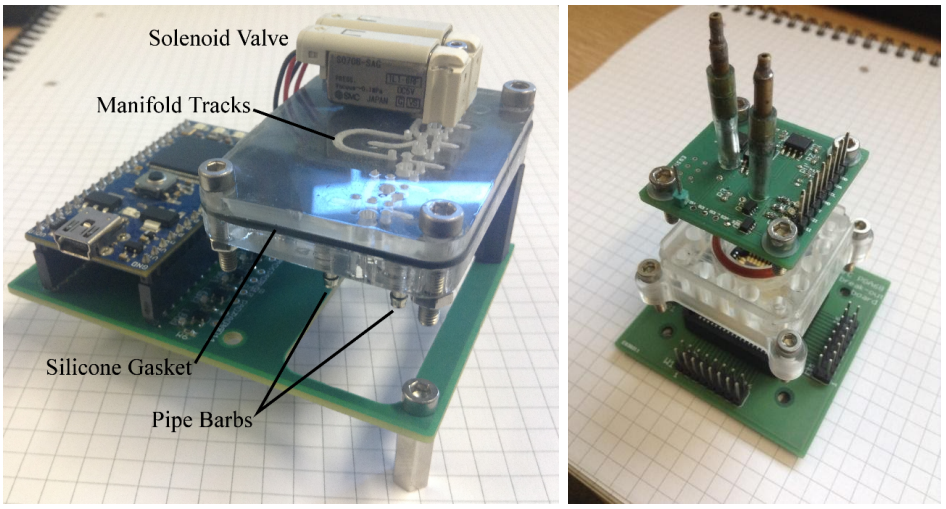

FIGURE 3.6: Left, an exploded view of the first manifold design manufactured with four of the solenoid valves removed to show the manifold tracks, and right, an exploded view of the accompanying micro-chamber. This version of the micro-chamber was published in the proceedings for ISCAS 2018.

syringe to provide gas pressure. This was remedied via the use of a pump and pressure reservoir in order to provide a steady source pressure that was minimally impacted by the operation of the solenoid valves. In the end, pressure control was achieved with a ±5% error up to 50kPa above ambient, shown in figure 3.7, with a source pressure of up to 100kPa.

The effects of atmospheric pressure increase were tested on formed Pt/TiO2/Pt devices, with the effects found to be negligible at the pressures achievable with the system, which is in line with existing research. [36]

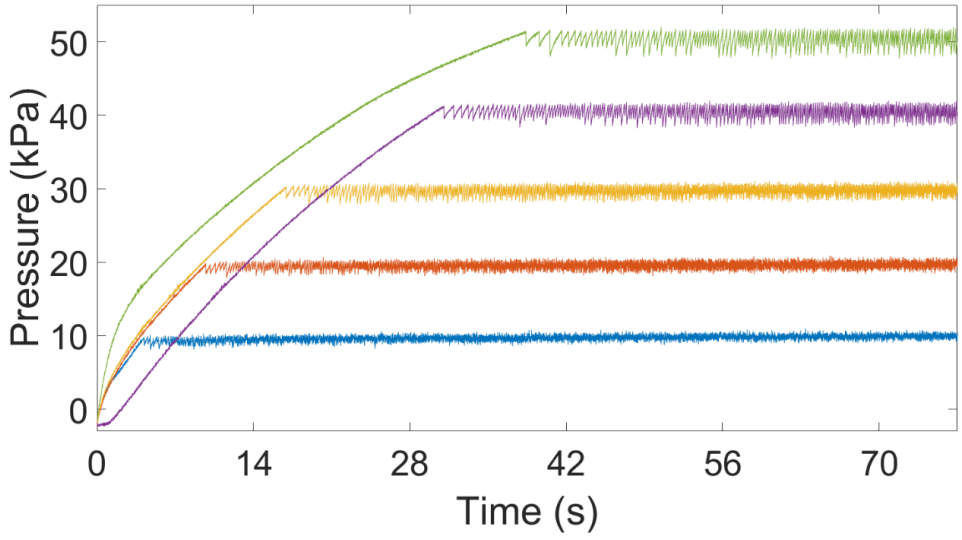

FIGURE 3.7: The achieved pressure control response of the micro-chamber with targets of 10kPa to 50Kpa in 10kPa steps. The ramp up time is a result of the gradual pressurisation of the pressure reservoir.

3.2.3 Humidity Control

Humidity control was developed alongside pressure control, however, it was discovered that the low air flow rates required for accurate pressure control prohibited the control of humidity more than a small amount above the ambient conditions. The minimal observed impact of pressure on memristor performance observed led to the abandonment of pressure control as a focus for the system, and subsequent implementation of humidity control as the sole pneumatic function, as there was evidence in literature to support the fact that humidity would have a more significant effect upon the behaviour of a memristor. [36, 37] This was built upon the existing framework of the pressure control, utilising solenoid valves, a pneumatic pump and a manifold with the addition of a bubbler humidifier. In order to reach high humidity using a bubbler, the airflow required is much greater than that which was required for the pressure control, subsequently, the manifold was re-designed to minimise the track resistance, with the tripling of the channel width and increase in depth. The manifold was reduced in size, improving the seal between the gasket and acrylic surfaces, and reducing the required track lengths. This alteration would in turn reduce the air loss through the manifold without use of a gasket sealant. This system is shown in figure 3.8. These alterations enabled a maximum controllable humidity of 80% at room temperature to be achieved shown in figure 3.9. This maximum achievable humidity decreases rapidly with temperature, resulting in temperature and humidity control being dependent. [87]

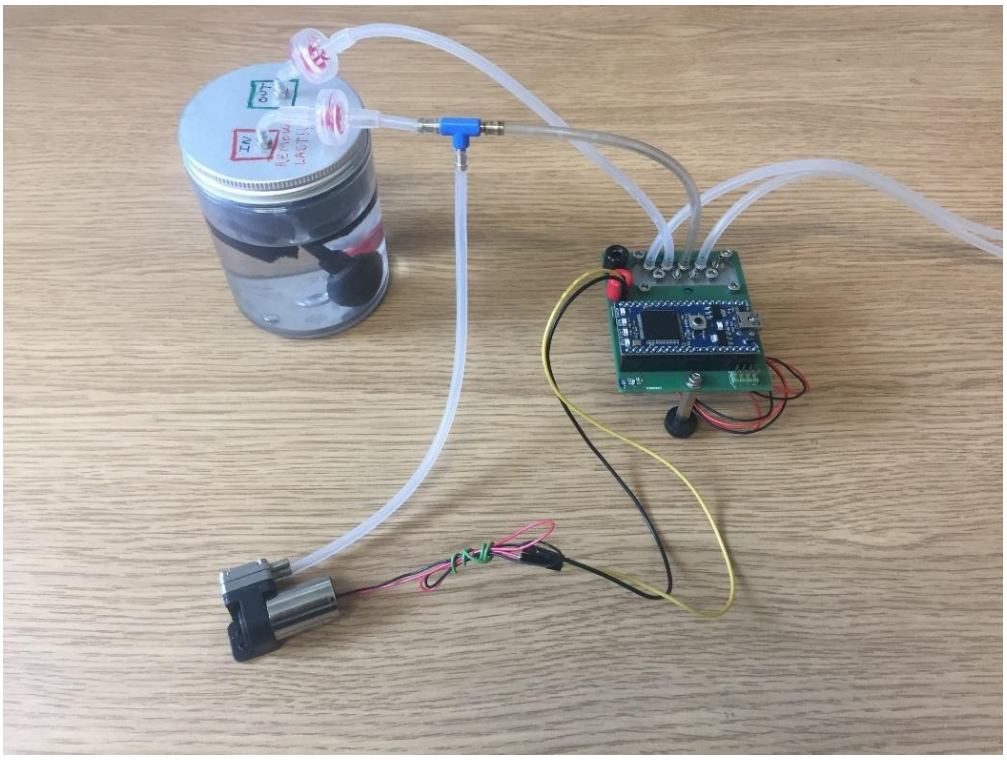

FIGURE 3.8: The components required for humidity control of the system. The pump (bottom) provides air flow which is split to either go straight to the chamber via the manifold (right) or through the bubbler (left) to humidify it first.

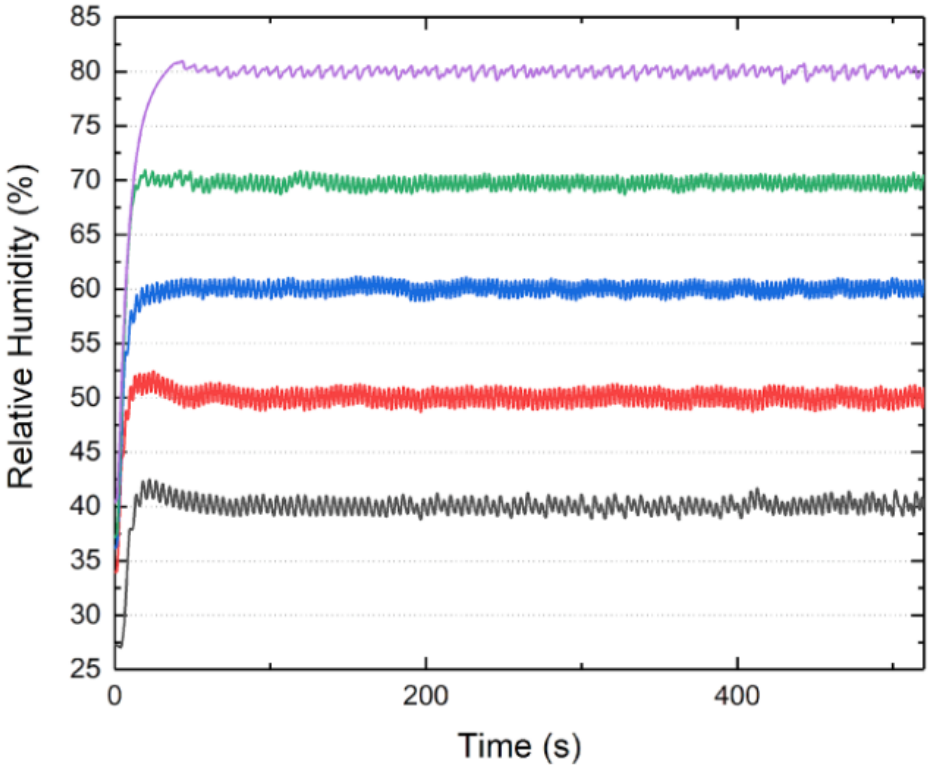

FIGURE 3.9: The control response of the humidity control system for the final version of the micro-chamber when set targets of 40% to 80% in steps of 10% relative humidity at room temperature.

Chapter 4

Temperature Dependencies in Metal Oxide Memristors

4.1 Devices Used

The primary devices used for my research consist of a sputter deposited 10nm platinum top electrode, 25nm titanium oxide layer and a 20nm gold bottom electrode. These devices have an area of 20x20µm and were manufactured on an oxidised silicon substrate with an additional 5nm titanium adhesion layer, this stack is depicted in figure 2.1. These devices were manufactured by Dr Ali Khiat. This device architecture was selected due to the increased stability of pristine devices compared to devices with platinum for both electrodes, with pristine Pt/Pt devices presenting loops in their IV curves at high enough voltages. In order to be used with the micro-chamber, the devices had to be packaged. This was achieved by cutting the die from the wafer and bonding the die to a PLCC68 package using epoxy cured by heating at 120°C. After this, gold wires are bonded to the pads of the die, connecting them to the external pins of the package. This process was performed by Dr Spyros Stathopoulos.

4.2 Conductivity Effects

Experiments investigating the effects of air temperature on the conductivity of memristors were an initial focus of my research. Early results showed that pristine devices are more sensitive to temperature changes than formed devices. In figure 4.1, long term monitoring of the temperature along with the resistance of a packaged device at a sample rate of one reading per second at 0.2V bias was performed. The change in temperature was produced by the passive change in room temperature throughout the time period. 0.2V was selected as the read voltage as a compromise between a reasonable signal to

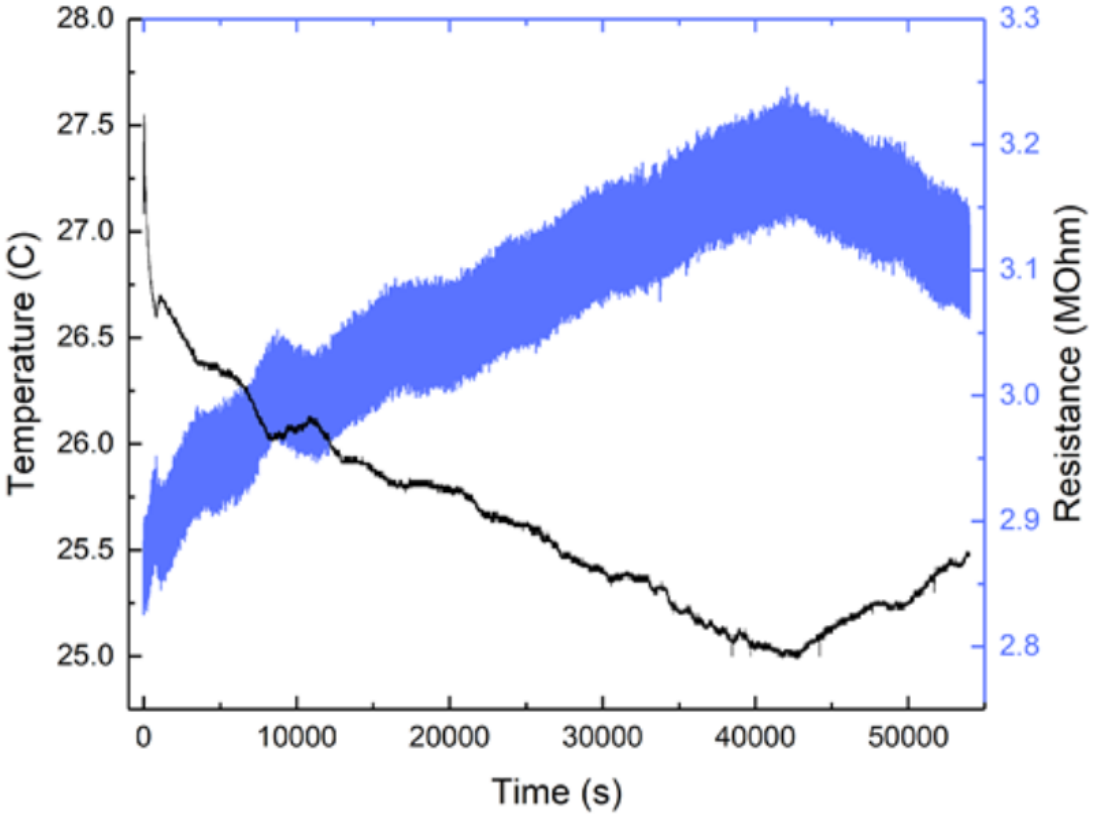

FIGURE 4.1: Results of a retention test with varying room temperature, the pristine device shows a high sensitivity to temperature.

noise ratio for high resistance devices and the risk of the voltage applied causing the device values to drift. This revealed that a temperature decrease of around 1.1°C resulted in an increase in resistance of 175kΩ (±50kΩ), 5.83% (±1.67%).

The primary method used to indicate changes in the behaviour of memristors is a current-voltage (IV) curve, as this allows for features such as asymmetries in set/reset to been more easily observed. [88] These IVs can be categorised as invasive or non-invasive, non-invasive IVs are performed at a voltage below switching voltages, allowing for IV characteristics to be measured without affecting the device resistance, and invasive IVs are at higher voltages, and may be used to observe switching behaviour. An asymmetry is present in these tests due to the use of a platinum top electrode and a gold bottom electrode, this results in two Schottky barriers of different heights, indicating that the transport is controlled by the two asymmetric interfaces. The settings used for figure 4.2 were a max/min voltage of ±2.5V, voltage step of 0.05V, interpulse time of 10ms, step width of 50ms and staircase biasing mode. In order to confirm that the device was stable and non-volatile, three IV curves were taken for each temperature and checked to confirm that there was negligible change in conductivity between each cycle. From these results, a clear, monotonic increase in current can be observed. For these results, the chamber was allowed to come up to the target temperature, then a equilibration period of ten

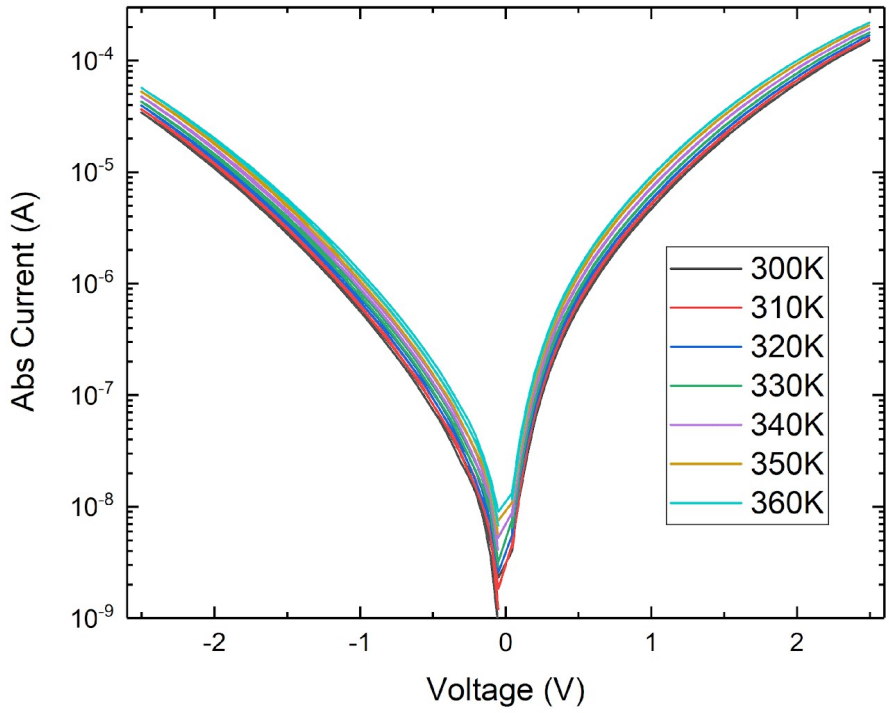

FIGURE 4.2: The IV curves for a pristine device at varying temperatures with a ten minute warm up period for each temperature, later found to be insufficient time for the temperature of the devices to have reached equilibrium.

minutes was given to allow the devices to come up to temperature before performing the IV measurements. Comparing these results to those taken using a wafer probe station with a thermal chuck (the surface of which the wafer is placed and secured via vacuum) as the heating mechanism shows a clearer separation between temperatures for the probe station results, due to the temperature transfer mechanism of the thermal chuck being conductive, versus the convective heating mechanism employed by the micro-chamber, resulting in a much quicker temperature transfer for the probe station. This observation indicated that the devices under test required more than ten minutes to reach the air temperature. The effect of temperature on the IV curve of a formed device has also been investigated. The experimental method for the results in figure 4.3 was mostly identical to those in the previous figure, the only change being the reduction of the max/min voltage being reduced to ± 2.1V to avoid device failure and instability. [88] As predicted by the literature [15], the change in resistance due to temperature is reduced compared to the pristine devices, and the high resistance state is more greatly affected by the temperature increase compared to the low resistance state showing the presence and effects of different conduction mechanisms.

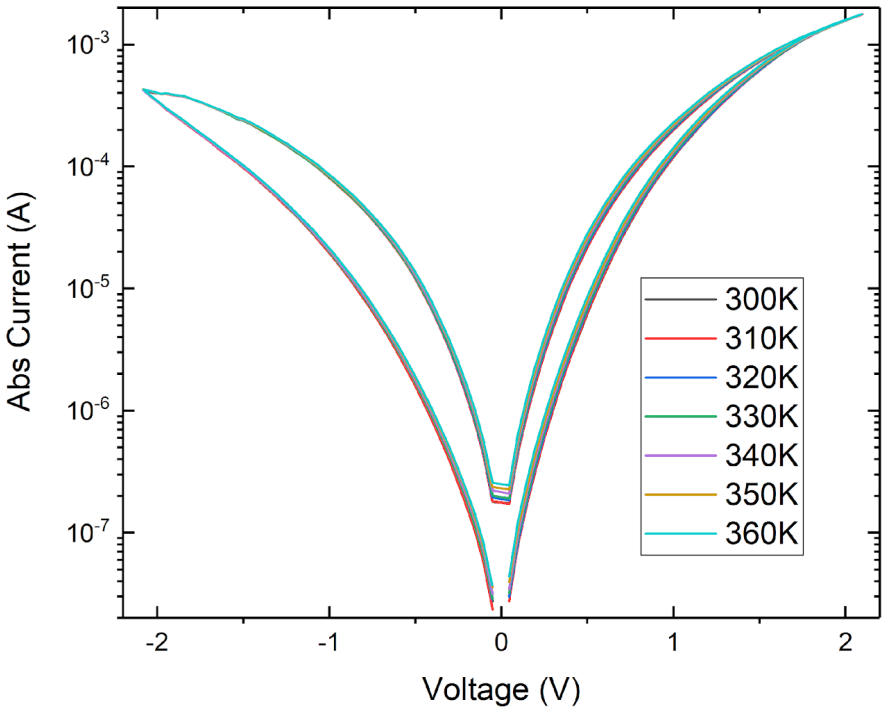

FIGURE 4.3: The IV curves of a formed memristor at various temperatures, showing the reduced impact of temperature on the conductivity and voltage induced switching.

4.3 Use of Memristors as Temperature Sensors

In order to develop the use of memristors as temperature measurement devices, a new and improved methodology was developed due to the sensitivity of the devices to temperature.

4.3.1 Methodology Development

Due to the heating time and the volatility of formed devices, which resulted in multiple IV curves having to be taken for each measurement, a different measurement method was developed. In this case, volatility presents as a drift in the IV curves, due to the resistance of the device drifting in the LRS during measurement. It was decided that retention tests should be performed for measuring device's response to heating due to their non-invasive nature, while also providing information on the transient response of the devices. Heating of the devices is not instantaneous, as indicated by the smaller separation in the IV curves compared to measurements taken on wafer. To establish an appropriate wait time, the system was set to a temperature of 50°C, starting from room temperature and a retention test started on a pristine device. This experiment

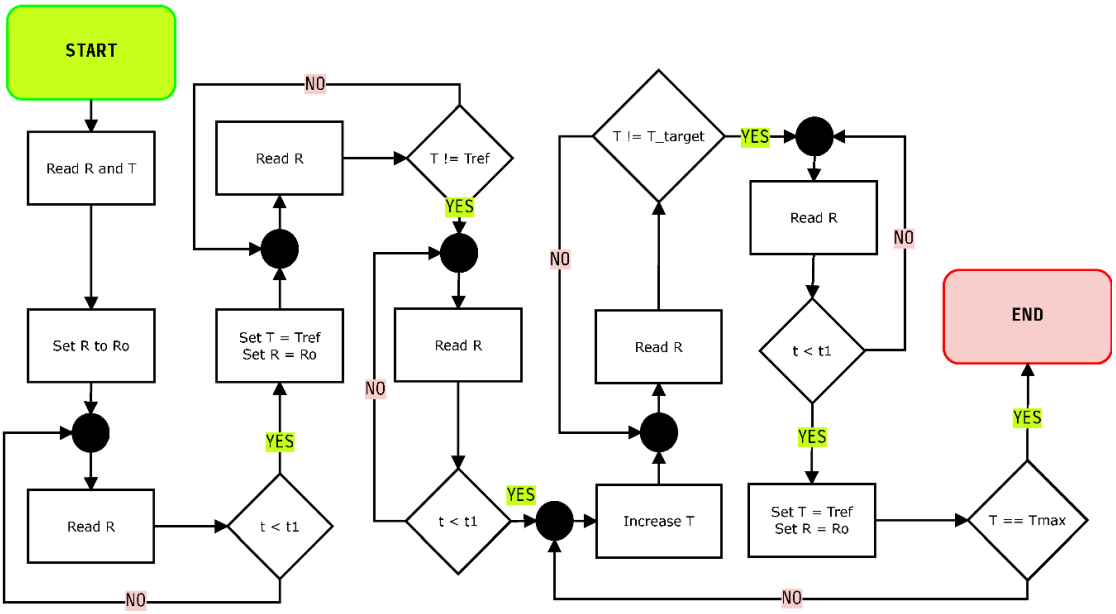

FIGURE 4.4: The block diagram for the developed methodology for temperature characterisation.

showed that the devices took around 45 minutes for the gradient of the temperature increase to decrease to a low level. In order to improve the reliability of these results, the time for the heating period was decided at 1 hour. Firstly, the devices are heated up to 300K and the chamber sealed to ensure a constant concentration of water vapour during the experiment, these conditions are considered the base conditions and used as the reference point for results. Once the chamber had reached the specified temperature of 300K, the devices were left to acclimatise for one hour. In previous methodologies, the temperature was increased, and the devices left for an hour to equilibrate, before the temperature was reduced back to 300K. This method introduced long wait times, limiting the resolution of the temperature steps to 20K. This was subsequently improved by stepping through the temperatures in 10K steps from 300K without cooling between measurements. Comparing results from both methods yields no discrepancy in results. The block diagram for this methodology is shown in figure 4.4.

The way of categorising the devices measured by their resistive level was developed. This was due to observations of the "natural" values the devices tended to form to. These values (the resistivity of the HRS measured at 300K) were categorised as pristine, Level 1 (L1, 1M-500kΩ), Level 2 (L2, 250k-150kΩ), Level 3 (L3, 20k-15kΩ) and Level 4 (L4, 10k-8kΩ). Resistances between these levels had a tendency to be unstable or highly volatile, and would sometimes end up drifting into the range of one of the levels during usage. At least 4 devices in each state were studied, allowing for the exclusion of an outlying result if necessary. In the process of forming these devices, a fairly reliable methodology for forming these types of devices was developed. Previously, forming devices was mainly achieved via ramping the voltage of the pulses applied to the device from around 5V to 12V, which quite frequently had the effect setting the device to a low

resistance and destroying its ability to switch. The developed methodology used only a small change in voltage, but instead focuses on increasing the forming pulse duration. For devices on the outer edge of the package, a train of pulses with lengths of around 100µs are used, increasing exponentially as you move towards the centre of the package, with pulse widths of up to 500ms. To allow for a more controlled formation, this process is repeated in steps, first forming the device to L1, before decreasing the pulse voltages and then lowering the device's resistance to the desired range. This methodology leads to a much greater yield of successfully formed devices.

4.3.2 Resistivity Impact

If the property of a resistance change is to be implemented as a method for temperature measurement, stability and consistency between devices is key to ensure easy implementation and accuracy. Figure 4.5 shows that the high resistance devices have the highest consistency between them, with the results from several devices lying on top of one another and presenting the lowest variability in results. The devices in both the L1 and pristine state are very tightly grouped in their response, indicating that these devices would be also be well suited for temperature sensing applications, with the L1 devices still allowing for the possibility of switching of the resistive state. As the resistivity of the operating region drops further, the devices become less consistent, resulting in them being unsuitable for use as an accurate temperature sensing device. In the varying operating regions, it is best to compare the devices in terms of the proportional change in resistivity rather than absolute. This method of comparison reveals that the operating regime of the device is more critical to its temperature response rather than its absolute value, with devices in the L1 operating region having values within a 25% range, but a near identical proportional resistive response. It can be seen that devices below L1 have a response that is close to linear with L2, or can be approximated to that. These devices would provide a less accurate temperature reading than the pristine/L1 devices, but leads to the possibility of having an incredibly small sensor footprint, avoiding the need for a Wheatstone bridge configuration to provide a linear response. The analysis of the data in figure 4.5 is shown in figure 4.6. The spread of values (error) was calculated by taking the difference between the maximum and minimum values and dividing it by the average resistance ($\frac{R_{max}-R_{min}}{R_{avg}}$) at the end of the experiment before converting to a percentage. This spread was then divided by the percentage reduction and converted into a percentage to get the proportional error. These values show that the proportional spread of results converges for devices with higher resistances, and diverge for low resistances. This is likely due to the combination of conduction mechanisms, with varying weights on their influence.

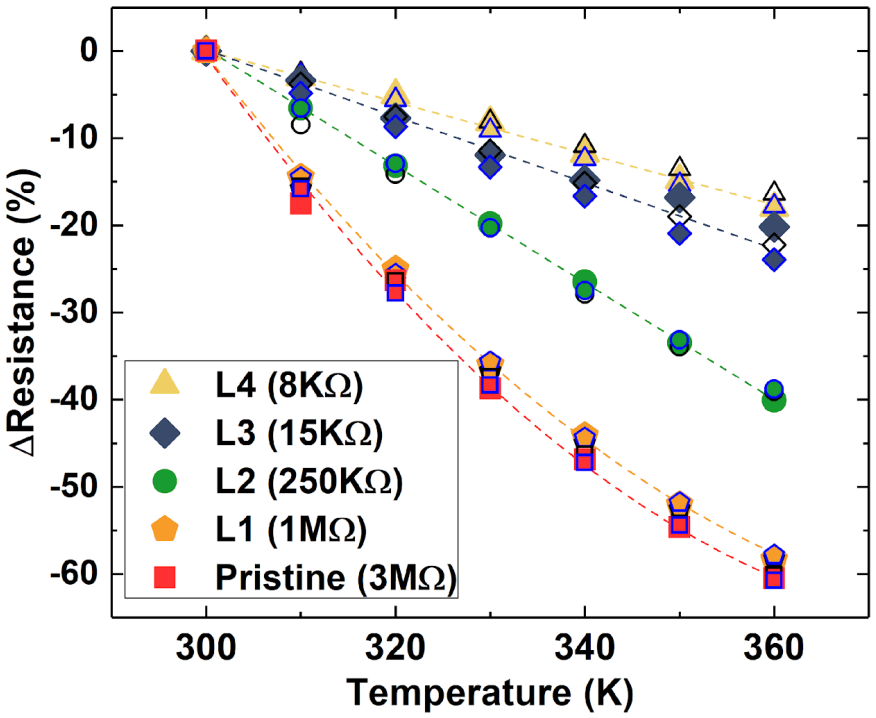

FIGURE 4.5: The proportional resistivity response of devices in the selected operating regions (3 devices in each category), the reference point is the resistance at 300K.

4.3.3 Passive Memristor Thermometer

An experiment demonstrating the use of a pristine memristor as a passive thermometer has been undertaken. For this, a read pulse of 0.2V was applied every two seconds while a stepped temperature profile was applied to the device. This experiment shows a clear separation of resistivities as the temperature changes, and despite the use of an active heating/passive cooling system, the response and settling time for the devices is largely the same, with both directions taking approximately 30 minutes to equilibrate, shown in figure 4.7. In the process of capturing this data, it was discovered that three separate devices had significantly reduced resistivity. Upon further inspection it was seen that this resistance drop occurred on all three devices in the first heating step at separate times, from room temperature to 360K. In the case of figure 4.8, a pristine device starting at around 1.5MΩ dropped its resistance to 400KΩ. Upon later testing, this device had slightly increased its resistance back to 700KΩ, but behaved identically to any high resistance pristine device, showing no switching ability, and the same IV curve asymmetry. The devices do gradually increase their resistivity again as can be seen from the 50kΩ increase in the 300K resistance in figure 4.8, but do not return to their original resistances, revealing potentially a new way of adjusting the resistivity of the devices without forming them. As this effect had not been previously observed in

Temperature																				
	310K			320K			330K			340K			350K			360K				
Operating Region	ΔResistance	Error	Proportional Error	ΔResistance	Error	Proportional Error	ΔResistance	Error	Proportional Error	ΔResistance	Error	Proportional Error	ΔResistance	Error	Proportional Error	ΔResistance	Error	Proportional Error		
Pristine	16.28	1.97	12.1	26.83	1.45	5.4	38.14	1.34	3.51	46.78	1	2.14	54.42	0.41	0.75	60.46	0.65	1.07		
L1	14.91	1.28	8.58	25.65	1.29	5.03	36.11	1.04	2.88	44.49	0.83	1.87	52.1	0.67	1.29	58.12	0.64	1.1		
L2	7.19	1.91	26.56	13.41	1.25	9.32	20.13	0.51	2.53	27.29	1.39	5.09	33.53	0.8	2.39	39.3	1.3	3.31		
L3	3.99	1.48	37.1	7.95	1.15	14.47	12.22	1.88	15.38	15.55	1.8	11.58	18.92	4.12	21.78	22.12	3.78	17.09		
L4	2.8	0.42	15	5.41	0.56	10.35	8.48	1.03	12.15	11.7	1.51	12.91	14.56	1.77	12.16	17.39	1.64	9.43		

FIGURE 4.6: Analysis of the proportional resistance change vs temperature graph, the proportional error is the range of values across the devices compared to the average resistance change. All values are given as percentages.

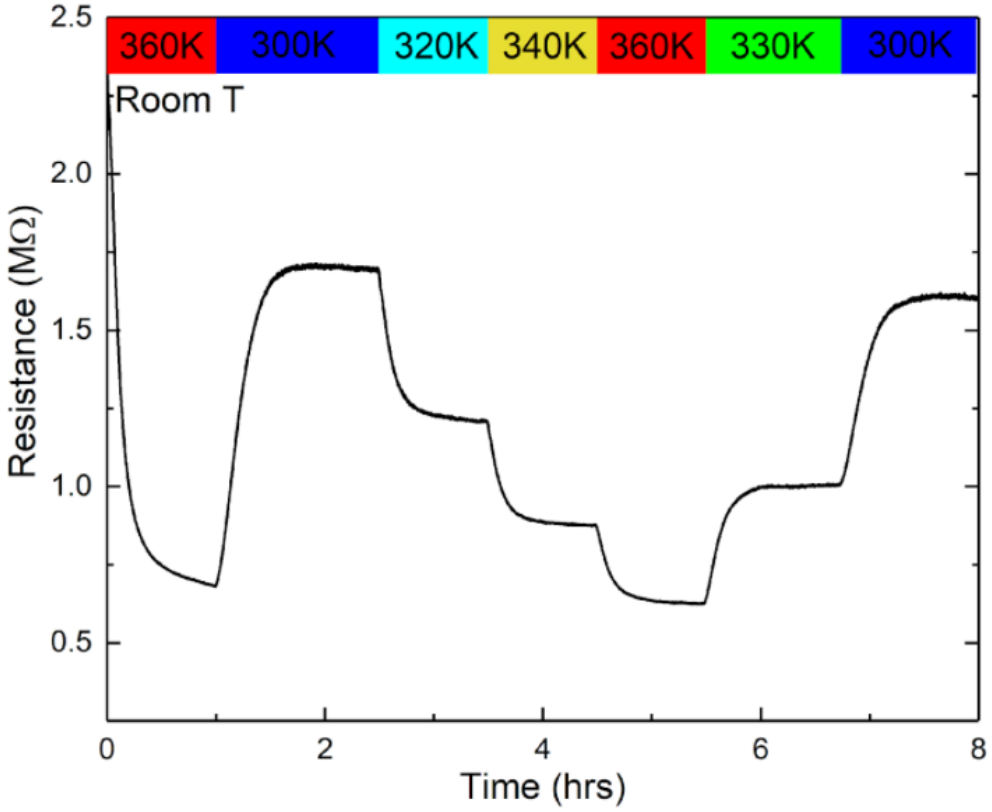

FIGURE 4.7: A pristine memristor used as a thermometer.

experiments where the temperature was stepped more gradually, it is suspected that it may be due to the rate of heating of the device, rather than the temperature. This is supported by the fact that pristine devices in a package have a resistance of around 3.5MΩ to begin with, whereas devices on wafer tend to be around 5MΩ. The process for packaging the devices involves heating them in a 120°C oven in order to cure the epoxy securing the die, providing additional credibility to the hypothesis.

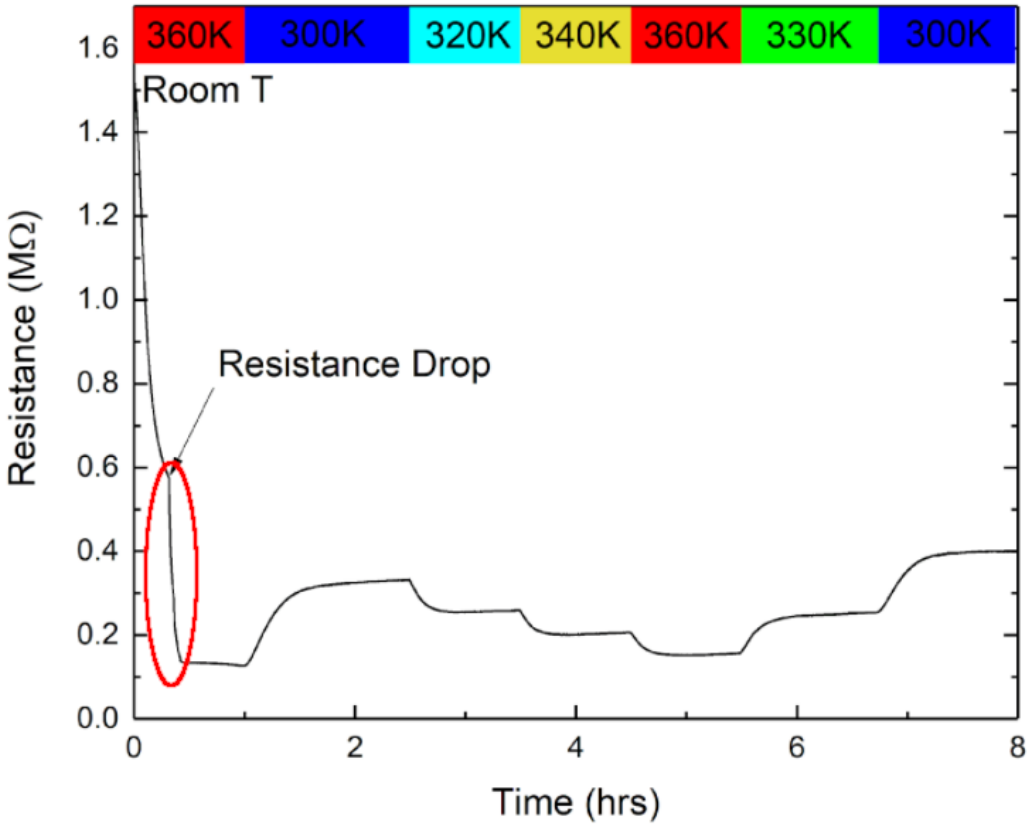

FIGURE 4.8: A pristine device dropping its resistance during heating, note the consistency of the correlation between resistance and temperature post-resistance drop. We currently do not have a conclusive explanation for this behaviour.

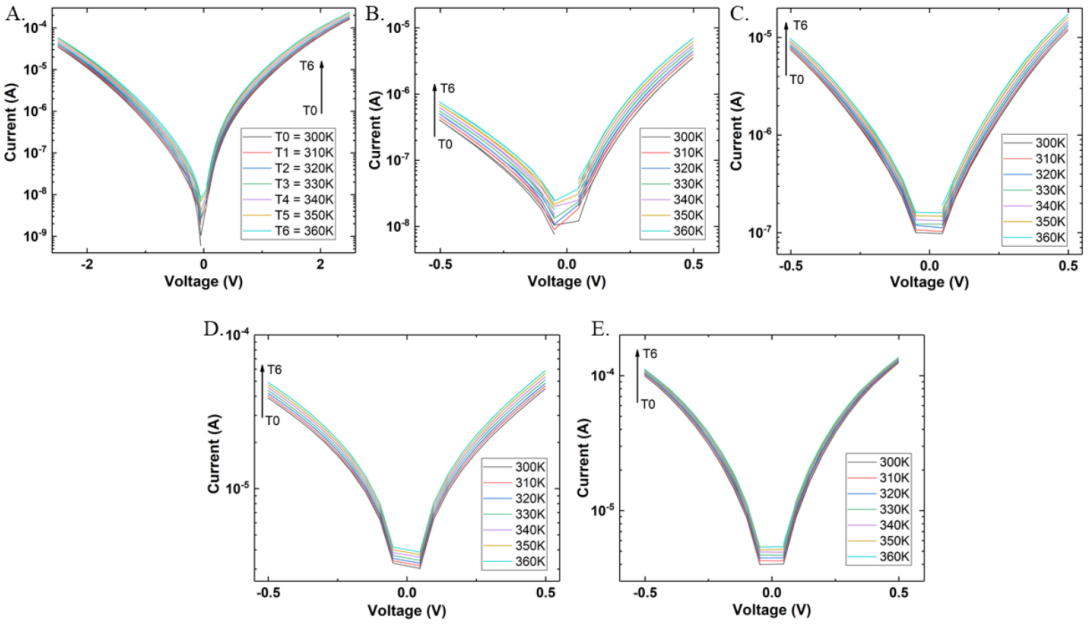

FIGURE 4.9: The symmetry of the IV curve of a device at varying temperature in each operating region (P, L1, L2, L3 and L4). The asymmetry observed in the high resistance devices is due to the dominance of interfacial conduction mechanisms, which are governed by the materials used in the construction of the devices.

4.4 Barrier Modification

In order to analyse the conduction mechanisms present in these devices and the nature of the asymmetry of the devices, low voltage IVs (from ±0.05V to ±0.5V to ensure no switching occurs) were taken of a device in each operating region. From this, the current at each voltage, positive and negative, was taken. From figure 4.9 it can be seen that the devices become more symmetrical as the resistance of the operating region is reduced, while their sensitivity to temperature is also reduced. This indicates the transition from interface controlled transport towards core material controlled as asymmetry will be present in interface transport-dominated devices due to the differing contact materials creating Schottky barriers of different heights due to the differing work functions of the metals. The reducing resistance indicates that the Schottky barriers of the devices are lowered by the forming process. In order to confirm the mechanism, the signature plot for each device is created by manipulating equation 2.1 regarding the conduction to plot linear results in figure 4.10 (see appendix A).

$$I = AT^2 e^{-\frac{\Phi_{B0} - \alpha\sqrt{V}}{kT}} \tag{4.1}$$

becomes:

$$ln(\frac{I}{T^2}) = ln(A)\frac{1000}{k}\phi_{App} \tag{4.2}$$

This results in the gradient of the produced plot to be the value of ϕ_{App}. From this graph, the gradient for each line is taken and plotted against the square root of the

voltage in figure 4.11 to produce a plot with a gradient of α. From this plot, a straight line is extrapolated back to 0v in order to extract the barrier height of the interface without the impact of the barrier lowering coefficient (α). Devices in the Pristine, L1 and L2 regions were analysed using this method, with pristine and L1 devices providing good Schottky conduction signatures, whereas L2 appears to be something of a limiting case, with the plots only providing rough straight lines, corresponding to a low barrier height.

Figure 4.12 shows the effect of the levels of formation on the calculated barrier height of the devices, with increasingly formed devices having a lowered barrier as predicted. Below the L2 operating region, the Schottky effect is no longer the dominant conduction mechanism, with core material controlled transport mechanisms becoming more dominant as electrons at room temperature will have enough energy to overcome the barrier, with an electron at 300K having an energy of around 0.026eV. If the electrons have more thermal energy than the barrier height, the barrier will not prevent conduction. The dominance of core material controlled transport mechanisms in the lower operating regions can be confirmed through the creation of Arrhenius plots in figure 4.13. The straight lines confirm the presence and dominance of core material controlled transport mechanisms in the higher temperature regions.

These calculated barrier heights are lower than predicted by calculations. The electron affinity of TiO_2 is around 4eV [89], and the work functions of Pt and Au being 6.35 and 5.1eV respectively, giving values for ϕ_{b0} of 1.2eV for the TiO/Au interface and 2.45eV for the TiO/Pt interface. Possible reasons for this discrepancy are that the affinity of TiO can vary depending upon the structure of the oxide and oxidation state, and the fact that the use of sputtering to construct these devices will provide a much more intimate contact and gradual transition between the two materials. With these factors combined, we can expect to retrieve a lower than expected barrier height.

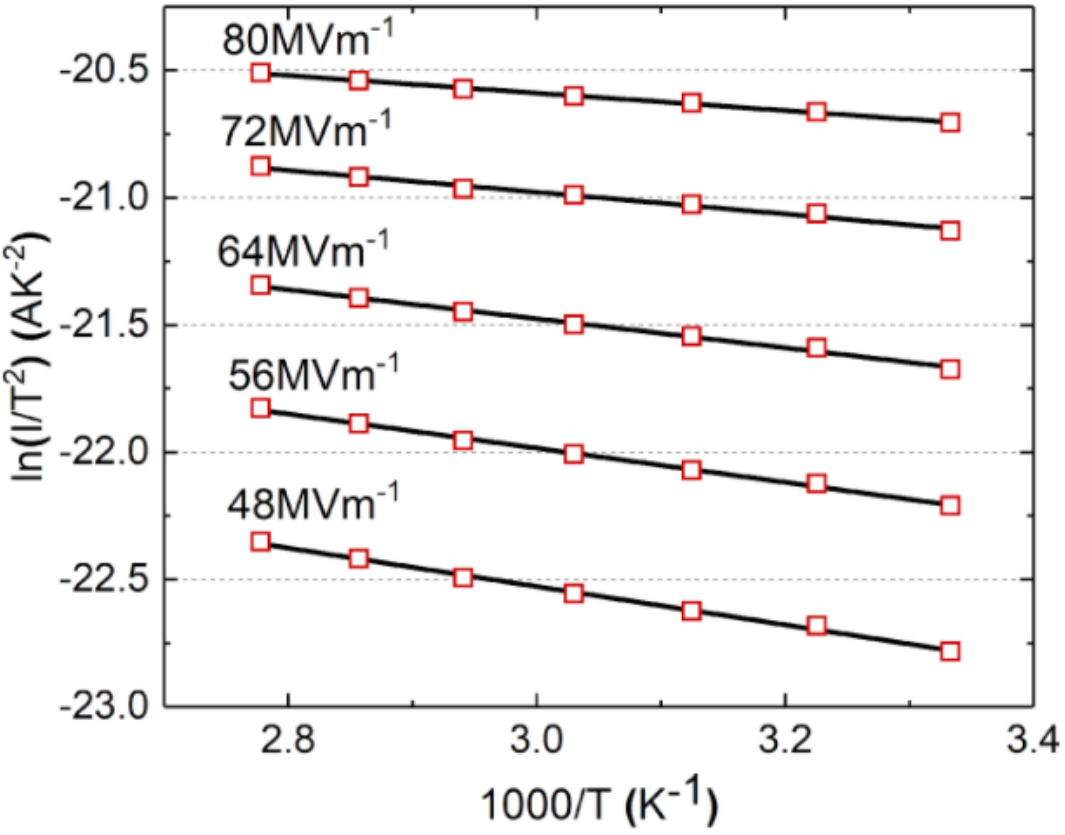

FIGURE 4.10: The Schottky signature plot of a pristine memristor. The dominance of the barrier in this operating region are demonstrated by the straight line relationship. Each line corresponds to a different voltage/electric field strength across the device.

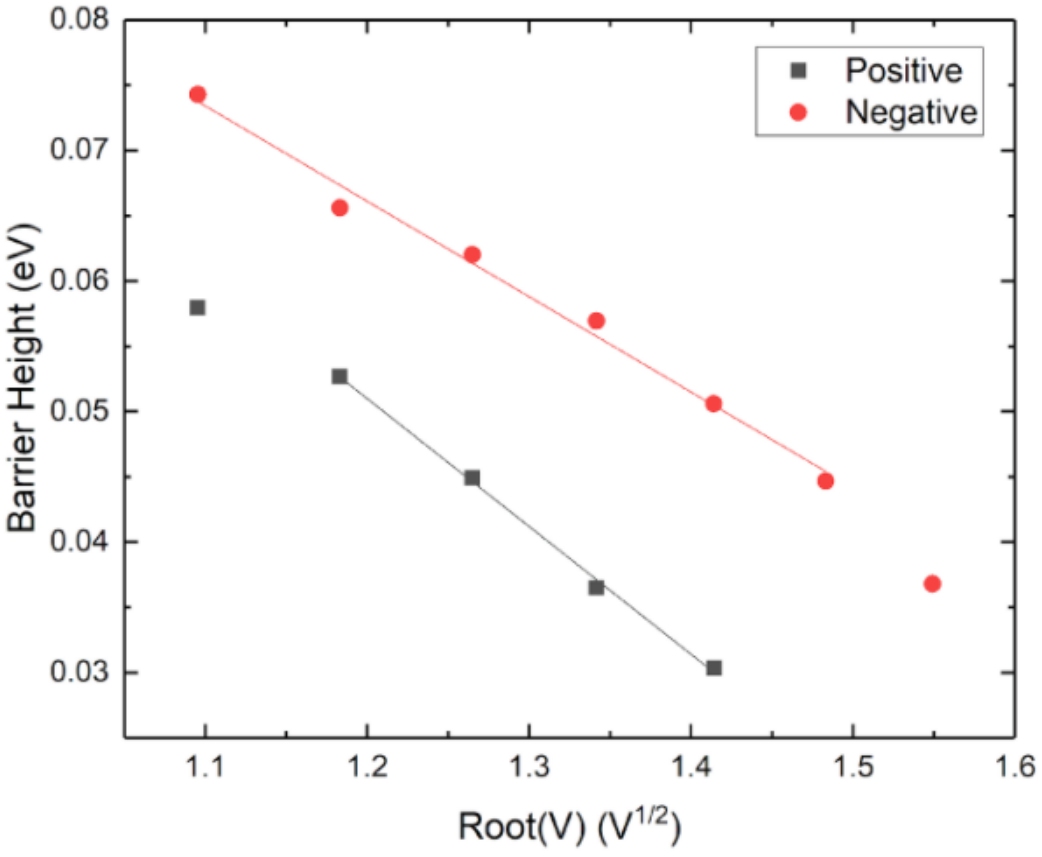

FIGURE 4.11: The gradient of the pristine Schottky signature plot lines, plotted against $\sqrt{V}$ for one device. Voltages are taken from >1V as these reduce the effect of noise on the measurments.

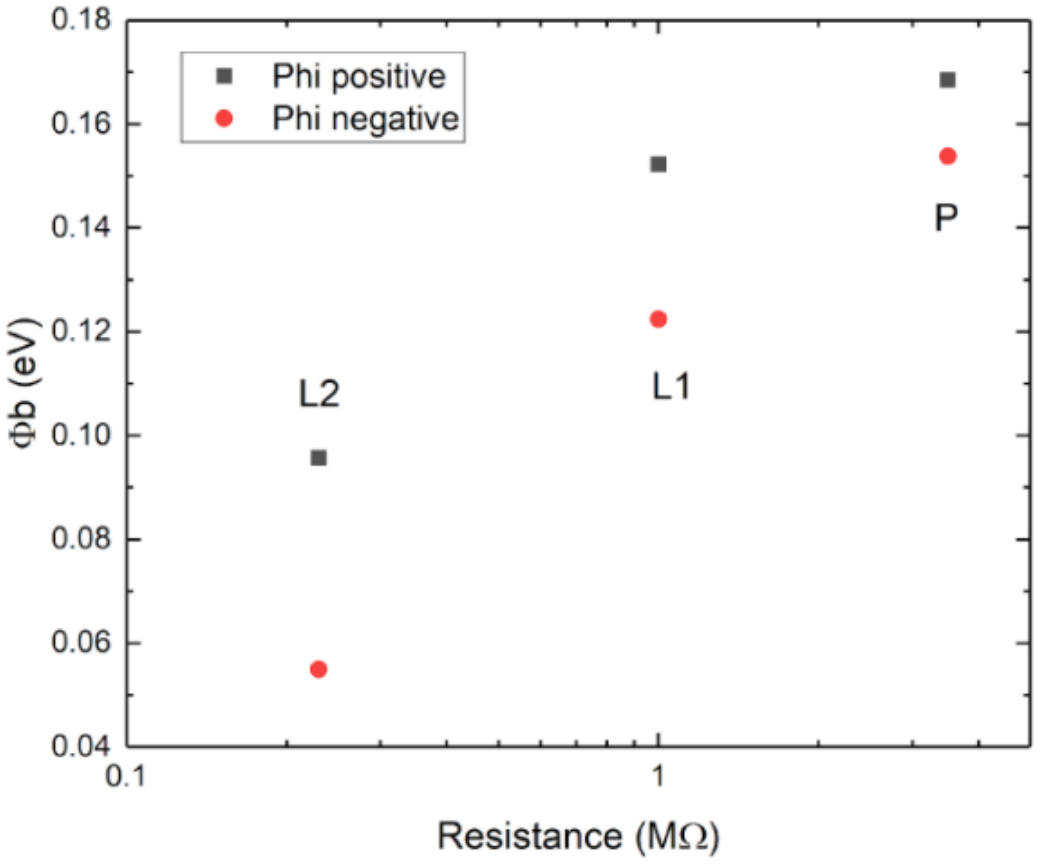

FIGURE 4.12: The calculated Schottky barrier height (ϕ_b) for three devices, one in each operating region, in both polarities, phi positive for voltages >0, and negative for voltages <0.

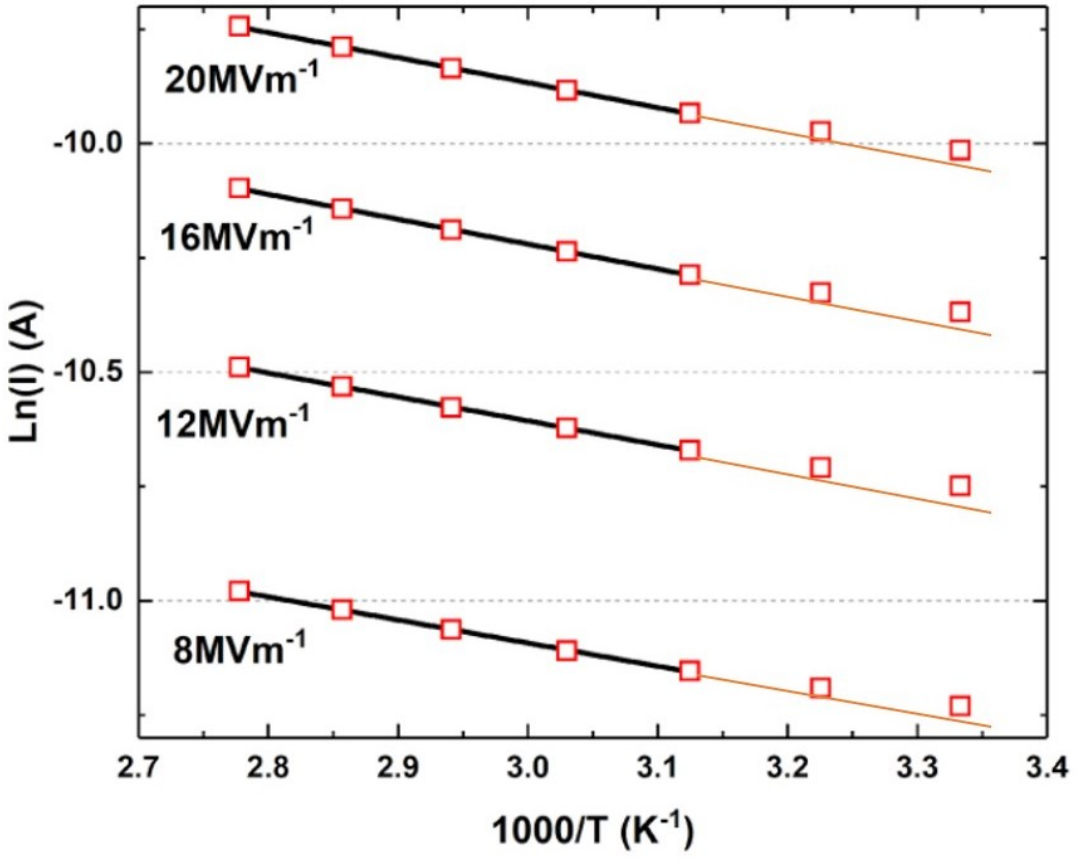

FIGURE 4.13: The Arrhenius plot of an L2 device, showing much lower linearity (extrapolations of the straight lines in orange), indicating the presence of other conduction mechanisms.

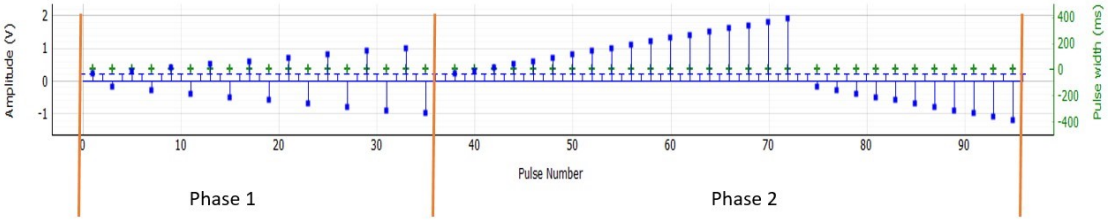

FIGURE 4.14: The pulsing scheme used by the ArC ONE switchseeker algorithm, showing the two measurement phases. Blue dots correspond to the voltage of the pulse, and the green marks indicate the pulse width.

4.5 Thermal Switching

The impact of temperature on the switching behaviour of TiO_2 devices is largely unexplored. Again, a new methodology had to be developed in order to achieve clear results for this method of measurement. Various methods were tested, but invasive IV curves were avoided due to their more aggressive nature which would likely destroy a greater number of devices, while yielding results that would be more difficult to compare at a glance due to the larger range of values that would be present, and the introduction of drift to the memristor's baseline resistance.

4.5.1 Methodology Development

Initially the switchseeker program available on the ArC One was used [90]. This is a two phase process, as shown in figure 4.14. Firstly the system performs a voltage sweep, measuring the change in resistivity as it goes. This sweep stops once a percentage threshold of the change in resistivity has been reached (Phase 1). For example, the voltage applied will increase from 0V upwards until the device's resistivity changes 10% from its initial value, at which point, the polarity of the sweep changes, with the system then sweeping from 0v downwards until the device has again changed by 10% from the initial value. After the sweep stage, the system enters a cumulative stage (Phase 2). At this point, the system applies pulses of increasing voltage until the change in resistivity, plus the change in resistivity from the previous pulses reaches the threshold, before again, swapping polarity. In this case, if the change in resistivity on the first voltage is 1%, the second 3% and the third 6%, then the threshold is reached.

This method was shown to be ill-suited to these devices however, due to their relatively high volatility, resulting in the cumulative switching producing results with a very high level of noise, obscuring possible conclusions. Despite the cumulative switching being largely un-successful, the switchseeker program did provide evidence that the temperature of the devices had an impact on more aggressive switching performance produced by phase 1. In figure 4.15 an increase in the apparent switching threshold of the device

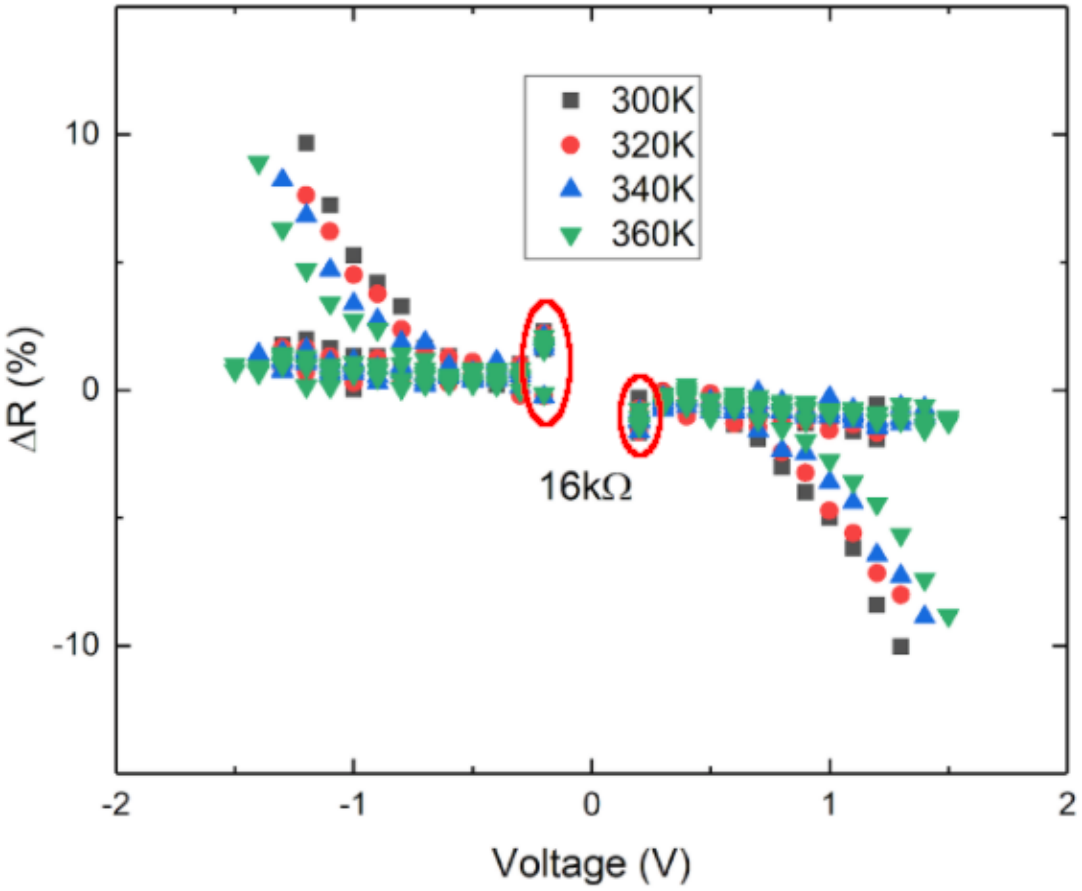

FIGURE 4.15: The result of a switchseeker test on one 16kΩ device with a switching threshold of ±10% and a voltage limit of ±1.5v. These results were produced using a cascade probe station with devices on wafer. The circled areas of the graph display the volatility present in the device, showing changes in resistance at sub-switching voltages.

can be seen above the cumulative switching results. This set of experiments were performed on a set of devices still on wafer using a probe station, as opposed to devices in package. The volatility of the device can be observed at ±0.2v, with a larger change in resistivity being shown despite the voltage being far below the switching threshold of the device.

Due to these un-clear results, it was decided to utilise the parameter fit function on the ArC One for future measurements, figure 4.16. This program applies a train of pulses in both positive and negative voltages, stepping through the voltage range until the limit is reached [88]. The resistivity of the device is measured after the application of each pulse. In order to reduce the stress on the devices the number of pulses was set to 200 and voltages kept below any "hard" switching voltage (over 10% change in resistance), the pulse duration was set to 100µs. For these experiments, the device's resistance was normalised with temperature by converting the results to a percentage change in the device's resistivity seen in figure 4.17. As can be seen from the plot, this method introduced issues with regards to inducing drift in the high resistive state of the

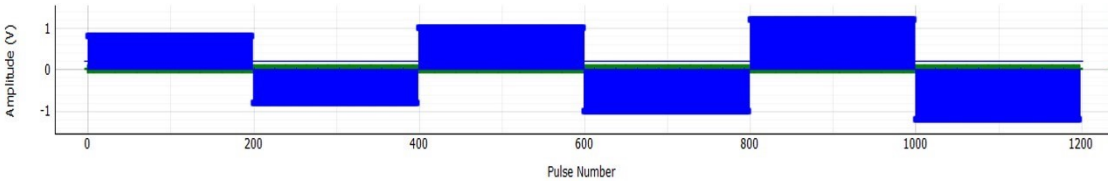

FIGURE 4.16: An example of the alternating voltages applied by the parameter fit algorithm.

device away from 0. Many voltage ranges were investigated, however, the only voltage ranges that did not produce the drift effects also generated changes in resistivity that were much smaller than was deemed measurable due to the noise floor of the system. The particular device in figure 4.17 appeared to show some evidence of a threshold effect, with the temperature having little effect on the switching of the device until the temperature reached 340K, at which point the impact of switching voltages became much stronger, seen in figure 4.18, counter to what was observed when using the switch seeker program. This threshold effect was observed in one other device. It was found that the devices being used in these experiments were fairly volatile, creating a problem with experiments on devices in the low resistive state of each operating region, as the devices over time would drift back to the HRS. Due to this, and the switching dynamics presented by the transition from HRS to LRS being less abrupt, the focus was put on switching from the HRS state (positive voltages). From these conclusions, it was decided that each case of the switching should be isolated. Using the parameter fit program again, the pulsing scheme was set to apply 200 pulses at 100µs length with only one voltage, after the switching pulses were applied, a train of 0.2v read pulses is applied, allowing for the volatility of the device to be observed. Using this methodology, stepping through the voltages was manually attempted, using the converge to state program to reset the device's resistivity between each application of the switching pulses. This however, did not reduce the drift observed in the devices' HRS, and again, after trying a large number of different voltages, this approach was abandoned in favour of a simpler methodology.The methodology settled on was similar to the previous, however, only applying one switching voltage for each temperature and device. To allow for easier comparison, this voltage was kept constant across all devices at 1.5v, maintaining the pulse length and number, with the retention applied after switching again. After the switching pulses, the converge to state program was again used to reset the device to its initial resistive level. This combined with the hour allowed for the device to equilibrate with the temperature of the air inside the micro-chamber removed the drift that was previously observed in other methodologies.

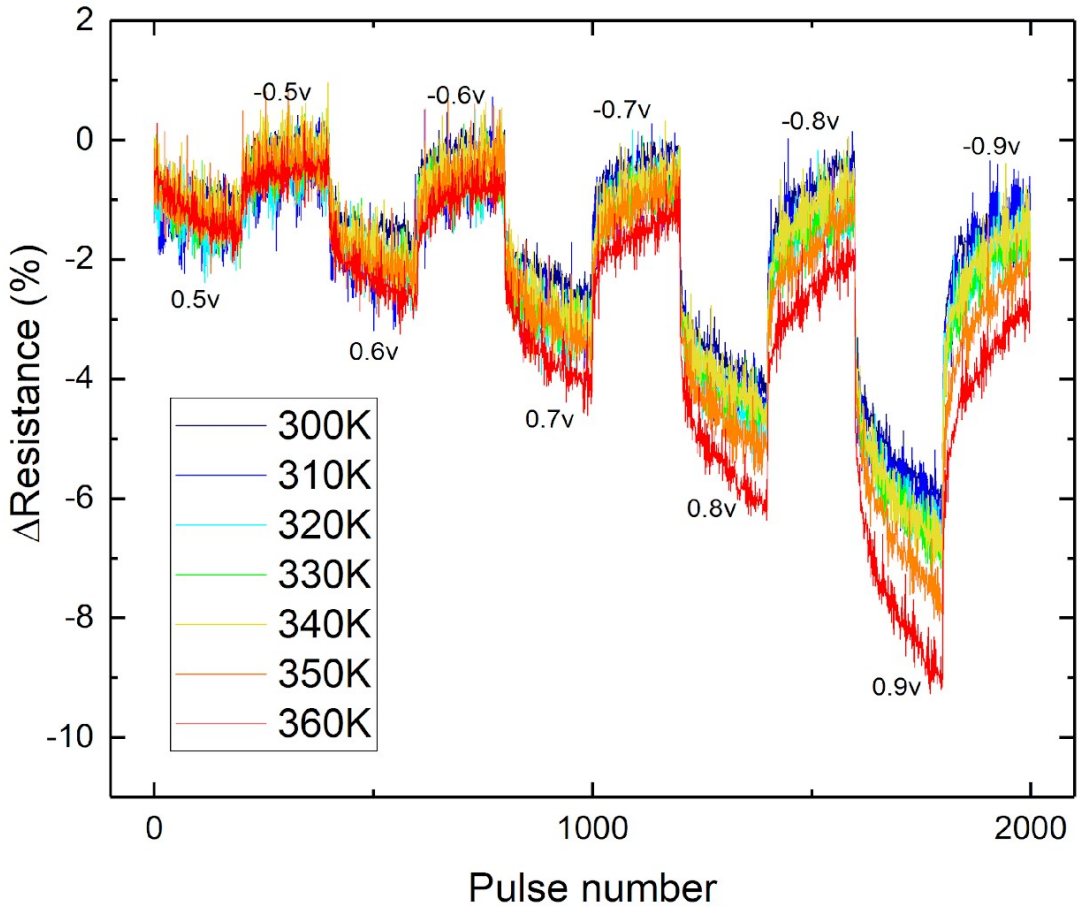

FIGURE 4.17: The results obtained by applying the parameter fit program to a 150kΩ device. Each voltage is applied for 200 pulses at 100μs per pulse.

4.5.2 Results

Four sets of four devices were utilised for these results, four devices at each resistive level (L1, L2, L3 and L4). Devices in the L1 operating region were found to have a strong and repeatable temperature dependency on switching behaviour shown in figure 4.19, with increasing temperature decreasing the magnitude and rate of switching, with a saturating effect. Of the four devices formed to this region, three exhibited this behaviour, showing that this phenomenon is reproducible. The noise floor for these results is relatively large due to their high resistivity, as can be seen by the reduction of the noise floor at higher temperatures as the device's resistivity falls, increasing the measured current. Devices in the other operating regions however, did not show any consistent temperature dependencies, with individual devices showing some evidence of temperature affecting their behaviour, but other devices in the same region not displaying the same effects. This switching behaviour can be explained by the manipulation of 2.1. When differentiated with respect to dR/dϕ and with some manipulation, this

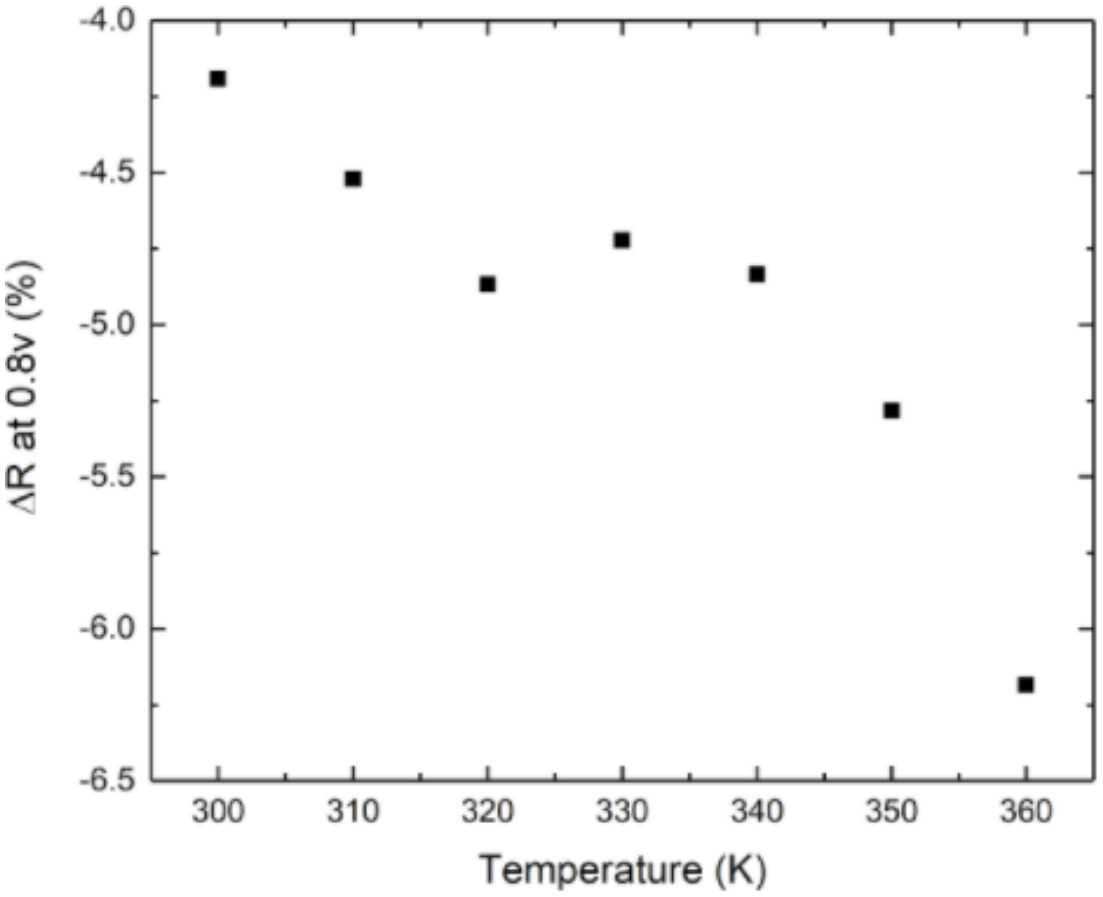

FIGURE 4.18: The change in resistance produced by 200 0.8v pulses on the above device. There appears to be a temperature dependent threshold at around 340K, after which the change in resistivity increases rapidly.

equation becomes 4.3 (see Appendix A).

$$dR = A^{**}T^{-3}e^{-\frac{\phi_{App}}{e^{kT}}}d\phi_{App} \tag{4.3}$$

Where dR is the change in resistance, A** is a constant of 1/the Richardson constant divided by the boltzmann constant , T is temperature and k is the Boltzmann constant. From this equation it can be seen that for a constant change in ϕ_{App}, the magnitude of dR will decrease with increasing T. This also demonstrates that changes in dR are not a result of the "passive" resistance decrease due increases in temperature, presented previously. This theory is supported when a graph of ln(dR T^3) vs 1000/T is plotted in figure 4.20, showing a linear relationship up to 340K. The axes of this graph were derived from equation 4.3, in order to provide a straight line should it be accurate to real-world data. The straight line for temperatures up to 340K indicates that this is accurate for lower temperatures. At higher temperatures it appears that other conduction mechanisms may come into prominence, or that temperature affects the LRS/HRS differently, showing that the value of dR will saturate towards 0, while the resistance of the device's HRS continues to decrease. In order to achieve a better understanding of the impact

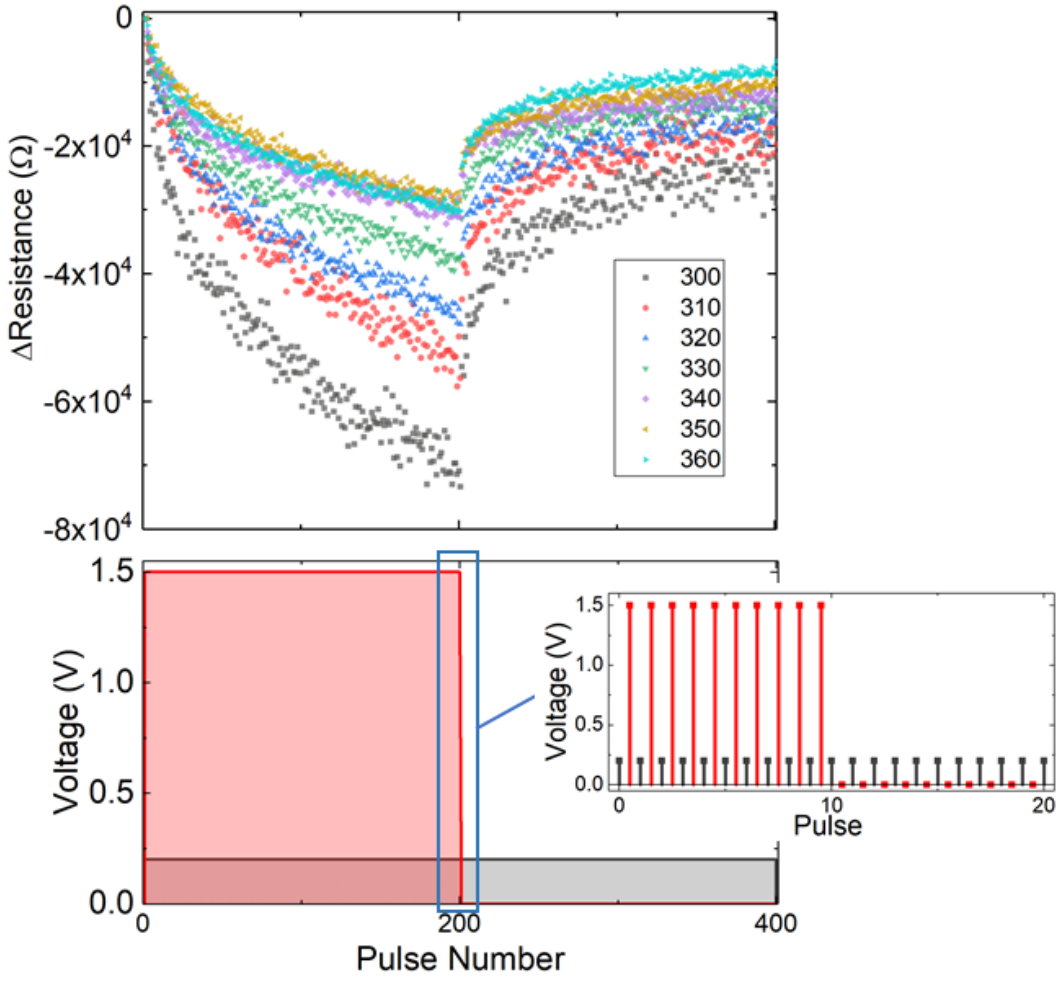

FIGURE 4.19: The response of a 1MΩ device to the same stimulus with varying temperature, showing the inhibiting effect that temperature has on the magnitude and speed of switching for these devices. This change in magnitude does not correlate with the drop in resistance due to temperature, shown by the results at 340-360K being very similar.

of temperature on switching, a "TV" graph was generated from a separate L1 device that also exhibited this temperature dependency. This generated graph, shown in figure 4.21, illustrates the relationship between the voltage of the stimulus, the temperature of the device and the change in resistance that results from the combination of these factors. This graph also demonstrates the fact that a threshold voltage needs to be reached before the device begins to switch, proving that the read voltages are not high enough to affect results. It is also possible to observe a small increase in the threshold voltage of the device. If this threshold is treated as the voltage at which the resistivity of the device is altered by 2%, then the contour line for a change of 25KΩ demonstrates an increase in the threshold voltage from around 0.98V to 1.12V, approximately a 15% increase.

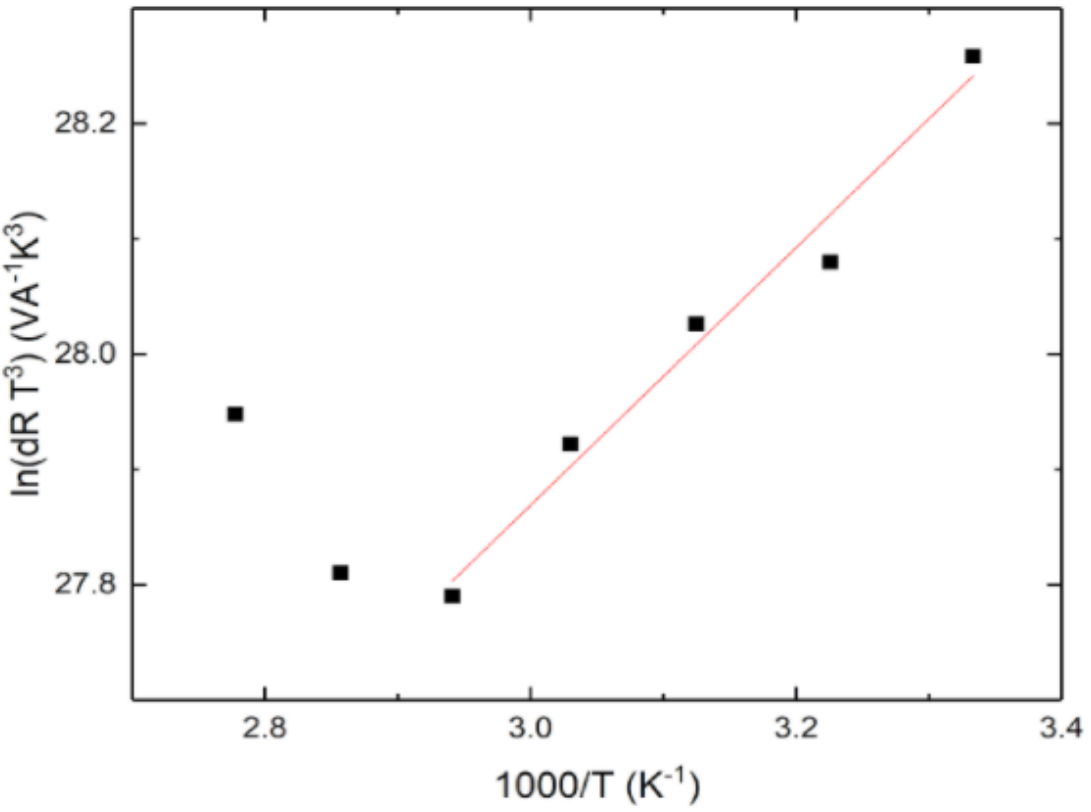

FIGURE 4.20: A graph comparing change in resistance (taken from an average of the last 20 data points for the 1.5v stimulus) with temperature. The straight line with positive gradient shown up to 340K supports the derived equation 4.3

4.6 Thermal Volatility

Understanding the transient characteristics of a memristor's switching behaviour is vital when implementing these devices into a complete system. Volatile characteristics influence parameters such as expected memory lifetime, likelihood of a read error and provide information on the thresholds required for non-volatile memory storage, for example, if the device has a volatile drift back to equilibrium of X%, it may need to be displaced to the desired resistance plus X% further to compensate if long term data storage is desired. This also indicates that there may be issues with memory becoming available only after some settling delay when it is within tolerance, unless we can account for this volatility. It is additionally of import to investigate how these parameters may be affected by the presence of changing temperatures, as this may affect the performance of the devices if the system they are in is still warming to thermal equilibrium or under high strain.

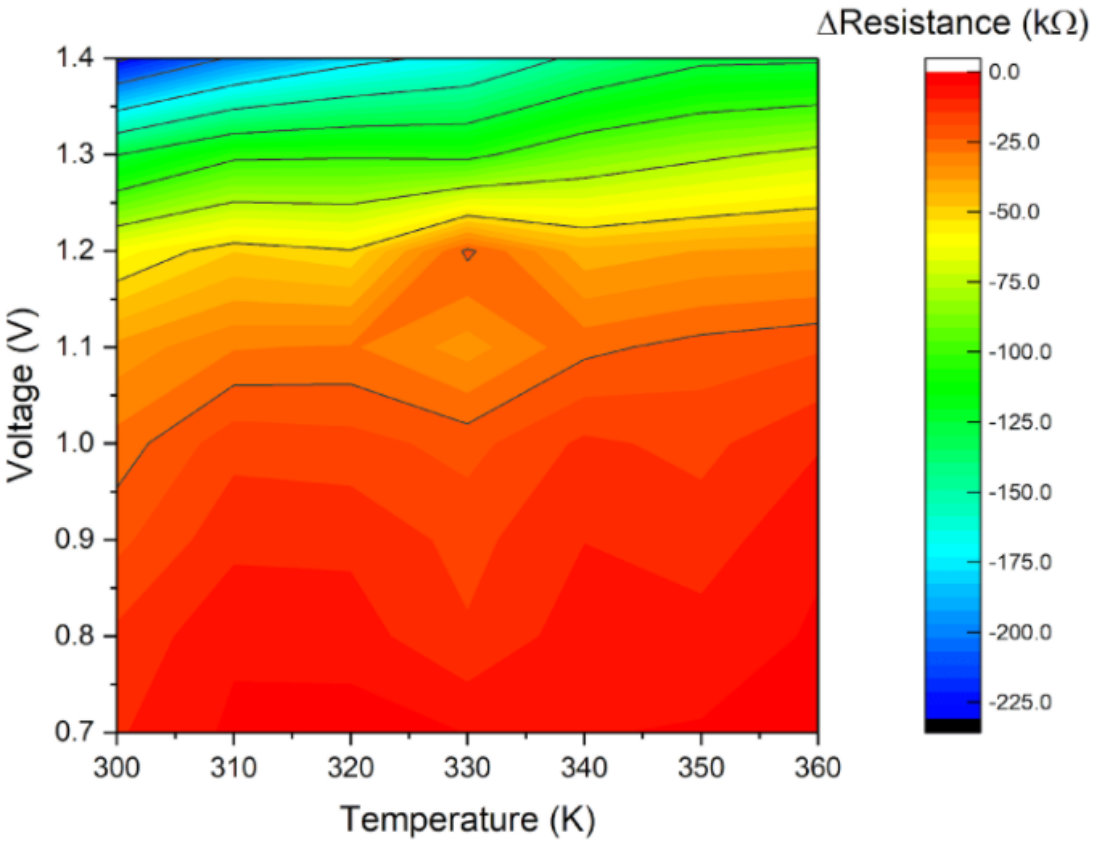

FIGURE 4.21: The voltage-temperature-displacement graph for an L1 device with an applied stimulus of 200 100µs pulses ranging from 0.7V to 1.4V at temperatures from 300K to 360K.

4.6.1 Methodology Development

Initially, the second half of the data generated in the switching investigation, figure 4.19 was analysed for temperature relationships. For this, a series of 200 1.5v pulses were applied to a device in the L1 operating region, after this, the device's recovery was measured for a period of 8 seconds, from the end of stimulation pulsing. This section of data was analysed for trends in behaviour, treating the resistance value after the final pulse as the reference resistance for recovery, figure 4.22.

From these results it was found that this methodology would only likely work for higher resistance devices, as lower resistance devices exhibited significantly non-monotonic volatile behaviour, where changes in behaviour result in the crossing of data traces, showing an inconsistent change in behaviour, making any modelling inaccurate. In order to compensate for the tendencies of formed devices to be non-monotonic, likely due to the presence of non-volatile switching behaviours, the focus of this experiment was moved to pristine and L1 devices as, unless forming occurs within the device, any changes in resistance are volatile, and if the device does form at all, the results are very easy to identify and discount. The length of the volatile recovery period was also increased

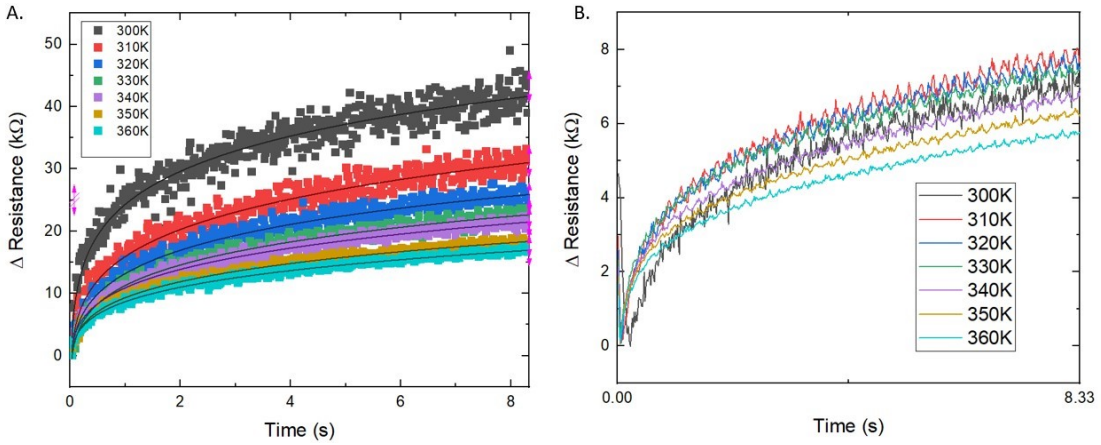

FIGURE 4.22: A. The volatile recovery of a device after pulsing, B. The volatile recovery of a lower resistance device, displaying non-monotonic recovery effects, where recovery behaviours at different temperatures result in crossing traces.

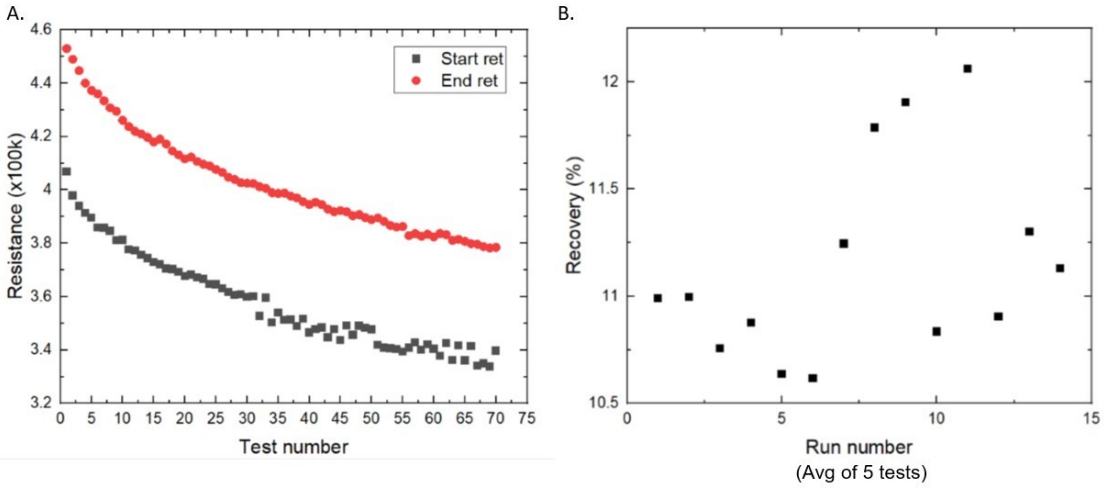

FIGURE 4.23: A. The effects of repeatedly stimulating (Start ret) and allowing a device to recover (End ret). Despite the residual reduction in resistance, the magnitude of the recovery remains constant, B. The average proportional recovery of the device. Each point is an average of a group of five recoveries. The residual change in resistance was not incorporated into this model due to the focus on proportional change in resistance, and is a complex feature that is yet to be fully investigated.

from around 8 seconds to 3 minutes, in order to expand the window of study from the transient towards the steady-state.

To ensure the validity of repeated results, the effect of running multiple stimulation-measurement cycles was analysed, figure 4.23. This revealed that although the resistance of the device would decrease, the magnitude of its recovery would be unaffected. This is supported by figure 4.23 B, where the proportional recovery of the device resistance can be seen to remain fairly constant, with a value of 11.1± 0.9%.

It was observed during the course of these measurements that the very first stimulation-recovery loop did produce recovery values of a significantly higher level, seen in figure

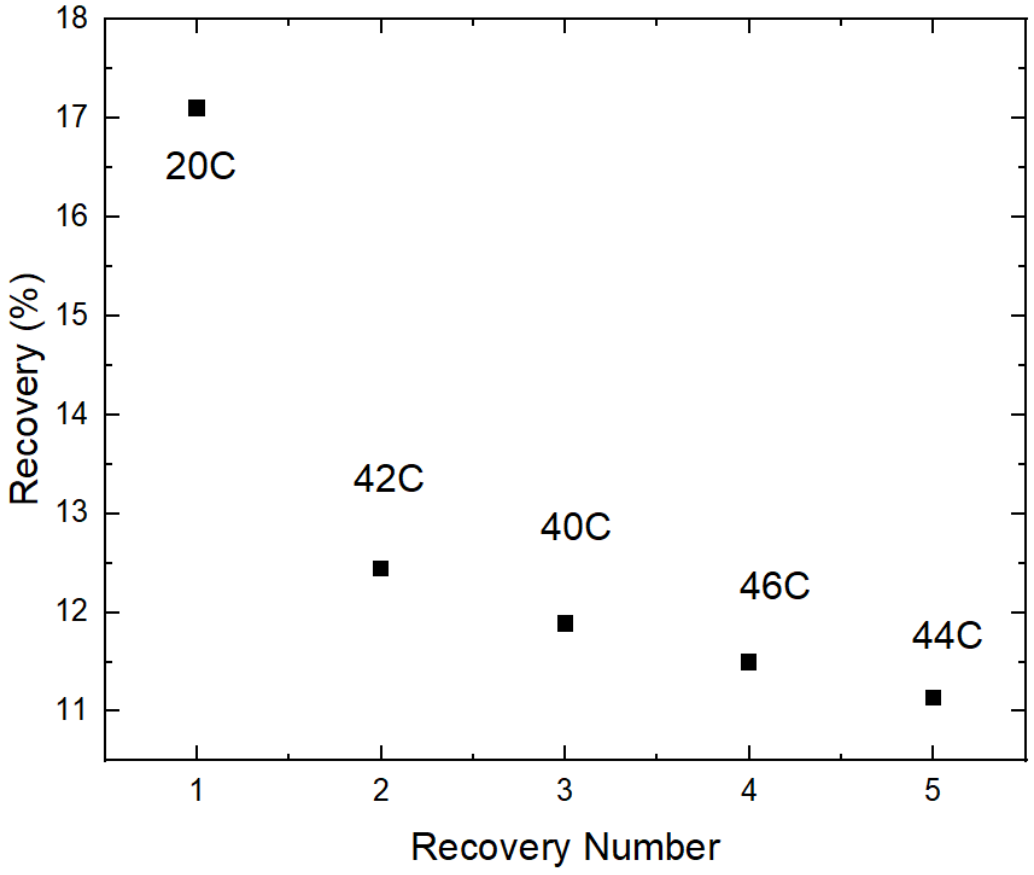

FIGURE 4.24: The proportional recovery of a pristine device with a stimulation voltage of 10v, during the first five stimulation-recovery cycles at five different temperatures, showing that the impact of the measurement order is higher than temperature at this resolution.

4.24. This indicated that there was an element of order-dependence on the results, which was more significant than the impact of temperature on proportional recovery at a resolution of 2°C. The large initial difference was compensated for by running a stimulation cycle prior to recording any results from the device under study. This also reinforced the need for each measurement to be averaged and repeated in a randomised order, to account for this effect.

4.6.1.1 Recovery

The impact of voltage on displacement and recovery was investigated to ascertain any unexpected impact that the stimulation voltage may have on the device's recovery behaviour. This revealed that with the extended recovery period of three minutes, a pristine device would more or less return to its original resistance independent of voltage stimulus, shown in figure 4.25. These measurements were recorded in a randomised order, with each measurement being repeated five times in order to eliminate the displacement behaviour observed in figure 4.24. This behaviour indicates that the volatile

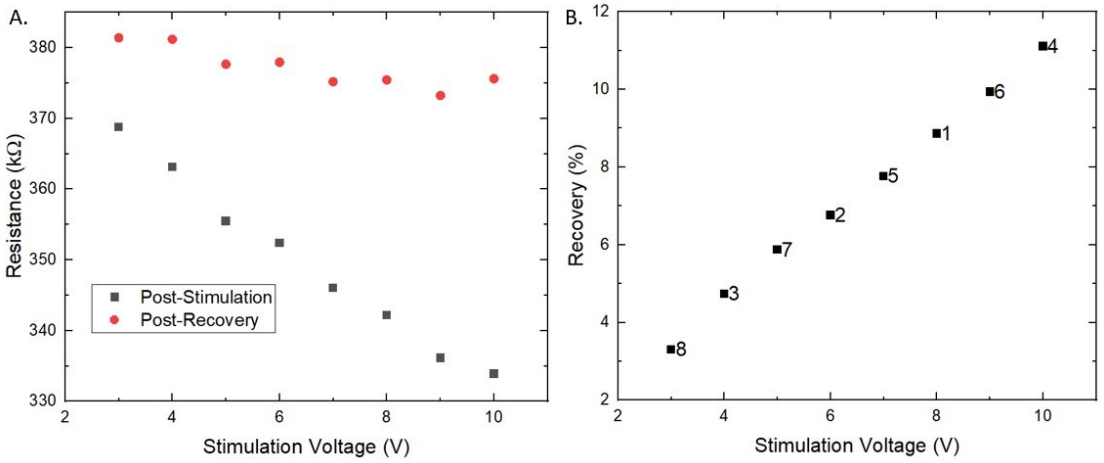

FIGURE 4.25: A. The initial displacement and final recovered resistances of a pristine device with varying stimulation amplitude, B. The proportional recovery of the device. The numbers adjacent to the data points correspond to the order of measurements.

switching characteristics exhibit a "rubber banding" effect, where more significant displacements will result in a more rapid return to R0. This also demonstrates the lack of non-volatile switching effects in pristine devices, making them unsuitable for applications as long term memory devices. From this data, it was indicated that high stimulation voltages would be useful for investigating the effects of temperature on volatile behaviour, providing a maximum signal to noise ratio without the results being incomparable to those of lower voltage stimulation/displacements. The results in figure 4.26 were achieved by pulsing each device 500 times with 10v 100μs pulses in order to displace the device from it's equilibrium state. The recovery was measured via the change in resistance from after the last stimulation pulse over the course of a three minute time period. These results show a clear decrease in the magnitude of the device's recovery with increasing temperature, and this is common across the three devices tested, providing a linear trend. The recovery curves of the devices show that it is primarily the magnitude of the recoveries being affected by temperature, with all three temperatures having very similar curves with an offset, indicating that the effect of temperature on this volatile behaviour is primarily in magnitude, rather than changing a rate of recovery.

This methodology of measuring the effects of temperature on volatile recovery was subsequently replaced with one developed in parallel by Christos Giotis [78] .

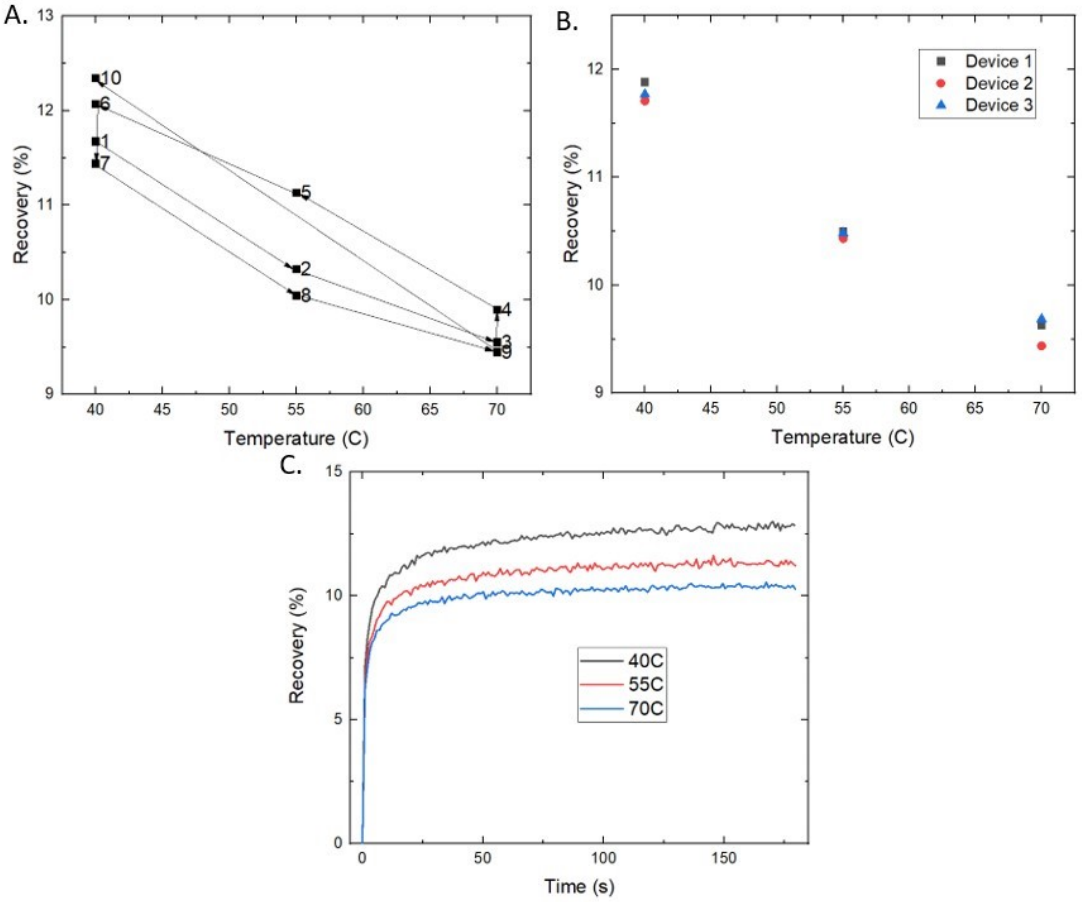

FIGURE 4.26: A. The effect of temperature on the recovery of a device over several cycles (order numbered), B. The averaged effect of temperature on proportional recovery on three separate devices over three trials , C. The recovery curves of a device at three temperatures.

Chapter 5

Modelling

5.1 Thermal Behavioural Modelling

5.1.1 Static IV Model

5.1.1.1 Methodology

For this work, the methodology for fitting the data had been developed by Ioannis Messaris, another member of the research group, and was achieved by applying a pulsed IV sweep from 0.05V to 0.5V and from -0.05V to -0.5V in 0.05V steps for formed devices. The final voltage for pristine devices was increased to ±2.5V.

5.1.1.2 Initial Parameters

Firstly, the IV curve for the positive voltages of each device at 300K is separated and fitted with a line of the form of eq. 5.1, with all parameters free. This fitting was selected due to previous experience from other team members generating similar behavioural models and is shown in figure 5.1.

$$I = Ae^{BV^C} \tag{5.1}$$

From the values produced by this fitting, the value of C is fixed to the initial calculated value, in this case to 0.4. The equation with this fixed value is then applied across the temperature range in figure 5.2 to acquire the temperature dependencies of A and B in figure 5.3.

This best fitting for the temperature dependency of A was found to be of the form 5.2 and for B a simple linear fit, leading to the current model of 5.3.

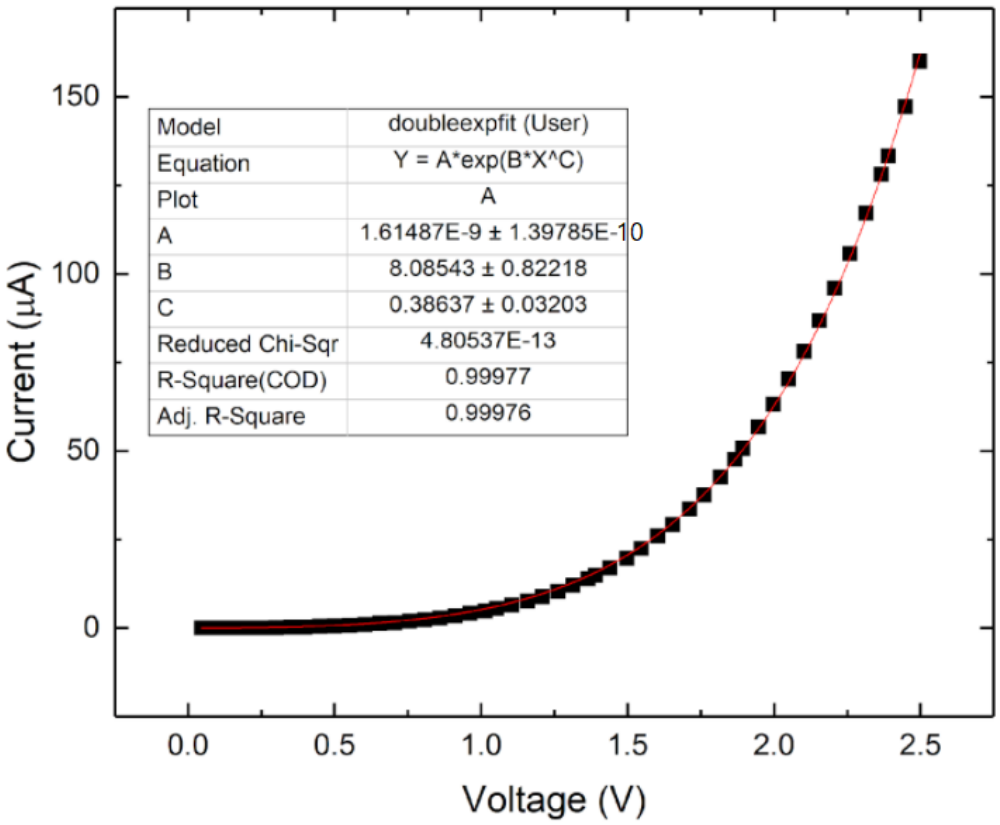

FIGURE 5.1: Free-fitting a device IV.

$$A = ae^{T^b} + c \tag{5.2}$$

$$I = (ae^{T^b} + c)e^{(fT+g)V^{C(R)}} \tag{5.3}$$

This process was repeated for the negative halves of the IV curve on each device, and across a total of 19 devices across the various operating regions before collating the parameters generated from the fittings of A and B. This is done to establish if A, B or C have resistance dependencies, allowing for the creation of a model that applies across multiple operating regions. Due to its more simple relationship with temperature, the relationship between B and resistance was investigated first in figure 5.4. These graphs reveal that the relationship between the variables in B and the operating level of the device is widely spread, but unrelated, leading to averaged constants for these being 0.01289 for f and 14.23 for g. The variables for A were then plotted against resistance of the device. The values calculated for the +c term of the fitting were found to have very low values compared to the magnitude of the values generated by the ae^{T^b} term, and pivoted either side of 0. Due to this, the d term was removed from the model, and the values of a and b re-fitted in figure 5.5.

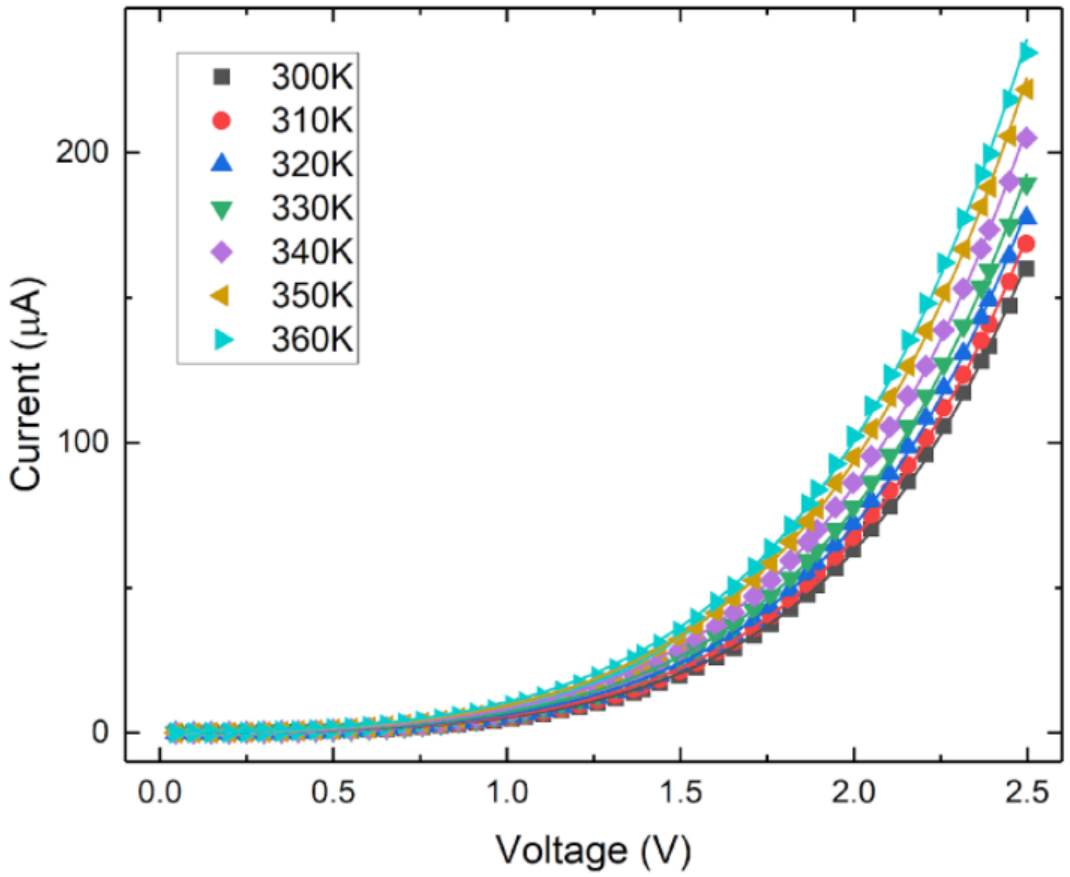

FIGURE 5.2: Free fitting a device IV at varying temperatures.

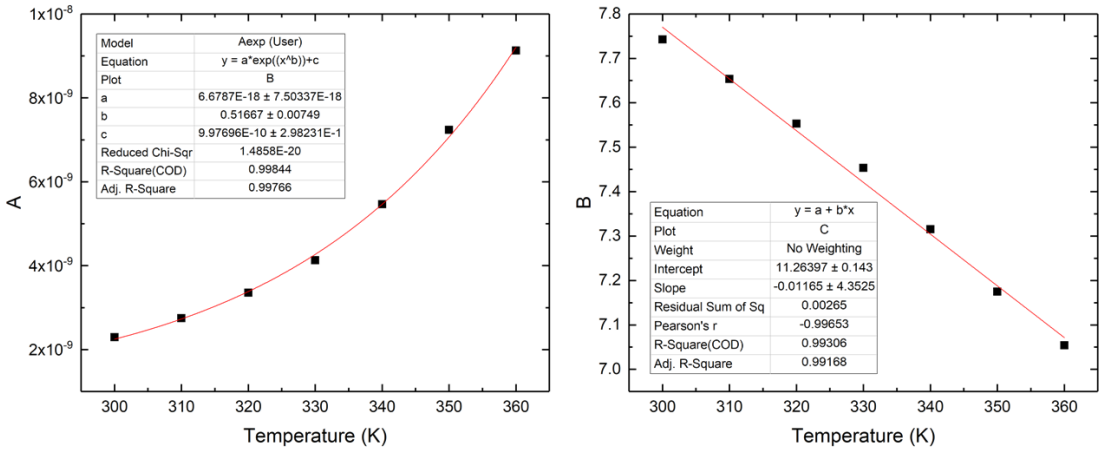

FIGURE 5.3: Extracted temperature relationships for variables A and B with fixed C.

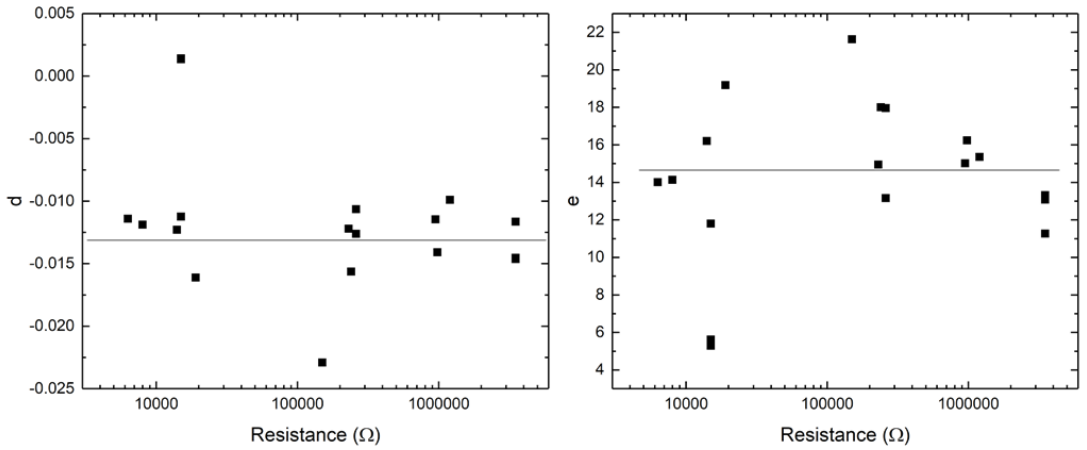

FIGURE 5.4: Resistance dependencies for the internal terms of B.

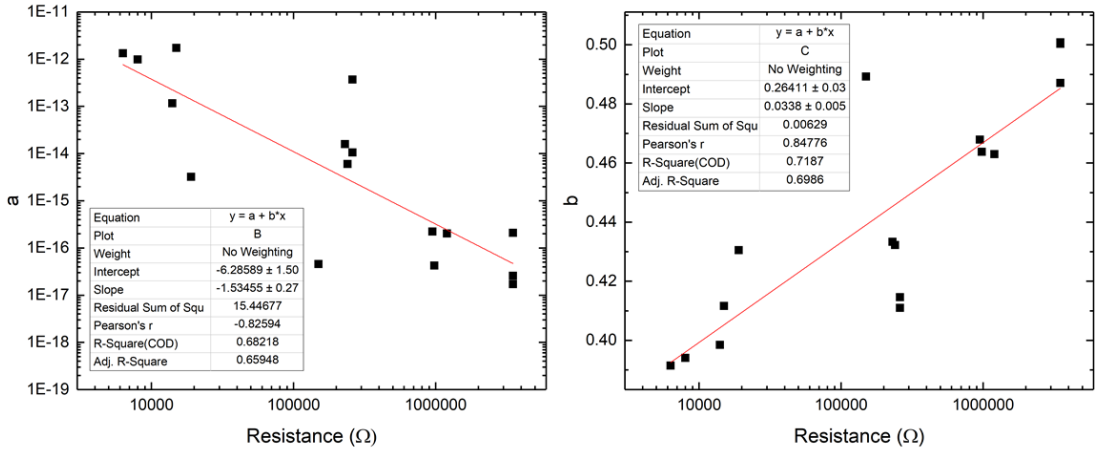

FIGURE 5.5: Resistance dependencies of the internal terms a and b for A.

Both variables of A were found to be affected by the resistance of the device logarithmically, and generated graphs that could best be approximated to a straight line. This leads to the extraction of the relationships 5.4 and 5.5.

$$log(a) = R - 6.286 \tag{5.4}$$

$$b = 0.0338 \cdot log(R) + 0.264 \tag{5.5}$$

This leaves the current model with only one variable left, C, and the model at 5.6.

$$I = (10^{-1.53 \cdot log(R) - 6.29} e^{T^{0.034 \cdot log(R) + 0.26}}) e^{(-0.013T + 14.23)V^C} \tag{5.6}$$

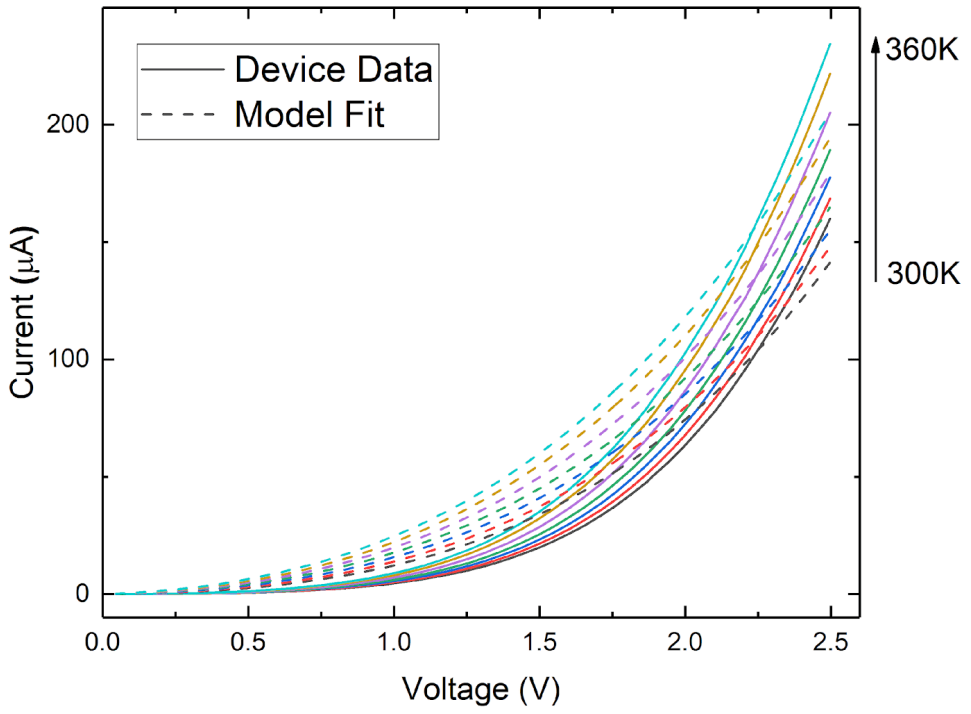

FIGURE 5.6: The fitting of the model with all extracted parameters, and a free C.

However, upon attempting to fit this, the results are not accurate, as seen in figure 5.6. Due to this, the values for C cannot be extracted, but the value of C does show a downward trend with decreasing resistance. This problem can be remedied by leaving the variables a and C free. Doing so leads to a very good fitting of actual device data, with an R-square value of 99.99%, seen in figure 5.7. With this model, values of a cannot be extracted, with the values of a having no stable relationship to temperature. This equation can still be used to model devices virtually if values of a and C are estimated, around 1.5E-17 and 0.3 for a pristine device. This leaves the model with the final form of 5.7.

$$I = (ae^{T^{0.034 \cdot log(R)+0.26}})e^{(-0.013T+14.23)^{V^C}} \tag{5.7}$$

Base Model	$I = Ae^{BV^C}$
First Level (T dependence)	$A = ae^{T^b}$
	$B = fT + g$
Second Level (R dependence)	$log(a) = R - 6.29$
	$b = 0.034\, log(R) + 0.26$
	$f = -0.013$
	$g = 14.23$

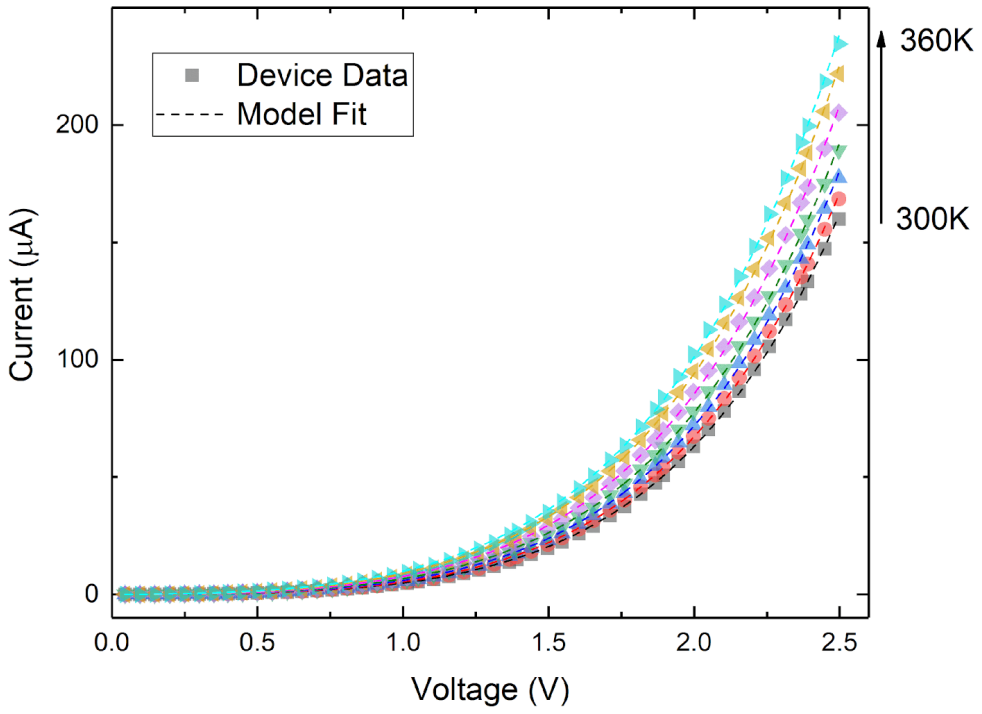

FIGURE 5.7: The fitting of the model with free a and C.

5.1.2 Displacement IV Model

The key feature of a memristor is it's ability to change resistance. This change in resistance may also lead to an alteration in the IV characteristics of the device, so this was investigated and modelled.

In order to achieve this, a simple methodology was developed. This involved taking a non-invasive IV measurement of the device, then subsequently displacing the device from its "R0" value using a train of pulses, taking another IV, then repeating this process several times in a row, gradually increasing the device's displacement. Figure 5.8 shows the process of selecting the stimulation voltage, due to the application of this being desired for formed devices, calibration tests were performed on a device with a resistance of around 80KΩ. It can be seen from subfigure A, that the initial round of stimulation results in a significantly larger displacement than subsequent ones, which resulted in any further displacement being overshadowed. Due to this, it was decided that the device resistance after the first round of stimulation should be treated as the R0 for modelling purposes. For the displacement measurements of these devices the resistance value was measured from the corresponding voltage point on the IV as opposed to a standalone read pulse, this was in order to minimise the time between stimulation and reading, minimising the impact of volatile effects causing the displacement of the device and

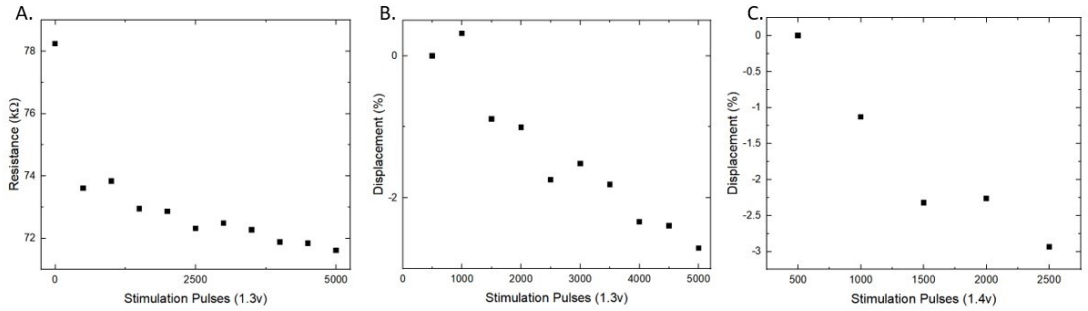

FIGURE 5.8: A. The resistance of a device during the applied displacement-IV routine, B. The proportional decrease in resistance of the device for 1.3v stimulation pulses, C. The proportional decrease in device resistance for 1.4v stimulation pulses.

its IV to be mis-matched. Subfigure B shows the displacement from R0 provided by 1.3v pulses. This displacement was decided to be too low, only resulting in an average change of around 0.27% per stimulation round, which would likely be close to the noise floor for higher resistance devices. In subfigure C, the stimulation pulses were increased to 1.4v, resulting in a significantly higher displacement of an average of around 0.6%. This provided a good tradeoff between device displacement and the risk of burning the devices

5.1.2.1 Model One

This model was based on the IV fitting equation of the form:

$$I = a(1 - e^{-bv}) \tag{5.8}$$

For generating this model, the IV-Stimulation loop was repeated twenty times. This model was initially chosen for compatibility with other work within the research group. From this data, the IVs closest to 1% displacement steps were selected, for the device shown in figure 5.9 device giving a spread of displacements.

Each of these IV curves was subsequently modelled using the above equation, with a example fitting shown in figure 5.10 A. After modelling the IV at each displacement the behaviour of the individual parameters was analysed, revealing them to be modellable using simple exponential relationships. These relationships indicate that as the device is displaced further down from R0, the IV curve has a greater curvature, and the size of the current through the device increases. Both of these characteristics have a saturating effect, possibly leading to the saturation effect seen in figure 5.9.

Comparing the modelling results for three separate devices indicated that this model was not likely to be made universal for these devices, requiring each one to be modelled on an individual basis, shown in figure 5.11. This is due to the non-monotonicity shown when comparing the parameter values of three devices, with the same devices appearing

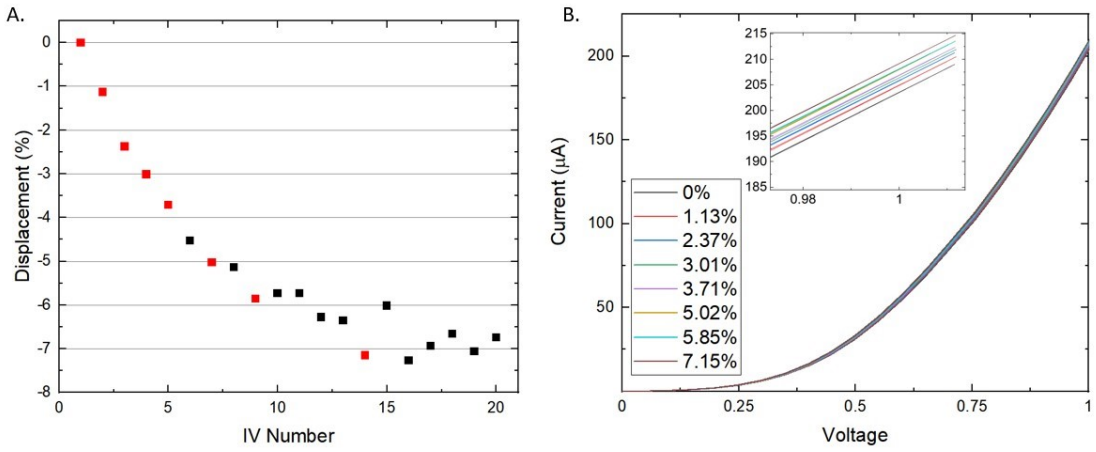

FIGURE 5.9: A. The proportional resistance change for the device, selected IVs highlighted in red, the IV at 7% displacement was later discounted, B. The selected IVs

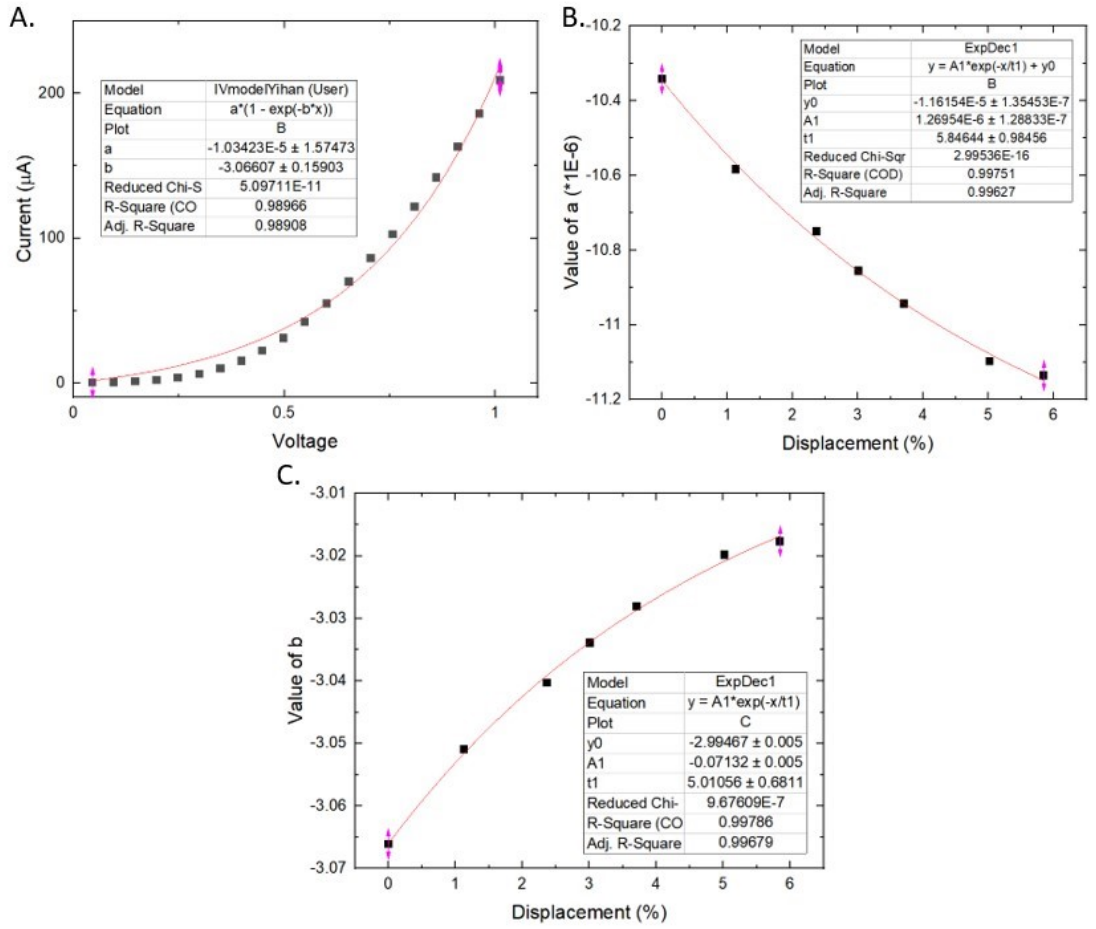

FIGURE 5.10: A. The fitting of the IV model, B. The displacement-a parameter relationship, C. The displacement-b parameter relationship.

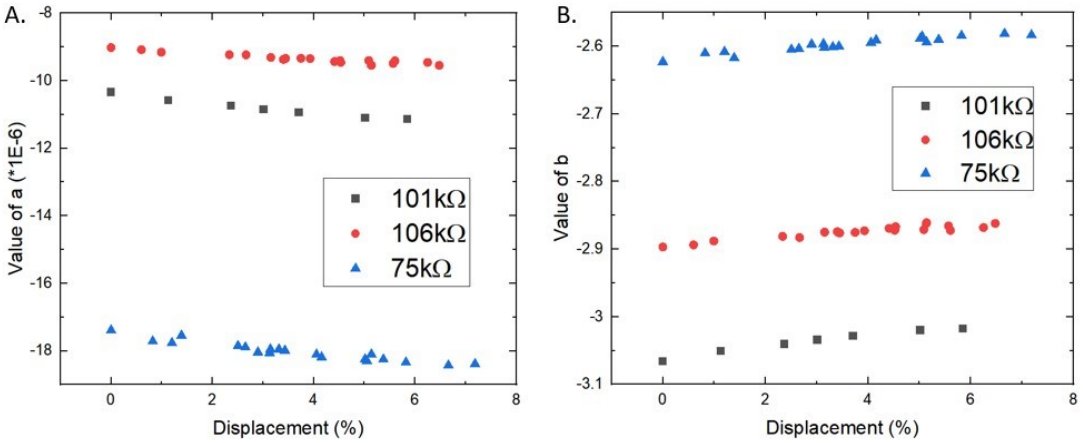

FIGURE 5.11: A. A comparison of the values of a for three devices , B. A comparison of the values for b of three devices.

in different orders on the graphs. It however, is clear that the lower resistance device exhibited significantly larger values in a and lower values in b, thus having a higher conductance and lower IV curvature. This matches the observed trend across previously tested devices.

This model indicates that as a device is displaced from its R0 value, the conductivity increases with some eventual saturation, and the IV curve of the device will flatten, becoming more linear/ohmic, again with saturating effects.

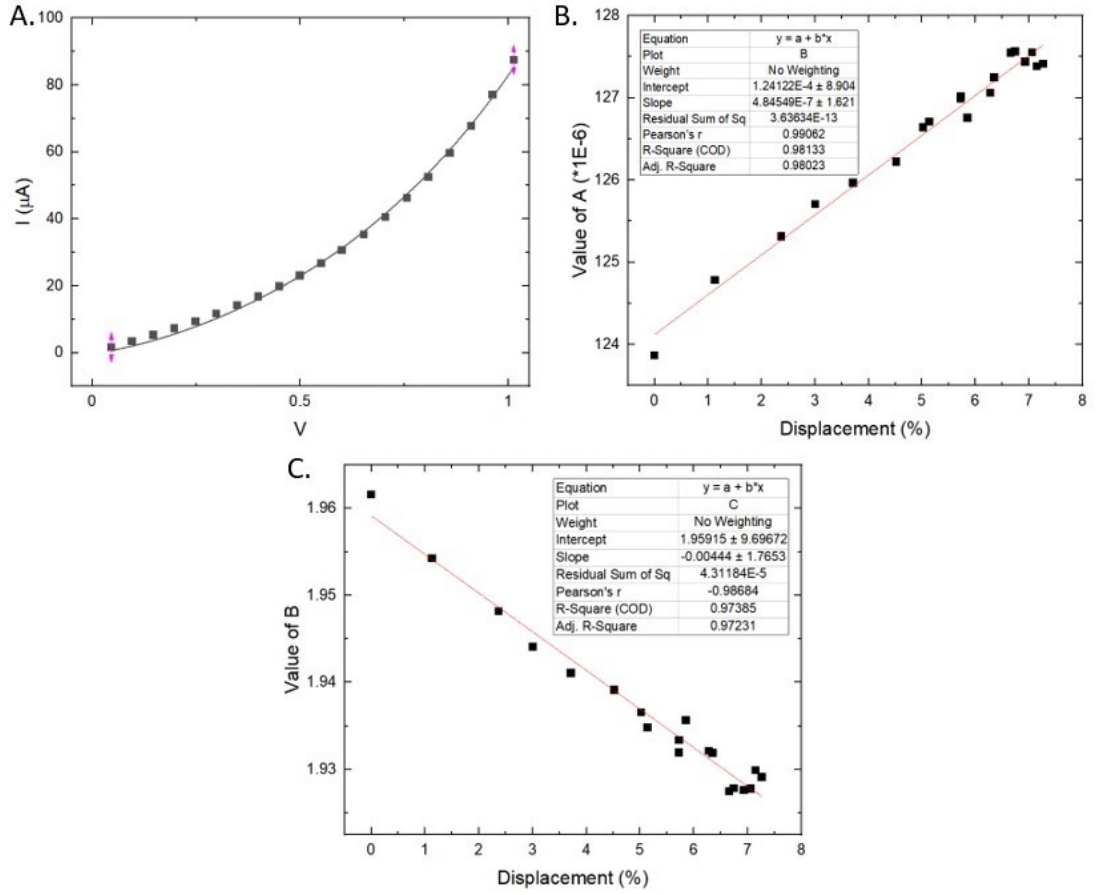

FIGURE 5.12: A. The fitting of the IV model, B. The displacement-A parameter relationship, C. The displacement-B parameter relationship.

5.1.2.2 Model Two

The previously developed methodology was subsequently applied to more devices, this time utilising a simplified version of the IV model developed earlier in the project due to the closer fitting ability. The fitting equation used in this case was 5.9,

$$I = A(e^{V^B} - 1) \tag{5.9}$$

Comparing figure 5.10 A and 5.12 A shows the closer fitting of the newer model's IV characteristics. The relationship between the fitting parameters and displacement from R0 exhibits a linear relationship in this case. This means that each device's displacement-IV behaviour can be modelled using the following equation:

$$I = (a + b\Delta R)(e^{V^{c+d\Delta R}} - 1) \tag{5.10}$$

Where ΔR is the proportional displacement of the device from R0, I is current and V is the voltage across the device. The remaining variables are fitting parameters to be calibrated for each device. The possible relationship between resistance and the values

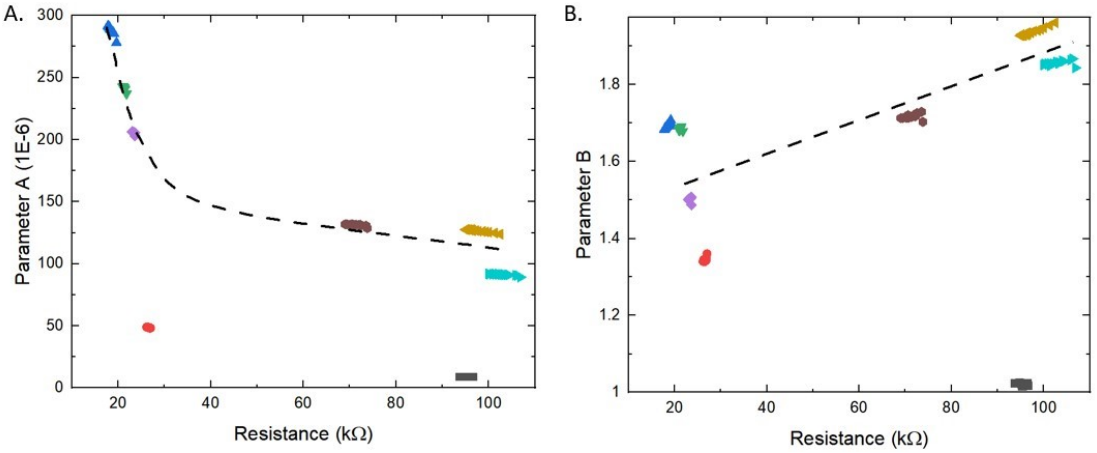

FIGURE 5.13: A. The resistance dependence of parameter A, including a proposed line of best fit, B. The resistance dependence of parameter B with a proposed line of best fit. Each colour represents data from a different device.

of the fitting parameters were further investigated, with the hope of generating a more generic model that would not need to be tailored to each individual device.

While there is not enough data to conclusively draw a connection between device resistance and the fitting parameter values, some relationships can be proposed for further investigation, these relationships being a logarithmic relationship for A, and linear for B, figure 5.13.

5.1.3 Volatile Switching Model

Understanding the transient characteristics of a memristor's switching behaviour is vital when implementing these devices into a complete system. Volatile characteristics influence parameters such as an expected memory lifetime, likelihood of a read error and provide information on the thresholds required for non-volatile memory storage, for example, if the device has a volatile drift back to equilibrium of X%, it may need to be displaced to the desired resistance plus X% further to compensate.

From previous work carried out by Christos Giotis, a voltage-volatility model was developed [78, 79]. Based upon this model, thermal dependencies on the various parameters were investigated. For the purposes of this work, volatility is defined as the transient change $R(t)$ in a device's resistance during a given time period t_w (for these experiments, t_w was selected to be 1 minute) after displacement due to invasive voltage stimulation. After stimulation, the device's resistance is measured using non-invasive pulses of 0.2v.

5.1.3.1 Voltage-Volatility Model

The first stage of the methodology for extracting the data is measuring the pre-stimulation resistance (R_{pre}) using the standard, non-invasive 0.2v pulse. Following this, N identical stimulation pulses of V_P are applied to the device in order to displace it from R_{Pre}, resulting in a saturating, controlled displacement (like that seen in figure 4.19). After stimulation, the device resistance is measured using the standard read voltage pulsing method, for the pre-defined relaxation period. The beginning of the relaxation period is recorded as R_{Start}, and the resistance at the end of the relaxation period recorded as R_{End}. The response of R_T exhibits an exponential decay behaviour, with a decay time constant of τ.

The form of the developed model was established to be 5.11.

$$R(t) = \alpha e^{-\left(\frac{t}{\tau}\right)^{\beta}} + \gamma \tag{5.11}$$

Where α corresponds to the relative offset of the device from R_{Pre} to R_{Start}, τ is the exponential decay time constant, β is the exponential stretch factor and γ is the predicted saturation point of the device at t = ∞.

5.1.3.2 Thermal-Volatility Model

From the base provided by the voltage-volatility model, the thermal dependencies were investigated. This was undertaken by re-tooling the methodology, primarily in order to reduce the time required for each set of measurements to around 30mins per device, per temperature, removing the study of pulse width on device behaviour. Three pristine devices were studied at temperatures of 25, 40, 55 and 70°C. Very limited difference in behaviour was noted between the three devices studied. The order of the applied temperatures was configured in such as way as to test some temperatures twice in a row in order to enable the identification of any drift in the results, and each temperature was tested at least three times to ensure a large enough data set for proper analysis.

From these sets of data the previously defined model was extracted and the parameters plotted against temperature to determine any dependencies. The primary parameters of interest were found to be the time constant and volatile jump.

5.1.3.3 Model Development

The first step undertaken using the extracted parameters was to model their voltage dependency at each temperature. This allowed for the unfolding of relationships, which for the purpose of clarity will be investigated on a parameter by parameter basis.

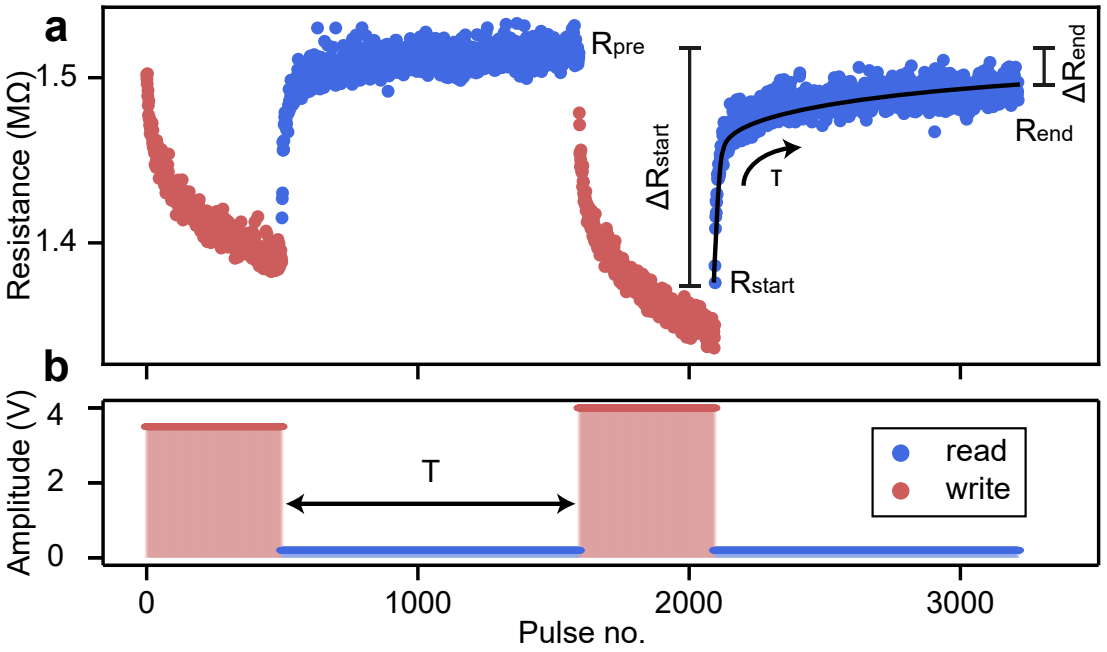

FIGURE 5.14: A snapshot of the protocol used to extract data for the thermal volatility model with key measurement parameters labelled, a. shows the change in resistance with increasingly invasive stimulation pulses, with the colours indicating the stages in stimulation/measurement in b.

5.1.3.4 Alpha

This is the scalar multiplier seen in equation equation 5.11.

This provides α with the relationship:

$$\alpha(V) = m(T)V + c(T) \tag{5.12}$$

The temperature dependencies of m and c can then be investigated. These relationships are *both* modelled using the same exponential decay relationship, giving the form:

$$m(T) = A1 \cdot e^{\frac{-T}{t1}} + y0 \tag{5.13}$$

Seen in figure 5.18. The numerical values for α's voltage and temperature relationship is derived to be:

$$\alpha(V,T) = (-300500 \cdot e^{\frac{-T}{10.5}} - 1320) \cdot V + (676150 \cdot e^{\frac{-T}{7.5}} + 300) \tag{5.14}$$

Base Equation	$R(t) = \boldsymbol{\alpha} e^{-\left(\frac{t}{\tau}\right)^{\beta}} + \gamma$
First Level (V dependence)	$\alpha(V) = m(T)V + c(T)$
Second Level (T dependence)	$m(T) = A1 \cdot e^{\frac{-T}{t1}} + y0$
	$c(T) = A2 \cdot e^{\frac{-T}{t2}} + y1$

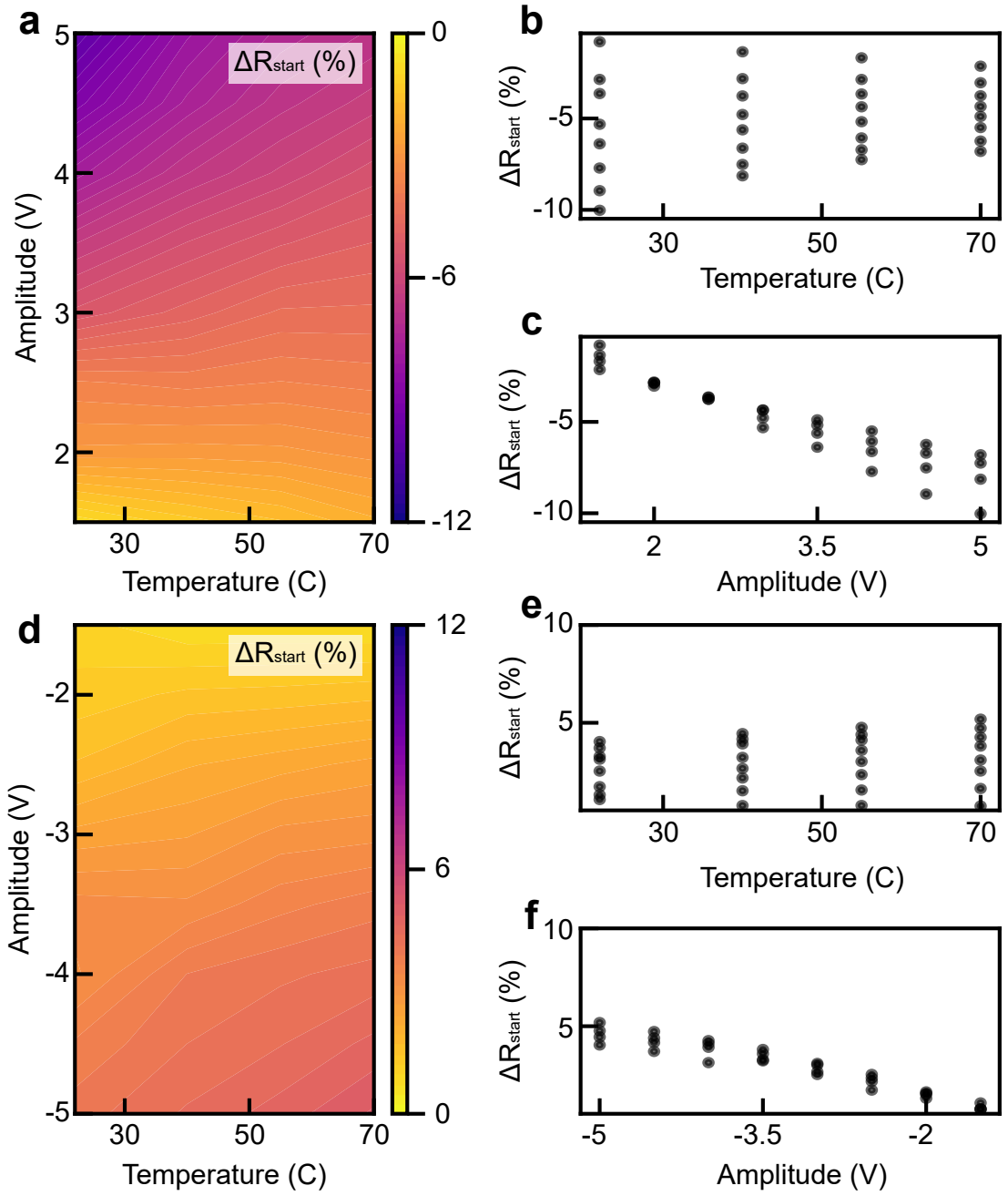

FIGURE 5.15: a. The volatile jump (ΔR) and it's temperature and positive voltage dependence, b. The projection of the ΔR-temperature relationship, c. The projection of the ΔR-voltage relationship, d-f. The same as the previous sub-figures, but with opposite voltage polarity (negative voltage stimulation).

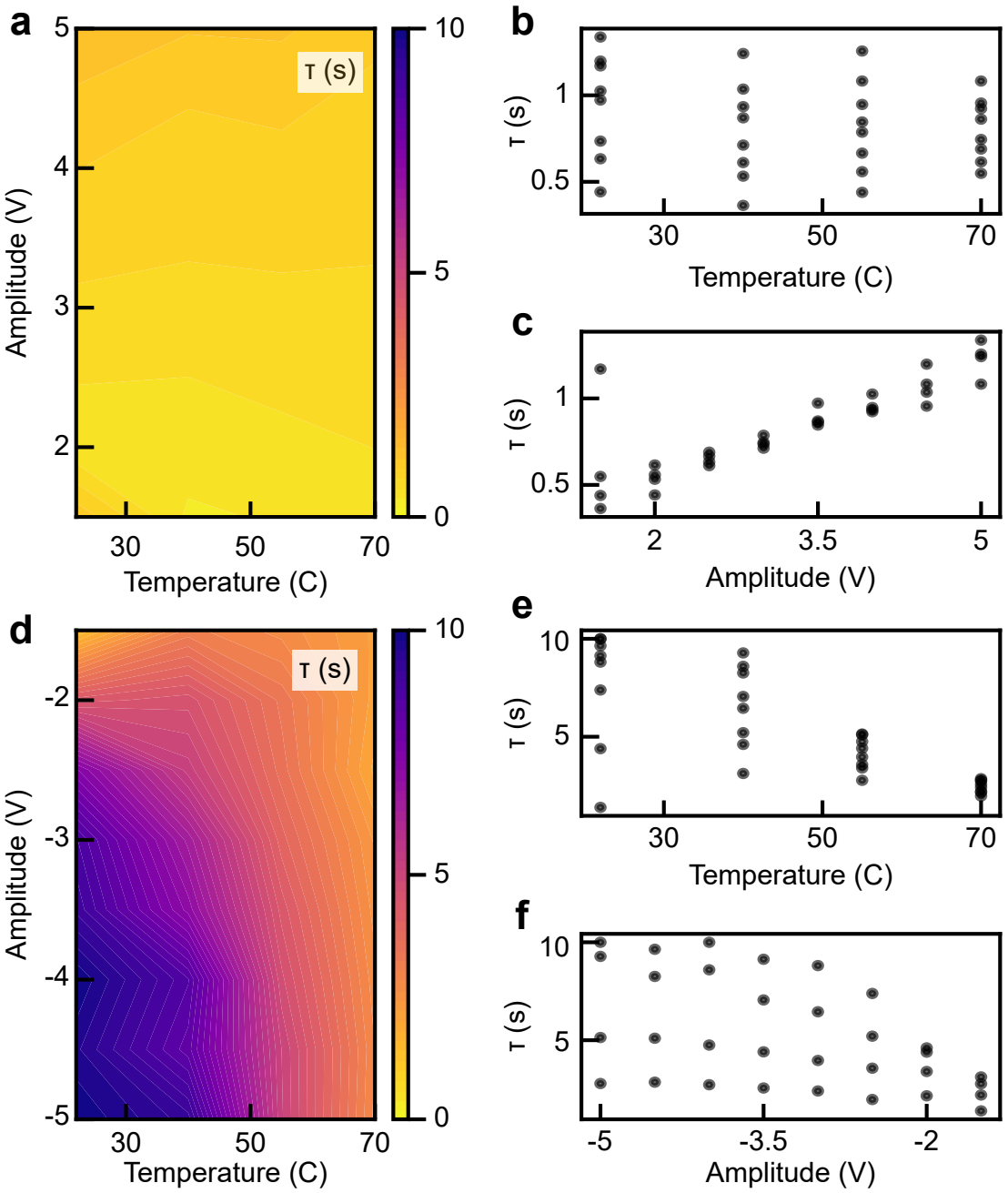

FIGURE 5.16: a. The relaxation time constant and its relationship to temperature and voltage, b. The projection of the time constant-temperature relationship, c. The projection of the time constant-voltage relationship, d-f. The same graphs as the previous sub-figures when the opposite polarity stimulation is applied.

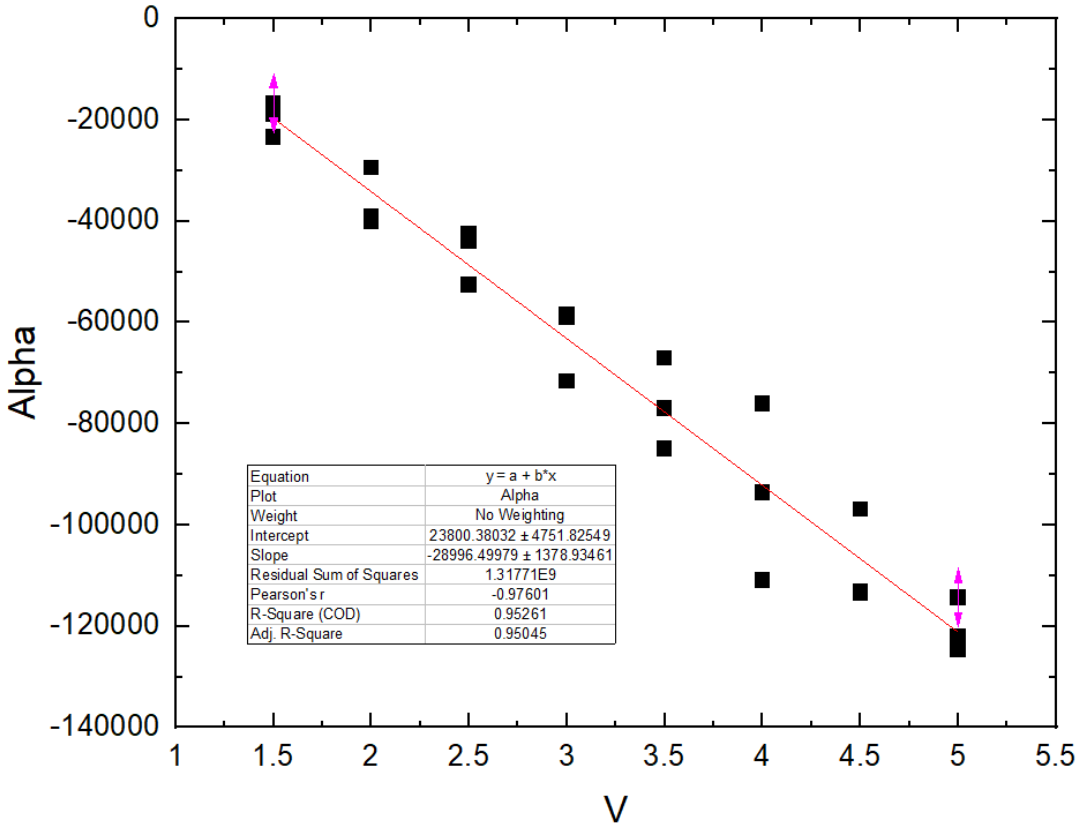

FIGURE 5.17: The voltage dependency of Alpha at 25°C, showing a strong linear relationship.

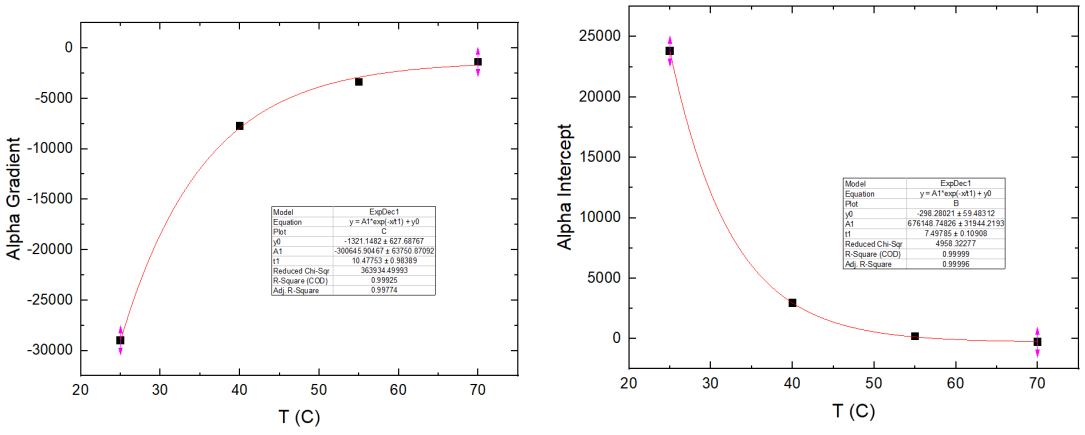

FIGURE 5.18: The temperature dependency of the Alpha parameters.

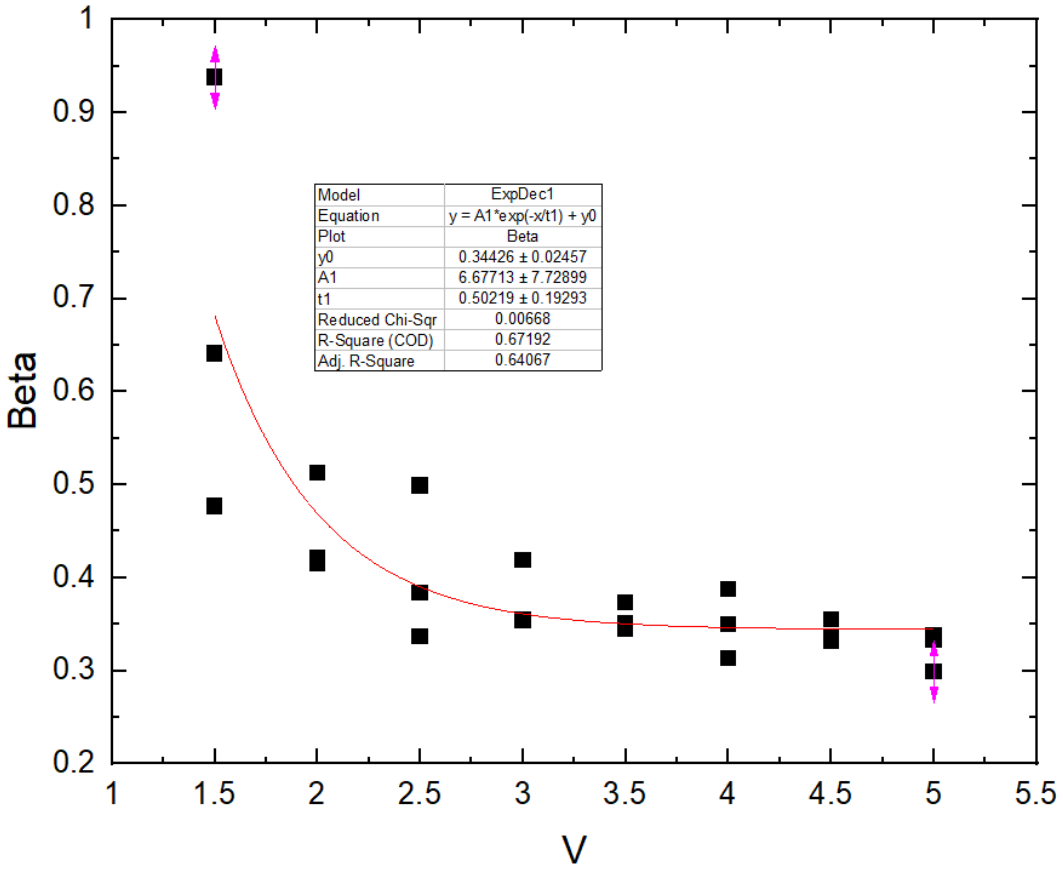

FIGURE 5.19: The voltage dependency of the β variable.

5.1.3.5 Beta

The next parameter investigated was the exponential stretch factor of 5.11, β.

The voltage dependency here can be modelled as another exponential decay relationship, figure 5.19, giving us three variables to check for temperature dependency, as before labelled $A1$, $t1$ and $y0$. Once checked for temperature dependencies, $A1$ shows another exponential decay, $t1$ a linear relationship. $y0$ appears to have no significant correlation with temperature, and is thus approximated to a constant value of 0.344, figure 5.20.

This allows for us to arrive at the numerical form of β as:

$$\beta(V,T) = (150 \cdot e^{\frac{-T}{7.6}} + 1.03) \cdot e^{\frac{-V}{0.1+0.014T}} + 0.344 \tag{5.15}$$

Base Equation	$R(t) = \alpha e^{-\left(\frac{t}{\tau}\right)^{\boldsymbol{\beta}}+\gamma}$
First Level (V dependence)	$\beta(V) = A1(T) \cdot e^{\frac{-V}{t1(T)}} + y0$
Second Level (T dependence)	$A1(T) = A2 \cdot e^{\frac{-T}{t2}} + y1$
	$t1(T) = mT + c$

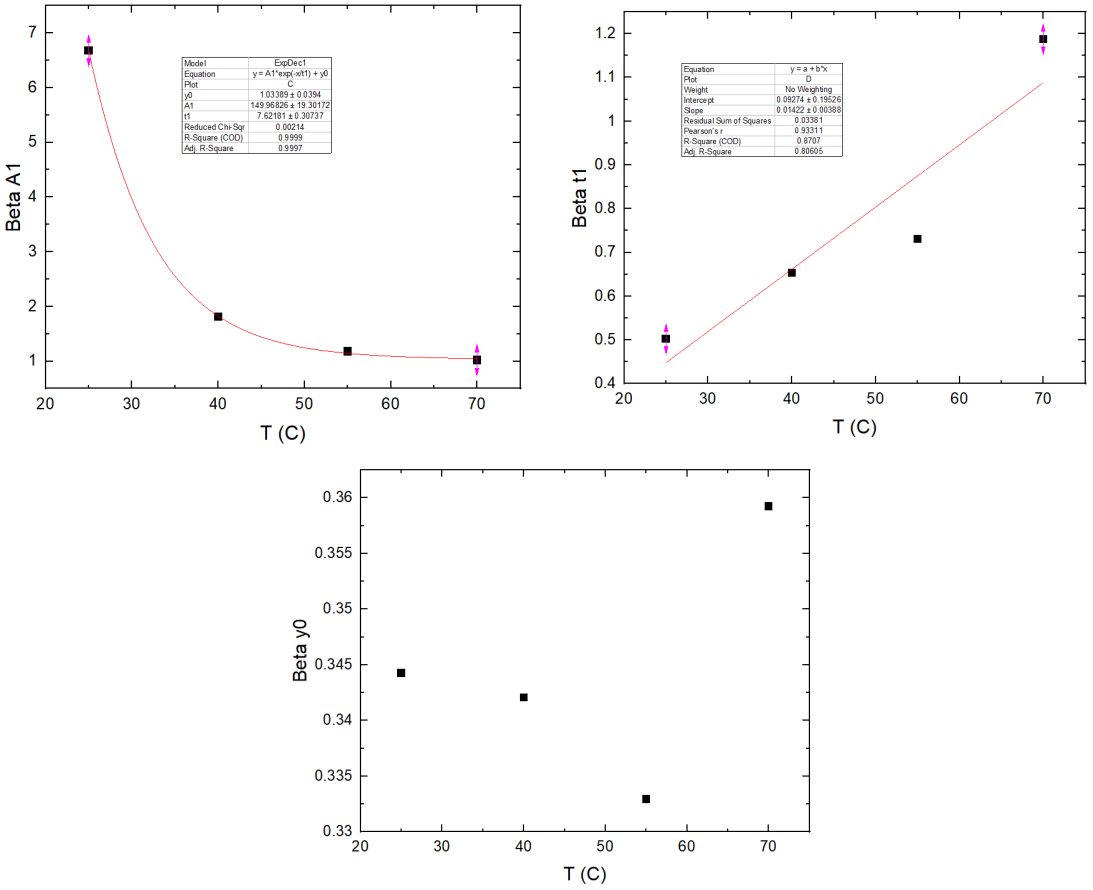

FIGURE 5.20: The temperature dependencies of the beta fitting parameters.

5.1.3.6 Tau

This is the time constant seen in 5.11. This parameter shows a linear relationship to voltage, figure 5.21, and the generated parameters can also be modelled using a straight line fit.

The numerical form of τ end up as:

$$\tau(V,T) = (0.354 - 0.0026T)V + (-0.336 + 0.0087T) \tag{5.16}$$

Base Equation	$R(t) = \alpha e^{-\left(\frac{t}{\tau}\right)^{\beta}} + \gamma$
First Level (V dependence)	$\tau(V) = m(T)V + c(T)$
Second Level (T dependence)	$m(T) = m1T + c1$
	$c(T) = m2T + c2$

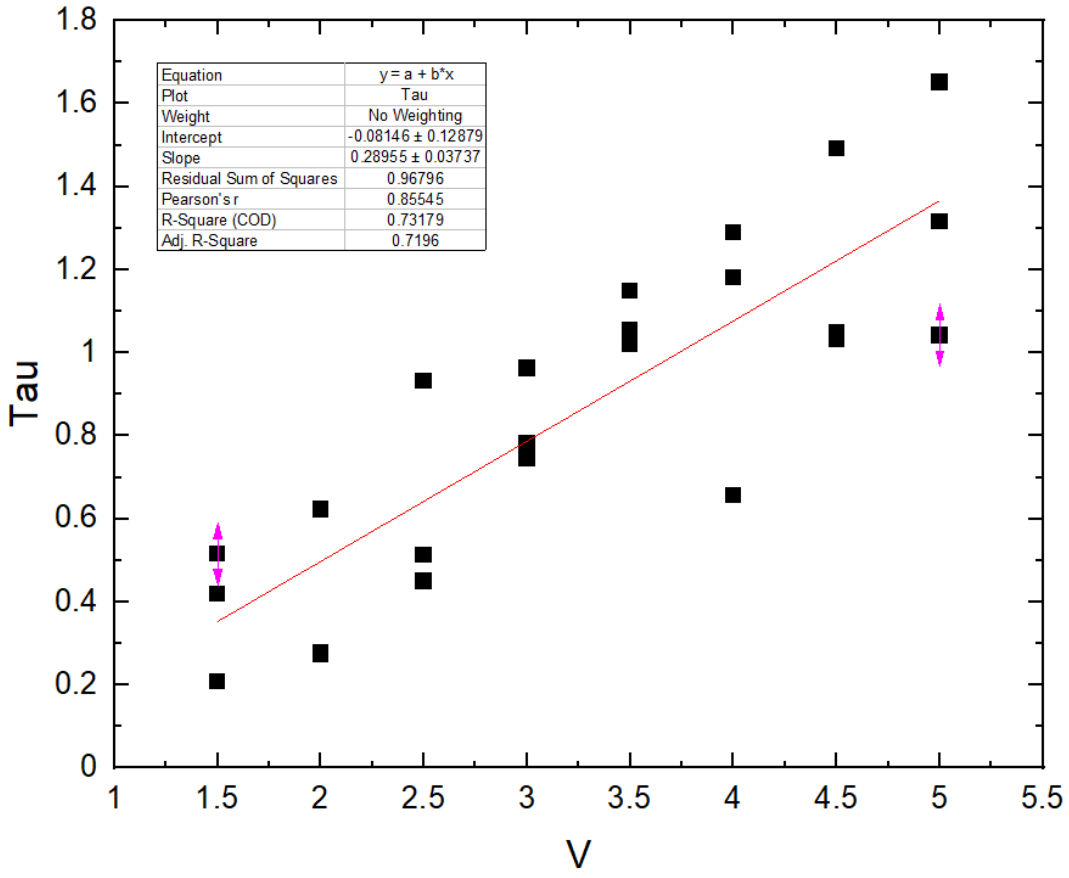

FIGURE 5.21: The time constant - voltage relationship of the volatility model.

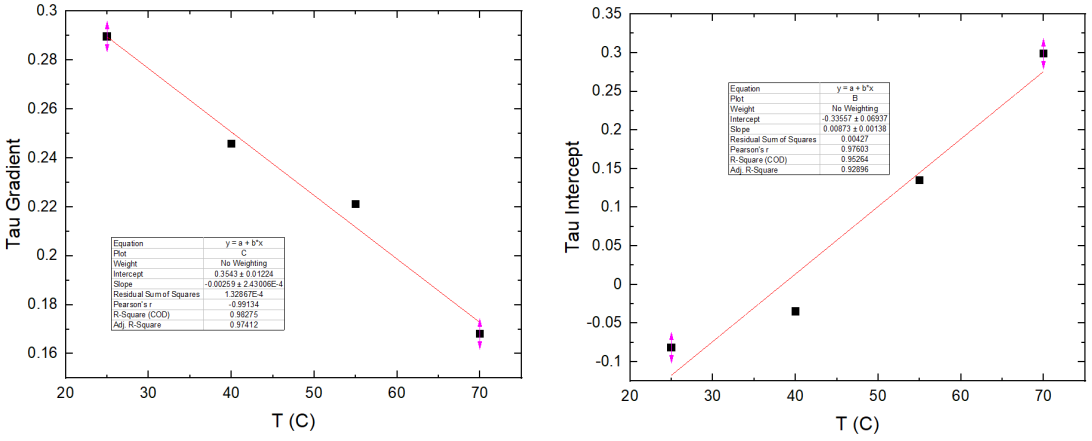

FIGURE 5.22: The temperature dependencies of the fitting parameters in Tau.

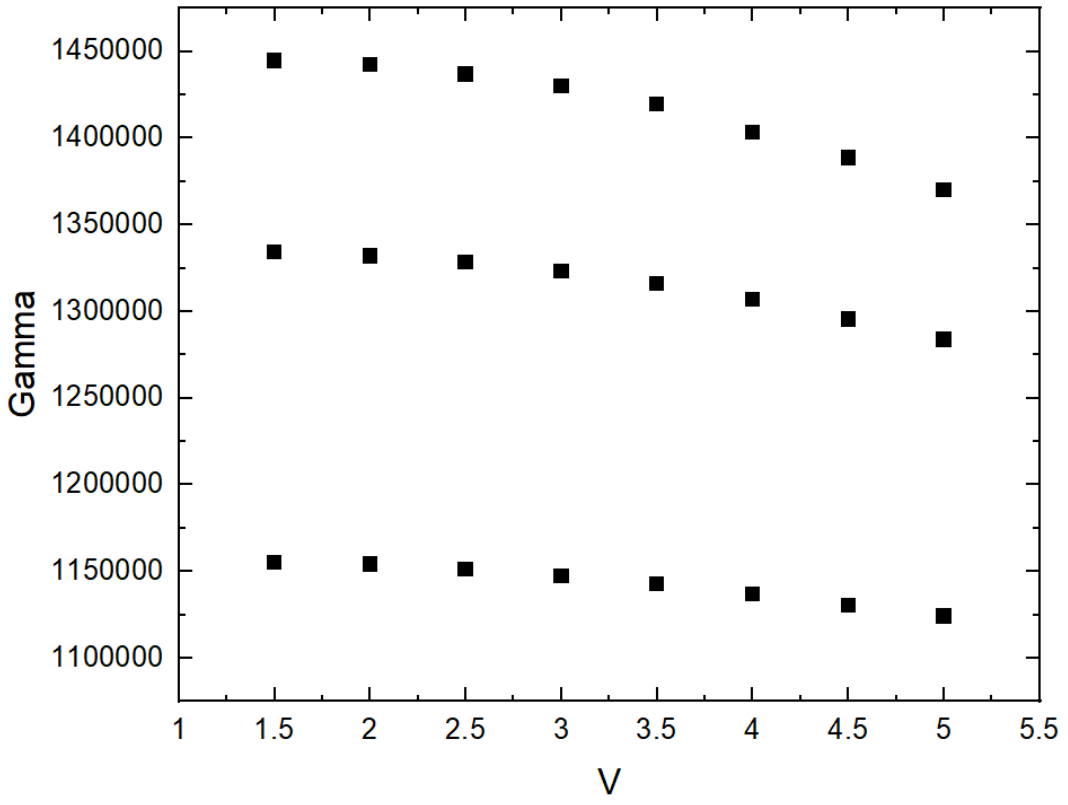

FIGURE 5.23: The voltage dependency of γ, showing each set of measurements having a different voltage relationship.

5.1.3.7 Gamma

Unlike the other parameters of the voltage-volatility model, γ does not exhibit a strong voltage dependency, leading to γ being modelled via temperature relationships, with which it once again exhibits exponential decay. The numerical form of γ is derived to be

$$\gamma(T) = 835600 \cdot e^{\frac{-T}{13}} + 65050 \tag{5.17}$$

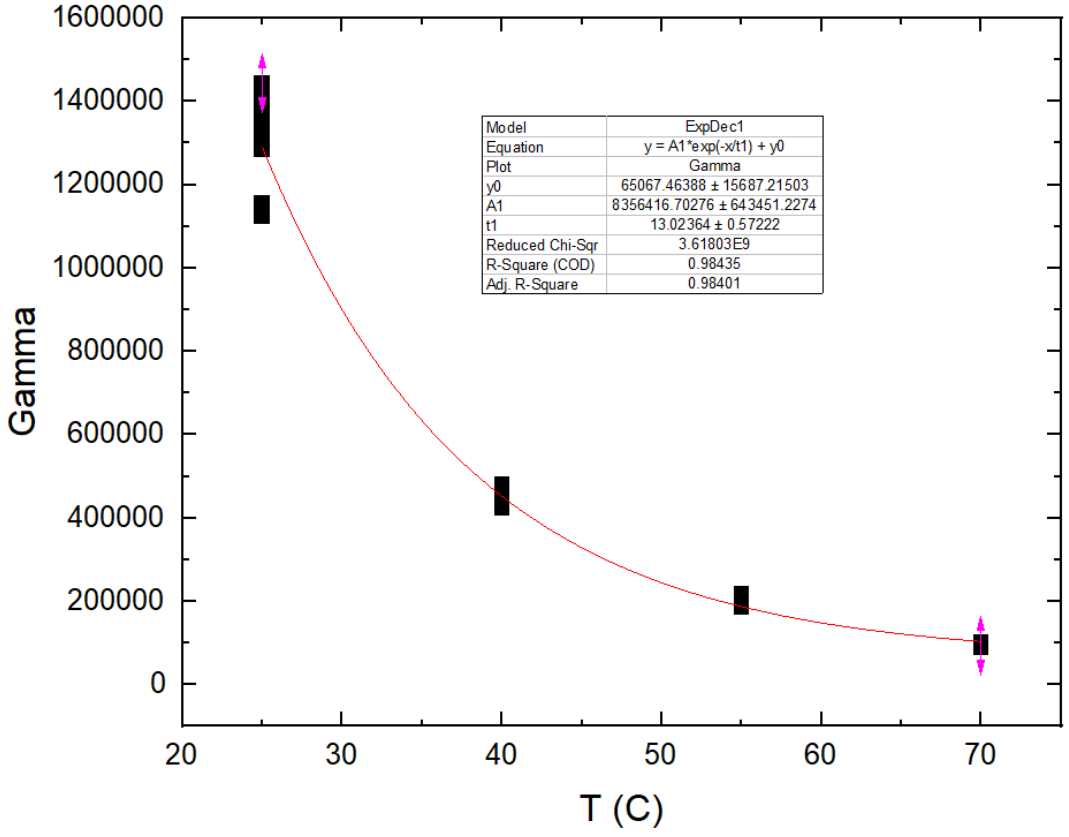

FIGURE 5.24: The temperature dependency of gamma, showing a strong exponential decay fitting.

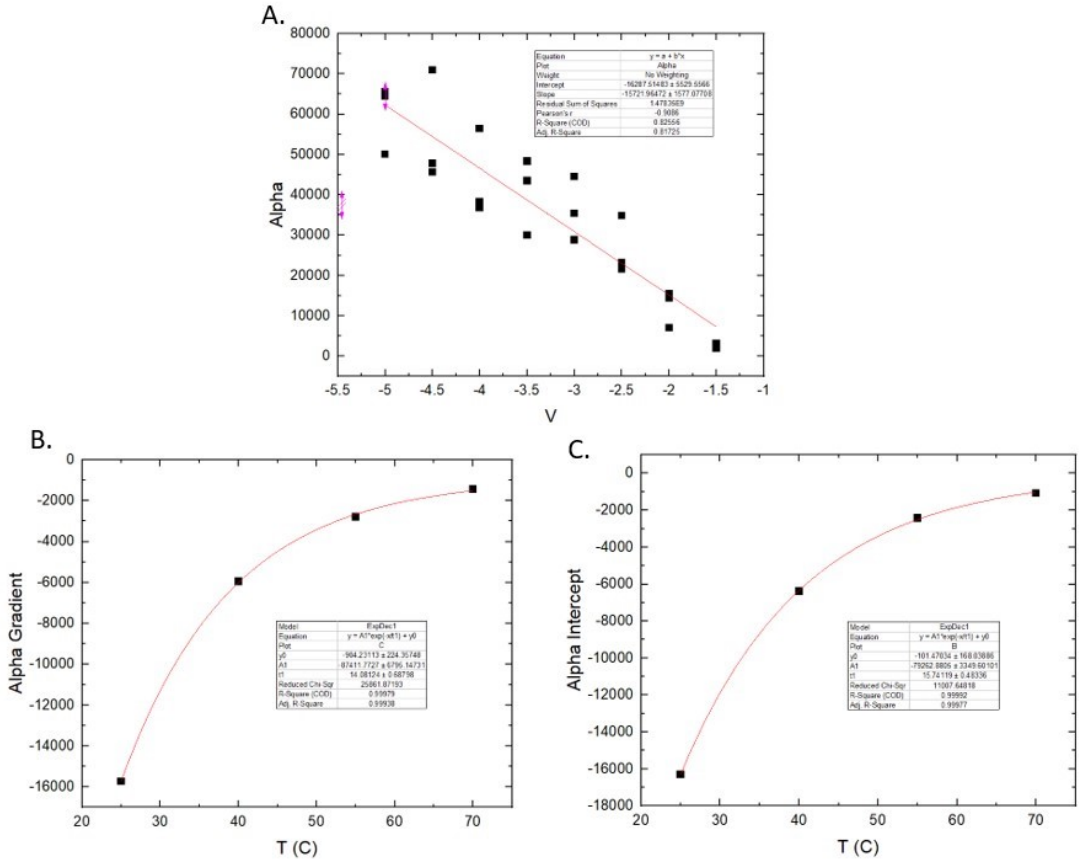

FIGURE 5.25: The voltage and subsequent temperature dependencies of the alpha parameter for negative voltages.

5.1.3.8 Positive Displacement Model

The previous modelling methodology was subsequently applied to the negative voltage pulsing results, which give positive changes in device displacement. Due to the asymmetrical nature of the devices studied, this gave similar behaviours, but with differing values, figures 5.25, 5.26 and 5.27. The model of γ is polarity independent.

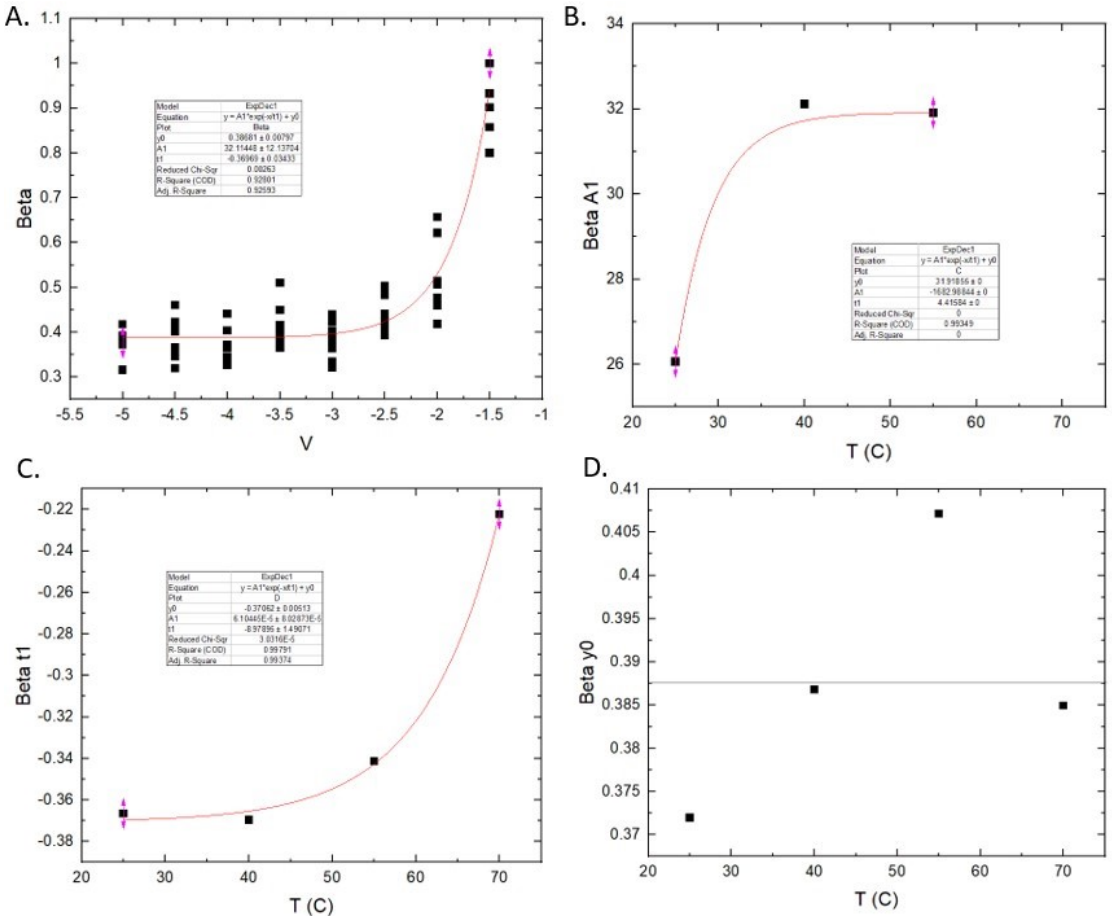

FIGURE 5.26: The voltage and subsequent temperature dependencies of the beta parameter for negative voltages.

Base Equation	$R(t) = \alpha e^{-\left(\frac{t}{\tau}\right)^{\beta}} + \gamma$
Alpha:	$\alpha(V) = m(T)V + c(T)$
	$m(T) = -87400 \cdot e^{\frac{-T}{14.1}} - 900$
	$c(T) = -79250 \cdot e^{\frac{-T}{15.7}} - 100$
Beta:	$\beta(V) = A1(T) \cdot e^{\frac{-V}{t1(T)}} + y0$
	$A1(T) = -1683 \cdot e^{\frac{-T}{4.4}} + 31.9$
	$t1(T) = 6.1E-5 \cdot e^{\frac{T}{9}} - 0.37$
	$y0 = 0.39$
Tau:	$\tau(V) = m(T)V + c(T)$
	$m(T) = 0.044T - 3.34$
	$c(T) = -0.27T + 0.033$

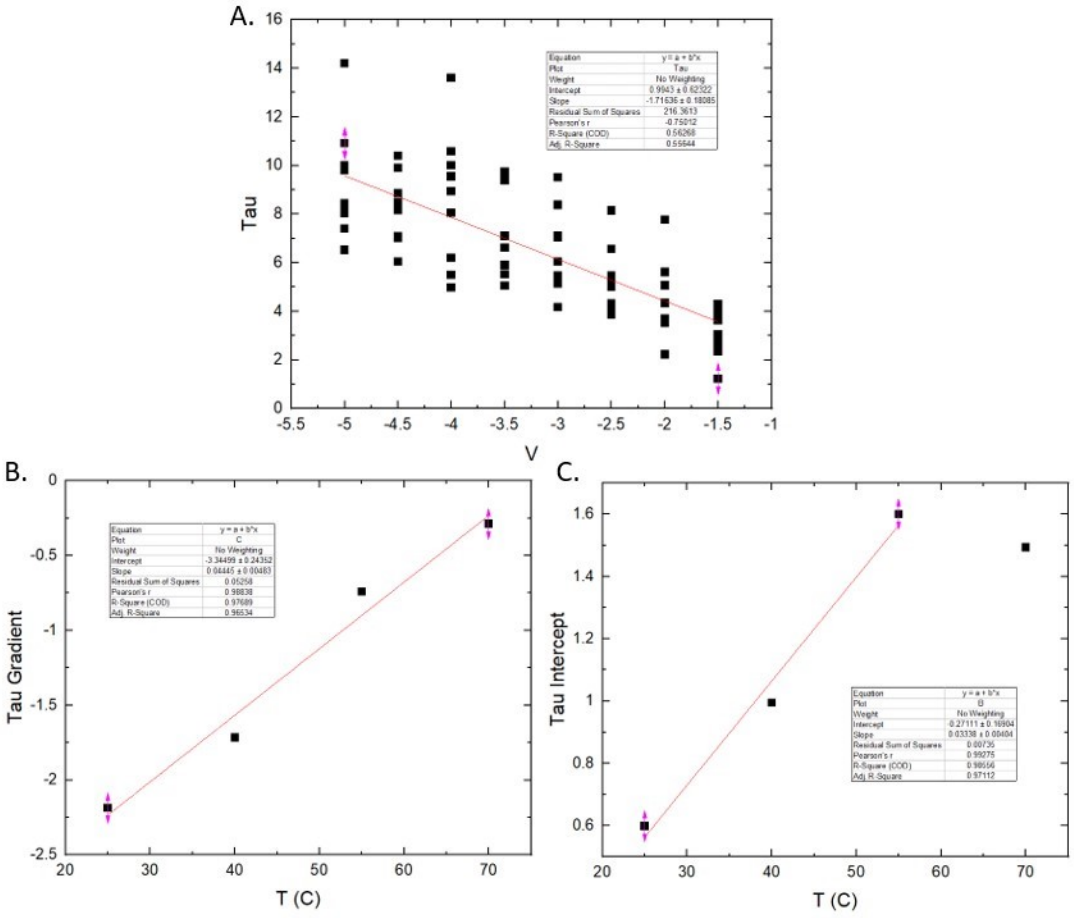

FIGURE 5.27: The voltage and subsequent temperature dependencies of the tau parameter for negative voltages.

5.1.4 Implications of Thermal Volatility Effects

From the projection of 5.15c [91], it is shown that increasing the voltage of the stimulus linearly increases the displacement of the device, with an increase in variability at higher displacements/voltages. Figure 5.15b indicates that temperature has the opposite effect on the spread of results, increasing the magnitude of smaller resistance changes, but decreasing the size of larger changes. This indicates that increases in temperature enhance the switching ability of the devices for lower voltages, but inhibit the device's switching ability at higher voltages.

In the case of negative voltage stimulation, 5.15f once again shows a linear increase in displacement with increasing voltage magnitude, however this time a saturating effect is observed above 3.5v. This time, temperature is shown to increase the variability of the resistance jumps, with low voltages being relatively insensitive to temperature variations and larger jumps being slightly enhanced with increased temperature.

The behaviour of the time constant in 5.16c [91] and f shows that a larger stimulation voltage and thus initial displacement will result in a longer time constant. Similarly to the initial displacement behaviours, this behaviour is a linear increase with voltage and once again shows saturating behaviour for negative voltages. Comparing 5.16a and d shows that the magnitude of the effect temperature has on the time constant for positive stimulation voltages is minimal, where as a much more significant impact is shown for negative voltages, with the value of τ dropping and becoming increasingly voltage insensitive with increases in temperature.

From these results we can see that the qualitative behaviour of these temperature dependencies varies quite heavily with different voltage polarities. With these devices, not only does temperature inhibit switching for positive polarities while enhancing switching for negative voltages at high bias values, but the enhancement/inhibition is reversed at low voltages. This indicates that we could possibly map the two halves of this behaviour as a mirror image of the other, with some re-scaling. It is currently un-clear as to what conduction mechanisms or electro-chemical processes may give rise to this mirrored behaviour, but does hint towards a distinct balance of multiple mechanisms being present under volatile switching conditions.

The difference in the impact of temperature on time constants is even more disparate, with the value of τ varying significantly with voltage polarity and showing a large difference in temperature sensitivity. Additionally, for negative voltages, at least two regions can be identified; at low voltages, we see at most a weak temperature dependence, compared to the high magnitude case. This split behaviour across polarities and the qualitatively different behaviour vs. stimulation voltage for negative polarities supports the conclusion that there are likely multiple volatility inducing mechanisms interacting with each other.

Finally, we can also observe a narrow band of bias voltages in both polarities where the temperature sensitivity for both the volatile jump and (positive) time constant is approximately 0. This region is around the ± 2v point. This has some interesting implications for practical circuit designs exploiting volatile behaviour:

1) There is a region of voltages that these devices can be operated with volatile behaviour independent from temperature (figure 5.15a).

2) By reversing the orientation, or reversing the bias of the memristor in the circuit and independently controlling the voltages used for positive/negative stimulation, we may select the volatile characteristics of the device.

3) There is limitation to the value of the temperature coefficient depending upon voltage polarity, i.e it is easier to inhibit the volatile jump for positive stimulation than enhance.

4) Selecting your bias voltage polarity may allow for the option to operate in temperature sensitive or temperature independent modes.

This model shows that the volatile behaviour of these devices is much more heavily impacted by temperature in the traditional "forward bias" mode that we operate them in. This implies that by controlling the bias of a device, you will be able to select a mode of volatile operation that is either more or less effected by changes in temperature.

Chapter 6

Temperature Based Emulation of a Homeostatic Neuron

6.1 Homeostasis

One of the most commonly investigated implementations for practical memristors is in emulating the behaviour of synapses. It was decided that given the static temperature-resistance relationship of the studied devices, the emulation of a homeostatic neuron would be undertaken, leveraging the temperature dependencies of the memristors in order to implement the homeostatic properties. Homeostasis is the property of the output of a neuron to have a relatively stable and fixed output across a set of constant (i.e. steady-state) inputs set at different levels, while producing transient output spikes/spike bursts upon sudden changes to the input. This allows for the neuron to essentially filter out background information.

To explore the possible application of utilising the temperature behaviour of these devices, an implementation of a thermally-stabilised synapse was developed, initially in mathematical simulation, followed by a practical realisation of the system.

6.2 Mathematical Model

The proposed system is based around the concept of a leaky-integrate-fire (LIF) neuron model. This model consists of three key sections, the input(s), the accumulator and the output, seen in figure 6.1.

The inputs can be any number of inlets to the accumulator, each of which has an individual weight. At each time step of the simulation the value at each input is multiplied

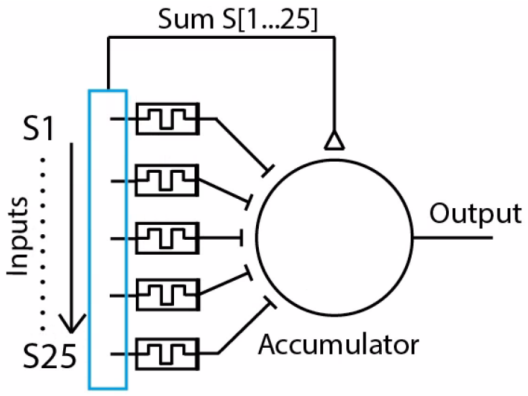

FIGURE 6.1: The schematic/symbol for the modelled neuron, showing the negative feedforward control system.

by it's weight, this value is then fed into the accumulator at each time step. The accumulator adds the sum of the inputs multiplied by weights, providing the integrate function of the LIF. Once the value of the accumulator reaches a threshold value, the output fires, reading as a "1", at this point the value in the accumulator is reset to 0. The accumulator is defined as being "leaky". This is defined by the accumulator at each time step losing some of the stored value, meaning that given no input to the system, the accumulator will trend towards 0.

For each of these models the inputs were all fed through memristors, with the resistance of the memristor providing the input's weight. The input values were simplified to binary values, either providing no input, or the weight of the pulsed input. The number of inputs selected to be used in this system was 25. Inputs were provided in an array of weighted random values.

The array of input values was generated by first filling the array with random decimal values between 0 and 1. In order to set input strengths, these values were then rounded to 0 or 1 depending upon the selected threshold. For example, if an input strength of 25% was desired for a section of the input array, the decimal values in the targeted section of the array would be rounded up if the value was over 0.75, and rounded down if below. Each input array comprised of six thousand sets of input values, ensuring that sample size would provide sufficient randomness, so as not be an impacting factor in input behaviour. Inputs to neuromorphic systems don't normally have a high proportional frequency, so the high end of input possibilities were ignored for this simulation, mostly focusing on the range of 15-25%.[92, 93]

The model of the neuron was developed in three stages with increasing complexity.

The most basic version of this model ignored any temperature dependencies of the memristors used in the study, essentially acting as a summing input to PWM amplifier, seen in figure 6.2.

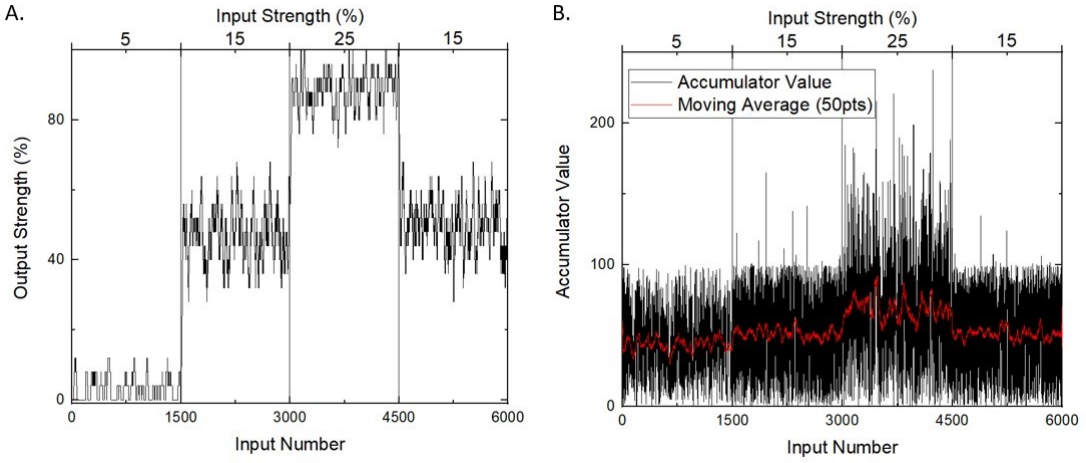

FIGURE 6.2: A. The simulated output of the neuron model ignoring temperature dependencies, B. The value in the accumulator at each input phase.

For this data, the output strength of the neuron is defined by the number of times it has fired within a 25 sample time frame, giving a more granular snapshot of the output pulse density.

After the basic function of the neuron model was demonstrated, basic temperature dependency was incorporated into the model. It was during the development of this model that the negative feedforward control system was implemented as opposed to the more traditional negative feedback. This was undertaken as it would allow for the heater to have a much more rapid response to changes on the input. The simulation was updated with memristors with a linear thermal coefficient, approximated from the static thermal behaviour of a pristine device, shown in figure 4.5. The temperature of the microchamber for varying input strengths was modelled from the physical system by setting the heater to a series of specified powers, to create a heater power/temperature model and allow for the simulation of the microchamber's thermal inertia. These additions to the simulation result in the attenuation of the output with increasing input values, reducing the outputs for 15 and 25% input from 45 and 85% down to 28 and 45%, seen in figure 6.3. From this point, it was the case of finding the thermal gain (input strength to heater strength ratio) required to compensate for changing inputs in order to produce a stable output when at a steady state.

From the demonstration of thermal effects being capable to controlling the output of the system, an input response curve can be generated, and controlled by adjusting the strength of the simulated chamber's thermal gain. These curves in figure 6.4 show that increasing the thermal gain reduces the gain of the output, alongside reducing the width of the optimal input loading area, the section of the input strength where the output remains fairly constant. The effect of changing the thermal gain can thus be utilised as a method of increasing selectivity in the input, or as a method of modulating the output gain of the system.

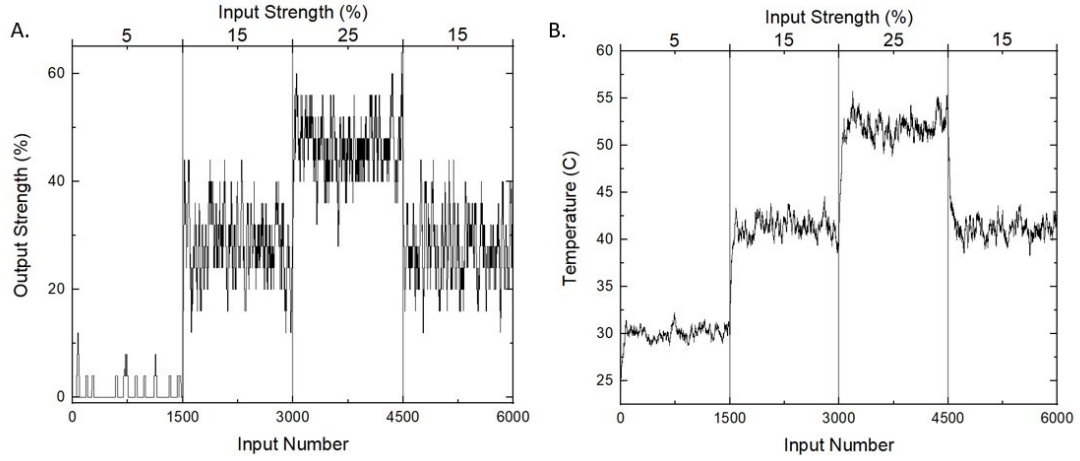

FIGURE 6.3: A. The simulated output of the neuron model with temperature affected input weighting, B. The simulated chamber temperature.

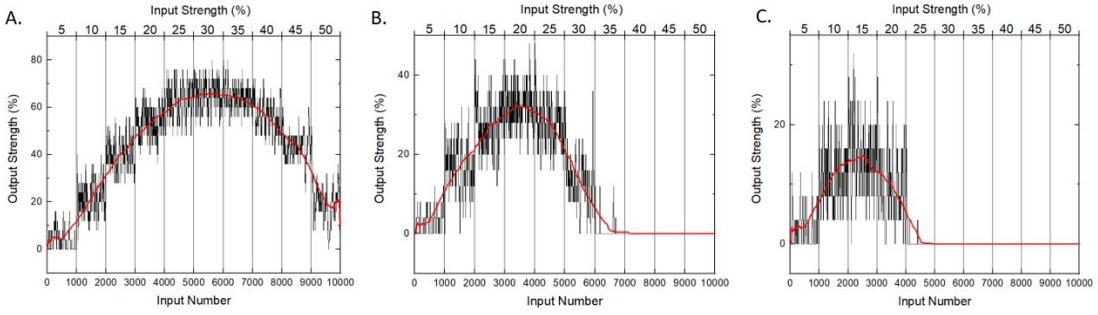

FIGURE 6.4: The effect of increasing thermal gain on the simulation output, A. the results of a thermal gain of 4, B. 6, and C. 8.

The final stage of the simulation was to implement a further stage of thermal inertia into the memristor weights. This would allow for the simulation to exhibit the spikes desired when the input strength is changed, as the output strength changes faster than the temperature control system can account for. This was implemented using a leaky integrator whose value would change depending on the difference between the current value and that of the microchamber, resulting in the temperature of the memristors gradually approaching that of the chamber, much more closely emulating experimental behaviours. Figure 6.5.

These simulated results were a very strong proof of concept for the proposed system for physically implementing a homeostatic neuron using thermal control methods, and provided a starting point for the variable parameters implemented in the physical system.

6.3 Practically Emulating a Homeostatic Neuron

In order to emulate the homeostatic neuron, a new program was created for use with the ArC ONE system. This program replicates the previously developed simulation (figure

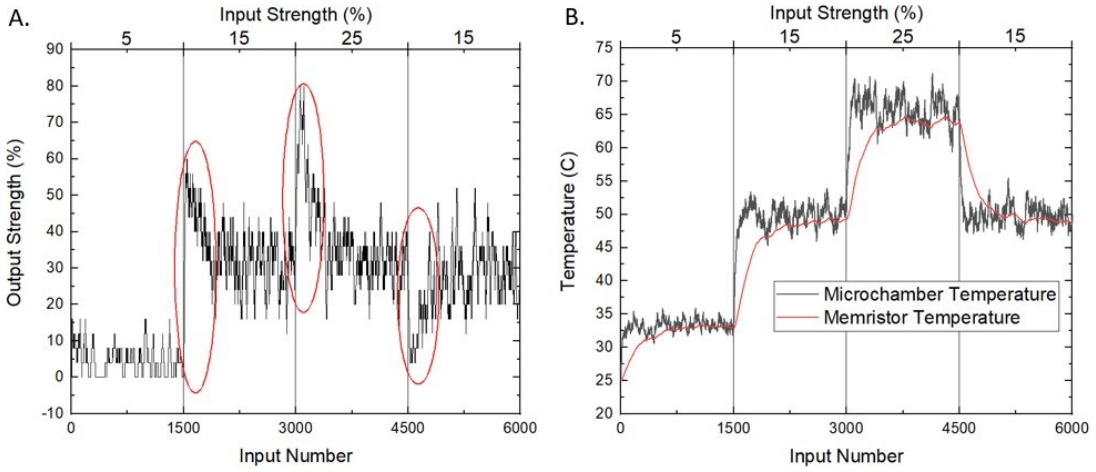

FIGURE 6.5: A. The output of the simulated system exhibiting spiking behaviour on the leading edges of changes in input strength (circled in red), B. The response of the microchamber temperature compared to the memristors.

6.1), and incorporates communications with and control of the environmental control microchamber. For these experiments, 25 devices were selected, and a series of 144,000 randomised inputs were provided to the program's synapses at a rate of 10 per second, resulting in each input block in the following sections lasting for a period of one hour.

From figure 6.6A, it can be seen that the in/out gain curve of the physical system is improved compared to that of the simulation, with the usable input range being comfortably 15-40%, with this spread of input values providing an output that ranges from 10-12% at steady states. This was a significant improvement over the initially specified input range of 15-25% input loading. This is likely due to the reduction in temperature sensitivity observed in pristine devices in figure 4.5, which was not included in the simulation, and would prevent the drop off in output observed in the simulated gain curves. In this configuration, the maximum operating temperature of the microchamber is a limiting factor, with higher than 40% input strength being close to the rated maximum temperature.

Figure 6.6B shows the output behaviour of the system when provided the same input, both with and without thermal control enabled, this output behaviour closely resembles that of the simulated version, with C and D showing the system responses to the same input weights in different orders.

This system is successful in it's attempts at reproducing homeostatic effects, with a narrow steady state band of around 2% (between 10-12% at the output), with the spiking upon a change in input being much larger than this, with the largest spike on input change having a magnitude of 10% (figure 6.6D, at input 36,000) and the smallest being 4% (figure 6.6C, at input 72,000), with both of these output spikes being significantly larger than the steady state band.

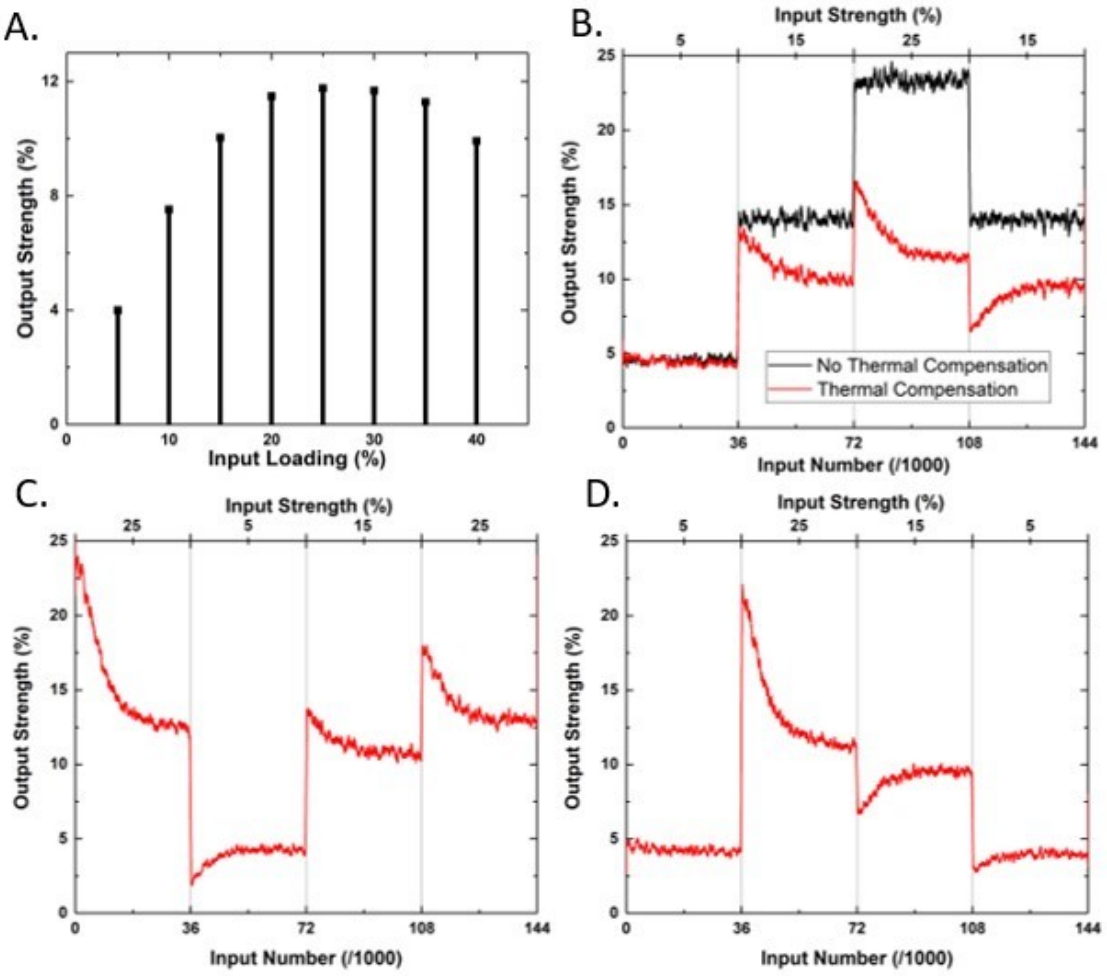

FIGURE 6.6: A. The in/output spiking gain of the tuned physical system, B. The difference in output behaviour of the system given the same input pattern, with and without the thermal compensation enabled, C and D. The output behaviour of the physical system when fed the same input strengths in different orders.

Chapter 7

The Impact of Atmospheric Humidity on TiOx Devices

7.1 Steady State Effects

From the literature it is expected that humidity will have some effect of the conductivity of TiOx memristors, however, the magnitude of this effect is known to be small, and experiments must be carefully designed in order to capture the alterations caused.

7.1.1 Methodology

After developing the methodology for measuring the effect of temperature on the resistivity of the devices, a variation was developed use with humidity. It the "room" temperature of the system should be kept constant, originally aiming for a temperature of 300K, however this was later increased to 305K due to room temperatures getting very close to or slightly exceeding 300K resulting in slight temperature drifts in the earlier experiments. Due to the release of moisture from the devices not being expected, the rest time between tests was reduced to an hour, during which, the air pump would run continuously through the chamber in order to purge it using air from the ambient conditions.

With the temperature of the system set to 305K, the devices were left to warm up for 1.5 hours before the relative humidity in the chamber was set to 45% for 1 hour, followed by 1 hour rest while the chamber was purged, with this repeated again for 55% and 65% relative humidity.

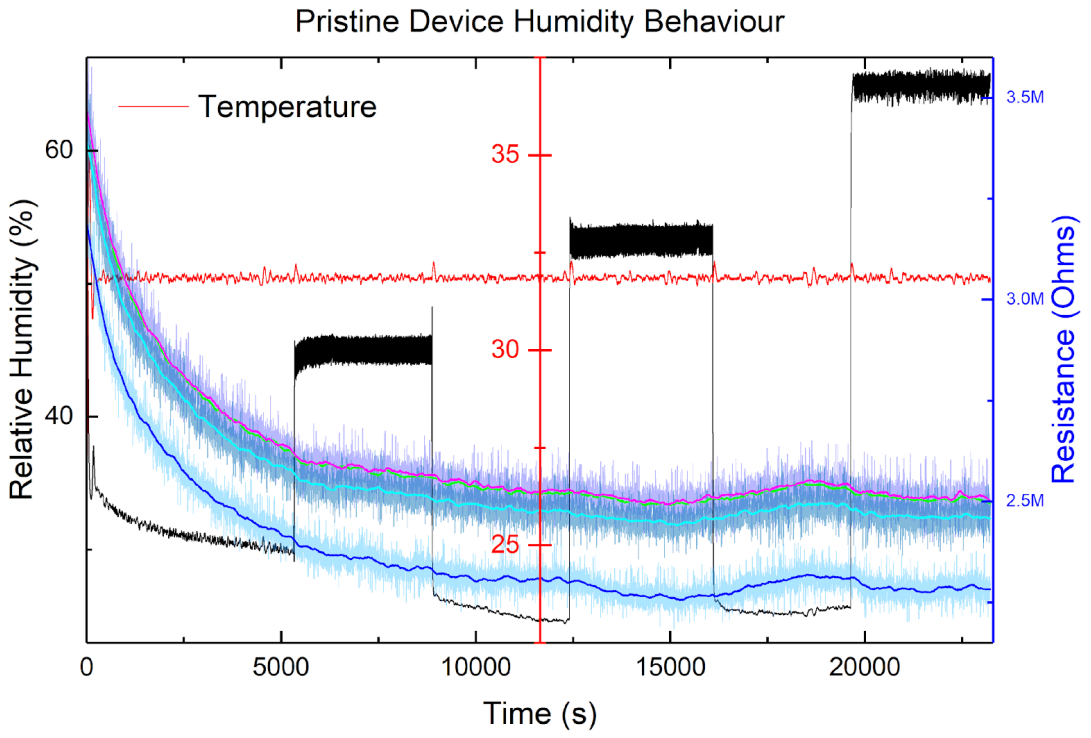

FIGURE 7.1: The results obtained from a continuous study on the impact of humidity on four pristine devices.

7.1.2 Results

From the results shown in figure 7.1, the effects of humidity are not entirely clear. The results do indicate that the temperature of the devices doesn't fully stabilise with the temperature of the chamber until around 12,000 seconds, meaning that the first usable results are for the 55% relative humidity. During the 55% measurements, it can be seen that the resistivity of the devices does decrease which is in line with the literature predictions, however, at around 15,000 seconds the resistivity begins to increase very slightly again, which is not expected. Once the chamber is purged, the resistivity continues to increase at a more substantial rate, before decreasing slightly before the application of the 65% humidity. No clear conclusions can be drawn from these results, however, possible alterations to the experiment can be identified. There may be some fluctuation in the temperature of the devices which is not being detected by the air temperature sensor. If in further experiments where only temperature is controlled and the same variation in resistivity is not observed, then it is possible that these variations are due to TiOx devices releasing some of the absorbed moisture over the time period of around 45 minutes. Further investigation into this involved passing air through the chamber which was first pulled through a large amount of silica desiccant. This provided an environment with around 15-20% relative humidity, compared to the usual

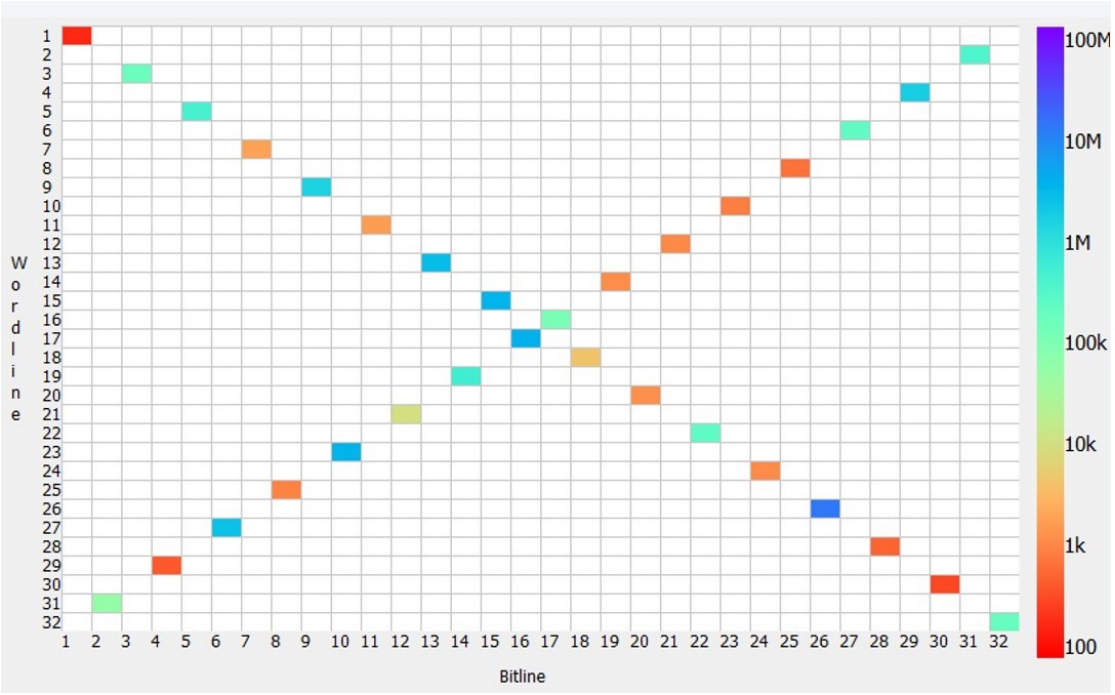

FIGURE 7.2: The state of the devices on the package subjected to high humidity at t=0s.

35-40%. The resistivity of the devices was monitored during this, however, no alteration to the resistivity occurred. These results indicate that it is likely that the devices were saturated, and will not release moisture without being exposed to significantly elevated temperatures, which would subsequently introduce the possibility of further oxidation of the devices and alteration of the oxide structure resulting in the need to perform this heating under an inert atmosphere.

7.2 Humidity Triggered Recovery of Memristors

It is known anecdotally, that application of small quantities of water onto a used or burned TiOx memristor can result in the restoration of functionality. The possibility of using high humidity atmospheres to achieve similar results was investigated. This methodology is more desired than the direct application of moisture, due to the ability to perform electrical measurements on the devices during the process of reviving them, and for the ability to utilise the devices immediately after recovery, without having to wait for the applied water to evaporate.

To investigate this, a package containing 26 formed or burned devices (figure 7.2) was subjected to an atmosphere at 90% relative humidity for the period of one week, while the resistance of the devices was measured at intervals of 3 seconds.

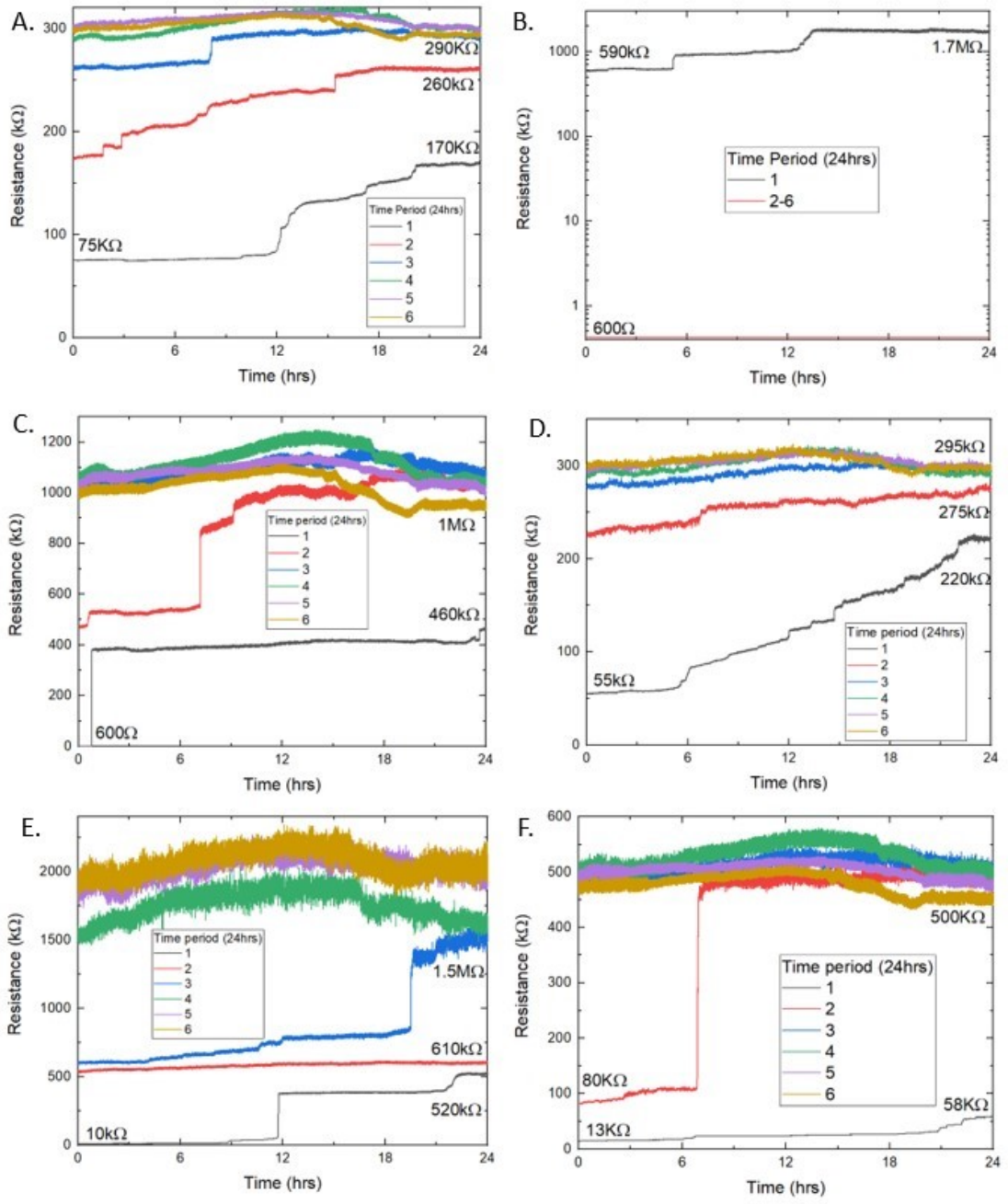

FIGURE 7.3: Spontaneous recovery of resistive state observed in 6 devices.

7.2.1 Results

Of the 26 formed or burned devices, 6 of them exhibited significant changes in resistance, seen in figure 7.3. These devices, especially C, E and F displayed very sudden and large jumps in resistance. The effect that humidity had on these devices also appears to be time limited, with no further changes in resistance happening after 72 hours of exposure. The large drop in resistance exhibited by device b in figure 7.3 was due to the switching measurements burning the device during the measurements taken at the 24 hour mark.

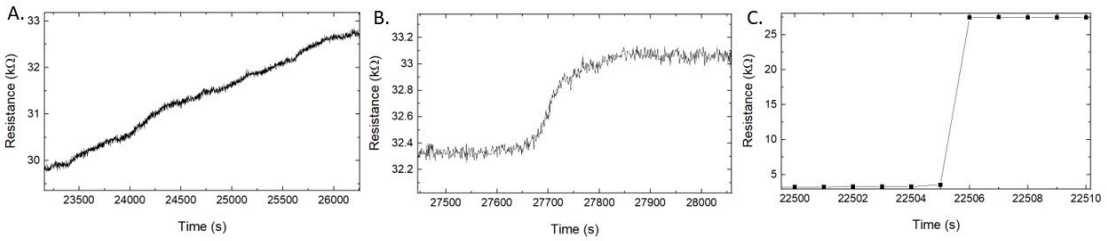

FIGURE 7.4: The observed "modes" of resistance increase, A. linear, B. exponential and C. jump

Scaling in to these resistance changes indicates three "modes" of operation highlighted in figure 7.4, a gradual, more linear increase, an exponential increase and a sudden, large jump in resistance. This large jump appears to happen well within a 1 second time frame.

At the moment, we cannot provide a conclusive explanation for these observed behaviours, however, these patterns may indicate three separate forms of re-oxidation in the device. The linear recovery within the device is possibly due to re-oxidation of the bulk material in the device, which would provide a more gradual increase in resistivity as the side-paths for charge transport through the bulk are removed. The exponential increases shown in panel B could be due to the reduction of filament width as it is re-oxidised from the outside in, reducing the conducting channel cross-sectional area, thus exponentially increasing the resistance of that channel. The final panel, depicting the large resistance jumps are possibly due to the disconnection of a filament between the electrodes, which would result in a very sudden and large jump in resistance.

Despite this experiment being conducted without shielding, we can rule out the possibility of voltage fluctuations being the cause of these resistance changes, due to the voltage applied to the devices being constantly monitored and measurements being recorded simultaneously. Further more, changes caused by these effects would likely affect multiple devices at the same time, which is not observed in these results.

The IV and switching characteristics of these devices were also investigated, with measurements taken pre-humidity and after every 24 hour cycle. Figure 7.5 shows the switching behaviour of one of the devices which increased its resistance. The initial switching behaviour (the data labelled 460kΩ) is highly unstable, with consecutive pulses of the same voltage causing the resistance to change in an unpredictable manner. After the initial resistance increase to 1MΩ the switching behaviour past -0.9v becomes regular, predictable, and of a much higher amplitude than the previous results. This clearly demonstrates that the increases in resistance in these devices also corresponds with a restoration in switching behaviour, with results matching those expected from a device originally formed into the operating region of L1. This restoration of behaviour is also observed in the IVs of the recovered devices, shown in figure 7.6, with the device's IVs

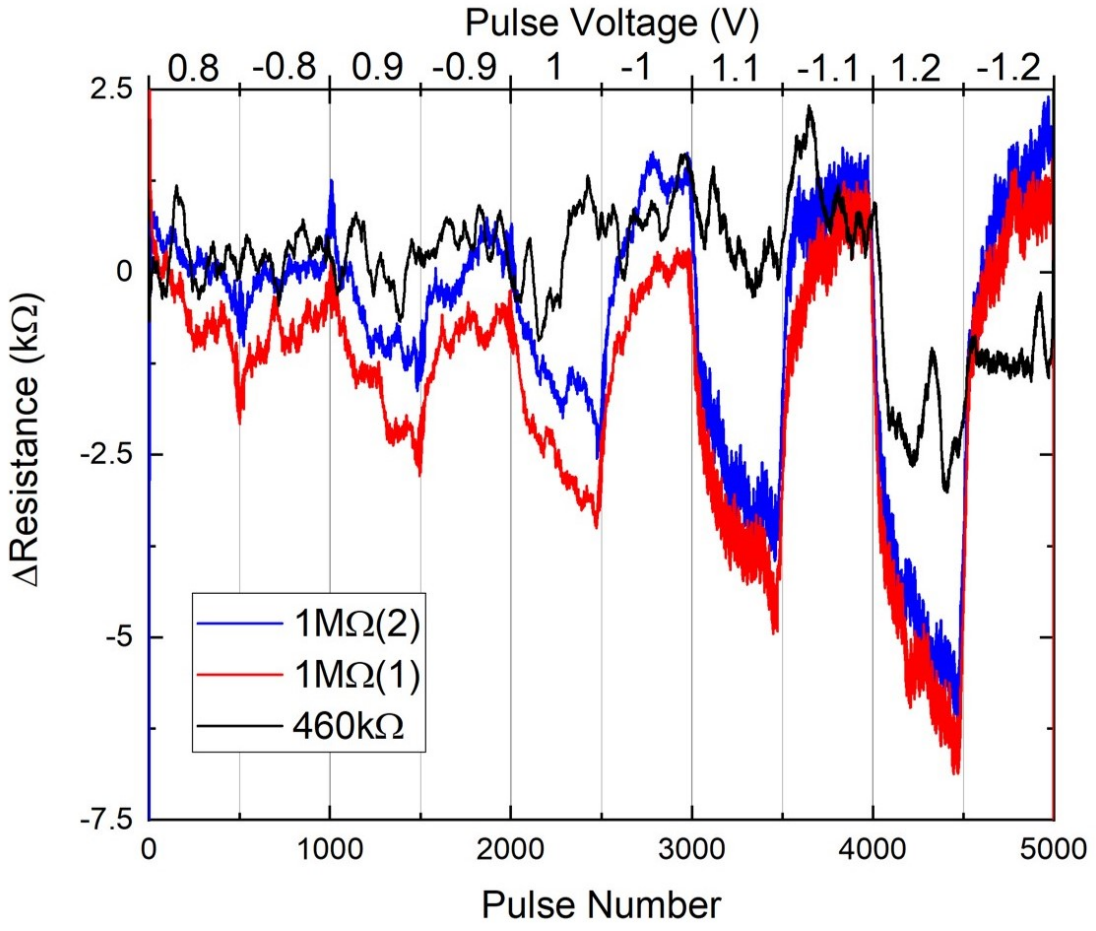

FIGURE 7.5: The switching behaviour of a device that showed recovery of resistance when exposed to high humidity over the course of 3 seperate trials. Each voltage indicated above is applied over 500 pulses of 100μs

becoming more asymmetrical as resistance increases, and the natural log current/$\sqrt{V}$ relationship becoming more linear.

7.2.2 Repeatability

In order to test if this recovery was repeatable and to attempt to ascertain what level of humidity may be required to induce the recovery, the devices which recovered were deliberately broken by aggressively switching the devices before exposing them to humidity again, in this case at room humidity (around 40%), 50%, 75% and 90%RH for a period of 3 days for each humidity. Of these devices, only one displayed an increase in resistance, seen during the 75%RH testing, however, this change occurred during a switching measurement, indicating that it was likely caused by an internal instability in the device rather than the effects of the applied humidity.

To further investigate repeatability, a dehydration of the package was attempted, by exposing the devices to temperatures of 120-140°C for a period of three hours, before

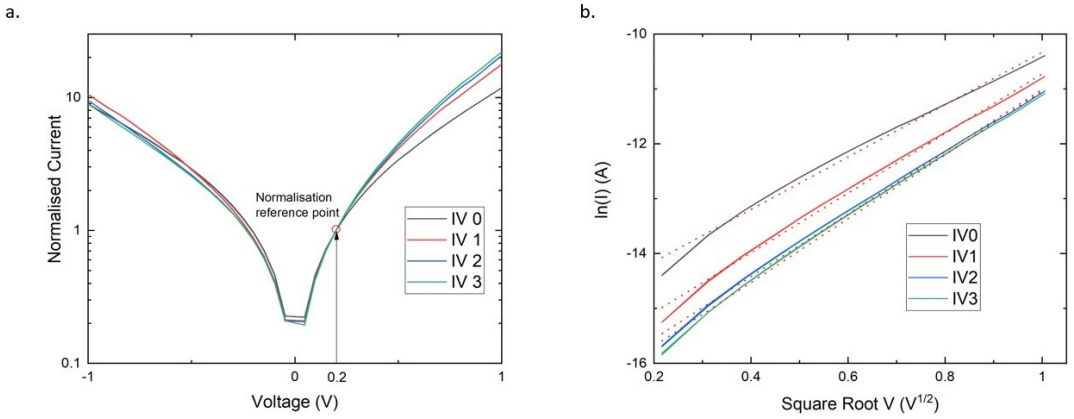

FIGURE 7.6: a. The IVs taken from a device as it recovers during humidity exposure (normalised), b. comparing the linearity of the IV curves when processed to account for Schottky characteristics. The more linear the trace, the stronger the presence of Schottky conduction.

allowing them to cool gradually back to room temperature for a period of one day. When humidity was applied to these devices, some did show increases in resistance, however, these resistances were incredibly noisy, with variations in reading up to $\pm$ 20%, indicating that the observed increases in resistance were likely due to degradation of the electrical contacts as opposed to a change within the memristor being measured, seen in figure 7.7. This was also supported by an observed drop in resistance after cleaning the contacts.

7.2.3 Future Experiments

These experiments provide strong evidence that the application of atmospheric humidity can restore the resistance, switching and IV characteristics of a previously damaged device. However, the period of time required for this effect to happen, whether we can fully rule out the impact of atmospheric oxygen and the level of humidity required for these resistance recoveries to be observed remains to be seen. The inconclusiveness of these experiments leads to the need for more careful experiments unable to be performed due to time constraints. Firstly, the possibility of atmospheric oxygen resulting in the witnessed resistance increases should be accounted for. To this end, supplying the devices with an atmosphere of nitrogen should be attempted, with this atmosphere supply being subsequently humidified. If this results in a repeat of the previously presented results, it will be confirmation that it is indeed humidity that restores these devices. Secondly, the concentration of humidity at which the restoring effects may come into play needs to be established. This is relatively simple to achieve during the testing under nitrogen atmosphere by slowly ramping the humidity applied to the devices.

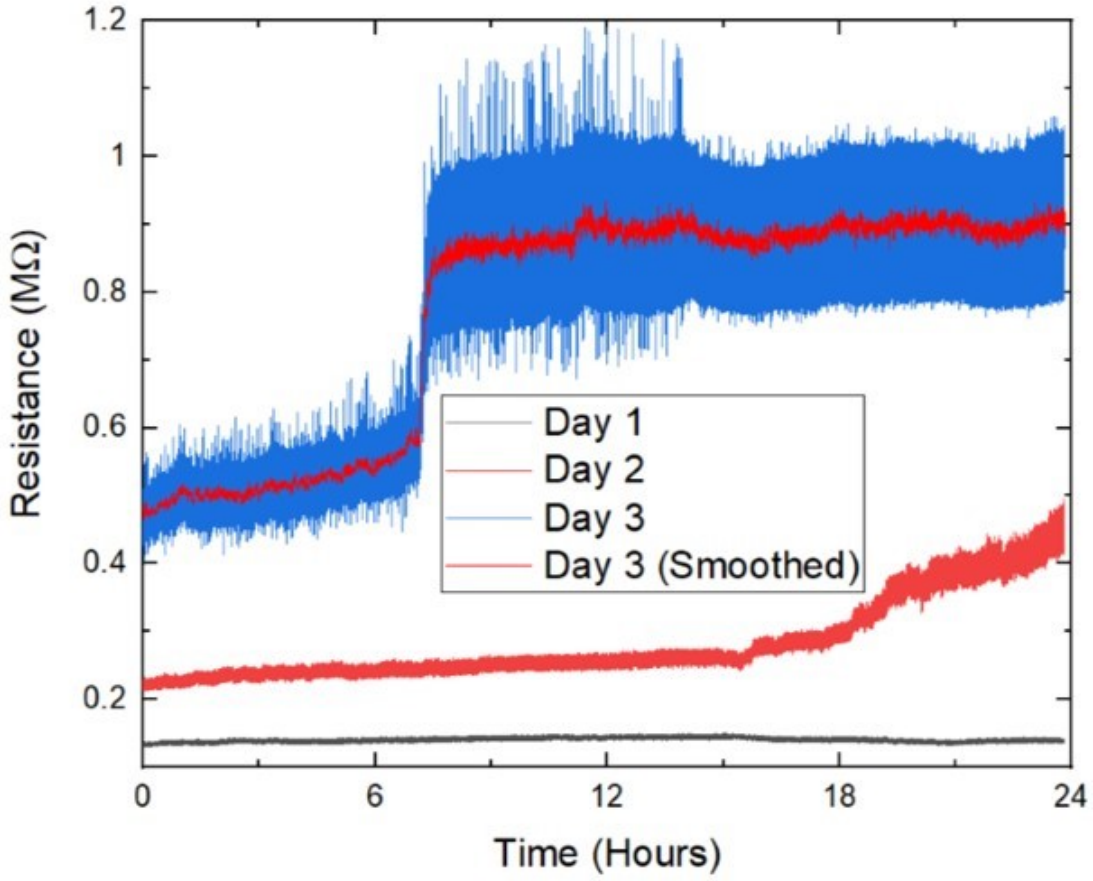

FIGURE 7.7: A device exhibiting changes in resistance during exposure to high humidity, with the noise level of the measurements indicating contact degradation as opposed to humidity induced recovery, the Day 3 data is smoothed to show the average resistance measurement.

Chapter 8

Conclusions

8.1 Temperature

8.1.1 Static Behaviour

Temperature has a strong effect on the resistivity of the TiO_2 memristors studied in the experiments, with the initial resistivity or forming level of the device having a large impact on the sensitivity of the device to temperature, as well as the proportional consistency of the measured reduction. Out of the devices tested so far, pristine devices are the most consistent and sensitive, with all the devices tested having over 60% reduction in resistivity, likely making them the most accurate if implemented as environmental temperature sensors. If switching of the sensors is desired, then having the devices in as high a resistive state as possible is desired.

It is likely that the most accurate and reliable method for measuring the reduction in resistivity (and thus the increase in temperature) of the devices is through proportional changes in resistivity, as with the devices tested in the high resistive state had a difference in resistance value of around 25%. When the results from this were converted into proportional change, this large variance was reduced to a maximum spread of 1.28% - a proportional error of 8.58% as shown in table 1. Furthermore, the proportional reduction in resistivity was within 3% of the values for the pristine devices, which had a resistivity far greater than that of the high resistive state devices (3MΩ vs. 1MΩ). This implies that by using proportional resistivity changes, a much wider range of device values can be used, making it much more suitable for real life devices.

8.1.2 Dynamic Behaviour

The magnitude of the switching of the devices is inhibited by increasing temperature, with the change in resistivity for a L1 device being reduced from around 70kΩ to 30kΩ for

an identical electrical stimulus with an increase in temperature of 60K. This reduction in electrical sensitivity is also exhibited by the threshold voltage of the device, defined as the point at which a device's resistivity is reduced by a fixed value, with the threshold of a separate L1 device increasing by 15% over the same temperature range. These effects appear to be far more visible in L1 devices compared to other operating regions due to the dominance of interface controlled conduction mechanisms compared to core material controlled conduction. These reductions in switching sensitivity are not directly proportional to the reduction in resistivity observed under static conditions, with the ratio between the HRS/LRS at higher temperatures becoming larger at the voltages used for switching these devices.

The thermal volatility model created in this work indicates that increases in temperature enhance the switching ability of the devices at lower voltages (corroborating the previous observation), but inhibit the device's switching ability at higher voltages, and the impact of temperature on the volatile behaviour is different for these devices depending upon stimulation polarity. At negative voltages, temperature was shown to increase the variability of the resistance jumps resulting from stimulation, with low voltages being relatively insensitive to temperature variations and larger jumps being slightly enhanced with increased temperature. The behaviour of the time constant in the model shows that a larger stimulation voltage results in a longer time constant. Similarly to the initial displacement behaviours, this behaviour is a linear increase with voltage and once again showed saturating behaviour for negative voltages. It was shown that the effect of temperature on the time constant for positive voltages is minimal, but has a much more significant impact was observed for negative voltages, with the value of τ dropping and becoming increasingly voltage insensitive with increases in temperature.

From these results we can see that the qualitative behaviour of these temperature dependencies varies quite heavily with different voltage polarities. With these devices, not only does temperature inhibit switching for positive polarities while enhancing switching for negative voltages at high bias values, but the enhancement/inhibition is reversed at low voltages. It is currently un-clear as to what conduction mechanisms or electrochemical processes may give rise to this mirrored behaviour, but does inform us that multiple mechanisms are present under volatile switching conditions. The difference in the impact of temperature on time constants is even more disparate, with the value of τ varying significantly with voltage polarity and showing a large difference in temperature sensitivity. Additionally, for negative voltages, at least two regions can be identified; at low voltages, we see at most a weak temperature dependence, compared to the high magnitude case. This split behaviour across polarities and the qualitatively different behaviour vs. stimulation voltage for negative polarities supports the conclusion that there are likely multiple volatility inducing mechanisms interacting with each other.

An accurate model for the static IV characteristics of a memristor has been developed, featuring two free variables that can be estimated to provide good simulated devices. The

temperature-variable relationships indicate that as temperature increases, the magnitude of the current through the device increases, while the IV curve becomes more linear. The process of modelling this also revealed that for varying device "base" resistance (its value at 0.2v without previous displacement), the curve of the IV is relatively constant.

The effects of displacement from the base resistance was also investigated and modelled, indicating that as the device is displaced further from its R0, the associated IV curve becomes less linear.

8.2 Neuron Emulation

The emulation of a homeostatic neuron has been successfully achieved, both in simulation and using physical memristors, creating a system with a stable output for steady state inputs, that produces significant changes in output spiking rate when the input changes. The memristive synapses in this system are temperature controlled, with the raw input to the system being used to control the temperature of the chamber containing the devices, with a higher total input value resulting in a higher temperature. The weight of each synapse multiplied by its input value are added to an accumulator, which produces a spike at the output upon reaching a threshold value, after which, the accumulator is reset. Increasing the temperature of the synapses decreases their corresponding weights, reducing the output spiking rate. This allows for the simulation of homeostasis to be performed. This function ignores constant inputs while providing a change in output upon a change in input, with the polarity of the output change matching the change in input. The output spiking rate is held at a constant rate by the balance of temperature and input strength. The change in input strength then results in a time delayed temperature change of the synapses, with the thermal inertia of the system resulting in a strong change in output. The change in input strength results in the temperature of the chamber balancing with the weights of the synapses once again to bring the output back to the baseline spiking rate. This concept works across a variety of input patterns, in both polarities of input change, showing the system versatility as well as resilience of the presented approach.

8.3 Humidity

It has been demonstrated that atmospheric humidity has little to no impact on the functionality of the devices studied in this work, however, promising effects were observed in some devices held at high humidity for extended periods of time. Several devices were observed to display significant increases in resistance, starting after around six hours of exposure to a 90% relative humidity air. These changes in resistance also corresponded with the restoration of functionality to some previously broken devices, indicating that

this methodology could be utilised for the purposes of making the electroforming of sensitive devices a higher yield endeavour. It is likely that these resistance changes are due to the re-oxidation of conductive filaments within the device. Within these resistance increases, three different behaviours were observed, a gradual linear increase, an exponential increase, and a sudden, large jump. This indicates the possibility of different modes of resistance change, a general bulk material oxidation, the thinning of a metallic filament and the disconnecting of a conductive filament. This area of study requires more thorough investigation in order to confirm these results, firstly by eliminating the possibility of these resistance changes being possibly the result of atmospheric oxygen rather than humidity, which could be confirmed by utilising an inert gas (nitrogen) as the medium through which the humidity would be applied. During this experiment, the concentration of moisture in the atmosphere should be gradually ramped up, in order to test if there is a humidity threshold at which these effects are triggered.

Appendix A

Derivations

Derivation for equation 4.2:

$$I = AT^2 e^{-\frac{\phi_{B0}-\alpha\sqrt{V}}{kT}} = AT^2 e^{-\frac{\phi_{App}}{kT}} \tag{A.1}$$

$$\frac{I}{T^2} = Ae^{\frac{\phi_{App}}{kT}} \tag{A.2}$$

$$ln(\frac{I}{T^2}) = ln(A)\frac{\phi_{App}}{kT} \tag{A.3}$$

Plotting $ln(I/T^2)$ against 1000/T leads to right hand side becoming:

$$ln(A)\frac{1000}{k}\phi_{App} \tag{A.4}$$

Where A and k are constant, leading to the gradient being the apparent barrier height.

Derivation for equation 4.3:

$$I = AT^2 e^{-\frac{\phi_{B0}-\alpha\sqrt{V}}{kT}} = AT^2 e^{-\frac{\phi_{App}}{kT}} \tag{A.5}$$

$$R = \frac{V}{I} = \frac{V_{R0}}{AT^2 e^{-\frac{\phi_{App}}{kT}}} = A^* T^{-2} e^{\frac{\phi_{App}}{kT}} \tag{A.6}$$

Differentiate with respect to $\frac{dR}{d\phi_{App}}$:

$$dR = A^* T^{-2} d\big(e^{\frac{\phi_{App}}{kT}}\big) d\phi_{App} = A^* T^{-2} e^{\frac{\phi_{App}}{kT}} \frac{1}{kT} d\phi_{App} \tag{A.7}$$

$$dR = A^{**} T^{-3} e^{\frac{\phi_{App}}{kT}} d\phi_{App} \tag{A.8}$$

Appendix B

Neuron Emulation Script

```
%%% Simulated homoeostatic neuron %%%

%%Initialisations and declarations
%System size parameters.
N = 25; %No. of synapses in neuron. FREE
T = 6000; %No. of time steps to run simulation for. FREE

%%linear ramp options
Linoption = 0;
Lmin = 1;
Lmax = 1;
LinInc = Lmin:(1/T)*Lmax:Lmax;

%Working arrays.
pattern = zeros(N,T); %Probabilities of a spike at any given moment in time.
input = zeros(N,T); %Input vector N at time T.
RSstd = zeros(N,1); %Weights at standard T.
RS = zeros(N,T); %RS matrix - just initialise and the next time-steps are computed automatically.
weights = zeros(N,T); %Weight matrix - automatically computed.
output = zeros(1,T); %Output vector.

%Mapping RS to weights - always linear.
Rmin = 1; %Minimum RS. Anything <Rmin is mapped to w=0. FIXED
Rmax = 15; %Max. RS. Anything >Rmax is mapped to w=1. FIXED

%Neural accumulator
INtot = 0; %Combined weighted input.
K = 30/N; %Input-to-accumulator multiplier. FREE
Acc = zeros(T,1); %Neuron membrane potential/accumulator.
Leak = 0.5; %Leakage parameter for neural accumulator. FREE
Ath = 100; %Accumulator size, or threshold.

%Thermal accumulator
TPower = 1; %Power to thermal control Range: 0-1.
TK = 6; %Thermal gain: full input changes T by TK in 1x time-step. FREE
TAcc = zeros(T,1); %Thermal state variable (T).
TAcc(1,1) = 25;
Tss = 25; %Steady-state temperature. FREE
Tleak = 0.037; %Thermal leakage towards Tss. FIXED

%Thermal function - keep linear. (Tss is baseline).
TRSc = -0.014; %Thermal coefficient of RS. FIXED
TResistor(1,1) = 25; %Resistor start temp
TDeltaR = 0.005; %Maximum T change per second

t=1;

%% Initial state generator
% Specity initial RS matrix.
RSstd = 12*ones(N,1);
RS(:,1) = (RSstd(:) + RSstd(:)*TRSc*(TAcc(t) - Tss));
```

```
%% Input pattern generator
if Linoption == 1
    for t=1:1:T
        pattern(:,t) = LinInc(t);
    end

else
    for t=1:1:T
        pattern(:,t) = 0.15;
    end
    for t=1:1:floor(3*T/4)
        pattern(:,t) = 0.25;
    end
    for t=1:1:floor(T/2)
        pattern(:,t) = 0.15;
    end
    for t=1:1:floor(T/4)
        pattern(:,t) = 0.05;
    end
end

%% Operation

for t= 1:1:T-1 %Sweep time.
    input(:,t) = (rand(N,1)<=pattern(:,t)); %Generate (binary) input.

    %Compute weights
    weights(RS(:,t)<Rmin,t) = 0; %Clear undersaturated weights.
    weights(RS(:,t)>Rmax,t) = 1; %Clear oversaturated weights.
    weights(RS(:,t)>=Rmin & RS(:,t)<=Rmax,t) = (RS(RS(:,t)>=Rmin & RS(:,t)<=Rmax,t)-Rmin)/(Rmax-Rmin); %Compute non-saturated weights.

    INtot = sum(weights(:,t))*sum(input(:,t)); %Compute combined, weighted input.
    Acc(t) = Acc(t) + INtot*K; %Update neural accumulator

    %%% Neural signalling segment %%%
    %If spiking conditions are met, emit spike.
    if Acc(t) > Ath
        output(t) = 1;
        Acc(t) = Acc(t) - Ath; %Decrease the accumulator.
    end

    Acc(t+1) = Acc(t)*(1-Leak); %Apply leakage.

    %%% Thermal signalling segment %%%
    %TAcc(t) = TAcc(t) + INtot*TK; %Update thermal accumulator.
    TResistor(t+1) = TResistor(t)+(TAcc(t)-TResistor(t))*TDeltaR; %Update resistor temperature
    TAcc(t) = TAcc(t)+ (TK*TPower*sum(input(:,t))/N); %Update thermal accumulator
    RS(:,(t+1)) = (RSstd(:) + RSstd(:)*TRSc*(TResistor(t) - Tss)); %Update RSs according to thermal function.
    TAcc(t+1) = TAcc(t) - (TAcc(t)-Tss)*Tleak; %Apply leakage.



end
```

Appendix C

Contributions

C.1 Journal Papers

"Thermal Effects on Initial Volatile Response and Relaxation Dynamics of Resistive RAM Devices", **T. Abbey**, C. Giotis, A. Serb, S. Stathopoulos and T. Prodromakis, in IEEE Electron Device Letters, vol. 43, no. 3, pp. 386-389, March 2022, doi: 10.1109/LED.2022.3145620.

"Emulating homoeostatic effects with metal-oxide memristors T-dependence", **T. Abbey**, A. Serb, S. Stathopoulos, L. Michalas, T. Prodromakis, Out for review, arXiv:2110.04102

"Compact Modeling of the Switching Dynamics and Temperature Dependencies in TiO_x-Based Memristors—Part I: Behavioral Model", D. Vaidya, S. Kothari, **T. Abbey**, A. Khiat, S. Stathopoulos, L. Michalas, A. Serb, T. Prodromakis, in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 4877-4884, Oct. 2021, doi: 10.1109/TED.2021.3101996.

"Compact Modeling of the Switching Dynamics and Temperature Dependencies in TiO_x Memristors—Part II: Physics-Based Model", D. Vaidya, S. Kothari, **T. Abbey**, A. Khiat, S. Stathopoulos, L. Michalas, A. Serb, T. Prodromakis, in IEEE Transactions on Electron Devices, vol. 68, no. 10, pp. 4885-4890, Oct. 2021, doi: 10.1109/TED.2021.3102002.

"Conduction channel configuration controlled digital and analog response in TiO2-based inorganic memristive artificial synapses", F.Simanjuntak, C. Hsu, **T. Abbey**, L. Chang, S. Rajasekaran, T. Prodromakis, T. Tseng, in APL Materials, vol 9, no. 12, pp. 121103, Dec. 2021, doi: 10.1063/5.0067302.

"Monitoring PSA levels as chemical state-variables in metal-oxide memristors", I. Tzouvadaki, S. Stathopoulos, **T. Abbey**, L. Michalas, T. Prodromakis, Sci Rep 10, 15281 (2020), doi: 10.1038/s41598-020-71962-3.

C.2 Conference Papers

"An Embedded Environmental Control Micro-chamber System for RRAM Memristor Characterisation", **T. Abbey**, A. Serb, N. Vasilakis, L. Michalas, A. Khiat, S. Stathopoulos, T. Prodromakis, 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 2018, pp. 1-4, doi: 10.1109/ISCAS.2018.8351673.

C.3 Misc. Contributions

"Live Demonstration: An Embedded Environmental Control Micro-chamber System for RRAM Memristor Characterisation", **T. Abbey**, A. Serb, N. Vasilakis, L. Michalas, A. Khiat, S. Stathopoulos, T. Prodromakis, 2018 IEEE International Symposium on Circuits and Systems (ISCAS), 2018, pp. 1-1, doi: 10.1109/ISCAS.2018.8351845, Memrisys 2018.

"A Temperature Dependant Static IV Model for Au/TiO_2/Pt ReRAM Devices", **T. Abbey**, A. Serb, L. Michalas, A. Khiat, S. Stathopoulos, T. Prodromakis, 2019 Memrisys.

"The Impact of Forming on Conduction in Au/TiO_2/Pt ReRAM Devices", **T. Abbey**, L. Michalas, A. Khiat, S. Stathopoulos, T. Prodromakis, 2019 Memrisys.

"High-Density Digital RRAM-based Memory with Bit-line Compute Capability", S. Agwa, Y. Pan, **T. Abbey**, A. Serb, T. Prodromakis, 2022 IEEE International Symposium on Circuits and Systems (ISCAS), 2022.

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