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Om Kumar Prasad,[1] Sridhar Chandrasekaran,[2] Chin-Han Chung,[1,a)] Kow-Ming Chang,[3] and Firman Mangasa Simanjuntak[4,a)]

AFFILIATIONS

[1]International College of Semiconductor Technology, National Yang-Ming Chiao Tung University, Hsinchu 30010, Taiwan
[2]Center for System Design, Department of Electronics and Communication Engineering, Chennai Institute of Technology, Chennai 600069, India
[3]Department of Electronics Engineering and Institute of Electronics, National Yang-Ming Chiao Tung University, Hsinchu 30010, Taiwan
[4]School of Electronics and Computer Science, University of Southampton, Southampton SO17 1BJ, United Kingdom

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[a)]**Authors to whom correspondence should be addressed:** king@nycu.edu.tw and f.m.simanjuntak@soton.ac.uk

ABSTRACT

The effect of annealing on the switching characteristics of memristor devices cannot be overlooked because the thermal process can exhibit both positive and negative effects on the performance of the devices. We investigated the switching behavior of TaO_x-based memristors (electrochemical metallization cell type, ECM) that were Ar-ambient annealed under two conditions, with and without the active electrode. We found a high concentration of metal species in the TaO_x films, even in the device where the TaO_x was annealed without the active top electrode. This indicates that the properties of the annealed films encourage the diffusion of metal species in the oxide. We suggest that the increase in non-lattice oxygen (by 4.1%, indicating a higher concentration of V_o defects) after the annealing process plays a role in this phenomenon. In addition, the concentration of metal species that exist prior to the switching activation as well as the structure of the conducting bridge determines the switching stability of the devices. The device that annealed before top electrode deposition shows the worst stability; conversely, the device that annealed after top electrode deposition has the best coefficient of variation of the LRS and HRS which is 4.69% and 78.8%, respectively. Electrical and materials analyses were conducted to understand this phenomenon. This study provides insight into the compatibility of ECM in CMOS post-processing.

Electrochemical metallization memory (ECM) is one of the important memory technologies for future electronics.[1] ECM has several advantages, such as low power consumption, high switching speed, and multilevel programmable potential.[2] ECM cell consists of a metal/insulator/metal (MIM) two-terminal configuration that relies on the drift of metal species of an active electrode to form a conducting bridge connecting both electrodes.[3,4] Several choices of metal, such as Ag,[5] Cu,[6] In,[7] or Te,[8] can be used as the metal cation source. The formation of the bridge brings the ECM to a low resistance state (LRS, On) and conversely, the rupture of the bridge leads to a high resistance state (HRS, Off).[9] In-circuit integration,[10] ECM needs to be stacked with a selective device to avoid the sneak-path in crossbar configurations, usually in the form of a 1-transistor 1-ECM configuration which is fabricated at the back end of the line process (BEOL),[11] where the ECM is manufactured on top of a source or drain[12] and is followed with a post-thermal process (annealing). The sneak path current in a high-density array hinders the realization of large-scale crossbar arrays and 3D interconnected array.[13] Nevertheless, before we can integrate the ECM device and address the sneak path issue, we need to make sure the devices are compatible with the BEOL process. There has been a lot of effort to decrease the annealing temperature at the BEOL, a post-annealing temperature of higher than 450 °C may result in a

detrimental effect on the standard CMOS wafers,[14] and it is suggested that the temperature should be below 400 °C.[15] Nevertheless, this study found that even a post-annealing with a low thermal budget (as low as 300 °C) still affects the switching characteristics of ECM devices.

This work studied the impact of such an annealing process on the switching behavior of Ni/TaO_x/TaN ECM cells. Ni has widely been used in the mainstream CMOS technology as a source/drain contact material,[16] but it is rarely investigated in ECM development as compared to other active metals.[17–19] Tantalum oxide (TaO_x) is one of the potential materials for memristor devices, as suggested by Samsung Electronics.[20] Nevertheless, this study has found that this material is sensitive to the processing temperature. This Letter explains the physics behind the annealing effects and provides insight into the TaO_x-based ECM device development employing Ni metal and its compatibility with the BEOL process.

A 200-nm thick TaN bottom electrode was deposited onto the Ti-coated SiO_2 wafer at 180 °C; the sputtering power, working pressure, and Ar ambient flow were 300 W, 5 mTorr, and 100 sccm, respectively. Then, a TaO_x film was deposited at room temperature with sputtering power, working pressure, and Ar/O_2 ambient flow of 300 W, 5 mTorr, and 100/50 sccm, respectively. Hereafter, 80-nm thick Ni top electrodes with a diameter of 125 μm were deposited at room temperature and patterned using a metal shadow mask; the sputtering power, pressure, and Ar ambient flow of 300 W, 5 mTorr, and 100 sccm, respectively. All films were deposited using the DC sputtering technique. Figure 1(a) shows the schematic of the Ni/TaO_x/TaN memristor stack, denoted as S-1. An optical microscope (Olympus BH2-MJLT) and transmission electron microscope (TEM, JEOL JEM-2010F) were used to observe the top view and cross-sectional images of the fabricated devices, respectively. The cross-sectional TEM image of the Ni/TaO_x/TaN stack shows that the thickness of the TaO_x film was approximately 5 nm, as depicted in Fig. 1(b). To investigate the effect of the post-annealing process,[15,21] we annealed a TaO_x/TaN stack in Ar ambient at 300 °C for 5 min in a tube furnace (Thermo Scientific); hereafter, the Ni top electrode was deposited, and this device is denoted as S-2. For comparison, we also annealed the S-1 device (a complete Ni/TaO_x/TaN MIM structure) following the same annealing condition as S-2, this annealed device is denoted as S-3. Electrical characteristics of the devices were measured using an Agilent B1500A semiconductor parameter analyzer employing W needle probes; voltage biases were applied on the top electrode while the bottom electrode was grounded, and a current compliance (CC) of 100 μA was used to avoid permanent breakdown. The defect concentration in the TaO_x film was analyzed by using x-ray photoelectron spectroscopy (XPS, ULVAC PHI versa probe). Chemical elements across the MIM stacks were studied using a secondary ion mass spectroscopy (SIMS, ATOMIKA 4500, MA-Tek, Taiwan; the primary beam was O^{2+} with an energy of 0.5 keV, and the analysis was conducted on a 37.5 × 37.5 μm^2 square area). Surface topography and grain boundary analysis were conducted using an atomic force microscope (AFM, NT-MDT, NTEGRA).

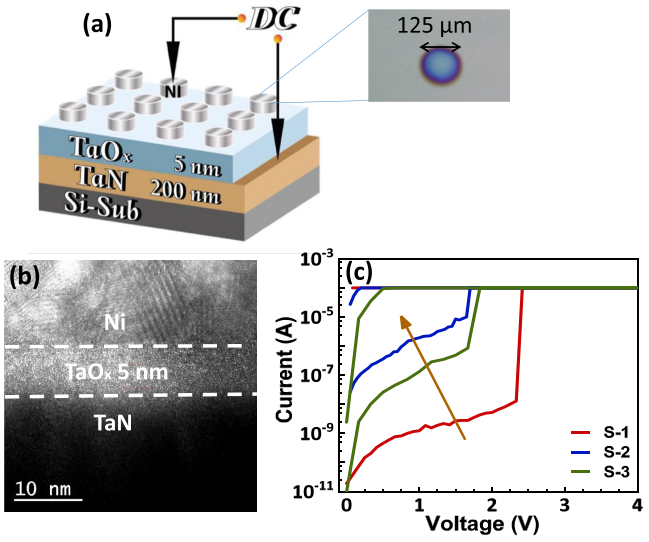

FIG. 1. (a) Schematic of the Ni/TaO_x/TaN memristor device structure. Right hand top: (a) top-view image of the fabricated devices; (b) cross-sectional TEM image of the TaO_x memristor device; and (d) forming voltages of pristine and annealed devices.

All devices require an electroforming process (pristine state to LRS state, On) to activate their switching behavior. The forming voltages (V_{FORM}) of S-1, S-2, and S-3 were 2.4, 1.8, and 1.6 V, respectively, as depicted in Fig. 1(c); the leakage current of the S-1 device prior to the electroforming was significantly lower than that of S-2 and S-3 devices, where S-2 devices had the highest leakage; the pristine resistance of the three devices are shown in Fig. S1 in the supplementary material. Hereafter, the devices could be switched from the HRS to LRS (Off, set process) employing a negative bias (V_{RESET}) of approximately −0.8, −1.8, and -2.2 V for S-1, S-2, and S-3 devices, respectively, as shown in Fig. 2. S-1, S-2, and S-3 devices can be turned back On (HRS to LRS) with a positive bias sweep (V_{SET}) of between 1.1 and 1.4 V. The switching procedure that employed an opposite polarity to switch the devices back into the HRS indicates that the Ni/TaO_x/TaN ECM had a counterclockwise bipolar switching mode; note that the devices cannot be switched using the same polarity.

All devices exhibit switching up to 100 cycles; however, the devices made with the annealing process have a smaller memory window (On/Off ratio) than S-1 devices, as depicted in Figs. 2(d) and 2(e). S-1 devices demonstrated a ratio of 83, while S-2 and S-3 devices exhibited a ratio of 17 and 28, respectively. We evaluated the LRS and HRS instabilities by conducting a statistical distribution,[22] and the result is shown in Fig. 3(a). It was found that the variation coefficient of the LRS and HRS of S-2 devices is the highest (unstable) as compared to the other devices; meanwhile, S-3 devices had the tightest distribution indicating that it has the most stable switching behavior. Nevertheless, the LRS of both S-1 and S-3 devices was stable and could be programmed to show a multilevel behavior by controlling the CC. S-1 and S-3 devices can be operated with various CC ranging from 50 to 500 μA, as shown in Figs. 3(b) and 3(c); this suggested that these devices could be programmed to have multiple LRS levels, and this capability would be useful for making high-density multi-bit data storage.[23] Note that there is no dependency between switching voltages and current compliance, see Fig. S2 in the supplementary material for details.

Based on the above-mentioned electrical measurement, the trade-offs were observed. The devices made with the annealing process (S-2 and S-3 devices) had a lower V_{FORM}, but they had a higher V_{RESET}

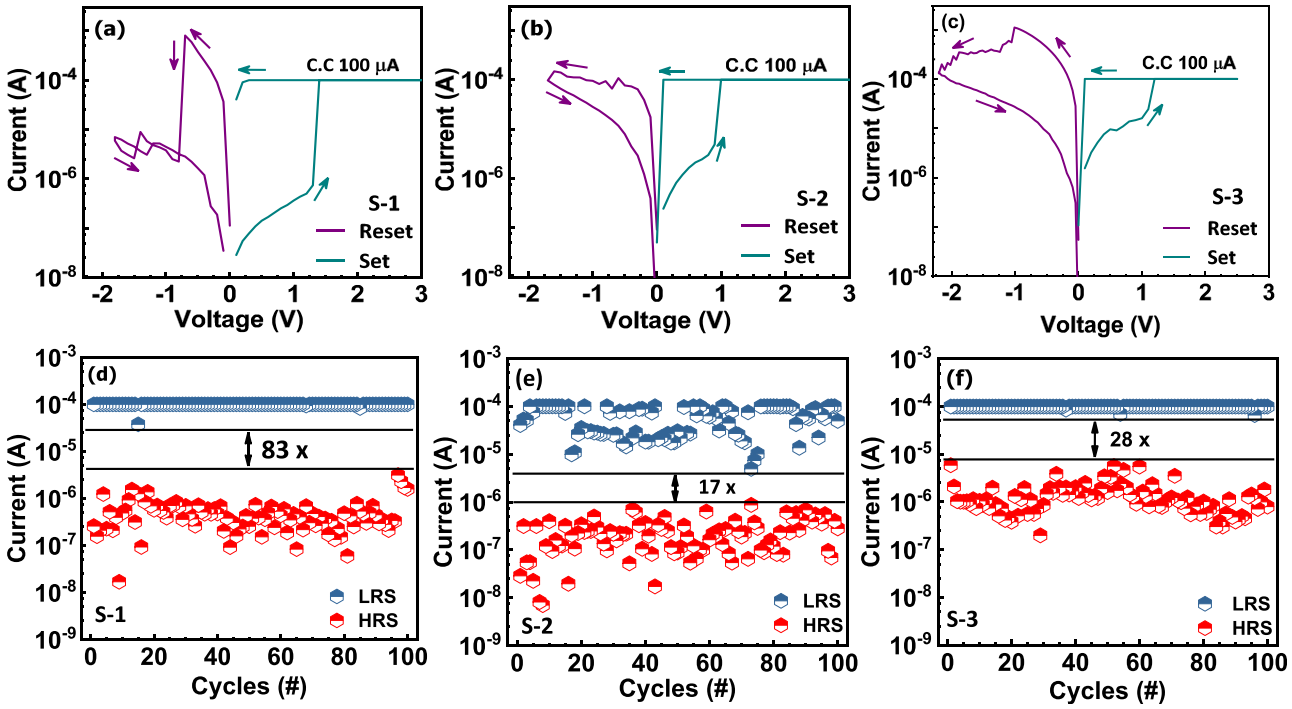

FIG. 2. (a) Typical I–V curves of the Ni/TaO_x/TaN device at (a) S-1, (b) S-2, and (c) S-3. Endurance performance of (d) S-1, (e) S-2, and (f) S-3. 0.1 V is taken as the readout voltage.

than that of the S-1 device [Figs. 1(c) and 2(a)–2(c)]; see Fig. S3 in the supplementary material for the statistical analysis of the switching voltages. On the other hand, the devices made without an annealing process had the highest On/Off ratio, yet the stability could only be improved if a complete (MIM) stack was annealed [Figs. 2(d) and 2(f)]. Material analysis was conducted to understand the physics behind the trade-off phenomenon. Figures 4(a)–4(c) show the SIMS depth profile of the Ni/TaO_x/TaN stack of S-1, S-2, and S-3, respectively; it was found that the Ni concentration in the S-2 and S-3 devices had a more gradual slope than that of S-1 devices. This indicated that the Ni could diffuse more easily into the oxide once the TaO_x film had endured an annealing process. It has been reported that the concentration of intrinsic defects, such as oxygen vacancies (V_o), in oxide films could affect the diffusion of metal ions into the films.[24] Hence, XPS spectra was analyzed the O 1s core level to evaluate the V_o concentration in the films. The O1s spectra were fitted with two Gaussian–Lorentzian peaks for the higher and lower binding energies of 530.53 (O_i) and 531.6 eV (O_{ii}),[25] which represent the lattice and non-lattice oxygens in the TaO_x film, respectively; the non-lattice is associated with the amount of V_o.[26] It was found that the non-lattice after the annealing process increased by 4.1%, indicating a higher concentration of V_o defects. The high concentration of V_o in the annealed films reduced the bulk resistivity of the films and provided a higher Ni diffusion rate [Figs. 4(d) and 4(e)] in oxygen-poor films.[27,28] Hence, this factor eased the electroforming process in the annealed devices [a reduced V_{FORM}, Fig. 1(c)]. However, some fundamental questions remain; why the V_{RESET} and On/Off ratio of the annealed devices were higher and lower, respectively, than that of S-1 device and why S-3 devices showed higher stability while the endurance of S-2 device was highly non-uniform. This study hypothesized that these phenomena could be due to the shape and number of the conducting bridges. It is known that the structure of the bridge is controlled by the microstructure of the films;[29] hence, a grain analysis was conducted employing an AFM technique to evaluate the film properties, and the result is shown in Fig. 5. It was found that the TaO_x annealed film had much larger grains than that of the as-deposited film. Most of the grains in the pristine film were just tens of nm, implying some parts of the films could have even smaller grains or no grains at all (amorphous), which cannot be detected beyond the calculation capability of our system. Henceforth, the analysis indicated that the film was a mixture of crystalline and amorphous.

Grain boundaries (GBs) provide pathways for ionic diffusion in the polycrystalline film.[30] The films with small grains have a high number of boundaries, and theoretically, the conducting bridge will form a branched structure.[31,32] However, if an amorphous region exists in the film, in the case of S-1 film, the metal ions tend to drift through the amorphous region of the film rather than the GB.[33] Therefore, it was implied that the number of bridges in S-1 devices was less than that of the annealed devices; consequently, the pristine device had a relatively moderate switching capability [Fig. 3(a)], and the fewer number of branches that needed to be ruptured during the reset process resulted in a higher On/Off ratio [Fig. 2(d)]. The rupture of a single or small number of bridges tends to be assisted by a Joule heating effect, which results in a low V_{RESET} with an abrupt current fall during the reset process.[34] On the other hand, the annealed devices had more crystalline regions facilitating the formation of a high number of bridges (or branched structure) in the devices that led to the

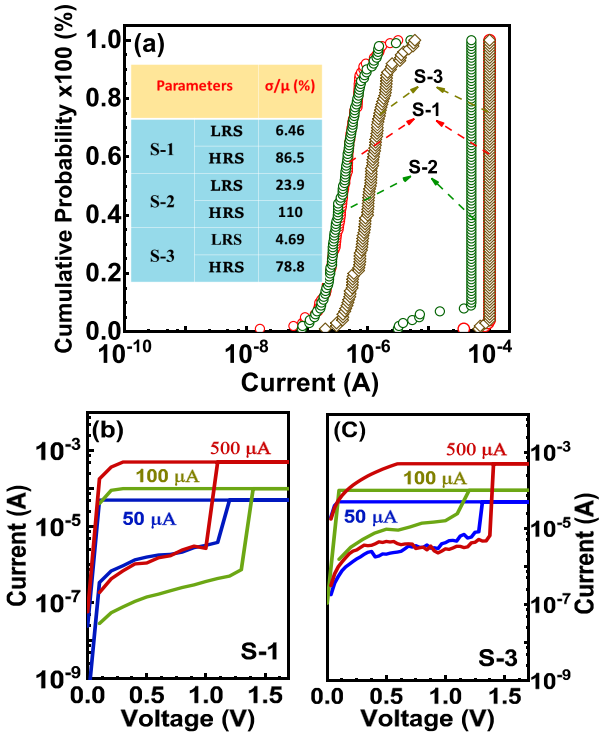

FIG. 3. (a) Statistical distribution of HRS and LRS of the fabricated devices. (b) S-1 and (c) S-3 devices operated at various current compliance.

requirement of high energy (high V_{RESET}) to rupture all bridges at the top interface [Figs. 2(b) and 2(c)]. The rupture of the bridges/branches could occur step-by-step (not a single event), leading to a gradual reset process [Figs. 2(b) and 2(c)]. Nevertheless, the Ni species in the TaO_x of the S-3 device was higher [Fig. 4(c)] since the annealing process was conducted after the top electrode (Ni) deposition, where the thermal effect facilitated the Ni diffusion during the annealing. The high concentration of the pre-existing Ni species not only eased the formation of the conducting bridge in S-3 device [Figs. 1(c) and 4(c)] but also reduced the number of bridges/branches in the TaO_x, and hence, enhanced the switching stability.

In conclusion, the effect of annealing on the resistive switching characteristics of TaO_x-based ECM has been studied. The properties of the oxide film are responsible for determining the metallic species diffusion in the film, both prior to and during the electrical programming. The switching stability of the ECM cells is dictated by two factors, such as the concentration of metallic species in the oxide film of the as-fabricated devices and the number of conducting bridges or branches involved in the set and set processes. Physical and chemical properties, such as GBs and **Vo**, determine the drift of the metallic ions which affect the structure of the bridges. This study provides valuable insight into the grain boundary engineering for making the memristor device compatible with CMOS post-processing. Device integration and practical application analysis will be conducted in our future investigation.

See the supplementary material for the additional data on pristine resistance, switching voltage at different current compliance, statistical analysis of V_{SET} and V_{RESET}, and LRS stability.

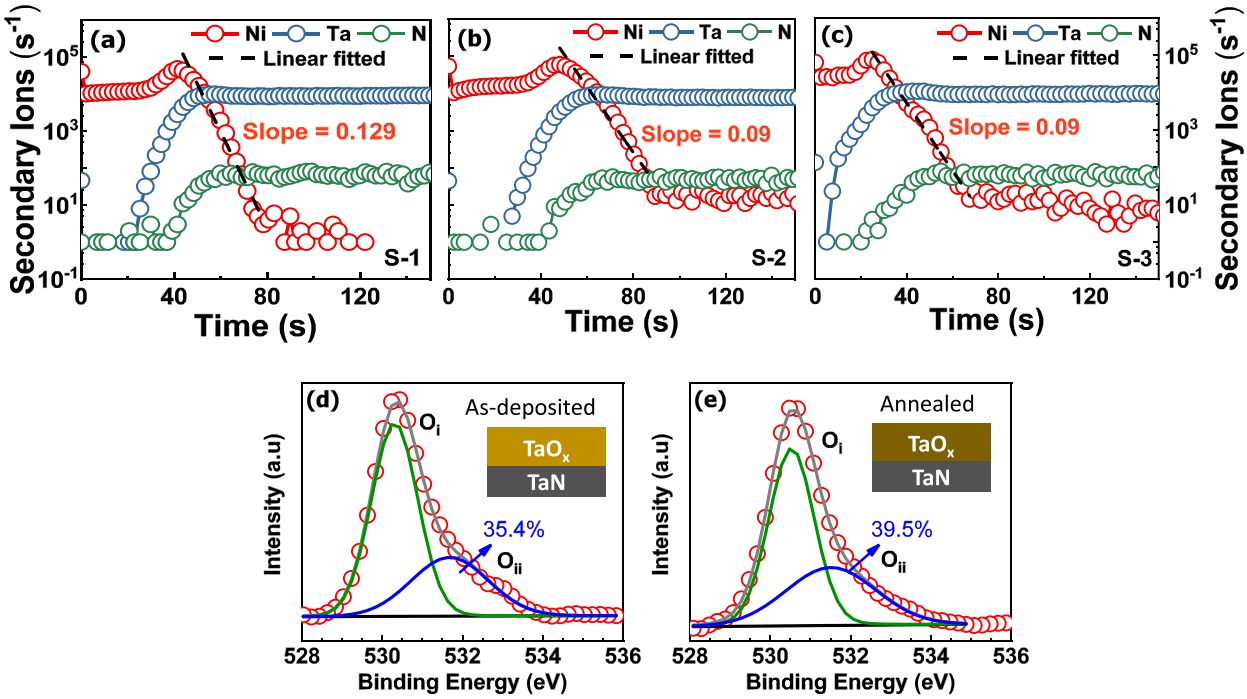

FIG. 4. SIMS depth profile of Ni/TaO_x/TaN: (a) S-1, (b) S-2, and (c) S-3. XPS spectra of O 1s core levels of TaO_x films with oxygen vacancy %: (d) before and (e) after annealing.

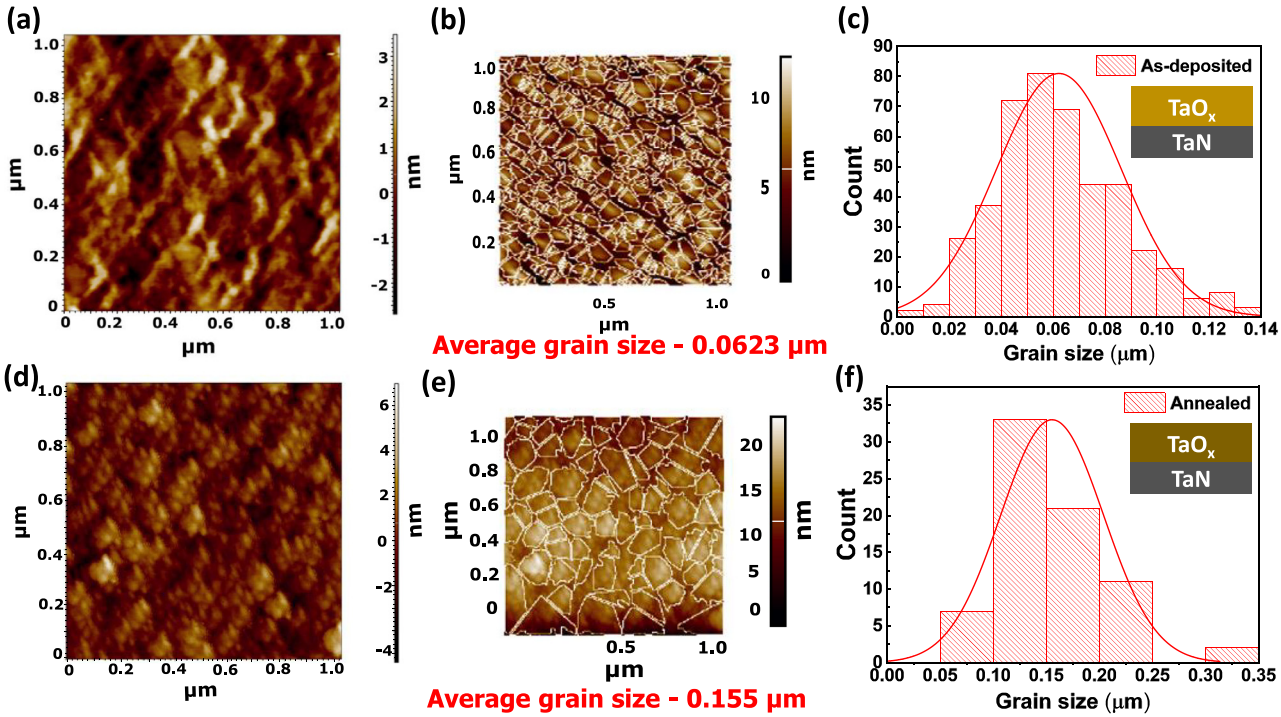

FIG. 5. AFM images of TaO_x S-1 and annealed at 300 °C. (a) and (b) Top view and grain boundary-scan image of S-1 sample; (c) histogram graph of S-1 samples; (d) and (e) top view and grain boundary-scan image of 300 °C annealed sample; and (f) histogram graph of 300 °C annealed sample.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Om Kumar Prasad: Conceptualization (lead); Formal analysis (lead); Investigation (lead); Validation (lead); Visualization (equal); Writing – original draft (lead); Writing – review & editing (lead). **Sridhar Chandrasekaran:** Conceptualization (equal); Formal analysis (equal); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal). **Chin-Han Chung:** Investigation (equal); Funding acquisition (lead); Resources (lead); Supervision (lead); Writing – review & editing (equal). Kow-Ming Chang: Supervision (equal); Resources (Supporting); Writing – review & editing (equal). **Firman Mangasa Simanjuntak:** Conceptualization (equal); Formal analysis (equal); Funding acquisition (supporting); Investigation (equal); Methodology (equal); Supervision (equal); Validation (equal); Visualization (equal); Writing – original draft (equal); Writing – review & editing (equal).

DATA AVAILABILITY

The data that support the findings of this work are available from the corresponding author upon reasonable request.

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