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UNIVERSITY OF SOUTHAMPTON

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES

Electronics and Computer Science

On the Feasibility of Using Current-based Monitors to Detect Ageing in CMOS Circuits

by

Radi Husin Ramlee

Thesis for the degree of Master of Philosophy

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ABSTRACT

FACULTY OF ENGINEERING AND PHYSICAL SCIENCES
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ON THE FEASIBILITY OF USING CURRENT-BASED MONITORS TO DETECT AGEING IN CMOS CIRCUITS

by Radi Husin Ramlee

The ageing effects have taken the attention as it shows the unavoidable sign as the device size is shrinking. Three most crucial ageing effects that are known to give threat to circuits reliability and performances are Bias-Temperature-Instability (BTI), Hot Carrier Injection (HCI) and Time-Dependent Dielectric Breakdown (TDDB). And between these ageing effects, BTI is the most prominent ageing effect than others. These effects have been reported to compromise CMOS technology in sub-100nm region that degrades the critical performance parameter, which includes the shifting of threshold voltage and degradation of the drain current. These degradations are then led to the degradation of circuit frequency, affecting the overall efficiency of the whole circuit. This phenomenon eventually shortens the lifespan of the chip to only a few years. In this report, we discuss some of the effects of BTI (particularly NBTI since it is more dominant than PBTI), focussing on the degradation of the drain current. The significance of drain current for becoming a dominant device ageing barometer is revealed. An NBTI ageing sensor is proposed based on monitoring the drain current with optimised implementation on critical gates. Based on the results simulated, the incorporation of drain current degradation as being the ageing sensor monitored parameter has significantly higher resolution in term of degradation compared to the threshold voltage degradation for the same period of stress time. This report is also discussed

on the feasibility of employing such monitoring circuit that measured drain current for ageing effects prediction mechanism.

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Declaration of Authorship

I, Radi Husin Ramlee , declare that the thesis entitled *On the Feasibility of Using Current-based Monitors to Detect Ageing in CMOS Circuits* and the work presented in the thesis are both my own, and have been generated by me as the result of my own original research. I confirm that:

- this work was done wholly or mainly while in candidature for a research degree at this University;
- where any part of this thesis has previously been submitted for a degree or any other qualification at this University or any other institution, this has been clearly stated;
- where I have consulted the published work of others, this is always clearly attributed;
- where I have quoted from the work of others, the source is always given. With the exception of such quotations, this thesis is entirely my own work;
- I have acknowledged all main sources of help;
- where the thesis is based on work done by myself jointly with others, I have made clear exactly what was done by others and what I have contributed myself;
- parts of this work have been published as listed in Section 1.4

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Nomenclature

I_{ddt}	The drain transient current
I_{ddq}	The drain quiescent current
V_{TH}	Threshold Voltage
BTI	Biased-temperature instability
NBTI	Negative Biased-temperature instability
PBTI	Positive Biased-temperature instability
HCI	hot carrier injection
TDDB	time-dependent dielectric breakdown
SPICE	Simulation Program with Integrated Circuit Emphasis
CMOS	Complementary Metal Oxide Semiconductor
MOSRA	MOS Reliability Analysis
BICS	Built-In Current Sensor
SEU	Single Event Upset
SET	Single Event Transient
CPU	Central Processing Unit
ALU	Arithmetic Logic Unit
RISC	Reduced Instruction Set Computer
CP	Critical path
ISCAS89	International Symposium on Circuits and Systems 89
CPD	Current Peak Detector
PWM	Pulse-Width Modulated
C2T	Current-to-Time
CPD	Current Peak Detector

Chapter 1

Introduction

In the recent years of circuit designs, reliability has turned into a significant design constraint for on-chip systems [24]. Years after years, the size of Complementary Metal Oxide Semiconductor (CMOS) transistors were scaled-down, doubled in every year, bringing new concerns for reliable circuit or system. As the transistor size decreases every year, it brings a new challenge in the field of circuit reliability.

Ageing effects are becoming more distinctive than before. Three leading ageing effects are Negative-Bias Temperature-Instability (NBTI), Hot Carrier Injection (HCI) and Time-Dependent Dielectric Breakdown (TDDB) [41][64][24]. NBTI however, is the most prominent compared to the other two effects which have been reported in [35][51][81][89]. These emerging reliability challenges could potentially reduce the lifespan of CMOS circuits by a few years if no adequate measurements are taken [70]. NBTI ageing effect is proved to shift threshold voltage gradually by more than a few hundreds of Volts (0 mV to 50 mV) [88][18] which eventually reduce the drain current [18][97], performance degradation (delays) of digital circuits [23][48] and affecting the signal noise margin (SNM) on SRAM cells [86][99][40].

With the risk of NBTI on PMOS transistor in sub-100 nm region, techniques for predicting and monitoring the wear-out effect has been attracting a significant amount of interest in recent years. In the present, research interest on monitoring

aspect of ageing has been focussing on monitoring the delay due to the feasibility by measuring the latency of a signal produced from digital circuits.

Current-based monitoring circuit for ageing is known to be unintrusive to the circuit. The Drain current is proof in this thesis to be affected more in resolution compared to delay degradation. The implementation of Build-in-current-sensor (BICS) type of monitoring added some more advantages for the current-based monitor. BICS-type sensor circuit can be implemented in post design of the circuit because of the simple approach of tapping to the device bulk without having to meddle in the process designing the actual function of circuit-under-test. However, with the advancement of CMOS process technology, the design for current-based monitor might become not feasible to be deployed.

1.1 Research Motivation

System-level detection requires a sophisticated sensing and processing operation. Sensitive device parameters such as the frequency, delay, and leakage current can be manipulated to estimate the circuit ageing long before it happens. There are significant numbers of literature discussing on how ageing effect detection was implemented by monitoring the device ageing parameters, but still, only a few that exploits the drain current to predict end-of-lifetime of a CMOS circuit [53][45][49][21][93].

The drain current has been demonstrated to be the signature of the peak power supply and the quiescent current, which correlate to threshold voltage [36][76]. This method will be adapting a sequence of circuitry beginning with capturing the current with Built-In-Current Sensor (BICS), detecting the changes in the current's value and converting them on later stage into digital forms of information. This research aims to develop a counterpart of the ageing effect sensing mechanism that will anticipate ageing by having closed monitoring of circuits drain current degradation.

Ageing effect detection has focused more on the increased in the circuit's delay because it has a direct relationship with the shift in threshold voltage. With the addition of an auxiliary circuit that could monitor other parameter affected by ageing effect could provide more accuracy to the ageing prediction. The main motivation comes from the principles for device failure that is often benchmarked at 50mV shift or $\delta I_{ds}/I_{ds} \sim 10\%$ [35][97].

For circuits below 90nm, it is easy for the drain saturation current to violate that 10% margin value. Thus, by monitoring the drain current not to exceed the failure margin percentile is possible. The drain current based monitoring will deploy BICS to mirror the current and reading the current will be a smart way because it will have no interruption on the circuit functionality. This non-intrusive characteristic of detection mechanism gives it an advantage over the delay degradation approach. Since it is only working as an auxiliary circuit for ageing monitoring, it will not cause any penalties to the circuit under observation, aside from the area overhead and perhaps the power consumed by the monitoring circuits.

With the obtained data, the extrapolated data can be produced to predict the ageing of a circuit from the degradation of drain current. In this report, the proposed ageing sensor mechanism is predicted to enhance the capabilities of the monitoring ageing effect by not only relying on the delay monitoring technique but with the reduction of the drain current in digital circuits.

1.2 Research Aims

The research aims of this study are as follows:

1. to design an auxiliary detection system based on the drain current degradation of gates on the critical path,
2. to design a sensory circuit that would translate the feed signal from each the drain current sensor that will be translated into 'error signal',

3. to analyse the feasibility of deploying current-based monitor to detect ageing.

1.3 Research Contributions

This thesis combined important features that made up an ageing effect detection mechanism in the CMOS circuit, as follows:

1. An NBTI-aware detection mechanism based on drain current degradation to predict ageing circuits.
2. A non-intrusive ageing effect detection to the circuit under observation.
3. Implementation strategies for small current detection for various ageing CMOS circuits in 32nm and 45nm CMOS technologies.

1.4 Published Papers

From the research work presented in this thesis, the following papers have been published:

- **Ramlee, R. H.**, & Zwolinski, M. (2016, September). Using I ddt current degradation to monitor ageing in CMOS circuits. In *Power and Timing Modeling, Optimization and Simulation (PATMOS), 2016 26th International Workshop* on (pp. 200-204). IEEE.

1.5 Thesis Organization

This chapter has described the research motivation and the reasons why drain saturation current has become a significant ageing parameter as the CMOS

process technology is going beyond 100nm. An ageing sensor mechanism based on monitoring the drain saturation current is proposed.

Chapter 2 presents an overview of the ageing effects in general. This chapter covers all three main ageing effect in brief. The disadvantages, challenges and literature review of drain current testing in the CMOS circuit are also mentioned.

Chapter 3 outlines a more detail discussion regarding NBTI and its model. Static, dynamic and long-term degradation modelling are discussed in detail. NBTI-aware degradation monitoring is mentioned, and the recovery techniques in the literature are discussed. Finally, works of literature about drain current degradation in NBTI are presented.

Chapter 4 describes the current degradation measurement in terms of its implementation as an on-chip or off-chip test. The bulk-BICS is discussed in detail for its feasibility implementation and how it could be implemented for ageing effects prediction.

Chapter 5 presents the implementation of NBTI ageing sensor based on the drain current degradation. The method mentioned has a high potential in producing an optimum monitoring sensor with a low area overhead. These results are crucial and a testament to how worth is drain saturation current in NBTI ageing degradation.

Chapter 6 discussed in detail regarding the I_{ddt} current degradation in various CMOS circuits. The circuits considered in this chapter are ranging from basic gates up to a complex Arithmetic Logic Unit circuit of OpenRISC1200 processor.

Chapter 7 concludes the research work and highlights the potential future work of this project.

Chapter 2

Reliability in CMOS Technology and Ageing Effects

CMOS technology is a very promising and robust for integrated circuits and well-known for its reliability, integration capability, low power consumption, and high-frequency operation. From time to time, researchers and foundries around the world have been working to scale down the size of CMOS devices. The improvement can be seen with the increase of operating speed, circuit density, much lower power consumption as it enters into the sub-micron region, CMOS technology started to show some critical reliability issues. It has been pointed out that NBTI, HCI and TDDB are three significant wear-out effects that caused the reliability issue.

2.1 Ageing Effects

Ageing effects are a major reliability concern for digital and analogue circuits in sub-100 nm CMOS technologies [70]. Persistent oxide thickness downscale has led to an increase in electric fields in MOSFET devices, tunnelling effects, and other temporal and ambiguous failures. Bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), and hot carriers injection (HCI)

are the most critical ageing effects related that have been identified to cause the transistor to aged drastically through time during operation.

2.1.1 Negative Bias Temperature-Instability

BTI is known to degrade the transistor threshold voltage, thus reducing the circuit performances in general. Two types of BTI; Negative-Bias Temperature-Instability (NBTI) and Positive-Bias Temperature-Instability (PBTI). For the NBTI, the stress condition is when the transistor is negative-biased, which is a common biasing situation in PMOS transistors. Complementary to NBTI, the stress condition of PBTI is when the transistor is positive-biased, which is a common biasing situation in NMOS transistors.

However, for NBTI, has been singled out as the most prominent effect compared between these two BTI ageing effects [55]. Figure 2.1 shows the dominance NBTI over PBTI for all four cases studied in the literature [55]. The critical BTI ageing effect is observed to be NBTI for PMOS device, followed by NBTI for NMOS and finally PBTI for both devices.

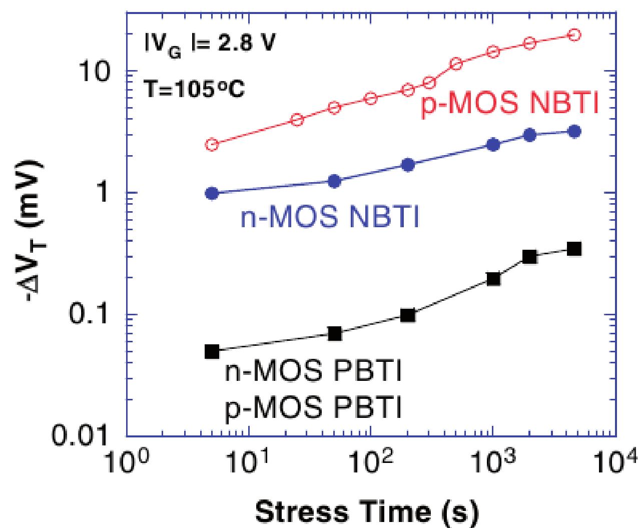


Figure 2.1: Threshold voltage (V_{th}) shifts for PMOS and NMOS for both positive and negative gate bias [55]

Negative Bias Temperature-Instability (NBTI) is a related ageing mechanism that leads to a decrease in current in P-type CMOS devices as transistors wearing out. NBTI is temperature-induced and is typical to shift the PMOS transistor threshold voltage and to degrade its drain current. PMOS transistors are susceptible to this ageing mechanism at strong negative bias with preeminent temperature [80].

The NBTI effect has been recognized as the primary parametric ageing mechanism in modern and dense integrated circuits. NBTI occurs due to the generation of the interface traps along the silicon-oxide (Si-SiO2) interface when a negative voltage is applied to the PMOS gate (stress) [35][75][87][62].

The stress stage of NBTI happens because of the chemical reaction involving the electrical field, holes and temperature [76]. These reactions of electrons affect the magnitude of the threshold voltage of the PMOS transistors to increase through time [97]. An annealing stage (removal of the stress when $V_{gs} = 0$) can reduce some of the interface traps and relaxed the stress condition, resulting in partial recovery.

As more traps are formed, the threshold voltage increase and resulting in poor drive current until the circuit eventually comes to a total failure. NBTI leads to the circuit wear-out by lowering noise margin, increasing delays, creating mismatches in some circuits and shorten the device lifetime [26][48]. A detailed overview will be discussed later in the next chapter.

Recent studies have been conducted verifying that this phenomenon can increase the absolute threshold voltage by more than 50mV over ten years, resulting in a circuit's performance degradation of more than 20% [21]. NBTI is shown not to be frequency-dependent as well [53]. For deep sub-micron region CMOS devices, the nanometre-sized transistors have been observed to have NBTI as a stochastic ageing effect rather than a definite failure [36][24].

2.1.1.1 Physical Mechanism of NBTI

The generation of the interface states and the diffusion of the hydrogen can be modelled by the RD system [41]. Two processes occur according to the RD system, which is local reaction and diffusion. Equation 2.1 represents the rate of interface state generation due to NBTI.

$$\frac{dN_{it}}{dt} = \underbrace{k_F(N_0 - N_{it})}_{generation} - \underbrace{K_R N_H(0) N_{it}}_{annealing} \tag{2.1}$$

where :

- N_0 - the initial number of Si-H bonds,
- N_{it} - the number of interface states,
- k_F - the rate constant of broken bond creation,
- $N_H(0)$ – the number of hydrogen atoms at the Si/SiO2 interface,
- k_R - the rate constant of reverse annealing.

This diffusion of stress can also be healed or reversed. This is described by the second term of the equation (annealing part). This recovery effect is a distinct attribute of NBTI, where the process of Si-H bond breaking is able to recover when the stress is removed.

The creation of interface states is limited by the diffusion (or drift) of hydrogen. This is modelled by Equation 2.2:

$$\frac{dN_{it}}{dt} = -D_H \frac{dN_H}{dx} + N_H \cdot \mu_H \cdot E_{ox} \tag{2.2}$$

where:

- D_H - the diffusion coefficient,

- μ_H - the mobility in Hydrogen,
- E_{ox} - the electrical field across the oxide.

k_R and D_H are temperature-dependent while k_F depends on the temperature and electrical field. Because of the electrical field dependency for K_F, an electrical field is required during the generation of interface states but not for the annealing and the diffusion. With some assumptions made, Equations 2.1 and 2.2 can be solved together to produce Equation 2.3.

$$N_{it}(t) = \sqrt{\frac{k_F N_0}{2k_R}}(D_H t)^{\frac{1}{4}} \tag{2.3}$$

Assumptions are made by [41] that Nit is much smaller than N_0. The time dependence for H diffusion is 1/4, and for H_2 diffusion, it is 1/6. Equation 2.4 represents the dependence of N_{it} on V_{th} [35].

$$V_{th} \propto -\frac{qN_{it}(\Phi_S)}{C_{ox}} \tag{2.4}$$

where :

- C_{ox} - the oxide capacitance,
- Φ_S - the surface potential

With the increase in the number of interface states, Nit, the absolute value of Vth is increased. Other device parameters are also going to change due to Vth as stated in Equation 2.5 and 2.6

$$I_d \propto (V_{gs} - Vth)^2 \tag{2.5}$$

$$g_m \propto (V_{gs} - Vth) \tag{2.6}$$

The drain current Id is important for the performance of digital circuits and the transconductance gm is relevant for analogue circuits.

2.1.2 Hot Carrier Injection

The second most critical ageing, HCI, is the results of high current across the transistor channel during switching that leads some carriers to accidentally injected into the gate oxide. This then could shift the threshold voltage value of the transistor.

Hot Carrier Injection (HCI) occurs as carriers moving along the channel of a transistor and experience impact ionization at the end of the channel closed to the drain in saturation mode [70].

During switching, the changes of states from non-conducting to conducting of a transistor, highly energized charges flow through the channel between the source and the drain. A small percentage of hot electrons channel from the source to the drain may acquire enough kinetic energy that could enable them to overcome the insulator potential barrier and penetrate the gate oxide layer. This is possible when these hot carriers received enough kinetic energy from the channel electric field and consequently redirected their movement directly towards the gate oxide layer as depicted in Figure 2.2

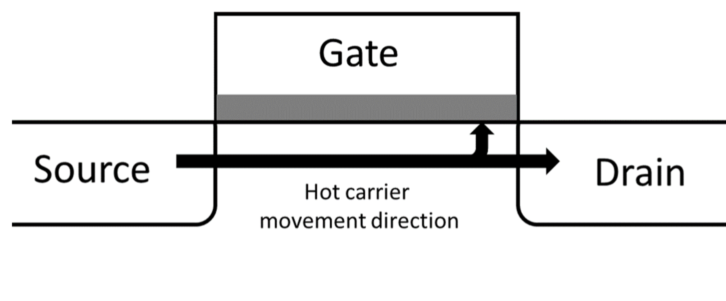


Figure 2.2: Charges injection into the gate oxide layer during HCI occurs

Carriers gaining high energy (deem as 'hot carrier') from intense electric fields. The impact might occur either on the interface within the layer, or even on the

sidewall of the gate oxide. As transistor switching, these carriers are injected and trapped into the device gate-oxide, changing the IV characteristic of the device, hence decreasing drain current in NMOS transistor. As the VLSI fabrication technologies are advancing, they primarily focus on the reduction of

In principle, the phenomenon of charge-trapping cause threshold voltage to shift, degrading channel mobility (consequently, degrade high-frequency switching) [62], and create a signal mismatch in some matched circuits. The HCI affects the transistor's operating speed as circuit wearing out as well. In the logic circuit, the problem is worst for fast-rising input logic gates. At high temperatures, this ageing effect worsens but decelerates as the temperature decrease [27][80]. It is possible to analyse HCI by simulation, by manipulating input signal rise time together with the stage electrical effort [80]. It has been shown by literatures that HCI is not frequency independent, but temperature-dependent [43][52].

2.1.3 Time-Dependent Dielectric Breakdown

Time-Dependent Dielectric Breakdown (TDDB) is known to create a bridge/channel through the gate oxide in the transistor that promotes electrical current conduction path between through the insulating layer - a dielectric breakdown. It has the potential to introduce a significant increment in static power consumption, which then could affect the speed and DC voltage levels of a CMOS circuit.

TDDB happen as large electric fields present at the gate-oxide of a nanometre CMOS device, a formation of a conducting path through the oxide layer to the substrate. This phenomenon will eventually cause the oxide layer to damage, making it impossible to control the gate voltage [70]. With the decreasing of the gate oxide thickness as the device becomes smaller every year (less than 2 nm)[20], the dielectric exhibits higher tunnelling currents and these influence the device reliability [27][83]. Since the gate oxide thickness is the main cause for this

wear-out effect, the current CMOS device technologies are more susceptible to TDDB compared to its predecessor.

The elimination of the insulating property of the gate oxide is directly proportional to the oxide thickness and the electric field magnitude. Thinner oxides need less aligned defects to get through its thickness, and higher electrical fields encourage the defects acceleration. Figure 2.3 illustrates the dependence of the breakdown process (increase in the leakage current) for different applied gate voltage. From the figure, it can be observed that the device is more prone to suffer dielectric breakdown with higher gate voltage [1].

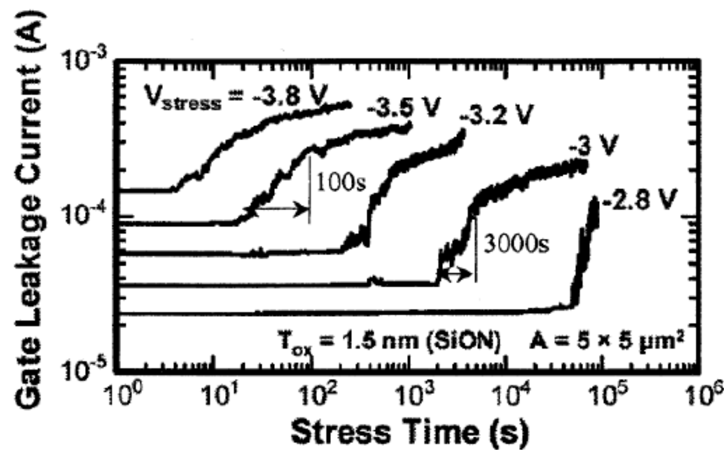


Figure 2.3: TDDB progress breakdown, with different V_{stress} during oxide breakdown [1]

There are two categories of the breakdown in TDDB. The first category is hard-breakdown, is the most harmful mode, which provokes a complete loss of the oxide dielectric properties. The dielectric will severely be destroyed, short-circuiting the gate, and completely make the oxide layer in conducting mode.

For deep sub-micron CMOS devices, hard-breakdown can be preceded by the second category of breakdown; soft-breakdown. The soft-breakdown is what has become a critical concern in recent years. It has been observed as a temporal loss of the dielectric properties and gate oxide current's magnitude and noise. The oxide layer's insulation properties will degrade aggressively because of the

drain current by approximately 10% degradation and shift in threshold voltage by approximately 75mV [30][18].

2.2 The Disadvantages of Ageing Effects

Penalties such as the shift in threshold voltage, the increases in leakage currents and degradation in performance are among the long list of drawbacks resulting from the ageing effects [70]. The wear-out effect does not only affect the digital but analogue circuits as well. When an analogue circuit subjected to high voltages, the threshold voltage of the transistor can shift significantly during the lifetime of a chip.

For a matched circuit in an analogue system, symmetrical or identical stress will also present a potential time-dependent mismatch to the circuit. In a matched circuit such as comparators, the uneven wear-out will produce a time-dependent mismatch that degrades the offset and other circuit parameters. Even though the performance of an analogue circuit does not directly affect by a small transistor variation, this failure could threats the whole functionality of a circuit.

In digital circuits (sequential circuit), ageing will cause changes in oscillation frequency, power consumption and large variations on the degradation in flip-flops. This type of drawback usually measured by observing the degradation in ring oscillator frequency before, during and after stress condition.

It has been reported in [87], that the ring oscillator is working fine with a slight frequency reduction under controlled NBTI stress environment. The power consumption and integrity have also been observed to have an impact on NBTI wear-out. A small decline in power consumption is explained as the consequences of oscillator frequency reduction. The decrease in power consumption will have a ripple effect throughout the entire circuit due to the sharing of the same power supply. Thus, degradation in power consumption from any part of the circuit

caused by ageing effects should not be taken lightly because it will affect other parts of the circuits.

In literature [90], a study has been conducted to evaluate the degradation in delays of five different static flip-flop topologies under NBTI, HCI and TDDB influences. It is found that higher degradation happens under NBTI and HCI effects. TDDB however, caused an increase in static power dissipation by order of magnitude.

The ageing effect does not only a problem on physical or device abstraction level. In the system level, ageing affects system performances and other unpredictable issues. The effects are much worse in system-level where every circuit are cascaded and connected to others circuitry [29]. A ripple-effect type of failures is something to be considered.

2.3 Challenges in Ageing Effects Simulation

Equations and models describing the ageing effects degradation such as NBTI in literature [26] have transistor-level parameters such as threshold voltage (V_{th}), gate-source voltage (V_{gs}), gate-oxide capacitance (C_{ox}), gate-oxide thickness (t_{ox}) and etc. (Detailed explanation of these models will be discussed in Chapter 3). The ageing effects analysis requires circuits to undergo SPICE simulation that runs on the electrical level based on mathematical analysis. However, on gate-level abstraction there are gates, flip-flops and latches which are understood as a functional block rather than the transistor-level perspective, and these parameters are unknown on gate-level processes.

Thus, the challenge is to do ageing simulation and estimation of electrical level parameters for a gate-level abstraction circuit. On the other hand, the functional block of gates, flip-flops and latches have different transistor structure, making it much possible, but hard to implement in the present VLSI design framework. Apart from these problems, a gate-level simulation has the potential to solve it as shown in [16][63], in a propagation delay degradation domain. Gate-level

simulation is still the preferred approach because of its simpler abstraction models, and the speed is significantly faster.

2.4 Drain Current Testing in CMOS Devices

There are two types of drain current can be measured during the operation of a circuit. The first type is the quiescent supply current, a current that flows when the device is in a stable state. Ideally, when a CMOS circuit is in a stable state, the drive current for the device is equal to zero. However, due to the physics of junction between two different types of extrinsic semiconductor, the quiescent supply current will not remain zero for real-life applications. Thus, in general, it is also known to be a combination of leakage and bias currents.

The second type of drain current is the transient supply current. This part of the supply current is called the switching or transient current. It is regenerated for each switching of the circuits and ideally does not degrade because it sourced directly from the power supply. Using the switching or transient current as a source of information to differentiate between good and defective circuits has only recently been the subject of various research activities.

Transient supply current (I_{DDT}) testing is a test technique based on measuring the dynamic supply current of the device under test. I_{DDT} measurements are done when the circuit under test is active. The test decision is based on combining one or more parameter extracted from the current waveform produced from the test. Typical parameters that are observed are the peak values, pulse with values (pulses with negligible value are ignored), the average current or the charge related to a period of the current waveform. The latter parameter provides a lot of information regarding the proper switching of the circuit observed.

For any CMOS circuits, drain current is the current that flows through PMOS transistor and NMOS networks, which is also known as the power supply current. An open connection exists through both networks only during the logic transition

happens, making the transient current to flow. Since the transient current is in a pulse form and is part of the power supply current, the peak of transient current can also be called peak power supply current.

Taking a CMOS inverter circuit as an example, the peak power supply current with both transistor's operating regions is depicted in Figure 2.4. In theory, the maximum amount of current flows from V_{dd} to the ground occurs when both transistors are in the saturation region ($V_{in} = V_{out} = V_{dd}/2$) as shown in Region III in Figure 2.4. At this moment, drain current and power dissipation will be at the maximum.

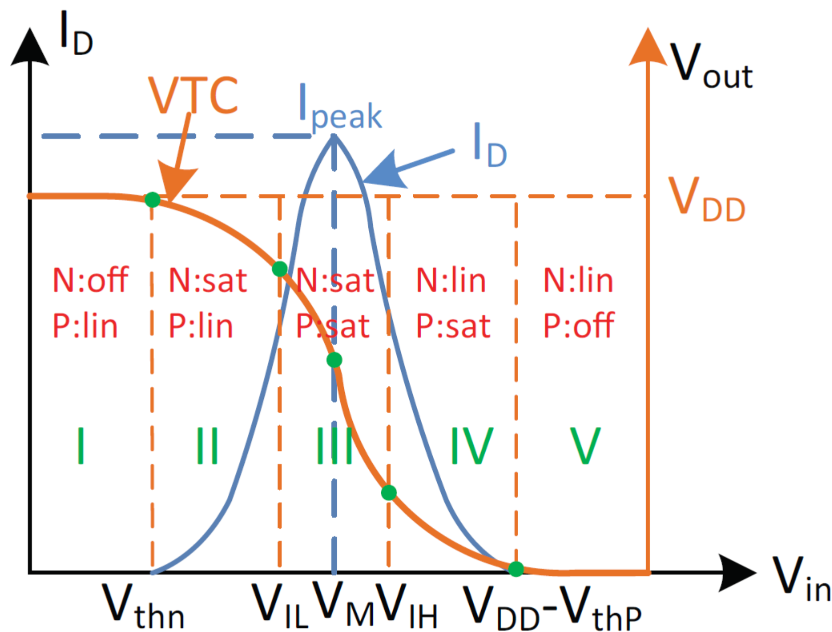


Figure 2.4: A typical VTC and power supply current of a CMOS inverter circuit [62].

This fundamental idea is applicable to any CMOS circuit. Thus, speculation can be made that for a fresh circuit (has yet to undergo an ageing process) should have the highest value of drain current. The peak value of transient current in an ideal case should remain the same all the time. For an ageing transistor where a shift in threshold voltage happens, it will affect the drain current, hence reducing it during the state transition. The reduction in transient currents brings down the

peak value of the transient current. In other words, any changes to the peak value of transient current could be an indicator of ageing.

A detailed approach will be discussed later in the next chapter on the implementation of ageing detection by monitoring the drain current degradation and how crucial it has been, as when the supply voltage is reduced from 1.5 Volts to 0.8 Volts (In general, the reduction of the supply voltage (V_{dd}) is proportional to the reduction in threshold voltage (V_{th}) and transistor sizes).

2.5 Ageing Effect Models and Simulations

In this section, the three ageing effects mathematical model (BTI, HCI and TDDB) from works of literature will be discussed briefly.

2.5.1 NBTI, HCI & TDDB models

The NBTI predictive models are based on Reaction-Diffusion (R-D) model [51][26] has two types of stress; which is static stress and dynamic stress. NBTI occurrence in PMOS is more prominent [55] compared to PBTI. The model for this ageing effect will be discussed in detail in the next chapter.

A developed analytical compact model for HCI has been developed in literature [12] for FinFETs technology. The reported model has taken into account quantum mechanical effects, short-channel effects (SCEs) and other secondary effects, such as mobility degradation, saturation velocity and series resistance.

$$\%\Delta V_t \propto \Big[-1.5V^{-1}\Big(V_{ds} - (V_{gs} - V_t)\Big)\Big] \tag{2.7}$$

From Equation 2.7, as the V_t degradation increases follow closely to the increment of V_{gt}. This is due to the increase of the carrier density, reaching the most damaging condition at $V_{stress} = V_{ds} = V_{gs}$ in agreement with previous literature [52][70][62].

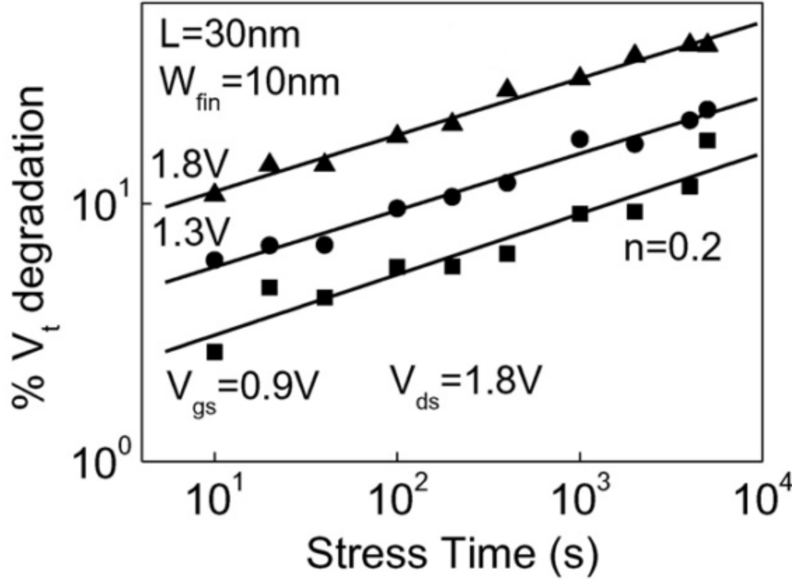


Figure 2.5: Normalized $\%\Delta V_t$ shift with stress time for stress bias voltages $V_{ds} = 1.8V$ and $V_{gs} = 0.9, 1.3 and 1.8V$ [12]

A plotted Equation 2.7 is depicted in Figure 2.5. The figure shows the $\%\Delta V_t$ shift with stress time for stress bias voltages $V_{ds} = 1.8V$ and $V_{gs} = 0.9, 1.3 and 1.8V$ for a FinFET device ($L = 30nm, W_{fin} = 10nm$). The same HCI model can be implemented for bulk n-MOSFETs with some modification value for the interface trap generation mechanism as pointed out in [11].

$$I_g = \Delta N(t_1) ln \Big[\frac{1 + exp(\beta(E - \alpha))}{1 + exp(\beta E)}\Big] \tag{2.8}$$

Equation 2.8 is the compact TDDB models [59] that correlated by discrete random trap generation where $\Delta N(t)$ is the trap number and E is the trap energy ($E = 1.4 \pm 0.15eV$). This compact model improves the short term errors in conventional TDDB model (t^n model), which only excel in the long-term data but not the

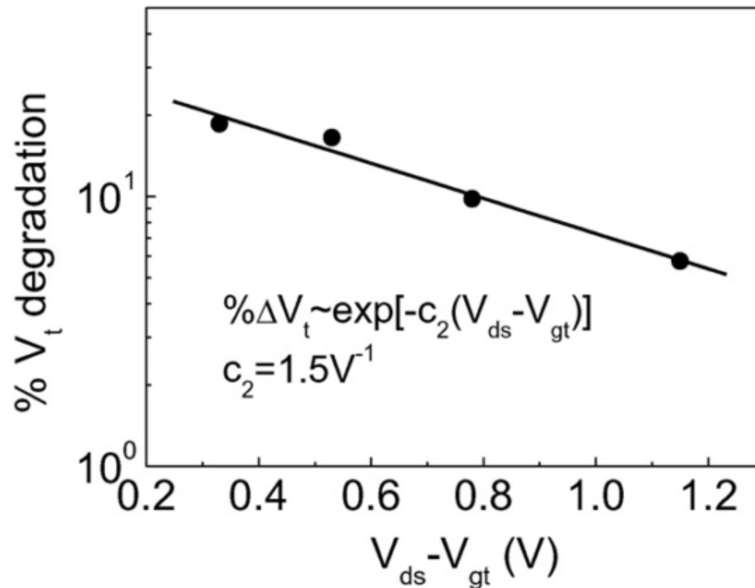


Figure 2.6: Normalized $\%\Delta V_{th}$ shift on stress voltage V_{ds}–V_{gt} for stress time 100 s [12]

short term. While t_1 is the time when the first time TDDB happens, the random increase in trap number ($\Delta N(t_1)$) are considered.

Equation 2.8 is best understood by illustrated in Figure 2.7. The dependence of leakage current I_g due to the dielectric breakdown is sensitive to the changes of N and E as also pointed out in [58][57]. It can be observed from Figure 2.7 that leakage current if proportionally changes with N and exponentially to E as modelled in Equation 2.8.

2.5.2 Simulation in SPICE

A Simulation Program with Integrated Circuit Emphasis (SPICE) tool is used to simulate the ageing effects on the CMOS circuitry. HSPICE by Synopsys has an ageing effect simulator called MOS Device Ageing Analysis (MOSRA) that incorporate the HCI and BTI conditions for circuit analysis [54].

A MOSRA model is used for its capability of simulating actual device degradation information based on the amount of electrical stress in term of voltages, currents,

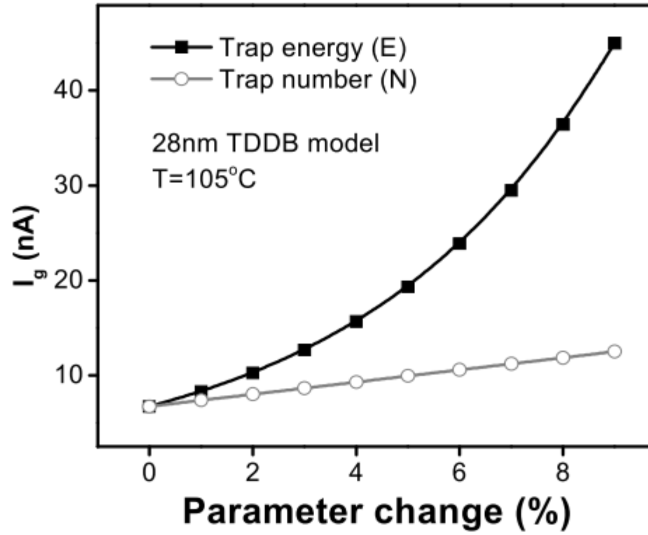


Figure 2.7: Dependence of I_g on different parameters E and N percentage [59]

temperatures as well as device geometries. These are handy when one has an existed technology libraries and working circuit designs and need to have an ageing effects simulation to be done.

For BTI model, HSPICE MOSRA considered two principal physical mechanisms; effect of interface traps on ageing and effects of traps deep inside the dielectric layer as represented by Equation 2.9and Equation 2.10.

$$\Delta V_{TH,IT} \sim exp\Big(-\frac{E_a}{K \cdot T}\Big) \cdot \Big[\frac{\epsilon}{t_{ox}}(V_{gs} - V_{TH})\Big]^{TITCE} \cdot exp\Big[TITFD \cdot E(V_{gs}, V_{ds})\Big] \cdot t^{NIT} \tag{2.9}$$

$$\Delta V_{TH,OT} \sim exp\Bigg[-\frac{TOTFD + \frac{TOTTD}{T}}{E(V_{gs}, V_{ds})}\Bigg] \cdot t^{NOT} \tag{2.10}$$

where:

- $E(V_{gs}, V_{ds})$:- strength of the electric field of dielectrics.

- TITCE:- inversion charge exponent for interface trap inducing threshold voltage degradation.
- TITFD:- oxide electric field dependence for interface trap inducing threshold voltage degradation.
- TOTFD:- oxide electric field dependent component for oxide trap inducing threshold voltage degradation.
- TOTTD:- temperature-dependent component for oxide trap inducing threshold voltage degradation

In MOSRA, dynamic BTI also considered by deploying dynamic BTI model as Equation 2.11. This model took the stress stimulus duty cycle into account during the stress test. These enable researches to incorporate BTI partial recovery process of BTI and such consideration is essential to observe the degradation dynamically. This is depicted in Figure 2.8.

$$\Delta V_{TH,AC} = TTD0 \cdot \Delta V_{TH} \cdot exp(-TDCD \cdot g) \tag{2.11}$$

where:

- g:- models the effect of duty cycle.
- TDCD:- duty cycle dependent exponent for transient degradation of threshold voltage

The dynamic BTI effect illustrated in Figure 2.8 is for PMOS device. The annealing process can be observed to happen during positive gate voltage which relaxed the PMOS, having the ΔI_{Dsat} to recover from degradation and continue to degrade when the device is being stressed during stress stage (negative gate voltage bias).

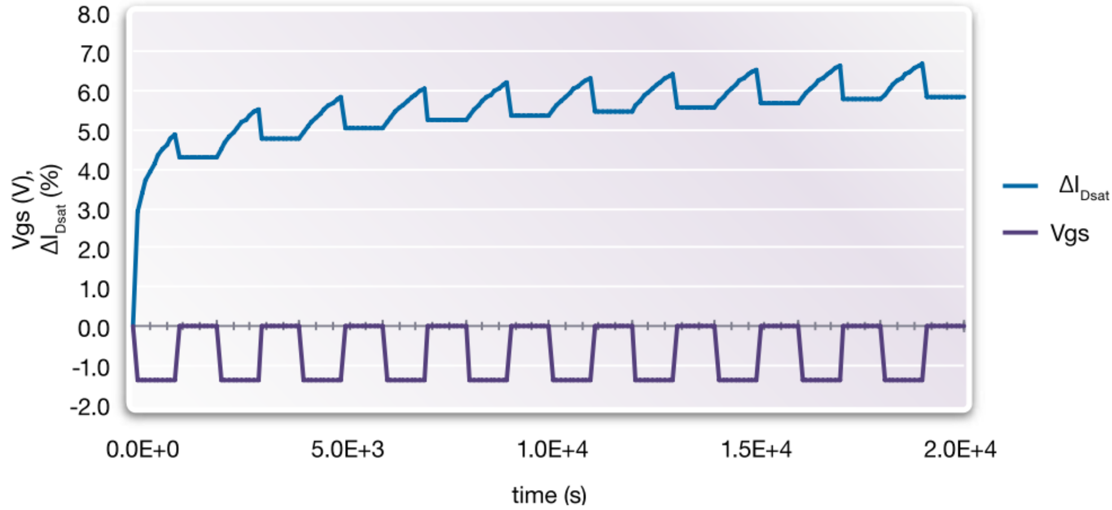


Figure 2.8: Dynamic BTI simulation by HSPICE MOSRA [54]

HSPICE MOSRA also incorporated HCI model for its ageing analysis tool. The HCI module used by MOSRA considered over a wide range of parameters such as drain, gate, substrate biases, and over different temperatures.

$$\Delta V_{TH,HCI} \sim THCI1 \cdot \left(\frac{I_{ds}}{W_{eff}}\right)^{TDCE} \cdot \left(\frac{I_{sub}}{I_{ds}}\right)^{TDII} + THCI2 \cdot V_{ds}^{TDVD} \cdot \left(\frac{I_{ds}}{W_{eff}}\right)^{TDID} \tag{2.12}$$

Equation 2.12 is the HCI model used by MOSRA. This model is based on the Lucky Electron Model [50], as shown in the first term of the equation, as discussed in the previous chapter.

The MOSRA implementation flow has both pre-stress simulation phase and the post-stress simulation phase. During the pre-stress simulation phase, the HSPICE computes the electrical stress of user-selected MOSFETs in the circuit, based on the MOSRA models. Through the transient analysis, duration of stress predefine by the user will use the calculated electrical simulation condition, and the stress value will then be integrated over the circuits simulation time. The result of the integration is then extrapolated to calculate the total stress after a finite time of circuit operation.

During the post-stress phase, the degradation of device characteristics translated to performance degradation parameters. The post-stress MOSRA simulation phase can be based on a different type of analysis such as DC analysis, AC analysis and transient analysis. These two-phase is best described in Figure 2.9 [61].

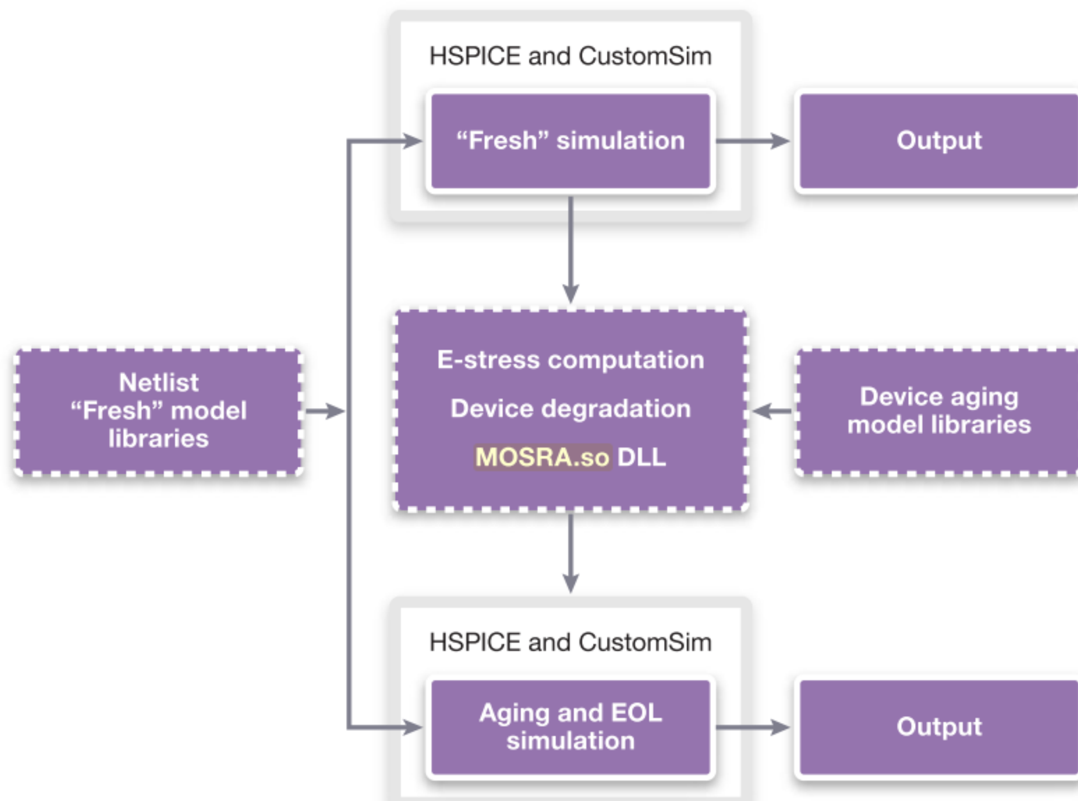


Figure 2.9: MOSRA Simulation flow.

2.5.3 Process, Voltage and Temperature Variations

Process, Voltage and Temperature (PVT) Variations is an analytical simulation to model variations in Process, Voltage and Temperature. It is a good practice to do PVT variations for testing the reliability of a circuit design that would have all these three variations.

Process variation is to statistically simulate the deviation that could happen during the process of manufacturing of any die. While manufacturing any die, it has been seen that the dies that are having a minimal deviation from the model are

considered to be accurate in their process values. However, in the process of manufacturing, there is always some die tend to deviate from this process value. Even though the deviation is not big, this variation could contribute to the timing for the circuit, hence affect the integrity and performance of the circuit. The drain current of a MOS transistor in the saturation region is represented in Equation 2.13, and the linear region is express in Equation 2.14 [101]. The channel length (L) represents the process value. K' is the transconductance parameter and V_{th} is the threshold voltage. If the temperature and voltage values are to be constant, any variations happen in channel length could affect the current, hence affect the delay and timing for the circuit. Due to process variations, K', V_{th} and other parameters may vary, and affect the drain current and junction capacitances. As discussed in International Technology Roadmap for Semiconductors (ITRS), in a typical situation of process variation, an increase in K' is accompanied by a decrease in V_{th}.

$$I_D = \frac{K'}{2}\frac{W}{L}(V_{GS} - V_{th})^2 \tag{2.13}$$

$$I_D = \frac{K'}{2}\frac{W}{L}\left[(V_{GS} - V_{th}) - \frac{V_{DS}}{2}\right] V_{DS} \tag{2.14}$$

For Voltage Variation, deviation in supply voltage is simulated for the circuit under test. Ideally, the power source is expected to be constant at all time, but in reality, that is not what happens. The output voltage of the voltage regulator might not be a constant over a period of time. For example, an expected voltage regulator/supply is to give 1.2V throughout the years, but after four years, its voltage dropped down to 1.08V or increased up to 1.32V. This is when the need to model Voltage variations becomes useful, that is to know whether the circuit would function well under voltage variation. Based on Equation 2.14, with the increase in voltage, the current will increase, thus the circuit will have less delay.

The third variation, Temperature Variation is when the temperature for the circuit is to operate is sweep from a set of values. This is because the ambient temperature also known to impacts the timing. Therefore, a good circuit design should function correctly in the temperatures between -40 to +150 degrees. The higher the temperature, the higher the collision rate of electrons within the device.

This increased collision rate forbids other electrons in the circuit to move. Since electron movement is responsible for current flowing in the device, the current would decrease with increase in temperature. Therefore, delays are expected to increase at higher temperatures.

$$K' = \frac{K'_0}{T^{1.5}} \tag{2.15}$$

$$V_{th} = V_{th0} - (m_{V_{th}})T \tag{2.16}$$

The temperature dependence of MOS devices is an important performance characteristic of CMOS circuits as expressed in Equation 2.15 and 2.16 [101] that has the temperature dependence variable of K' and Vth [ITRS].

At absolute zero temperature, K'_0 and V_{th0} are the value for K' and V_{th}. Based on Equation 2.13 and 2.14, when the value of K' decreases (increase in temperature), the drain current decreases. Also, when the value of V_{th} decreases (increase in temperature), the drain current increases. However, as the temperature increases up to a certain point, the drain current is observed to decreases, because temperature dependence is more intense in K' than V_{th}.

Chapter 3

Overview of NBTI

3.1 Modelling NBTI-Aware Degradation

Throughout this work, a developed predictive model for NBTI [51][26] based on Reaction-Diffusion (R-D) model is used. The model covers two types of cases; static NBTI and dynamic NBTI. Static NBTI is a pessimistic approach in predicting ageing and does not true for switching devices. It corresponds to the case where PMOS transistor is under constant stress throughout the time. Dynamic NBTI is a case where the annealing process was taken into account for any NBTI-induced circuits. The recovery stages give a much lower degradation rate compared to static NBTI, thus proving it is much more realistic to use it for much more realistic investigation. The principles for device failure is often benchmarked at 50mV shift or $\Delta I_{ds}/I_{ds} \sim 10\%$ [35][97].

3.1.1 Reaction-Diffusion Model

Reaction-diffusion (RD) is the classical and established NBTI model in literature and industry[94][33][32][25][81]. The model describes NBTI ageing in two stages; reaction and diffusion. The first stage is the reaction process. According to the

model, when voltage stress is applied, the SiH bonds tend to break with a linear dependence of the stress time.

The product of this breakdown is hydrogen atoms and holes. Progressing to the second stage (the diffusion process), diffusion of the hydrogen ($H or H_2$) atoms into the oxide or substrate happens. The hydrogen atoms penetrate into the oxide with time dependency (t^n), where n is a neutral hydrogen species commonly given as 0.25 [55].

The hydrogen species may diffuse into the substrate with much slower rates compared to the diffusion into the oxide layer. Diffusion of hydrogen species at the SiO_2 interface creates charged interfacial states, N_i (t). This state's density over oxide capacitance is directly proportional to the threshold voltage shift (ΔV_{th}) as expressed in Equation 3.1 [68].

$$\Delta V_{th}(t) = \frac{qN_i(t)}{C_{ox}}, i.e. \Delta V_{th} \propto N_i(t) \tag{3.1}$$

For PMOS transistor with a negative bias, the positively charged interface decreases the threshold voltage, requiring more volts to be applied on the gate as compensation because of Silicone (Si) ions at the interface having positive charge [68]. Detail explanation of this model can be found in[94][33][81]. This report will not discuss in detail about the RD model, but it has to be known that most NBTI predictive modelling was developed based on this model.

3.1.2 Static NBTI Model

PMOS transistor suffers a static NBTI Under constant stress. The changes in threshold voltage (ΔV_{th}) due to time (t) is expressed as Equation 3.2.

$$\Delta V_{th} = A\left((1+\delta)t_{ox} + \sqrt{C(t-t_0)}\right)^{2n} \tag{3.2}$$

where:

$$A = \left(\frac{qt_{ox}}{\epsilon_{ox}}\right) \sqrt[3]{K^2 C_{ox}(V_{gs} - V_{th}) \left(\exp(\frac{E_{ox}}{E_0})\right)^2} \tag{3.3}$$

$$E_{ox} = \frac{V_{gs} - V_{th}}{t_{ox}} \tag{3.4}$$

$$n = \begin{cases} 1/6 & \text{, for } H_2 \text{ diffusion based model} \\ 1/4 & \text{, for } H \text{ diffusion based model} \end{cases} \tag{3.5}$$

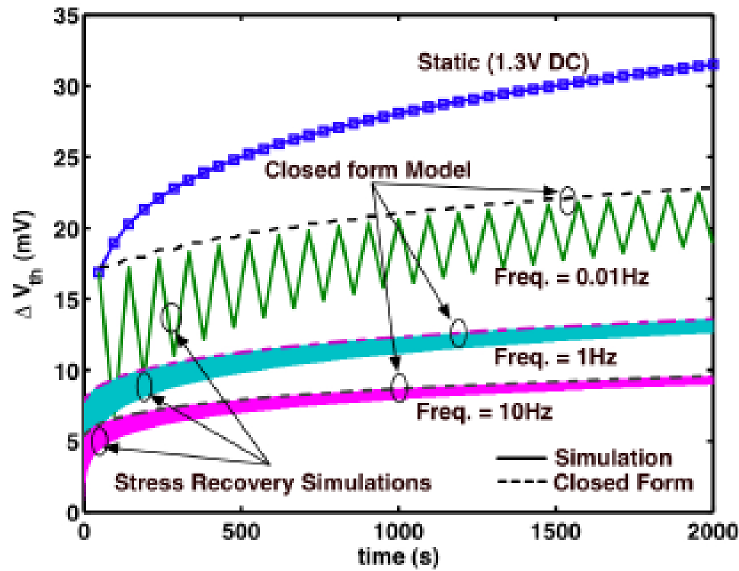


Figure 3.1: Static NBTI, Dynamic NBTI and Long-Term NBTI [55]

A is proportional to the hole density and has an exponential dependence on temperature (T) and the electric field. n is the time exponential, which is commonly given as 1/4 [55] but has recently discovered that it has different values depending on the diffusion model. For a H_2 diffusion based model, $n = 1/6$ and for a H diffusion based model, $n = 1/4$. Figure 3.1 shows the static NBTI projection

to $t = 2000s$ in the dotted blue line. The projection shown is pessimistic, and the value of ΔV_{th} is too high compared to dynamic NBTI.

3.1.3 Dynamic NBTI Model

Dynamic NBTI corresponds to the case where the PMOS transistor is in AC stress where stress ($V_{gs} = -V_{dd}$)and recovery ($V_{gs} = V_{dd}$) condition happen alternately. Equation 3.6 and Equation 3.7 are both expressing NBTI in Stress Phase and Recovery Phase respectively.

It has been pointed out in [15][76] that recovery is a 2-steps with fast recovery (drastic ΔV_{th} fall at the start of recovery) driven by H in oxide, and slow recovery (steady ΔV_{th} fall at the end of recovery) by H or H_2 back diffusion from poly-Si as shown in Figure 3.2 (t_{e1} and t_{e2}).

The 2-steps relaxation condition can be separately expressed int_e, where t_e is either equal t_{ox} or the diffusion distance of hydrogen in the initial stage of recovery. Based on this observation, [65] has concluded the dependency of the fractional recovery on t_{ox}. This can be observed in Figure 3.2 over a wide range of the supply voltage (V_{dd}) and duty cycle (α).

Stress phase:

$$\Delta V_{th} = \left(K_v (t - t_0)^{1/2} + \sqrt[2n]{\Delta V_{th0}} \right)^{2n} \tag{3.6}$$

Recovery phase:

$$\Delta V_{th} = V_{th0} \left(1 - \frac{2\epsilon_1 t_e + \sqrt{\epsilon_2 C (t - t_0)}}{2t_{ox} + \sqrt{Ct}} \right) \tag{3.7}$$

where,

$$K_v = \left(\frac{q t_{ox}}{\epsilon_{ox}} \right)^3 \cdot K^2 C_o x (V_{gs} - V_{th}) \cdot \sqrt{C} \cdot \exp\left(\frac{2E_{ox}}{E_0} \right) \tag{3.8}$$

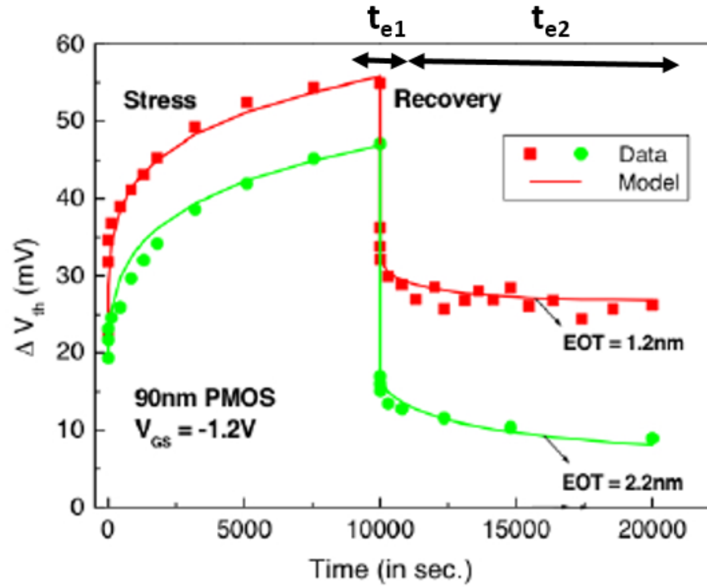


Figure 3.2: Dynamic NBTI in stress and recovery conditions [65]

$$C = T_o^{-1} \cdot \exp\left(\frac{-E_a}{kT}\right) \tag{3.9}$$

$$t_e = \begin{cases} t_{ox} & , t - t_0 \geq t_1 \\ t_{ox}\sqrt{\frac{t-t_0}{t_1}} - \sqrt{\frac{\epsilon_2 C(t-t_0)}{2\epsilon_1}} & , \text{otherwise} \end{cases} \tag{3.10}$$

3.1.4 Long-Term NBTI Model

A model proposed in [65] for a long-term threshold voltage degradation (ΔV_{th}) degradation due to NBTI at a time (t) based on the stress and recovery phases given in Equation **??** and **??**. The approach used for this model is a simplified way to observed dynamic NBTI. Instead of simulating the rise and fall of threshold voltage degradation, [65] developed an expression which only obtains a closed form for the upper bound on the ΔV_{th} as a function of the duty cycle (α), stress period (T_clk) and time (t). Equation 3.11 shows the expression for the long-term NBTI model.

$$|\Delta V_{th}| = \left(\frac{\sqrt{K_v \alpha T_{clk}}}{1 - \beta_t^{1/2n}} \right)^{2n} \tag{3.11}$$

where,

$$\beta_t = 1 - \frac{2\epsilon_1 t_e + \sqrt{\epsilon_2 C(1-\alpha) T_{clk}}}{2t_{ox} + \sqrt{Ct}} \tag{3.12}$$

Details on the derivation and explanation for all the equations can be found in [65]. The long-term degradation model in Equation 3.11 has a very high accuracy estimation with an error less than 0.1%. The trend of long-term degradation over time is shown in Figure 3.1, right over the dynamic NBTI curves in dotted lines.

3.2 NBTI Degradation Observation and Detection

There are a number of techniques used to measure ageing effect deterioration in literatures. Some of the techniques are measuring transition delays from ring oscillators, monitoring the static noise margin of the SRAM, measuring the degradation in drain current as well as the power dissipation of the ageing circuits. A correlation between these parameters with the ageing mechanism is proved in [86][46][62].

The conventional method for detecting ageing is ring oscillators. To reduce the extra area consumed by this technique, the ring oscillator is usually deployed on the circuit where it is most susceptible to ageing. Such an effort could save the space, and monitoring will only concentrate on the crucial part of the circuit, corresponding the whole condition of the system. Nevertheless, the concern on the area overhead still persists.

A pair of on-chip ring oscillators for high-resolution degradation measurements proposed in [45]. The core circuit for detecting frequency degradation consists of two free-running ring oscillators and a phase comparator During the stress period, one of the ring oscillators is stressed, while the other remains unstressed. The supply voltage of the stressed ring oscillator is raised to VDD-STRESS during stress periods and lowered to VDD-nominal during the periodic measurements, while the supply of the reference oscillator is lowered to 0 V and raised to VDD-nominal during the stress and measurement periods, respectively. The reference oscillator's supply voltage is grounded during the stress periods to prevent device ageing. Once the measurement signal is triggered, a phase comparator uses the reference ring oscillator to sample of the output of its stressed duplicate.

Similar approaches are made in [93] and [53], which beat-frequency is measured from both pairs of ring oscillators. Works were done in [93] is the further extended version of the same idea to an "all- in-one" sensor for NBTI, HCI, and TDDB. The basic idea of this sensor is to measure the differences in beat frequency, which one of the ring oscillators is under stressed conditions. It does not exclusively measure ΔV_{th} because the frequency shift is linked to actual device degradation by simulation. The unique feature of this ageing sensor is it produced a digital output, making it easier for any further data processing of the output.

Despite the improvement in detecting all three wear-out mechanisms, the increase of area overhead still exists. In order to implement this high resolution in sensing NBTI, hundreds of ring oscillators are required.

A compact in-situ sensor is proposed in [49] for monitoring NBTI and TDDB. This sensor has high sensitivity because it works in the sub-threshold region for leakage current monitoring. Although this approach has a low area and power overhead, it suffers for its own sensitivity. Too sensitive to process, voltage and temperature variation is the drawback of this wear-out monitoring.

A slightly different method is suggested in [21] where sensors comparing the speed of an inverter stressed with high switching activity to that of a non-stressed

inverter. The sensor is designed to track current degradations with temperature and varying activity factors. The sensing scheme achieved accuracies of better than 10% given a total sensing area of at least 7000μm^2. Sensor layouts showed steps taken in physical design to reduce the variation impacts. This small NBTI sensor consists of cross-coupled inverters; however, it is extremely sensitive to process variation and susceptible to error.

A different approach for using the same delay violation mechanism is studied in [75]. This NBTI ageing effect monitors a late transition in the combinational circuit of a critical data-path. In this literature, the monitoring circuit is able to detect NBTI performance degradations in the combinational part of a critical timing data-path. Our monitor requires a lower area than recently proposed alternative solutions, and a lower or comparable power consumption. Moreover, our monitor is also self-checking with respect to its possible internal faults, thus avoiding the useless negative impact on system performance and negative impact on system reliability, which could otherwise take place in case of non-self-checking sensors, should they get affected by faults. This work is crucial for measuring the wear-out information on a circuit level. Instead of relying on transistor ageing, a broader perspective has been considered. The self-checking sensors only require a small area and consumed low power compared to other delay violation sensors.

Aside from evaluating the ageing effect with frequency degradation, another reputable approach is by monitoring the change in leakage, transient and transistor drain currents. In recent years, researchers have been starting to consider current as of the circuit parameter that can be monitored to assess the ageing effect. As circuits approaching their end-of-life cycle, the drain current exhibits better sensitivity than the threshold voltage (ΔV_{th}). The leakage currents are due to NBTI, HCI or even TDDB as discussed in the previous chapter. A correlation between drain current, leakage current and threshold voltage (ΔV_{th}) are discussed in [36][76][46][62]. This validates the relevancy of the proposed ageing monitoring based on CMOS drive current.

In literature [86], an ageing effect detection is proposed to monitor the NBTI effects by sensing the leakage current reduction by implementing the idea of IDDQ testing in [77]. This sensor utilized the standby circuit leakage current (I_{DDQ}) as a metric to detect and characterize temporal NBTI degradation. Compared to the delay degradation method, this approachable to estimate the reliability of a complex circuitry such as Arithmetic Logic Units (ALUs) and memory arrays.

A different approach has been used for measuring device presented in [62] on monitoring the degradation of the peak power supply current (I_{PP}). This novel on-chip ageing sensor is capable of detecting both NBTI and HCI ageing effect by assuming that they caused by joint failure mechanism. Degradation in peak power supply current (I_{PP}) of a circuit has the same signature as the total drain current and has been proved to correlate with NBTI and HCI wear-out effect. This sensor features a unique way of assessing any ageing circuit.

The ageing sensor in [46] utilized the isolated leakage current change in the critical path from a full-chip leakage measurement result to monitor NBTI wear-out effect. The off-chip sensor can predict NBTI-induced circuit ageing without being intrusive to the area of the circuit under test, thus independent of the circuit parameter variation.

There also wear-out detection mechanism suggested by monitoring the power dissipation [96][87] and Signal Noise Margin (SNM) of SRAM memory [99][96][14][40]. The power dissipation of a circuit heavily depends on the changes in leakage current and threshold voltage (ΔV_{th}).

On the other hand, the SNM of SRAM memory is very much related to the wear-out effect because of the continuous writes and read operation create mismatches on the internal memory circuitry. An interesting finding of SRAM cell is that PMOS transistors are observed to age sooner when the memory cell stores constant data for a very long time [74]. This finding is confirmed in [26][37][63]. The correlation between temporal degradation in SNM of SRAM array and frequency degradation are discussed in detail in [86] showing this relation can be expended to predict circuit reliability.

In conclusion, the vast attention for wear-out monitoring has been focussing on one method. In order to have a better ageing prediction, one should also consider a combination of more than one technique. The used of delay degradation to measure ageing could be combined with another detection mechanism such as drain current monitoring circuitry as a counterpart. These approaches could increase the effectiveness of such a detection scheme and give a higher resolution of data in predicting the wear-out effect. Thus, in this report, it is highly considerate to explore the current sensor based wear-out detection and later to find a solution to integrate both sets of data for further processing.

All contending CMOS technologies in the sub-100 nm region will put delay degradation much harder to measure for the high-frequency system, e.g. 1 GHz clock speed will require at least 1 ns detection accuracy, but will have a fair amount of drain current to measure during operation (transient drain current for 65nm technology is 50μA).

3.3 NBTI Recovery (Annealing) Techniques

Recently it has been recognized that an interruption in the stress voltage resulting in a partial recovery on degradation (the recovery of ΔV_{th}). However, the ΔV_{th} relaxation has implication to the lifetime prediction of a device under ageing stress [68]. Several techniques to mitigate or reduce NBTI degradation have been proposed.

A method is proposed in [17] by replacing the degraded critical gates with a fresh gate. The gates were categorized based on its susceptibility to degrade under NBTI because not all PMOS transistors are under NBTI effects. The detection is based on delay degradation, which consists of a sensor to monitor NBTI degradation.

In [47], gate sizing algorithm based on Lagrangian relaxation (LR) has been proposed by increasing the sizes of the critical gates to reduce gate delay in the design stages. The method can ensure NBTI-immune circuit operation for ten

years with a penalty of an average of 8.7% area overhead. The similar gate sizing technique can also be found in [37] and [69]. In [79], up to 60% reduction on the delay of degradation can be achieved by lowering the chip temperature.

3.4 Drain Current Degradation by NBTI

An experiment was conducted in [36] reveals that the drain current is very much affected by NBTI, which highly depends on the supply voltage. The relationship between transistor drain saturation current (I_{dsat}) degradation and the supply voltage (V_{dd}) shown in Figure 3.3 and 3.4, where it can be observed clearly the dependence of NBTI degradation on V_{dd}.

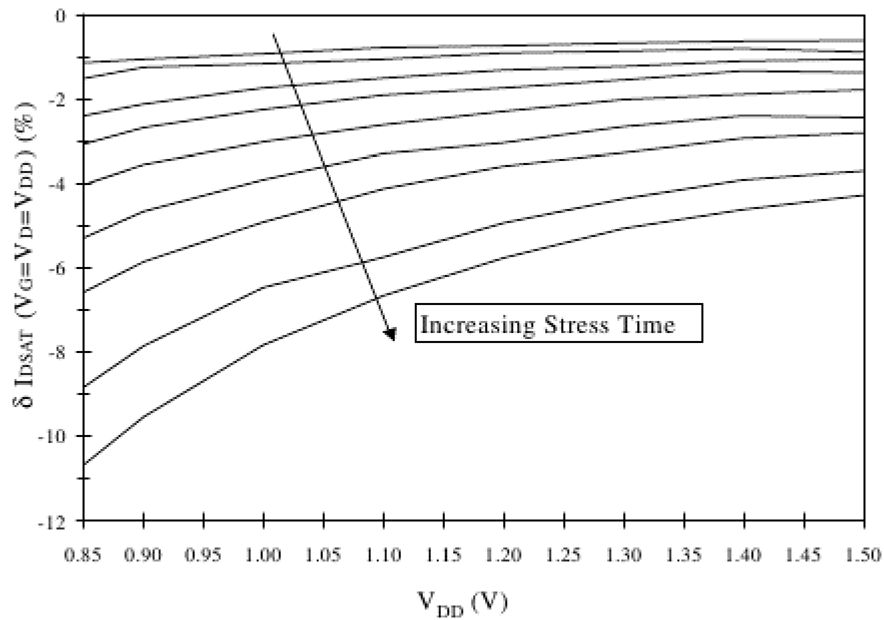


Figure 3.3: Drain saturation current (I_{dsat}) degradation over supply voltage (V_{dd}) after NBTI stress [23]

Figure 3.4 shows the frequency degradation versus V_{dd} for the same circuit. The characteristic of both frequency and drain saturation current exhibits similar degradation trait; both degraded more worst in lower V_{dd}. The degradation worsens at a lower V_{dd} is due to the reduction of gate drive voltage ($V_g - V_{th}$).

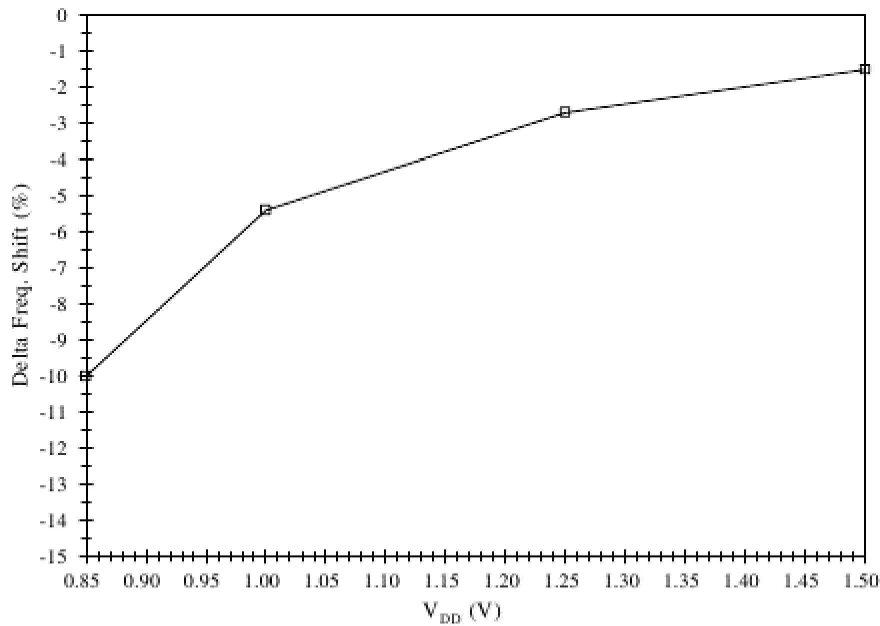


Figure 3.4: Frequency degradation over supply voltage (V_{dd}) after NBTI stress [36]

Since the gate voltage is equal to V_{dd} during the I_{dsat} measurement, drive voltage decreases because of as the decreases in V_{dd}. This can be expressed in mathematical representative as below.

$$I_{dsat} \propto (V_g - V_{th})^{\theta} \tag{3.13}$$

By examining the Equation 3.13, the relationship between a change in V_{th} and I_{dsat} can be expressed as below.

$$\frac{\Delta I_{dsat}}{I_{dsat}} \propto \theta \frac{-\Delta V_{th}}{V_g - V_{th}} \tag{3.14}$$

From Equation 3.14, a graph can be illustrated to understand the relative change in I_{dsat} for any shifted value of V_{th}. The illustration of Equation 3.14 can be found

as Figure 3.5.

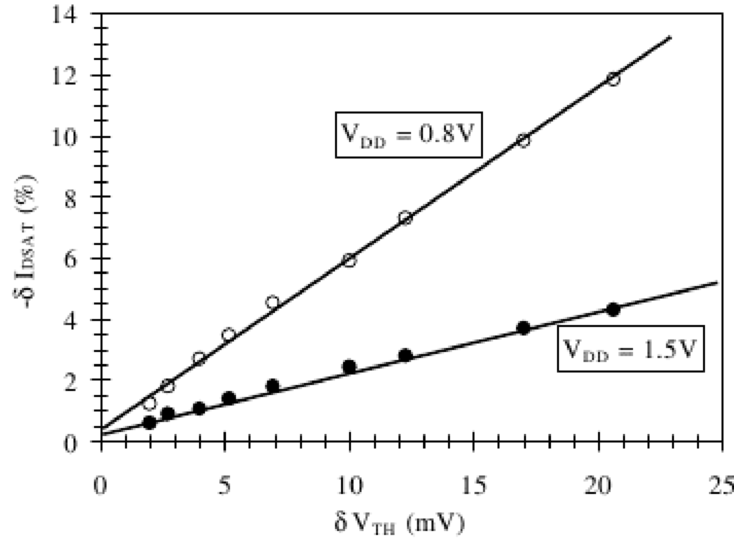


Figure 3.5: The relationship between percent changes of drain saturation current (I_{dsat}) versus the ΔV_{th} shift for two different supply voltages (V_{dd}) [36]

Based on this evidence, it is safe to speculate that with the decrease in V_{dd}, the size of the CMOS process is decreasing as well, but not with proper scaling of dimension-supply power. Thus, with the decreasing of the V_{dd}, the degradation of device parameters are proportionally increasing.

From Figure 3.5, it can be observed that the percentage of I_{dsat} degradation at $\Delta V_{th} = 20mV$, is reaching -11.5%. This is already 40% of the benchmarked value of ΔV_{th} (before a device become a total failure [35]) for $V_{dd} = 0.8V$. The I_{dsat} degradation is lower for $V_{dd} = 1.5V$, only -4.0%. This is due susceptibility of smaller CMOS technology to ageing effects. CMOS technology below 32nm is more susceptible to ageing as mentioned in the previous chapter.

This data gives some insight on how significant is the degradation on I_{dsat} for NBTI effect, thus focussing on this parameter for predicting and monitoring NBTI effect should give an upper hand in combating NBTI.

Chapter 4

Current Degradation Measurement

4.1 Self-Calibrated Sensor

Advancements in sensor network technology in recent years have led to a growth in the use of various kind of sensors including in the field of ageing effects. Sensors are typically connected in clusters which are then the cooperation of a sensor network. These sensors are usually intended to be low-powered due to power constraint.

The sensor network should not interfere with the normal operation of the circuits under observation. These connections of sensors are networked with each other and have the capabilities to send signals to the controller circuit when the monitored objects activate the sensors. Being a low-powered signal circuit, they are often in standby mode or sometimes known as ”sleep” mode.

Considering the nature of the ageing effect, all the circuits are affected and could ageing depending on the stress level being put on the circuit, even during ”sleep mode” [5][4]. However, the ageing effect is almost negligible or minimal in those modes. Hence, sleep mode has become one of the mitigation ideas for combating ageing effects.

In the field of I_{ddq} testing, both the absolute value and the variability of the chip on test quiescent current varies between chips even for the same process on the same wafer of the same fabrication batch. As a consequence, a complex computation to distinguish these variabilities in the initial fresh circuit current requires the following attention [3]:

1. Differential computation and measurements: Performing any comparison between two or more measurements to determine a defective circuit. This requires the sensor to be able to compute differential between a measured value of current at time t_n with the initial current value at time t_0 (current value when the circuit is "fresh").

2. Complexity: It is assumed that the sensing circuit is able to remember measurements in a previous time for at least a few previous values for the computation in (1) to take place.

An off-chip test such as the Automatic Test Equipment (ATE) has a better advantage in doing I_{ddq} testing because of its simplicity of implementation and high accuracy measurements with better precision. However, the ATE is an extremely slow process of testing. It requires the circuit under test to be unplugged and place inside of the testing rig, and the cost of the ATE itself is expensive for an I_{ddq} testing. Thus, it brings interest to many researchers to study the on-chip I_{ddq} test approach.

The main problem for an on-chip test is that variability in process technology that affects the "fresh current". This problem encouraged the on-chip test to have a self-calibrated feature for the current sensor to be implemented.

Another concern for on-chip testing is the requirement to have high-performance ADC for this particular I_{ddq} testing [2]. The characteristic of small in magnitude and resolutions requires a good ADC to handle signal conversion from analogue to digital with a minimal error during the process.

4.2 Bulk-BICS in SET Implementation

In order to implement a current degradation measurement, the implementation of bulk Build-In Current Sensor (bulk-BICS) in Single Event Transient is made as a reference. In CMOS digital circuits, there are two types of upset mechanisms due to ionizing particles can be described as described in [9]. The first of these is single-event upset (SEU). The second is referred to as a single-event transient (SET).

An SEU is a static upset in a storage cell such as a latch or shift register. The latch's state can be flipped by a radiation particle creating a charge on any node in the circuit. The error rate of SET is dependent on the clock frequency. The faster the clock, the more latching clock edges to capture a transient signal.

4.2.1 Bulk-BICS Circuits

There are significant numbers of research on monitoring the SEU effect based on the bulk-BICS approach [6][8][10][7]. Bulk-BICS are very useful for circuit testing; both, online and offline. In the early years, bulk-BICS is known to cause performance degradation of the circuit under test from the voltage drop across the sampling device. However, this has since been solved by implementing current mirror circuit which enables the sensor to be totally isolated from the circuit under test.

In general, bulk-BICS is able to sample the I_{DDQ} from the circuit under test directly and non-intrusively as depicted in Figure 4.1. The insertion of BICS can be easily implemented due to its simplicity of tapping to the supply voltage of any CMOS circuit that needed to be tested. Figure 4.2 depicts the bulk-BICS being implemented to the bulk of an exclusive-OR logic gate [6].

The Bulk Built-In Current Sensors (bulk-BICS) is used to detect transient errors such as SET analyses the current that appears at the bulk terminal. During normal operation, the current exist in the bulk is only the leakage current. Only the

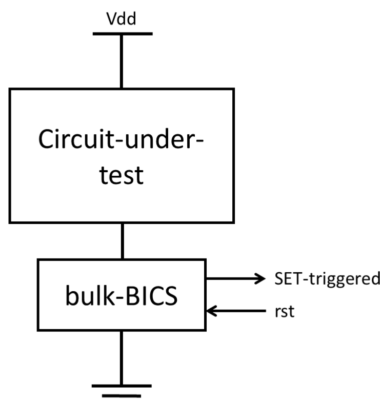


Figure 4.1: General implementation of BICS for online testing.

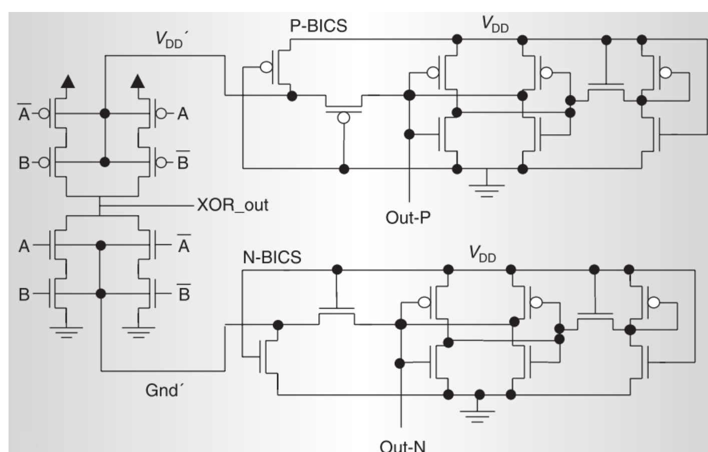


Figure 4.2: The connection of bulk-BICS to the bulk of an exclusive-OR logic gate [6]

leakage current flows through the biased junction during normal circuit operations. During SET happens, when an energetic radiation particle strikes any node in the circuit, a significant increase in transient current in the bulk. This sudden high amount of current is clear to the bulk-BICS that a SET has happened. The bulk-BICS circuitry will then generates a signal indicating that a current peak in the bulk was detected which triggered the controller circuit for SET fault. Once a SET is detected, the bulk-BICS output that signals the occurrence of a SET is activated, and it remains in this state until the reset input is activated.

4.2.2 Implementing Bulk-BICS in Ageing Effects

This idea of detecting SET by implementing bulk-BICS is very interesting and could be modified to work for monitoring ageing effects. The fundamental principle is similar between these two cases where parameters being observed is the transient current of a circuit under test. In the case of SET, the bulk-BICS only trigger output when there is a significant increase in transient current in the bulk as depicted in Figure 4.3.

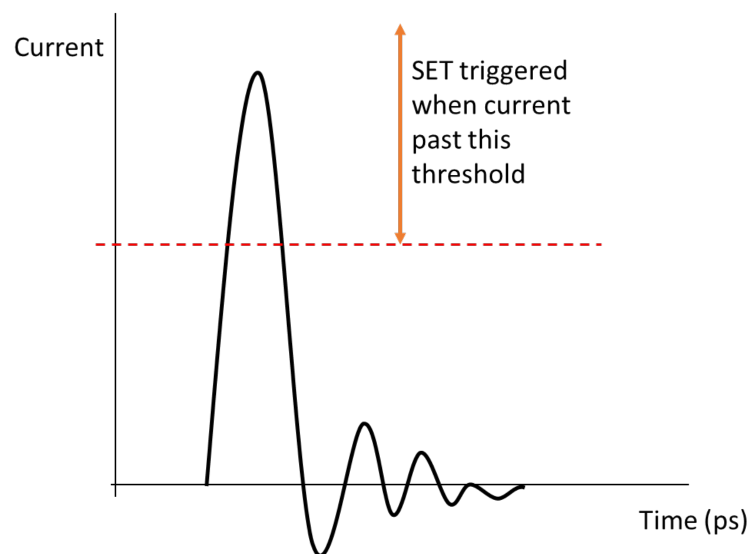


Figure 4.3: SET triggered mechanism in bulk-BICS.

Figure 4.3 illustrates the working principle of BICS in detecting any SET during particle radiation. The increase in transient above the set threshold is determined as an upset, and the control circuitry will be alerted such that any data or signal from the memory element circuit is to be corrected or taken into any SET mitigation process.

The same principle could be inverted for ageing effect implementation. This is best presented in Figure 4.4. From the figure, the fresh or un−aged circuit has optimal current value. It has been discussed in the previous chapter that the ageing effect reduces the drain current and thus affecting all other key performance parameters.

Thus, is the set threshold of certain allowable value of current could be set as the cut-off before the circuit is categorized as critically aged.

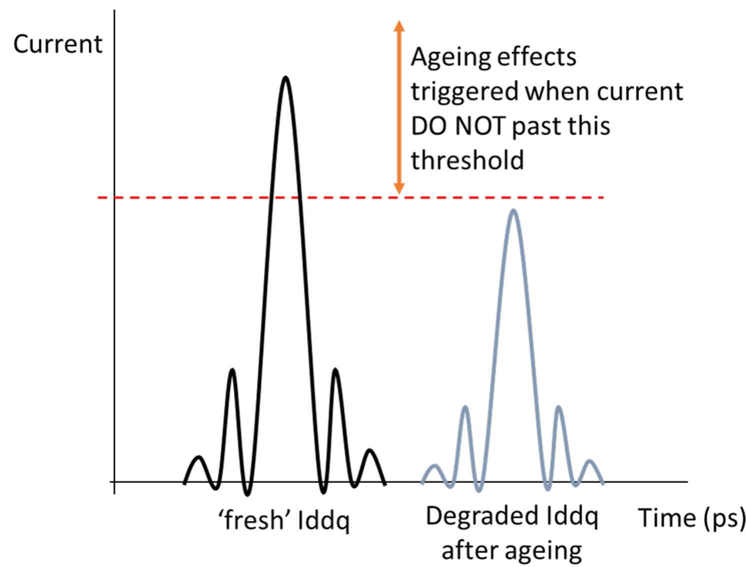


Figure 4.4: Proposed BICS for ageing effect monitoring.

The basic principle of BICS on SET implementation can be quickly deployed by inverting the output of the BICS. The BICS could trigger any absent of transient current above the threshold. This absent of transient current could be determined as a non-optimal drain current in the circuit, thus predicting that the circuit is critically ageing.

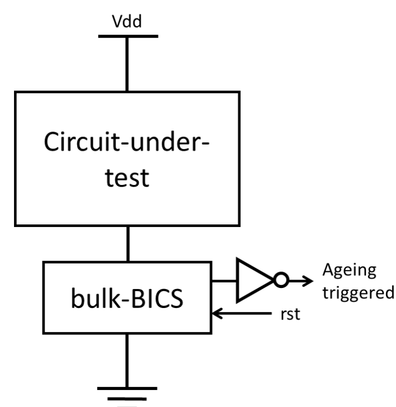


Figure 4.5: Proposed implementation of BICS for ageing.

The proposed implementation is best illustrated as in Figure 4.5. In a critical condition, such as in medical electrical apparatus, military weaponry system, space exploration electronics system or aviation industry, such alert of an ageing circuitry is very important and need the utmost attention.

4.3 The Strategy for Current Sensor Locations

The deployment of the current sensor in monitoring ageing effects need to plan strategically. Four locations could be considered in placing the sensors:

- Only on the Critical Gates on the Critical Paths.
- On all of the Critical Path of the circuit.
- Only on the high priority Critical Path of the circuit (all the gates on the path).
- The whole circuit.

Consideration has to be taken on the total number of sensor that leads to the area overhead, power consumption, and the simplicity of employing a large number of the current sensor. The results in Chapter 6 will be discussed in detail on all four plans and how does it different, based on the absolute values measured, the % of degradation observed.

Sensor locations deployment will determine the resolution and the precision of ageing circuits. It is ideal for monitoring the top priority Critical Path, and possibly extended to only the Critical Gates in on the Potential Critical Paths. This is important because these the critical path is the one under stress during the normal operation of the circuits and within the critical path, the critical gates are the gates that having the most stress, that is prone to age faster than the rest of the circuit.

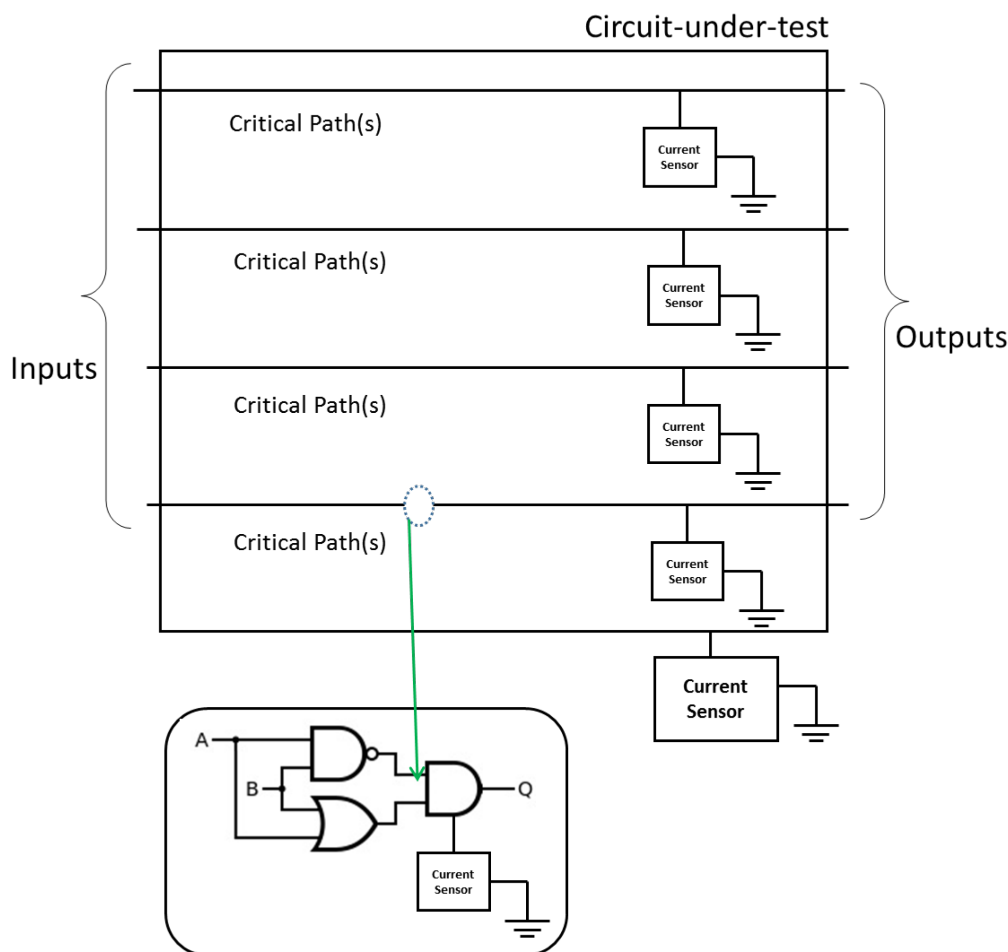


Figure 4.6: Various current sensor locations consideration.

Deployment of sensors only on the whole circuits is not practical, but for initial monitoring phase, this could be useful since the overall current degradation of the whole circuit could be the trigger that shows the circuits is ageing.

4.4 Conclusion

Implementing a current sensor that is self-calibrated is compulsory for ageing effects detection purposes mainly because of process variation drawbacks in sub 100-nm CMOS technology. This is affirmed with the need of having an on-chip monitoring system based on the I_{ddq} degradation test. An on-chip testing is much faster, and not expensive compared to off-chip test. With the advance in BICS

design throughout the years, it is becoming more apparent that implementing I_{ddq} degradation test is feasible. The bulk-BICS is a non-intrusive method for measuring I_{ddq} for any given CMOS circuits.

Chapter 5

Implementing NBTI Ageing Current Sensor

This chapter will discuss in detail on the method that will be used for finding the critical path and gates that are susceptible to NBTI, to designing the drain current monitoring circuitry.

5.1 NBTI-Aware Critical Path

The method proposed in [72] will be considered to predict the relative importance of gates under NBTI reliably. In contrast to pessimistic techniques where all PMOS transistors are believed to age at the rate, this technique can identify critical gates. By doing so, the number of PMOS transistor that needs to be considered to monitor, relax, and mitigate can be reduced. This method distinguished gates by calculating the timing degradation. Thus, protecting the circuit from ageing will be more efficient, with the minimum design overhead. Figure 5.1 shows the structure of the framework for NBTI-based static timing analysis.

For a given circuit, the process starts with the standard timing analysis, denoted in the framework as Static Timing Analysis (STA), without considering the NBTI effect. Results from STA will produce sets of Potential Critical Paths (PCPs)

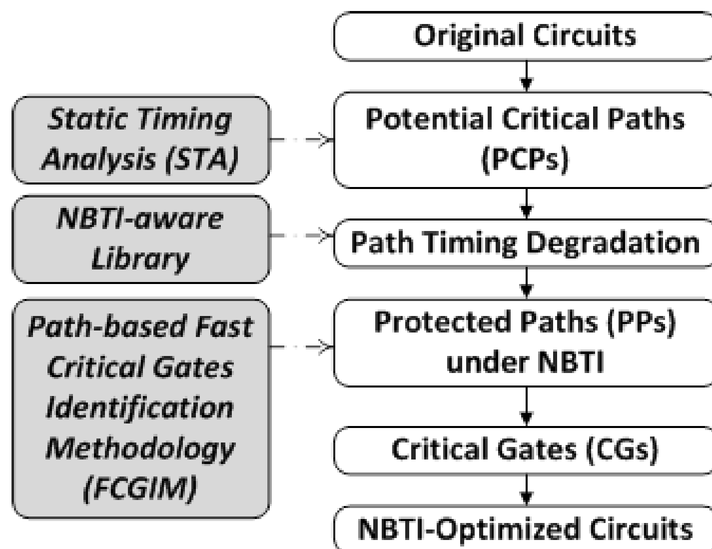


Figure 5.1: NBTI-based static timing analysis framework [72]

based on the generated timing information for all the paths inside the circuit. The PCPs only contain sets of the critical path, reducing the total devices that need to be simulated for the next process. These sets of critical paths are then needed to be filtered again by analysing them with NBTI aware library. In this process, PCPs that exceed the maximum delay margin after degradation (set to be 110% of the maximum delay before degradation) will be considered as the Protected Paths (PPs). In other words, these selected Protected Paths (PPs) are the critical paths that are most susceptible to NBTI because of the timing analysis.

They are critical paths that could exceed the time margin requirement, which is bad for the whole circuit. In the next process, the Critical Gates (CGs) within the PPs will be located by carrying out a fast critical gates identification algorithm for all the gates in the PPs. Optimisation techniques are then applied to minimise the delay degradation of these critical gates until the timing for all the protected paths satisfies the requirement.

The framework is very promising in finding the critical gates. This could reduce the amount of time needed to have NBTI simulation and very efficient in computation. Instead of having to run SPICE simulation of the whole circuit (a complex circuit

could have thousands of PMOS devices), only small selected gates will need to be run under such simulation. In this same framework, the probability for an ageing path to becoming the critical path is high. A critical set to be during the static timing analysis could not be critical anymore after a certain time.

5.2 NBTI Drain Current Degradation Monitoring

In [62], a direct measurement of drain current for the ageing effect has been proposed and is depicted in Figure 5.2. This method detects a change in peak power supply current (I_{pp}) (a signature of the drain current) based on the speculation that drain saturation current (I_{dsat}) degrades because of NBTI. For this technique, the mirrored value of I_{pp} is concurrently connected to Current Peak Detector (CPD) and later to Current-to-Time (C2T) circuitry, converting the information gathers into digital forms of data for the next prediction process.

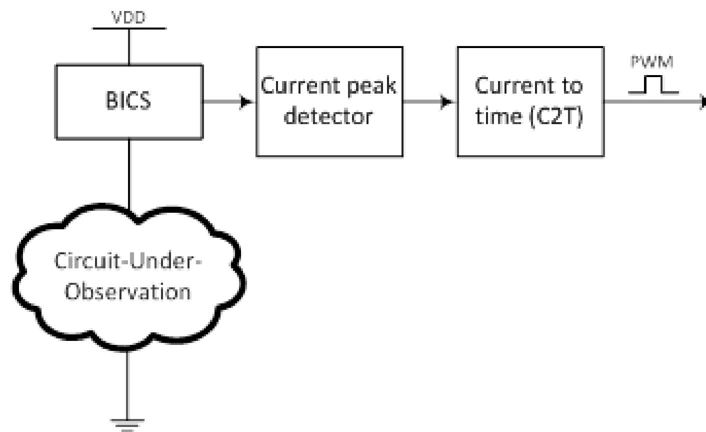


Figure 5.2: The measurement scheme proposed in [62]

The Current Peak Detector (CPD) is consisted of a current memory cell and a current comparator to determine if the present mirrored current has differed than the stored peak value. The operations of CPD start when the circuit operates at the initial stage, where the unstressed drain current is captured by

the Built-In-Current-Sensor (BICS). The peak value is then saved in the current memory cell. As the circuit under observation ageing, a degradation of the peak value in the transient drain current will happen. Any degradation in the power supply current (at the condition when pull-up and pull-down network are drawing the same amount current) will trigger the current comparator in CPD to trigger a signal to Current-to-Time (C2T). The C2T is functioning as a converter, translating the current values into a Pulse-Width Modulated (PWM) signal.

The area overhead for implementing such techniques is 20 transistors for every sensor deployed. The implications are discussed later in the next chapter.

5.3 Kogge-Stone Adder Circuit

A circuit is needed to analyse NBTI degradation for this study. Consideration has been made to implement a common design circuit with high performance to undergo NBTI-induced simulation. One way of doing it is by implementing it to the Arithmetic Logic Unit (ALU). ALU is known to be in constant switching activity because of all the computation activity. Part of the ALU is the adder circuit. Since the adder circuit can provide a wide range of parameters with multiple critical paths, it is chosen to be the circuit under test in this study. Carry look-ahead adder is the main contender because of its speed and low fan-out at each stage.

The Kogge-Stone adder is one of the members from carrying look-ahead family adders. Kogge-Stone adder utilized parallel algorithm that could generate all outputs in time proportional to $log_2 N$, for N^{th}-degree polynomials [82]. The trade-off between circuit speed and area in CMOS is frequently in the debate, and designers of high-performance chips have to sacrifice area overhead to gain a few percents of the speed. Kogge-Stone adder formulation for prefix addition is getting the speed by the pervasive introduction of parallel, logically-redundant paths enabling a real speed-up of about 15% compared to the previous predecessor when implemented in contemporary CMOS processes. However, the cost of achieving

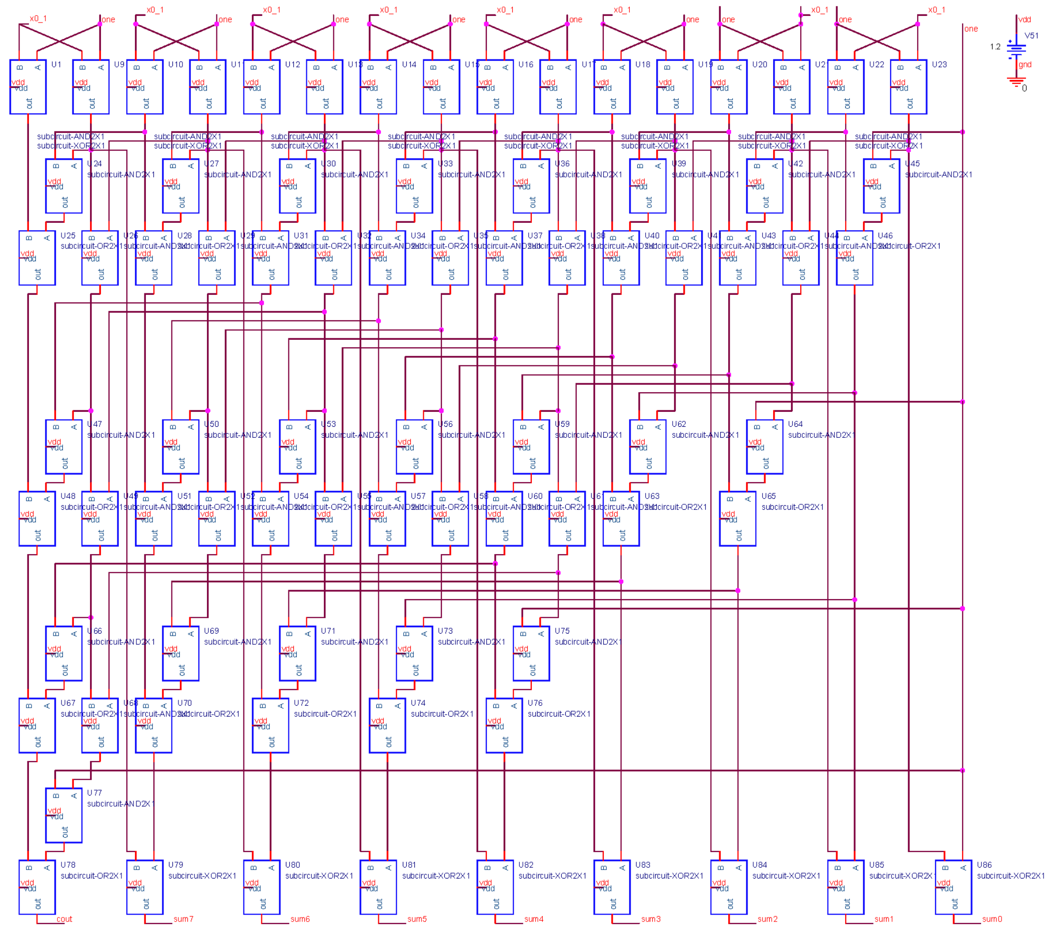


Figure 5.3: RTL Circuit of 8-bit Kogge-Stone adder

this full potential by adopting the Kogge-Stone structure is quite large in terms of wiring, and hence area and power. Figure 5.3 and 5.4 shows the circuitry in 8-bit Kogge-Stone adder.

5.4 Drain Current Degradation Detection

Initial experiments have been conducted with 8-bit Kogge-Stone adder with 90nm CMOS process technology. The simulation was run with SPICE simulation, and the results are presented as in Table 5.1 and Table 5.2. By closely relying on the information given in [35][97], which device failure is often benchmarked at 50 mV

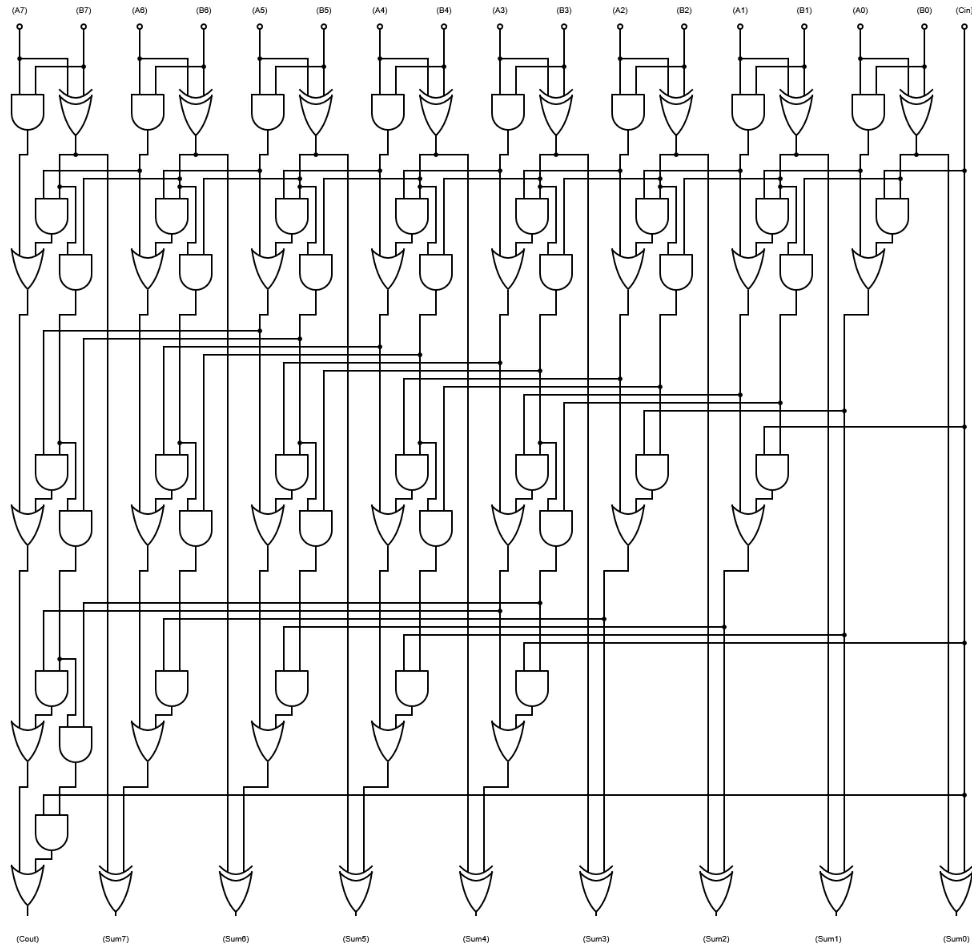


Figure 5.4: Logical Diagram of 8-bit Kogge-Stone adder

maximum shift in threshold voltage regardless of its end-of-life, the V_{th} for the PMOS transistors in Kogge-Stone adder were swept from 0% to 20% ΔV_{th}.

From Table 5.1, two of the longest paths were observed in their respective rising ($t_{p(lh)}$) and falling ($t_{p(hl)}$) propagation delays. The peak transient current was also measured. It can be seen clearly that the degradation of all parameters measured was worsening as the ΔV_{th} increased. From the table, the delay degrades by less than 500ps. The percentile of degradation relative to the unstressed propagation delay is quite small to be measured as tabulated in Table 5.2.

The worst degradation observed is the drain current degradation. With only 5% ΔV_{th} ($\sim$ 13.8 mV), the drain current has shown a decrease in value to 4.52%. Aside from that, the maximum current value is also observed. The peak current

Table 5.1: Measured values for delay and drain current degradation in 8-bit Kogge-Stone Adder

	Measured values				
ΔV_{th}	sum7		cout		I_{dd} (μA)
	$t_{p(lh)}$ (ns)	$t_{p(hl)}$ (ns)	$t_{p(lh)}$ (ns)	$t_{p(hl)}$ (ns)	
0%	2.47	1.53	2.77	2.56	668.51
5%	2.50	1.57	2.84	2.57	659.13
10%	2.53	1.61	2.93	2.64	622.84
15%	2.58	1.66	3.00	2.70	623.53
20%	2.60	1.67	3.09	2.74	590.97

Table 5.2: Percentage degradation for delay and drain current degradation in 8-bit Kogge-Stone Adder

	% of degradation				
ΔV_{th}	sum7		cout		$\%I_{dd}$
	$\%t_{p(lh)}$	$\%t_{p(hl)}$	$\%t_{p(lh)}$	$\%t_{p(hl)}$	
0%	0.00%	0.00%	0.00%	0.00%	0.00%
5%	1.39%	2.68%	2.80%	0.60%	-4.52%
10%	2.60%	5.06%	5.96%	3.39%	-7.82%
15%	4.58%	8.36%	8.45%	5.80%	-9.02%
20%	5.47%	8.87%	11.70%	7.18%	-14.10%

is in the range of 600 μA to 700 μA for a circuit that consists of a total 79 gates. This shows how feasible it is to deploy an ageing effect sensor to measure this current in real circuits. The range of hundreds of μA is a challenge to measure, but it is not impossible.

Table 5.3: Kogge-Stone adder critical paths

Critical path	**Absolute delay**
Cout	2.46 ns
Sum7	2.21 ns
Sum6	2.03 ns
Sum5	2.03 ns
Sum4	2.03 ns

5.5 Drain Current Degradation in Critical Paths

An experiment was conducted to observe the changes in critical paths of the Kogge-Stone adder circuit. The arrangements of the stimulus were made where the critical paths candidates were listed by calculation and static timing analysis. The top 5 of Kogge-Stone adder critical paths are listed as in Table 5.3. As expected from the calculation, the most critical path is the one with the longest connection with the most gates. The main objective for this experiment is to validate the changing of the most critical path during ageing and the effect of such changes to drain current degradation.

Three cases were considered for the experiments.

1. Only Critical Path 1 (cout) is to undergo ageing.
2. Only Critical Path 2 (sum7) is to undergo ageing.
3. Both Critical Path 1 (cout) and Critical Path 2 (sum7) are to undergo ageing.

The results are presented in Figure 5.5 and 5.6. It can be seen in the graph that the degradation in drain saturation current is happening as predicted in the literature. The degradation in Case 1 and Case 2 are much worse compared to Case 3. This is due to the fact that when a variant of V_{th} is done in critical path 1, Critical Path 2 drive current will be affected as well. This is because both critical paths

are sharing some gates within the line of those critical paths. However, different degradation happens in Case 3 because when the majority of the transistors V_{th} are changed at the same rate.

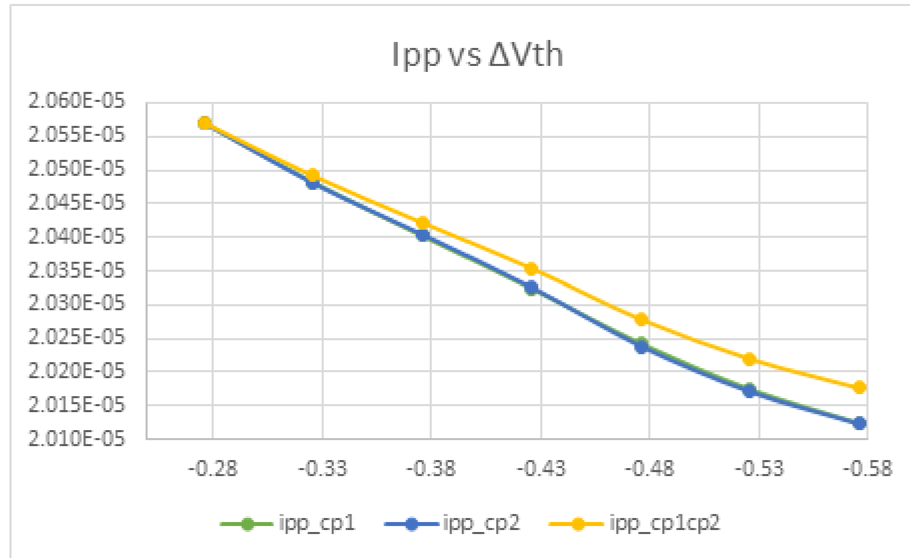
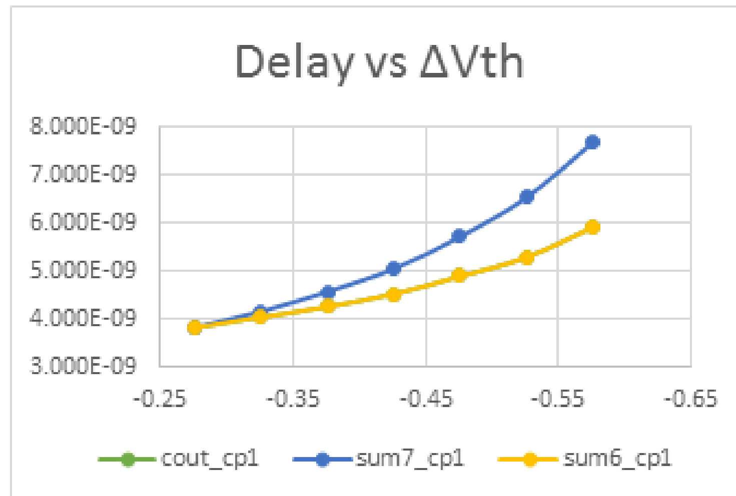


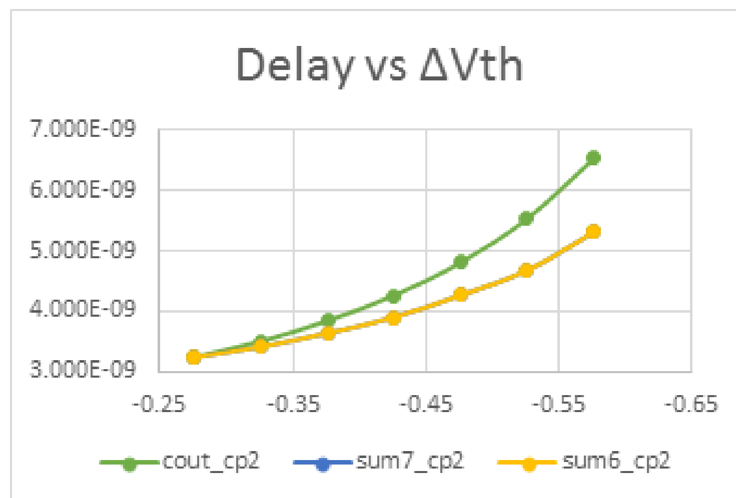
Figure 5.5: Drain current degradation in critical path

An interesting finding found in Figure 5.6 where it shows that the critical paths severity arrangement do changes for all three cases. It is expected that in Case 1, when Critical Path 1 is aged, cout will not become the most critical path anymore. The same observation can be seen in Case 2 and Case 3. In Case 2, the sum7 path shown to drop and have the same delay degradation as sum6. The same thing happens in Case 3.

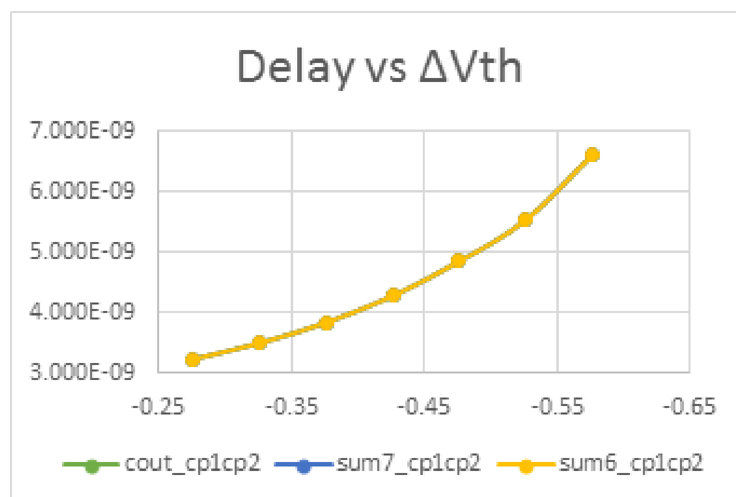
From this data, the consistency of drain current degradation as an ageing parameter should be taken into consideration. The changes in critical path severity arrangement reflect the conclusion given in [76] where delay degradation in different experiment setup with different signal probabilities and duty cycle will produce different results.



(a) Case 1



(b) Case 2



(c) Case 3

Figure 5.6: Delay degradation in critical paths for three different cases

5.6 Drain Current Degradation Sensor Overhead

Drain saturation current detection in a complex circuit like Kogge-Stone adder requires the right gates for placing the current sensor. Since different gates have different time of signal logic transition, the drive current drawn from the power supply is also different. If the technique illustrated in Figure 5.2 is implemented, the peak current measured will not be really useful because it is the peak of the sum of all drives current drawn at that particular period of time.

This explanation is best shown in Figure 5.7. In this figure, the green line shows the sum of drive current from a simple six gates circuit where only 5 of the gates is switching that the same clock cycle but at slightly different times. These differences in time are due to the intrinsic delay for each gate. By observing this characteristic of the drive current drawn by multiple gates, a modified technique needs to be used. Instead of measuring the whole circuit's drain current, the position of the sensor should only be on the critical gates. An ageing critical gate of a circuit reflects the ageing for the whole circuit.

Careful planning on how to place the drain current degradation sensor will result in having optimum area overhead. The method proposed in [72] will be used to narrow down the critical gates that need to be monitored. Based on the results from the paper, a draft calculation is done to give an overview of how much of the area overhead should be expected. Table 3 shows the total area overhead if such current degradation sensors are deployed.

In Table 5.4, two cases of timing margin were presented; *Case 1:* where time margin allowed is 5%, and *Case 2:* where the margin allowed is increased to be 10%. A calculation was done to estimate the area overhead for the implementation of drain current degradation sensor to be implemented in different circuits. The calculated gates overhead is bold in Table 5.4.

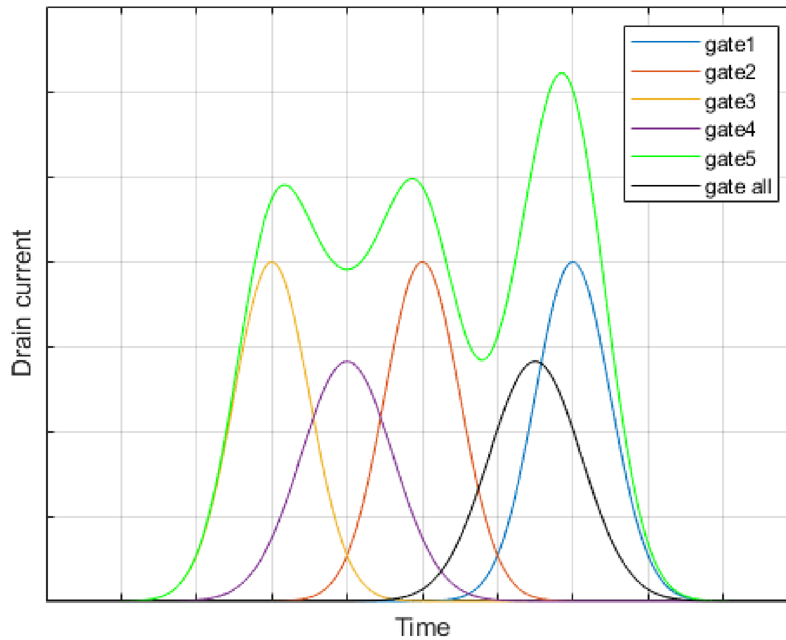


Figure 5.7: Drain currents in digital circuits

Benchmark circuits that consist of thousands to a tenth of thousand gates taken into consideration. For all these benchmark circuits, if the ageing sensors implemented to all Critical Gates, it would only cost a considerable amount of area. As the time margin increased, the area overhead is reduced simply because the ageing transistors are allowed to have less stress compared to a tight timing margin. Only those transistors that violate the timing margin will consider as the Critical Gates. From Table 5.4, the maximum gates overhead is 7.98% for q=5%, and 4.07% for q=10%.

From the table, we could also observe that the size of a circuit does not imply the same overhead because it depends on the number of Critical Gates that resides in the Potential Critical Paths. The higher the number of Critical Gates, the greater the value for % overhead since more gates needed to be monitored and tapped with the current sensor. ISCAS'89 S9234 circuit is shown to be the one with the highest.

Table 5.4: Gates overhead estimation [62]

Circuit	Potential Critical Paths	Total Number of Gates in Circuit	q= 5%				q = 10%			
			Critical gates	% Critical gates	[62] (Gates added)	**% Area Overhead**	Critical gate	% Critical gates	[62] (Gates added)	**% Area Overhead**
B14	315066	4485	91	2.03	252.15	**5.62**	46	1.03	127.46	**2.84**
B15	746232	8849	172	1.94	476.58	**5.39**	110	1.24	304.79	**3.44**
B20	1109228	11729	98	0.84	271.54	**2.32**	49	0.42	135.77	**1.16**
B21	1109641	11602	116	1.00	321.42	**2.77**	44	0.38	121.92	**1.05**
B22	2192997	16991	151	0.89	418.40	**2.46**	78	0.46	216.13	**1.27**
C5315	100746	1677	32	1.91	88.67	**5.29**	18	1.07	49.88	**2.97**
C7552	17127	1946	44	2.26	121.92	**6.26**	18	0.92	49.88	**2.56**
K2	2449	1541	41	2.66	113.60	**7.37**	15	0.97	41.56	**2.70**
S9234	2118	1770	51	2.88	141.31	**7.98**	26	1.47	72.04	**4.07**
S13207	64528	2691	70	2.60	193.96	**7.21**	18	0.67	49.88	**1.85**
S15850	3972408	3530	59	1.67	163.48	**4.63**	24	0.68	66.50	**1.88**
S35932	5632	10920	176	1.61	487.67	**4.47**	96	0.88	266.00	**2.44**
S38417	192977	10556	161	1.53	446.10	**4.23**	13	0.12	36.02	**0.34**
S38584	5475	12651	38	0.30	105.29	**0.83**	18	0.14	49.88	**0.39**

5.7 Conclusion

Implementing drain current sensors as a detection mechanism to predict the ageing effect has been proposed in this chapter. The area overhead and the significance of monitoring the drain current has been discussed as well. With the timing margin of 5%, the worse gates overhead are calculated to be below 8%. It was mentioned in the previous chapter that this mechanism of ageing prediction is best to implement as a counterpart to the delay degradation method. By having both delay and drain current monitoring, an increase in prediction probability will be higher.

Chapter 6

I_{ddt} Current Degradation Measurement in CMOS Circuits

MOS devices for CMOS process technologies below 45nm are known to be susceptible to ageing effects such as BTI and HCI. The correlation between the supply current degradation and the propagation delay degradation is shown to provide crucial information in monitoring circuit ageing. The ageing analysis was conducted for various CMOS circuits and the ALU of the OpenRisc 1200 processor using 32nm process technology. Results showed that the I_{ddt} current degradation might vary up to -11.97% compared to delay degradation of 7.15% of the same critical path. A significant I_{ddt} current degradation of -23.34% can be observed for the ALU circuit block. Evaluating the I_{ddt} current degradation in the broader perspective provides not only a better percentage change, but it also provides a much bigger absolute current.

6.1 Introduction

In recent years, CMOS circuit reliability has become a significant design issue for on-chip systems. As the transistor size has decreased, it brings a new challenge in the field of circuit reliability as ageing effects are becoming more significant.

The three main ageing effects are Bias Temperature-Instability (BTI), Hot Carrier Injection (HCI) and Time-Dependent Dielectric Breakdown (TDDB) [41][24]. The ageing effects are known to potentially reduce the lifetime of the CMOS circuit by a significant number of years [70].

The BTI effect has been proved to gradually shift the threshold voltage [88][18], and subsequently affects the speed of the circuit. For a 32nm CMOS process technology, a 50mV shift in the threshold voltage for five years of operation is predicted, [24]. There are two types of BTI, the Negative-Bias-Temperature-Instability (NBTI) and Positive-Bias-Temperature-Instability (PBTI). NBTI affect the P-type transistors because of the negative gate bias stress during input logic 0 at the gate, and likewise, the PBTI affect the N-type transistors. Hot carrier injection (HCI) is an ageing mechanism that happens when a majority carrier is injected or trapped in the gate dielectric of a MOS transistor that caused the threshold voltage to change.

BTI and HCI have been identified as the most prominent long-term effect in sub-45nm technologies [81][89][78]. The degradation in the threshold voltage is known to reduce the drain current [18][97], slowing down a digital circuit's performance [100][48] and affecting the signal noise margin (SNM) for SRAM cells, [74][40].

Currently, most of the research has been focussing on monitoring the ageing effect by observing the propagation delay degradation. An increase in delay after a few years of lifetime implies that the circuit is ageing. Monitoring this parameter in a circuit is very likely to predict a reliability problem before it malfunctions in the field.

An alternative approach for monitoring the ageing effects is by observing the circuits' second degrading parameter, the drain current. The drain current of a CMOS device consists of the transient current (I_{ddt}) and the quiescent current (I_{ddq}). It has been reported in [36][76] that the drain current is closely correlated

to the threshold voltage. From I_{ddt} point of view, device failure is benchmarked when $\Delta I_{ds}/I_{ds}$ has a variation of more than ~10% [38][97].

In this chapter, an alternative approach for monitoring ageing in a circuit based on the I_{ddt} current presented. In this approach, the main problem of measuring the small value of I_{ddt} current is addressed, and the placement of such a sensor in a processor is discussed.

6.2 Previous Work

There have been several research ideas in the literature for ageing prediction. One approach uses a pair of on-chip ring oscillators for high-resolution measurement of degradation, [45] where they used 265x132 μ^2 test chip and fabricated in a 1.2 V, 130 nm CMOS technology fabricated in a 1.2 V, 130 nm CMOS technology. The target initial counter output with sensing resolution of 0.02% (or 0.8 ps). The ring oscillators proposed in this literature contain trimming circuits allowing a wider and finer calibration range for the initial count.

A similar idea used the beat-frequency from both ring oscillators [53][93] accomplished with a pair of modified ring oscillators (ROSCs) which are representative of standard CMOS circuits. The author use a "backdrive" concept, in which one ROSC drives the voltage transitions in both structures during stress, such that the driving oscillator ages due to both BTI and HCI, while the other suffers from only BTI. In addition, long term or high voltage experiments facilitate TDDB measurements in both oscillators. Measurement results are presented using a 65 nm test chip over a range of stress conditions.

An "all-in-one" sensor further extended the same idea for NBTI, HCI, and TDDB [49]. The author introduces two compact structures to digitally quantify the change in performance and power of devices undergoing NBTI and defect-induced oxide breakdown. The small size of the sensors makes them amenable to use in a standard-cell design with the low area and power overhead. The sensors can

be implemented in large numbers to collect data on degradation and statistical performance of the devices. A test-chip containing 144 oxide-degradation sensors and 96 NBTI sensors with 44 20-bit storage registers is fabricated in 1.2V/3.3V 0.13μm CMOS technology. The nominal gate-oxide thickness for standard devices is 2.2nm, while the nominal threshold voltage is 355mV for NMOS devices and -325mV for PMOS devices. The test chip consists of 11 blocks, each containing 16 to 32 sensors, a 20- bit counter and 4-entry shift register for rapid measurement of NBTI. Instead of evaluating the ageing effect from frequency degradation, another approach is to monitor the change in leakage, transient and/or drain currents of the transistors under observation.

In [77][86], the idea of leakage current testing was used in an ageing effect detector to monitor the NBTI effects by sensing the leakage current reduction. This sensor used the standby circuit to detect and characterise temporal NBTI degradation. The author proposes to utilize the standby circuit leakage IDDQ as a metric to detect and characterise temporal NBTI degradation in digital circuits. Compared to the f_{MAX} based approach, the proposed IDDQ based technique benefits from lower test cost and improved capability of estimating the reliability of complex circuitries such as ALUs and SRAM arrays. They have derived an analytical expression for circuit IDDQ from the analytical PMOS V_{th} degradation model. The proposed model is verified with measurement data obtained from a test chip fabricated in 130nm technology. The results from this study show that the temporal degradation in static noise margin (SNM) of SRAM array and f_{MAX} of random logic circuits are highly correlated to the IDDQ measurement. This finding is highly beneficial for long term circuit reliability prediction.

In [62], a different approach monitored the degradation of the peak power supply current ($I_{V_{dd}-peak}$). This on-chip ageing sensor that is capable of detecting both NBTI and HCI ageing effects is a novel on-chip ageing sensor able to detect the amalgamated ageing effects of ICs caused by joint failure mechanisms. This is achieved by detecting the peak power supply current (Ipp) degradation from the device and/or circuit, which is a signature of the total drain current. Unlike the existing ageing sensors, which indirectly estimate the ageing status of a device,

the proposed sensor allows for direct ageing assessment for a single device and/or circuit blocks. Simulation results using the TSMC 65nm technology indicate that the proposed sensor can operate at 1GHz. Accelerated test simulation in Cadence for a set of ISCAS85 benchmark circuits indicates that the drain current exhibits a similar ageing rate as the threshold voltage for the entire circuit lifetime, but with a better sensitivity towards the End-of-Life (EOL), which demonstrates the validity and practical relevance of the proposed ageing monitoring framework.

The off-chip ageing sensor in [46] used the isolated leakage current change in the critical path from a full-chip leakage measurement to monitor the effect of NBTI. The experiments are simulated using PTM 65nm technology library using some of the ISCAS benchmark circuits. The chip-level leakage changes under a set of measurement vectors are first formulated as an equation set, hence obtaining the leakage changes in the gates along the critical path is possible from calculation proposed. The correlation between leakage change and delay increase was used to predict delay degradation on an arbitrary critical path.

The drawback of these current-based sensors is that a very small current is measured (tens of pA). I_{ddt} testing has largely been abandoned since the 1990s mainly because of the difficulty of measuring the small currents. Recently, researchers have been tried implementing I_{ddq} and I_{ddt} testing in fields such as hardware security and counterfeit detection [34], as well as in instruction-level functional tests analysing large processors [95], and open fault detection in 3D ICs, [44]. These methods, however, are off-line tests and require the circuit to be taken to a test rig.

6.3 Drain Current Degradation by Ageing Effects

The motivation for this work came from the observation that the magnitude of the total power dissipation increases as the circuit ages. As shown in Equation

(6.1), the dynamic current (I_{ddt}) is more dominant than the static current. This current increases proportionally with the dynamic power dissipation. A study in [85] pointed out that the power of a CMOS circuit reduces with ageing. A study in [36] reveals that ageing effects affect drain current degradation, which is highly dependent on the supply voltage.

$$P_{total} = \frac{C \cdot V^2 \cdot freq}{2} + I_{static} \cdot V + I_{ddt} \cdot V \tag{6.1}$$

Equations (6.2) and (6.3) give the transistors' drain saturation current (I_{dsat}) and the transistors' gate drive voltage ($V_g - V_{th}$), [71][73].

$$I_{dsat} \propto (V_g - V_{th})^{\alpha} \tag{6.2}$$

$$\frac{\Delta I_{dsat}}{I_{dsat}} \propto \alpha \frac{-\Delta V_{th}}{(V_g - V_{th})} \tag{6.3}$$

The velocity saturation index (α) models the velocity saturation of carriers according to the α-power law, [84]. Equations (6.2) and (6.3) show that a change in V_{th} will affect the drain current as much as it will affect the propagation delay. In [36], it has been pointed out that a V_{th} degradation of $\Delta V_{th} = 20mV$, could cause up to 12% decrement. Similar findings are presented in [38] for the NBTI effect.

6.4 I_{ddt} Current Degradation in CMOS Circuits

All results presented in this chapter are from HSPICE simulations, and the ageing analysis is done using MOSFET Model Reliability Analysis (MOSRA). HSPICE reliability analysis for HCI and BTI run in a two-phase simulation, the fresh and post-stress phase. During the fresh simulation phase, HSPICE computes the electron age/stress of selected MOS transistors in the circuit based on circuit

behaviour and the HSPICE built-in stress model. During the second phase, HSPICE simulates the degradation effect on circuit performance based on the stress information produced by the first phase.

For BTI model, HSPICE MOSRA analysis based on the trapping/de-trapping model that considering two principal physical mechanisms, the interface traps and the traps deep inside the dielectric layer. This enabled HSPICE MOSRA to calculate the degradation of the device threshold voltage. HSPICE MOSRA is also capable of analysing the BTI effect dynamically with the partial-recovery effect. The partial-recovery effect modelled by taking into account the stress stimulus duty cycle. For HCI model, HSPICE MOSRA analysis is based on the improved Lucky Electron Model [50]. The improved model is to retain model accuracy in the high current regime of MOS model.

In this subchapter, all simulations were designed and synthesised with 32nm process technology and simulated at 400 Kelvin for HCI and BTI ageing analysis. The HSPICE MOSRA analysis simulated dynamically (to consider the realistic stress and recovery phase of circuit operation), running from $t = 0s$ to $t =$ 3.154x10^8s (10 years) of circuit operations. The stress period is set to 90% stress to 10% recovery.

6.4.1 NAND and NOR Gates

A preliminary analysis was done to demonstrate the severe degradation of the I_{ddt} current. The first analysis was done for two basic gates, NAND and NOR gates. Figure 6.6 illustrates the results of I_{ddt} current degradation and delay degradation for both gates.

The strategy of selecting the input for each gate is explained in Table 6.1 for NAND gate and Table 6.3 for NOR gate. In order to observe the degradation of drain current, the CMOS gate level is studied. As illustrated in Figure 6.1, the drain current driven by the pull-up network that consists of PMOS devices draws current during switching from the V_{DD} to the output of the gate. For logic gates,

the peak drain current drawn is when the gates are switching from logic '0' to logic '1'. This is because of the changes of state from 0 Volt to V_{DD} Volts draws more energy compared to the changes of state from logic '1' to logic '0'.

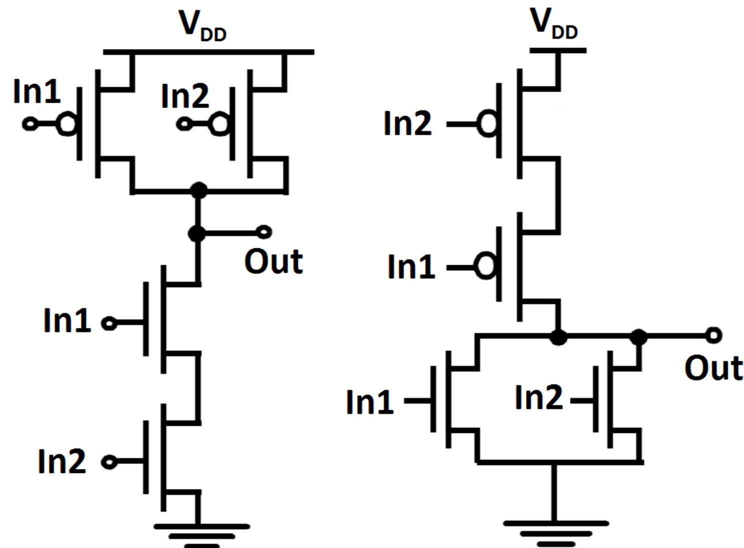


Figure 6.1: CMOS NAND and NOR gate circuits.

Table 6.1: State transition table for NAND gate.

NAND gate					
In1		In2		Out	
Present state	Next state	Present state	Next state	Present state	Next state
0	0	0	0	1	1
0	0	0	1	1	1
0	1	0	0	1	1
0	1	0	1	1	0
0	0	1	0	1	1
0	0	1	1	1	1
0	1	1	0	1	1
0	1	1	1	1	0
1	0	0	0	1	1
1	0	0	1	1	1
1	1	0	0	1	1
1	1	0	1	1	0
1	0	1	0	0	1
1	0	1	1	0	1
1	1	1	0	0	1
1	1	1	1	0	0

Thus the combination of inputs is investigated to produced a maximum peak drain current for the observation for this experiment. Based on Table 6.1, considering the present states and the next states of NAND gates, the outputs logic is calculated. In the table, the green shades show the condition at which the gates switching from logic '0' to logic '1' and vice versa.

From this information, Table 6.2 are constructed. Taking into account that only output state transition from logic '0' to logic '1' is to be considered, the input taken as the input pattern for stress test simulation. To illustrates the state transition in Table 6.2, the inputs and outputs interaction is best to describe in Figure 6.2. Condition numbered (1), (2) and (3) are the inputs pattern that caused the output to change state from logic '1' to logic '0'. Consecutively, condition numbered as (4), (5), and (6) are the inputs pattern that caused the output to change state from logic '0' to logic '1'. The peak drain current is preferred to be observed when it draws maximum current for any degradation during the ageing stress test is easily monitored and calculated. Figure 6.3 show the validity for the value of the peak drain current as simulated in SPICE.

Table 6.2: Output state transition for NAND gate.

	Out: 1 → 0	
	In1	**In2**
(1)	0 → 1	0 → 1
(2)	0 → 1	1 → 1
(3)	1 → 1	0 → 1

	Out: 0 → 1	
	In1	**In2**
(4)	1 → 0	1 → 0
(5)	1 → 0	1 → 1
(6)	1 → 1	1 → 0

The input patterns the potentially useful for NAND gate during ageing prediction monitoring are $In1 : 1 \rightarrow 0$ & $In2 : 1 \rightarrow 0$, $In1 : 1 \rightarrow 0$ & $In2 : 1 \rightarrow 1$, and $In1 : 1 \rightarrow 1$ & $In2 : 1 \rightarrow 0$.

The same case for NOR gate is implemented. Table 6.3 tabulates the state transition table for NOR gate while Table 6.4 filtered out the interested input patterns that changes output logic from logic '0' to logic '1'.

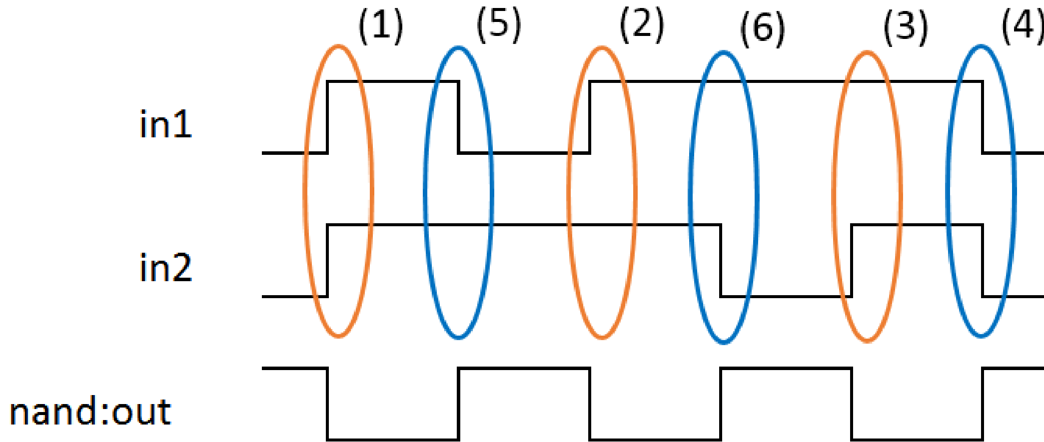


Figure 6.2: Input/output state transition for NAND gate.

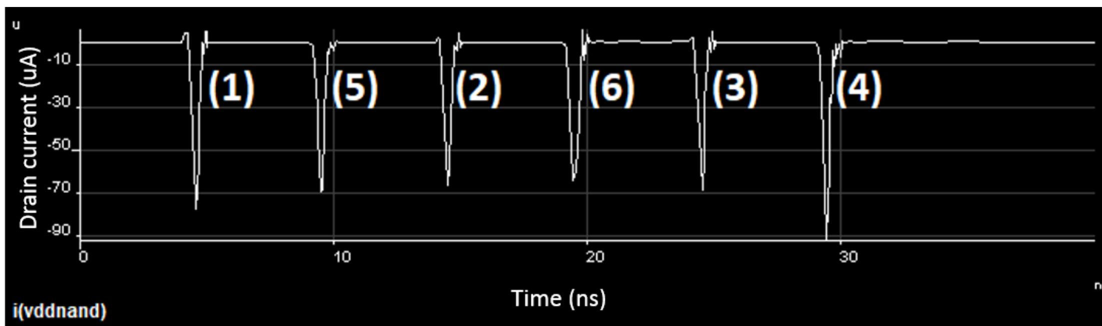


Figure 6.3: I_{ddt} response during state transition for NAND gate.

The input patterns potentially useful for NOR gate during ageing prediction monitoring are $In1 : 0 \rightarrow 0$ & $In2 : 1 \rightarrow 0$, $In1 : 1 \rightarrow 0$ & $In2 : 0 \rightarrow 0$, and $In1 : 1 \rightarrow 0$ & $In2 : 1 \rightarrow 0$. The SPICE simulation of the peak drain current for NOR gate is illustrated in Figure 6.5.

By referring to Figure 6.6, it can be observed that the I_{ddt} current degradation has the same shift pattern as the delay degradation but with a more significant degradation percentage overall. The delay degradation for NAND and NOR gates is up to 8.69% and 6.37% respectively, while the I_{ddt} degradation are at -18.49% for the NAND gate and -20.09% for the NOR gate. These changes in I_{ddt} are significant for the next steps in observing the I_{ddt} current.

Table 6.3: State transition table for NOR gate.

NOR gate					
In1		In2		Out	
Present state	Next state	Present state	Next state	Present state	Next state
0	0	0	0	1	1
0	0	0	1	1	0
0	1	0	0	1	0
0	1	0	1	1	0
0	0	1	0	0	1
0	0	1	1	0	0
0	1	1	0	0	0
0	1	1	1	0	0
1	0	0	0	0	1
1	0	0	1	0	0
1	1	0	0	0	0
1	1	0	1	0	0
1	0	1	0	0	1
1	0	1	1	0	0
1	1	1	0	0	0
1	1	1	1	0	0

Table 6.4: Output state transition for NOR gate.

	Out: 1 → 0	
	In1	In2
(1)	0 → 0	0 → 1
(2)	0 → 1	0 → 0
(3)	0 → 1	0 → 1

	Out: 0 → 1	
	In1	In2
(4)	0 → 0	1 → 0
(5)	1 → 0	0 → 0
(6)	1 → 0	1 → 0

6.4.2 32-bit Adder

Further analysis was conducted for a more complex circuit – a 32-bit adder. For this circuit, two cases were observed for their respective delay and I_{ddt} current degradations. Those cases are as follow:

1. The most critical paths.
2. The most critical gate in the most critical path.

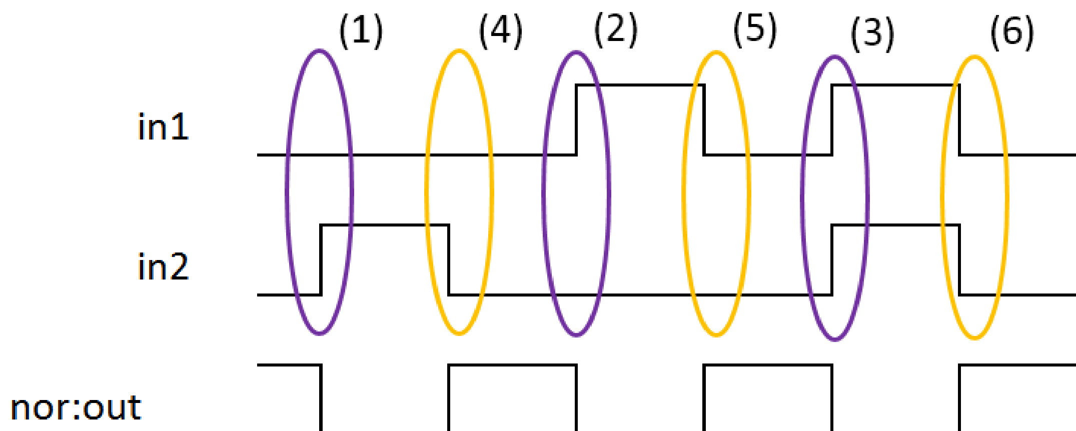


Figure 6.4: Input/output state transition for NOR gate.

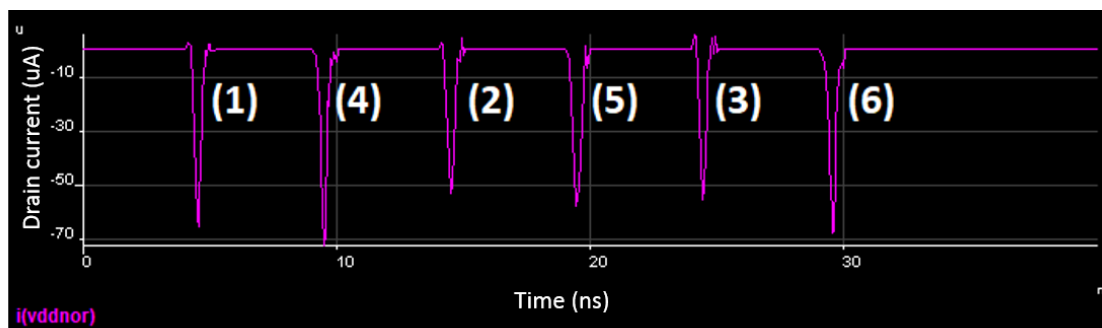


Figure 6.5: I_{ddt} response during state transition for NOR gate.

The critical path is the slowest logic path between any two registers. Therefore the overall circuit speed performance is critically based on this path. The 32-bit adder has a total of 33 paths, and the most critical path are known to be the paths with output pins of either *Cout* or *sum(31)*. For Case 1, the three most critical paths with output pins of *Cout*, *sum(31)* and *sum(30)* were considered. All paths share the majority of the gates that are closer to the input pins. The gate that is shared the most by all paths chosen for Case 1.

Figure 6.7 illustrates the delay and I_{ddt} current degradations for Case 1. After 10 years of circuit operations, all three of the most critical path exhibit similar rates of degradation. From the figure, the delay degradation for critical paths 1, 2 and 3 are predicted to vary up to 5.93%, 5.87% and 5.84%, respectively. However, the

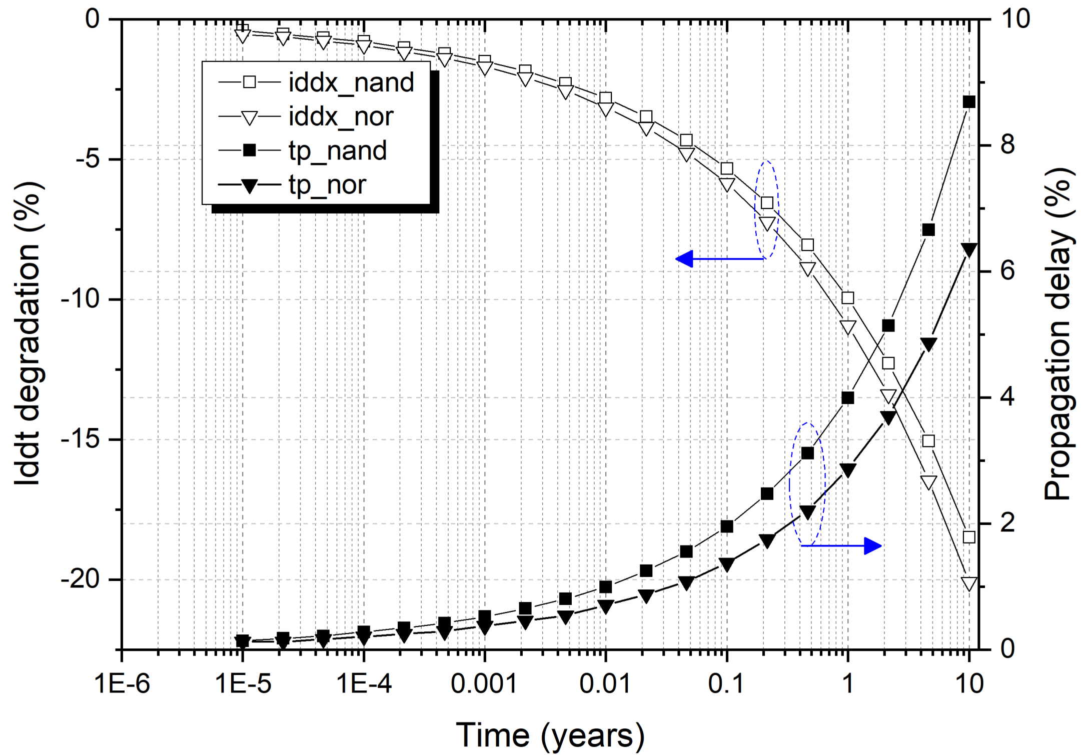


Figure 6.6: I_{ddt} & propagation delay degradations of NAND and NOR gates.

I_{ddt} current degradation shown in the same figure shows much more significant changes. The three critical paths have -15.14%, -15.14% and -15.13% degradation in I_{ddt}, respectively. Figure 6.8 shows the I_{ddt} current degradation in Case 2. The degradation for a single gate is slightly lower than for the critical path simply because of the number of logic gates. The gate degradation is shown to vary up to -14.17% compared to -15.14% for the critical path. This percentage degradation in the I_{ddt} current remains significant compared to that for the delay degradation.

These results show how to utilize the degradation in I_{ddt} to observe circuit ageing. One of the main problems of monitoring the I_{ddt} current is its small value. In a complex circuit, each transistor likely degrades at the same rate as the neighbouring transistors in the same signal path and hence the I_{ddt} current degrades overall. By measuring the I_{ddt} current over several transistors, the total amount of current that is monitored increases. From on Figure 6.8 , the same pattern of degradation was seen in both gates and the critical path because they

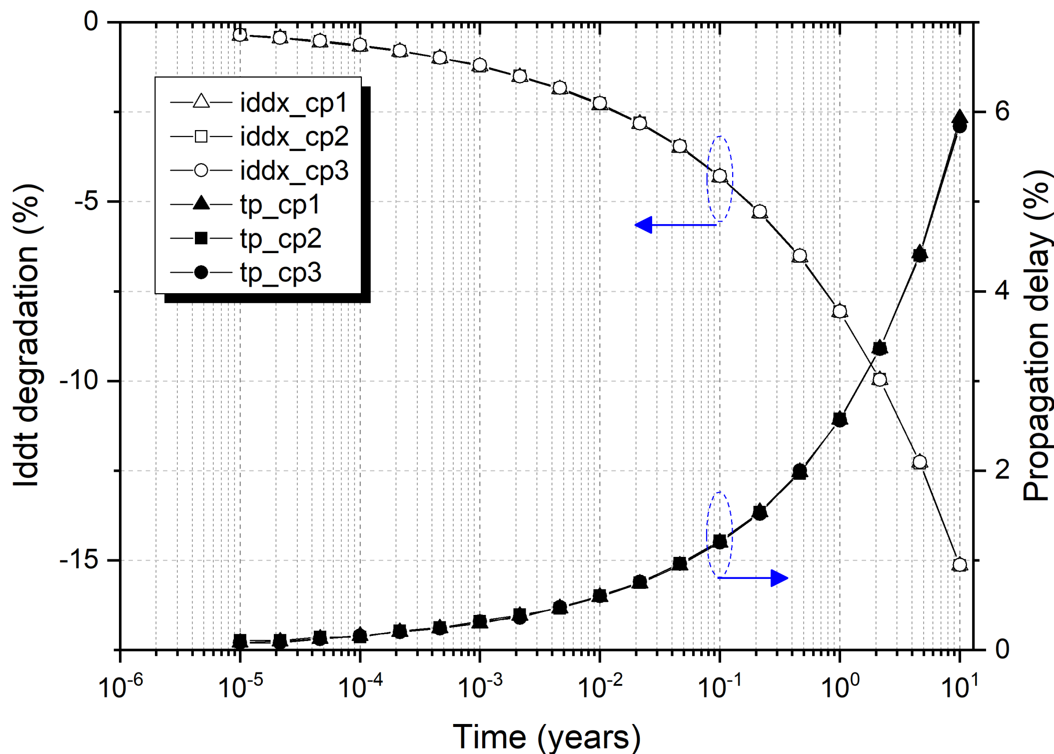


Figure 6.7: I_{ddt} & propagation delay degradations in 32-bit adder.

are ageing at the same rate. This happens because all neighbouring transistor devices would have the same variability after the fabrication process, and are operating at a similar temperature and stress.

6.5 Iddt Current Degradation in CPU

6.5.1 OpenRisc 1200 and RISC-V Processors

OpenRisc 1200 processor is an open-source, 32-bit scalar RISC with Harvard microarchitecture, 5 stage integer pipeline, virtual memory support and basic Digital Signal Processing (DSP) capabilities. OpenRisc 1200 architecture was implemented from its predecessor, OpenRisc 1000. This processor is originally intended to have performance comparable to other commercialized processor architecture such as ARM10, ARC and Tensilica RISC processors. OpenRisc

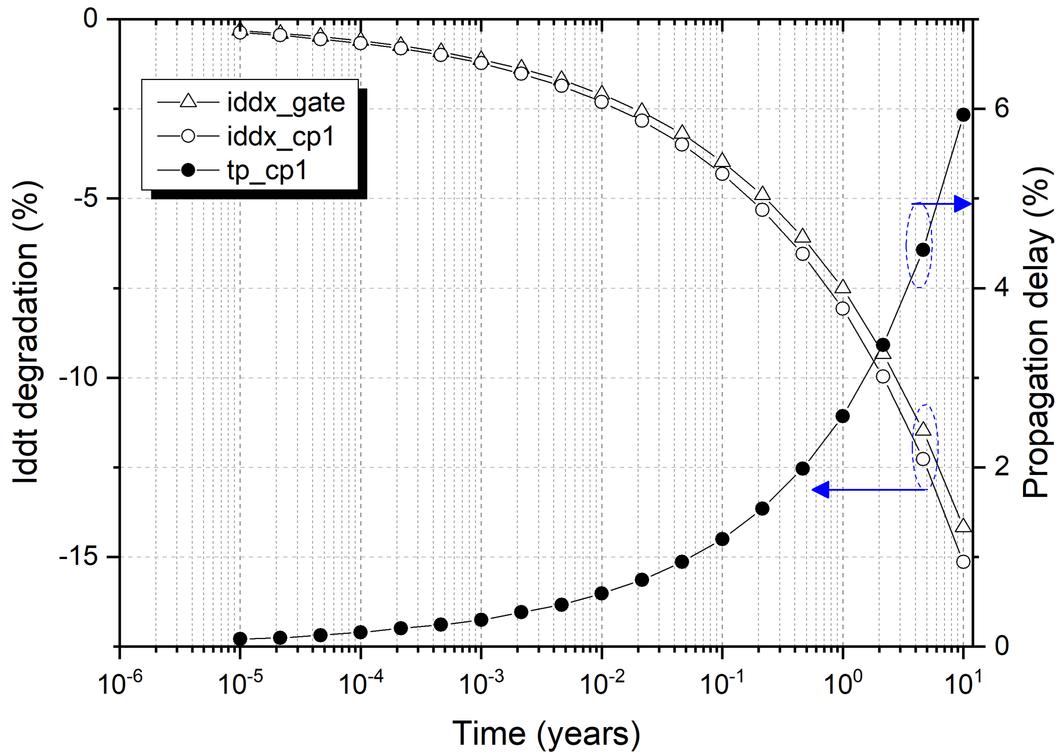


Figure 6.8: I_{ddt} degradations of critical gate and path in 32-bit adder.

1200 has been proved to work on hardware by its community, which is mainly in the field of embedded, portable and networking applications.

RISC-V Processors is also an open-source processor, first introduced by the University of California, Berkeley in 2010. Its open ISA (instruction set architecture) attracts many developers and contributors outside of the academic world. This open ISA enables the community to do any development tailored specifically to their interest.

Similar to previous subchapter experiment settings, all simulations were designed and synthesized with 32nm process technology and simulated at 400 Kelvin for HCI and BTI ageing analysis. The HSPICE MOSRA analysis simulated dynamically (to consider the realistic stress and recovery phase of circuit operation), running from $t = 0s$ to $t = 3.154\text{x}10^8 s$ (10 years) of circuit operations. The stress period is set to 90% stress to 10% recovery.

6.5.2 Sensors in OpenRisc 1200 Processor

The strategy for including sensors in a complex circuit is demonstrated in the OpenRisc 1200 processor. The current is monitored from the bulk of the device with a Built-in-Current-Sensor (BICS). As discussed in the previous section, the attributes of current degradation are similar for a single gate or a larger circuit, but there is an advantage in measuring the total absolute current. Positioning current sensors on critical gates in the critical path might seem appropriate but would be expensive given that the number of gates could be in the thousands. For a critical path, even if this were feasible, the value of the absolute current would still be too small to measure.

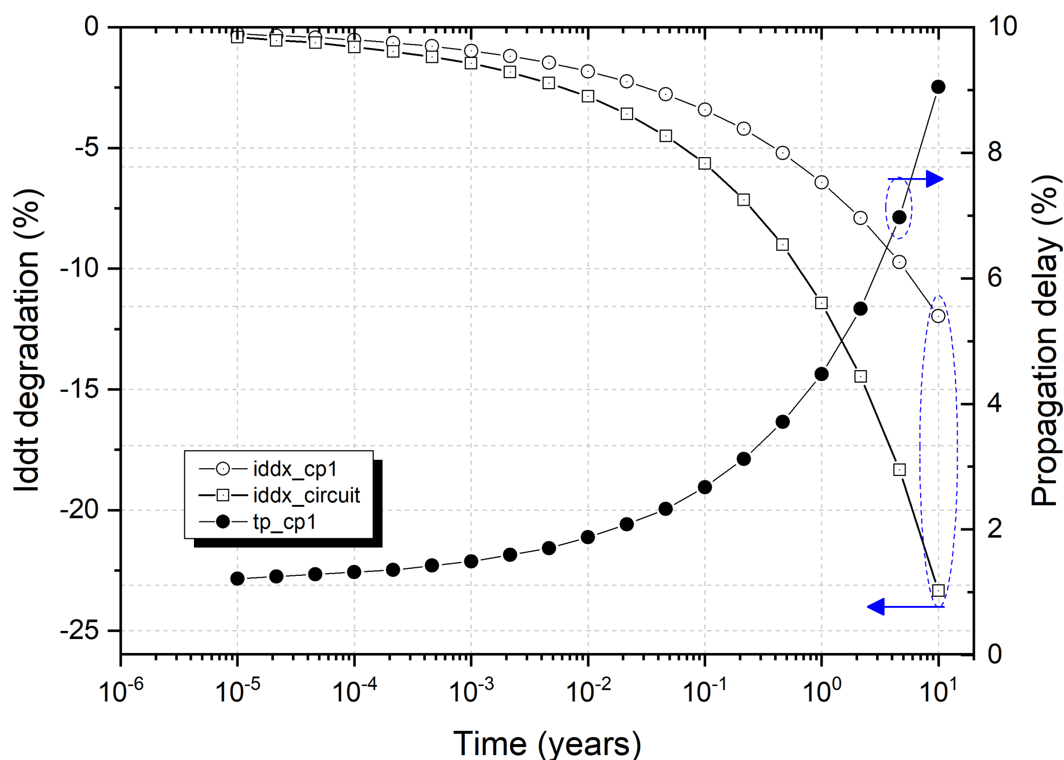


Figure 6.9: I_{ddt} & propagation delay degradations in 16-bit multiplier.

Based on the timing report generated by synthesising the OpenRisc 1200 processor, the majority of the first 100 critical paths are passing through two major circuit block – the Arithmetic Logic Unit (ALU) and the multiplier. This information can be used to position the current sensor. These functional circuit block can

be classified as critical circuit block for a sensor circuit to monitor its current degradation. The ALU of the OpenRisc processor was analysed for ageing effects, and the results are depicted as Figure 6.9.

Based on four degradation curves shown in Figure 6.9, the delay degradation could potentially increase up to 7.15% and a significant decrease in I_{ddt} current degradation curves for both critical path and the critical circuit block. A decrease of -21.34 is recorded from HSPICE MOSRA simulation for the critical circuit block, that is twice than the critical path measured the degradation of -11.97%. This substantial difference between these two cases is because of the gates count in both cases. A total of 45 gates are counted on the critical path, compared to 1154 gates count for the whole ALU circuits. This is the reason for the increase in I_{ddt} current degradation between these two cases.

6.6 Over Temperature Variations

The relationship between temperature and current has been discussed in Chapter 2.5.3. With the increase of temperature, the drain current is expected to decrease. In this section, the experiment is done to analyse the effect of temperature variation by sweeping the temperature at 300K, 350K and 400K for all cases discussed in the previous subsection.

Figure 6.10 illustrates the results of temperature variance for RISC-V ALU. Both CP propagation delay degradation (%) and supply current degradation (%) are projected in this graph. From Figure 6.10, at $t = 10 years$, both measurements suffered less when $T = 300K$, where the propagation delay is 0.8% compared to 1.05% when $T = 350K$. The worst degradation happened at $T = 400K$, which degraded the propagation delay to 1.55%.

Compared these values to the supply current degradation, the measurement is shown to be more crucial. The supply current degradation is measured at $t = 10 years$ to be at 8%, 15% and 24% for $T = 300K$, $T = 350K$ and $T = 400K$,

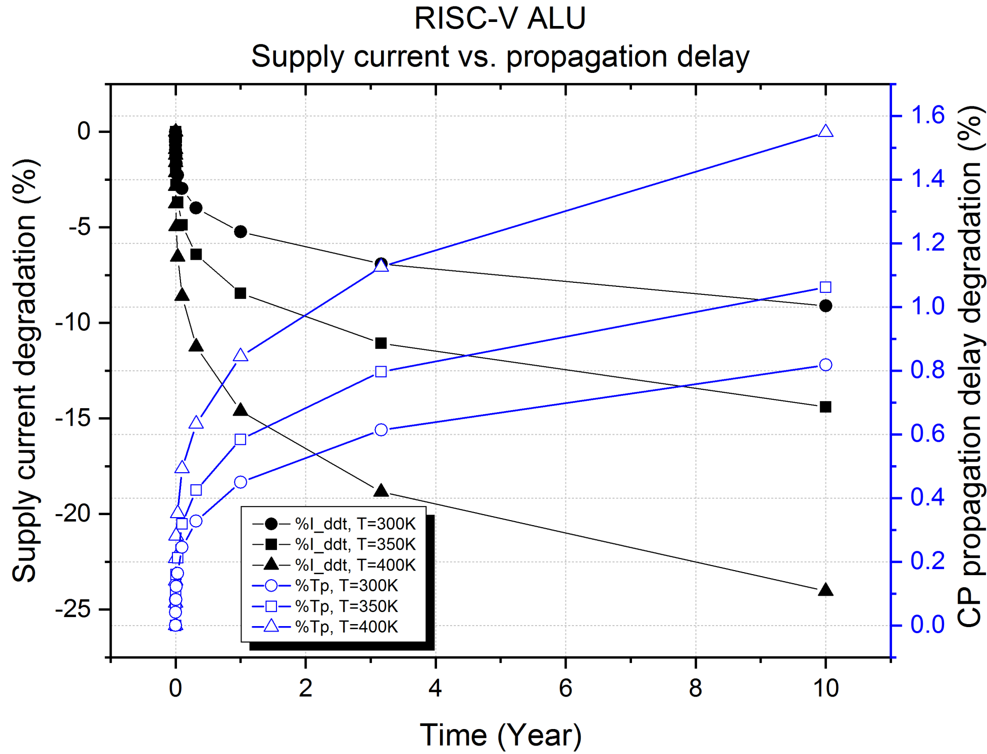


Figure 6.10: RISC-V ALU over different temperature variance of 300K, 350K, 400K

respectively. The same pattern of degradation can be observed in Figure 6.11, Figure 6.12 and Figure 6.13.

Table 6.5 tabulates and summarized the data measured in this section for all 4 circuits: RISC-V ALU circuit, OpenRISC 1200 ALU circuit, 4-bit adder, and ISCAS c6288 (16-bit multiplier) circuit, for all 3 temperature variance.

Based on these result, it is clear that the circuits underwent much severe stress at a higher temperature. All measurement reflects the same for both parameters measured. From observation, all four circuits inherit the same pattern of degradation of t_p and worst for I_{dtt}. The degradation of t_p is measured at 1.55% for both ALU circuits but higher for adder circuits. The 4-bit adder circuit suffers 2.25% of t_p degradation and slightly higher for 16-bit multiplier circuit at 3.75%. The increase in the adder circuit is closely related to the operation of the circuit under stress during the simulation.

The 16-bit multiplier circuit has a higher t_p degradation because of the shared

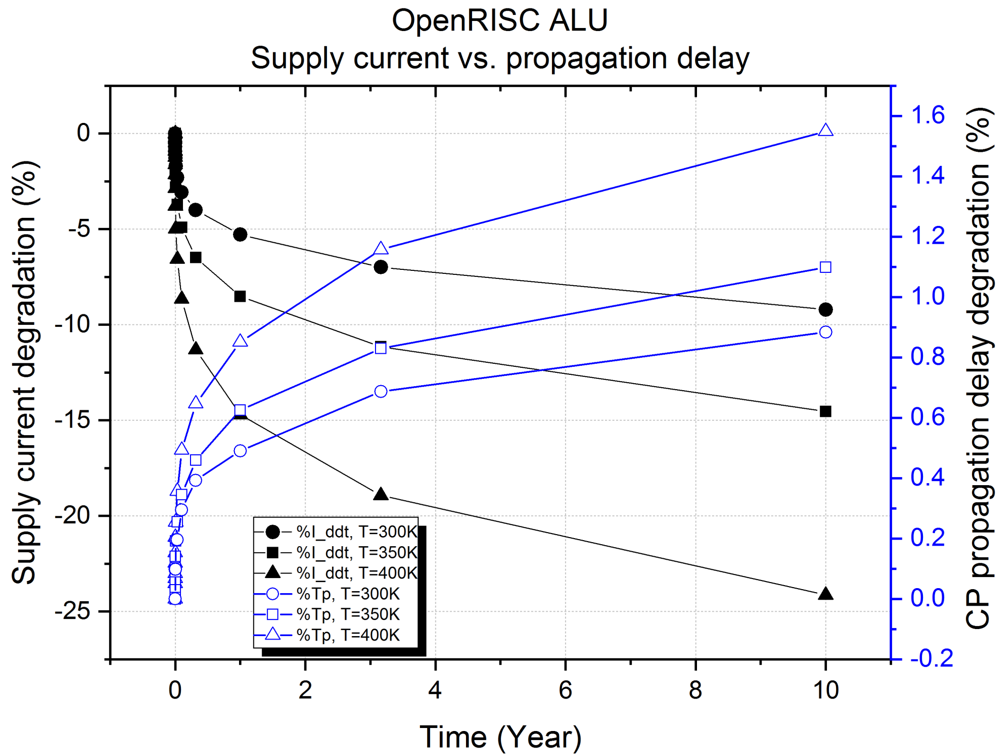


Figure 6.11: OpenRISC 1200's ALU over different temperature variance of 300K, 350K, 400K

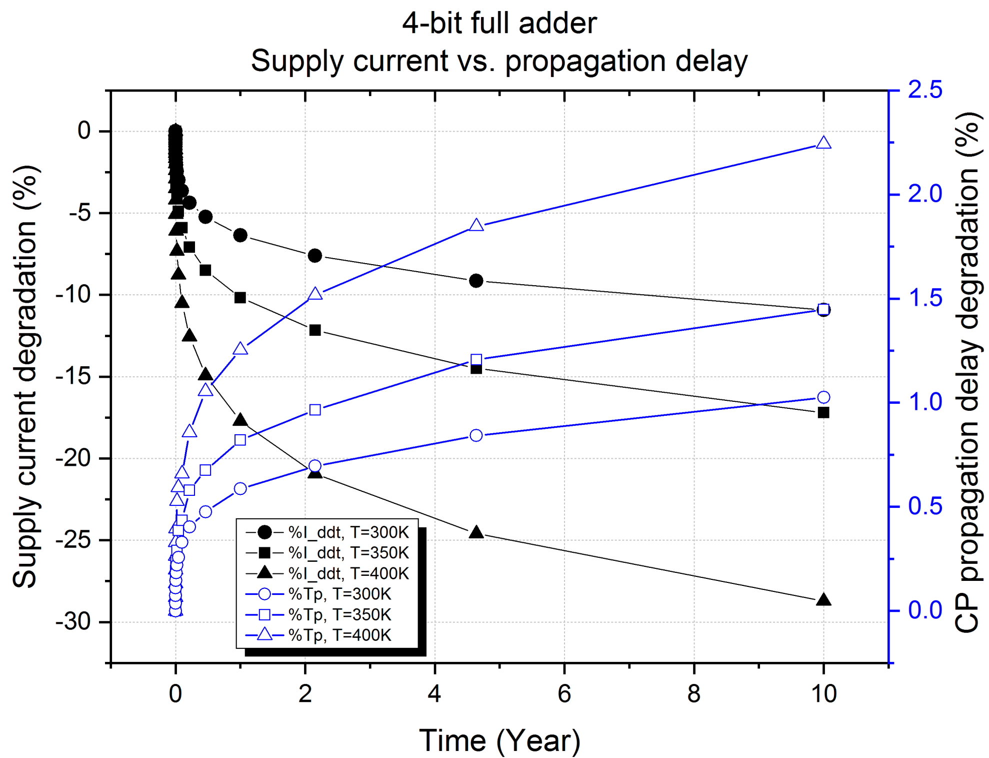


Figure 6.12: Four-bit adder over different temperature variance of 300K, 350K, 400K

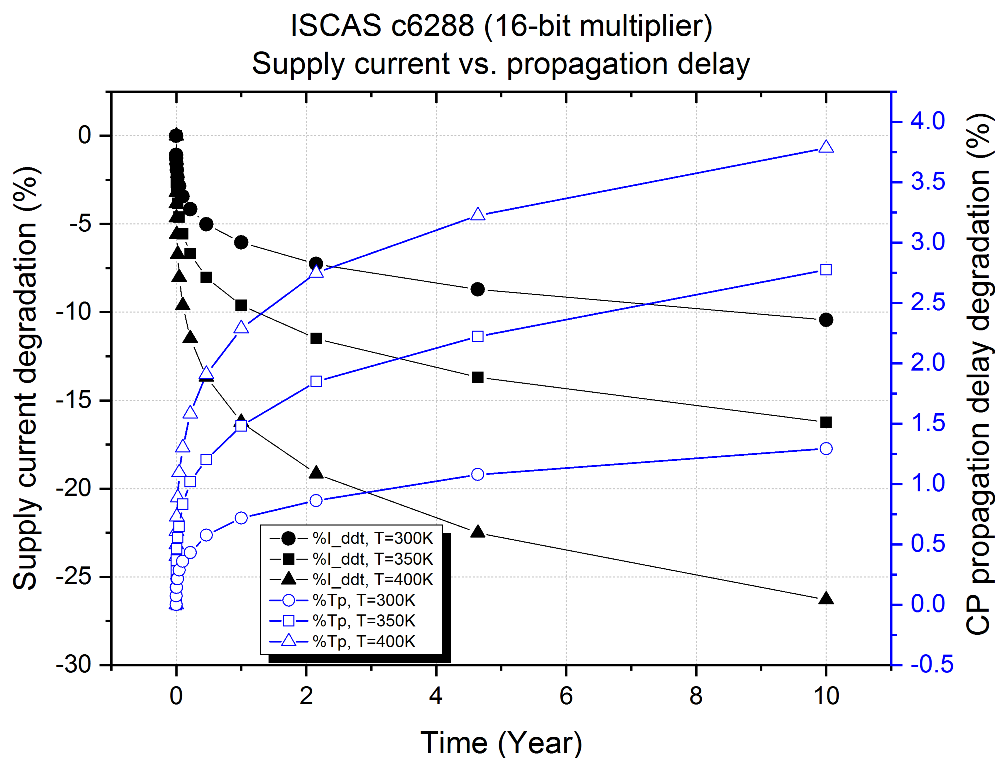


Figure 6.13: 16-bit multiplier (ISCAS c6288) over different temperature variance of 300K, 350K, 400K

critical path being stress or underused by most of the other branches of other paths. This stress put pressure on the said critical path, hence contributing to a higher percentage of ageing on this circuit. Similar case happens to 4-bit adder circuit where the sum 0 paths (the most critical path for 4-bit adder) is being stressed and used by most of the other path quite often than the rest of the circuit.

Comparing this to the degradation of the ALU for both processor architecture, the percentage of circuitry in the ALU being stressed most of the time is quite small compared to the adder circuit. It depends on which of the ALU function is being used. Thus this slows gives a smaller effect on the degradation of the propagation delay.

Changing our view to the current degradation delay perspective, all four circuits show similar attributes, where at $t = 10years$, the current degradation is measured not less than 24%. This significant changes in term of degradation from $t = 0$ to

Table 6.5: Summary for the t_p and I_{ddt} degradation over temperature variance of 300K, 350K and 400K for four different circuits.

	Temperature	$T = 300K$	$T = 350K$	$T = 400K$
RISC-V ALU	t_p	0.8%	1.05%	1.55%
	I_{ddt}	8%	15%	24%
OR1k2 ALU	t_p	0.9%	1.1%	1.55%
	I_{ddt}	9%	14%	24%
4-bit adder	t_p	1.0%	1.4%	2.25%
	I_{ddt}	11%	17.5%	28%
ISCAS c6288	t_p	1.25%	2.75%	3.75%
(16-bit multiplier)	I_{ddt}	10%	17%	26%

$t = 10years$ are seen from 0% to $\sim$ 25% for current degradation and from 0 to $\sim$ 5%.

This is significant in term of measuring or monitoring the degradation of a circuit. These differences are crucial for any monitoring scheme to predict the ageing of any CMOS circuit.

6.6.1 Monitoring An Ageing Circuit

Predicting ageing effects by deploying two types of monitoring circuit could give an advantage in providing information about a dying circuit. The degradation of I_{ddt} current is shown to suffer more compared to delay degradation. Based on the results from the ALU of the OpenRisc processor, the I_{ddt} current degradation is calculated to be almost three times more compared to the delay degradation.

The ALU circuit is just one example of how the I_{ddt} current degradation can be useful to monitor ageing. It is possible to apply the same approach to other

circuits. A consideration of selecting the critical functional circuit block would increase the possibility of monitoring the I_{ddt} current.

The delay degradation is usually measured digitally. However, the I_{ddt} current sensor circuit has to be an analogue circuit. In order to analyse both data, an arbiter circuit is needed. Ageing effects monitoring is possible to be implemented in a system that required to last for years, for example, in space and military purposes, instead of for commercialised consumer product. Moreover, for that, system-level applications could become the arbiter to analyse this information provided by the two different sensors.

This technique for analysing the I_{ddt} current can be executed for any pre-determined time window, specified by the arbiter circuit or at the system level. The test pattern can be a process that is run by the processor and does not has to be a separate test pattern. For example, a pre-determined process/program that consists of a series of known operations, i.e. addition and multiplication, with specific input data can be flagged as an input for the test to be executed. Such known test pattern will have its time frame of $[t_0 : t_{end}]$ (t_0 as the start and t_{end} as the end of test). This time-lapse of completing the process is taken to be the detection window for the circuit.

This pre-determined process/program can be a part of the real circuit operations. The arbiter will have to know that this specific flagged program beforehand during the program counter operations. As the processor executes the flagged program, the arbiter will trigger the sensor circuit to monitor that specific time window, while not interrupting the processor operation. This strategy would give a unique attribute to the sensor as being non-interruptive for the processors' operations.

6.7 Monitoring Circuits Implementation and Challenges

The implementation of the monitoring circuit for the presented technique is quite generic and simple to design by utilizing a series of data processing circuitry such as Built-in-Current-Sensor, ADC, comparator and etc. However, the challenge for designing an on-line sensor is its requirement for high-speed detection and high resolution of the current to be measured. The new perspective presented in this chapter can be used to solve the problem of small current values by observing the current from the critical functional circuit block that would increase the absolute currents.

Table 6.6 and Table 6.7 shows the measured parameters' absolute values at $t = 0$ and $t = 10$ years for references. As we expected, bigger circuits such as the ALUs has a higher degradation magnitude because of the total number of gates and devices. Comparing the Critical Path and the whole circuit, the value has a quite significant difference. It is worth to point out that in most huge circuitry such as ALUs, the Critical Path consists of the majority of the gates in the circuit.

Table 6.6: The absolute values for I_{ddt} presented in Section 6.4 and 6.5.

	Time, t	**t = 0**	**t = 10 years**	Δ
NAND gate	I_{ddt}	2.27x10^{-5}	1.85x10^{-5}	-0.42x10^{-14}
NOR gate	I_{ddt}	1.30x10^{-4}	1.04x10^{-4}	-0.26x10^{-13}
32-bit adder	I_{ddt}(CP1)	8.20x10^{-5}	7.04x10^{-5}	-1.16x10^{-14}
	I_{ddt}(circuit)	2.69x10^{-3}	2.28x10^{-3}	-0.41x10^{-12}
ALU of OR1k2	I_{ddt}(CP)	6.83x10^{-3}	6.02x10^{-3}	-0.81x10^{-12}
	I_{ddt}(circuit)	2.20x10^{-1}	1.69x10^{-1}	-0.51x10^{-10}

The current degradations for all circuit under test are tabulated in Table 6.6. The table shows that NAND gate current degradation is just a magnitude different from NOR gates. NAND gate suffers as much as -0.42x10^{-5} in I_{ddt} degradation

Table 6.7: The absolute values for t_p presented in Section 6.4 and 6.5.

	Time, t	**t = 0**	**t = 10 years**	Δ
NAND gate	t_p	7.84x10^{-12}	8.52x10^{-12}	0.68x10^{-12}
NOR gate	t_p	2.40x10^{-11}	2.56x10^{-11}	0.16x10^{-11}
32-bit adder	t_p(CP1)	9.42x10^{-10}	9.98x10^{-10}	0.56x10^{-10}
	t_p(CP2)	2.80x10^{-10}	2.96x10^{-10}	0.16x10^{-10}
	t_p(CP3)	2.50x10^{-10}	2.65x10^{-10}	0.15x10^{-10}
ALU of OR1k2	t_p(CP)	3.21x10^{-10}	3.43x10^{-10}	0.22x10^{-10}

compared to -0.26x10^{-4} for NOR gate. This can be explained by looking at the CMOS topology for both gates as depicted in Figure 6.14. NOR gate is expected to suffer more in current degradation because both of its PMOS transistors are connected in series. One transistor ageing would directly affect the other. Unlike the NAND gate, the PMOS transistor is connected in parallel. One transistor ageing would not directly affect the neighbouring transistor.

The same explanation is valid to explain the delay degradation for both gates, as seen in Table 6.7. The result shows that the NAND gate has a delay of 0.68x10^{-12} for ten years stress test compared to 0.16x10^{-11} for NOR gate.

For the 32-bit adder and the ALU of OpenRISC1200, the difference is significant because it is clearly known that ALU has a greater number of gates compared to the adder circuit. The delay degradation in ALU of OpenRISC1200 is greater simply because it has longer Critical Path and has a higher value in current because of the number of gates.

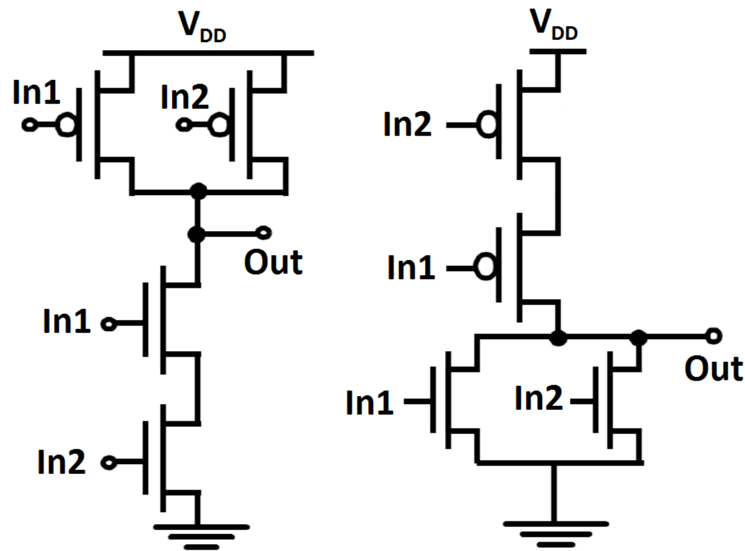


Figure 6.14: CMOS topology for NAND and NOR gate.

6.8 Conclusion

An alternative means of measuring I_{ddt} current degradation for monitoring circuit ageing caused by BTI and HCI is presented in this chapter. The result shows that the I_{ddt} current degradation follows the delay degradation closely. The I_{ddt} current degradation exhibit more degradation percentile for three different areas of measurements; the critical gate, the critical path, and the critical functional circuit block. The behaviour of I_{ddt} current degradation suggested that having this type of sensor as a secondary monitor would provide more accuracy in monitoring CMOS circuit ageing. The results presented in this chapter proved the feasibility of implementing the current based sensor for monitoring ageing on a very large CMOS circuit.

Chapter 7

Conclusion

7.1 Conclusions

An ageing effects detection method for detecting NBTI ageing based on the degradation of drain current has been studied. The initial SPICE simulation demonstrates the significance of drain current degradation in NBTI-induced circuit. A consideration for opting this technique as a counterpart for the existing monitoring method based on delay degradation could considerably improve the detection mechanism in CMOS circuits.

Ageing effects has been discussed to have negative effects for digital and analogue circuits in sub-100 nm CMOS technologies. Persistent oxide thickness downscale has led to an increase in electric fields in MOSFET devices, tunnelling effects, and other temporal and ambiguous failures. Disproportionate scaling of device geometries with downscaling of the power supply also becomes the main factor for the ageing effects. Bias temperature instability (BTI), time-dependent dielectric breakdown (TDDB), and hot carriers injection (HCI) are the most critical ageing effects related that have been identified to cause the transistor to aged drastically through time during operation.

The importance of having a different mechanism in ageing prediction has been discussed in detail. The prospect of observing the drain current degradation is

very promising since the degradation in current is more significant than the delay degradation. The I_{ddt} current degradation is observed to suffer -23.34% from its "fresh" current compared to 1.55% in delay degradation for RISC-V ALU circuit. A similar pattern of degradation in I_{ddt} and delay has been recorded to be valid for OpenRISC 1200 ALU, the 4-bit adder and the 16-bit multiplier (ISCAS c6288). The degradation is worsening in high temperature as pointed out in literature and proved by the result as discussed in Chapter 6.

I_{ddt} testing of CMOS digital circuits has been recognised as an advantageous methodology to detect defects; fault, variability, ageing effect, single event upset. The benefits of this methodology have been recognised because of the enhanced observability and sensitivity. However, the advancement of circuit design limited the development for this type of testing. With the sophisticated design for a test in the present, this method for measuring small current could be more useful for implementation.

The results from this research have shown promising utilisation of I_{ddt} testing for ageing effects for any CMOS circuitry. With the significance drain current degradation caused by the ageing effect, the prediction for ageing circuits could have a better resolution and precision. Any defective or ageing circuits can be notified much better especially in the crucial application such as space exploration, military weaponry system, aviation industry and medical instruments since an ageing circuit could bring disaster quicker that one usually intended.

7.2 Future Enhancement

The research work that has been presented in this thesis has successfully met the research objectives outlined in Section 1.2. However, further improvements could be carried out and oriented towards incorporating all known ageing effect, including TDDB and electro-migration. There are not many tools in the market that could provide such features.

The technology used in this research is limited to 32nm bulk CMOS technology. The ageing effects are known to affect all different type of CMOS technology such as FinFETs, gate-all-around-FET (GAAFET) and other emerging design which falls in the sub-10nm device region. Similar/worse degradation in drain current is hypothesized to be the same as the bulk CMOS technology. It should get worse as the device geometries decreased.

Appendix A

SYNOPSYS® HSPICE® MOSRA Manual

19

MOSFET Model Reliability Analysis (MOSRA)

Describes the procedures for HSPICE MOSFET reliability analysis (MOSRA).

The following sections cover the these topics:

- MOSRA Overview
- MOSRA Commands and Control Options
- Level 1 MOSRA BTI and HCI Model Parameters

MOSRA Overview

As the industry scales down CMOS technology, reliability requirements to maintain the long-term device become both more challenging and more important. Two of the most critical reliability issues, the hot carrier injection (HCI) and the bias temperature instability (BTI) can change the characteristics of MOS devices. HSPICE reliability analysis allows circuit designers to predict the reliability of their design to allow enough margin for their circuits to function correctly over their lifetime.

A unified custom reliability-modeling API is available or custom reliability model development. Contact your Synopsys technical support team for more information about the MOSRA API.

HSPICE MOSRA analysis currently supports Level 49, Level 53, Level 54, Level 57, Level 66, Level 69, Level 70, Level 71, and Level 73, and external CMI MOSFET models.

The following sections discuss these topics:

- Reliability Analysis Use Model
- Example Setup

Reliability Analysis Use Model

HSPICE reliability analysis (or HCI and BTI analysis), is a two-phase simulation: the fresh simulation phase and the post-stress simulation phase. The two-phase simulation can run separately or together.

- Fresh simulation phase: HSPICE computes the electron age/stress of selected MOS transistors in the circuit based on circuit behavior and on the HSPICE built-in stress model including HCI and/or BTI effect.
- Post-stress simulation phase: HSPICE simulates the degradation effect on circuit performance, based on the stress information that the fresh simulation phase produces.

Figure 102 presents the HSPICE reliability analysis process.

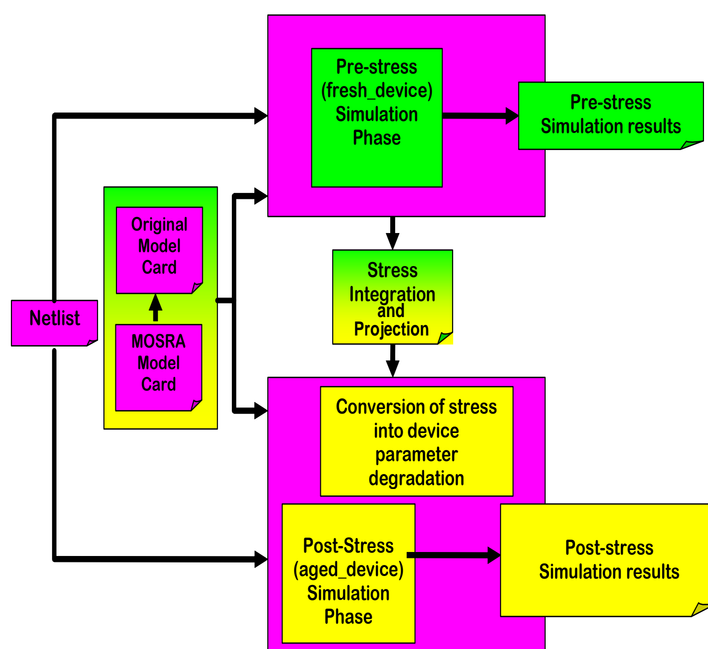


Figure 102 HSPICE Reliability Simulation Flow

Example Setup

The following example file demonstrates how to set up a HSPICE reliability reliability analysis.

```
* MOSRA TEST
vdd 1 0 2
mp1 3 2 1 1 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
mn1 3 2 0 0 n1 l=0.1u w=5u ad=5p pd=6u as=5p ps=6u
mp2 4 3 1 1 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
mn2 4 3 0 0 n1 l=0.1u w=5u ad=5p pd=6u as=5p ps=6u
mp3 2 4 1 1 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
mn3 2 4 0 0 n1 l=0.1u w=5u ad=5p pd=6u as=5p ps=6u
c1 2 0 .1p

.model p1 pmos level=54 version=4.5
.model n1 nmos level=54 version=4.5

.model p1_ra mosra level=1
+tit0 = 5e-8  titfd = 7.5e-10  tittd = 1.45e-20
+tn = 0.25

.appendmodel p1_ra mosra p1 pmos
.mosra reltotaltime=1e8

.ic v(2)=2
.tran .1ps 5ns
.options post
.end
```

MOSRA Commands and Control Options

The following sections discuss these topics:

- .MOSRA
- Getting Measurements in a MOSRA Analysis
- .MOSRAPRINT
- .MOSRA_SUBCKT_PIN_VOLT
- .MODEL
- .APPENDMODEL
- Simulation Output Files

- RADEG Output Sorting (.OPTION MOSRASORT)
- CSV Format Degradation Information (.OPTION RADEGOUTPUT)

.MOSRA

Starts HSPICE HCI and/or BTI reliability analysis.

Syntax

```
.MOSRA RelTotalTime=time_value
+ [RelStartTime=time_value] [DEC=value] [LIN=value]
+ [RelStep=time_value] [RelMode=1|2|3] SimMode=[0|1|2|3]
+ [AgingStart=time_value] [AgingStop=time_value]
+ [AgingPeriod=time_value] [AgingWidth=time_value]
+ [AgingInst="inst_name"]
+ [Integmod=0|1|2] [Xpolatemod=0|1|2]
+ [Tsample1=value] [Tsample2=value]
+ [Agethreshold=value] [DegradationTime=value]
+ [MosraLlife=degradation_type_keyword] [DegF=value]
+ [DegFN=value] [DegFP=value]
+ [Frequency=value]
```

Argument	Description
RelTotalTime	Final reliability test time to use in post-stress simulation phase. Required argument where *time_value* can be in units of: ▪ sec (default with no unit entry required) ▪ min ▪ hr ▪ day ▪ yr
RelStartTime	Time point of the first post-stress simulation. Default is 0.
DEC	Specifies number of post-stress time points simulated per decade.
LIN	Linear post-stress time points from RelStartTme to RelTotalTime.
RelStep	Post-stress simulation phase on time= RelStep, 2* RelStep, 3* RelStep, … until it achieves the RelTotalTime; the default is equal to RelTotalTime. If you set values for DEC or LIN HSPICE ignores them.

Argument	Description
RelMode	HSPICE reliability model mode selects whether a simulation accounts for both HCI and BTI effects or either one of them. If you define the RelMode in the `.MOSRA` command as 1 or 2, it takes higher priority and applies to all MOSRA models. If you do not set its value or enter 0, RelMode in the .MOSRA command, then the RelMode inside individual MOSRA models takes precedence for that MOSRA model only; the rest of the MOSRA models take the RelMode value from the `.MOSRA` command. If you set any other value, except 0, 1, or 2, HSPICE issues a warning, and RelMode automatically resets to the default value 0. ▪ 0: both HCI and BTI, Default ▪ 1: HCI only ▪ 2: BTI only
SimMode	▪ 0: Select pre-stress simulation only ▪ 1: Select post-stress simulation only ▪ 2: Select both pre- and post-stress simulation, Default ▪ 3: Select continual degradation integration through alters See also, MOSRA Support for DC/AC/MC Analysis in Post-Stress Simulation. When `SimMode=1`: ▪ HSPICE reads in the `*.radeg0` file, updates the device model for reliability analysis; then generates a new transient-output in a `*.tr1` waveform file. ▪ The `*.radeg` file and input netlist must be in the same directory. ▪ The netlist stimuli could be different from the SimMode=0 netlist that generated the `*.radeg` file. When `SimMode=3`: ▪ If you do not specify `.option radegfile` in the top level netlist, simulation starts from fresh device. ▪ If you specify `.option radegfile` in the top level netlist, HSPICE reads in the last suite degradation in the `radeg` file, and continues the degradation integration and extrapolation from the corresponding circuit time in the `radeg` file. ▪ In consecutive alters, HSPICE reads in the `radeg` generated from the previous `alter` run. See also Usage Model: SimMode=3 (continual degradation integration through alters) **Note**: You can use the command-line option `-mrasim` to overwrite the value of `SimMode` in a `.MOSRA` command card. Possible values are: ▪ 0: Selects pre-stress simulation only ▪ 1: Selects post-stress simulation only ▪ 2: Selects both pre- and post-stress simulation ▪ 3: Selects continual degradation integration through `.ALTERs`

Argument	Description
AgingStart	Optionally defines time when HSPICE starts stress effect calculation during transient simulation. Default is 0.0.
AgingStop	Optionally defines time when HSPICE stops stress effect calculation during transient simulation. Default is tstop in `.TRAN` command.
AgingPeriod	Stress period. Scales the total degradation over time.
AgingWidth	The AgingWidth (circuit time "on") argument works with the AgingPeriod argument. For example: if you specify AgingPeriod=1.0s and AgingWidth=0.5s, then the circuit turns on for 0.5s, and turns off for 0.5s. (The period is 1.0s.)
AgingInst	Selects MOSFET devices to which HSPICE applies HCI and/or BTI analysis. The default is all MOSFET devices with reliability model appended. You must enclose the name in quotes. HSPICE allows Multiple names /and supports wildcards.
Integmod	The flag selects the integration method and function. ▪ 0 (default): User-defined integration function in MOSRA API ▪ 1: True derivation and integration method ▪ 2: Linearized integration method (support non-constant n coefficient)
Xpolatemod	The flag selects the extrapolation method and function. ▪ 0 (default): User-defined extrapolation function in MOSRA API ▪ 1: Linearization extrapolation method (support non-constant n coefficient) ▪ 2: Two-point fitting extraction and extrapolation method
Tsample1	First simulation time point of stress_total sampling for Xpolatemod=2
Tsample2	Second simulation time point of stress_total sampling for Xpolatemod=2
Agethreshold	Only when the degradation value >= Agethreshold, the MOSFET information is printed in the MOSRA output file `*.radeg` or `*.cvs` file. Default is 0.
DegradationTime	If you specify this argument, the MOSRA API calculates the degradation at the degradation time, and generates a `.degradation` output file.
MosraLife	Argument to compute device lifetime for the degradation type specified. This argument has the same function as `.option mosralife.`
DegF	Sets the MOSFET's failure criteria for lifetime computation. This argument has the same function as `.option degf`. If you specify `.option degf`, it takes precedence over `.mosra degf`.
DegFN	Sets the NMOS's failure criteria for lifetime computation. This argument has the same function as `.option degfn`. If you specify `.option degfn`, it takes precedence over `.mosra degfn`.

Argument	Description
DegFP	Sets the PMOS's failure criteria for lifetime computation. This argument has the same function as `.option degfp`. If you specify `.option degfp`, it takes precedence over `.mosra degfp`.
Frequency	User-specified frequency of the signal for BTI frequency-dependent recovery effect calculus. If you do not specify a value, The API automatically calculates it.

Description

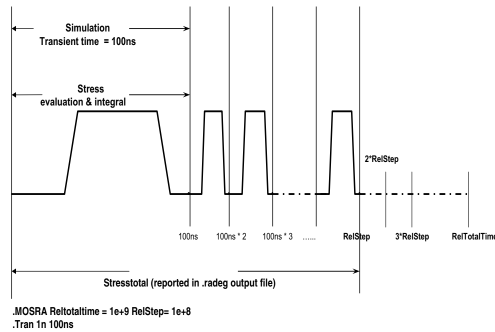
Use the `.MOSRA` command to initiate HCI and BTI analysis. This is a two-phase simulation, the fresh simulation phase and the post stress simulation phase. During the fresh simulation phase, HSPICE computes the electron age/stress of selected MOS transistors in the circuit based on circuit behavior and the HSPICE MOSFET reliability model. During the post stress simulation phase, HSPICE simulates the degradation effect on circuit performance, based on the stress information produced during the fresh simulation phase.

If you specify either DEC or LIN the API ignores the RelStep value. See Figure 103 on page 614 for an illustration of the `.MOSRA` command/syntax.

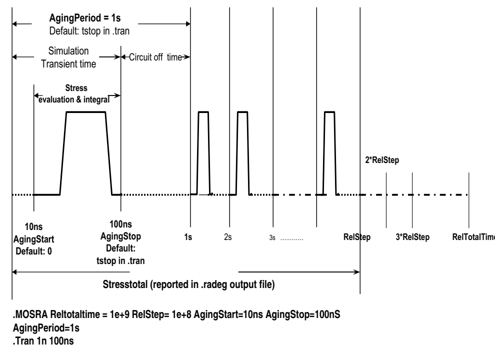
Example

```
.mosra reltotaltime=6.3e+8 relstep=6.3e+7
+ agingstart=5n agingstop=100n
+ aginginst="x1.*"
```

Command/syntax for HSPICE reliability simulation (1/3)



Command/syntax for HSPICE reliability simulation (2/3)



Command/syntax for HSPICE reliability simulation (3/3)

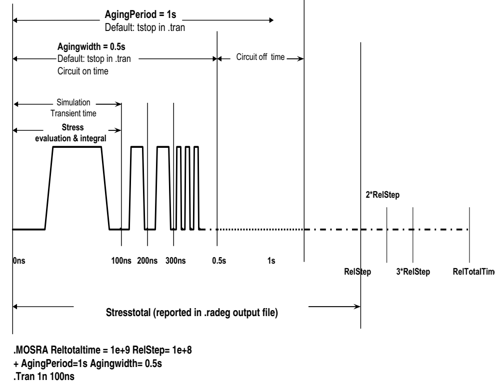


Figure 103 Graphic Illustration of MOSRA Command/Syntax

MOSRA Support for DC/AC/MC Analysis in Post-Stress Simulation

HSPICE MOSRA supports the DC/AC and Monte Carlo sweep in a `SimMode=1` Post-stress simulation. (HSPICE does not support `SimMode=0/2`.) A general MOSRA netlist must specify `SimMode = 1` in the `.MOSRA` command line to start the Post-stress simulation, and provide previously generated device degradation information through a user-specified *.radeg* input file. The syntax is as follows:

```
.mosra reltotaltime='10*365*24*60*60' lin=11 simmode=1
.option radegfile = 'radeg file name'
```

Then you can specify the DC/AC analysis command. You can combine analysis commands with different sweeps (including Monte Carlo sweep).

```
.dc vdd 0 -1.2 -0.1 sweep monte=10
.ac dec 1 1e5 1e9 sweep parm1 25 75 125
.tran 1n 10n sweep monte=10
```

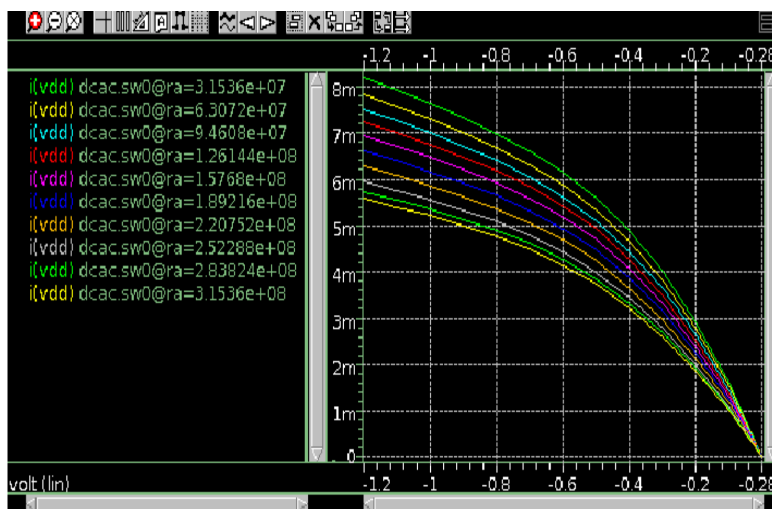
Examples

The following example netlist does a DC and AC simulation in MOSRA post-stress.

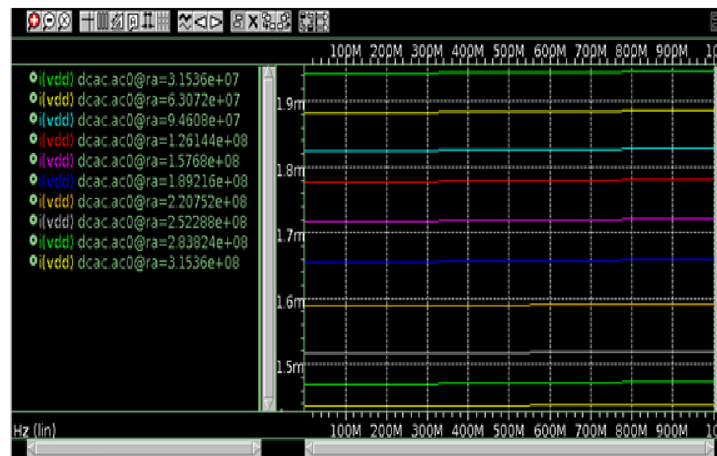
```
* MOSRA DC/AC TEST

.option radegfile = 'simmode2.radeg0'

vdd 1 0 -2 ac=1
mp1 1 2 0 0 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
vgs 2 0 -2

.model p1 pmos level=54 version=4.5

.model p1_ra mosra level=1

.appendmodel p1_ra mosra p1 pmos

.mosra reltotaltime='10*365*24*60*60' lin=11 simmode=1
.dc vdd 0 -1.2 -0.1
.ac dec 1 1e5 1e9
.options post
.print dc i(vdd)
.print ac i(vdd) ii(vdd)
.end
```

HSPICE parses the specified *radeg* file and do the post-stress simulation in the specified relstep, then generate the corresponding DC/AC output files:

```
dcac.sw0@ra=3.1536e+07
dcac.sw0@ra=6.3072e+07
dcac.sw0@ra=9.4608e+07
dcac.sw0@ra=1.26144e+08
dcac.sw0@ra=1.5768e+08
dcac.sw0@ra=1.89216e+08
dcac.sw0@ra=2.20752e+08
dcac.sw0@ra=2.52288e+08
dcac.sw0@ra=2.83824e+08
dcac.sw0@ra=3.1536e+08
```




```
dcac.ac0@ra=1.89216e+08
dcac.ac0@ra=2.20752e+08
dcac.ac0@ra=2.52288e+08
dcac.ac0@ra=2.83824e+08
dcac.ac0@ra=3.1536e+08
```



The following example netlist does a DC plus Monte Carlo simulation in MOSRA post-stress.

```
* MOSRA DC/MONTE TEST
.option radegfile = 'simmode2.radeg0'
vdd 1 0 -2
mp1 1 2 0 0 p1 l=0.1u w=10u ad=5p pd=6u as=5p ps=6u
vgs 2 0 -2
.param
+random1=AGAUSS(0,1,3)
+par1=random1
+A1_ms='par1*5.5225/2.0*3'
+toxn_ms_global ='(-9.462e-11)*A1_ms'
.model p1 pmos level=54 version=4.5
+ toxe = '3e-9 + toxn_ms_global'
.model p1_ra mosra level=1
.appendmodel p1_ra mosra p1 pmos
.mosra reltotaltime='10*365*24*60*60' lin=11 simmode=1
.dc vdd 0 -1.2 -0.1 sweep monte=10
.options post
.print dc i(vdd)
.end
```

Getting Measurements in a MOSRA Analysis

See Measurements in MOSRA Analysis in Chapter 12, Simulation Output for instructions on generating multiple measurement files.

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