A Flexible and Decoupled Space Vector Modulation Scheme With Carrier-Based Implementation for Multilevel Converters

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Abstract—This article proposes a novel space vector pulse width modulation (SVPWM) scheme for multilevel converters in *abc* coordinate system, in which the reference vector is decomposed into an offset vector and a remainder vector that can be synthesized using two-level SVPWM. The switching state satisfying a specific relationship is first selected as the offset vector such that the common-mode components are eliminated and therefore the phase voltages are decoupled. A dynamic reference point mechanism establishes a one-to-one correspondence between all available vector combinations and one unique variable, i.e., the number of level shifts. This feature further facilitates a general approach to determining the optimum switching states to satisfy different control objectives, such as common-mode voltage rejection. Besides, phase decoupling enables the introduction of carrier-based modulation to simplify implementation, where the duty cycle of the zero vector can be flexibly adjusted while the non-zero vectors remain the same to generate an equivalent output. Consequently, two-level SVPWM-based method and carrier-based PWM are combined to exploit their respective strengths. The proposed scheme achieves overmodulation operation, and provides more flexibility, i.e., redundant switching states and adjustable duty cycles, to optimize switching patterns. Simulation and experimental results validate the proposed algorithm.

Index Terms—Multilevel converter, space vector pulse width modulation (SVPWM), dynamic reference point mechanism, carrier-based implementation.

ABBREVIATION

CBPWM   Carrier-based PWM.
CHB   Cascaded H-bridge.
CMV   Common-mode voltage.
FC   Flying capacitor.
NLM   Nearest level modulation.
NTVs   Nearest three vectors.
OSS   Optimum switching state.
PDPWM   Phase-disposition PWM.
PWM   Pulse width modulation.

RP   Reference point.
RSC   Redundant switching combination.
RSS   Redundant switching state.
RVV   Reference voltage vector.
SVD   Space vector diagram.
SVPWM   Space vector PWM.
THD   Total harmonic distortion.

I. INTRODUCTION

MULTILEVEL converters with their advantages of low total harmonic distortion (THD), high power density, low voltage stress, high efficiency, and low *dv/dt* have been widely used in machine drives, train traction, photovoltaic power generation, and ship propulsion systems [1]–[4]. Amongst them, the neutral-point clamped, flying capacitor (FC) and cascaded H-bridge (CHB) converters have been the most popular topologies [5]–[7]. Along with the growth of the multilevel topologies, various pulse width modulation (PWM) techniques have been developed: carrier-based PWM (CBPWM), including phase-shifted PWM [8], [9] and phase-disposition PWM (PDPWM) [10]–[12]; space vector PWM (SVPWM) [13]–[15]; and nearest level modulation (NLM) [16], [17]. Compared with the other two methods, SVPWM provides higher voltage utilization and more flexibility to optimize converter's performance via redundant switching states (RSSs). Therefore, SVPWM has become more widespread as a solution for multilevel converters.

The implementation of conventional multilevel SVPWM can be divided into the following four steps [18]: 1) identifying the location of the reference voltage vector (RVV); 2) selecting the switching states of the nearest three vectors (NTVs); 3) calculating the duty cycles; 4) generating the switching sequence and gate pulses. However, an n-level converter has n^3 switching states and $6(n-1)^2$ triangle sectors [19], leading to increased computational complexity to deal with the first two steps as the number of levels increases. Moreover, the last two steps become particularly tedious. In other words, as the number of levels increases, the synthesis of the RVV becomes more complicated and computationally more demanding. This has stimulated research into generalized, flexible and computationally efficient modulation schemes.

In carrier-based implementations [20]–[22], an output equivalent to SVPWM is achieved by injecting a zero-sequence component into the reference voltage, thus avoiding the time-consuming calculation needed to identify the NTVs. More

importantly, the switching sequence along with gate pulses are naturally generated by comparison with triangular carriers. However, similar to CBPWM, carrier-based SVPWM does not effectively utilize RSSs to achieve specific optimization objectives, which may lead to high common-mode voltage (CMV) and non-uniform power loss distribution amongst the switching devices.

Other multilevel SVPWM schemes use nonorthogonal coordinate systems such as the *gh* coordinate [23], 45° coordinate [3], [24], line voltage coordinate [25], [26], and others [18], [19]. In these methods, the RVV can be synthesized using simple mathematical operations, as the space vector diagram (SVD) coordinates are all integers and there are no RSSs in these nonorthogonal coordinate systems. Also, sector judgment and trigonometric operation are typically avoided. However, the key issue with most of these approaches is that intricate coordinate transformation and inverse transformation are required, and RSSs need to be compared with each other and properly selected when transferred back to *abc* coordinates, which complicates the process and hinders application.

Other common approaches are based on two-level SVPWM [27]–[38]. In [27], the synthesis of a given RVV is simplified by decomposing a multilevel SVD into its constituent two-level hexagons. The RVV is then decremented by the voltage vector that locates the origin of the two-level hexagon where the RVV lies to produce a remainder vector within it. This enables the calculation of the duty cycles in a similar way to two-level SVPWM. In [29], the origin of the two-level hexagon containing the RVV is located by a first mapping that iteratively locates the origins of the surrounding set of larger nested hexagons starting with the central origin. This eliminates the need for look-up tables and reduces memory requirements. However, as the number of levels increases, the number of mapping iterations and corresponding computational effort increase significantly. The number of iterative calculations is reduced in [30] by decomposing the multilevel SVD into judicially selected two-level SVDs, but look-up tables are now required, which would limit implementation for high number of levels. Therefore, these algorithms share a common problem that their computational complexity or storage requirements rises sharply with the number of levels.
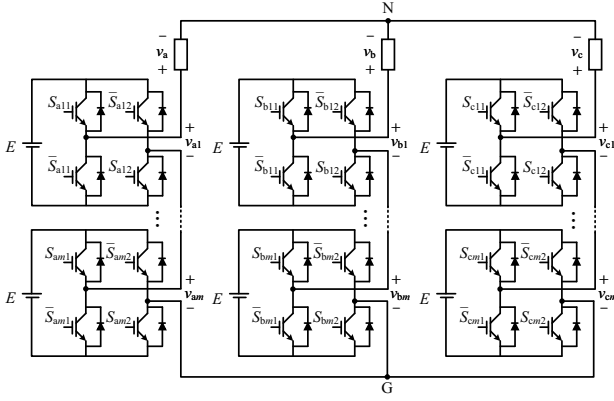
To solve the aforementioned problems, several further simplified techniques have been proposed. In [33], the available origins of the two-level hexagons are reduced to the designated layers, and two discriminant variables are introduced to identify the region containing the RVV. This processing is independent of the number of levels, whereas the acquisition of RSSs and the generation of the switching sequence are not involved. In [34], the RVV is decomposed into an offset vector and a remaining reference vector, in which the offset vector is immediately identified based on phase-voltage modulation, while the calculation of the duty cycles is based on two-level SVPWM. But sector judgment and multi-step mapping needed to determine the switching sequence increase computational and programming complexity. Similarly, the RVV is decomposed into integer part and fractional part in [37], except that switching pulse durations instead of the switching sequence are directly derived from matrix operations. How-

ever, the bulky matrix calculations can undoubtedly lead to low efficiency. In fact, few of these simplified methods involve a systematic solution to determining the switching sequence, and complex encoding is typically required for three or four switching states and their respective duty cycles, which causes extra memory consumption [38]. NLM-based implementations are thus introduced in [5], [38], which encode each phase separately instead of processing all phases simultaneously. Nevertheless, the sequence order has to be alternately reversed to reduce THD. In essence, these methods tend to utilize two-level SVPWM only in the calculation of the duty cycles, while the generation of the switching sequence is irrelevant to it. Besides, alternative RSSs and possible overmodulation operation are normally ignored, either to reduce the computational burden or due to limitations of the algorithm itself.

One of the most prominent features of SVPWM is that the converter's performance can be optimized by appropriately selecting RSSs [13], [25]. Intensive research has been conducted on CMV rejection since it can cause the bearing current, electromagnetic interference and insulation failures [6], [15], [26]. The three switching states with the minimal CMV magnitude in the NTVs are chosen as the output in [6], [33], where only a five-segment sequence is available and thus the CMV cannot be thoroughly eliminated. In [3], zero CMV is achieved at each moment by flexibly converting phase and line voltages, but the switching vectors obtained are not the NTVs, resulting in substantially increased THD. In [19], the time-averaged CMV elimination is achieved within each switching period by introducing a fourth switching state. However, the additional vector judgement and duty cycle redistribution as well as the aforementioned deficiencies in nonorthogonal coordinate systems hinder its application. Furthermore, these approaches generally no longer apply when another converter objective arises. Therefore, a general, versatile and efficient approach for the selection of the optimum switching state (OSS) is still the subject of active research.

This article proposes a novel SVPWM scheme in *abc* coordinate system, which combines two-level SVPWM-based method and CBPWM. Compared with the previous SVPWM methods, the proposed scheme has the following advantages.

1) It avoids look-up tables, trigonometric operation, coordinate transformation, and only requires simple logical judgment and arithmetic calculation. Also, complicated calculation of the duty cycles is avoided.
2) A one-to-one correspondence between all available vector combinations and one unique variable, i.e., the number of level shifts, is established. On this basis, a generalized method is proposed to determine the OSS.
3) The switching sequence along with gate pulses are naturally generated through the PDPWM, which can flexibly adjust the duty cycle of the zero vector by injected zero-sequence components while keeping non-zero vectors unchanged to produce an equivalent output.
4) It provides more flexibility, i.e., RSSs and adjustable duty cycles, to optimize switching patterns.
5) It can be easily configured to operate in the overmodulation region.

Fig. 1. The n-level three-phase CHB converter.

Fig. 2. Space vector diagram of the five-level CHB converter.

Fig. 3. Two-level space vector diagram.

The proposed scheme can be applied to conventional CHB and FC converters, while other converters with different topologies are not discussed in this paper. The rest of this article is organized as follows. Section II outlines the configuration of a candidate multilevel converter system and problems in existing methods. Section III details the proposed modulation scheme. Section IV presents methods for handling overmodulation operation and the case with an even number of levels. The determination of the OSS is described in Section V. Section VI validates the proposed scheme by simulation and experimental results. Section VII concludes this article.

II. SYSTEM DESCRIPTION

A. System Configuration

As shown in Fig. 1, the CHB converter is chosen as a candidate here to illustrate the proposed modulation scheme. Each phase of an n-level CHB converter consists of m ($n = 2m + 1$) H-bridges connected in series. With different switching signals S_{xij}, each H-bridge can output three voltage levels, denoted by $\{0, 1, 2\}$, corresponding to the dc voltages $v_{xi} = \{-E, 0, E\}$, where $x = \{a, b, c\}$, $i = \{1, 2, ..., m\}$, and $j = \{1, 2\}$. By this means, the voltage levels per phase can be yielded as $\{0, 1, 2, ..., n-1\}$, and the combination of three-phase voltage levels forms n^3 switching states.

Referring to [29], the output space vector for an n-level converter in this paper is defined as

$$\boldsymbol{V}_{\text{out}} = V_{\text{dc}}(S_{\text{a}} + S_{\text{b}}e^{j\frac{2}{3}\pi} + S_{\text{c}}e^{j\frac{4}{3}\pi}) \qquad (1)$$

where V_{dc} represents the dc bus voltage for FC converters, while $V_{\text{dc}} = (n-1)E$ for CHB converters, and S_{a}, S_{b}, and S_{c} denote the switching states of phases a, b, and c.

Based on (1), a five-level SVD in *abc* coordinate system is presented in Fig. 2 as an example, where each coordinate of the switching states represents the voltage level of the corresponding phase. Except for those located on the edges of the outer hexagon, the remaining vertices contain more than one switching state, namely RSSs. For instance, the vector $\boldsymbol{OP}$ can be expressed as (2, 1, 0), (3, 2, 1) or (4, 3, 2), which can achieve the same output line voltage but have different impact on specific control objectives, such as CMV cancellation. Also, there are several redundant switching combinations (RSCs) for
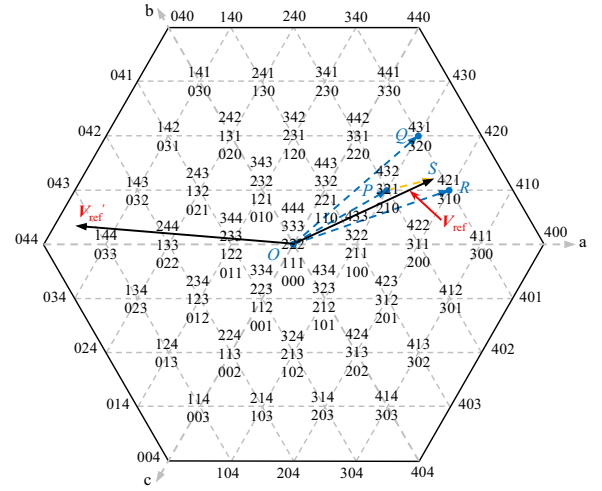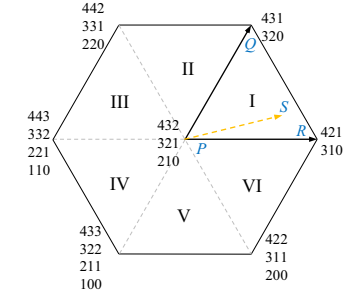
some voltage levels. For example, level 1 can be generated by $(S_{x11}, S_{x12}, S_{x21}, S_{x22})$ with (1, 0, 0, 0), (0, 1, 0, 0), (0, 0, 1, 0) or (0, 0, 0, 1) for a five-level CHB converter. The RSSs along with RSCs complicate the synthesis of the RVV, which is further accentuated as the number of levels increases.

B. Problems in Existing Methods

For multilevel converters, the NTVs are most commonly employed to synthesize the RVV. Taking $\boldsymbol{V}_{\text{ref}}$ in Fig. 2 as an example, the relationship can be described as

$$\boldsymbol{V}_{\text{ref}} = d_1 \boldsymbol{OQ} + d_2 \boldsymbol{OR} + (1 - d_1 - d_2)\boldsymbol{OP} \qquad (2)$$

where d_1 and d_2 represent the duty cycles of the vectors $\boldsymbol{OQ}$ and $\boldsymbol{OR}$, respectively.

By introducing the offset vector, the RVV in two-level SVPWM-based methods can be rewritten as

$$\boldsymbol{V}_{\text{ref}} = \boldsymbol{OP} + d_1 \boldsymbol{PQ} + d_2 \boldsymbol{PR} = \boldsymbol{OP} + \boldsymbol{PS} \qquad (3)$$

where $\boldsymbol{OP}$ and $\boldsymbol{PS}$ are defined as offset vector $\boldsymbol{V}_{\text{off}}$ and remainder vector $\boldsymbol{V}_{\text{rmd}}$, respectively. Obviously, $(\boldsymbol{OQ}, \boldsymbol{QS})$ and $(\boldsymbol{OR}, \boldsymbol{RS})$ can also be chosen as $(\boldsymbol{V}_{\text{off}}, \boldsymbol{V}_{\text{rmd}})$. The duty cycles can subsequently be calculated by synthesizing $\boldsymbol{V}_{\text{rmd}}$ based on two-level SVPWM, as shown in Fig. 3. Therefore, one of the key concerns in two-level SVPWM-based methods is the determination of the offset and remainder vectors.

A widely used method presented in [34]–[36] is utilized here to detail the existing prevalent problems. As shown in

Fig. 2, the offset vector with its tip located on one of the vertices of the SVD is actually a switching vector, so it can be represented by the switching state as $\boldsymbol{S}_{\mathrm{off}} = (S_{\mathrm{a}}, S_{\mathrm{b}}, S_{\mathrm{c}})$, while the remainder vector with fractional coordinates needs to be newly defined as $\boldsymbol{R}_{\mathrm{rmd}} = (R_{\mathrm{a}}, R_{\mathrm{b}}, R_{\mathrm{c}})$.

In [34]–[36], $\boldsymbol{S}_{\mathrm{off}}$ and $\boldsymbol{R}_{\mathrm{rmd}}$ are directly calculated as

$$\begin{cases} S_x = \mathrm{int}(S_{x,\mathrm{ref}}) \\ R_x = S_{x,\mathrm{ref}} - S_x \end{cases} \tag{4}$$

where $S_{x,\mathrm{ref}}$ denotes the coordinate of the RVV in *abc* coordinate system, and $\mathrm{int}(S_{x,\mathrm{ref}})$ is the largest integer not greater than $S_{x,\mathrm{ref}}$. For the switching states defined in Fig. 2 (i.e., $S_x \in [0 \ n-1]$), $S_{x,\mathrm{ref}}$ is typically derived by normalizing and scaling the reference phase voltage $v_{x,\mathrm{ref}}$ as [35], [36]

$$S_{x,\mathrm{ref}} = v_{x,\mathrm{ref}}/E + (n-1)/2. \tag{5}$$

Given that the sum of phase voltages is zero in a balanced three-phase system, (6) can be obtained based on (5).

$$S_{\mathrm{a,ref}} + S_{\mathrm{b,ref}} + S_{\mathrm{c,ref}} = 1.5(n-1). \tag{6}$$

Based on (4), (6), and $0 \le R_x < 1$, one can get

$$\begin{cases} R_{\mathrm{sum}} = \{0, 1, 2\} \\ S_{\mathrm{sum}} = 1.5(n-1) + \{0, -1, -2\} \end{cases} \tag{7}$$

where R_{sum} and S_{sum} are the sum of the three coordinates in $\boldsymbol{R}_{\mathrm{rmd}}$ and $\boldsymbol{S}_{\mathrm{off}}$, respectively.

Considering $S_{x,\mathrm{ref}} = S_x + R_x$, the output voltages per phase relative to point G in Fig. 1 defined by the offset and remainder vectors can be derived by substituting it into (5) as

$$\begin{cases} v_{x\mathrm{g,off}} = -(n-1)E/2 + S_x E \\ v_{x\mathrm{g,rmd}} = R_x E. \end{cases} \tag{8}$$

According to (7) and (8), the sum of output voltages defined by the offset vector may not be zero, indicating that the offset vector may yield a non-zero CMV between neutral point N and point G (see Fig. 1). The same finding can be derived from the remainder vector. Thus, the phase voltages defined by the offset and remainder vectors can be expressed as

$$\begin{cases} v_{x,\mathrm{off}} = v_{x\mathrm{g,off}} - v_{\mathrm{off,cmv}} \\ v_{x,\mathrm{rmd}} = v_{x\mathrm{g,rmd}} - v_{\mathrm{rmd,cmv}} \end{cases} \tag{9}$$

where $v_{\mathrm{off,cmv}}$ and $v_{\mathrm{rmd,cmv}}$ represent the CMVs generated by the offset and remainder vectors, respectively.

Clearly, the CMVs $v_{\mathrm{off,cmv}}$ and $v_{\mathrm{rmd,cmv}}$ make the three phases of the offset and remainder vectors coupled with each other, respectively. The above implementation brings about the following drawbacks:

1) The value of the CMV $v_{\mathrm{off,cmv}}$ is variable according to (7), which results in an indefinite offset vector coordinate relationship, making it difficult to quantitatively analyze the effect of RSSs on converter's performance. Determining the OSS becomes particularly cumbersome.
2) The switching sequence is generated based on line-to-line voltages (i.e., all phases are dealt with simultaneously), implying that complex encoding is indispensable for assigning the duty cycles to respective switching

states at each cycle [38]. Thus, it is more complicated than phase-voltage modulation (e.g., CBPWM).

3) A limited switching pattern or limited modulation range may be caused. Considering $\boldsymbol{V}_{\mathrm{ref}}'$ with ($v_{\mathrm{a,ref}}$, $v_{\mathrm{b,ref}}$, $v_{\mathrm{c,ref}}$) = (-2.4E, 1.3E, 1.1E) in Fig. 2, the offset vector can be derived as (0, 4, 4) based on (4) and (5), as (-1, 3, 3) is out of range. In this case, if the seven-segment pattern is employed, the fourth switching state ($S_{\mathrm{a}} + 1$, $S_{\mathrm{b}}+1$, $S_{\mathrm{c}}+1$) will exceed the maximum level, indicating that it is difficult to apply a seven-segment sequence across the entire region. In fact, different combinations of the offset and remainder vectors can be selected as explained previously. If the offset vector is chosen as (0, 3, 3), the seven-segment sequence will still be available.

III. PROPOSED DECOUPLED SVPWM SCHEME

A decoupled scheme is presented in this section to solve the aforementioned problems. Similarly, the RVV coordinates need to be calculated first. As SVPWM works with line-to-line voltages [38], $(S_{\mathrm{a,ref}}+\alpha, S_{\mathrm{b,ref}}+\alpha, S_{\mathrm{c,ref}}+\alpha)$ $(\alpha \in \mathbb{R})$ represents the same voltage vector. However, the RVV coordinates derived from (5) are unique, reducing system flexibility. From this point, it is necessary to establish the relationship between the RVV coordinates $(S_{\mathrm{a,ref}}, S_{\mathrm{b,ref}}, S_{\mathrm{c,ref}})$ and reference phase voltages $(v_{\mathrm{a,ref}}, v_{\mathrm{b,ref}}, v_{\mathrm{c,ref}})$. Here, a voltage reference point (RP) is explicitly introduced, which specifically refers to a point on the converter side that has the same potential as the neutral point. In this way, the reference phase voltages are equal to the reference line-to-RP voltages (i.e., leg voltages), and the RVV coordinates can be directly calculated based on the reference leg voltages, which can be expressed as

$$S_{x,\mathrm{ref}} = (v_{x,\mathrm{ref}} - v_{\mathrm{min}})/E \tag{10}$$

where v_{min} denotes the voltage of the negative terminal of the dc bus relative to the RP for FC converters, while the minimum leg voltage per phase for CHB converters. Obviously, different RVV coordinates can be derived by selecting different RPs (i.e., different v_{min}). Notice that point G is first selected as the RP to calculate $S_{x,\mathrm{ref}}$, i.e., $v_{\mathrm{min}} = -V_{\mathrm{dc}}/2$. In this case, (10) is clearly the same as (5), and (6) is still satisfied.

A. Phase Decoupling of the Vectors

After the RVV coordinates are obtained, a straightforward method to decompose the RVV is to choose the vector $\boldsymbol{V}_{\mathrm{nst}}$ nearest to the RVV as the offset vector, and the resulting coordinates of $\boldsymbol{S}_{\mathrm{off,nst}}$ and $\boldsymbol{R}_{\mathrm{rmd,nst}}$ can be derived as

$$\begin{cases} S_{x,\mathrm{nst}} = \mathrm{round}(S_{x,\mathrm{ref}}) \\ R_{x,\mathrm{nst}} = S_{x,\mathrm{ref}} - S_{x,\mathrm{nst}} \end{cases} \tag{11}$$

where $\mathrm{round}(S_{x,\mathrm{ref}})$ denotes the integer closest to $S_{x,\mathrm{ref}}$.

As done in Section II-B, it can be easily shown that the three phases of both the offset and remainder vectors derived from (11) are still coupled with each other. To address this issue, a modification is made to $\boldsymbol{S}_{\mathrm{off,nst}}$ and $\boldsymbol{R}_{\mathrm{rmd,nst}}$ as

$$\begin{cases} S_x = S_{x,\mathrm{nst}} + \mathrm{sign}(R_{\mathrm{sum,nst}})f_x \\ R_x = S_{x,\mathrm{ref}} - S_x \end{cases} \tag{12}$$
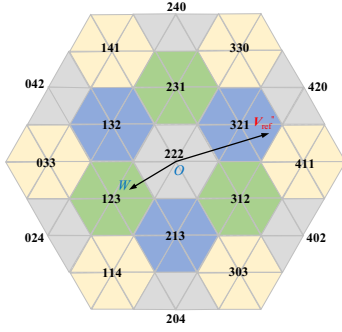
Fig. 4. Region division of the five-level space vector diagram.

TABLE I
DIFFERENT COMBINATIONS OF THE OFFSET AND REMAINDER VECTORS

n_s	(S_a, S_b, S_c)	(R_a, R_b, R_c)	Offset Vec.	Remainder Vec.
-3	(4, 3, 2)	(0.55, -0.15, -0.4)	*OP*	*PS*
-2	(4, 3, 1)	(0.217, -0.483, 0.266)	*OQ*	*QS*
-1	(4, 2, 1)	(-0.117, 0.183, -0.066)	*OR*	*RS*
0	(3, 2, 1)	(0.55, -0.15, -0.4)	*OP*	*PS*
1	(3, 2, 0)	(0.217, -0.483, 0.266)	*OQ*	*QS*
2	(3, 1, 0)	(-0.117, 0.183, -0.066)	*OR*	*RS*
3	(2, 1, 0)	(0.55, -0.15, -0.4)	*OP*	*PS*

where f_x is the correction factor, $R_{\text{sum,nst}}$ denotes the sum of $R_{x,\text{nst}}$ in three phases, and sign($\cdot$) stands for the sign function. For $R_{\text{sum,nst}} > 0$ ($R_{\text{sum,nst}} < 0$) with $R_{x,\text{nst}}$ being the qth maximum (minimum) value in $\boldsymbol{R}_{\text{rmd,nst}}$, if $q \leq R_{\text{nst,sum}}$, $f_x = 1$; otherwise, $f_x = 0$.

In this manner, the sum of R_x in three phases becomes zero, and a definite offset vector coordinate relationship can be established according to (6) as

$$S_a + S_b + S_c = 1.5(n-1). \tag{13}$$

According to (8) and (9), the CMVs between the neutral point and RP (i.e., point G) yielded by both vectors become zero. Thus, the phase voltages and leg voltages defined by the offset vector are equal to each other, which means that per-phase voltage is defined by the leg voltage of that phase only. In this sense, the three phases of the offset vector are decoupled from each other. The same is true for the remainder vector. According to (13), phase decoupling is essentially to select the switching state satisfying a specific relationship as the offset vector, such that the CMVs are eliminated and therefore the output phase voltages are decoupled. Further, considering $v_{x,\text{ref}} = v_{x,\text{off}} + v_{x,\text{rmd}}$, the desired phase voltages can thus be directly regulated by controlling the leg voltages defined by the offset vector and the remainder vector separately, which will be detailed in Section III-C.

For a five-level converter, the sum of the coordinates in $\boldsymbol{S}_{\text{off}}$ can be accordingly derived as $1.5(n-1) = 6$. Subject to this constraint, the positions of all offset vectors related to varying RVVs can be found visually, as marked by the origins of the different colored areas in Fig. 4. Clearly, (1, 2, 3) and (3, 2, 1) will be chosen as offset vectors if the RVV is located at *OW* and $\boldsymbol{V}_{\text{ref}}''$, respectively.

B. Calculating Redundant Switching States

As shown in Fig. 4, when the RP is fixed at point G, the combination of the offset and remainder vectors obtained previously is unique for a given RVV, which reduces algorithm flexibility. Thus, a dynamic RP mechanism is further introduced, by which all possible offset vectors along with their RSSs can be deduced from one unique variable.

According to (10), the coordinates of the RVV are subject to the chosen RP. If the RP is shifted from point G to a virtual

point G$'$ such that $v_{\min}$ changes by Δv, the coordinates will be changed to

$$S_{x,\text{ref}}{}' = S_{x,\text{ref}} - \Delta v/E. \tag{14}$$

Likewise, $\boldsymbol{S}_{\text{off,nst}}{}'$ and $\boldsymbol{R}_{\text{rmd,nst}}{}'$ can be calculated by (11). Also, a modification shown in (12) should be made to $\boldsymbol{S}_{\text{off,nst}}{}'$ and $\boldsymbol{R}_{\text{rmd,nst}}{}'$ to eliminate the CMV between the neutral point and new RP. In the same way, a new relationship instead of (13) can be derived as

$$S_a{}' + S_b{}' + S_c{}' = 1.5(n-1) - 3\Delta v/E \in \mathbb{N}. \tag{15}$$

Hence, Δv must comply with the rule below.

$$\Delta v = n_s \Delta v_s = n_s E/3 \tag{16}$$

where Δv_s represents the minimum shifted potential difference between the two RPs that can still decouple the phases of the vectors, and n_s is defined as the number of level shifts, $n_s \in \mathbb{Z}$.

Equations (14) and (15) can thus be updated to

$$S_{x,\text{ref}}{}' = S_{x,\text{ref}} - n_s/3 \tag{17}$$

$$S_a{}' + S_b{}' + S_c{}' = 1.5(n-1) - n_s. \tag{18}$$

According to (18), if the potential of the RP is shifted by Δv_s (i.e., $n_s = 1$), the sum of the coordinates of the offset vector will change by 1, which means that one and only one coordinate will be altered. Meanwhile, another combination of the offset and remainder vectors is selected. Taking $\boldsymbol{V}_{\text{ref}}$ with $(v_{a,\text{ref}}, v_{b,\text{ref}}, v_{c,\text{ref}}) = (1.55E, -0.15E, -1.4E)$ in Fig. 2 as an example, the offset and remainder vectors at $n_s = 0$ can be derived from (10)–(12) as (3, 2, 1) and (0.55, -0.15, -0.4), respectively. On this basis, the coordinates of these two vectors at $n_s = 1$ can be calculated as (3, 2, 0) and (0.217, -0.483, 0.266) by (17), (11), and (12) in sequence. Similarly, other vector combinations can be derived as shown in Table I. Hence, all possible vector combinations can be obtained just by regulating the value of n_s.

In effect, not all values of n_s need to be treated that way. According to (17) and (18), when the potential of the RP is shifted by $3\Delta v_s$, each coordinate of the RVV as well as the offset vector changes by 1, while the remainder vector remains the same, which can also be found from Table I. Therefore, only the coordinates of the offset and remainder vectors at $n_s = \{0, 1, 2\}$ need to be calculated, while the coordinates at other values of n_s can be directly deduced as

$$(S_x^k, R_x^k) = (S_x^w - \text{int}(k/3), R_x^w), \text{ for } w = \text{mod}(k, 3) \tag{19}$$

where S_x^k and R_x^k are the coordinates of the offset and remainder vectors at $n_s = k$, respectively, and $\mathrm{mod}(k, 3)$ denotes the remainder of k divided by 3.

Furthermore, since the number of vector combinations is finite, the range of n_s has to be accurately evaluated. As shown in Table I, three distinct switching vectors (i.e., **OP**, **OQ**, and **OR**) can be selected as the offset vector, and each vector may contain multiple RSSs. Also, each RSS has a one-to-one correspondence with the value of n_s. Thus, each vector corresponds to a maximum value $n_{sv,max}$ and a minimum value $n_{sv,min}$. For example, $n_{svp,max} = 3$ and $n_{svp,min} = -3$ can be explicitly obtained for **OP**. On this basis, the range of n_s can be derived as

$$\begin{cases} n_{s,max} = \max\left\{n_{svp,max}, n_{svq,max}, n_{svr,max}\right\} \\ n_{s,min} = \min\left\{n_{svp,min}, n_{svq,min}, n_{svr,min}\right\}. \end{cases} \quad (20)$$

Further, for each offset vector, at least one coordinate is $n - 1$ at $n_{sv,min}$ and zero at $n_{sv,max}$ as shown in Table I. In this way, once the switching state of the offset vector at $n_s = k$ is given as (S_a^k, S_b^k, S_c^k), the ones at $n_s = n_{sv,max}$ and $n_s = n_{sv,min}$ can be expressed as

$$\begin{cases} S_x^{k,min} = S_x^k - \min\limits_{x=a,b,c}\left\{S_x^k\right\} \\ S_x^{k,max} = S_x^k + n - 1 - \max\limits_{x=a,b,c}\left\{S_x^k\right\} \end{cases} \quad (21)$$

where the six switching states of the three offset vectors can be acquired by setting $k = \{0, 1, 2\}$.

Based on (20) and (21), the range of n_s can be obtained as

$$\begin{cases} n_{s,max} = \max\limits_{k=0,1,2}\left\{\sum\limits_{x=a,b,c} S_x^0 - \sum\limits_{x=a,b,c} S_x^{k,min}\right\} \\ n_{s,min} = \min\limits_{k=0,1,2}\left\{\sum\limits_{x=a,b,c} S_x^0 - \sum\limits_{x=a,b,c} S_x^{k,max}\right\} \end{cases} \quad (22)$$

In consequence, phase decoupling together with dynamic RP mechanism provides two immediate benefits: 1) the CMVs between neutral point and each virtual RP generated by both the offset and remainder vectors are kept at zero, enabling the introduction of carrier-based implementation as described below; 2) since the value of n_s has a one-to-one correspondence with all available switching states, the acquisition of the OSS is naturally translated into the selection of the optimal n_s, which facilitates a general approach to optimizing converter's performance, as explained in Section V.

C. Generating Switching Sequence Along With Gate Pulses

Once the optimal vector combination is determined, as described in Section V, the calculation of the duty cycles and the generation of the switching sequence have to be scheduled. To reduce processing time and memory requirements for the detection of all NTVs and complex encoding in earlier methods, this section introduces a carrier-based implementation. To aid the explanation, the RVV **OW** with $S_{off} = (1, 2, 3)$ and $R_{rmd} = (0.4, -0.1, -0.3)$ in Fig. 4 is adopted as an example.

As explained in Section III-A, the reference phase voltages can be generated by controlling the leg voltages defined by
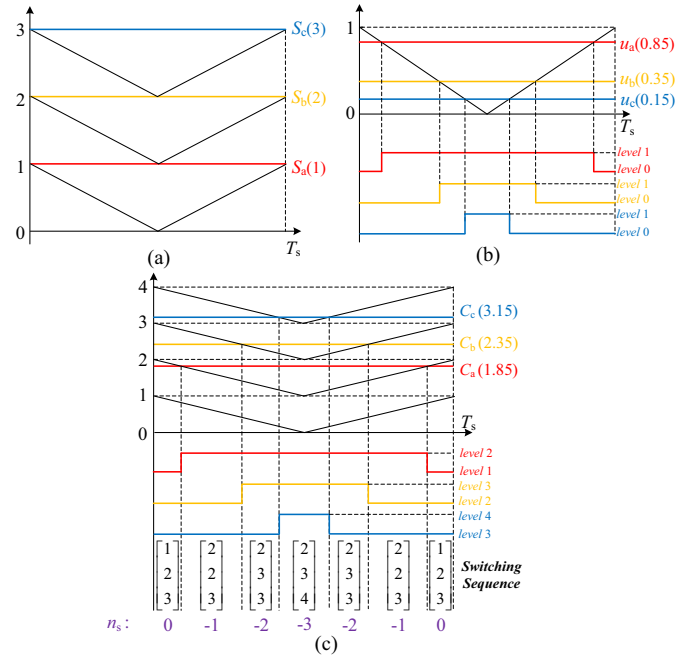

Fig. 5. Generated switching sequence along with gate pulses. (a) Phase-voltage modulation for the offset vector. (b) Two-level SVPWM for the remainder vector. (c) Equivalent seven-segment switching sequence in the PDPWM.

the offset vector and the remainder vector separately. For the offset vector with the switching state of integer form, the leg voltages defined by it can be exactly produced by directly outputting the corresponding switching state. For $S_{off} = (1, 2, 3)$, carrier-based implementation is shown in Fig. 5(a).

However, the remainder vector with fractional coordinates cannot be directly generated by outputting constant leg voltages like the offset vector, but needs to be pulse-width modulated. Therefore, when it comes to hardware implementation, the three phases of the remainder vector are actually still coupled with each other since the CMV $v_{rmd,cmv}$ (see (9)) cannot be kept at zero throughout the switching period. In this sense, phase decoupling transforms the difficulty of the switching sequence generation into the synthesis of the remainder vector.

As stated previously, the remainder vector can be synthesized by two-level SVPWM. According to Figs. 3 and 4, the remainder vector $R_{rmd} = (0.4, -0.1, -0.3)$ is located in the first sector of the two-level SVD, and the seven-segment sequence can thus be represented as (0, 0, 0)-(1, 0, 0)-(1, 1, 0)-(1, 1, 1)-(1, 1, 0)-(1, 0, 0)-(0, 0, 0). Evidently, one of $n - 1$ $S_{xij} - \bar{S}_{xij}$ branches per phase can be extracted to form an equivalent two-level three-phase converter to output the remainder vector, and the equivalent dc-link voltage is clearly $V_{eq} = E$. Further, carrier-based implementation can be utilized here to avoid the calculation of the duty cycles as the equivalent output to two-level SVPWM can be accomplished by injecting zero-sequence components [22], which is expressed as

$$u_x' = r_x + v_z \quad (23)$$

where

$$r_x = \frac{v_{x,\mathrm{rmd}}}{V_{\mathrm{eq}}/2} = 2R_x \tag{24}$$

$$v_{\mathrm{z}} = (2\lambda - 1) - \lambda r_{\max} - (1 - \lambda)r_{\min} \tag{25}$$

and r_x stands for the normalized value, $r_{\max}$ and $r_{\min}$ are the maximum and minimum values of $\{r_{\mathrm{a}}, r_{\mathrm{b}}, r_{\mathrm{c}}\}$, respectively, and λ denotes the distribution factor of the zero vector, $0 \le \lambda \le 1$. The value of λ can be flexibly tuned to adjust the duty cycle of the zero vector while keeping the non-zero vectors unchanged to generate an equivalent output. The range of $u_x{}'$ derived from (23) is [-1 1], which can be resized to [0 1] by

$$u_x = (u_x{}' + 1)/2. \tag{26}$$

For standard seven-segment sequence (i.e., $\lambda = 0.5$), $(u_{\mathrm{a}}, u_{\mathrm{b}}, u_{\mathrm{c}})$ can be accordingly calculated as $(0.85, 0.35, 0.15)$ in this case, and carrier-based implementation can subsequently be exploited, as shown in Fig. 5(b).

Combining Figs. 5(a) and (b), we can get the final form of carrier-based implementation as shown in Fig. 5(c), which is explicitly the PDPWM. The final values compared with the phase-disposition carriers are given as

$$C_x = S_x + u_x. \tag{27}$$

An emerging problem is that since one of $n-1$ $S_{xij} - \bar{S}_{xij}$ branches per phase has been used for the synthesis of the remainder vector, only $n - 2$ branches per phase can be employed to generate the offset vector. Consequently, the maximum voltage level of the offset vector should be reduced from $n - 1$ to $n - 2$. As explained in the previous section, all switching states in the triangle formed by the NTVs have a one-to-one correspondence with the values of n_{s}. Hence, the switching sequence composed of the NTVs can also be represented in terms of n_{s}. According to Fig. 5(c), if the switching state of the offset vector at $n_{\mathrm{s}} = n_{\mathrm{s}0}$ is selected, the seven-segment sequence of n_{s} can be expressed as $\{n_{\mathrm{s}0}, n_{\mathrm{s}0} - 1, n_{\mathrm{s}0} - 2, n_{\mathrm{s}0} - 3, n_{\mathrm{s}0} - 2, n_{\mathrm{s}0} - 1, n_{\mathrm{s}0}\}$. Obviously, if the switching state at $n_{\mathrm{s}} = n_{\mathrm{s},\min}$ is chosen as the offset vector, $n_{\mathrm{s},\min} - 3$ will be out of range. Similar conclusions can be found from discontinous modulation (i.e., $\lambda = 0$ or 1). In summary, the range of n_{s} should be adjusted to

$$\begin{cases} N_{\mathrm{s},\min} = n_{\mathrm{s},\min} + 2 + \mathrm{ceil}(\lambda) \\ N_{\mathrm{s},\max} = n_{\mathrm{s},\max} + \mathrm{int}(\lambda). \end{cases} \tag{28}$$

where $\mathrm{ceil}(\lambda)$ denotes the smallest integer not less than λ.

As described in Section II-A, there are RSCs for some voltage levels in CHB and FC converters. The carrier-based implementation allows existing improved PDPWM methods to be used for the selection of the RSCs. For instance, the PDPWM with sorting algorithm in [11] can be exploited here to evenly distribute switching losses. For FC converters, either the rotation-carrier technique in [10] or cost function-based method in [12] can be employed to balance capacitor voltages. Therefore, the proposed scheme offers an effective interface to other advanced methods. Clearly, the determination of the RSCs is also decoupled from the selection of the RSSs, which simplifies implementation while providing more flexibility.
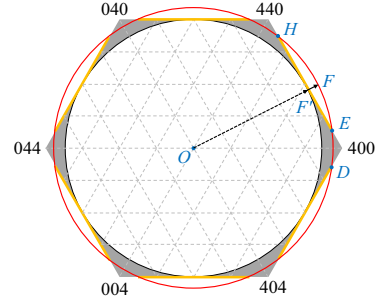

Fig. 6. Schematic of the RVV in the overmodulation region.

IV. PERFORMANCE EXTENSION

A. Overmodulation Operation

Define the modulation index as $M = \sqrt{3}V_{\mathrm{p}}/V_{\mathrm{dc}}$, where V_{p} represents the amplitude of the phase voltage. As shown in Fig. 6, the inscribed circle of the outer hexagon in an n-level SVD represents the maximum linear modulation voltage, i.e., $M = 1$. For $M > 1$, if the tip of the RVV is located in the shaded area beyond the inscribed circle but within the outer hexagon, it can still be synthesized by the NTVs. Otherwise, the converter is not able to generate it, i.e., the RVV lies in the overmodulation region, such as **OF**. In practice, whether the overmodulation operation occurs can be directly judged based on the relationship between $N_{\mathrm{s},\max}$ and $N_{\mathrm{s},\min}$ as follows:

1) $N_{\mathrm{s},\min} \le N_{\mathrm{s},\max}$. At least one switching state can be selected as the offset vector.
2) $N_{\mathrm{s},\min} > N_{\mathrm{s},\max}$. There is no offset vector available. In this case, the RVV is beyond the outer hexagon of the n-level SVD, i.e., in the overmodulation region.

In order to achieve full-region operation, the magnitude of the RVV located in the overmodulation region will be scaled down to the maximum modulation voltage of the converter without changing its direction. Taking the RVV trajectory *DEFH* as an example, when the tip is located on the arc *DE*, it can be exactly synthesized without additional manipulation. But for those lying on the arc *EFH*, their magnitudes will be scaled down to the straight line *EF'H*. For instance, the vector **OF** is regulated to **OF'**, which can be expressed as

$$\boldsymbol{OF'} = \beta\boldsymbol{OF} \tag{29}$$

where β represents the scaling factor, $0 < \beta < 1$.

Based on (10) and (29), the coordinates of the new RVV can be derived as

$$S_{x,\mathrm{ref}}{}'' = \beta S_{x,\mathrm{ref}} + (\beta - 1)v_{\min}/E. \tag{30}$$

Actually, the RVV located on the outer hexagon can only be synthesized by the nearest two vectors with the tips lying on the outer hexagon as well, while the duty cycle of the third vector is zero. For example, **OF'** can be uniquely synthesized by (4, 1, 0) and (4, 2, 0). Besides, as shown in Fig. 2, for arbitrary two adjacent vectors located on the outer hexagon, only one of the coordinates is different, while one of the remaining two coordinates is kept at $n - 1$ and the other remains zero, which means that the new coordinates satisfy

$$\max_{x=\mathrm{a,b,c}} \left\{ S_{x,\mathrm{ref}}{}'' \right\} - \min_{x=\mathrm{a,b,c}} \left\{ S_{x,\mathrm{ref}}{}'' \right\} = n - 1 \tag{31}$$

where $\max\{\gamma_1, \gamma_2, \gamma_3\}$ and $\min\{\gamma_1, \gamma_2, \gamma_3\}$ represent the largest and smallest values among γ_1, γ_2 and γ_3, respectively.

By substituting (30) into (31), the scaling factor is given as

$$\beta = \frac{n-1}{\max\limits_{x=a,b,c}\{S_{x,\text{ref}}\} - \min\limits_{x=a,b,c}\{S_{x,\text{ref}}\}}. \tag{32}$$

As a consequence, the new coordinates are derived from (30), and the range of n_s can be accordingly recalculated.

B. Converters With an Even Number of Levels

According to (13) and (18), the proposed scheme appears to be inapplicable to converters with an even number of levels owing to $1.5(n-1) \notin \mathbb{N}$. In fact, this deficiency is caused by an inappropriate preselected RP. Absorbing the idea of the virtual RP, this issue can be easily overcome.

Apparently, if a virtual RP is preselected such that the RVV coordinates satisfy (33), phase decoupling can still be achieved.

$$S_{a,\text{ref}} + S_{b,\text{ref}} + S_{c,\text{ref}} = 1.5n. \tag{33}$$

By substituting (10) into (33), the virtual RP can be identified as

$$v_{\text{min}} = -\frac{n}{2(n-1)}V_{\text{dc}}. \tag{34}$$

In such a way, the previous implementation will still work except that (13) and (18) are accordingly amended to

$$S_a + S_b + S_c = 1.5n \tag{35}$$

$$S_a' + S_b' + S_c' = 1.5n - n_s. \tag{36}$$

V. OPTIMUM SWITCHING STATE SELECTION

Based on the dynamic RP mechanism, the determination of the OSS is translated into the identification of the optimal n_s, as explained in Section III-B. Meanwhile, only the OSS of the offset vector needs to be determined, since other switching states can be naturally generated by carrier-based implementation. Theoretically, any control objective can be achieved by establishing its relationship with n_s. Here, a widely desired objective, CMV rejection, is considered.

Referring to (8), the output voltage per phase relative to point G can be expressed as

$$v_{xg} = -(n-1)E/2 + C_x E. \tag{37}$$

If $v_{ng} = 0$, namely $v_{ag} + v_{bg} + v_{cg} = 0$, we can get

$$C_a + C_b + C_c = 1.5(n-1). \tag{38}$$

Based on (27) and (38), the relationship between n_s and λ can be obtained as

$$\lambda = \frac{2n_s/3 + r_{\text{min}}}{2 - r_{\text{max}} + r_{\text{min}}}. \tag{39}$$

Since both n_s and λ are unknown, and r_{max} and r_{min} are subject to n_s, it is difficult to solve (39) directly. According to (39), $\lambda \leq 0$ and $\lambda \geq 1$ can be obtained for $n_s \leq 0$ and $n_s \geq 3$, respectively. Thus, $0 < \lambda < 1$ can only be acquired at $n_s = \{1,2\}$. Since the output waveform with the lowest THD is reached at $\lambda = 0.5$ [21], the distribution factors at $n_s = \{1,2\}$
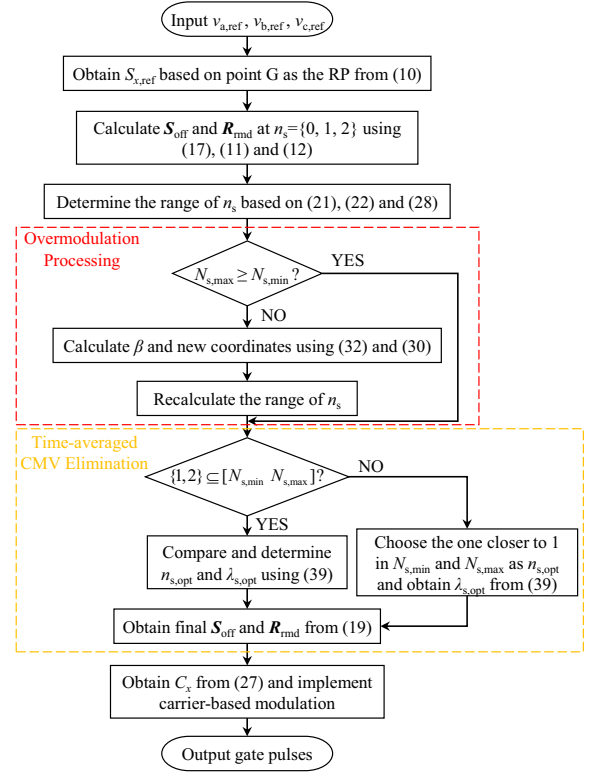

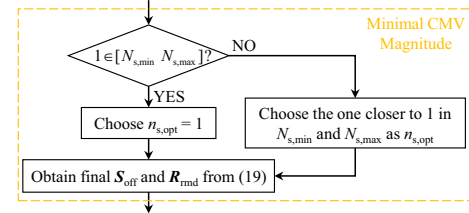Fig. 7. Flow chart of the proposed scheme with time-averaged CMV elimination.

Fig. 8. Flow chart of the minimal CMV magnitude implementation.

can be initially calculated. Subsequently, the distribution factor closest to 0.5 and its corresponding n_s are taken as the optimal values λ_{opt} and $n_{s,\text{opt}}$, respectively. In fact, $\{1, 2\}$ may not all fall within the range of n_s (i.e., $N_{s,\text{min}} \geq 2$ or $N_{s,\text{max}} \leq 1$). In this case, the one closer to 1 (or 2) in $N_{s,\text{min}}$ and $N_{s,\text{max}}$ is chosen as $n_{s,\text{opt}}$, and λ_{opt} can be further calculated by (39). Notice that the final value of λ_{opt} should be limited to [0 1]. The flow chart of the proposed scheme is shown in Fig. 7.

As a result, the proposed approach achieves time-averaged CMV elimination while ensuring high waveform quality, which is especially critical for long distribution feeders. In addition, it can also be flexibly tuned to meet different applications. According to (37), the CMV of each switching state in the sequence can be expressed as

$$v_{ng} = -n_s E/3. \tag{40}$$

As explained previously, the switching sequence can also be represented in terms of n_s, which will be $\{1, 0, -1, -2, -1, 0, 1\}$ for $n_{s,\text{opt}} = 1$ and $\{2, 1, 0, -1, 0, 1, 2\}$ for $n_{s,\text{opt}} = 2$. Hence, the maximum CMV magnitude is $2E/3$, which may not be
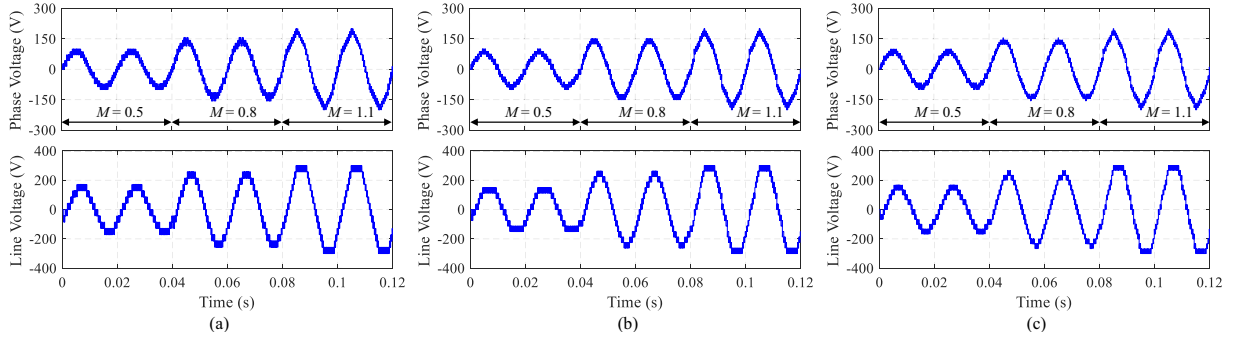
Fig. 9. Simulation results of phase voltage v_a and line voltage v_{ab} in CHB and FC converters under different distribution factors (λ) and various modulation indices (M). (a) Eight-level FC converter with $\lambda = 0$. (b) Nine-level CHB converter with $\lambda = 0.5$. (c) Ten-level FC converter with $\lambda = 1$.
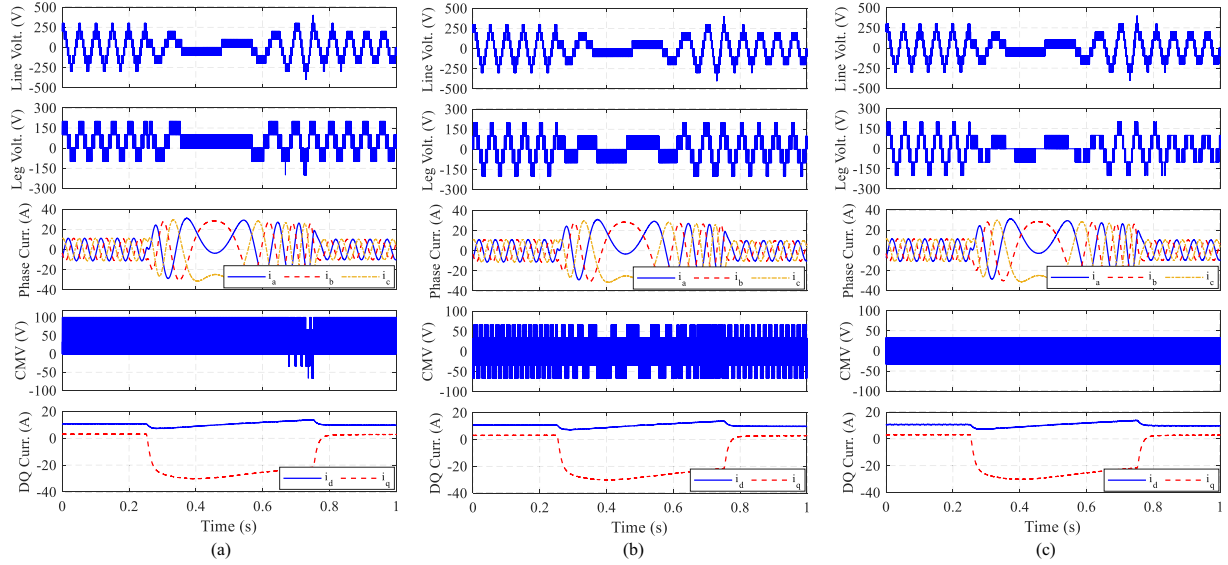

Fig. 10. Simulation results of line voltage v_{ab}, leg voltage v_{ag}, phase currents, CMV v_{ng}, and *dq*-axis currents in the schemes (a) without optimization, (b) with time-averaged CMV elimination, and (c) with minimal CMV magnitude.

TABLE II
SIMULATION PARAMETERS OF THE INDUCTION MOTOR

Variable	Value	Variable	Value
Stator Inductance	0.071 H	Rotor Inductance	0.071 H
Mutual Inductance	0.069 H	Number of Pole Pairs	2
Stator Resistance	0.435 Ω	Rotor Resistance	0.816 Ω
DC-link Voltage of H-bridge	100 V	Carrier Frequency	2 kHz

suitable for some cases with low protection voltage. For these applications, the minimal CMV magnitude can be realized by configuring $n_{s,opt} = 1$ and $\lambda_{opt} = 0$. In consequence, the sequence {1, 0, -1, 0, 1} of n_s is used, and the maximum CMV magnitude is evidently reduced to $E/3$. The flow chart is accordingly updated as shown in Fig. 8.

VI. SIMULATION AND EXPERIMENTAL RESULTS

A. Simulation Verification

To verify the proposed decoupled SVPWM scheme comprehensively, simulations using both an inductive load and an induction motor load are carried out.

1) With an Inductive Load: The CHB and FC converters [13] with different number of voltage levels are first simulated to verify the generality of the algorithm, where the dc bus voltage is set to $V_{dc} = 300$ V, i.e., $E = V_{dc}/(n-1)$ for the CHB converter. The parameters of the inductive load are 20 Ω and 3 mH. The fundamental and carrier frequencies are 50 Hz and 2 kHz, respectively. In addition, the capacitor voltages of the FC converter are configured to be constant since they are not the focus of this article and can be balanced by introducing improved PDPWM methods, as explained in Section III-C.

The SVPWM strategy without optimization is tested here, in which the offset and remainder vectors derived in Section III-A are directly determined if $n_s = 0 \in [N_{s,min} \ N_{s,max}]$; otherwise, the vector combination corresponding to the value closer to zero in $N_{s,min}$ and $N_{s,max}$ is selected. The output voltages of the nine-level CHB converter as well as the eight- and ten-level FC converters under different distribution factors and various modulation indices including overmodulation (i.e., $M = 1.1$) are shown in Fig. 9. As can be seen, the proposed scheme is still operative in the overmodulation region, except that the distortion of the voltage waveform increases. Therefore, the proposed scheme can achieve full-region operation
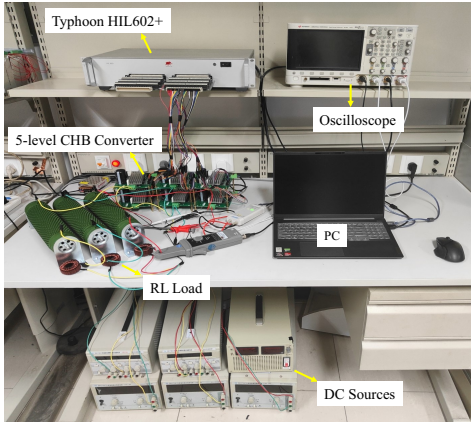
Fig. 11. Experimental platform of the five-level CHB converter.

for CHB and FC converters with different number of levels.

2) With an Induction Motor Load: An induction motor driven by a five-level CHB converter is then simulated to verify the schemes with CMV suppression, where the schemes without optimization, with time-averaged CMV elimination (see Fig. 7), and with minimal CMV magnitude (see Fig. 8) are tested for comparison. The motor parameters are shown in Table II, and the field-oriented control (FOC) with constant rated flux [39] is applied to the motor control unit.

A transient profile is designed to evaluate the schemes over a wide operating point, where the load torque is kept at 5 N·m and the operating speed is reversed from 600 r/min to -600 r/min (i.e., electrical frequency from 20 Hz to -20 Hz) in 0.5 s at 0.25 s. The resulting waveforms of the voltages and currents are shown in Fig. 10. As can be seen, the output phase and dq-axis currents are highly similar in different schemes. However, when it comes to CMV, the scheme without optimization causes a significant dc offset, and the peak reaches 100 V (i.e., E). By contrast, the other two schemes with CMV suppression can completely eliminate the dc offset. Besides, the CMV peak is reduced to 66.7 V (i.e., $2E/3$) in the scheme with time-averaged CMV elimination, and it is further reduced to 33.3 V (i.e., $E/3$) in the scheme with minimal CMV magnitude due to the removal of the fourth switching state, which is consistent with the theoretical analysis.

B. Experimental Validation

To further validate the proposed SVPWM strategy, experiments are carried out on a five-level three-phase CHB converter, as shown in Fig. 11. The system parameters are the same as the simulation with an inductive load, except that the dc-link voltage of each H-bridge is adjusted to $E = 30$ V. The modulation algorithm is implemented on an ARM Cortex A9 core, while PWM signals are generated by an FPGA. Both of them are integrated into Zynq-7000 SoC in Typhoon HIL602+ device, where the modulation index can be directly regulated via the dedicated SCADA panel on the host PC.

Similarly, the experiments of the five-level CHB converter without optimization are first conducted under different distribution factors and various modulation indices. The resultant line voltage v_{ab}, leg voltage v_{ag}, and phase current i_a are
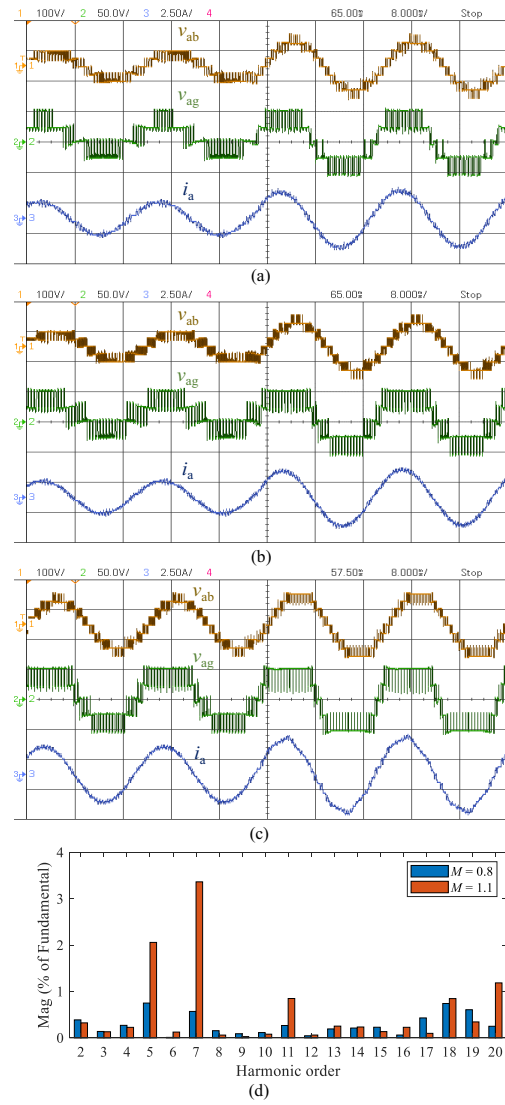

Fig. 12. Experimental results of the five-level CHB converter without optimization under different distribution factors (λ) and various modulation indices (M). (a) M steps from 0.5 to 0.8 and $\lambda = 0$. (b) M steps from 0.5 to 0.8 and $\lambda = 0.5$. (c) M steps from 0.8 to 1.1 (i.e., overmodulation) and $\lambda = 0.5$. (d) FFT results of the line voltage at $M = 0.8$ and $M = 1.1$.

shown in Fig. 12(a)–(c). As can be seen, different switching patterns can be accessed by flexibly adjusting distribution factor λ, and the proposed scheme is operative in both linear modulation and overmodulation regions. To evaluate the proposed scheme quantitatively, the FFT results of the line voltage at $M = 0.8$ and $M = 1.1$ are presented in Fig. 12(d). Compared with those at $M = 0.8$, the results at $M = 1.1$ clearly contain more low-order harmonic content, especially the 5th and 7th, due to the scaled voltage vector in the overmodulation region despite applying a higher modulation index. Moreover, the fundamental amplitudes of the line voltage at $M = 0.8$ and $M = 1.1$ are calculated as 95.48 V and 125.32 V, respectively. Compared with the expected values (i.e., 96 V and 132 V), the errors are 0.54% and 5.1%, respectively. These results indicate that the proposed scheme can exactly produce the desired voltages in the linear modulation region, while the effect is slightly weakened in the overmodulation region.
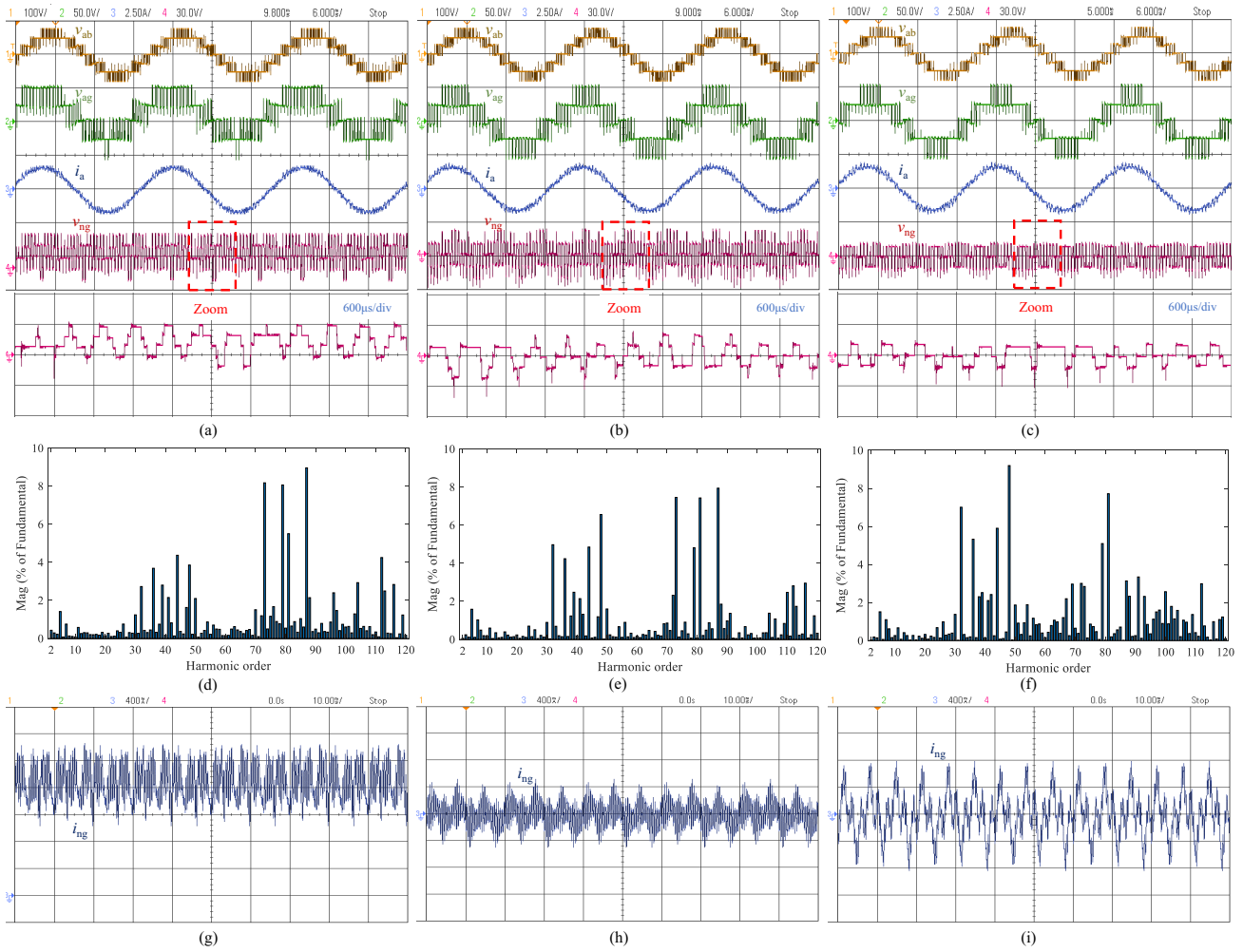
Fig. 13. Experimental results of the five-level CHB converter under $M = 0.6$. Line voltage v_{ab}, leg voltage v_{ag}, phase current i_a, CMV v_{ng}, and FFT results of the line voltage in the schemes (a)(d) without optimization, (b)(e) with time-averaged CMV elimination, and (c)(f) with minimal CMV magnitude. Common-mode current i_{ng} with an additional inductive load (3 mH) connected between points N and G in the schemes (g) without optimization, (h) with time-averaged CMV elimination, and (i) with minimal CMV magnitude.
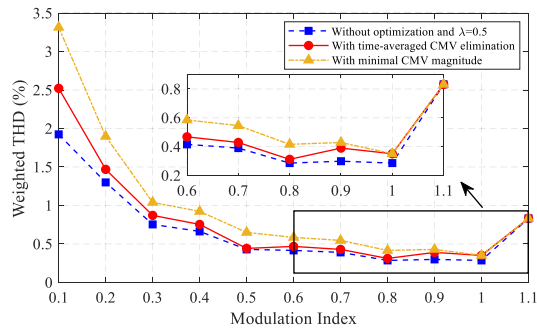

Fig. 14. Weighted THD of the line voltage in the five-level CHB converter with different modulation schemes.

Fig. 13(a)-(c) shows the experimental results of the converter under $M = 0.6$ in the schemes without optimization, with time-averaged CMV elimination, and with minimal CMV magnitude. Clearly, the CMV results are in line with those in Fig. 10: the CMV peak of the scheme without optimization reaches 30 V (i.e., E) with an explicit dc offset, and it is restricted to below $2E/3$ and $E/3$ in the schemes with time-averaged CMV elimination and with minimal CMV magnitude, respectively, accompanied by zero dc offset.

Fig. 13(d)-(f) presents the FFT results over a wider range to compare the waveform quality of the line voltage in these three schemes. It can be seen that their low-order harmonics are similar but the harmonics around the switching frequency (i.e., 40th-order) are evidently different: they are lowest in the scheme without optimization due to keeping the distribution factor λ at 0.5 [21], and highest in the scheme with minimal CMV magnitude as λ remains zero. Not surprisingly, those in the scheme with time-averaged CMV elimination are in between due to the varying λ. Further, the weighted THD of the line voltage that considers the harmonic components with orders up to 120 (i.e., 6 kHz) is calculated under different modulation indices [37], as shown in Fig. 14. Clearly, the results are consistent with the previous analysis. Besides, the weighted THD in the scheme with time-averaged CMV elimination is closer to that in the schemes without optimization and with minimal CMV magnitude for lower and higher modulation indices, respectively. This is due to the
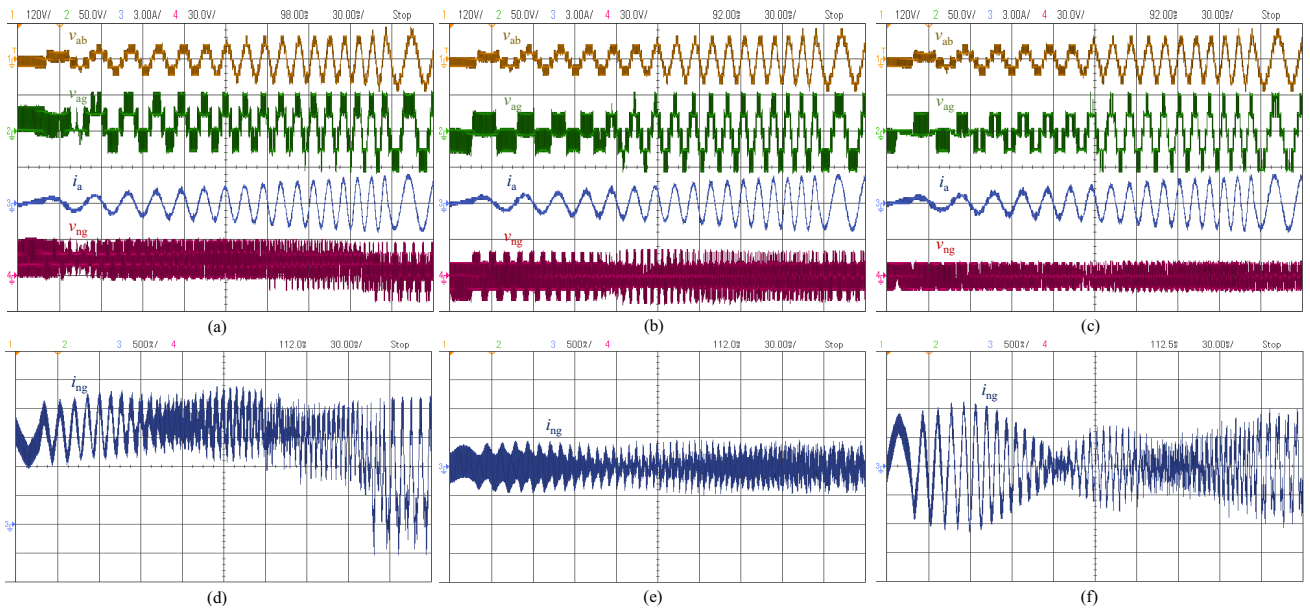
Fig. 15. Experimental results of the five-level CHB converter under transient conditions. Line voltage v_{ab}, leg voltage v_{ag}, phase current i_a, and CMV v_{ng} in the schemes (a) without optimization, (b) with time-averaged CMV elimination, and (c) with minimal CMV magnitude. Common-mode current i_{ng} with an additional inductive load (3 mH) connected between points N and G in the schemes (d) without optimization, (e) with time-averaged CMV elimination, and (f) with minimal CMV magnitude.

TABLE III
COMPARISON OF THE PROPOSED SCHEME AND THE EXISTING SVPWM METHODS IN DIFFERENT ASPECTS

SVPWM Schemes	Optimized Switching Sequence	Adjustable Duty Cycles	Region or Triangle Identification	Coordinate Transformation	Generalized Gate Pulses Generation	All RSSs or RSCs Available	Converter Optimization	Overmodulation Operation
In [3]	Not provided	Not provided	Not required	Required	Not provided	Neither	Specific obj.	Nonoperative
In [4]	Online calculation	Not provided	Required	Not required	Carrier-based	Neither	Specific obj.	Nonoperative
In [5]	Sequence matrix	Not provided	Required	Not required	Switch matrix	Neither	Not provided	Nonoperative
In [6]	Cost function	Not provided	Required	Required	Not provided	Neither	Specific obj.	Nonoperative
In [19]	Not provided	Provided	Required	Required	Not provided	RSSs	Specific obj.	Operative
In [28]	Lookup tables	Provided	Required	Not required	Not provided	Neither	Not provided	Nonoperative
In [29]	Second mapping	Provided	Required	Not required	Not provided	RSSs	Not provided	Operative
In [32]	Reverse mapping	Not provided	Required	Required	Not provided	Neither	Not provided	Operative
In [37]	States sorting	Not provided	Not required	Not required	Matrx operation	Neither	Not provided	Nonoperative
In [38]	Second mapping	Provided	Required	Not required	NLM-based	RSSs	Not provided	Nonoperative
Proposed	Carrier-based	Provided	Not required	Not required	Carrier-based	Both	Versatile	Operative

fact that as the modulation index increases, the redundancy of the switching states decreases, which results in a reduced probability of keeping λ around 0.5.

To evaluate the scheme with time-averaged CMV elimination in depth, an additional inductive load (3 mH) is connected between points N and G referring to [19], and the common-mode current i_{ng} flowing from N to G is measured, as shown in Fig. 13(g)-(i). Accordingly, there is a dc offset of about 2 A in addition to the fluctuating ac component in i_{ng} for the scheme without optimization. Although the CMV peak is minimized in the scheme with minimal CMV magnitude, the non-zero CMV at each cycle results in a considerably increased common-mode current (up to 0.8 A). Compared with the other two schemes, the scheme with time-averaged CMV elimination has lowest common-mode current (less than

0.5 A). Therefore, the proposed scheme can meet different application requirements and provides more flexibility than conventional specific-objective implementations [6], [33]. For instance, the scheme with minimal CMV magnitude can be applied to reduce the system protection voltage, while that with time-averaged CMV elimination can efficiently lower the common-mode current and improve voltage quality in long distribution feeders.

Furthermore, a transient profile is also designed, in which the modulation index increases linearly from 0.2 to 0.8 in 0.25 s, while the fundamental frequency rises linearly from 10 Hz to 50 Hz in the same time. The experimental results of the converter without and with additional inductive load are shown in Fig. 15. As can be seen, the CMV magnitudes in different schemes are similar to the results shown in Fig.

SVPWM Schemes	Time Required (μs)	Memory Req. in Bytes	Time Complexity	Space Complexity
In [4]	6.17	11531	$O(n)$	$O(n)$
In [6]	4.84	6620	$O(1)$	$O(1)$
In [28]	5.28	42709	$O(n)$	$O(n^3)$
In [29]	4.36	8796	$O(n)$	$O(n)$
Proposed	2.42[a] 2.88[b]	3166[a] 3501[b]	$O(1)$	$O(1)$

[a] the proposed scheme with minimal CMV magnitude.
[b] the proposed scheme with time-averaged CMV elimination.

13. Nevertheless, in terms of the common-mode current, it can still be constrained to below 0.5 A in the scheme with time-averaged CMV elimination, while the higher magnitude (up to 1.2 A) is observed in the scheme with minimal CMV magnitude due to the accumulated CMV during the transient process. Not surprisingly, the scheme without optimization not only leads to a dc offset in i_{ng}, but also produces an ac amount with a larger amplitude. The associated results provide further strong evidence of the effectiveness of the proposed method.

C. Comparison With the Existing SVPWM Methods

Table III presents a general comparison between the proposed scheme and typical existing SVPWM methods. Further, Table IV compares the total time and memory requirements in several algorithms, where the algorithms are written in C and implemented in the linear modulation region on a DSP TMS320F28377D, considering the partial underlying constraints of Typhoon. Tables III and IV show the superiorities of the proposed scheme in terms of:

1) System Flexibility: The three or four switching states are typically uniquely determined for a given RVV in many earlier methods [3]–[6], [28], [32], [37]. Even if the RSSs are available in some solutions [19], [29], [38], few can effectively utilize them to optimize converter's performance, which undoubtedly jeopardizes system flexibility. In the proposed scheme, the dynamic RP mechanism not only establishes a one-to-one correspondence between all available RSSs and one unique variable, i.e., the number of level shifts, but also contributes to a general approach of determining the OSS according to control objectives. Moreover, the introduction of carrier-based implementation allows some underlying goals, such as evenly distributing switching losses in CHB converters or balancing capacitor voltages in FC converters, to be achieved by rationally aligning carriers, as explained in Section III-C. Thus, a higher flexibility is achieved.

2) Operation Region: The proposed scheme is able to achieve full-region operation including overmodulation, just as done in [19], [29], [32]. Thus, the output capacity of the converter can be utilized to the greatest extent. However, the other methods can only operate in the linear region with the modulation index M less than 0.866 [3] or 1, implying that at least the shaded area beyond the inscribed circle but within the outer hexagon shown in Fig. 6 is not effectively exploited.
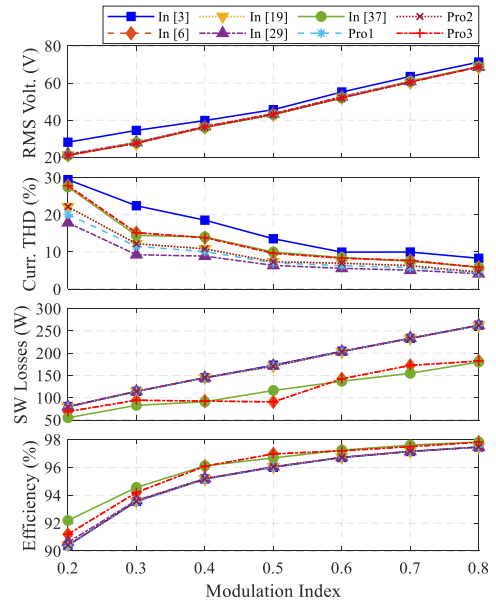

Fig. 16. Comparison of RMS line voltage, current THD, switching losses and converter efficiency in the five-level CHB converter (Pro1: the proposed scheme without optimization; Pro2: the proposed scheme with time-averaged CMV elimination; Pro3: the proposed scheme with minimal CMV magnitude).

3) Time and Space Complexity: As shown in Table IV, very low execution time and memory space are required in the proposed scheme. In [4], since the pulse duration of each switch needs to be calculated by the predefined formulas and a larger number of variables are indispensable, the much longer execution time and higher memory footprint are required. In [6], though both time and space complexity are independent of the number of levels, the fact that almost all computations including time-consuming cost function are based on floating-point operations and complex encoding to generate gate pulses also leads to higher resource requirements. Compared with the other methods, the proposed scheme avoids look-up tables (as in [28]), iterative operation (as in [29]), trigonometric computation, coordinate transformation, and only requires simple logical judgment and arithmetic calculation.

4) Implementation Cost: The proposed scheme achieves a lower implementation cost. On the one hand, the lower execution time and space requirements reduce the performance demands on the real-time processor. On the other hand, the switching sequence and gate pulses in the proposed scheme are generated by carrier-based implementation, which means that the entire algorithm of the proposed scheme can be executed on common DSP chips with integrated PWM modules. In contrast, the switching sequence in many other methods (e.g., [5], [6], [19], [28], [29], [32]) is produced based on line-to-line voltages and it is necessary to assign the duty cycles to respective switching states to output gate pulses at each time step, as explained in Section II-B, which may require a higher performance and more expensive FPGA chip, especially in the case of high switching frequency.

Furthermore, Fig. 16 compares the RMS line voltage, current THD, switching losses and converter efficiency in methods with similar optimization objectives [3], [6], [19] or

switching patterns [29], [37], where the RMS line voltage and current THD are experimented with the parameters same as in Section VI-B, while switching losses and converter efficiency are simulated with the parameters of the switching devices from IKFW50N60DH3 produced by Infineon and the dc-link voltage of each H-bridge and the switching frequency are increased to 300 V and 50 kHz to highlight the differences of different algorithms. As can be seen, the methods using the NTVs to synthesize the RVV (except for [3] using the non-NTVs) produce very similar RMS line voltages. Besides, the proposed method can be flexibly configured to output current waveforms of comparable quality to those of [6], [19], [29], [37]. Fig. 16 also shows that the proposed method can yield switching losses close to existing continuous [19], [29] and discontinuous [6], [37] modulation techniques, since the number of switching actions in each switching period can be changed by adjusting λ. When it comes to converter efficiency, similar conclusions can be found, except that the introduction of conduction losses narrows the gap between different algorithms. In summary, these results show that the proposed method can maintain equivalent voltage output, comparable waveform quality and converter efficiency while providing the aforementioned advantages.

VII. CONCLUSION

In this article, a flexible and decoupled SVPWM algorithm for multilevel converters is proposed, which innovatively combines two-level SVPWM-based method and carrier-based implementation. The three phases of the offset vector are decoupled both in real-time calculation and in hardware implementation, which not only facilitates a dynamic RP mechanism to provide all RSSs to maintain high flexibility, but also enables the introduction of carrier-based implementation to reduce complexity considerably. Simulation and experimental results show that the proposed scheme can achieve full-region operation for any n-level CHB and FC converters, can be flexibly regulated to cater to different applications, and only requires very low execution time and storage requirements.

The proposed scheme can be potentially extended to operate under fault conditions. Since the value of the number of level shifts n_{s} has a one-to-one correspondence with the available switching states, fault-tolerant operation can be accomplished by tuning the range of n_{s} in accordance with the type of fault, which will be further investigated in future work.

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