Ductile dicing for optical facets and waveguides in silicon nitride

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Silicon nitride boasts high refractive index and optical transparency from around 250nm up to 7um, enabling low-loss planar-integrated devices spanning the UV to the mid-infrared. As a platform, silicon nitride benefits from wafer-scale fabrication, CMOS compatible processes, and can be tailored for different applications during fabrication, including nonlinear applications [1,2]. However, as with many integrated photonic platforms, it can be challenging to process facets for end coupling, where grating couplers can not be used. Traditional polishing is not only time consuming and challenging to produce precisely placed facets, but chipping and delamination of the waveguide layers result in poor yields.

In recent years diamond machining, typically using dicing saws, has opened routes to machine optical quality surfaces in materials such as lithium niobate, silicon, and silica [3,4,5]. In this work, we have refined these techniques to dicing waveguides and optical-quality facets in a silicon nitride platform in a single step, with no requirement for polishing. Here, we have used the saw to laterally define the waveguide to demonstrate both the precision, the lack of delamination, and the lack of chipping.



Fig. 1 (a) shows a schematic of the silicon nitride platform and use of a dicing blade for facet cuts. (b) shows microscope images of one resulting waveguide, the top shows an end view of the facet, the lower shows a top-down view of the waveguide.

The platform consisted of a silicon substrate with a 3 μ m SiO₂ layer, coated with 300 nm of silicon nitride and capped with a 1.4 μ m TEOS layer. A DISCO DAD3430 dicing saw was used to cut waveguides 24 μ m deep and 15 μ m wide. A 24 μ m deep facet cut was then performed perpendicular to the waveguides to allow for optical coupling. Microscope images showed good waveguide form with little topside chipping. We will present ultra-precision machining for facet preparation of integrated silicon nitride devices, including surface roughness, and coupling and propagation losses of the resultant features. We will also discuss prevention of surface chipping and delamination, and extension of these techniques to other platforms such as silicon-on-insulator.

References

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