POWER BALANCE CONTROL FOR A TWO-STAGE SOLAR INVERTER WITH LOW VOLTAGE RIDE THROUGH CAPABILITY

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ABSTRACT: The latest grid codes require the renewable energy sources (RES) to provide ancillary services during fault and post fault conditions. More specifically, in case of a short-duration voltage dip, the grid-tied photovoltaic (PV) system should stay connected and support the grid by injecting reactive power. However, meeting these requirements during voltage sags is a challenge for two-stage systems, due to the power imbalance between the dc/dc converter and the inverter, resulting in dc-link voltage excursions and output current overshoots. In this paper, a power balance control scheme is proposed, by which, a successful low voltage ride through (LVRT) and smooth dc-link voltage variation are achieved, while the output current is kept within the predefined limits. Two reactive power injection strategies are investigated that exhibit different dynamic response during voltage sags. The effectiveness of the proposed LVRT control is verified though simulations of a 2 kVA solar system.
Keywords: Grid code, grid connected inverter, low voltage ride through (LVRT), photovoltaic (PV), power control, voltage support

1 INTRODUCTION

The high penetration level of grid-connected solar inverters raises concern regarding their effect on grid stability and response under disturbances [1]. Although interconnection standards of the recent past (e.g. IEEE 1547 and UL1741) required disconnection of PV power plants in case of voltage sags (e.g. when the voltage at the point of common coupling (PCC) drops below a certain threshold [2]), the high PV penetration levels reached have imposed a fundamental differentiation of requirements in new grid codes, according to which:

- Distributed generation (DG) should not disconnect in case of grid faults, i.e. it should exhibit Fault Ride-Through (FRT) capability
- It should support the grid voltage by injecting reactive current during voltage depressions.

LVRT requirements are quantified via voltage-time characteristics, such as the ones shown in Figure 1 for certain grid codes, [3], [4]. The required reactive current injection as a function of the magnitude of the voltage dip is presented in Figure 2.

PV generators are interfaced to the network through either a single-stage inverter or a two-stage converter with an intermediate dc-link [5]. The later offers the possibility of transformerless interconnection to the low voltage (LV) grid, leading to higher system efficiency. In addition, two independent/decoupled controllers can be adopted [6], with the dc/dc converter tracking the maximum power point (MPP) of the PV source and the inverter being responsible for dc voltage and output current control.

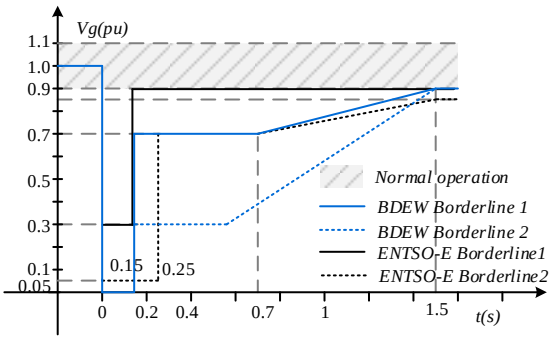

Figure 1: LVRT characteristics for different grid codes.

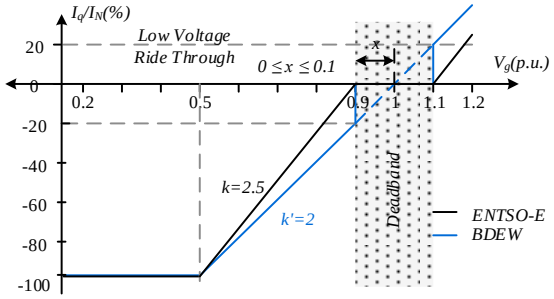

Figure 2: Reactive current injection against voltage.

A common approach for meeting the LVRT requirenents in single-stage systems is to disable the MPPT algorithm and shift the operating point of the PV generator according to a constant output current command, [7]–[9]. However, these techniques cannot be applied in a two-stage topology, due to the imbalance between the power provided by the PV generator and that fed to the grid, creating dc overvoltages. One solution would be to utilize energy storage systems (ESS) across the dc-link, such as batteries [10] or super capacitors [6], in order to absorb excess power during voltage sags. This, however, inevitably impacts cost and complexity. In [11] and [12] it is proposed that the dc/dc converter pauses MPP tracking and shifts the operating point of the PV system to a suboptimal power level. The PV current I_{PV} is reduced by the ratio of the voltage sag to the nominal voltage. However, these techniques rely on a linear approximation of the relation between PV current and power and are susceptible to the power losses of the two-stage converter.

A more sophisticated control scheme has been presented in [13], where a combination of a proportional-integral (PI) and a proportional-derivative (PD) controller is used to determine the operating point of the PV generator during faults. This is an effective, yet complex approach that requires real time gain readjustment (gain scheduling strategy) to meet the response times imposed by the grid codes.

The purpose of this work is to propose a simple and effective control scheme that meets LVRT requirements with minimum dc voltage variations, limited output

current overshoot, short response time, without employing additional ESS, switching devices or sensors. Two reactive current injection strategies are investigated, namely *active current priority*, in order to effectively limit dc voltage overshoot, and *reactive current priority*, in order to minimize the response time of reactive power injection. The performance of the proposed controller is validated through simulations using Matlab/Simulink.

2 POWER BALANCE CONTROLLER

The overall diagram of the grid-tied solar inverter is shown in Figure 3, in which the power circuit is indicated in black color and measurement signals in blue. The front-end stage is a boost dc/dc converter, responsible for regulating the operating point of the PV generator. The standard perturb and observe (P&O) MPPT algorithm is applied during normal operation for tracking the MPP, while a PI controller becomes active during fault mode to shift the operating point of the PV generator in order to keep the inverter output current within limits. In all cases, the transformerless inverter maintains the dc-link voltage to its reference.

2.1 Phase locked loop

The phase locked loop (PLL) algorithm is a key feature for a successful LVRT response. A double second order generalized integrator (DSOGI) PLL is used, which cancels out harmonics at twice the line frequency, introduced by the negative sequence components, [14], [15]. The block diagram of the PLL is presented in Figure 4. This technique is based on the quadrature signal generator (QSG) equations (1) - (2) with an appropriate sequence extraction relation, as in (3), where ξ denotes phase shift of -90 deg and ω is the line frequency.

$$H_d = \frac{V_{out}}{V_{in}} = \frac{k \cdot \omega \cdot s}{s^2 + k \cdot \omega \cdot s + \omega^2} \tag{1}$$

$$H_q = \frac{\xi V_{out}}{V_{in}} = \frac{k \cdot \omega^2}{s^2 + k \cdot \omega \cdot s + \omega^2} \tag{2}$$

$$\begin{bmatrix} V_\alpha^+ \\ V_\beta^+ \end{bmatrix} = \frac{1}{2} \cdot \begin{bmatrix} 1 & -\xi \\ \xi & 1 \end{bmatrix} \cdot \begin{bmatrix} V_\alpha \\ V_\beta \end{bmatrix} \tag{3}$$

2.2 Inverter current controller

A proportional resonant (PR) regulator is selected for the inverter inner current control loop [13], which has significant gain around the line frequency and sufficient attenuation at higher frequencies. The block diagram of the current control is illustrated in Figure 5. The PR controller is described by the transfer function (4).

$$H_{PR}(s) = K_p + K_i \frac{s}{s^2 + \omega_0^2} \tag{4}$$

Alternatively, the integral term of the PR controller can be expressed by (1), in which case, an adjustable gain at the resonant frequency is obtained, [16]. The grid voltage in the stationary reference frame is added to the output of the PR controller to perform a feed-forward loop that enhances the controller response, [17] (Figure 5).

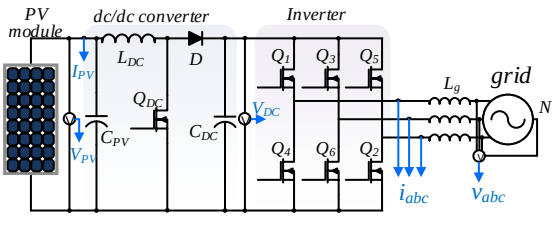

Figure 3: Schematic diagram of a two-stage PV inverter.

A common PI controller regulates the power to be transferred to the grid, P_g, in order to keep V_{dc} at its reference, as depicted in Figure 6. Given that the q component of the grid voltage is zero via the PLL [18], the active current is given by (5).

$$i_{d\_PI} = \frac{2}{3} \cdot \frac{P_g}{V_d} \tag{5}$$

In Figure 6, the output of the PI controller is saturated to a maximum power level determined by the actual grid voltage and the maximum permissible current I_{max}, according to (6). Thus, i_{d_PI} cannot surpass I_{max}.

$$P_{max} = \frac{3}{2} \cdot V_d \cdot I_{max} \tag{6}$$

2.3 Dc/dc converter power controller

Figure 7 illustrates the proposed power balance controller of the front end converter. The voltage sag detection mechanism is based on continuous monitoring of the d component of the grid voltage. While V_d is greater than 90 % of the nominal value (normal operation), the P&O algorithm is executed, otherwise the MPP tracking is paused and the PI controller is activated to ensure operation at a reference power, P^*_{PV}.

The reference power is calculated as the minimum of *the pre-fault power at MPP*, P_{mp}, and a limit to the permissible PV power, P_{lim}, given in (7), where i_{q_LVRT} is the reactive current determined in Figure 2.

$$P_{lim} = \frac{3}{2} \cdot V_d \cdot \sqrt{I_{max}^2 - i_{q\_LVRT}^2} \tag{7}$$

According to this reactive power injection (RPI) strategy, the operating point of the PV generator is shifted in order to ensure that the output current magnitude, i_s, never exceeds I_{max}. The PI controller remains active after fault clearance, until P_{PV} is restored to its pre-fault level.

It is worth noting that the new suboptimal power

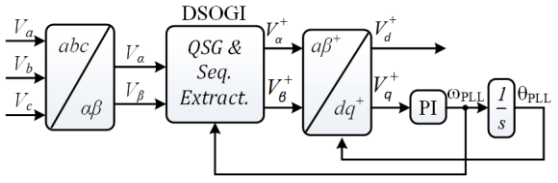

Figure 4: Block diagram of the PLL.

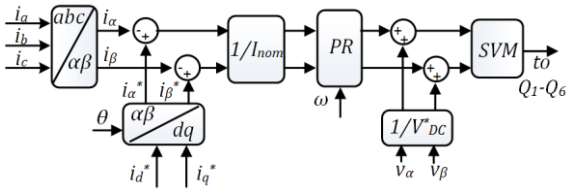

Figure 5: Block diagram of the inverter current control.

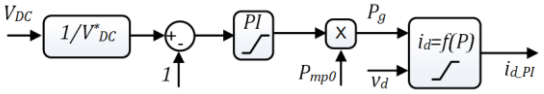

Figure 6: Control scheme of the dc-link voltage controller.

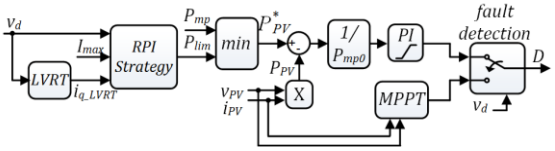

Figure 7: Power balance controller of the dc/dc converter.

level corresponds to a PV voltage greater than that at the MPP (right hand side of the *P-V* curve). This operation is preferable for several researchers compared to the left part of the characterisitc [19], [20]. The transition is controllable by adjusting the maximum allowable duty-cycle step and the gains of the PI controller, thus avoiding surge currents in the power device, [12]. Throughout this process, the inverter control remains unaffected. However, the actual power fed to the grid is slightly lower than P_{lim}, due to the system power losses.

Concerning the calculation of the reference currents, i_d^* and i_q^*, two alternatives are proposed and evaluated, exhibiting different response during sag transients.

- *Case A*: *active current priority*

In this case, the active and reactive current references are given in (8). During the voltage sag transient, the inverter provides the active current needed to contain V_{dc} variations, setting the active reference current i_d^* (Figure 5) equal to the output of the dc-link controller i_{d_PI} (Figure 6). On the contrary, the reactive reference current i_q^* is saturated in order to keep the total current within limits, essentially giving a lower priority to the reactive power injection.

$$\begin{cases} i_d^* = i_{d\_PI} \\ i_q^* = min\left(i_{q\_LVRT}, \sqrt{I_{max}^2 - i_d^{*2}}\right) \end{cases} \quad (8)$$

- *Case B*: *reactive current priority*

The (i_d^*, i_q^*) references are now determined by (9). The provision of the required i_{q_LVRT} by the inverter is prioritized, setting the reactive reference current i_q^* (Figure 5) directly equal to i_{q_LVRT} as determind via Figure 2. On the other hand, the active current reference i_d^* is now saturated to keep i_s within limits. This approach may lead to increased V_{dc} overshoot.

$$\begin{cases} i_d^* = min\left(i_{d\_PI}, \sqrt{I_{max}^2 - i_q^{*2}}\right) \\ i_q^* = i_{q\_LVRT} \end{cases} \quad (9)$$

The main advantage of the proposed control technique, compared to previous works, is the robustness and ease of implementation of the dc/dc converter controller. The reference power during voltage sags is directly calculated, in contrast to earlier works [13], where the power set point is indirectly applied, based on the dc voltage variation, through additional controllers that increase the complexity of the system. Further, with the developed strategy the inverter control remains unaffected by grid voltage sags, resulting in smoother fault and post-fault transients. No gain scheduling is required, rendering the proposed scheme suitable for implementation in a digital signal processor (DSP).

3 SIMULATION RESULTS

The effectiveness of the proposed controller is evaluated through simulation of a 2 kVA PV inverter, connected to the LV grid. The values of the circuit parameters and the controller gains are listed in Table I. As shown, the maximum allowable current is 1.5 times the nominal one.

Table I: Simulation parameters.

C_{PV}	220 μF	$k_{P\text{-}Pow}$	0.04
C_{DC}	560 μF	$k_{I\text{-}Pow}$	40
L_{DC}	600 μH	$k_{P\text{-}DC}$	25
L_g	10 mH	$k_{I\text{-}DC}$	2500
I_{nom}	3.93 A	k_{PR}	0.05
I_{max}	$1.5 \cdot I_{nom}$	$k_{P\text{-}PR}$	0.6
P_{mp0}	1920 W_p	$k_{I\text{-}PR}$	1.8
Irrad	800 W/m^2	k_{PLL}	3
Temp	25 ºC	$k_{P\text{-}PLL}$	0.05
F_{sw}	20 kHz	$k_{I\text{-}PLL}$	0.2

A symmetrical 60 % voltage sag (0.4 *pu* remaining voltage) is considered, as shown in Figure 8. The responce of the DSOGI PLL technique during the voltage dip is quite satisfactory, as illustrated in Figure 9. Both active/reactive current prioritization approaches (*Case A* and *B*) are examined.

Prioritizing active current injection (*Case A*) leads to a more effective control of V_{dc}, as observed in Figure 10 (blue line), associated with the immediate increase of the active current reference, i_d^*, up to I_{max}, shown in Figure 11(a). On the other hand, a delay in reactive current injection, i_q^*, of ~20 ms is noted in Figure 11(b). With the alternative *Case B*, the required i_q^* is provided with no delay, leaving a reduced margin for i_d^* increase, which in turn, has a notable impact on V_{dc} regulation (red line in Figure 10). In both scenarios, the output current magnitude never exceeds I_{max}.

Figure 12(a) illustrates the active power produced by the PV source and injected to the grid for both cases. The PV power (yellow line) is reduced at the same rate in both examined scenarios, while the dc/dc converter effectively reaches the new set point, P_{PV}^*, (purple line) within 20 ms. An increased amount of active power is initially transferred to the grid in *Case A* (blue line) compared to *Case B* (red line), that discharges the dc-link capacitors and thus mitigating the dc voltage overshoot (blue line in Figure 10). The reactive power injected is

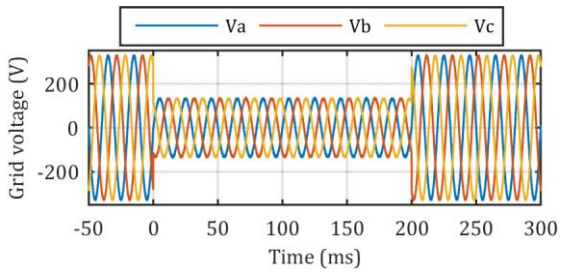

Figure 8: Grid voltage during symmetrical 60% voltage sag.

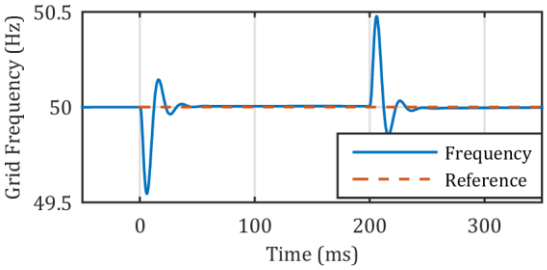

Figure 9: Responce of the DSOGI PLL algorithm.

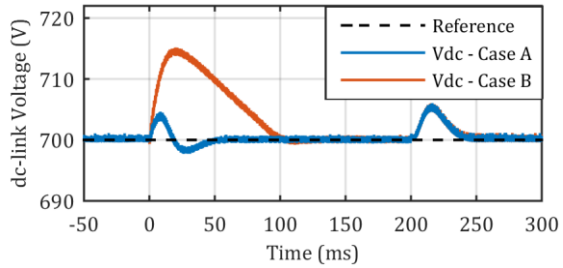

Figure 10: Dc-link voltage variation during voltage sag.

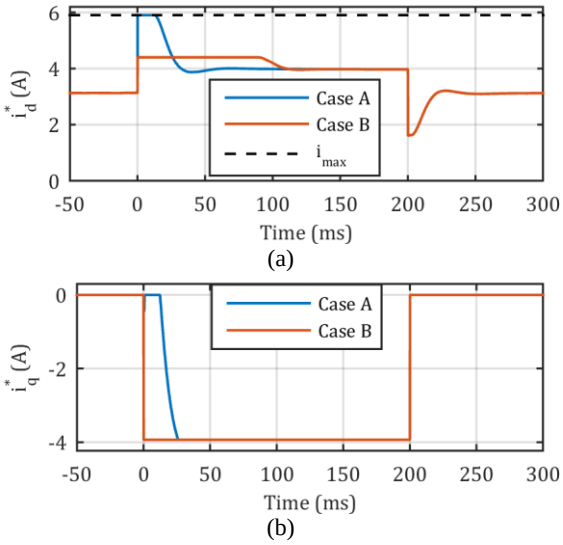

Figure 11: (a) Active and (b) reactive output current references.

shown in Figure 12(b), exhibiting a delay time of 20 ms in *Case A* as expected.

The ac-side currents are illustrated in Figure 13. It is evident that the output currents are in good agreement with the reference values of Figure 11, verifying the effectiveness of the inverter controller.

The voltage and current of the PV generator, along

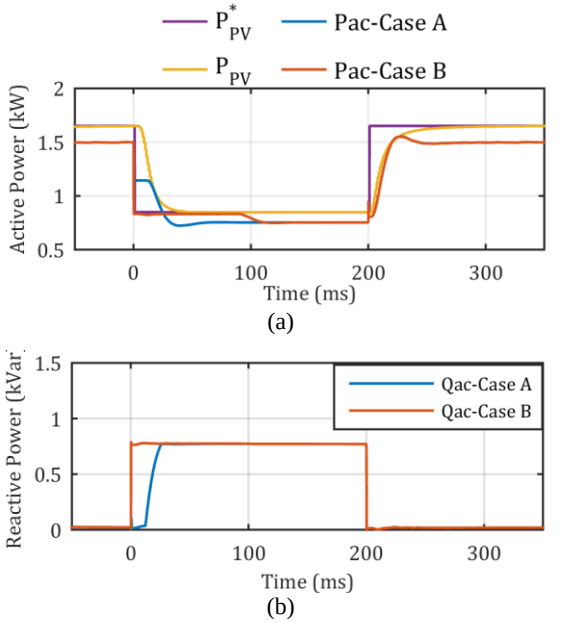

Figure 12: (a) Active and (b) reactive power at the dc and ac side.

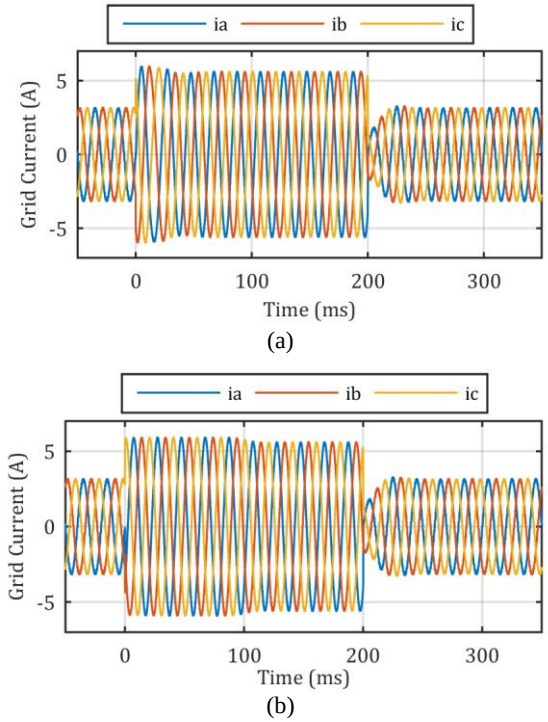

Figure 13: Output currents in (a) *Case A* and (b) *Case B*.

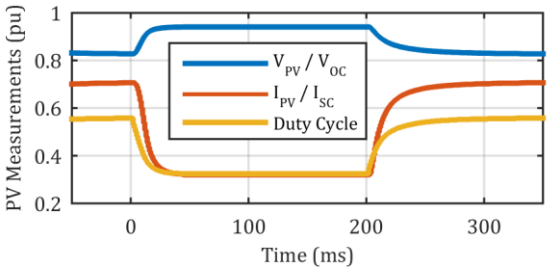

Figure 14: PV voltage and current variation along with the respective duty cycle.

with the duty cycle command of the dc/dc converter, are depicted Figure 14.

4 CONCLUSIONS

In this paper, a power balance control strategy for two-stage PV systems with LVRT capability is introduced. Low dc-link voltage variation is achieved by giving priority to the active current reference, while a faster response of reactive power is accomplished by giving priority to the reactive current reference. The developed technique does not rely on any approximations or other limiting assumptions and does not require any additional sensors. The robustness and ease of implementation renders the developed technique suitable for practical applications. Simulation results have confirmed that the inverter meets LVRT requirements, with very good overall response characteristics.

5 ACKNOWLEDGMENTS

Mr. G. Kampitsis and Mr. E. Batzelis are supported in their PhD studies by "*IKY Fellowships of Excellence for Postgraduate Studies in Greece - Siemens Program*".

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