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Buried 3D spot-size converters for silicon photonics

W. Zhang,[1] M. Ebert,[1] J. D. Reynolds,[1,2] B. Chen,[1] X. Yan,[1] H. Du,[1] M. Banakar,[1] D. T. Tran,[1] C. G. Littlejohns,[1] G. T. Reed,[1] and D. J. Thomson[1,*]

[1]Optoelectronics Research Centre, Zepler Institute for Photonics and Nanoelectronics, Faculty of Engineering and Physical Sciences, University of Southampton, Southampton SO17 1BJ, UK
[2]Sustainable Electronic Technologies Research Group, Electronics and Computer Science, Faculty of Engineering and Physical Sciences, University of Southampton, Southampton SO17 1BJ, UK
*Corresponding author: d.thomson@soton.ac.uk

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In this article, an efficient spot-size converter (SSC) for low-loss optical mode transition between large and small waveguides based upon a buried three-dimensional (3D) taper is demonstrated. The SCC can pave the way for scalable, low-loss coupling between on-chip waveguides of different sizes and with external components such as optical fibers and III-V active components, and it can be a key element in solving the challenges surrounding the economic high volume packaging and assembly of photonic integrated circuits. Through the use of a bespoke fabrication process, continual tapering of the waveguide dimensions both in width and height is achieved, offering minimal perturbance of the optical mode throughout the structure. The SSC exploits the space of the buried oxide (BOX) on a standard silicon-on-insulator wafer, leaving a planar top wafer surface, meaning that, crucially, further processing of the wafer is not inhibited in any way. Fabricated proof-of-concept devices demonstrate coupling between standard single-mode 220 nm thick silicon waveguides and large-core waveguides with dimensions about 3 μm wide and 1.5 μm height with BOX thickness of 2 μm. Coupling losses as low as 0.56 dB are achieved, limited mostly by the material loss of the polysilicon used. Substantial improvements can be yielded by simply changing the infill material and through optimization of the fabrication process and design. The demonstrated SSC approach can further be applied to other photonic platforms such as silicon nitride on insulator and so on. © 2021 Optical Society of America under the terms of the OSA Open Access Publishing Agreement

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1. INTRODUCTION

Silicon photonics (SiPh) has been developed as a mature platform for the mass production of versatile integrated photonic circuits powered by the compatible, complementary metal-oxide-semiconductor (CMOS) technology. This has made it possible for SiPh interconnects to replace the traditional low-bandwidth electrical input/output (I/O) ports for high-performance and high-bandwidth optoelectronics applications [1]. Co-packaged optics is believed to be the next integration phase, requiring optics to be closer to high-performance system-on-chips (SoCs). It is becoming a scalable optical technology enabling high-volume, low-cost transceivers that can be co-packaged within larger electronic systems, e.g., switch application-specific integrated circuits (ASICs). It will also allow dense optical/electrical (O/E) chiplet integration and provide high bandwidth as well as energy and cost efficiency for data communication and computation [2].

At the present stage, beyond the challenges of achieving a high bandwidth [3,4], a robust solution for SiPh component assembly and packaging is required, which is currently orders of magnitude more expensive than electronic packaging. This is mainly due to the fact that SiPh packaging and assembly faces several challenges, such as automated high throughput [5,6], accurate alignment of optical fibers [1,7] as well as the hybrid and heterogeneous integration of III-V active components (laser, amplifiers, and detectors [8–12]).

To address these problems, robust and highly precise vertical and horizontal alignment is typically required for fiber array packaging and the monolithic/butt-coupled integration of III-V components where the optical mode is butt-coupled to a silicon rib waveguide [6,7,9,10]. The main challenge for butt-coupling strategies is matching the mode field of SiPh waveguides with optical fiber and output facets of III-V components. This has been widely explored in the last 20 years to provide a reduction in coupling losses while operating over a wide optical bandwidth and with tolerance to practical alignment errors.

For high-efficiency coupling to standard single-mode optical fibers (SMF28), the typical mode field diameter (MFD) of the waveguide couplers should be matched with that of the fiber, which is around ∼10 μm at 1.55 μm wavelength. Typical single-mode silicon photonic waveguide have dimensions ∼220 nm × 450 nm and therefore result in almost a 3 order of magnitude mode area mismatch to that of standard optical fibers. To solve this issue, inversely tapered SiPh waveguides have been proposed to couple light from the waveguide core to the fibers [13–17]. The efficiency of coupling is high between inversed waveguides and fibers, but

its implementations are concerned with the fabrication tolerance, yield, and required package alignment accuracies. Thus, spot size converters (SSC) have been introduced to transfer the optical mode from a high-index waveguide to a low-index large waveguide [7]. The SSCs are usually part of the cladding of the high-index contrast waveguides, bridging the inverse high-index taper and large core low-index cladding waveguides. Typical materials used for the SSC are SU8 [16,18,19], silicon oxide [20], silicon nitride [21–25] and SiON [26]. These SSCs protrude from the planar waveguide surface and can impede further CMOS wafer-scale processing, for example, chemical mechanical polishing (CMP). Besides, for most of these demonstrated SSC solutions, non-silicon materials are used, or silicon deep-trench etching with suspended SiO_2 waveguides must be adopted, which are not well suited for CMOS-compatible processing. For a universal SSC design, the photonic mode expansion requires both lateral and vertical dimension tapering. It should give the designers the flexibility to control the SSC size for different edge coupled components [1,7–10].

Under such context, here a buried 3D SSC approach has been realized, capable of converting a traditional submicrometer silicon rib waveguide mode into a micrometer-scale waveguide. The SSC is composed of polysilicon, which is filled into a 3D tapered trench on conventional silicon-on-insulator (SOI) wafers with 220 nm silicon overlayer and 2 μm buried silicon dioxide (BOX) layer. The fabrication process uses aspect-ratio-dependent lag etching of the BOX, of which the etch depth is trench width dependent, a technique that has been used in microelectromechanical system (MEMS) device fabrication [27]. The BOX trench depth was engineered from 0 nm to approximately 1.3 μm in depth with the width enlarged up to around 3 μm. The trench is filled with polysilicon and later planarized. The demonstrated 3D SSC approach only requires silicon-based materials and provides a top planar surface, which does not restrict further processing options. The total mode transition loss of the fabricated SSC is as low as 0.5 dB, limited by the material loss of the polysilicon material used. Excluding the polysilicon material loss, the 3D SSC exhibits an optical loss ~ 0.2 dB that is mainly due to the geometrical designs and roughness from fabrication.

Previous demonstrations of SSC based upon 3D tapers have had many drawbacks, meaning that they are not well suited for the silicon photonics industry. For example, the demonstrations in [28–30] rely on anisotropic chemical etch to a specific crystal plane to create the taper shape. This limits how the taper can be orientated on the wafer, creating a design restriction, and it requires non-standard SOI wafers with a specific crystal orientation, fixes the taper length based upon the two waveguide heights required, is limited to a linear taper shape in depth, and limits the material of the taper to one with a crystal plane-dependent etch. In [31], the taper was formed using a gray-tone lithography approach, which results in high surface roughness and therefore high optical loss. In [32], multiple lithography and etching steps were required, which would add significant process effort and result in abrupt steps in waveguide height. The 3D taper in [33] uses a submicrometer loading effect requiring multiple oxidation and etching steps in order to smooth the taper surface, which again adds process complexity. Reference [34] uses a non-standard fabrication technique to impress a height taper in SU8, which would be difficult to realize in a CMOS manufacturing facility. In [35], localized focused ion beam milling is used to create the height taper; however, again, this is a non-standard technique for CMOS processing that would not provide the throughput required for the high-volume fabrication. Demonstrations [28–33] start with a thick silicon layer and etch it down to make the thin silicon layer. The thickness of the thin silicon will then vary by the same original silicon thickness variation across the wafer plus any etch rate variation. The thickness variation of thick SOI wafers is, however, typically large comparable to final thickness that would be required for a thin silicon layer containing a high-speed silicon optical modulator, for example (220–340 nm), and therefore an intolerably large thickness variation will likely result in the thin silicon layer. In all cases of 3D-taper-based SSC [19,28–33,35] and non-3D-taper-based SSC, for example [18,20–22,26,36,37], the top surface of the wafer is not planar after the taper formation, which impacts onward processing. For example, CMP is not possible on the thin silicon layer as required for the hybrid integration of lasers and amplifiers and the fabrication of modulators and detectors. The method introducing a multilayer SSC [22,23,25] is also difficult for leveraging current silicon photonic lines that are mostly processing a single high-index waveguide layer, but this is promising for future 3D photonic circuit integration.

Our demonstrated 3D-taper-based SSC can be formed using a single lithography and etching step followed by deposition of the waveguide taper material and planarization. These are all processes that can be simply implemented in a typical CMOS fabrication facility. For our proof-of-concept demonstration, polysilicon was used as the waveguide taper material; however, our approach is flexible through the deposition of other photonic materials to form the waveguide taper such as silicon nitride and its photonic Damascene process [38]. In our approach, the taper shape can be nonlinear and optimized both through the layout and the etch process. The length and orientation is also flexible, and standard 100 SOI wafers can be used. The starting material, which is where the small waveguides are eventually formed, is thin SOI with a thickness variation smaller than ± 10 nm. The thick waveguides, which are more tolerant to thickness variation, are then formed in the etched trenches. Finally, in our approach the top surface of the wafer remains planar after the taper formation with the thicker waveguides extending downward into the wafer, and thus forward processing of the wafer is not impacted.

This work paves the way for scalable, low-loss butt-coupling for fibers and bonded III-V active components. In addition to this, our demonstrated 3D SSC can facilitate the realization of an optimal photonic platform where multiple waveguide sizes can be formed on chip to achieve the best performance from each component, rather than using a universal waveguide height where the performance of each component is compromised to an extent. For example, high-bandwidth components such as optical modulators and detectors can be formed in submicrometer waveguides where low capacitance, low access resistance, and a compact optical mode is critical, while passive elements can be formed in larger waveguides, where propagation loss, sensitivity to fabrication tolerances, and polarization dependence are of more importance. Our proposed SSC can act as the low-loss optical bridge between the different waveguide sizes and also to form the larger waveguides themselves. The trench etching of this SSC could also be used as an interlayer slope waveguide coupler for a multilayer silicon photonics platform [39].

2. DESIGN AND FABRICATION

A. Design of the SSC

The 3D SSC design is schematically shown in Fig. 1 based on SOI with a 220 nm silicon overlayer and a 2 µm BOX. In Fig. 1(a), conventional single crystalline SOI rib waveguide [Fig. 1(c)] is connected with a buried polysilicon 3D SSC and a thick polysilicon waveguide [Fig. 1(b)], of which the thickness is limited by the 2 µm BOX, and the width can have an extensive range >3 µm. The SSC exploits the space of the BOX and provides a planar surface above the silicon and polysilicon layer. The slope of the BOX in Fig. 1(d) is realized through reactive ion etching and will be explained in Section 2.B. The single-mode rib waveguide has a height of 220 nm and width 450 nm [Fig. 1(c)], and the large waveguide realized here has a width of 3 µm and height 1.5 µm. The optical modes of small and large waveguides are shown in Figs. 1(e) and 1(f), respectively. From thick waveguide to thin waveguide, the polysilicon depth was designed to decrease linearly as shown in Fig. 1(d), which was experimentally focused on. By 3D finite-difference time-domain (FDTD) simulation verification, the polysilicon width can be linearly or nonlinearly modulated to have a transmission efficiency above 99% for both the TE polarization (220 nm × 450 nm SOI rib/strip waveguide) and TM polarization (220 nm × 450 nm strip waveguide). No polarization sensitivities of the SSC concept were observed in simulation. It should be noted that, referring to the previously reported 1.5 µm SOI platform with 300 nm BOX [40], the mode leakage to the handle wafer is negligible for the designed SSCs and thick waveguides shown in Fig. 1. Hereafter, the experimental work focuses on the TE polarization.

B. Fabrication of the SSC

The fabrication process flow of the SSC is shown in Fig. 2. Starting from the SOI wafer, a 30 nm silicon dioxide layer was thermally grown on the surface as a chemical mechanical polishing (CMP) stopping layer for step 6. Next, DUV-248 scanner lithography was used to define the positions of SSC trenches in the photoresist. The silicon dioxide and silicon overlayer were then etched by inductively coupled plasma (ICP) etching in step 3. For the SSC trench etching, a new recipe was developed employing the lag effect to form the taper shape within the BOX. The etched BOX trench was then filled with amorphous silicon, which was deposited by low-pressure chemical vapour deposition (LPCVD). Next, the wafer was annealed to transform amorphous silicon into polycrystalline silicon and CMP was used to planarize the wafer back to the 30 nm silicon dioxide stop layer. Again, scanner lithography was used to pattern the waveguides and grating couplers in the top silicon layer, which are etched by ICP. Finally, a 1 µm silicon dioxide top cladding layer was deposited by plasma-enhanced chemical vapor deposition (PECVD). The developed in-house CMP process results in less than 10 nm trench thickness thinning (dishing)

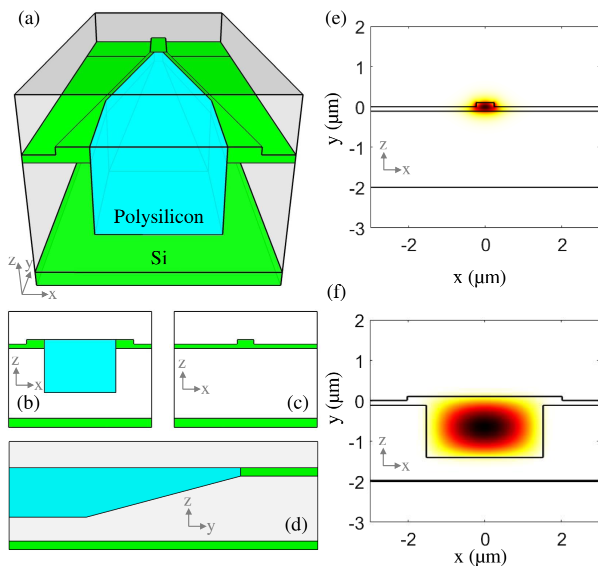

Fig. 1. (a) Schematic drawing of a buried 3D SSC; (b) cross section of the larger waveguide; (c) cross section of the submicrometer silicon rib waveguide; (d) cross section of the propagation direction, including thick waveguide, SSC, and silicon rib waveguide; (e) optical mode of the submicrometer single-mode silicon rib waveguides (width 450 nm, height 220 nm); (f) optical mode of the large waveguide (width 3 um, height 1.5 um).

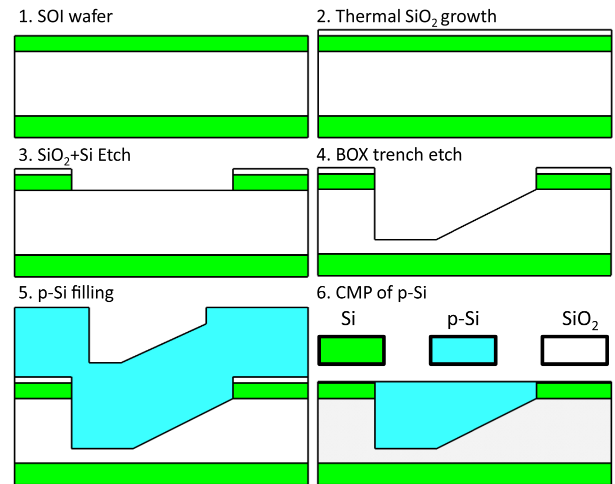

Fig. 2. Fabrication process flow of the 3D polysilicon SSC.

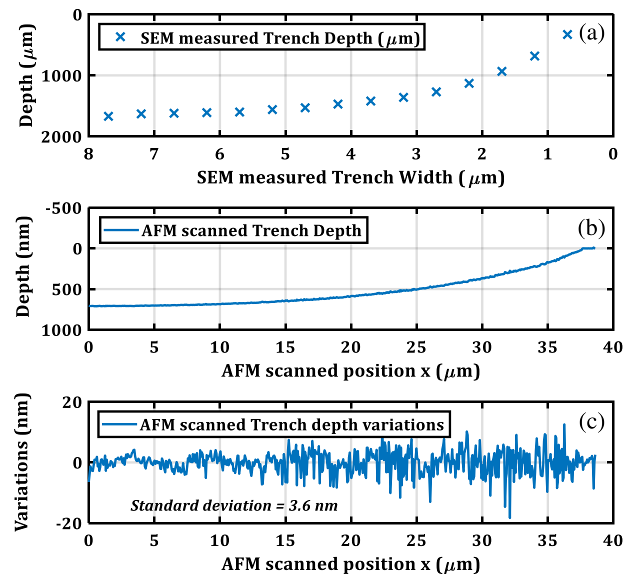

Fig. 3. (a) Measured relationship between the patterned resist trench width and etched depth of silicon oxide. (b) AFM scanned depth profile of the SSC trench. (c) The depth variations of the etched sloping trench.

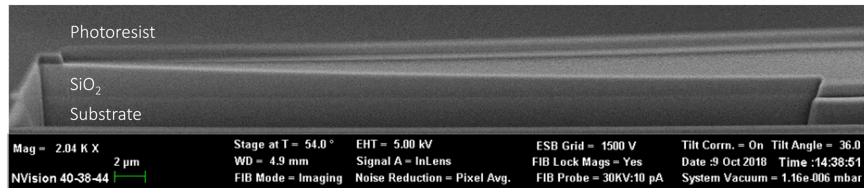

Fig. 4. Cross-section view of the etched sloping trench on silicon dioxide.

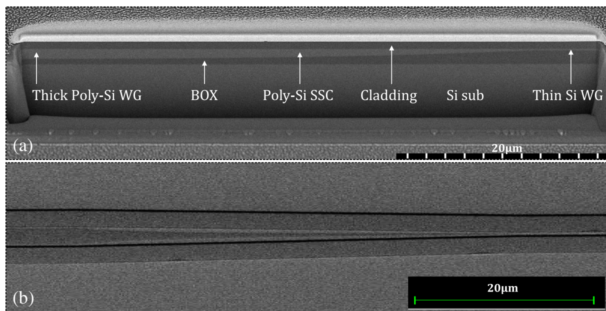

Fig. 5. (a) Cross-section view and (b) top view of the fabrications of the polysilicon SSC.

when trench width is 7 µm. No additional steps were introduced to reduce any roughness resulting from the CMP process.

The developed SSC trench etching recipe used C_4F_8 and Ar at flow rates 35 sccm and 15 sccm, respectively. The RF platen power and chamber pressure were 100 W and 3mT respectively. A thick resist with total height 1.3 µm was coated for the etching steps 3 and 4 in Fig. 2. For recipe development, 2 µm thermal SiO_2 on bulk silicon wafers were used. Ultimately, the developed etching recipe allows SiO_2 etch rate variation by changing the trench window width defined by the thick top resist as shown in Fig. 3(a). Explicitly, the SSC trench structures were realized by exploiting the aspect ratio dry etching (ARDE) effect [41], where the etch rate at the bottom of the trench correlates with the aspect ratio [42]. The etch rate depends on several mechanisms such as ion shadowing, Knudsen transport of neutrals, differential charging of the insulator, and an influx of neutrals, ions, and electrons as well as the removal of the reaction products [43]. Using a C_4F_8 gas chemistry in the plasma promotes the amount of polymerization within the process, enabling an even stronger ARDE [44]. During the etch process, the narrow and thin tip of the SSC should not be attacked, while the SiO_2 in the wider and thicker waveguide area can be etched down deeply. By changing the trench width from 0 to 8 µm, the etched depth varies from 0 to 1.7 µm. The trench slope was scanned by atomic force microscopy (AFM) on the test wafer during the recipe development to verify the profile and roughness of the trench surface as exhibited in Fig. 3(b). A trench depth of zero was successfully realized at the beginning of the slope on the right side, which is essential to achieve low optical transition loss in the 3D SSC. The scanned region covers a trench depth and length around 700 nm and 37 µm, respectively. Roughness on the surface of the taper is within ±10 nm for the entire scanned length, and it is within ±5 nm for depths larger than 600 nm as shown in Fig. 3(c), which is interpreted from Fig. 3(b). Longer etching times can be used to adjust the trench depth while simultaneously keeping a smooth depth transition as will be shown in the fabricated device. The trench aspect ratios are changeable by modifying the recipe. For example, for two different recipe variants

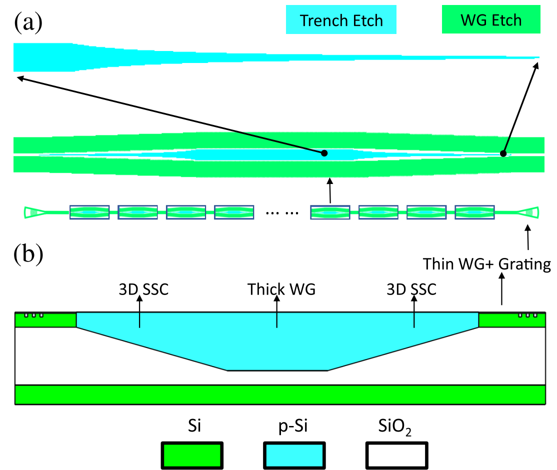

Fig. 6. (a) Top view of polysilicon section width variation of the SSC; (b) side view of the waveguide, SSC to 220 nm SOI rib waveguides.

in our process development, with a 7 µm wide trench a similar depth was achieved, whereas for a 700 nm wide trench a difference in etch depth of around 750 nm was observed. The etching recipe is therefore flexible and can be redesigned for different application requirements.

An example of the trench profile achieved in SiO_2 on bulk Si wafers taken by scanning electron microscope (SEM) is displayed in Fig. 4. The taper length is 50 µm, and the width of the trench was linearly tapered from 200 nm to 3 µm, which results in a trench slope with depth from 0 to 1.3 µm. The optimized maximum etched depth of the recipe has a limit of 2 µm as depicted in Fig. 3(a), which considers the targeted SOI wafers that have a 2 µm thick BOX. To this step, we have demonstrated that a sloped trench etched into the BOX of an SOI wafer can be realized to form a 3D tapered polysilicon SSC.

To achieve a gently varied slope along the 3D SSC length, the width of the SSC was modulated by following the depth versus width relation of Fig. 3(a) as shown in Fig. 6(a). The width of the SSC is designed to increase from the tip to the large waveguide end slowly and nonlinearly. The final achieved 3D SSC in standard SOI wafers is shown in Figs. 5(a) and 5(b). In Fig. 5(a), the cross-section SEM of the taper clearly shows different sections, including the thick waveguide, 3D SSC, and top thin silicon waveguides. The top-view SEM image of Fig. 5(b) reveals the adiabatic change of the BOX trench width and top-layer waveguide profiles. The total length of the taper shown in Figs. 5(a) and 5(b) is 50 µm. The top waveguide layer [Fig. 6(a)] after etching has a width of 4 µm and 1 µm for the thick waveguide and thin waveguide, respectively, in the SSC region. Beyond the SSC, the 1 µm wide waveguide in the thin silicon layer then linearly tapers down to 450 nm.

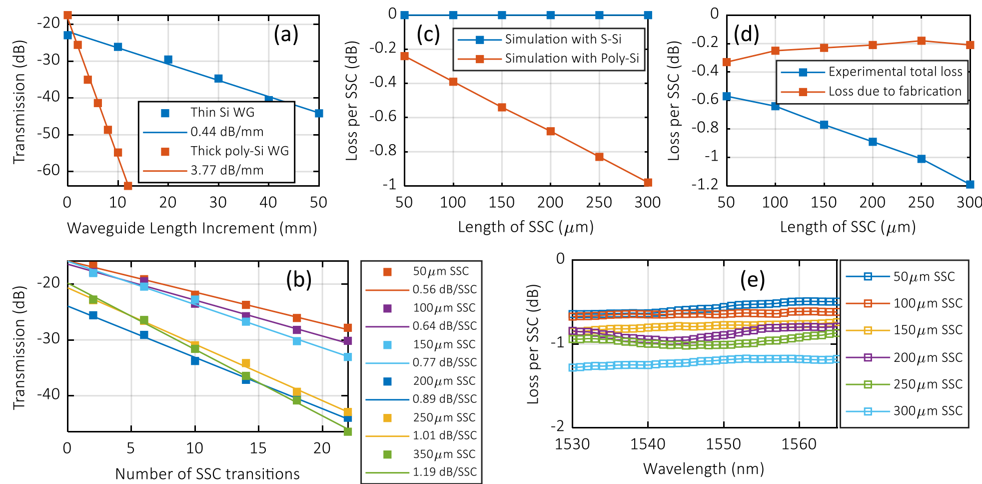

Fig. 7. (a)–(d) Loss analysis at wavelength 1550 nm. (a) Measured optical loss of the thick polysilicon waveguides (3.77 ± 0.23 dB/mm) and thin silicon overlayer waveguide (0.44 ± 0.06 dB/mm); (b) measured optical transmission losses of the SSCs with different lengths. The extracted losses per SSC are 0.56 ± 0.05, 0.64 ± 0.10, 0.77 ± 0.09, 0.89 ± 0.07, 1.01 ± 0.07, and 1.19 ± 0.08 dB for different SSC lengths 50, 100, 150, 200, 250, and 300 μm, respectively; (c) simulated transmission losses of the SSCs consisting of single-crystalline silicon (S-Si) and polysilicon. (d) Summary of the experimental total optical loss and loss due to experimental fabrications after excluding the polysilicon loss. (e) Measured C-band insertion loss per SSC.

3. RESULTS AND DISCUSSION

To quantify the optical transition loss of the fabricated SSCs at wavelengths around 1550 nm, a series of waveguides, each consisting of a different number of SSCs, were fabricated as designed in Fig. 6(a). Separately, different lengths of the thick polysilicon waveguides have also been fabricated to characterize the optical losses resulting from the polysilicon material. The optical losses are fitted by the cutback method. As shown in Fig. 7(a), the measured optical loss of the polysilicon waveguide ($\alpha_{p-\mathrm{wg}}$) is 3.77 dB/mm, and the single-mode top layer thin waveguide ($\alpha_{Si-\mathrm{wg}}$) is 0.44 dB/mm. The measured transition loss of the 3D SSC grows with length as shown in Fig. 7(b). Explicitly, the optical losses of the SSCs are measured to be 0.56, 0.64, 0.77, 0.89, 1.01, and 1.19 dB for lengths of 50, 100, 150, 200, 250, and 300 μm, respectively. The optical loss of the SSC mostly stems from the material loss of the polysilicon. A detailed influence of the polysilicon material loss is analyzed as follows.

To make a conservative estimate of the polysilicon material-induced losses (α_p), the contribution from surface roughness (α_r), which is treated to be as high as the losses of the thin silicon waveguide, is subtracted from the measured thick polysilicon waveguide loss. The optical power confinement factor for the polysilicon region (Γ_p) of the thick waveguide is calculated to be 99.79%. The polysilicon material loss is then calculated as 3.34 dB/mm by $\alpha_p = (\alpha_{p-\mathrm{wg}} - \alpha_r)/\Gamma_p$. To further analyze the polysilicon contribution to the transition loss of the SSCs, 3D FDTD simulations of the SSC were performed by considering the material used to fill the trench as polysilicon with loss 3.34 dB/mm or single-crystalline silicon (S-Si) with negligible loss. The results show the SSC optical losses are negligible for S-Si and, in contrast, are very profound for polysilicon as shown in Fig. 7(c). Therefore, the maximum optical losses due to fabrication-induced imperfections of the SSC and roughness of all sections can be estimated by deducting the polysilicon-induced material loss from the total measured loss of the SSC as shown in Fig. 7(d), which indicates losses as low as about 0.2 dB for taper lengths from 100 to 300 μm.

In the future, the 3D SSC transition loss reductions can therefore be realized by using a lower-loss infill material. Optimizing the optical properties of the polysilicon can achieve losses down to 0.92 dB/mm [45,46], which can result in a material loss of 0.05 dB for a 50 μm long SSC. Similarly, depositing single crystalline silicon by PECVD and recrystallization with a proximity single crystalline silicon seed [47,48] can reduce the loss sources from polysilicon: light absorption by sub-bandgap states in silicon grain boundaries and optical scattering by Si crystalline grains. Waveguides in an SOI platform with a 1.5 μm thick single crystalline silicon overlayer show losses less than 3 dB/cm as reported in 2005 [40], even with relatively low-quality sidewall etching. Further loss reduction can be achieved by smoothing the etched trench surfaces [38] to therefore reduce scattering losses close to the tip region of the SSC. Hence, overall loss below 0.2 dB can be expected through design and process optimization. Figure 7(e) presents the insertion loss across the entire C band with a loss variation less than ± 0.1 dB. Furthermore, the demonstrated SSC approach can also be applied to the silicon nitride photonic platform, where the deposited silicon nitride material usually has very low optical losses compared with polysilicon [38,49].

To the first concerned application toward coupling with standard cleaved optical fibers with MFD around 10 μm, the demonstrated SSC approach successfully enlarged the 220 nm SOI waveguide to approximately 1.5 μm. With this MFD, directly interfacing with a cleaved single-mode fiber would result in large coupling losses as indicated by the 3 μm × 3 μm waveguide to fiber coupling in [50]. However, it is feasible with our 3D SSC approach to expand the waveguide to 3 μm by using SOI wafers with thicker BOX layer. Microscale SOI platforms are another mature and commercialized solution for photonics applications, where standard fiber-to-chip coupling has been realized with around 1 dB and 1.2 dB losses for TE and TM polarizations, respectively [51]. In that work, buried 2D tapered SSCs have been implemented with a cross section of 13 μm × 13 μm for interfacing with fibers and performing mode conversion to small micrometer-scale waveguides [51]. By combining our buried 3D SSC with this work, low-loss coupling between submicrometer

waveguides and optical fibers is possible. With a much thicker BOX layer, or the use of localized SiO_2 infilling trenches, 3D tapers to a waveguide depth of 10 um would be possible, allowing a direct interface with optical fibers.

The second scenario is butt-coupling with III-V components, a hybrid integration approach allowing edge-coupling of III-V and SOI chip to chip and a common approach for flip-chip bonding technology. III-V semiconductor optical amplifiers (SOAs) are widely reported with integration with silicon chips to build power-efficient, tuneable, and low-linewidth external cavities lasers [52,53], for which SSCs are used for low-loss light coupling between chips. The calculated mode field diameter of the thick waveguide part of the SSC [Fig. 1(f)] is about 2.9 μm × 1.5 μm, which is close to the mode field diameter (2 μm × 1.3 μm) of the indium phosphide SOA waveguides reported in [54]. Conventional inverse taper SSCs have been used to expand the SOA mode to match the mode of a Si inverse taper waveguide with a SiON core [54]. The 3D buried SSC approach can be feasibly and purposely optimized and applied to such scenarios that allow the silicon waveguide mode to be directly matched with the SOA waveguides. As shown in [54], the MFD is sensitive to inverse tapering of the width but much less sensitive to waveguide expansion, which is in favor with our micrometer-scale 3D buried SSC for light coupling from chip to chip. The proposed buried 3D SSC can also be widely exploited for other silicon photonic applications, which will not be addressed in detailed hereafter.

4. CONCLUSION

In conclusion, a low-loss buried 3D SSC integration approach for silicon photonics has been demonstrated. Smooth gradient and width modulated trenches have been developed by performing an optimized width-dependent ICP etching recipe and filling the etched trenches with polysilicon to realize a 3D taper allowing optical transitions from large waveguides to standard thin silicon waveguides. The demonstrated total losses for the polysilicon SSC are as low as 0.56 dB. The material loss of the polysilicon has been shown to contribute significantly to the total loss with the loss contribution from experimental fabrication calculated to be just 0.2 dB. Through the use of a lower-loss infill material, together with improvements in design, fabrication losses below 0.2 dB are expected. The buried 3D SSC requires only silicon materials and leaves a flat, planar wafer surface, enabling compatibility with standard SiPh components and process steps for wafer-scale mass production. Such a SSC can be used for scalable, low-loss butt-coupling for optical fibers, III-V active components, and the development of multilayer photonics.

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Data Availability. Data underlying the results presented in this paper are available in Ref. [55].

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