# Wafer-Scale Demonstration of Low-Loss (~0.43 dB/cm), High-Bandwidth (>38 GHz), Silicon Photonics Platform Operating at the C-Band

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Abstract—The key advantage of silicon photonics comes from its potential for large scale integration, in a low-cost and scalable fashion. This has sustained the growth in the area despite disadvantages such as the lack of a monolithic light source, or the absence of a second order non-linear response  $(\chi^{(2)})$ . Thus far, the work in the field has focused on reporting individual devices from a single die, with excellent performances. Wafer-level results, an area which has not been addressed sufficiently, is a critical aspect of silicon photonics and will provide the community with information regarding scalability and variation, which will be the key differentiating advantage of silicon photonics over other photonic platforms. In this work, we report the development of a low-loss, high-bandwidth C-band silicon photonic platform on a 200 mm CMOS-compatible process line, demonstrating wafer-level performance in the process. Ultra-low waveguide propagation loss with median values as low as 0.43 dB/cm has been achieved. Silicon Mach-Zehnder and microring modulators with median bandwidth of 38.5 and 43 GHz respectively are presented. Finally, germanium waveguide-integrated photodetectors with median bandwidth of 43 GHz are reported. The results reported in this work are comparable to prior demonstrations concerning individual devices. The baseline designs on this platform presented in this work can be accessed commercially from CompoundTek.

*Index Terms*—Modulator, photodetector, photonic integrated circuits, silicon photonics, wafer-level platform, waveguide.

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#### I. INTRODUCTION

HE increasing levels of investment into the silicon photonics industry has affirmed its status as a disruptive technology. Just recently, Rockley Photonics [1] and Aeva Technologies [2] has been the subject of IPOs with market capitalization at the billion-dollar scale; silicon photonics forms the core technology of both companies. Lightmatter has raised a \$80 million series B for the early access program to their photonic AI accelerator [3]. Cisco has further emphasized its commitment to silicon photonics in the optical communication space via the acquisition of Acacia Communications [4]. On the academic front, new frontiers are being discovered. Instances, include topological photonics [5]–[6], quantum key distribution [7], quantum information processing [8] and programmable photonic circuits [9]–[10]. It appears that the silicon photonic platform will play an ever-growing role in the field of integrated optics in context of the vibrant cyclical growth between novel pioneering applications and subsequent attempts at commercialization.

Similar to the case of electronic integrated circuits, it is important to know that silicon photonics will likely, not have a performance edge over discrete devices based on other material platforms with a few exceptions [11]. However, the opportunity to implement large number of components in a photonic circuit in a scalable, reproducible, and potentially low-cost fashion has been the impetus behind the growth in the area. Key to the advantages mentioned has been the fact that silicon photonic chips can be manufactured by repurposing manufacturing technologies in older CMOS nodes. Nonetheless, there are distinctions in the manufacturing process of silicon photonics circuits and their electrical counterparts. An example would be the inherent difference in the topology, layout-wise, of the two. There is a fundamental difference between the curvilinear designs of photonic devices and rectilinear designs of CMOS devices [12]. Furthermore, digital IC manufacturing, traditionally, optimizes critical dimension (line/space metrology) with less regard for line edge roughness metrics. Photonic circuits with periodic acute discontinuities will impact waveguide propagation loss and device functionality [13]. Translation of existing CMOS process for the fabrication of silicon photonic circuits is not trivial. However, the above is important as it will lead to the realization of a silicon photonic platform that has low-loss, high

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Fig. 1. 3-D schematic of (a) strip waveguides, (b) rib waveguides, (c) depletion-mode microring modulators, (d) depletion mode Mach-Zehnder modulators (travelling wave on one Mach-Zehnder arm is removed for illustration, (e) germanium waveguide integrated photodetectors (metal contact on one side is removed for illustration). The parameters of the devices are annotated. The metal layers are simplified for illustration.

bandwidth and can be reproducible on a wafer-scale in a scalable fashion.

As of now, most published work has focused on the demonstration of individual devices that demonstrates high performance. However, there has been little data that report the scalability and variability of silicon photonic devices. The above metrics will be important [11] as silicon photonics moves from device to circuit level demonstration to realize advanced functionalities such as optical-phased arrays [14], optical neural nets [15] and programmable photonics [9], [16]. Such systems have large footprints and are comprised of fundamental silicon photonics structures (i.e., strip waveguide, Mach-Zehnder interferometer, microring resonator, MMI) that will have better repeatability and yield over a large chip area in comparison to complex devices. Due to the size of these circuits ( $\sim$  few cm<sup>2</sup>), it is also imperative that the propagation loss of silicon waveguides is kept low to reduce power consumption. Furthermore, as silicon photonics encroaches into the commercial-space, performance, repeatability, and scalability will directly affect the bottom line of silicon photonic companies, thereby determining the long-term viability of the technology.

In the silicon photonics ecosystem, there consists of academic research groups, integrated device manufacturers, fabless companies as well as open-access foundries [17]. Due to the high upfront investment for CMOS manufacturing infrastructure, most silicon photonic design groups have relied on open-access foundries for the fabrication of their chips. This has initiated a series of open-access foundries such as AIM Photonics [18], AMF [19], CORNERSTONE [20], CEA-LETI [21], CompoundTek, VTT [22] and LIGENTEC [23]. A more comprehensive list of open-access foundries can be found in [17], [24]. The current manufacturing environment offers the silicon photonic designer a wide range of platforms (i.e., thin-SOI, thick-SOI, silicon nitride), subject to different lead times and capacities.

Currently, the 220 nm SOI platform is the most widely used [25]-[31]. The adoption of the platform was initially attributed to the 220 nm SOI supporting exactly one guided slab mode for both TE and TM polarization about the C-band [17]. This work reports the 200 mm wafer-level demonstration of a low-loss, high-performance active and passive silicon photonics platform, operating at the C-band. Three different baseline waveguide dimensions are fabricated (strip (Fig. 1(a)) and rib waveguides (Fig. 1(b)), and propagation loss values measured. Median loss as low as 0.43 dB/cm and 0.65 dB/cm are measured for rib and strip waveguides, respectively. Following, baseline design silicon depletion-mode microring (Fig. 1(c)) and Mach-Zehnder modulators (Fig. 1(d)) of this platform are measured for waferlevel efficiency and bandwidth. Mach-Zehnder/microring modulator median efficiency and bandwidth of 1.6/1.8 V.cm and 38.5/43 GHz are obtained. Wafer-level characterization of germanium waveguide integrated photodetectors (Fig. 1(e)) (baseline design) are also performed, where the median bandwidth is found to be 43 GHz. The technology stack of the silicon photonic platform is shown in Fig. 2(a) (not drawn to scale). The wafer-level passive and active characteristics reported in this work compares favorably with existing silicon photonic platforms and will be useful in the realization and subsequent commercialization of large-scale photonic integration. The baseline waveguide, modulator and photodetector designs on this silicon photonic platform presented in this work will be commercially accessible. In Fig. 2(b)-(e), some SEM images of the platform are shown.

# II. PROCESS OVERVIEW

The silicon photonic platform is fabricated in a commercial CMOS process line (CompoundTek). A 200 mm SOITEC SOI was used, with a Boron-doped silicon device layer of



Fig. 2. (a) Device cross-section relating to the strip and rib waveguides, depletion-mode microring and Mach-Zehnder modulators, germanium waveguide integrated photodetectors. SEM images of (b) strip waveguide (W = 500 nm), (c) strip waveguide (W = 450 nm) transition to rib waveguide (W = 450 nm), (d) microring resonator composed of strip waveguide (W = 500 nm), (e) C-band focusing grating coupler.

220 nm-thick and resistivity of 10  $\Omega$ .cm. The buried oxide (BOX) is 3  $\mu$ m thick, to prevent the leakage of optical mode into the silicon substrate [32]. The silicon substrate has a high resistivity of 750  $\Omega$ .cm to minimize parasitic surface conduction that is present in an oxidized silicon substrate [33]. Thereby, good RF performance can be achieved. Waveguide patterning for etching depths of 70, 130 and 220 nm are enabled with 193 nm Argon Fluoride (ArF) immersion lithography and optical proximity correction; the 193 nm ArF immersion lithography technology has a minimum single-exposure size of about 40 nm but is hardmask-limited. The 70 nm etch is critical for devices such as I/O grating couplers [34] or breaking the symmetry of a waveguide mode for polarization rotation [35]. The 130 nm partial etch is mainly used in the phase-shifter sections of optical modulators, where a trade-off between doping-induced loss and contact resistance can be achieved. The silicon full-etch (220 nm) enables optical isolation between optical components. The waveguides are defined with Inductively Coupled Plasma-Reactive Ion Etching process. Prior to cladding encapsulation, the hydrogen annealing process was utilized. During the annealing process, the mobility of the silicon atoms at the waveguide surface increases, resulting in the migration of Si atoms to smoothen waveguide sidewall roughness through the reduction of surface energy [36]; scattering due to sidewall roughness is the most significant contributor to waveguide propagation loss. Via the application of the abovementioned immersion lithography,

resist, etching and annealing systems, low waveguide loss has been demonstrated in this work as a result of lower line-edge roughness [37]. The ion implantation steps are implemented before and after the definition of the waveguides. The contact areas of the PN-junction are heavily doped (ohmic) to reduce contact resistance, and the core of the waveguide is subject to low doping concentrations ( $\sim 5 \times 10^{17} \text{ cm}^3$ ) to prevent significant optical loss due to carrier absorption. The germanium waveguide integrated photodetectors are realized via a two-step epitaxial growth of germanium. Upon the growth step, implantation steps are carried out to form the P-I-N diode. Rapid thermal annealing is used for carrier activation. After the silicidation of Si/Ge, a backend of line (BEOL) process is used to contact the silicide, two metal layers with one via layer in between. The two metal layers and one via layer are also used to contact the TiN, for thermo-optic tuning. Following, passivation is conducted, and contact pads are implemented after. Inline wafer-level testing (optical and electrical) during the fabrication process is utilized to monitor the processing wafers.

# **III. WAFER-LEVEL TESTING**

The 200/300 mm wafer-level testing solution used a CompoundTek customized solution with hardware and in-house proprietary software with AI and big data analytics [38]. The system includes the FormFactor CM300xi-SiPh prober, with 6628609



Fig. 3. Cross-sectional electric-field distribution of strip waveguide (a) W = 450 nm, (b) W = 500 nm, (c) rib waveguide, W = 450 nm.

automated wafer-level positioning which can achieve a twosided optical-to-optical (O-O) setup with alignment resolution and time of lower than 300 nm and 3 seconds respectively [39]. The KeySight N4373E, 67 GHz lightwave component analyzer was utilized for device bandwidth characterization.

## **IV. LOW-LOSS SILICON WAVEGUIDES**

Silicon strip waveguides with width (W) of 450, 500 nm, and silicon rib waveguide with width of 450 nm are fabricated; only the fundamental mode is supported according to eigenmode analysis. The cross-sectional electric-field distribution of strip waveguides (W = 450, 500 nm), rib waveguides (W = 450) are indicated in Fig. 3(a)–(c) respectively.

To determine waveguide propagation loss, spiral waveguides with lengths of 0.54, 1.14, 2.34, 3.54 cm are fabricated, and the transmission measured. Grating couplers are used for I/O, with cleaved SMF-28 fibers. The grating couplers has a period, duty cycle and etch depth of 630 nm, 0.5 and 70 nm respectively. The grating couplers on the wafer has a mean and median insertion loss of 4.31 dB and 4.29 dB respectively, with a standard deviation of 0.13 dB. The power meter in the testing system has an uncertainty of smaller than 0.05 dB. The bending radius used is 15  $\mu$ m to prevent bending losses. Via the linear regression of the transmission of each waveguide length with fixed cross-sectional dimension, the propagation loss can be determined. Fig. 4(a) and (c) shows an example for strip/rib waveguide (W = 500/450 nm) in a single die, illustrating the transmission measured for each of the four spiral waveguides. As the envelope of the grating coupler spectrum is a parabola, a poly-fit was used. A linear regression is then taken from the peak of the four transmission curve fits and the waveguide propagation loss is indicated in Fig. 4(b) and (d). The wafer-level test results for the strip waveguides (W =450, 500 nm) and rib waveguides (W = 450 nm) are indicated in Fig. 4(e)–(g). The mean, median and standard deviation of each waveguide dimension is shown in Table I. By comparing both the rib and strip waveguides with W = 450 nm, it is found that the losses from the rib waveguide is lower than the strip waveguide. This is due to the relatively lower sidewall scattering in the rib waveguide. On the other hand, the strip waveguide with W = 500 nm demonstrates the lower waveguide propagation loss in comparison to the strip waveguide with W = 450 nm. This is attributed to the stronger confinement of the optical mode in the wider waveguide. The propagation loss result of the rib waveguide with W = 450 nm represents the lowest on the

TABLE I Waveguide Propagation Loss Median, Mean, and Standard Deviation Values of Rib Waveguide (W = 450 nm), Strip Waveguides (W = 450, 500 nm)

Waveguide	Median Loss	Mean Loss	Standard
width, W (nm)	(dB/cm)	(dB/cm)	Deviation
			(dB/cm)
450, rib	0.43	0.48	0.19
450, strip	0.78	0.81	0.19
500, strip	0.65	0.65	0.19

platform. Furthermore, both strip waveguides also demonstrate low propagation loss. The waveguides developed in this platform will be critical as the extent of photonic integration increases [14]–[15], even moving beyond the single reticle limit [40].

## V. SILICON MODULATORS

# A. Silicon Mach-Zehnder Modulators

The Mach-Zehnder configuration is the most implemented architecture amongst optical modulators [41]-[43]. The Mach-Zehnder modulator is an interferometric device that modulates the intensity of light. The input lightwave is split into two via a MMI into two Mach-Zehnder arms and combined into a MMI at the end. Phase shifters are implemented on one or both arms to enable a phase difference between the two optical paths leading to constructive/destructive interference. This gives rise to intensity modulation. The depletion-mode Mach-Zehnder interferometer presented in this work is asymmetrical with a length difference of 45  $\mu$ m, corresponding to a FSR of 5.69 nm. The 3-D schematic of Mach-Zehnder modulator is illustrated in Fig. 1(c), with critical device parameters annotated. The dimensions of the rib waveguide width and slab thickness are 0.41  $\mu$ m and 90 nm, respectively. Two levels of n and p-type doping was realized about the center of the Si rib waveguide (45 nm offset) in a P-I-N doping configuration, where the width of the intrinsic region is 30 nm; doping configuration from left to right, as indicated by the P-I-N-junction illustrated in the inset of Fig. 1(c) are p++, p+, p, intrinsic, n, n+ and n++ respectively. In order to avoid carrier absorption by the heavily-doped regions, the p+ and n+doped regions are placed 0.505  $\mu$ m away from the center of the rib waveguide, and the p++ and n++ are implemented 0.3  $\mu$ m from the edge of the p+ and n+ regions respectively; overlap analysis via eigenmode calculations indicates that all the optical energy are contained within the p and n-doped regions. For the Mach-Zehnder modulator presented in this work (Fig. 5(a)), the length of the phase shifter regions is 2 mm (L = 2 mm). The phase shifters are implemented through a lateral P-I-N junction with coplanar metal strips. The transmission line electrodes are designed to such that the effective index of the optical and wave and microwave are matched (neff. $_{Optical} = neff._{Microwave}$ ). This would enable synchronization between the optical wave and microwave, thereby, increasing the extent of interaction between the two, and reducing RF loss along the electrodes. When a bias voltage (V<sub>bias</sub>) is applied to a phase shifter, the depletion region widens, and this results in an increment of the effective refractive index of the optical mode travelling in one of the Mach-Zehnder



Fig. 4. (a) The measured transmission of the four spiral waveguides with lengths of 0.54, 1.14, 2.34, 3.54 cm in a die; the strip waveguides measured has a width of 500 nm. (b) Propagation loss determined from Fig. 4(a) in a die. (c) The measured transmission of the four spiral waveguides with lengths of 0.54, 1.14, 2.34, 3.54 cm in a die; the rib waveguides measured has a width of 450 nm. (d) Propagation loss determined from Fig. 4(c) in a die. Wafer-level measurement results of (e) strip waveguides (W = 450 nm), (f) strip waveguides (W = 500 nm), (g) rib waveguides (W = 450 nm).



Fig. 5. (a) Micrograph images of the silicon Mach-Zehnder modulator. (b) Transmission spectra when  $V_{bias} = 0, 1, 2, 3, 4 V$  in a die. (c) Electro-optic response of the device highlighted in Fig. 5(b) when  $V_{bias} = 4 V$ . Wafer-level measurement of (d) bandwidth, (e) modulation efficiency when  $V_{bias} = 4V$ .

TABLE II BANDWIDTH AND MODULATION EFFICIENCY MEDIAN, MEAN, AND STANDARD DEVIATION VALUES OF THE SILICON MACH-ZEHNDER MODULATOR WHEN  $V_{\rm BIAS}=4\rm V$ 

	Median	Mean	Standard Deviation
Bandwidth (GHz)	38.50	37.10	4.70
Modulation Efficiency,	1.60	1.59	0.06
$V_{\pi}$ L (V.cm)			

arms. This causes a red shift at the output transmission spectrum of the Mach-Zehnder modulator. In Fig. 5(b), we show such an example from a die in the wafer, where the  $V_{bias} = 0$ , 1, 2, 3, 4 V. The Mach-Zehnder modulator has a median and mean insertion loss of 2.94 dB and 3.18 dB respectively, with a standard deviation of 0.33 dB, considering wafer-scale results. The electro-optic response (S<sub>21</sub>) of the device highlighted in Fig. 5(c), where the bandwidth is indicated to be 42 GHz in Fig. 5(c) when  $V_{bias} = 4$  V. The wafer map bandwidth and efficiency ( $V_{\pi}L_{\pi} = V_{bias}L_{\pi}/\Delta\varphi$ ,  $\Delta\varphi$  is the phase change) of the modulators are illustrated in Fig. 5(d) and (e) respectively at  $V_{bias} = 4$  V. The mean and median values in terms of bandwidth and modulation efficiency when  $V_{bias} = 4$  V are indicated in Table II.

## B. Silicon Microring Modulators

The silicon material has a weak refractive index dependence regarding hole and electron concentrations. As such, this has resulted in the Mach-Zehnder modulators requiring a long device length such that a  $\pi$  phase shift can be implemented, under lower V<sub>bias</sub> and swing (V<sub>pp</sub>). In 2004, Xu et al. overcame the abovementioned footprint issue by exploiting the resonant property of the microring resonator [44]. The effective optical path length is extended when the microring circumference corresponds to integer multiples of wavelength. As such, through this implementation, the effective index change brought about by varying V<sub>bias</sub> will result in a significant shift of the microring modulator resonance giving rise to the basis for intensity modulation. The 3-D schematic of the microring modulator is shown in Fig. 1(d), with key device parameters indicated. For the depletion-mode microring modulators presented in this work, the width of the rib waveguide is 450 nm. The radius is 10  $\mu$ m, corresponding to a FSR of 9.69 nm; the microring radius and correspondingly, FSR can be designed according to the channel spacing in wavelength division multiplexing schemes. The phase shifter is implemented through a P-N junction, where n and p-type doping were realized at the centre of the Si rib waveguide (0 nm offset); doping configuration from left to right, as indicated by the P-N-junction illustrated in the inset of Fig. 1(d) are p++, p+, p, intrinsic, n, n+ and n++ cm<sup>3</sup> respectively. The distance from the edge of the rib waveguide to the p+/n+ and p++/n++ doping regions are 0.3 and 0.7  $\mu$ m respectively to prevent carrier absorption. The phase shifter length corresponds to 33.3% of the microring modulator circumference. The micrograph image of the microring modulator is shown in Fig. 6(a). Similarly, to the Mach-Zehnder modulator, the microring

TABLE III BANDWIDTH AND MODULATION EFFICIENCY MEDIAN, MEAN, AND STANDARD DEVIATION VALUES OF THE SILICON MICRORING MODULATOR WHEN  $V_{\rm BIAS}$  = 4 V

	Median	Mean	Standard Deviation
Bandwidth (GHz)	43.00	44.00	4.50
Modulation Efficiency, $V_{\pi}$ L (V.cm)	1.85	1.80	0.13

modulator is based on the plasma dispersion effect (depletion mode). In Fig. 6(b), an example is shown where the microring resonance redshifts as V<sub>bias</sub> increases from 0 to 4 V; the die is obtained from the wafer presented in this work. As the microring modulator is implemented in an add-drop configuration, it will always operate in the under-coupled state, where coupling between the bus waveguide and the microring resonator is larger than the round-trip microring loss. As it can be seen in Fig. 6(b), the extinction ratio of the microring resonance decreases with increasing V<sub>bias</sub>. The electro-optic response of the device highlighted in Fig. 6(b) is illustrated in Fig. 6(c), where the bandwidth if measured to be 46 GHz when  $V_{\rm bias}$ = 4 V. The wafer level results in terms of bandwidth and modulation efficiency ( $V_{\pi}L_{\pi} = 1/2 \times [L_{\pi} \times FSR]/[\partial \lambda/\partial V], L_{\pi}$ corresponds to length percentage of microring circumference) are indicated in Fig. 6(d) and (e), respectively. The median and mean values of bandwidth and modulation efficiency when  $V_{\rm bias} = 4$  V are summarized in Table III. With regards to microring modulators, thermo-optic heaters can be implemented to compensate for variations in microring resonances caused by fabrication variations or environmental thermal fluctuations. However, for the microring modulator presented in Fig. 6(a)–(e), thermo-optic heaters were not implemented. Nevertheless, based on the technology stack of the platform shown in Fig. 2(a), thermo-optic heaters can be implemented on the microring modulators. During the development of this photonic platform, Mach-Zehnder and microring modulators with different design parameters (i.e., relative doping offset) were fabricated. The selection of the two modulator designs in this work was based empirically on performance.

Silicon-based modulators, based on carrier-depletion mechanism has been one of the promising technologies in the communication space [45]–[46]. The ability for high-yield, low-cost manufacturing has stimulated the interest of silicon-based modulators in industry. The wafer-level results of the modulators reported in this work, justifies the interest of the technology. The Mach-Zehnder modulators indicates a median bandwidth of 38.5 GHz. It is of note that one could make further improvement to the baseline design presented in this platform by optimizing three aspects: travelling wave electrode impedance matching, reduction of microwave attenuation, micro and lightwave velocity matching. Approaches to attain the above, while not exhaustive, are substrate removal at the phase shifters [47], reduction of active region series resistance [48] as well as application of copper electrodes [49]. The silicon microring modulators presented



Fig. 6. (a) Micrograph images of the silicon microring modulator. (b) Transmission spectra when  $V_{bias} = 0, 1, 2, 3, 4 V$  in a die. (c) Electro-optic response of the device highlighted in Fig. 6(b) when  $V_{bias} = 4 V$ . Wafer-level measurement of (d) bandwidth, (e) modulation efficiency when  $V_{bias} = 4 V$ .

in this work displays a median bandwidth and modulation efficiency of 43 GHz and 1.85 V.cm respectively. It is of note that the results presented for the baseline Mach-Zehnder and microring modulators are comparable to the results reported in literature. In order to improve modulator performance, the shape of the PN-junction that constitutes the phase shifter could be modified. Examples include the wrapped-around [50], interleaved [51] and L-shaped [52] PN-junction. It is, however, important to note that such modified P-N junctions requires additional process steps, adding to fabrication complexity. As a result, device yields could potentially be adversely affected.

### VI. GERMANIUM WAVEGUIDE INTEGRATED PHOTODETECTOR

The silicon material has an indirect bandgap of 1.12 eV. As such, this would imply that Si-based photodetection would be challenging at O- and C-bands. Germanium, on the other hand, has a quasi-direct bandgap of 0.8 eV which corresponds to the C-band. In order to overcome the 4.3% lattice mismatch between silicon and germanium, a two-step epitaxial process is used. The first step requires the growth of a thin layer of germanium under low temperatures such that the strain between silicon and germanium is reduced, and the dislocations are confined within the Si/Ge interface. Following, a thicker germanium layer would be grown under high temperature conditions, thereby achieving superior, tensile-strained germanium films. Tensile strain reduces the bandgap of the germanium, resulting in enhanced

TABLE IV BANDWIDTH MEDIAN, MEAN AND STANDARD DEVIATION VALUES OF THE GERMANIUM WAVEGUIDE INTEGRATED PHOTODETECTOR WHEN  $\rm V_{BIAS}=3~V$ 

	Median Loss	Mean	Standard Deviation
Bandwidth (GHz)	43.00	42.60	1.20

absorptive properties at the C-band. Germanium photodetectors on silicon can be broadly classified into vertical incidence or waveguide integrated photodetectors. Vertical-coupled photodetectors generally requires thick germanium layers for photoabsorption. This results in increased capacitance and dark currents and reduced responsivity-bandwidth product. The abovementioned problems can be alleviated with the waveguide integrated photodetectors. Through waveguide integration, the germanium photoabsorption section is in the plane of light propagation in a silicon photonic circuit [53]–[54]. In this section, the wafer-level performance regarding the baseline design waveguide integrated photodetector in this platform is presented.

The germanium waveguide integrated photodetector is realized using the vertical P-I-N junction for photocurrent collection; key device parameters are indicated in the 3-D schematic at Fig. 1(d). This implementation imposes less complexity on fabrication. The lightwave is evanescently coupled into from silicon to the germanium device layer for photo absorption. The



Fig. 7. (a) Micrograph images of the germanium waveguide integrated photodetector. (b) Electro-optic response of a photodetector on a single die; the bandwidth is indicated when  $V_{\rm bias} = 3$  V. (c) Wafer-level measurement of photodetector bandwidth when  $V_{\rm bias} = 3$  V.

width, length and thickness of the germanium layer are 4, 10  $\mu$ m and 500 nm respectively; the rest of the device dimensions are indicated in Fig. 1(e). The micrograph image of the photodetector is shown in Fig. 7(a). In Fig. 7(b), the electro-optic response of a photodetector at  $V_{\rm bias} = 3$  V in a die is illustrated as an example; the bandwidth is characterized to be 43 GHz. The wafer-level results of the photodetector in terms of bandwidth when  $V_{\text{bias}} = 3 \text{ V}$  are illustrated in Fig. 7(c). The median and mean results in terms of bandwidth when  $V_{\rm bias} = 3$  V is shown in Table IV. The median and mean bandwidth when  $V_{\text{bias}} = 2 \text{ V}$ is 41.21 and 41.79 GHz respectively with a standard deviation of 0.05 GHz. When  $V_{\rm bias} = 1$  V, the median and mean bandwidth is 38.79 and 39.01 GHz respectively with a standard deviation of 0.05 GHz. At Vbias = 3V, the wafer-level responsivity of the photodetector has a median and mean value of 0.835 A/W and 0.837 A/W, respectively, with a standard deviation of 0.05 A/W. The wafer-level dark current of the photodetector has a median and mean value of 2.58 nA and 2.79 nA respectively, with a standard deviation of 0.86 nA.

# VII. CONCLUSION

Silicon photonics stands out from other photonic platform due to its potential for large scale integration and be manufactured with low-cost and variability. This is in spite of the fact that silicon photonics will not have a performance edge, discrete device-wise, over other photonic platform. Unlike most work in silicon photonics, which has analysed devices on the individual-level, this paper addresses the issue on scalability and variability on a wafer-level. The silicon photonics platform developed operates at the C-band. Ultra-low loss silicon strip and rib waveguides are developed. Median waveguide propagation loss as low as 0.43 dB/cm is achieved. Silicon Mach-Zehnder and microring modulators with median bandwidth of 38.5 and 43 GHz respectively are presented. In addition, the germanium waveguide-integrated photodetector is demonstrated to have a median bandwidth of 43 GHz. The platform described in this work will be useful as silicon photonics moves towards the exploration of more complex functionalities, as well as commercialization.

#### REFERENCES

- "Chips supplier rockley photonics to go public in \$1.2 billion spac deal," *Reuters*, Mar. 19, 2021. [Online]. Available: https://www.reuters.com/ article/us-rockley-photonics-m-a-sc-health-corp-idUSKBN2BB1A9
- [2] K. Korosec, "Lidar startup aeva to go public via \$2.1 billion spac merger," *TechCrunch*, Nov. 2, 2020. [Online]. Available: https://techcrunch.com/2020/11/02/lidar-startup-aeva-to-go-publicvia-2-1-billion-spac-merger/
- [3] "Lightmatter raises \$80m series b and brings photonic compute chip to market that accelerates AI with 10x-plus speed and energy advantage," Bus. Wire, May 6, 2021. [Online]. Available: https: //www.businesswire.com/news/home/20210506005271/en/Lightmatter-Raises-80M-Series-B-and-Brings-Photonic-Compute-Chip-to-Market-That-Accelerates-AI-With-10x-Plus-Speed-and-Energy-Advantage
- [4] "Cisco completes acquisition of acacia communications, inc.," Cisco, Mar. 1, 2021. [Online]. Available: https://www.cisco.com/c/en/us/about/ corporate-strategy-office/acquisitions/acacia.html
- [5] Y. Chen et al., "Topologically protected valley-dependent quantum photonic circuits," Phys. Rev. Lett., vol. 126, 2021, Art. no. 230503.
- [6] N. Parappurath, F. Alpeggiani, L. Kuipers, and E. Verhagen, "Direct observation of topological edge states in silicon photonic crystals: Spin, dispersion, and chiral routing," *Sci. Adv.*, vol. 6, no. 10, 2020, Art. no. eaaw4137.
- [7] G. Zhang *et al.*, "An integrated silicon photonic chip platform for continuous-variable quantum key distribution," *Nature Photon.*, vol. 13, pp. 839–842, 2019.
- [8] X. Qiang *et al.*, "Large-scale silicon photonics implementing arbitrary two-qubit processing," *Nature Photon.*, vol. 12, pp. 534–539, 2018.
- [9] W. Bogaerts *et al.*, "Programmable photonic circuits," *Nature*, vol. 586, pp. 207–216, 2020.

- [10] X. Chen *et al.*, "Silicon erasable waveguides and directional couplers by germanium ion implantation for configurable photonics circuits," *Opt. Exp.*, vol. 28, no. 12, pp. 17630–17642, 2020.
- [11] T. Baehr-Jones, T. Pinguet, P. L. Guo-qiang, S. Danziger, D. Prather, and M. Hochberg, "Myths and rumors of silicon photonics," *Nature Photon.*, vol. 6, pp. 206–208, 2012.
- [12] C. Meagher *et al.*, "Patterning challenges for monolithic silicon photonics: AP/DFM: Advanced patterning /design for manufacturability," in *Proc.* 29th Annu. SEMI Adv. Semicond. Manuf. Conf., 2018, pp. 155–158.
- [13] K. H. Nakagawa and N. Fahrenkopf, "Translating IC-centric photomask manufacturing to photonics-centric applications: Linking photomask process to photonics waveguide performance," *Proc. SPIE*, vol. 11518, 2020, Art. no. 115180S.
- [14] J. Sun, E. Timurdogan, A. Yaacobi, E. S. Hosseini, and M. R. Watts, "Large-scale nanophotonic phased array," *Nature*, vol. 493, pp. 195–199, 2013.
- [15] Y. Shen *et al.*, "Deep learning with coherent nanophotonic circuits," *Nature Photon.*, vol. 11, pp. 441–446, 2017.
- [16] W. Bogaerts and A. Rahim, "Programmable photonics: An opportunity for an accessible large-volume PIC ecosystem," *IEEE J. Sel. Topics Quantum Electron.*, vol. 26, no. 5, Sep./Oct. 2020, Art. no. 8302517.
- [17] A. Rahim, T. Spusens, R. Baets, and W. Bogaerts, "Open-access silicon photonics: Current status and emerging initiatives," in *Proc. IEEE*, vol. 106, no. 12, pp. 2313–2330, Dec. 2018.
- [18] A. 29, A. 20, A. 14, and M. 29, "Aim photonics," AIM Photon. [Online]. Available: https://www.aimphotonics.com/
- [19] S. Y. Siew *et al.*, "Review of silicon photonics technology and platform development," *J. Lightw. Technol.*, vol. 39, no. 13, pp. 4374–4389, 2021.
- [20] C. G. Littlejohns *et al.*, "CORNERSTONE's silicon photonics rapid prototyping platforoms: Current status and future outlook," *Appl. Sci.*, vol. 10, 2020, Art. no. 8201.
- [21] Q. Wilmart *et al.*, "A complete Si photoncis platform embedding ultra-low loss waveguides for O- and C-band," *J. Lightw. Technol.*, vol. 39, no. 2, pp. 532–538, 2021.
- [22] "Silicon photonics," VTT. [Online]. Available: https://www.vttresearch. com/en/ourservices/silicon-photonics
- [23] "Home," LIGENTEC, Nov. 2, 2021. [Online]. Available: https://www. ligentec.com/
- [24] A. Rahim et al., "Open-access silicon photonics platform in Europe," IEEE J. Sel. Topics Quantum Electron., vol. 25, no. 5, Sep./Oct. 2019, Art. no. 8200818.
- [25] J. X. B. Sia *et al.*, "Compact silicon photonic hybrid ring external cavity (SHREC)/InGaSb-AlGaAsSb wavelength-tunable laser diode operating from 1881-1947 nm," *Opt. Exp.*, vol. 28, no. 4, pp. 5134–5146, 2020.
- [26] J. X. B. Sia *et al.*, "Sub-kHz linewidth, hybrid III-V/silicon wavelengthtunable laser diode operating at the application-rich 1647-1690 nm," *Opt. Exp.*, vol. 28, no. 17, pp. 25215–25224, 2020.
- [27] J. X. B. Sia *et al.*, "1 × N (N = 2, 8) silicon selector switch for prospective technologies at the 2 μm waveband," *IEEE Photon. Technol. Lett.*, vol. 32, no. 18, pp. 1127–1130, Sep. 2020.
- [28] H. Xu, D. Dai, and Y. Shi, "Low-crosstalk and fabrication tolerant fourchannel CWDM filter based on dispersion-engineered Mach-Zehnder interferometers," *Opt. Exp.*, vol. 29, no. 13, pp. 20617–20631, 2021.
- [29] W. Shen, J. Du, K. Xu, and Z. He, "On-chip selective dual-mode switch for 2-μm wavelength high-speed optical interconnection," *IEEE Photon. Technol. Lett.*, vol. 33, no. 10, pp. 483–486, May 2021.
- [30] X. Luo et al., "Silicon high-order coupled-microring-based electro-optical switches for on-chip optical interconnects," *IEEE Photon. Technol. Lett.*, vol. 24, no. 10, pp. 821–823, May 2012.
- [31] X. Li *et al.*, "Phase noise reduction of a 2 μm passively mode-locked laser through hybrid III-V/silicon integration," *Optica*, vol. 8, no. 6, pp. 855–860, 2021.
- [32] P. Chiang and T. Shih, "Analysis of leakage loss in silicon photonics with finite gain compression," *IEEE Photon. J.*, vol. 9, no. 5, 2017, Art. no. 1505310.

- [33] D. Lederer, C. Desrumeaux, F. Brunier, and J. -P. Raskin, "High resistivity SOI substrates: How high should we go?," in *Proc. IEEE Int. Conf. SOI*, Newport Beach, CA, USA, 2003, pp. 50–51.
- [34] R. Msrchetti, C. Lacava, L. Carroll, K. Gradkowski, and P. Minzioni, "Coupling strategies for silicon photonics integrated chips," *Photon. Res*, vol. 7, no. 2, pp. 201–239, 2019.
- [35] M. Asmer *et al.*, "CMOS compatible Silicon-on-Insulator polarization rotator based on symmetry breaking of the waveguide cross section," *IEEE Photon. Technol. Lett.*, vol. 24, no. 22, pp. 2031–2034, Nov. 2012.
- [36] F. P. Payne and J. P. R. Lacey, "A theoretical analysis of scattering loss from planar optical waveguides," *Opt. Quantum Electron.*, vol. 26, pp. 977–986, 1994.
- [37] K. Giewont *et al.*, "300-mm Monolithic silicon photonics foundry technology," *IEEE J. Sel. Topics Quantum Electron.*, vol. 25, no. 5, Sep./Oct. 2019, Art. no. 8200611.
- [38] P. M. editors, "Keysight, FormFactor, and Compoundtek join forces," *Pho-tonics Media*, Feb. 2, 2021. [Online]. Available: https://www.photonics.com/Articles/Keysight\_FormFactor\_and\_CompoundTek\_Join\_Forces/a65316
- [39] "Silicon Photonics: Automated Wafer-level probing meets silicon photonics." [Online]. Available: https://www.laserfocusworld.com/optics/ optics-design/article/16556357/silicon-photonics-automated-waferlevelprobing-meets-silicon-photonics
- [40] W. Jin, A. Feshali, M. Paniccia, and J. E. Bowers, "Seamless multi-reticle photonics," Opt. Lett., vol. 46, no. 12, pp. 2984–2987, 2021.
- [41] X. Tu et al., "50-Gb/s silicon optical modulator travelling-wave electrodes," Opt. Exp., vol. 21, no. 10, pp. 12776–12782, 2013.
- [42] D. J. Thomson *et al.*, "High contrast 40 Gbit/s optical modulation in silicon," *Opt. Exp.*, vol. 19, no. 12, pp. 11507–11516, 2011.
- [43] A. Samani et al., "Silicon photonic Mach-Zehnder modulator architectures for on chip PAM-4 signal generation," J. Lightw. Technol., vol. 37, no. 13, pp. 2989–2999, 2019.
- [44] Q. Xu, B. Schmidt, S. Pradhan, and M. Lipson, "Micrometre-scale silicon modulator," *Nature*, vol. 435, pp. 325–327, 2005.
- [45] A. Rahim *et al.*, "Taking silicon photonics modulators to a higher performance level: State-of-art and a review of new technologies," *Adv. Photon.*, vol. 3, no. 2, 2021, Art. no. 024003.
- [46] G. T. Reed *et al.*, "Recent breakthroughs in carrier depletion based silicon optical modulators," *Nanophotonics*, vol. 3, no. 4-5, pp. 229–245, 2014.
- [47] X. Xiao, M. Li, Z. Li, L. Wang, and S. Yu, "Substrate removed silicon Mach-Zehnder modulator for high baud rate optical intensity modulations," in *Proc.Opt. Fiber Commun. Conf.*, 2016, Paper Th4H.5.
- [48] M. Lu, L. Wang, X. Li, X. Xiao, and S. Yu, "Silicon intensity Mach-Zehnder modulator for single lane 100 Gb/s applications," *Photon. Res.*, vol. 6, no. 2, pp. 109–116, 2018.
- [49] Y. Yang, Q. Fang, M. Yu, X. Tu, R. Rusli, and G. Lo, "High-efficiency Si optical modulator using Cu travelling-wave electrode," *Opt. Exp.*, vol. 22, no. 24, pp. 29978–29985, 2014.
- [50] D. J. Thomson *et al.*, "High performance Mach-Zehnder based silicon optical modulator," *IEEE J. Sel. Topics Quantum Electron.*, vol. 19, no. 6, Nov./Dec. 2013, Art. no. 3400510.
- [51] H. Xu et al., "High speed silicon Mach-Zehnder modulator based on interleaved PN junction," Opt. Exp., vol. 20, no. 14, pp. 15093–15099, 2012.
- [52] J. Sun, R. Kumar, M. Sakib, J. B. Driscoll, H. Jayatilleka, and H. Rong, "A 128 GB/s PAM4 silicon microring modulator with integrated thermooptic resonance tuning," *J. Lightw. Technol.*, vol. 37, no. 1, pp. 110–115, Jan. 2019.
- [53] D. Marris-Morini *et al.*, "Germanium-based integrated photonics from near- to mid-infrared applications," *Nanophotonics*, vol. 7, no. 11, pp. 1781–1793, 2018.
- [54] D. Benedikovic *et al.*, "Silicon-germanium receivers for short-waveinfrared optoelectronics and communications," *Nanophotonics*, vol. 10, no. 3, pp. 1059–1079, 2021.