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Optical modulation using the silicon platform

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Abstract

Optical modulator devices in silicon have experienced dramatic improvements over the last decade, with data rates demonstrated up to 50Gb/s and ultra-lower power consumption with a few fJ/bit[1]. However a significant need exist for high speed low power devices with a small footprint and broadband characteristics with extinction ratio above 5dB. Here we describe the work within the UK silicon photonics program, which has led to the fabrication and preliminary results of novel nano cavity optical architecture as well as self-aligned pn junction structures embedded in a silicon rib waveguide with an active length in the millimetre range producing high-speed optical phase modulation whilst retaining a high extinction ratio.

Keywords: microphotonics, waveguide, silicon-on-insulator, optical modulator, carrier depletion, integrated optic.

Introduction

With the transition to parallel chip architecture, efficient communication among processing nodes can become a limiting factor to both programming and performance. A photonic communication layer can provide distance independent and low latency interconnection. CMOS compatible silicon-based photonics has generated an increasing interest in the recent years with an aim for monolithic integration of electronic devices with both active and passive optical components. In the race where the required energy per bit and the device footprint are as important as the modulation bandwidth and modulation depth, we report a family of modulator devices addressing the requirements for high-speed interconnects and the future needs for compact low power operation. These devices have evolved from micrometer size waveguides using mostly the plasma dispersion effect in injection mode to sub-

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micrometer size waveguides where Ge and Si-Ge based devices as well as plasma dispersion is in the majority of cases using majority carriers to obtain high-speed and low-power modulation.

High speed Plasma dispersion modulators

In 2005, a sub-micrometer modulator based on the depletion of a pn junction was proposed by Gardes et al. which was the first of its kind at the time of publication [2]. The depletion-type phase shifter is not limited by the minority carrier recombination lifetime as it is based on the principle of removing carriers from the junction when a reverse bias is applied. The main advantage of using depletion to adjust the index of refraction in the waveguide is the fast response time, simulated in this work to be 7 ps. In 2007, Liu et al. [3, 4] experimentally demonstrated a pn carrier depletion-based silicon optical modulator with a structure very similar to that proposed by Gardes et al. [2] in 2005. The research trend of moving towards smaller waveguides to reduce power consumption and device real estate led to structures such as the one recently reported by Gardes et al. [5] in 2009. The principal issues regarding the fabrication of pn junction in a rib waveguide was the inaccuracy of the positioning of the junction due to processing tolerances [5]. This issue was solved by Thomson et al [6, 7] and Gardes et al [8] with a new design of carrier depletion based silicon optical modulator for which a self aligned process was used to form the pn junction. The new process led to the fabrication and demonstration of two devices based on a self aligned pn junction in a rib waveguide.

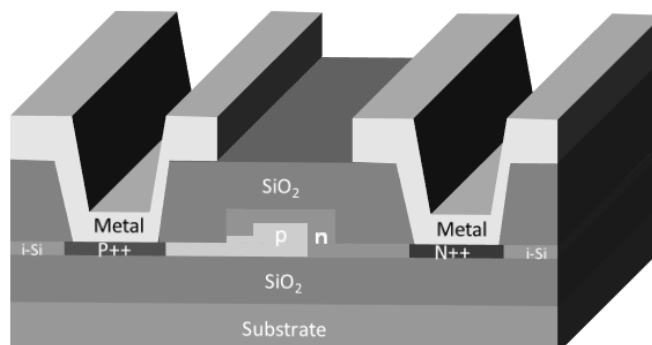


Figure 1 – Cross sectional diagram of self-aligned pn junction phase modulator

A cross-sectional diagram of Gardes et al device is shown in figure 1. The phase modulators are formed by implanting a pn junction in a rib waveguides with dimensions of 400nm in height, 410nm in width and 100nm in slab height. The pn junction is implanted such that the

rib waveguide is surrounded by an n type doping region and the centre of the waveguide is formed by a p region. To ensure resistive contact to the electrodes, highly doped regions are formed below the contacts, positioned sufficiently far away from the waveguide edge such that excessive optical loss is lessened. The phase modulators are incorporated into Mach Zehnder interferometers (MZI) to translate the phase modulation into intensity modulation where compact Y branches splitters structures are used to perform the splitting and combining function in the MZI. Phase modulators are placed into both arms of the MZI to balance the optical power and therefore permit a large static extinction ratio. Coplanar waveguide (CPW) electrodes are used to drive the modulator at high frequency. Shown figure 2, the CPWs were designed to have a characteristic impedance of 50ohms, taking into account the effects of the diode capacitance.

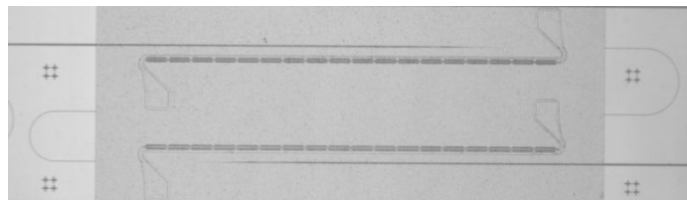


Figure 2 – Top view of the metal coplanar waveguide electrode

Device fabrication was performed in the clean room facilities at CEA-LETI using 400nm overlayer SOI from SOITEC with a 1 μ m thick buried oxide layer. Further to the waveguide etch; five photolithography steps using self aligned features were necessary to complete the active area of the device. The remaining process steps used to form the vias and metal patterning were performed using standard CMOS processes.

The efficiency $V_{\pi} \cdot L_{\pi}$ (voltage-Length required to achieve a π phase shift for a given length) extracted from the transmission shift against reverse voltage for TE and TM polarisations are $\sim 11\text{V}\cdot\text{cm}$ and $\sim 14\text{V}\cdot\text{cm}$. The on-chip insertion loss is $\sim 15\text{dB}$ which includes $\sim 5.7\text{dB}$ and 6.7dB of passive waveguide transmission loss for TE and TM polarisations respectively. A total waveguide propagation loss for TE and TM polarisations of $\sim 1.5\text{dB}$ and 1.9dB respectively was measured for the 410nm wide passive waveguide sections outside of the phase shifter devices themselves where the insertion loss of the phase shifter in isolation was only $\sim 7.7\text{dB}$ and 5.4dB (for TE and TM polarisations respectively) for a length of 1350 micrometer. The loss due to the doping in the waveguides was estimated to be approximately $5.7\text{dB}/\text{mm}$ for TE and $4\text{dB}/\text{mm}$ for TM polarisations, and is responsible for the majority of the phase shifter insertion loss. On the transmission loss figure 3, it is worth noting that the transmission of the

phase shifter is very similar for both TE and TM polarisations, which is clearly an advantage for a polarisation insensitive modulation scheme.

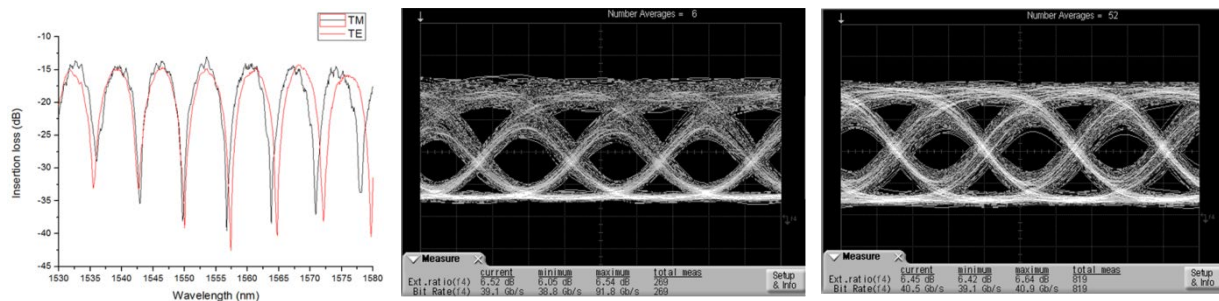


Figure 3 – (Left to right) Top view of the metal coplanar waveguide electrode. Eye diagram for a 1350 micrometers long device measured at 40Gb/s, and at a wavelength of ~1557nm for TE polarisation. The extinction ratio is approximately 6.5dB. (Right) Eye diagram for a 1350 micrometers long device measured at 40Gb/s, and at a wavelength of ~1557nm for TM polarisation. The extinction ratio is approximately 6.5dB.

The data rate measurements were performed using a 40Gb/s PRBS generator (and DEMUX to obtain 10Gb/s), fed into a microwave amplifier providing 6.5 V_{pp} and 6 V_{pp} swings at 40 Gb/s. The phase shifter was reverse biased at -3V using a bias tee and the CPW electrode was terminated by a DC block and a 50ohm load. A collimated polarisation controlled CW beam was used to feed the modulator, and the modulated laser beam coming out of the chip was fed into an EDFA followed by a band pass tuneable filter and finally measured by a Digital Communications Analyser (DCA) for which the optical head has a bandwidth of approximately 65GHz. Prior to each measurement, the DCA optical input was calibrated to the background noise of the EDFA to provide an accurate result of the modulation depth (extinction ratio). The measurements were performed at ~ 1557nm for both polarisations with a data stream of 40Gb/s for TM and TE polarisations as shown in figure 3. The extinction ratios achieved are similar for both TM and TE polarisations, at 6.5dB. The measurements performed here demonstrate the maximum obtainable extinction ratio for both polarisations; this is however, at the expense of the insertion loss which is in the order of 25dB. It is important to note that for this device the extinction ratio at quadrature is similar to the one measured for TE by Intel at 1dB [9]. Hence a trade off can be found between insertion loss and extinction ratio depending on the requirements. With a data rate of 40Gb/s and an input swing voltage is 6V fed into a 50ohm load the power consumption is estimated to be about 4.5pJ/bit.

A simplified implant design using the same self-aligned process was demonstrated by Thomson et al [7] (Figure 4) . Experimental results have demonstrated data transmission for

TE polarisation at 40Gbit/s with 10dB of modulation depth from a 3.5mm long phase shifter (Figure 5) and operation at 50Gb/s was recently demonstrated from a similar device with a length of 1mm.

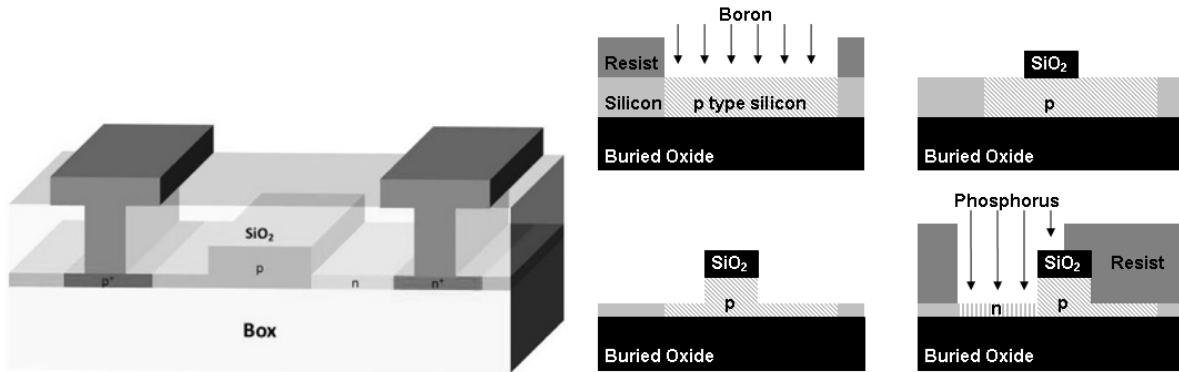


Figure 4. Cross section of the modulator and processing involved for the self-aligned junction[7].

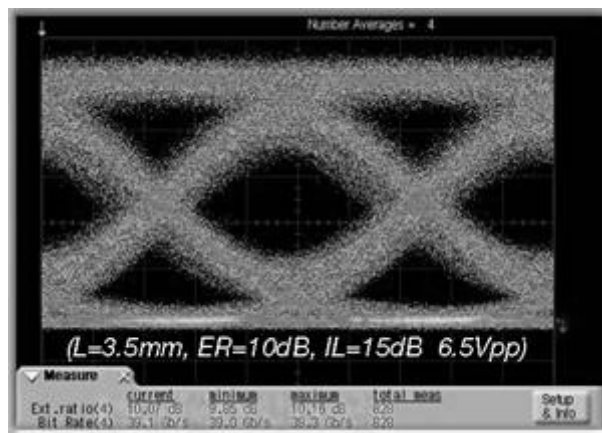


Figure 5. 40 Gb/s eye diagram for TE polarisation[7].

Cavity Modulators

Integration density, channel scalability, low switching energy and low insertion loss are the major prerequisites for on-chip WDM systems. A number of device geometries have already been demonstrated that fulfil these criteria, but combining all of the requirements is still a difficult challenge. Here, we propose and demonstrate a novel architecture consisting of an array of photonic crystal modulators connected by a dielectric bus waveguide. The device architecture features very high scalability and the modulators operate with an AC energy consumption of less than 1 fJ/bit. Furthermore, we demonstrate cascadeability and multichannel operation by using a comb laser as the source that simultaneously drives 5 channels.

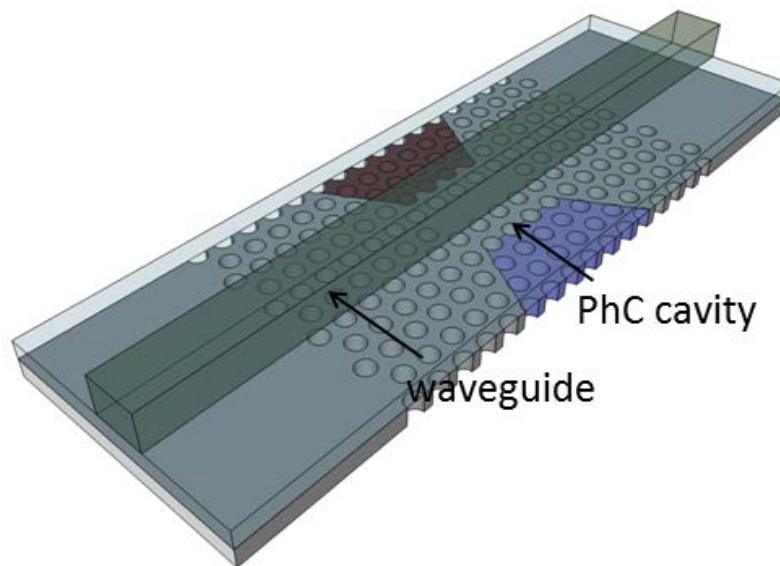


Figure 6. Schematic of the device, where the PhC cavity and the bus waveguide are vertically coupled through a buffer layer.[1]

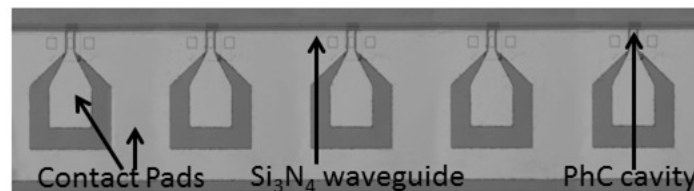


Figure 7. Top view of the cascaded PhC cavity based modulator set, where five cavities are coupled to a single silicon nitride waveguide.[1]

The transmission spectrum of the fabricated device was first characterised with a tuneable laser end-fire coupled into the bus waveguide. The loaded quality factor of the cavities is around 15,000, which corresponds to an unloaded quality factor of 70,000. Since the ultimate limit on the modulation speed is given by the photon life time in the cavity, by design the cavities were limited to $Q \approx 15,000$ by the coupling coefficient; for a Q-factor of 15,000, the photon lifetime is ≈ 12 ps and the modulation limit is 10s of GHz. The extinction ratio depends on the coupling coefficient between the cavity and the waveguide, and was designed to be >10 dB.

In order to test the high speed electro-optic modulation properties of the device, a PRBS unit, generating 127 bit long sequence, was used to drive the PhC cavities electrically and the electrical signal was applied to the devices via a high speed RF probe. An additional DC bias was added via a bias T. The peak-to-peak voltage of the driving signal was 700mV and the DC bias was set to +4V and a modulated optical output at 1Gbit/s, respectively. The extinction ratio was 3.5dB at 1Gbit/s, which corresponds to a resonance wavelength shift of 20 pm and a refractive index change in the silicon device layer of $\Delta n = 4.48 \times 10^{-5}$. This

refractive index change corresponds to a carrier density change of $\Delta N=5 \times 10^{15} \text{ cm}^{-3}$ in the intrinsic region of the modulator. Given the physical volume of the intrinsic region of $2.2 \mu\text{m}^3$, the averaged AC energy consumption for our device is therefore approximately 0.4 fJ/bit, which is amongst the lowest energy consumptions ever reported. We calculate the AC energy consumption as the energy required to switch the device from the OFF to the ON state. This energy excludes the energy consumed by any DC bias which was $38 \mu\text{W}$ (38 fJ/bit for 1 Gbit/s operation) in this case. We note that the DC bias was required because of the high contact resistance (tens of $\text{K}\Omega$) of our current device.

To observe multiplexing, we applied the driving signal successively to each modulator shown figure 7 and recorded the optical output at the resonance wavelength of each individual modulator. Eye diagrams of the five channels were measured each operating at 0.5 Gbit/s. To improve the extinction ratio further, the peak-to-peak voltage of the driving signal was set to 1.7 V. This resulted in an extinction ratio of more than 7dB for each channel.

Conclusion

We have reported the work on optical modulation based on plasma dispersion effect in a rib waveguide showing data rates up to 50Gb/s and ER up to 10dB at 40Gb/s at quadrature. We have also demonstrated a compact cascaded modulator architecture based on PhC nano cavities connected by a dielectric bus waveguide. The key feature of the architecture is the efficient coupling between the low index bus waveguide and the high index silicon PhC cavities. We demonstrated how an array of such cavities can be operated to achieve on-chip WDM operation, one of the first demonstrations of this kind. The AC energy consumption was only 0.4 fJ/bit, one of the lowest yet reported for a silicon electro-optic modulator.

Reference

1. Debnath, K., et al., *Cascaded modulator architecture for WDM applications*. Opt. Express, 2012. **20**(25): p. 27420-27428.
2. Gardes, F.Y., et al., *A sub-micron depletion-type photonic modulator in silicon on insulator*. Optics Express, 2005. **13**(22).
3. Liu, A., *High-speed optical modulation based on carrier depletion in a silicon waveguide*. Opt. Express, 2007. **15**: p. 660-668.
4. Liao, L., et al., *40 Gbit/s silicon optical modulator for highspeed applications*. Electronics Letters, 2007. **43**(22).
5. Gardes, F.Y., et al., *High-speed modulation of a compact silicon ring resonator based on a reverse-biased pn diode*. Opt. Express, 2009. **17**(24): p. 21986-21991.
6. Thomson, D.J., et al., *High speed silicon optical modulator with self aligned fabrication process*. Opt. Express. **18**(18): p. 19064-19069.

7. Thomson, D.J., et al., *High contrast 40Gbit/s optical modulation in silicon*. Opt. Express. **19**(12): p. 11507-11516.
8. Gardes, F.Y., et al., *40 Gb/s silicon photonics modulator for TE and TM polarisations*. Opt. Express. **19**(12): p. 11804-11814.
9. Liao, L., *40 Gbit/s silicon optical modulator for high speed applications*. Electron. Lett., 2007. **43**: p. 1196-1197.