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### Low energy silicon on insulator ion implanted gratings for optical wafer scale testing

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#### ABSTRACT

Silicon photonics shows tremendous potential for the development of the next generation of ultra fast telecommunication, tera-scale computing, and integrated sensing applications.

One of the challenges that must be addressed when integrating a "photonic layer" onto a silicon microelectronic circuit is the development of a wafer scale optical testing technique, similar to that employed today in integrated electronics industrial manufacturing. This represents a critical step for the advancement of silicon photonics to large scale production technology with reduced costs.

In this work we propose the fabrication and testing of ion implanted gratings in sub micrometer SOI waveguides, which could be applied to the implementation of optical wafer scale testing strategies.

An extinction ratio of over 25dB has been demonstrated for ion implanted Bragg gratings fabricated by low energy implants in submicron SOI rib waveguides with lengths up to 1mm. Furthermore, the possibility of employing the proposed implanted gratings for an optical wafer scale testing scheme is discussed in this work.

#### **1. INTRODUCTION**

The field of Silicon Photonics is currently witnessing incredible progress in the development of integrated devices based on silicon on insulator materials [1] system compatible with CMOS technology. Very interesting advancements have been recently reported for many classes of integrated photonic devices, most notably modulators [2], integrated detectors [3], and Raman amplification in silicon [4]. Very remarkable progress has also been achieved regarding the possibility of integrating III-V devices on an SOI material substrate, as demonstrated by the research on hybrid silicon lasers [5]. Furthermore, different research groups are also investigating the possibility of employing SOI and Ge material systems to implement photonic applications at the mid-infrared wavelengths [6] that would benefit a range of applications such as environmental sensing, biomedical sensing, and free space communications.

Despite these advancements, one of the challenges that Silicon Photonics has still to address in order to be promoted to a large scale and economically viable technology is the possibility of developing a large scale optical wafer scale testing infrastructure, in a similar fashion to what happens today in integrated electronics. This is a critical step for an integration technology, as without a practical wafer scale testing plan for photonic devices, the benefits deriving from Si photonics would remain confined to smaller scale applications.

Device testing in integrated photonics has not been extensively studied, and several approaches have been reported within the literature, concerning how to couple light into integrated silicon photonic devices. Some of these approaches involve integrated waveguide device is by end fire coupling, prism coupling [7], inverted tapers [8], and cantilever structures [9]. These methods usually require critical sample modification and preparation, and therefore potentially limit the robustness of these techniques for a larger scale procedure. A very popular approach in light coupling in SOI devices is utilisation of etched grating couplers. Grating couplers have been extensively investigated in the literature and although they have witnessed a constant improvement in their performance [10], they also involve a modification of the tested device/wafer due to the fabrication techniques employed.

In this work we present low energy ion implanted Bragg grating devices which have been fabricated by low dose ion implantation of Ge ions  $(10^{15}ions/cm^2)$  in sub-micrometrical (epitaxial thickness = 400nm) SOI waveguides. The

Silicon Photonics VI, edited by Joel A. Kubby, Graham T. Reed, Proc. of SPIE Vol. 7943, 794310 · © 2011 SPIE · CCC code: 0277-786X/11/\$18 · doi: 10.1117/12.873288 refractive index change which allows grating formation is obtained by silicon amorphization [11]. A refractive index change of approximately 0.5 between the wavelengths 1310nm and 1550nm has been previously reported in [12] for Ge implants with the same characteristics of those employed in this work. These devices have been successfully tested as optical filters and initial results on the possibility of thermally erasing ion implanted gratings are also presented. With further development, this principle of operation might be successfully applied to other classes of resonant or diffractive devices such as couplers in order to develop a minimally invasive device testing scheme.

#### 2. DEVICE FABRICATION

The waveguide structure employed in the fabrication of ion implanted Bragg gratings is shown in figure 1-a. The waveguide dimensions have been chosen in order to achieve single mode operation. The total silicon overlayer thickness H is  $0.4\mu m$ , the target rib etch depth D is  $0.2\mu m$ , the target rib width W is  $0.5\mu m$ , and the buried oxide thickness (BOX) is  $1\mu m$ .

If a refractive index change of period  $\Lambda$  is transferred to the waveguide via ion implantation, some of the wavelengths satisfying a specific phase matching condition [13] will be reflected back while travelling inside the waveguide. The reflected resonant wavelengths are given by  $\lambda_{Bragg} = 2_{neff} \Lambda/m$ , where  $n_{eff}$  is the optical mode effective index, and *m* is

the grating order. In the case of the waveguide dimensions described above, first order Bragg gratings (m=1) have been designed with a 212nm period and a 50% duty cycle, resulting in a theoretical central Bragg wavelength of 1310nm.



Figure 1. Waveguide dimensions used for grating fabrication.

Device fabrication started with a  $SiO_2$  hardmask deposition on the SOI wafers. The  $SiO_2$  hardmask was patterned by deep wavelength UV (DUV) lithography and subsequently etched with reactive ion etching (RIE) in order to define the grating template on the top of the wafer. An SEM image of the grating hardmask patterning is reported in figure 2-a.



Figure 2. SEM top view of the hardmask template used for grating implantation (a), SEM top view of the same sample after ion implantation and waveguide etching (b).

The wafers were subsequently implanted with germanium at a dose of  $10^{15}$ ions/cm<sup>2</sup>. Following ion implantation, the SiO<sub>2</sub> hardmask was stripped and the rib waveguides were defined by another photolithography step followed by a second etching step.

A top view of the rib waveguide after ion implantation and hardmask strip is shown in figure 2-b. SEM analysis of the fabricated waveguides showed that the waveguide target dimensions have been achieved within a  $\pm 20$ nm difference, and a small variation in the waveguide surface colour is recognizable in correspondence of the implanted areas.

Implanted Bragg gratings with a period of 212nm, have been fabricated on Si rib waveguides, with lengths of 100µm, 200µm, 400µm, 600µm and 1mm. The grating target resonant wavelength was 1310nm. The use of DUV lithography allowed producing a large number of devices with relatively large lengths, preventing the appearance of "stitches" across the device length, as opposed to electron beam lithography patterning previously presented [12].

Ion implantation has been simulated by using KING3D software [14] in order to relate different ion energies and implantation conditions to the grating depth. The chosen implantation energy for the devices results presented is 30keV, and is expected to produce a grating depth of 50nm. As an example a simulated damage profile is reported in figure 2.

The use of a 50% duty cycle hardmask with period  $\Lambda = 212$ nm leads to a predicted amorphous material distribution with width of 132nm, which leads to an increase of the effective duty cycle of 62%.



Figure 2: Simulated ion damage distribution for a single grating period.

#### **3. DEVICE TESTING**

Ion implanted gratings have been tested in transmission by using a Denselight DLCS3207A, unpolarized broadband source operating at 1310nm, coupled into the device by a lens tapered fiber. The device output has been collected also by a lens tapered fiber, and analyzed with an Hewlett Packard HP86140A optical spectrum analyzer. Figure 3-a shows the measured reflection spectra for gratings of different lengths.



Figure 3: Extinction ratio in transmission measured for Ge ion implanted Bragg gratings of different lengths. Ion dose =  $10^{15}$ ions/cm<sup>2</sup>, energy = 30keV.

Implanted Bragg gratings tested in transmission exhibited an average extinction ratio of 2.7dB for the 100 $\mu$ m devices, 7.4dB for the 200 $\mu$ m devices, 16.3dB for the 400 $\mu$ m devices, and 21dB and 24dB for the 600 $\mu$ m and 1000 $\mu$ m devices respectively, showing repeatability within ±2dB across 15 devices fabricated with the same design

Optical losses have been measured by the Fabry-Perot resonance technique using a 27% reflectivity value, which has been obtained by simulating the analyzed structure by Eigenmode Expansion Method [15]. Figure 4 shows the average optical loss measured for the implanted grating devices.



Figure 4. Average ion implanted Bragg grating optical loss measured with the Fabry-Perot resonance method.

Grating optical losses for "as implanted" devices have been measured in the range of  $4.2\pm1.2$ dB/cm. This measured loss is comparable to the unimplanted waveguide loss, measured to be  $3.1\pm1.2$ dB/cm. This data may lead to the assumption that the optical loss contribution introduced by the ion implantation process and by the grating itself is small if compared to propagation loss inside the unimplanted waveguide structure. For the same reason, as the loss contribution appears to moderately affect light propagation, the uncertainty on the measurements appears to be comparable with the loss itself. The measured grating bandwidth allows estimation of the grating efficiency ( $\kappa$ ) by using the coupled mode theory [13]. The analyzed devices produced an average coupling constant of  $62\pm10$ cm<sup>-1</sup>, demonstrating a grating efficiency comparable to that of etched gratings in silicon on insulator reported in literature [16]-[17].

#### 4. OPTICAL WAFER SCALE TESTING CONCEPT

The fabrication of periodic optical structures into silicon by ion implantation may be used as a starting point to implement a wafer scale testing strategy in future silicon photonics applications.

Figure 5 shows a hypothetical implementation of the wafer scale testing technique in order to test an integrated photonic device.



Figure 5. Wafer scale testing concept based on ion implanted gratings.

When processing a wafer containing integrated optical devices, an extra step is included in the manufacturing process in order to add input and output implanted gratings near any of the fabricated devices that require testing.

Once implanted couplers have been patterned on the wafer, a test signal can be routed into the wafer by using single mode optical fibres. Depending on how the gratings are arranged on the wafer, light can either be collected by a single exit point (also an implanted grating) or by multiple exit points by using similar fibres.

#### **5. CONCLUSION**

In this paper we demonstrated the possibility of fabricating ion implanted Bragg gratings with potentially sub millimetre length on sub-micrometrical waveguides.

An extinction ratio up to 26dB has been demonstrated for devices length up to 1mm. Preliminary loss analysis indicated that the loss contribution from ion implantation is on the order of 2dB/cm, opening the way to low loss applications.

The device performance resulted to be comparable, if not higher, than SOI Bragg gratings presented in literature. The device design presented in this paper also represents a step forward if compared to the work previously reported by the same authors [12], as device size and implantation energy have been dramatically reduced, while improving the grating performance in terms of extinction ratio.

With further development, the fabrication of periodic optical structures by ion implantation into silicon may be used as a starting point to implement a wafer scale testing strategy in future silicon photonics applications.

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