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Effects of annealing silicon ion irradiated rib waveguides with respect to free carrier lifetime

Nicholas. M. Wright*, Andrew J. Smith, Konstantin Litvinenko, Russell Gwilliam, Goran Mashanovich, Graham. T. Reed
Advanced Technology Institute, University of Surrey, Guildford, GU2 7XH, UK;

ABSTRACT

Previously we have reported the effects of silicon ion irradiation on free carrier lifetime and propagation loss in silicon rib waveguides, and simulated net Raman gain based on experimental results. We further extend this work by reporting the effects of thermally treating a silicon irradiated sample with a higher dose and energy than previously reported, which produced a poor trade-off between free carrier lifetime and excess optical absorption prior to thermal treatment. Excess losses greater than 80dB/cm were recorded prior to annealing. After thermal treatment, the sample demonstrated characteristics of excess loss and free carrier lifetime recorded previously in much lower energy and dose silicon ion irradiated samples, suggesting that thermally treating samples could enhance the trade-off between free carrier lifetime and excess loss introduced to the rib waveguides. Raman gain simulations based on the new experimental data are reported and show an increase in net gain over previously reported data, suggesting that higher dose, shallow silicon ion implantation is the most efficient way of optimising the trade-off between lifetime reduction and excess optical absorption in silicon rib waveguides, a proposal in our earlier work. The effects of thermally treating low temperature oxide clad waveguides with respect to free carrier lifetime are also reported. Results show that thermally treating a low temperature oxide clad waveguide can vary the intrinsic lifetime. The results of this investigation as well as a discussion into the possible origin of the lifetime change are given.

Keywords: Waveguides, Integrated optoelectronic circuits, Optical amplifiers

1. INTRODUCTION

It has already been shown that irradiating a silicon waveguide can reduce the free carrier lifetime [1-3]. However there is a significant increase in propagation loss when this method is utilized. It has been suggested recently that shallow high dose irradiation may provide the best trade-off between lifetime reduction and excess loss introduced into the waveguide [3, 4].

Annealing self-ion irradiated silicon waveguides has already been investigated [5, 6]. It was shown that the excess optical absorption loss associated with the implanted damage, annealed out completely by 300 °C. It was postulated that the defect responsible for this was the silicon di-vacancy.

In this paper we investigate reduction of excess loss in rib waveguides implanted with medium dose high energy Si^+ ions.

The following section gives a detailed account of the effects of increasing the anneal temperature on the free carrier lifetime and excess loss in the silicon implanted rib waveguides. During this investigation it was found that the un-implanted waveguide lifetime varied with anneal temperature. A theory and possible explanation as to why this occurred has been given in this paper.

In section 4 Raman modelling is presented, using some of the experimental parameter values measured in section 3. As annealing temperature was increased the trade-off between excess loss and free carrier lifetime changed, allowing, in some cases, a sweet-spot to emerge resulting in high modelled net gain.

*Nicholas.wright@surrey.ac.uk; phone +44 (0) 1483682740

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2. EXPERIMENTAL METHOD

This study investigates the annealing of test chips pre-implanted with a dose of $1x10^{13}cm^{-2}$ silicon ions with an implantation energy of 750 keV (we have previously reported the effect of implanting at different ion doses and energies [3]). This was the highest dose and energy which could be measured optically due to excess loss from implantation exceeding 80dB/cm. The silicon rib waveguides were fabricated on a (100) silicon-on-insulator wafer. The ribs were nominally 1 µm wide and 1.35 µm high. The waveguides had a length of 8000 µm. The ribs had a 0.3 µm thermally grown oxide over-layer initially used as a hard mask. In addition to this the whole chip was covered in a 0.3 µm low temperature oxide used as a protective layer. The chip was annealed using a 10 minute isochronal annealing scheme from room temperature up to 950 °C. The format of this study was intended to be similar to the one performed in [5] to allow comparison between excess loss annealing characteristics.

2.1 Excess optical absorption measurements

The pre-implanted test chips had a maximum of 8 straight waveguides per chip. Each of these waveguides had an implanted region which varied along the test chip from un-implanted to fully implanted in roughly 2000µm steps. A diagram representing this can be seen in figure 1.

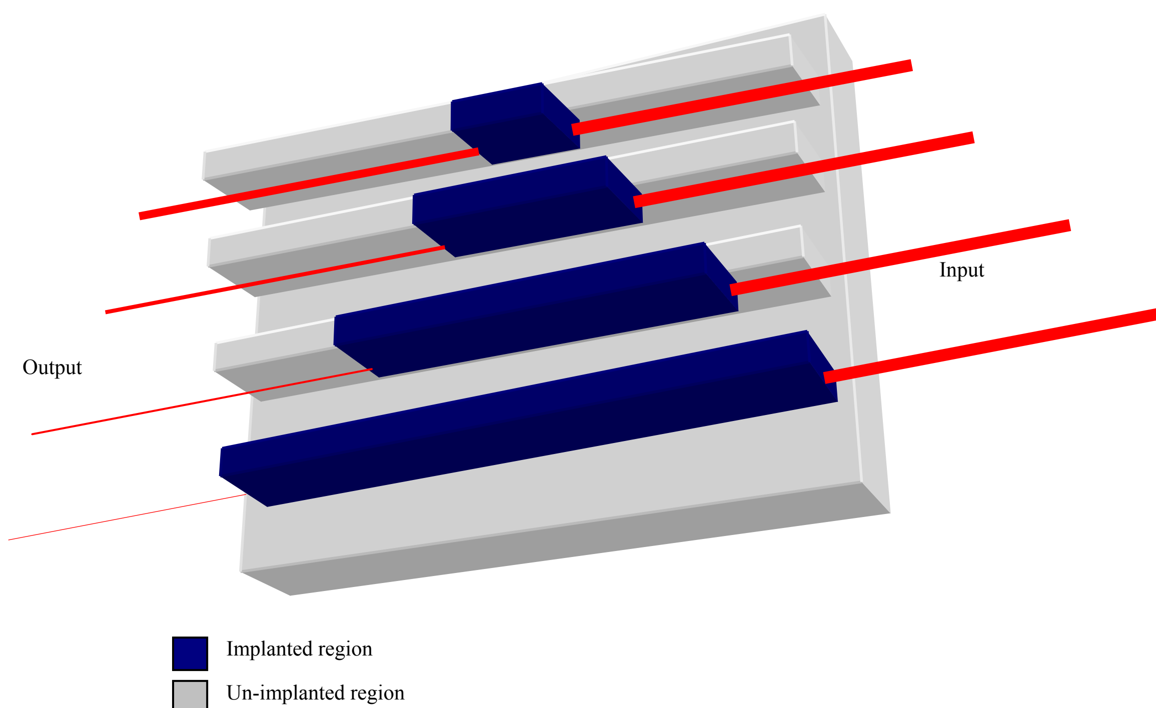

Figure 1. Diagram of optical loss measurement showing output beam reducing in intensity as the implanted region increases in length.

The varying lengths of the implanted region on each test chip allowed excess loss to be calculated in a similar fashion to that of the cut-back method, whilst not destroying the test chip, allowing repeat measurements to be performed.

A broadband source (1530nm-1610nm) was systematically coupled to each waveguide in turn, and the output power for each waveguide was measured. The broadband source was chosen as it had a broad spectral range. This was required because the test chips used in this investigation did not have anti-reflection coatings, which would cause Fabry-perot reflections to be generated if a laser source was used, affecting the output power measured.

In general as the broadband source was coupled to each waveguide, the output power would reduce as the implanted region increased. This is displayed diagrammatically in figure 1. In order to calculate the excess propagation loss for each test chip, the insertion loss had to be calculated for each waveguide and plotted against its corresponding implanted

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length. The gradient of this plot gives the excess propagation loss for the chosen implant parameters used for that test chip, in this case $1x10^{13}cm^{-2}$ dose with an implantation energy of 750 keV.

This measurement technique was performed after each isochronal anneal in the temperature range being studied. This was why a non destructive method of measuring excess loss was required. Other techniques such as cut-back or Fabry Perot technique are either destructive or loose accuracy as loss in the waveguide increases. Since optical losses greater than 80dB/cm were present in this study, implant windows were seen as the obvious choice to measure excess loss.

2.2 Free carrier lifetime measurement technique

Ion implantation windows were also utilized to measure the free carrier lifetime. This allowed almost simultaneous measurement of implanted and un-implanted regions of the same waveguide. This method of lifetime measurement is viable when comparing to the co-linear approach for example, since in that approach implanted and un-implanted waveguides have to be measured separately; this can cause a discrepancy when comparing lifetimes as both waveguides may not have the same intrinsic lifetime.

A top down technique was utilized, where an 800nm femto-second pulsed laser beam was directed onto the surface of the waveguide, generating free carriers via one photon absorption. Figure 2 displays a diagram showing the top down approach to lifetime measurement.

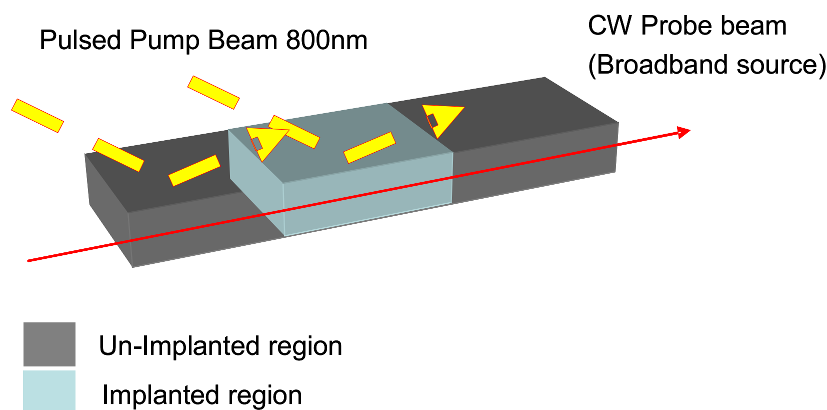

Figure 2. Diagram showing how top down approach allows almost simultaneous measurement of implanted and un-implanted carrier lifetime utilizing only one waveguide.

In this case the penetration depth of the 800nm laser beam has been calculated to be ~16.5µm which relates well with a published penetration depth of 10µm [7]. This top-down technique has also been used by Waldow et al [2], to investigate switching speeds in silicon micro-ring resonators.

The advantage with the top down method of lifetime measurement is the near simultaneous measurement of un-implanted and implanted lifetime, limiting the effects of waveguide variation and allowing a true change between the two regions to be calculated.

3. EXPERIMENTAL RESULTS

The aim of this work is to successfully modify the free carrier lifetime of silicon rib waveguides. As such it was decided to represent the data in a way that truly shows the effectiveness of this work as a lifetime reduction technique. Therefore the data in figure 3 has been shown as a percentage reduction in lifetime, which is the change in lifetime between the implanted and un-implanted lifetimes on the test chip.

Figure 3 shows the effect of annealing temperature on excess optical absorption and percentage reduction in free carrier lifetime. It is clear that excess loss is greatly affected by increasing temperature, whereas the percentage reduction in lifetime remains almost unchanged up to T = 400 °C. By 400 °C excess optical absorption has reduced from ~83dB/cm to an amount deemed negligible after repeat measurements. Free carrier lifetime reduced from 98% to an 88% for the

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same temperature range, corresponding to a free carrier lifetime of 0.8ns still well below the average un-implanted lifetime of 4ns.

There is evidence that at low silicon doses (>$1x10^{13}cm^{-2}$) point defects and vacancy clusters containing 4 centres can anneal out by 200 °C, and are replaced by 5 vacancy centres which finally anneal out between 550 °C and 600 °C [8]. The position of these clusters and higher stability may give an idea as to why there is negligible loss associated with a low free carrier lifetime. Beyond 600 °C other defects incorporating oxygen and carbon from the oxide for example and possible modification to the surface due to irradiation may explain the low lifetime until ~700 °C.

From [3] a carrier lifetime reduction of 79.5% for an excess loss of 0.25dB/cm was found to result in the highest simulated Raman gain, utilizing an input power of 1W. This was carried out for a silicon implanted dose of $5x10^{11}cm^{-2}$ with implantation energy of 400 keV. Figure 3 shows a higher lifetime reduction at T=400 °C, with negligible excess loss.

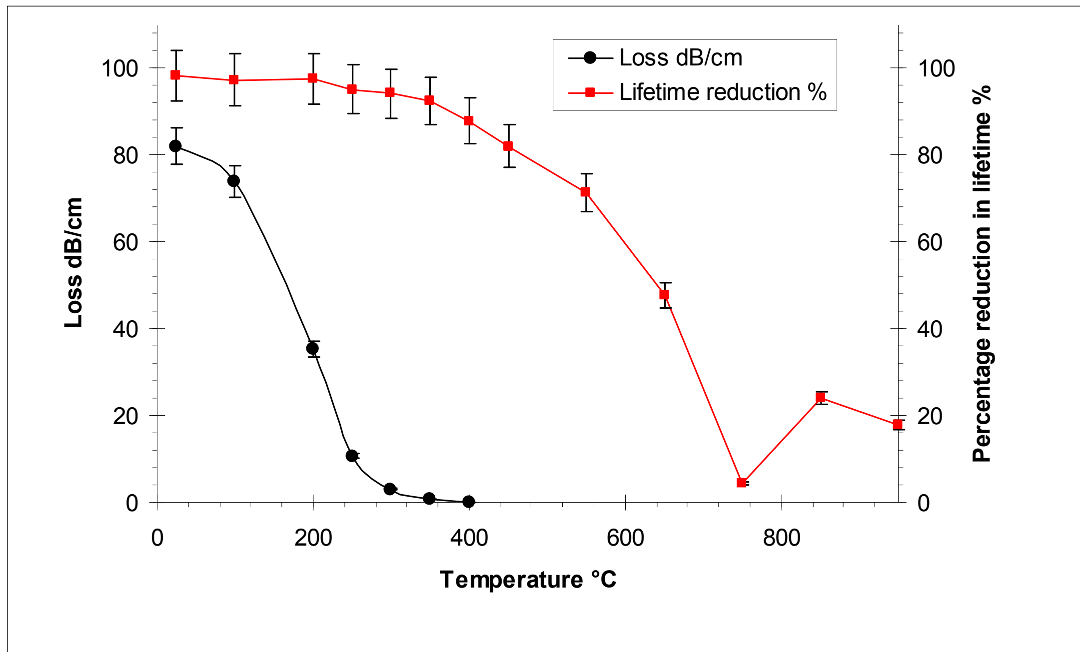

Figure 3. Graph showing the effects of annealing on excess loss and percentage reduction in free carrier lifetime for an oxide clad rib waveguide. Note that after 750 °C the graph becomes inaccurate due to the oxide affecting the carrier lifetime.

The loss curve in figure 3 corresponds well with data from Foster et al [5] which showed that after 300 °C excess loss had been completely annealed from the waveguides. Foster et al suggested that the defect responsible for the excess loss was the silicon di-vacancy.

From figure 3 it can be seen that thermal tuning of a sample, initially with high excess loss, can enhance the trade-off between excess loss and reduction in lifetime, to potentially allow for a higher performance device. In this case the lifetime reduction (~88%) coupled with negligible excess loss at T = 400 °C has provided a more efficient trade-off than seen previously [3], where no thermal tuning was carried out.

The percentage reduction in lifetime curve in figure 3 at T = 750 °C "jumps" before reaching its final value. This "jump" was found to be due to the un-implanted lifetime varying with annealing temperature. Since the percentage reduction in lifetime curve is a comparison between un-implanted and implanted lifetimes, variation in the un-implanted lifetime will affect the curve.

When the carrier lifetime of the un-implanted waveguides on this test chip were investigated, it was found that they varied with anneal temperature. Since the implanted waveguide did not vary in this way, it was thought that the varying

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lifetime was due to a surface effect. Figure 4 displays this variation in lifetime. Sample 1 (un-implanted) and sample 1 (implanted) are results taken from the annealing study seen in figure 3. Samples 2 and 3 were used to confirm repeatability of this variation in lifetime with annealing temperature.

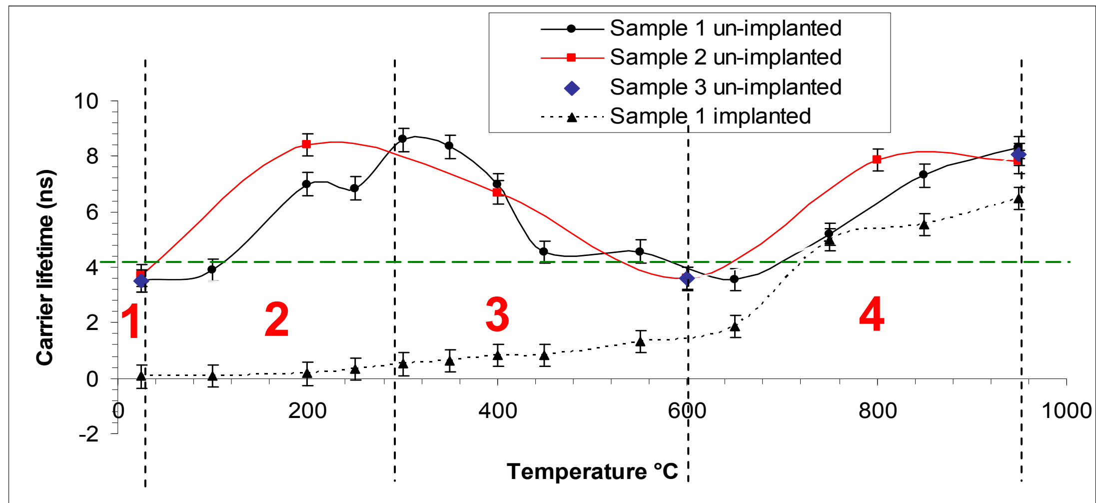

Figure 4. Effect of annealing temperature on carrier lifetime. Sample 1 is used in this annealing study; samples 2 and 3 are used to confirm repeatability of trends seen in sample 1. The dotted horizontal line running through the graph represents the average un-implanted lifetime prior to annealing, 4 ±0.5ns.

A possible explanation for the variation in un-implanted lifetime was devised after consultation with colleagues from the National Ion Beam Centre at Surrey. Referring to figure 4, four distinct regions can be identified. These are defined in figure 4 by dashed vertical lines. The numbers ranging from 1-4 identify the four distinct regions. A description of the effects occurring in each region will now be given. It should be noted that the waveguides used in this study had a deposited oxide produced via a low temperature PE-CVD technique.

In region 1 low temperature oxide was deposited onto the sample via PE-CVD. This technique for oxide deposition can incorporate a large quantity of hydrogen from the reaction [9]. The plasma deposition causes light damage to the interface of the silicon (e.g. sputtering) [10], which has the effect of lowering the free carrier lifetime, as carriers diffuse to disordered material readily (higher concentration of dangling bonds).

In region 2 the lifetime is seen to increase in the un-implanted samples. This is due to light damage caused during oxide deposition being repaired at low temperatures up to ~300 °C. This is not seen in the implanted sample as the lower implanted lifetime is dominant, suggesting a surface effect causing the variation in un-implanted waveguides. During interface repair, the lifetime increased to an ~8ns lifetime in figure 4, due to the oxide passivating the surface of the waveguide [11].

In region 3 there is a decrease in lifetime most likely caused by hydrogen diffusion to the silicon interface which was incorporated during the oxide deposition stage. Hydrogen would act as trapping centres near the surface of the waveguide, reducing the free carrier lifetime. In figure 4, a value of ~4ns has been recorded at 600 °C.

In region 4 the lifetime in the un-implanted and implanted waveguides increases. This is expected in the implanted sample since damage repair is expected, however the implanted and un-implanted lifetimes exceed the average un-implanted lifetime by T = 950 °C.

At 600 °C hydrogen would begin to diffuse out of the deposited oxide. This would result in an increase in lifetime, due to the concentration of trapping sites decreasing. At this temperature silicon starts to re-crystallize, repairing damage caused by RIE etching [10, 11]. Hydrogen diffusion out of the oxide appears to reduce trapping concentration and increases oxide quality. Silicon re-crystallization from RIE etching at this temperature also contributes to an increase in lifetime to a value of ~8ns in figure 4.

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In order to verify that the variation in lifetime was a surface effect, facilitated by the low temperature oxide, the oxide was removed from an un-implanted sample using Hydrogen Fluoride (HF) after a 200 °C anneal. The intrinsic lifetime prior to annealing was ~4.5ns which rose sharply to ~7ns after annealing at 200 °C. This trend followed that seen in figure 4 for an un-implanted sample. The sample was re-measured without an oxide and then annealed from 400 °C to 950 °C in ~200 °C steps. The results can be seen in figure 5. This figure displays free carrier lifetime for varying anneal temperatures. After 200 °C the oxide is stripped off the sample.

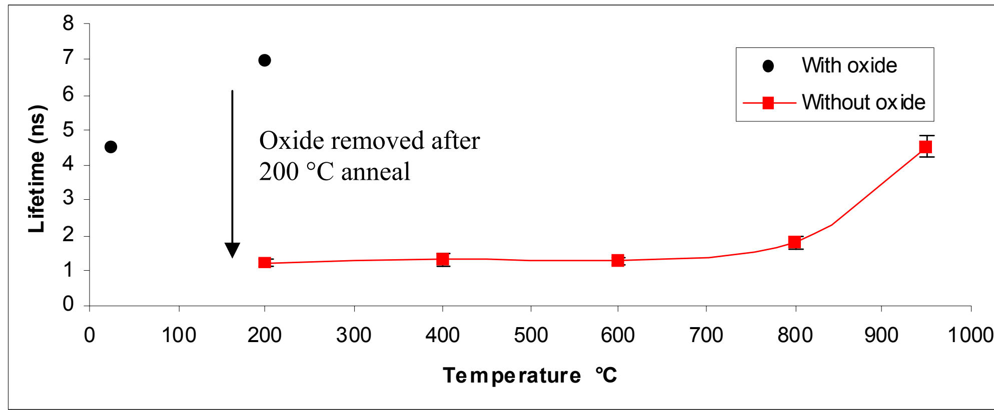

Figure 5. Effects of removing oxide layer from a silicon rib waveguide. Note that the lifetime decreases with the removal of the oxide.

With the oxide removed the carrier lifetime dropped to a value of ~1.2ns. Without the oxide the silicon interface now has increased recombination centres due to an un-passivated surface, hence greater concentration of dangling bonds.

Subsequent anneals show little change in the carrier lifetime with the oxide removed until ~800 °C when the lifetime starts to rise to a value comparable to an un-implanted lifetime prior to annealing and oxide removal.

An explanation for this increase in lifetime is most likely due to silicon re-crystallisation from RIE etching and possible irradiation damage and oxide growth. Using ellipsometry the native oxide thickness of an annealed sample was measured and compared to an un-annealed sample. The result was more than doubling of the native oxide in the annealed sample. The oxide increased from ~15nm to ~32nm after annealing. As mentioned previously re-crystallisation starts to occur at ~600 °C and would repair damage caused by reactive ion etching. Thermal oxidation usually occurs between ~800 °C and 1200 °C [12], and would increase the native oxide thickness, to produce a thin thermal oxide, passivating the surface further.

4. RAMAN SIMULATIONS

Assuming low loss waveguides and no thermal loading, knowing the excess loss and free carrier lifetime values for various thermal anneals, the net Raman gain can be calculated using the approach of Liu et al. [13]. Several excess loss and free carrier lifetime reduction regimes have been taken from figure 1 and simulated with respect to Raman gain. For comparative purposes the same parameters as in [3] have been chosen to compare the best result from as-implanted to thermally tuned devices. The following values were used in the modelling, taken from Liu et al for a waveguide of comparable dimensions used in this study [13]:- $\alpha = 0.2$dB/cm, $\beta = 0.5$cm/GW, $\sigma = 1.45\text{x}10^{-17}\text{cm}^{-2}$, $\sigma_s = 1.71\text{x}10^{-17}\text{cm}^{-2}$, $A_{eff} = 1.5\mu\text{m}^2$, $\lambda_{pump} = 1550$nm, $\lambda_{stokes} = 1684$nm, $g_r = 9.5$cm/GW. That group reported that a value of $g_r = 9.5$cm/GW gave good agreement between theoretical and experimental results. They also noted that there are differing values for the TPA coefficient, which may require further investigation.

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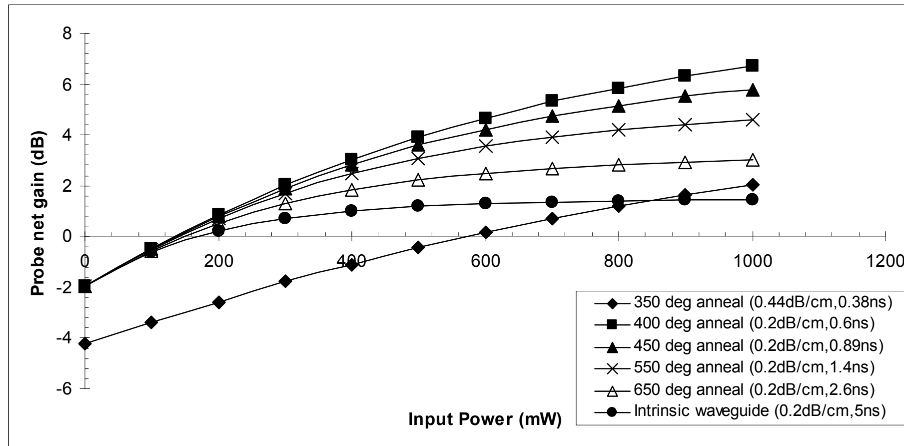

Figure 6. Modelled optical net continuous wave Raman gain as a function of input pump power in a 9.6cm long silicon rib waveguide for varying anneal temperatures. Highest net gain was for a 400 °C anneal, corresponding to 6.7dB net gain.

The same length devices as in [3] were modelled and in each case the thermally tuned device produced higher simulated net gain, due to the higher percentage reduction in lifetime coupled with negligible excess loss for certain annealing temperatures. It was found that the highest simulated net gain (400 °C anneal corresponding to 6.7dB net gain) was produced in the longest device (9.6cm) simulated, figure 6 displays this graph. However it was thought that the extra gain achieved for this length device was offset by the extra length. A waveguide length of 4.8cm, half the length, achieved a simulated net gain of ~5.2dB, again for a 400 °C anneal, which corresponded to a lifetime reduction of 88% with negligible excess loss, figure 7 shows the net gain achieved for this length device.

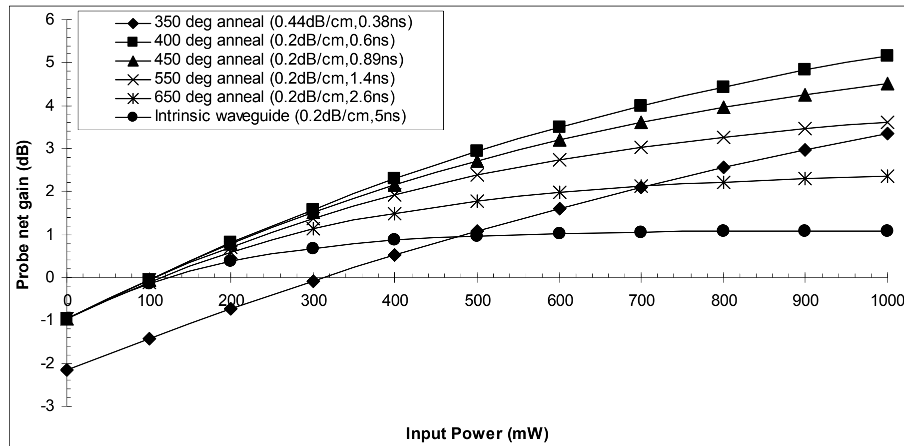

Figure 7. Modelled optical net continuous wave Raman gain as a function of input pump power in a 4.8cm long silicon rib waveguide for varying anneal temperatures. Highest net gain was for a 400 °C anneal, corresponding to 5.2dB net gain.

5. SUMMARY

This work has shown that it is possible to thermally tune and optimise a silicon implanted rib waveguide. The trade-off between low carrier lifetime and low excess loss has been optimised through thermal annealing. Previous results have shown a simulated net Raman gain of ~2.2dB for a dose of $5x10^{11}cm^{-2}$ silicon ions, implanted at 400 keV into a 4.8cm long rib waveguide with the same dimensions as seen here [3]. A $1x10^{13}cm^{-2}$ dose of implanted silicon ions at 750 keV after a 400 °C produced a net Raman gain of ~5.2dB for the same simulated length device. The increase of the net Raman gain compared to the previous case is due to a higher reduction in lifetime which reduced the effects of FCA, coupled with negligible excess loss, reducing the overall loss that the device had to overcome to achieve net gain.

This investigation also highlighted the effects of annealing an oxide clad rib waveguide. The variation in lifetime with annealing temperature needs to be investigated further, however preliminary results on three separate test chips show that

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thermal annealing alters the intrinsic carrier lifetime of rib waveguides if covered by a low temperature deposited oxide layer.

6. ACNOWLEDGEMENTS

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